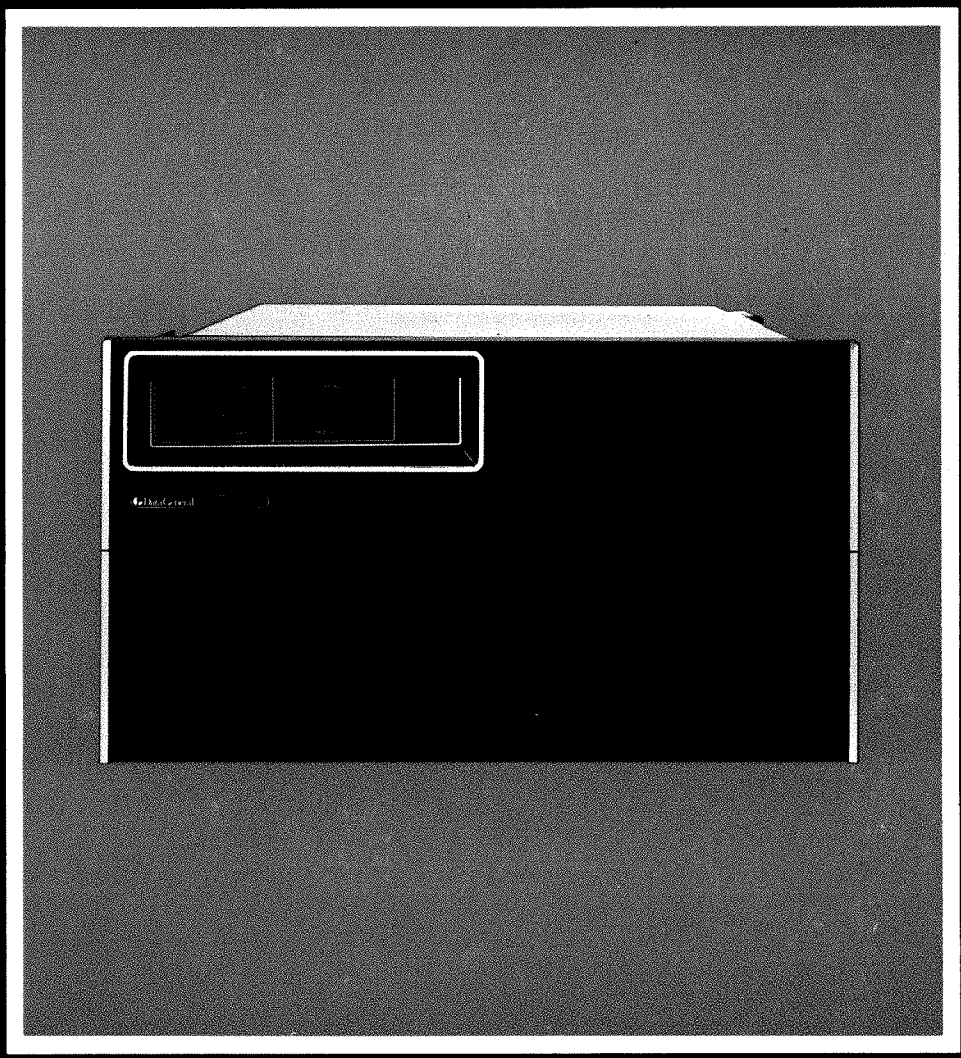
Maintenance Service Guide

NOVA®/ECLIPSE®
Disk Subsystem

Models 6234/6280



DataGeneral

MAINTENANCE

SERVICE GUIDE

FOR

MODELS 6234/6280

DISK SUBSYSTEM

Prepared by

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SECTION 1

INTRODUCTION

Data General Model 6234 is a Disk Subsystem (see Figure 1-1) compatible with the NOVA and ECLIPSE computer systems. The Model 6280 is a Disk Subsystem compatible with micro ECLIPSE computer systems. Both disk subsystems are similar except for the controller. The 6234 uses a data channel controller (DCH) and the 6280 uses an ECLIPSE S20 microBMC. The microBMC is similiar to the ECLIPSE line BMC and provides a high speed data channel for the S20. The disk subsystems consist of: a CPU controller and a sealed data module containing the head and disk assembly. The CPU controller contains all logic necessary to transfer data between the disk drive and the CPU. The drive capacity is 50,724,864 bytes utilizing three platters. Each platter surface provides two data recording surfaces. Each data surface uses two heads, contains 192 tracks per head, and 43 sectors per track.

The 6234/6280 Disk Subsystem features:

- A single PCB controller
- Ability of the controller to store a position, or data transfer command for later execution
- 50.7 Mbyte, drive capacity
- Winchester technology
- Rack mountable
- Twelve moving heads for 3 platters, 2 heads per platter surface

1.1 DESCRIPTION OF MODELS

The 6234/6280 subsystems provide 50,724,864 bytes of storage for NOVA/ECLIPSE and ECLIPSE S20 computers. The 6234 uses a DCH controller and the 6280 uses a microBMC controller. The 6234/6280 disk series rigid drive has three platters consisting of six surfaces. All six surfaces are used for recording data.

1.2 SUBSYSTEM MODEL NUMBERS

Table 1-1 describes the power requirements and respective suffixes for the 6234/6280 disk subsystems.

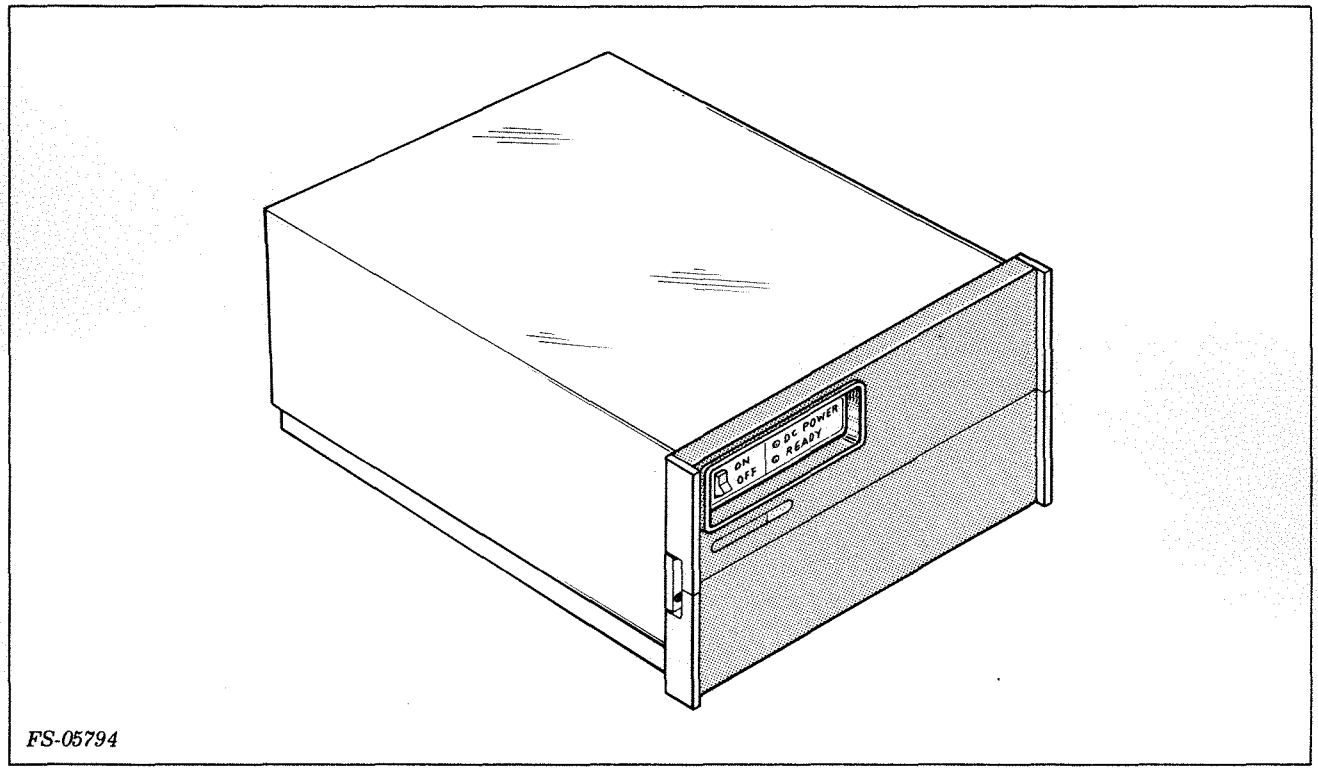

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Figure 1-1. 6234/6280 Disk Subsystem

Table 1-1. Model 6234 Suffix Number Power Requirements

MODEL NUMBER SUFFIX FIELD	POWER DESIGNATIONS
6234-none	120 Vac, 60 Hz
6234-1	100 Vac, 50 Hz
6234-2	220 Vac, 50 Hz
6234-4	240 Vac, 50 Hz
6280-none	120 Vac, 60 Hz
6280-1	100 Vac, 50 Hz
6280-2	220 Vac, 50 Hz
6280-4	240 Vac, 50 Hz

1.3 PERFORMANCE DATA

Table 1-2 lists the subsystems performance data.

Table 1-2. Model 6234/6280 Performance Data

ITEM	DESCRIPTION
Drive capacity (formatted)	16.91 Mbytes/platter 50,724,864 bytes total
Heads	12 (2 per surface)
Spindle speed (RPM)	2385 +/- 2%
Track density	65t/cm 166t/in
Bit density	7678 bpi
Sectors	43/track 568 bytes unformatted 512 bytes formatted
Tracks	192/head 384/surface
Actuator	Open loop; stepper motor driven rotary actuator
Average Access: 1 track 1/3 stroke full stroke recalibrate	 15 millisec 60 millisec 120 millisec 150 - 540 millisec
Rotational latency	12.5 millisec average
Data rate	7.768 Mbyte/sec 971 Kbyte/sec
Data transfer rate	1/4 of data rate, Model 6234, 244 Kbyte/sec Same as data rate, Model 6280 971 Kbyte/sec
Mapping factor - consecutive sector transfers	Model 6234 4 to 1 (every fourth sector transferred) Model 6280 1 to 1 (contiguous sector transfers)
Read Error Rate	10^{9} bits soft; 10^{12} bits hard

1.4 MODEL 6234 CONTROLLER PCB

The controller as shown in Figure 1-2, is a single 38.2 x 38.2 cm (15 x 15 in) square PCB that contains all the logic required to transfer data between main memory and the disk via the DCH interface. The controller PCB also contains jumpers for selecting the device code, and a microprocessor chip to act as a supervisor for all control functions.

An internal I/O cable connects a 50-pin paddleboard to the appropriate back panel pins. An external cable connects the paddleboard to the rigid drive (see Figure 1-3).

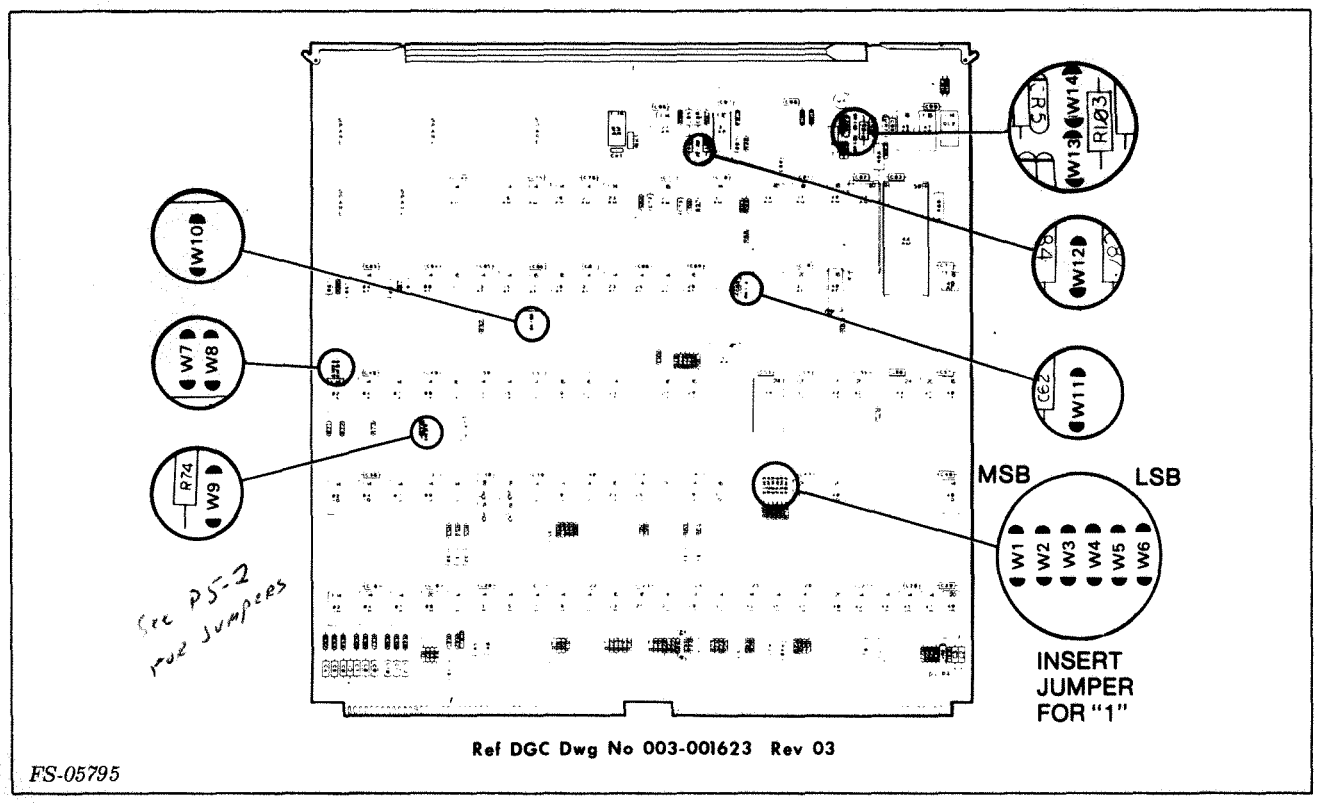

Figure 1-2. 6234 Controller PCB

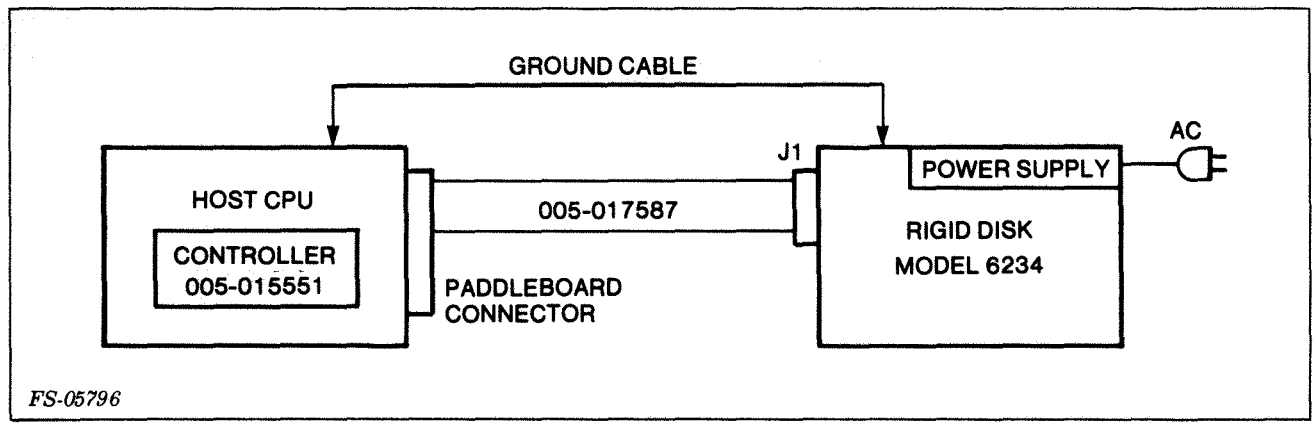

Figure 1-3. 6234 Interconnection Diagram

1.5 MODEL 6280 CONTROLLER PCB

The controller as shown in Figure 1-4, is a single 19 x 24 cm (7.5 x 9.5 in) square PCB that contains all the logic required to transfer data between main memory and the disk via the microBMC interface. The controller PCB also contains dip switches for selecting the device code and bus priority. The controller may be set to any one of eight possible bus priorities by means of eleven dip switches. A microprocessor chip is also located on the controller to act as a supervisor for all controller functions.

For a hardened ECLIPSE S20 the controller connects to the disk drive via a 50-pin 'A' connector. There is a CPU internal cable that transitions the 50-pin card edge connector to a 50-pin 'D' connector mounted at the rear of the computer chassis. This accepts the external shielded disk I/O cable connector (see Figure 1-5).

For an unhardened ECLIPSE S20, there is a 50-pin external I/O cable which connects the 50-pin PCB 'A' edge connector and the bulk-head connector at the disk subsystem.

Ref DGC Dwg No 003-001911 Rev 02

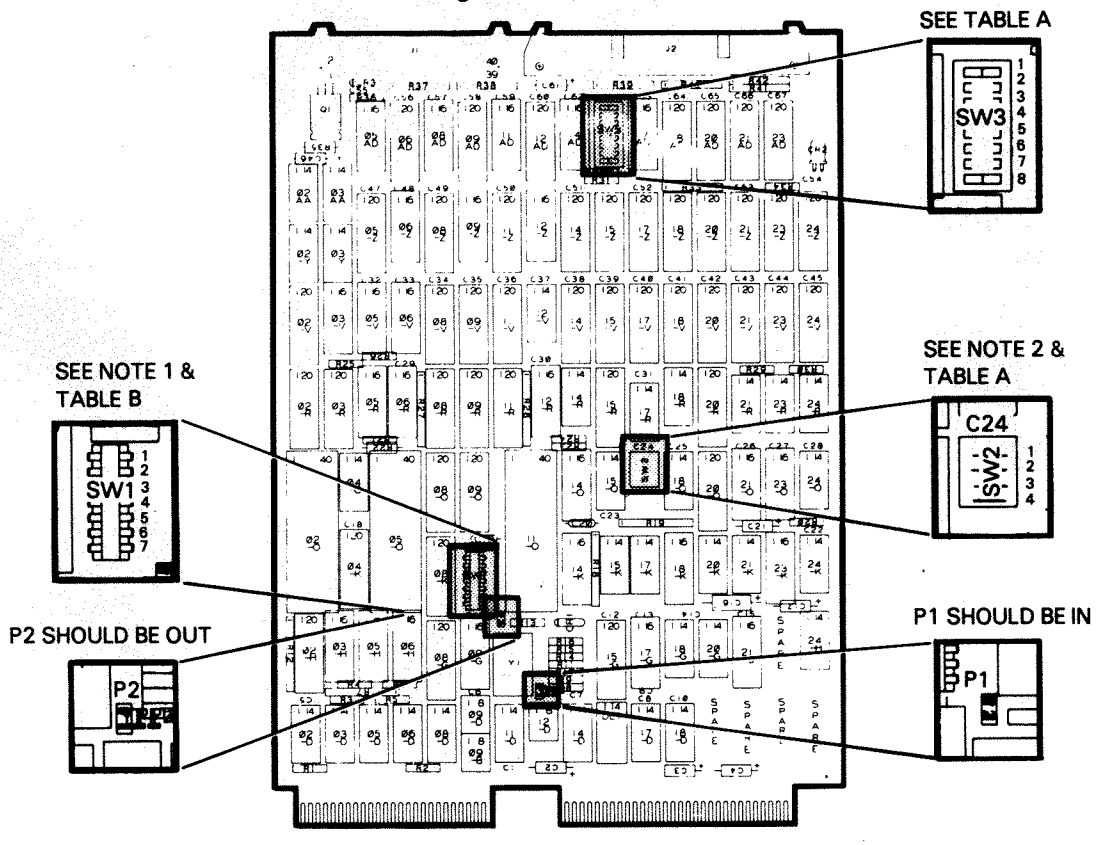

TABLE A

PRIORITY SELECT	S2			S3
	SW4	SW3	SW2	
HSCR7	ON	ON	ON	SW8
HSCR6	ON	ON	---	SW7
HSCR5	ON	---	ON	SW6
HSCR4	ON	---	---	SW5
HSCR3	---	ON	ON	SW4
HSCR2	---	ON	---	SW3
HSCR1	---	---	ON	SW2
HSCR0	---	---	---	SW1

NOTE:
TO SELECT BMC PRIORITY LEVEL 0-7, SET SWITCHES 2-4 OF S2 AS SHOWN AND TURN ON ONE SWITCH IN S3 AS INDICATED.

TABLE B

S1	DEVICE CODE (OCTAL)	
	25	65
SW1	OFF	ON
SW2	ON	ON
SW3	OFF	OFF
SW4	ON	ON
SW5	OFF	OFF
SW6	ON	ON

SWITCH NOTES:
1. SW1 TO SW6 OF S1 ARE DEVICE CODE SELECTION SWITCHES CORRESPONDING TO DS0 TO DS5 RESPECTIVELY, SWITCH ON FOR A-1, SW7 NOT USED.
2. SW1 OF S2 SHOULD BE ON.

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Figure 1-4. 6280 Controller PCB

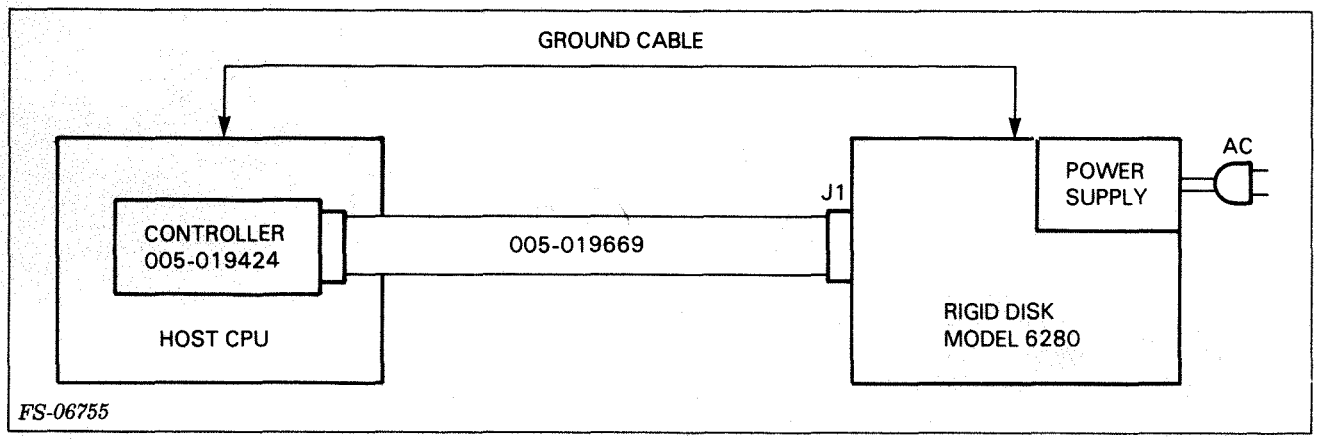

Figure 1-5. 6280 Interconnection Diagram

1.6 THE RIGID DRIVE

The 50.7 Mbyte disk drive uses three platters, a six surface, nonremovable platter stack as the recording media. This platter stack together with 12 read/write heads (two per surface) reside in a sealed data module. The heads are designed according to Winchester technology. The shape of the head pads produce sufficient aerodynamic lift to maintain correct flying height above the rotating disk. The heads also have a smooth, low friction landing face that comes in contact with the disk as it stops spinning.

The heads mount on a simple rotary actuator (similar to a record player arm). A precision stepping motor moves the heads to selected data tracks. This motor eliminates the need for closed loop servomechanisms commonly found in moving head disk drives.

A viscous damper is mounted below the stepping motor. It dampens the acceleration and deceleration of head movement and helps the heads to settle quickly.

Also mounted below the stepping motor is a home transducer. The home transducer detects head movement across the boundary between the recording area and the heads landing area on the disk. This boundary is the actuator home position.

The read/write and clock PCB mounts on the front of the drive (behind the front dress panel and front RF cover). This PCB contains circuitry that:

- Encodes and decodes the data in MFM format as it is transferred between the controller and the recording heads.
- Checks for fault conditions.
- Monitors the speed of the rotating disk.
- Keeps track of which sector is presently passing under the read/write heads.

A spindle motor and blower are located in the drive. The spindle motor rotates the recording platter via a drive belt. The blower, mounted on top of the spindle motor, forces air circulation inside the drive to provide cooling.

The disk drive is powered by a power supply assembly located in the drive. This power supply assembly consists of an ac power distribution PCB, a power transformer, and a power supply PCB.

The ac power distribution PCB routes ac power to the power transformer, the spindle, and the blower. The ac power distribution assembly is configured for various line voltages via a power ID plug which plugs into the ac power distribution PCB.

The power supply PCB receives power from the transformer, and generates all the dc power needed to operate the disk drive circuits.

1.7 RELATIONSHIP TO OTHER PRODUCTS

The 6234 disk subsystem is designed for use with NOVA or ECLIPSE computer systems. The 6280 disk subsystem is designed for use with microECLIPSE computer systems.

1.8 FIELD REPLACEABLE UNITS

Table 1-3 lists the FRUs that comprise the 6234/6280 Disk Subsystems.

Table 1-3. FRU List for Model 6234/6280

DESCRIPTION	PART NO.
Power Cord (220V and 240V)	005-010642
Power Cord (100V and 120V)	005-009935
Motor Assembly	005-009921
On/Off Power Cable	005-009944
P/S R/W System Signal Cable	005-009952
R/W System Power Cable	005-010638
AC Sequence Cable	005-010639
AC/PD PCB	005-010641
Home Transducer Assembly	005-010652
R/W Led Cable	005-010761
AC Power Harness	005-010764
Ground Jumper Kit	005-012005
Power ID plug 100V	005-012592
Power ID plug 120V	005-012593
Power ID plug 220V	005-012594
Power ID plug 240V	005-012595
Ground Strap Assembly	005-009536
Front Panel (blue)	005-014213
Front Panel, (paji brown)	005-019576
Controller PCB (NOVA/ECLIPSE)	005-015551
Controller PCB (ECLIPSE S20)	005-019424
Signal Cable	005-016974

Table 1-3. FRU List for Model 6234/6280 (Cont.)

DESCRIPTION	PART NO.
Power Supply PCB	005-017474
50 MByte Disk, Basic	005-017586
50 MByte Module w/drive	005-017589
R/W Clock PCB	005-017591
Hardware Mounting Kit	005-019126
Transformer	005-009930
Blower Wheel	123-001351
Capacitor 145-175 MFD/165V	103-000387
Switch 3 Position Single Throw 15A	110-000359
Fuse 2A - 250V	113-000041
Fuse 5A - 250V	113-000047
Fuse 10A - 32V	113-000054
Fuse 0.5A - 250V	113-000061
Fuse 7A - 100/120V	113-000175
Fuse 1.5A - Fast Blow	113-000176
Fuse 4A - 220/240V	113-000177
Semi-elastic Belt	118-001740
Mounting Kit Paddleboard (NOVA/ECLIPSE)	005-013627
CPU Int. Cable (NOVA 3, S/230, C/330, S/130, C/150, AP/130	005-001802
CPU Int. Cable (NOVA 4, S/140, S/120	005-012472
CPU Int. Cable (S/250, C/350, M/600	005-012496
CPU Int. Cable (hardened MV Series)	005-019499
Ext. I/O Cable (nonhardened NOVA/ECLIPSE)	005-017587
Ext. I/O Cable (hardened MV Series)	005-018480
Ext. I/O Cable (nonhardened S20)	005-019669
BMC Cable (S20 Model 6280 only)	005-020210
BMC Terminator (S20 Model 6280 only)	005-013419

SECTION 2

OPERATING CONTROLS AND PROCEDURES

This section contains descriptions of operator controls and indicators for Model 6234/6280 disk subsystems.

NOTE

The operating instructions and controls described in this section are intended for the maintenance engineer only. Equipment operators should refer to the operator's guide, 014-000748 for the disk operating instructions.

2.1 OPERATING PROCEDURES

Set the Power ON/OFF switch to ON. Wait for the DC POWER LED and READY LED to light. When both LEDs are on, the drive is ready to accept commands from the controller located in the host computer.

2.2 CONTROL SWITCHES AND INDICATOR LAMPS

The following switches and indicators are located on the front of the disk drive (see Figure 2-1).

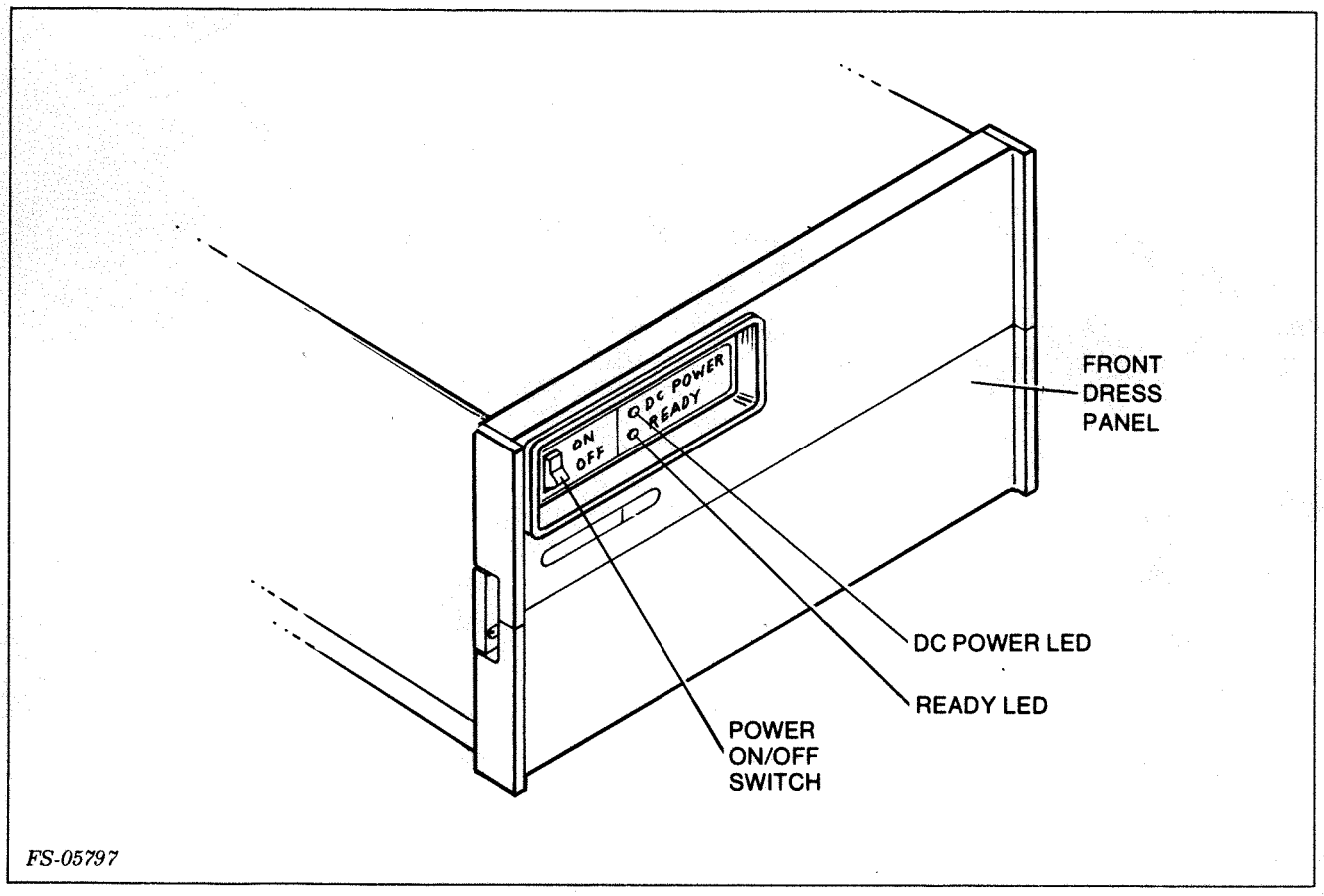

Figure 2-1. Front Panel ON/OFF Switch and Indicators

ON/OFF - This is the power switch. Setting this switch to the ON position powers up the drive. Setting the switch to OFF removes power from the drive after a one second delay. During this one second the heads move out of the recording area of the disk and into the landing area where they come to rest on the disk.

DC POWER - When ON, this LED indicates that the DC power supply is energized.

READY - When this LED is on, the spindle motor is up to speed, the power up reset signal has timed out, the DC voltages are within operating specifications, and the drive is not in a seek operation. The READY LED is off during any head positioning (seek, recalibrate) operations.

WRITE PROTECT and UNIT SELECT Switches - Removing the front dress panel exposes these two switches. The switches are on the Read/Write and Clock PCB and are reached through a cutout in the front panel.

- UNIT SELECT - When this switch is set to the right, the normal position for the switch, (see Figure 2-2) the disk drive is addressed as unit 0. This switch should always be set to the right-hand position with the following exception. If an optional flexible drive is connected to a 6234 disk subsystem then the UNIT SELECT switch can be set to the left-hand side, allowing the flexible drive to boot a program. After booting the program from the diskette, return the switch to the normal position. If the disk subsystem is a 6280, the UNIT SELECT switch is nonfunctional.

- WRITE PROTECT - Place this switch in the left-hand position to stop write operations on the disk drive.

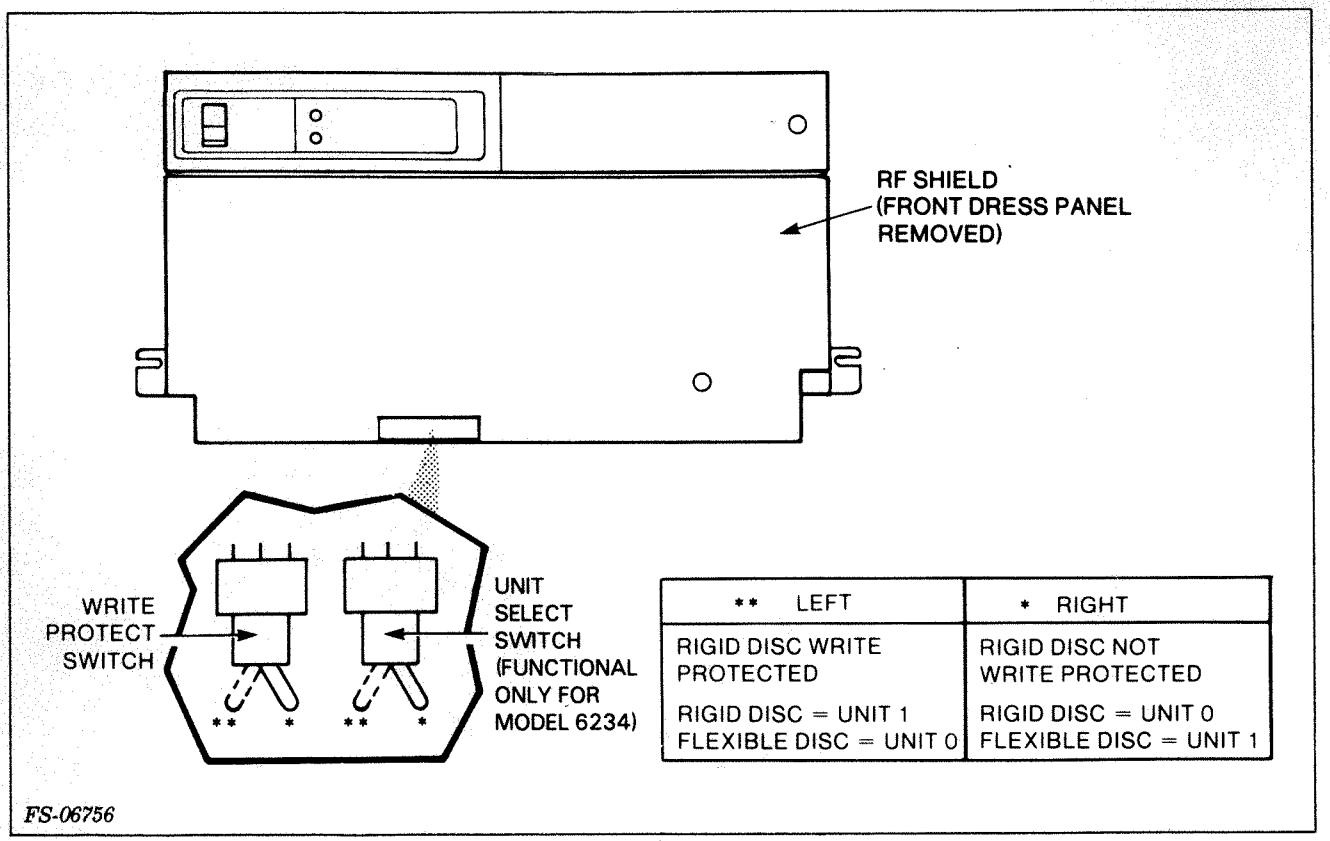

Figure 2-2. Unit Select and Write Protect Switches

SECTION 3

THEORY OF OPERATION

This section provides an overview of the theory of operation for the 6234/6280 disk subsystem. The theory discussion contains descriptions of both the subsystem architecture and operation functions.

Figure 3-1 is a block diagram of both the major hardware and logic areas. There are four PCBs controlling system operation. Three of the PCBs are located within the disk drive and the fourth PCB is the system controller located in the host CPU. The 6234 host CPU can be either a NOVA or ECLIPSE computer. The 6280 host CPU is a microECLIPSE computer. The three PCBs resident in the disk drive are the read/write and clock, power supply, and ac power distribution.

Other major FRUs contained in the disk drive are:

- Sealed data module
- Power transformer
- Power switch
- Power ID plug
- Home transducer
- Spindle motor
- Blower
- Drive belt

3.1 MODEL 6234 CONTROLLER PCB

The controller contains logic blocks as shown in Figure 3-2. In addition to the logic blocks there are two I/O interfaces. One I/O interfaces the CPU with the drive control logic, and:

- Translates between the CPU 16-bit data bus and the controller 8-bit bus
- Controls a 256 word RAM for full sector buffering on disk drive read/write operations

The second I/O interface connects the controller PCB to the disk drive via the paddleboard connector on the host CPU.

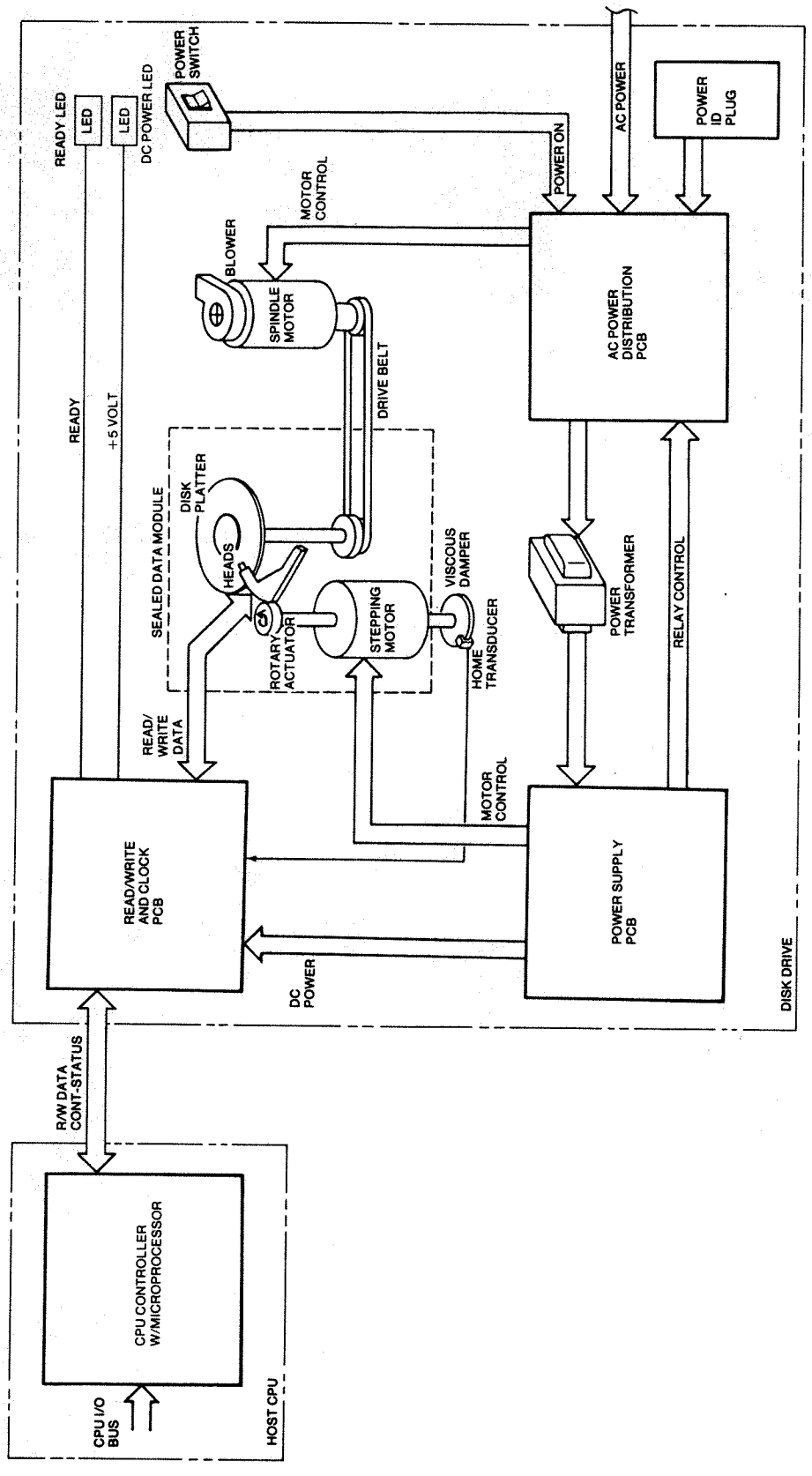

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Figure 3-1. 6234/6280 Block Diagram

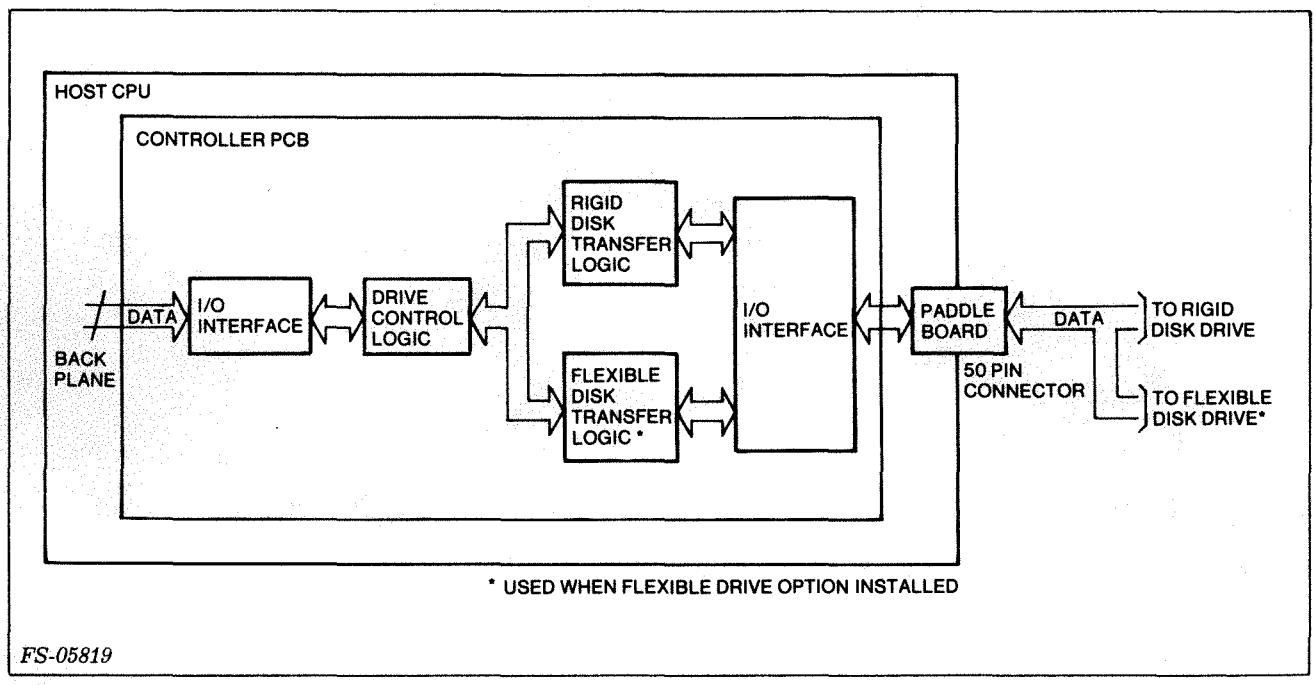

Figure 3-2. 6234 Controller PCB Block Diagram

The logic blocks on the controller are:

- Drive control
- Rigid disk transfer
- Flexible disk transfer

3.1.1 Drive Control Logic - The drive control logic contains the microprocessor and associated firmware. The microprocessor receives instructions (command signals and control information) from the I/O interface to set up and initiate seek, recalibrate, and read and write operations. The drive control:

- Determines Read/Write/Seek/Recalibrate operations
- Provides subsystem status on request
- Directs drive operations
- Programs (ROM firmware) microprocessor subsystem operation
- Fetches, decodes and executes host CPU commands
- Informs the host CPU that operation is complete by setting the Done flag and clearing the Busy flag
- Provides positioner commands
- Gives logical to physical sector conversion

3.1.2 Rigid Disk Transfer Logic

- Handles data logic
- Converts parallel data to serial data for a write operation
- Converts serial data to parallel data for a read operation
- Checks address
- Checks CRC (Cyclical Redundancy Check) characters

3.1.3 Flexible Disk Transfer Logic

- Handles data logic
- Checks addressing
- Checks CRC characters
- Handles all flexible disk drive functions

3.2 MODEL 6280 CONTROLLER PCB

The controller contains logic blocks as shown in Figure 3-3. In addition to the logic blocks there are two I/O interfaces, computer and device.

- The computer interface takes two paths. In path one, Commands, parameters and status signals are transferred via the backpanel I/O Control (IOC) bus (which conforms to the microNOVA bus standard) to the controller. In path two data is transferred via the 60 line bus to the Burst Multiplexor Channel Controller directly to/from main memory. Should the 6280 controller be the last controller on the 60 line bus, the connector accepts a shunt plug to terminate the bus.
- The second interface connects the controller PCB to the disk drive via a 50-pin "A" connector.

The controller logic blocks are:

- Hard Disk Control (HDC)/Microprocessor
- 32-word FIFO
- I/O Control

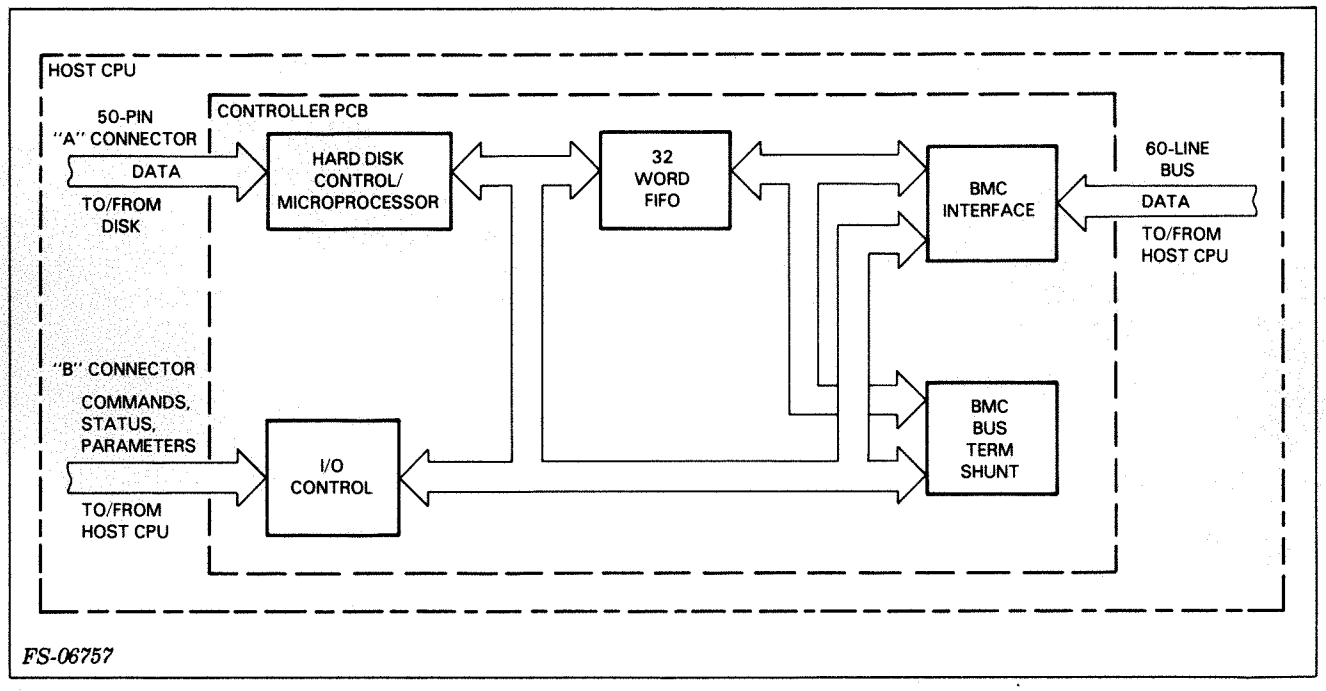

Figure 3-3. 6280 Controller PCB Block Diagram

3.2.1 Hard Disk Control/Microprocessor - The HDC/microprocessor logic contains the disk control, microprocessor and associated firmware. The microprocessor interfaces with the HDC to initiate all read/write operations and check status after the operation is complete. The microprocessor receives instructions (common signals and control information) from the I/O interface to set up and initiate seek, recalibrate, and read and write operations. The HDC/microprocessor:

- Determines Read/Write/Seek/Recalibrate operations
- Provides subsystem status on request
- Directs drive operations
- Programs (ROM firmware) microprocessor subsystem operations
- Fetches, decodes and executes host CPU commands
- Informs the host CPU that operation is complete by setting the Done flag and clearing the Busy flag
- Provides positioner commands
- De-maps sector addresses during read/write operations to provide a 4x increase in data throughput (completely transparent to host software)
- Handles data logic
- Converts parallel data to serial data for write operation

- Converts serial data to parallel data for a read operation
- checks address
- checks CRC characters

3.2.2 32-word FIFO - The HDC is designed to handle one sector per command. The microprocessor is not fast enough to restart the HDC between sectors during multi-sector transfers. To overcome this a pipelining scheme is utilized to perform this task. Data is buffered between the HDC and the BMC by a 32-word FIFO array.

3.2.3 I/O Control - The I/O control logic interface with I/O bus to provide Command, Status, Parameter, and Interrupt signals.

3.3 HEAD PRECOMPENSATION

Precompensation is done in the controller and sent over the I/O cable. Used with MFM encoding, precompensation allows the recording of an edge cell early or late to partially compensate for the effect of track density. When writing, precompensation uses one of three values:

0
6 nanoseconds
12 nanoseconds

The outer tracks and outer heads receive 0 second. The inner tracks and inner heads receive 12 nanoseconds. The boundries of the tracks receiving 6 nanoseconds is under software control. Head precompensation is shown in Table 3-1.

Table 3-1. Model 6234/6280 Head Precompensation

PRECOMPENSATION	OUTER HEAD	INNER HEAD
0	TRACK 0 - 127	NONE
6 NANOSECONDS	TRACK 128 - 191	TRACK 0 - 63
12 NANOSECONDS	NONE	TRACK 64 - 191

3.4 SEALED DATA MODULE

Three major assemblies in the sealed data module (see Figure 3-4) are:

- The head positioner
- The sector disk
- The clean air system

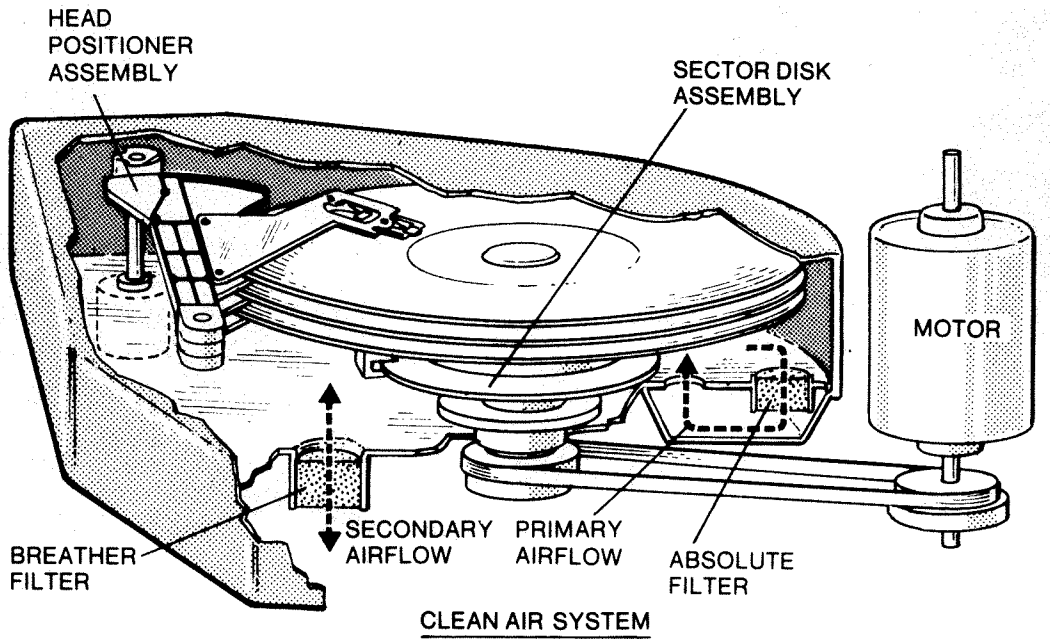

Figure 3-4. Sealed Data Module

3.4.1 Head Positioner - Figure 3-5 shows the mechanical assembly that moves the recording heads across the disk surfaces. It has two major parts:

- An actuator arm to rotate around a pivot and swing the heads toward and away from the spindle.
- A stepping motor to move the arm in small increments to position the heads over individual data tracks.

The rotary actuator arm mounts on a ball bearing pivot. Plates are attached to the upper and lower surfaces of the arm and support the head assemblies. The heads move in an arc across the disk surface, but the angle of the arc is never severe enough to degrade the data.

The stepping motor shaft rotates in precise 0.9 degree steps. Each step moves the heads to the next track. Two steel bands link the

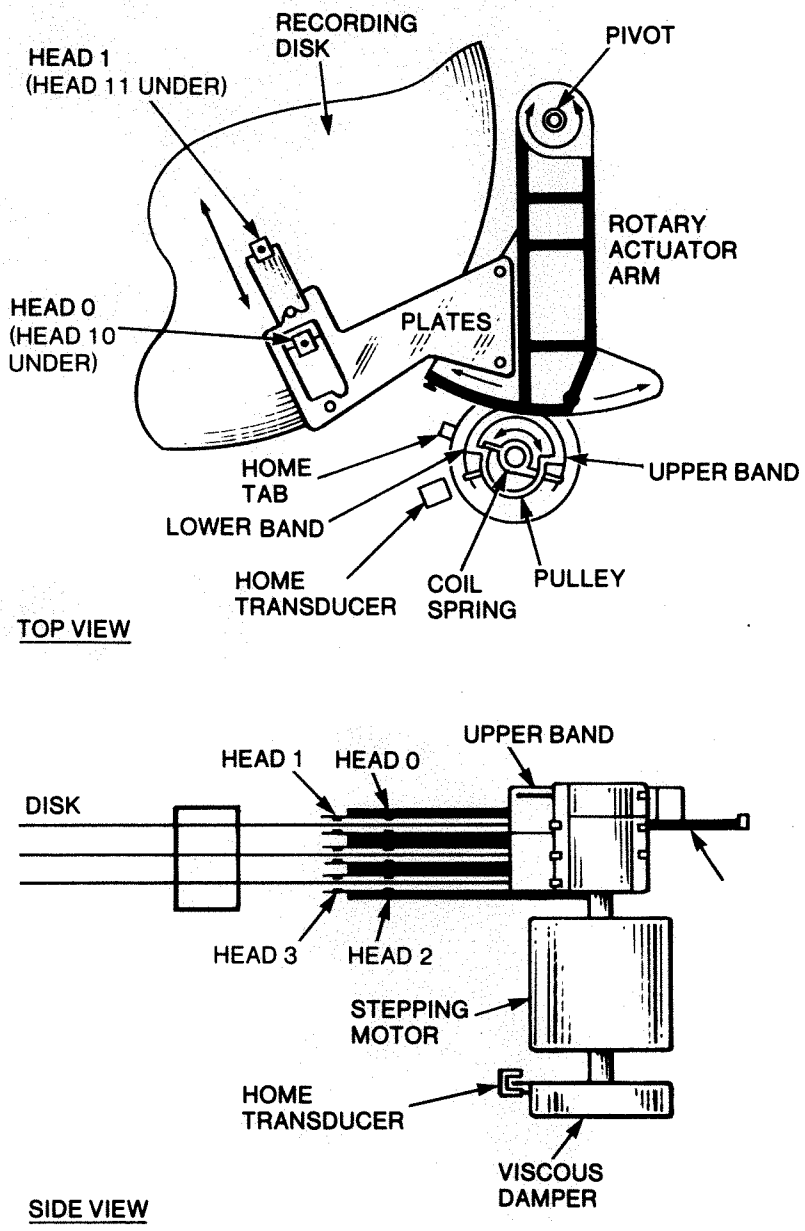

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Figure 3-5. Head Positioner

actuator arm to a pulley on the motor shaft. A coil spring inside the pulley holds the bands under constant tension. As the motor turns, one band winds onto the pulley, and the other one unwinds. This pulls the arm back and forth and prevents slippage that could degrade positioning accuracy. The stepping motor and rotary actuator are so precisely controlled, that positioning accuracy is obtained without feedback servo.

A viscous damper is mounted on the bottom of the motor shaft. This damper ensures that the heads settle rapidly on the destination track (i.e, prevents oscillation of the heads after a seek operation).

A home transducer sensor, also mounted below the stepping motor, detects head movements across the boundary between the data zone and the head landing zone on the disk. A tab that projects from the viscous damper, breaks the light path in the sensor as the stepping motor moves the heads into the landing zone.

3.4.2 Sector Transducer and Sector Disk - The sector disk is a separate disk, mounted below the recording disk. It has 688 evenly spaced holes around its outer edge. An optical sector transducer is mounted on the sector disk (see Figure 3-6). As the spindle turns, the holes on the sector disk alternately break the light path in the optical sector transducer. This causes the transducer to generate pulses to sense sector boundries, monitor rotational speed, and provide a write data clock.

Two of the webs between holes on the sector disk are cut off. This pattern provides an index mark to locate the beginning of sector zero.

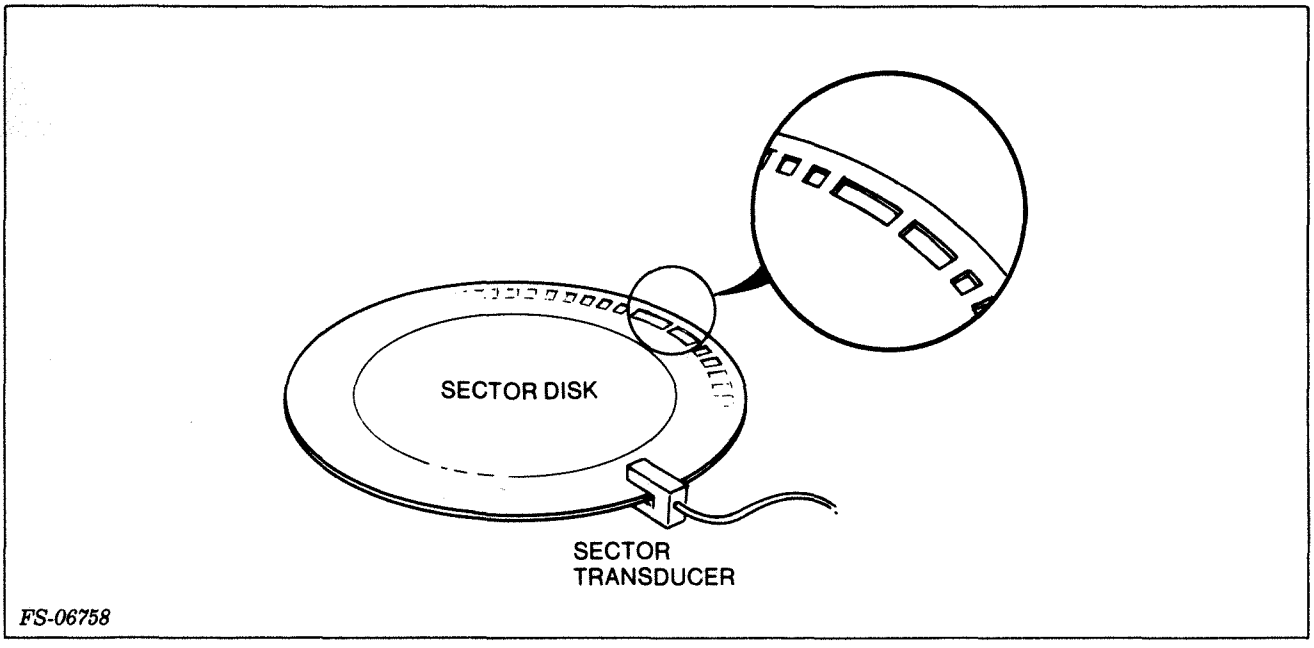

Figure 3-6. Sector Disk

3.4.3 Clean Air System - Figure 3-7 shows how air flows in the sealed data module. There are two airflow paths:

1. The primary airflow path recirculates air within the sealed module. An impeller mounted below the sector disk draws air from the center and the recording disk and forces it toward the outer edges of the sealed data module. As the air moves, it passes through an absolute filter. This traps any foreign particles that could damage the heads or disk.

2. The secondary airflow path vents the sealed module. This accommodates atmospheric pressure changes. A breather filter prevents particles from entering the sealed data module.

NOTE

A very dirty breather filter may indicate an air leak in the data module.

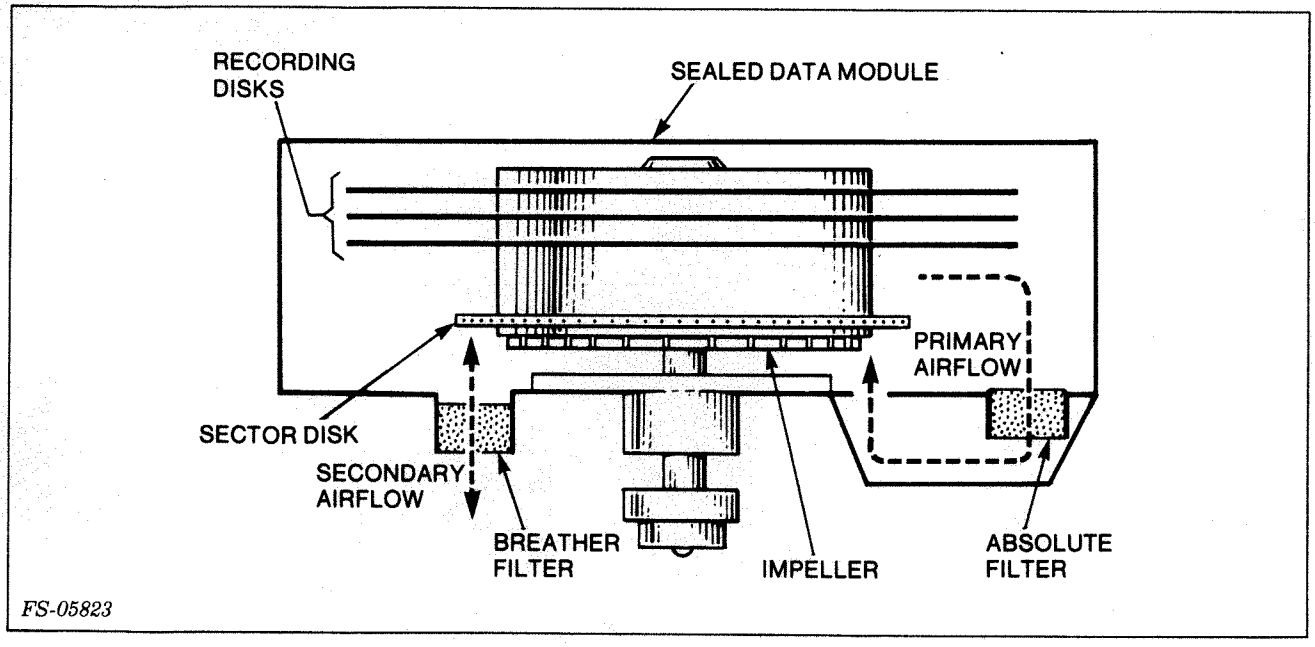

Figure 3-7. Clean Air System

3.5 READ/WRITE AND CLOCK PCB

The read/write and clock PCB contains circuitry (see Figure 3-8) that decodes data in MFM format as the data transfers to the CPU controller from the sealed data module. MFM encoded data is prepared at the controller before being sent through the Read/Write and Clock PCB to the data module. The Read/Write and Clock PCB also keeps track of which sector is presently passing under the read/write heads, monitors the speed of the rotating disk and checks for fault conditions. The Read/Write and Clock PCB governs the following circuits:

- Write
- Read
- Sector clock
- Sector counter
- Read clock
- Home transducer

3.5.1 Write Circuits - The write circuits include: a write driver, control and fault logic, and chip select (CS) and head select (HS) decode logic.

Precompensated RZ (return to zero) MFM encoded data arrives from the controller over a bidirectional balanced terminated line. The logic is converted to TTL, ECL and then to NRZ (nonreturn to zero). RZ means that each positive going signal edge corresponds to a flux transition. NRZ is defined as a high representing head current in one direction and a low as current in the other direction. The digital data X and data Y lines are bidirectional and are gated off during a read. At this time these lines become analog instead of digital.

The control and fault logic determines mainly write type faults. Checked are buss overcurrent and unsafe conditions. Multiple head select is not checked. If the WRT SEL/CT BUSS line draws more than 100 ma, DRVFLT (drive fault) comes high. Unsafe faults are checked in the head chip. If the write frequency is too low, or if a head is open or shorted, the circuit is set up to draw excessive current causing UNSAFE to go high. Another fault that can be detected by the fault logic is the write current-no command. When sensed, current on the WRTI line is diverted away from the heads to the UNSAFE line which causes DRVFLT to come high.

WRT is a power fault line from the power supply. It is low if any of the four voltages are either too high or too low which disables the drive from writing by pulling signal WRT SEL/CT BUSS low.

The decoder is used as a chip select for the four head interface ICs. One of the four CS (chip select) lines is pulled to ground, selecting one chip. The head numbering in the module is scrambled in order to simplify CS code. Figure 3-9 shows the head numbering and Table 3-2 the decode truth table.

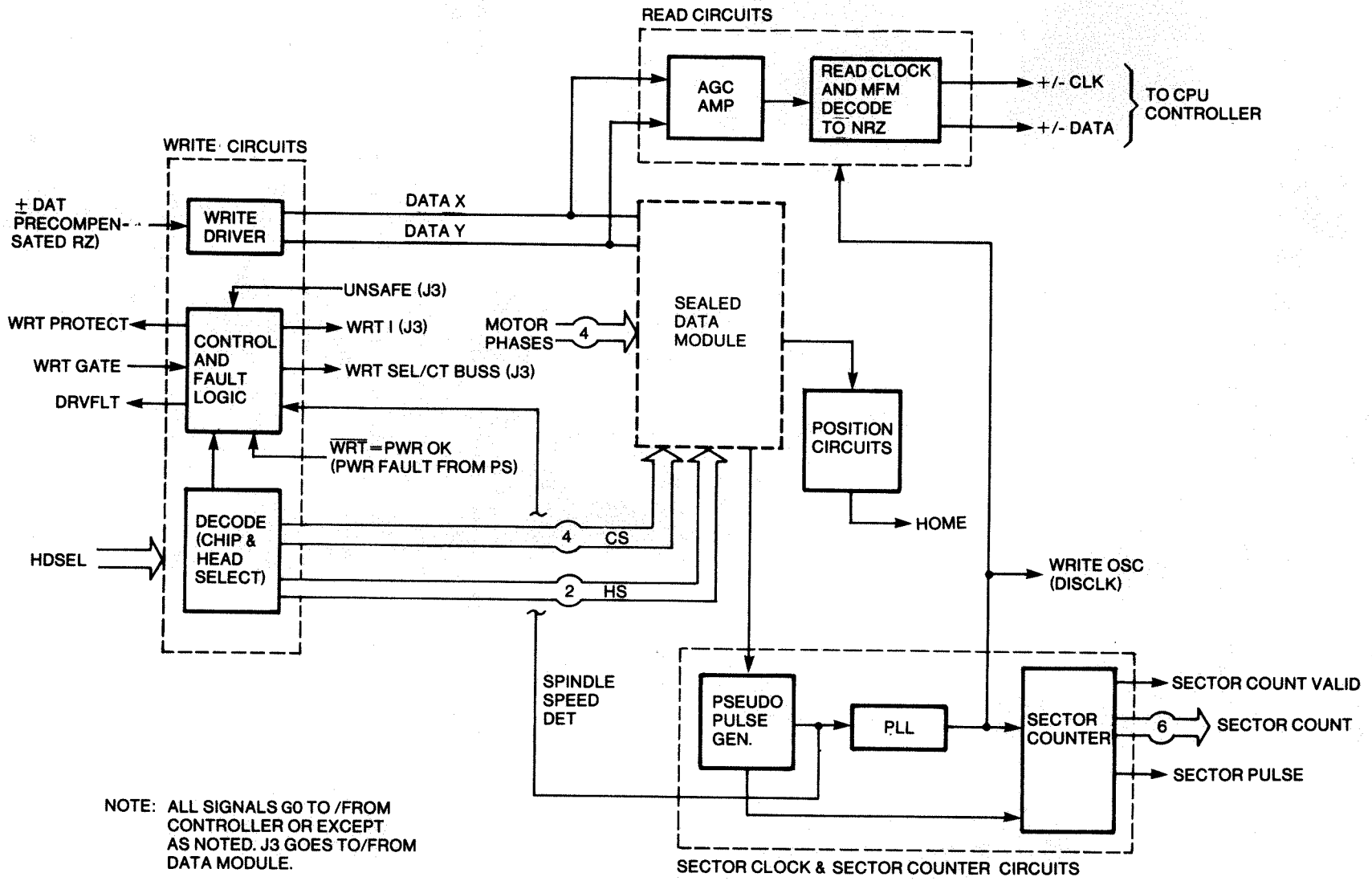

Figure 3-8. Read/Write and Clock PCB Block Diagram

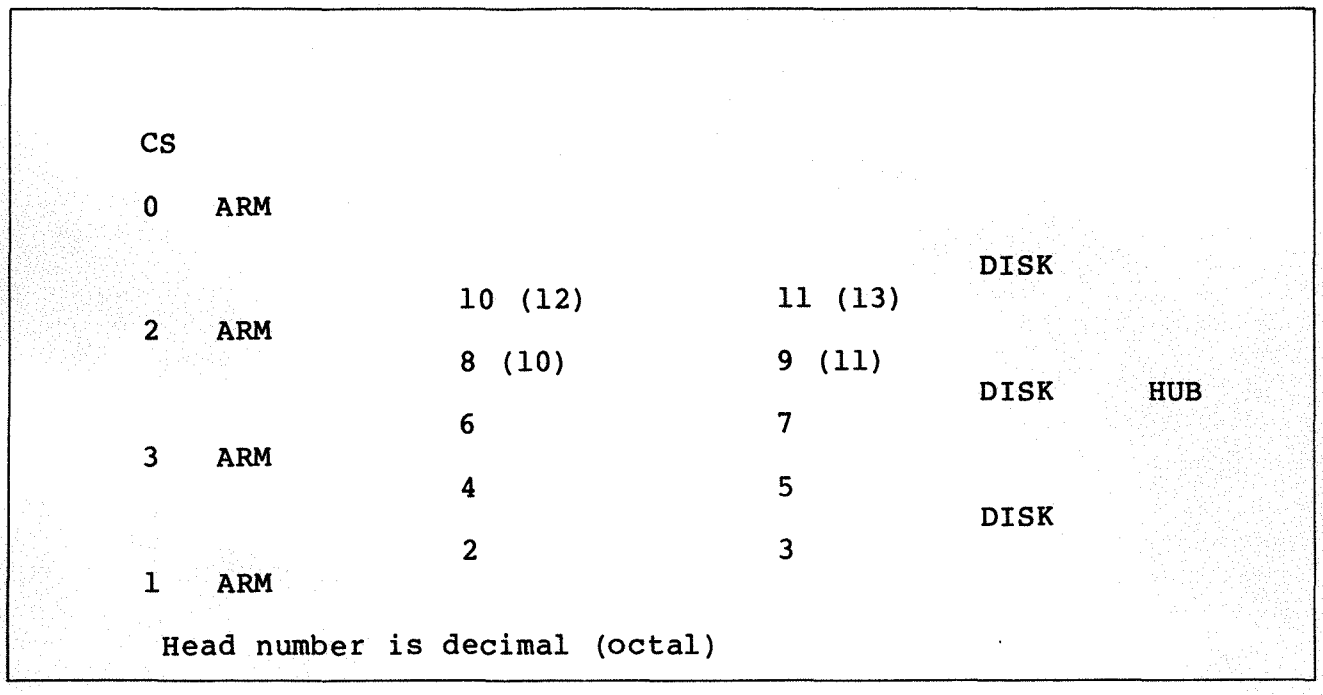

Figure 3-9. 6234/6280 Head Numbering

Table 3-2. Truth Table for Head Decode Head Select (HS), Chip Select (CS)

HS3	HS2	HS1	HS0	CS
0	0	0	X	0
0	0	1	X	1
0	1	0	X	3
0	1	1	X	3
1	0	0	X	2
1	0	1	X	2
1	1	X	X	*

* No chip selected due to an illegal head address

3.5.2 Read Circuits - The head chip in the sealed data module contains a two-stage read amplifier with a gain of 40 and a 100 MHz bandwidth. A read back signal is obtained with "Daisy" type heads and an associated head chip. The read data from the data module is sent via a bidirectional buss as DATA X and DATA Y to an AGC amplifier in the read circuits. The signal is sent through the read circuits where it is MFM decoded to NRZ and sent back to the controller as signal +/- DAT and +/- CLK.

3.5.3 Sector Transducer - The sector disk is a 200 mm diameter disk with 688 slots (two webs between holes are missing from the sector wheel) and is located just below the lower disk. Speed and position are sensed with a LED-Photo transistor pair. This assembly is referred to as the sector transducer. A backup pair is fixed in place in case of failure. If failure does occur, the FE turns connector J4 over to bring the transducer spare label into view.

The output, after passing through a pseudo-pulse generator, has a frequency 27,520 Hz (40 Hz x 688 holes). This frequency is multiplied up twice the data rate by a phase locked loop (PLL). The factor used is 568. The hole frequency is counted down by 16 to obtain sector pulse and further counted down by 43 to obtain the index mark.

The phase/frequency detector produces pulses (UPS/DNS) to direct the oscillator frequency to go up, go down, or not change. The net result WRT OSC is sent to the controller (DISCLK) to serve as a reference.

3.5.4 Sector Counter - WRT OSC is counted down by a factor of four. The frequency for WRT OSC corresponds to 1/2 of a bit cell and is 15.6 MHz. WRT OSC/4 is called 2BIT and is used to clock all subsequent synchronous counter stages that count down to 40 Hz (one revolution). The first stage in the sector counter is a divide by 142 counter which counts down to the sector wheel hole frequency. There are 16 holes in a sector so the next stage, after the count, produces SCTPLS (a sector pulse) and SCNTVALID (sector count valid). The latter is low during the final eighth of the sector to inform the controller that a sector pulse is coming soon.

The final stage counts sectors from zero to 42. This stage along with all previous stages are reset by INDEX. A ....1010... hole pattern in the sector disk is also looked for to define INDEX.

The six sector count lines (SCNTVALID and SCTRPLS) are buffered and sent to the CPU controller.

3.5.5 Read Clock - The purpose of the read clock is to lock up to MFM encoded data recovered from the disk and to decode it. This is necessary due to the uncertainty in head location in relation to the disks. This occurs in the order of +/- 4-bit cells and so the data appears to arrive in random phase each time it is read. The loop is also required to compensate for spindle speed variations. Because the MFM phase detector can lock on a harmonic, it is necessary to keep the loop locked-in with the sector clock when not actually reading data. The phase-frequency detector, part of the read circuits, is used for this purpose. RD OSC is divided by two to derive RD CLK which is then sent to the CPU controller (CLK) along with the decoded data (DAT). The proper phase of RD CLK is determined by knowing that the 2f received during preamble is defined as all zeros. The proper phase detector is selected by RD GATE. During

preamble RD CLK phase is also set. After PREAMBLE comes up, the MFM data signal is decoded.

3.5.6 Home Transducer - The home transducer is a LED-phototransistor pair similar to the sector transducer except there is no spare. The output current is compared to a reference and sent to the controller. The HOME line is high for tracks 0 through 191 and low for tracks 193 or greater. Home 191 is defined at track 192.

Stepping motor signals are generated by the CPU controller and sent to the power driver stages on the power supply (if there is no speed fault [SPD FLT]).

3.6 POWER SUPPLY PCB

The block diagram in Figure 3-10 shows all of the power supply circuits. Most of them are located on either the ac power distribution PCB or the power supply PCB. Only the line filter, line fuse, and power transformer mount directly on the disk drive enclosure.

The four transformer secondary windings connect to rectifiers on the power supply PCB. The rectifiers produce six unregulated dc voltages. The +16 volt source energizes the stepping motor. The +24 volt source is an unused regulated voltage. The remaining four voltages are regulated to supply power for the rigid drive circuits. These voltages are -15 V, +15 V, -5 V, and +5 V.

When the power switch is turned on and DC power comes up, the power control logic generates a POR (power-on reset) pulse. At the same time, the power control logic turns on the motor start and the ac relays, located on the ac power distribution PCB. During power up, the motor start relay turns off when the spindle comes up to speed, or after 8 seconds. During power down, the ac relay remains on for one second after the power switch is turned off. This gives the disk drive time to move the heads to the landing zone.

Power fail detectors on the power supply PCB monitor the -15 V, +15 V, -5 V, and +5 V that power the disk drive circuits. If any voltage goes above or below a preset threshold, the power control logic disables the write operation, and resets the CPU controller.

There are five CPU LEDs on the power supply PCB. The LED connected to the +8.5 volt unregulated supply indicates the presence of ac current.

3.7 AC POWER DISTRIBUTION PCB

This PCB routes ac power to the power transformer and spindle motor. Current flows through the line filter, fuse, and power switch and into primary windings of the power transformer. The primary windings are tapped to route power to a full-wave rectifier on the ac distribution board.

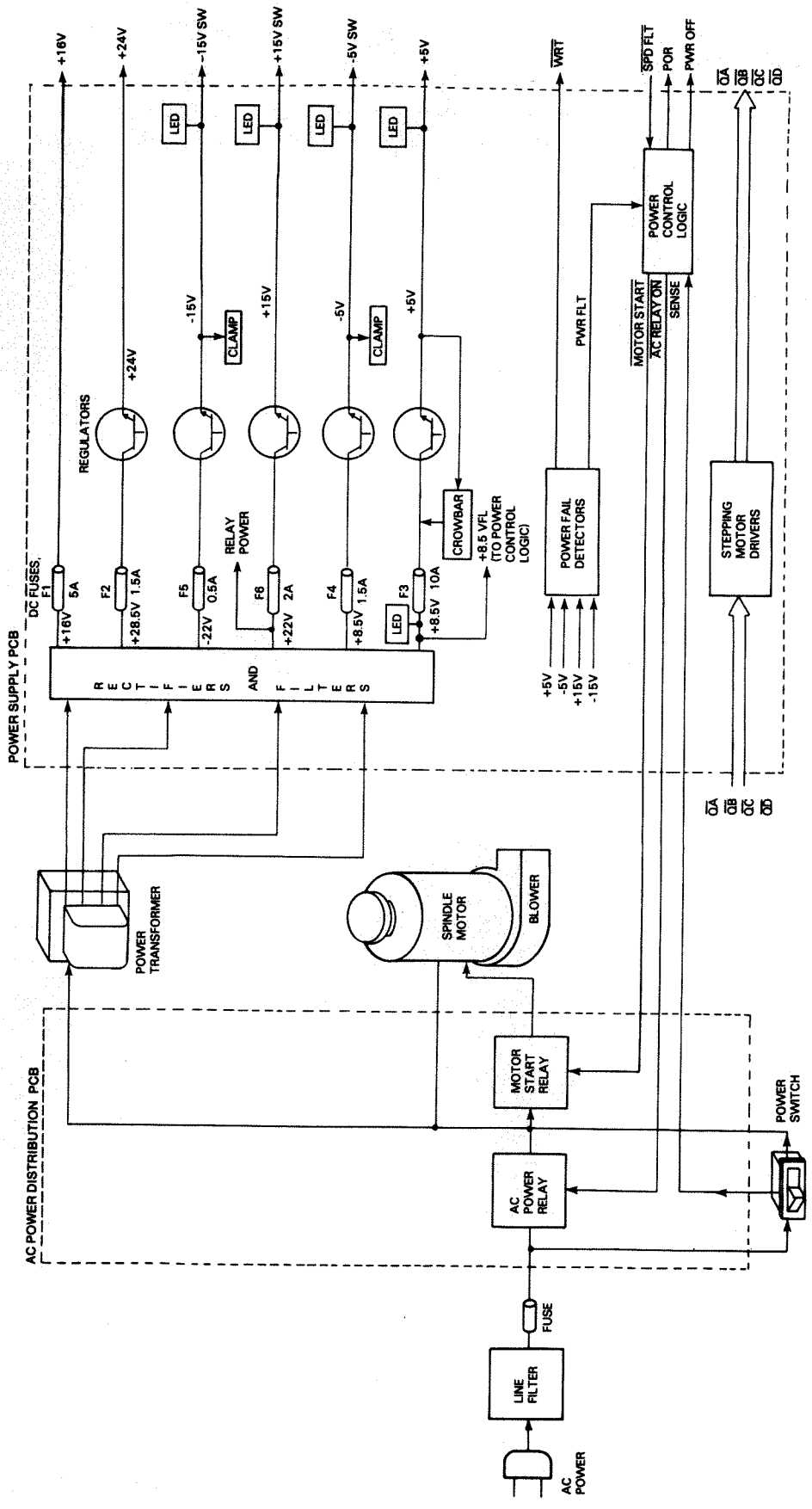

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Figure 3-10. Power Supply Block Diagram

3.8 FORMAT OPERATION

The sector format is shown in Figure 3-11 and defined in Table 3-3. The disk drive will not function properly unless the data surfaces of the disk are formatted. The format procedure delineates an address field and a 512-byte field in each sector of every data track on the recording disk. The address field of a sector is a coded header that precedes the data block. The format operation records the field at a specific location within the sector to give the read and write control circuits enough time to initialize and settle before the field is read.

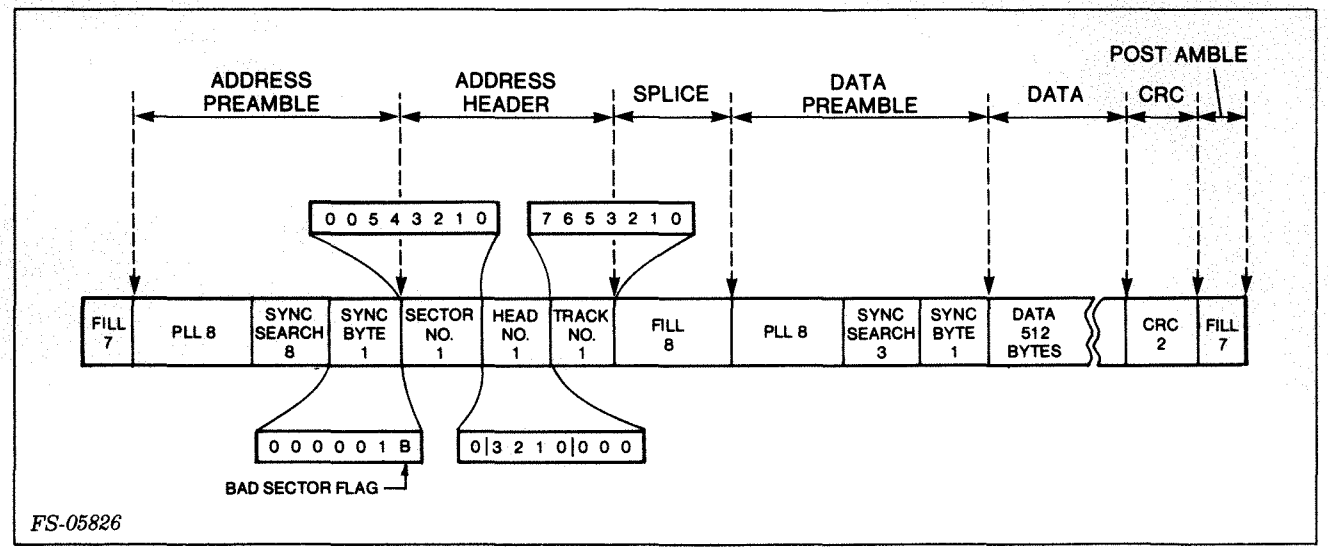


Figure 3-11. Sector Format

Table 3-3. Sector Format Description

NO OF BYTES	NAME	DESCRIPTION
7	FILL	+/- 6 BYTES ALLOWED FOR XDUCER UNCERTAINTY
8	PLL	LOCK READ CLOCK AND SET UP MFM DECODER
8	SYNC SEARCH	LOOK FOR SYNC MARK
1	SYNC BYTE	0000001B IS PATTERN (B IS BAD SECTOR FLAG)
1	SECTOR NO	0- 42 (DECIMAL) 0- 52 (OCTAL)
1	HEAD NO	0- 11 (DECIMAL) 0- 13 (OCTAL)
1	TRACK NO	0-191 (DECIMAL) 0-277 (OCTAL)
8	FILL	LOCK READ CLOCK TO SECTOR CLOCK
8	PLL	LOCK READ CLOCK AND SET UP MFM DECODER
3	SYNC SEARCH	LOOK FOR SYNC MARK
1	SYNC BYTE	00000001 IS PATTERN
512	DATA	
2	CRC	CHECKWORD
7	FILL	LOCK READ CLOCK TO SECTOR CLOCK
---		
568 TOTAL		

For Model 6234, the disk drive uses a "hard sector" technique to locate sectors. Transfers to and from the drive are fully sector buffered to prevent the drive from exceeding throughput capacity of the DCH. This means that the drive cannot transfer contiguous physical sectors. If a multiple sector transfer is to be executed at the maximum possible speed, the sector numbering must be interleaved. These sectors are interleaved by a factor of 4 (see Figure 3-12), meaning the disk drive can transfer every fourth physical sector.

For Model 6280, the ECLIPSE S20 microBMC is used for data transfers. This is a high speed channel. The 6280 controller transfers contiguous sectors. For system capability, the 6280 uses the same sector format as the 6234 with address mapping in the disk headers as shown in Figure 3-12. However, since it transfers contiguous sectors, the 6280 controller "demaps" the sector addresses when it does transfers.

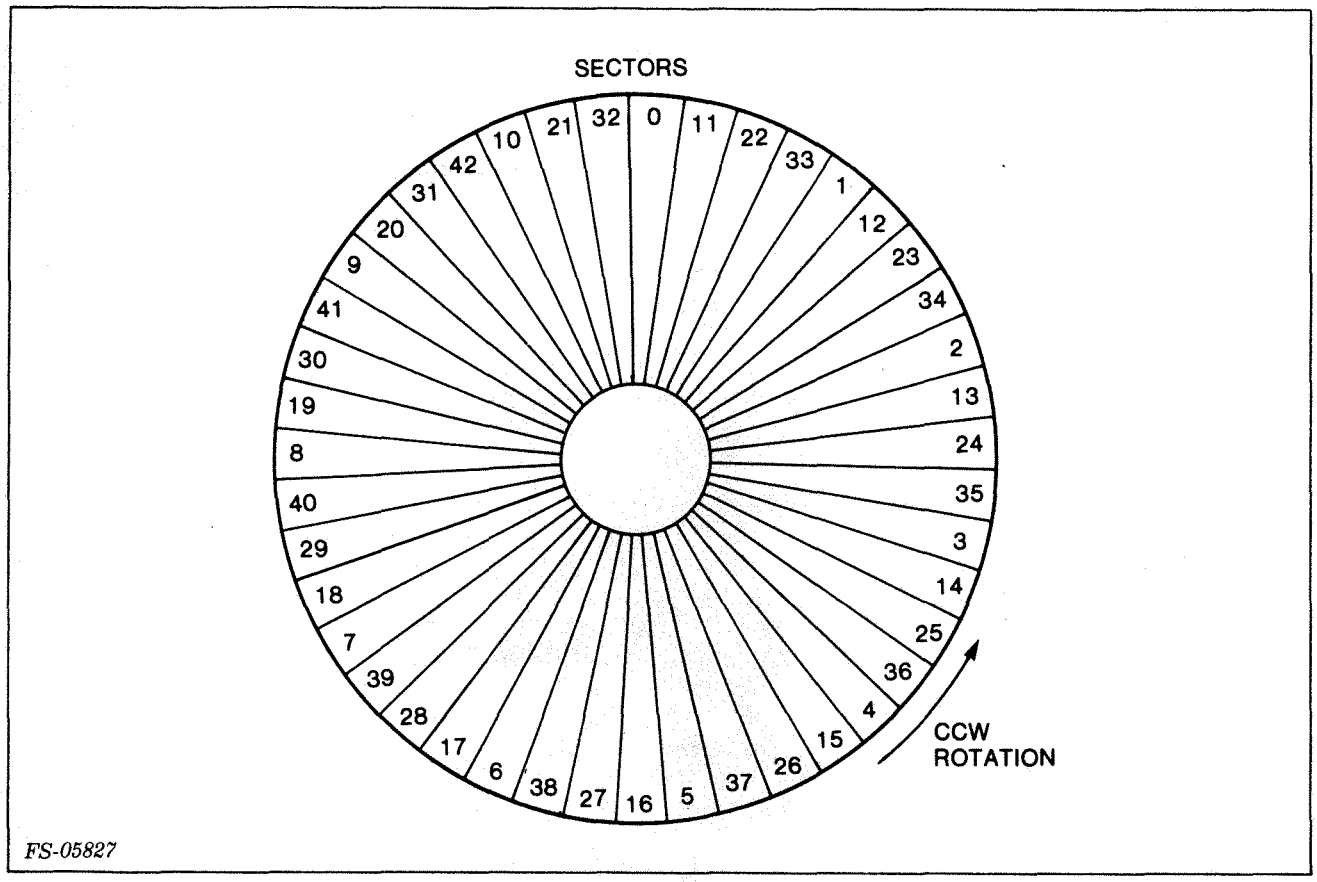


Figure 3-12. Sector Interleaving

The disk rotates counterclockwise, spanning 43 sectors per revolution. Each sector is divided into seven parts according to a preset format. This is shown in Figure 3-13 and described as follows.

3.8.1 Address Preamble - gives the drive time to prepare for the address header transfer. During this time, the read circuits stabilize the read signal amplitude, derive a data clock from the data stream, and search for the synchronization word that signals the beginning of the address word. The preamble also allows for "jitter" in the position of the sector pulse that marks the beginning of the sector. (Sector position information is obtained from a mechanical sector, disk-mounted below the recording disk. Mechanical variations can therefore move the position of the sector pulse relative to the boundries of the actual recorded sector.)

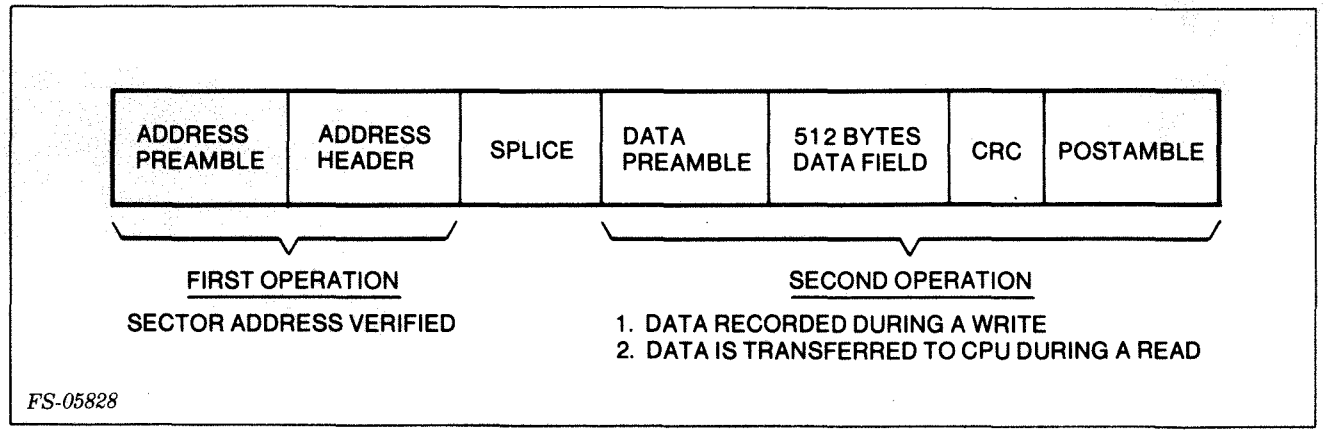


Figure 3-13. R/W Sector Format

3.8.2 Address Header - The Address Header indicates the track, head, and sector address of the sector. The CPU controller uses this information to detect seek, head select, and sector count errors. The header also includes a bad sector flag which can be set when the disk is formatted to prevent the drive from recording data in that sector.

3.8.3 Splice Zone and Data Preamble - The Splice Zone and Data Preamble give the drive time to prepare for the data block transfer. During this time, the read circuits:

1. Shut down until the splice passes by
2. Restabilize the read signal amplitude
3. Derive a data clock from the data stream
4. Search for the synchronization word that signals the start of the data field.

The splice occurs because the address word and the data field are recorded at different times and they are not synchronized. This causes random signal patterns at the actual location of the splice and phase differences between the two data fields. This means the data clock must be resynchronized during the data preamble.

3.8.4 Data Field - The Data Field contains 512 bytes. It is followed by the CRC which detects transcription errors. The CPU controller calculates a checkword during a write operation and appends it to the data field. It recalculates a checkword during a read operation and compares it to the recorded checkword to detect data errors.

3.8.5 Postamble - The Postamble contains the second splice and allows for "jitter" in the position of the sector pulse that marks the end of the sector.

3.9 MFM RECORDING

The disk drive uses the MFM encoding technique to record serial binary data on the disk. MFM encoded data can be recorded with very high bpi densities which increase the storage capacity of the disk. In addition, MFM allows the read circuits to use a clock, recovered directly from the data stream.

The timing diagram in Figure 3-14 shows the principal read/write waveforms for a particular binary data stream. The write circuits process the clock and binary data signals by producing MFM encoded data, which is recorded as "magnetic flux reversals" on the disk. The recorded signals contain a flux transition at the center of each binary one bit, and a flux transition between each pair of zero bits. (There is a delay of 1.5 clock times between the binary data stream and the recorded data as shown in the timing diagram. This occurs because the MFM encoder must process the data ahead of time to detect pairs of zeros.)

Each flux reversal induces a voltage in the read head. The resulting read signal looks somewhat like a sine wave with positive and negative peaks centered at the magnetic flux reversals. The read circuits produce a raw data stream that has a pulse centered on each peak of the sine wave read signal. The MFM decoder examines the relationship between the peaks and produces the binary data stream.

The MFM encoded waveform contains three different frequencies. A binary 101 pattern produces a flux reversal for every other bit. This is called 1F frequency and is half the data base rate. A 001 or 100 pattern causes a flux reversal every 1.5 bit time. This is called 1.33F frequency. Finally, an 11 or 000 pattern results in reversal for every bit. This corresponds to the 2F data rate. These three frequencies have a least common denominator of 4F, which is the read/write clock frequency.

Because the read circuits must recover a fixed clock, they use a PLL clock to produce their own 4F clock.

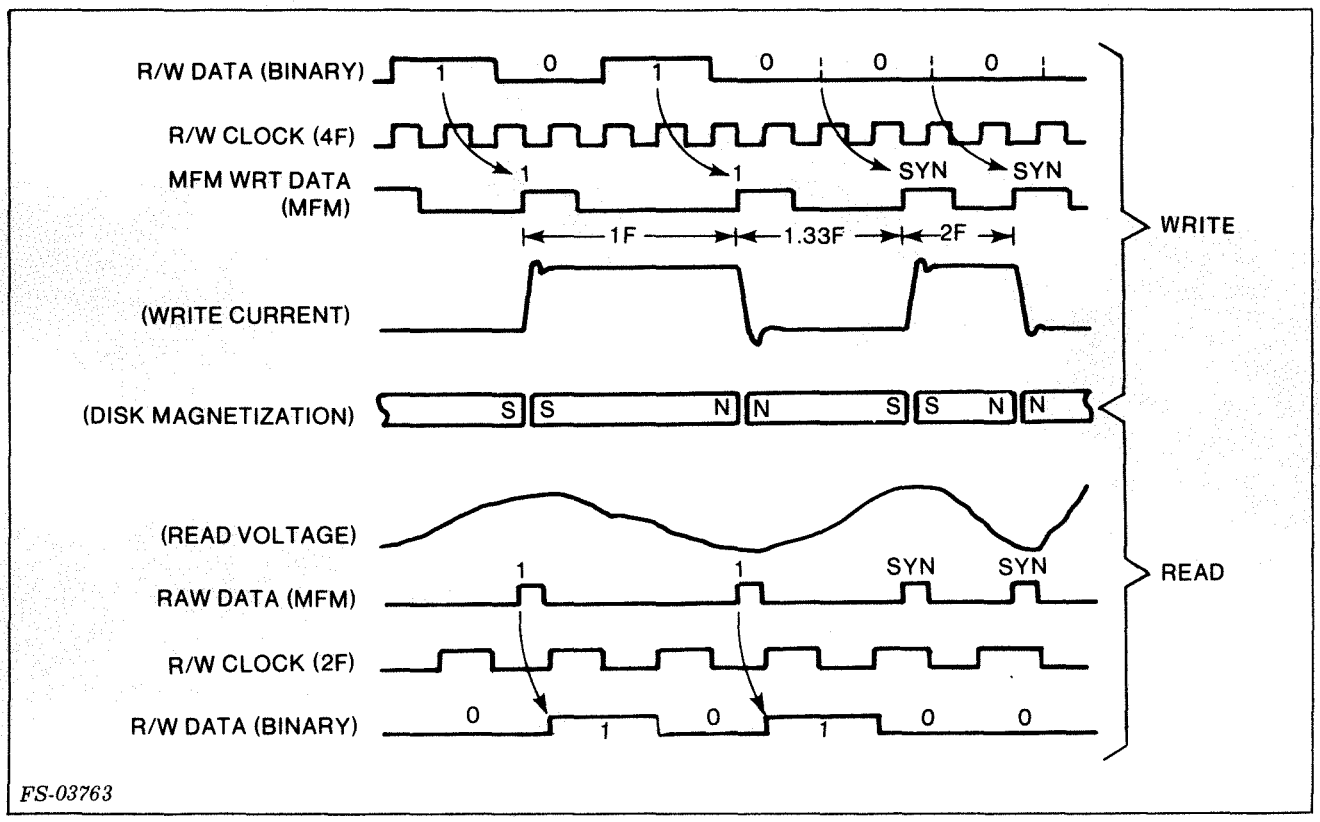


Figure 3-14. MFM Timing Diagram

3.10 RIGID DISK OPERATIONS

The rigid disk operations are:

- Seek
- Recalibrate
- Write
- Read

3.10.1 Seek Operation - A seek operation positions the drive read/write heads over the track that contains the data to be transferred to or from the CPU memory. The seek operation is set up by loading the command and disk address register with the seek command and the track address. On receipt of a start pulse from the CPU, the microprocessor on the CPU controller reads in the command, then reads in the new track address. The CPU controller microprocessor now has all the information required to step the home transducer to the new track. The microprocessor first checks that the new track address is valid, then calculates the difference between the current track address and the new track address. The microprocessor then activates the stepper motor to move the heads in or out to the specified track. In controlling the stepping motor, the microprocessor accelerates and decelerates the stepping motor to optimize seek times. When the operation is complete, the CPU controller microprocessor delays 15 milliseconds to allow the home transducer to settle, then it initiates a program interrupt request by setting the Done flag.

3.10.2 Recalibrate Operation - The recalibrate operation positions the drive read/write heads at cylinder zero. Recalibration is set up similar to a seek operation, except that the command and disk address registers are loaded with the recalibrate command with no specified track address.

In a recalibrate operation, the microprocessor uses the home transducer to locate track 0. To do this, the heads first move to the home position (track 192 or less). The stepping motor then steps back until reaching the phase position corresponding to track 0.

NOTE

If the drive is not accessed for two minutes, the microprocessor turns off the stepping motor.

3.10.3 Write Operation - Once the heads are in position, the drive is ready to accept a read or write command. A write command transfers blocks of data (512 bytes/block) from the CPU memory to the disk via the DCH.

To initiate a write operation, the CPU loads a write command, the head address, the starting sector address, and a number of sectors to be transferred into registers on the CPU controller. The starting memory address is also loaded to set up the transfer. The Busy flag is set to one when the pulse is received by the microprocessor to start the write operation.

For Model 6234, the microprocessor now starts a DCH operation to fill a buffer in the disk transfer logic with 512 bytes. Data words move from the CPU to the CPU controller via an internal I/O bus and are then stored in the sector buffer. When the buffer is full (512 bytes transferred), the microprocessor sets up the write transfer. It places first the current track address (from the preceding home transducer command), the head address, and the sector address into a register. When the selected sector approaches (i.e., the sector count from the drive is one less than the selected sector), the microprocessor starts the read/write operation.

The disk transfer logic first verifies that the address header is correct by comparing the address stored in the controller PCB to the word being read from the disk sector format. If an error is detected, the microprocessor sets the Done flag, and the operation terminates.

The disk transfer logic now performs the next operation which is to transfer the 512 bytes and develop a CRC. The logic first waits for a specified time after the correct address header is read (splice zone), then writes a preamble to be used by future read operations to sync the read data clock. The 512 byte transfer is then performed and written to the disk. During this transfer, the logic calculated a checkword and writes this checkword to the disk after a transfer. A postamble is then written to the disk to indicate to future read commands that the sector ended.

For Model 6234, up to 16 sectors may be written with one command sequence.

For Model 6280, operation is similiar to the Model 6234 with the following exceptions:

- Full sector buffer is not used and preloaded
- A 32-word FIFO transfers data during the operation
- Up to 64 sectors may be transferred with one command

3.10.4 Read Operation - A read operation transfers blocks of data from the disk to the CPU via the DCH. It is similar to a write operation except that the CPU controller registers are loaded with the read command and the DCH does not fill the buffer of the disk transfer logic. The read operation can read up to 16 sectors with one command.

The microprocessor first verifies that the address header is correct by comparing the address stored in the controller to the word read from the sector format on the disk. If an error is detected, the microprocessor sets the Done flag and the operation terminates.

Once the address header check is complete, the disk transfer logic adjusts the read clock to the input data stream of the data preamble. When the data preamble sync bit is detected, the disk transfer logic starts to transfer 512 bytes from the disk to the buffer. As this transfer takes place, a checkword is calculated through the CRC. When the 512 bytes transfer, the calculated checkword is compared to the checkword read from the disk. If they do not match, it is a CRC error.

For Model 6234, the microprocessor then starts a DCH operation. Data words flow from the buffer in the disk, through the controller to the CPU via the DCH. When all 512 bytes transfer, the Done flag sets which resets the Busy flag and generates a program interrupt request.

For Model 6280, operation is similiar to the Model 6234 with the following exceptions:

- Full sector buffer is not used and preloaded
- A 32-word FIFO transfers data during this operation
- Up to 64 sectors may be transferred with one command

SECTION 4

FAULT DIAGNOSIS

4.1 MODEL 6234/6280 INITIAL CHECKOUT

1. Prior to arriving on site, if possible, inquire about the problem and status of the host CPU and associated peripherals.

2. On site, verify that the CPU operates correctly. If not operating correctly, refer to the host CPU Maintenance Manual for the respective diagnostic information.

   Reference to the subsystem addresses are:

   - CA (cylinder address)
   - DA (disk address)
   - MA (memory address)
   - SA (starting address)

3. Power down the disk subsystem and the host CPU.

4. Remove the disk controller PCB from the CPU chassis (subsection 5.1) . Make sure that the correct jumpers are installed along with the correct device code. Replace the controller PCB.

5. Remove the top and bottom covers of the disk drive and the front panel see subsections 5.2 and 5.3. Make sure that the UNIT SELECT and WRITE PROTECT switches are in the correct positions as shown in Figure 4-1.

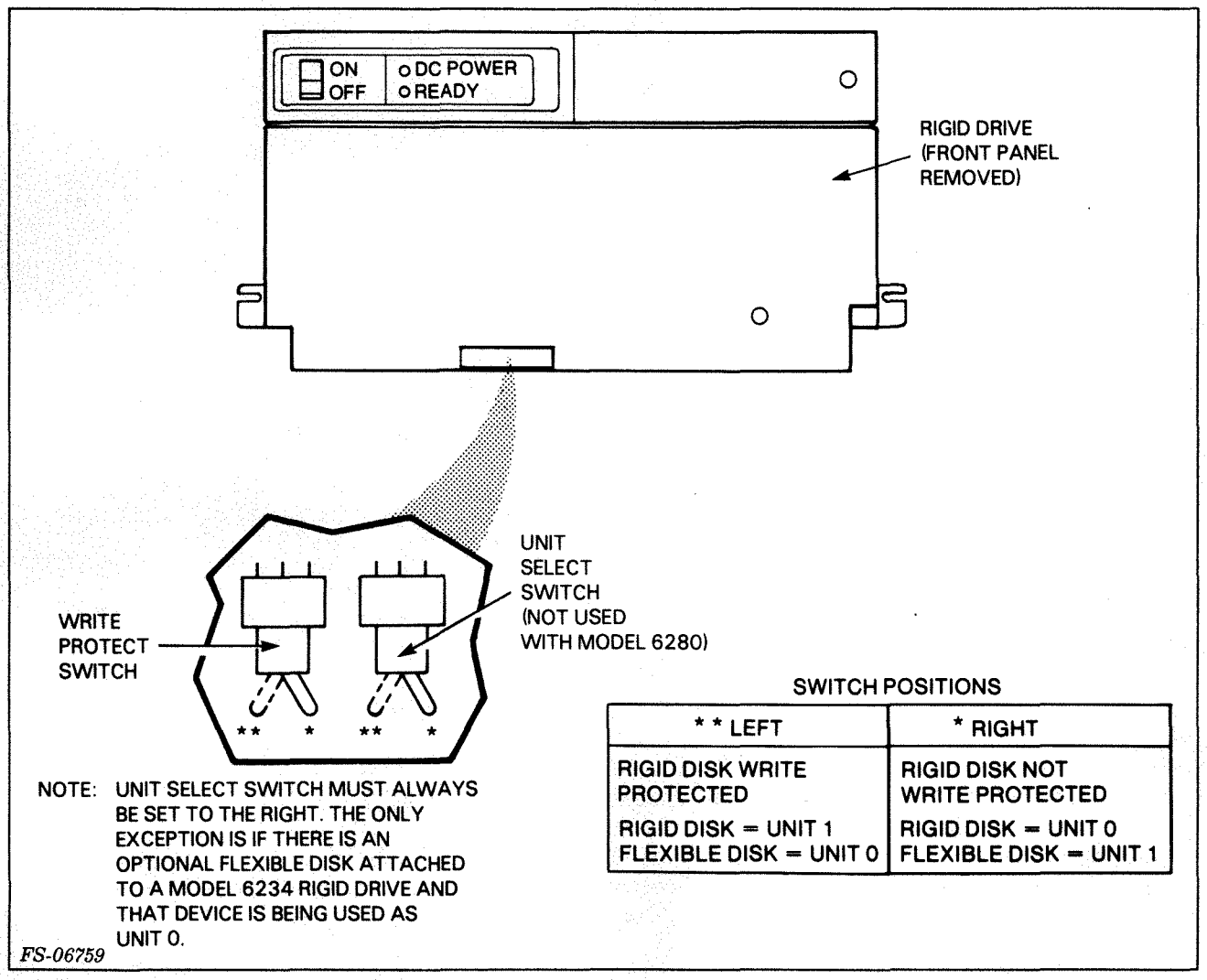
   Model 6234

   - With the UNIT SELECT switch pressed to the right, the drive is Unit 0. If the drive has an optional flexible disk drive, the flexible drive is Unit 1. With this switch pressed to the left, the drive is unit 1 and the flexible drive is unit 0. The normal switch position for the drive is to the right.

   Model 6280

   - The UNIT SELECT switch is always in the right hand position. The Model 6280 does not use this switch.

   - With the WRITE PROTECT switch pressed to the left, write operations cannot be performed on the drive. Press the switch to the right to perform write operations.



SWITCH POSITIONS

* * LEFT	* RIGHT
RIGID DISK WRITE PROTECTED RIGID DISK = UNIT 1 FLEXIBLE DISK = UNIT 0	RIGID DISK NOT WRITE PROTECTED RIGID DISK = UNIT 0 FLEXIBLE DISK = UNIT 1

Figure 4-1. UNIT SELECT and WRITE PROTECT Switches

6. Check the wire connections on the power switch. Verify the wire connections as shown in Figure 4-2.

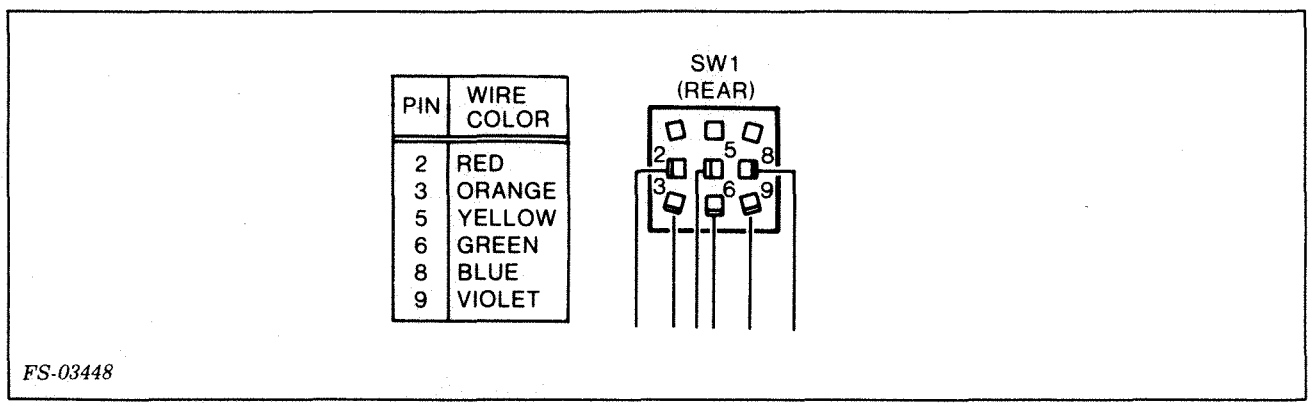


Figure 4-2. Power Switch Wire Connections

7. The power supply PCB in the disk drive has five LEDs. See Figure 4-3. When the power switch is ON, all five LEDs light. Table 4-1 lists the voltage requirements for the J1 connector on the power supply PCB.

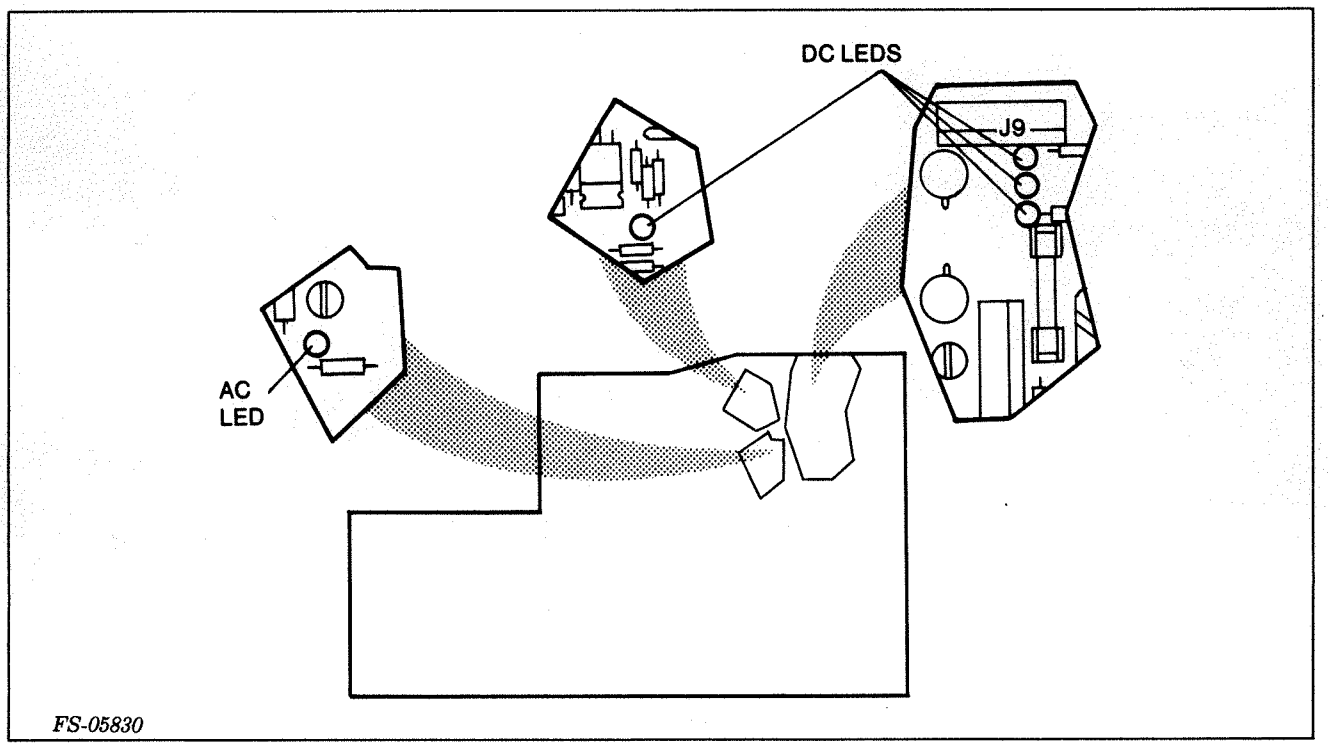


Figure 4-3. Power Supply PCB LED Locations

Table 4-1. Power Supply PCB Connector J1 Voltages

PIN	VOLTAGE
2	+ 5.0
4	- 5.0
3	-15.0
5	+15.0
6	+24.0

4.2 TROUBLESHOOTING FLOWCHARTS

For the procedures required to troubleshoot the 6234/6280 disk subsystems, use Figures 4-4 and 4-5 to begin the troubleshooting procedures. Figure 4-4 is the master flowchart and refers to Figures 4-6 through 4-21 for the necessary troubleshooting flow. Figure 4-5 provides cable information. When a flowchart specifies a FRU replacement, do the following:

1. Refer to Section 5 for detailed replacement procedures.

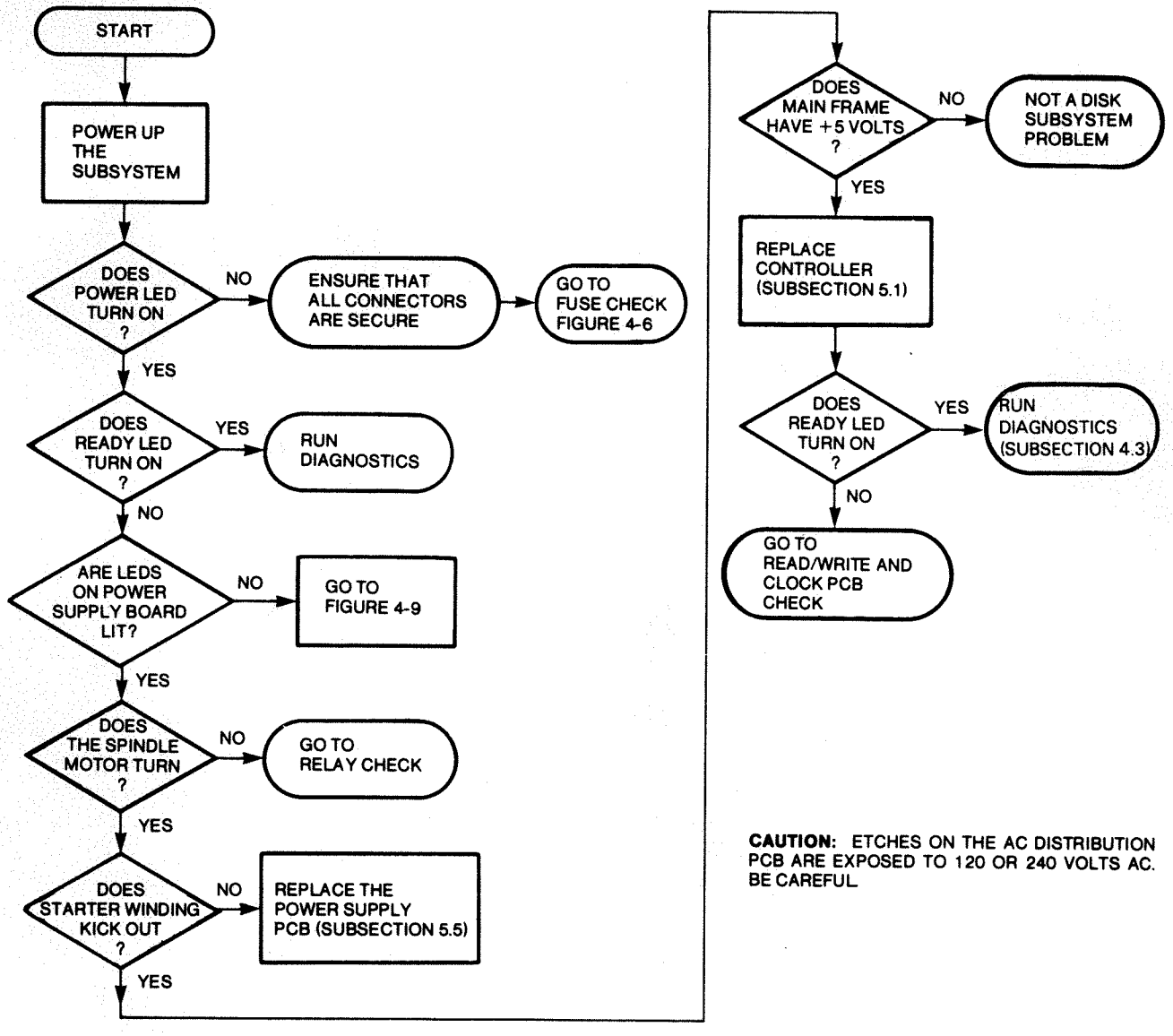


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Figure 4-4. Master Troubleshooting Flowchart for Model 6234/6280

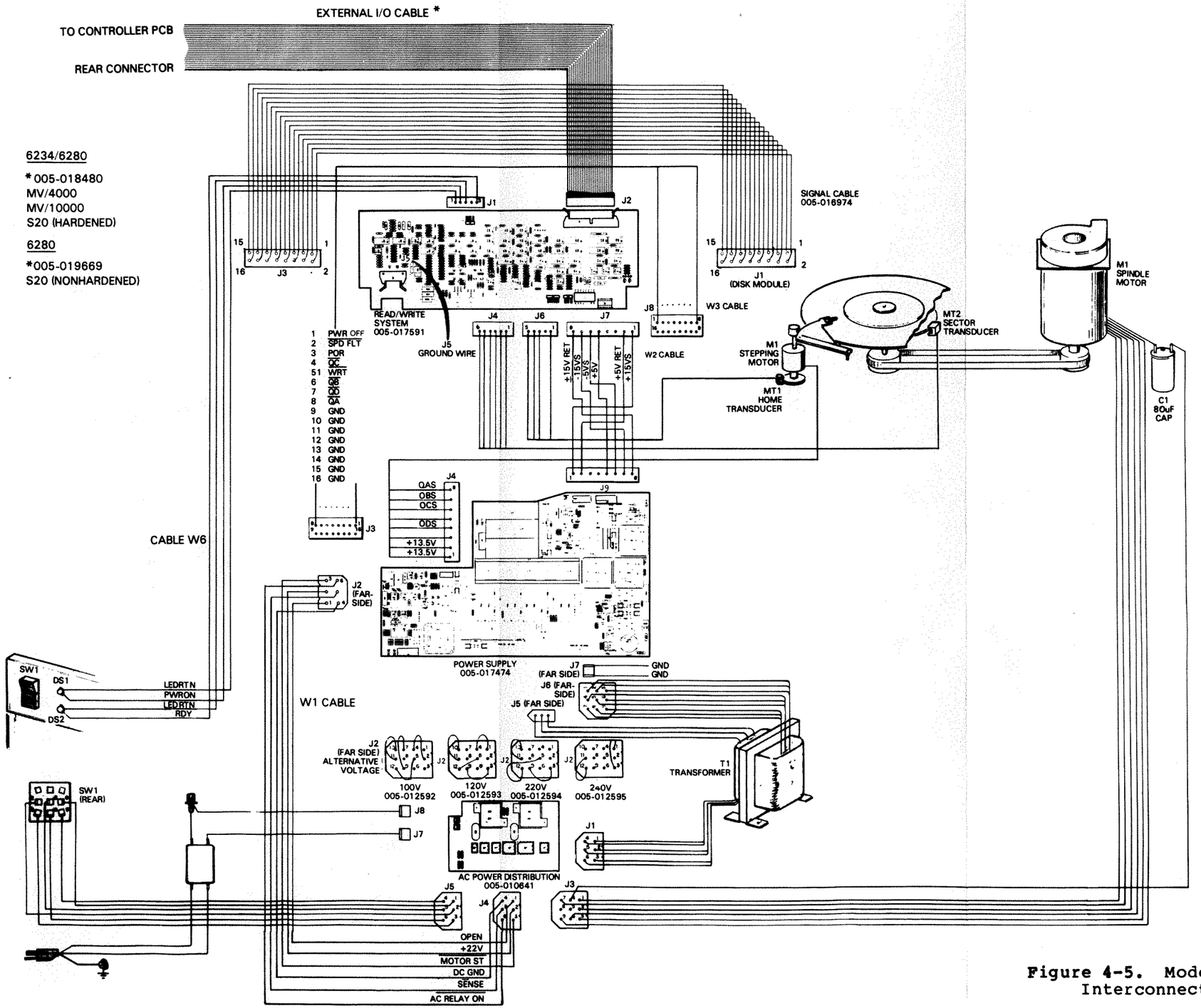

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Figure 4-5. Model 6234/6280 Interconnection Diagram

2. After replacing a FRU, try the subsystem again. If a different error condition occurs, return to Figure 4-4. If the error condition remains, reinstall the original FRU and perform the following steps. Then return to Figure 4-4.

3. Check all cables connected to the unit replaced. Refer to Figure 4-5, the Interconnection Diagram, and Tables 4-2 and 4-3. Use an ohmmeter to check the connecting cable ends for open lines. If a line on a cable is open, repair the cable by replacing the open wire. If the faulty cable is the signal cable connecting to J3 on the read/write and clock PCB, replace the entire cable as a ribbon cable cannot be repaired.

4. Check the dc voltages required by the drive. Table 4-1 lists the voltages for connector J9 on the power supply PCB (A4). The dc voltage on fuse F7 located next to J4 on the power supply PCB should read +16.0 Vdc.

5. Make sure the disk subsystem is properly configured with the system and operates under the correct environmental conditions. Refer to the installation specifications in Section 6 for environmental conditions.

Table 4-2. Model 6234 Disk Controller Cable (005-017587)
(Page 1 of 3)

SIGNAL NAME	BACK PLANE	PADDLE BOARD	DISK END (J2/P1)	DISK R/W
GND	A1	U	1	1
X POR	A47	17	34	2
GND	---	V	18	3
X PWR OFF	A49	18	2	4
GND	---	W	35	5
HOME	A79	19	19	6
GND	---	X	3	7
QD	A81	20	36	8
QC	A84	21	20	9
QB	A83	22	4	10
QA	A86	23	37	11
GND	---	a	21	12
HDSEL0	A85	24	5	13
HDSEL1	A88	25	38	14
HDSEL2	A87	26	22	15
GND	---	d	6	16

Table 4-2. Model 6234 Disk Controller Cable (005-017587)
(Page 2 of 3)

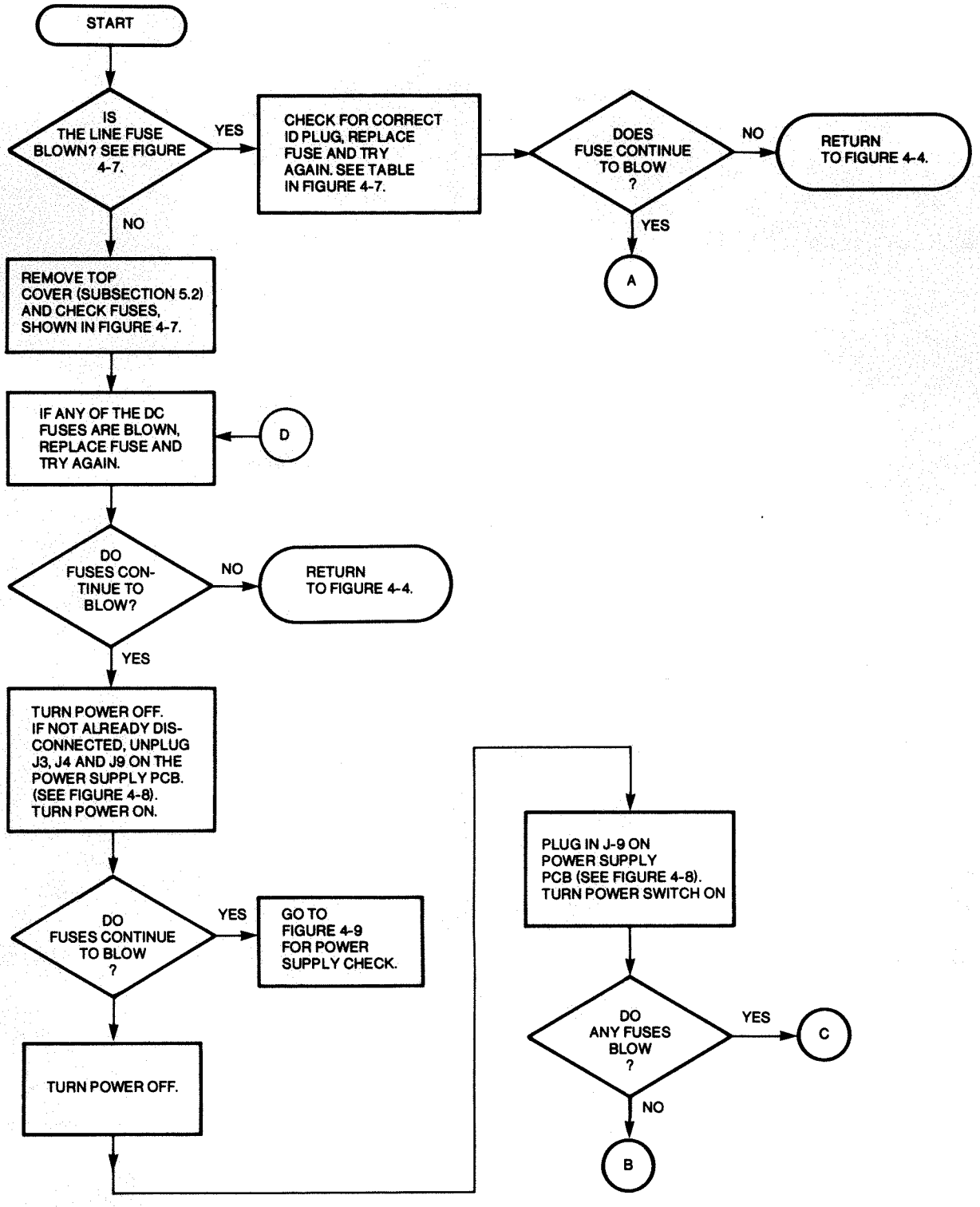
SIGNAL NAME	BACK PLANE	PADDLE BOARD	DISK END (J2/P1)	DISK R/W
$\overline{\text{RDGATE}}$	A89	27	39	17
GND	---	e	23	18
$\overline{\text{WRTGATE}}$	A90	28	7	19
GND	---	f	40	20
$\overline{\text{PREAMBLE}}$	B6	29	24	21
GND	---	h	8	22
XSC4	B11	30	41	23
XSC3	B13	31	25	24
XSC2	B15	32	9	25
XSC1	B19	33	42	26
XSC0	B23	34	26	27
GND	---	n	10	28
$\overline{\text{XSCTRPLS}}$	B25	35	43	29
GND	---	p	27	30
XSCNTVALID	B27	36	11	31
$\overline{\text{XSC5}}$	B31	37	28	33
$\overline{\text{WRTPRO}}$	B69	49	12	34
$\overline{\text{HDSEL3}}$	B34	38	45	35
GND	---	s	29	36
DRVFLT	B36	39	13	37
SPARE	B38	40	46	38
GND	---	t	30	39
DISCLK+	B40	41	14	40
DISCLK-	B48	42	47	41
GND	---	w	31	42
$\overline{\text{RDY}}$	B49	43	15	43
$\overline{\text{SWAP}}$	B51	44	48	44

Table 4-2. Model 6234 Disk Controller Cable (005-017587)
(Page 3 of 3)

SIGNAL NAME	BACK PLANE	PADDLE BOARD	DISK END (J2/P1)	DISK R/W
GND	---	x	32	45
DAT-	B52	45	16	46
DAT+	B53	46	49	47
GND	---	AB	33	48
CLK-	B54	47	17	49
CLK+	B67	48	50	50
+DRAIN	---	AD	---	Shell

Table 4-3. Model 6280 Disk Controller Cable (005-019669)

SIGNAL NAME	RIGID DISK SOCKET CONNECTOR 50 PIN P1	I/O CABLE P2 CONNECTOR PIN	I/O CABLE PCB EDGE PIN
GND	1	1	1
XPOR	34	A	2
GND	18	2	3
X PWR OFF	2	B	4
GND	35	3	5
HOME	19	C	6
GND	3	4	7
QD	36	D	8
QC	20	5	9
QB	4	E	10
QA	37	6	11
GND	21	F	12
HDSEL0	5	7	13
HDSEL1	38	H	14
HDSEL2	22	8	15
GND	6	J	16
RDGATE	39	9	17
GND	23	K	18
WRGATE	7	10	19
GND	40	L	20
PREAMBLE	24	11	21
GND	8	M	22
XSC4	41	12	23
XSC3	25	N	24
XSC2	9	13	25
XSC1	42	P	26
XSC0	26	14	27
GND	10	R	28
XSCTR PLS	43	15	29
GND	27	S	30
XSCNTVALID	11	16	31
GND	44	T	32
XSC5	28	17	33
WRT PRO	12	U	34
HDSEL3	45	18	35
GND	29	V	36
DRV FLT	13	19	37
SPARE	46	W	38
GND	30	20	39
DIS CLK+	14	X	40
DIS CLK-	47	21	41
GND	31	Y	42
RDY	15	22	43
SWAP	48	Z	44
GND	32	23	45
DAT-	16	a	46
DAT+	49	24	47
GND	33	b	48
CLK-	17	25	49
CLK+	50	c	50
+DRAIN	SHELL	NC	NC



NOTE: BEFORE STARTING, MEASURE ALL VOLTAGES. USE FIGURE 4-10.

FS-05833

Figure 4-6. Fuse Check Flowchart (1 of 3)

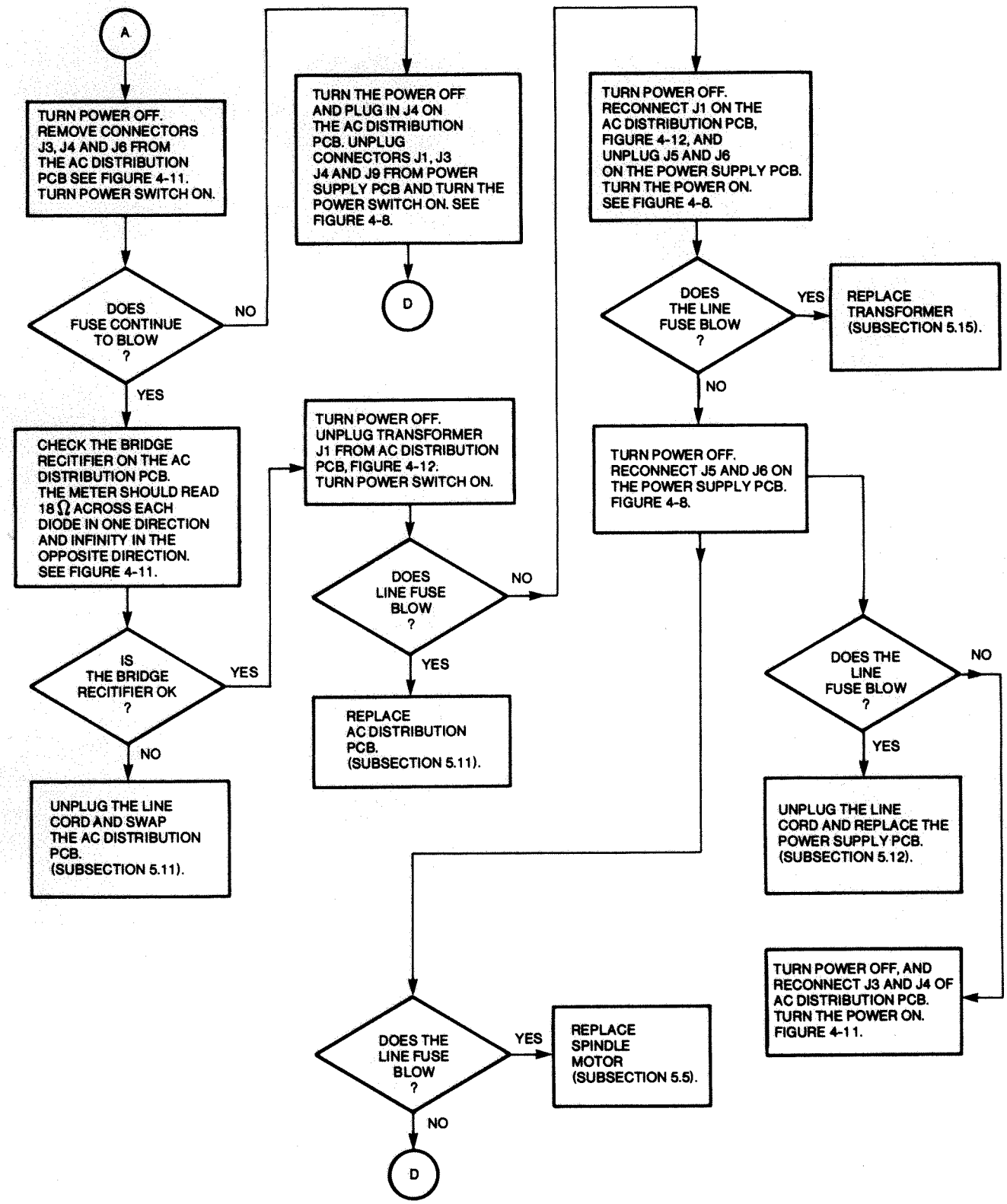


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Figure 4-6. Fuse Check Flowchart (2 of 3)

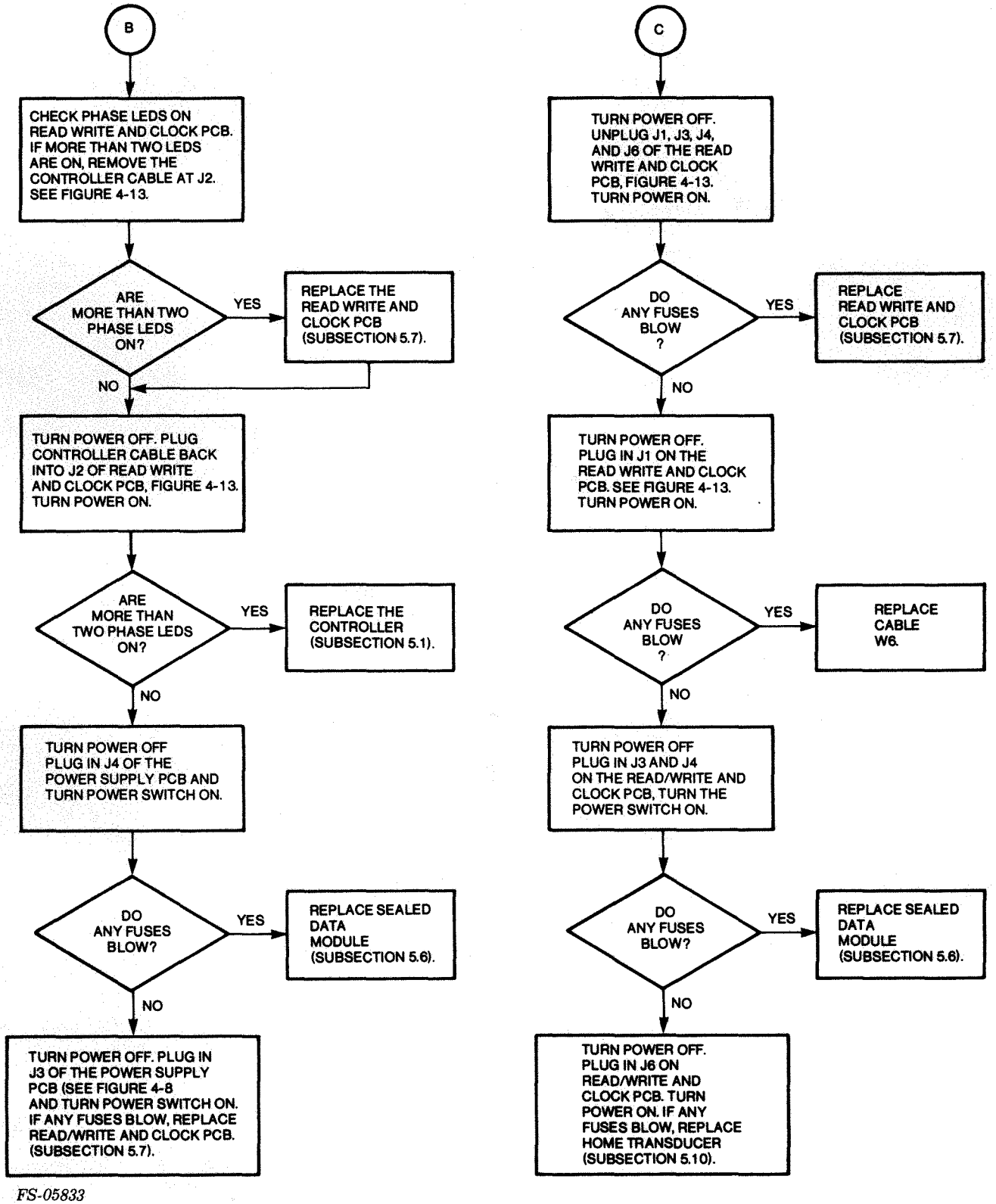

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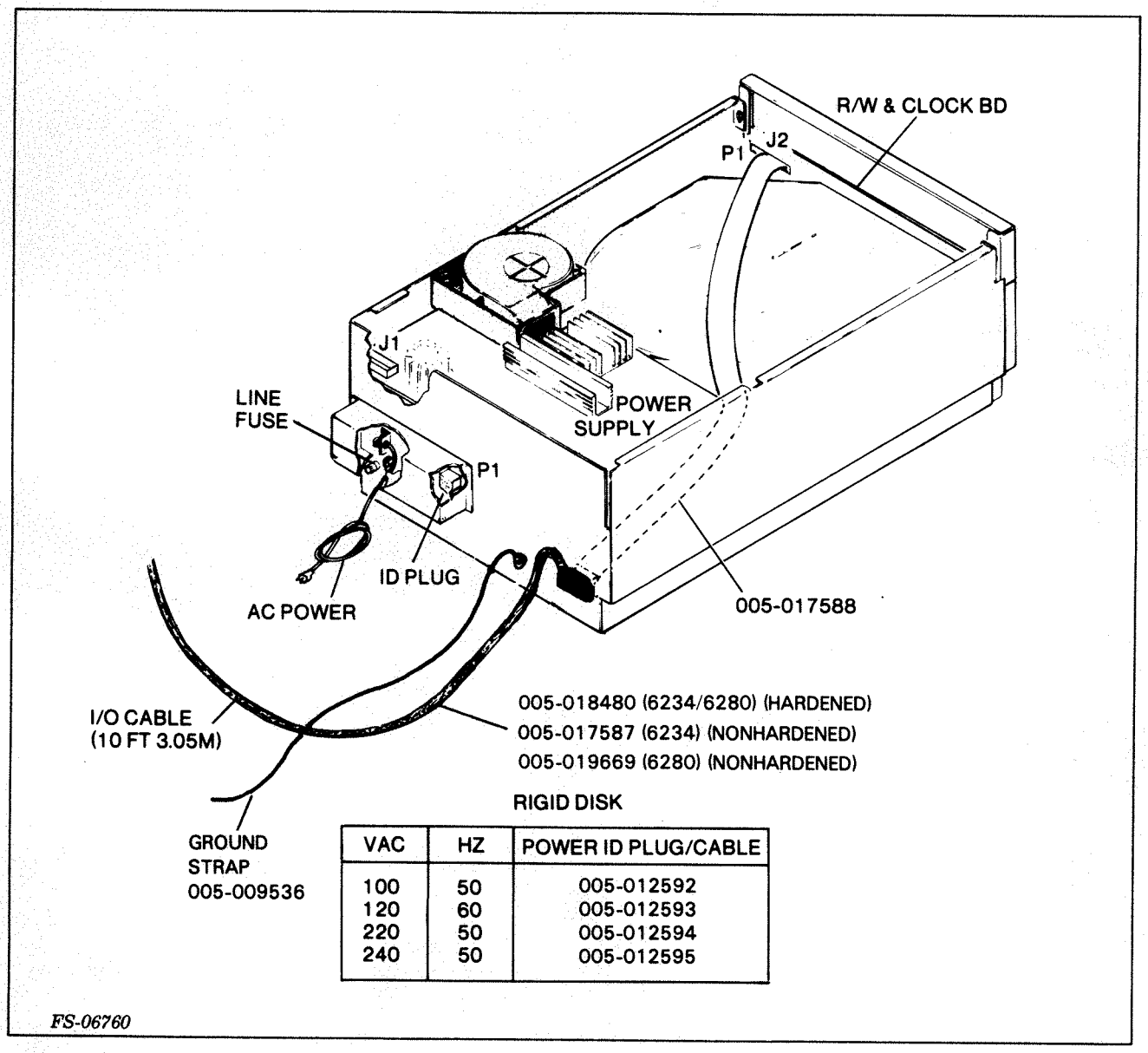
Figure 4-6. Fuse Check Flowchart (3 of 3)



VAC	HZ	POWER ID PLUG/CABLE
100	50	005-012592
120	60	005-012593
220	50	005-012594
240	50	005-012595

Figure 4-7. Cable and Power Identification

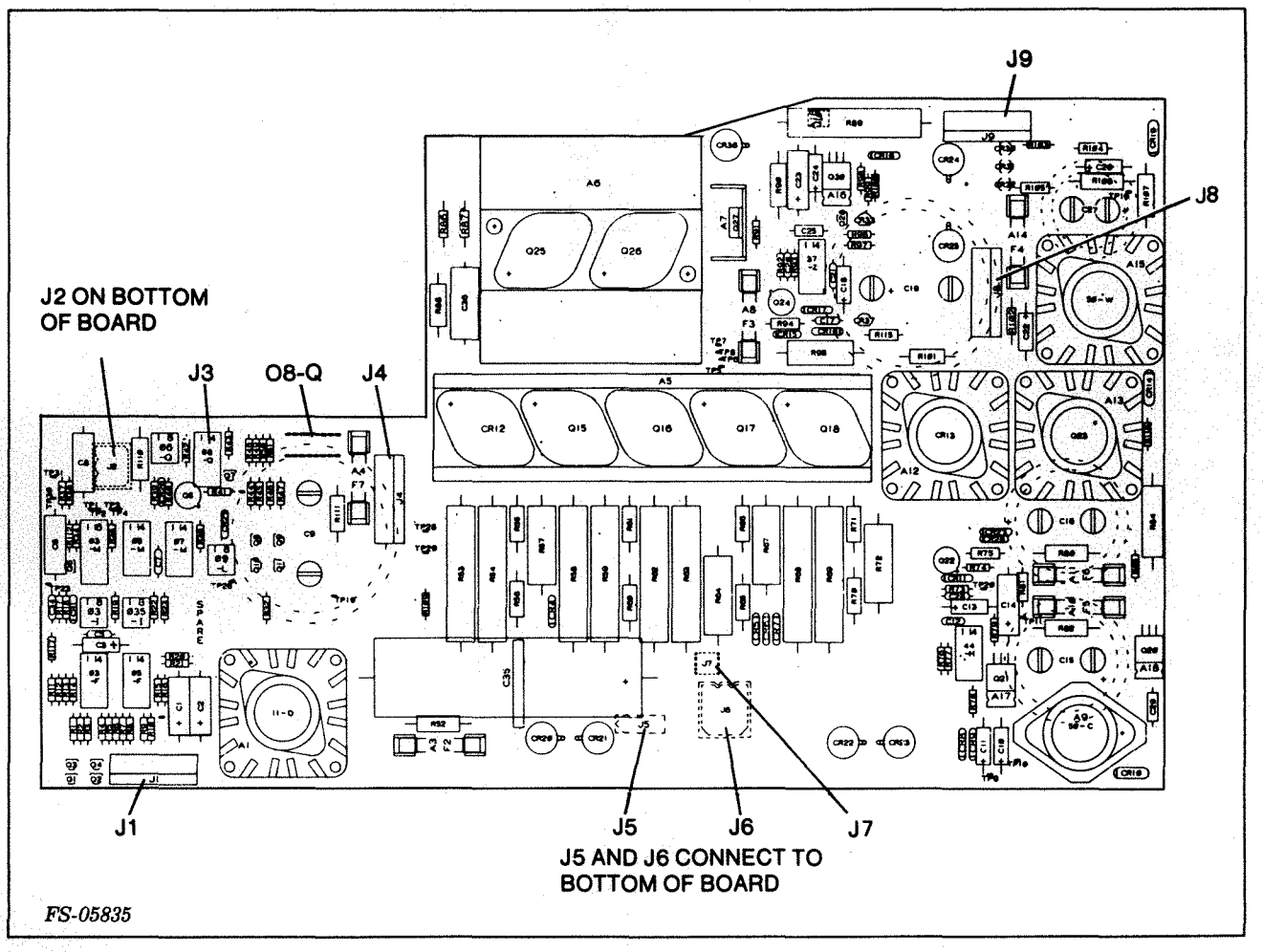


Figure 4-8. Power Supply PCB Connectors

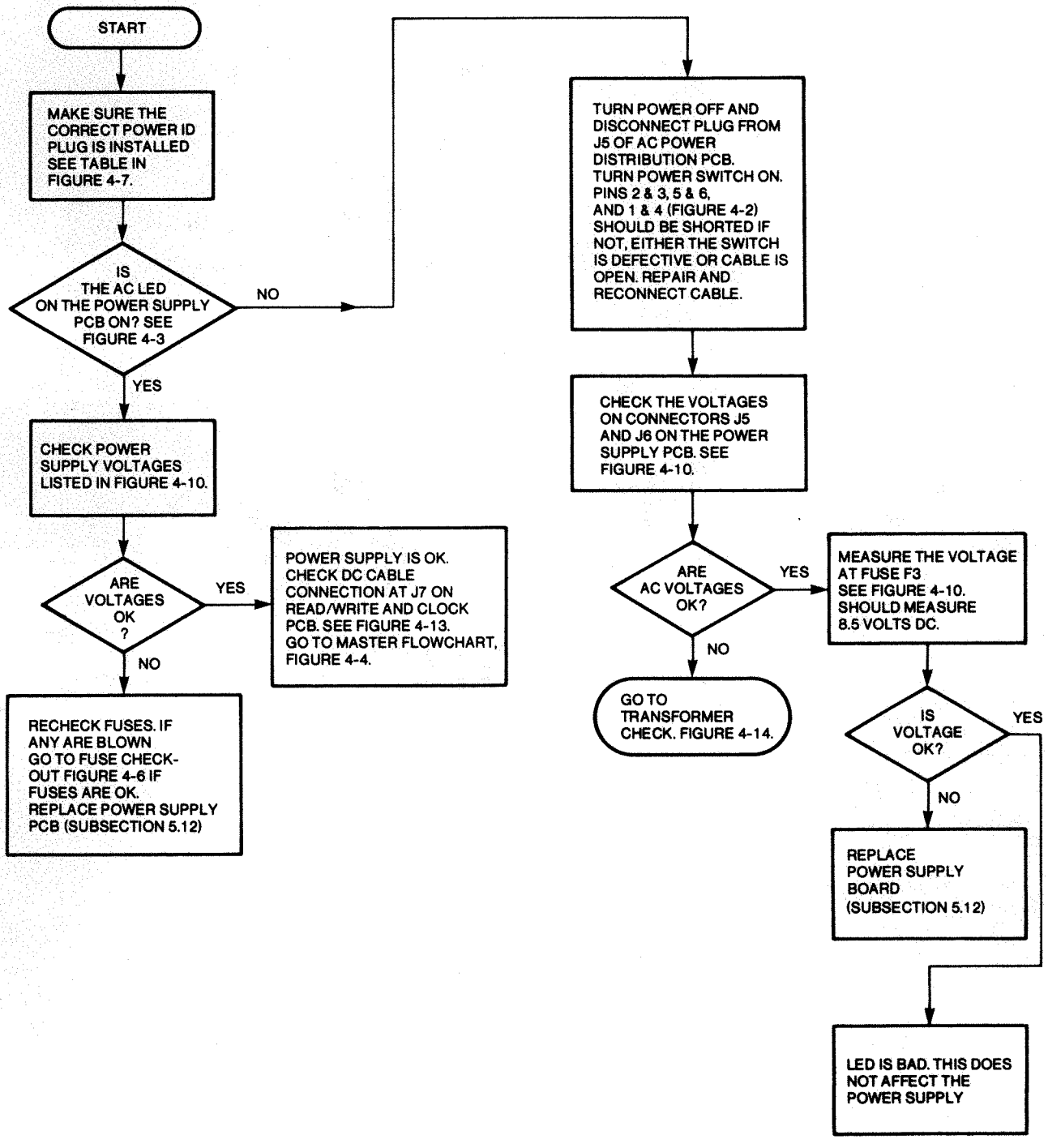


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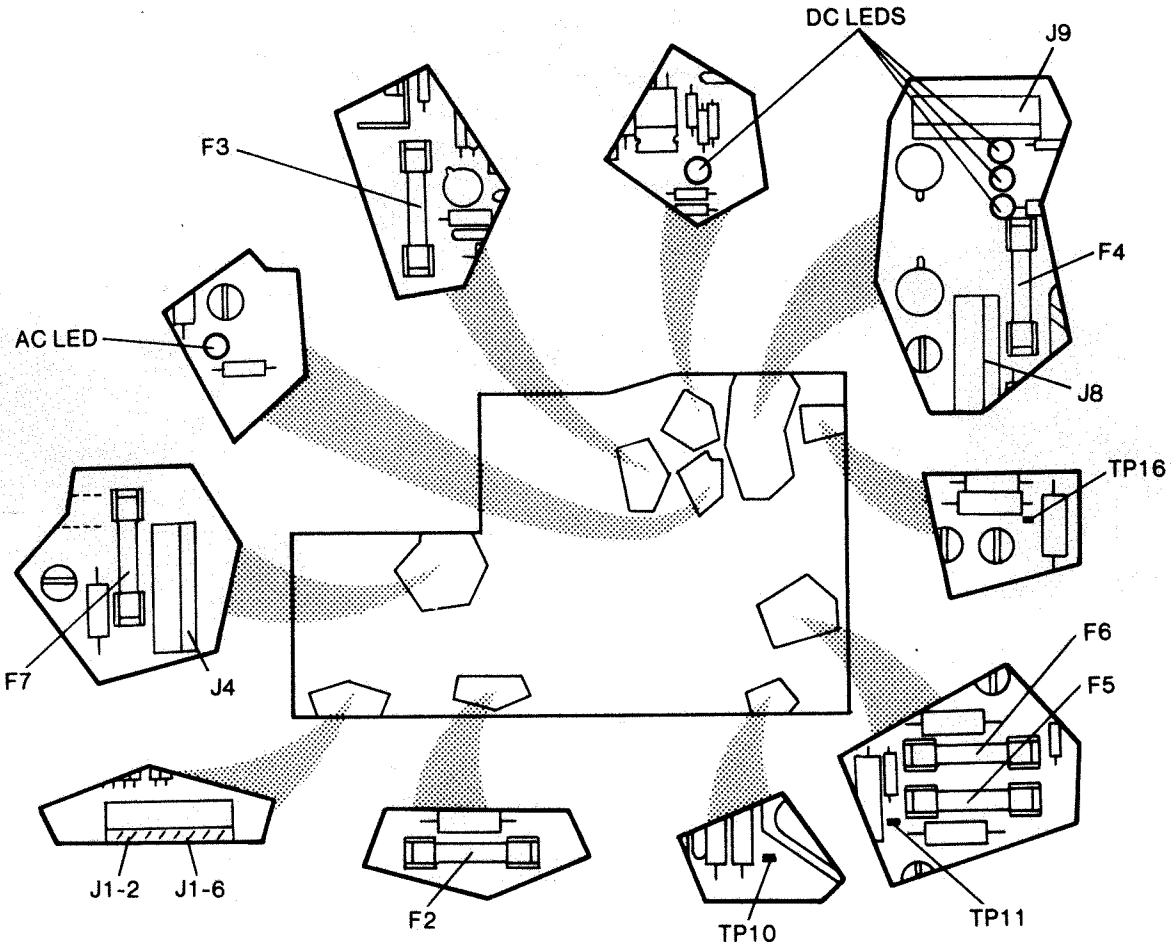
Figure 4-9. Power Supply PCB Check Flowchart



FUSES

		TYPE	PART NUMBER
120 VAC	F1	7A SLO BLO	113-175
220 VAC	F1	4A SLO BLO	113-177
	F2	1.5A	113-176
	F3	10A	113-054
	F4	2A	113-041
	F5	.5A	113-061
	F6	1.5A	113-176
	F7	5A SLO BLO	113-047

VOLTAGE CHECKS

-5V ON TP-16	MIN. -4.75	MAX. -5.25
5V ON J1-2	MIN. 4.9	MAX. 5.25
-15V ON TP-10	MIN.-14.25	MAX. -15.75
15V ON TP-11	MIN. 14.55	MAX. 15.45
24V ON J1-6	MIN. 22.8	MAX. 25.2
16V ON F7	MIN. 13.5	MAX. 23.1

NOTE: FUSE F1 LOCATED ON REAR OF DRIVE

ID PLUG

6101/6104
6098/6100

VAC	HZ	DGC
100	50	005-12592
120	60	005-12593
220	50	005-12594
240	50	005-12595

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Figure 4-10. Power Supply PCB Voltage Checks

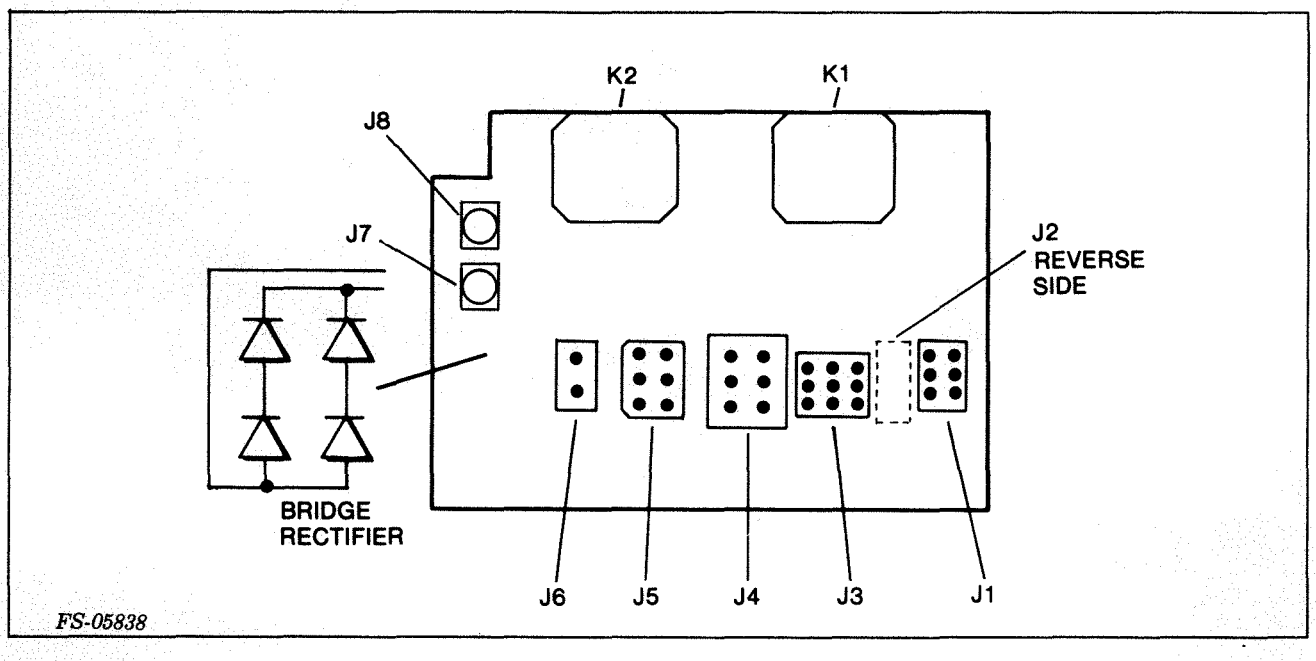

Figure 4-11. AC Distribution PCB

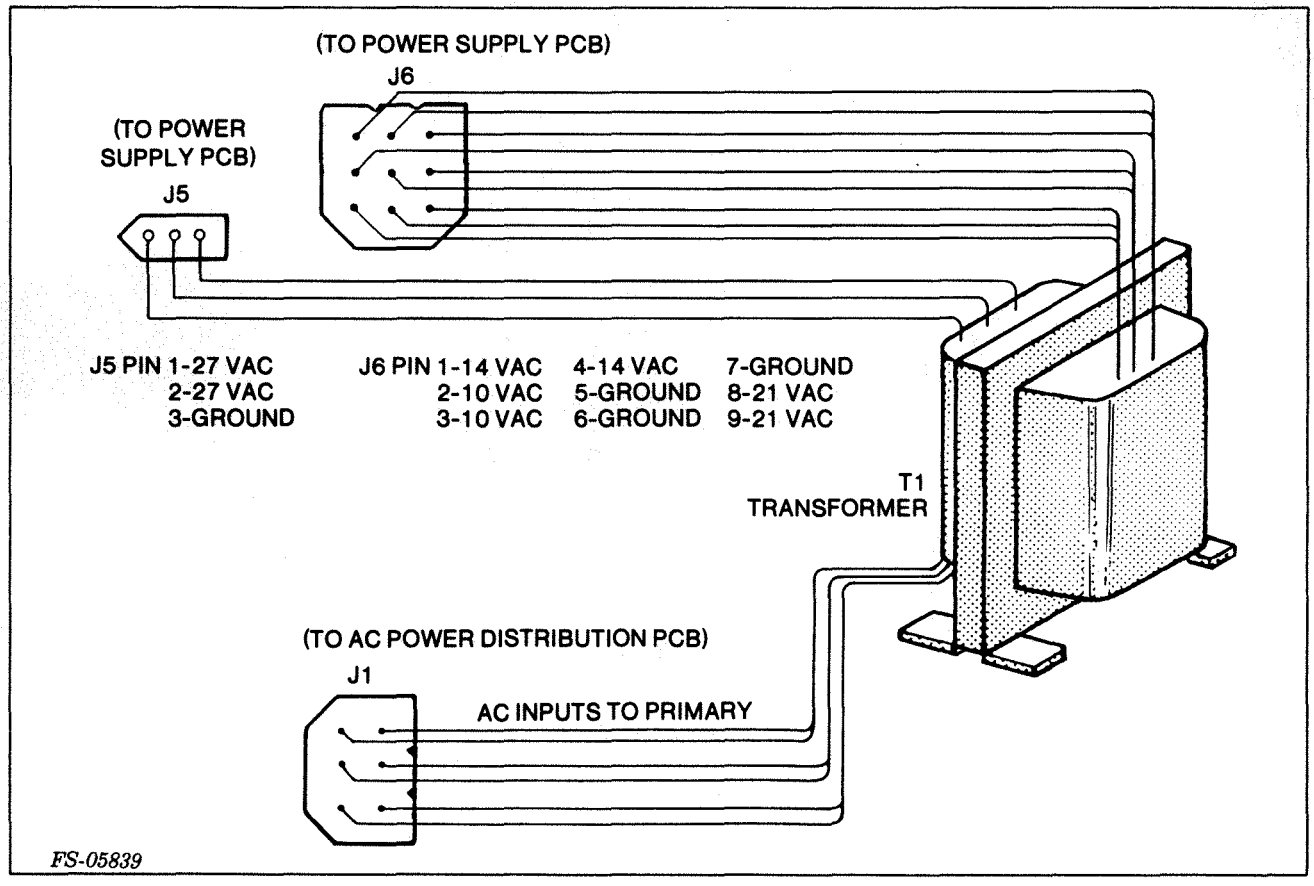

Figure 4-12. Power Transformer T1 Connectors

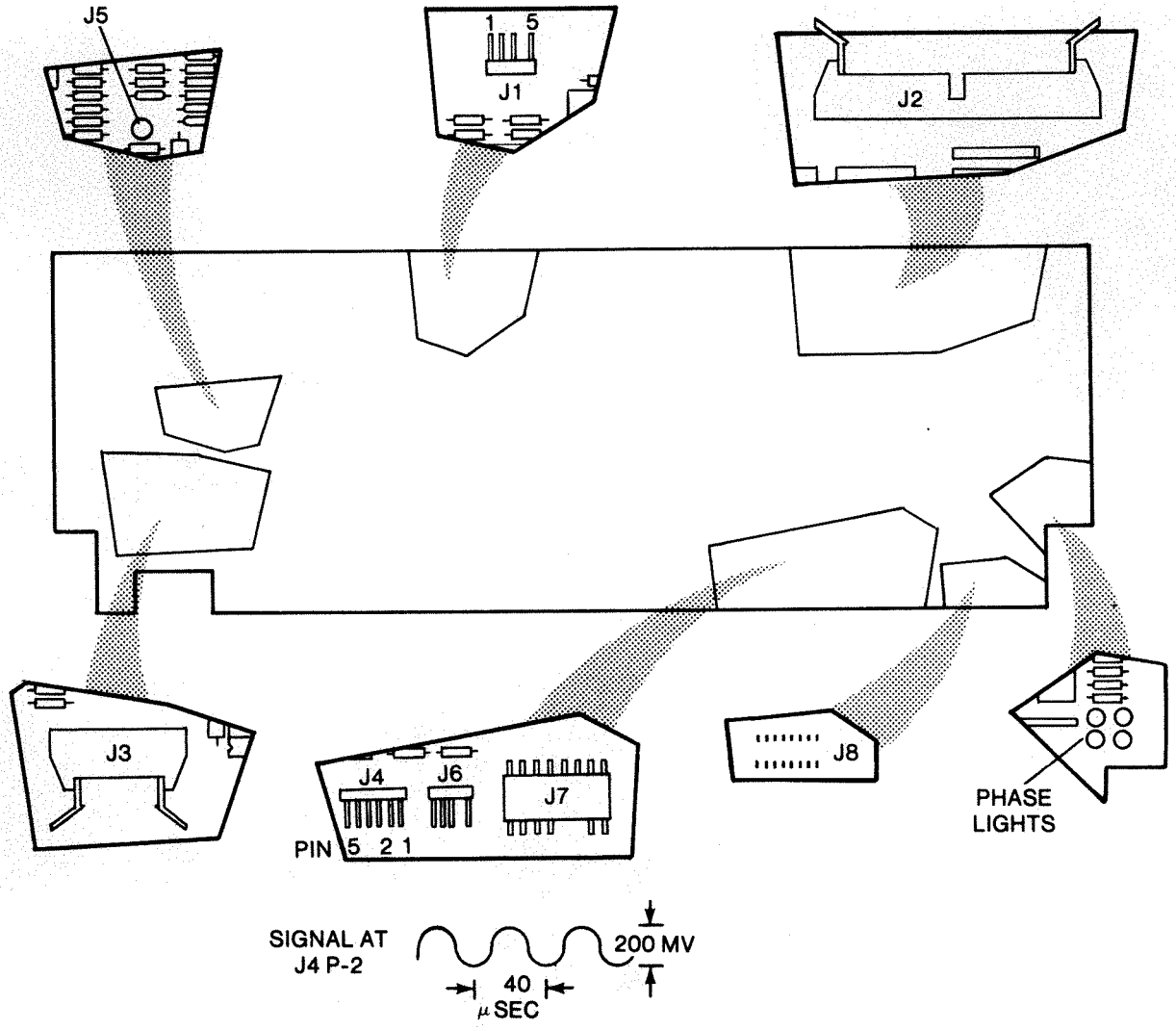

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Figure 4-13. Read/Write and Clock PCB Connectors

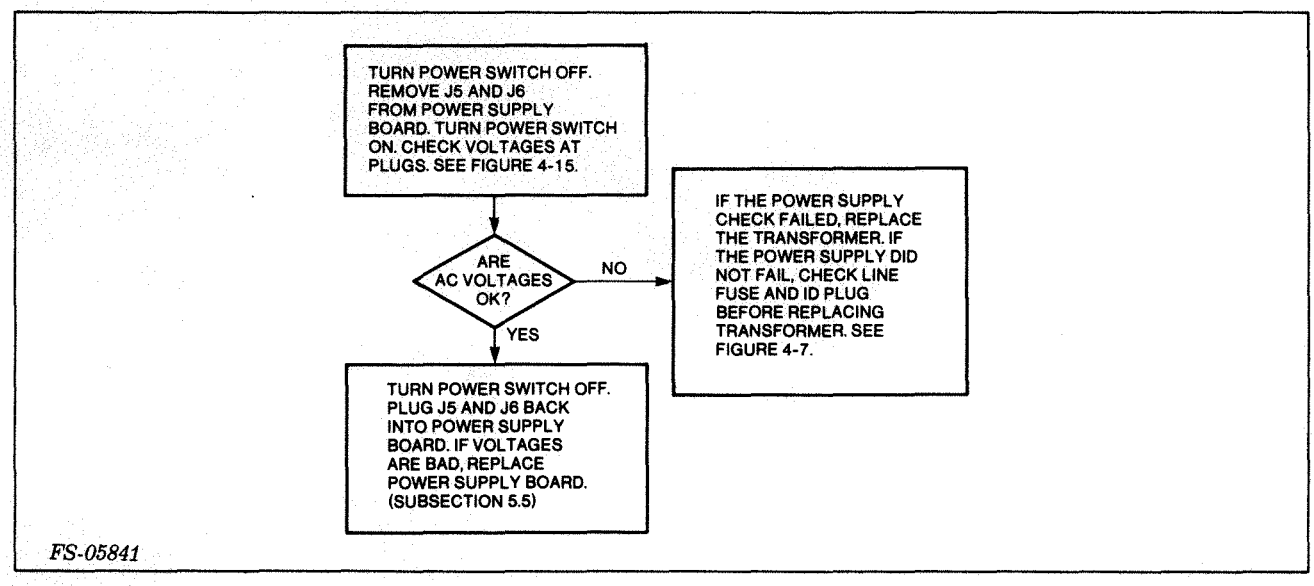

Figure 4-14. Transformer Check Flowchart

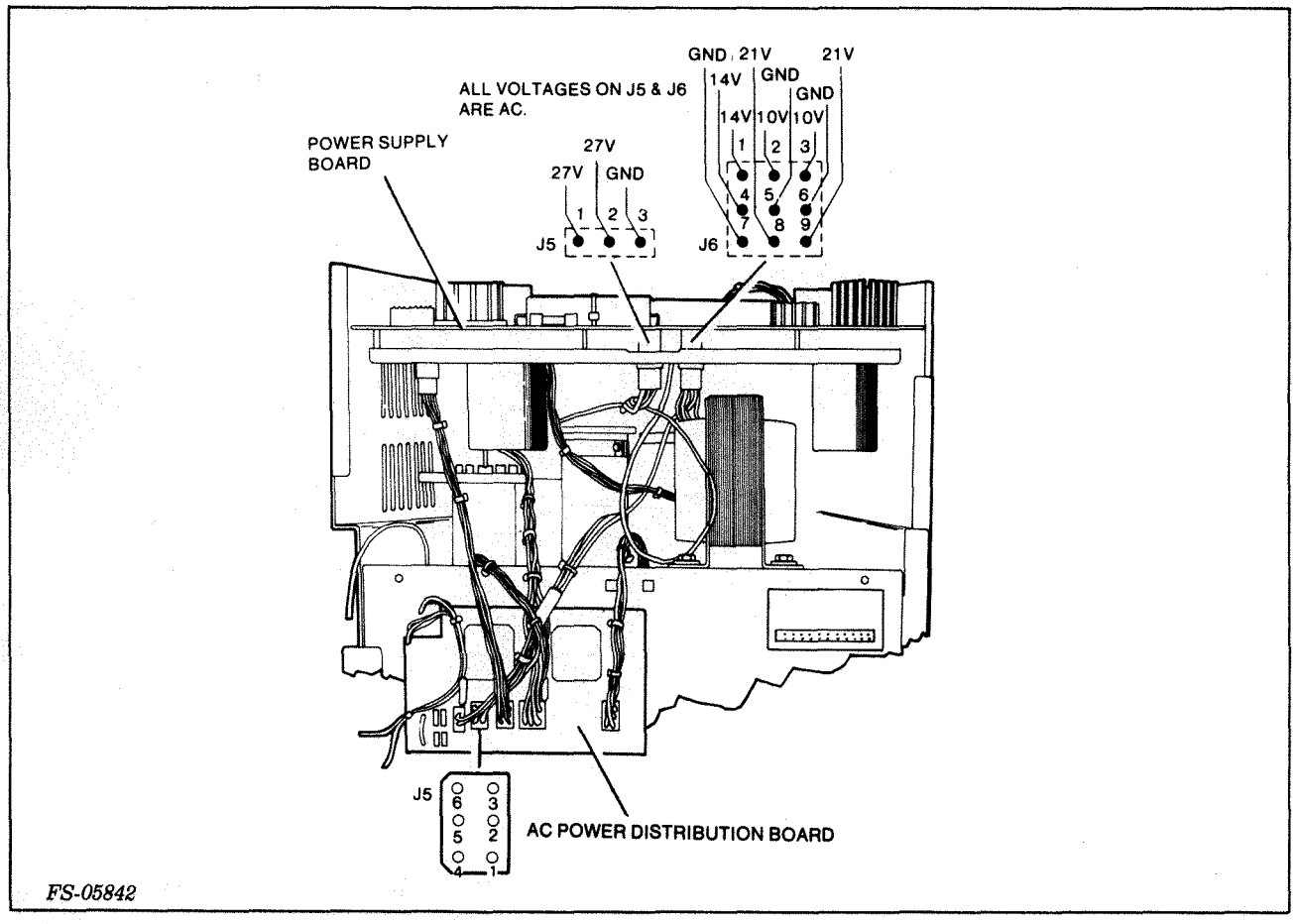

Figure 4-15. Voltage Checks on J5 and J6 Power Supply PCB

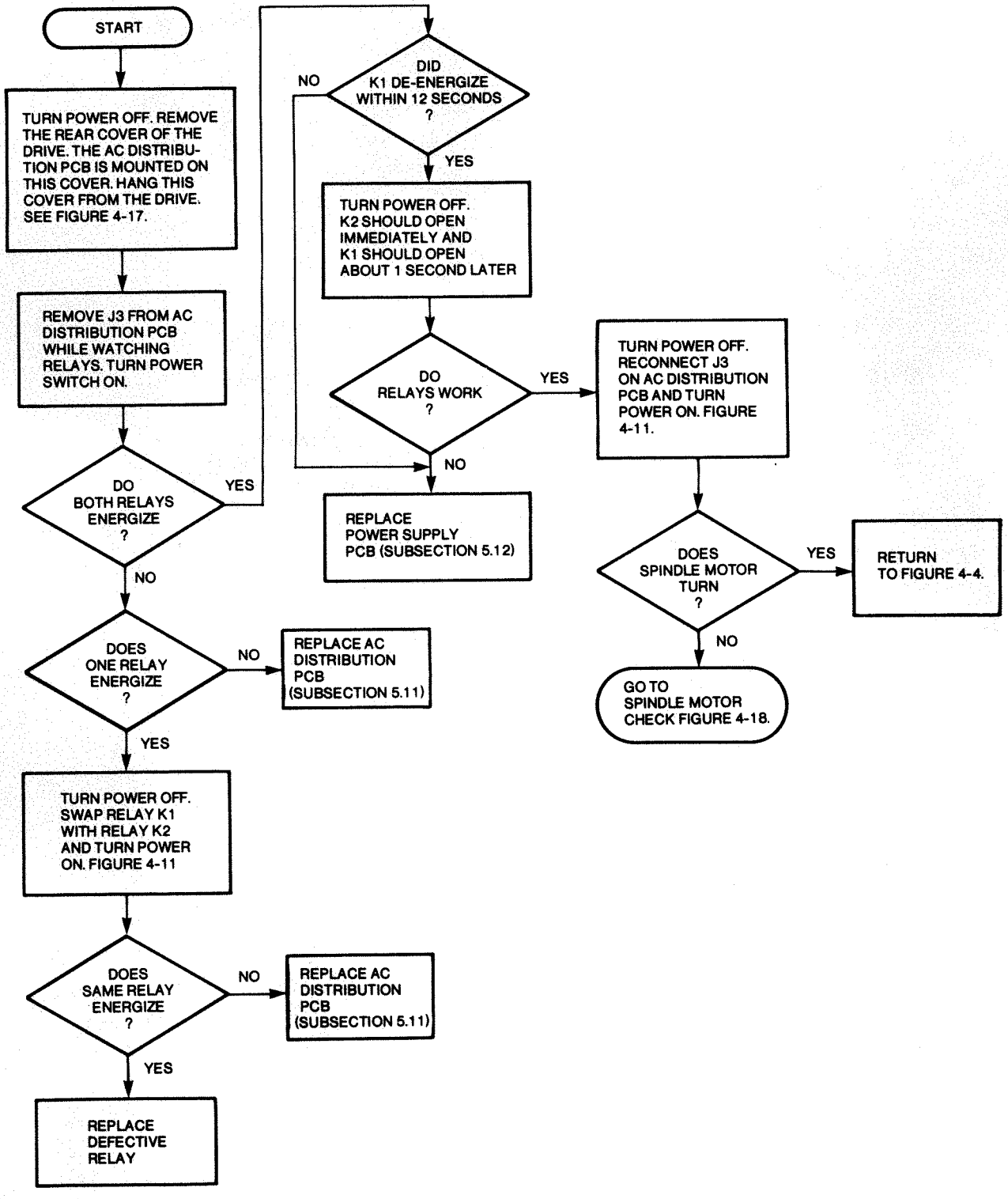

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Figure 4-16. Relay Check Troubleshooting Flowchart

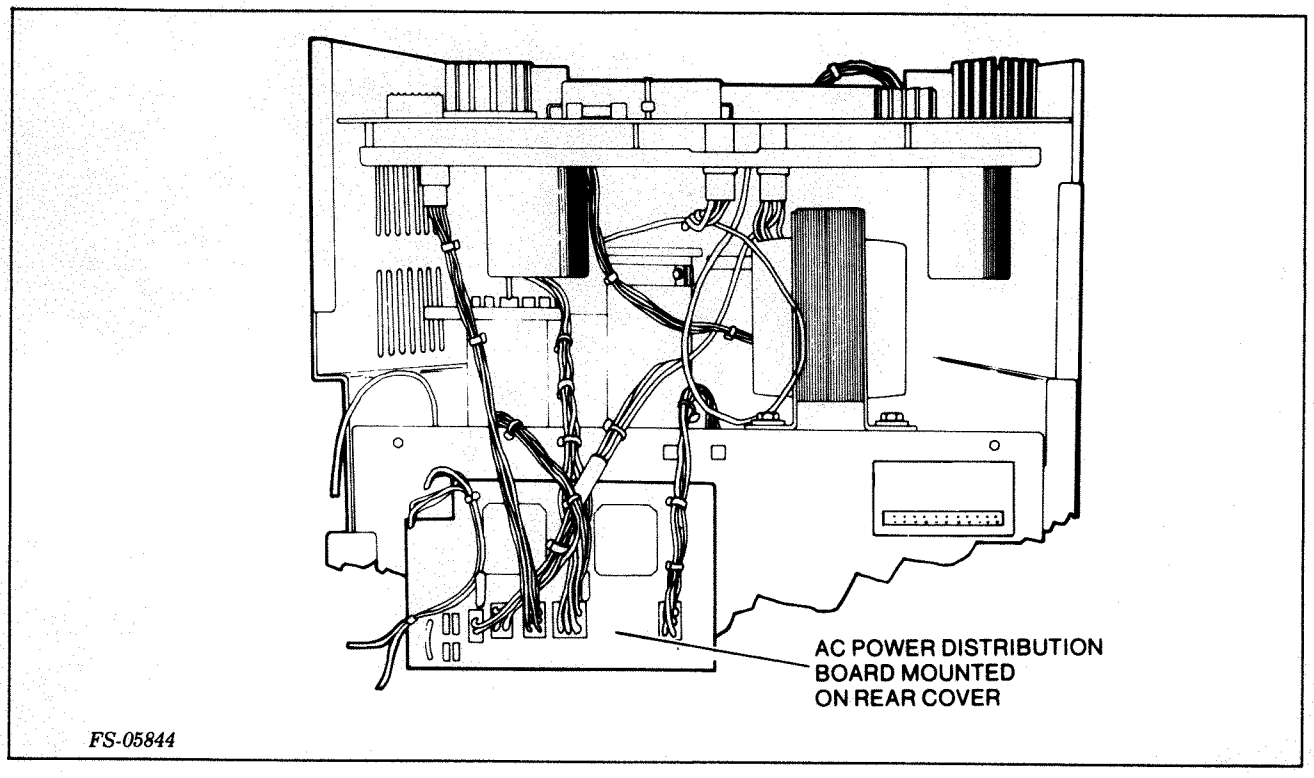

Figure 4-17. AC Power Distribution PCB Mounted on Rear Cover

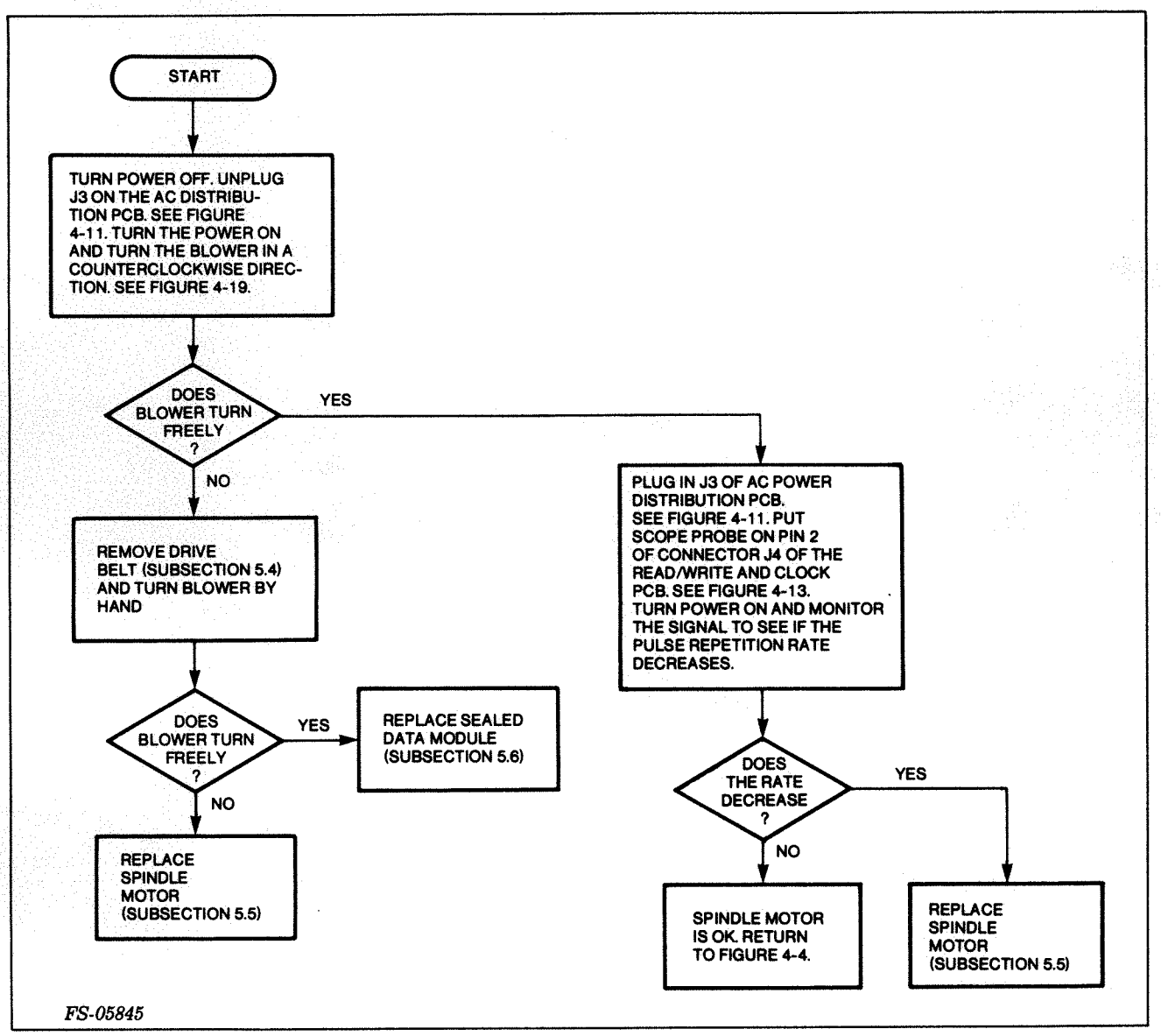

Figure 4-18. Spindle Motor Check Flowchart

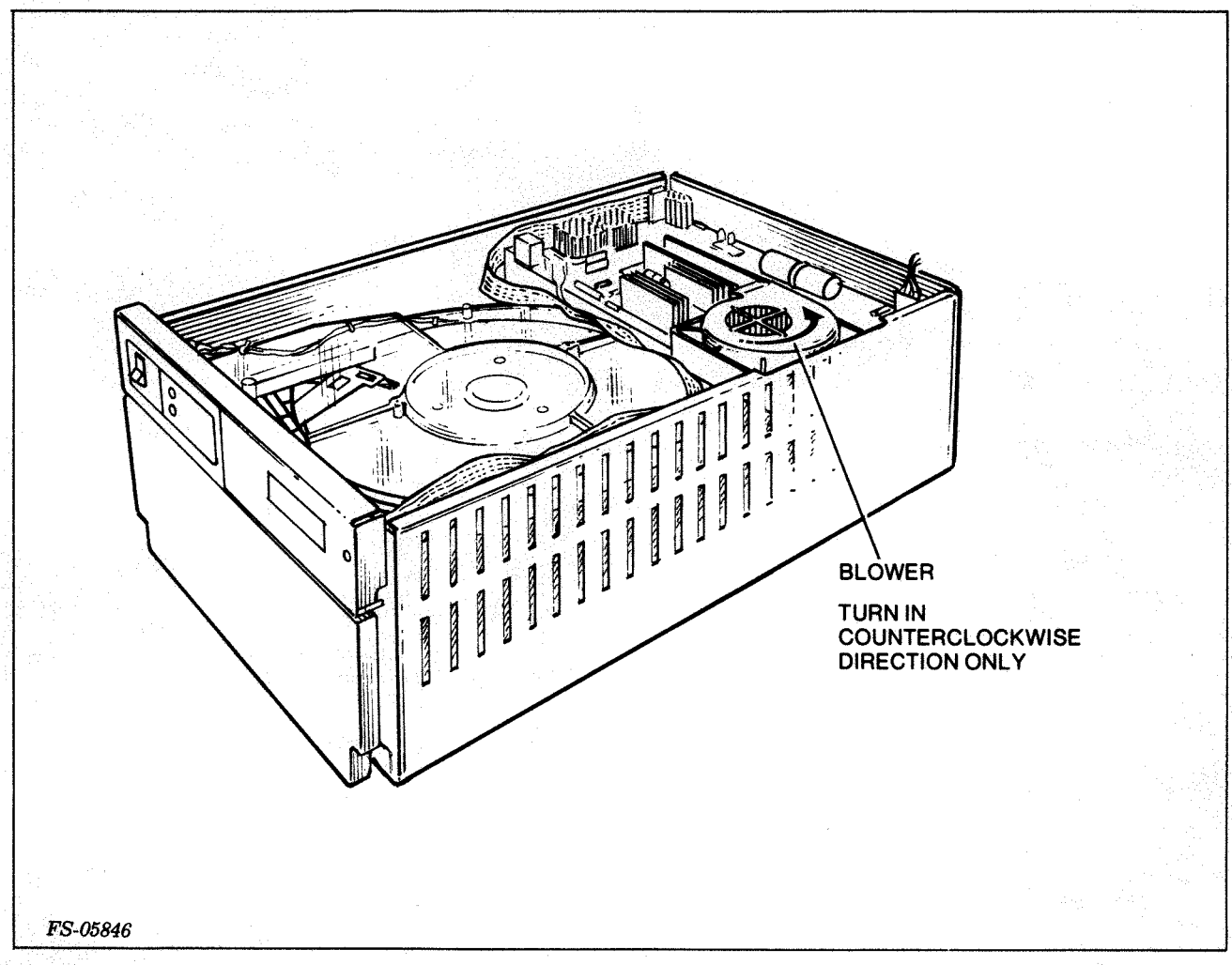

Figure 4-19. Rigid Drive, Cover Removed

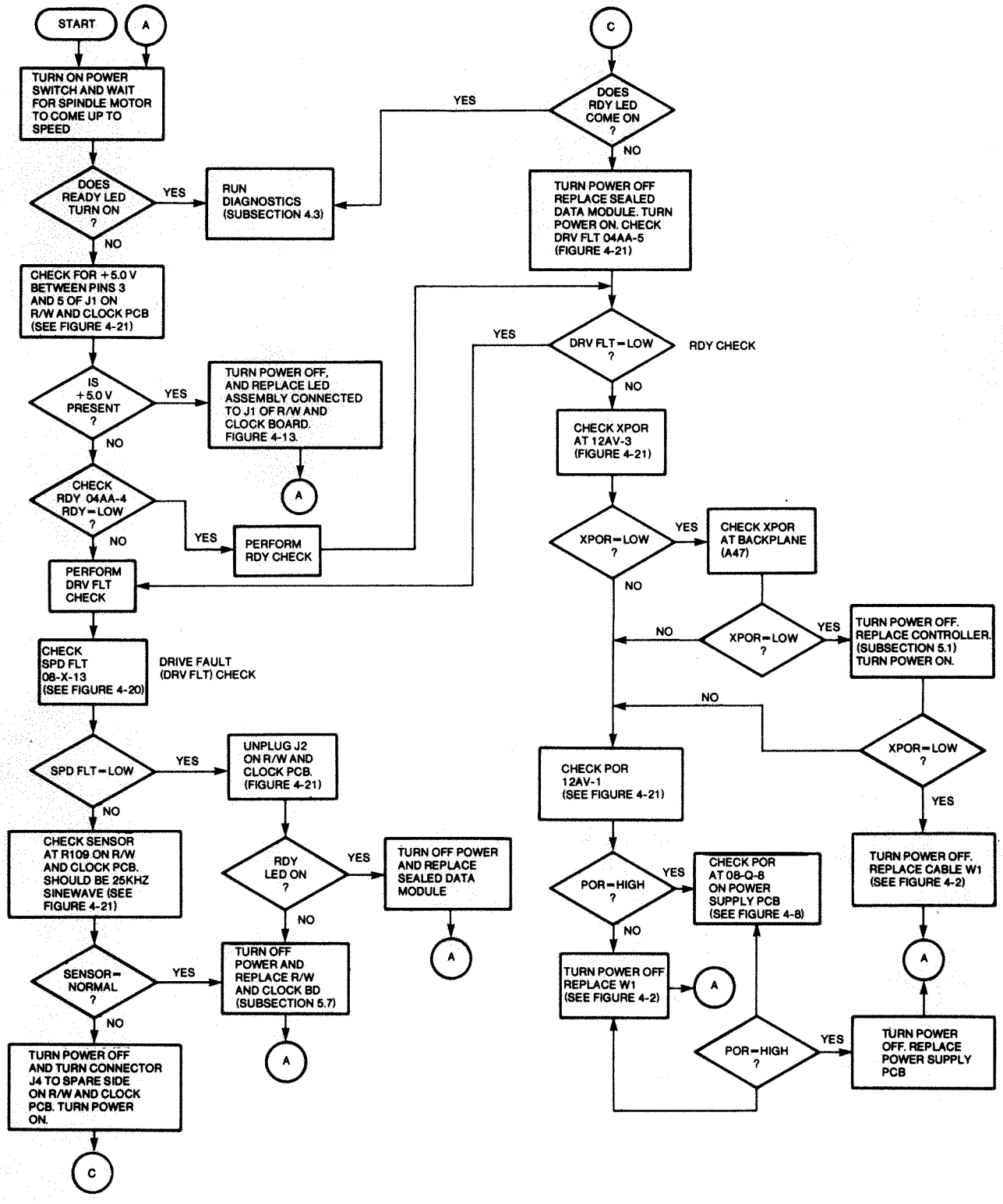

Figure 4-20. Read/Write and Clock PCB Troubleshooting Flowchart

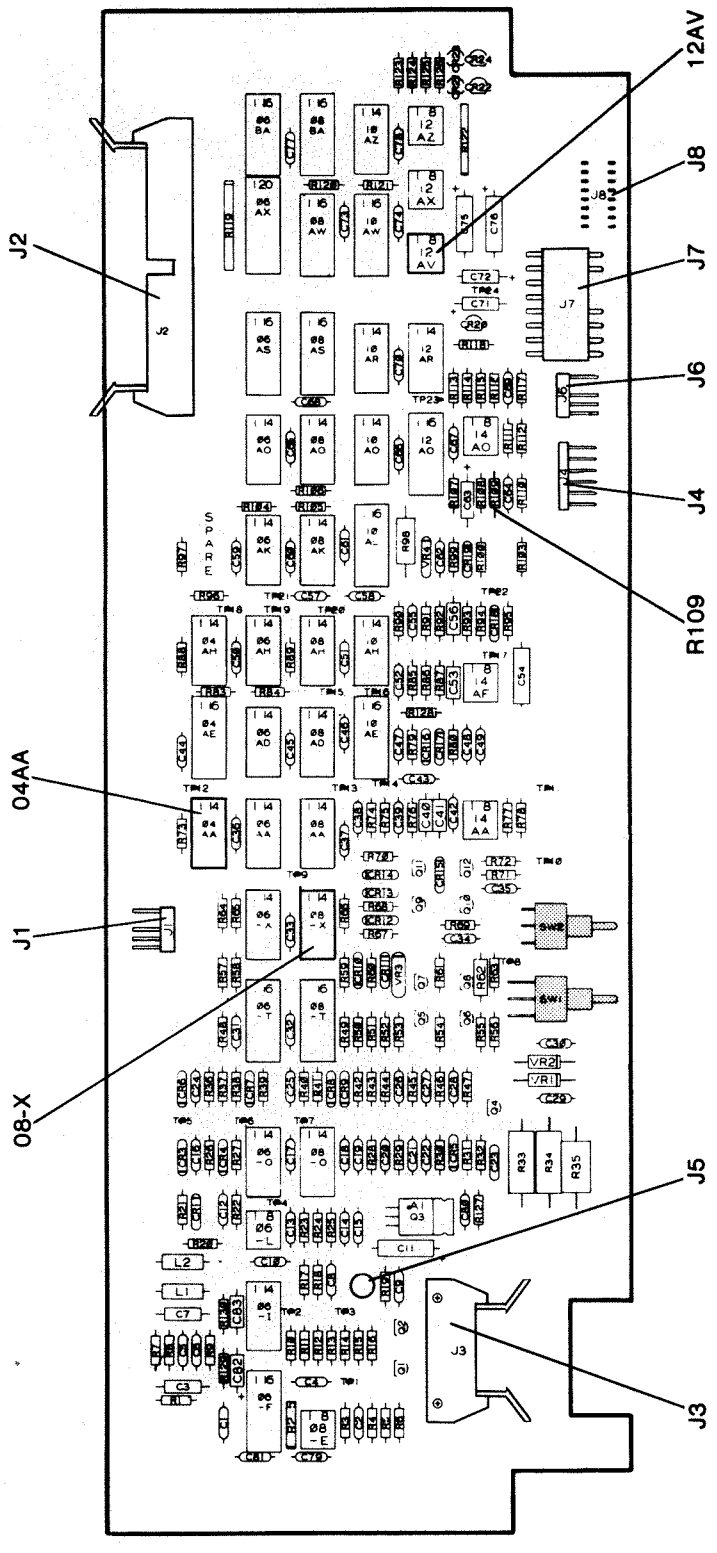

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Figure 4-21. Read/Write Clock PCB

4.3 MODEL 6234 DIAGNOSTIC TROUBLESHOOTING PREPARATION

The disk subsystem diagnostic programs allow you to test and verify the operation of the entire subsystem. In order to run the programs, the system must have the following equipment/programs:

- A NOVA or ECLIPSE computer with at least 16K of read/write memory
- An asynchronous interface (standard I/O)
- A flexible disk drive (other than the disk subsystem to be tested) or a paper tape reader, or a tape drive. If one of these devices is not present, the Data General Field Service cassette can be used.
- A system terminal (i.e. Dasher video display)
- Moving Head Disk/Floppy Diagnostic
  Program No. 095-002654 Rev. 01
  Listing No. 096-002654
- Moving Head Disk/Floppy Reliability
  Program No. 095-001141 Rev. 03
  Listing No. 096-001141

NOTE

The cassette is available to authorized Data General Field Service representatives only.

Run the diagnostic and reliability programs for subsystem installation or problems not covered in the troubleshooting flowcharts.

The diagnostic program is a short test (less than 15 minutes) that checks most of the controller logic. It uses diagnostic commands to check the DCH interface, data buffer and serial read/write chain at the controller level. It does not test the disk drive under test for maximum data transfer and is not intended to be used for long term testing.

For the detected errors, an error printout message along with the first, second, third, and sometimes fourth most probable failing FRU is printed to the terminal. The user is cautioned that the diagnostic program may or may not call out the correct failing FRU (the diagnostic program does not troubleshoot cables).

Run the reliability program after successful completion of the diagnostic program. The reliability program tests the subsystem for maximum disk activity and data transfer. Optional addressing and data patterns can be selected when running the random and sequential exerciser programs. Seek exercisers check timing using converging/diverging and random seek patterns.

The reliability program executes a string of individual tests. A detailed log of all surface related addresses, as well as a summary of all errors and seek/write/read statistics available via keyboard request.

4.3.1 Using the Programs - Run the diagnostic program for two passes (approximately 15 minutes) after a disk subsystem installation, then run the reliability program for 30 minutes. The SA for the reliability program is 505 octal which is also the RUNALL SA.

When troubleshooting the subsystem, the diagnostic program should be run first to find the failing FRU. After FRU replacement, run the diagnostic program for two error-free passes. Then run the reliability test 505 - RUNALL for two passes.

4.3.2 Preparation for Running the Diagnostics - Use these programs to verify subsystem performance after installation or to isolate problems in the subsystem. For problems causing either the READY light, the DC POWER light, or both to turn off, refer to the troubleshooting flowcharts in subsection 4.2. Otherwise, load the diagnostic.

CAUTION

For user data present on the rigid disk, back up the data if possible. If backup facilities are not available, limit diagnostic testing to the diagnostic track of the rigid disk (301 octal).

The WRITE-PROTECT Switch is located at the front of the drive. To reach this switch remove the front dress panel of the rigid drive. For more information on this switch see Section 2, Operating Controls and Procedures. For a drive suspected of having seek errors, set the WRITE-PROTECT switch on to protect against data loss until the problem is fixed. Otherwise, the WRITE-PROTECT switch should be in the off or rightmost position. When in this off position the rigid drive is not write-protected. Write operations can not be performed if the WRITE-PROTECT switch is on. Write protecting the disk seriously limits the diagnostic testing. The write-protect feature should never be used when running diagnostics except to verify that the write-protect feature works.

4.4 MODEL 6234 DIAGNOSTIC PROGRAM LOAD

To load the diagnostics refer to either the DTOS Summary Manual, Data General P/N 015-000082, or the Field Service Maintenance Manual for the respective NOVA or ECLIPSE computer the disk subsystem is using.

4.4.1 Program Load Commands - When using DTOS, enter the following command to load the diagnostic program:

```
*LOAD 6225 DIAG
```

Once the program is loaded, the following text is printed:

```
LOAD : 6225 DIAG REV. 01

TOP OF MEMORY = XXXXXX

***6225 MOVING HEAD DISC DIAGNOSTIC***
```

Starting addresses are:

SA	4	HOME ALIGNMENT
SA	6	RANDOM SEEK EXERCISER
SA	177	ODT/ DIRECT ENTRY ONLY
SA	200	START DIAGNOSTIC

4.4.2 Operator Questions and Answers for Diagnostic Program - After program load, the system asks the questions shown in Table 4-4. Answer each question. Be careful not to allow writing on the entire disk if the data on the disk is not backed up. See previous CAUTION.

Restart the program if a question is answered incorrectly. The SA is 200 octal. The program continues to repeat a question if the operator gives an answer that the program does not understand.

4.4.3 Switch Register (SWREG) Options for Diagnostic Program - Once the operator answers all the program questions, the program begins operation according to the modes selected by the SWREG switches (see Table 4-5). You can control the program operation by setting bits in the switch register. To display the present contents of SWREG, strike the M key on the system terminal. Change the bits by hitting keys 1-9, A-F. To change a value of a bit in the register, strike the respective number key on the terminal. Each key complements the stage of the bit affiliated with it. For example, to change the value of bit 4, strike the 4 key. Setting of any bit of location "SWREG" will set bit 0. (Default mode is defined as all bits of SWREG set to 0). The program continues running after updating the options. Table 4-5 contains the definitions of the SWREG bits.

Table 4-4. Questions Asked by the Diagnostic Program

Program Output	Notes	Sample Operator Input
HELP ? (YES/NO) If HELP is answered YES, the following 4 categories of help are provided: 1. STARTING ADDRESSES 2. SWREG/CONSOLE CONTROL 3. PROGRAM COMMANDS 4. FAILING REPLACEMENT UNIT	Help information is only available on Program Load.	YES
INITIALIZE ? (YES/NO)	This question is asked only on program restarts. If answered "NO", the program bypasses the following questions.	YES
SET SWREG AS PER 8.0, HIT CR TO CONTINUE		
DEVICE SELECT =	Enter octal device code.	20 - 76 (octal)
UNITS TO TEST	0,1, 2, 3 represents possible operator responses.	0
50,15,5 MBYTE DRIVE (50,15,5) OR (QF) FOR 1.2 MBYTE FLOPPY UNIT:__	Specify drive corresponding to each unit specified above.	50
DRIVE WRITE MODE - DIAGNOSTIC TRACK ONLY, OR ALL TRACKS (DIAG, ALL) - UNIT: 0	Selects which tracks to write to - the DIAG track or ALL tracks (see note).	ALL
MIN/MAX HEADS (2 OCT #'S) TESTING UNITS	Selects lowest and highest head number.	0,13

NOTE

For a wrong response to the DRIVE TEST MODE, abort the test by hitting ^0 once the program begins testing.

Table 4-5. Definitions of SWREG Bits, Diagnostic Program

Bit	Octal Value	Binary Value	Interpretation
1	40000	0	Loop on error
		1	Skip looping on error
2	20000	0	Print to console
		1	Abort printout to console
3	10000	0	Do not print % failure
		1	Print % failure
5	02000	0	Do not print on the line printer
		1	Print on the line printer
6	01000	0	Do not exit to ODT on error
		1	Exit to ODT on error
8	00200	0	Not Applicable
		1	Recalibrate during scope loop (not valid for DIAG TEST TRACK ONLY Mode)
9	00100	0	Not Applicable
		1	1 second delay during scope loop

4.4.4 Other Diagnostic Commands - (^ = Control Key)

"CR" Type a "RETURN" to continue the program after it is locked in a switch modification mode.

^D This command, given at any time, resets "SWREG" to default mode and restart the program.

^R This command, given at any time, restarts the program. Switches are left with the values they had before the command was issued.

^O This command, given at any time, causes the program control to go to ODT (this is an optional command and available only if ODTPK is present).

M This command, given at any time prints the current switch register bits.

O This command, given at any time, locks the program into switch modification mode where more than one bit can be changed.

4.4.5 Diagnostic Program Tests - The diagnostic program tests the logic, control, firmware, etc. of the disk controller and functioning (seek, read, write, recalibrate) of the drive attached to the subsystem and selected during diagnostic initialization. The diagnostic program is a progressive series of individual tests. In general, each test assumes that previous logic and function tests passed without error. The test complexity usually increases with test progression.

The diagnostic program contains the following tests:

(A) Series Tests Check:

- Busy, Done, I/O Bus Select Logic
- DIB, DOB, DIC, DOC, data paths and loading of the CA and DA registers
- Clear of CA and DA registers
- Disk select logic
- DOA to DIA data transfer
- DOA to DIC data transfer
- Control Program revision
- Controller/Drive configuration data
- Loading and reading of the hard disk control, floppy current track, current sector, and data registers
- That the MA register counts properly
- The writing and reading of the controller DCH buffer
- The Start, Busy, and Clear logic

(B) Series Tests Check:

- Recalibrate, Attention, and Interrupt logic
- Interrupt disable, Inta logic
- The Sector Count Valid and Sector Counter logic
- Recalibrate for status, current track, valid stepper phases, and home state
- Seeks to cylinders 0,42,25, maxcy for proper status, current track, stepper phases, home state, and header for Head 0, Sector 0
- Recalibrate followed by 8 step in's, 8 step out's for proper status, current track, stepper phases, home state, and header for Head 0, Sector 0

(C) Series Tests Check:

- Stepping to the diagnostic track for proper current track stepper phases, and home state
- Formatting of the entire diagnostic track
- Write operations for proper status
- SELD, clear logic
- Write/Read operations for proper status, ending MA, ending DA, and full core compare after read
- Read header operation on all heads
- Writes to different HDS, sectors
- Multisector writes (4,8,16)
- Writes to all sectors
- The increment head logic
- Seek/Write operations for proper status
- Illegal sector, illegal surface, end of cylinder, and illegal cylinder conditions

(E) Series Tests Check:

- 1 Sector Write/Read operations (9 different data patterns with core compare and write CRC verified)
- 8 sector Write/Read operations (9 different data patterns), all heads, at CYL 0, MAX/2, MAX with full core compare
- The bootstrap operation with full core compare (if Unit 0)
- Write CYL# to Head 0, Sector 0 of all cylinders
- Write Head # to Sector 0 of all heads on CYL 0
- Each of the above operations is followed by a corresponding Read/Check operation to verify (DA) logic
- Seek/write and seek/read operations for full track seeks, all heads, with full core compare
- Seek 1,2,4,.../recal/read operations

(F) Series Tests Check (Hard Disk Diag. Track Only):

- Address check and bad sector logic by altering the format on CYL 0, Head 0, Sector 0, 1 bit at a time and monitoring the results after a write

- The unsafe logic by formatting a sector, followed by a read of that sector before any Write operation
- The CRC logic by formatting a sector, with a data sync set, arbitrary data, and a zero CRC. This operation is then followed by a read, which should cause a CRC error.
- The unsafe logic by a special format command to format a sector with NRZ write data, followed by a read operation
- That a normal format operation followed by a normal write operation may be executed

Seek Exerciser Tests

- Writes track # to Head 0, Sector 0 of each track
- Performs random seeking. Each seek is followed by a read to Head 0, Sector 0

4.4.6 Diagnostic Error Reports - Detailed error and command summary information is printed on detection of an error. Additionally, tests that perform error checking issue a "probable failing FRU" report. This report identifies the first, second, third, and sometimes fourth most likely failing FRU for the detected error; e.g., controller PCB, media, read/write and clock PCB. The error report gives the operator information such as:

- The last command
- The last address issued before failure detection
- Status information down to the bit level.

For a detected error, the program prints the error PC, AC 0, 1, and 2 at the point of error, plus an option printout. The program then goes into a scope loop between entries to .SETUP and .LOOP allowing the operator to set SWPAK. In general the error PC points to a call error.

The option printout is done in one of the formats shown in Figure 4-22.

NOTE

The diagnostic program may or may not call out the correct failing FRU. Further investigation may still be required by referencing and then performing the procedure given in the diagnostic flowcharts (refer to subsection 4.2)

```
A.  STAND-ALONE CONTROLLER TEST FAILURES-

FAILING MODULE - DISK CONTROLLER

B.  STATUS ERRORS

MODE      UNIT      #      DATA
STARTING DISK ADDRESS
CYL       #       HEAD              SECTOR  #
AC1(STATUS) SHOULD =AC0
DESCRIPTIONS OF FAILING STATUS BITS
PROBABLE FAILING MODULES -(AS PER EACH FAILING BIT)

C.  MEMORY/DISK ADDRESS ERROR

MODE      UNIT     #        DATA
STARTING DISK ADDRESS
CYL       #       HEAD      #               SECTOR  #
ENDING MEMORY/DISK ADDRESS ERROR

AC1(MA/DA) SHOULD =AC0

D. INTERRUPT TIMEOUT

MODE     UNIT     #          DATA
STARTING DISK ADDRESS
CYL       #       HEAD       #              SECTOR  #
INTERRUPT TIMEOUT
```

Figure 4-22. Model 6234 Sample Error Report

CAUTION

Replacing the data module or reformatting the disks in the data module will destroy all stored data.

When you receive a failing FRU (module) report, replace one FRU at a time and rerun the diagnostic program. If the diagnostic fails after replacing one FRU, reinstall the original FRU and then replace the other FRU called out by the error report and try again. Refer to Section 5 for replacement procedures.

If the medium is called out as a failing module, try reformatting before replacing the data module.

Additional test significance can be found in the program listing, although it is hoped that a need for the listing will be minimal. SWPACK (SWREG) provides all control over test loop options and printouts.

Data errors cause the first three good/bad pairs and their addresses to be printed along with the total count. If an ECC error is detected, the call EHECC acknowledges the fact and returns to the main test for the data compare. Printouts result on the first error pass only. As the check routine checks the entire read buffer, any error accompanied by an ECC error, terminating the read, may cause all data in succeeding sectors to appear bad.

Tests that perform a recalibrate have a 2 second delay built into the scope loop. Set SWPAK 9 = 1 to introduce an additional 1 second delay during the scope loop.

In general, each successive test assumes all previous tests work. Bypassing errors can result in confusing situations in the set up of more complex tests.

4.4.7 Special Notes/Features of the Diagnostic Program - The following information is helpful when using the diagnostic program.

1. If the disk has bad sector flags set on Cylinder 0 or 'DIAG', or on the first 8 sectors of Head 0 on any cylinder, error printouts result when the flags are encountered. The DIA status word will indicate that the bad sector bit is set and may or may not indicate a data error. These error printouts (that indicate a bad sector bit is set) should be ignored.

2. Some scope loops require a recalibrate to initialize the disk drive following a failure. Set SWPAK 8 = 1 to introduce the RECALIBRATE to the unit under test.

3. Identified FRUs:

FRU	Location
Disk controller PCB	NOVA or ECLIPSE CPU Chassis
Read/write and clock PCB	Model 6234 Chassis
Power supply PCB	Model 6234 Chassis
Head/Sealed Data Module	Model 6234 Chassis

NOTE

In addition to the FRUs listed, three LSI chips on the controller PCB, and two transducers will be treated as FRUs to a limited extent. These five submodules are:

a. The DCH Controller chip (DCH chip)
b. The Hard Disk Controller chip (HDC chip)
c. The Floppy Disk Controller chip (FDC chip) "option"
d. Home Transducer
e. Sector Transducer

4.5 THE RELIABILITY PROGRAM FOR MODEL 6234

The reliability program tests the subsystem for maximum disk activity and data transfer. Optional addressing and data patterns can be selected when running random and sequential exerciser programs. Seek exercisers check timing using converging/diverging and random seek patterns. The program executes a string of individual tests. A detailed log of all surface related addresses, as well as a summary of all errors and seek/write/read statistics is available by keyboard request.

CAUTION

The reliability program writes on the entire disk. If the disk cannot be backed up, do not run the reliability program.

Do not run 504 FORMAT unless absolutely necessary. All bad sector information will be lost. The 504 VERIFY program does flag bad sectors but may not find as many as the special test equipment used in the manufacturing test.

NOTE

Specific areas of the disk may be tested using a min/max Head/CYL option contained in the reliability program.

4.5.1 Loading Model 6234 Reliability Program - When using DTOS, enter the following command to load the reliability program:

```
*LOAD 6098 RELI
```

4.5.2 Reliability Program Tests - The reliability program contains several different test programs. Each program has its own SA as shown in Table 4-6.

4.5.3 Reliability Program Operator Questions and Answers Operator Responses - Table 4-7 lists the questions the operator answers to continue the reliability program. After the operator answers all the program responses, the program indicates test(s) are in progress by responding:

```
TESTING DEVICE:  XX UNIT: X,X,
```

NOTE

DTOS starts the program at SA 505 on Load.

Table 4-6. Reliability Program Starting Addresses

SA (Starting Address)	Test Program
176	Memory dump
177	ODT - direct entry only
200	RUNALL tests (same as 505)
500	Random reliability test, all cylinders
501	Reliability test, options
502	Incremental disk address test
503	Command string interpreter
504	Formatter/Verify
505	RUNALL (same as 200)
506	Seek exerciser (converging/diverging)
507	Seek exerciser (random)
510	Error count/log recovery

Table 4-7. Questions Asked by the Reliability Program

Program Output	Notes
TTY BAUD RATE (DEC. #) = # BITS/CHAR = ? (10 or 11)	Only asked if RTC is not present for program timing
HELP ? (YES/NO) 1. STARTING ADDRESSES 2. SWREG/CONSOLE CONTROL 3. DATA PATTERNS 4. COMMAND STRING	1. If help is requested, the user has the choice of four categories. 2. Help information is only available on program load.
INITIALIZE (Y/N) ? (Asked only if initial data already loaded by previous start.)	If NO, the following 6 questions are bypassed.
DEVICE CODES -	1 to 8 device codes may be entered.
UNIT NUMBER -	Enter a 0 for Model 6234. 0,1 for floppy disk option.
50,25,15,12,5 MBYTE OR QF (1.2 MB FLOPPY) UNIT: 0	Enter size of each unit to be tested.
CHANGE MIN/MAX HEAD/CYLINDER SETTINGS ? (Y/N)	If NO, the following 2 questions are bypassed.
MIN/MAX HEAD LIMITS UNIT: 0 0 2 (example)	Enter 2 OCTAL # (0 13 is max)
MIN/MAX CYLINDER LIMITS UNIT: 0 0 200 (example)	Enter 2 OCTAL # (0 277 is max)
START TIME ? MON,DAY,YEAR,HR,MIN	
SET SWREG AS PER 8.0, OR HIT (CR) TO CONTINUE	Refer to 4.5.8 for SWREG options.

4.5.4 Reliability Data Patterns - Several of the programs require the operator to specify a data pattern for writing to and reading back from the drive. The data patterns used are listed as follows:

RAN = RANDOM DATA
ALO = ALL ONES
ALZ = ALL ZEROS
PAT = 1 5 5 5 5 5 DATA
ALT = 5 2 5 2 5 DATA
FLO = FLOATING ONE pattern
FLZ = FLOATING ZERO pattern
ADR = ALTERNATING CYLINDER AND HEAD & SECTOR WORDS
XXX = XXX represents operator entered string of up to seven octal words for data use. The words entered are used repeatedly to makeup a sector block. Type CR (carriage return) to use previous entry.
ROT = rotated 1 5 5 5 5 5 pattern - this is a data option that applies to Incremental DA Test (SA 502) and Format Verify (SA 504) only. It results in a total of 4 passes across the pack, rotating the pattern after each pass. After each pass and before the pattern rotates, it prints ***PASS*** on the terminal. This data pattern ensures that a peak phase shift occurs across each bit cell on the media. This test pattern is recommended when running error rates.
ALTERNATELY = UP TO 7 OCTAL WORDS MAY BE ENTERED AS OPERATOR DATA

4.5.5 Reliability Program Descriptions - The reliability program is made up of a series of smaller programs, each with its own starting address (SA). Table 4-8 describes and lists the starting addresses of these programs.

Table 4-8. Reliability Program Descriptions (page 1 of 4)

SA 177	-	Direct entry to ODT The reliability program is equipped with a built-in ODT (octal debugging tool). For more information on using ODT, refer to the DTOS Summary Manual, Data General No. 015-000082.
SA 200	-	RUNALL See SA 505
SA 500	-	Reliability test This program uses a random number generator to select a disk drive, cylinder, head, beginning sector, and number of consecutive sectors. Random data is then written and read. The sequence is repeated indefinitely.

Table 4-8. Reliability Program Descriptions (page 2 of 4)

SA 501 - Reliability test

This test is the same as the previous test except that the operator is given the option of selecting data patterns and choosing a constant cylinder, head, sector, or number of sectors. Any letter response to CYL, HEAD, etc. selects the random function for that variable. A CR (carriage return) selects the random function for all variables. All inputs are checked for range and rejected if out of range.

SA 502 - Incremental disk

This test gives the operator the option address test of selecting data patterns. Requested data is first written over the selected disk surface, then data is read from all sectors. This ensures that the disk surface blocks are useable and are formatted properly. This test will not guarantee to read every sector. The test is then repeated for all ready disks, and PASS is printed to the system terminal. The sequence is then repeated indefinitely until manually stopped by the operator.

NOTES: 1. Should a write error occur on the write pass (e.g., address or bad sector error) which terminates the write transfer, a read error will also occur at the failing address on the read pass. In such instances, ignore the read error.
2. If SWREG 8 = 1(refer to subsection 4.5.8), the program is put into read only mode, SAs 501, 502 only. If SA is 501, data must be a constant.

SA 503 - Command string

This program allows the operator to type interpreter in test loops for troubleshooting. Refer to subsection 4.5.6 for a detailed operating description.

SA 504 - Format/Verify

NOTE

Format is run serially while verify runs all controllers in parallel.

This program gives the operator the program option of either formatting or verifying the disk or both. If the format operation is requested, the disk is first formatted after which a format done message is printed. If a verify was requested, then a 1 5 5 5 5 5 pattern is written to the entire pack and read back, and PASS is printed. The data pattern is

Table 4-8. Reliability Program Descriptions (page 3 of 4)

SA 504 - Format/Verify continued

then rotated 1 bit and the write/read process is repeated. When the number of passes specified by the operator are completed, a log is printed and the drive is released. It is recommended that at least six passes (write/read) be allowed to insure pack quality. Hard data or address errors will set the bad sector flag for that sector. Soft data or address errors encountered twice will also set the bad sector flag. Any other error will be printed on the console and and the program will stop on that unit, unless SWREG 14 =1 (refer to subsection 4.5.8). Verify is guaranteed to read every sector.

SA 505 - RUNALL

This program executes the following programs in a "top down" fashion:

SA 501 - Random reliability with data patterns: PAT, RAN, FLZ, FLO
SA 502 - Incremental disk address with data patterns: ROT (3 TIMES), RAN, ADR, ALT, ALZ, ALO
SA 507 - Random seek exerciser.

NOTE

SA 501 and 502 tests all controllers in parallel.

SA 507 tests all controllers serially.

SA 506 - Seek Exerciser

This program provides a seek scan sequence converging from the extreme outermost tracks in the center, the diverging again to the extreme outermost tracks. All seeks in programs SA 506 and 507 are followed by a one sector read at a random sector with no data check. All seeks are timed with maximum, minimum, and average times being logged in milliseconds. Seek paths for maximum and minimum values are also logged. Incremental disk address test (SA 502) should be run prior to running either seek exerciser to avoid possible checkword errors during reads.

Table 4-8. Reliability Program Descriptions (page 4 of 4)

SA 507 - Random Seek Exerciser

This is the same as SA 506 except that the seek sequence is random.

SA 510 - Error Count/log recovery

In the event a program was stopped during a run, the error logs may be recovered at this starting address. This MUST be done before any program restart as the program initialization zeros all logs.

4.5.6 Command String Interpreter for the Reliability Program - This program is an aid which allows the user to type in test loops. The program starts at SA 503. Once started the program responds by asking the following questions.

```
DEVICE:
UNIT #:
DATA:

COMMAND STRING:
```

The unit number is 0. The data can be either a data pattern or any specified data (data must be all octal numbers). The command string can consist of either one or a combination of the following commands.

• READ	HEAD,SECTOR, # OF SECTORS
• WRITE	SAME
• SEEK	CYLINDER
• RECALIBRATE	
• DELAY	N (N= MS DELAY)
• LOOP	- LOOP TO LR OR CSI START
• LR	- LOOP RETURN
	..* HARD DISK ONLY..*
• BAD	CYLINDER,HEAD,SECTOR (SET BAD SECTOR)
• FORMAT	CYLINDER,HEAD,SECTOR
• RDH	(READ LAST ACCESS SECTOR HEADER)

For example, the following command string causes unit 0 to seek cylinder 50. It then repeatedly writes sector 2 and 3 using head 1, reads it back and checks the data. The data is specified as alternate words of zeros then ones.

```
DEVICE: 63
UNIT #: 0
DATA: 0,177777

COMMAND STRING: SEEK 50 LR WRITE 1,2,2, READ SAME LOOP
```

A space or a comma must be used to separate the commands. If more room is needed on a line, type "New Line" on the system terminal. Use "CR" (carriage return) to terminate the line. If the command string is too long, the message "INPUT OVERFLOW" is printed on the terminal.

The following additional commands are used to control the reliability program operation.

- Type R to interrupt the execution of the current command and return to the DRIVE #: prompt.
- Type a CR as a response to the DRIVE #:, UNIT #:, DATA:, and or COMMAND STRING to use the previous entries.
- Type ESC to bypass DRIVE #:, UNIT #:, and DATA: prompts, using previous entries.
- Type CTRL O to enter ODT

4.5.7 Reliability Error and Statistics Logs - The reliability program maintains an error log and statistics log during operation. To access the error log, strike the L key on the system terminal. The error log gives the user information concerning: seek errors, data errors, address errors, bad sectors, sectors read, and sectors written. To access the reliability statistics log, strike the W key on the system terminal. Table 4-9 gives an example of the statistics log.

Table 4-9. Reliability Statistics Log Example

Name	Quantity
DEVICE 63	0
DRIVE	0
BAD SECTOR	0
SECTORS READ	11249
SECTORS WRITTEN	11264
TOTAL SEEKS	1544
SEEK ERRORS	0
ADDR ER DIAG. AS SEEK ERROR	0
PERM ADDRESS ERROR	0
DATA ERRORS	0
DATA W/O CHKWD ERR	0
CHKWD ERR/DATA OK	0
DATA LATE	0
INTERRUPT TIMEOUTS	0
ENDING MEM ADDR ERROR	0
ENDING DISC ADDR ERROR	0
MULTIPLE FAULTS	0
NO R/W DONE	0
UNSAFE	0
OPERATION TIMEOUT	0
END ERROR	0
LOSS OF READY	0

4.5.8 Reliability Switch Register (SWREG) Options - The user can control program operation by setting bits into the SWREG. To display the present contents of the SWREG, strike the M key on the system terminal. To change the bit value in the register, strike the respective number key on the terminal (i.e., to change the 4 bit value, strike the 4 key). The definition of the SWREG bits are listed in Table 4-10.

Table 4-10. Definitions of SWREG Bits, Reliability Program

Bit	Octal Value	Binary Value	Interpretation
1	40000	0	Loop on error
		1	Skip looping on error
2	20000	0	Print to console
		1	Abort printout to console
5	02000	0	Do not print on the line printer
		1	Print on the line printer
6	01000	0	Do not exit on error
		1	Exit to ODT on error
8	00200	0	Not Applicable
		1	For read only mode (SA 501, 502)
9	00100	0	Not Applicable
		1	Bypass data check
11(B)	00020	0	Not Applicable
		1	Enable bad sector printouts
12(C)	00010	0	Not Applicable
		1	Enable expanded error printout
13(D)	00004	0	Not Applicable
		1	Print I/O trace on error (last 5 I/O calls PCs + commands)
14(E)	00002	0	Exit on nonsurface related errors
		1	Do not exit on nonsurface related errors (applies to SA 504 only)
15(F)	00001	0	Not Applicable
		1	Loop on last format CMD (SA 504 only)

4.5.9 Reliability Program Output and Error Description - Table 4-11 provides the user with an interpretation of the reliability program output and error descriptions.

4.5.10 Reliability Error Report - The following error status prints on the system terminal whenever an error occurs.

```
MODE DEVICE # 73  UNIT: n
CYL - n  HEAD - n   SECT - n   #SECT - n
```

CYL, HEAD, SECT refer to the final disk address at the point of the error. #SECT refers to the number of sectors of data actually transferred.

When data errors are found, only the first three are printed per encounter. When looping is involved, (retries or scoping) the status prints on the first pass only.

Table 4-11. Reliability Program Output and Error Description (page 1 of 3)

Function	Description
Loss of Ready	When running a single drive, the program prints the appropriate error message and halts. If two drives are under test, the program continues with the remaining drive. If the down drive is placed back on-line, the program resumes testing of that drive. A "loss of ready" when using the command string interpreter (SA 503) causes the appropriate error message to print, but does not remove the failing drive from testing. The program loops on the failure.
Recalibrate	Any unusual status is reported immediately and a return executed.
Seek	Any positioner faults increment a seek error counter. Any error status results in a status printout and an error return. A recalibrate is performed by the error handler. The program logs the first 20 cylinders (to/from) on finding seek errors.

Table 4-11. Reliability Program Output and Error Description (page 2 of 3)

Function	Description
Write	The "Done" flag is set after a write, and errors are checked in the sequence that follows. An error recovery procedure is outlined for each case. If the error is not present, the next check is made. 1. Interrupt timeouts, any drive fault - increments the appropriate error count, prints the illegal status and does an error return. 2. Bad sector error - checks for sectors which have their bad flag set denoting surface defects. The program logs the first 100 bad sector addresses encountered. No printout results unless SWREG 10 = 1. A "soft" error is recorded if the sector under scrutiny passes at least 1 of 4 of the retries. Soft errors print out regardless of the state of SWREG 10. 3. Address error - prints error header, the Byte # and the contents of the first header byte in error. Repeats the write, and if the test passes the second time, it increments the soft address error count and does a normal return. If the test fails the second time, it increments the hard address error count and does an error return. If an address error occurs on the first sector transfer, a read on an adjacent head will be attempted to determine whether the fault should be classed as a seek error or an address error. The first 20 errors have their addresses logged. 4. Ending memory address error - increments the memory address error count, prints the error message, checks for a disk address error and does an error return. 5. Ending disk address error - increments the disk address error count, prints the error message, and does an error return.

Table 4-11. Reliability Program Output and Error Description (page 3 of 3)

Function	Description
Read	All read errors with the exception of data related errors are handled in the same manner as those described for write errors.
Data Errors	Data is read 3 times (4 times for an undetected checkword). If the program is in write/read mode and the data is bad on two passes, a hard error count is incremented and an error return taken. If data is good on all retries, a soft error count is incremented and a normal return taken. If SWREG 9 = 1, the data check is bypassed, and hard or soft data errors are to be determined by the checkword status. The disk addresses of data problems are printed and the first 100 logged. The first three good/bad word pairs and respective addresses are printed. Data errors reporting on the same cylinder number, head number, and sector number at different times during RELI usually indicate that a bad sector has been encountered and must be flagged using command string SA 503.
Checkword Failed	Two conditions may fall into this category. 1. A checkword was detected with no accompanying data error. This error indicates, checkword problem. 2. A data error occurred without a corresponding checkword error. Both of these checkword failures are counted once per error path under the corresponding drive statistics summary headings.

4.6 MODEL 6280 DIAGNOSTIC TROUBLESHOOTING PREPARATION

The disk subsystem diagnostic programs allow you to test and verify the operation of the entire subsystem. In order to run the programs, the system must have the following equipment/programs:

- A ECLIPSE S20 computer with at least 16K of read/write memory
- An asynchronous interface (standard I/O)
- A flexible disk drive (other than the disk subsystem to be tested) or a paper tape reader, or a tape drive. If one of these devices is not present, the Data General Field Service cassette can be used.
- A system terminal (i.e. Dasher video display)
- Moving Head Disk/Floppy Diagnostic
  Program No. 095-003209 Rev. 00
  Listing No. 096-003209
- Moving Head Disk/Floppy Reliability
  Program No. 095-001138 Rev. 03
  Listing No. 096-001138

NOTE

The cassette is available to authorized Data General Field Service representatives only.

Run the diagnostic and reliability programs for subsystem installation or problems not covered in the troubleshooting flowcharts.

The diagnostic program is a short test (less than 5 minutes) that checks most of the disk system. It uses I/O and diagnostic commands to check the BMC interface, data buffer and serial read/write chain at the controller level and disk drive. It is not intended to be used for long term testing.

For the detected errors, an error printout message along with the first, second, third, and sometimes fourth most probable failing FRU is printed to the terminal. The user is cautioned that the diagnostic program can only isolate 80% of faults to a FRU (the diagnostic program does not troubleshoot cables).

Run the reliability program after successful completion of the diagnostic program. The reliability program tests the subsystem for maximum disk activity and data transfer. Optional addressing and data patterns can be selected when running the random and sequential exerciser programs. Seek exercisers check timing using converging/diverging and random seek patterns.

The reliability program executes a string of individual tests. A detailed log of all surface related addresses, as well as a summary of all errors and seek/write/read statistics are available via keyboard request.

4.6.1 Using the Programs - Run the diagnostic program for two passes (approximately 10 minutes) after a disk subsystem installation, then run the reliability program for 30 minutes. The SA for the reliability program is 505 octal which is also the RUNALL SA.

When troubleshooting the subsystem, the diagnostic program should be run first to find the failing FRU. After FRU replacement, run the diagnostic program for two error-free passes. Then run the reliability test 505 - RUNALL for two passes.

4.6.2 Preparation for Running the Diagnostics - Use these programs to verify subsystem performance after installation or to isolate problems in the subsystem. For problems causing either the READY light, the DC POWER light, or both to turn off, or the controller self test fault LED (CR2) to turn on (Figure 4-23), refer to the troubleshooting flowcharts in subsection 4.2. Otherwise, load the diagnostic.

CAUTION

For user data present on the rigid disk, back up the data if possible. If backup facilities are not available, limit diagnostic testing to the diagnostic track of the rigid disk (301 octal).

The WRITE-PROTECT Switch is located at the front of the drive. To reach this switch remove the front dress panel of the rigid drive. For more information on this switch see Section 2, Operating Controls and Procedures. For a drive suspected of having seek errors, set the WRITE-PROTECT switch on to protect against data loss until the problem is fixed. Otherwise, the WRITE-PROTECT switch should be in the off or rightmost position. When in this off position the rigid drive is not write-protected. Write operations can not be performed if the WRITE-PROTECT switch is on. Write protecting the disk seriously limits the diagnostic testing. The write-protect feature should never be used when running diagnostics except to verify that the write-protect feature works.

4.7 MODEL 6280 DIAGNOSTIC PROGRAM LOAD

To load the diagnostics refer to either the ADES Operator's Manual, Data General P/N 014-000744, or the Field Service Maintenance Manual for the host computer the disk subsystem is using.

4.7.1 Program Load Commands - When using ADES, enter the following command to load the diagnostic program:

```
*PCDD DIAG
```

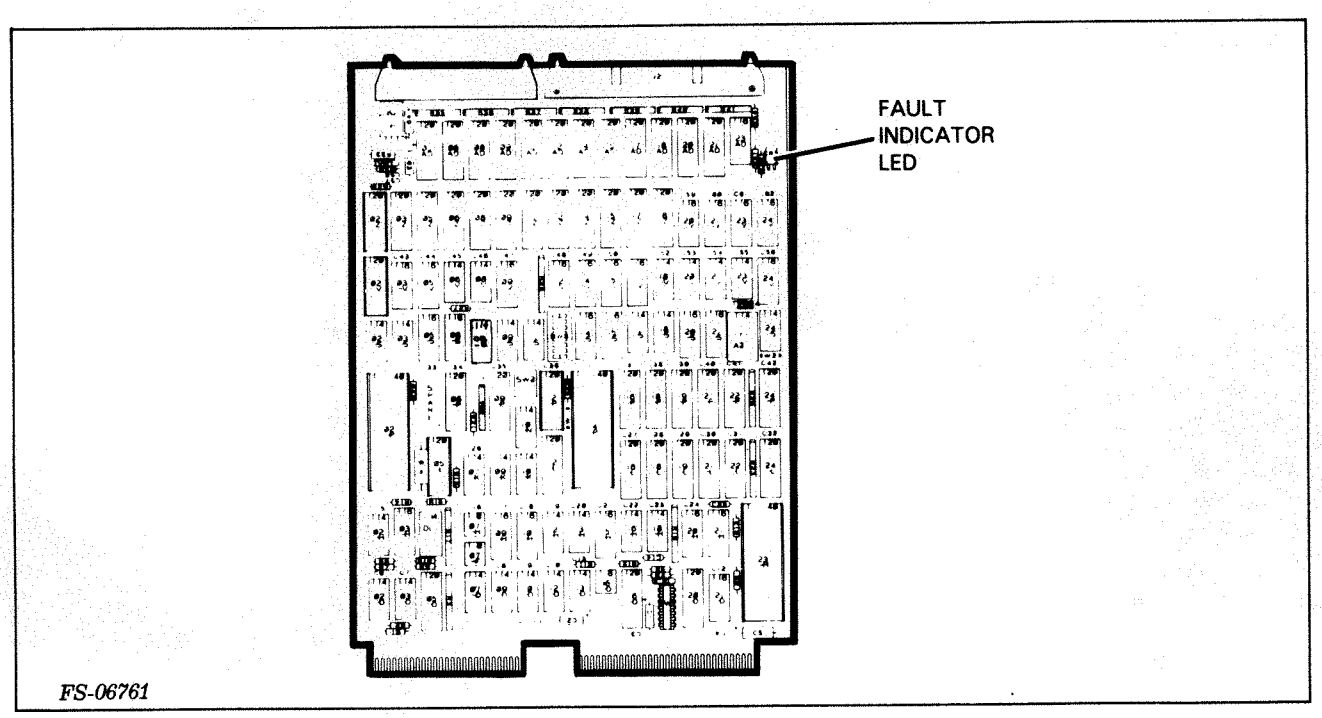


Figure 4-23. Model 6280 Fault Indicator LED

Once the program is loaded, the following text is printed:

```
LOAD : PCDD DIAG REV. 00

TOP OF MEMORY = XXXXXX
```

Starting addresses are:

```
SA   4        HOME ALIGNMENT

SA   6        RANDOM SEEK EXERCISER

SA 177        ODT/ DIRECT ENTRY ONLY

SA 200        START DIAGNOSTIC

SA 500        SAME AS 200
```

4.7.2 Operator Questions and Answers for Diagnostic Program - After program load, the system asks the questions shown in Table 4-12. Answer each question. Be careful not to allow writing on the entire disk if the data on the disk is not backed up. See previous CAUTION.

Restart the program if a question is answered incorrectly. The SA is 200 octal. The program continues to repeat a question if the operator gives an answer that the program does not understand.

4.7.3 Switch Register (SWREG) Options for Diagnostic Program - Once the operator answers all the program questions, the program begins operation according to the modes selected by the SWREG switches (see Table 4-13). You can control the program operation by setting bits in the switch register. To display the present contents of SWREG, strike the M key on the system terminal. Change the bits by hitting keys 1-9, A-F. To change a value of a bit in the register, strike the respective number key on the terminal. Each key complements the stage of the bit affiliated with it. For example, to change the value of bit 4, strike the 4 key. Setting of any bit of location "SWREG" will set bit 0. (Default mode is defined as all bits of SWREG set to 0). The program continues running after updating the options. Table 4-13 contains the definitions of the SWREG bits.

Table 4-12. Questions Asked by the Diagnostic Program

Program Output	Notes	Sample Operator Input
HELP ? (YES/NO) If HELP is answered YES, the following 4 categories of help are provided: 1. SWREG/CONSOLE CONTROL 2. STARTING ADDRESSES 3. PROGRAM COMMANDS 4. FAILING REPLACEMENT UNIT (FRU)	Help is only available on Program Load.	YES
INITIALIZE ? (YES/NO)	Only asked on program restarts. If 'NO' program will bypass following questions.	YES
SET SWREG AS PER 8.0, HIT CR TO CONTINUE		
DEVICE CODE =	Enter octal device code.	20 - 76 (octal)
DRIVE TEST MODE -	Diagnostic track only, or all tracks	DIAG, ALL
UNIT: 0		ALL
MIN/MAX HEADS (2 OCT #'S)	UNIT 0	N1, N2
TESTING UNITS 0	Indicates test in progress	

Table 4-13. Definitions of SWREG Bits, Diagnostic Program (Page 1 of 2)

Bit	Octal Value	Binary Value	Interpretation
1	40000	0	Loop on error
		1	Skip looping on error
2	20000	0	Print to console
		1	Abort printout to console
3	10000	0	Do not print % failure
		1	Print % failure
5	02000	0	Do not print on the line printer
		1	Print on the line printer
6	01000	0	Do not exit to ODT on error
		1	Exit to ODT on error

Table 4-13. Definitions of SWREG Bits, Diagnostic Program (Page 2 of 2)

Bit	Octal Value	Binary Value	Interpretation
7	00400	0	Not Applicable
		1	Print optional system status data
8	00200	0	Not Applicable
		1	Recalibrate during scope loop (not valid for DIAG TEST TRACK ONLY Mode)
9	00100	0	Not Applicable
		1	1 second delay during scope loop
A	00040	0	Not Applicable
		1	Print test number at start of each test

4.7.4 Other Diagnostic Commands - (^ = Control Key)

"CR" Type a "RETURN" to continue the program after it is locked in a switch modification mode.

^D This command, given at any time, resets "SWREG" to default mode and restart the program.

^R This command, given at any time, restarts the program. Switches are left with the values they had before the command was issued.

^O This command, given at any time, causes the program control to go to ODT (this is an optional command and available only if ODTPK is present).

M This command, given at any time prints the current operating modes.

O This command, given at any time, locks the program into switch modification mode where more than one bit can be changed.

4.7.5 Diagnostic Program Tests - The diagnostic program tests the logic, control, firmware, etc. of the disk controller and functioning (seek, read, write, recalibrate) of the drive attached to the subsystem. The diagnostic program is a progressive series of individual tests. In general, each test assumes that previous logic and function tests passed without error. The test complexity usually increases with test progression.

In general, each successive test assumes all previous test's work. Bypassing errors can result in confusing situations in the setup of more complex tests.

The diagnostic program contains the following tests:

A SERIES	CONTROLLER TESTING	
0	RESET W/O CHECKS	
1	CHECK RESET BUSY/DONE	
2	DOB/DIB	77777
3	RESET DOB	
4	DOB (DEVICE 0) NO EFFECT	
5	DOB/DIB	FLOAT 1/0
6	DOB (ALL DEVICE CODES) NO EFFECT	
7	CHECK FOR DRIVE READY	
8	LDIA DIAG CMND	125/252
9	LDIA DIAG CMND	FLOAT 0/1
10	CHECK SELF TEST FAULTS	
11	XFER DOC/DIC	ALL
12	CHECK XFER DOA (0-7)/DIC	00/37
13	CHECK XFER DOA (8-15)/DIC	0
14	TEST SEQ 0 REG DIAG	ALL
15	TEST SEQ 1 REG DIAG	ALL
16	TEST SEQ 2 REG DIAG	ALL
17	TEST SEQ 3 REG DIAG	ALL
18	REPORT CONTROL PROG REV	
19	CHECK CONTROLLER ID BITS	
20	CONTROL PROG ROM CHECKSUM	
21	CHECK XFER DOC/SHIFTER/DIC	ALL
22	CHECK EXTENDED STATUS FOR 0	
23	CHECK DATA FIFO PATH	ALL
24	++	
25	MEASURE SECTOR COUNT VALID PULSE WIDTH	
26	TEST DISK SECTOR COUNTER VIA DIAG CMND	
B SERIES	REC/SEEK TESTING	
27	FIRST RECAL	
28	VERIFY DONE AND CLEAR	
29	CHECK INTERRUPT DISABLE	
30	CHECK FOR OPEN INTERRUPT DISABLE	
31	VERIFY DISK WILL CAUSE INTERRUPT ON NOP CMND	
32	++	
33	++	
34	TRACK 0 STEPPER PHASES	
35	STEP IN/ STEP OUT	
36	STEPPER PHASE SEQUENCE	
37	FIRST SEEK WITH READ HEADER	
38	2 CYLNDER SEEK	
39	SEEK 0/ SEEK MAX WITH READ HEADER	
40	CHECK SEEK AFTER CLEAR	
41	CHECK SEEK AFTER CLEAR DURING SEEK	
42	STEP TO DIAG TRACK	
43	FORCE END OF CYLINDER	

++ = TEST NUMBER NOT USED

C SERIES — WRITE/READ TESTING

44	SEEK MAX CYLNDER (C LEVEL SETUP)	
45	SEEK/STEP TO DIAG TRACK	
46	FORMAT DIAG TRACK	
47	WRITE 1 SECTOR	
48	CHECK SELECT DONE/BUSY AFTER WRITE	
49	WRITE READ 1 SECTOR	
50	READ HEADERS ALL HEADS SECTOR 0	
51	WRITE TO MIN/MAX HEAD 1 SECTOR	
52	WRITE HEAD 0,SECT 7 & MAX, 1 SECTOR	
53	1 SECTOR WRITE TO ALL SECTORS	
54	FORCE ADDR ERROR BY WRITE SECTOR MAX+1	
55	2 SECTOR WRITE HEAD 0,SECT 0	
56	4 SECTOR WRITE HEAD 0,SECT 0	
57	HEAD BUMP VIA WRITE MAX SECT-1, SC=4	
58	16 SECTOR WRITE HEAD 0,SECT 0	
59	32 SECTOR WRITE HEAD 0,SECT 0	
60	64 SECTOR WRITE HEAD 0,SECT 0 (15,50 MBYTE ONLY)	
61	FORCE END OF CYLINDER ERROR	
62	SEEK/WRITE SEQUENCE	
63	SEEK/WRITE SEQUENCE	

E SERIES — DRIVE FUNCTIONAL TESTS

64	WRITE/READ WITH DATA CHECK 9 PATTERNS	
65	WRITE/READ WITH DATA CHECK 3 CYLINDERS/ALL HEADS	
66	CHECK BOOTSTRAP FUNCTION	
67	ADDRESS CHECK VIA SEEK/WRITE ALL CYLINDERS	CYLND #
68	ADDRESS CHECK VIA SEEK/READ ALL CYLINDERS	CYLND #
69	SECTOR ADDR CHECK VIA WRITE ALL SECTORS	SECT #
70	SECTOR ADDR CHECK VIA READ ALL SECTORS	SECT #
71	HEAD ADDR CHECK VIA WRITE ALL HEADS	HEAD #
72	HEAD ADDR CHECK VIA READ ALL HEADS	HEAD #
73	SEEK/WRITE/SEEK/READ EXERCISER	ALT0
74	SEEK/WRITE/SEEK/READ EXERCISER	ALT1
75	VERIFY NEW TRACK ADDR REG VIA SEEK/RECAL/SEEK	

F SERIES — FORCED ERROR CHECKS

76	STEP TO DIAG TRACK	
77	FORCE ADDR ERROR VIA SECTOR BIT FLOAT	
78	FORCE ADDR ERROR VIA HEAD BIT FLOAT	
79	FORCE ADDR ERROR VIA CYLINDER BIT FLOAT	
80	CHECK BAD SECTOR FLAG	
81	FORCE DRIVE UNSAFE WITH DIAG CMND	
82	FORCE DRIVE UNSAFE READ AFTER FORMAT	
83	FORCE CRC ERROR WITH FORMAT/READ	
84	REFORMAT 0,0,0	
85	WRITE WITH FORCED BMC ADDRESS ERROR	
86	READ WITH FORCED BMC ADDRESS ERROR	

S SERIES — SEEK EXERCISER

87	WRITE ALL CYLINDERS HEAD=0, SECT=0	CYLND #
88	SEEK EXERCISER WITH READ CHECK	CYLND #

END OF TESTING

4.7.6 Diagnostic Error Reports - Detailed error and command summary information is printed on detection of an error. Additionally, tests that perform error checking issue a "probable failing FRU" report. This report identifies the first, second, third, and sometimes fourth most likely failing FRU for the detected error; e.g., controller PCB, media, read/write and clock PCB. The error report gives the operator information such as:

- The last command
- The last address issued before failure detection
- Status information down to the bit level.

For a detected error, the program prints the error PC, AC 0, 1, and 2 at the point of error, plus an option printout. The program then goes into a scope loop between entries to .SETUP and .LOOP allowing the operator to set SWPAK. In general the error PC points to a call error.

The option printout is done in one of the formats shown in Figure 4-24.

NOTE

The diagnostic program may or may not call out the correct failing FRU. Further investigation may still be required by referencing and then performing the procedure given in the diagnostic flowcharts (refer to subsection 4.2)

```
WHEN AN ERROR IS DETECTED THE PROGRAM PRINTS THE ERROR PC, AC'S
0,1,AND 2 AT THE POINT OF ERROR, PLUS AN OPTION PRINTOUT.  THE
PROGRAM THEN GOES INTO A SCOPE LOOP BETWEEN THE ENTRIES TO .SETUP
AND .LOOP ALLOWING THE OPERATOR TO SET SWPAK.  IN GENERAL THE ERROR
PC WILL POINT TO A CALL ERROR.

THE OPTION PRINTOUT WILL BE OF ONE OF THE FOLLOWING FORMATS:

A.  STANDALONE CONTROLLER TEST FAILURES-

    FAILING MODULE - DISK CONTROLLER

B.  STATUS ERRORS

    MODE     UNIT     #     DATA
    STARTING DISK ADDRESS
    CYL     #      HEAD              SECTOR  #
    AC1(STATUS) SHOULD =AC0
    DESCRIPTIONS OF FAILING STATUS BITS
    PROBABLE FAILING MODULES -(AS PER EACH FAILING BIT)

C.  MEMORY/DISK ADDRESS ERROR

    MODE     UNIT     #       DATA
    STARTING DISK ADDRESS
    CYL     #       HEAD     #              SECTOR  #
    ENDING MEMORY/DISK ADDRESS ERROR
    AC1(MA/DA) SHOULD =AC0

D.  INTERRUPT TIMEOUT

    MODE    UNIT    #         DATA
    STARTING DISK ADDRESS
    CYL     #       HEAD      #              SECTOR  #
    INTERRUPT TIMEOUT

ADDITIONAL TEST SIGNIFICANCE CAN BE FOUND IN THE PROGRAM LISTING,
ALTHOUGH IT IS HOPED THAT A NEED FOR THE LISTING WILL BE MINIMAL.
SWPACK (SWREG) WILL PROVIDE ALL CONTROL OVER TEST LOOP OPTIONS AND
PRINTOUTS.
```

Figure 4-24. Model 6280 Sample Error Report

CAUTION

Replacing the data module or reformatting the disks in the data module will destroy all stored data.

When you receive a failing FRU (module) report, replace one FRU at a time and rerun the diagnostic program. If the diagnostic fails in the same manner after replacing one FRU, reinstall the original FRU and then replace the other FRU called out by the error report and try again. Refer to Section 5 for replacement procedures.

If the medium is called out as a failing module, try reformatting before replacing the data module.

Additional test significance can be found in the program listing, although it is hoped that a need for the listing will be minimal. SWPACK (SWREG) provides all control over test loop options and printouts.

Before reformatting is done allow the customer to back up the disk if possible. Insure that the disk is in the middle of its operating temperature for best results.

Run the formatter with at least six passes of Verify to insure all bad spots are found. Verify that all bad spots labelled (from manufacturer) have been found - if not, manually flag these spots using SA 503 RELI: Bad Command.

Data errors cause the first three good/bad pairs and their addresses to be printed along with the total count. If a CRC error is detected, the call EHECC acknowledges the fact and returns to the main test for the data compare. Printouts result on the first error pass only. As the check routine checks the entire read buffer, any error accompanied by a CRC error, terminating the read, may cause all data in succeeding sectors to appear bad.

4.7.7 Special Notes/Features of the Diagnostic Program - The following information is helpful when using the diagnostic program.

1. If the disk has bad sector flags set on Cylinder 0 or 'DIAG', or on the first 8 sectors of Head 0 on any cylinder, error printouts result when the flags are encountered. The DIA status word will indicate that the bad sector bit is set and may or may not indicate a data error. These error printouts (that indicate a bad sector bit is set) should be ignored.

2. Some scope loops require a recalibrate to initialize the disk drive following a failure. Set SWPAK 8 = 1 to introduce the RECALIBRATE to the unit under test.

3. Identified FRUs:

FRU	Location
Disk controller PCB	Host CPU Chassis
Read/write and clock PCB	Model 6280 Chassis
Power supply PCB	Model 6280 Chassis
Head/Sealed Data Module	Model 6280 Chassis
BMC PCB	Host CPU Chassis

NOTE

In addition to the FRUs listed, a LSI chip on the controller PCB, and two transducers will be treated as FRUs to a limited extent. These three submodules are:

a. The Hard Disk Controller chip (HDC chip)
b. Home Transducer
c. Sector Transducer

4.8 THE RELIABILITY PROGRAM FOR MODEL 6280

The reliability program tests the subsystem for maximum disk activity and data transfer. Optional addressing and data patterns can be selected when running random and sequential exerciser programs. Seek exercisers check timing via converging/diverging and random seek patterns. The program executes a string of individual tests. A detailed log of all surface related addresses, as well as a summary of all errors and seek/write/read statistics is available by keyboard request.

CAUTION

The reliability program writes on the entire disk. If the disk cannot be backed up, do not run the reliability program.

Do not run 504 FORMAT unless absolutely necessary. All bad sector information will be lost. The 504 VERIFY program does flag bad sectors but may not find as many as the special test equipment used in the manufacturing test.

NOTE

Specific areas of the disk may be tested using a min/max Head/CYL option contained in the reliability program.

4.8.1 Loading Model 6280 Reliability Program - When using ADES, enter the following command to load the reliability program:

```
*SECR RELI
```

4.8.2 Reliability Program Tests - The reliability program contains several different test programs. Each program has its own SA as shown in Table 4-14.

4.8.3 Reliability Program Operator Questions and Answers Operator Responses - Table 4-15 lists the questions the operator answers to continue the reliability program. After the operator answers all the program responses, the program indicates test(s) are in progress by responding:

TESTING UNIT X

NOTE

DTOS starts the program at SA 505 on Load.

Table 4-14. Reliability Program Starting Addresses

SA (Starting Address)	Test Program
4	Change device code
11	Octal debugger - direct entry
200	DTOS Start - RUNALL (same as 505)
500	Random Reliability Test
501	Random Reliability Test, operator options
502	Incremental Disk Address Test
503	Command String Interpreter
504	Formatter/Verify
505	RUNALL (same as 200)
506	Converging/Diverging Seek Exerciser
507	Random Seek Exerciser
510	Statistics/Error Log recovery

Table 4-15. Questions Asked by the Reliability Program

Program Output	Notes
HELP ? (YES/NO) If HELP is requested, the following 4 categories of help are provided: 1. SWREG/CONSOLE CONTROL 2. STARTING ADDRESSES 3. DATA PATTERNS 4. COMMAND STRING	Help is only available on Program Load
SET SWPAK AS PER 8.0, HIT (CR) TO CONTINUE	
TTY BAUD RATE (DEC. #) =	Only asked if RTC is not present for programming timing.
INITIALIZE (YES/NO) ?	If no following questions bypassed.
START TIME ? MON, DAY, YEAR, HR, MIN	
UNITS TO TEST - 0	Only unit 0 is possible on the 6280 system
50,25,15,12,5 MBYTE OR QF (1.2 MB FLOPPY)	Unit 0 - 50
MIN/MAX HEAD LIMITS (2 NUMBERS)	Unit 0 - 0,1 (CR gets all)
LOWER/UPPER TEST TRACK LIMIT PAIRS	Unit 0 - 0,100 (CR gets all)
***SELECTED TEST OPTIONS (SEE 3.2)	
TESTING UNITS 0	Indicates test in progress

4.8.4 Operator Input Controlled Printouts -

L = FIRST 50 (decimal) ADDRESSES OF BAD SECTORS, DATA ERRORS, OR 20 (decimal) ADDRESS ERRORS

S = SEEK TIMING STATISTICS (507 ONLY)

W = SECTORS W/R PLUS ERROR COUNTS

NOTE

Any character typed will end printouts at the next change of data type.

4.8.5 Reliability Operating Modes - One of three Memory/Interrupt Modes may be used with the reliability program. These programs are:

Mode	Description
1. Background Only, Wait on Interrupt	One buffer is used for all writing and reading. Data read is checked by reconstructing each write data word, word by word. Used for SAs 503, 506, and 507.
2. Background/Foreground Modes, two buffers used for both Read and Write Purposes	One buffer is used for current I/O, while the other is used for checking read data from the previous read, and/or generating write data for the next write operation. Used for constant patterns.
3. Background/Foreground Modes, three buffers (two for Read and one for Write)	One Read buffer is used for current I/O, the other is used for checking the previous Read data. The common Write buffer is used for both current Write data and for checking the previous Read data, using a Buffer Compare. Used for variable data patterns.

4.8.6 Reliability Program Descriptions - The reliability program is made up of a series of smaller programs, each with its own starting address (SA). Table 4-16 describes and lists the starting addresses of these programs.

Table 4-16. Reliability Program Descriptions (Page 1 of 4)

SA	Program Name	Description
4	Change Device code	
11	Octal debugger - direct entry	The reliability program is equipped with a built-in ODT (octal debugging tool). For more information on using DTOS Summary Manual, Data General P/N 015-000082.
200	DTOS Start - RUNALL	See SA 505
500	Random Reliability Test	This program uses a random number generator to select a disk drive, cylinder, head and sector. Random data is then generated, written and read. This sequence repeats indefinitly. 1024. Seek/ Write/Seek/Read operations are executed per pass.

Table 4-16. Reliability Program Descriptions (Page 2 of 4)

SA	Program Name	Description
501	Random Reliability test with options	This test is the same as the previous test except that the operator is given the option of selecting data patterns and the choice of a constant cylinder, head, or sector. Any letter response to CYL, HEAD, etc. selects the random function for that variable. A CR (carriage return) selects the random function for all variables. All numbers entered above must be in octal. Any non-octal input is treated as a letter. Any letter input for CYC, HEAD, SECTOR gets random function in the reliability test with options.
502	Incremental disk address test	This option gives the operator the option of selecting data patterns. Requested data is first written over the entire disk surface, then data is read from all sectors. This ensures that the disk surface blocks are useable and formatted properly. The test is then repeated for all ready disks, and PASS is printed to the system terminal. This sequence is repeated indefinitely until manually stopped by the operator. NOTE: This test is not guaranteed to check every disk sector and is not a media verify. For media verification use SA 504 Verify.
503	Command string interpreter	This program allows the operator to type in test loops for troubleshooting. After starting at SA 503, three arguments must be entered in response to three program questions - UNIT, DATA and COMMAND STRING. All numbers must be entered in octal. The command string is limited to 116 (decimal) characters. UNIT: Type unit # or return to use the previous entry.

Table 4-16. Reliability Program Descriptions (Page 3 of 4)

SA	Program Name	Description
503	Command String Interpreter (cont.)	DATA: RAN = RANDOM DATA ALO = ALL ONES ALZ = ALL ZEROS PAT = 1 5 5 5 5 5 PATTERN ROT = 1 5 5 5 5 5 PATTERN ROTATED ON EACH PASS ALT = 0 5 2 5 2 5 PATTERN FLO = FLOATING ONE PATTERN FLZ = FLOATING ZERO PATTERN ADR = CYL (BITS 0-7) HEAD (BITS 8-10) AND SECTOR (BITS 11-15) VAR = EXISTING WORDS ENTERED PREVIOUSLY AS DESCRIBED BELOW Alternatively entered a string of up to 7 octal 16-bit words to be used as data. The words entered are used repeatedly to make up a sector block. Type return to use the previously entry.
504	Format/Verify program	This program gives the operator the option of either formatting or verifying the disk or both. A default (CR) gives both operations. If the format operation is requested, the disk is first formatted after which a format done message is printed. If a verify was requested, then a 1 5 5 5 5 5 pattern is written to the entire pack and read back and PASS is printed. The data pattern is then rotated 1 bit left and the write/read process repeated. When the number of passes specified by the operator are completed, a log is printed and the drive released. It is recommended that at least six passes (write/read) be allowed to ensure pack quality. If time permits, longer runs will further insure quality. Hard data or address errors set the bad sector flag for that sector. Soft data or address errors encountered twice also set the bad sector flag. Any non data related error prints out on the console and the program will stop testing on that unit, unless SW14(E)=1.

Table 4-16. Reliability Program Descriptions (Page 4 of 4)

SA	Program Name	Description
		NOTE This program is not intended to be a diagnostic program for the disk subsystem and in general assumes the control and drive to be properly operating. A hard address error is defined as; after two attempts have been made and both attempts result in an address error. A hard data error is defined as; after up to eight read retries have been made and one or more of the retries has been unsuccessful.
505	RUNALL	This program sequences through the following programs in a "top down" fashion: SA 501 - PAT, RAN, FLZ, FLO SA 502 - ROT (3 times), RAN, ADR, ONES, ZEROS, ALT SA 507 - Random seek exerciser.
506	Seek exerciser	This program provides a seek scan sequence converging from the extreme outermost tracks into the adjacent center track and then diverging again to the extremes. All seeks are followed by a one sector read with no data check. All seeks are timed with maximum, minimum, and average times logged in milliseconds. Seek paths for maximum and minimum values are also logged. This is a read only program and requires that the disk pack be previously written to.
507	Random seek exerciser	This is the same as SA 506 except that the seek sequence is random.
510	Error Count/Log recovery	In the event a program stopped during a run, the error logs may be recovered at this starting address. This must be done before any program restarts as the program initialization zeros all logs.

4.8.7 Command String Interpreter for the Reliability Program - This program is an aid which allows the user to type in test loops. The program starts at SA 503. Once started the program responds by asking the following questions.

```
UNIT:
DATA:

COMMAND STRING:
```

The unit number is 0. The data can be either a data pattern or any specified data (data must be all octal numbers). The command string can consist of either one or a combination of the following commands.

```
COMMAND STRING:

1.  READ              HEAD, SECTOR, # SECTORS
2.  WRITE             SAME
3.  SEEK              CYLINDER
4.  RECALIBRATE
5.  LOOP              (GO TO BEGINNING OR LR)
6.  DELAY             N (N= DELAY IN MS)
7.  LR                (BEGIN LOOP HERE)
8.  FORMAT            CYL, HD, SEC
## NOTE A FORMAT:     1.  WILL DESTROY DATA AT THE SPECIFIED SECTOR
                      2.  MUST BE FOLLOWED WITH A WRITE (ANY DATA
                          PATTERN) TO THE SPECIFIED SECTOR
9.  BAD               (SET BAD SECTOR FLAG) CYL, HEAD, SEC
## NOTE A Seek is included in Options 8 and 9.
10. RDH HEAD          SECTOR -READ HEADER
11. RWH HEAD          SECTOR - READ WITHOUT HEADER CHECK.
12. NOP               DISK NOP COMMAND
13. TYPE CARRIAGE RETURN ONLY TO USE THE PREVIOUS COMMAND STRING.
```

For example, the following command string causes unit 1 to seek cylinder 50. It then repeatedly writes sector 2 using head 5, reads it back and checks the data. The data is specified as alternate words of zeros then ones.

```
UNIT:  1
DATA:  0,177777
COMMAND STRING:  SEEK 50 LR WRITE 3,2,1 READ SAME LOOP
```

A space or a comma may be used as an argument delimiter. Each response is terminated by hitting the "CR" key. If more room is needed on a line, hit the "NEW LINE" key on the system terminal. Typing the word "SAME" when used with a Read or Write will cause the previous disk address parameters to be used.

Typing an "R" while a string is being executed will cause the program to return to the unit prompt. The "ESC" (escape) key, when hit, will bypass the Unit and Data prompts and default to the Command String prompt.

4.8.8 Reliability Error and Statistics Logs - The reliability program maintains an error log and statistics log during operation. To access the error log, hit the "L" key on the system terminal. The error log gives the user information concerning: the first 50 (decimal) disk addresses of bad sectors and data errors. The first 20 (decimal) address errors and seek errors (seek path). If error addresses are encountered more than once (first pass), a count of up to 32 (decimal) will be recorded in the log. A count of up to 15 (decimal) hard errors will also be recorded. This count will be a subset of the first count. The address information will be in octal while the counts will be decimal.

To access the reliability statistics log during testing hit the "W" key on the system terminal. The log will list the number of sectors written (and/or) read, plus the error counts in decimal.

Seek timing statistics can be accessed by hitting the "S" key on the system terminal while running either seek exerciser.

NOTE

A ^S will stop the error listing at any time and a ^Q will restart it.

The program will account for up to a maximum of 2**31 sectors written or read. Special test runs exceeding this facility will require an operator's test log to augment software accounting. 2**31 sectors = approximately 5.5* 10**11 words.

4.8.9 Reliability Program Output/Error Description - All errors are identified, counted and the program is routed via base to a call to CKSW. On the basis of switch option settings (see 4.8.10) the program will go into a scope loop, or proceed, depending on the SWPAK settings.

If Loss of Ready with a single drive, the program will print the appropriate error message and exit to the Octal Debugger (ODT). The same also applies to loss of Write Enable if the program is in a write mode.

During a recalibrate any unusual status is reported immediately and an error return is executed.

Table 4-17 describes the different error types.

Table 4-17. Reliability Error Descriptions (Page 1 of 3)

Error	Description
Seek	Any error status results in a status printout and error return. A recalibrate will be performed by the error handler. The program will log the first 20 (decimal) cylinders to/from on finding seek errors.

Table 4-17. Reliability Error Descriptions (Page 2 of 3)

Error	Description
Write	Following a "DONE" on a write, errors are checked in the sequence shown below. The error recovery procedure is outlined for each case. If an error is not present the next check is made. 1. Operation Timeouts or any Other Drive Faults - Increment the appropriate error count, print the illegal status and do an error return. Any drive fault will cause a recalibrate to be performed by the error handler. 2. Address Error - Repeat the write. If the test passes the second time, increment the soft address error count and do a normal return. Otherwise increment the hard address error count and do an error return. If a hard address error occurs, a read on an adjacent head will be attempted to determine whether the fault should be classed as a seek error or an address error. The first 20 (decimal) address errors will have their addresses logged. 3. Bad Sector - Log the disk address (first 50 [decimal]) and do a normal return. No printout will result unless SW11=1, although the I/O operation was prematurely terminated. A "soft" error will be recorded if the sector under test passes at least one of four retrys. The log denotes soft errors by a count greater than 0, representing the error count tallied. 4. Ending Memory Address - Increment the memory address error count, print the error message, check for a disk address error and do an error return.
Read	All read errors with the exception of data related errors are handled the same as described for a write operation.
Data	Data is reread three times (four times if a CRC is undetected). If the data is bad all four tries, a hard error count is incremented and an error return is taken. If data is good on any four tries, a soft error count is incremented and a normal return is taken.

Table 4-17. Reliability Error Descriptions (Page 3 of 3)

Error	Description
	The disk address of all data problems will be printed and the first 50 (decimal) will be logged. The first three good/bad word pairs and respective addresses will be printed. If SWPAK9=1 (bypass data check) hard or soft data errors will be determined by CRC status.

4.8.10 Reliability Switch Register (SWREG) Options - The user can control program operation by setting bits into the SWREG. While running under this location is loaded by the monitor. Under stand alone and program load modes this location is set according to the answers supplied by the operator. In any case the options can be changed or verified by one of the commands listed in subsection Reliability Switch Commands (see 4.8.11). The definition of the SWREG bits are listed in Table 4-18.

Table 4-18. Definitions of SWREG Bits, Reliability Program (Page 1 of 2)

Bit	Octal Value	Binary Value	Interpretation
1	40000	0	Loop on hard error
		1	Skip looping on hard error
2	20000	0	Print to console
		1	Abort printout to console
5	02000	0	Do not print on the line printer
		1	Print on the line printer
6	01000	0	Do not exit on hard error
		1	Exit to ODT on hard error
8	00200	0	Not Applicable
		1	For read only mode (SA 501, 502)
9	00100	0	Not Applicable
		1	Bypass data check
11(B)	00020	0	Not Applicable
		1	Enable hard bad sector printouts
13(D)	00004	0	Not Applicable
		1	Print I/O trace on hard error (last 5 I/O call PC's + commands)

NOTE

14(E) and 15(F) apply only to SA 504/Formatter

Table 4-18. Definitions of SWREG Bits, Reliability Program (Page 2 of 2)

Bit	Octal Value	Binary Value	Interpretation
14(E)	00002	0 1	Exit on non-surface related errors Do not exit on non-surface related errors. (i.e., CRC, HEADER, or BAD SECTOR are surface-related errors)
15(F)	00001	0 1	Do not loop on last format operation Loop on last format operation (for scope loop)

4.8.11 Reliability Switch Commands - Once the program starts executing the state of any of the bits may be changed by hitting keys 1 - 9, A - F. The program will continue running after updating the options. To change the bit value in the register, strike the respective number key on the terminal (i.e., to change the 4 bit value, strike the 4 key). Setting of any bit of location "SWREG" will set bit 0 (The default mode is defined as all bits of SWREG set to 0).

4.8.12 Other Reliability Commands - (^ = Control Key)

"CR" A "RETURN" can be typed to continue the program after its locked in a switch modification mode.

^D This command, given at any time, resets "SWREG" to default mode and restarts the program.

^R This command, given at any time, restarts the program. Switches are left with the values they had before the command was issued.

^O This command, given at any time, causes the program control to go to ODT (this is an optional command and available if ODTPK is present).

M This command, given at any time prints the current operating modes.

O This command, given at any time, locks the program into switch modification mode where more than one bit can be changed.

4.8.13 Octal Debug Tool (ODT) - This diagnostic is equipped with a built in ODT which can be accessed by typing a CTRL O (^O) at any time during program execution (after setting parameters). On entering ODT the address of the location having the next instruction to be executed will be typed-out.

4.8.13.1 ODT Conventions and Symbols - The following conventions are used by the ODT:

?	Pressing any illegal key causes the ODT to respond with a "?".
*	ODT is ready and at your service.

4.8.13.2 ODT Command Structure - An ODT command has the following format:

[ARGUMENT] [COMMAND]

An argument may be one of the following:

"EXP"	An octal expression consisting of octal numbers separated by plus (+) or minus (-) signs. Leading zeros need not be typed.
"ADR"	An address is the same as an expression except that bit 0 is neglected.

A command is a single teletype character.

4.8.13.3 ODT Commands - Locations that can be examined and modified by the user are called cells. There are two cell types:

Internal CPU cells and Memory locations

Opening Internal Cells - The command to open one of the internal registers is "NA". N is any octal expression between 0 and 7. The expressions are defined as:

0 - 3	For accumulators 0 - 3
4	For PC of the next instruction to be executed in the event of a "P" command.
5	CPU and TTO status

Bit	Interpretation
15	Status of TTO Done flag
14	Status of interrupts (Ion flag)
13	Status of carry bit

6	Address of the location having the break point (if any)
7	Instructions at the break point location

Additional commands to open cell are:

"ADR"/	Open cell and print its contents
./	Open the cell currently pointed to by the pointer and print its contents
.+"ADR"/	Add "ADR" to the pointer, open the cell and print its contents
.-"ADR"/	Subtract "ADR" from the pointer, open the cell and print its contents
"CR"	The return key is used to close the open cell with or without modification
"LF"	Line feed is used to close the open cell with or without modification and to open the succeeding cell
^	Close the open cell with or without modification and open the preceeding cell
/	Close the open cell without modification, and open the cell pointed to by its contents
+"ADR"/	Close the open cell without modification, and open the cell pointed to by its contents - "ADR".
-"ADR"/	Close the open cell without modification, and open the cell pointed to by its contents - "ADR".

Cell Modification - Once a cell has been opened its contents can be modified by typing the new value the cell is to contain in the form of an octal expression followed by "CR" or "LF". If a + or - is typed as the first character of the expression then the value of the expression is added to or subtracted from the contents of the cell. The address itself or an expression relative to the address can be deposited by typing a "." or ".+/-octal expression". A rubout command given right after opening a cell allows the modification of its contents as if they were typed in just before the command was issued.

Other ODT Commands -

RUBOUT	This key is used to delete erroneously typed digits. Each time the key is pressed the right most digit is deleted and echoed on the terminal. If the rubout key is pressed right after opening a cell, then it deletes the right most digit of the cell's contents. This allows the modification of the cell as if its contents were typed in just before the key was depressed.
"ADR"B	Insert a break point at location "ADR". Only one break point can be inserted and any entry to ODT after executing a break point will cause it to be deleted.

D	Delete the break point if any.
P	Restart the execution of the program at location pointed by 4A.
"ADR"R	Start executing the program at "ADR" after an IO-reset.
K	Kill the string typed so far. The ODT responds with a "?" and the open cell is closed without modification.
=	Print the octal value of the input only. This will close any open cells without modification and will not open a cell.
C	Core dump, user is asked for starting/ending addresses. Dump will also go to printer if SWREG bit 5 is on.

NOTE

In programs which relocate themselves the user should place break points only in the original program area. If a break point is placed outside this area the results will be unpredictable.

SECTION 5

REMOVAL AND REPLACEMENT PROCEDURES

This section provides detailed instructions on the removal and replacement procedures for the 6234 disk subsystem FRUs. The following is a list of the removal and replacement procedures. Also included in this section is a procedure to align the home transducer, and a procedure for using the sector transducer spare.

CAUTION

In all removal procedures the disk subsystem is to be powered down prior to performing the procedure.

CAUTION

All PCBs contain MOS devices. These devices are sensitive to static electricity and must be protected by special handling and packaging. The pink ziplock bag has a soap film coating. If this bag becomes scratched, it looses its nonconductive properties.

Two types of plastic envelopes are used for shipments of PCBs:

1. Velostat (antistatic, conducting) -black
2. Sentinel ASF919 (antistatic, nonconducting) -pink

Use the following guidelines to ensure proper handling of the PCBs.

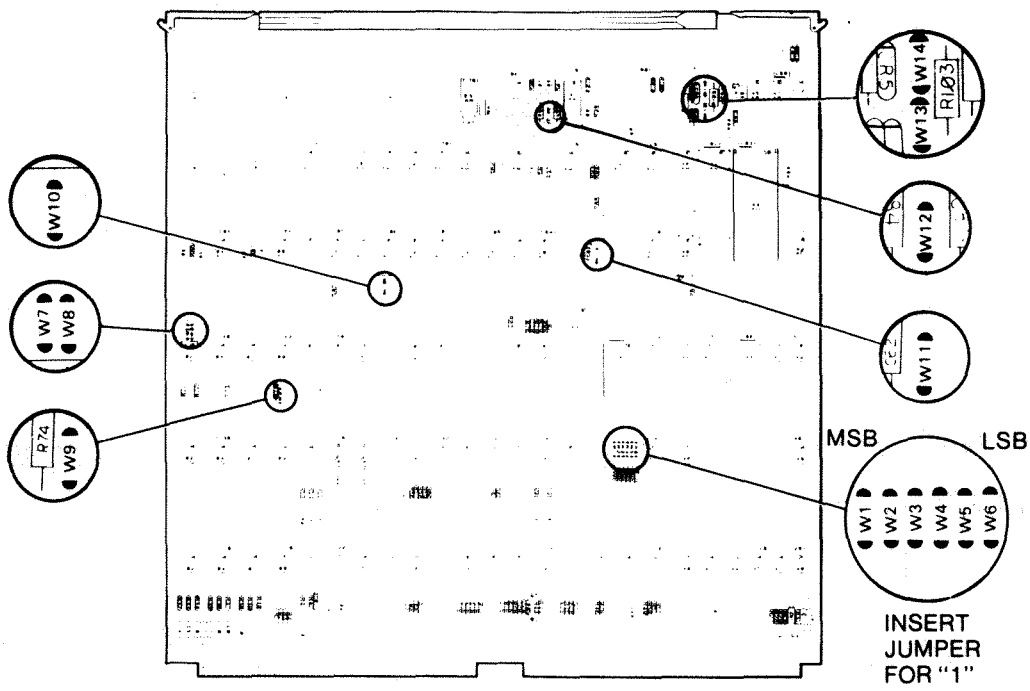
- Unpack the PCBs at the installation site only. Do not discard the packaging envelopes.
- Touch a grounded object to eliminate static electricity before unpacking the PCB.
- Place the PCBs on the plastic bags when installing or removing jumpers. Never slide PCBs across a table top or other surface.
- Handle the PCB by the edges to avoid skin contact with the components.
- Use the same envelopes and packing material for PCBs returned for repair.

5.1 CONTROLLER PCB REPLACEMENT

NOTE

The controller PCB for the disk subsystem is located in the host CPU. Observe MOS caution when handling.

1. Power down the host computer (refer to the CPU FRU or operator manual for the proper procedure).
2. Remove any CPU panels required to expose the PCB.
3. Determine which CPU chassis slot the disk subsystem controller PCB is in, note, and remove.
4. Check and match the replacement controller PCB jumpering against the controller PCB just removed. See Figures 5-1 and 5-2 for correct jumper locations.



JUMPER NOTES:

1. JUMPERS W1 AND W6 ARE DEVICE CODE SELECTION JUMPERS.
2. JUMPERS W8, W11 AND W12 ARE IN.
3. JUMPERS W7 AND W10 ARE OUT.
4. W14 IS IN FOR ALL CPU'S EXCEPT MV/4000, 6000, 8000,10000.
5. W13 IS IN FOR MV/4000, 6000, 8000, 10000.
6. IF ONE DISKETTE AND ONE HARD DISK ARE ATTACHED, W9 IS IN.

CONTROLLER DEVICE CODE SELECT		
JUMPER NUMBER	DEVICE CODE 33	DEVICE CODE 73
1	OUT	IN
2	IN	IN
3	IN	IN
4	OUT	OUT
5	IN	IN
6	IN	IN

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Figure 5-1. 6234 CPU Controller Jumpering

Ref DGC Dwg No 003-001911 Rev 02

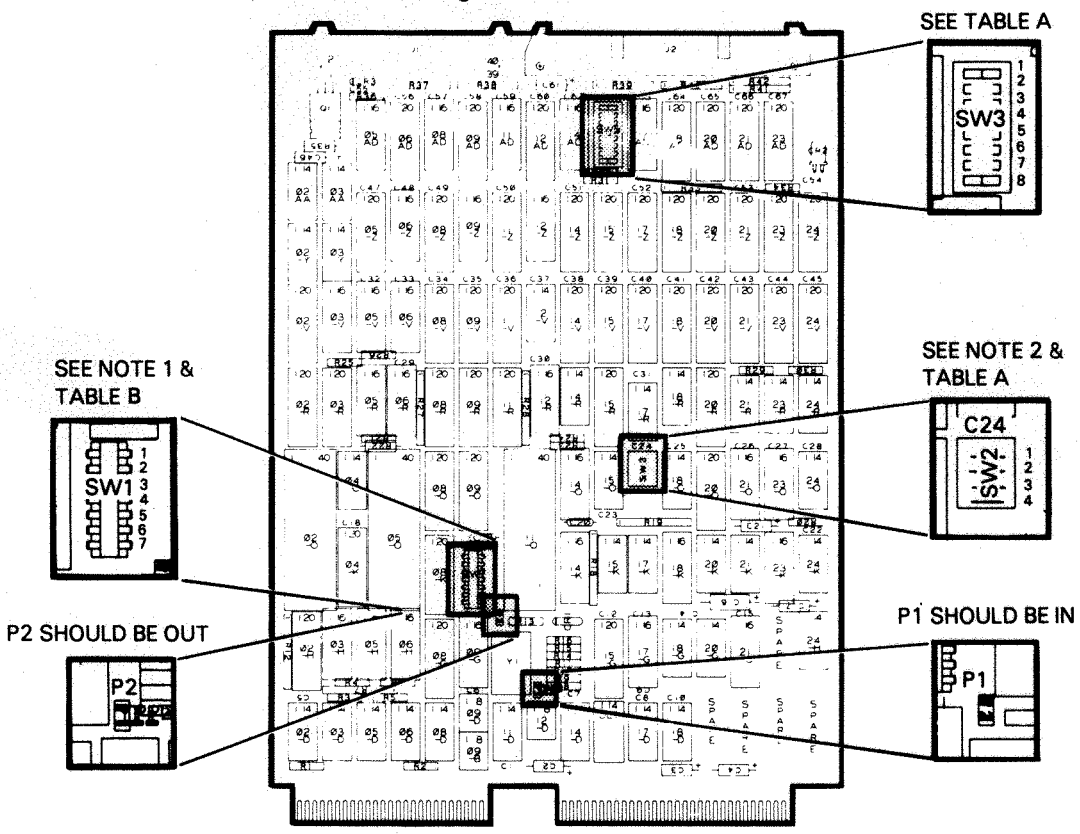

TABLE A

PRIORITY SELECT	S2			S3
	SW4	SW3	SW2	
HSCR7	ON	ON	ON	SW8
HSCR6	ON	ON	---	SW7
HSCR5	ON	---	ON	SW6
HSCR4	ON	---	---	SW5
HSCR3	---	ON	ON	SW4
HSCR2	---	ON	---	SW3
HSCR1	---	---	ON	SW2
HSCR0	---	---	---	SW1

TABLE B

S1	DEVICE CODE (OCTAL)	
	25	65
SW1	OFF	ON
SW2	ON	ON
SW3	OFF	OFF
SW4	ON	ON
SW5	OFF	OFF
SW6	ON	ON

NOTE:
TO SELECT BMC PRIORITY LEVEL 0-7, SET SWITCHES 2-4 OF S2 AS SHOWN AND TURN ON ONE SWITCH IN S3 AS INDICATED.

SWITCH NOTES:
1. SW1 TO SW6 OF S1 ARE DEVICE CODE SELECTION SWITCHES CORRESPONDING TO DS0 TO DS5 RESPECTIVELY, SWITCH ON FOR A-1, SW7 NOT USED.
2. SW1 OF S2 SHOULD BE ON.

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Figure 5-2. 6280 CPU Controller Jumpering

6. For Model 6280, check that the external I/O cable is securely attached to the PCB "A" connector. Replace the BMC cable removed from J2 of the controller PCB. If the BMC cable connected at J2 ends there should have been a terminator plug connected on J1 of the controller PCB. Install the terminator on the replacement controller PCB.

7. Replace the removed CPU panels.

8. Power up the host CPU (refer to the CPU FRU or Operator's Manual for power up procedures).

5.2 TOP COVER REMOVAL/REPLACEMENT

1. Power disk subsystem down and disconnect ac power cable from ac power source.

2. Remove the two screws that secure the disk subsystem to the cabinet.

3. Pull the disk subsystem forward on the cabinet slides.

4. Remove four M3 housing cover retaining screws (see Figure 5-3).

5. Remove housing cover.

6. To replace cover, align the enlarged screw holes in the housing cover with the screw holes in the disk housing frame.

7. Insert and tighten the four M3 housing cover retaining screws.

8. Push the disk subsystem back on the cabinet slides to a fully stopped position.

9. Replace the two screws that secure the drive to the cabinet.

10. Reconnect the ac power cord to the ac power source.

5.3 BOTTOM COVER REMOVAL/REPLACEMENT

1. Power disk subsystem down and disconnect ac power cable from ac power source.

2. Remove the two screws that secure the disk subsystem to the cabinet.

3. Pull the disk subsystem forward on the cabinet slides.

4. Loosen the four M3 housing cover retaining screws (see Figure 5-3).

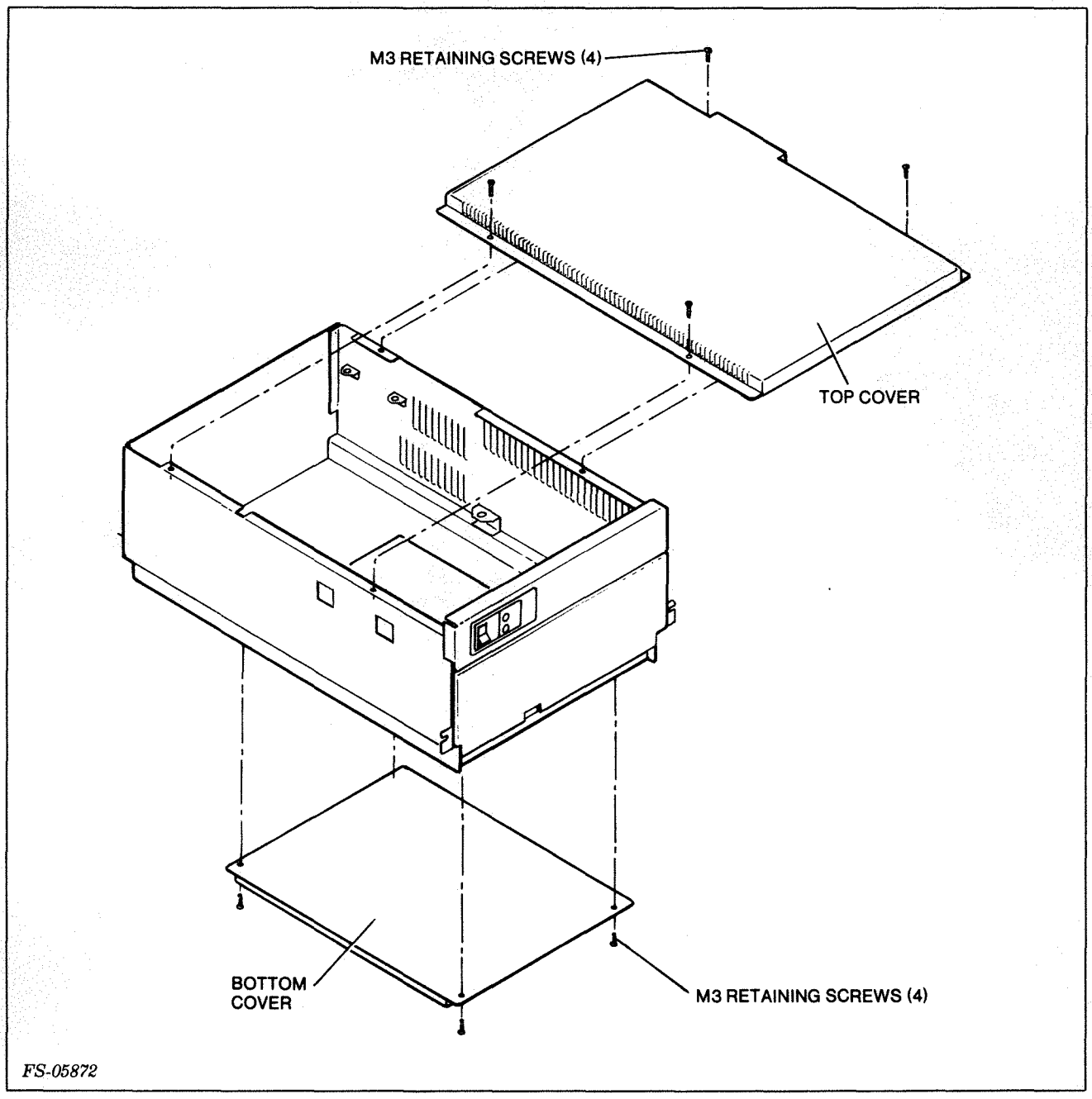


Figure 5-3. Top and Bottom, Cover Removal

5. Slide the cover so that it disengages from the retaining screws and remove the bottom cover.

6. To replace the cover, align the enlarged screw holes of the cover with the screw holes in the disk housing frame.

7. Tighten the four M3 housing cover retaining screws. Ensure that the flat washers are in place prior to tightening each M3 retaining screw.

5.4 BELT REPLACEMENT (DG 118-001740)

1. Power down the drive and remove the bottom cover (see 5.3).

CAUTION

Do not turn the pulley counterclockwise. This can damage the read/write heads. Observe the direction label on the bottom of sealed data module for pulley direction.

2. Turn the sealed data module pulley clockwise (see Figure 5-4) and apply downward pressure on the belt until the belt slips off.

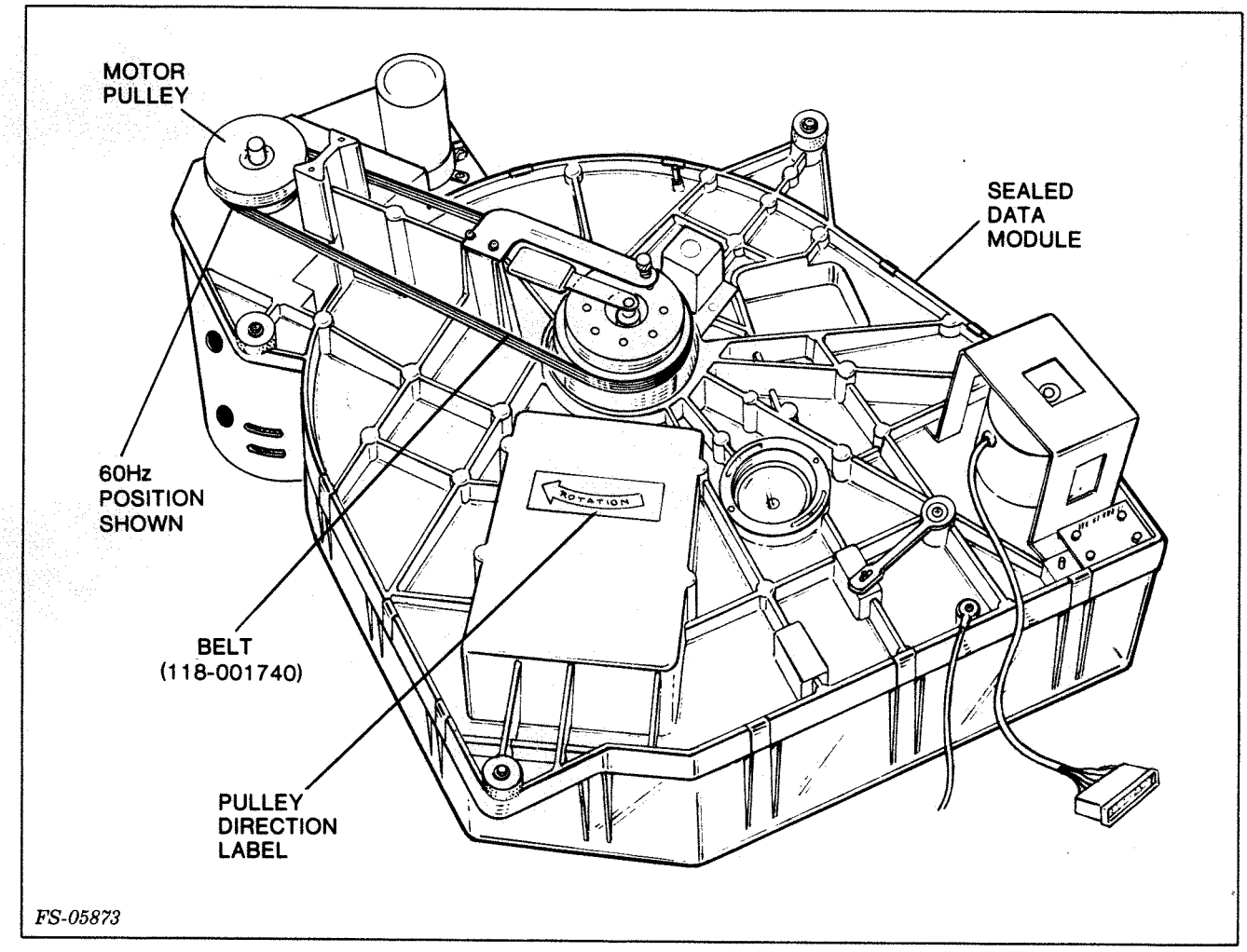


Figure 5-4. Sealed Data Module Belt Replacement

3. Place the new belt (DGC 118-001740) on the motor pulley and turn the sealed data module clockwise while pressing inward on the belt.

4. Turn the motor pulley clockwise to allow the belt to center on the pulleys.

5. Reconnect the ac power cord and power up the drive to check the belt position.

6. Power down the drive and replace the bottom cover (see 5.3).

5.5 SPINDLE MOTOR REPLACEMENT (005-009921)

Use the following special adhesive to complete this procedure.

Description	DGC P/N
Loctite adhesive	120-000007

1. Power down the drive, unplug the line cord, and remove the top and bottom covers (see 5.2 and 5.3).

2. Remove the belt (see 5.4).

CAUTION

Do not turn the pulley counterclockwise. This can damage the read/write heads.

3. Loosen the four screws that hold the back cover to the drive. Slide the cover up and away from the drive. Now hook it to the back of the drive (see Figure 5-5).

4. Unscrew the pulley setscrew and remove the pulley from the motor shaft (see Figure 5-6).

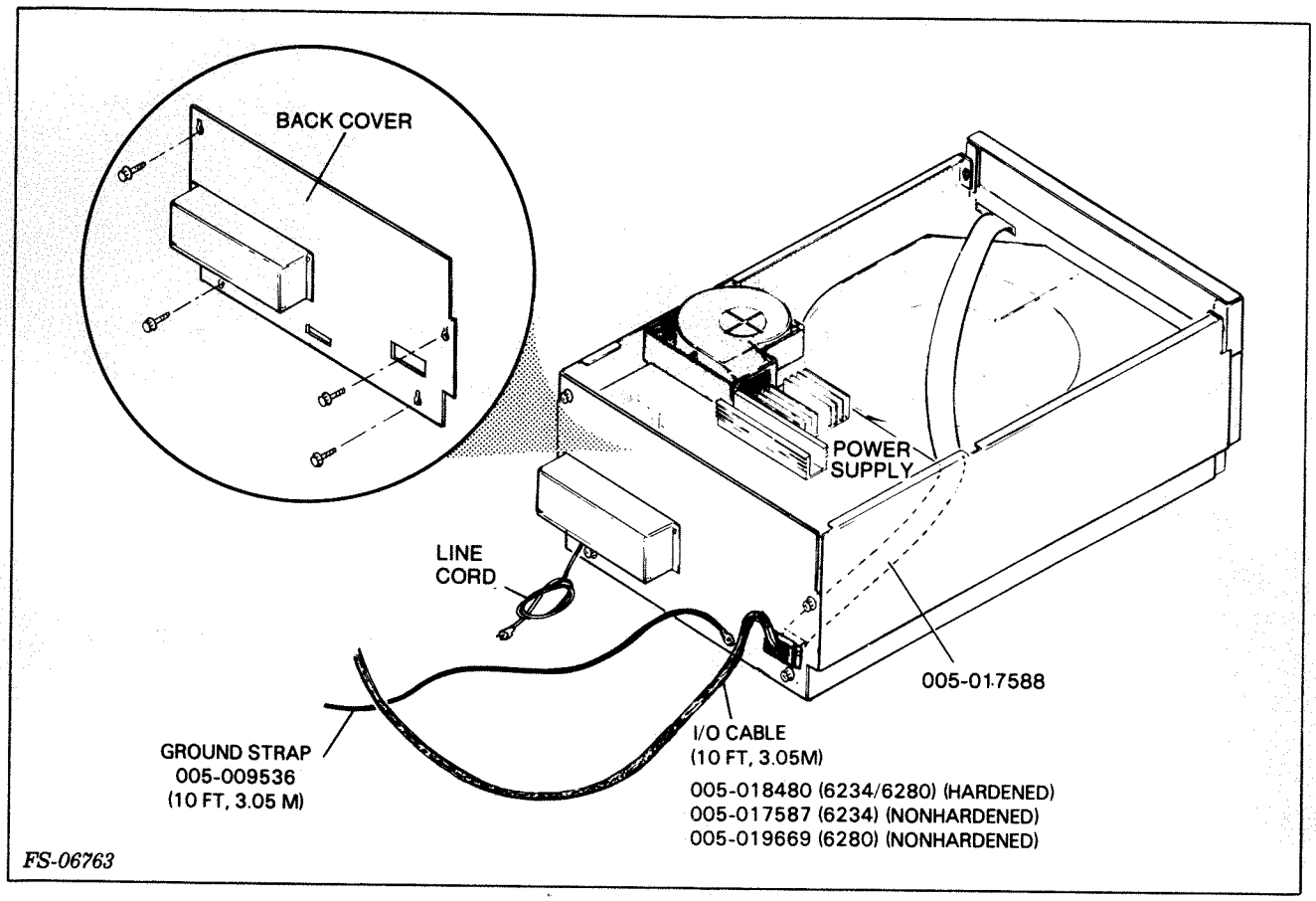


Figure 5-5. Rigid Disk Drive, Back Cover Removed

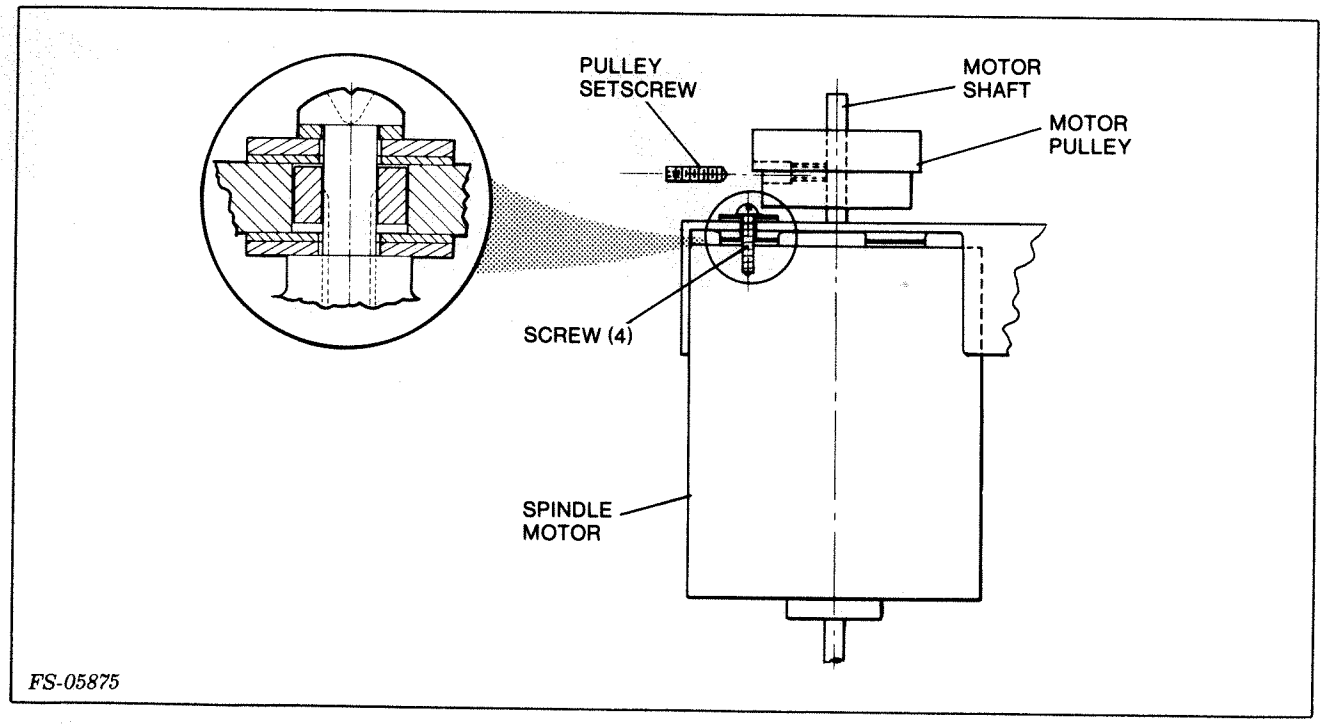


Figure 5-6. Spindle Motor with Motor Pulley

5. Unscrew and remove the three screws that hold the blower cover to the base plate and remove the cover. Now pull the blower wheel off of the motor shaft (see Figure 5-7).

6. Unscrew the four screws that hold the base plate of the blower assembly to the motor, and remove the base plate (see Figure 5-7).

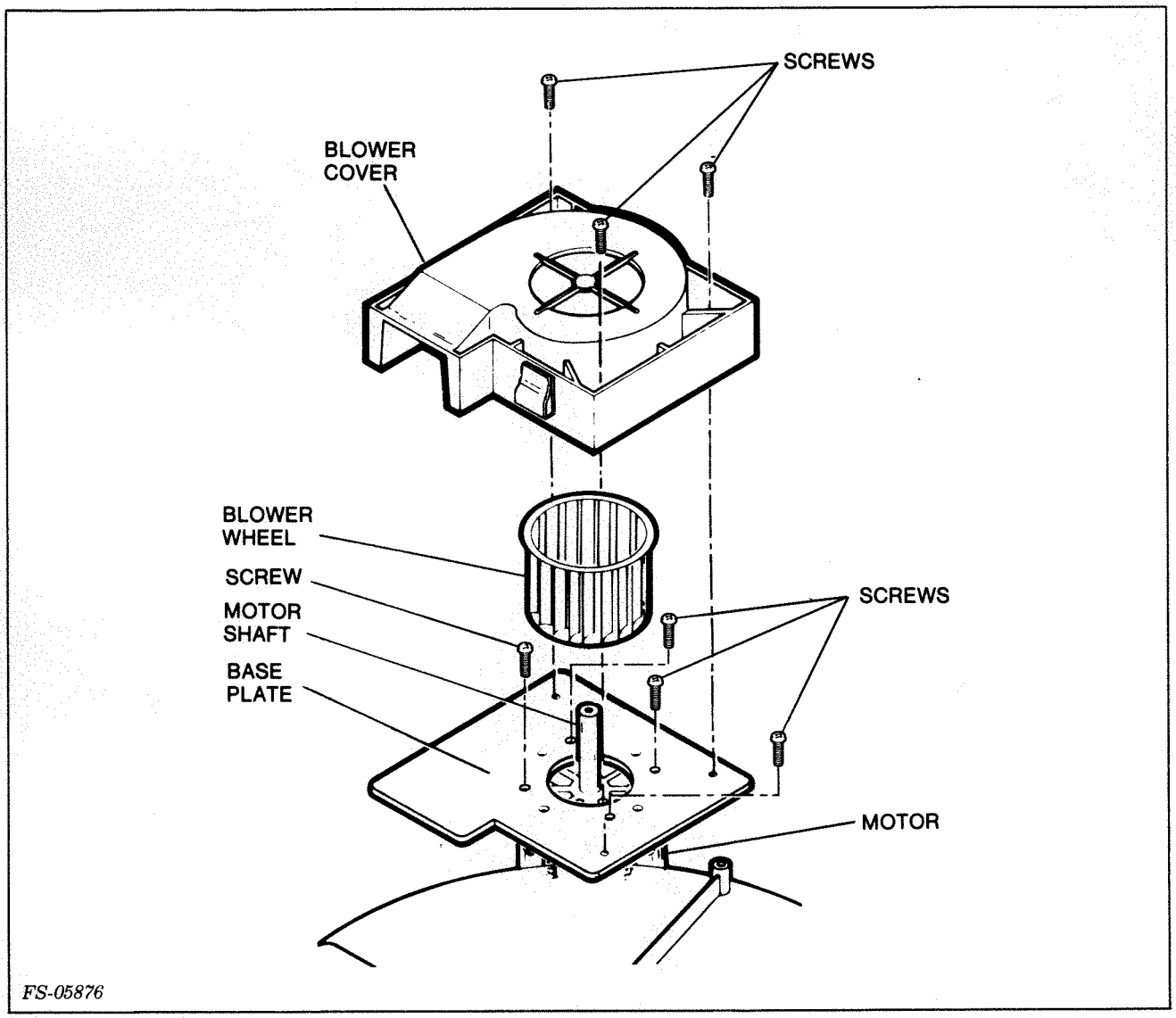


Figure 5-7. Blower Assembly (Exploded View)

7. Unplug the connector at J3 on the ac power PCB (see Figure 5-8) and disconnect the two wires connected to the capacitor.

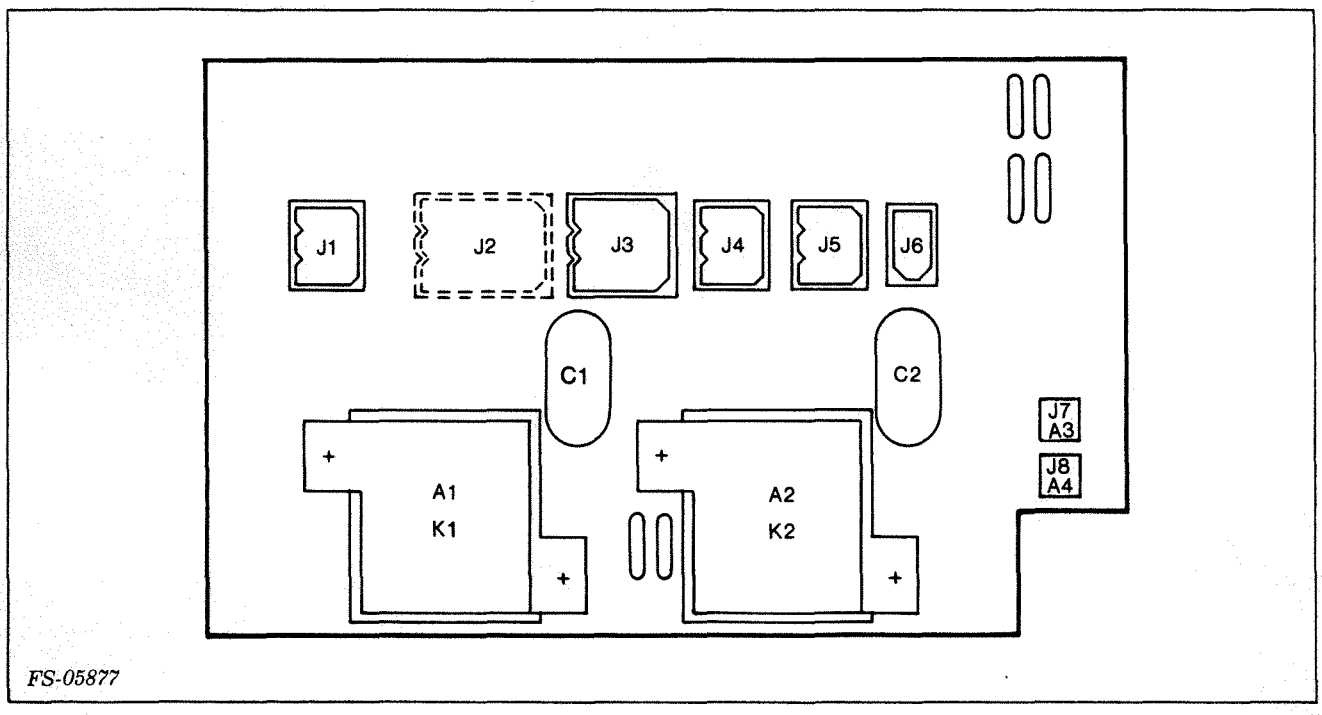


Figure 5-8. AC Power Distribution PCB, Connectors

8. Unscrew the four 8/32 x 3/4 screws (see Figures 5-4 and 5-6) that hold the spindle motor to the casting and remove the spindle motor. Remove the washers and insulators shown in Figure 5-9.

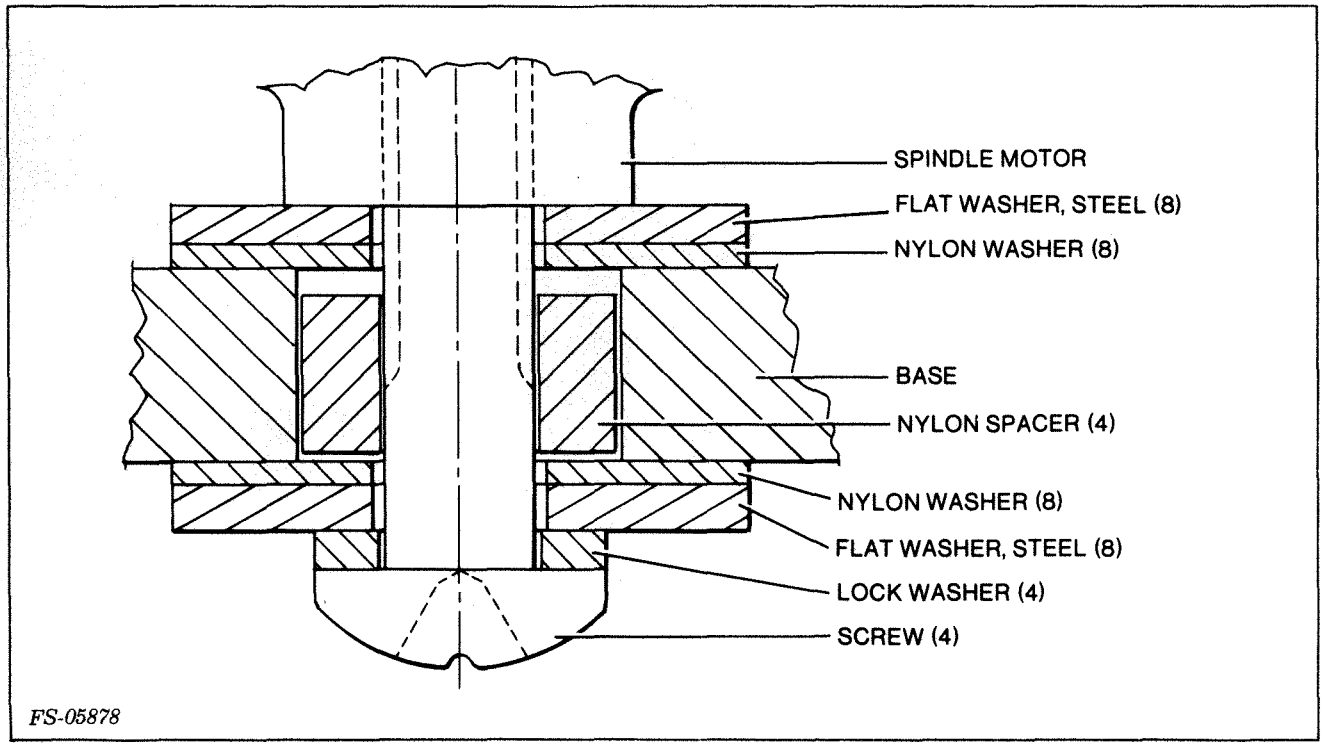


Figure 5-9. Spindle Motor Mount Assembly

9. Place the new spindle motor on the casting. Replace the washers, insulators and screws (see Figure 5-9). Tighten screws.

10. Plug the motor connector into the ac power PCB at J3 (see Figure 5-8) and reconnect the two wires to the capacitor.

11. Place the base plate on the motor. Insert the four retaining screws and tighten.

12. Put the blower wheel on the motor shaft. Now place the cover over the blower wheel and secure it with three retaining screws.

13. Place the pulley on the motor shaft and ensure that it does not rub on the base plate screws. Align the setscrew hole in the pulley so that it is parallel to the flat on the shaft.

14. Set a straightedge along the bottom of the sealed data module spindle pulley and adjust the spindle motor pulley to the same height as the spindle pulley (see Figure 5-10). The straightedge must make contact with at least one point on the motor pulley.

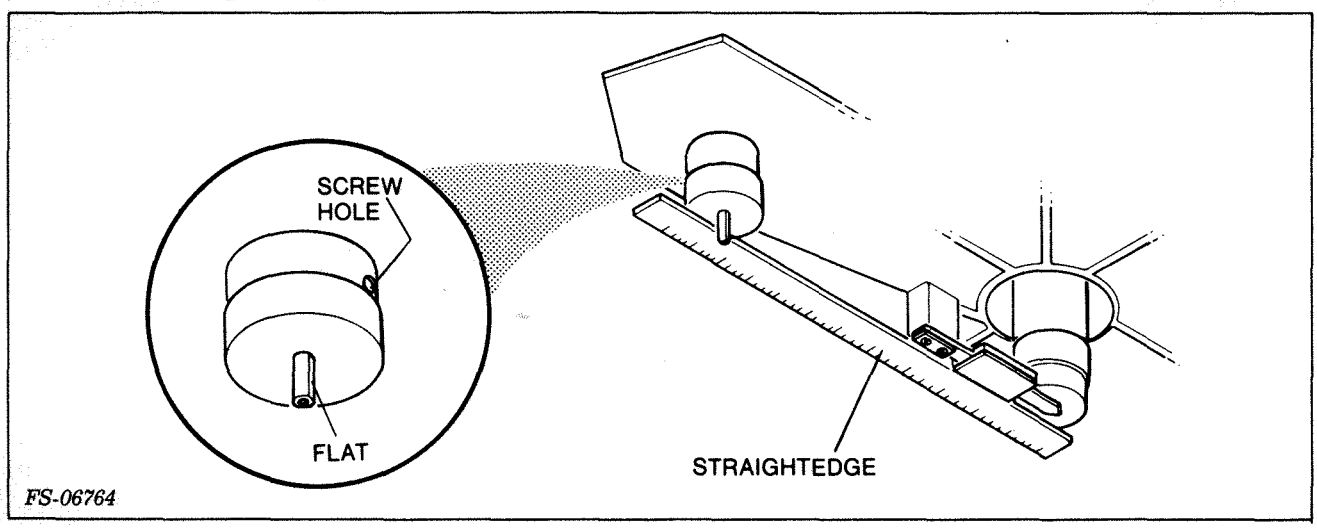


Figure 5-10. Spindle Motor Pulley Adjustment

15. Put a drop of Loctite on the setscrew. Insert the setscrew into the pulley and adjust torque to 13 in-lbs.

16. Unhook the cover from the back of the drive and place it in the operating position. Tighten the four retaining screws.

17. Place the belt on the motor pulley and turn the sealed data module clockwise while pressing inward on the belt.

18. Plug in the ac line cord.

19. Adjust the belt so that it rides on the middle of each pulley. Power up the drive and check the belt position.

20. Replace the top, bottom, and back covers.

5.6 SEALED DATA MODULE REPLACEMENT (DGC 005-017589)

1. Power down the drive, unplug the line cord and remove the top and bottom covers (see 5.2 and 5.3).

2. Unscrew and remove the three screws that hold the blower cover to the base plate and remove the cover. Now pull the blower wheel off of the motor shaft (see Figure 5-7).

3. Remove front dress panel and RF cover to reach the read/write and clock PCB.

4. Unplug J3, J4, and J6 from the read/write and clock PCB (see Figure 5-11). Mark J4 for correct position as to which sector transducer is in use.

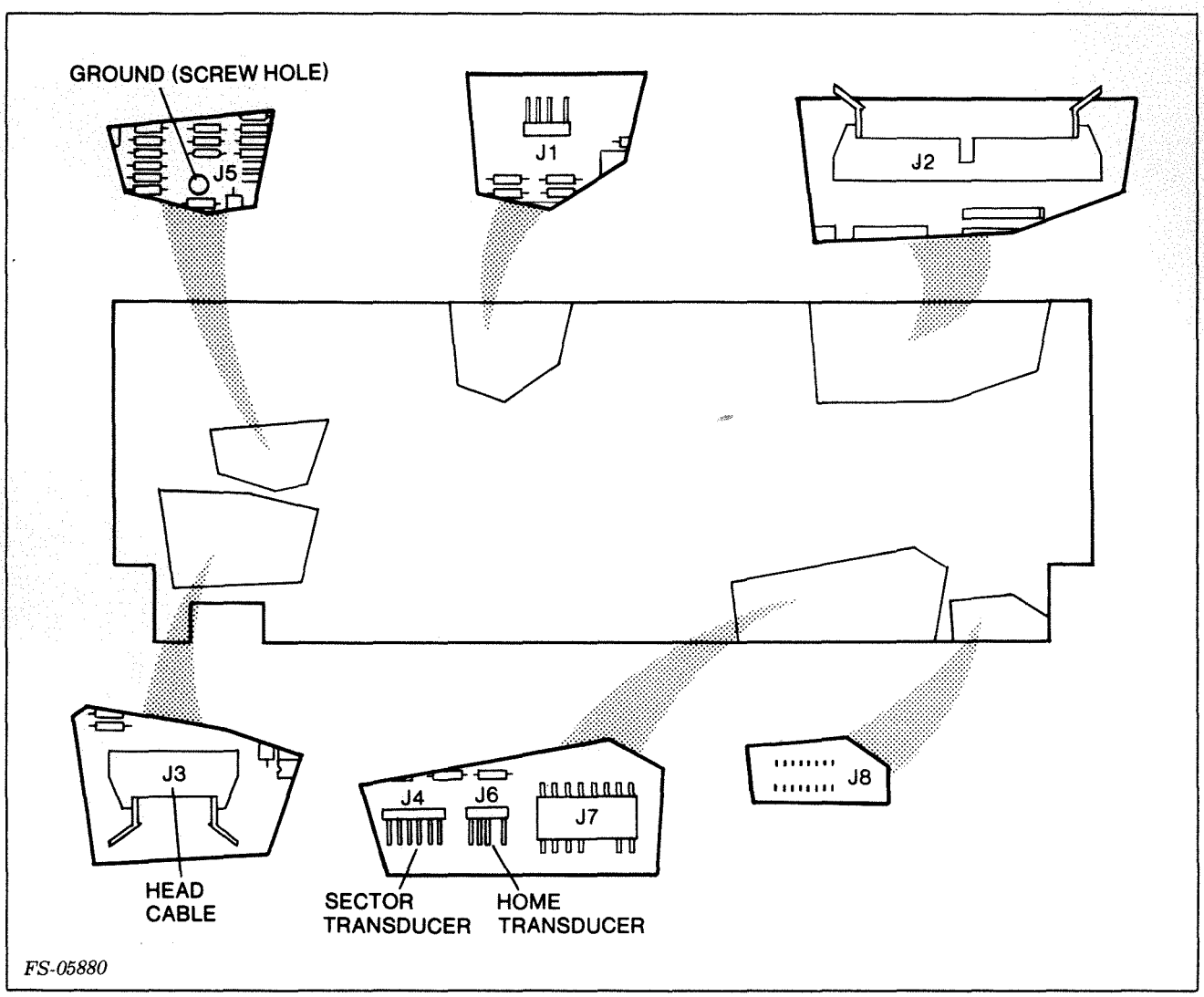


Figure 5-11. Read/Write and Clock PCB Connectors

5. Unplug J3 from the ac power distribution PCB (see Figure 5-8).

6. Remove the power switch (leave switch wires in place).

7. Remove the ground cable quick disconnect terminal running from the power supply to sealed data module at the power supply.

8. From the bottom of the drive, unscrew the three shock mount nuts that hold the sealed data module to the casting (see Figure 5-12). Remove the sealed Data Module from the drive.

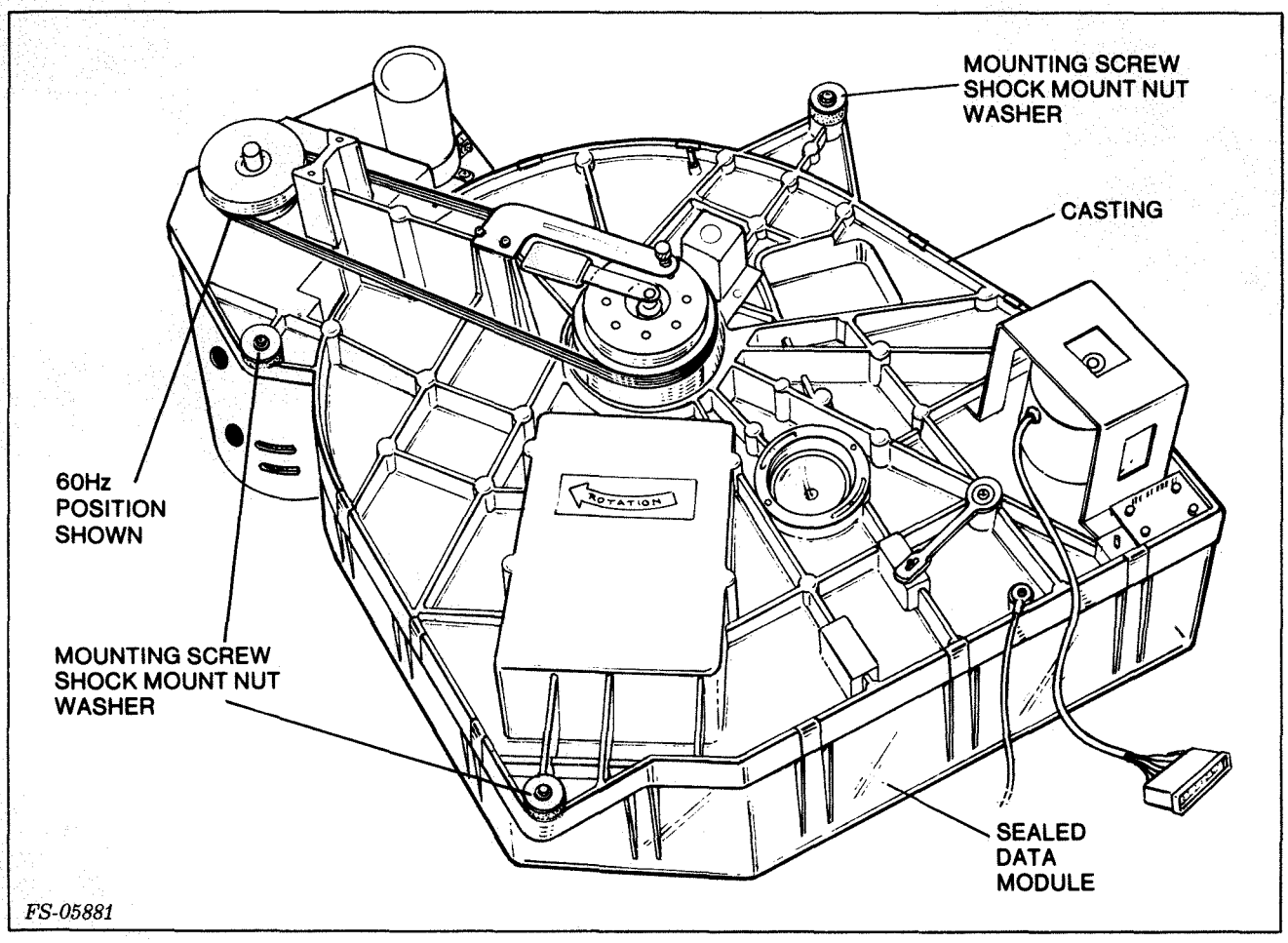


Figure 5-12. Sealed Data Module Mounting Screw Locations

9. Place the new sealed data module in the drive. Replace the three securing shock mount nuts and washers. Connect the ground cable disconnected in step 7.

10. Plug the following three connectors from the sealed data module plugged into the read/write and clock PCB:

    J3 Head Cable
    J4 Sector Transducer No. 1
    Sector Transducer No. 2 (Spare connected to reverse side of J4. Turning J4 180 degrees activates Transducer No 2 and deactivates Transducer No 1).
    J6 Home Transducer

11. Put the blower wheel on the motor shaft. Now place the cover over the blower wheel and secure it with three retaining screws.

12. Reinstall the power switch and RF cover and front dress panel.

13. Replace the top and bottom covers.

5.7 READ/WRITE AND CLOCK PCB REPLACEMENT (005-017591)

1. Power down the drive and remove the front RF cover. See Figure 5-13.

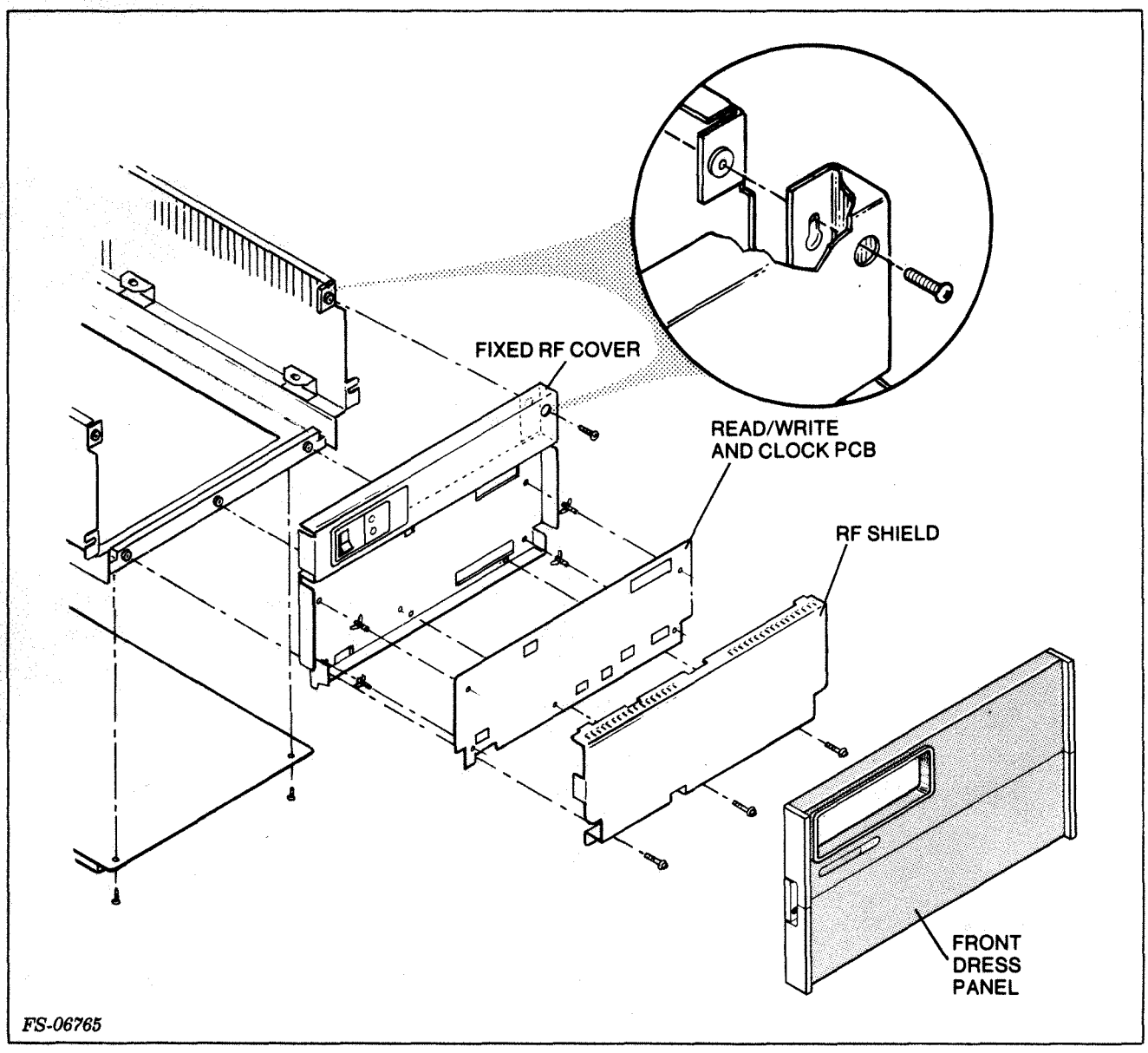


Figure 5-13. Front Covers and Dress Panel

2. Before removing the cable connector that is connected to J4, mark the cable connector as to which of the two sector transducers is in the up position.

3. Remove the PCB from the fixed RF cover by unplugging the seven connectors from the PCB, and unscrew and remove the ground screw at J5.

4. Remove the PCB from its standoffs.

5. Place the PCB on the standoffs. Replace the ground screw.

6. Plug the following seven connectors back into the PCB:

Plug	Description
J1	Drive LED
J2	Logic PCB J1
J4	Sector Transducer No. 1 Sector Transducer No. 2 (Spare)
J5	Ground stud
J6	Home Transducer
J7	Power Supply PCB J9
J8	Power Supply PCB J3

7. Replace the front RF cover.

5.8 SECTOR TRANSDUCER SWITCHING

NOTE

The Sealed Data Module comes with two sector transducers, neither of which are field replaceable. If the sector transducer becomes inoperative, do the following:

1. Power down the drive and remove the front RF cover. See Figure 5-13.

2. Unplug connector J4 from the read/write and clock PCB (see Figure 5-11). Turn connector J4 180 degrees and replug back into connector J4. Rotating the connector 180 degrees activates the spare sector transducer and deactivates the faulty unit.

3. If the backup transducer does not work, the entire Sealed Data Module assembly needs to be replaced. See subsection 5.6, Sealed Data Module Replacement.

4. Replace the drive front RF cover.

5.9 HOME TRANSDUCER REPLACEMENT (005-010652)

1. Power down the drive. Remove the front RF cover top, and bottom covers.

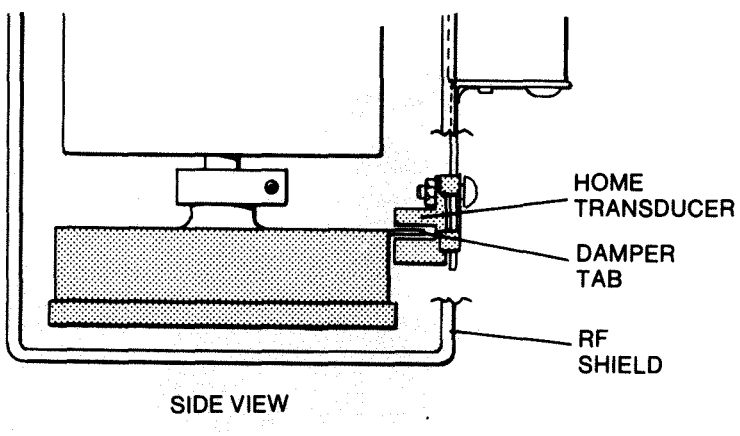
2. Unplug the connector at J6 on the read/write and clock PCB (see Figure 5-11).

3. Unscrew and remove the single screw that holds the home transducer mounting bracket to the casting.

CAUTION

Do not let the transducer touch the damper tab. The home transducer will be damaged if the damper tab touches it.

4. Move the home transducer away from the damper (see Figure 5-14).



FS-05883

Figure 5-14. Home Transducer in Position

5. Unscrew and remove the screw and nut that holds the home transducer to the mounting bracket.

6. Place the new home transducer on the mounting bracket and replace the nut and screw. Do not tighten.

7. Place the home transducer and mounting bracket on the casting, and align the transducer so that the tab is positioned in the middle of the transducer. Do not let the transducer touch the damper tab.

8. Insert the bracket retaining screw and tighten.

9. Plug the connector into J6 on the read/write and clock PCB.

10. Perform the home transducer alignment procedure described in 5.10.

5.10 HOME TRANSDUCER ALIGNMENT

Use the following special tools and parts to align the home transducer.

Description	DGC P/N
2.5 mm Allen bit with 1/4" adapter	128-002634
DTOS tape (800 BPI)	074-060200
(1600 BPI)	074-061200
DTOS diskettes (3)	065-060200 065-060201 065-060202

NOTE

Load the 6225 DIAGNOSTIC for the 6234 from the DTOS tape or diskette. Load the PCDD DIAGNOSTIC for the 6280 from the DTOS tape or diskette. Answer all questions, then type a "CTRL O". When the prompt (!) comes up, type "4R" and follow instructions.

1. Power down the drive. Remove the top, front RF cover, and bottom drive covers (see 5.2 and 5.3).

2. Power up the drive and wait for the READY LED to come on.

3. Unplug the connector at J4 on the power supply PCB (see Figure 5-15).

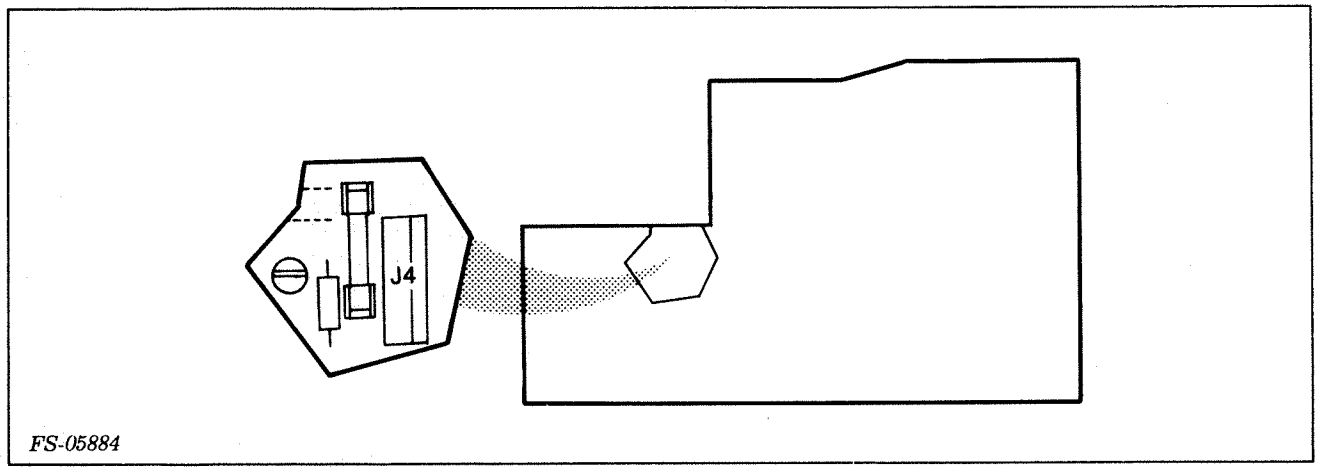


Figure 5-15. Power Supply PCB, Connector J4

4. Place the plastic locking arm onto the locked pin. The plastic locking arm is located under the bottom cover near the front of the drive (see Figure 5-16).

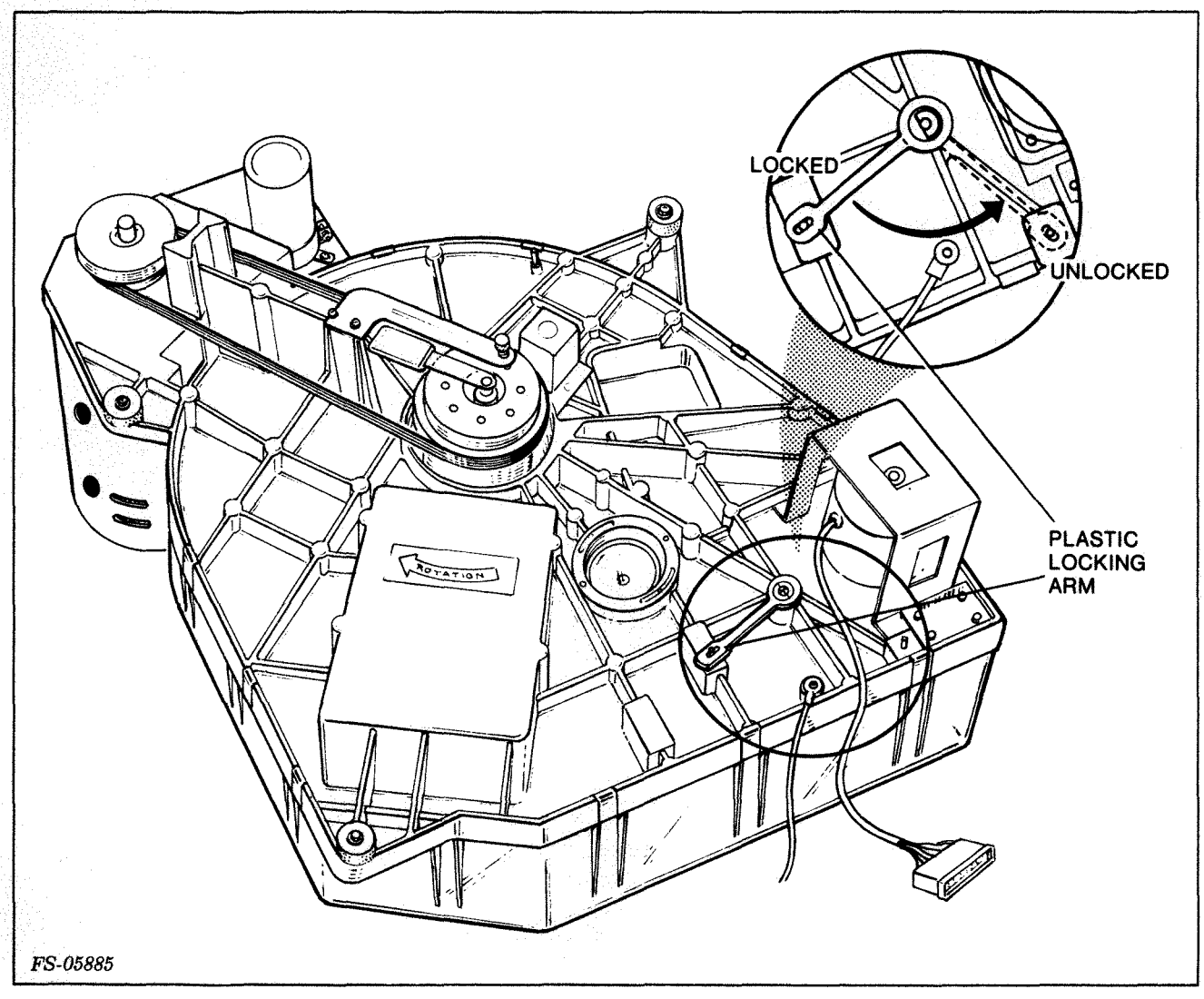


Figure 5-16. Sealed Data Module, Plastic Locking Arm

5. Place the locking arm lever back onto the unlocked pin. Only Stepper phase LED QA will be on (see Figure 5-17).

6. Reconnect the connector at J4 on the power supply PCB.

NOTE

The heads are now positioned over track 192 (300 octal). To verify the alignment only, omit steps 7 and 8 and proceed to step 9.

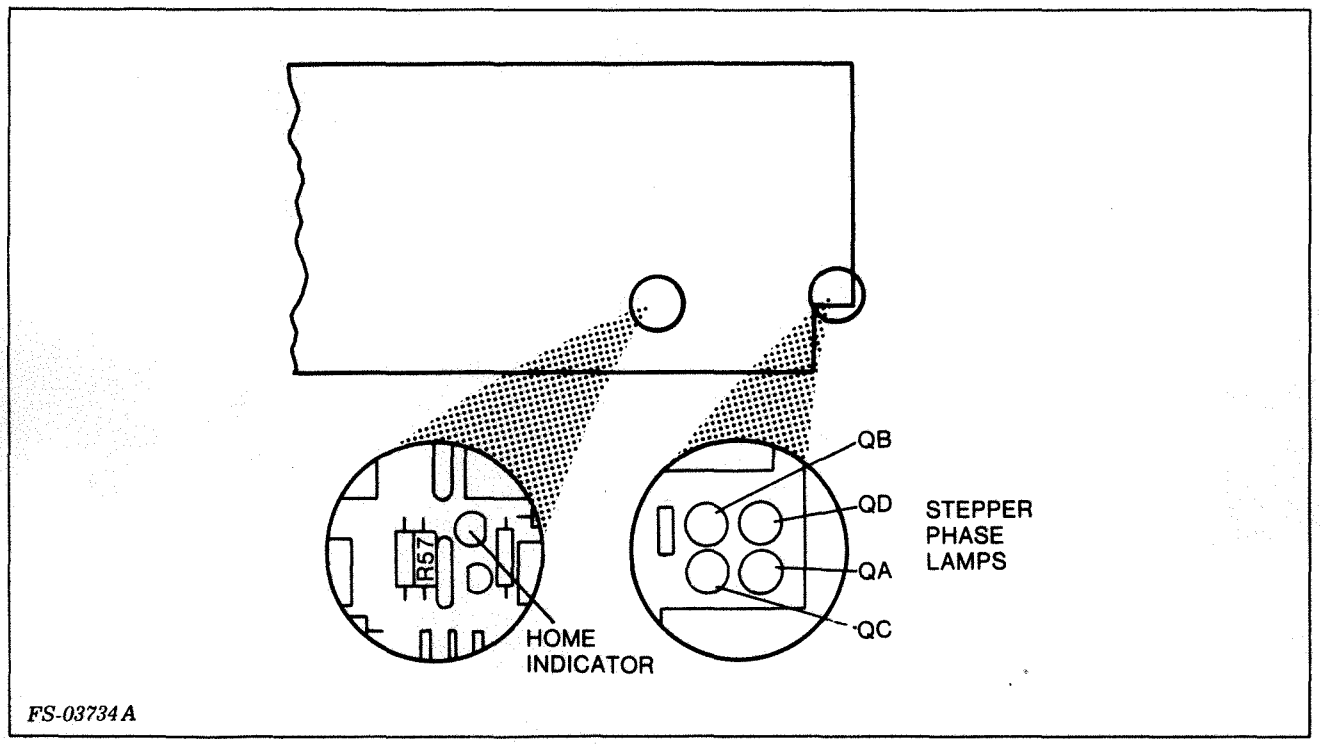


Figure 5-17. Read/Write and Clock PCB Stepper Phase and Home LEDs

7. Hold the damper and loosen the screw in the hub clamp (see Figure 5-18).

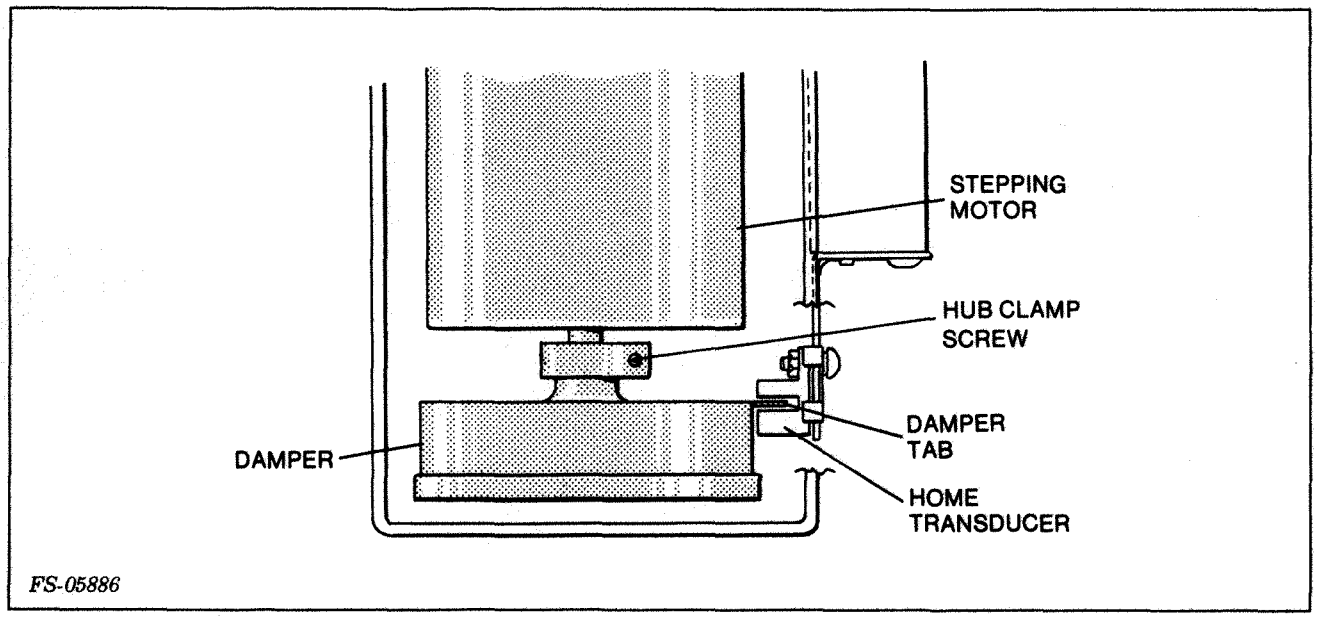


Figure 5-18. Damper (Side View)

CAUTION

The Home Transducer will be damaged if the damper tab touches it.

8. Rotate the damper assembly on the motor shaft until the home indicator LED just makes the transition to just off or just on.

NOTE

Either tab edge will cause this condition. The one used for alignment is the tab edge that first interrupts the home transducer when the damper is rotated clockwise (as viewed from the bottom of the drive). The tab must also be vertically centered in the home transducer. The damper should be pushed all the way onto the shaft. If the tab is not centered, adjust the home transducer. When the damper is just at the transition point, torque the damper hub clamp screw to 13 inch-pounds.

9. Verify that the heads are positioned over track 191 (277 octal). The home indicator LED is off. If not, type (R) to repeat the procedure from step 7.

NOTE

The heads are now positioned over track 192 (300 octal).

10. Power off the drive. The arm should move inward to the head landing zone track 207 (317 octal).

11. Replace the top, front RF cover and bottom covers (see 5.2, 5.5 and 5.3).

12. Power up the drive.

NOTE

The transducer alignment is complete. Restart the diagnostic at SA 500 as a final alignment check. Repeat this procedure if head alignment errors still exist.

If this procedure was correctly performed, the head positioning should be exactly correct. Reformatting should not be necessary unless the drive was previously formatted incorrectly with a hardware fault or a gross misalignment of the home transducer.

5.11 AC POWER DISTRIBUTION PCB REPLACEMENT (005-010641)

1. Power down the drive and unplug the ac line cord.

2. Loosen the four screws that hold the back cover to the drive. Slide the cover up and hook it to the rear of the drive.

3. Unplug the four connectors at J1, J3, J4, and J5. Disconnect the two wires at J7 and J8 (see Figure 5-8).

4. Remove the two relays from the board (see Figure 5-8) and unscrew the six screws that hold the board to the back cover.

5. Unplug the jumper at J2 and plug it into the new PCB.

6. Secure the new PCB to the cover with the six retaining screws. Plug in the four connectors and reconnect the two wires to J7 and J8. Reference the following:

Connector	Description
J1	Transformer
J2	ID Jumper Plug
J3	Spindle Motor
J4	Power Supply PCB J2
J5	Power Switch
J7	Filter
J8	Fuse

7. Plug the two relays into the new PCB.

8. Unhook the cover from the back of the drive and place it in the operating position. Tighten the four retaining screws.

9. Plug in the line cord, power up the drive and verify the voltages on the power supply PCB.

5.12 POWER SUPPLY PRINTED CIRCUIT BOARD (PCB) REPLACEMENT (005-017474)

1. Power down the drive and unplug the line cord. Remove the top cover of the drive (see 5.2).

2. Unplug all connectors from the top of the power supply PCB (see Figures 5-19 and 5-20).

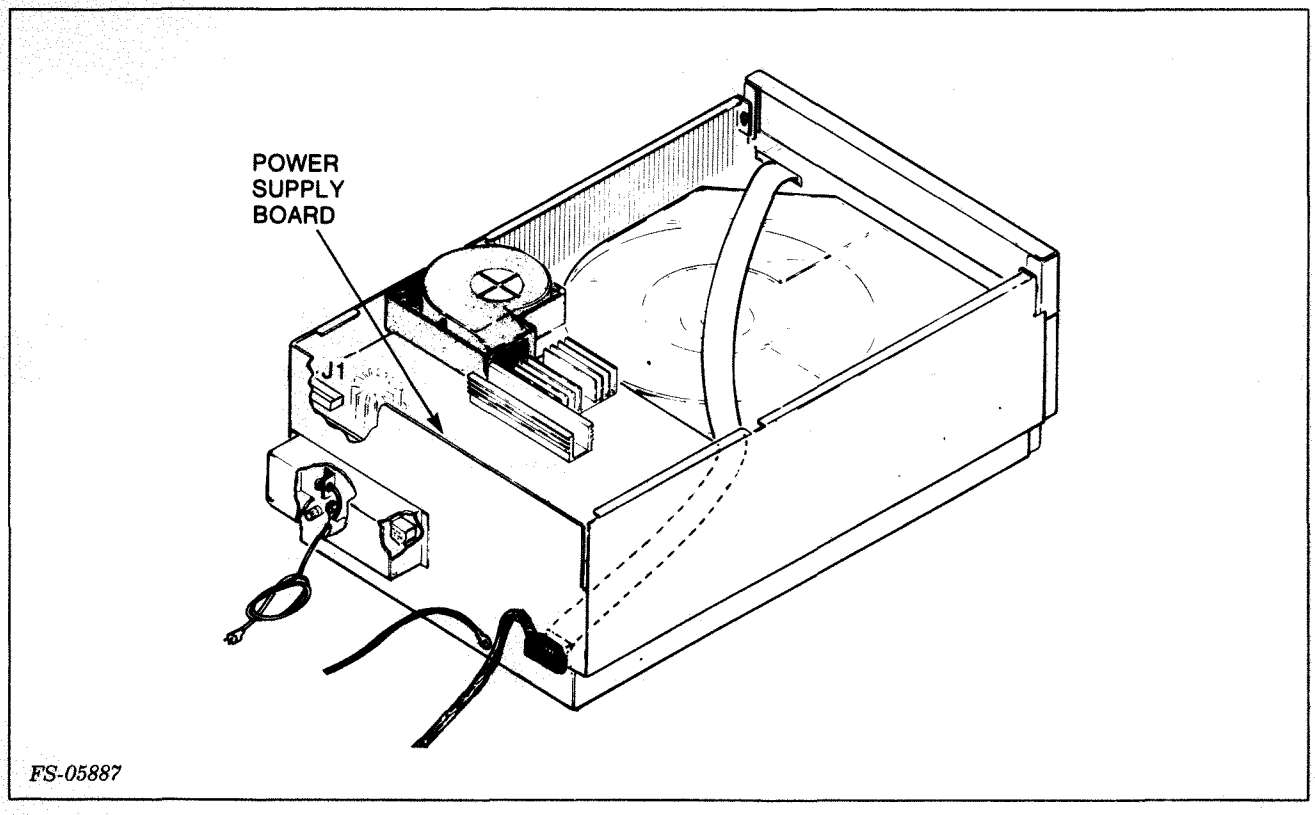


Figure 5-19. Power Supply PCB Location

3. Unscrew and remove the eight screws that hold the PCB to the drive.

NOTE

Do not lose the insulating washers.

4. Loosen the four screws that hold the back cover on the drive. Slide the cover up and hook it to the rear of the drive.

5. Unplug the three connectors and two ground straps (see Figure 5-19) from the bottom of the power supply PCB. Remove the PCB from the drive.

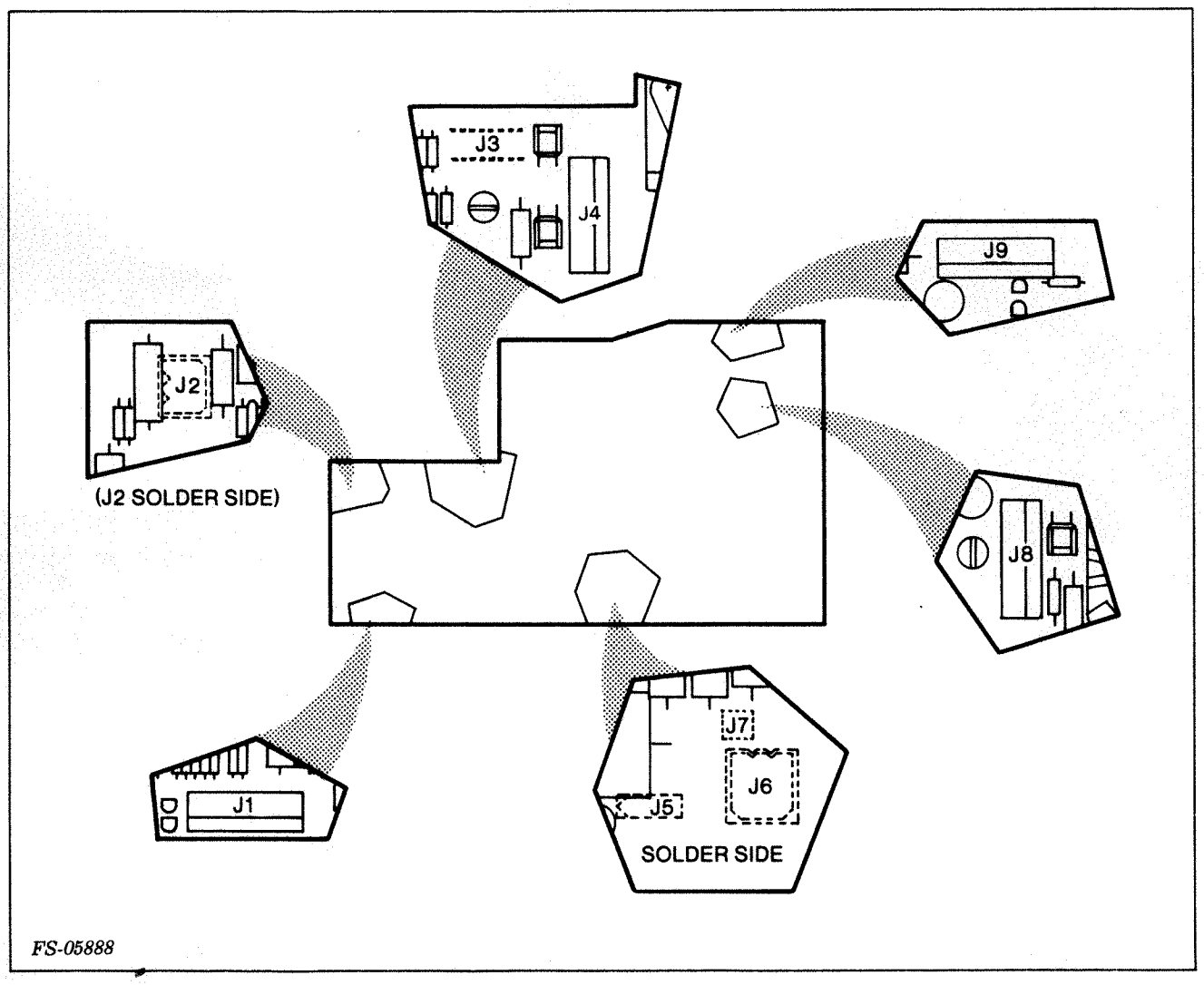


Figure 5-20. Power Supply PCB, Connector Locations

6. Place the new power supply PCB in the drive. Plug the three connectors and the two ground straps into the bottom of the board:

Connector	Description
J2	AC Power PCB J4
J5	Transformer
J6	Transformer
J7	Ground Strap

7. Insert the eight retaining screws and tighten.

8. Plug the remaining connectors into the top of the power supply PCB and plug in the line cord.

Connector	Description
J1	not used
J3	Read/Write and Clock PCB J8
J4	Stepping Motor J1
J9	Read/Write and Clock PCB J7

9. Power up the drive. The power supply PCB has five LEDs. When the power switch is turned on, all five LEDs should light (see Figure 5-21). If any of them do not, go to the power supply check flowchart (Figure 4-9) before continuing.

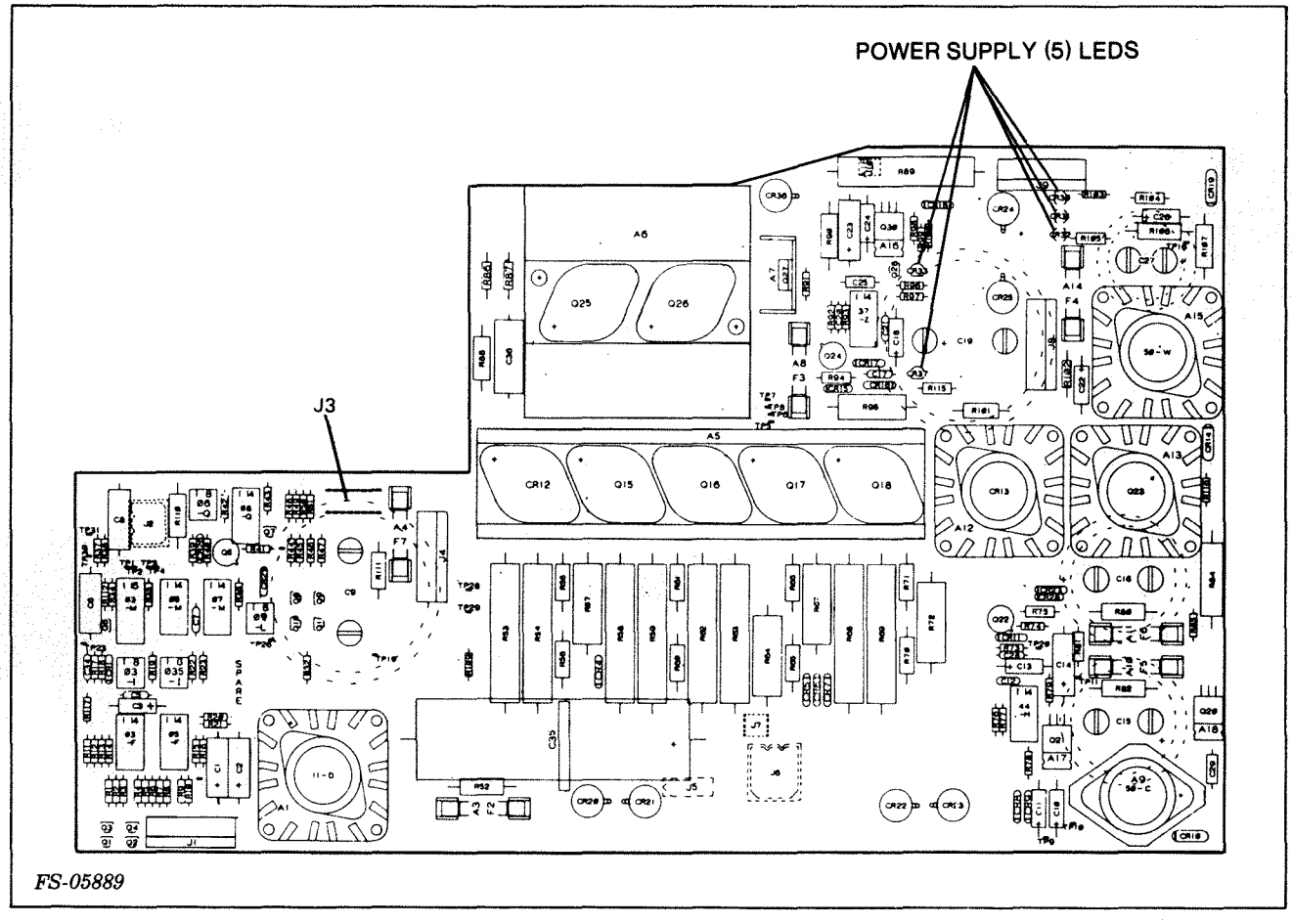


Figure 5-21. Power Supply LEDs

10. Replace the top and back covers (see 5.2 and 5.3).

11. Reformat the Data Module to insure compatibility between format and head locations.

5.13 POWER SWITCH REPLACEMENT (110-000359)

1. Power down the drive and unplug the line cord. Remove the top cover of the drive (see 5.2).

2. Locate the front panel power switch.

3. Pull one spade lug wire from the back of the switch and seat it on the back of the new switch. Repeat this process until all wires have been replaced (see Figure 5-22).

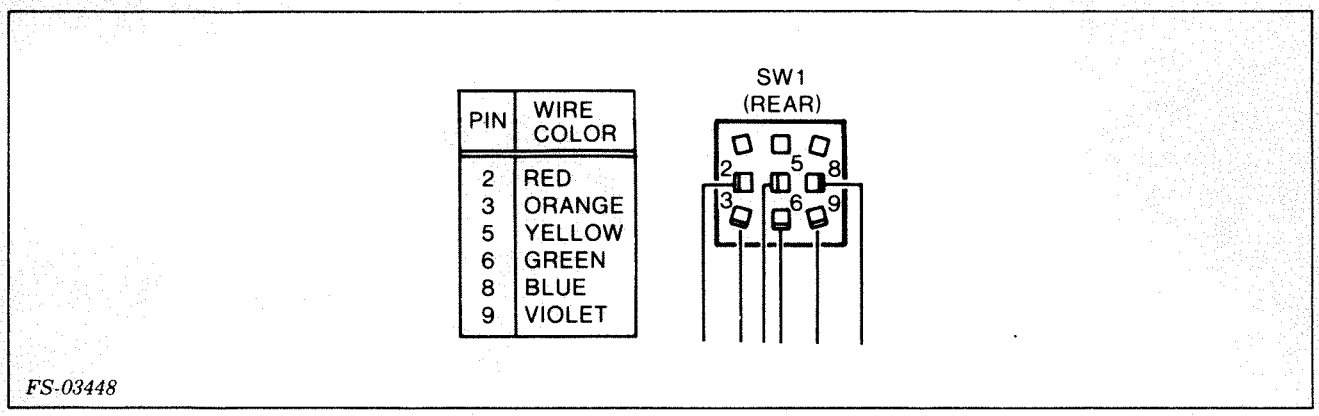


Figure 5-22. Power Switch Wire Connections

4. Remove the two switch mounting screws retaining the switch being replaced.

5. Seat the new switch and fasten into place with the screws removed in step 4.

6. Replace the top cover (see 5.2) and plug in the line cord.

5.14 SPINDLE MOTOR STARTER CAPACITOR REPLACEMENT (Capacitor (103-000387))

1. Power down the drive and unplug the line cord. Remove the bottom cover of the drive (see 5.3).

2. Locate the starter motor capacitor (see Figure 5-23).

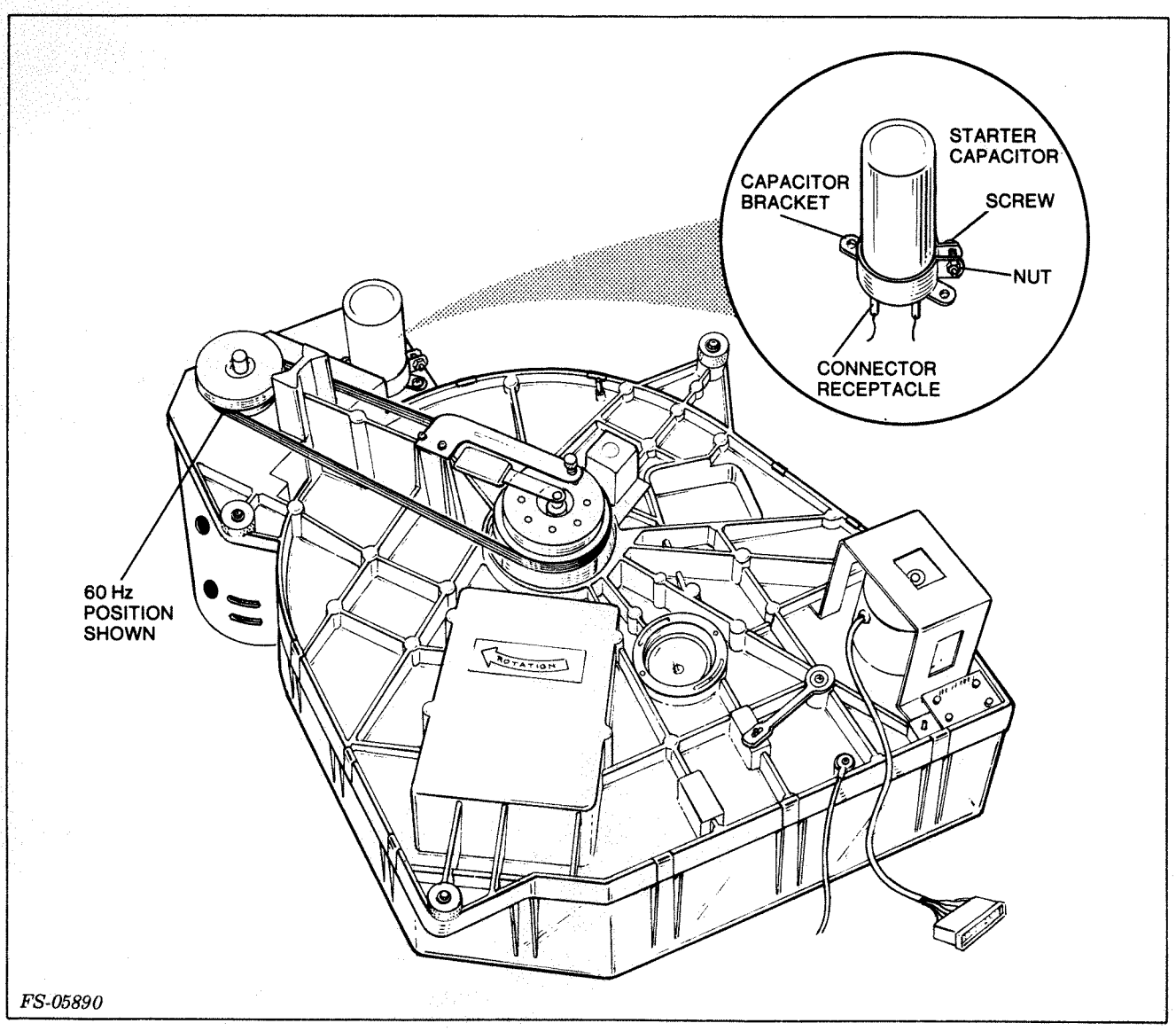


Figure 5-23. Spindle Motor Starter Capacitor Replacement

3. Loosen the capacitor bracket retaining screw.

4. Pull the capacitor straight down and change the wires over to the replacement capacitor.

5. Position the capacitor back into the retaining bracket.

6. Tighten the capacitor bracket retaining screw.

5.15 TRANSFORMER T1 REPLACEMENT (005-009930)

1. Power down the drive and unplug the line cord. Remove the top cover of the drive (see 5.2).

2. Remove the power supply PCB (see 5.12).

3. Remove the power supply support bracket located below the power supply PCB. The bracket is held in place by four M3 X 8 hex head screws.

4. Locate transformer T1 (see Figure 5-24). It is located directly below the support bracket.

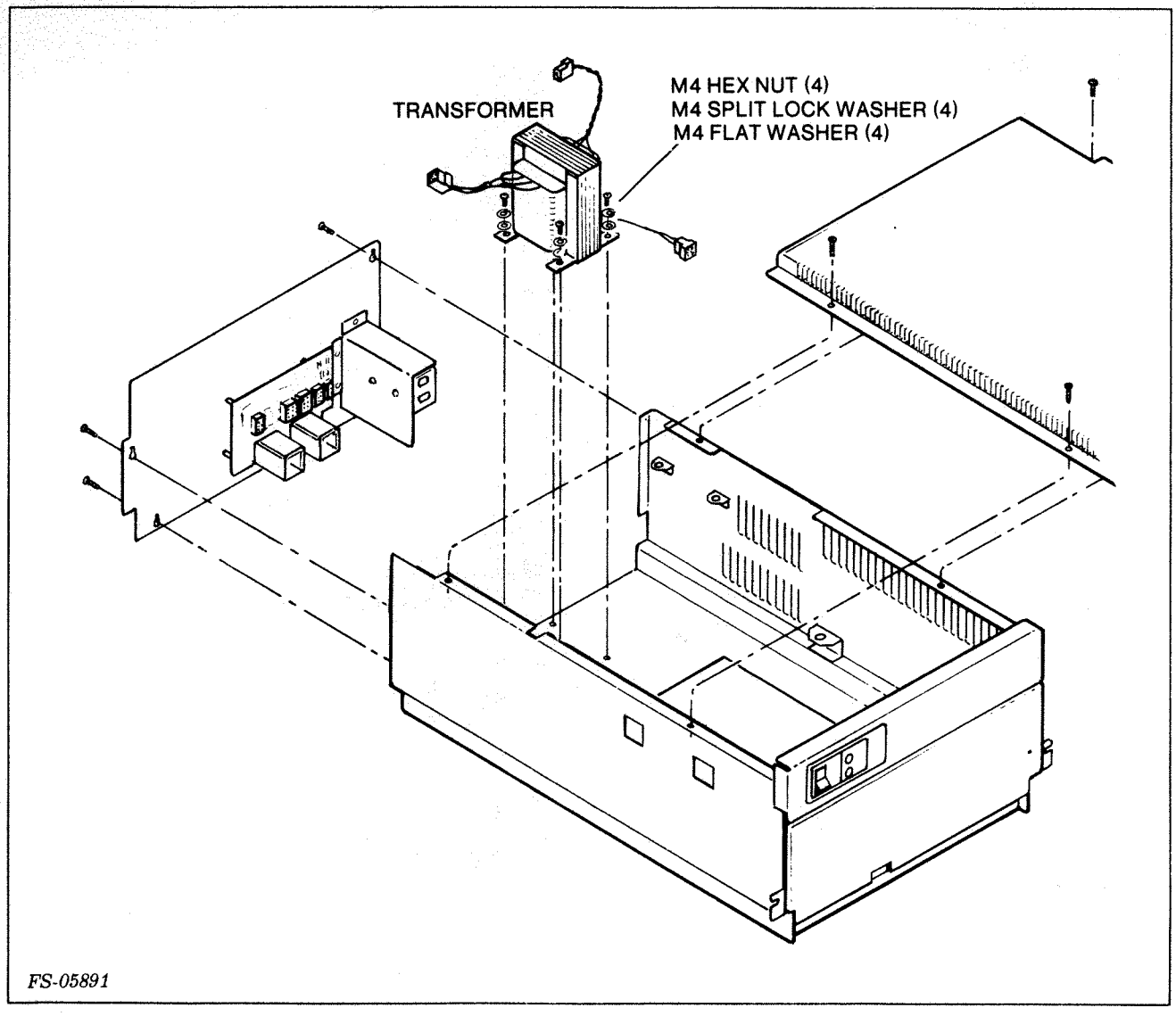


Figure 5-24. Transformer Removal

5. Disconnect cable connector P1/J1 from the ac power distribution PCB.

6. Remove the transformer retaining nuts and associated washers.

7. Seat the new transformer on the four studs in the same position as the transformer just removed.

8. Reconnect cable P1/J1 to the ac power distribution PCB.

9. Replace the power supply support bracket removed in step 3.

10. Replace the power supply PCB (see 5.12).

11. Replace the top cover (see 5.2).

12. Reconnect the ac line cord and power up the drive.

SECTION 6

INSTALLATION/REMOVAL

This section describes installation and removal procedures for Model 6234/6280 Disk subsystems. Service personnel should be familiar with the complete installation procedure and requirements before installing the disk subsystem to a CPU system.

6.1 SITE PREPARATION

Table 6-1 provides the site preparation requirements. Figure 6-1 shows the equipment service clearance requirements.

Table 6-1. Model 6234/6280 Site Preparation Requirements (page 1 of 2)

Equipment Physical Specifications:

DIMENSIONS:	WIDTH	DEPTH	HEIGHT
Centimeters	48.3	75.9	26.7
Inches	19.0	29.8	10.5

WEIGHT: FULLY LOADED

Kilograms	37.3
Pounds	82.0

HEAT OUTPUT (MAX)

Volt	Hz	Watts	BTU/hr
100	50/60	125	427
120	60	125	427
220	50	125	427
240	50	125	427

OPERATING ENVIRONMENT

	Room	Cabinet
Temperature (Max)	+38 degC +100 degF	+43 degC +109 degF
Relative Humidity (Max)	80% (noncondensing)	

Table 6-1. Model 6234/6280 Site Preparation Requirements (page 2 of 2)

Altitude Operating	-304 to 3,048 m (-1,000 to 10,000 ft)
Nonoperating	-304 to 18,000 m (-1,000 to 59,055 ft)

U.S.A. POWER REQUIREMENTS

Voltage	120 +10/-15%
Frequency (Hz)	60 +/- 1%
Amps per Phase (Max)	1.8
Phase	1
Startup Surge	8.5 A for 10 sec

OTHER POWER REQUIREMENTS

Voltage	100 +/-10%	220 +10/-15%	240 +10/-15%
Frequency (Hz)	50 or 60 +/-1	50 +/-1	50 +/-1
Amps per Phase (Max)	2.2	1.0	0.9
Phase	1	1	1
Startup Surge for 10 sec	10.0	4.7	4.3

CAUTION

To prevent equipment damage, do not allow the customer to connect any equipment until the line voltage is within specifications.

CABLES

Primary Power		Length	Connector
U.S.A.	60 Hz	1.8 m (6 ft)	515-P
Other	50/60 Hz	to be provided by installing engineer	

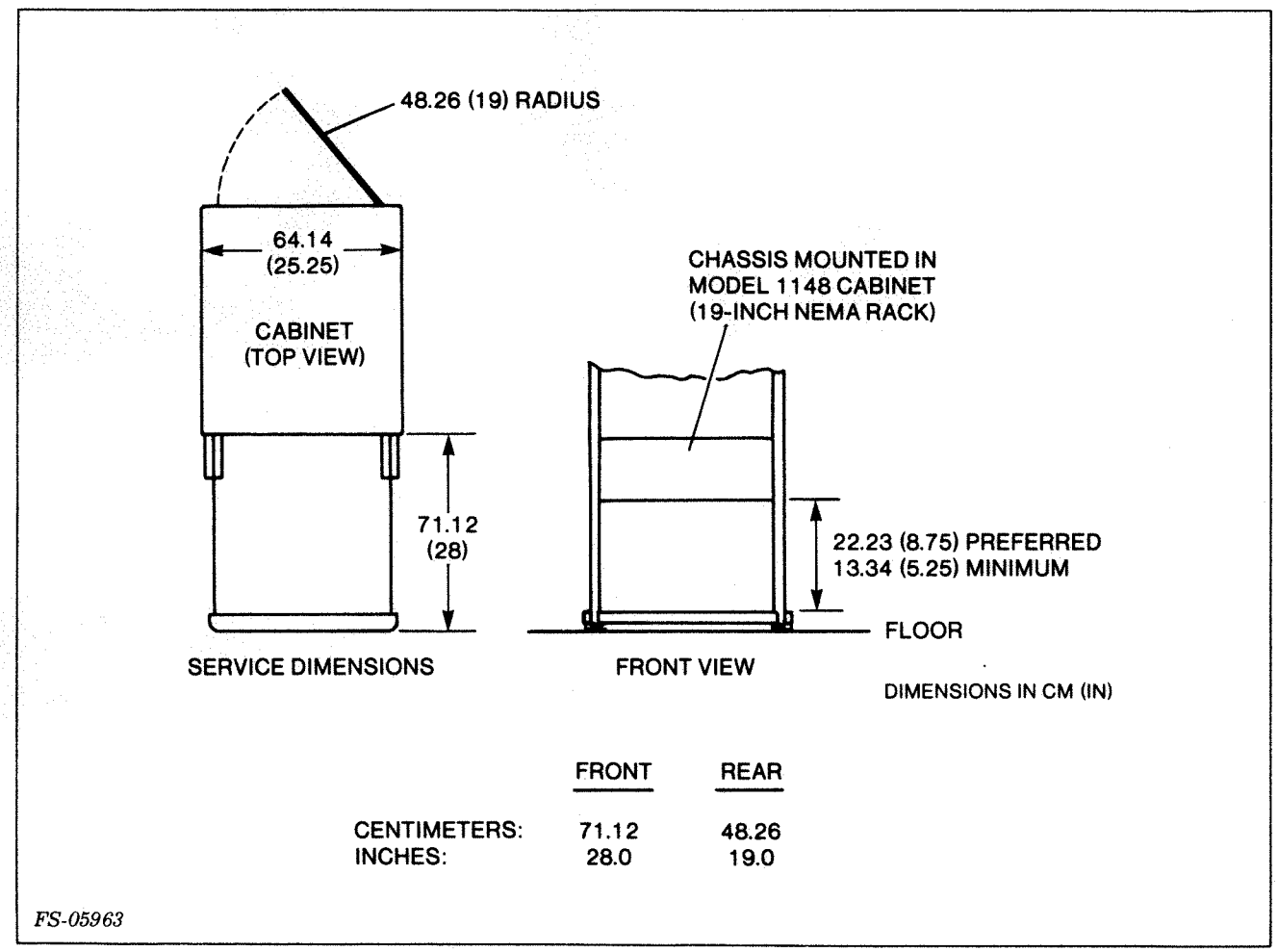


Figure 6-1. Service Clearance

6.2 TOOLS/EQUIPMENT/MATERIALS REQUIRED

A standard tool kit is required to install Model 6234/6280.

6.3 UNPACKING, CHECKLIST AND INSPECTION

NOTE

It is the customer's responsibility to negotiate with the carrier for any visible damage to the exterior of the shipping carton while in the possession of the carrier.

Unpack the disk subsystem as shown in Figure 6-2 and follow the checklist in Figure 6-3. Check the packing list against the equipment list to verify that all the equipment was delivered. Check the subsystem identification label to ensure a voltage/frequency match to the installation location. List on the packing slip missing equipment. One or more of the part numbers shown in Figure 6-3 should be in the shipment.

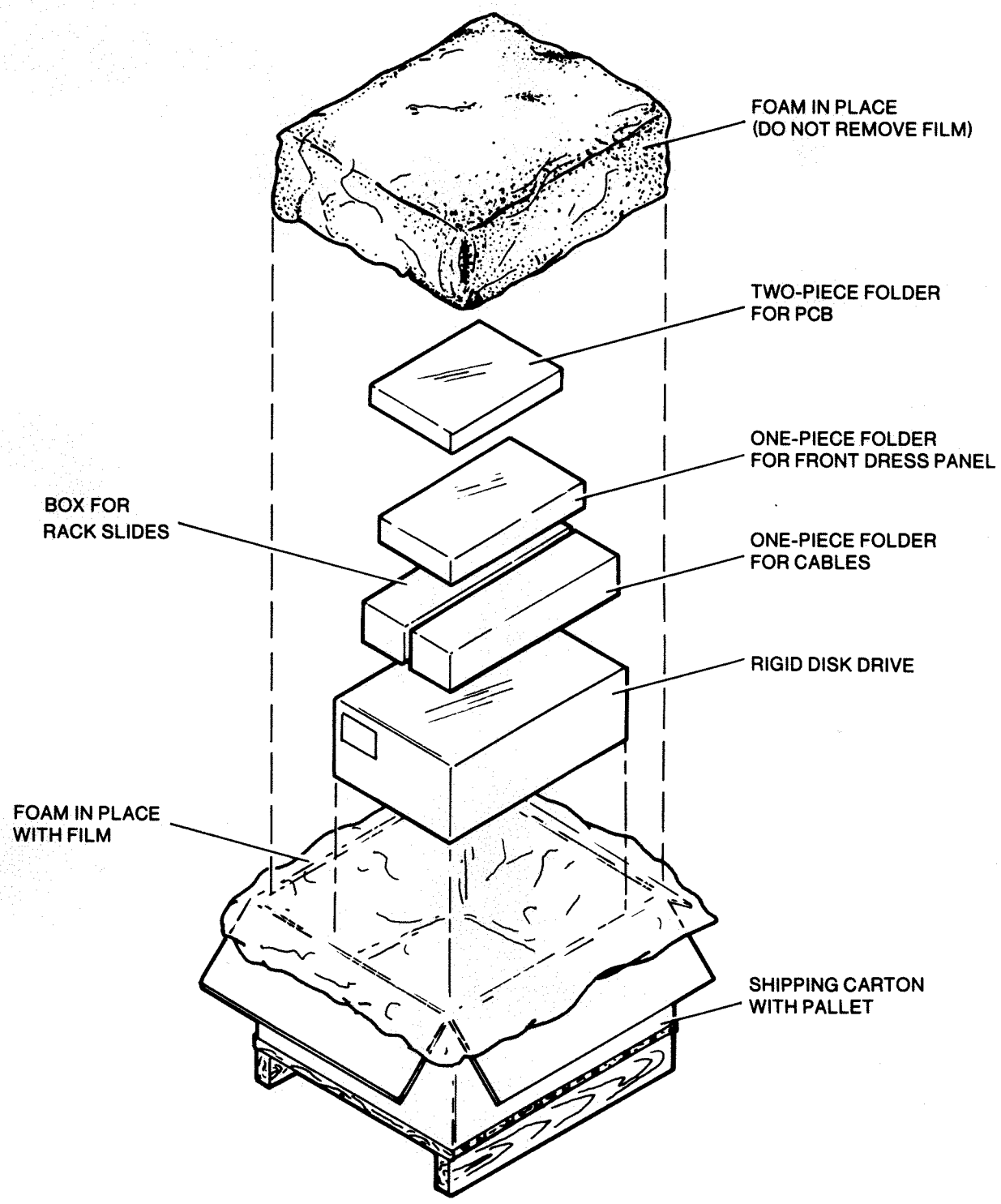


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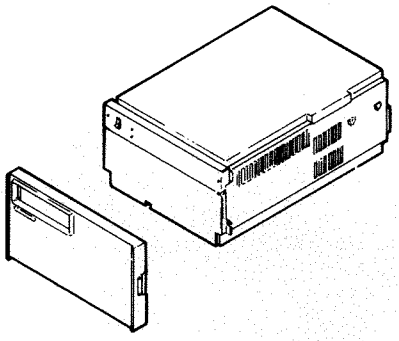
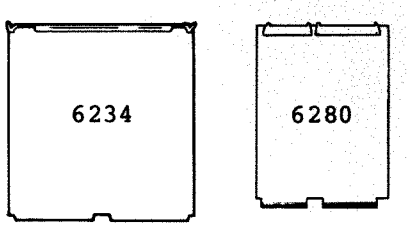
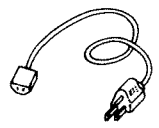
Figure 6-2. Disk Subsystem Packaging

MAJOR COMPONENT		PART NO.	ILLUSTRATION
RIGID DISK DRIVE			
V/Hz	Model		
100/50	6234-1/6280-1	005-017580	
120/60	6234/6280	005-017581	
220/50	6234-2/6280-2	005-017582	
240/50	6234-4/6280-4	005-017583	
Front Dress Panel			
Blue		005-014213	
Paji Brown		005-019576	
Controller PCB			
6234		005-015551	
6280		005-019424	
External I/O Cable *			
6234 (nonhardened)		005-017587	
6234/6280 (hardened)		005-018480	
6280 (nonhardened)		005-019669	
BMC Terminator (6280)		005-013419	
BMC Cable (6280)			
BMC to disk controller		005-020210	
Disk controller to bulkhead		005-019434	
Ground Braid		005-009536	
Power ID Plug			
100 V		005-012592	
120 V		005-012593	
220 V		005-012594	
240 V		005-012595	
AC Power Cable			
100/120 V		005-009935	
220/240		005-010642	
Mounting Hardware Kit		005-019126	

* When used with a 6096-CV (one 1.2 MB diskette subsystem nonhardened) or 6096-DV (two 1.2 MB diskette subsystem non-compliant) omit 005-017587 external I/O cable (nonhardened CPUs only). 005-017383 Y cable is supplied with diskette subsystems.

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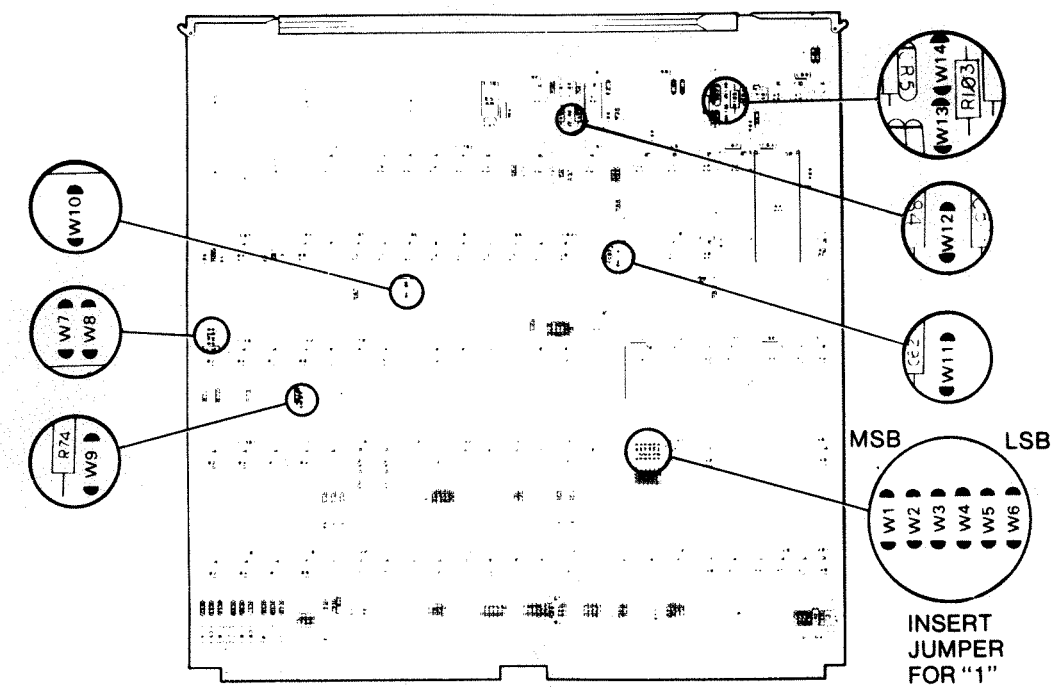
Figure 6-3. Shipment Verification

6.4 JUMPERING

Controller PCB tailoring information is shown in Figures 6-4 and 6-5. The controller PCB for the disk subsystem is located within the host CPU.



JUMPER NOTES:

1. JUMPERS W1 AND W6 ARE DEVICE CODE SELECTION JUMPERS.
2. JUMPERS W8, W11 AND W12 ARE IN.
3. JUMPERS W7 AND W10 ARE OUT.
4. W14 IS IN FOR ALL CPU'S EXCEPT MV/4000, 6000, 8000,10000.
5. W13 IS IN FOR MV/4000, 6000, 8000, 10000.
6. IF ONE DISKETTE AND ONE HARD DISK ARE ATTACHED, W9 IS IN.

CONTROLLER DEVICE CODE SELECT		
JUMPER NUMBER	DEVICE CODE 33	DEVICE CODE 73
1	OUT	IN
2	IN	IN
3	IN	IN
4	OUT	OUT
5	IN	IN
6	IN	IN

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Figure 6-4. Controller PCB Jumpering for Model 6234

Ref DGC Dwg No 003-001911 Rev 02

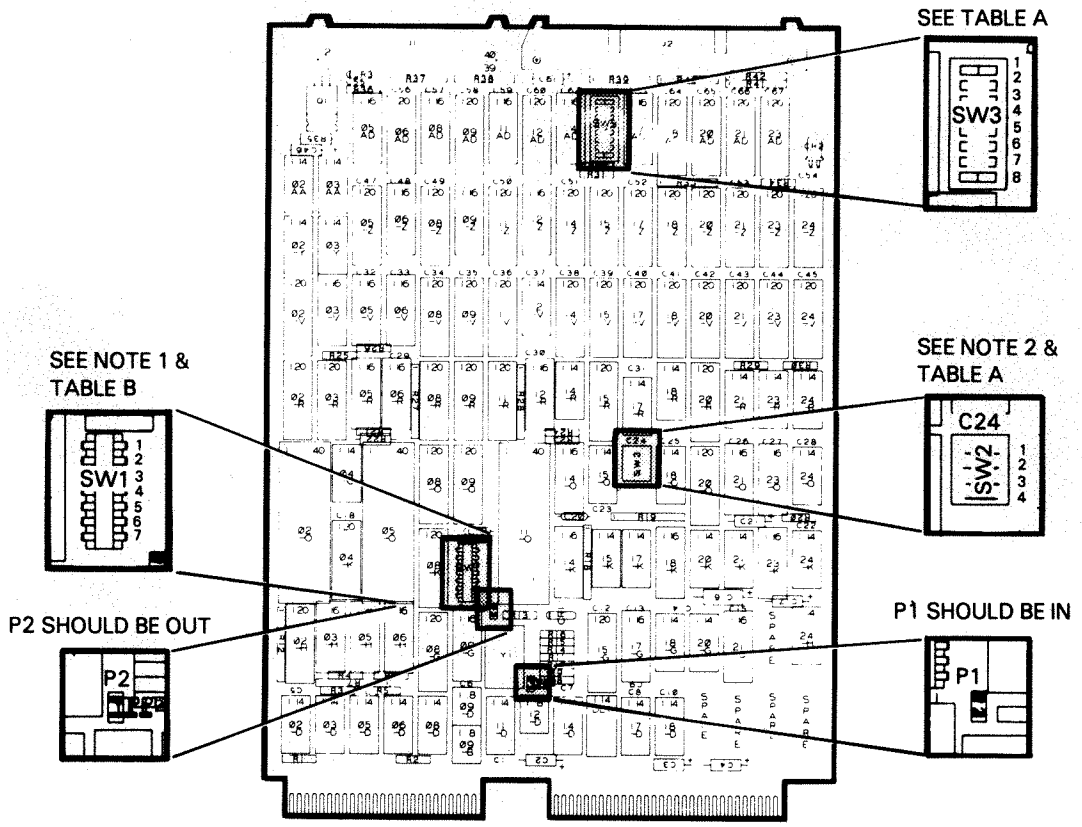


TABLE A

PRIORITY SELECT	S2			S3
	SW4	SW3	SW2	
HSCR7	ON	ON	ON	SW8
HSCR6	ON	ON	---	SW7
HSCR5	ON	---	ON	SW6
HSCR4	ON	---	---	SW5
HSCR3	---	ON	ON	SW4
HSCR2	---	ON	---	SW3
HSCR1	---	---	ON	SW2
HSCR0	---	---	---	SW1

NOTE:
TO SELECT BMC PRIORITY LEVEL 0-7, SET SWITCHES 2-4 OF S2 AS SHOWN AND TURN ON ONE SWITCH IN S3 AS INDICATED.

TABLE B

S1	DEVICE CODE (OCTAL)	
	25	65
SW1	OFF	ON
SW2	ON	ON
SW3	OFF	OFF
SW4	ON	ON
SW5	OFF	OFF
SW6	ON	ON

SWITCH NOTES:
1. SW1 TO SW6 OF S1 ARE DEVICE CODE SELECTION SWITCHES CORRESPONDING TO DS0 TO DS5 RESPECTIVELY, SWITCH ON FOR A-1, SW7 NOT USED.
2. SW1 OF S2 SHOULD BE ON.

FS-06754

Figure 6-5. Controller PCB Jumpering for Model 6280

6.5 INSTALLATION PROCEDURE FOR MODEL 6234/6280

Installation of the 6234/6280 disk subsystem consists of mounting the subsystem in a suitable cabinet (19-inch NEMA rack) having the necessary power and interface connection. The disk subsystem is designed to fit into a standard Data General peripheral cabinet. Install the subsystem according to the following procedure.

NOTE

Observe the hardware mounting torque requirements as shown in Figure 6-6.

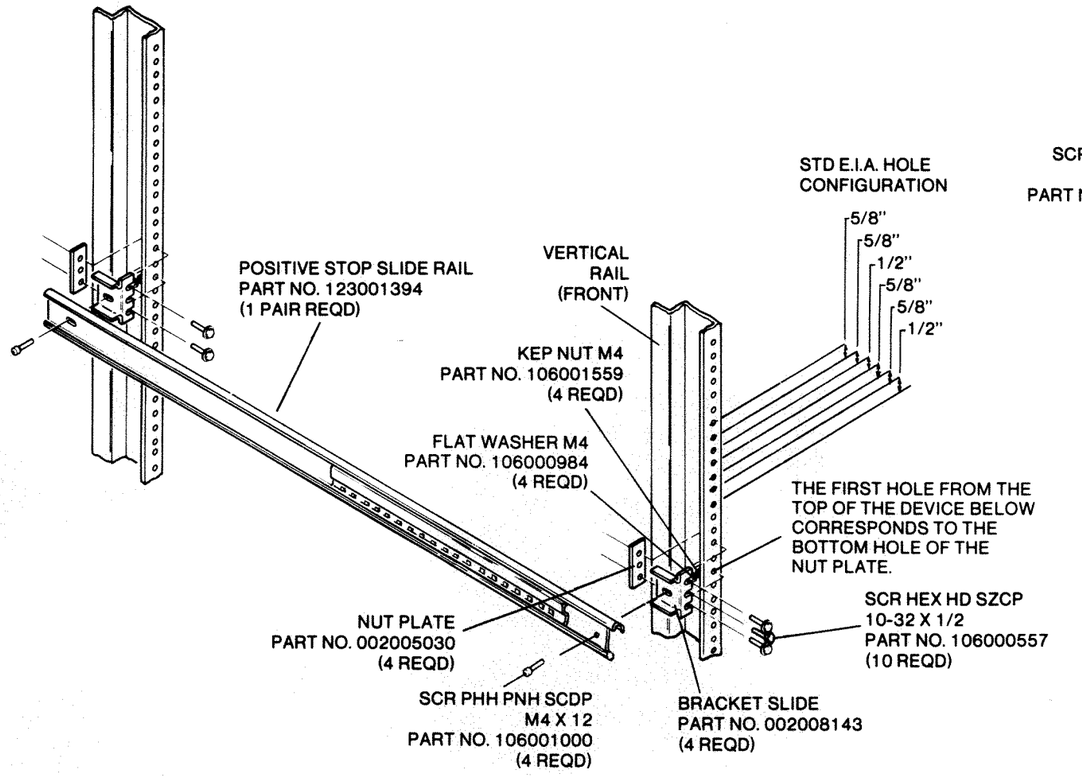
All mounting hardware is contained in the kit (DG 005-009934) and shipped with the drive.

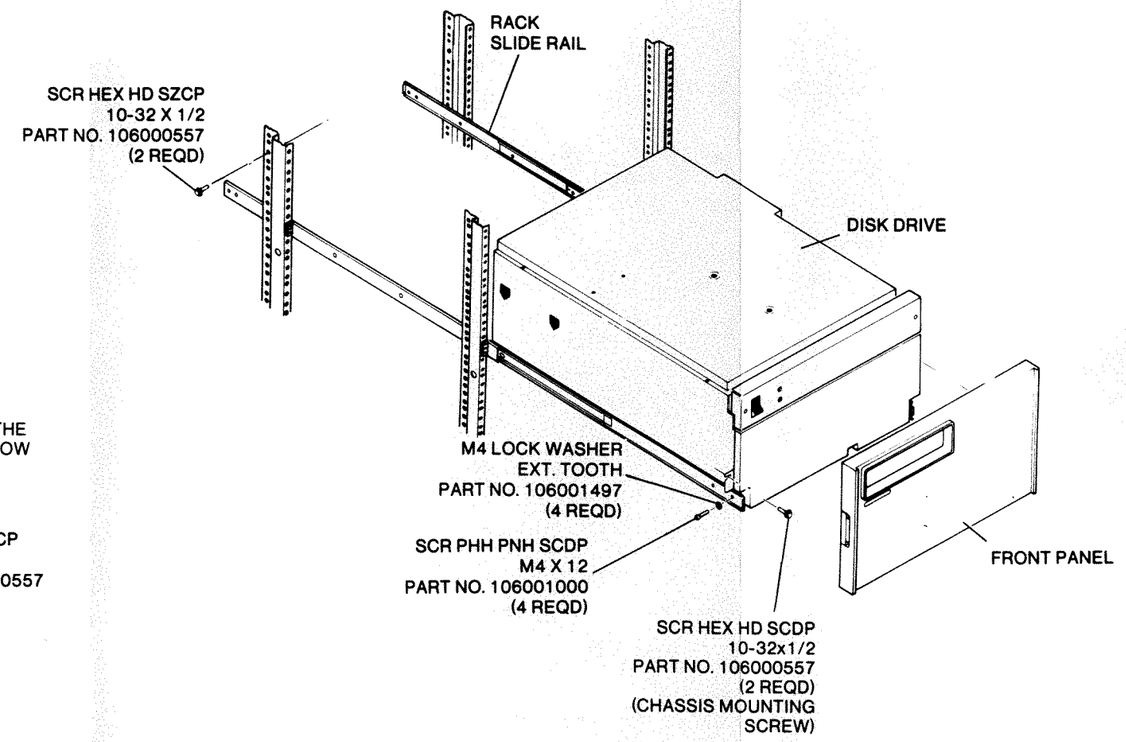
1. Mount the chassis slides, one on each side of the disk drive, as shown in Figure 6-6.
2. Remove the bottom cover (see 5.3)
3. Release and unlock the sealed data module shipping restraints as shown in Figure 6-7 and the shipping restraints shown in Figure 6-8 for the subsystem.
4. Replace the bottom cover removed in step 2.
5. Power down any equipment operating in the cabinet.
6. Power down the host CPU.
7. Mount the cable support arm (two) as shown in Figure 6-6.
8. Determine the height that the drive is to be mounted at (see Figure 6-1 for service clearance) and mount the two rack slide rails as shown in Figure 6-6. Chassis slides must be mounted a minimum of 45.72 cm (18 in) off the floor for bottom service clearance.
9. Position and secure the left and right guide pins as shown in Figure 6-6.

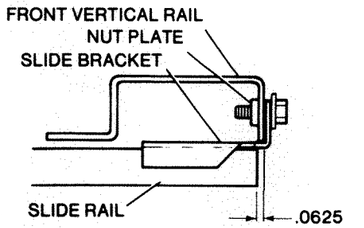
CAUTION

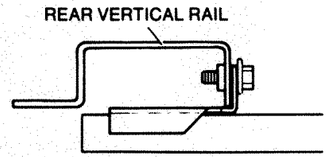
The disk subsystem weighs 37.3 kilograms (82 pounds). Two service people are required when lifting the disk subsystem.

10. Lift the disk subsystem and set it into the slide assembly. Push the drive back as far as it will go.
11. Insert and secure the two chassis mounting screws.
12. Install the front dress panel.









SLIDE BRACKET IN FRONT OF RAIL

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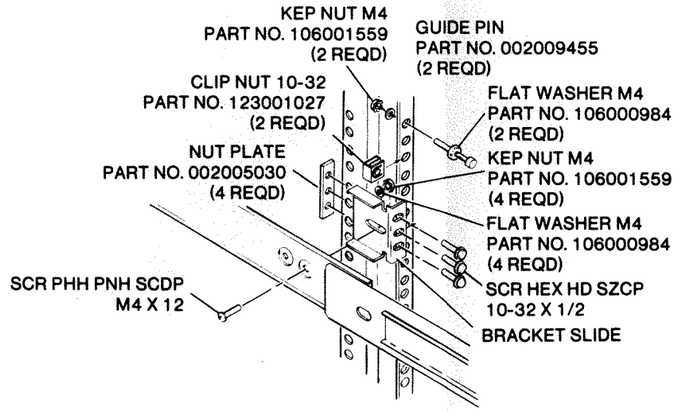


TORQUE REQUIREMENTS		
SCREW NO	IN/LB	N/M
M4	13.27-15.04	1.5-1.70
8-32	14.5-15.5	1.63-1.75
10-32	33-35	3.7-3.95

Figure 6-6. Disk Subsystem, Hardware Mounting Kit Installation

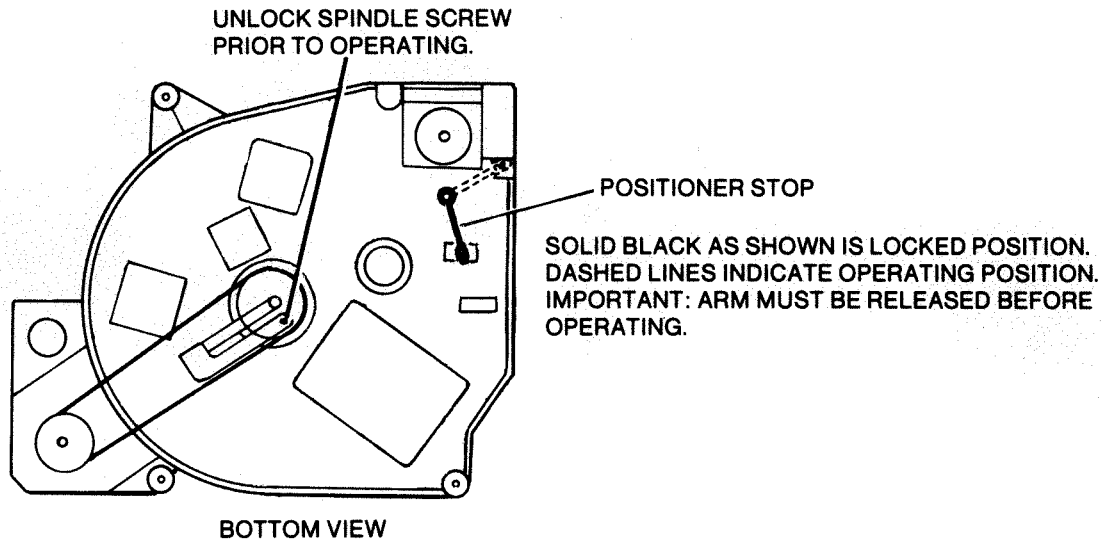


Figure 6-7. Sealed Data Module Shipping Restraint

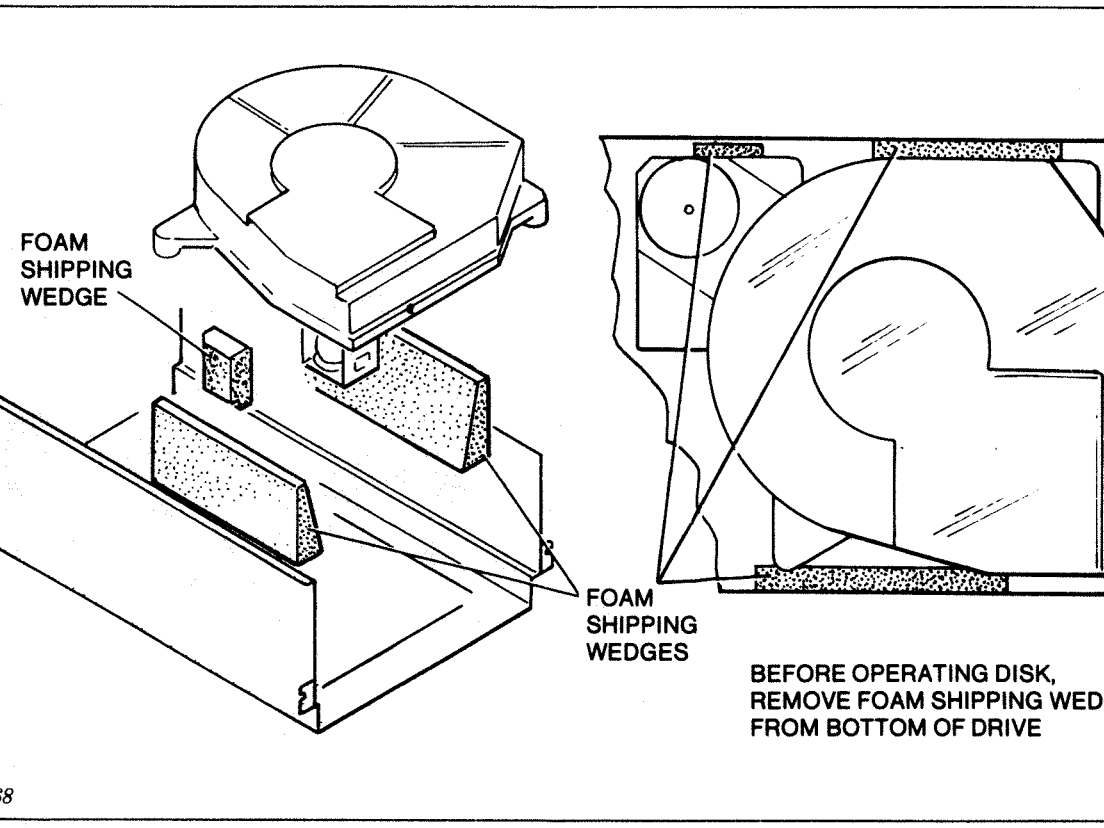


Figure 6-8. Disk Subsystem Shipping Restraints

6.6 POWER/INTERFACE CONNECTION

Connect the subsystem as follows:

1. Power down the host CPU.
2. Check the controller PCB for correct jumpering. See Figures 6-4 or 6-5.
3. Select the correct slot in the host CPU and install the controller PCB (reference the appropriate host CPU maintenance documentation).
4. Install the signal cables as shown in Figure 6-9 for a Model 6234 or Figures 6-10 and 6-13 for a Model 6280.

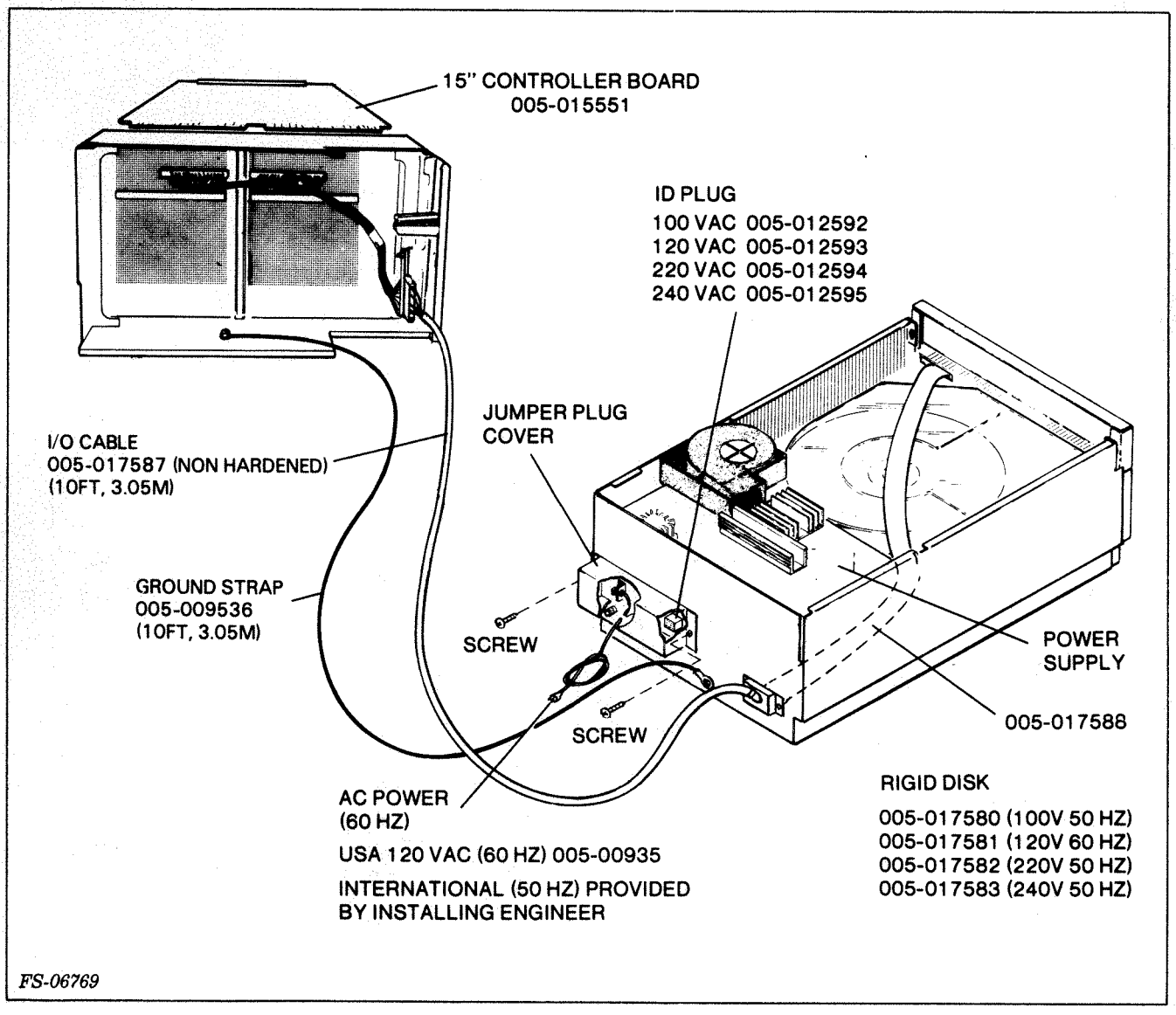


Figure 6-9. 6234 Signal/Power Cable Installation

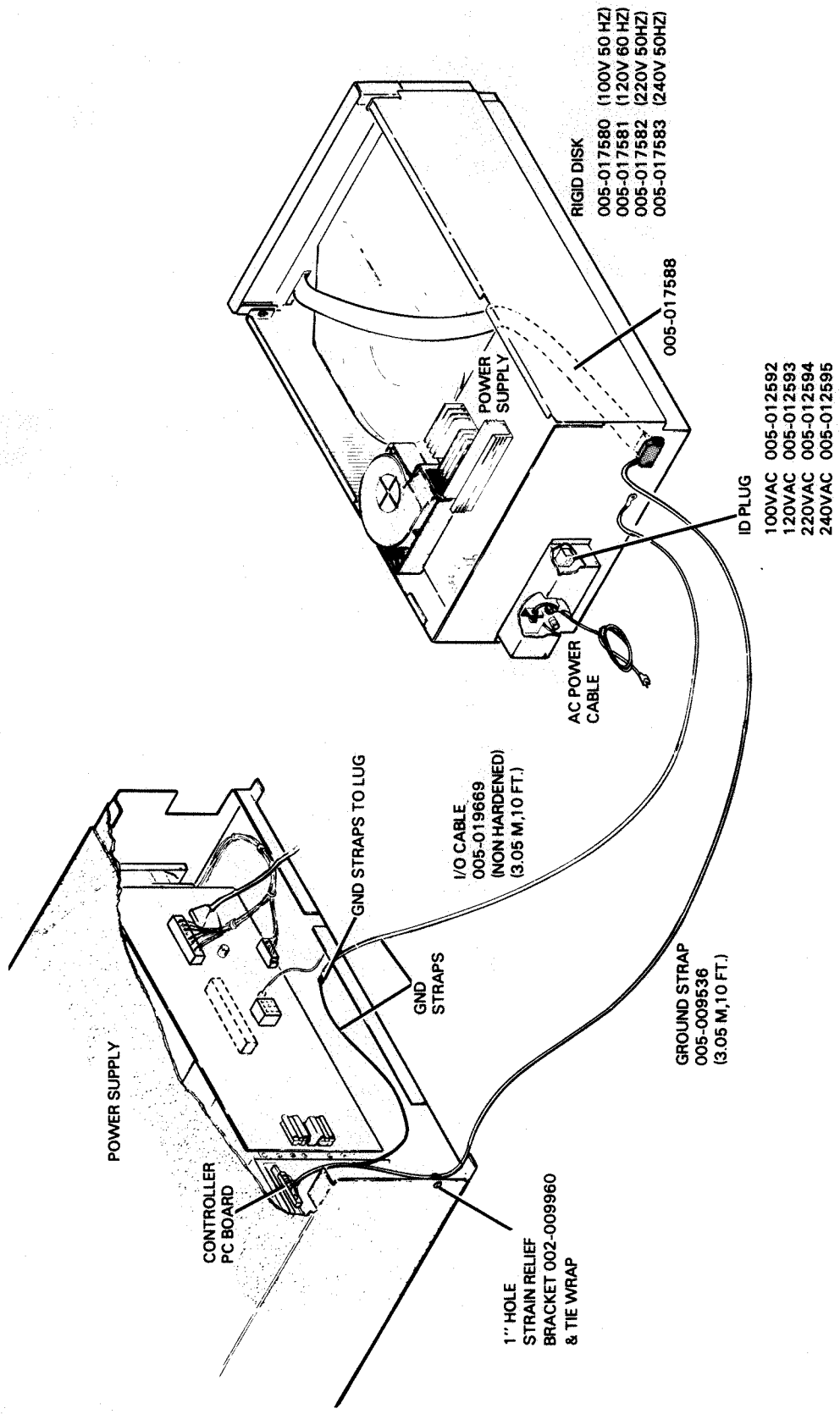


Figure 6-10. 6280 Signal/Power Cable Installation

NOTE

The disk subsystem has been provided with a 1.8 meter (6-foot) power cord and a standard three-prong plug for connection to a polarized 115 Vac outlet. If the subsystem is an international model, the service installer will provide the correct power cord.

5. Check the power ON/OFF switch to make sure that it is in the OFF position.

6. Remove the two screws securing the jumper plug cover (see Figure 6-9).

7. Verify that the ID plug connected at P1/J2 has the correct part number to match the line voltage (see Figures 6-9 or 6-10).

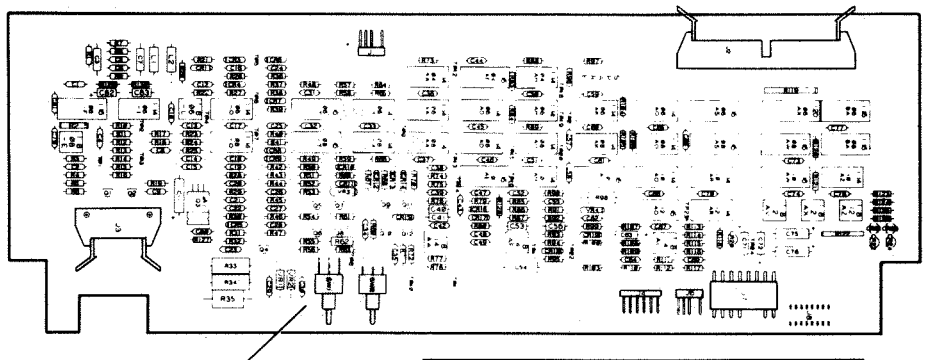
8. Connect the power cord to the drive, then to the power source.

9. Power up the host CPU.

6.7 POWER UP, SHUT DOWN, AND EMERGENCY CONDITIONS

6.7.1 Power Up - Use the following procedure to power up and test the subsystem operation (reference Figures 6-11 and 6-12).

1. Remove the front dress panel and the front FR cover to expose the Unit Select and Write Protect switches located on the Read/Write and Clock PCB (Figure 6-11).



SWITCH SETTINGS	
SWITCH	* OPEN
SW-1	RIGID DISK = UNIT 0 FLEXIBLE DISK = UNIT 1
SW-2	RIGID DISK NOT WRITE PROTECTED
	** CLOSED
SW-1	RIGID DISK = UNIT 1 FLEXIBLE DISK = UNIT 0
SW-2	RIGID DISK WRITE PROTECTED

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Figure 6-11. Read/Write and Clock PCB Switches

2. Set switch SW1 (Unit Select) to right hand position and switch SW2 (Write Protect) to left hand position (Write Protect).

3. Place the power ON/OFF switch to the ON position. When the spindle motor is up to speed. The READY LED goes on (Figure 6-12).

4. Test the disk subsystem using the test programs in Section 4.

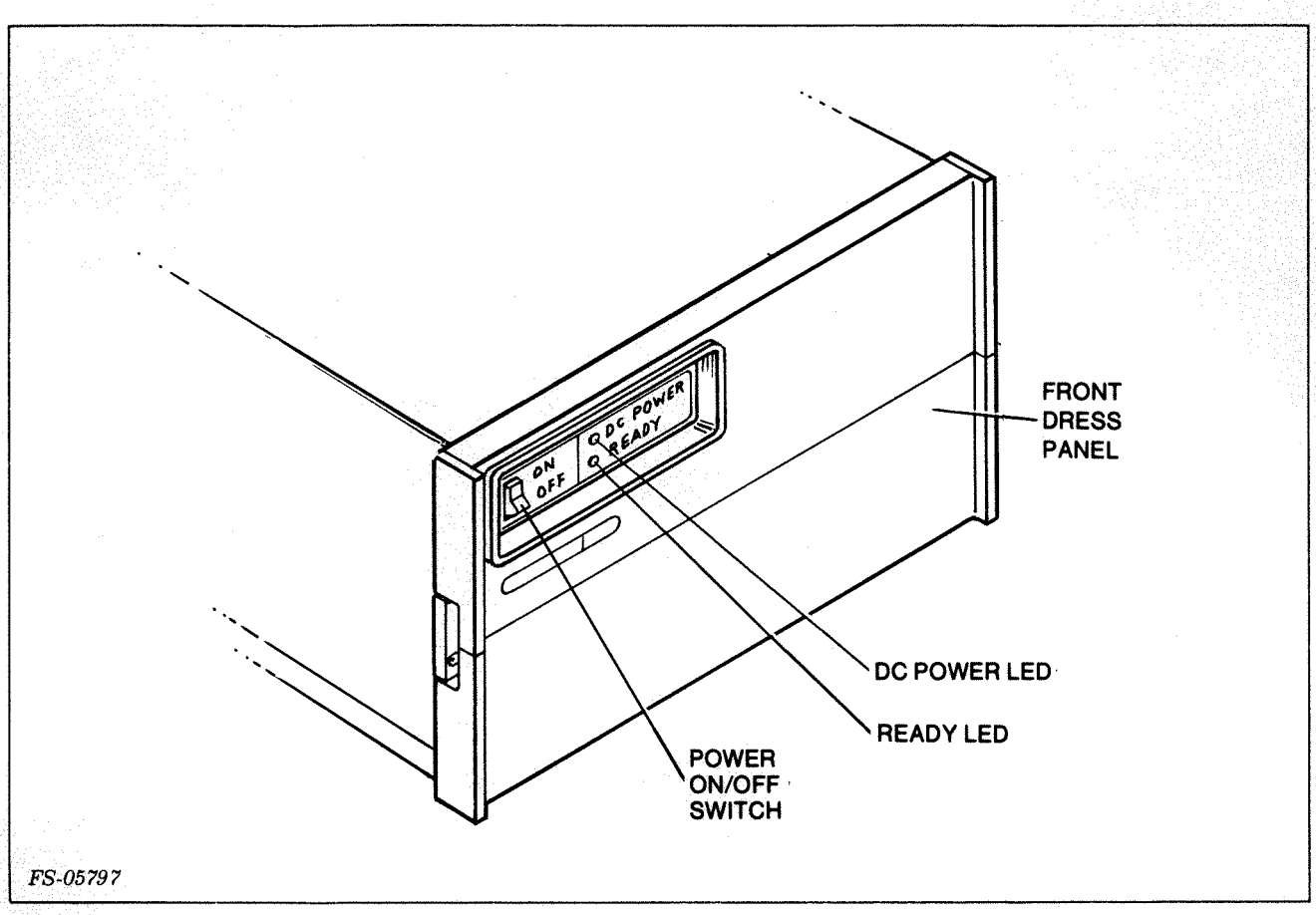


Figure 6-12. Disk Subsystem Front Panel Indicators and Switches

6.7.2 Shut Down - Prior to disk subsystem shut down, make sure that the disk is not in seek, read, or write operation. If none of these actions are in process, place the power ON/OFF switch to the OFF position.

6.7.3 Emergency Conditions - If an emergency condition should arise, place the power ON/OFF switch to the OFF position.

6.8 MODEL 6280 SUPPORTING INSTALLATION FIGURES

Figures 6-13 and 6-14 are included to support the 6280.

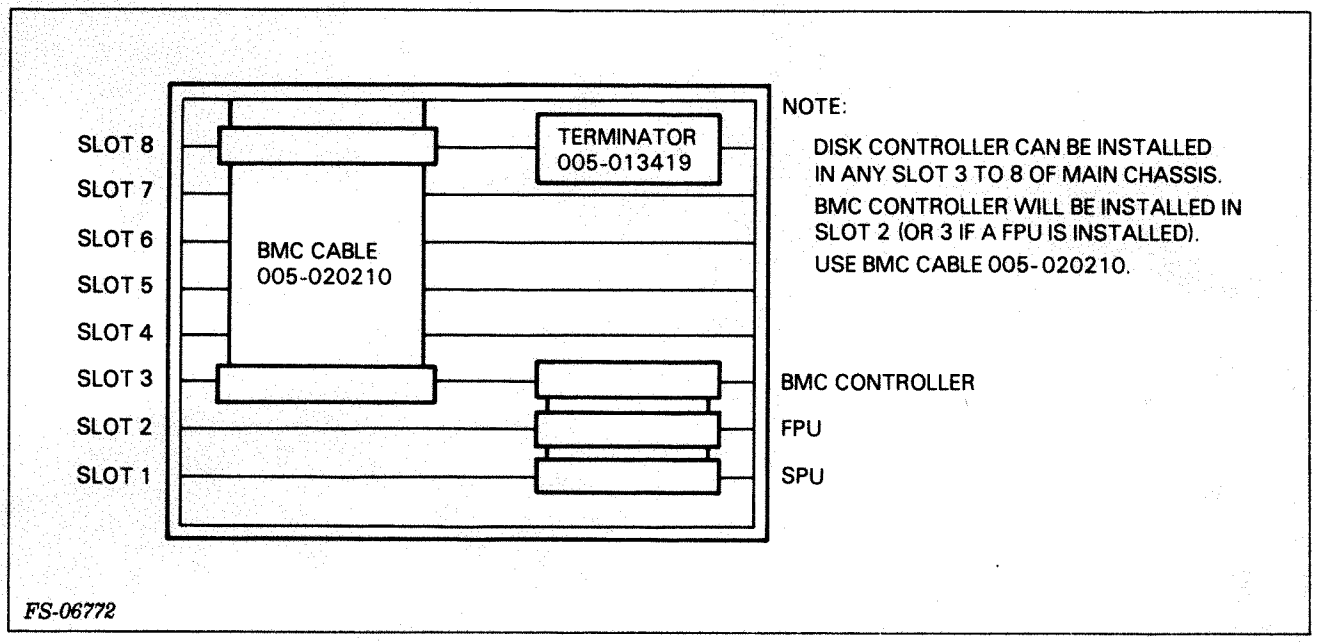
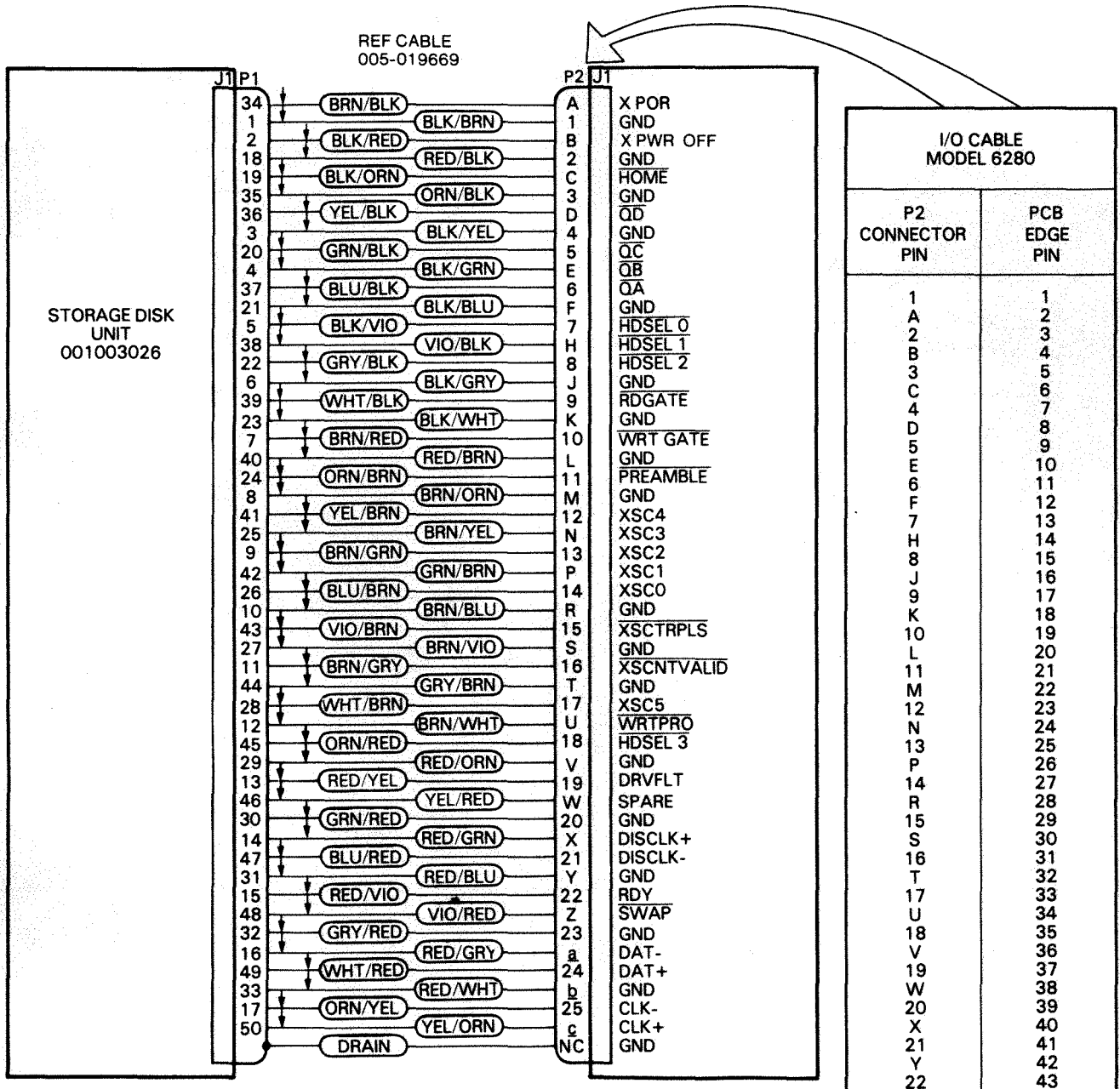


Figure 6-13. Internal BMC Cabling for 6280



I/O CABLE
MODEL 6280

P2 CONNECTOR PIN	PCB EDGE PIN
1	1
A	2
2	3
B	4
3	5
C	6
4	7
D	8
5	9
E	10
6	11
F	12
7	13
H	14
8	15
J	16
9	17
K	18
10	19
L	20
11	21
M	22
12	23
N	24
13	25
P	26
14	27
R	28
15	29
S	30
16	31
T	32
17	33
U	34
18	35
V	36
19	37
W	38
20	39
X	40
21	41
Y	42
22	43
Z	44
23	45
a	46
24	47
b	48
25	49
c	50
NC	NC

NOTE :

UNLESS OTHERWISE SPECIFIED REF. DES. SHOWN ARE FOR OPTION 005-019669. OTHER OPTIONAL SIGNAL CABLES HAVE THEIR OWN REF. DES. (P1 + P2) HOWEVER THEIR CIRCUIT IS IDENTICAL TO A CORRESPONDING SECTION OF CABLE 005-019669

FS-06773

Figure 6-14. 6280 Paddle Board Connector Cable Schematic

6.9 INSTALLATION OF OPTIONAL FLEXIBLE DISK DRIVE

Installation instructions for the flexible disk drive will be found in Data General maintenance manual 015-000109 for Model 6096.

Figures 6-15 through 6-21 are included to support the flexible disk drive installation for Models 6096-CV and 6096-CD with a Model 6234.

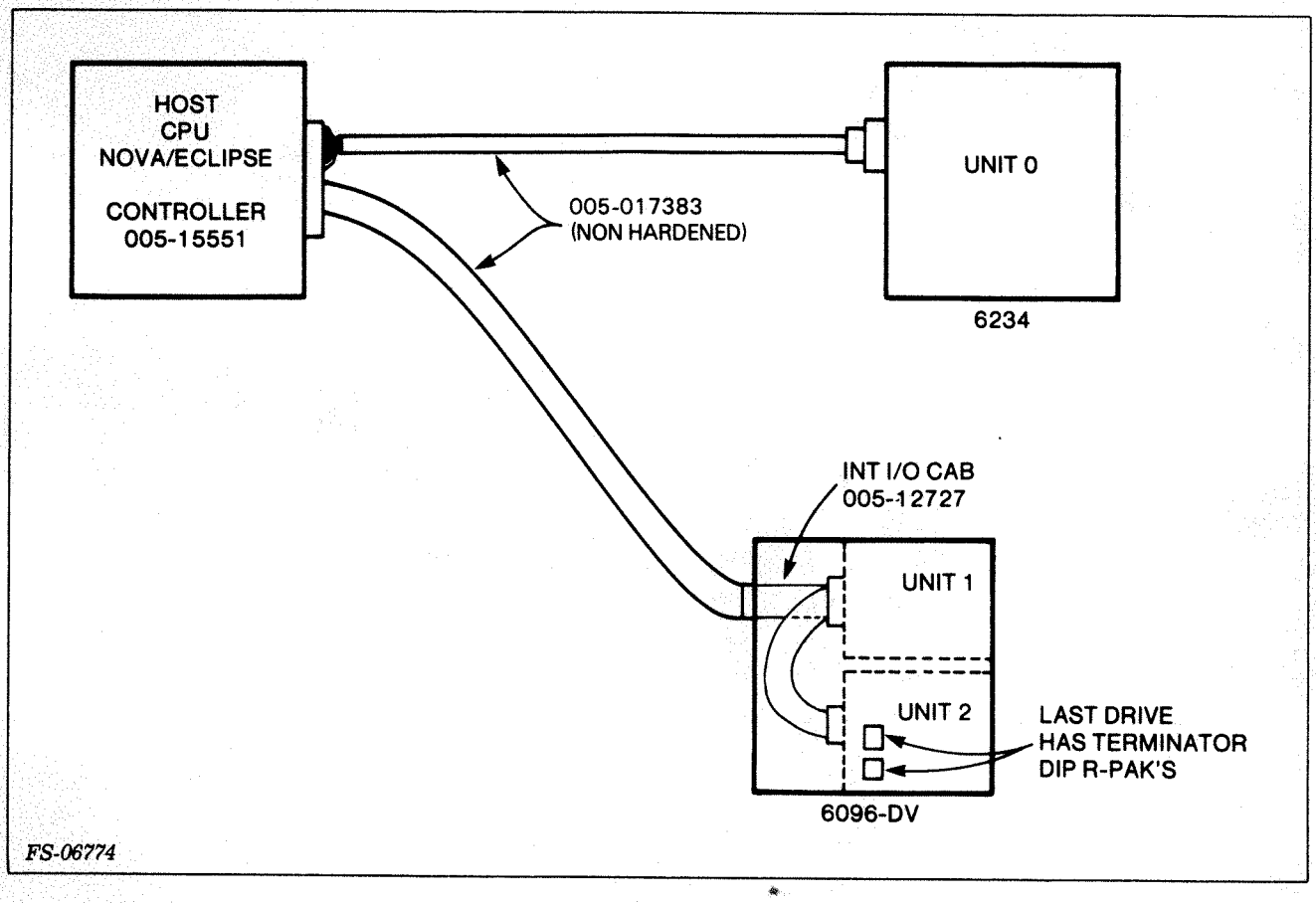
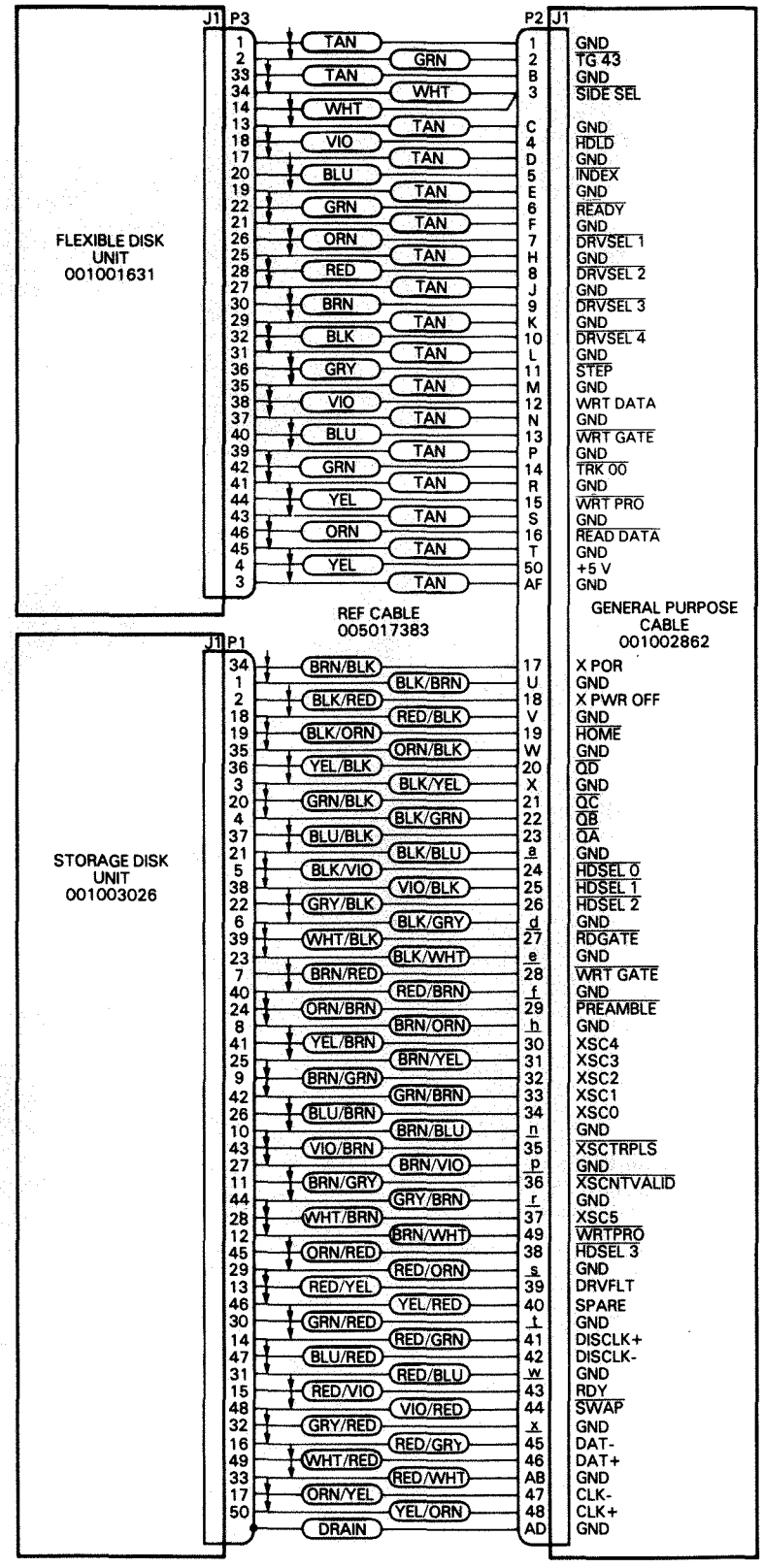


Figure 6-15. 6234 with Dual Flexible Drive Option

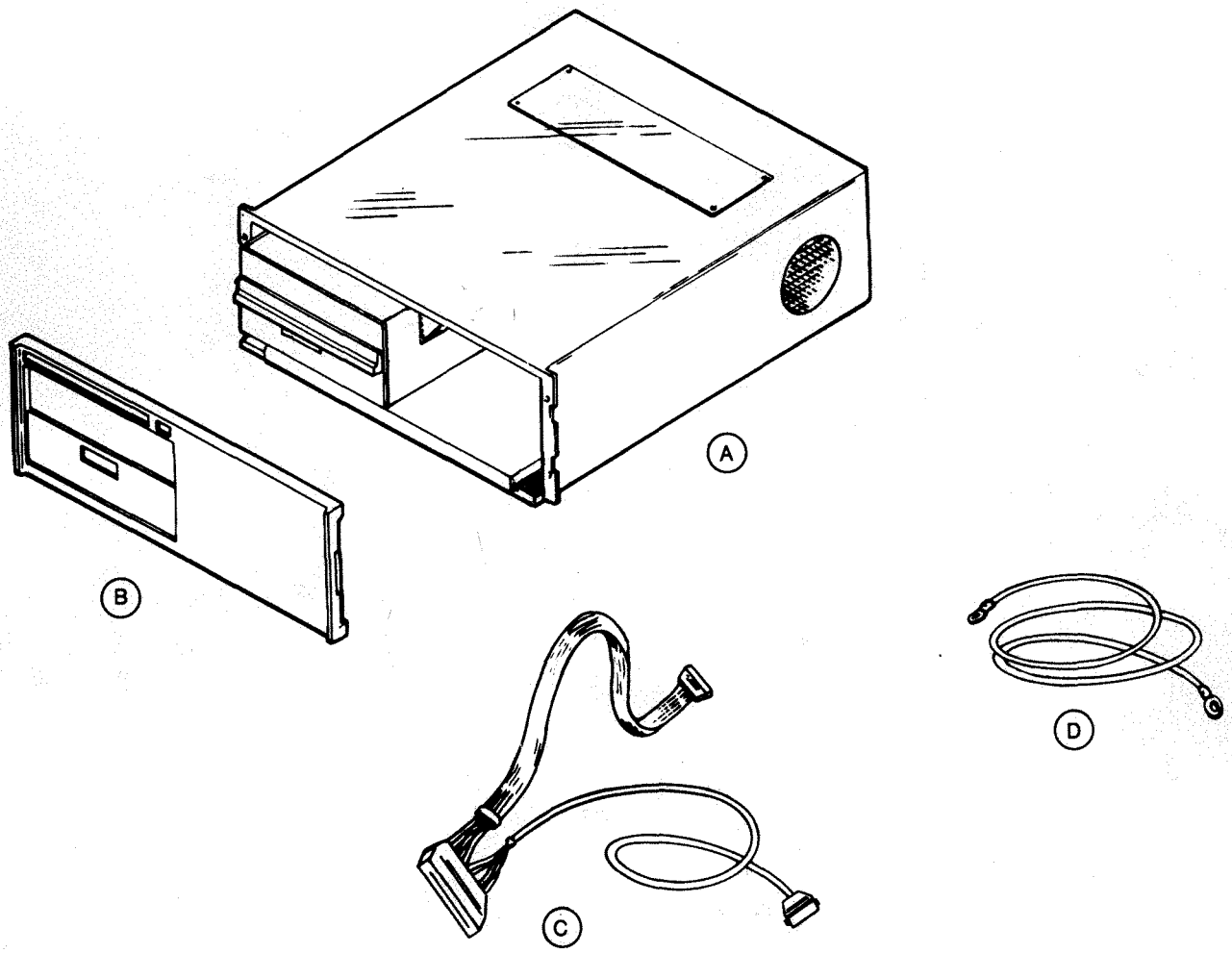


NOTES:
1. UNLESS OTHERWISE SPECIFIED REF DES. SHOWN ARE FOR OPTION 005017383. OTHER OPTIONAL SIGNAL CABLES HAVE THEIR OWN REF. DES.(P1 + P2) HOWEVER THEIR CIRCUIT IS IDENTICAL TO A CORRESPONDING SECTION OF CABLE 005017383.

2. OPTIONAL CABLE:
STG. DISK/CPU (005017587) 018001085
DOUBLE FLPY/CPU (005013637) 018000580
DOUBLE FLPY/STG DISK/CPU (005017383) 018001060

FS-05972

Figure 6-16. 6234 Paddle Board Connector Cable Schematic



MAJOR COMPONENTS

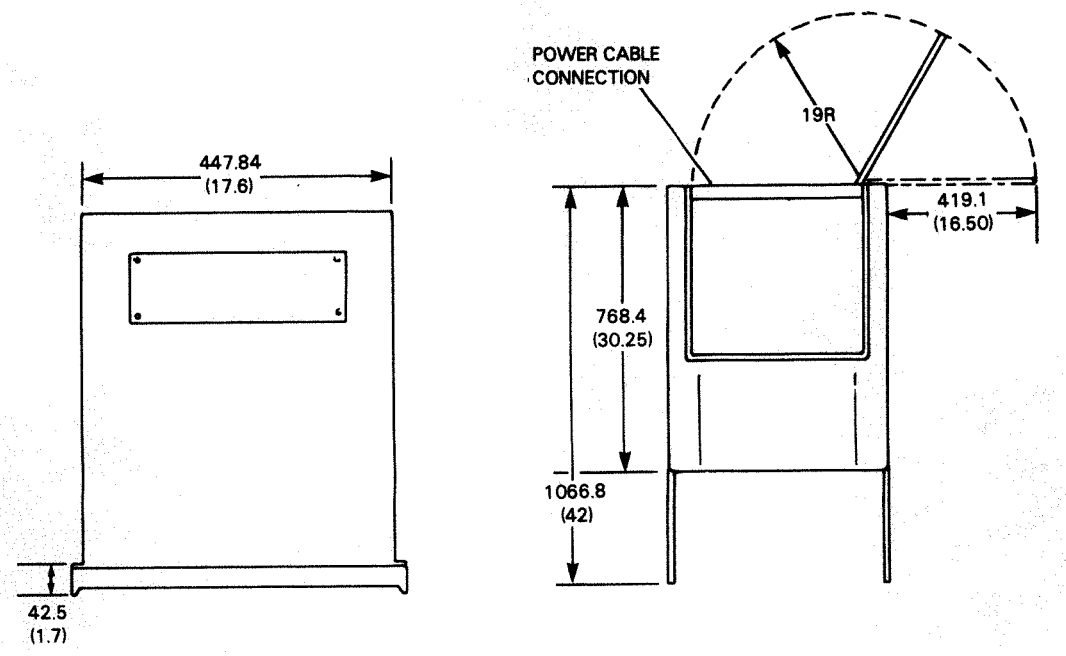
ITEM	COMPONENT	MOUNTING LOCATION	NOTES
A	ENCLOSURE W/TWO DRIVES	CABINET	
B	FRONT PANEL	CABINET	

CABLE

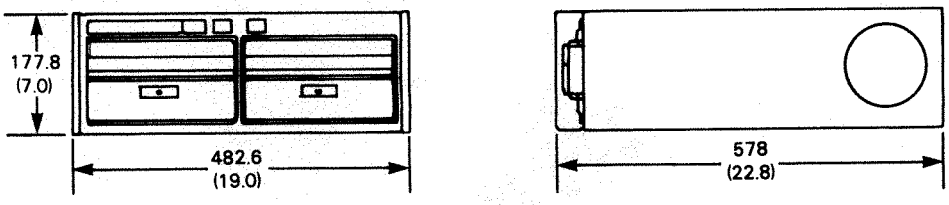
ITEM	CABLE	CONNECTING	MAX ALLOWED LG		NOTES
			FT	M	
C	I/O CABLE	CONTROLLER AND DRIVE	10	3	005-017383
D	GROUND CABLE	CPU AND DRIVE	10	3	005-009536

FS-05973

Figure 6-17. Add-on 6096-CV Installation Specifications (sheet 1 of 2)



Dimensions in mm (in)



DIMENSIONS:	WIDTH	DEPTH	HEIGHT
Millimeters	482.6	578.0	177.8
Inches	(19.0)	(22.8)	(7.0)

SERVICE CLEARANCES:	FRONT
Millimeters	914.4
Inches	(36)

WEIGHT:	
Kilograms	22.7
Pounds	50

HEAT OUTPUT:	WATTS	BTU/HR
	80	273.2

OPERATING ENVIRONMENT:		
Temperature (max)	43°C	109°F
Relative Humidity (max)	85°F	Wet bulb
Altitude	3048m	(10,000 ft)

POWER REQUIREMENTS:			
(Domestic)			
Voltage	120 V		
Hz	60		
Max Amp per Phase	0.67 A		
Phase	1		
Startup Surge per Phase	11.A		
(Export)			
Voltage	100 V	220 V	240 V
Hz	50	50	50
Max Amp per Phase	0.80 A	0.36 A	0.33 A
Phase	1	1	1
Startup Surge per Phase	0.94 A	0.42 A	0.39 A

CABLES:		
Primary Power		
	Length	DGC Cable No.
Domestic 60 Hz	1.8m(6')	1118E
120 V		
Export 50 Hz		
100 V	1.8m(6')	1118D
220 V	1.8m(6')	1118G
240 V	1.8m(6')	1118F

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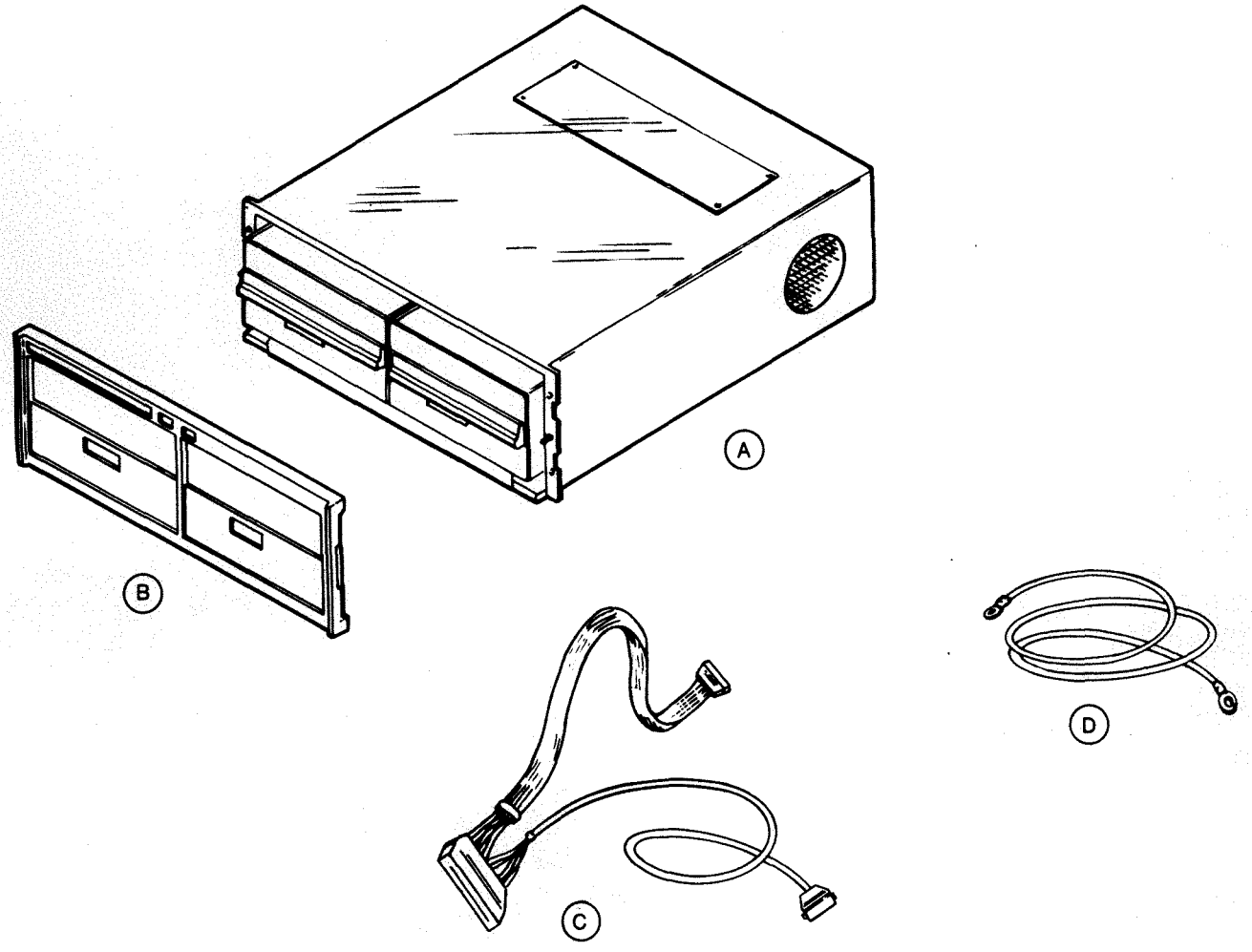
Figure 6-17. Add-on 6096-CV Installation Specifications (sheet 2 of 2)



MAJOR COMPONENTS

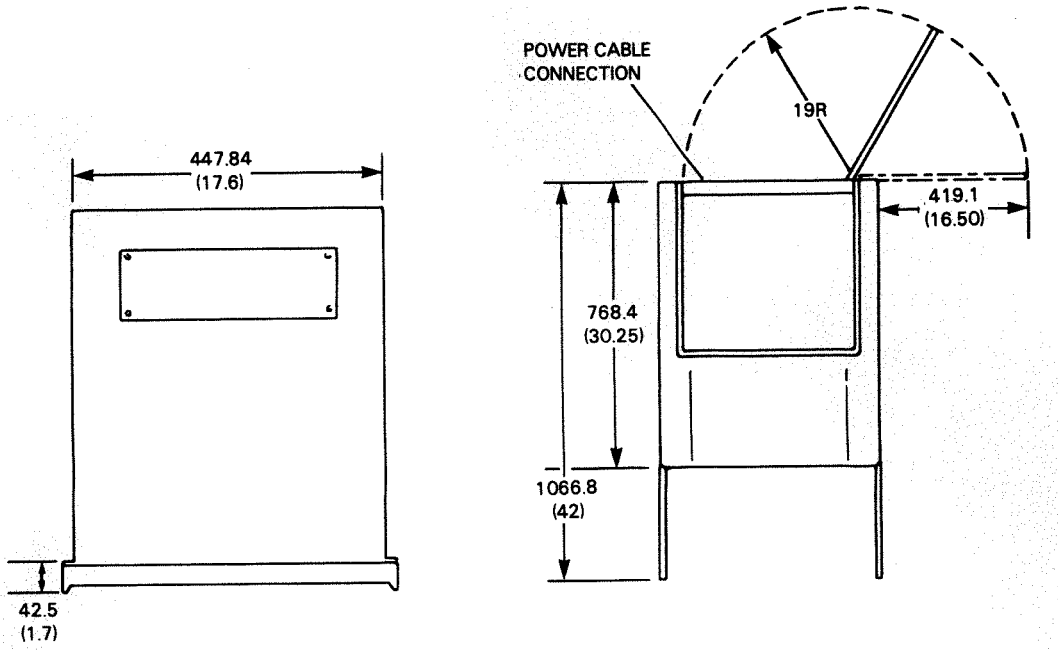
ITEM	COMPONENT	MOUNTING LOCATION	NOTES
A	ENCLOSURE W/TWO DRIVES	CABINET	
B	FRONT PANEL	CABINET	

CABLE

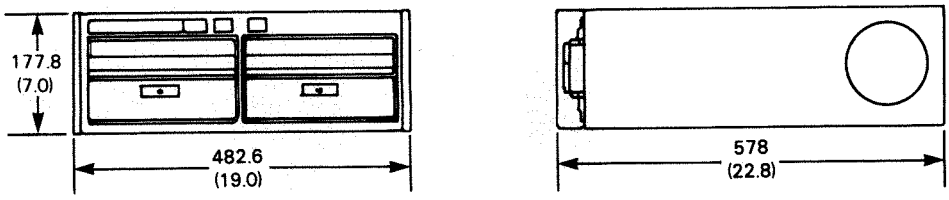
ITEM	CABLE	CONNECTING	MAX ALLOWED LG FT / M	NOTES
C	I/O CABLE	CONTROLLER AND DRIVE	10 / 3	005-017383
D	GROUND CABLE	CPU AND DRIVE	10 / 3	005-009536

FS-05974A

Figure 6-18. Add-on 6096-CD Installation Specifications (sheet 1 of 2)



Dimensions in mm (in)



DIMENSIONS:	WIDTH	DEPTH	HEIGHT
Millimeters	482.6	578.0	177.8
Inches	(19.0)	(22.8)	(7.0)

SERVICE CLEARANCES:	FRONT
Millimeters	444.5
Inches	(17.5)

WEIGHT:	
Kilograms	29.5
Pounds	65

HEAT OUTPUT:	WATTS	BTU/HR
	140	478.1

OPERATING ENVIRONMENT:		
Temperature (max)	43°C	109°F
Relative Humidity (max)	85°F	Wet bulb
Altitude	3048m	(10,000 ft)

POWER REQUIREMENTS:			
(Domestic)			
Voltage	120 V		
Hz	60		
Max Amp per Phase	1.2 A		
Phase	1		
Startup Surge per Phase	1.4 A		
(Export)			
Voltage	100 V	220 V	240 V
Hz	50	50	50
Max Amp per Phase	1.4 A	0.64 A	0.58 A
Phase	1	1	1
Startup Surge per Phase	1.6 A	0.75 A	0.68 A

CABLES:

Primary Power

	Length	DGC Cable No.
Domestic 60 Hz	1.8m(6')	1118E
120 V		
Export 50 Hz		
100 V	1.8m(6')	1118D
220 V	1.8m(6')	1118G
240 V	1.8m(6')	1118F

FS-05974A

Figure 6-18. Add-on 6096-CD Installation Specifications (sheet 2 of 2)

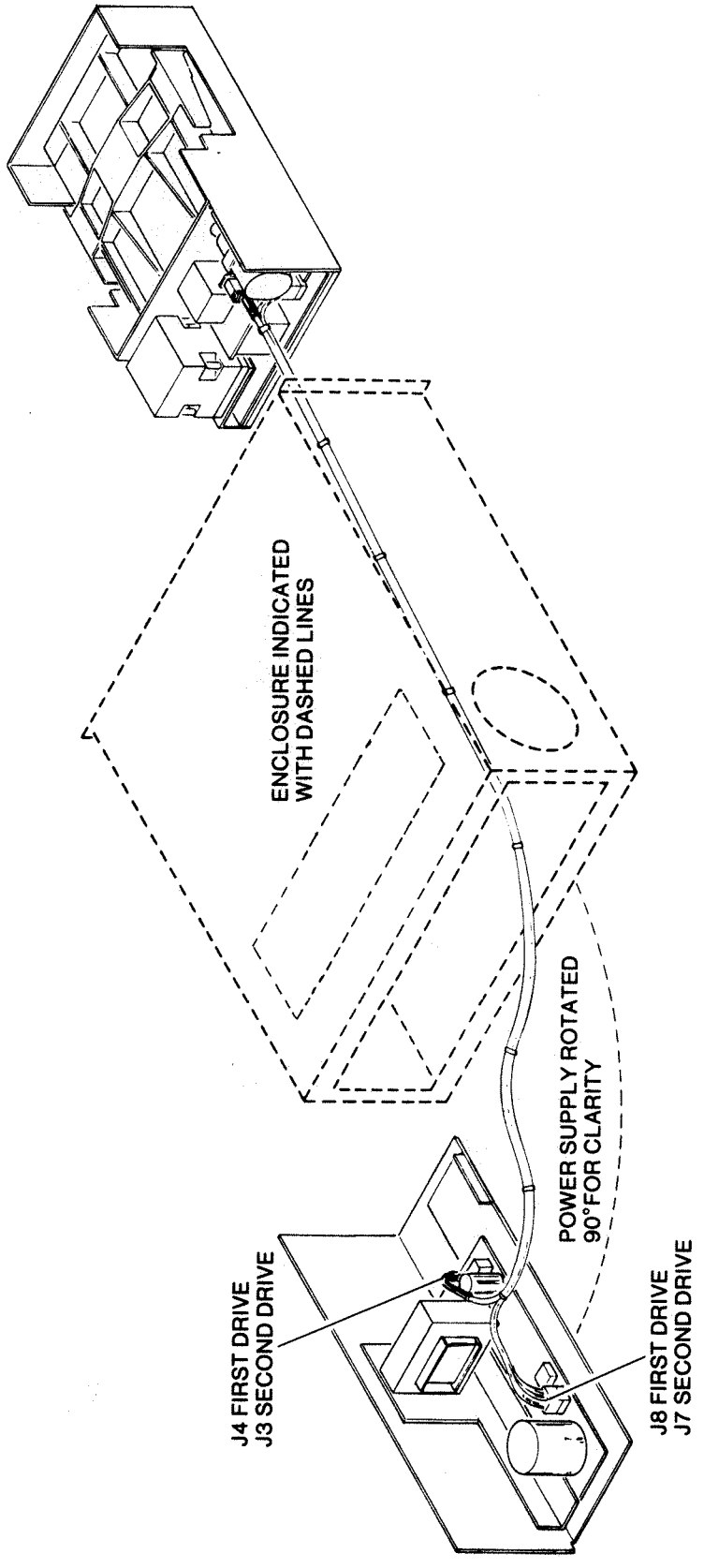


Figure 6-19. 6096-CV/CD Internal Cabling for AC/DC Power

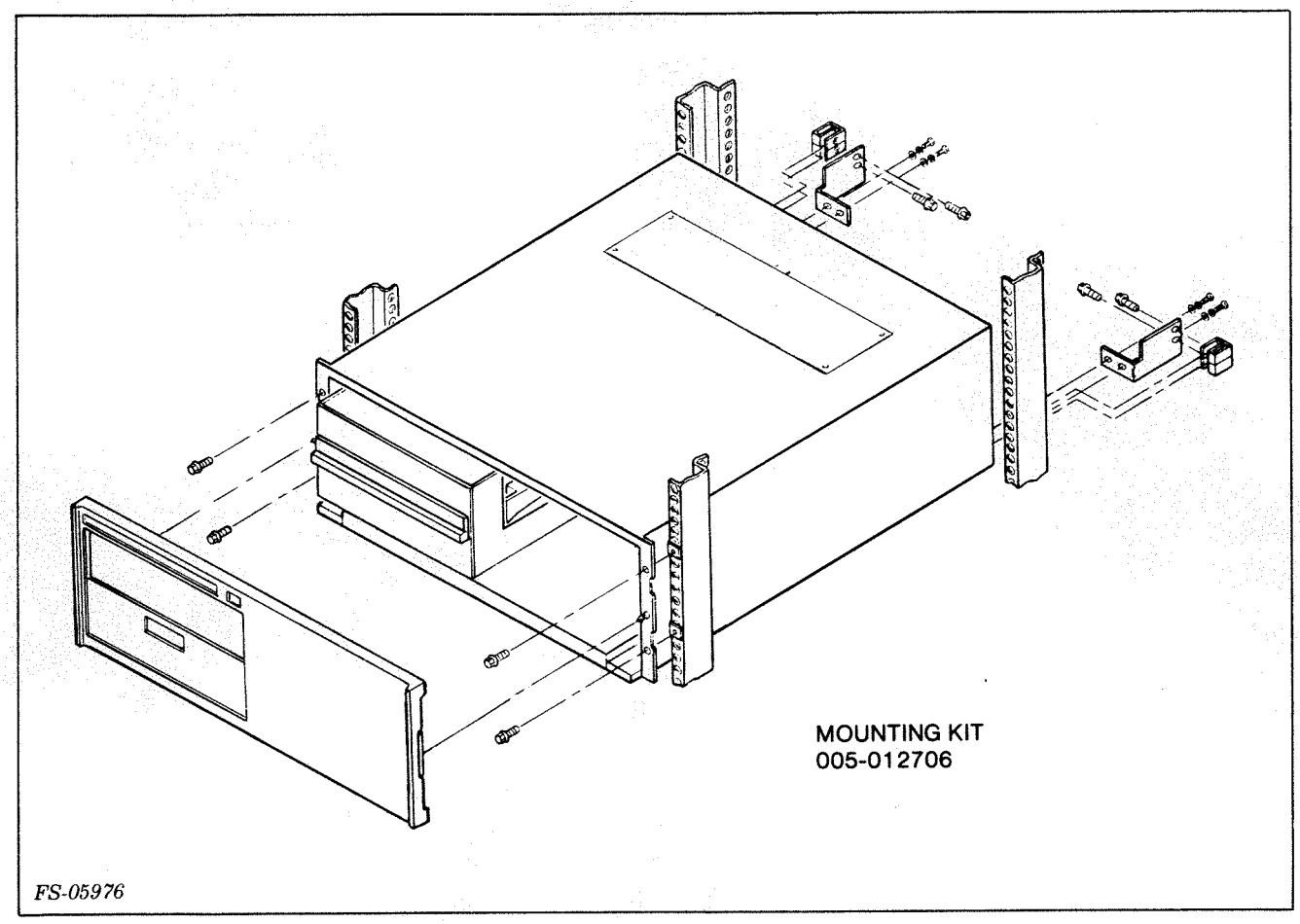
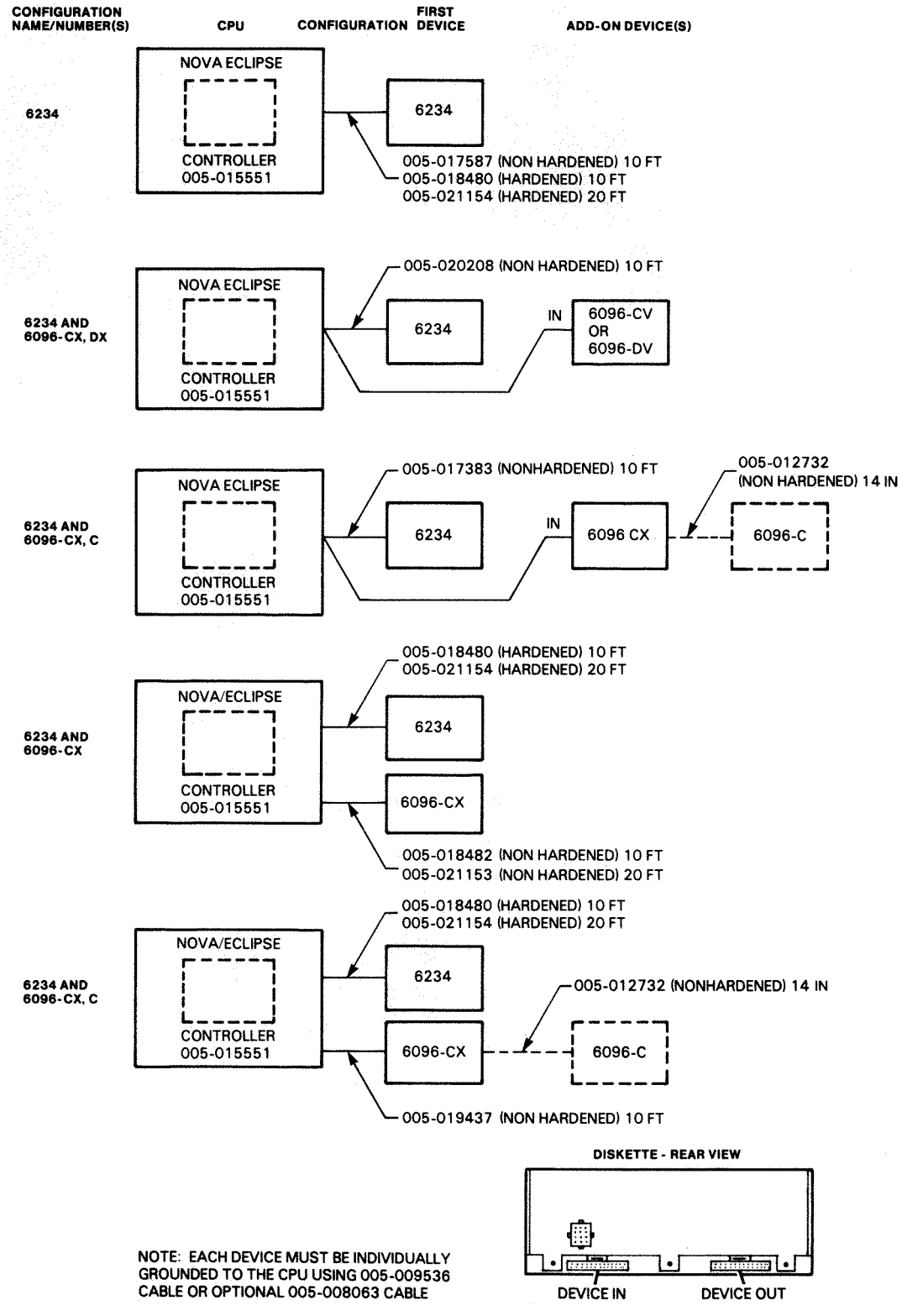


Figure 6-20. 6096-CV/CD Cabinet Mounting



FS-06775

Figure 6-21. Configuration Diagram, 6234/6096

6.10 REMOVAL/REPACKING

In the event the disk subsystem is to be shipped to another location, careful packing minimizes the possiblity of damage. Use the following procedure for removal and repacking the drive.

1. Power down the disk subsystem to be repacked.
2. Power down the host CPU.
3. Open the back cabinet door.
4. Disconnect the power and I/O cables from the disk subsystem.
5. Remove the front dress panel (see Figure 6-6). Panel will release when pulled forward.
6. Remove the two chassis mounting screws (see Figure 6-6).
7. Pull the disk subsystem forward until slide stop is felt.

CAUTION

The disk subsystem weighs 37.3 kilograms (82 pounds). Two service people are required to lift the disk subsystem.

8. With the aid of a second person, disengage the disk subsystem from the slide rails and place the drive on its side.
9. Remove the bottom cover (see 5.3).
10. Move the positioner stop to the lock position (see Figure 6-7).
11. Lock the spindle by engaging the captive screw (see Figure 6-7).

WARNING

The disk subsystem warranty can be voided if the subsystem is not properly secured prior to shipment.

12. Obtain the original shipping carton. The shipping carton should contain three foam shipping wedges. Insert the foam shipping wedges as shown in Figure 6-8.
13. Replace the bottom cover removed in step 8.
14. Remove the chassis slide from each side of the disk drive by removing the four retaining lock washers and screws. Save this hardware so that it may be installed on the replacement drive.
15. Pack the disk subsystem into the original shipping carton as shown in Figure 6-2.
16. Power up the host CPU.

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