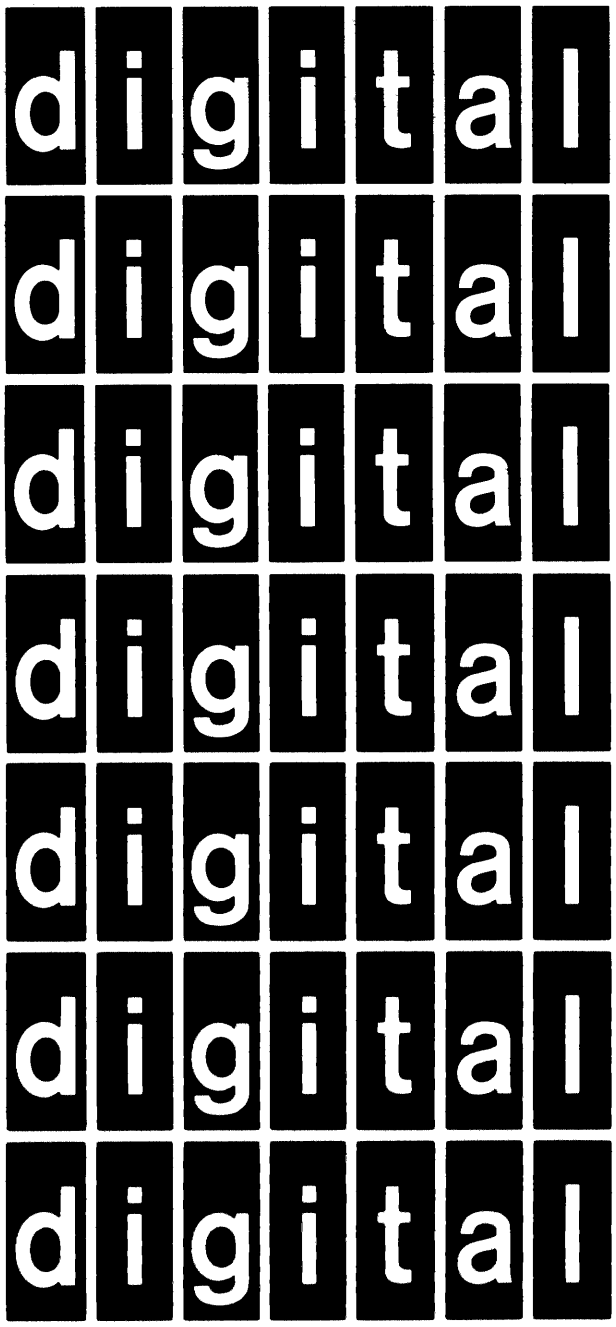


PCL11 Communications Systems

General Introduction and Configuration Guide

Computer Special Systems

NOTEBOOK SECTION

OPTION NUMBER

PCL11-B

DRAWING SET NUMBER

B-DD-PCL11-00

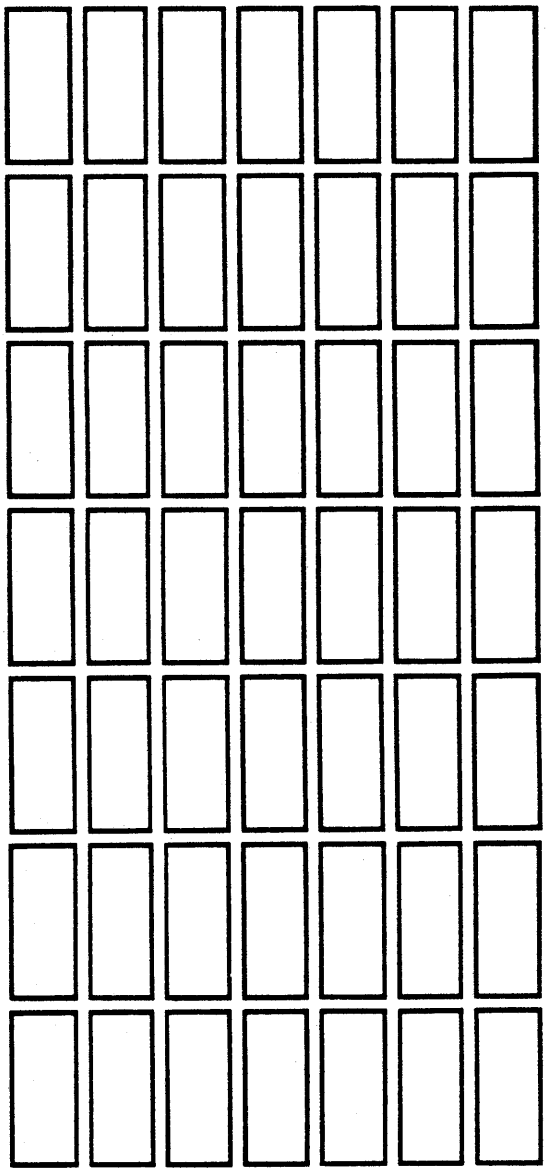
PROGRAM NUMBER

CZPLABAO
CZPLAAO

DOCUMENT NUMBER	**REVISION**
YC-A20TC-01	B

DATE

FEBRUARY 1979



PCL11 Communications Systems

General Introduction and Configuration Guide

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Computer Special Systems

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SECTION 1

INTRODUCTION

1.1 General Description

A PCL11 Communications System is a network which enables data communication between a number of PDP-11 computers. This system is suitable for the building of high availability, high reliability multiprocessor networks. Sixteen bit words are transferred over parallel data lines between up to 16 PDP-11 computers. Data transferred is checked using CRC and parity detection techniques. The data is transferred over an interconnecting bus called the TDM Bus, which provides a highway for communication between any unit attached to the bus. Computers may be added or removed from the system by attaching to or detaching from this bus. Units may be removed from the TDM Bus for maintenance functions without breaking or "hanging" the bus.

1.2 General Operation

Figure 1.1 shows a general block diagram for a PCL11 Communications System. Each computer that is part of the network has a PCL11-B interface unit attached to its Unibus. This unit is the heart of the communications system as it provides an interface between the Unibus and the TDM Bus. Each PCL11-B may control transfer of parallel 16 bit words to another PCL11-B over the bus. The PCL11-B contains independant logic to control both transmission the reception of messages simultaneously. The transmit logic may retreive data directly from memory via DMA access to transfer to another PCL11-B on the TDM Bus. Similarly, the receive section may receive data from any unit on the bus and transfer it directly to memory via DMA transfers.

The TDM Bus is a time division multiplexed bus. This means each transmitter is assigned a certain "timeslice" by a bus controller within which one data word of a message may be sent to a receiver. In a PCL11 Communication System this controller is called the TDM Bus Master. Each PCL11-B contains master logic and one unit on the bus is designated as TDM Bus Master. A different unit may be assigned to be Secondary Master. This unit would become Master automatically in the event that the first Master was powered down or otherwise disabled.

1.3 Features

The PCL11 Communication System has many features desirable in a multiprocessor system to ensure security and speed of transfer as well

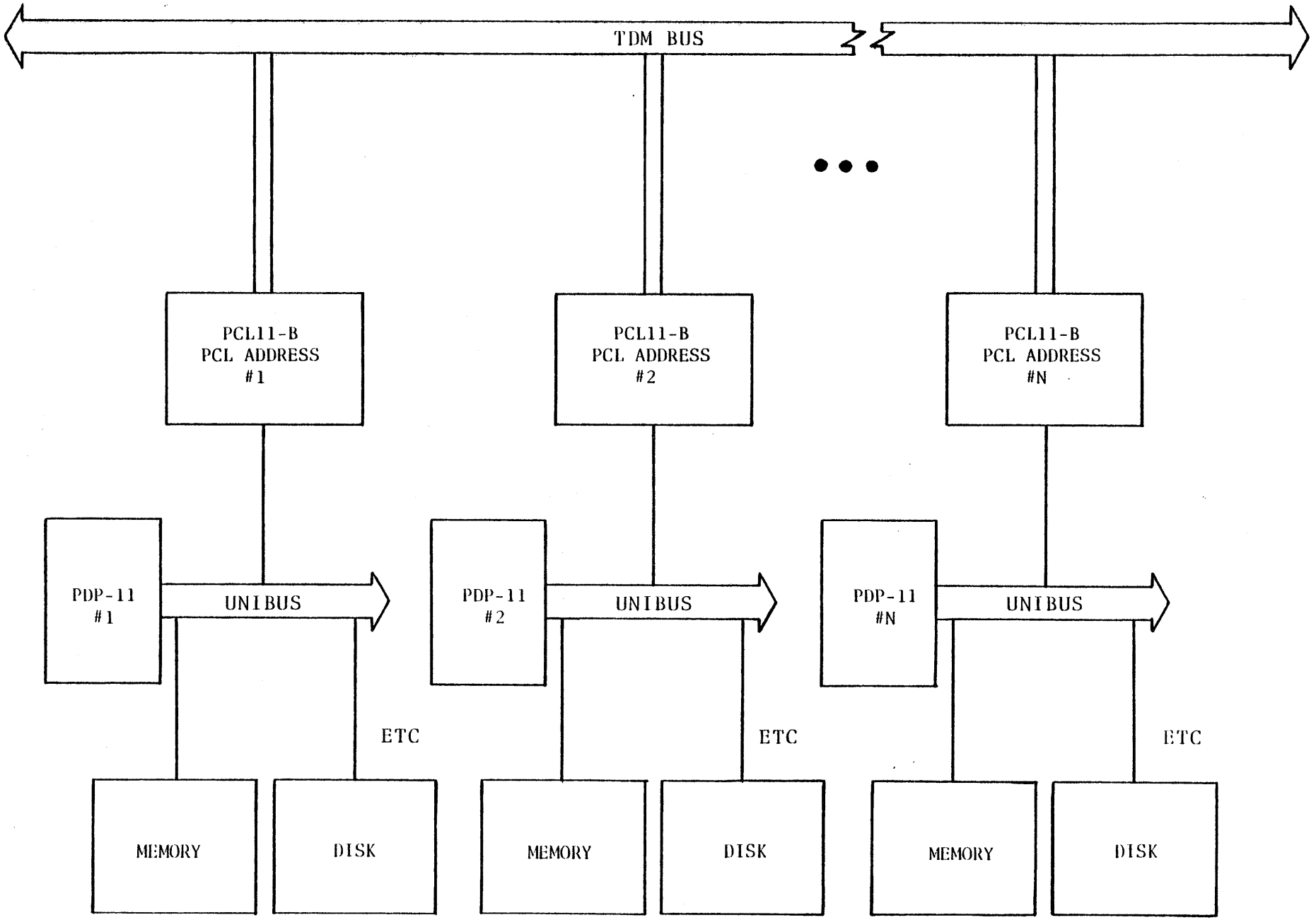


FIGURE 1.1
PCL11-B SYSTEM BLOCK DIAGRAM

as ease of maintenance. These include:

- Minimal software involvement required in the transmission of data. Data to be transferred from one PCL11-B to another may be retrieved from memory over the Unibus using Direct Memory Access (DMA). Similarly, data received from another PCL11-B may be moved into memory using DMA.

- Data is transferred over a Time Division Multiplexed (TDM) bus. Time Division Multiplexing implies that each transmitting PCL11-B unit will be assigned a period of time, at a regular interval, to transfer a data word. In such a scheme a number of PCL11-B units may be in the process of transmitting data simultaneously. No single unit may "hang up" the bus in this system.

- Both receiver and transmitter have FIFO (First In First Out Data Silo) buffers for the data being transferred. This ensures that there are no synchronization problems between the TDM Bus and the Unibus. The PCL11-B units will wait, without error, until there is room for more data in the FIFO before accepting a word off of the TDM Bus or initiating a transfer from memory on the Unibus.

- The receiver may reject or terminate messages it does not wish to complete.

- Time Division Multiplexing implies each transmitter has a certain time in which to transfer data, and thus may use only a certain percent of bus bandwidth. The percentage alloted to each transmitter may be changed by the software in the computer of the designated Master PCL11-B

- Block CRC-16 and word parity error detection on every message.

- Secure communications. Message is not considered complete until all CRC and parity checks have been accomplished successfully and the data has been moved from one Unibus to another. Any error condition will abort the messages which would then be retransmitted under software control. The available PCL11-B software driver (RSX11-M) will automatically retransmit a message upon error.

- PCL11-B units connect to the TDM BUS in a T-Junction. This means any unit may be disconnected from the TDM bus without breaking the connection between any other units on the bus.

- Units may be powered down without halting bus operation. This is a valuable maintenance feature because in the event of a failure in any PCL11-B, the unit may be turned off and removed for diagnosis without stopping other activity in the system.

- Flexibility and expandibility. A new system may be added to the system with the addition of only one interface to the TDM Bus on the new computer. All other computers already in the system may communicate with the new computer using their existing hardware.

1.4 Software

PCL11-B Communications interfaces are fully supported with a RSX11-M Device Driver. A description of the functions of the Driver is contained in section 3.6.

1.5 Reference Documents

This manual is intended to give a general overview of a communications system. For a more detailed decription of the various components of a system refer to one of the following following documents:

Document Description	Document Number
PCL11-B Option Description	YC-A20TC-00
PCL11-B Communications System (Installation and Maintenance Guide)	YC-A20TC-02
RSX11-M PCL User Guide	YC-T012C-U0
RSX11-M PCL Driver Documentation (Support Manual)	YC-T012C-S0

1.6 Specifications

MECHANICAL

Mounting	PCL11-B interface requires space for a nine slot double system unit backplane. PCL11-B is not suited for mounting in a BA11-L mounting box.
Modules	PCL11-B contains 7 hex sized modules and one quad sized module.
Cables	Each PCL11-B is shipped with 1 BC20K cable to implement the T-junction. BC20P-xx cables are required to connect together units contained in separate mounting boxes.
TDM Bus length	Maximum TDM bus length is 300 feet (90 meters)
Max no. of PCL11-B units on TDM bus	16

ELECTRICAL - PCL11-B

Voltage/ Current	14 amps ` +5 volts .5 amps ` -15 volts
Logic Levels	TTL
Common Mode	No common mode voltage is acceptable between units.

OPERATIONAL

TDM bus Bandwidth — This depends on bus length as per the following table

BUS LENGTH	50'	100'	240'	300'
BUS BANDWIDTH (KBYTES/SEC)	1000	800	500	400

Message Length	64 K bytes
Error Detection	Parity checked on each word CRC character checked after 200(octal) words

SECTION 2

SYSTEM CONSIDERATIONS

2.1 Suitablity

PCL11 Communication Systems are suitable for building multiprocessor networks using PDP-11 computers. These multiprocessor systems are suitable for a variety of general applications.

Distributed functionality systems may be built in which tasks may be assigned to various computers in the network. The network may appear as a single unit to the user with some control software assigning the tasks to an appropriate unit through the PCL11 Network. This assignment may be made on the basis of availability or suitability of the computers in the system.

Data aquistion systems may be built using a number of smaller computers to handle inputting of data. These computers may perform simple operations on the data and pass the results on to other computers over the PCL11 link. This system has the advantage of not loading down one computer with the aquistion as well as the manipulation of data. It also has the flexibility of passing control instructions back over the link to the other computers.

In a similar manner distibuted control systems may be put together. These would have the peripheral computers interfaced with the hardware to be controlled and receiving instructions over the PCL11 link.

Building a multiproccesor system to handle problems requiring large computing power has advantages over solving the same problem with one big computer. PCL11 multiprocessor systems are very flexible and can be easily expanded or changed to meet new system needs. These systems can be built by an initial investment of only a few computers and expanded later when larger capability is needed. PCL11 is designed to allow parts of the system to be turned off for repair without bringing down the whole system. Thus in the event of a failure a system may still run in a degraded mode until the problems are resolved.

2.2 Site Considerations

Before configuring a PCL11 Communications System review carefully the system specifications found in this document (section 1.6) and in the Installation and Maintenance guide (YC-A20TC-02). The proposed system should be evaluated to determine whether there will be any problems such as common mode voltage between between units, supply of power for the units, etc. In the event of any difficulty in determining

that the system will meet the needs of the desired application, a CSS Application Engineer should be consulted.

As well as system specifications, the site consideration and site preparation sections of the Installation and Maintenance Guide should be consulted. The site considerations and the installation procedure for the PCL11-B unit is contained in the Option Description (YC-A20TC-00) and should be reviewed as well.

2.3 Physical Description

As indicated in figure 1.1 a system consists of a number of PCL11-B units connected together via a TDM Bus. The PCL11-B unit is described in detail as far as operation, specifications, installation, etc., in the PCL11-B Option Description (YC-A20TC-00). Shipped with every PCL11-B unit are the logic boards and backplane required for the interface as well as all prints, diagnostics, and manuals required for installation and operation of the unit. A TDM Bus terminator (one terminator, which is passive and does not require power, must be connected at each end of the bus) is included along with a short section of TDM Bus cable (the T-junction, BC20K). The only other hardware which must be obtained for a system is an extension TDM Bus cable (BC20P-xx) required whenever two PCL11-B units are mounted in separate mounting boxes.

2.4 Configuration Possibilities

Not all systems need be simple TDM Bus systems as outlined in figure 1.1. Figure 2.1 shows a dual TDM Bus system configuration. This type of configuration is suitable for high relialability applications. If any problems were detected on the main TDM Bus then backup is provided by the second bus. This second bus can also be used for messages during normal operation. Since both busses may operate indepentantly, the throughput of the system may be increased. The dual bus concept may be expanded to three or more busses. This would be suitable for systems that require a heavily loaded bus, a faster lightly loaded bus and a backup bus.

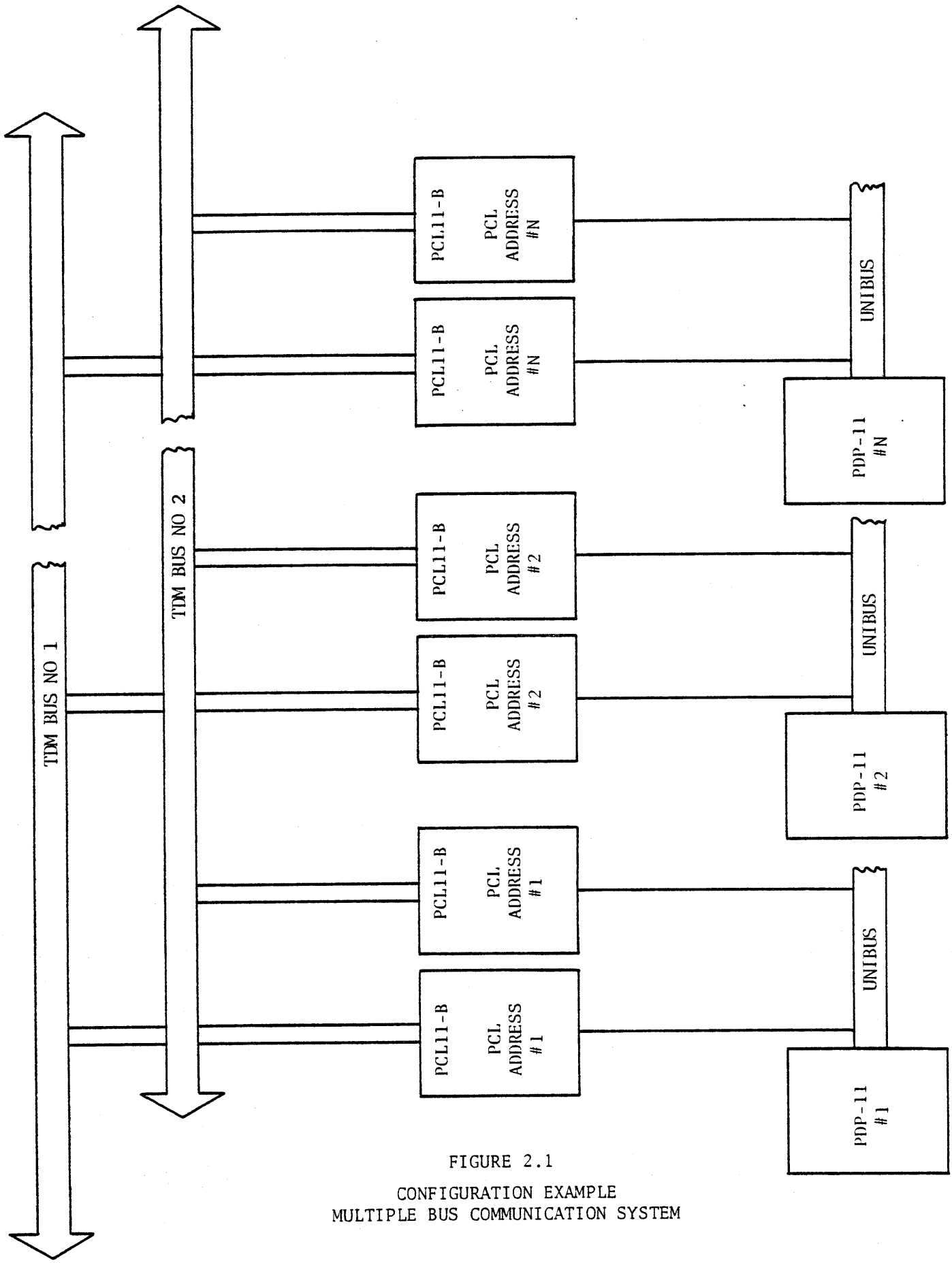


FIGURE 2.1

CONFIGURATION EXAMPLE
MULTIPLE BUS COMMUNICATION SYSTEM

SECTION 3

GENERAL OPERATION

3.1 General Outline

Systems are comprised of a number of PCL11-B units connected together as shown in Fig 1.1. Each PCL11-B unit contains three sub-sections of logic called the Transmitter, the Receiver and the Master section. Each transmitter and receiver on the TDM Bus has its own unique five bit address on the TDM Bus which is set up during installation on switches in the logic modules. Messages are sent between the transmitter logic of the PCL11-B unit and the receiver logic of the receipient unit. The timing required on the TDM Bus is generated by a PCL11-B unit which is designated as the TDM Bus Master. The logic to generate this timing is contained in the Master section in all PCL11-B units, but only one of these may be enabled at any one time.

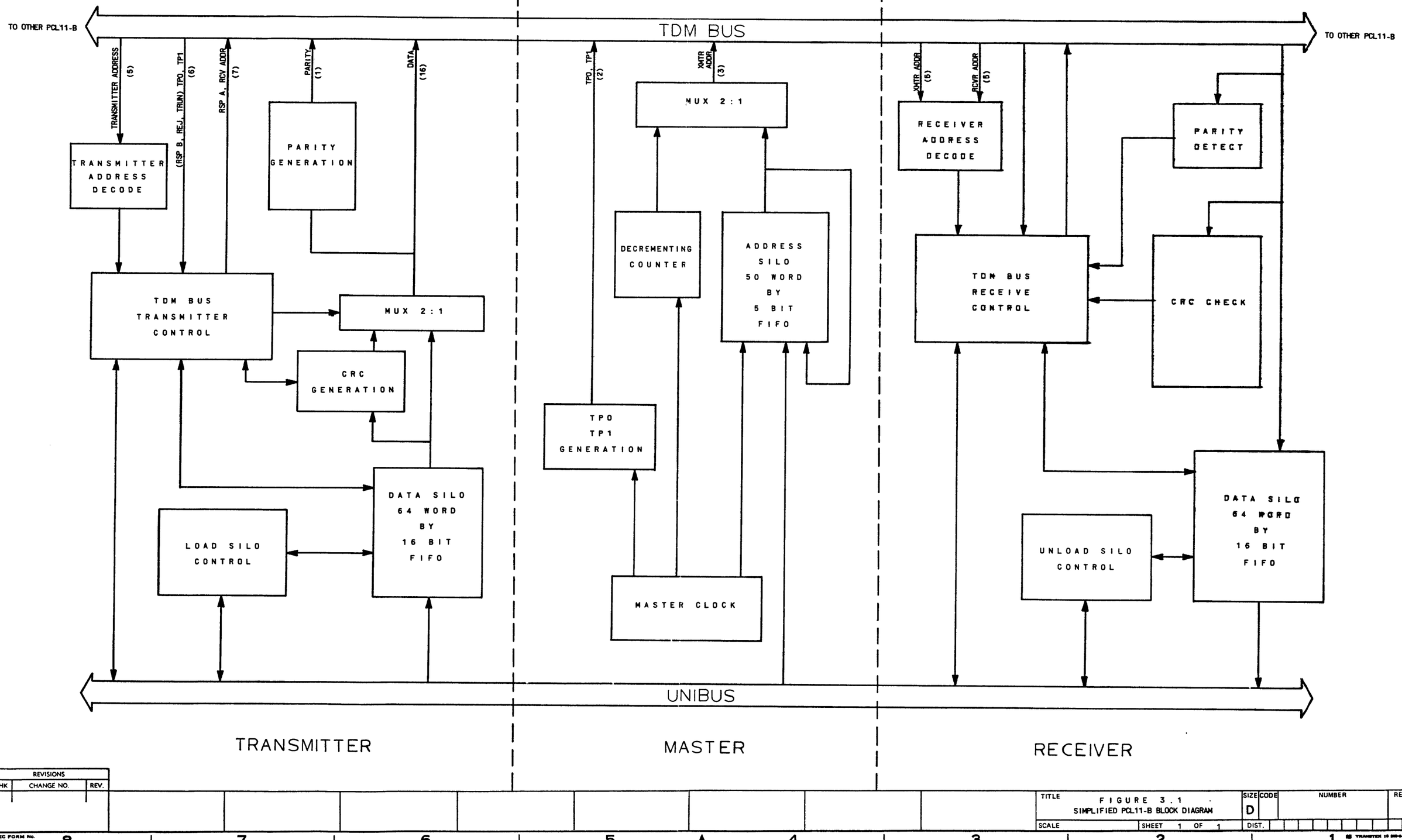
Figure 3.1 is a general block diagram for the PCL11-B interface. The transmitter, receiver and master sub-sections are independant of each other. Thus a receive section may be in process of accepting a data transfer from one PCL11-B at the same time that the transmitter is sending to a different PCL11-B and the Master section is generating the timing for all units on the TDM Bus.

3.2 TDM Bus Timing

A single PCL11-B unit on a TDM bus is designated as TDM bus master. Any PCL11-B unit may be designated as Master but only one unit may be Master at any time. This unit, once designated, remains master and generates the required timing for the bus as long as there is no failure in its Master section and this section of logic is left enabled. (This Master should not be confused with a Unibus Master which gains control of the Unibus, effects a transfer, and then gives up the bus. The TDM bus master is NOT performing any data transfers, it is merely generating the signals required by the various transmitters which are moving data.)

As well as containing logic to be a designated TDM bus Master each PCL11-B may also be set up as a backup Master, or Secondary. Only a single unit may be designated as Secondary in a system and this unit will automatically become Master in the event that the first Master is disabled or powered down.

The TDM bus Master contains logic which assigns periods of time called "timeslices" to each transmitter on the bus. This is accomplished by the generation of two square waves called Time Phase 0 and Time Phase 1 (TP0 and TP1). Each unit on the bus uses these signals



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
FIGURE 3.1 SIMPLIFIED PCL11-B BLOCK DIAGRAM	D			
SCALE	SHEET 1 OF 1	DIST.		

DEC FORM No. DRD 126

to determine the beginning of each timeslice as well as the beginning of one of four phases within the timeslice. Action required to accomplish data transfer takes place at the beginning of these phases. In conjunction with these two signals, the Master also generates five transmitter address lines. These lines are decoded by the transmitter section of the PCL11-B units who look for their own unique timeslice by comparing their TDM Bus address with the transmitter address lines produced by the Master. Once the transmitter has determined that it has been assigned a timeslice it may then send one word during that timeslice to the receiver with which it is in communication.

3.3 Data Transfer

All data transfers are initiated by the transmitter section. The transmit logic will remain inactive and not use any timeslices until the software supporting the hardware performs three tasks. First, the software must get data to the transmitter by either initiating a block NPR transfer or moving data to the transmitter silo buffer location. Second, the software must indicate the address of the receiver to which the data is being sent by loading Destination Code bits in the logic. Third, the software must set the appropiate GO bits. Once this is done the transmitter will wait until its next timeslice, then try to send one word to the designated receiver. After this word has been successfully sent to the receiver, the transmitter then considers that there is a "channel open" with that receiver. Depending on the commands given it by the software, the transmitter may send one word at a time to the receiver and then interrupt its processor, or else it may send a whole message and only interrupt after the entire message has been received and CRC check performed on the data.

The receiver must be enabled by the software before any data is accepted. Once enabled the receiver logic will accept a word from the first transmitter that sends data to it. After accepting the first word, the receiver considers that it has a channel open with the transmitter that has sent it the first word and will not accept any data from any other transmitter unit until the message is complete and the receiver is enabled again. The receiver may either accept data one word at a time, and then interrupt its processor, or else it may accept a whole message and only interrupt after the entire message is received and the CRC has been checked. If the receiver is set up to only receive one word at a time then after the first word has arrived the software has the option of accepting more of the message or rejecting the message completely and closing the channel immediately.

Messages are transferred by sending one 16 bit word at a time between units that have a channel open. The channel will remain open until the message has been successfully sent or a error has occured. If for any reason during a particular timeslice a receiver cannot accept a word (for example the receiver silo is full) or the transmitter cannot send a word (for example a word is not ready on the output of the silo) a null cycle will take place. This is not a error condition, another attempt will be made to send the same data on the next timeslice. An error will only occur if approximately two seconds pass without any data being passed from transmitter to receiver.

After the channel is opened, if either the transmiter or receiver detects an error, then this unit sends an indication of this error to the other PCL11-B and then closes the channel. Following this, both units will interrupt their respective proccessors to indicate the message was not successfully transferred. A message transfer is not considered complete by either the transmitter or the receiver until all the data has been moved out onto the receiver's Unibus and all parity and CRC checks have been successful. Only after this will both units interrupt their respective processors and indicate a successful completion of the operation.

3.4 General Description of a PCL11-B Unit

Figure 3.1 shows a block diagram for a PCL11-B unit. This unit is a Unibus peripheral and as such both receiver and transmitter receive data and control signals from this bus. They provide independant interfaces to the TDM Bus.

The heart of the transmitter is the Data Silo which is a 64 word by 16 bit FIFO or Silo. Data to be transferred to a receiver is loaded into the Silo by the Load Silo Control. This is accomplished in one of two ways. The Load Silo Control may be responding as a Unibus slave to the computer moving data directly to the silo, which appears as a register on the Unibus. (This may be accomplished in software by performing a MOV to the Silo location). As well, the Load Control may iniate a transfer of a block of data directly from memory to the silo without processor intervention. This DMA is performed by making a NPR request for the Unibus every time there is room in the silo for the next word of the block.

The TDM Bus Control logic controls the transfer of the data from the output of the silo to the receiver over the TDM Bus. This section will wait until enabled by the software, and there is a word on the output of the silo. The Transmitter Address Decode logic determines when it is the transmitter's timeslice. The TDM Bus Control Logic will determine from the time phase signals (TP1, TP0) the correct time to drive the TDM bus with the signals required for the transfer. This section asserts the address of the receiver being talked to, as well as two lines called the response lines, (RSP A 1, RSP A 0). These two lines indicate to the receiver what will occur during the timeslice. As well, the control section will multiplex the data lines with the output of the silo or the CRC character, whichever is appropriate.

The CRC Generation logic will calculate a CRC-16 character for the data being sent. Included in this logic is a counter which counts the number of words transferred. After 200 (octal) words have been sent the CRC character will be sent during the next timeslice.

The Parity Generation circuit calculates a Parity bit to accompany every 16 bit word transferred, including the CRC character.

The receiver section logic performs the reverse to that of the transmitter. The data Silo (another 64 word by 16 bit FIFO) is loaded with the data received from a transmitter over the TDM Bus. Data is removed from the silo by the Unload Silo Control by either NPR requests whenever the data is ready, or move instructions received from the

computer.

The TDM Bus Control logic controls the reception of the message and the loading of the data into the silo. The Receiver Address Decode determines when the receiver is being addressed and, if a channel is open with a particular transmitter, qualifies this with the address of the unit doing the addressing. The control logic uses the time phase signals to determine exactly when to remove the data off of the bus and load into the Silo. This section will assert four lines on the bus during the timeslice to indicate to the transmitter what was done by the receiver during the timeslice.

The CRC and Parity logic check the data as it arrives at the receiver. If an error is detected, the Control logic will indicate this to the transmitter using one of the four response lines.

The Master section produces two types of signals to control transfers on the TDM bus. The first type are the time phase signals, (TP0,TP1), which are simply two square waves, 90 degrees out of phase. The second type are transmitter address signals which may be generated in one of two ways. The simpliest is a Decrementing Counter which puts out all the addresses on the TDM bus out in order from highest to lowest, in descending order. The second method is an Address Silo which can be loaded by software. Once enabled, this silo will circulate the addresses, allowing one transmitter to be assigned more of the bus bandwidth. The Master Clock produces the timing to run all sections of the master. This must be adjusted to the correct timing for the particular bus length.

3.5 Timeslice Allotment and Bandwidth

The chart in section 1.6 shows the specification for the bandwidth of the TDM Bus. This figure, which depends on the length of the bus, is an indication of the maximum rate at which data could be moving between all units on the bus. Obviously, with a number of different units transfering data simultaneously, each transmitting unit could only be moving data at a rate which is some percentage of the bandwidth. For example if a network consisted of 4 PCL11-B units on a fifty foot bus, each transmitting unit could be transferring data at the same time at a maximum rate of 1/4 (1/no. of units) of the bus bandwidth (ie 1/4 of 1000 kbytes/sec or 250 kbytes/sec). It should be noted this is not a throughput specification, as there are other limitations on the system such as speed at which the data can be moved between the silo and the Unibus, software overhead, receiver busy with other units, etc.

Each Master section will default to assigning equal timeslices to each transmitter. However, as indicted in section 3.4 there is an alternative method of assigning timeslice using the Address Silo. This silo may be loaded with a sequence, for example with a four PCL11-B network:

1 2 1 3 1 4 1 2 1 3 1 2 1 3 1 4 1 2 1 3

(A minimum of 20 addresses must be loaded into the silo)

(A maximum of 50 addresses may be loaded into the silo)

This would result in transmitter 1 having 10 of every 20 timeslices, transmitter 2 and 3 would get 4 of 20 and transmitter 4 would get only 2 of 20. Translating this into bandwidth would mean that transmitter 1 would have a message bandwidth of 500 kbytes/sec, transmitters 2 and 3 would have a message bandwidth of 200 kbytes/sec and transmitter 4 would have 100 kbytes/sec.

It should be noted that no transmitter may be assigned succesive timeslices so that the most bandwidth any one transmitter or receiver unit may have is 500 kbytes/sec.

3.6 Driver Functions

The following functions are included in the RSX11-M driver to enable user software to control a PCL11 system.

Attempt Transfer

A transmission is initiated to the indicated destination processor. The receiving task in the destination processor is presented with the source PCL11 TDM Bus address as well as a "flagsword" which must be supplied by the transmitting task. The receiving task may use this information to decide whether to accept or reject the rest of the transmission. For the flagsword to be successfully transmitted the receiver task must have already performed a Connect for Reception.

Connect for Reception

This declares the issuing task to be the sole receiver of PCL11 transfers within a computer. This will set up the PCL11 receiving hardware to accept a message from the first PCL11 transmitter that communicates with it. When a "flagsword" (or first word of a message) is received from a transmitting PCL11, a user specified event flag is set to indicate that a transfer is pending and the user must take some action to complete the transmission. At this time the user may either accept or reject the transfer based on the flagsword and PCL11 identification which is passed to the user.

Reject Transfer

This function will cause the receiving PCL11 hardware to reject (ie not accept) the rest of the transfer from the transmitter PCL11 hardware.

Accept Transfer

This function will cause the receiving hardware of the PCL11 to accept the rest of the message from a transmitter. It will also allocate a buffer into which the received data will be stored. This function can be issued before a flagsword is received from a transmitter in which case the flagsword would be discarded and the message accepted without an event flag being set to inform the user task.

Disconnect from Reception

This function is is to disconnect the issuing task from reception.

Set Master Section Characteristics

This function will allow the user task to use the Master section of logic in the PCL11. This logic generates the timing for the Time Division Multiplexed Bus. Only one PCL11 unit may become TDM Bus master. The characteristics which may be set up include:

State: Put unit as Master, Secondary or neutral.
Mode: Auto TDM Bus addressing or Silo addressing.

The silo addressing mode allows the user to supply a list of PCL11 addresses to be loaded into the address silo.

SECTION 4

CONFIGURATION AND ORDERING OF SYSTEMS

4.1 Configuring Networks

The following procedure should be followed for each TDM Bus when configuring a PCL11-B system.

1. Determine the number of PDP-11 computers to be connected together. This number must be 16 or less.

2. Obtain a configuration chart for all systems in the network to determine where the PCL11-B units are to be mounted. As a general rule the PCL11-B units should be the last DMA device on the Unibus as the data Silos or FIFO's help ensure that the device will not have any data late problems. Full site considerations for the PCL11-B are included in the Option Description (YC-A20TC-00)

3. Review the PCL11 Communication System specifications to ensure that the system meets all the requirments set out therein.

4. Determine the cable distance required between each mounting box in the system in which PCL11-B units are mounted. As a guide, estimate the distance a cable would have to travel to be routed between the two cabinets. Add sufficient length to allow for the height of the mounting box plus about four feet to allow for sliding of the box in and out of the cabinet.

5. Use the configuration charts as outlined in figures 4.1 and 4.2, these charts may be found in appendix B. Beginning at one end of the bus, (at the terminator) assign a unique TDM Bus address (from 1 to 37 octal) to the first PCL11-B unit. Write this address into the box next to TDM Address. Determine the length of cable which would be requiried to connect to the next unit on the bus. (If these units are in the same mounting box no interconnect cable is required. In this case join the lines on the chart but do not write anything above them.) Connect the lines between the first two units on the chart and write the length of cable (if required) above the line. This cable length should be the length of TDM bus required, rounded up to an avaiable length of 5, 10, 15, 25, 50 or 100 feet. Assign a unique TDM Bus address to the second unit and proceed as in the first unit. Continue this process until all units in the system are included. Indicate on the chart the terminator postions.

6. Determine the total bus length. Add up the lengths in the configuration chart. Add this total to ten times the number of PCL11-B units in the system. The result will be the total bus length in the system - which MUST be less than 300'.

   In the example of a five CPU system in fig 4.2 the total bus length would be:

```
                 10'
                 25'
                 10'
                 10'
                ------
                 55'
                ------
5 units ` 10'    50'
                ------
                 105'   total bus length
```

   If the total bus length is greater than 300' than an attempt should be made to move the various computers and mounting boxes closer together. When configuring a system, care must be taken to ensure that there is enough slack cable behind all mounting boxes to allow them to be pulled open without disconnecting the TDM Bus. If problems persist in configuration then a CSS Application Engineer should be consulted.

7. Order the following eqipment:

   1 PCL11-B for every box used in the chart. All terminators, other cables, power harnesses, and diagnostics are included in the PCL11-B

   1 BC20P-xx for every length of cable of length xx required. The value of xx must be 5, 10, 15, 25, 50 or 100.

   Any spare PCL11-B or cables that may be required if on site spares are desired.

   Any operating system software desired must be ordered separately.

   For the example shown in figure 4.2 the following equipment would be ordered:

   5 PCL11-B

   3 BC20P-10

   1 BC20P-25

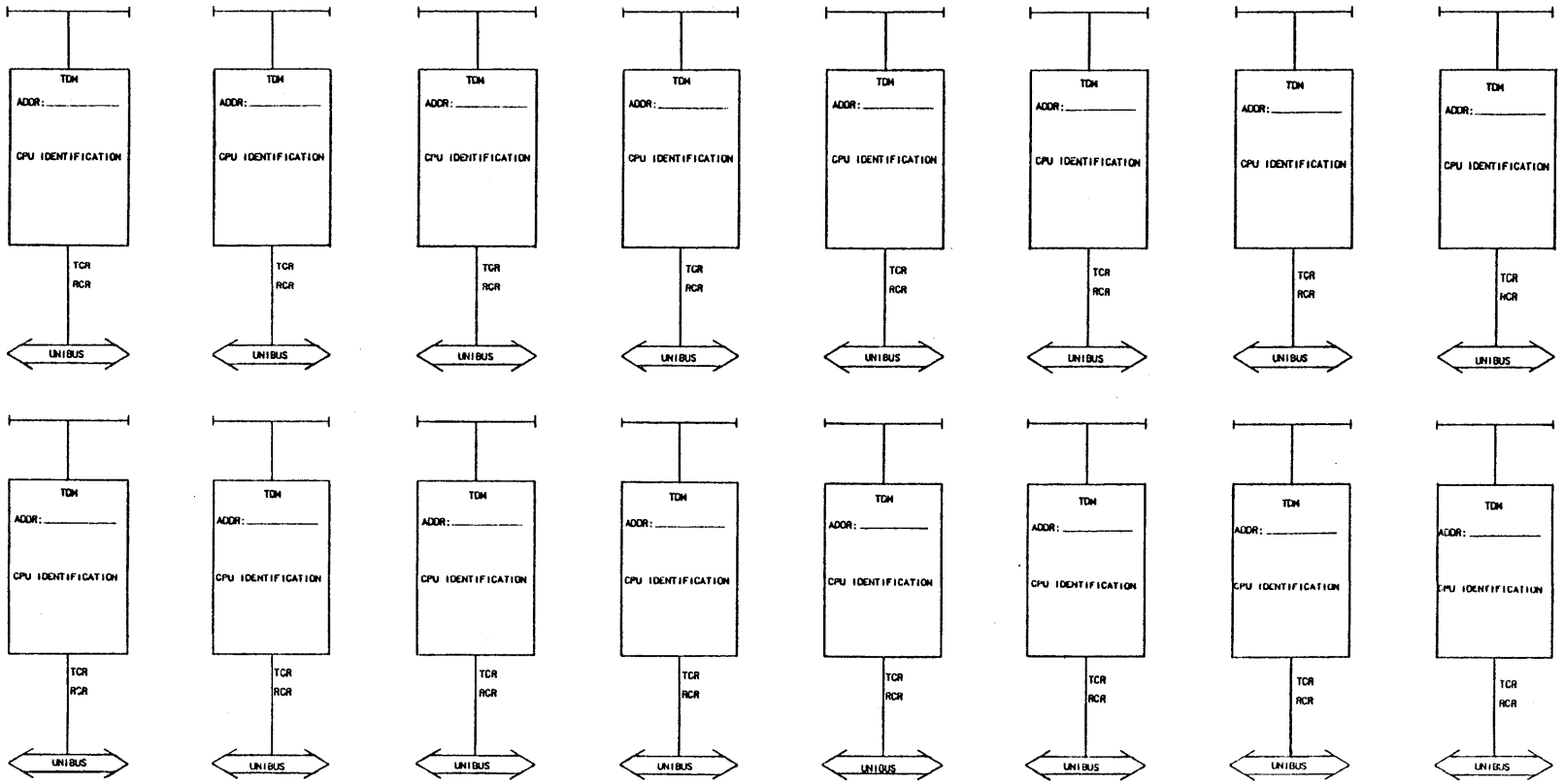


FIGURE 4.1

BLANK CONFIGURATION CHART

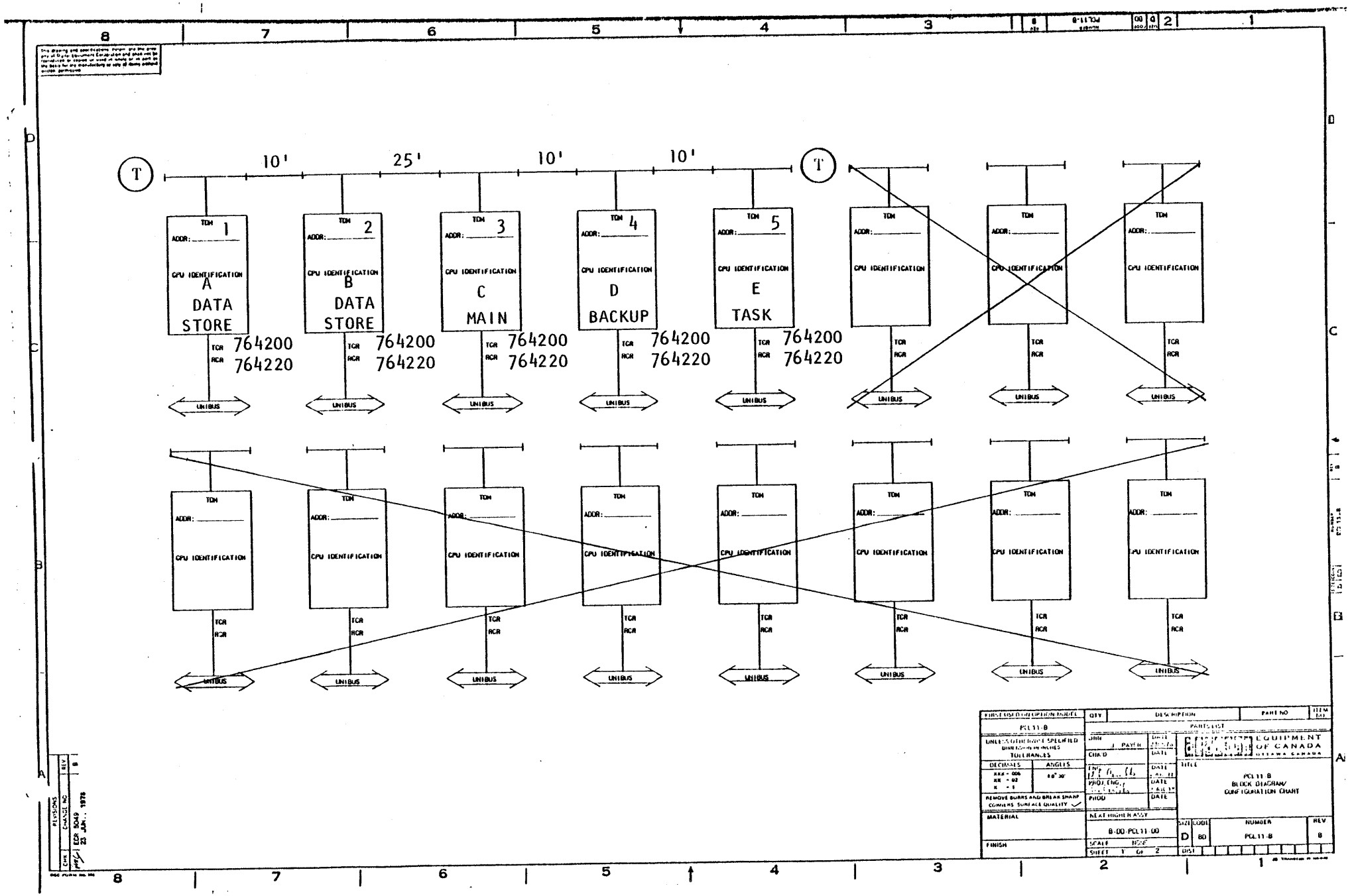
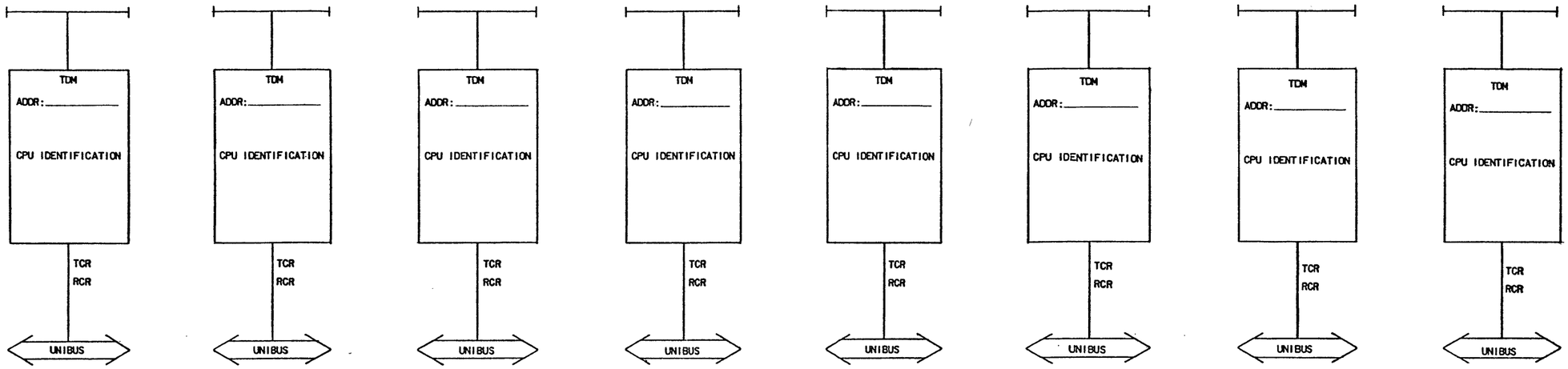


FIGURE 4.2

EXAMPLE OF A COMPLETED CHART

Appendix A List of Documentation

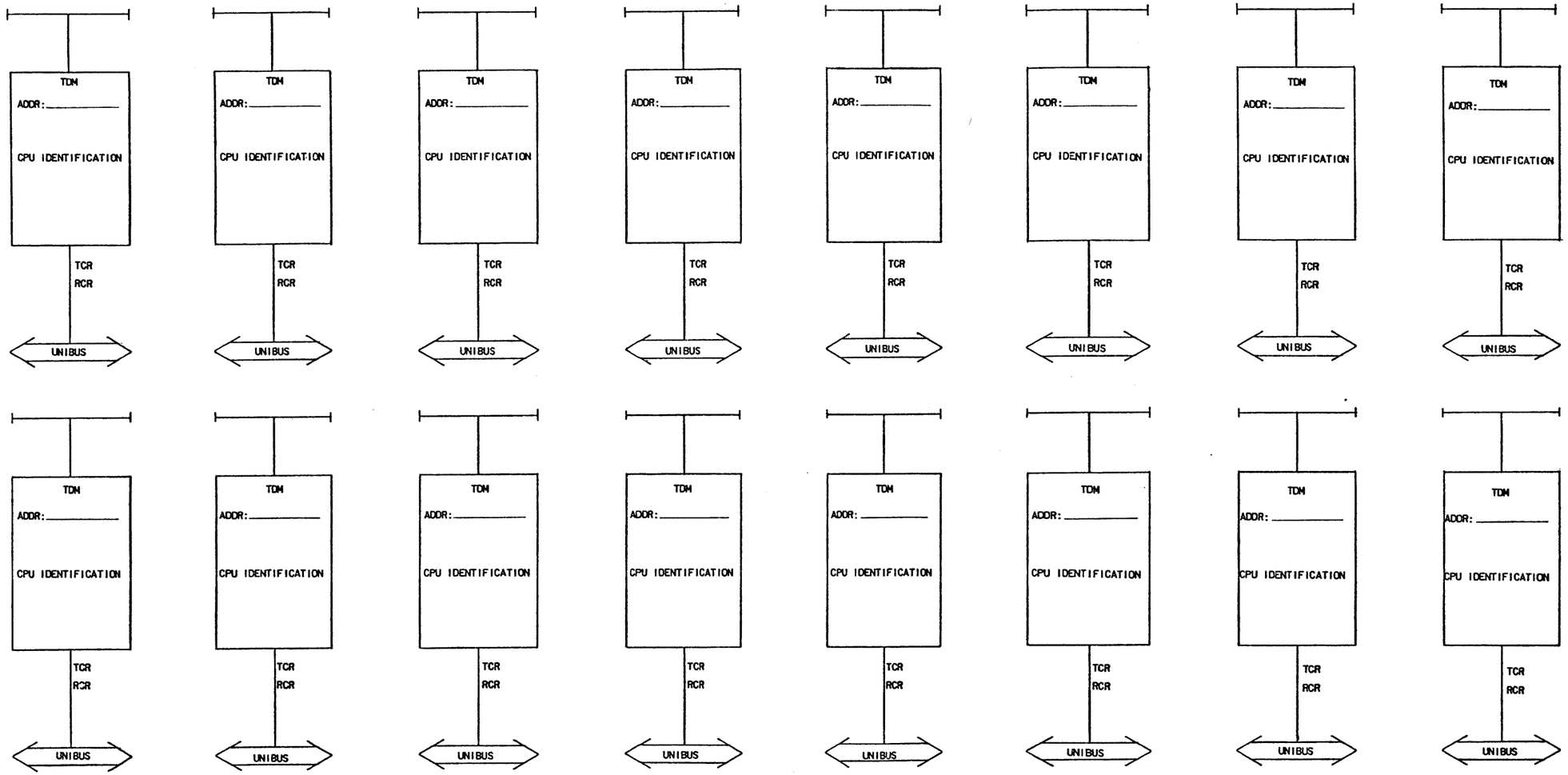
PCL11-B Option Description	YC-A20TC-00
PCL11 Communications Systems General Introduction and Configuration Guide	YC-A20TC-01
PCL11 Communications Systems Installation and Maintenance Guide	YC-A20TC-02
PCL11 Standalone Test (CZPLBA0)	Listing AC-E262A-MC Paper Tape AK-E264A-MC
PCL11 Exersiser (CZPLAA0)	Listing AC-E259A-MC Paper Tape AK-E261A-MC
PCL11 Customer Print Set	B-DD-PCL11-00
RSX11-M PCL User Guide	YC-T012C-U0
RSX11-M PCL Driver Documentation Support Manual	YC-T012C-SO



REVISIONS		
CHK	CHANGE NO.	REV.
MRC	ECR 5049 23 JAN., 1978	B

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PCL11-B		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	DRN. J. PAYER	DATE 230678	DIGITAL EQUIPMENT OF CANADA OTTAWA CANADA
DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'	CHK'D.	DATE	TITLE: PCL11-B BLOCK DIAGRAM/ CONFIGURATION CHART
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	ENG. D.J. Smith	DATE 2-AUG-78	
MATERIAL	PROJ. ENG. D.J. Smith	DATE 2-AUG-78	
FINISH	PROD.	DATE	
	NEXT HIGHER ASSY. B-DD-PCL11-00	SIZE D / CODE BD / NUMBER PCL11-B / REV. B	
	SCALE NONE	DIST.	
	SHEET 1 OF 2		



REVISIONS		
REV.	CHANGE NO.	CHK
B	ECR 5049 23 JUN., 1978	

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PCL11-B		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

DRN.	J. PAYER	DATE 230678
CHK'D.		DATE
ENG.		DATE
PROJ. ENG.		DATE
PROD.		DATE
NEXT HIGHER ASSY.	B-DD-PCL11-00	
SCALE	NONE	
SHEET	1 OF 2	

DIGITAL EQUIPMENT OF CANADA OTTAWA CANADA

TITLE

PCL11-B
BLOCK DIAGRAM/
CONFIGURATION CHART

SIZE	CODE	NUMBER	REV.
D	BD	PCL11-B	B

DIST.

DEC FORM No. 102

SIZE D | CODE BD | NUMBER PCL11-B | REV. B