NOTEBOOK SECTION

OPTION NUMBER

PCL11 - B

DRAWING SET NUMBER

B - DD -PCL11 -B

PROGRAM NUMBER

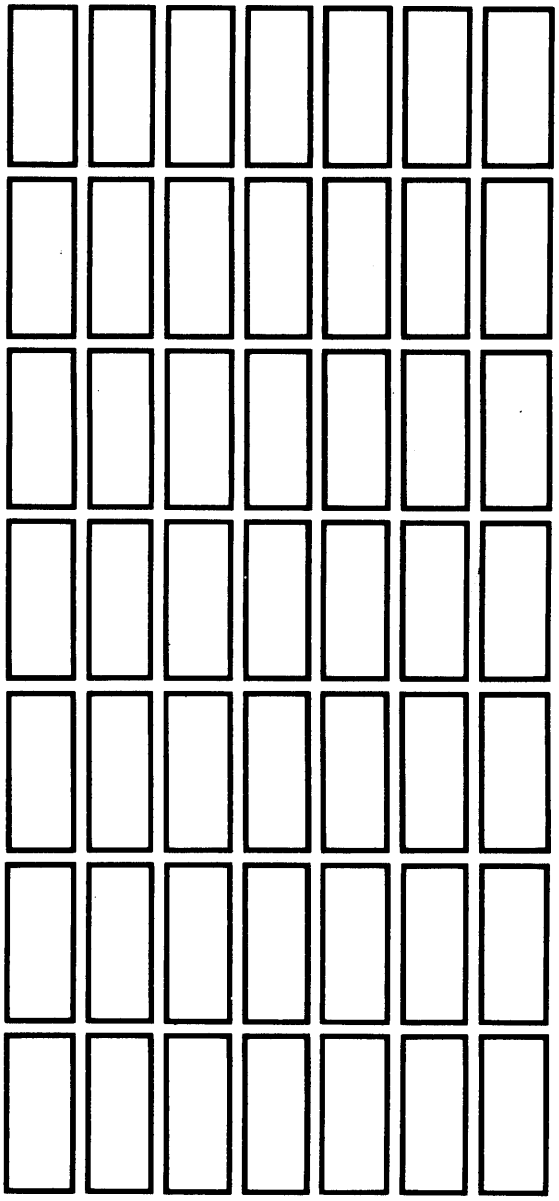
CZPLBA0

DOCUMENT NUMBER **REVISION**

YC - A20TC - 00 B

DATE

FEBRUARY 1979



PCLII-B

PARALLEL COMMUNICATION LINK

DIFFERENTIAL TDM BUS

digital

Computer Special Systems

KANATA

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SECTION 5

APPENDIX A

APPENDIX B

FIG.

TABLE

SECTION 1

1.1 GENERAL DESCRIPTION

The Parallel Communications Link (PCL11-B) is an interface which creates a Time Division Multiplexed (TDM) bus over which several PDP-11 computers can transfer data to each other. Each interface consists of a transmitter, receiver, and master section. The transmitter section may transfer parallel 16-bit words along the TDM bus to a receiver section of a separate PCL11-B housed on a different PDP-11 computer's Unibus. One of the PCL11-B units attached to the TDM bus must have its master section enabled. This logic will generate the necessary timing signals for proper data transfer.

1.2 GENERAL OPERATION

Each transmitter and receiver section has its own unique TDM bus address, selectable by switches on the PCL11-B modules. When a master section is enabled it puts out a transmitter address on the bus for a period of time (one timeslice). During this period of time the selected transmitter addresses the desired receiver section, sends one word to it, then waits for either acknowledgement of the receipt of the word, or indication that the word was not accepted. If for some reason the receiver cannot accept the word, the transmitter will try again on its next timeslice. A transmitter may send up to one word per timeslice to the selected receiver until the entire message is sent. In general, a different transmitter will have its timeslice directly following the first, thus allowing it to send a different message to a different receiver.

In this manner a number of transmitters may be sending data at the same time, although only one transmitter may be active at any given moment. Any message length up to 32K words may be sent. Each word transferred will be accompanied by a parity bit and each message includes Cyclic Redundancy Checking to ensure validity of received data.

In order to accomplish a transfer between two computers, the software in each machine must complete two basic tasks. In the transmitter, the host software is responsible for getting data to be transferred into a data silo in the interface. This may be done by either setting up an NPR transfer or else moving each word to the interface. Then the software must load up the receiver's address and set the proper command bits.

The receiver software (which may even be in the same computer) must perform similar tasks. It must remove the transferred data from the data silo in the interface - either by setting up a NPR transfer or moving each word out of the interface. As well, this software must set the proper command bits which causes the receiver to accept a transmission from the first transmitter who addresses it.

1.3 SPECIFICATIONS

a) Mechanical

Mounting:	9 slot double system unit. Must be mounted in a mounting box or interior of a PDP-11 such as PDP 11/10 N/C or PDP11/40. PCL-11B units are not suited for mounting in BA11-L mounting boxes
Modules:	PCL11-B requires 7 hex modules M7991 through M7997 and 1 Quad module M8003.

b) Electrical

Required Voltages:	+5 volts -15 volts
Current and Power Requirements:	14 amps @ +5V 70 watts .5 amps @ -15V 7.5 watts
Logic Potentials:	TTL
Differential Bus Levels:	0v,5v

Power harness suitable for BA11 style mounting boxes will be supplied unless otherwise specified.

c) Operational

i) TDM BUS

Length:	Total TDM bus length must not exceed 300'.
Units:	Any number up to 16 units may be accommodated on one TDM bus.
Bus Bandwidth:	Refer to Table 1.1.
Maximum Transfer Rate:	"

ii) TIMESLICE ALLOTMENT

Default:	Decrementing counter, continually counts down from highest TDM Bus address to 1. All units receive same portion of bus bandwidth. Switch must be set to an address greater than 1.

		BUS LENGTH			
		up to 50'	up to 100'	up to 240'	up to 300'
BUS BANDWIDTH		1000	800	500	400
MAXIMUM TRANSFER RATE	1 unit	500	400	250	200
	2 units	500	400	250	200
	8 units	125	100	62	50
	16 units	62	50	31	25

-all transfer rates and bandwidths in kilobytes per second.

TABLE 1.1

BANDWIDTH AND TRANSFER RATES

Address Silo: A cycling address silo may be used to dynamically allot bus bandwidth. This silo has the following specifications:

Max number of addresses: 50
Min number of addresses: 20

No transmitter may be assigned 2 timeslices in succession.

Timeslices remain the same length whether they are used or not.

iii) Message Length: Up to 32 K words may be sent in any one message. Each word is accompanied by a parity bit. After every 200_8 words transferred, and at the end of the message a CRC character is sent and checked.

d) Unibus

Load: PCL11-B presents one and a half unit loads to the Unibus.

Register: PCL11-B transmitter and receiver registers may be given separate addresses. PCL11-B transmitter requires 8 consecutive register address (20_8 bytes). PCL11-B receiver requires 8 consecutive register addresses (20_8 bytes).

Interrupt: Receiver and transmitter interrupt on BR5. Each has its own vector.

NPR: Both Receiver and Transmitter section are NPR devices.

1.4 PHYSICAL DESCRIPTION

PCL11-B consists of a backplane (a double system unit), and seven hex modules: M7991 through M7997 and one quad module M8003. The backplane must be mounted in a suitable mounting box and supplied with the correct power. Unibus connections must be made with the proper cables or M920 modules. The PCL11-B is shipped with one M920. Also included is one terminator for the TDM BUS (H3370) as well as a short section of TDM BUS Cable to connect the PCL11-B to the TDM BUS (BC20K).

TRANSMITTER | MASTER | RECEIVER

UNIBUS

ADDRESS

NPR, MSYN, SACK

BRS, INTER, BBSY

UNIBUS DATA DRIVERS/MUX M7993

UNIBUS RECEIVERS M7994

UNIBUS DATA DRIVERS/MUX M7995

ADDRESS

ADDRESS C B TS

INTERRUPT CONTROL M7992

UNIBUS ADDRESS DECODE M7994, M7992

TMMR (HIGH BYTE) M7994

CLOCK M7994

TIME PHASE GENERATOR M7994

UNIBUS ADDRESS DECODE M7994, M7996

INTERRUPT CONTROL M7996

RCR 164220 M7995 M7996 M7997

RSR 164222 M7995 M7996 M7997

RDBC 164226 M7995

RDBA 164230 M7995

TSR 164202 M7991, M7992

TCR 164200 M7991, M7992, M7993

50 WORD BY 5 BIT ADDRESS SILO TMMR LOW BYTE M7994

5 BIT DECREMENTING COUNTER M7994

TSBA 164210 M7993

TSBC 164206 M7993

64 WORD BY 16 BIT SILO M7993

TDM BUS TRANSMIT CONTROL M7991

TDM BUS ADDRESS TRANSMITTER MUX M7994

TDM BUS RECEIVE CONTROL M7997

64 WORD BY 16 BIT DATA SILO M7995

DATA SILO TO UNIBUS CONTROL M7996

TPO TP1

RCV ADR DEC M7997

LOAD DATA SILO CONTROL M7992

CRC AND PARITY GENERATOR M7991, M7992, M7993

TXM ADDRESS DECODE M7991

TXM ADR

TDM BUS TTL TRANSCEIVERS (MASTER SIGNALS) M7994

TDM BUS TTL TRANSCEIVERS RCV ADR RSP A PARITY M7994

TDM BUS TTL TX RSP B REJ, TRUN M7994

CRC AND PARITY CHECKER M7996, M7997

TDM BUS TTL TRANSCEIVERS (DATA LINES) M7991

TDM BUS DIFFERENTIAL TRANSCEIVERS M8003

TDM BUS DIFFERENTIAL TRANSCEIVERS (MASTER SIGNALS) M8003

TDM BUS DIFFERENTIAL TRANSCEIVERS M8003

TDM BUS DIFFERENTIAL TRANSCEIVERS M8003

TDM BUS

REVISIONS

REV.	CHANGE NO.	CHK
B	ECR 5049 23 JAN., 1978	RC

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PCL11-B		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

DRN.	J. PAYER	DATE 230678
CHK'D.		DATE
ENG.	[illegible]	DATE 8-AUG-78
PROJ. ENG.	[illegible]	DATE 2-AUG-78
PROD.		DATE

NEXT HIGHER ASSY.

SCALE NONE

SHEET 2 OF 2

EQUIPMENT OF CANADA OTTAWA CANADA

TITLE

PCL11-B
BLOCK DIAGRAM/
CONFIGURATION CHART

SIZE	CODE	NUMBER	REV.
D	BD	PCL11-B	B

DIST.

DEC FORM No. 102

REV.	SIZE	CODE	NUMBER
B	D	BD	PCL11-B

SECTION 2

2.1 SITE CONSIDERATIONS

The PCL11-B Backplane Assembly may be mounted inside a mounting box, or the interior of a PDP-11 computer, if there is room. The Backplane Assembly requires a double system unit space in the mounting box. The backplane assembly should not be mounted in a BA11-L mounting box.

Since PCL11-B does not include its own power supply, care should be taken to insure that the existing supply can provide the required amperage. PCL11-B draws 14 amps out of the +5V supply and .5 amp out of the -15 supply. PCL11 has two plugs for power which must be plugged into the same regulator.

The entire PCL11-B system is one and a half unit loads on the Unibus. The entire number of unit loads on any Unibus may not exceed twenty, without use of a bus repeater.

When configuring PCL11-B units on a Unibus, these units may be placed towards the rear of the B Unibus. This is due to the fact that all data transfers are silo buffered to avoid "data late" problems. However, it is not recommended to configure PCL11-B behind a bus repeater.

2.1.1 Installation Procedure

The following procedure should be followed for each PCL11-B unit in a system. Before installing a unit in a system, a configuration chart must be filled out as outlined in section 2.1 of 'PCL11 Communication Systems - Installation and Maintenance Guide' (YC-A20TC-02).

1. Mount the PCL11-B Backplane Assembly in the Mounting box or PDP-11 computer using the four mounting screws provided.

2. Plug the power cable onto the appropriate clips on the Backplane Assembly and to a free output of a power supply. The power supply must be able to provide the required amperage. Both plugs must be plugged into the same regulator.

3. Using the M920 provided, a BC11A Unibus cable, and/or a terminator connect the Unibus to the Backplane Assembly. The Unibus enters and leaves via the slots indicated in Figure 2.1.

SIZE	CODE	NUMBER	REV
D	MU	PCL11-B	B

CONNECTOR LEVEL 'F'	CONNECTOR LEVEL 'E'	CONNECTOR LEVEL 'D'	CONNECTOR LEVEL 'C'	CONNECTOR LEVEL 'B'	CONNECTOR LEVEL 'A'	
SLOT 01	M8003-00			UNIBUS IN		
SLOT 02	M7991 TXM INTERFACE MODULE					
SLOT 03	M7992 TXM UNIBUS CONTROL AND CRC MODULE					
SLOT 04	M7993 TXM REGISTERS MODULE					
SLOT 05	M7994 MASTER SECTION MODULE					
SLOT 06	M7995 RCV REGISTERS MODULE					
SLOT 07	M7996 RCV UNIBUS CONTROL MODULE					
SLOT 08	M7997 RCV INTERFACE MODULE					
SLOT 09	M8003-00 OPTIONAL LOCATION			UNIBUS OUT		

VIEWED FROM PIN SIDE

NOTES:

REVISIONS			
CHK	CHANGE NO	REV	
	PROTOTYPE 1 23 AUG 76	P1	
	FIRST RELEASE 15 OCT. 76	A	
	ECR 5049 23 JAN., 1978	B	

FIRST USED ON OPTION MODEL: PCL11-A	QTY.	DESCRIPTION	PART NO. / ITEM NO.
	PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	DRN. B. DAVY	DATE 23/8/76	DIGITAL EQUIPMENT CORPORATION OF CANADA OTTAWA CANADA
DECIMALS: .XXX ± .005, .XX ± .02, X ± 1 — ANGLES: ±0° 30'	CHK'D.	DATE	
	ENGR.	DATE	TITLE: PARALLEL COMMUNICATION LINK (PCL11-B)
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓	PROJ. ENG.	DATE	
	PROD.	DATE	
MATERIAL: NONE	NEXT HIGHER ASSY.		
	B-DD-PCL11-00		SIZE D / CODE MU / NUMBER PCL11-B / REV. B
FINISH: NONE	SCALE N.T.S.		
	SHEET 1 OF 1		DIST

DEC FORM NO 102

4. a) On the M7991 module, set up the DIP switch (S1) to contain the transmitter's five bit TDM bus address (in octal). Switch 1 is the most significant bit, switch 5 the least; turn the switch OFF for a 1. Plug the M7991 in slot 2 (see figure 2.1). This transmitter address must be unique and should be determined from the system configuration chart.

b) Plug M7992 into slot 3 (see figure 2.1).

c) Plug M7993 into slot 4 (see figure 2.1) after insuring the transmitter's interrupt vector jumpers are correct. Table 2.1 indicates which jumpers should be inserted for a given vector.

d) Set up the DIP switch (S1) on the M7994 to contain the highest transmitter address existing on the TDM bus (in octal). (Switch 1 is the most significant bit, switch 5 is the least. Turn OFF for a 1.) Two transmitters may not have successive timeslices, therefore the address set up in this switch must be greater than one. Referring to Table 2.2, insure the transmitter and receiver address jumpers are inserted properly. Plug the M7994 into slot 5 (see Figure 2.1). The highest TDM bus address may be determined from the configuration chart.

e) Referring to Table 2.3, ensure that the receiver's interrupt vector jumpers are correctly installed on the M7995. Then plug this module into slot 6 (see Figure 2.1).

f) Jumper W1 is installed when the M7996 modules are shipped. When inserted, this jumper allows some NPR's to be honoured before BR's, despite the fact the BR's were asserted first. When W1 is cut, the circuitry for this is disabled. This jumper must be cut if this PCL11-B is being used with an early PDP11/20 or PDP11/15 without KH-11 option. After ensuring W1 is correctly installed, plug the M7996 into slot 7 (see Figure 2.1).

g) On the M7997 module, set up the DIP switch (S1) to contain the receiver's 5 bit TDM bus address (in octal). (Switch 1 is the most significant bit, switch 5 the least. Turn OFF for a 1). Plug the M7997 into slot 8 (see figure 2.1). Refer to the system configuration chart to determine the unique Receiver TDM bus address.

h) One BC20K cable kit is included with every PCL11-B unit. It consists of two cables, one with an orange dot on the label, one with a blue dot. Write the TDM bus address of the unit on each label of both cables.

VECTOR/JUMPER INSERTION TABLE			
VECTOR	JUMPER	INSERTED/NOT USED	NOTE
V8=0	W1	INSERTED	2
V8=1	W1	NOT USED	NIL
V7=0	W2	INSERTED	2
V7=1	W2	NOT USED	NIL
V6=0	W4	INSERTED	NIL
V6=1	W4	NOT USED	NIL
V5=0	W5	INSERTED	NIL
V5=1	W5	NOT USED	NIL
V4=0	W7	INSERTED	NIL
V4=1	W7	NOT USED	NIL
V3=0	W3	INSERTED	NIL
V3=1	W3	NOT USED	NIL
V2=0	W5	INSERTED	2
Y2=1	W5	NOT USED	NIL

TABLE 2.1
Jumpers for
Transmitter Vector

XMT UNIBUS ADDRESS JUMPER TABLE			
ADDR.	JUMPER	INSERTED/NOT USED	NOTE
A12=0	W1	INSERTED	7
A12=1	W19	INSERTED	NIL
A11=0	W2	INSERTED	NIL
A11=1	W20	INSERTED	7
A10=0	W3	INSERTED	7
A10=1	W21	INSERTED	NIL
A09=0	W4	INSERTED	7
A09=1	W22	INSERTED	NIL
A08=0	W5	INSERTED	7
A08=1	W23	INSERTED	NIL
A07=0	W6	INSERTED	NIL
A07=1	W24	INSERTED	7
A06=0	W7	INSERTED	7
A06=1	W25	INSERTED	NIL
A05=0	W8	INSERTED	7
A05=1	W26	INSERTED	NIL
A04=0	W9	INSERTED	7
A04=1	W27	INSERTED	NIL

TABLE 2.2
Jumpers for
Transmitter
&
Receiver
Unibus Add.

RCV UNIBUS ADDRESS JUMPER TABLE			
ADDR.	JUMPER	INSERTED/NOT USED	NOTE
A12=0	W10	INSERTED	8
A12=1	W28	INSERTED	NIL
A11=0	W11	INSERTED	NIL
A11=1	W29	INSERTED	8
A10=0	W12	INSERTED	8
A10=1	W30	INSERTED	NIL
A09=0	W13	INSERTED	8
A09=1	W31	INSERTED	NIL
A08=0	W14	INSERTED	8
A08=1	W32	INSERTED	NIL
A07=0	W15	INSERTED	NIL
A07=1	W33	INSERTED	8
A06=0	W16	INSERTED	8
A06=1	W34	INSERTED	NIL
A05=0	W17	INSERTED	8
A05=1	W35	INSERTED	NIL
A04=0	W18	INSERTED	NIL
A04=1	W36	INSERTED	8

VECTOR/JUMPER INSERTION TABLE			
VECTOR	JUMPER	INSERTED/NOT USED	NOTE
V8=0	W1	INSERTED	3
V8=1	W1	NOT USED	NIL
V7=0	W2	INSERTED	3
V7=1	W2	NOT USED	NIL
V6=0	W3	INSERTED	NIL
V5=1	W3	NOT USED	NIL
V5=0	W4	INSERTED	NIL
V5=1	W4	NOT USED	NIL
V4=0	W5	INSERTED	NIL
V4=1	W5	NOT USED	NIL
V3=0	W6	INSERTED	NIL
V3=1	W6	NOT USED	NIL
V2=0	W7	INSERTED	NIL
V2=1	W7	NOT USED	NIL

TABLE 2.3
Jumpers for
Receiver Vector

Note 2: Default Vector= 170, insert only W1,W2,W3.
Note 3: Default Vector= 174, insert only W1,W2.
Note 7: Default Address TCR:164200,insert W1,W20,W3-5,W24,W7-9.
Note 8: Default Address RCR:164220,insert W10,W29,W12-14,W33, W16,W17,W36.

i) Plug the middle connector of the Blue data cable into J2 of the M8003 module. Plug the middle connector of the Orange control cable into J3 of the M8003.

j) Ensure the switch on the M8003 is in the off position away from the connectors. Plug the M8003, with cables, into slot 1.

2.2 INTERCONNECTIONS REQUIRED

PCL11-B must be connected to the Unibus of the computer to which the unit is attached. The Unibus enters PCL11-B Backplane Assembly in slot AB01. The unit is shipped with a M920 jumper module which is used to connect the PCL11-B to its host computer's Unibus. If this is the last peripheral on the bus a terminator should be inserted in slots AB09.

2.3 FIELD CHECKOUT PROCEDURE

In order to ensure that the PCL11-B is operating properly the following steps must be followed once the unit has been installed as per section 2.1.1.

1. Ensure the switch on M8003 is in OFF position. (i.e. pointed down, away from the cable connectors.)

2. Turn on power, check the power supply voltages. Measure the voltage on D04L1. This must be between -12.6 volts and -11.4 volts.

3. Put an oscilloscope probe on F05T2. Run the PCL11 Standalone diagnostic (CAPLBA0) (starting address 200). Detailed description of how to run the diagnostic is included in the listing. Once all the parameters have been entered the diagnostic will ask which test should be run (1, 2, 3, 4). A 1 should be entered to run the transmitter logic test. This test should be run with all switches on the console switch register off. If there is no hardware switch register, the diagnostic will print out the contents of the software switch register. This should be modified to be all zero by typing a 0, carriage return, then a control P. After a while the diagnostic will print out a message indicating it is in a "scope loop".

4. Observe the square wave on the oscilloscope on F05T2. (This is a time phase signal, TP0.) Adjust the period of this square wave so that its period is correct for the particular TDM bus length of the system to which this unit will be connected. This may be found from Table 2.4. This adjustment is accomplished using the potentiometer situated at the rear of the M7994 module.

Bus Length	50' or less	50'-100'	100'-240'	240'-300'
Set TP0 to have a period of	2 µsec	2.5 µsec	4 µsec	5 µsec

- Use Oscilloscope to adjust the period of TP0 which may be observed on F05T2
- Adjust the period using the potentiometer on M7994

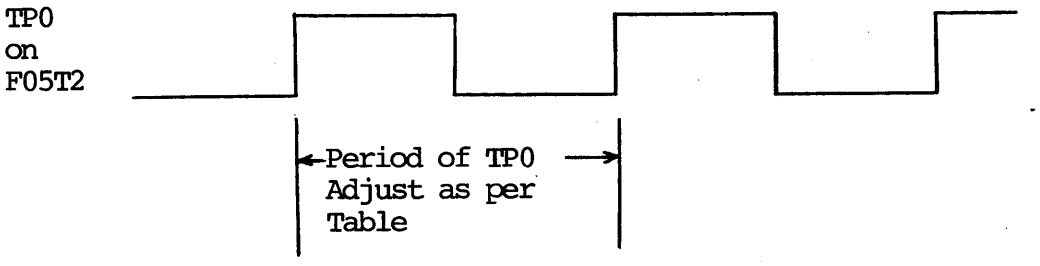


TABLE 2.4 Timeslice Adjustment

5. When this is accomplished correctly, raise switch 9 and 11 of the hardware switch register. On non-switch register machines type control S. Then modify the contents to be 5000 (octal).

   This section will test all the facilities of the transmitter accessable to the Unibus. This includes checking initialization pulses, setting and clearing of all possible bits, checking the data silo, data paths, and checking out the CRC logic.

6. When the transmitter test has run a number of passes without error halt the processor. Start at address 204 but run test 2 (the receiver section test). This test is similar to the transmitter except all tests are performed on the receiver logic. This test may be run with switch 11 of the hardware switch register on. Enter 1000 (OCTAL) on the software switch register.

7. When the receiver test has run a number of passes without error halt the processor. Run the transmitter receiver loop test. (Start at location 204 but run test 3.) This will test the ability of both the receiver and transmitter to NPR to a peripheral device, test communication between the receiver and transmitter through the TDM bus TTL transceivers and tests all reject, truncation and error logic.

8. In the event of an error on any one of the above tests, section 5 should be referred to as an aid in determining which module is at fault.

2.4 ACCEPTANCE PROCEDURE

The following procedure should be followed to determine if PCL11-B meets its operating requirements.

1) Ensure that the switch on M8003 is turned off (i.e. it points away from cable connectors).

2) Load PCL11 Standalone Test (CZPLBA0). Start it at location 200 (OCTAL). Enter all required information and when asked to select test, run test 4.

3) Let test run for a minimum of 100 passes without error.

4) Load PCL11 Exerciser (CZPLAA0) and start it at location 200, (OCTTAL). Set Master (type MASTER SET <CR>), set RIB (type RIB SET <CR>), and add the receiver address. Let run for five minutes and check to ensure there are no errors.

5) Configure a DECX/11 diagnostic for the system which this PCL11 module is part of. Run this diagnostic at least until the PCL Module has run successfully in all parts of memory (ie. at least one complete relocation cycle through memory and back to 000000).

6) After this has been accomplished correctly the PCL11-B is operating successfully as a Unibus peripheral. It still remains to check out the PCL11-B as part of a communications system. This procedure is outlined in the PCL11 Communications Systems Installation and Maintenance Guide (YC-A20TC-02).

2.5 RELATED LITERATURE

The following DEC publications contain material which supplements the information in this option description:

a) PDP11 Peripherals Handbook
b) PDP11 Maintenance Manual
c) PCL11 Standalone Test Listing and Instructions
d) PCL11 Exerciser Listing and Description
e) PCL11 DECX/11 Listing and Description
f) PCL11 Communications Systems - General Introduction and Configuration Guide (YC-A20TC-01)
g) PCL11 Communications Systems - Installation and Maintenance Guide (YC-A20TC-02).

SECTION 3

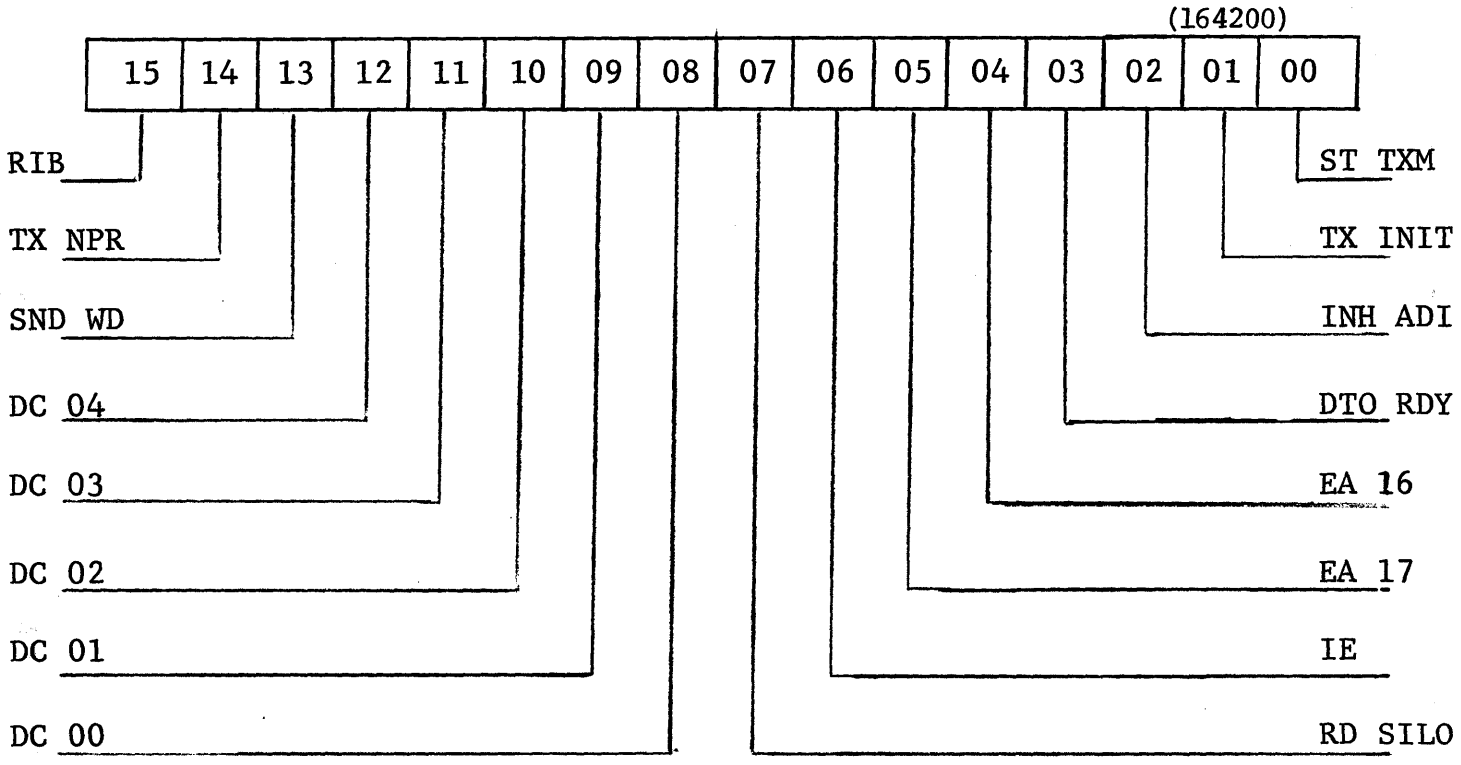
OPERATION AND CODING

3.1 INPUT/OUTPUT CODING

The following is a detailed bit assignment and description for all registers in the PCL11-B. There are seven registers associated with the transmitter. One of these, the TMMR, contains bits which control the master section. This means the master section, conceptually, is part of the transmitter logic; although in fact it is an independent section of logic. Default addresses are shown in brackets.

3.1.1 Transmitter Command Register (TCR)

Figure 3.1 shown the TCR register format.

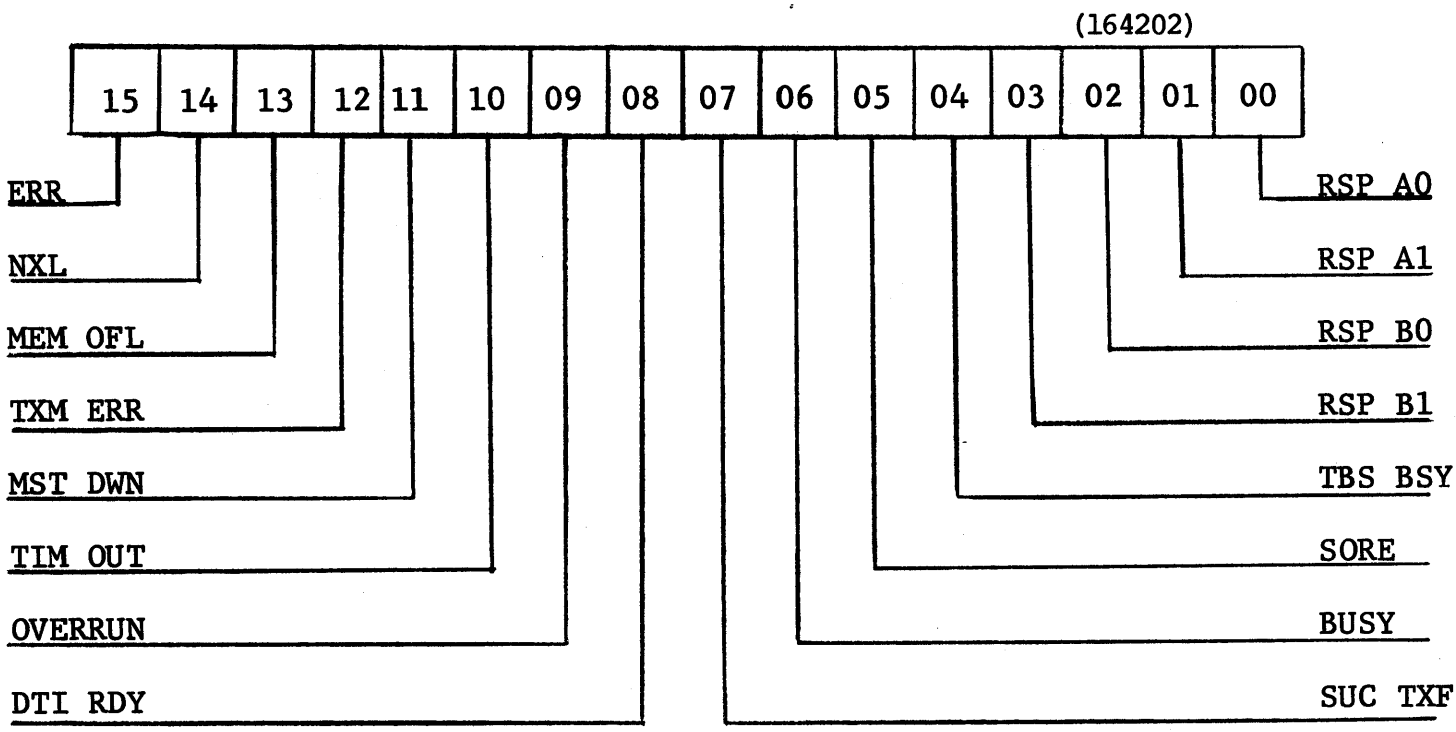


BIT		
0	ST TXM	START TRANSMISSION (R/W) When set will cause data and CRC character to be transmitted to receiver, selected by destination bits, (8-12) until the end of message. Will be cleared by an interrupt request (see bit 6) or TX INIT.
1	TX INIT	TRANSMITTER INITIALIZE (WO) When set will initialize all bits in the transmitter. Their initialized state is indicated in their description. This bit is asserted for only one instruction time. It is also generated by a BUS INIT or a Reset instruction.
2	INH ADI	INHIBIT ADDRESS INCREMENT (R/W) When set will inhibit incrementing of the Transmitter Source Bus Address (TSBA) register on NPR cycles. Cleared by TX INIT.
3	DT O RDY	DATA OUTPUT READY (RO) This bit will be set whenever a word is available to be moved out of the data silo (used primarily for maintenance). Cleared by TX INIT.
4	EA 16	EXTENDED BUS ADDRESS 16 (R/W) Together with EA 17 and the TSBA form an 18 bit address for NPR cycles. EA 16 and EA 17 will be automatically incremented when the TSBA overflows. Cleared by TX INIT.
5	EA 17	EXTENDED BUS ADDRESS 17 (R/W) As described above. Cleared by TX INIT.
6	IE	INTERRUPT ENABLE (R/W) An interrupt request is made if any of the following bits are set in the TSR: ERR, SUC TXF, SORE, or if RCV BSY is set and RIB is clear. When set, this bit will enable an interrupt request to cause an interrupt, if the processor is running on a lower priority then PCL11-B. Cleared by TX INIT.
7	RD SILO	READ SILO (R/W) When set, a read of the TSDB or low byte of the TMMR will remove a word from the data or address silo, respectively. When set no words may be loaded into either silo. Used primarily for maintenance. Cleared by TX INIT.

8	DC 00	DESTINATION CODE 00 (R/W) TCR bits 8-12 are loaded with the TDM bus address of the receiver with which communication will take place. (This address must not be zero.) Cleared by TX INIT.
9	DC01	DESTINATION CODE 01 (R/W) Cleared by TX INIT.
10	DC 02	DESTINATION CODE 02 (R/W) Cleared by TX INIT.
11	DC 03	DESTINATION CODE 03 (R/W) Cleared by TX INIT.
12	DC 04	DESTINATION CODE 04 (R/W) Cleared by TX INIT.
13	SND WD	SEND WORD (R/W) Must be set to open a channel. When set will cause one word to be sent to receiver, if ST TXM is clear. Cleared by interrupt request (see bit 6) and TX INIT.
14	TX NPR	TRANSMITTER NPR (R/W) When set, if the TSBC has been loaded with data will cause hardware to initiate a NPR transfer of one word to the TSDB when the TSDB is ready to accept a word. NPR cycles will continue until TSBC overflow, or an error occurs. No words may be moved into silo when set. Cleared by TSBC overflow and TX INIT.
15	RIB	RETRY IF BUSY (R/W) When set, will cause hardware to continue trying to open a channel with a receiver, even after receiving a busy response, until a TIME OUT error occurs. Cleared by TX INIT.

3.1.2 Transmitter Status Register (TSR)

Figure 3.2 shows the TSR register Format.



BIT

0 RSP A 0 RESPONSE A 0 (RO) TSR Bits 0 and 1 contain the Response A generated during the most recent transmitter timeslice (see section 3.3.3-2). In the event of an error these bits will be frozen in the state at which the error occurred, while in some cases, a 00 Response is returned to the receiver.
Cleared by TX INIT or SUC TXF.

1 RSP A 1 RESPONSE A 1 (RO)
Cleared by TX INIT or SUC TXF.

The RESPONSE A bits accompany every data word sent to the receiver. They indicate to the receiver what the transmitter is sending during the timeslice.

RSP A 1	RSP A 0	
0	0	Transmitter has an error or is off line
0	1	Null Cycle
1	0	Valid Word or CRC on data lines.
1	1	Last CRC on data lines

2 RSP B 0 RESPONSE B 0 (RO) TSR Bits 2 and 3 contain the Response B codes received during the most recent timeslice. These codes will be frozen in the same manner as TSR bits 0 and 1 in the event of an error.
Cleared by TX INIT or SUC TXF.

3 RSP B 1 RESPONSE B 1 (RO)
Cleared by TX INIT or SUC TXF.

The RESPONSE B bits are returned to the transmitter to indicate what the receiver will be doing with the data during the timeslice.

RSP B 1	RSP B 0	
0	0	Receiver has an error or is off line.
0	1	Null Cycle
1	0	Check failure (CRC or parity error has been detected on previous data).
1	1	Acknowledge CRC or data.

4 TBS BSY TDM BUS BUSY (R/W) This bit will be set if a busy response is received from a receiver while trying to open a channel. Will make an interrupt request only if RIB (TCR bit 15) is clear.
Cleared by CHN OPN or TX INIT.

5	SORE	SOFTWARE REJECT (R/W) This bit will be set if the receiver rejects or truncates a message. If SUC TXF is set and SORE is set, then a truncate has taken place. If SUC TXF is clear and SORE is set, then a Reject has taken place. Will cause an interrupt request. Cleared by TX INIT.
6	BUSY	BUSY (RO) Indicates the transmitter is engaged in a transmission. This bit will be set if either SND WD or CHN OPN is set. Cleared by TX INIT.
7	SUC TXF	SUCCESSFUL TRANSFER (R/W) When set indicates: (1) If SND WD was set and ST TXM was clear; one word has been moved into the receiver data silo. (SUC TXF and BUSY set, SORE clear). (2) Entire message has been sent, parity and CRC checked, data moved onto receiver's Unibus (SUC TXF set, SORE and BUSY clear). (3) Message has been truncated, but data transferred has succesfully passed CRC and parity decks (SUC TXF and SORE set, BUSY Clear). Cleared by TX INITT.
8	DTIRDY	DATA INPUT READY (RO) When set indicates a word may be loaded into the TSDB. Set by TX INIT.
9	OVERUN	DATA OVERRUN (R/W) When set indicates a data word has been lost by moving it into the TSDB before DTIRDY was set. Cleared by TX INIT.
10	TIM OUT	TIME OUT (R/W) This bit will set if, after SEND WORD is set, more than one time out period (approximately 2 sec) passes without a successful transfer of a word. Cleared by TX INIT.
11	MST DWN	MASTER DOWN (R/W) This bit will set if the transmitter has a word ready to send while the TDM bus master active line is unasserted. Cleared by TX INIT.

12 TXM ERR TRANSMISSION ERROR (R/W) When set indicates an error condition detected in communicating with a receiver. The type of error can be determined by looking at the RSP B and A bits.

i) CHECK FAIL (Parity or CRC error)
TSR Bit 15 = 1 ERR
12 = 1 TXM ERR
3 = 1 RSP B = 10
2 = 0
RSP A = don't care

ii) OFFLINE (Receiver has gone offline during message either due to error or unexpected shut down).
TSR BIT 15 = 1 ERR
12 = 1 TXM ERR
3 = 0
2 = 0 RSP B = 00
RSP A = don't care
(This will not cause an error on the first word (only a RCV BUSY) or while closing the channel for a SUC TXF).

iii) RCV ACCEPTS A NULL
TSR BIT 15 = 1 ERR
12 = 1 TXM ERR
3 = 1 RSP B = 11
2 = 1 (acknowledge)
1 = 0 RSP A = 01
0 = 1 (Null)

iv) RCV DOES NOT ACCEPT FIRST WORD
TSR BIT 15 = 1 ERR
12 = 1 TXM ERR
3 = 0 RSP B = 01
2 = 1 (Null)
1 = 1 RSP A = 10
0 = 0 Valid Word
If RCV not ready to accept the word, should return a busy.
Cleared by TX INIT.

13	MEMO OFL	MEMORY OVERFLOW (R/W) When set indicates TSBA has overflowed, and both EA 17 and EA 16 were set. Cleared by TX INIT.
14	NXL	NON-EXISTENT LOCATION (RO) When set indicates, an aborted NPR transferred was made to the address that was contained in the TSBA which does not exist on the Unibus. Cleared by writing a zero into this bit or by TX INIT.
15	ERR	ERROR (RO) This bit will set whenever any TSR bit 9 through 14 is set. Will make an interrupt request. Cleared by TX INIT.

3.1.3 Transmitter Source Data Buffer (TSDB)

Figure 3.3 shows the TSDB register format.

(764204)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Writing into this register will load a word into the transmitter's data silo. This may be done by NPR transfer or direct moves. If a MOV is used, the DTIRDY (TSR bit 8) should first be checked before loading this location. Only words may be loaded into this location.

For maintenance purposes, the silo may also be read. The data read from this location will be the next word to be removed from the silo. Further, if RD SILO (TCR bit 7) is set, after reading this location the word will be removed from the silo. No writes into this location will be executed while the RD SILO bit is set. Because the TSDB is the output of a 64 word FIFO during reading and the input of the FIFO during writing, instructions that involve a read restore cycle (e.g. BIS, ROR, ADD, INC) may not be executed accurately.

3.1.4 Transmitter Source Byte Count (TSBC)

Figure 3.4 shows the TSBC register format.

(764206)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

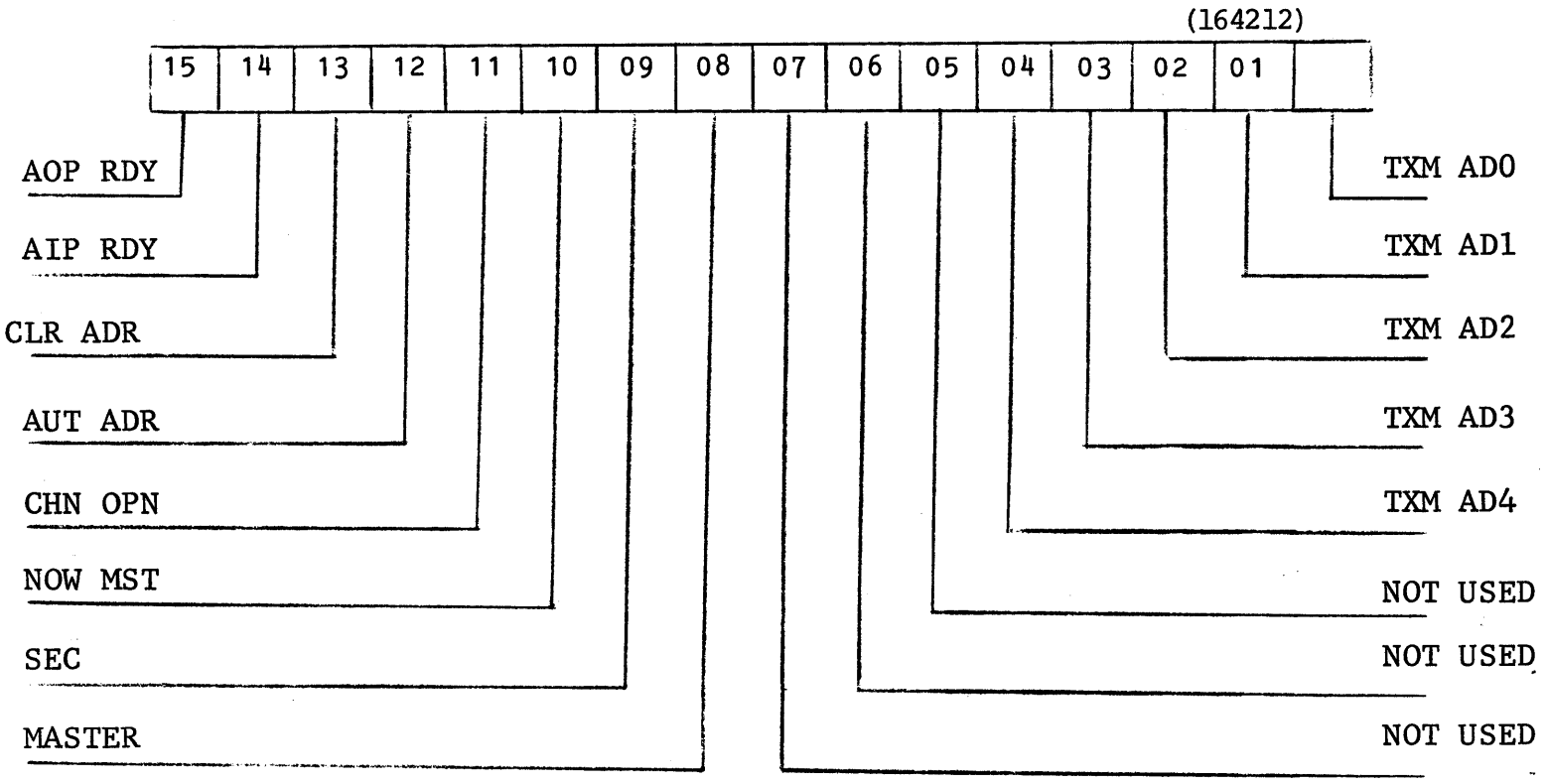
ALL BITS ARE READ/WRITE ALL BITS CLEARED BY TX INIT

FIGURE 3.5

This register is loaded with the address of the first word of the buffer to be transferred to the TSDB. The TSBA will be incremented after each NPR cycle executed, unless INH ADI (TCR bit 2) is set.

3.1.6 Transmitter Master/Maintenance Register (TMMR)

Figure 3.6 shows the TMMR format.



BIT

0	TXM AD0	TRANSMITTER ADDRESS 0
1	TXM AD1	TRANSMITTER ADDRESS 1
2	TXM AD2	TRANSMITTER ADDRESS 2
3	TXM AD3	TRANSMITTER ADDRESS 3
4	TXM AD4	TRANSMITTER ADDRESS 4

The low byte of the TMMR contains the address silo (see section 3.3.2-2). Data words are loaded into the silo by executing of MOVB instruction to the low byte. (AIP RDY should be checked before instruction is actually executed.) Silo is loaded with AUT ADR set and RD SILO clear. This silo must be loaded with at least 20 addresses but not more than 50 addresses.

The silo is used to generate transmitter addresses on the TDM bus which are not necessarily sequential. To implement this, it is first loaded with the desired sequence of addresses. (Before loading address silo bit 13 of the TMMR (CLR ADR) must be asserted.) (Care must be taken to insure the same address does not appear on successive timeslices.) When the unit becomes master, AUT ADR is cleared, thus enabling the silo to cycle.

Like the TSDB the low byte of the TMMR may also be read in a maintenance mode. The word read will be the one appearing on the output of the silo. If RD SILO is set, this word will be removed from the silo after reading. No loads of the silo will be executed with RD SILO set. (AUT ADR must also be set to obtain valid data when reading.) Because the low byte of the TMMR appears as the output of a 64 word silo during reading and the input of the silo during writing, instructions involving a read restore write cycle (e.g. BIS, ROR, ADD, INC) may not be executed accurately.

8	MASTER	MASTER (R/W) When set indicates this unit is TDM Bus MASTER. Cannot be set if there exists another master on the TDM bus. Cleared by external switch or BUS INIT. Set if SEC is set and there is no other TDM bus master, or by external switch.
9	SEC	SECONDARY MASTER (R/W) When set indicates this unit is a backup to the TDM bus master. May be set by external switch. Cleared by MASTER, external switch or BUS INIT.
10	NOW MST	NOW MASTER (R/W) When set indicates unit was secondary (SEC was set) and Master on the TDM bus was unasserted. (Unit has become Master.) (N.B. When checking this bit, byte manipulation should be used.) Cleared by BUS INIT.

11 CHN OPN CHANNEL OPEN (RO) When set indicates there is a channel open with a receiver.
Cleared by TX INIT.

12 AUT ADR AUTO ADDRESS (R/W) When set, counter will generate transmitter addresses and the transmitter address silo will be frozen. When clear the address silo will cycle putting out transmitter addresses in the desired sequence.

Set by an empty address silo or BUS INIT.

13 CLR ADR CLEAR ADDRESS SILO (WO) When set will clear out the address silo. This bit is only asserted for one instruction time. Also generated by a BUS INIT.

14 AIP RDY ADDRESS INPUT READY (RO) When set indicates the address silo may be loaded with a word.
Set by asserting CLR ADR or a BUS INIT.

15 AOP RDY ADDRESS OUTPUT READY (RO) When set indicates a word is ready to be moved out of the address silo.
Cleared by asserting CLR ADR or a BUS INIT.

3.1.7 Transmitter Source CSC (TSCRC)

Figure 3.7 shows the TSCRC register format.

(764214)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

FIGURE 3.7

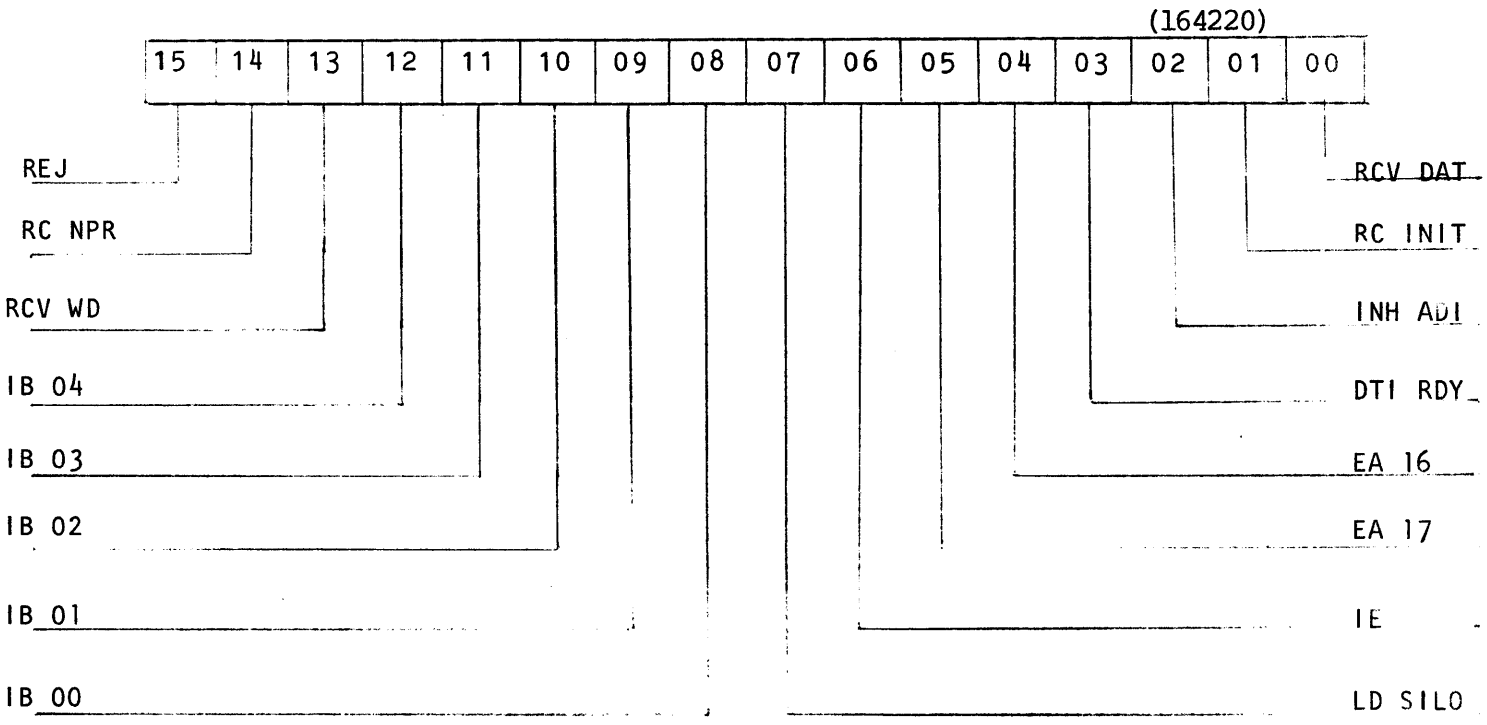
Each time a word is ready at the output of the data silo it is strobed through the CRC logic. The resulting character may be read in this location. This is used for maintenance purposes only.

3.2 RECEIVER BIT DEFINITIONS

There are six registers associated with the receiver.

3.2.1 Receiver Command Register (RCR)

Figure 3.8 shows the RCR register format.

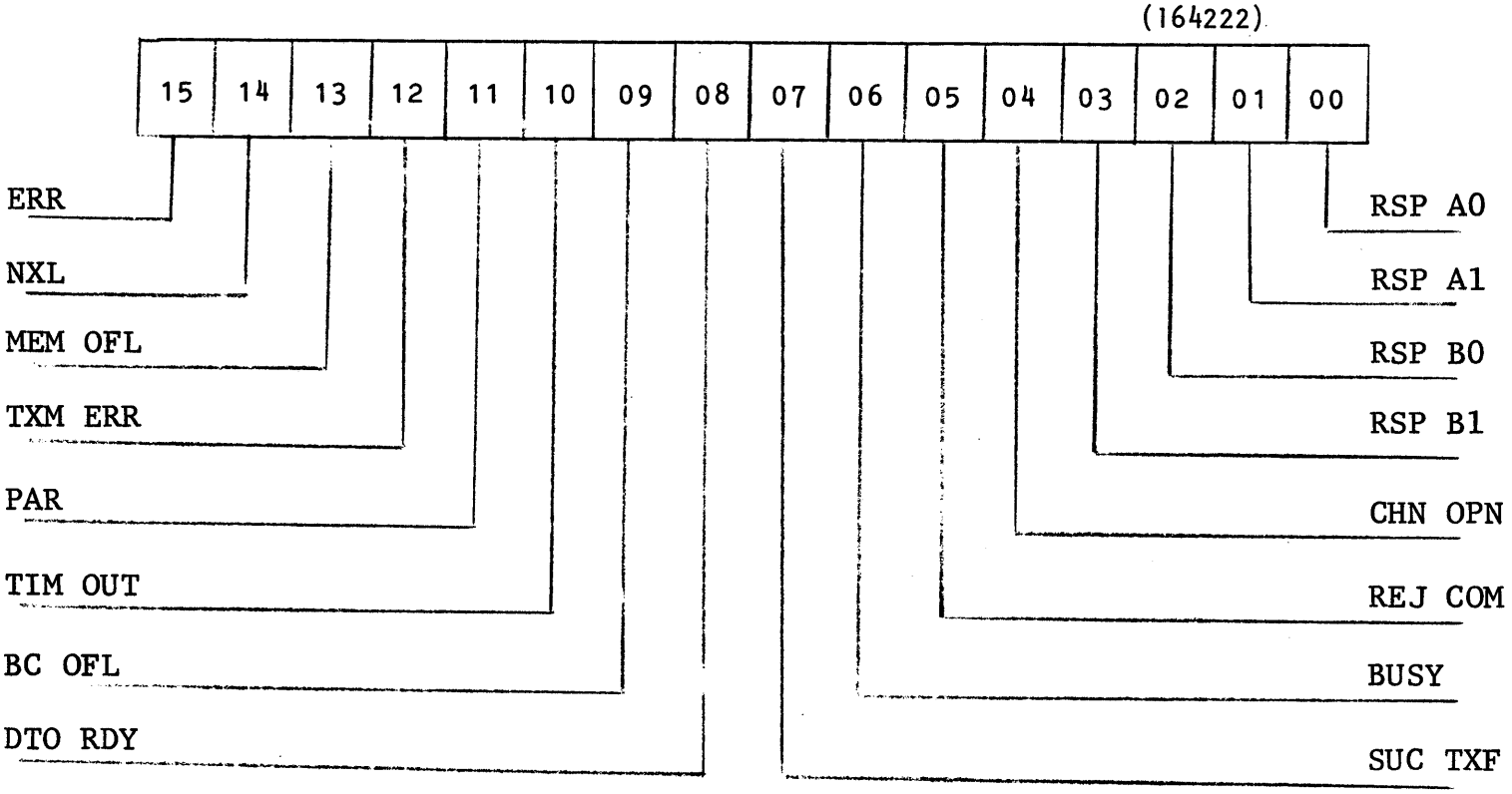


BIT		
0	RCV DAT	RECEIVE DATA (R/W) When set, will accept all words and CRC characters until the end of message from a transmitter with which there is a channel open. Cleared by an interrupt request (see bit 6), (except that of a DTO RDY or RC INIT.
1	RC INIT	RECEIVER INITIALIZE (WO) When set will initialize all bits in the receiver. Their initialized state is indicated in their description. This bit is asserted for only one instruction time. It is also generated by a BUS INIT or Reset instruction.
2	INH ADI	INHIBIT ADDRESS INCREMENT (R/W) When set will inhibit incrementing of the Receiver Destination Bus Address (RDBA) register on NPR cycles. Cleared by RC INIT.
3	DTIRDY	DATA INPUT READY (RO) The bit will set whenever the data silo is ready to accept loading of a word. (Primarily used for maintenance purposes.) Set by RC INIT.
4	EA 16	EXTENDED BUS ADDRESS 16 (R/W) Together with E17 and the RDBA form a 18 bit address for NPR cycles. EA 16 and EA 17 will be automatically incremented when the RDBA overflows. Cleared by RC INIT.
5	EA 17	EXTENDED BUS ADDRESS 17 (R/W) As described above. Cleared by RC INIT.
6	IE	INTERRUPT ENABLE (R/W) An interrupt request is made if any of the following bits are set: ERR, SUC TXF, REJ COM or DTORDY is set and RC NPR is clear. When set, IE will enable an interrupt request to actually interrupt processor, if it is running on a lower priority than the PCL11-B. Cleared by RC INIT.
7	LD SILO	LOAD SILO (R/W) When set the data silo may be loaded by moving a word into the RDDB. Reading the RDDB will not remove a data word if LD SILO is set. Cleared by RC INIT.

8	IB 00	IDENTIFICATION BIT 00 (RO) RCR bits 8-12 contain the address of the transmitter which is communicating, or last was in communication with the receiver. Cleared by INIT.
9	IB 01	IDENTIFICATION BIT 01 (RO) Cleared by RC INIT.
10	IB 02	IDENTIFICATION BIT 02 (RO) Cleared by RC INIT.
11	IB 03	IDENTIFICATION BIT 03 (RO) Cleared by RC INIT.
12	IB 04	IDENTIFICATION BIT 04 (RO) Cleared by RC INIT.
13	RCV WD	RECEIVE WORD (R/W) Must be set to open a channel. When set will cause one word to be accepted, (if RCV DAT is clear) from the first transmitter to address the receiver. Cleared by interrupt request, receipt of a word or RC INIT.
14	RC NPR	RECEIVER NPR (R/W) When set, if the RDBC is loaded, will cause hardware to initiate a NPR transfer of one word from the Data silo, when such a word is ready. NPR cycles will continue until the silo is empty, an error occurs or the RDBC overflows. No words may be moved from the silo, when RC NPR is set. Cleared by RC INIT.
15	REJ	REJECT (R/W) After channel is open, if REJ is set before RCV DAT receiver will reject message. If set after RCV DAT receiver will truncate message. Cleared by RC INIT.

3.2.2 Receiver Status Register (RSR)

Figure 3.9 shows the RSR format.



0 RSP A 0 RESPONSE A 0 (RO) RSR bits 0 and 1 contain the response codes received from the transmitter during the most recent timeslice. In the event of an error, these will be frozen while a RSP B = 00 is returned to the transmitter.

Cleared by RC INIT or SUC TXF.

1 RSP A 1 RESPONSE A 1 (RO)
Cleared by RC INIT or SUC TXF.

The Response A bits accompany every data word sent to the receiver. They indicate to the reciever what the transmitter is sending during the timeslice.

RSP A 1	RSP A 0	
0	0	Transmitter has an error or is off line.
0	1	Null Cycle
1	0	Valid Word or CRC on data lines.
1	1	Last CRC on data lines.

2 RSP B 0 RESPONSE B 0 (RO) RSR bits 2 and 3 contain the Response bits last sent out to the transmitter. In the event of an error these will be frozen while a RSP B = 00 is returned to the transmitter.
Cleared by RC INIT or SUC TXF.

3 RSP B 1 RESPONSE B 1 (RO)
Cleared by RC INIT or SUC TXF.

The Response B bits are returned to the transmitter to indicate what the reciever will be doing with the data during the timeslice.

RSP B 1	RSP B 0	
0	0	Receiver has an error or is off line.
0	1	Null Cycle
1	0	Check failure (CRC or Parity error has been detected on previous data).
1	1	Acknowledge CRC or data.

4. CHN OPN CHANNEL OPEN (RO) When set indicates there is a channel open with a transmitter.
Cleared by RC INIT.

5 REJ COM REJECT COMPLETE (R/W) When set indicates a rejection or truncation has been completed. If SUC TXF is clear, this has been a reject. If SUC TXF is set, it was a truncate. Will cause an interrupt request.
Cleared by RC INIT.

6	BUSY	BUSY (RO) Indicates the receiver is engaged in a reception. Will be set if CHN OPN or SND WD is set. Cleared by INIT.
7	SUC TXF	SUC TXF (R/W) When set indicates: 1) Entire message has been received, with parity and CRC checks. (SUC TXF set; REJ COM clear). 2) Message has been truncated but CRC and parity have been checked. (SUC TXF set; REJ COM clear.) Will cause an interrupt request. Cleared by RC INIT.
8	DTORDY	DATA OUTPUT READY (RO) When set indicates a word is ready on the output of the data silo. Will cause an interrupt request if RC NPR is clear. Cleared by RC INIT.
9	BC OFL	BYTE COUNT OVERFLOW (R/W) When set indicates the RDBC has overflowed. Cleared by RC INIT.
10	TIM OUT	TIME OUT (R/W) This bit will set if, after a channel is open, more than one time out period (approximately 1.5 secs) passes without a successful tranfer of a word. Cleared by RC INIT.
11	PAR	PARITY (R/W) When set indicates a parity error has been detected on an incoming word or CRC character. Cleared by RC INIT.
12	TXM ERR	TRANSMISSION ERROR (R/W) When set indicates an error condition has been detected in communicating with a transmitter. The type of error can be defined by looking at the RSP B & A bits. i) CHECK FAIL (Parity or CRC error) RSR bit 15 = 1 ERR 12 = 1 TXM ERR 3 = 1 RSP B = 10 2 = 0 RSP B = 10 RSP A = don't care

ii) OFFLINE (Transmitter has error)
RSR bit 15 = 1 ERR
12 = 1 TXM ERR
3 = d
2 = d RSP B = don't care
1 = 0 RSP A = 00 (offline)
0 = 0

iii) FAILED TO OPEN CHANNEL
RSR bit 15 = 1 ERR
12 = 1 TXM ERR
3 = 0 RSP B = NULL
2 = 1
1 = 0 1 RSP A indicates
or first word was
0 = 1 1 not valid.
(occurs only on first word).
Cleared by RC INIT.

13 MEM OFL MEMORY OVERFLOW (R/W) When set indicates RDBA has overflowed and both EA 17 and EA 16 were set.
Cleared by RC INIT.

14 NXL NON-EXISTENT LOCATION (RO) When set indicates address that was contained in RDBA does not exist on the Unibus and an NPR to the location was aborted.
Cleared by writing a zero into this bit or by RC INIT.

15 ERR ERROR (RO) This bit will set whenever any RSR bit 9 through 14 is set. Will make an interrupt request.
Cleared by RC INIT.

3.2.3 Receiver Destination Data Buffer (RDDB)

Figure 3.10 shows the RDDB format.

(764224)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Figure 3.10

All data received from the transmitter will appear on the output of the data silo at this location. This data must be read, then removed before the transfer is considered complete. This may be done by NPR transfers or direct moves. If a MOV instruction is used, the DTORDY (RSR bit 8) should first be checked. (This bit may cause an interrupt if RC NPR is clear).

For maintenance purposes the silo may also be loaded. If LD SILO is set, moving a word into this location will load it into the data silo. With LD SILO set, reading the TSDB will not remove the word read from the silo.

Because the RDDB is the input of a 64 word silo when writing and the output of the silo when reading, instructions that involve a read restore write cycle (e.g. BIS, ROR, ADD, INC) may not be executed accurately, on this location.

3.2.4 Receiver Destination Byte Count (RDBC)

Figure 3.11 shows the RDBC register format.

(764226)

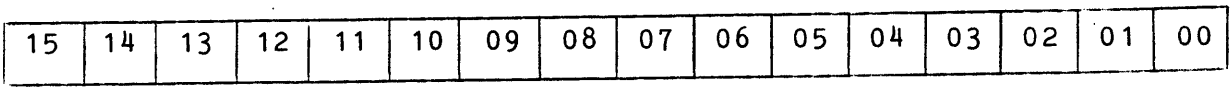


Figure 3.11

This register is loaded with the 2's complement of the number of bytes of the length of the buffer area to which the received data is to be placed via NPR transfers. During NPR's this register will increment twice every time a word is transferred from the silo to its destination. If more data is sent than indicated in the RDBC, BC OFL will set. The host computer may then decide to allocate more room, or truncate the message.

3.2.5 Receiver Destination Bus Address (RDBA)

Figure 3.12 shows the RDBA register format.

(764230)

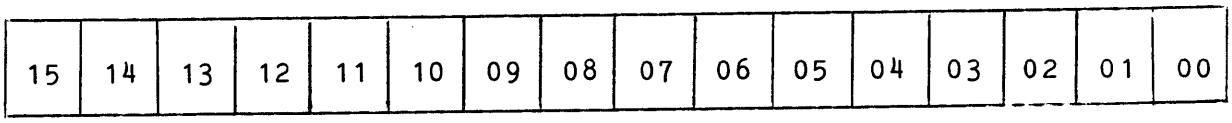


Figure 3.12

The register is loaded with the address of the first word of the buffer area to which the received data is transferred. The RDBA will be incremented after each NPR cycle is executed, unless INH ADI (RCR bit 2) is set.

3.2.6 Receiver Destination CRC (RDCRC)

Figure 3.13 shows the RDCRC register format.

(764234)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

ALL BITS READ ONLY ALL BITS CLEARED BY RC INIT

Figure 3.13

Each time a word is loaded into the silo it is also strobed through the CRC logic. The resulting character may be read in this location. This is used for maintenance purposes only.

3.2.7 Summary of Registers and Mnemonics

Transmitter

The following is a list of registers and their standard addresses:

Transmitter Command Register	764200	TCR
Transmitter Status Register	764202	TSR
Transmitter Source Data Buffer	764204	TSDB
Transmitter Source Byte Counts	764206	TSBC
Transmitter Source Bus Address	764210	TSBA
Transmitter Master/Maintenance Reg.	764212	TMMR
Transmitter Source Cyclic Redundancy Character	764214	TSCRC
Interrupt Vector	170	

Receiver

The following is a list of registers and their standard addresses.

Receiver Command Register	764220	RCR
Receiver Status Register	764222	RSR
Receiver Destination Data Buffer	764224	RDDB
Receiver Destination Byte Count	764226	
Receiver Destination Bus Address	764230	RDBA
Receiver Destination Cyclic Redundancy Character	764234	RDCRC
Interrupt Vector	174	

NOTE: PCL11-B will respond to addresses 764216, 764232, 764236. However, since these registers are not part of the device writing into them will have no effect, and reads will be returned all zeros.

3.3 PCL11-B OPERATION

This section is a general discussion of the manner in which one PCL11-B may transfer data to another over the TDM bus. Timing, detailed description of TDM bus signals, the protocol for proper transfer and descriptions of software/hardware interactions will be discussed. Section 4 provides a relationship between this discussion, the block diagram and the physical layout and implementation of the concept described in this section.

3.3.1 General Operation

One 16 bit word may be transferred from a transmitter to a receiver every 2 microseconds. The timing signals for the transfer are generated from an enabled Master section, (only one section may be enabled on a TDM at any time) and the control signals are generated from the transmitter (e.g. Receiver address and type of transfer). Before a successful transfer can take place both the transmitter and receiver involved must be properly set up by programs residing in their respective computers.

3.3.2 Master Section

The master section has two functions. It divides the bus up into "Timeslices" by generation of two timing signals TP 0, TP 1. These timing signals are used by both the transmitter and receiver to complete data transfers. The master section also provides a new five bit transmitter address every timeslice. This will be decoded by one transmitter on the bus and enable it to effect a word transfer.

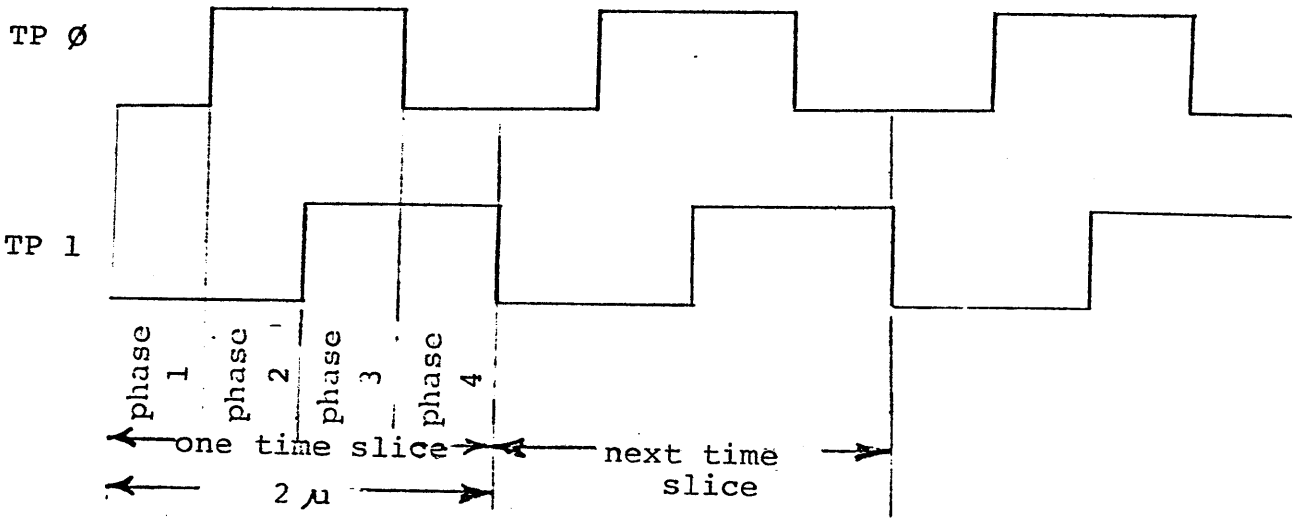


Fig. 3.14
TP 0 and TP 1

3.3.2-1 Time Phase Signals

Each master section has a clock which produces the two time phase signals TP 0 and TP 1. These are both square waves, 90 degrees out of phase. They may be adjusted so as to have a correct period corresponding to bus length, and they are seen by all transmitter and receivers on the bus (see figure 3.14).

As can be seen from figure 3.14 these two signals further divide each timeslice into 4 phases. During each phase one part of the data transfer will take place.

3.3.2-2 Address Generation

The master section also provides a transmitter address every timeslice. Every transmitter section contains a five bit address switch which is set up to the transmitter's TDM bus address. During Phase 1 of each timeslice, every transmitter on the TDM bus will compare this switch to the address generated by the master section. If it compares, the transmitter may use the rest of the timeslice to send one 16 bit word of a message to a receiver of its choice. Since a new transmitter may be selected every timeslice, a number of transmitters may be in the process of transmitting a message at the same time. Each will wait its turn to send one word of its message to the receiver.

The master section may generate these transmitter addresses in one of two ways. The first, and simplest, method involves the use of a five bit decrementing counter. The counter is loaded with the number contained in a five bit switch residing in the master section. The counter is decremented, by one, every timeslice, until address number one is being put out onto the bus. The counter will then be reloaded with the number in the switch in time for the next timeslice, whereupon the entire process will repeat itself.

The second means of address generation involves use of a five bit by fifty word address silo (which consists of a FIFO: First In, First Out memory). This silo may be loaded, by software, with five bit transmitter addresses in any sequence (the only exception to this being that no address may appear in succession). When this silo is enabled, the addresses contained in the silo are put out onto the bus for one timeslice, and then returned to the top of the silo. They will continue circulating like this until disabled. Generating transmitter addresses in this manner allows great flexibility in assigning the speed of transfer of messages. If one transmitter's address is loaded into the silo, for example, so as to appear every second timeslice, while all other addresses appear only once, then this transmitter will be able to send an entire message more quickly than any other.

Which of the above two methods is used by an enabled master section is determined by the state of the Auto-Address (AUT ADR) bit in the TMMR register (see Section 3.1.6). When this bit is set, the counter method of address generation is operational, when cleared the address silo is used. This bit will be set whenever the address silo is empty or when set via the Unibus. This bit must be set during the time which the address silo is being loaded. Once the silo is loaded this bit may be cleared, thus enabling the silo to circulate. It should be noted that at least 20 addresses must be loaded into the silo before reliable operation will occur.

3.3.2-3 Enabling the Master Section

Although each PCL11-B unit contains its own master section, only one of these may be enabled at any one time, when a number of units are connected together on a TDM bus. A master section is enabled when the MASTER bit is set in the TMMR register. There are three ways in which this bit may be set. First, it may be set from its host computer, via the Unibus. Second, it may be set via external switches.

The last method involves another bit in the TMMR, the Secondary (SEC) bit. This bit is used to transfer mastership of the TDM bus from the enabled master section to a backup master, automatically, in the event the first master is removed from the bus for any reason. An enabled master section will assert a TDM bus line called MASTER ACTIVE. Assertion of this line will prevent setting of a different Master bit by the above two methods. If a master section has its SEC bit set, and sees MASTER ACTIVE become unasserted, it will set its own MASTER bit and take over mastership of the bus; then clear SEC. At the same time NOW MST sets in the TMMR indicating this PCL11-B has assumed the role of TDM bus master.

The SEC bit may be set via the Unibus, or through use of external switches. Care must be taken to ensure no more than one SEC bit is set at any one time. This will guarantee that upon any master going down, only one new master will take its place.

3.3.3 Data Transfer

The transmitter uses the address and time phase signals generated by the master section to syncronize communication. During each phase one part of the transfer of one word of the message takes place.

3.3.3-1 Phase 1

During this period of time the transmitter is comparing the 5 bit transmitter address on the TDM bus with its own address switch. When the two compare, this indicates the transmitter's timeslice. Before the transmitter will use the timeslice however, one of two conditions must occur. The transmitter must either be in communication with a receiver (have a channel open) or be in the process of opening one. If one of these conditions exists, and the TDM bus transmitter address compares with its own, then active communication will commence during phase 2.

3.3.3-2 Phase 2

During this period the transmitter will assert the TDM bus data lines, putting out the word it wishes to transfer. This word comes from the output of a 64 word by 16 bit data silo (which is a FIFO, First In, First Out memory). At the same time, the receiver address is asserted on the TDM bus, as well as two Response A lines. These two lines indicate to the receiver what type of transfer is coming during the next two phases. These two lines allow four possibilities:

RSP A 1	RSP A 0	
0	0	<u>OFFLINE</u> If neither line is asserted one of two possibilities exists: 1) the transmitter either does not exist on the bus or it did not satisfy either condition for commencing communication as per 3.3.3-1. (If this case exists all receiver address lines will also be 0's.) 2) The transmitter, during communication, has come up with an error and will consider the channel closed after this timeslice.
0	1	<u>NULL CYCLE</u> The transmitter will assert only the RSP A 0 line if either data is not ready to be sent or no command bit to send a word is set. A null cycle should only occur with a channel already open.
1	0	<u>VALID WORD OR CRC</u> Only RSP A 1 line is asserted if the data lines on the bus are being driven by a word to be transferred or a Cyclic Redundancy Check (CRC) character.
1	1	<u>LAST CRC</u> Both lines are asserted for these timeslices. The last character to be sent is always a CRC check character. This response is an indication to the receiver to begin channel closing procedure.

Both the receiver and transmitter separately remember whether a channel is opened. A channel is opened on the successful transfer of the first word of a message, and will be closed after sending of either the first or last of the Response A codes above.

During this phase the receiver decodes the five receiver address lines being driven by the transmitter. Decoding is accomplished by comparison of these five lines with the five bit address switch residing in the receiver section. At the end of phase 2 the receiver will decide if it has been addressed, and then take the appropriate action.

3.3.3-3 Phase 3

Once the receiver has decided that it has been addressed, it will set up its own Response Codes to be sent back to the transmitter. These codes will indicate to the transmitter exactly the receiver's response to what the transmitter has done during the timeslice.

Before setting up these codes, the receiver looks at a number of different things in the interface. First, the address of the transmitter will be checked. If the word being sent is the first of a message, this address will not matter. However, if a channel is already opened, the receiver will compare the address of the transmitter presently talking to it with that of the transmitter with which it has an open channel. If the address does not compare, the receiver will return a busy response. The receiver also looks at the response codes that the transmitter has sent. From these the receiver can discover the type of transfer occurring in the timeslice, and thereby deduce what its response should be.

Finally, the receiver will check the command bits in the interface. They will indicate whether a word, (or message) should be accepted.

The receiver has two response lines (called RSP B 0 & 1) allowing four possible responses:

RSP B 1	RSP B 0	
0	0	<u>BUSY OR OFFLINE</u> Neither line will be asserted if: 1) The receiver does not exist on the bus or is not set up to receive a message. 2) The receiver has an open channel with a different transmitter. 3) The receiver, during communication, has come up with an error and will consider the channel closed after this timeslice.

0	1	NULL CYCLE The receiver will assert only the RSP B 0 line if it is not prepared to receive a word during this timeslice (e.g. silo full), it does not have the proper command bits sets, or if the transmitter is executing a null cycle. A null cycle may only occur when the channel is open.
1	0	CHECK FAIL Only RSP B 1 will be asserted if the receiver has detected a CRC or parity error.
1	1	ACKNOWLEDGE Both lines will be asserted if: 1) The transmitter has sent a valid word and the receiver will take it and put it into its silo. 2) The transmitter has sent a CRC on a previous timeslice and it has been checked by the receiver and found to have no errors.

3.3.3-4 Phase 4

At the beginning of this phase the receiver actually removes the data from the bus by strobing it into a 64 word by 16 bit data silo. During this phase the receiver is driving the TDM bus with its response to the transmitter. At the end of the phase the transmitter will strobe these responses into its interface. Depending on what these response bits actually are, it will begin setting up for the next transfer. If the receiver has accepted a data word, the transmitter will remove the sent word from it's silo.

3.3.4 Checking of Data

There are two checks made on the data sent from the transmitter to the receiver. First, every 16 bit word transferred is accompanied by a parity bit (odd parity is used). In the event that the receiver detects a parity error in any word received, the receiver will return a CHECK FAIL response, and consider the channel closed, on the succeeding timeslice.

As well as parity, Cyclic Redundancy Check (CRC) characters are used to further guard against data errors during transmission. This method of error detection involves modulo 2 division of the message by a selected polynomial, in this case $1 + X^8 + X^{15}$. Both receiver and transmitter contain logic to perform division by the polynomial. This logic keeps track of only the remainder of the division. Before each word is removed from the transmitter's data silo it is divided by the polynomial. The remainder after the entire block of the message has been sent will be the CRC character. The receiver performs the identical division as the words are loaded into its silo. The remainders after all data words have been processed are equal if no errors have occurred. The check character will be sent as part of the message and when divided by the receiver, modulo 2, will result in a remainder of zero, if transmission was error free.

If $Q(x)$ was message polynomial
$P(x)$ was selected polynomial
$S(x)$ the quotient of $\frac{Q(x)}{P(x)}$

$R(x)$ the remainder of $\frac{Q(x)}{P(x)}$

then in transmitter we perform:

$$\frac{Q(x)\,X^{16}}{P(x)} = S(x) + \frac{R(x)}{P(x)}$$

$Q(x)$ is shifted by 16 bits (as the remainder $R(x)$ will be appended to message) by multiplying by X^{16}.
In the receiver we perform:

$$\frac{Q(x)\,X^{16} + R(x)}{P(x)} = \frac{\text{Received message}}{P(x)}$$

$$= S(x) + \frac{R(x)}{P(x)} + \frac{R(x)}{P(x)}$$

$$= S(x)$$
(Modulo 2 addition)

Any error, not divisable by $P(x)$ will be detected by a non-zero remainder after the division. If the error is represented by $E(x)$, when the check is performed:

$$\frac{Q(x)\,X^{16} + R(x) + E(x)}{P(x)} = S(x) + \frac{R(x)}{P(x)} + \frac{R(x)}{P(x)} + \frac{E(x)}{P(x)}$$

$$= S(x) + \frac{E(x)}{P(x)}$$

a non-zero remainder result.

The selected polynomial will detect the following errors:

a) any odd number errors.
b) all double errors.
c) all burst errors of length 15 or less.
d) 99.994% of bursts of length 16.
e) 99.997% of bursts longer than 16.

Because of the fact that the above error detection capabilities will only be valid with messages of up to 2635_{10} bits (164_{10} words), a block length of 128_{10} (200_8) words was selected.[10] The transmitter will insert a CRC character after every block, and then begin calculation of a new CRC character. The last block transmitted may be less than or equal to 200_8 words, only one CRC will be sent after this block, no matter what size it is.

Both receiver and transmitter are counting the number of words being transferred and thus are able to tell when a CRC is to be transferred. The CRC is actually sent in exactly the same manner as a data word. It is accompanied by a RSP A of 10, unless it is the last CRC in the message, in which case RSP A = 11.

3.3.5 Channel Opening and Closing

As indicated in section 3.3.3-2 a channel is opened between a receiver and transmitter upon the successful transfer of one word between them. Both units have a channel open bit (CHN OPN, see sections 3.1 and 3.2) in one of their registers which is set upon this transfer and cleared only at the end of a message or in the event of an error.

In the transmitter, in the event of receipt of a check-fail or an off line response from the receiver or else a Master Down or Time Out error, the transmitter will immediately clear CHN OPN and interrupt its processor with an error. Other transmission errors, over run, and non-existent location errors will wait until the next transmitter timeslice, then send out a RSP A = 0 0 to the receiver before clearing CHN OPN and interrupting. The RSP A & B bits, which may be read by the transmitter's processor, will remain frozen in the state which they were at the time the error occurred.

Memory overflow errors will result in a suspension of NPR cycles until the error condition is removed. TDM bus transfer may continue as usual, but the silo is liable to empty out, causing only Null Cycles to occur, on the TDM bus.

The receiver, in the event of the receipt of an offline response from the transmitter or a check fail having been sent to the receiver, will immediately clear CHN OPN and interrupt its processor with the error. In the event of other transmission errors or a non-existent location error the receiver will wait until the next time the transmitter with which the channel is opened addresses its receiver, and then send out a RSP B = 0 0. After the timeslice CHN OPN will be cleared and the processor interrupted. As in the transmitter, the response codes which may be read by the computer are frozen at the time that the error occurred. Memory overflow and byte count errors will only result in the suspension of NPR activity until the error is handled. However, the receiver silo may become full, resulting in a number of null cycles occurring on the TDM bus. If a timeout error occurs, the receiver will immediately clear CHN OPN and cause an interrupt.

When the end of message occurs, there is a definitive sequence for the closing of the channel between the transmitter and receiver. First, the transmitter decides that all of the data has been sent. This is considered done when the data silo is empty and the byte count register has overflowed. (The byte count register is originally loaded with the 2's complement of the number of words to be sent, and is incremented twice every time a word is loaded into the silo from the Unibus). When this occurs, the transmitter prepares and sends the last CRC character accompanied by RSP A = 11. This response is an indication to the receiver that the message has been entirely transmitted. The receiver will check the CRC character, and then wait until its silo has been emptied into its Unibus. After this the receiver will respond with a RSP B = 1 1. When the transmitter sees this response it will wait then expect to see RSP B = 0 0. This will ensure the response lines have not become permanently stuck in the asserted state. After this has happened the receiver and transmitter will clear CHN OPN.

CHN OPN will also be cleared after a reject or truncate operation. This is discussed in Section 3.7.

3.3.6 Command Procedure

Sections 3.3.1 through 3.3.5 discussed in detail how data is transferred, one word per timeslice, until the entire message is sent and checked. It only remains to look at the host computer's function in the transfer.

3.3.6.1 Transmitter

The transmitter logic will remove data from its silo and send it to the desired receiver. The host computer has three functions to fulfill in order to complete the transfer. First, it must load the silo with the data to be transferred. This can be done in two ways. The silo input appears on the Unibus as a register (the Transmitter Source Data Buffer, TSDB). Moving a word to this location will cause it to be loaded into the silo, where upon it will migrate towards the output. Thus, the transmitter may load up the silo with as many words as desired simply by moving them into the TSDB.

As well as simple moves, the host processor may set up an NPR transfer of a section of memory to the TSDB. This can be effected by loading the Transmitter Source Byte Count (TSBC) with the 2's complement of the number of bytes to be loaded, and loading the Transmitter Source Bus Address (TSBA) with the first address of the section of memory to be loaded. When these registers have been loaded the actual NPR cycles are initiated by setting the TX NPR (bit 14, section 3.1.1) bit in the Transmitter Command Register (TCR). Once this bit has been set, moves to the TSBD will be inhibited.

Both direct move and NPR transfer methods of loading the silo may be used in the sending of a message. It is important to realize, however, that the TSBC is incremented twice every time a word is loaded into the silo, by moving or by NPR transfer. Therefore the TSBC should be loaded with the total number of NPR transferred to the silo. The TSBC is used by the transmitter logic to determine if there are any more words to be transferred, and hence should be loaded even if no NPR's are to take place. (The TSBC need not be loaded if the user can ensure the data silo will not be empty until the last word of the message has been sent to the receiver.)

The second function which the transmitter host computer must fulfill is to specify the receiver to which the message is destined. This is achieved by loading the five bit TDM BUS address of the receiver into the destination code bits in the TCR. (DC 00 - DC 04 are bits 8 through 12).

Finally, the host computer must enable the transmission by setting the proper command bits in the TCR. Send Word (SND WD bit 13) must be set to open a channel with a receiver. It will cause one word to be sent out before interrupting the processor after opening the channel. If so desired it may be set again a number of times, each time sending out only one word before interrupting. While waiting for the bit to be set, after the channel is opened, the hardware will execute a number of null cycles. Start transmission (ST TXM - bit 0) will cause all words to be sent, on successive timeslices if possible, until the entire message has been transmitted. After the CRC has been checked, and the channel properly closed the processor will be interrupted. The ST TXM bit may be set at the beginning of the message as well as SND WD. In this case no interrupts will occur until the entire message has been transferred. ST TXM may be set at any time and, even if SND WD is also set, no interrupts will occur until the end of the message. However, SND WD must be set at the beginning of the message to open the channel.

3.3.6-2 Receiver

The receiver's host computer must perform similar functions to that of the transmitter's, except these are involved in unloading the silo onto the Unibus. The receiver contains command bits similar in function to the transmitter's, which must be manipulated.

The receiver's host computer is responsible for unloading the data silo in one of two ways. The silo output appears as a register on the Unibus (the Receiver Destination Data Buffer RDDB). Moving a word from this location will cause it to be removed from the silo. Thus, the receiver may unload the silo simply by moving data words out of the TSDB.

On the other hand, the host processor may set up an NPR transfer of the data in the silo to a buffer area in memory. This buffer area is defined by a Receiver Destination Byte Count RDBC) and a Receiver Destination Bus Address (RDBA) register. The RDBA is loaded by the host computer with the first address of the buffer, and the RDBC with the 2's complement of the number of bytes. Once these registers are loaded and RC NPR (RCR bit 14 - section 3.2.1) is set, a word being ready at the output of the silo will begin an NPR cycle to remove the data to the buffer. Setting RC NPR bit will inhibit program moves out of the silo.

The RDBC will be incremented every time an NPR cycle is executed. After a message is successfully received, this register may be used to determine the number of words actually transferred into the buffer. If the incoming message has more words than set up in the RDBC, then a byte count overflow error will occur. The host computer may then set up a new buffer or merely truncate the message (see section 3.3.7) at that point.

The receiver also has two command bits, similar in use to the transmitter's: Receive Data (RCV DAT) and Receive Word (RCV WD). RCV WD must be set to open the channel. Every time it is set one word will be accepted, causing an interrupt. If RCV DAT is set the entire message would be received before interruption. As in the transmitter, both bits may be set to allow interrupt free reception of the entire message.

3.3.6-3 End of Message

Both receiver and transmitter host computers are informed of a successful completion of transfer of a message by an interrupt from the Successful Transfer (SUC TXF) bit in their respective status registers, Receive Status Register (RSR) and Transmitter Status Register (TSR). Setting of this bit indicates data has moved from the transmitter's Unibus to the receiver's Unibus without error.

3.3.7 Rejection and Truncation

The receiver has the capability of terminating the message before the last word is received from the transmitter. A receiver may reject an entire message after only a few words have been received, or truncate the remainder of the message if it decides it does not want any more data.

3.3.7-1 Rejection

Rejection is an indication by the receiver to the transmitter that the receiver does not wish to receive any of the message being sent. Rejection can only take place before RCV DAT is set. The receiver, after having received one or more data words, may decide, from information contained in these words, or from the identification bits indicating the transmitter's address, that it does not wish to receive the message at all. It could then reject it, if so desired.

Rejection is accomplished by setting the Reject (REJ) bit in the RCR. This will cause the receiver hardware to assert the Reject line on the TDM bus during the next addressed timeslice, as well as returning a Response B = 0 1, a null cycle. After this timeslice the channel open bit in the receiver will be closed and the Reject Complete (REJ COM) bit in the RSR will be set causing an interrupt. The channel open bit in the transmitter will also be cleared, and Software Reject (SORE) set in the TSR. This will interrupt the transmitter's computer to indicate the message was not accepted at all.

3.3.7-2 Truncation

Truncation occurs when the receiver decides that it cannot, or does not wish to, accept any more data from the transmitter. This would occur, for example, if the receiver's memory buffer had been filled, and no other space was available for the rest of the message. The receiver could, at that point, truncate the message. Truncation can only take place after RCV DAT has been set.

Truncation is initiated by setting the REJ bit in the RCR. Truncation is differentiated from rejection by RCV DAT having been set during reception of the message. During the next addressed timeslice, the receiver will respond with a null cycle, as well as asserting the Truncate line on the TDM bus. Both receiver and transmitter data silo's will be cleared, along with the TSBC. Then a CRC check character will be prepared and the channel will be closed in exactly the same manner as in a successful transfer. This means the SUC TXF will be set in both the receiver and transmitter. To differentiate between a regular successful transfer and a truncation the SORE bit will also be asserted in the transmitter, and the REJ COM bit will also be asserted in the receiver.

3.4 PROGRAMMING EXAMPLES

The PCL11-B is an extremely flexible device, and hence it may be programmed in many different ways to achieve communication. The following are simple examples of some of the features of transfers utilizing a PCL11-B. These are examples of communications between two different PCL11-B units over a TDM bus and, as such show two different programs. One is the code in computer A which does the transmitting, the other resides in computer B which is receiving. It is imperative that, in the actual running of these programs, the receiver code be initiated before the transmitter's so that the receiver will be enabled in time for the transmission. In all of the following examples it is assumed that one PCL11-B has been assigned as TDM BUS master (see Section 3.3.2-3).

3.4.1 Transmission of a Single Word

Words may be transferred one at a time using the following code:

COMPUTER A

```
TCR:        164200
TCRH:       164201
TSR:        164202
TSDB:       164204
TSBC:       164206
RCV:                        ; contains Receiver's TDM address
WORD:                       ; contains Word to be sent
START;      MOV#2,@TCR      ; TX INIT
            MOV#-2,@TSBC    ; Load TSBC with 2's complement
                            ; of number of bytes to be sent
            MOV RCV, RO     ; get receiver's address
            BIC 177740, RO  ; Insure valid address
            MOVB RO,@TCRH   ; Load destination
SEND:       MOV WORD,@TSDB  ; Load word to be sent into data
                              silo
            BISB#40,@TCRH   ; Set send word
WAIT:       TSTB@TSR        ; SUC TXF?
            BMI END         ; YES, FINISH
            BIT#100060,@TSR ;NO, IS there an error, or
                            ; is receiver busy
            BEQ WAIT        ; NO, continue waiting
            JMP ERR         ; YES, GO TO ERROR routine
END:        :
            :
ERR:        HALT
```

This will only send one word. If it is desired to send a number of words, one at a time the same program may be used. However, the TSBC should be loaded with the 2's complement of the number of bytes to be sent. In the END routine, SUC TXF should be cleared, WORD loaded with the new word, and then a jump back to SEND executed.

These single words are only checked by parity. If a CRC check for the message is desired, when all words have been sent, SUC TSF should be cleared and ST TXM set. When SUC TXF is set the entire message has been sent and checked.

COMPUTER B

```
RCR:        164220
RSR:        164222
RDDB:       164224
RCVWD:                      ; Received word to be
                            ; placed here.
START:      MOV#2,@RCR      ; RC INIT
RECEIVE:    MOV#20000,@RCR  ; SET RCV WD
WAIT:       BIT#400,@RSR    ; Is data ready on output (DOP RDY
                            ; set
            BNE END         ; YES; FINISHED
            TST@RSR         ; NO; Is there a SUC TXF ?
```

```
            BMI FIN          ; YES, ALL WORDS RECEIVED
            BIT#100040,@RSR  ;NO, Is there an ERR or RECOM
            BEQ WAIT         ; NO, continue waiting
            JMP ERR          ; YES, Go to error routine
END:        MOV@RDDB,@RCVWD  ;Unload word
            :
            :
FIN:        HALT
ERR:        HALT
```

This program will receive only one word. If a number of words are desired to be received in this manner, then in the END routine jump to RECEIVE should be executed after moving the data out of RCVWD. This will continue running until a SUC TXF is detected.

3.4.2 Transmission of a Message

Entire messages may be transferred, using NPR cycles to load and unload the data silos, in the following manner.

COMPUTER A

```
TCR:        164200
TCRH:       164201
TSR:        164202
TSBC:       164206
TSBA:       164210
RCV:                         ; Contains receiver's TDM
                             ; bus address
POINT:                       ; Points to first address
                             ; of data block
NOWDS:                       ; Contains number of words
                             ; to be sent

START:      MOV#2,@TCR       ; TX INIT
            MOV POINT,RO     ; Set first address of block
            BIC#1, RO        ; Ensure an even address
            MOV RO,@TSBA     ; Load TSBA
            MOVE NOWDS,RO    ; Set number of words
            ROL RO           ; Convert to bytes
            BCS ERR          ; Too many words, go to ERR
            NEG RO           ; Get 2's complement of
                             ; byte no.
            MOV RO,@TSBC     ; Load TSBC
            MOV RCV RO       ; Get address of receiver
            BIC 177740       ; Ensure address is valid
            MOVB RO, @TCRH   ; Load TCR with receiver's
                             ; address
            BIS #60001,@TCR; Set TX NPR, SND WD, ST TXM
WAIT:       TSTB@TSR         ; SUC TXF ?
            BMI END          ; YES, Finished
```

```
                BIT#100060,@TSR; NO, is there any unexpected bits?
                BEQ WAIT        ; NO, continue waiting
                JMP ERR         ; YES, go to an error routine
    END:        :
                :
    ERR:        HALT

COMPUTER B

    RCR:        164200
    RSR:        164202
    RDBC:       164206
    RDBA:       164210
    BUFLEN:                     ; Buffer length, in words,
                                ; for storing received data
    BUF ADD:                    ; First address of this buffer

    START:      MOV#2,@RCR      ; RC INIT
                MOV BUFLEN,RO   ; Get buffer length
                ROL RO          ; Convert to bytes
                BCS ERR         ; If length too large; go
                                ; to error routine
                NEG RO          ; Get 2's complement of
                                ; buffer length
                MOV RO,@RDBC    ; Load this into RDBC
                MOV BUFADD,RO   ; Get 1st address of buffer
                BIC#1, RO       ; Ensure that its even
                MOV RO,@RDBA    ; Load this into RDBM
                MOV#60001,@RCR  ; Set RCV WD, RCV DAT, & RC NPR
    WAIT:       TSTR@RSR        ; SUC TXF ?
                BMI END         ; YES, Finished
                BIT#100040,@RSR; NO, Is there any unexpected bits?
                BEQ WAIT        ; NO, Continue waiting
                JMP ERR         ; YES, Go to error routine
    END:        :
                :
    ERR:        HALT
```

3.4.3 Examples of Special Features

3.4.3-1 Rejection and Truncation

The following programs demonstrate one way which a message may be sent using reject and truncate features. The transmitter will preface the message with a word equal to the number of words in the message to be sent. The transmitter will utilize both direct moves and NPR transfers to load its silo.

The receiver will check the ID of the sending device. It will not accept any messages from odd numbered transmitters. The receiver program will truncate any message that overloads its buffer of 2000_8 words. The receiver will also not accept any messages of ten words or less. (Both criteria for rejection are entirely arbitrary.)

COMPUTER A

```
TCR:      164200
TCRH:     164201
TSR:      164202
TSDB:     164209
TSBC:     164206
TSBA:     164210
RCV:                    ; Contains receiver's TDM
                        ; bus address
POINT                   ; Points to first address of
                        ; data block
NOWDS:                  ; Contains number of words
                        ; to be sent.

START:    MOV#2,@TCR    ; TX INIT
          MOV NOWDS,RO  ; Get number of words
          INC RO        ; Increase them by 1 as 1st
                        ; word is to be added to message
          ROL RO        ; Convert to BYTES
          BCS ERR       ; If too many words go to
                        ; error routine
          NEG RO        ; Get 2's complement of bytes
          MOV RO,@TSBC  ; Load TSBC
          MOV NOWDS,@TSDB; Load data buffer with 1st word
          MOV POINT,RO  ; Get 1st address of message
          BIC#1, RO     ; Insure an even address
          MOV RO,@TSBA  ; Load TSBA
          MOV RCV, RO   ; Get receiver address
          BIC#177740,RO ; Insure it is valid
          MOVB RO,@TCRH ; Load TCR with receiver's
                        ; address
          BIS#60001,@TCR ; Set TX NPR, SND WD, ST TXM
WAIT:     BIT@100020,@TSR         ; Is ERR or RCV busy set
          BNE ERR       ; YES, go to error
          BIT#240@TSR   ; NO, Is SUC TXF or SORE set
          BEQ WAIT      ; NO, TRY AGAIN
FINISH:   TSTB@TSR      ; YES, Is SUC TXF set?
          BPL REJECT    ; NO, This is a reject
          BIT#40,@TSR   ; YES, Is SORE set as well
          BEQ SUCTXF    ; NO, This is a regular success
          JMP TRUNC     ; YES, This message has been
                        ; truncated.
REJECT:   :             ; Processor will come here in
                        ; the event of a message reject
TRUNC:    :             ; Processor will come here in
                        ; the event that a message has
                        ; been rejected.
SUCTXF:   :             ; Processor will come here
                        ; in the event of a successful
                        ; transfer.
ERR:      HALT
```

COMPUTER B

```
RCR:      164220
RCRH:     164221
RSR:      164222
RDDB:     164224
RDBC:     164226
RDBA:     164230
BUFLEN:   174000 (-4000) ; Define buffer length as
                         ; 2000 words (4000 BYTES)
BUFADD:   BEGIN          ; BEGIN is an even address

START:    MOV#2,@RCR     ; RC INIT
          MOV BUFLEN,@RDBC;Set up byte count
          MOV BUFADD,@RDBA;Set up bus address
          MOV#20000,@RCR ; Set RCV WD
WAIT1     BIT#400,@RSR   ; Received 1st word
          BNE ACCEPT     ; YES, go to ACCEPT
          BIT#100040     ; NO, Have we got unexpected bits?
          BEQ WAIT1      ; NO, TRY again
          JMP ERR        ; YES, Go to error routine
ACCEPT:   MOV@RDDB, RO   ; Remove word from silo
          CMP RO, #10    ; Less than 10 words in message
          BLE REJ        ; YES, Reject message
          MOV@RCRH, RO   ; Get transmitter ID
          BIC #177776, RO; Clear out all but bit 0
          BNE REJ        ; If old address, reject message
          BIS#40001,@RCR ; Set RCV DAT & RC NPR
WAIT2:    TST@RSR        ; IS ERROR SET
          BMI OVFL       ; YES, FIND OUT IF THERE IS
                         ; an overflow
          TSTB@RSR       ; NO, Is transfer complete
          BMI SUC        ; YES
          BIT#40,@RSR    ; NO, is RECOM set when it
                         ; shouldn't be
          BEQ WAIT2      ; NO, continue
          JMP ERR        ; YES, there's an error
OVFL:     BIT#4000,@RSR  ; Was BC OVF the error
          BEQ ERR        ; NO, a real error
          BIC#4000,@RSR  ; YES, Clear it
          BIS#100001@RCR ; and truncate (note:  must
                         ; set RCV WD again)
WAIT3:    BIT#240,@RSR   ; SUC TXF or RECOM set
          BNE            ; Check if they are both set
          TST@RSR        ; ERR set
          BMI ERR        ; YES; ERR
          JMP WAIT3
CHECK:    CMP#240,@RSR   ; NO; Were SUC TXF & RECOM
                         ; both set
          BNE ERR        ; NO; ERR
          HALT           ; HALT
REJ:      BIS#100000,@RCR; Set Reject
WAIT4:    BIT#100200,@RSR; SUC TXF or ERR set
          BNE ERR        ; YES; error
          BIT#40,@RSR    ; NO; RECOM set
          BEQ WAIT4      ; NO; continue
          HALT           ; YES; Finished
```

3.4.3-2 Use of Address Silo

The following program will load and enable the address silo. It will only run if there are no other masters on the bus. (It will load a 50 word buffer into the silo).

```
TMMR:     164212
TMMRH:    164213
ADBUF:    BEG              ; Start Address of 50 word buffer.
LEN:      62               ; 50 (62₈) word length

START:    MOV#1,@TMMRH     ; Try to set Master
          BIT#1,@TMMRH     ; Did it get set?
          BEQ END          ; NO, another master is on
                           ; the bus
          BISB#60,@TMMR    ; YES, clear silo and set
                           ; AUT ADR
          MOV BEG, R1      ; Put 1st address in R1
          MOV LEN, R0      ; Put NO of words in R0
LOAD:     MOVB (R1),TMMR   ; LOAD Word into silo
          ADD#2, R1        ; Update address
          DEC R0           ; Update no of words remaining
          BEQ LOAD         ; FINISHED?
END:      HALT             ; YES
```

SECTION 4

THEORY OF OPERATION

Introduction

This section is intended to assist in the maintenance of a PCL11-B by discussing the implementation of the PCL11-B operation discussed in Section 3.3. Each functional unit of the block diagram (see Figure 1.2) will be discussed, its physical location in the PCL11-B as well as its diagram location in the prints will be detailed.

All the logic is contained on eight modules; M7991, M7992, M7993, M7994, M7995, M7996, M7997 and M8003. Each of these modules has its own schematic and will be referred to in the following format: nPm, (n=mod number, Pm=page number of schematics).

4.1 MASTER SECTION

This section is found on M7994. Its purpose is to provide the transmitter address and the two time phase signals TP 0 and TP 1. This section has one register associated with it, the Transmitter Master/Maintenance Register - TMMR). The high byte of this register contains control and status bits while the low byte is the address silo. A clock section runs the address counter and the cycling of the address silo as dictated by the high byte of the TMMR. Figure 4.1 Outlines the timing signals used in the address generation section.

4.1.1 Clock

The clock is a pair of 74123 one shots (CLKA, CLKB 4P3-D/4) which are triggered whenever MASTER is set. The period of the clock may be adjusted by changing the time constant of CLKA (74123) with the potentiometer R20 located near the handle of M7994.

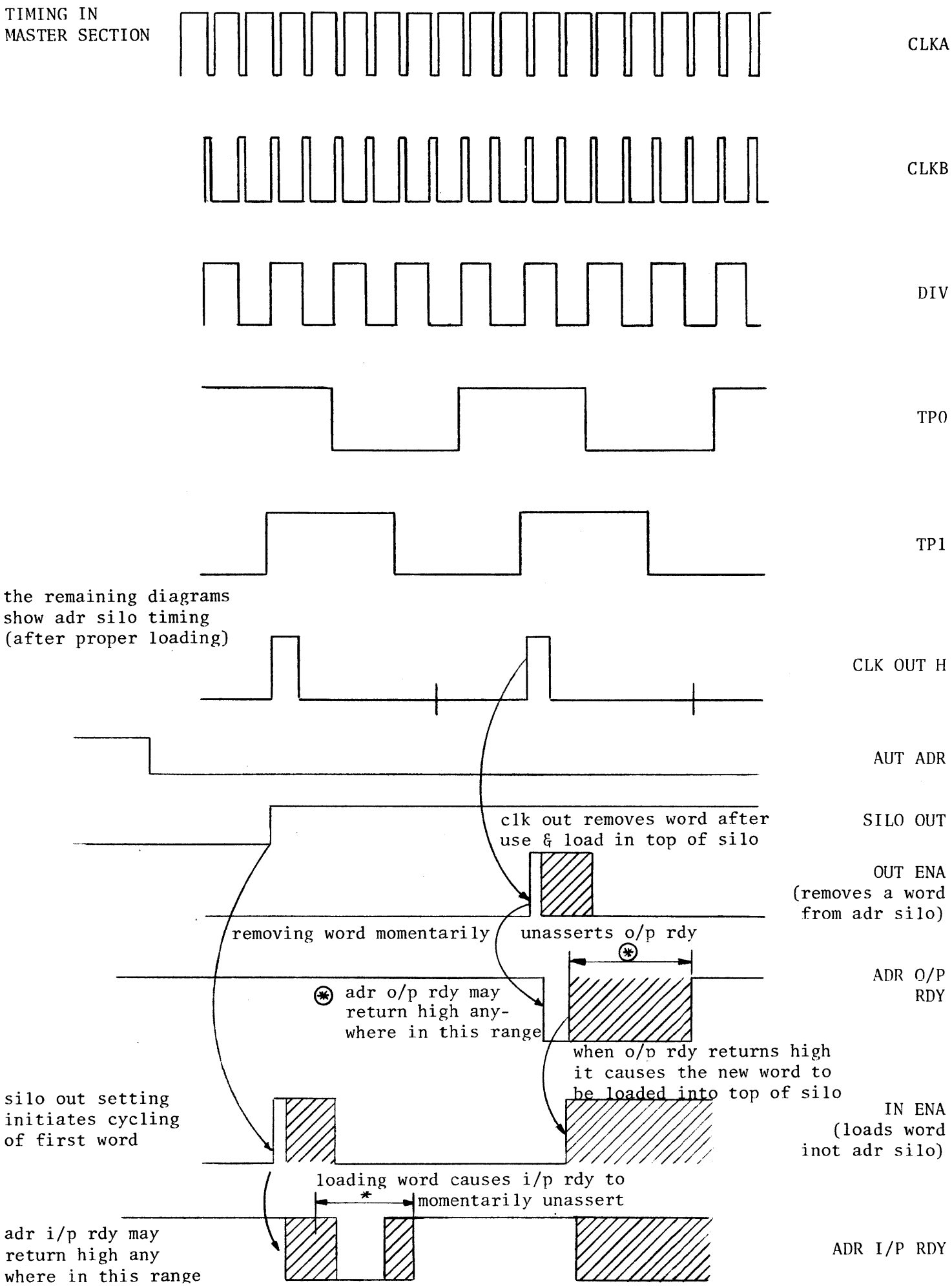
4.1.2 Time Phase Generator

The frequency of the wave form at CLKB is divided by two by the DIV flip-flop (4P3) whose output clocks the flip-flop TP 0 and TP 1 (4P3). The two flip-flops produce square waves, 90 degrees out of phase, at four times the period of the output of DIV. These square waves are the time phase signals and are driven on the TDM bus (4P5 - C/6) whenever MASTER is set.

4.1.3 Transmitter Address Generation - 5 Bit Decrementing Counter

The 5 bit decrementing counter (E40 counter & E46 flip-flop 4P3 C,B/3) is clocked by the trailing edge of TP 0, as at this time both transmitter and receiver have no use for this address until the next leading edge of TP 0. E52 (flip-flop 4P3

FIG 4.1


TIMING IN MASTER SECTION
CLKA
CLKB
DIV
TP0
TP1
the remaining diagrams show adr silo timing (after proper loading)
CLK OUT H
AUT ADR
SILO OUT
clk out removes word after use & load in top of silo
OUT ENA (removes a word from adr silo)
removing word momentarily
unasserts o/p rdy
ADR O/P RDY
adr o/p rdy may return high anywhere in this range
when o/p rdy returns high it causes the new word to be loaded into top of silo
silo out setting initiates cycling of first word
IN ENA (loads word inot adr silo)
loading word causes i/p rdy to momentarily unassert
* adr i/p rdy may return high any where in this range
ADR I/P RDY

D/3) will provide a load pulse whenever the top four bits of the counter are zero. This ensures the number in the whole 5 bit counter (E56 flip-flop is the least significant bit) is never less than one. The counter is loaded with the number contained in S1. The output of the counter and of the address silo (TXM ADR 00H to TXM ADR 04H - 4P3 A/1) are multiplexed into the 5 transmitter address lines (T TA 00 OUT H to T TA 04 OUT H 4P3 C,B/2). These lines will drive the TDM bus if MASTER is set (4P5 - B/6).

4.1.4 Transmitter Address Generation - Address Silo

The address silo is the two FIFO chips shown on 4P3 (3341 A,B/6). The silo is either loaded with data from the Unibus, or data from the output of the silo, this being switched by the multiplexers E33, E34 (74157 4P3 A,B/7). When the silo is cycling, the data on the output is loaded. A word is loaded into the silo whenever the IN ENA (4P4 C/4) flip-flop is set, and a word is removed whenever OUT ENA (4P4 C/4) flip-flop is set. When cycling, a word is removed from the silo at the first CLKB pulse to occur after both TP 0 and TP 1 are set. A new word will fall into place in time for the next time slice. As soon as this new word is ready, it is loaded into the top of the silo.

The silo is loaded from the Unibus by setting IN ENA and a word removed onto the Unibus by setting OUT ENA. The two integrating one shots on 4P4 are used to determine if there is any data in the silo.

4.1.5 TMMR High Byte

The high byte of the TMMR contains the control and status bits to run the logic just described, Bits 14 and 15; AIP (Address Input Ready) and AOP (Address Output Ready) indicate whether the address silo is ready to accept a word or has a word ready on its output, and come from ADR I/P RDY and ADR O/P RDY (4P3 C/1).

Bit 13 - CLR ADR - will assert CLR ADR SILO L at 4P3 B/3. Bit 12 - AUT ADR (4P3 B/2) will dictate whether the address silo will cycle and be put out on the T TA OUT lines (4P3 B,C/1). This flip-flop will be set if the address silo is empty.

Bits 8 and 9 - MASTER and SEC - are found in the flip-flop by the same name (4P3 C/6). These can be set or cleared from the Unibus as well as from switches which may be externally connected.

4.1.6 TDM BUS TTL Transceivers

On 4P5 the transceiver chips for the TTL TDM bus are located. These receive and drive all TDM bus signals save the data lines - these are driven from 1P6.

4.1.7 Other Functions on M7994 - Unibus Receivers, Address Decode

Also contained on the M7994 module are the Unibus receivers (4P1). All Unibus signals are received here so as not to present more than one load to this bus. On 4P2, are the receiver and transmitter Unibus address jumpers. This logic will produce a select signal (TXM SEL L (4P2 C/5) or RCV SEL L (4P2 C/1)) whenever the PCL11-B is addressed; leaving the transmitter or receiver sections to select the individual register, and return SSYN.

4.2 TRANSMITTER SECTION

The transmitter section physically resides in three modules; the M7991 contains the transmitter address decode, TDM bus transmit control. The M7992 contains the address decode, the Load Silo control, CRC Generation logic, and Interrupt Control. The M7993 contains the TSBA, TSBC registers, the data silo, and Unibus data drives.

4.2.1 Address Decode

The address decode logic is found on 2P5. TXM SEL L (Source on 4P5 - on 2P5 at C/8) is asserted whenever MSYN, and Unibus address bits 13 through 17 are asserted and bits 4 through 12 correspond to the transmitter address. TXM SEL L, along with Unibus address bits 1, 2 and 3 (these having been received on M7994 become BA01H, BA02H, BA03H), enter a 7442 (one of 10 decode chip 2P5 C/7) and produce SEL 0 through SEL 12 pulses. The Unibus C bits and address bit 0 are used to derive the OUT HIGH L and OUT LOW L (2P5 - B/7) which are combined with the SEL signals to produce the LOAD pulses - one for the high byte and one for the low byte for each register. Also produced is the signal IN L (2P5 - B/3) which is asserted whenever data is being read from the transmitter registers.

4.2.2 Interrupt Control

This section is found on 2P1. Whenever a condition occurs which should cause an interrupt, INTR REQ H (Source: 1P4 - 2P1 A/5) is asserted. If the interrupt enable bit is set (Source 3P2 2P1 - A/5) then this section will make a Bus Request and perform an interrupt cycle. The level at which the PCL11-B makes this request is determined by the priority plug on 2P2 - C/7. Both the receiver and transmitter sections interrupt on this level, with the transmitter always being closer to the processor. All grant signal enter the transmitter, are passed to the receiver, then continued on the Unibus.

When this section executes an interrupt cycles, first BR L (2P1 D/1) is asserted. When acknowledged with a grant, SACK2 (2P1 C/2) is set until control of the bus is gained, at which time SACK2 is cleared and BBSY2 is set (2P1 B/2). When BBSY is set, BUS BUSY and INTERRUPT are asserted on the Unibus. As well, data lines 4 through 8 (3P3 and 3P4) are driven according to the jumpers W1 through W5. (IN for a 0, OUT for a 1). This provides the device vector.

4.2.3 Load Data Silo Control

The data on the Unibus will be loaded into the data silo whenever STB IN (2P5 A/2) is set. STB IN can only be set if the silo is ready to accept a word (DATA I/P RDY L is asserted). This flip-flop may be set in one of two ways, depending on the state of the TX NPR (3P2 A/7) bit. If TX NPR is clear, the STB IN flip flop will be set if OUT HIGH or OUT LOW and SEL 4 are asserted. (No byte transfers of data are allowed in PCL11-B). This means all moves to the TSDB will load the source data into the silo.

If TX NPR is set then logic on 2P1, 2P2 and 2P3 will perform a NPR cycle to retrieve the data and load it into the silo. However, before this cycle may occur the Load Data Silo Control will wait until the silo can accept a word, there are no errors, and the byte count register has been loaded. (The latter is determined by TSBC BUSY 2P3 - C/3) which is set when the TSBC is loaded, and cleared when it overflows). GET BUS (2P1 B/2) will set if all these conditions are met when TX NPR is set, and will cause a NPR to be made on the Unibus (2P1 D/7). (E35 - the 74123 2P3 B/6 is used only to provide a suitable clock pulse for GET BUS on multiple NPR cycles). The NPR circuitry on 2P1 operates similar to that of the interrupt circuitry on the same page. When BBSY1 is asserted, so is the Unibus BUS BUSY and at the same time the NPR cycle timing control on 2P2 is initiated. This logic will provide the enable signal to drive the 18 Unibus Address Lines, (3P1 and 2P3 - A/4), and Unibus MSYN. When and if SSYN is returned, DATA STROBE L (2P2 D/1) will be asserted, causing STB IN (2P5 A/2) to set, loading the data into the silo. If SSYN is not returned within 20 usecs, NXL (2P2 A/6) will set and the cycle will be aborted. At the end of the NPR cycle END CYCLE will be asserted which clears GET BUS, giving up the bus and incrementing the TSBA if INHIBIT ADDRESS INCREMENT is clear.

4.2.4 CRC and Parity Generation

The logic which controls and produces the parity and CRC checks is scattered over the 3 transmitter modules.

The actual CRC character is generated in the logic shown on 2P4. The 7486 XOR gates perform the division by the selected polynomial. The division is performed on the data to be sent out onto the TDM bus (TD00 - TD15) by exclusive OR'ing it with existing character. The result is stored in the 16 bit register shown on 2P4.

Since the CRC check character is sent out on the TDM bus data lines it must be multiplexed with the output of the data silo. This implementation is shown on 3P2 (E32, E25, E52, E54 - 74157).

The signals which control this circuitry come from M7991 - 1P2. Every time OUT RDY L (Source 3P2 - 1P2 D/8) becomes asserted, indicating a new word is at the output of the silo, the counter is incremented (pair of 74161 1P2 B,C/7) and a 200 ms one shot is triggered (E45 - 1P2 - B/5). This delay is to allow the new data to filter through all the gating on 2P4. At the trailing edge of this one shot, a second one is triggered upon which the new CRC character is loaded and CRC RDY (1P2 B/3) is set. Note that a word is not considered ready on the output of the Silo until this flip-flop is set.

Whenever the counter has determined that 200_8 words have been run through the CRC circuitry a CRC check character will be prepared. INH DATA L (1P2 - C/1) will be asserted, forcing TD00 through TD15 to be zero. (DE SEL L (1P2 - C/1) will be asserted until CRC RDY is set causing the output of the 74157 on 3P2 to output zeros). After the check character is prepared the 74157's on 3P2 will output C00 to C15 on the TDM bus. Once the check character has been accepted CRC ACCD (1P2 B/2) will set clearing the counter and CRC register. The same sequence will occur when the TDM BUS TRANSMIT CONTROL asserts LAST WORD (1)H (Source 1P4; 1P2 D/8).

Every word that is sent out on the TDM bus is accompanied by an odd parity bit generated by the two 74180 parity chips on M7993 (3P2 C,B/1).

4.2.5 Transmitter Source Bus address Register

This register contains the address of the location which the next NPR cycle will retrieve data from. It is shown on 3P1 (E15, E17, E43, E45). The TSBA is loaded from the Unibus with load pulses generated from the Address Decode section (LOAD TSBA LOW L, LOAD TSBA HIGH L). It will drive the Unibus address lines when it receives the correct signal from the Load Data Silo Control (TSBA TO A BUS L) and will be incremented twice after the NPR cycle, if the Load Data Silo Control asserts a CLK TSBA H pulse.

4.2.6 Transmitter Source Byte Count Register

This register data is incremented twice every time a word is loaded into the silo. It is normally loaded with the 2's complement of the number of bytes to be transferred over the TDM bus. The TSBC will overflow when all words to be transferred have been loaded into the silo. The TSBC is located on 3P1 (E16, E18, E44, E46) and is loaded from the Unibus with signals from the address decode section (LOAD TSBC LOW L, LOAD TSBC HIGH L). It will be incremented when the silo is loaded with a STB IN (1) H signal from the Load Data Silo Control section.

4.2.7 64 Word by 16 Bit Data Silo

The data silo is the heart of the transmitter section, it provides the syncronization necessary between the two separate buses - the TDM bus and the Unibus. Because data may be strobed in and out at different rates the Load Data Silo Control may load the silo with a word whenever there is space, while at the same time the TDM Bus Transmitter Control may be unloading words at the rate at which the receiver can take them.

The data silo consists of four 4 bit by 64 word FIFO chip (3341 - 3P2 E26, E33, E53, E55). These chips will assert OUT RDY L (3P2 - A4) when there is a 16 bit word ready on their output and DATA I/P RDY (3P2 - A/4) when the silo is ready to accept a word.

4.2.8 Unibus Data Drivers/Mux

Located on M7993 are 16 74151 (16:1 MUX) chips with 16 Unibus data drivers. This section uses IN L, generated in the Address Decode section whenever data is being read from the transmitter section, as well as Unibus address bits to select the correct register. All data which is to be read is brought to these MUX's (3P3, 3P4) where it is channelled onto the Unibus when required.

4.2.9 TXM Address Decode

The transmitter decodes its own timeslice by continually comparing the TDM bus transmitter address lines with the address set up in S1. If, on the leading edge of TP 0, the comparison of the address lines and switch is true and a channel is opened or FIRST L is asserted (this indicates all conditions are true for the transmission of the first word 1P1 - B/5) then TIMSL (1P1 B/3) will set. When TIMSL sets the TDM Bus Transmit Control will use the remaining timeslice to try and transmit a word or CRC.

4.2.10 TDM Bus Transmit Control

When TIMSL sets, RSP A 0 and RSP A 1 will be clocked. Depending on the state of the transmitter one of three responses will be loaded into these flip-flops to be sent to the receiver. The state is determined by the logic in D,C/5, 8 on 1P1. The RSP A flip-flops will not be clocked if there is an error so that the responses will be frozen in the error conditions.

TIMSL will be cleared by the trailing edge of TP 1 (see E57, E56 A/5,4 1P1). This will assert CLK RSP B H (1P4 - C/7) if there are no errors. At this time the transmitter is looking at the receiver's response back to the transmitter indicating what was done during the timeslice. A number of flip-flops will be clocked and will set or clear depending on the value of the TDM bus RSP B lines at this time:

i) RSP B 1 and RSP B 0 (1P4 B,C/6) will be clocked storing the RSP B received during the current timeslice. This data may be utilized by software in the event of an error.

ii) TDM BUS BUSY (1P4 - C/3) will be set if RSP B 0 and RSP B 1 are both zero (RCV OFFLINE) on the first word being sent.

iii) TXM ERR (1P4 B/3) will set if the responses indicate an error condition.

iv) STB OUT (1P4 C/3) will set if the responses indicate the receiver has accepted a valid word. (This flip-flop may also be set by RD WD which may be set in a maintenance situation to read a word from the silo, then strobe it out). CHAN OPEN (1P3 B/6) will set whenever STD OUT is set as a channel is considered open whenever a word is sent from the transmitter to the receiver.

v) SORE (1P3 D/6) will set if the TDM bus reject line is asserted at this time. This will clear the channel by setting CLR CHAN (1P3 C/2) and request an interrupt.

vi) TRUNCATE (1P3 C/6) will set if the TDM bus truncate line is asserted. This will clear BC BUSY (2P3 C/3) and the data silo and then close the channel in the normal way, except END TXM will set SORE.

In the event of an error FRZRO (1P3 B/3) will be set, to send a RSP A of 00 to the receiver, at the beginning of the timeslice. CLR CHAN (1P3 B/2) will set at the end of the same timeslice to close the channel and allow the error to interrupt the processor. Exceptions to this are OFF LINE and CHECK FAIL errors which will set CLR CHAN the same timeslice which they occur in.

The logic determines that no more words are to be sent when the silo is empty (SILO LOADED H is asserted) and the byte count register is empty (TSBC LOADED is clear). When this situation occurs LAST WORD (1P4 D/7) is set. This will cause the final CRC character to be generated (see 4.2.3) and sent to the receiver. When this character is checked WAIT will be set (1P4 D/6). The next time a RSP B of 00 is received END TXM (1P4 D/5) will be set which will close the channel and set SUC TXF (1P1 C/2).

4.2.11 Other functions on M7991 - TDM BUS TTL Transceivers (DATA)

Also to be found on the M7991 are the TDM bus TTL transceivers (1P6) as well as an active terminator (1P5). This "terminator" will, when this unit is TDM bus MASTER, insure the important TDM bus control lines are forced to zero after each timeslice. If this were not done then the high impedence of the line, if no drivers are running it, may cause a control or address line to remain in the one state long enough to cause an error in the succeeding timeslice.

4.2.12 Transmitter Command Register and Transmitter Status Register

Since these registers were described in detail in section 3.1 only these bit's location in the print set will be given:

BIT	TCR NAME	LOCATION	TSR NAME	LOCATION
0	ST TXM	1P1 B/2	RSP A 0	1P1 D/4
1	TX INIT	2P5 D/1	RSP A 1	1P1 C/4
2	INH ADR INC	3P2 D/7	RSP B 0	1P4 C/6
3	DAT O/P RDY	1P2 D/1	RSP B 1	1P4 B/6
4	EA 16	1P4 B/7	TDM BUS BUSY	1P4 C/3
5	EA 17	1P4 B/7	SORE	1P3 D/6
6	IE	3P2 C/7	BUSY	1P1 C/5
7	RD SILO	3P2 C/7	SUC TXF	1P1 B/3
8	DC 00	3P2 B/7	DAT I/P RDY	2P5 A/2
9	DC 01	3P2 B/7	OVERRUN	1P3 A,B/4
10	DC 02	3P2 B/7	TIME OUT	1P3 B/6
11	DC 03	3P2 B/7	MST DWN	1P3 C/6
12	DC 04	3P2 B/7	TXM ERR	1P4 B/3
13	SND WD	1P1 A/3,4	MEM OFL	2P3 D/6
14	TX NPR	3P2 /A/6	NXL	2P2 A/6
15	RIB	3P2 A/7	ERR	1P3 B/2

4.3 RECEIVER SECTION

The receive section is also located on 3 modules; the M7995 contains the RDBC, RDBA registers, the data silo, and Unibus data drivers. The M7996 module contains the address decode, data silo to Unibus control, parity check and interrupt control. The last module, M7997, contains the CRC check logic, TDM bus Receive Control and RCV/TXM address decode.

Much of the logic in the receive section, especially that which interfaces to the Unibus, is similar to logic in the transmitter. In this case references to the description of the appropriate transmitter section will be made as opposed to redescribing the logic.

4.3.1 Address Decode

The address decode logic is found on 6P4. This logic operates similar to that in the Transmitter Address Decode section (4.2.1). RCV SEL L (Source 4P2 - on 6P4 D/8) is asserted whenever Unibus Address bits 4 through 17 equal the receivers Unibus addresses and MSYN is asserted. This signal, along with the C bits, Unibus address bits 0 through 3, produces a load pulse for each byte of each register (except RDDB which is word oriented) and IN L. SSYN is asserted on the Unibus after a suitable delay.

4.3.2 Interrupt Control

This logic is found on 6P1. When a condition occurs which should cause an interrupt INTR REQ H (Source 6P3 - 6P1 A/5) is asserted. If IE is set (Source 5P2 6P1 A/5) an interrupt cycle is executed in the same manner as in the transmitter interrupt control (4.2.2). However the receiver interrupt control will receive its bus grant from the transmitter interrupt control and then pass it on to the Unibus - meaning the receiver always has lower priority than the transmitter and its BR level is determined by the priority plug on 2P2 C/7. When BBSY4 is set, the Unibus data lines (2 to 8) will be driven with the receive vector determined by the jumpers W1 to W7 (see 5P3 A/3 and 5P4 A-D/6 and C,D/3).

4.3.3 Data Silo to Unibus Control

Any word which is on the output of the data silo may be removed by setting STB OUT (6P4 C/2). In order to read a word from the data silo, the data must be put out onto the Unibus and after this data has been read STB OUT must be set. This will remove the word and allow a new one to fall into its place. Which of the two ways is utilized is determined by the state of the RC NPR flip-flop (5P2 D/7).

If RC NPR is clear, then at the trailing edge of IN L and SEL 4, WASRD will be set (6P4 C/3). (This indicates the RDDB was just read.) This will set STB OUT, removing the word.

If RC NPR is set, when any word is ready on the output of the data silo (DAT O/P RDY H - see 6P3 D/4 - is asserted), there is something in the byte count register (RDBC BUSY - 6P3 C/3 - is set) and there are no errors (ERR L - see 6P3 D/4 - is not asserted) then the Data Silo to Unibus Control will perform a NPR cycle, then set STB OUT.

This operation is very similar to that of the transmitter's Load Data Silo Control operation (4.2.3). REQ BUS (6P3 D/2) will be set which will trigger the logic on 6P2 (D/7) to become Unibus Master via a NPR request. When this happens (BBSY3 - 6P1 B/5 - sets) the logic on 6P2 is triggered to produce the timing for the cycle (BUST - 6P2 C/6 - sets). This logic will output a signal to the RDBA to assert the destination address on the Unibus address lines, assert MSYN and C1 on the Unibus as well as the Unibus data lines (with the output of the data silo). If no SSYN is received within 20 usecs NXL will set (6P2 A/3) and the cycle aborted. At the end of the cycle END CYCLE (6P2 D/6) will be set to give up Unibus Mastership and increment the RDBC and RDBA (if INHIBIT ADDRESS INCREMENT is not set). At this time STB OUT will be set removing the transferred word from the data silo.

4.3.4 Other Functions on M7996

Normally the data silo is loaded with data received from the transmitter over the TDM bus. However, in a maintenance mode the data may be loaded from the Unibus. Four multiplexers (E17, E21, E29, E25 on 6P3) will switch the correct data into the silo depending on the state of LD SILO (5P2).

4.3.5 Receiver Destination Bus Address Register (RDBA)

This register (E18 - E21 on 5P1) contains the address to which the silo output will be sent on the next NPR cycle. It is loaded with data from the Unibus when the address decode section asserts the correct pulse (LOAD RDBA LOW L - see 5P1 A/8 or LOAD RDBA HIGH L - see 5P1 C/3,4) and will drive the Unibus address lines when the Data Silo to Unibus Control asserts the correct pulse (RDBA TO A BUS L). It will be incremented twice with the correct pulse from the Data Silo to Unibus Control (CLK RDBA see 5P1 B/8).

4.3.6 Transmitter Destination Byte Count Register (RDBC)

This register (E22 to E25) is loaded with the 2's complement of the number of bytes of the buffer area for received data. It is loaded with data from the Unibus when the address decode section asserts the correct pulse (LOAD RDBC LOW L - see 5P1 C/8 or LOAD RDBC HIGH L - see 5P1 C/3,4). It will be incremented twice when the correct pulse is received from the Data Silo to Unibus Control (END CYCLE (1) H - see 5P1 C/8). If this register overflows (RDBC OFL L - 5P1 D/1 - is asserted) and there are still more words to be removed from the data silo with NPR cycles (RC NPR - 5P2 - and DAT O/P RDY- 5P2 both set) then BC OFL (6P3 C/4) will set.

4.3.7 64 Word by 16 Bit Data Silo

The receive section data silo performs a similar function to the transmit section's silo (see 4.2.7). It is shown on 5P2 as four 3341 FIFO chips (E42 - E45). These chips will assert DAT O/P RDY H (5P2 C/1) whenever a 16 bit word is ready on the output of the silo and DAT I/P RDY (5P2 A/2) whenever the FIFO's are ready to accept a new 16 bit word on their input.

4.3.8 Unibus Data Drivers/Mux

Also located on M7995 are 16 74151 (16:1 MUX) chips with 16 Unibus data drivers. When IN L is generated by the Address Decode section, this section of logic (5P3, 5P4) will use Unibus Address bits 1, 2 and 3 to select one register to drive the Unibus data lines. All data which is to be read is brought to the input of these MUX's to be switched onto the Unibus at the correct time.

4.3.9 CRC and Parity Check

The receive section calculates its own CRC character, to be checked against the transmitter's, on 7P4. The character is stored in the 16 bit register (E58 - E60 7P4). The new character is formed from the existing character and the data being loaded into the data silo. The new character is formed when the TDM BUS Receive Control asserts STB DATA (7P3 B/5) which will assert CLK CRC H (7P3 B/2). At the same time a counter will be incremented (E39, E43 (2) 74161 on 7P3 C,B/2,3) which will assert BLK H (7P3 C/2) when 200_8 words have been loaded, which in turn will assert CRC H (7P2 B/3) indicating the next data received will be a CRC check character. When the check character is transmitted STB CHK H (7P3 5/B) will go low which asserts CLK CRC H to load the check character (in the same manner as a data word) into the CRC register. After this is done the CRC register will be zero if no errors are detected. At the end of the timeslice STB CHK H will be asserted clocking CRC GOOD (7P2 B/7) and CRC ERR (7P2 A/7). The former will set if no errors are detected, the latter will set if the CRC register is non-zero, indicating problems.

Parity is checked on M7996. At the same time as the CRC register is loaded, PAR (6P3 C/1) is clocked. If there is a difference in the TDM bus Parity line - which is the parity calculated by the transmitter - and the output of the two 74180 parity chips (E22, E30 6P3 A,B/2) - which is the parity calculated on the received data - PAR sets, indicating an error.

4.3.10 RCV/TXM Address Decode

The receiver monitors the TDM bus receiver address lines to determine if it has been addressed by a transmitter. This occurs on 7P1 - SEL RCV H (7P1 A/4) is asserted whenever the address lines are the same as the Receiver Address contained in S1 on M7997. If the receiver has not received any words of a message, and has been set up to open a channel, FIRST L (7P1 B/4) will be asserted when SEL RCV H is true. At the leading edge of TP 1, BD ADR (7P2 C/6) will be clocked. If it sets the receiver will respond to the transmitter during the timeslice. BD ADR will set if FIRST L is asserted and it will always be cleared on the leading edge of TP 0. At the same time a five bit register will be loaded with the address of the transmitter whose timeslice it is (7P1 - E38 - C/2).

On succeeding addresses of the receiver it is not sufficient that SEL RCV H is asserted. After the channel is opened the transmitter address lines must compare to the Identification bits before BD ADR is set (see E37 7P2 C/7).

4.3.11 TDM Bus Receive Control

When BD ADR sets, RSP A 0 (7P2 C/5) and RSP A 1 (7P2 B/5) will be clocked, if there are no errors, storing the RSP A sent over by the transmitter. This data may be utilized by software in the event of an error.

At the same time ACCEPT (7P2 D/4) will be clocked. This flip-flop will set if the receiver is transferring a valid word which the receive section is prepared to accept.

Once BD ADR has been set, STROBE H (7P2 C/5) will be asserted on the trailing edge of TP 0. When this is asserted RSP B 0 (7P2 B/5) and RSP B 1 (7P2 A/5) will be clocked. They will set up the receiver's response to the transmitter for the timeslice.

STROBE H will also clock STB DATA (7P3 C/5) which will set if ACCEPT has been set. STB DATA, when set, will load a word into the data silo. STB DATA may be set in a maintenance mode if the proper clock pulse is received from the address decode section (LOAD FIFO L) and LD SILO (5P2) is set.

On the trailing edge of STROBE H, TXM ERR (7P2 C/3) will be clocked. This flip-flop will set if any errors in communication have occurred at this time.

In the event of an error, and after the last CRC has been acknowledged a RSP B = 0 must be sent to the transmitter. FF (7P2 B/3) will set after the timeslice in which the last CRC was acknowledged (RSP A = 11; RSP B = 11) asserting FR RSP 00 H (7P2 B/2) insuring a RSP B = 00 is put out. FR RSP 00 H will also be asserted if an error condition has arisen. The next timeslice FF will be cleared - triggering END TXM (7P2 B/1) which sets SUC TXF (7P3 D/5) and clears CHAN OPEN (7P1 B/6). If an error condition exists ENA ERR will set, allowing an interrupt and clearing CHN OPN. (ENA ERR will also set right after returning a RSP B = 00 or 10 or receiving a RSP A = 00. TIME OUT (see 7P2 A/3) will not wait for any more timeslices, but causes an immediate interrupt request.

When REJ (7P1 C/7) is set, at the beginning of the next timeslice either TRUN MESS (7P1 C/6) or REJ MESS (7P1 B/6) will be set, depending on whether RCV DAT (7P1 B/7) has been set. If REJ MESS is set (RCV DAT not been set this message) the Reject line is asserted on the TDM bus and REJ COM (7P1 C/3) is set after the timeslice, closing the channel. If TRUN MESS is set, (RCV DAT has been set this message) the silo is cleared and the normal channel closing procedure followed, except REJ COM is set by END TXM.

4.3.12 Receiver Command Register and Receiver Status Register

Since these registers were described in detail in section 3.3 only these bits' location in the print set will be given.

BIT	RCR NAME	LOCATION	RSR NAME	LOCATION
0	RCV DAT	7P1 B/8	RSP A 0	7P2 C/5
1	RC INIT	6P4 B/3	RSP A 1	7P2 B/5
2	INH ADR INC	5P2 B/6	RSP B 0	7P2 B/5
3	DAT I/P RDY	5P2 A/2	RSP B 1	7P2 A/5
4	EA 16	6P3 C/5	CHAN OPEN	7P1 B/6
5	EA 17	6P3 C/5	REJ COM	7P1 C/3
6	IE	5P2 B/6	BUSY	7P1 D/3
7	LD SILO	5P2 B/6	SUC TXF	7P3 D/5
8	IB 00	7P1 B/1	DAT O/P RDY	5P2 C/1
9	IB 01	7P1 B/1	BC OFL	6P3 C/4
10	ID 02	7P1 C/1	TIME OUT	7P3 D/2
11	IB 03	7P1 C/1	PAR	6P3 C/1
12	IB 04	7P1 C/1	TXM ERR	7P2 C/3
13	RCV WORD	7P1 D/6	MEM OFL	6P3 B/4
14	RC NPR	5P2 D/6	NXL	6P2 A/3
15	REJ	7P1 C/7	ERR	7P3 A/3

4.4 TDM BUS DIFFERENTIAL BUS

Transceiver chips contained on modules M7991 and M7994 are tristate TTL drivers and receivers. They form a TTL TDM bus. (This is the actual TDM bus used in PCL11-A communication system.) PCL11-B units have a differential TDM bus which is driven from the M8003 module. This module is connected to the TTL TDM bus and the Differential TDM bus and drives one bus with signals from the other, as required. In the prints, all TTL-TDM bus signals are prefaced by the designation "T-BUS" and all Differential TDM bus signals are prefaced by "TDM BUS".

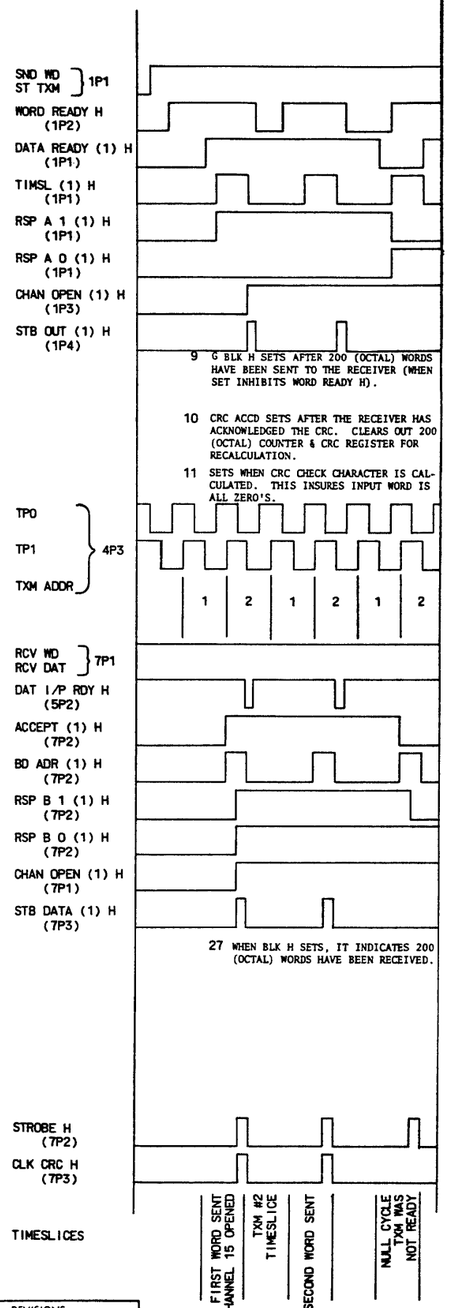
The transceiver chips consist of tristate differential drivers and receivers. When the PCL11-B is not Master, does not have a timeslice, and is not being addressed by a transmitter all these differential drivers are disabled and the receivers are enabled, driving the TTL TDM bus with differential data. If the receiver is addressed, during the time which BD ADR (7P2 C/6) is set, the differential transmitters for the RSP B, REJ and TRUNC lines are enabled and the differential receivers are disabled (8P1). Similarly, when TIMSL (1P1 B/3) sets, the differential transmitter for the DATA, PAR, RSP A and RCV ADR lines are enabled and their differential receivers are disabled (8P2, 8P3, 8P4). Finally, if MASTER (4P3 C/6) sets, the differential transmitters for TRANS ADR, TP 0, TP 1 and MASTER ACTIVE will be asserted and their differential receivers disabled (8P5). There is a disable switch (8P1 C/4) which when turned on will disable both differential receivers and drivers. To enable, switch must be pushed up towards cable connectors.

4.5 TIMING DIAGRAMS

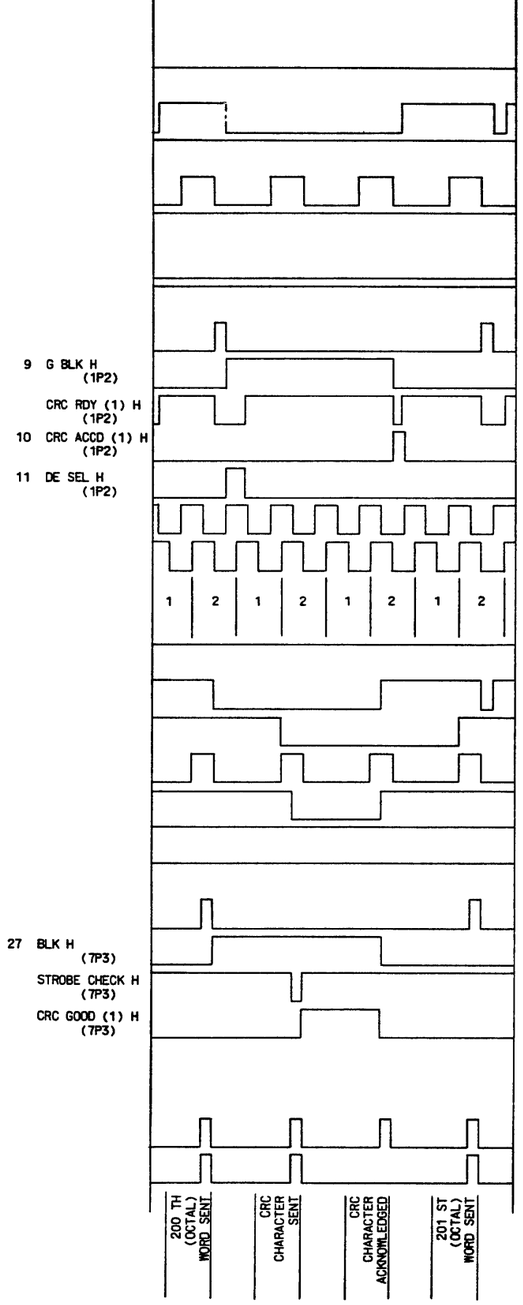
The following pages show timing diagrams for the transfer of data on the TDM Bus. The first shows the signals for a normal transfer of message of more than 200_8 words. All signals are described on the left and reference to the prints is made. The next page shows the signals in the event of an error as well as the timing required to load or unload a data word from the data silo.

OPENING THE CHANNEL

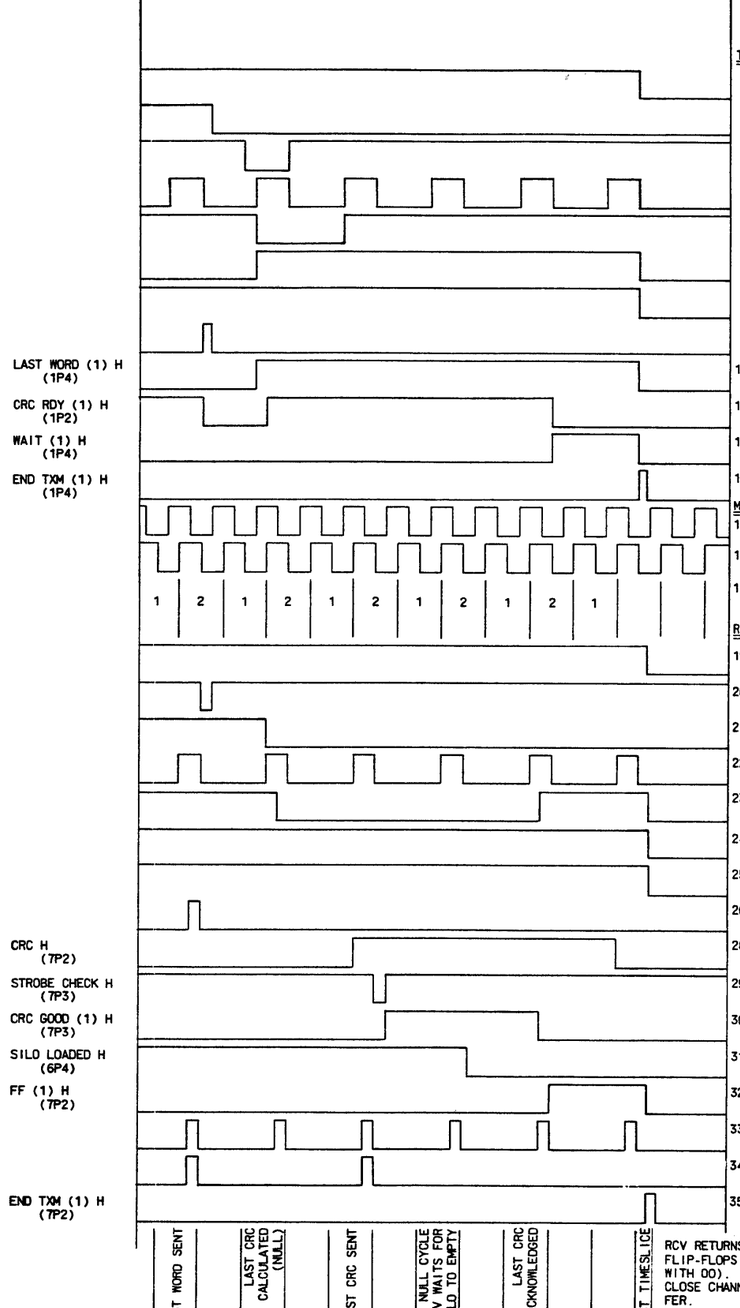
TRANSMISSION OF FIRST TWO WORDS



CRC CHECKING AFTER 200 (OCTAL) WORDS



FINAL CRC CHECK AND CHANNEL CLOSING



RCV RETURNS A RSP B = 00 (EVEN THOUGH FLIP-FLOPS SHOW 11 TDM BUS IS DRIVEN WITH 00). AFTER THIS BOTH RCV & TXM CLOSE CHANNEL AND SET SUCCESSFUL TRANSFER.

TRANSMITTER SIGNALS

1 SND WD / ST TXM } 1P1
2 WORD READY H (1P2)
3 DATA READY (1) H (1P1)
4 TIMSL (1) H (1P1)
5 RSP A 1 (1) H (1P1)
6 RSP A 0 (1) H (1P1)
7 CHAN OPEN (1) H (1P3)
8 STB OUT (1) H (1P4)
12 LAST WORD (1) H (1P4)
13 RCR RDY (1) H (1P2)
14 WAIT (1) H (1P4)
15 END TXM (1) (1P4)

MASTER SIGNALS

16 TP0
17 TP1 } 4P3
18 TXM ADDR

RECEIVER SIGNALS

19 RCV WD / RCV DAT } 7P1
20 DAT I/P RDY H (5P2)
21 ACCEPT (1) H (7P2)
22 BD ADR (1) H (7P2)
23 RSP B 1 (1) H (7P2)
24 RSP B 0 (1) H (7P2)
25 CHAN OPEN (1) H (7P1)
26 STB DATA (1) H (7P3)
28 CRC H (7P2)
29 STROBE CHECK H (7P3)
30 CRC GOOD (1) H (7P3)
31 SILO LOADED H (6P4)
32 FF (1) H (7P2)
33 STROBE H (7P2)
34 CLK CRC H (7P3)
35 END TXM (1) H (7P2)

NOTES:

1. SEND WORD & START TRANSMISSION ARE BITS IN THE TCR. THEY ARE SET TO BEGIN THE TRANSMISSION.
2. WHEN SET WORD READY INDICATES A WORD MAY BE REMOVED FROM THE SILO. WILL NOT SET UNTIL CRC FOR THE WORD HAS BEEN CALCULATED.
3. THIS FLIP-FLOP IS CLOCKED AT THE END OF EVERY TIMESLICE. AT THIS TIME A DECISION CAN BE MADE AS TO WHETHER A WORD COULD BE SENT ON THE NEXT TIMESLICE.
4. TIMSL WILL SET WHENEVER TRANSMITTER DECODES ITS ADDRESS AND HAS OPENED OR IS OPENING A CHANNEL. WHEN SET, DRIVES RECEIVER ADDRESS, RSD A, DATA LINES ON TDM BUS.
5. & 6.

RSP A 1	RSP A 0	
0	0	OFFLINE; ERROR
0	1	NULL CYCLE
1	0	VALID WORD OR CRC
1	1	LAST CRC

7. WHEN SET INDICATES TRANSMITTER IS SENDING A WORD TO A RECEIVER.
8. WHEN SET REMOVES ONE WORD FROM OUTPUT OF SILO.
12. SETS WHEN BYTE COUNT IS ZERO AND SILO IS EMPTY, INDICATES LAST WORD OF MESSAGE HAS BEEN SENT AND CRC SHOULD BE CALCULATED.
13. CRC RDY SETS AFTER CRC HAS BEEN CALCULATED FOR EACH WORD.
14. SETS AFTER LAST CRC HAS BEEN CHECKED. MEANS THAT RECEIVER SHOULD RETURN A 00 RSP NEXT TIMESLICE TO CLOSE CHANNEL.
15. THIS PULSE IS GENERATED AFTER MESSAGE HAS BEEN SUCCESSFULLY SENT. CAUSES SUX TXF TO SET ST TXM, SND WD, CHAN OPEN TO CLEAR.
16,17. THESE TIMING SIGNALS ARE GENERATED BY THE ENABLED MASTER SECTION.
18. NUMBERS SHOWN ARE THE TXM ADDRESS BEING PUT OUT ON THE TDM BUS.
A TWO NETWORK SYSTEM IS SHOWN HERE.
19. RECEIVE WORD, RECEIVE DATA ARE TWO BITS IN THE RCR. THEY MUST BE SET BEFORE THE UNIT CAN RECEIVE DATA.
20. WHEN SET INDICATES SILO CAN ACCEPT ANOTHER WORD. INHIBITED BY BLK H.
21. THIS IS CLOCKED WHEN BD ADR IS SET. WILL SET IF RECEIVER CAN ACCEPT A WORD.
22. WILL SET WHEN RECEIVER IS ADDRESSED BY A TRANSMITTER. WHEN SET DRIVES RSP B, REJ AN TRUNC LINES ON TDM BUS.
23. & 24.

RSP B 1	RSP B 0	
0	0	BUSY, OFFLINE, ERR
0	1	NULL CYCLE
1	0	CHECK FAIL
1	1	ACKNOWLEDGE

25. WHEN SET INDICATES RECEIVER IS RECEIVING A MESSAGE FROM A TRANSMITTER.
26. WHEN SET LOADS A WORD INTO THE DATA SILO.
28. SETS WHENEVER A CRC WILL BE THE NEXT DATA TO BE RECEIVED FROM A TRANSMITTER.
29. USED WHENEVER A CRC CHARACTER IS RECEIVED. THE LEADING EDGE CLOCKS THE DATA INTO CRC REGISTER, THE TRAILING EDGE CLOCKS THE CHECK LOGIC.
30. SETS IF CRC CHARACTER WAS CHECKED OK (IE. NO 0'S IN REGISTER AT CHECK TIME).
31. IS ASSERTED IF THERE IS ANY DATA IN THE SILO.
32. IS SET WHEN MESSAGE HAS BEEN RECEIVED, - INDICATES A 00 RSP SHOULD BE SENT OUT ON NEXT TIMESLICE AND THEN THE CHANNEL BE CLOSED.
33. STROBE IS USED TO CLK THE RSP B AND ERROR BITS WHEN THE RECEIVER IS ADDRESSED.
34. USED TO CLOCK THE CRC REGISTER.
35. THIS PULSE IS GENERATED AFTER THE MESSAGE HAS BEEN RECEIVED SUCCESSFULLY. WILL SET SUC TXF AND CLEAR RCV DATA, RCV WD AND CHAN OPEN.

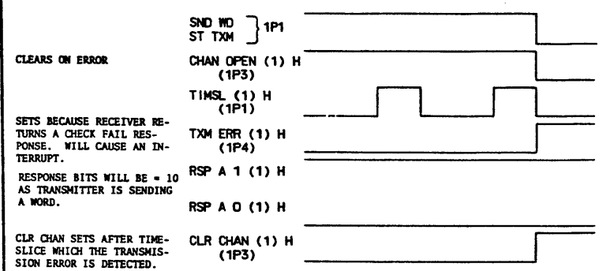
REVISIONS		
CHK	CHANGE NO.	REV.

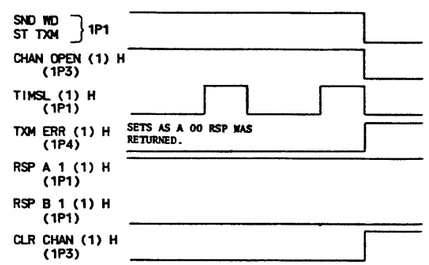
TITLE: TIMING DIAGRAM FOR A DATA TRANSFER
- USING NPR
- MORE THAN 200 (OCTAL) WORDS TRANSFERRED

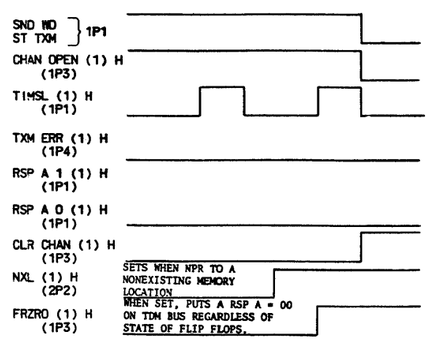
SIZE: D | CODE | NUMBER | REV.
SCALE | SHEET OF | DIST.

DEC FORM No. DRD 198

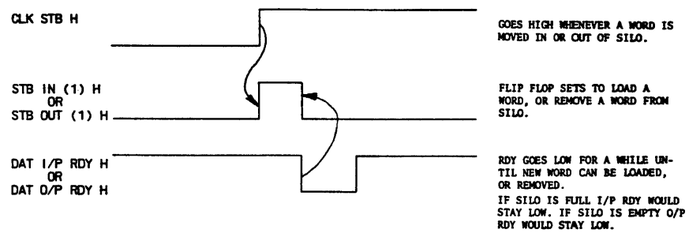
TRANSTEX 15 200-0-77



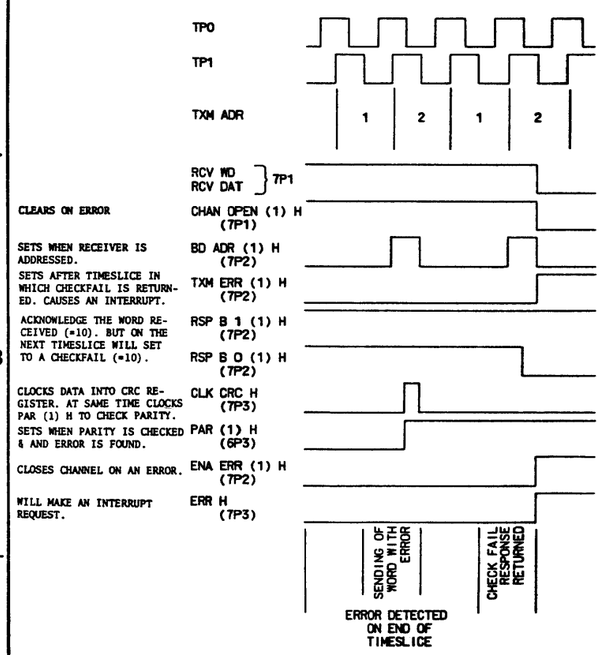




EXAMPLE OF SIGNALS USED TO LOAD OR UNLOAD DATA INTO SILO

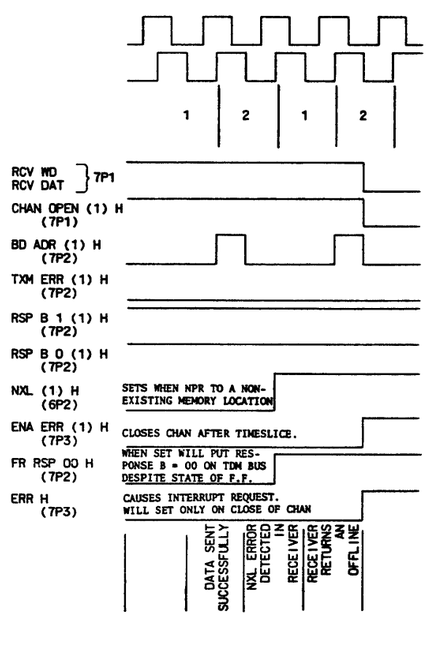


LOADING OR UNLOADING OF THE FIFO'S

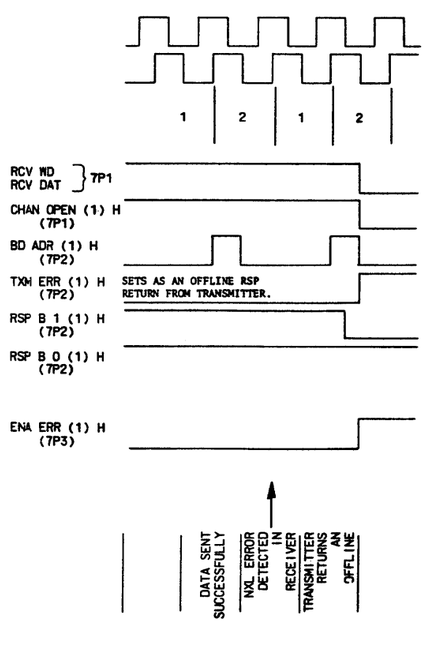


PARITY ERROR - CLOSING OF CHANNEL

A CRC ERROR WOULD CAUSE THE SAME TYPE OF SEQUENCE CRC ERR (1) H (7P3) WOULD SET INSTEAD OF CRC GOOD (1) H



NXL ERROR IN RECEIVER



NXL ERROR IN TRANSMITTER

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	PCL11 TIMING ON AN ERROR (AFTER CHANNEL IS OPEN)	SIZE / CODE	NUMBER / REV.
SCALE	SHEET OF	DIST.	

DEC FORM No. DRD 138

REV. | NUMBER | SIZE | CODE

SECTION 5

MAINTENANCE

5.1 DIAGNOSTIC SOFTWARE

PCL11-B Standalone Test (CZPLBA0) is used to trouble-shoot all errors. Detailed instructions on use of the diagnostic are included in the listing (AC-E252A-MC).

5.2 CORRECTIVE MAINTENANCE TECHNIQUES

PCL11-B is an interface which allows data to be transferred between a network of interfaces mounted in different computers. It may be used to build multiprocessor networks. The interface is divided into three main sections - transmitter, receiver and master sections. The transmitter section contains logic to control the transfer of data to the TDM BUS and is found mainly on the modules M7991, M7992 and M7993. The master section contains logic to generate timing pulses required by both transmitter and receiver and is found on module M7994. The receiver logic, which controls the reception of data from the TDM BUS, is to be found on modules M7995, M7996 and M7997. M8003 contains differential driver chips which are used by both receiver and transmitter to communicate with other processors. Both the receiver and transmitter have data Silos, or FIFOs, which buffer data transferred between PCL11 units and data received from or transferred to the Unibus.

The receiver and transmitter are independent sections of logic which transfer data over a bus called the TDM bus. This bus is a Time Division Multiplexed bus with all signals required to effect transfers being generated by the TDM bus Master. This master must not be confused with a Unibus master. The TDM bus master, (which every unit connected on the TDM bus has the logic to become but only one unit can be so designated) only generates the signals required by the other units on the bus. Each transmitter units is allotted, from the master, a certain portion of time to effect the transfer of one word of a message. All the transmitters in the system are allotted these "timeslices" so a number of messages may be transmitted simultaneously. A receiver in the same PCL11 unit as a transmitter looks exactly the same as one in a different unit. A transmitter may communicate with its own receiver through the TDM bus transceiver. This communication is tested by the standalone test.

Before debugging any problems with PCL11-B units, it is important to gain an understanding of the operation of the units. A general overview of a communications system is given in the general system manual YC-A20TC-01. A detailed description of the operation of the PCL11-B is detailed in Section 3.3. Once the operation has been understood Section 4 may be used to determine where the logic to implement the operation is located. This section may be utilized by first referencing the block diagram

for the PCL11-B. From this, a section of logic to be analysed may be found. Using the table of contents, a section describing where the logic is actually located in the unit can be found. This section will also describe the highlights of the logic itself. As a general rule, M7991 contains most of the transmitter logic which runs or interfaces to the TDM bus. M7992 contains the address decode for the transmitter, CRC generator for the transmitter, the NPR control logic and the interrupt logic. M7993 contains the transmitter data silo, the byte count and bus address register, and the multiplexers for the Unibus data lines. M7994 contains the master section logic, the Unibus receivers and most of the TDM bus transceivers. M7995 contains the receiver byte count and bus address registers, the receiver data silo, and the data multiplexers for the Unibus data lines. M7996 has the interrupt and NPR control logic and the receiver address decode. M7997 contains the receiver interface to the TDM bus. M8003 merely has the differential drivers for the TDM bus.

The following guideline may be followed to debug problems using the standalone test.

1. Disconnect the PCL11-B from the TDM bus. This may be accomplished by using the disable drivers switch on the M8003 module (turn off by pushing switch away from cable connectors) or by turning off the power on the PCL11-B unit and disconnecting both TDM bus cables from the M8003 module. The PCL11-B unit may be powered off while the rest of the system is in operation without fatal errors on the bus, however when powering off the unit care should be taken to ensure that some device is not drawing power from the same supply or power controller which cannot be powered off at this time. Because of the T-junction of the TDM bus cable, it may be disconnected from the M8003 without breaking the bus.

2. Load the standalone test (CZPLBA0 PCL11 STND-ALN V02) into the processor being used to check out the unit.

3. Start the program at location 200 (octal) and enter the information as required. The transmitter and receiver Unibus address, vector and priority will default. (164200, 164220, 170, 174, 5, 5) The TDM bus address will default to one, however a check should be made of the TDM bus addresses before continuing. These may be determined from the modules. M7991 contains a switch (5-bit) with the transmitter's address, most significant bit on the left, turned on for a zero. Similarly, M7997 contains a switch for the receiver's address.

4. When asked to select test, type a 4 to run all tests. If an error occurs then observe the error number and run the test required as per the following chart.

ERROR	1-121	Do section 5

ERROR	200-262	Do section 6
ERROR	300-355	Do section 7

In all cases, the module indicated to be swapped is only the most probable module on which the problem may occur. If following this guide does not solve the problem, then refer to the Theory of Operation for further aid.

5. When asked to select test, type a 1 to run the transmitter logic test. Use the following AS A GUIDE ONLY to help determine the module on which the errors may occur.

SUB-TEST 0 RESET TEST

This sub-test performs a Reset and then examines all registers to determine if they have been initialized properly.

In all errors in this sub-test, M7994 may have a problem as it contains Unibus receivers for address and data. M7992 have a problem because it decodes the register to be addressed and returns SSYN. It also generates the actual pulse (TX INIT - 2P5) which goes to the register. M7993 may have a problem as it contains the data multiplexers for the Unibus.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
1	TSBC not clear	M7993 - try swapping
2	TSBA not clear	M7993 - try swapping
3	TMMR not initialized	M7994 - try swapping
4	TSR not initialized	Determine which bit(s) is (are) bad. Refer to Section 4.2.12 and try swapping the module which the bit is on. (M7991 or M7992).
5	TCR not initialized	Determine which bit(s) is(are) bad. Refer to Section 4.2.12 and try swapping the module which the bit is on. (M7991, M7992, M7993).
6	TSCRC not initialized	M7992 - try swapping.

SUB-TEST 1 TCR TEST

This sub-test checks that all bits can be set in the TCR (Transmitter Command Register) (164200) and that TX INIT, which is generated by writing into bit 1 of the TCR, clears out the bits it is supposed to.

In all errors in this subtest, M7994 may have a problem as it contains Unibus receivers for address and data. M7992 have a problem because it decodes the register to be addressed and returns SSYN. It also generates the actual initialize pulse (TX INIT - 2P5). It also generates the load register pulses (LOAD COM HIGH H and LOAD COM LOW H - 2P5) which strobe the data into the TCR register. M7993 may have a problem as it contains the data multiplexers for the Unibus.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
7	Cannot set all dest. bits	M7993 - try swapping
10	Cannot clear dest. bits	M7993 - try swapping
11	Cannot set other TCR bits	Determine which TCR bit cannot be set. Refer to Section 4.2.12 and swap the module on which the bit is found. M7991, M7993).
12	TX INIT did not clear TCR	M7992 - try swapping. If this fails try swapping the module on which the bit(s) that did not clear are found. (See Section 4.2.12 - M7993, M7991).
13	TX INIT didn't clear TSBC	M7992 or M7993 - try swapping
14	TX INIT didn't clear TSBA	M7992 or M7993 - try swapping
15	TX INIT didn't clear TSR	Determine which bits of TSR did not get cleared. Refer to Section 4.2.12 to determine the module on which the bit resides and swap it. (M7991, M7992) If this fails, try swapping M7992.

SUB-TEST 2 TSBC TEST

This sub-test checks the TSBC (164206) by loading a sliding zeros bit pattern into it.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
16	Bad data in TSBC	M7993 - try swapping. If this fails try M7992, which contains the load and read pulses, or M7994 which contains Unibus address and data receivers.

SUB-TEST 3 TSBA TEST

This sub-test checks the TSBA (164210) with a sliding zeros bit pattern.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
17	Bad data in TSBA	M7993 - try swapping. If this fails try M7992, which contains the load and read pulses, or M7994 which contains Unibus address and data receivers.

SUB-TEST 4 MASTER SECTION TEST

This sub-test checks out the Master section of logic, which generates all the timing required for the transmitters and receivers of PCL11-B units on the TDM bus to exchange data. The sub-test begins by trying to set and clear all the bits in the TMMR (764212) which are associated with this section of logic. It ensures that if SEC is set with no other MASTER on the bus (which will be the case if the PCL11-B unit is offline) then MASTER and NOW MASTER will set and SEC will clear. (See sections 3.1.6, 3.3.2, 4.1 for more detailed information on this section of logic.)

This Master section contains an address silo for generation of TDM bus addresses. The sub-test checks that the silo (or FIFO) can be loaded and read with data correctly. It checks that it can be cleared with CLR SILO. It also checks that it can circulate to produce the TDM bus addresses. (See section 3.3.2-2 or 4.1.4 for more detailed information.)

The entire master section of logic is contained on module M7994. The actual load pulses for it come from M7992, so this module should be suspect in the event that the problem is not found on module M7994. The output from the TMMR is multiplexed onto the Unibus on module M7993, and as well the maintenance bit RD SILO is found on this module, so it should also be swapped if the problem persists.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
20 to 45	Master section problems	M7994 - try swapping

SUB-TEST 5 DATA SILO TEST

This sub-test checks out the data silo (or FIFO) in the transmitter section. All data which is transferred from this transmitter to a receiver passes through this silo. It appears

as a transmitter register on the Unibus, (TSDB 764204). When a word is moved to this location, it is loaded into the silo and begins to migrate to the end. The output of the silo is read by reading the TSDB. If the maintenance bit in the TCR (764200 bit 7) RD SILO is set, then no data can be loaded into the silo and the word on the output is discarded after being read. The silo can also be loaded by NPR cycles. (See sections 3.1.1 - bits 0, 3, 7, 3.1.2 - bit 8, 3.1.3; 4.2.7.)

After 200 (octal) words have been transferred to a receiver a CRC check character is inserted into the message. A counter is contained in the transmitter logic which counts the number of words removed from the silo. When it reaches 200 (octal) it will inhibit output ready. The last test in this sub-test will move 200 (octal) words through the silo and then check to ensure that output ready will not be asserted even though there is still data in the silo.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
46 to 54	Data cannot be moved through the silo	M7993 or M7992 - try swapping
55	Cannot set TX NPR in TCR	M7993 - try swapping
56	NPR not complete in 2 ms.	Let processor halt after the error (i.e. switch 15 should be a 0). Examine the TCR, TSR, TSBC, TSBA (764200, 764202, 764206, 764210 respectively), refer to sections 3.1.1, 3.2.2, 3.1.4, 3.1.5 for help in determining what should be in these registers. The TSBC (byte count) is loaded with 177600 and the TSBA (bus address) with "SILDAT:". The test decides that the NPR is complete when the byte count becomes zero. If the TSBC is unchanged and the bus address has moved, the problem may be in the increment byte count logic (M7992) or on the byte count itself (M7993). If neither the bus address or the byte count has moved then the NPR control logic may be faulty (M7992). If an NXL error (Non-existant location bit 14 TSR) is found, the extended address bits may be at fault (M7991). Any error

		will inhibit NPR cycles, so if an unexpected error is found in the TSR then the module associated with it should be changed. (This may be determined from section 4.2.12).
57 to 62	These indicate that NPR not successful	The failure may be due to many factors, wrong address put out on Unibus (M7993), byte count not incremented properly (M7992, M7993), or other sundry NPR problems (M7992, M7993).
63	O/P RDY after 200 words	M7991 or M7993 - try swapping

SUB-TEST 6 TSR AND ERRORS TEST

This sub-test checks that the read/write status bits set and clear properly. As well, some errors are generated to check whether the correct error bits will set.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
64	Cannot set TSR bit 7	M7991 or M7992 - try swapping
65	Cannot clear TSR bit 7	M7991 or M7992 - try swapping
66	TDM BUS BUSY not set	Let program halt on the error. This test is putting a receiver address of 0 on the TDM bus and expecting no one to respond. Examine the status register (TSR 164202). If none of bits 0-3 are set (these are RESPONSE bits) then the unit is likely not setting any timeslices. Check that the switch on M7994 is set to the highest address on the bus, and that the switch on M7991 is set to the correct address lower than the one on M7994. If these are correct, try swapping M7991, M7994, or M8003. If this does not solve the problem the register may not be putting data out correctly, in which case the problem may be on module M7993.

67	SND WD did not set BUSY	M7991 or M7993 - try swapping
70	SND WD set with interrupt	M7991 or M7993 - try swapping This error uses the fact that an interrupt request will clear SND WD. Following tests determine whether bits make interrupt requests by checking to see if setting them clear SND WD.
71	BUSY set SND WD clear	M7991 or M7993 - try swapping
72	Cannot set OVERRUN in TSR	M7991 - try swapping
73	OVERRUN did not set ERR	M7991 - try swapping
74	ERR did not cause INT REQ	M7991 - try swapping
75	OVERRUN set with I/P RDY	M7991 - try swapping
76	Cannot set TIMEOUT in TSR	M7991 - try swapping
77	TIMEOUT did not set ERR	M7991 - try swapping
100	Cannot set MASTER DOWN	M7991 - try swapping
101	MST DWN did not set ERR	M7991 - try swapping
102	Cannot set TXM ERR	M7991 - try swapping
103	TXM ERR did not set ERR	M7991 - try swapping
104	Cannot set MEM OFL	M7992 - try swapping
105	MEM OFL did not set ERR	M7991 or M7992 - try swapping
106	Unexpected NPR cycle	** This test loads 764176 into Bus Address register and tries to perform an NPR. It expects that 764176 does not exist on the Unibus. If there is such a location, then replace location **13164** in the diagnostic with a non-existent Unibus address in the I/O page. If the error persists then try swapping M7992 or M7993.
107	NXL did not set	M7992 - try swapping

110	NXL did not set ERR	M7991 - try swapping
111	OVERRUN not set on load	M7991 - try swapping
112	No TIMEOUT after 1 sec.	M7991 - try swapping
113	MASTER DOWN didn't set	This test tries to send a word with Master Clear and expects a Master Down error. Ensure this unit is off line. If the error persists try swapping M7991.

SUB-TEST 7 INTERRUPT TEST

This sub-test checks to ensure that an interrupt request will cause an interrupt cycle to be performed on the Unibus at the correct level and at the correct vector. If a problem arises with the vector try swapping M7993.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
114	Unexpected Interrupt	M7992 or M7991 - try swapping
115	No interrupt	M7992 or M7991 - try swapping
116	Interrupt at low priority	M7992 - try swapping
117	Interrupt at high priority	M7992 - try swapping

SUB-TEST 10 CRC TEST

This sub-test checks that the CRC is calculated properly. Every time a word appears on the output of the Silo it is run through the CRC accumulation logic on M7992. The calculation can be read at TSCRC (164214).

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
120	TX NPR not CLR'd by BC OFL	M7992 or M7991 - try swapping
121	Bad CRC calculated	M7992 or M7991 - try swapping

6. Start the diagnostic at location 204 (octal) when asked to select test type a 2 to run the receiver test. Use the following AS A GUIDE ONLY to help determine the module on which the errors may occur.

SUB-TEST 0 RESET TEST

This sub-test performs a Reset and then examines all registers to determine if they have been initialized properly.

In all errors that may occur in this sub-test, M7994 may be at fault since it contains all the Unibus receiver chips for the address and data lines. This module also does the decoding of the device address. M7996 may have a problem as it decodes the actual register to be addressed and then returns SSYN. The module also generates the actual initialize pulse (RC INIT - 6P4) which goes to all the registers. As well, M7993 may have a problem as it contains the multiplexers for the data being moved back out onto the Unibus.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
200	RDBC not cleared	M7995 - try swapping
201	RDBA not cleared	M7995 - try swapping
202	RCR not cleared	Determine which bit(s) is(are) bad. Refer to section 4.3.12 and try swapping the module which the bad bit(s) is(are) located. (M7995, M7996, M7997).
203	RDCRC not cleared	M7997 - try swapping
204	RSR not cleared	Determine which bit(s) is(are) bad. Refer to section 4.3.12 and try swapping the module which the bad bit(s) is(are) located. (M7995, M7996, M7997).

SUB-TEST 1 RCR TEST

This sub-test checks that all settable bits can be set in the RCR. It also checks that the RC INIT pulse generated by writing into bit 1 of this register initializes the registers as it is supposed to.

In all errors that may occur in this sub-test, M7994 may be at fault since it contains all the Unibus receiver chips for the address and data lines. This module also does the decoding of the device address. M7996 may have a problem as it decodes the actual register to be addressed and then returns SSYN. The module also generates the load register pulses (LOAD COM HIGH H and LOAD COM LOW H - 6P4) which go to all the registers. As well, M7995 may have a problem as it contains the multiplexers for the data being moved back out onto the Unibus.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
205	Can't set all bits in RCR	Determine which bit cannot be set by referring to the console output printed on the

		error. Try swapping the module on which the bit resides. (This may be determined by referring to section 4.3.12 - M7995, M7996, M7997). If the problem persists, swap M7996.
206	Can't clear above bits	Determine the bad bit from section 4.3.12 and swap the appropriate module. (M7995, M7996, M7997).
207	RCR not init. by RC INIT	M7996 - try swapping. If the error persists determine the bad bit and swap the appropriate module. (See section 4.3.12 and swap either M7995, M7996, or M7997.)
210	RCR not init. by RC INIT	M7996 - try swapping. If the error still persists, determine the bad bit and swap the appropriate module. (See section 4.3.12 and swap either M7995, M7996, or M7997.)
211	RDBC not clear by RC INIT	M7996 - try swapping. If the error persists, try swapping M7995.
212	RDBA not clear by RC INIT	M7996 - try swapping. If the error persists, try swapping M7995.

SUB-TEST 2 RDBC TEST

This sub-test checks the RDBC (164226) with a sliding zero's bit pattern.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
213	Bad data in RDBC	M7995 - try swapping

SUB-TEST 3 RDBA TEST

This sub-test checks the RDBA (164230) with a sliding zero's pattern.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
214	Bad data in RDBA	M7995 - try swapping

SUB-TEST 4 DATA SILO TEST

This sub-test checks out the data silo (or FIFO) in the receiver section. All data which is received from another transmitter is loaded into this silo until it can be moved onto the Unibus. The silo appears on the Unibus as a register (RDDB 764224). When read, the word on the output of the silo is removed. When LD SILO (RCR bit 7) is set, no words can be read from the silo but any data moved to the RDDB will be loaded into the top of the silo.

After 200 (octal) words have been transferred to the receiver it will expect that the next character to come along will be a CRC character. A counter is contained in the receiver logic to count the number of words received. When it reaches 200 (octal) it will inhibit input ready. The last test of this section moves 200 (octal) words through the silo and then expects that input ready will not be asserted.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
215	RC INIT didn't clear silo	M7995 or M7996 - try swapping
216	RC INIT didn't clear silo	M7995 or M7996 - try swapping
217	No word on silo output	M7995 or M7997 - try swapping
220	Bad data in silo	M7995 - try swapping
221	Word not out of silo	M7995 or M7996 - try swapping
222	Silo input not ready	M7995 - try swapping
223	Bad data in silo	M7995 - try swapping
224	Silo full/input is ready	M7995 - try swapping
225	NPR not complete in 2 ms	Let processor halt after the error (i.e. switch 15 should be a zero). Examine the RSR, RDBC, RDBA (764222, 764226, 764230 respectively), refer to sections 3.1.1, 3.1.2, 3.1.4, 3.1.5 for help in determining what should be loaded into these registers. The RDBC (byte count) is loaded with 177600 and the RDBA (bus address) with "CMPBUF:". The test decides that the NPR is complete when the byte count becomes zero. If the RDBC is unchanged and

		the RDBA has moved then the problem may be in the byte count M7995). If neither register has moved then the NPR logic may be faulty (M7996). If an NXL (Non-Existant Location error RSR - bit 14) has occurred the bus address (M7995) or the extended bus address M7996) may be at fault. Any error will inhibit NPR cycles, so if an error occurs it may be found in the RSR and the module on which it is on should be swapped. (The module may be determined by referring to section 4.3.12).
226	Data from silo is wrong	This may be due to a number of failures in the NPR transfer. For example Bad Address put out on bus (M7995), byte count not incrementing properly (M7995, M7996) or other sundry problems (M7995 or M7996). If after running this part of the test it is observed that part of the diagnostic has been corrupted this may be due to a problem in the address for the NPR transfer into memory. Try swapping M7995.
227	Word in silo after NPR	M7995 - try swapping
230	200 words/input still rdy	M7997 - try swapping

SUB-TEST 5 RSR

This sub-test checks that all bits in the Receiver Status Register (RSR - 16220) can be set and cleared. It will also test that certain errors can be caused and will set the appropriate error bits.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
231	RCV WD set but BUSY clear	M7997 - try swapping
232	Can't set SUC TXF	M7997 - try swapping
233	SUC TXF didn't clr SND WD	M7996 or M7997-by swapping. This test makes use of the fact that an interrupt

		request will clear SND WD. Following tests determine whether the various bits make interrupt requests by checking to see if setting them clears SND WD. M7997 - try swapping.
234	Can't clear SUC TXF	M7997 - try swapping
235	Silo emptied unexpectedly	M7996 - try swapping
236	TSBA incr but INH ADI set	M7996 - try swapping
237	BC OFL did not set	M7996 or M7995 - try swapping
240	BC OFL did not set ERR	M7997 - try swapping
241	BC OFL did not req inter	M7997 or M7996 - try swapping
242	Can't set TIM OUT	M7997 - try swapping
243	TIM OUT didn't set ERR	M7997 - try swapping
244	ERR didn't request inter	M7996 - try swapping
245	Can't set PARITY	M7996 - try swapping
246	PAR did't set ERR	M7997 - try swapping
247	Can't set TXM ERR	M7997 - try swapping
250	TXM ERR didn't set ERR	M7997 - try swapping
251	Can't set MEM OFL	M7996 - try swapping
252	MEM OFL didn't set ERR	M7997 - try swapping
253	Unexpected NPR cycle	**This test loads 764176 into Bus Address register and tries to perform an NPR. It expects that 764176 does not exist on the Unibus. If there is such a location, then replace location **21234** in the diagnostic with a Non-existent Unibus address in the I/O page. If the error persists then try swapping M7996 or M7995.
254	NXL did not set	M7996 - try swapping
255	NXL did not set ERR	M7997 - try swapping

SUB-TEST 6 INTERRUPT TEST

This sub-test checks that the receiver can interrupt at the correct vector and priority level. If any problem occurs with the vector in this test, then try swapping M7995.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
256	Unexpected interrupt	M7996 or M7995
257	No interrupts	M7996 - try swapping
260	Interrupt at low priority	M7996 or M7992 - try swapping
261	Interrupt at high priority	M7996 or M7992 - try swapping

SUB-TEST 7 CRC TEST

This sub-test checks that the CRC character is calculated properly. A running CRC is accumulated whenever a data word is loaded into the Data Silo.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
262	Bad CRC calculated	M7997 - try swapping

7. Start the diagnostic at location 204 (octal), when asked to select test type a3 to the receiver-transmitter loop test. Use the following AS A GUIDE ONLY to help determine the module on which the errors occur.

SUB-TEST 0 I/O PAGE NPR TESTS

This sub-test checks that NPR's can be made to the I/O page. Two NPR's are executed from the transmitter's to the receiver's data silo. One is controlled by the transmitter and the other by the receiver. These tests check that the extended address bits and the inhibit address increment bits work in both the receiver and the transmitter.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
300	RCV cntrl NPR not done	Let computer halt after the error and examine the registers. (TSR-164200, TSBC-164206, TSBA-164210, RSR-164222, RDBC-164226, RDBA-164230). This test decides the NPR is finished when 64 words have been moved into the TSBC. (The TSBC is incremented every time a word

		is moved into it.) If there is a NXL error in the receiver (RSR bit 14) try swapping M7996. If the RDBA is not loaded with the address of the TSDB (164204) the inhibit address increment may be at fault. Try swapping M7995. If any error bits are set in the TSR or RSR, then try to swap the module on which they reside. (See section 4.2.12 or 4.3.12 to determine the module on which the bits reside.)
301	Bad data NPR'd to silo	M7995, M7993, M7996, or M7992 - try swapping.
302	RDBA not zero	M7995 - try swapping
303	TXM NPR not completed	Let computer halt after the error and examine the registers. (TSR-164200, TSBC-164206, TSBA-164210, RSR-164222, RDBC-164226, RDBA-164230). This test decides the NPR is finished when the transmitter's byte count has become zero. If there is a NXL error in the transmitter (TSR bit 14) try swapping M7993 or M7991. If the TSBA is not loaded with the address of the RDDB (164224) the inhibit address increment may be at fault. Try swapping M7993 or M7992. If any error bits are set in the TSR or RSR, then try to swap the module on which they reside. (See section 4.2.12 or 4.3.12 to determine the module on which the bits reside).
304	Bad data NPR'd to silo	M7993, M7995, M7992 or M7996 - try swapping.

SUB-TEST 1 DATA LOOPS TESTS

This series of tests sends data from the transmitter section to the receiver section of the PCL11-B over the TDM Bus. Four messages are sent; the first two are just single word

transfers. These test that data can be moved to the receiver, but do not check channel closing. The third message is a 64 word transfer of data. This data is retrieved from a buffer area and stored in another buffer by NPR transfer. This will check the NPR facility, the channel opening and closing, and the CRC and Parity checking of data. The last message is a 300 (octal) word transfer. The transmitter transfers a test word into the data silo using NPR and inhibit address increment. The receiver will remove each word that arrives and check it without using NPR. This test will ensure that more than one block of data may be sent and the CRC will be sent and acknowledged correctly, both at the end of a 200_8 word block and at the end of the transmission.

The key to understanding what has caused an error in completing the data transfer is in the Response bits of the transmitter and the receiver. These bits accompany every word transferred and are the indication between the transmitter and receiver units of their status during the timeslice. These bits are frozen in the event of an error and thus give an indication of what was happening when the error occurred. These Response bits are explained in more detail in sections 3.3.3-2 and 3.3.3-3.

RSP A 1	RSP A 0	
0	0	Transmitter busy or offline
0	1	Null Cycle
1	0	Valid word or CRC on bus
1	1	Last CRC on bus (Indicates transmitter has initiated channel closing).

Bit 1 Bit 0 of the TSR (164202) and RSR (164222)

RESPONSE B Receiver Response Bits

RSP B 1	RSP B 0	
0	0	Receiver busy or offline
0	1	Null cycle
1	0	Check fail (Receiver has detected a CRC or Parity error)
1	1	Acknowledge word or CRC

Bit 3 Bit 2 of the RSR (164222) and TSR (164202)

The general procedure for detection of errors in this section is to let the computer halt and examine the status registers. Particular attention should be paid to the response and error bits to determine which state the logic was in when the failure occurred and what the failure was. Care must be taken to ensure all possibilities are considered as many errors may be contained in the receiver section and manifest themselves in the transmitter section or vice versa.

In all errors in this subtest, the M8003 may have a problem and should be swapped if the error persists.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
305	Word wasn't RCV'D in 2 ms	Check response A bits in the transmitter. If they are 00 and a TIME OUT error has occurred (TSR - bit 10) then the transmitter is likely not getting a timeslice. Check the address switches on M7994 and M7991 to see they are set up properly. If they are correct the problem may be in M7991 or M7994. If TDM BUS BUSY is set (TSR - bit 4) then the receiver did not respond to being addressed. Check the address switch on the M7997 module. The address for the transmitter and the receiver may be re-entered into the diagnostic by typing CNTRL C and entering the correct parameters as required. If there is no setup problems then the error is likely to be due to problems in either the M7991 or the M7997 module as these contain the TDM bus control logic. M7994 may also have a problem as it contains the Master Section and hence the address generation and the Time Phase signals.
306	Error on 1 word trans.	Determine which error bit is set in the RSR. If it is MEM OFL, NXL, or BC OFL then try swapping M7996. If the problem is TXM ERR, TIM OUT or PAR then try swapping M7991, M7994.
307		No SUC TXF in 2 ms. M7991 - try swapping.
310	Bad data received	M7991, M7994, M7993 or M7995 - try swapping.
311	TXM ID bits are wrong	This is likely due to the wrong transmitter address being entered into the diagnostic. If this is not the case then either M7997, M7994 or M7991 is at fault.

312	Word wasn't sent in 2 ms	Check response A bits in the transmitter. If they are 00 and a TIME OUT error has occurred (TSR - bit 10) then the transmitter is likely not getting a timeslice. Check the address switches on M7994 and M7991 to see they are set up properly. If they are correct the problem may be in M7991 or M7994. If TDM BUS BUSY is set (TSR - bit 4) then the receiver did not respond to being addressed. Check the address switch on the M7997 module. The address for the transmitter and the receiver may be re-entered into the diagnostic by typing CNTRL C and entering the correct parameters as required. If there is no set up problems then the error is likely to be due to problems in either the M7991 or the M7997 module as these contain the TDM bus control logic. M7994 may also have a problem as it contains the Master Section and hence the address generation and the Time Phase signals.
313	Error on 1 word trans.	Determine which error bit is set in the TSR. If it is MEM OFL, NXL, or BC OFL they try swapping M7996. If the problem is TXM ERR, TIM OUT or PAR then try swapping M7991, M7997, M7994.
314		No SUC TXF in 2 ms. M7991 - try swapping
315	Bad data received	M7991, M7994, M7993 or M7995 - try swapping.
316	64 word X-fer not done	Halt and examine the response and error bits. If the RSR shows a parity error then the

		problem is likely either on M7996 or on M7993 M7995 or M7991. If the response is a check fail for the last CRC on the bus (bits <3:0> = 1011 in RSR or TSR) then the problem is one of either CRC generation (M7992) or of checking (M7993) or of the data lines (M7991). If there is a problem with NPR on either the transmitter or the receiver (TSR bits 14, 13 - M7992 or RSR bit 14, 13, 9 - M7996) then swap the appropriate module. Other data transmission problems are likely due to faults in M7991 or M7997.
317	No SUC TXF in receiver	If this error occurs without error 316 then M7997 is liable to be at fault.
320	Bad data received	M7995 - try swapping
321	No word rcv'd for 10 ms	Check the number of words received and the error and response bits. If 200 (octal) words were received then it is likely that there is a CRC problem. This can be confirmed by checking the response and status bits. (try swapping M7991, M7997, M7992, M7994). Try the same modules if there is any parity errors. If there is an NPR problem on the transmitter logic try swapping M7992).
322	Bad data received	This may be due to a data path problem, but such an error is likely to have been caught by an earlier test. If the problem occurs on the 201th (octal) word received, then it may be the CRC character has been put in the data silo. The 200th CRC character is sent with the same response as any other data word. The receiver and

		transmitter both have separate counters to calculate when a CRC character should be sent. If there is a failure in either of these counters then one unit will consider that a data word is being sent while the other will treat the data as a CRC. The block counter may be at fault (M7991, M7997) or the logic to generate or check the CRC again on M7991 or M7997.
323	No SUC TXF in Transmitter	M7991 or M7997 try swapping
324	No SUC TXF in Receiver	M7991 or M7997 - try swapping

SUB-TEST 2 TRANSMISSION ERRORS TEST

This sub-test creates an error condition to determine if the error bits in the unit will set when they are supposed to. Explanation of the error creation is included in the listing. As a rule, a good understanding of the opration of the PCL11 is required before these tests can be understood.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
325 to 344	Status not as expected	M7991, M8003 or M7997 - try swapping.

SUB-TEST 3 REJECT AND TRUNCATE TEST

This sub-test checks that the unit can reject and truncate messages.

ERROR	PROBLEM	POSSIBLE MODULE OR ACTION
345	Reject no completed	M7997, M8003 or M7991 try swapping
346	SORE did not inter	M7991 - try swapping
347	REJ COM didn't clr REJ	M7997 - try swapping
350	SORE not set in TSR	M7991 - try swapping
351	REJ COM didn't interrupt	M7997 or M7996 - try swapping
352 to 355	Truncation did not complete properly	M7997, M8003 or M7991 - try swapping.

APPENDIX A.1

PCL11-B SHIPPING LIST

APPENDIX B

B.1 SUMMARY OF TDM BUS LINES

16	Data	(D)	Asserted by Transmitter
1	Parity	(PAR)	during 1 time slice.
2	Response A	(RSPA)	
5	Receiver Address	(RA)	
2	Response B	(RSPB)	
1	Reject	(REJ)	Asserted by Receiver
1	Truncate	(TRUN)	during 1 time slice.
5	Transmitter Addr.	(TA)	Asserted all the time by
2	Time Phase	(TP)	enabled Master Section
1	Master Active	(MST ACT)	
36	Lines Total		

B.2 TTL BUS - BACKPLANE PIN ASSIGNMENT

AA1	GND	BA1	GND
AA2	NC	BA2	NC
AB1	D15	BB1	MST ACT
AB2	NC	BB2	NC
AC1	GND	BC1	GND
AC2	GND	BC2	GND
AD1	D13	BD1	TA 00
AD2	D14	BD2	PAR
AE1	D11	BE1	TA 02
AE2	D12	BE2	TA 01
AF1	GND	BF1	GND
AF2	GND	BF2	GND
AH1	D09	BH1	TA 04
AH2	D10	BH2	TA 03
AJ1	D07	BJ1	RA 01
AJ2	GND	BJ2	GND
AK1	GND	BK1	GND
AK2	D08	BK2	RA 00
AL1	D05	BL1	RA 03
AL2	GND	BL2	GND
AM1	D03	BM1	TP 0
AM2	D06	BM2	RA 02
AN1	GND	BN1	GND
AN2	GND	BN2	GND
AP1	D01	BP1	RSP A 0
AP2	D04	BP2	RA 04
AR1	GND	BR1	GND
AR2	GND	BR2	GND
AS1	TRUN	BS1	RSP B 0

DIGITAL EQUIPMENT OF CANADA LTD.
OTTAWA, CANADA

SHIPPING LIST

MADE BY J. PAYER	CHECKED	SECTION C.S.S.
DATE 230678	DATE	
ENG [illegible]	PROD	ISSUED SECTION
DATE [illegible]	DATE	

ITEM NO.	PART NO.	DESCRIPTION	HARDWARE	DIAGNOSTIC PKG	PRINT SET	MANUAL	OTHER	PAPER TAPES	LISTINGS						
1	M7991-00	TXM INTERFACE MODULE	1												
2	M7992-00	TXM UNIBUS CONTROL AND CRC MODULE	1												
3	M7993-00	TXM REGISTERS MODULE	1												
4	M7994-00	MASTER SECTION	1												
5	M7995-00	RCV REGISTERS MODULE	1												
6	M7996-00	RCV UNIBUS CONTROL MODULE	1												
7	M7997-00	RCV INTERFACE MODULE	1												
8	M8003-00	PCL11-B DIFFERENTIAL BUS TRANSCEIVER MODULE	1												
9															
10	M920-00	UNIBUS JUMPER MODULE	1												
11	90-06042-01	SCREW PHIL PAN HD 8-32 X 7/8LG	4												
12	90-08151-00	WASHER LOCK EXTERNAL TOOTH NO 8-32	4												
13	12-09856-02	CLIP, MODULE HOLDER	3												
14	H3370-00	TERMINATOR ASSEMBLY	1												
15	BC20K-05	PCL CABLE	1												
16	BC20P-XX	PCL INTERCONNECT CABLE	-												SEE NOTE 1
17															
18															
19	2C-H238A-00	PCL BACKPLANE ASSEMBLY	1												
20															
21	B-DD-PCL11-00	PARALLEL COMMUNICATION LINK			1										CUSTOMER PRINT SET
22	YC-A20TC-00	PCL11-B OPTION DESCRIPTION				1									
23	YC-A20TC-01	PCL11-B GENERAL MANUAL				1									
24	YC-A20TC-02	PCL11-B COMMUNICATION SYSTEM MANUAL				1									
25	AK-E264A-MC	CZPLBA0 PCL11 STAND ALONE TEST (V-02)						1							
26	AC-E262A-MC	CZPLBA0 PCL11 STAND ALONE TEST (V-02)							1						
27															
28	AK-E261A-MC	CZPLAA0 PCL11 EXERCISER (V-02)						1							
29	AC-E259A-MC	CZPLAA0 PCL11 EXERCISER (V-02)							1						

NOTES:

1. BC20P-XX MUST BE ORDERED SEPARATELY. REFER TO YC-A20TC-02 FOR FURTHER INFORMATION.

E.C.O. NO. [illegible]

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.
PARALLEL COMMUNICATION LINK	B-DD-PCL11-00	B	SL	PCL11-B	A
	SHEET 1 OF 1	INSERTION PARTS LIST DATA BASE REV			

DRB 033

AS2	DO2	BS2	TP 1
AT1	GND	BT1	GND
AT2	DOO	BT2	RSP A 1
AU1	NC	BU1	NC
AU2	GND	BU2	GND
AV1	NC	BV1	NC
AV2	REJ	BV2	RSP B 1

NOTE: A corresponds to E01 and/or E09 and B corresponds to F01 and/or F09 on PCL11-B backplane assembly.

B.3 TDM BUS PIN ASSIGNMENTS (DIFFERENTIAL)

PIN	J2 SIGNAL NAME	J3 SIGNAL NAME
A	TDM BUS -	TDM BUS TP 00H
B	-	TP 00L
C	TRUN H	-
D	TRUN L	-
E	D00 H	RA 00H
F	D00 L	RA 00L
H	D01 H	RA 01H
J	D01 L	RA 01L
K	D02 H	RA 02H
L	D02 L	RA 02L
M	D03 H	RA 03H
N	D03 L	RA 03L
P	D04 H	RA 04H
R	D04 L	RA 04L
S	D05 H	RSP A 004
T	D05 L	RSP A 00L
U	D06 H	RSP A 01H
V	D06 L	RSP A 01L
W	D07 H	PAR H
X	D07 L	PAR L
Y	D08 H	TA 00 H
Z	D08 L	TA 00 L
AA	D09 H	TA 01 H
BB	D09 L	TA 01 L
CC	D10 H	TA 02 H
DD	D10 L	TA 02 L
EE	D11 H	TA 03 H
FF	D11 L	TA 03 L
HH	D12 H	TA 04 H
JJ	D12 L	TA 04 L
KK	D13 H	MAS ACT H
LL	D13 L	MAS ACT L
MM	D14 H	RSP B01 H
NN	D14 L	RSP B01 L
PP	D15 H	RSP B00 H
RR	D15 L	RSP B00 L
SS	REJ H	-
TT	REJ L	-
UU	SEC ACT H	TP 01 H
VV	SEC ACT L	TP 01 L

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