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Noise Issues in the ECL Circuit Family

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Noise Issues in the ECL Circuit Family

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January, 1990

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Abstract

Noise in electrical systems is unavoidable. In a digital system, the main concern is that the noise has to be controlled so as not to cause a false switch, which would result in system malfunction. ECL circuits are faster than most other circuit families because they use a smaller logic swing. Unfortunately, circuits using small logic swings also have small DC noise margins. To specify an appropriate logic swing for ECL circuits, designers must first identify all of the DC noise sources. In this report we analyze various kinds of DC noise sources and provide design techniques to minimize them, especially for high power, high density ECL integrated circuits.

1. Introduction

Noise in electrical systems is unavoidable. In a digital system, the main concern is that the noise has to be controlled so as not to cause a false switch resulting in system malfunction.

Noise margins are different for different circuit families. For example, the noise margin in CMOS is much better than that in NMOS circuitry because of the better transfer characteristic which results from replacing the depletion FET with a PFET. Because of the larger voltage swing, the MOS circuit families have in general much better noise margins than the ECL circuit family. Roughly speaking, the voltage swing ratio between MOS and ECL is about 10 to 1. In MOS circuit families the power consumption is mainly AC, especially in CMOS, while in the ECL circuit family DC power is the main concern. For a high power single chip ECL processor, the noise problem is further exacerbated by the high DC current demand. The immediate problem that arises is the IR drop on the power bus which in fact is the single most important noise source.

In this document, the noise margin definition, DC noise margin for ECL gates, and noise sources in the ECL environment will be discussed.

2. DC Noise Margin

In this chapter, our definition of noise immunity and unity gain noise margin will be introduced. The interpretation of noise margin in terms of the transfer curve of a basic gate is also discussed. Specifically, the transfer equation for a basic ECL gate is derived and the noise margin variation is discussed.

2.1. Definition

Noise immunity is defined as the amount of noise required at the input of the *first* receiving gate to cause a false switch in the subsequent gates of an infinite chain. This is depicted in Figure 2-1(a). For example, the noise immunity of a chip input receiver is the amount of cross talk, ringing, etc. that can be tolerated on the board without causing a false switch of the receiver. Since the output of a receiver is often latched, one can consider the infinite chain being replaced by the latch.

As depicted in Figure 2-1(b), *noise margin* is defined as the amount of noise required on the inputs of *each* gate of an infinite chain of gates that eventually causes a false switch down the chain. The difference here is that the noises are at the inputs of all gates, not just the first one.

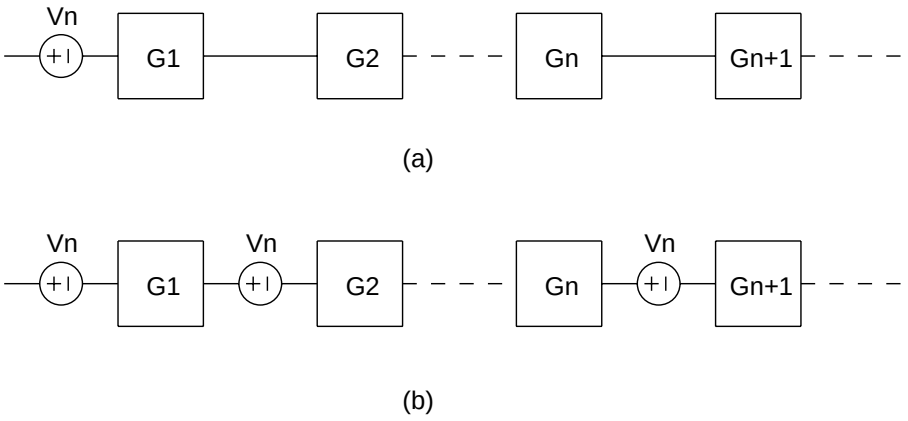

Figure 2-1: An infinite chain of gates defining (a) noise immunity and (b) noise margin

Noise immunity is always larger than noise margin, since it only guarantees that the first receiving gate will not false switch. Noise margin more conservatively considers the cumulative effect of noise at the inputs to each gate. In practice, noise margin is a better measure. In this report we will concentrate mainly on DC noise margin. Keeping the DC noise within the noise margin guarantees functional circuits.

Figure 2-2 shows the transfer relation of a non-inverting gate. Both y(x), x(y), and x=y are plotted. Noise margin is defined as the distance in x (or y) from the slope-of-one point of y(x) (or x(y)) to the y=x line. Since y(x) and x(y) are symmetric with respect to the y=x line, a different way of saying this is that the edge of the largest square that can be fit into the lobes defines the noise margin. In Figure 2-3, it is demonstrated that this is in fact the same definition as depicted in Figure 2-1(b). A similar definition exists for an inverting gate by simply rotating the diagram 90 degrees.

Assume V_n in Figure 2-1(b) equals the noise margin (NM). As shown in Figure 2-3, starting from the first input x_0 at perfect high level and subtract NM to x_0' which is the input level as seen by the gate, the output is obtained at y_1 through the transfer curve y(x). Since y_1 is again degraded by NM, y_1' is seen at the next input gate and x_2 is obtained through the transfer curve x(y). Going down the paths, it eventually converges to a loop which starts at x_{2n}, the slope-of-one point of x(y), to x_{2n}', the slope-of-one point of y(x), to y_{2n+1}, to y_{2n+1}' and returns to x_{2n}. If V_n is greater than NM, it will converge to the low side after some number of gates and cause a false switch.

A similar construction can be made for inverting gates. The derivation up to this point is completely general and can be applied to any circuit family. This completes the definition of noise margin.

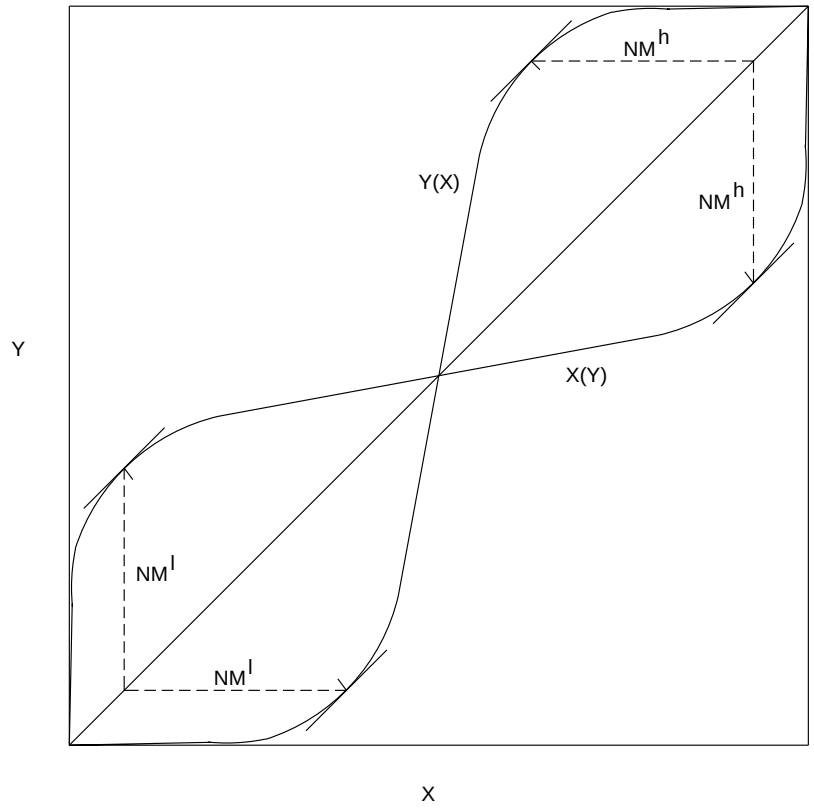

Figure 2-2: The transfer curve of a non-inverting gate

2.2. A Basic ECL Gate

A basic ECL gate structure is shown in Figure 2-4.

Let us define the normalized input, *x*, output, *y*, and voltage swing, *s*, as

$$x = \frac{v_{in} - v_{ref}}{v_T}, \tag{1}$$

$$y = \frac{v_o}{v_T} = \frac{-I_o \times R_c}{v_T}, \tag{2}$$

and

$$s = \frac{v_s}{v_T} = \frac{-I_t \times R_c}{v_T}, \tag{3}$$

where v_T is the thermal voltage and others are obvious in Figure 2-4.

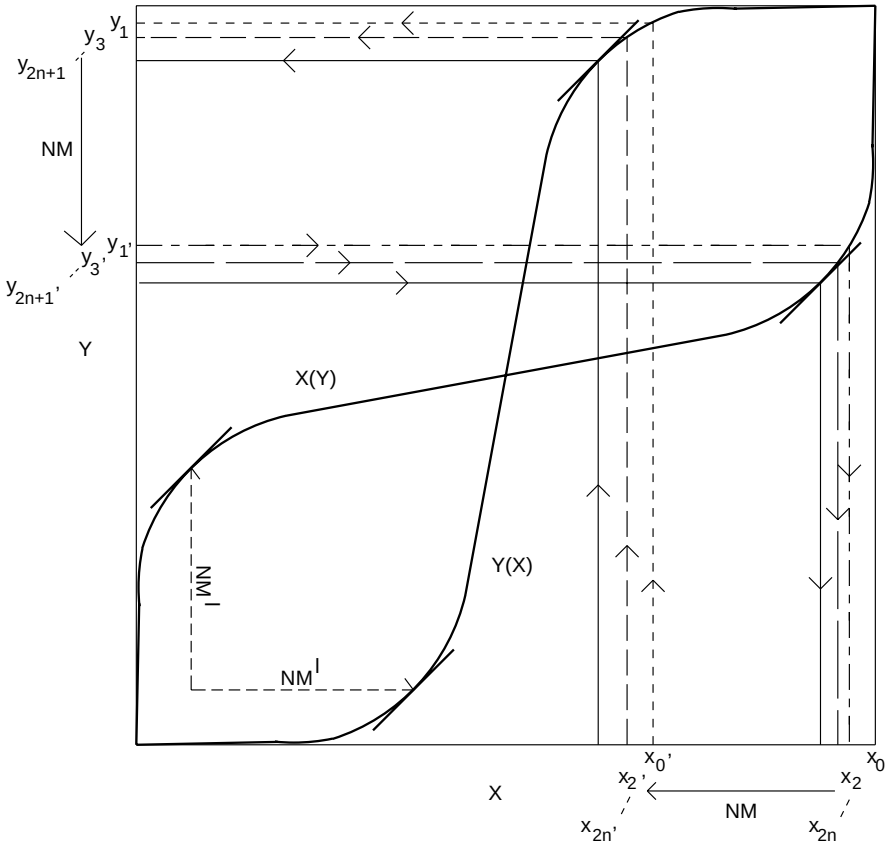

Figure 2-3: The transfer paths of a series of non-inverting gates each having a noise source equal to NM

In the simplest approximation, I_o and $I_{\sim o}$ can be expressed as

$$I_o = I_s \, exp\,(\frac{V_{be2}}{v_T}), \tag{4}$$

$$I_{\sim o} = I_s \, exp\,(\frac{V_{be1}}{v_T}). \tag{5}$$

The ratio of the two output currents becomes

$$\frac{I_{\sim o}}{I_o} = exp\,(\frac{V_{be1} - V_{be2}}{v_T}) = exp\,(\frac{v_{in} - v_{ref}}{v_T}) = exp(x). \tag{6}$$

Since the outputs are connected to bases of either the emitter followers in the ECL configuration or the next gate in the CML configuration, the base currents are negligible. Hence,

$$I_t = I_o + I_{\sim o}\,. \tag{7}$$

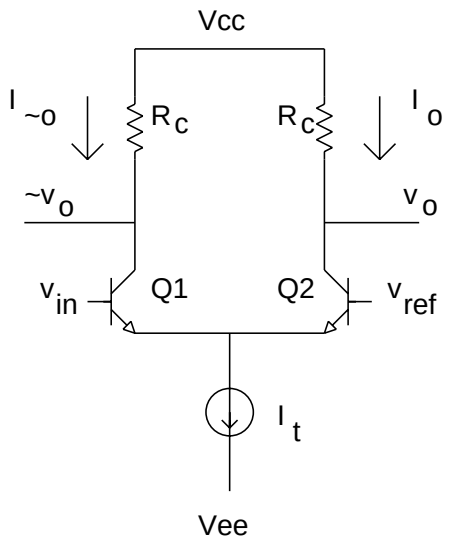

Figure 2-4: A basic ECL gate

From Equations (7) and (6), we get

$$I_o = \frac{I_t}{1 + exp(x)} . \tag{8}$$

From Equations (2), (3) and (8), the transfer equation is derived as

$$y = \frac{-s}{1 + exp(x)} . \tag{9}$$

The slope of the curve, which is the gain of the gate, can be derived as

$$G = \frac{dy}{dx} = \frac{s}{exp(-x) + 2 + exp(x)} . \tag{10}$$

Plotting the transfer curve and the gain with both y and x normalized to s, universal transfer curves for the basic ECL gate are obtained for two different normalized voltage swings, *s1* and *s2*, as shown in Figure 2-5.

Note that both the transfer curve and its derivative, the gain, depend *only* on s, the voltage swing which is normalized to the thermal voltage v_T. The larger the voltage swing, the narrower the transition region, the higher the voltage gain at threshold (x=0) and, obviously, the larger the noise margin.

To derive the noise margin as a function of the voltage swing, we replot the transfer curve of a non-inverting gate in Figure 2-6 with the geometrical representations of noise margins. Setting G, the gain, to one we get

$$x_g^{\,h} = ln(s - 2) \quad and \quad x_g^{\,l} = - ln(s - 2) \tag{11}$$

assuming that

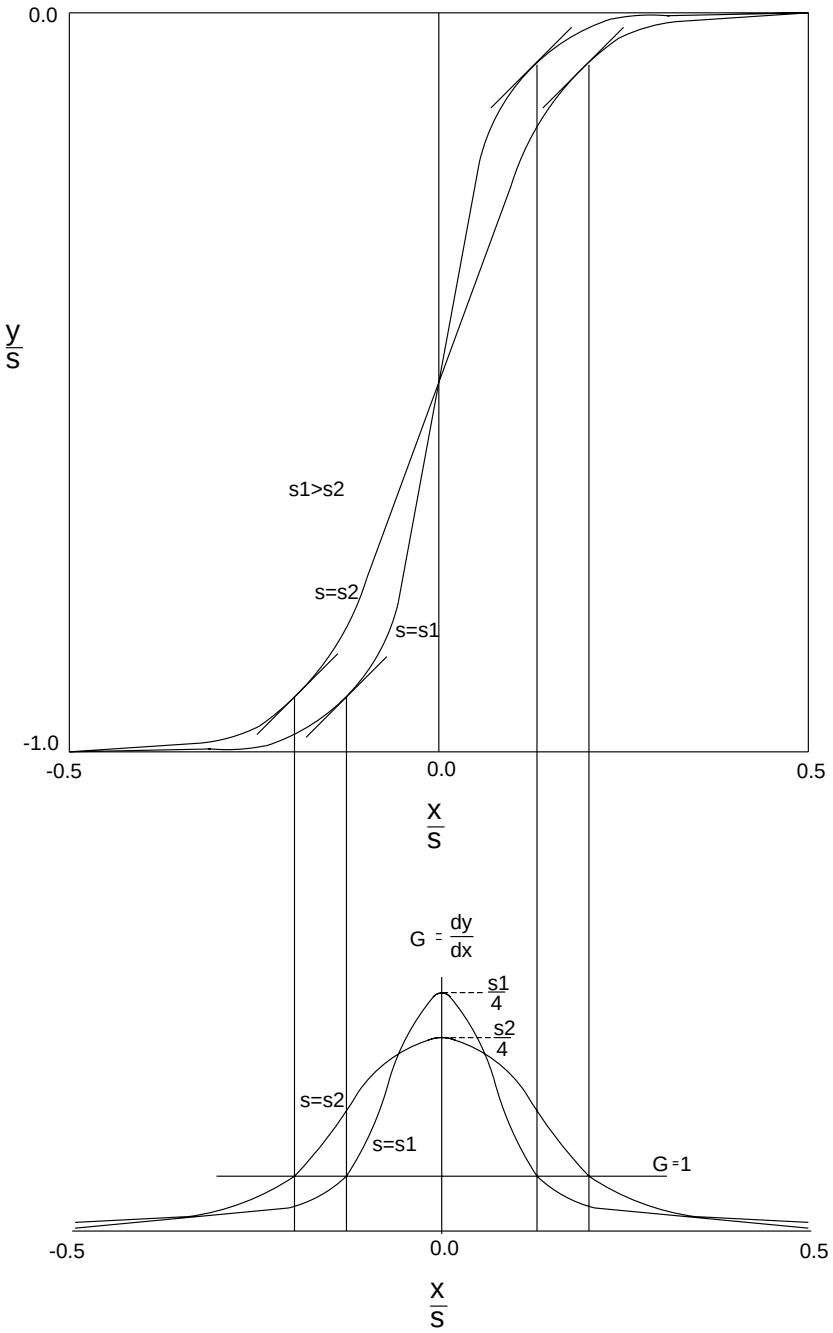

Figure 2-5: The transfer curve and the gain of a non-inverting gate

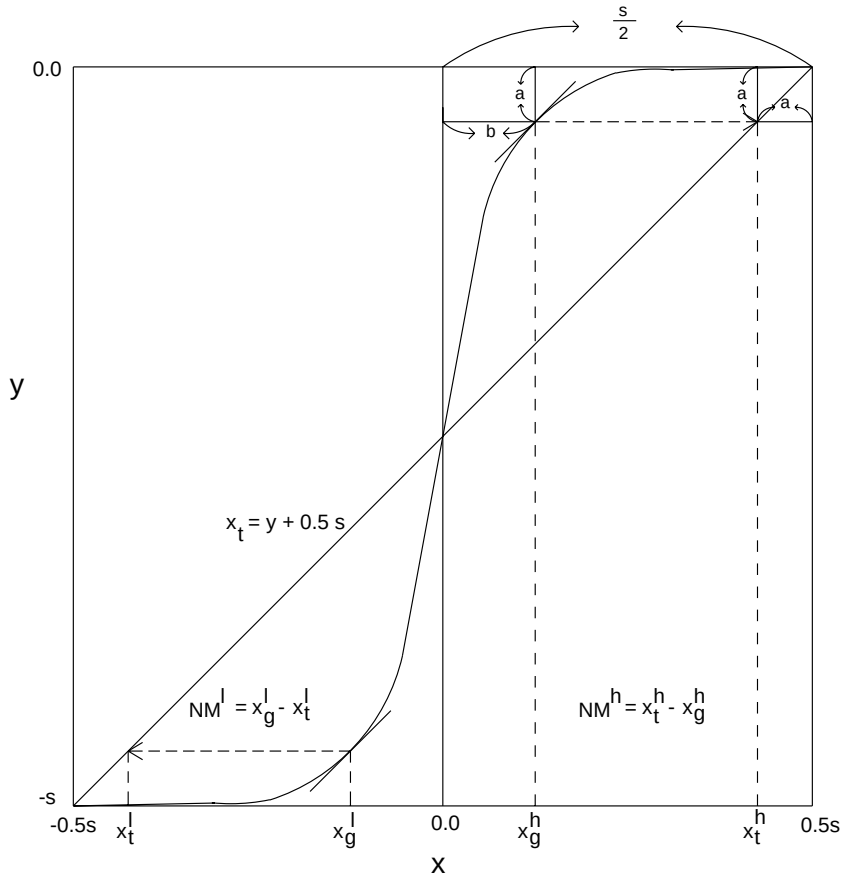

Figure 2-6: The transfer curve of a non-inverting gate with the geometrical representations of noise margins

$$2 >> e^{-x_g{}^h} \quad and \quad 2 >> e^{x_g{}^l}. \tag{12}$$

The superscripts indicate whether the logic level is either high or low.

Combining Equations (11) and (12), this assumption can be reduced to

$$s >> 2.5. \tag{13}$$

For all practical purposes, this is always true. For example, for 125 ° C and a voltage swing of 500 mV, s ~ 14.58, one sees that Equation (13) is well satisfied. Since the transfer curve is symmetric, we shall derive the high noise margin only. From Figure 2-6, the high noise margin is simply

$$NM^h = \frac{s}{2} - a - b, \tag{14}$$

where $a = |y(x_t^h)| = \frac{s}{s-1}$ from Equation (9), and $b = x_t^h = ln(s-2)$. Thus,

$$NM^h = x_t^h - x_g{}^h = \frac{s}{2} - \frac{s}{s-1} - ln(s-2). \tag{15}$$

Similar derivation for the low noise margin, NM^l, yields the same formula.

2.3. Noise Margin Variation

As pointed out in the previous section, noise margin for an ECL gate is only a function of the normalized voltage swing. Noise margin will only vary through variations of the normalized voltage swing.

The derivative of high noise margin with respect to s is

$$\frac{dNM^h}{ds} = \frac{1}{2} + \frac{1}{(s-1)^2} - \frac{1}{s-2}. \tag{16}$$

Equations (15) and (16) are plotted in Figures 2-7 and 2-8 respectively. Once the voltage swing of an ECL differential pair is known, the noise margin and its derivative with respect to the swing can be easily determined from the plots.

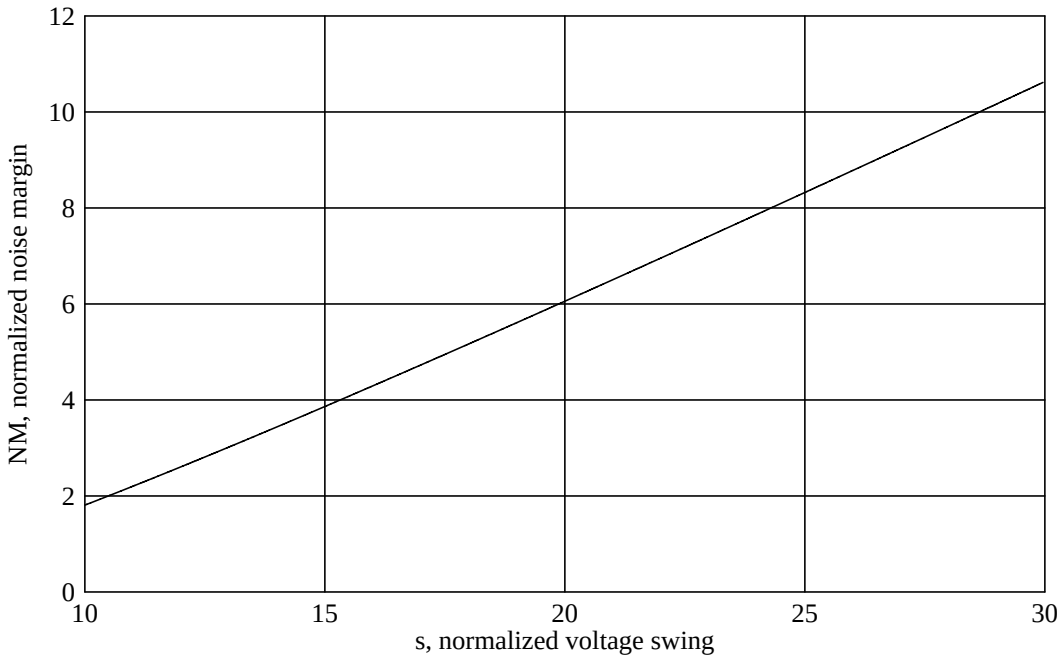

Figure 2-7: Normalized noise margin versus normalized voltage swing

Table 2-1 tabulates the noise margin at selected temperatures and voltage swings. It is clear from the derivative plot that noise margin increases almost linearly as the voltage swing increases.

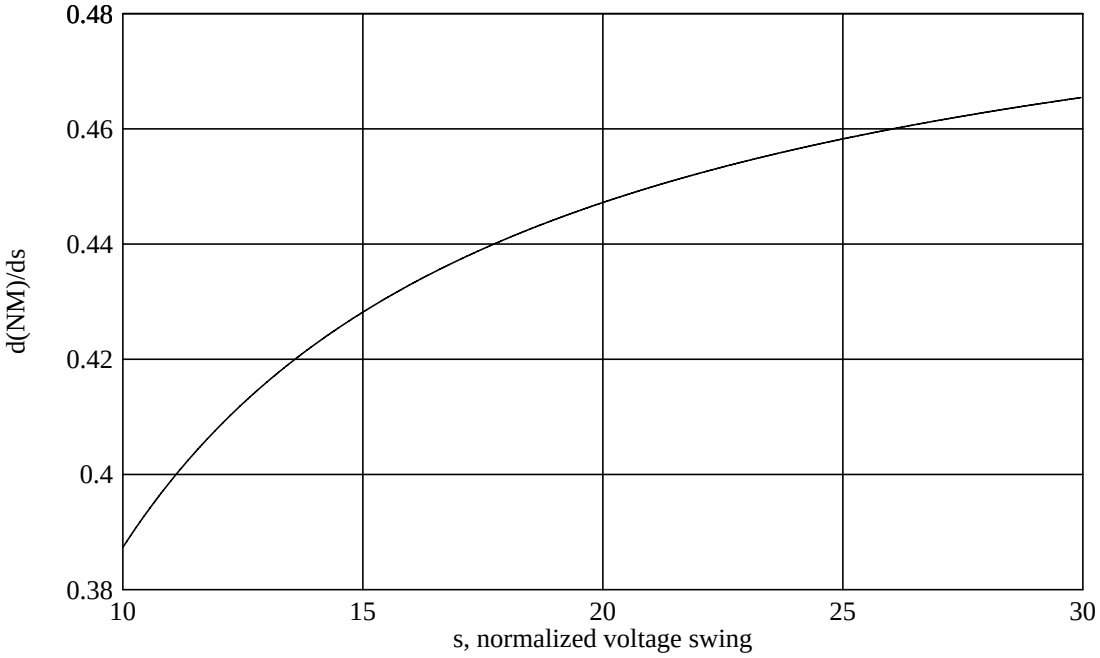

Figure 2-8: Derivative of normalized noise margin versus normalized voltage swing

Noise Margin [mV]

Temperature [C]	Voltage Swing [mV] 400	500	600	750	850	v_T [mV]
0	111	156	201	271	317	23.53
27	105	149	194	263	310	25.85
85	93	135	179	247	308	30.58
125	85	126	169	236	282	34.30
155	79	120	162	229	274	36.58

Table 2-1: Noise margin for different temperatures and voltage swings

3. DC Noise Sources

The nature of noise and various noise source types in an ECL environment will be discussed. Here, two types of noises are distinguished, intrinsic and extrinsic. Intrinsic noise is the type of noise associated with specific circuit configurations such as multiple fan-in, series gating, etc. Extrinsic noise is the type of noise associated with the circuit environment, such as ohmic drops on metal lines, temperature differences, short and long range process variations, etc.

3.1. Definition

As depicted in Figure 3-1, anything that causes v_{oh}-v_{ref} or v_{ref}-v_{ol} to degrade is defined as a noise source. The degradation of the former causes high noise margin NM^h to degrade while the degradation of the latter causes low noise margin NM^l to degrade. For example, if a certain IR drop causes all v_{oh}, v_{ol}, and v_{ref} to shift up by Δ, there is no degradation of the noise margin. But if it only causes v_{ref} to shift up by Δ, NM^h decreases while NM^l increases by Δ.

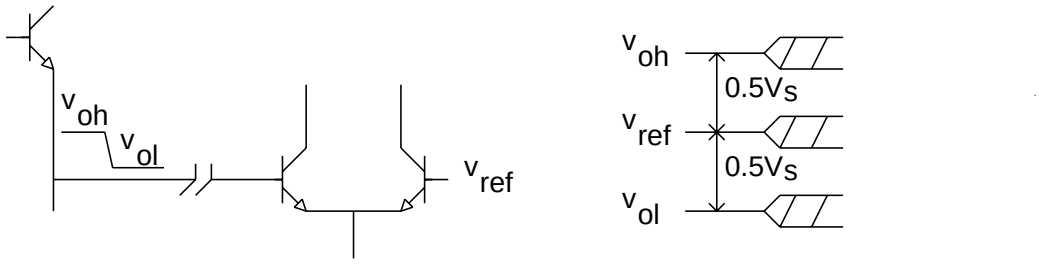

Figure 3-1: Definition of noise for a differential pair.

3.2. Intrinsic Noise

Intrinsic noise occurs in certain types of circuit configurations. In this section we will discuss three basic types of noise arising from current sharing, incomplete switching and V_{be} variations of level shifting.

3.2.1. Current Sharing Noise

Noise arising from current sharing is ubiquitous in ECL designs. Typical examples are gates with multiple fan-in, wired-OR (emitter-ORing) and emitter-ANDing (in multi-emitter decoders, diode decoders, or EFL circuits), as depicted in Figure 3-2.

The fundamental problem here is that any of the n-way input transistors can possibly take all I_o or 1/n I_o. From the basic Equation (4), the difference in V_{be} as a result can be expressed as

$$\Delta V_{be} = v_T \, ln(n). \tag{17}$$

Intuitively, ΔV_{be} will be the amount of noise margin lost. We will derive from a generalized gate structure to show that with proper scaling of the reference side transistor, this noise can be reduced down to half.

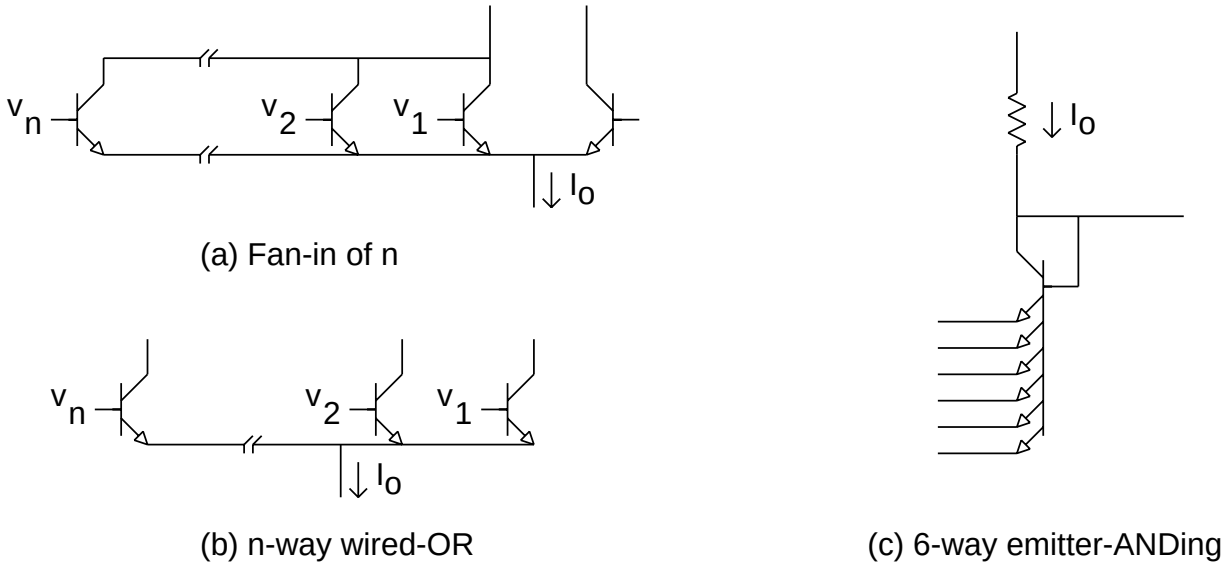

Figure 3-2: Typical examples of circuits with current sharing noise

3.2.1.1. Multiple Fan-In

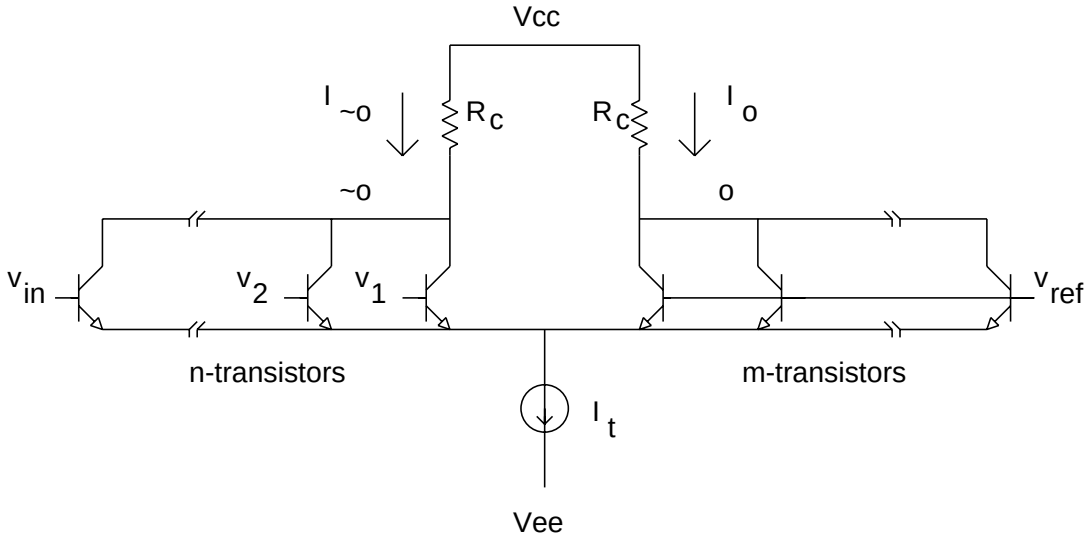

Figure 3-3: A generalized ECL gate

Figure 3-3 depicts an ECL gate with fan-in of *n* on the input side and *m* transistors in parallel on the reference side. These transistors are of the same size. Analogous to the derivation of Equations (6) and (9), if we assume that all *n* inputs are switching together, we have

$$\frac{I_{\sim o}}{I_o} = \frac{n}{m} exp(x), \tag{18}$$

and

$$y = \frac{-s}{1 + \frac{n}{m}\,exp(x)} = \frac{-s}{1 + exp[x + ln(\frac{n}{m})]}. \tag{19}$$

Assuming n > m, the transfer curve is shifted by $ln(\frac{n}{m})$ toward the negative x direction. This is shown in Figure 3-4 as y^l. In unnormalized terms, this means that the low noise margin NM^l has decreased and the high noise margin NM^h has increased by an amount $v_T\, ln(\frac{n}{m})$. For *m* equal to one, this is exactly the same as Equation (17). This is the worst case for the low noise margin but not for the high noise margin. Similar to Equations (11) and (15), the unity-gain point and the low noise margin are obtained as

$$x_g^{\,l} = -\,ln(s - 2) - ln(\frac{n}{m}) \tag{20}$$

and

$$NM^l = \frac{s}{2} - \frac{s}{s-1} - ln(s-2) - ln(\frac{n}{m}). \tag{21}$$

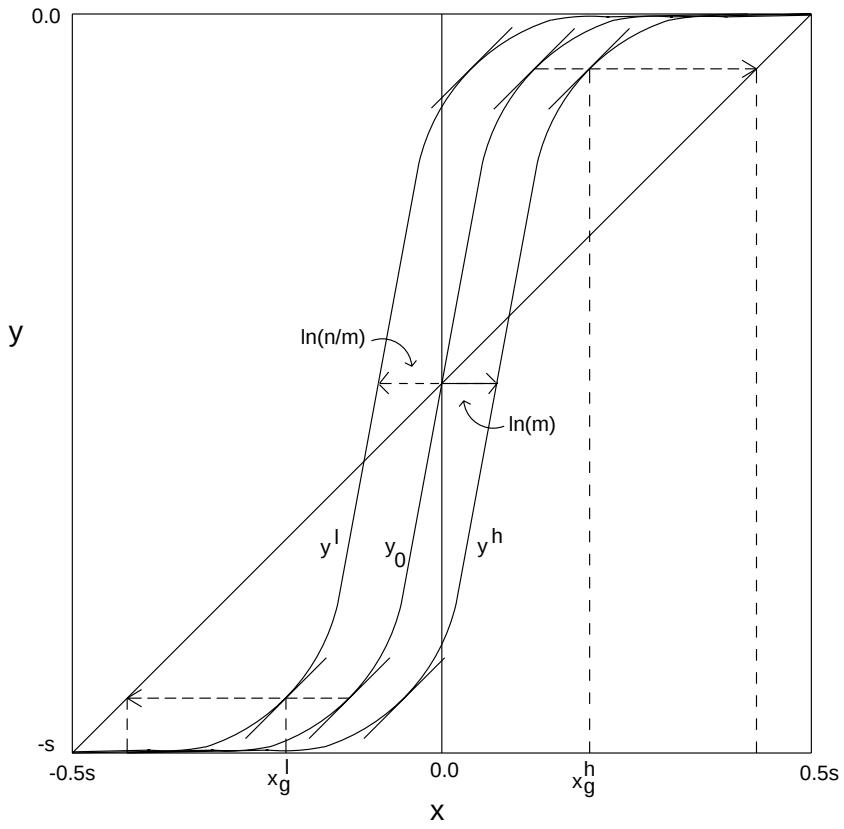

Figure 3-4: The transfer curve of a generalized gate

If one and only one of the *n* input transistors is switched against the *m* parallel reference transistors while all other *n-1* inputs stay at the highest possible low x_L but within the noise margin, Equation (19) becomes

$$y = \frac{-s}{1 + \frac{1}{m}\,exp(x) + \frac{n-1}{m}\,exp(-|x_L|)} \approx \frac{-s}{1 + exp[x - ln(m)]}, \tag{22}$$

assuming

$$\frac{n-1}{m}\,exp(-|x_L|) < \frac{n-1}{m}\,exp(x_g{}^l) = \frac{n-1}{n}\,\frac{1}{s-2} << 1\ , \tag{23}$$

which is a similar condition as dictated by Equation (13).

Note that $x_L < x_g{}^l$ is required to satisfy the low noise margin. In this particular case, the transfer curve is shifted by $ln(m)$ towards the positive x direction. Therefore, the high noise margin has decreased and the low noise margin has increased by $v_T\ ln(m)$ as shown in Figure 3-4. Similarly, the unity-gain point and the high noise margin are obtained as

$$x_g{}^h = ln(s - 2) + ln(m) \tag{24}$$

and

$$NM^h = \frac{s}{2} - \frac{s}{s-1} - ln(s-2) - ln(m). \tag{25}$$

From Equations (21) and (25), one sees that if *m* is set to $\sqrt{n}$, the high noise margin is the same as the low noise margin, and the loss of noise margin as compared to the basic gate becomes $v_T\ ln(\sqrt{n}) = 0.5\ v_T\ ln(n)$. This is only one half of that described in Equation (17).

If the inverting output is considered, as shown in Figure 3-5, the result is just the opposite. Where noninverting outputs suffer losses of high noise margin, inverting outputs suffer losses of low noise margin by the exact same amount.

Here are the guidelines:

- *The effect of having n input transistors (or one input transistor with n times the size) switched against one reference transistor is to shift the reference voltage down by $v_T\ ln(n)$. For a noninverting output, it means the low signal level suffers a degradation of $v_T\ ln(n)$, but the high signal level suffers no degradation. However, for an inverting output it means the high signal level suffers a degradation of $v_T\ ln(n)$, but the low signal level suffers no degradation.*
- *For a gate with a fan-in of n, the loss of noise margin can be reduced to 0.5 $v_T\ ln(n)$ if the reference transistor is sized up by $\sqrt{n}$ as compared to the input transistors. When the transistor is resized, losses of noise margin for high and low signal levels are equal for both inverting and noninverting gates. However, increasing transistor size will naturally increase capacitances. Tradeoffs between DC noise margin and AC perfomance must be considered.*

3.2.1.2. Wired-OR Configurations

Armed with the above results, the wired-OR configuration can be easily analyzed. Figure 3-6(a) shows a wired-OR output v_o driving a differential pair. Figure 3-6(b) shows the signal levels where thick lines correspond to unperturbed levels of a simple gate. The high output varies from the simple gate level with between one and n transistors on, while the low output always corresponds to n transistors on and is

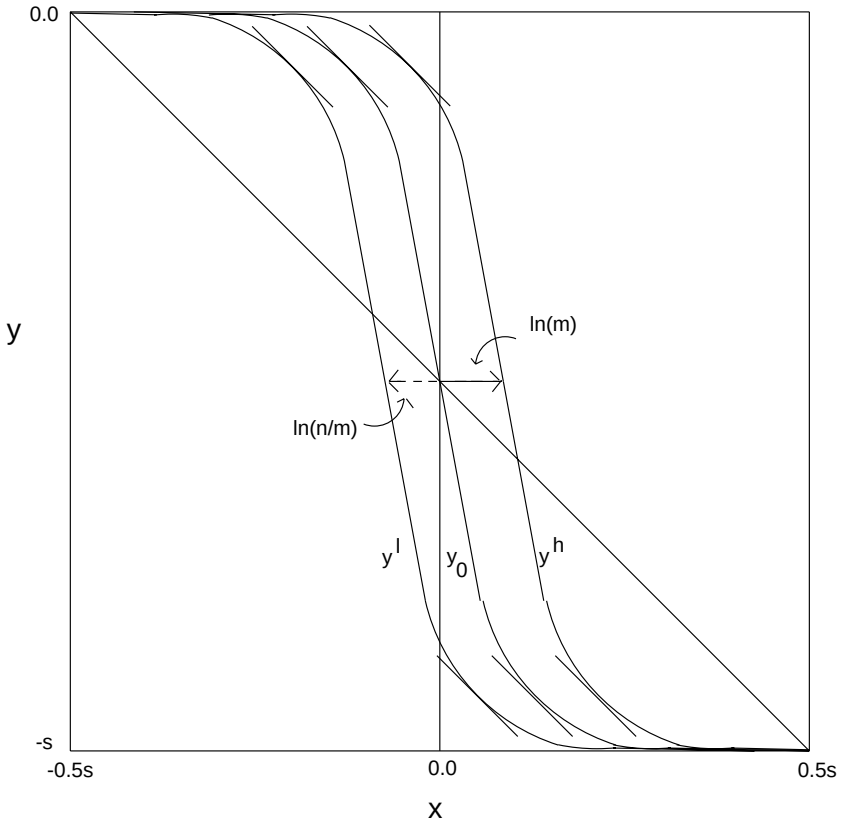

Figure 3-5: The inverting transfer curve of a generalized gate

shifted up by $v_T\ln(n)$. As depicted in the figure, if v_{ref} is shifted up by $0.5v_T\ln(n)$, the resulting level will be exactly in the middle of the worst case output levels, which is in the center of the lowest high (one transistor on) and the highest low (n transistors on).

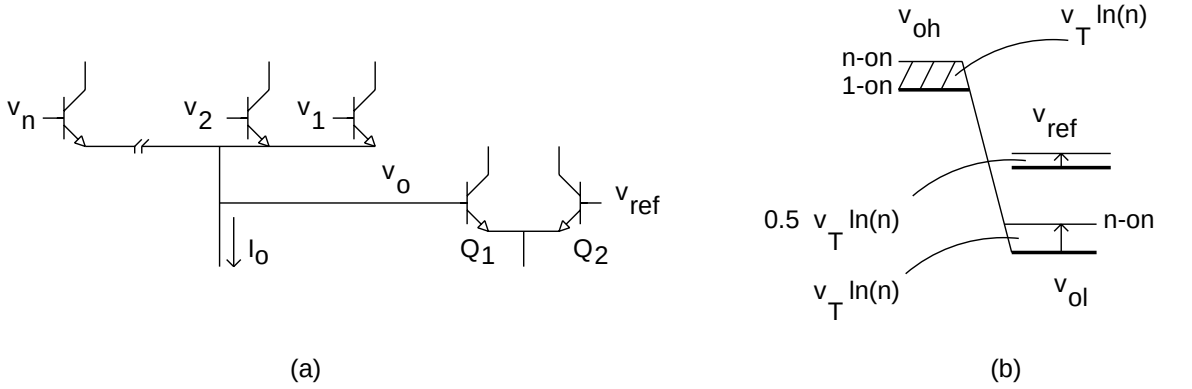

Figure 3-6: Wired-OR configuration

There are two ways of achieving this goal. One can either literally shift the reference voltage up by $0.5v_T\ln(n)$ with customed circuitry, or, as described in the first guideline above, one can size up the reference side transistor, Q_2, by $\sqrt{n}$. Here are similar guidelines:

- *For an n-way wired-OR driving a differential pair, the loss of noise margin is only 0.5 v_T ln(n) if the reference transistor Q_2 is sized up by $\sqrt{n}$ as compared to the input transistors Q_1 of the differential pair. If the reference transistor remains the same size as the input transistors, for noninverting gates there is no loss of noise margin for high inputs, but the loss of noise margin for the low inputs will be v_T ln(n).*
- *If the n-way wired-OR is not driving a complex gate with multiple fan-in where simple resizing cannot be done without affecting other inputs, the loss of noise margin takes the full value of v_T ln(n). In this case, the important parameter is the sum of n for wired-OR and number of OR inputs at the lower level.*

3.2.1.3. Emitter-ANDing

For emitter-ANDing, similar optimization to wired-ORing can be applied if it is driving a differential pair. For example, as depicted in Figure 3-2(c), the output of the 6-way decoder has its output low level shifted up by $v_T\ln(6)$. Assuming the output is to be compared to a reference voltage, one can shift up the reference by $1/2v_T\ln(6)$ to halve the noise.

Other situations may arise from application to application. Based on what has been discussed, one can easily figure out the loss of noise margin due to current sharing type circuits.

3.2.2. Incomplete Switching Noise

Incomplete switching is defined as shown in Figure 3-7. The problem here is that the degraded upper tree current results in a loss of low noise margin. If we define $\rho = I_t'/I_t$, then the loss of low noise margin is simply

$$\Delta NM^l = v_s(1-\rho)\,, \tag{26}$$

where v_s is the swing corresponding to I_t.

Multi-level series gating is the obvious candidate. Both two-level and three-level series gatings will be discussed. The degradation of I_t' will also be considered, as well as the method of compensating this incomplete switching noise.

3.2.2.1. Two-Level Series Gating

Figure 3-8 shows one case of a multi-level series gated ECL gate where the lower level consists of a simple differential pair. Here, the concern is that when the current is steered through transistor Q_a in the worst case, what is the relation between I_t and I_t'? Ideally, if $I_t = I_t'$ there is no loss of noise margin due to the extra level of series gating because the voltage swing for the upper level remains the same. Consider the single-ended case where $v_b=v_{ref}$. Referring back to Figure 2-6, the worst case I_t' occurs when v_a-v_{ref} is at x_g^h. In this situation the inputs have lost all the noise margin and are at the unity-gain point.

From Equations (6) and (11), we get

$$\frac{I_t'}{I_t - I_t'} = exp(x_g^h) = s-2, \tag{27}$$

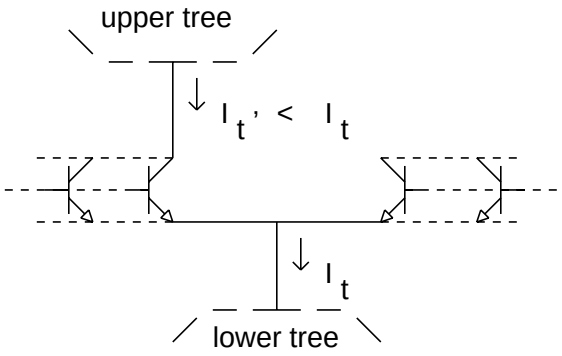

Figure 3-7: The definition of incomplete switching

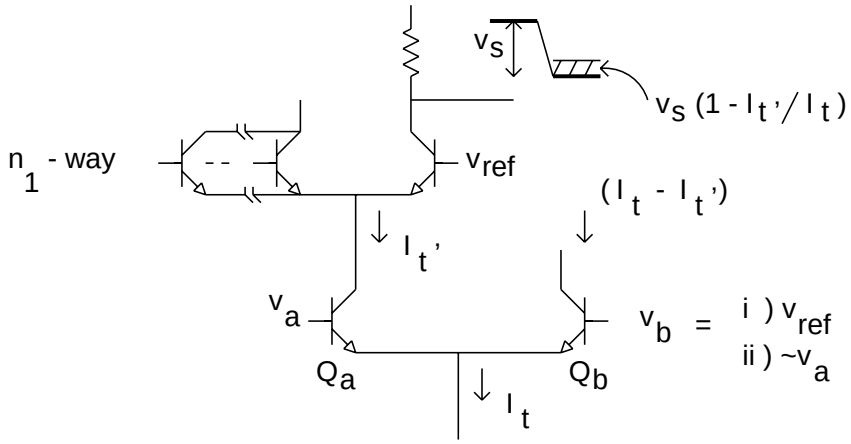

Figure 3-8: Two-level series gating

or

$$\frac{I_t'}{I_t} = \frac{s-2}{s-1}. \tag{28}$$

As depicted in Figure 3-8, where the thick lines represent the unperturbed signal levels, the amount of loss in the low noise margin can be expressed as

$$\Delta NM^l = v_s\,(1 - \frac{I_t'}{I_t}) = \frac{v_s}{s-1}. \tag{29}$$

Note that the high noise margin is in fact slightly improved since v_{oh} can only become more positive due to the incomplete switching.

In the case where $v_b = \sim v_a$, where the gate is being differentially driven, the worst case occurs when v_a is at x_g^h and v_b is at x_g^l. Similar to the above derivation, we have

$$\frac{I_t'}{I_t} = \frac{(s-2)^2}{(s-2)^2+1} \tag{30}$$

and

$$\Delta NM^{l} = \frac{v_s}{(s-2)^2 + 1}. \tag{31}$$

Note here that the differential signal swing only needs to be half the voltage swing since all common-mode noise is excluded. In fact, the noise margin of a half swing differential drive is much better than a full swing single-ended drive. Figure 3-9 depicts another case of two-level series gating where the lower level has a fan-in n_2. Assuming that the reference transistor is properly sized up by $\sqrt{n_2}$ according to the guideline discussed in section 3.2.1, the worst case I_t' occurs when all of the n_2 inputs are at the unity-gain point corresponding to the multiple fan-in case as described by Equation (20). With n/m= $\sqrt{n_2}$, the current ratio becomes

$$\frac{I_t'}{I_t - I_t'} = \frac{1}{\sqrt{n_2}} exp(-x_g^{l}) = s-2, \tag{32}$$

which is the same as Equation (27). Accordingly, the loss of noise margin is the same as that in Figure 3-8 which is described by Equation (29). The degradation of the tree current due to the case of a second level multiple fan-in is the same as that of a simple second level pair driven differentially. This is naturally true considering the way the down-shift of the unity-gain point was derived. All we really need to differentiate is whether the second level is driven differentially or single-endedly.

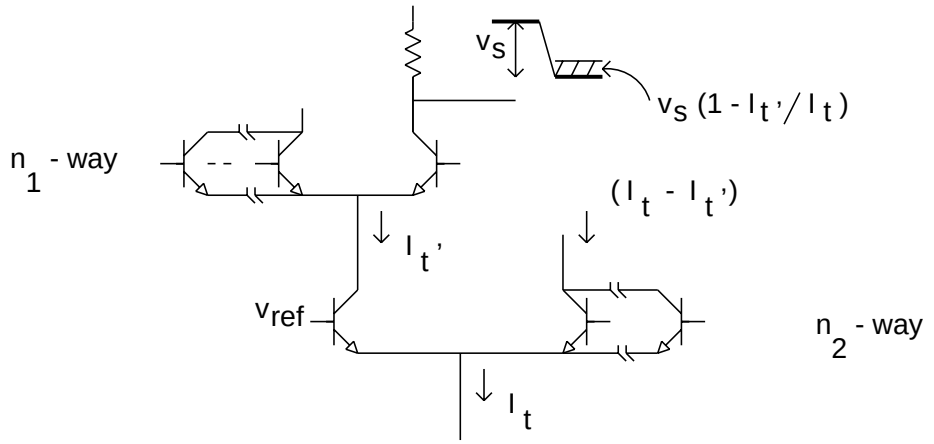

Figure 3-9: Two-level series gating with multiple fan-in on the lower level

3.2.2.2. Three-Level Series Gating

A three level series gated structure is shown in Figure 3-10. Based on the previous discussion, there are three possible relations between I_t'' and I_t, depending on whether the lower levels are driven differentially or single-endedly.

Case 1: if all lower levels are driven single-endedly, from Equation (28), we get

$$\frac{I_t''}{I_t} = \left(\frac{s-2}{s-1}\right)^2. \tag{33}$$

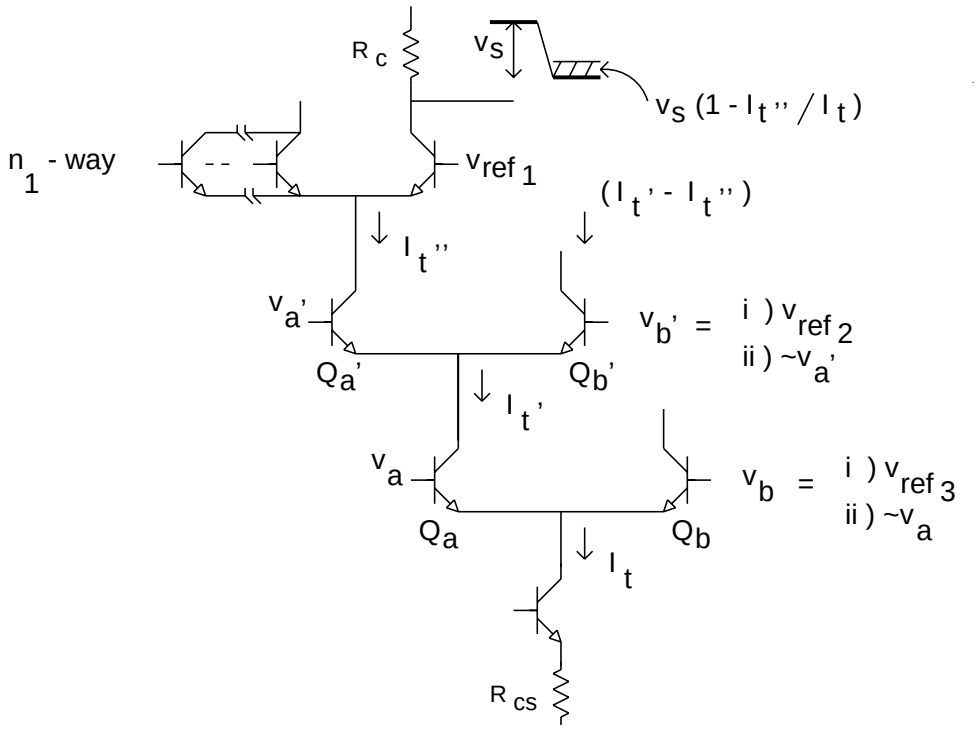

Figure 3-10: Three-level series gating

Case 2: if one of the lower levels is driven differentially and one single-endedly, from Equations (28) and (30) we get

$$\frac{I_t''}{I_t} = \frac{s-2}{s-1}\frac{(s-2)^2}{(s-2)^2+1}. \tag{34}$$

Case 3: if all lower levels are driven differentially, from Equation (30) we get

$$\frac{I_t''}{I_t} = \left(\frac{(s-2)^2}{(s-2)^2+1}\right)^2. \tag{35}$$

3.2.2.3. α Degradation

In Figure 3-11, a path of a three level tree is shown. Assuming the current switches one hundred percent to the path shown, there is still the degradation of current due to the base current as we move up the tree. The percentage degradation in the voltage swing can be expressed as $\rho = (1-\alpha^n)$, where n is the number of levels of series gating. If $\alpha = 0.99$, each extra level causes a loss of low noise margin of one percent of the voltage swing. Note that the effect is the same as that of the multi-level series gatings.

Theoretically this type of noise can be somewhat compensated. For example, if the output of an incomplete switching gate drives a simple differential pair, one can shift the reference voltage of the driven gate to halve the incomplete switching noise the same as the wired-OR situation discussed earlier. But if the driven gate is a complex gate where shifting the reference voltage affects other inputs, it is not feasible.

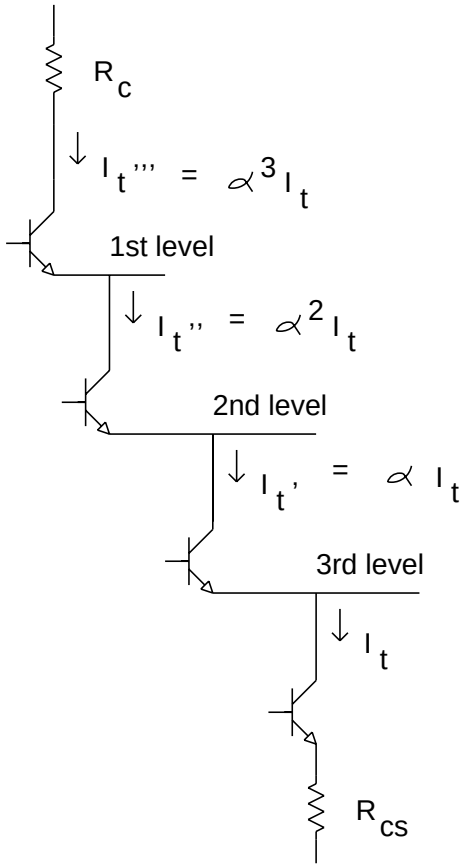

Figure 3-11: α degradation

An alternative is to modify the ratio of R_c and R_{cs} such that $R_c = \alpha^n R_{cs}$ so the degraded tree current generates the desired swing. There are three problems to this solution. Unless the layout grid is fine enough, one might not be able to resolve the 3% difference in resistances in the case of α compensation. In addition, the matching is degraded. Secondly, in the case of multi-level series gatings, since one does not always get the worst case condition, the added swing slows down the switching speed. Most seriously, β usually is not well controlled. It is difficult to predict the value for α.

Here are the guidelines:

- *All cases of multi-level series gating result in a loss of low noise margin, as* $\Delta NM^l = v_s(1-\rho)$, *where* ρ *is the ratio between current actually flowing through the resistor load and the total tree current.*
- *If the incomplete switching gate drives a simple differential pair similar to that discussed in a wired-OR situation, the reference voltage of the driven gate can be shifted to halve the noise.*
- *The ratio of* R_c *to* R_{cs} *can be modified to compensate the current degradation. Care should be exercised as to the real benefit of this option.*

3.2.3. V_{be} Variations of Emitter Followers

The emitter follower plays a very important role in ECL designs. It drives the capacitive load and shifts the signal level down to the desired value. One of the most important matchings in ECL designs is, in fact, the matching of the current density of the emitter follower, which guarantees matching of the diode drops in various parts of the circuits.

3.2.3.1. Pull-Down Resistors

In some ECL designs, a -2 volt power supply commonly referred to as V_{ee2} is used to generate the current source for emitter followers. As depicted in Figure 3-12, one sees that the current of the emitter follower changes as the output switches states. This results in variations of the diode drop V_{be} and hence a loss of noise margin as depicted in part (b) of the figure. Again, thick lines in the figure show the unperturbed levels. Assume that the emitter follower and the pull-down resistor are sized with respect to some mean current I_o. In order to balance both the high and the low side, it is required that

$$\Delta h = v_T \, ln(\frac{I_{oh}}{I_o}) \equiv \Delta l = v_T \, ln(\frac{I_o}{I_{ol}}) \, . \tag{36}$$

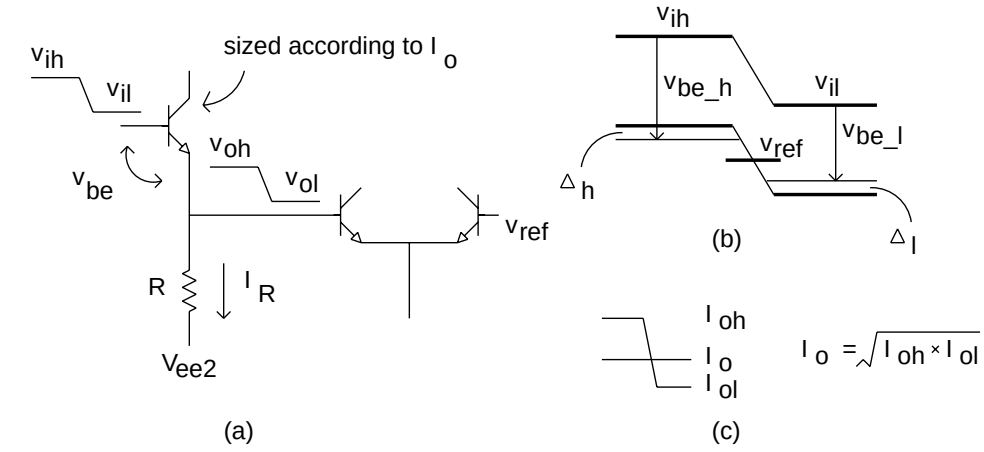

Figure 3-12: Pull-down resistors for emitter followers

As depicted in part (c) of the figure, I_o is simply the geometric mean of I_{oh} and I_{ol}.

The value of the resistor is determined by

$$R = \frac{\sqrt{(v_{oh} - v_{ee2})\,(v_{ol} - v_{ee2})}}{I_o}, \tag{37}$$

and the loss of noise margin can be easily derived as

$$\Delta = v_T \, ln(\sqrt{\frac{v_{oh} - v_{ee2}}{v_{ol} - v_{ee2}}}) \, . \tag{38}$$

For example, if v_{oh}=-0.9, v_{ol}=-1.4, V_{ee2}=-2.0, and v_T=0.03, then Δ=9.1 mV. Strictly speaking, the formula needs to be iterated to take into account the fact that the v_{oh} and v_{ol} values are changed as V_{be} is modified. But the computation error is very small and is hence neglected here. Note that the IR drops on the power distribution and the power supply variations are not accounted for here. In later sections where IR drops are discussed, the noise discussed here will be revisited.

3.2.3.2. Fan-Out

The fan-out issue is usually not a concern unless the fan-out is large or the tree current of the driven gate is large. Figure 3-13 shows two situations of fan-out. Part (a) consists of a pull down resistor while part (b) consists of a real current source.

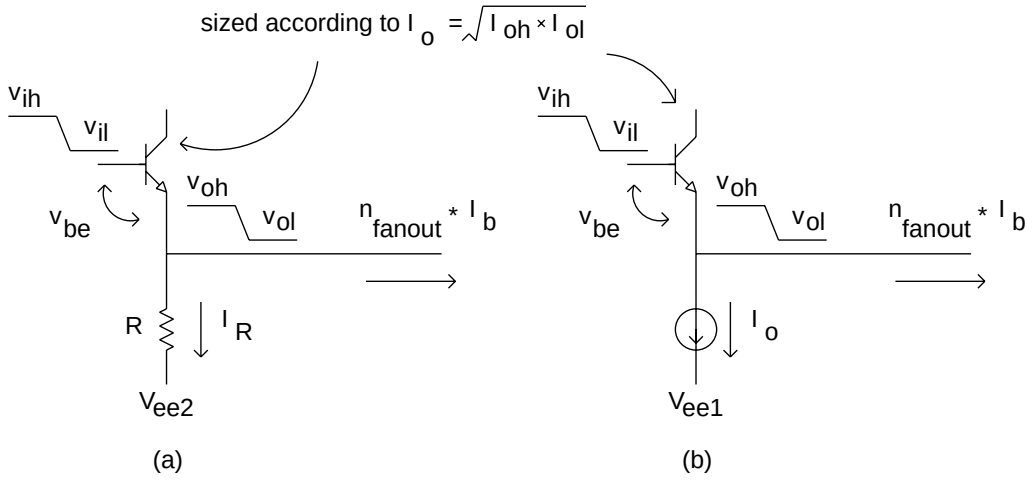

Figure 3-13: Multiple fan-out

The basic problems are exactly the same as that discussed in the previous section. For part (a), the equations for high and low output current are expressed as

$$I_{oh} = \frac{v_{oh} - V_{ee2}}{R} + n_{fan-out} \times I_b, \tag{39}$$

and

$$I_{ol} = \frac{v_{ol} - V_{ee2}}{R}. \tag{40}$$

For part (b), the equations for high and low output currents are $I_{oh} = I_o + n_{fan-out} \times I_b$ and $I_{ol} = I_o$, respectively. Given a desired current I_o, one can easily figure out the loss of noise margin by the following equations

$$\Delta NM^h = v_T ln(\frac{I_o}{I_{oh}})$$

and

$$\Delta NM^l = v_T ln(\frac{I_{ol}}{I_o}).$$

In practice, the emitter follower will not be resized unless the fan-out current loading is extremely large. Since the fan-out current loading is only active when output is in the high state, the extra loss of the high noise margin can be simply expressed as

$$\Delta NM^h = v_T ln(\frac{I_{oh}}{I_{oh} + n_{fan-out} \times I_b}) = -v_T ln(1 + \frac{I_{nfan-out} \times I_b}{I_{oh}}).$$

For example, if the fan-out current loading is 10% that of I_{oh}, the extra loss of noise margin on top of the emitter follower is only about 2.86 mV at 85 ° C. So if 3 mV is allocated in the noise budget for fan-out, it is equivalent to say that $n_{fan\text{-}out}$ x I_b has to be less than 10% of I_o.

3.3. Extrinsic Noise

Extrinsic noise is the result of the realistic environment where the circuit operates. The variations of the environment parameters cause the signal levels to drift, resulting in loss of noise margin. The noises caused by the IR drops in interconnect lines and the different types of variations that cause changes in device parameters or drifts of signal levels will be discussed.

3.3.1. IR Drops

The issue of IR drops on the power distribution is particularly a problem in ECL designs for two reasons: small DC noise margin and large DC current. In this section, the noise implications of different types of IR drops will be discussed.

3.3.1.1. IR Drops on the Top Rail

When an IR drop Δ occurs on the top rail (the V_{cc} supply line) between the sending gate and the receiving gate reference generator, Δ amount of either high or low noise margin is lost, depending on the polarity of the drops. Figure 3-14 depicts the situation corresponding to a loss of low noise margin and a gain of high noise margin.

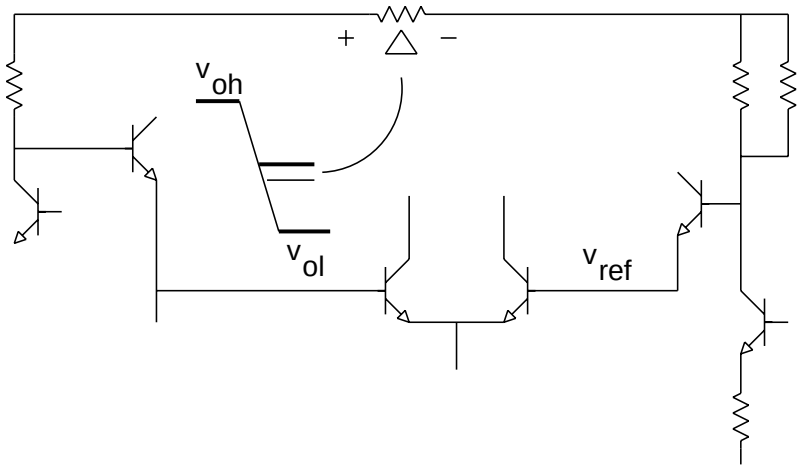

Figure 3-14: IR drops on the top rail, V_{cc}

It can be seen from the figure that if the polarity of Δ is reversed, a gain of low noise margin at the expense of high noise margin results. In theory, this type of noise can be halved, provided that the differential pair is properly sized. In practice, this is hard to do since Δ might not be a well managed quantity. If multiple fan-in exists, there is no way to optimize the gate because inputs are coming from different parts of the chip.

Here is the guideline:

- *IR drops on the top rail always translate into a change of (v_{oh}-v_{ref}) or (v_{ref}-v_{ol}), causing direct loss of either the high or low noise margin.*

3.3.1.2. IR Drops on the Bottom Rail

The bottom rail, V_{ee1}, is the reference rail for all current sources. A band gap generator generates a regulator voltage which is one diode drop plus a voltage swing (v_{be}+v_s) above the bottom rail. The main effect of IR drops on V_{ee1} bus is to cause a change in current generated by current sources.

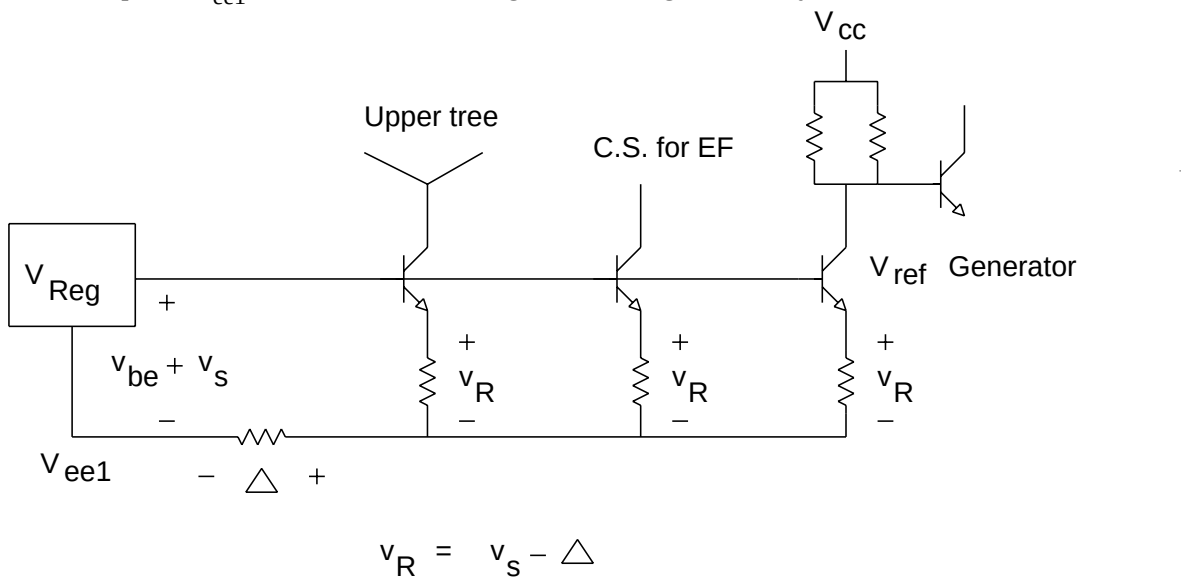

Figure 3-15: IR drops on the bottom rail, V_{ee}

Figure 3-15 depicts three different situations: a current source for a tree, a current source for an emitter follower and a current source for a reference generator. Also shown in the figure is that the voltage across the current source resistors becomes v_s-Δ due to the IR drop.

In the case of a tree, the voltage swing is degraded by Δ . Using the notation before, this is equivalent to ρ= 1-Δ / v_s. A loss of low noise margin of Δ results. The discussion in the previous section applies.

In the case of a current source for an emitter follower, the change in current due to the IR drop induces a change in the V_{be} of the emitter follower, resulting in signal degradation. The loss of noise margin is

$$\Delta NM = v_T ln(1 - \Delta / v_s).$$

For Δ=50 mV and v_s=500 mV, the loss of low noise margin calculated using this equation is only 2.86 mV at 85 ° C.

The noise associated with reference generators will be discussed in Section 3.4.

The IR drop on the other bottom rail, V_{ee2}, directly affects the emitter followers with a pull-down resistor as discussed in section 3.2.3.1. In most digital circuits, this is the only place V_{ee2} is used. From Equation (38) we see that Δ is subject to both v_{oh} and v_{ol} variations which result from V_{cc}, V_{ee1}, and V_{ee2} variations. In the worst case, the equation can be re-written as

$$\Delta = v_T ln(\sqrt{\frac{(v_{oh}-\Delta v_{oh})-(v_{ee2}+\Delta v_{ee2})}{(v_{ol}-\Delta v_{ol})-(v_{ee2}+\Delta v_{ee2})}}), \tag{41}$$

where Δv_{oh} and Δv_{ol} are functions of ΔV_{cc} and ΔV_{ee1}. As discussed earlier, $\Delta v_{oh}=\Delta V_{cc}$ and $\Delta v_{ol}=\Delta V_{cc}+\Delta V_{ee1}$, since they are translated directly into variations of the signal levels. Let us plug in some numbers here. Assuming v_{oh}=-850 mV, Δv_{oh}=150 mV, v_{ol}=-1350 mV, Δv_{ol}=175 mV, v_{ee2}=-2.0 V, Δv_{ee2}=100 + 150 = 250 mV (i.e. 5% of v_{ee2} and IR drop on the V_{ee2} line), and v_T=30 mV (T=85 ° C), the loss of noise margin, Δ is 0.5 $v_T$ln(3.33) = 18 mV.

In chapter 4, the concept of virtual V_{cc} and statistical distribution of the ΔV_{cc} and ΔV_{ee}'s will be introduced. Equation (41) will be revisited and modified.

3.3.1.3. IR Drops on Signal Nets

Two cases of IR drops occurring on signal nets are depicted in Figure 3-16. In general, the IR drop induced by the base current is less of a concern than the IR drop induced by emitter current. But when the signal net is long or the fan-out is large, the product of I and R is no longer negligible, and the degradation of signal levels has to be considered. In practice, the case one must pay attention to is the long wired-OR lines. The left half of Figure 3-16 shows that Δ , the IR drop, causes a down shift of both signal levels. Assuming that the reference voltage stays at the unperturbed level, a loss of high noise margin of Δ results.

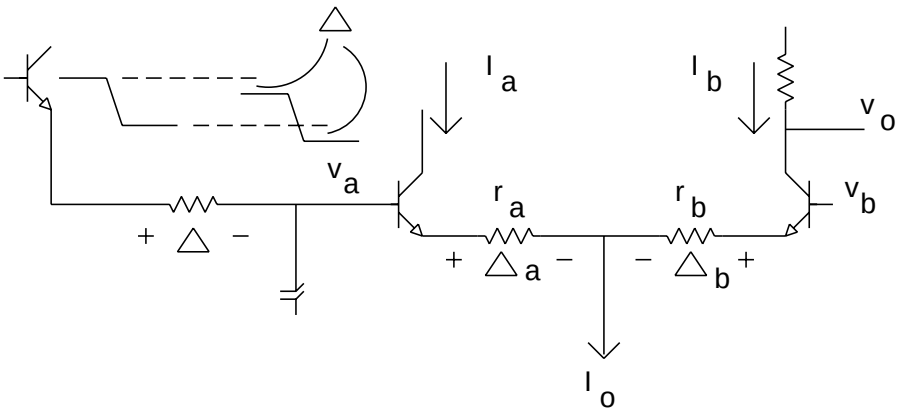

Figure 3-16: IR drops on signal nets

The right half of Figure 3-16 shows a situation in which there is substantial resistance between the two emitters. In some cases, we have to use an interconnect of higher resistivity, such as unsilicided poly to do the local routing. In other cases, maybe for layout reasons, two transistors have to be physically pulled far apart.

The current ratio for the differential pair is derived as

$$\frac{I_a}{I_b} = exp(\frac{v_a - v_b}{v_T}) exp(-\frac{I_a r_a - I_b r_b}{v_T}) = exp(x - \delta), \tag{42}$$

where $\delta = \frac{I_a r_a - I_b r_b}{v_T}$, and $x = \frac{v_a - v_b}{v_T}$.

Similar to the case of a basic ECL gate, the transfer curve in this case is derived as

$$y = \frac{-s}{1 + exp(x - \delta)}, \tag{43}$$

where s and y are the normalized voltage swing and output. This equation is not straightforward to solve since I_a and I_b are functions of x. Let us make the following observations. At the threshold where $I_a = I_b$, the mid-point of the transfer curve is shifted by an amount

$$\delta = 0.5 I_o (r_a - r_b), \tag{44}$$

where $\delta > 0$ if $r_a > r_b$, and $\delta < 0$ if $r_a < r_b$.

If we assume that the dependence of δ on x is weak near the unity-gain point, similar to the derivation before, we have $x_g{}^h = ln(s-2) + \delta_h$ and $x_g{}^l = -ln(s-2) + \delta_l$, where $\delta_h = \delta(x_g{}^h)$ and $\delta_l = \delta(x_g{}^l)$.

At $x_g{}^h$, we have

$$I_a = \frac{s-2}{s-1} I_o, \quad I_b = \frac{1}{s-1} I_o$$

and

$$\delta_h v_T = (\frac{s-2}{s-1} r_a - \frac{1}{s-1} r_b) I_o. \tag{45}$$

Similarly at $x_g{}^l$, we have

$$I_a = \frac{1}{s-1} I_o, \quad I_b = \frac{s-2}{s-1} I_o$$

and

$$\delta_l v_T = (\frac{1}{s-1} r_a - \frac{s-2}{s-1} r_b) I_o. \tag{46}$$

If $\delta_h > 0$, a loss of high noise margin occurs. On the other hand, if $\delta_l < 0$, a loss of low noise margin occurs.

For example, if $r_b = 0$ there is a loss of high noise margin of $\frac{s-2}{s-1} r_a I_o \approx r_a I_o$, while the low noise margin has gained by $\frac{1}{s-1} r_a I_o$. If $r_b = r_a = r$ there is a loss of high noise margin of $\frac{s-3}{s-1} r_a I_o \approx r_a I_o$ and a loss of low noise margin of $r_a I_o$. This slight asymmetry is a result of the approximation.

Note that all of the above discussion applies to the non-inverting output. For the inverting output the complementary results apply. In other words, when the non-inverting output suffers an amount of loss of high noise margin, the inverting output suffers the same amount of loss of low noise margin.

Here are the guidelines:

- *If a finite resistance exists between the emitters of a differential pair and the common node that connects to the lower tree, the threshold voltage and the noise margins are modified according to Equations (44) (45) and (46).*
- *For the non-inverting output, the resistance between the emitter of the input transistors and the common node tends to decrease the high noise margin, while the resistance on the other side tends to decrease the low noise margin.*
- *For the inverting output, the result is the reverse. The resistance between the emitter of the input transistors and the common node tends to decrease the low noise margin, while the resistance on the other side tends to decrease the high noise margin.*

3.3.2. Variations of Device Parameters and Operating Environment

Three different types of variations will be addressed: process variations, temperature variations and power supply variations. In short, the first two types of variations give rise to device parameter variations while the last type affects circuits that depend on V_{cc}-V_{ee1} and/or V_{cc}-V_{ee2}. The main concern for a circuit designer is to understand how his or her circuits will be affected by the variations and how some of the variations can be minimized by circuit design and layout matching techniques.

In ECL designs, basic matchings are expected of (a) transistor characteristics of both input and reference devices, (b) top and bottom resistors in a tree, and (c) V_{be}'s of emitter followers. Since the short range process variation is small, good trackings of input transistors and reference transistors can always be expected, as these transistors are usually physically adjacent. Only when a tree structure is physically apart do we need to consider variations in the transistor characteristics. By the same token, the top and bottom resistors in a tree are also well matched if they are laid out the same way. Except for the α degradation discussed earlier, the voltage swing is translated from the bottom resistor to the top resistor one for one even though the current may vary. In most cases, matching considerations for both (a) and (b) are not much of a problem.

The matching of (c) ensures the correct levels for both signals and references. Intrinsic noises related to (c) were discussed in section 3.2.3. In the extrinsic case, there is the change of V_{be} due to direct variations of either temperature or processing nonuniformity. There is also the indirect change of V_{be} due to resistance variations of the current source resistor. Let us derive the equations. Assuming the voltage across the current source resistor, V_R, is fixed, the current is simply $I_o = V_R / R_o$, where R_o is the mean value for the resistance. The change of current due to the change of resistances follows

$$\frac{\Delta I_o}{I_o} = -\frac{\Delta R_o}{R_o}. \tag{47}$$

The change of V_{be} can be derived as

$$\Delta V_{be} = v_T ln \frac{1 \pm \Delta I_o}{I_o} = v_T ln(1 \pm \frac{\Delta R_o}{R_o}). \tag{48}$$

As discussed in section 3.2.3, the loss of noise margin due to variations of V_{be} is one for one in the worst case. The loss of noise margin due to variation of the emitter follower can be determined by Equation (48).

3.3.2.1. Process Variations

Process variation is a strong function of the technology. In descending order of degrees of variations, there are lot to lot variations, wafer to wafer variations within a lot, and long range and short range variation within a die. Usually, one only worries about the lot to lot variation which gives the worst case tolerances, and the short and long range variation which concerns tracking of devices in close vicinity and on opposite corners of the chip.

Tolerances

	Process variation	Temperature Coefficient
V_{be}	±3 mV	-1.2 mV / C

Resistor Types		Process variation (lot to lot)	(within a slice)
ppoly	800 (8-wide)	±20%	±5%
Implant	600 (8-wide)	± 5%	±2%
	(5-wide)	± 8%	±2%
	(3-wide)	±12%	±2%
Implant	4K	±20%	±5%

Temperature variation

TC	ppoly 800	Implant 600	Implant 4K	Metal
% / C	- 0.1	0.1	0.29	0.4

Table 3-1: Device parameter tolerances due to process and temperature variations

All device parameters are subject to process variations. Table 3-1 shows an example of typical dependencies of selected device parameters on process and temperature variations. Note that the table is by no means complete and these numbers will vary depending on the technology.

In this example, the direct V_{be} variation of 6 mV in the worst case has to be subtracted from the noise margin. If only one type of resistor is used, only the variation within a slice needs to be considered. For example, if only 8-μm wide 800 Ω poly resistors are used, from Equation (48) the loss of noise margin is about 3 mV at 85 ° C. If different types of resistors are used to generate currents for emitter followers, one might have to use the lot to lot variation for the worst case, assuming no correlation exists between

the particular types. Taking the 8-μm wide 800 Ω poly resistor and the 8-μm wide 600 Ω implant resistors, for example, the worst case loss of noise margin is about 7 mV at 85 ° C.

3.3.2.2. Temperature Variations

Depending on the operation environment, temperature variations occur resulting in variations of device parameters. There are two types of variations: local variations (temperature gradients due to hot spots), and global variations (changes of operating temperature).

On-chip temperature gradients occur when hot spots consuming significantly larger than average power exist. Since the V_{be} diode drop has a negative temperature coefficient in the range of -1.2 to -1.5 mV/C, the V_{be} difference is 24 to 30 mV for two junctions with a temperature gradient of 20 ° C. Depending on which junction has a higher temperature, the driving gate or the receiving gate reference generator, it can either cause a loss of low or high noise margin of ΔV_{be}, since it translates directly into a shift of the signal level and/or the reference level.

Since no chip package is ideal, some finite thermal resistance always exists. The seriousness of this type of noise is largely a function of the packaging technology and the power consumption of the chip. Given a package technology and an estimated worst case temperature gradient, the potential loss of noise margin is figured into the noise budget.

Temperature variation as a whole is a slightly different issue. For example, the chip has to be guaranteed to work over a junction temperature from 27 to 125 ° C in typical commercial specification, and from 0 to 155 ° C for military specification. For noise margin the concerns are twofold: the variation of the output of the band gap generator which relates to the voltage swing, and the variation of the thermal voltage related noises. The guideline here is to figure out the worst case junction temperature and its associated worst case noise.

There are other device parameters that change with process and/or temperature variations. For example, the transistor current gain β can vary 20% from lot to lot and it increases with increasing temperature. If a particular circuit design is based on some average β, the loss of noise margin resulting from the drift of the operating point due to the variation of β should be considered in the noise budget. For example, when a PNP current mirror is used, one has to estimate the average β to compensate for the base current in order to mirror the desired amount of current. In such a situation, the percentage variation of the mirrored current resulting from the β variation should be included as a noise source.

3.3.2.3. Power Supply Variations

Power supply variation depends on a lot of factors. It is usually included in the chip specification. Circuit designers assume, for example, that no more than plus or minus five percent variation occurs on the power supply. It is the job of the package and board designers to guarantee the specification. Note that the power supply variations of concern here are global in the sense that all circuits on-chip see the same effect while the variations caused by local IR drops were considered in the previous section.

As mentioned earlier, circuits that depend on V_{cc}-V_{ee1} and/or V_{cc}-V_{ee2} will be affected by power supply variation. Assume that a perfect band gap generator that generates perfect V_{reg}'s for current sources exists; then, most circuits are shielded from the power supply variation except for emitter followers with a single pull-down resistor. The noise that results from these pull down resistors is proportional to a log function of $\{a\Delta V_{cc}+b\Delta V_{ee1}-c\Delta V_{ee2}\}$, which is quite complicated. This particular topic will be further examined in Chapter 4 when a resistor trimming scheme is discussed.

3.4. Noise from Reference Voltage Generation and Distribution

Usually on a chip, there are two units which are related to generation of reference voltages: the generation and distribution of V_{cs} or V_{reg}, the regulated voltage which is one diode drop above V_{cs}; and the generation of V_r's from V_{reg} or V_{cs}. The circuits used to generate V_{cs} or V_{reg} usually are referred to as the *master* reference generators, and the circuits used to generate V_r's usually are referred to as the *slave* reference generators.

3.4.1. Noise Associated with Master Reference Generators

Noise associated with master reference generators is essentially noise associated with IR drop on the bottom rail, as shown in Figure 3-15. Of course, base current also generates IR drop, but it is much smaller than IR drop on the bottom rail. In practice, a master reference generator services a number of slave reference generators which are arranged physically in such a fashion that the total IR drops are limited. It is a trade-off between the design constraints and the noise budget. An example will be given in Chapter 4.

3.4.2. Noise Associated with Slave Reference Generators

On the other hand, noise associated with slave reference generators is essentially generated by base current. V_r's are our notation for reference voltages applied to the bases of the differential pairs. V_{r0} is the reference for the CML level. V_{r1}, V_{r2}, and V_{r3} are the ECL levels with one, two and three diode drops from the CML level, respectively.

In Figure 3-17, (a) shows the generation of V_{r0}, (b) shows a basic CML gate where the signal levels are generated, and (c) shows the relation between the output high and low and the reference voltage V_{r0} where the thick lines represent the ideal, unperturbed levels. Superscript r indicates those notations are with respect to reference.

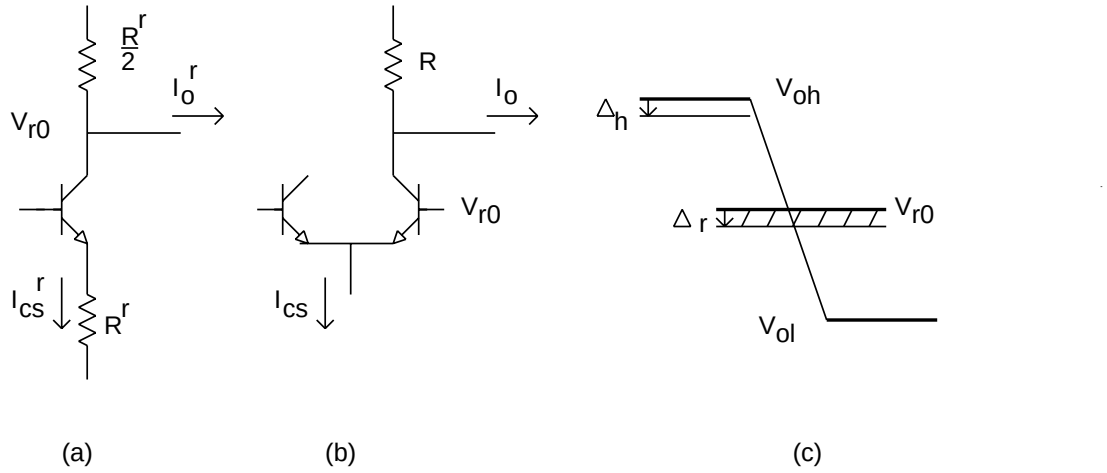

Figure 3-17: V_{r0} generation

Notice that I_o varies from $I_{o\ max}$ to $I_{o\ min}$ as output varies from V_{oh} to V_{ol}, and $I_{o\ min}$ will be zero if the output is not shifted down to lower levels. The signal levels, V_{oh} and V_{ol} and the reference level, V_{r0} can be expressed as

$$V_{r0} = -\frac{R^r}{2}(I_{cs}{}^r + I_o{}^r) = -\frac{V_s}{2}(1 + \frac{I_o{}^r}{I_{cs}{}^r}),$$

$$V_{oh} = -R\,I_{omax} = -V_s\frac{I_{omax}}{I_{cs}}$$

and,

$$V_{ol} = -R\,(I_{cs} + I_{omin}) = -V_s\,(1 + \frac{I_{omin}}{I_{cs}}), \tag{49}$$

where $R^r\,I_{cs}{}^r = R\,I_{cs} = V_s$, the logic swing, is assumed. The loss of noise margin follows as

$$\Delta NM^h = V_{oh} - V_{r0} - V_s/2 = -V_s(\frac{I_{omax}}{I_{cs}} - \frac{I_o{}^r}{2I_{cs}{}^r}),$$

and

$$\Delta NM^l = V_{r0} - V_{ol} - V_s/2 = -V_s(\frac{I_o{}^r}{2I_{cs}{}^r} - \frac{I_{omin}}{I_{cs}}). \tag{50}$$

Note that a loss of noise margin occurs when $\Delta NM < 0$. The complication here is that the difference between I_{omax} and $I_o{}^r$ depends on the state of the gates. From the above equations, we see that the worst case loss of high noise margin is $\Delta NM^h = -V_s(\frac{I_{omax}}{I_{cs}}) = -V_s(\frac{I_{o\_FO}}{I_{cs}} + \frac{I_{omin}}{I_{cs}})$ for $I_o{}^r=0$. Let us define fan-out (FO) as the current loading in the unit of I_{cs}/β. The loss of the high noise margin becomes $V_s(FO+1)/\beta$. The "1" in the numerator is to account for the base current of the level shifter, if there is one. If the CML gate is driving an identical gate (I_{cs}'s are the same), then FO will correspond to the actual number of driven gates. For $\beta=100$ and FO=4, 5% of the voltage swing is lost to noise in the worst case. This corresponds to 30 mV for a 600 mV voltage swing.

The worst case loss of the low noise margin is $\Delta NM^l = -V_s(\frac{I_o{}^r{}_{max}}{2I_{cs}{}^r} - \frac{I_{omin}}{I_{cs}})$ for $I_o{}^r = I_o{}^r{}_{max}$. By comparison, we see that if $\frac{I_o{}^r{}_{max}}{2I_{cs}{}^r} = \frac{I_{omax}}{I_{cs}} + \frac{2\,I_{omin}}{I_{cs}}$, $\Delta NM^h \approx \Delta NM^l$ in the worst case, and the fan-out for the reference voltage V_{r0} is twice that of the circuit fan-out, assuming $I_{cs}{}^r = I_{cs}$ and I_{omin} is negligible.

Here are the guidelines:

- *The loss of high noise margin due to the generation of V_{r0} and CML signal levels is $V_s(FO+1)/\beta$. The loss of low noise margin is the same if the fan-out for the V_{r0} generator, $FO^r = 2*FO*I_{cs}{}^r/I_{cs}$.*
- *If one desires a higher fan-out for the V_{r0} generator, one simply sizes up $I_{cs}{}^r$ to allow larger $I_o{}^r$. FO^r will be scaled by the ratio of $I_{cs}{}^r$ and I_{cs}, by definition.*

Figure 3-18 shows the generation of V_{r1} and V_{r2}. The only difference between Figure 3-18(a) and (b) is that $I_o{}^r$, the loading current, changes from I_{o2} to $I_{o2}+I_{o3}$. Depending on the current loading on V_{r2}, one would choose (b) to save a current source for smaller I_{r3} or (a) for larger I_{r3} since an extra current gain of β is available. Similar to Figure 3-17, Figure 3-18(c) and (d) show a basic ECL gate and the relation between output high and low levels, and the reference level V_{r1}. Again, thick lines depict the unperturbed

levels. Here we will derive the noise associated with V_{r1}, the result of which can be easily generalized to V_{r2} and V_{r3}.

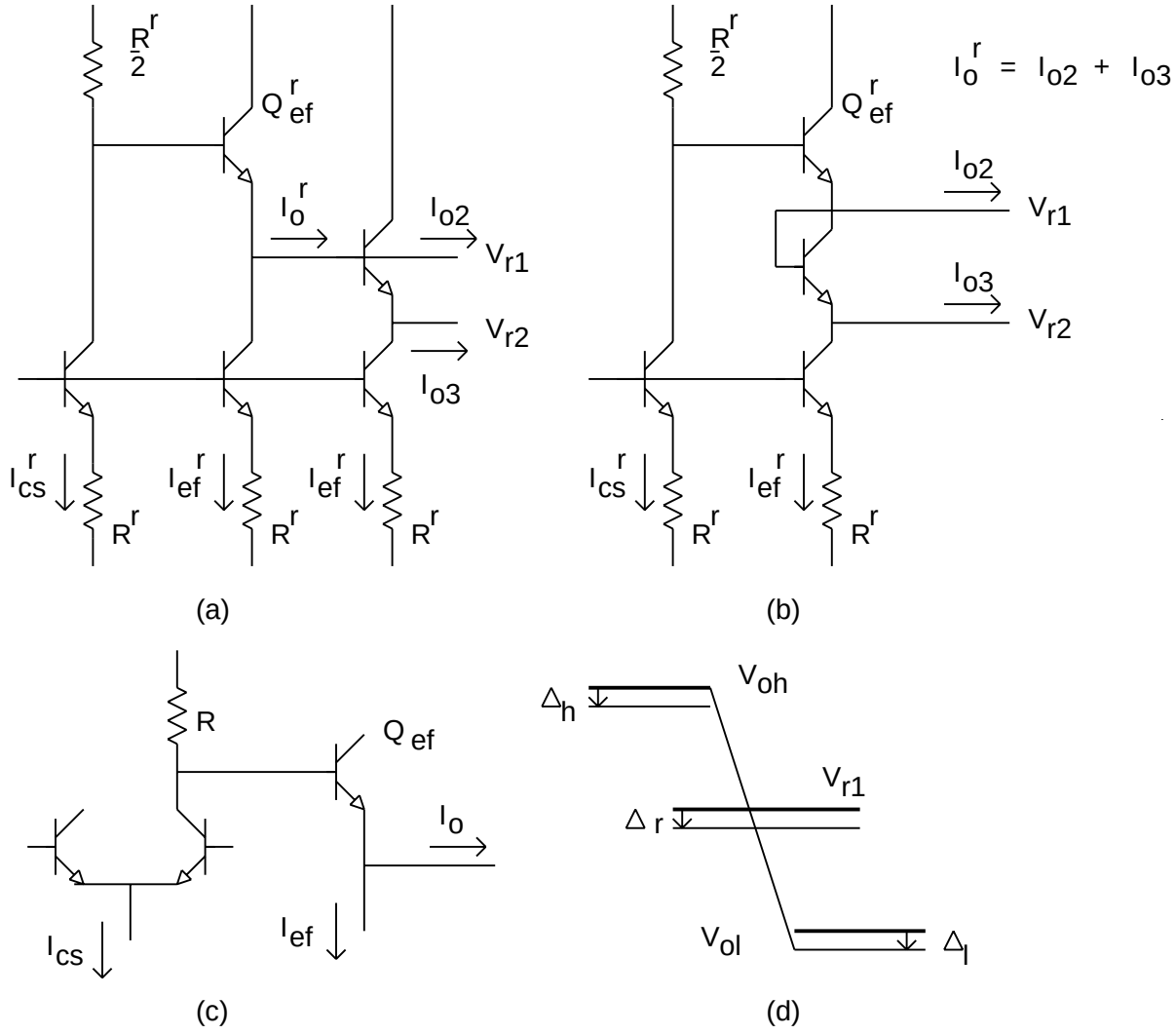

Figure 3-18: V_{r1} and V_{r2} and generation

Similar to the V_{r0} discussion, the signal levels V_{oh}, V_{ol}, and V_{r1} can be expressed as

$$V_{r1} = -\frac{R^r}{2}(I_{cs}{}^r + \frac{I_{ef}{}^r + I_o{}^r}{\beta}) - \phi^r = -\frac{V_s}{2}(1 + \frac{I_{ef}{}^r}{I_{cs}{}^r} + \frac{I_o{}^r}{I_{cs}{}^r}) - \phi^r,$$

$$V_{oh} = -R(I_{cs} + \frac{I_{ef} + I_{omax}}{\beta}) - \phi^h = -V_s(1 + \frac{I_{ef}}{I_{cs}} + \frac{I_o}{I_{cs}}) - \phi^h,$$

and,

$$V_{ol} = -R(I_{cs} + \frac{I_{ef} + I_{omin}}{\beta}) - \phi^l = -V_s(1 + \frac{I_{ef} + I_{omin}}{I_{cs}}) - \phi^l,$$

where $R^r I_{cs}{}^r = R I_{cs} = V_s$ is assumed and ϕ's stand for diode drops. The loss of noise margin follows as

$$\Delta NM^h = V_{oh} - V_{r1} - V_s/2 = -\frac{V_s}{\beta}\left(\frac{I_{omax}}{I_{cs}} - \frac{I_o{}^r}{2I_{cs}{}^r}\right) - \frac{V_s}{\beta}\left(\gamma - \frac{\gamma^r}{2}\right) - (\phi^h - \phi^r),$$

and

$$\Delta NM^l = V_{r1} - V_{ol} - V_s/2 = -\frac{V_s}{\beta}\left(\frac{I_o{}^r}{2I_{cs}{}^r} + \frac{I_{omin}}{I_{cs}}\right) - \frac{V_s}{\beta}\left(\frac{\gamma^r}{2} - \gamma\right) - (\phi^r - \phi^l), \quad (51)$$

where γ is the ratio of the follower current, I_{ef}, to the tree current, I_{cs}.

Note that except for the $1/\beta$ factor, the first terms in ΔNM are the same as those for V_{r0}. For the same fan-out condition, the noise generated is two orders of magnitude lower in the V_{r1} case. For FO=20 (or FO^r=40), V_s=500 mV and β=100, the loss of noise margin due to the first term is only about 1.05 mV.

The second terms are of opposite sign in ΔNM^h and ΔNM^l. If γ is between 1 and 3, then let γ^r=4, $|\gamma - \gamma^r/2| \le 1$. In the worst case, the loss of noise margin from the second term is V_s/β. So for β=100, a loss of noise margin of 1% of the voltage swing results. For V_s=500 mV, it is about 5 mV.

The third terms involve the V_{be} drops of the emitter followers, Q_{ef} and $Q_{ef}{}^r$. ϕ^r is the V_{be} drop for $Q_{ef}{}^r$ with $I_e = I_{ef}{}^r + I_o{}^r$. ϕ^h and ϕ^l are the V_{be} drops of Q_{ef} where I_e equals $I_{ef}+I_{omax}$ and $I_{ef}+I_{omin}$, respectively. As in the case of emitter follower sizing for pull-down resistors discussed in Section 3.2.3.1, similar sizing can be applied to minimize V_{be} variation, which results in better noise margin.

In practice, the emitter followers for either the signals or the V_r's may not be resized simply because of the complication and the small benefits.

Let us assume that the emitter followers are sized according to I_{ef} and $I_{ef}{}^r$ only . We have the following:

$$\phi^h = \phi + v_T ln\frac{I_{ef} + I_{omax}}{I_{ef}} = \phi + \Delta\phi^h,$$

$$\phi^l = \phi + v_T ln\frac{I_{ef} + I_{omin}}{I_{ef}} = \phi + \Delta\phi^l,$$

and

$$\phi^r = \phi + v_T ln\frac{I_{ef}{}^r + I_o{}^r}{I_{ef}{}^r} = \phi + \Delta\phi^r$$

where ϕ corresponds to the V_{be} drop at design current density. From Equation (51), the worst case loss of high noise margin occurs when $\Delta\phi^r$=0.

It follows that the losses of noise margin from the third term are

$$\Delta NM^{h(3rd)} = -v_T ln\frac{I_{ef} + I_{omax}}{I_{ef}} = v_T ln\left(1 + \frac{1}{\beta}\frac{(FO+1)}{\gamma}\right)$$

and

$$\Delta NM^{l(3rd)} = -v_T ln\frac{I_{ef}{}^r + I_{omax}{}^r}{I_{ef}{}^r} = v_T ln\left(1 + \frac{1FO^r}{\beta\ \gamma^r}\frac{I_{cs}}{I_{cs}{}^r}\right), \quad (52)$$

where as previously defined FO and FO^r are the number of fan-out of I_{cs}/β current loads, "1" in the numerator for $\Delta NM^{h(3rd)}$ accounts for current loadings for the level shifter, and γ and γ^r are the emitter follower to tree current ratios. Notice that variation of ϕ^l was ignored here since I_{omin} is usually very small. Assuming that I_{cs}'s and γ's are the same and $\gamma^r = 2\gamma$, the loss of high and low noise margin due to

the third terms are the same if the FO^r=2FO. Fan-out of signals causes high noise margin to degrade while fan-out of V_{r1} causes low noise margin to degrade. For 2FO=FO^r=40, β=100, and γ^r=2γ=4, the loss of noise margin at 85 ° C is about 2.86 mV. Since this noise is quite small, it is usually not worth resizing the emitter followers.

Here are the guidelines:

- *The contribution of the first term in Eq. (51) to the loss of high noise margin due to the generation of V_{r1} and the ECL signal levels is $V_s(FO+1)/\beta^2$. The loss of low noise margin is the same if the fan-out for the V_{r0} generator, $FO^r=2*FO*I_{cs}{}^r/I_{cs}$. Note that the loss of noise margin is a factor of β smaller as compared to the V_{r0} level.*
- *The contribution of the second term in Eq. (51) to the loss of noise margin is $\frac{V_s}{\beta} Max|\frac{\gamma^r}{2}-\gamma|$. Whenever there is a loss of the high noise margin from this contribution, there is a gain of the low noise margin of the same amount and vice versa. It is the worst case that counts.*
- *The contribution of the third term in Equation (51) to the loss of noise margin is described by Equation (52). The fan-out of the signal contributes to the loss of high noise margin while the fan-out of V_{r1} contributes to the loss of low noise margin.*

4. Noise Compensation Method: Resistor Trimming

In the last chapter we discussed various DC noise sources. For a given chip design, once the boundary conditions are fixed, circuit design guidelines and a noise budget can be established using the guidelines provided by the last chapter to ensure sufficient DC noise margins. For example, the metal systems of the technology (the number of metal layers and resistivities of different layers) and the power consumption of the given chip design set the worst case lower bound of the IR drop; the maximum allowable fan-in or wired-OR determine its related noise budget; and the maximum temperature gradient set the worst case V_{be} difference. In the case where the noise budget is tight, one has three options. One may increase the voltage swing or cut the IR drop budget by lowering the power consumption; however, this results in slower gates. Another alternative is to limit the fan-in or levels of series gating. This approach decreases functionality of the gates. In this chapter, a noise compensation method through resistor trimming [1] [3] will be discussed. In the ideal case, the ohmic drop related DC noise can be totally trimmed away, without resulting in slower gates.

4.1. The Basic Idea: The Ideal Case

Figure 4-1(a) depicts the basic idea for resistor trimming. The left part of Figure 4-1(a) shows a simple CML gate where a resistor is added to the top of the tree. Also shown is the V_{cs} generator supplying a reference for generating the current for the tree. The right part of Figure 4-1(a) shows a similar arrangement for a V_{r0} generator which can be anywhere else on the chip. The following discussions also apply to the ECL levels.

Because of the ohmic drops, the V_{cc}'s for the gate and for the V_r generator are ΔV_{cc} and ΔV^r_{cc} lower than the ideal Vcc supply for the chip. In order to compensate for the difference, trimming resistors R_{trim} and R^r_{trim} are included such that the virtual_V_{cc}'s, the new reference for the signal levels, are at the same level. Figure 4-1(b) depicts the ideal signal levels.

Conceptually, if ΔV_{cc}'s are exactly known and the voltage drop across R_{trim} can be tuned exactly, IR drops on the Vcc line can be completely compensated. As shown in the figure, there are Δ_{ee}'s in the V_{ee} lines such that the voltage drop across the current source resistor, R_{cs}, is not exactly V_s, the voltage swing, but $V_s \pm \Delta_{ee}$. Note that ΔV_{cc} is always positive while Δ_{ee} in the V_{ee} lines can be either positive or negative. If we further assume that ΔV_{ee}'s are exactly known, by the same token, R_{cs} can be trimmed to exactly compensate the voltage swing V_s.

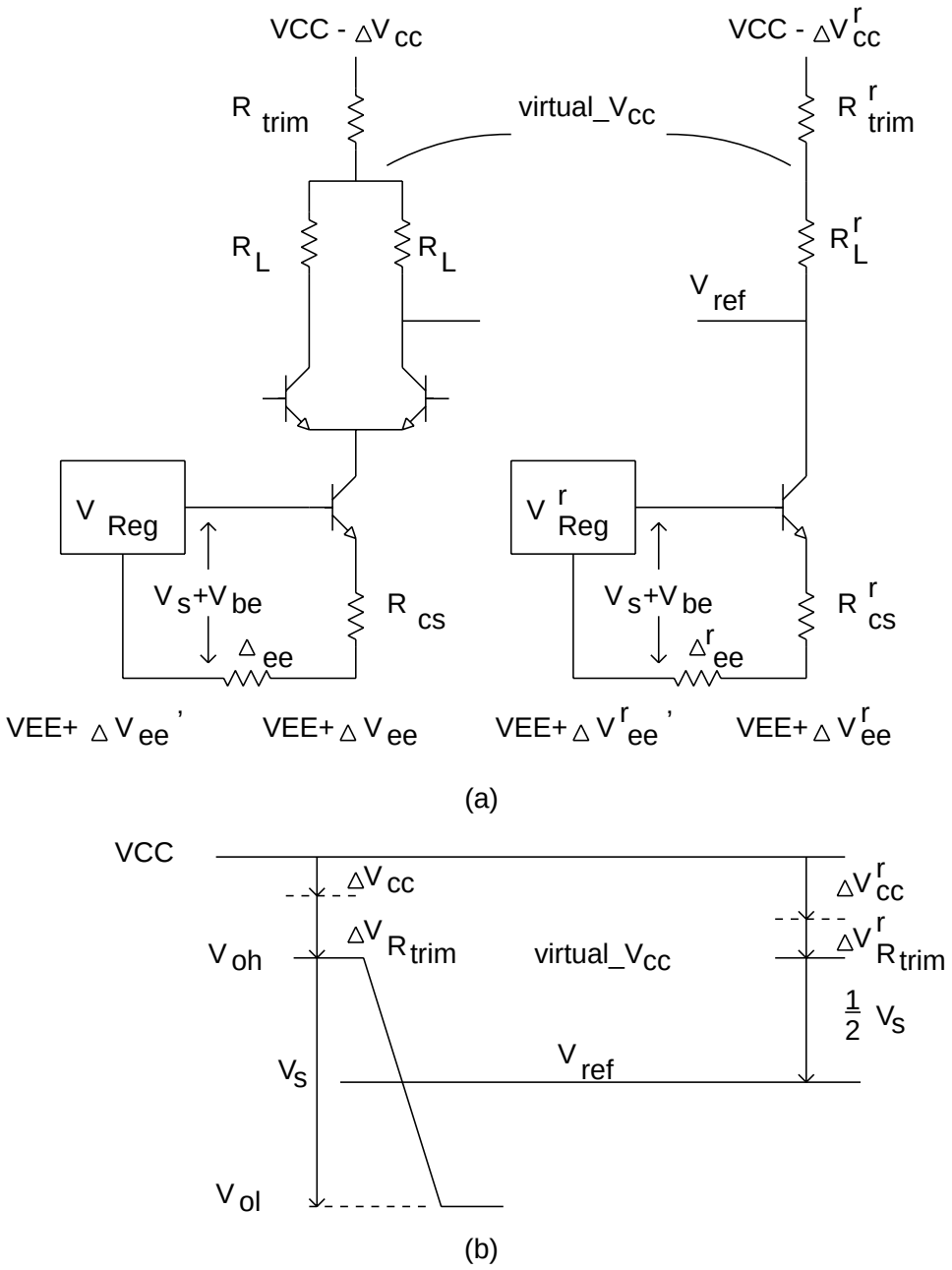

Figure 4-1: IR drop compensation

The equations describing the signal levels follow:

$$V_{oh} = V_{cc} - \Delta V_{cc} - \frac{R_{trim}}{R_{cs}}(V_s \pm \Delta_{ee}),$$
$$V_{ol} = V_{oh} - \frac{R_L}{R_{cs}}(V_s \pm \Delta_{ee}),$$

and

$$V_{ref} = V_{cc} - \Delta V^r_{cc} - \frac{R^r_{trim}}{R^r_{cs}}(V_s \pm \Delta^r_{ee}) - \frac{R^r_L}{R^r_{cs}}(V_s \pm \Delta^r_{ee}). \quad (53)$$

Here, $\pm$ is included so that Δ_{ee} is always positive. From these equations, we see that if ΔV_{cc}'s and ΔV_{ee}'s are exactly known as discussed above, the relative level of variation is only subject to the accuracy of the resistance ratios.

4.2. Non-tracking Resistors

If the resistors are all made of the same material, they track and the ratios are constant. But if two resistors of different material are ratioed, they do not necessarily track. In the worst case we have:

$$\frac{R_1(1 \pm \delta_1)}{R_2(1 \pm \delta_2)} = \frac{R_1}{R_2}[1 \pm (\delta_1 + \delta_2)], \quad (54)$$

in which case the ratio variations have to be figured in. Usually, R_L and R_{cs} are made of the same material, which is why trackings in ECL gates are perfect. However, R_{trim} and R_{cs} might be made of different material, since R_{trim} can be relatively small depending on the amount of compensation required at a given gate. The maximum variation of each of the three levels is the same. The worst case loss of noise margin happens when the maximum variation occurs on signal levels and the minimum variation occurs on the reference level, and vice versa. The loss of noise margin is expressed as

$$\Delta NM = -Max\{\frac{R_{trim}}{R_{cs}}(V_s \pm \Delta_{ee})(\delta_{trim} + \delta_{cs})\}. \quad (55)$$

For example, assuming $\max\{R_{trim}/R_{cs}\}=1/3$, $\delta_{trim}+\delta_{cs}=1/5$, V_s=500 mV and $\max\{\Delta_{ee}\}$=25 mV, ΔNM is approximately -35 mV. If only tracking resistors are allowed, this noise is insignificant.

4.3. Trimming the Intrinsic Circuit Noise

There are two types of intrinsic circuit noises: the current sharing type and the incomplete current switching type. Both can be removed by trimming the resistance ratios R_{trim}/R_{cs} and R_L/R_{cs}.

DC noise as has been discussed is presented as a degradation in the high output level, V_{oh}, the low output level, V_{ol}, or both. For example, when an incomplete current switching occurs in a tree, only a degradation of V_{ol} results. When taking the non-inverting output of a gate with multiple fan-in, if the resizing of the reference side transistor is not performed, again, only a degradation of V_{ol} results. The degradation of V_{ol} can be corrected by enlarging the ratio of R_L/R_{cs}. When taking the inverting output of a gate with multiple fan-in, regardless of the resizing, a degradation of V_{oh} results.

The method of compensation for the degradation of the high output level is a two step process. Since the reference rail is now the virtual V_{cc} which is controlled by the ratio of R_{trim}/R_{cs}, one can raise the local virtual V_{cc} by modifying the ratio of R_{trim}/R_{cs} to compensate for the high level degradation. Now that the

reference level is lifted by $v_T\ln(N)$, the output low is degraded by the same amount. The second step in the process is to increase the ratio of R_L/R_{cs} such that the output low level returns to its original value.

There is a practical issue with the resistance quantization. One can only expect to modify the resistance by some finite amount. For example, in a 0.1μm grid design where the minimum width of a 150 Ω/square resistor is 3.0μm, the minimum increment of resistance is 5 Ω. Assuming the minimum load resistance is 500 Ω, the minimum change in the resistance ratio is about 1%. With these numbers, it will be assumed that resistor trimming can only be effective down to the last 1% of the original noise.

4.4. ΔV_{cc} and ΔV_{ee} Estimation

Because V_{cc} is the reference for signals, its absolute level is of concern, while for V_{ee}, it is the relative level from the current source to the regulator that counts. As in most designs, placement of internal voltage regulators are such that the maximum relative V_{ee} difference is minimized.

By extracting the resistances and calculating voltage drops in a general way for a large custom design, experience has shown [2] that prediction of the voltage of a given node with respect to a fixed reference is correct within a tolerance of ± ~20%. To include this variation, the top rail reference V_{cc}=VCC-ΔV_{cc} can be considered as a Gaussian distribution whose 3σ variance equals $\Delta V_{cc}\delta_{cc}$, where Vcc is the supply to the chip and is considered a constant. Similarly, V_{ee}=VEE+ΔV_{ee} follows a Gaussian distribution whose 3σ variance equals $\Delta V_{ee}\delta_{ee}$. This applies to both V_{ee1} and V_{ee2}.

For two random variables x and y, the standard deviation of z=x ± y is expressed as

$$\sigma_z = \sqrt{\sigma_x^2 + \sigma_y^2 \pm 2\sigma_{xy}} \tag{56}$$

where σ_{xy} is the covariance, which can be either positive or negative depending on how x and y are correlated.

Assuming x is independent of y,

$$\sigma_{x\pm y}=\sqrt{2}\sigma_x \tag{57}$$

for $\sigma_x=\sigma_y$.

Assuming x and y are 100% correlated, there can be two cases: a) if they are in phase, $\sigma_{x+y}=2\sigma_x$ while $\sigma_{x-y}=0$; b) if they are 180 degrees out of phase, $\sigma_{x+y}=0$ while $\sigma_{x-y}=2\sigma_x$.

Note that if the worst case estimate is based on bounds, the variation of x ± y would have been $3\sigma_x+3\sigma_y=2*3\sigma_x$, which is equivalent to say that 100% in-phase correlation is assumed for x+y while 100% out-of-phase correlation is assumed for x-y. In other words, bounds-based analysis is a special case of the more general random process analysis. The bounds-based estimation is often overly pessimistic.

In reality, any two variables in a design are correlated in some way. Design guidelines should be set in such a way that favorable correlations prevail. In the following discussion, variables are always considered independent.

For Δ_{ee}'s as shown in Figure 4-1, the difference between two ΔV_{ee}'s is expressed as

$$\Delta_{ee} = (\Delta V_{ee} - \Delta V_{ee}') \pm \sqrt{(\Delta V_{ee}\delta_{ee})^2 + (\Delta V_{ee}'\delta_{ee})^2},$$

where $\Delta V_{ee}\delta_{ee}$ is the 3σ variance. For ΔV_{ee}=150 mV, $\Delta V_{ee}'$= 140 mV and δ_{ee}=0.2, the resulting Δ_{ee} is 10 ± 41 mV. As a comparison, Δ_{ee}= 10 ± 58 mV if bounds-based analysis is used. This is a classic problem of taking the difference of two large numbers where the error can be much larger than the difference. In fact, the worst case occurs when both ΔV_{ee} and $\Delta V_{ee}'$ assume the maximum values.

As has been discussed in Section 3.4.1, one of the design disciplines is to minimize the electrical distance between the master and the slave reference generators. As a design constraint, Δ_{ee}'s are assumed to have a mean value of Δ_{ee}^{m} bounded by $3\sigma_{\Delta_{ee}}=\max\{\Delta_{ee}\}$, which is symmetric around the mean. In most cases, the mean of Δ_{ee} will be zero.

4.5. General Derivation

In this section, Equation (53) will be revisited and modified using the concept of means and variances as discussed in the last section.

For a given gate, V_{oh}, V_{ol} and V_{ref} are functions of random variables ΔV_{cc} and Δ_{ee}. Here the random variables ΔV_{cc} and Δ_{ee} are independent and have means ΔV_{cc}^{m} and zero, and 3σ variances $\Delta V_{cc}^{m}*\delta_{cc}$ and Δ_{ee}^{max}, respectively. Note that the variance of ΔV_{cc} is a fixed percentage of its mean while Δ_{ee} has a fixed distribution bounded by the design constraints.

The modified set of Equations (53) are expressed as

$$V_{oh} = V_{cc} - \Delta V_{cc} - \frac{R_{trim}}{R_{cs}} V_s$$

with

$$3\sigma_{oh} = \sqrt{(\Delta V_{cc}\delta_{cc})^2 + (\frac{R_{trim}}{R_{cs}}\Delta_{ee}^{max})^2}, \tag{58}$$

$$V_{ol} = V_{oh} - \frac{R_L}{R_{cs}} V_s$$

with

$$3\sigma_{ol} = \sqrt{(3\sigma_{oh})^2 + (\frac{R_L}{R_{cs}}\Delta_{ee}^{max})^2}, \tag{59}$$

and

$$V_{ref} = V_{oh} - \frac{R^r_L}{R^r_{cs}} V_s$$

with

$$3\sigma_{ref} = \sqrt{(3\sigma_{oh})^2 + (\frac{R^r_L}{R^r_{cs}}\Delta_{ee}^{max})^2}. \tag{60}$$

Note that the variation of the ratio of R_{trim}/R_{cs} is not considered, implying tracking resistors are in place. The level variations are depicted in Figure 4-2.

From Figure 4-2, the loss of noise margin considered as random variables is expressed as

$$\Delta NM^h = V_{oh} - V_{ref} - 1/2\, V_s$$

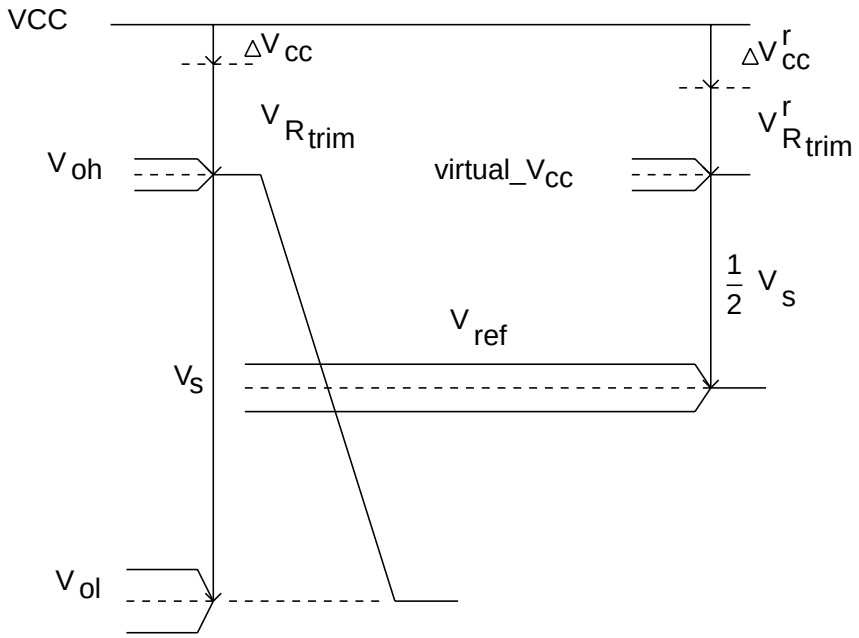

Figure 4-2: Signal levels after compensation

and

$$\Delta NM^{l} = V_{ref} - V_{ol} - 1/2\, V_{s},$$

where R^{r}_{L}/R^{r}_{cs} and R_L/R_{cs} are usually 1/2 and 1. It follows that the mean of ΔNM equals zero if the voltage drops on the V_{cc} and V_{ee} lines can be calculated exactly. The variance of ΔNM can be expressed as

$$3\sigma_{\Delta NM^{h}} = \sqrt{(3\sigma_{oh})^2 + (3\sigma_{ref})^2} = \sqrt{2\,(3\sigma_{oh})^2 + (\frac{R^{r}_{L}}{R^{r}_{cs}}\Delta_{ee}{}^{max})^2} = \sqrt{2\,(3\sigma_{oh})^2 + (0.5\,\Delta_{ee}{}^{max})^2}$$

and

$$3\sigma_{\Delta NM^{l}} = \sqrt{(3\sigma_{ol})^2 + (3\sigma_{ref})^2} = \sqrt{2\,(3\sigma_{oh})^2 + (0.5\,\Delta_{ee}{}^{max})^2 + (\frac{R_L}{R_{cs}}\Delta_{ee}{}^{max})^2} = \sqrt{2\,(3\sigma_{oh})^2 + (1.5\,\Delta_{ee}{}^{max})^2}.$$

Note that the loss of low noise margin is more than that of the high by the last factor. In order to obtain the maximum $3\sigma_{\Delta NM}$, the problem reduces to determining the maximum of σ_{oh}.

From the second equation of Equations (58), we see that σ_{oh} consists of two terms in the square root: the first term involves ΔV_{cc}, a random variable with a distribution; the second term involves R_{trim}/R_{cs}, a "constant", and Δ_{ee}, a random variable with a distribution. In fact, the resistance ratio R_{trim}/R_{cs} can be expressed as a function of the means as

$$\frac{R_{trim}}{R_{cs}} = \frac{V_{oh}{}^{m} - \Delta V_{cc}{}^{m}}{V_{oh}{}^{m}}$$

where $V_{oh}{}^{m}$ is the mean of V_{oh}, the unperturbed virtual V_{cc}. Figure 4-2 clearly shows that the two terms are complementary. The worst case V_{oh} variation follows

$$max\{\sigma_{oh}\} = Max\{max(1st\_term)\, and\, min(2nd\_term), min(1st\_term)\, and\, max(2nd\_term)\}.$$

Let us substitute in some numbers. Assuming that $\max(R_{trim}/R_{cs})=1/3$ when $\min(\Delta V_{cc})=0$, $\min(R_{trim}/R_{cs})=0$ when $\max(\Delta V_{cc})=150$ mV, $\Delta_{ee}^{max}=25$ mV, $V_s=500$ mV, and $\delta_{cc}=0.2$,

$$max\{\sigma_{oh}\} = max\{30mV, 8.33mV\} = 30mV.$$

It follows that $3\sigma_{\Delta NM}{}^{h} = \sqrt{2*(30)^2 + (0.5*25)^2} = 44.2$ mV and $3\sigma_{\Delta NM}{}^{l} = \sqrt{2*(30)^2 + (1.5*25)^2} = 56.6$ mV.

4.6. Emitter Follower with Pull-Down Resistors Revisited

The noise problem associated with the pull-down resistor of an emitter follower originates from V_{be} variations resulting from J_{ef} variations. As discussed before, the sources of J_{ef} variation in this case are output level variations and V_{ee2} variation. In this section, Equation (42) in Section 3.3.1.2 will be re-derived by using the concept introduced in Section 4.4. Let us copy Equation (42) here for reference.

$$\Delta = v_T ln(\sqrt{\frac{(v_{oh}-\Delta v_{oh})-(v_{ee2}+\Delta v_{ee2})}{(v_{ol}-\Delta v_{ol})-(v_{ee2}+\Delta v_{ee2})}}).$$

As discussed in the last section, V_{oh} and V_{ee2} are now considered as random variables. To simplify the mathematics, the numerator and the denominator inside the square root are treated separately and a bounds-based analysis will be applied afterwards. For the numerator *N* and denominator *D*, we get

$$N = V_{oh} - V_{ee2}$$

with

$$\sigma_N = \sqrt{(\sigma_{oh})^2 + (\sigma_{ee2})^2}$$

and

$$D = V_{ol} - V_{ee2}$$

with

$$\sigma_D = \sqrt{(\sigma_{ol})^2 + (\sigma_{ee2})^2}.$$

The revised equation for the V_{be} variation becomes

$$\Delta = V_T ln(\sqrt{\frac{V_{oh}{}^{m} - V_{ee2}{}^{m} - 3\sigma_N}{(V_{ol}{}^{m} - V_{ee2}{}^{m} - 3\sigma_D}}). \quad (61)$$

.

Assuming $V_{be}{}^{m}=0.85$ V, $V_{oh}{}^{m}=-1.0$ V, $V_{ee2}{}^{m}=-1.9$ V, $V_s=0.6$ V, $V_{ol}{}^{m}=-1.6$ V, $3\sigma_{oh}=30$ mV, $3\sigma_{ee2}=30$ mV and $\Delta_{ee}{}^{max}=25$ mV, we get $3\sigma_{ol}=50$ mV by Equation (59), $3\sigma_N=42.2$ mV and $3\sigma_D=58.3$ mV. The V_{be} variation, Δ, is 19 mV.

There is also the noise associated with variations of the resistance as discussed in Section 3.3.2. The J_{ef} variation resulting from the resistance variation shifts the signal levels. Assuming 20% lot to lot tolerance of the resistance, ΔV_{be} from Equation (49) is about 5.5 mV.

To summarize the above discussion, the worst case noise generated by the pull-down resistor of an emitter follower is around 24.5 mV with the above operating assumptions.

5. Noise Budget

In this chapter, a noise budget based on discussions in previous chapters will be presented.

5.1. General Discussion

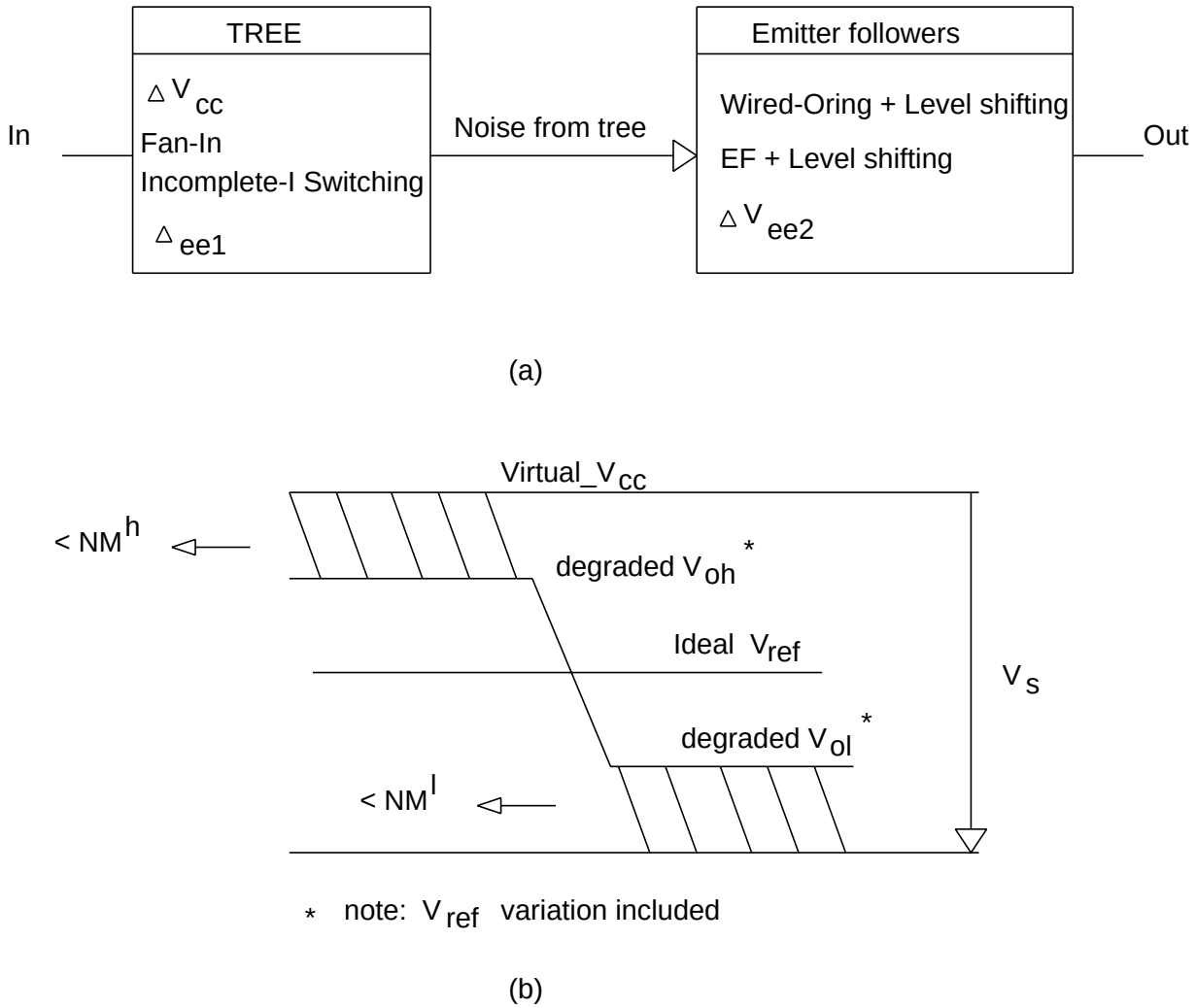

Figure 5-1: A global picture of noise margin

To review the basic problem of noise margin, Figure 5-1 shows a global picture depicting the essence of noise margin preservation. As depicted in Figure 5-1(a), a gate is composed of a tree section and an emitter follower section. The major noise sources pertaining to the tree section and the follower section as discussed in Chapter 3 are listed in the block diagram.

It is straightforward to figure out the loss of noise margin of a gate as defined by the block diagram. The total loss of noise margin is simply a sum of the contributions from all the participating sources. Note that wired-OR is always considered as part of the emitter followers. The noise budget is then defined as

the sum of the contributions of all possible participating sources of the most complex gate. As always, this will be the worst case noise budget.

5.2. A Sample Noise Budget

Table 5-1 shows a sample noise budget. The assumptions in creating this noise budget are as follows. The nominal operating junction temperature is 85 ° C at which $v_T \sim 30$ mV. The voltage swing is taken to be 600 mV which only affects the noise contribution from series gating. The worst case temperature gradient on chip is less than 20 ° C. The worst case voltage drops on the power distribution network for V_{cc}, V_{ee1} and V_{ee2} are 150 mV each. A master reference generator is placed within an electrical distance of plus or minus 25 mV from all the slave reference generators and the current sources connected to this master reference generator. In other words, 25 mV is the maximum Δ_{ee} as discussed in Chapter 4.

The first column of Table 5-1 lists the noise sources, all of which have been discussed in Chapter 3. The reader should refer to individual sections for details. The second column lists the noise in millivolts as generated by each noise source. The third column tabulates the noise after resizing of relevant transistors. The contributions of noise of the ones that are check-marked in the fourth column add up to the number at the bottom. This is the total noise contribution after transistor resizing. The fifth column tabulates the result of noises after resistor trimming of both the top resistor, R_{trim}, and the current source resistor R_{cs}. The last column summarizes the noise contribution after both transistor resizing and resistor trimming.

Transistor resizing is mainly for the cases of fan-in and/or wired-OR. The reason for the extra one millivolt in these cases stems from the assumption that only integer multiples of minimum size transistors are used. For example, the reference transistor is supposed to size up by a factor $\sqrt{8}$=2.8 but a factor of 3 is used instead. Note that within this category, an IR drop of 15 mV is also listed. This is to remind the designers that when either the fan-in or wired-OR transistors are pulled far apart, there is the emitter current flowing across the long common-emitter line creating an ohmic drop that translates directly into noise. This was discussed in Section 3.3.1.3. Note that this item is not check-marked in either columns 4 or 6. If this occurs, the designer has to make sure that he or she can steal the noise budget from other items for it.

In the second category, incomplete current switching as discussed in Section 3.2.2 is listed. The short hand notation 2s-3s stands for gates where both the second level and third level are driven single-endedly and there is no fourth level. The short hand notation 2s-3s-4d stands for gates where both the second level and third level are driven single-endedly and the fourth level is driven differentially. The fourth level signal is usually the differential clock at a half voltage swing. Here the second level corresponds to the first ECL level, while the first level corresponds to the CML level. With a 600 mV voltage swing, the normalized swing, s, is 20. With Equations (29) and (35) derived in Section 3.2.2.1 and 3.2.2.2 and the guidelines provided at the end of that section, the noise lost to series gating is calculated and listed in the table. As mentioned earlier, this is the one noise that is related to the voltage swing. If a different voltage swing is desired, this noise needs to be recalculated. It is evident from the equations that the smaller the voltage swing the larger the noise contributed from series gating.

There is a noise of 6 mV listed for α degradation which requires some explanation. As was discussed in Section 3.2.2.3, a β of 100 causes a degradation of 1% voltage swing every time a transistor is encountered going up a tree. For V_s=600 mV, this corresponds to a 6 mV degradation. Treating it as an incomplete switching noise, one can always trim R_{cs} to eliminate this noise. In a typical gate with

Noise Sources *		+ trans. sizing		+ resistor trimming	
Fan-In n = 8	62.0	33.0	√	1.0	√
Wired-Or n = 8	62.0	33.0	√	1.0	√
IR drop on emitter connect (e.g. 1mm min-m1 of 1mA)	15.0	15.0		15.0	
Incomplete I-switching					
Series gating 2s-3s	31.6	31.6		1.0	
Series gating 2s-3s-4d	33.3	33.3	√	1.0	√
Alpha degradation	6.0	6.0	√	1.0	√
J_{ef} variation					
real CS	7.0	7.0	√	7.0	√
R_{ef} as CS	24.5	24.5	√	24.5	√
Reference voltages					
bandgap gen.	5.0	5.0	√	5.0	√
Vr0	30.0	30.0		30.0	
Vr1-3	7.5	7.5	√	7.5	√
Vr's distribution	4.0	4.0	√	4.0	√
Process variation of Vbe	6.0	6.0	√	6.0	√
IR drops					
on Vcc & Vee	175.0 (150+25)	175.0	√	57.0	√
on signal line (10mm)	< 2.0	< 2.0	√	< 2.0	√
Δ_T = 20 C	30.0	30.0	√	30.0	√
			366.3		147.0

* In mV, T=85C , v_T =30 mV and V_s =600 mV

Table 5-1: Noise Budget

two-level series gating, one can simply tune up the V_{reg} generator to compensate for it without trimming the resistor. As it can only be compensated for a "typical" gate, the output of a gate with three-level series gating will still suffer one α degradation. For this reason one level of α degradation noise is included.

The third category relates to the current density variation of the emitter followers. The case for the pull-down resistor was discussed in Sections 3.2.3 and 3.3.1.2, and summarized in Section 4.6. The number listed in the table is a direct result of those analyses.

The case for a real current source has two parts. The first part has to do with resistance variation and was discussed in Section 3.3.2. The associated noise can be calculated from Equation (48) and will be referred to as contribution *A* with $3\sigma_A = v_T ln(1+\delta_r)$. The second part has to do with the Δ_{ee} variation which results in variation of the voltage across the current source resistor. This will be referred to as contribution *B* with $3\sigma_B = v_T ln(1+\frac{V_S + \Delta_{ee}^{max}}{V_S})$. The total contribution to noise is then $3\sigma_{A+B} = \sqrt{(3\sigma_A)^2 + (3\sigma_B)^2}$.

For a lot to lot variation of δ_r=20%, Δ_{ee}^{max}=25 mV and V_s=600 mV, the total noise is calculated to be about 7 mV.

The fourth category has to do with the noise associated with the reference voltage generation and distribution. This was discussed in detail in Section 3.4. Five millivolts are listed for the distribution of V_{cs} or V_{reg}. The contribution from the IR drop on the bottom rail is included in the category of IR drops of V_{cc} and V_{ee}. The last row in this category is essentially a design restriction where only a maximum of 4 mV is allowed between where V_r is generated and where it is referenced.

The variation of V_{be} is a technology parameter which is a measure of the consistency of the process.

The issues of IR drops were discussed extensively in Section 3.3.1. The trimming methodology was covered in Chapter 4 where detailed derivations can be found. The effectiveness of resistor trimming is obvious from these numbers. Voltage drops on signal lines are usually negligible as the loading currents, essentially base currents, are small. Here 2 mV is budgeted for this noise. It roughly corresponds to the voltage drop of a 10 mm minimum width metal line carrying a current of 1mA/100.

The last item is the on-chip temperature gradient. Here a 20 ° C maximum difference is assumed for a 1.5 mV/C V_{be} variation.

5.3. Summary

In the last section, a sample noise budget was presented with assumed boundary conditions. The noise budget varies from design to design as boundary conditions change. In order to guarantee functional circuits, a noise budget and associated design guidelines should first be established.

This document provides detailed analyses on DC noise issues associated with the ECL circuit family. It is the hope of the authors that by understanding the nature of the noise problem, a sound design methodology can be established.

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