SGEC specification V3.0
Part Number DC-541
For Internal Use Only

This document contains the specification for the Second Generation Ethernet Chip pass1 part. It has been reviewed by the development team and is now submitted for internal customers review.

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Change history:

Revision	Date	Description
3.0	June 6, 1988	Pass1 SGEC version, including: • SIA dropped. • CP-BUS parity support added. • Incorporated various inputs received at reviews.
2.0	July 7, 1987	Major update including: • DEQNA mode dropped. • SGEC host port interface redefined. • FIFOs size increased to 120 bytes. • Serial parameters programmability dropped. • Direct μVAX bus support dropped. • Incorporated various inputs received at reviews.
1.0	Oct 17, 1986	Major update including: • DEQNA mode added. • SGEC "native" mode defined. • Removed references to LANCE. • Incorporated various inputs received at first review.
0.x	Jan 30, 1986	Initial version

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Preface

Executive summary

The SGEC is one of a two (three) chips Ethernet controller for low-end systems connecting to 10BASE5 (10BASE2) cables. Another required chip is an SIA (and a 10BASE2 transceiver).

The SGEC device is a second generation VLSI Ethernet controller. It is part of the 32 bit CVAX VLSI device family, and directly compatible to the pinout and bus timing of the CVAX.

The SGEC is superior to comparable devices in the market due to a higher host bus transfer rate, better host bus utilization, provides higher integration, as well as other features.

The SGEC connects directly to the 32 bit *CP-BUS* (CVAX Pin Bus), communicating with the host through *CSR's - Command and Status Registers* and a "host communication area" set up in main memory. For data transfer it uses an on-chip DMA controller supporting both VAX virtual and physical memory addresses.

The SGEC features a dual, internal FIFO for decoupled and separate reception and transmission buffering facilitating efficient CP-BUS utilization. The FIFO holds the data until, at least, the collision window is passed.

The SGEC conforms to the DIGITAL CSMA/CD (ETHERNET) LOCAL AREA NETWORK SPECIFICATION (DEC STD 134B).

The device is fabricated in Digital's CMOS-II dual-metal process and is packaged in an 84 pin cerquad package.

Feature list

- Direct interface to the 32-bit CP-BUS.
- Host port interface supporting list structured descriptors with ownership flags, VAX virtual and physical memory addressing, and errors and statuses reporting.
- Up to 14 perfectly filtered addresses or a 512 bits imperfect hash filter.
- Two on-chip 120 byte FIFOs for reception and transmission.
- DIGITAL CSMA/CD (ETHERNET) LOCAL AREA NETWORK SPECIFICATION (DEC STD 134B) compliant.
- 25 MHz system clock rate and independent serial clock variable from 1 to 10 MHz.
- CP-BUS DMA octaword transfers at rates up to 20 MByte/sec.
- CP-BUS parity generation and checking.
- Meeting 9.6μS *IPG - Inter Packet Gap* - in most cases.
- Full frame encapsulation including preamble generation and removal, automatic 32-Bit FCS (CRC) generation and checking, and IEEE 802.3 pad bytes addition and stripping.
- Programmable watchdog timers to prevent babbling transmission and reception.
- Loopback capability.
- Single 5V power supply.
- 84 pin cerquad package.

1 Ethernet and IEEE 802.3 overview

1.1 Local Area Networks

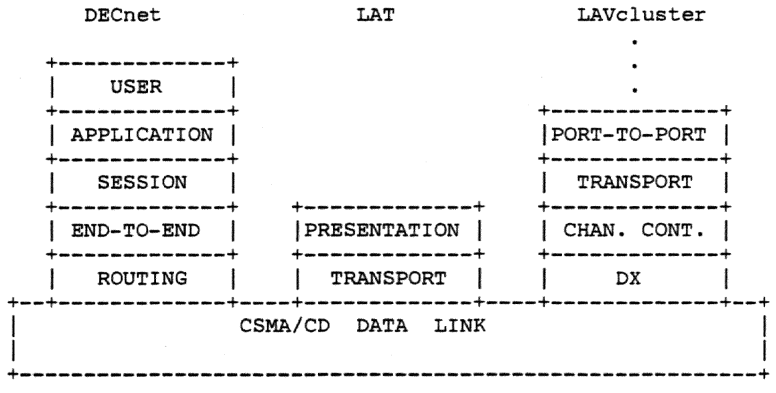
Local Area Networks are communication networks extending from several hundred to several thousand feet within a building or other facility. LANs are a means of connecting various types of equipment for the purposes of sharing resources and communicating in a distributed processing environment. Although LANs using a range of speeds (from 2400 bits/sec up to 10 Mbits/sec) exist today, the trend is clearly towards networks between 1 and 10 million bits per second. Both *Ethernet* and the *IEEE 802.3* specifications use 10 Mbits/sec speeds.

1.2 Ethernet in Digital

Ethernet has been Digital's LAN flagship in recent years. In 1982 Ethernet was introduced into the *DNA* - Digital Network Architecture, at the data link level, thus providing *DECnet* support over the Ethernet media for almost all the CPU offerings ranging from VAXes to Personal Computers. Recently, with the approval of the IEEE 802 family of LAN standards, Digital has added IEEE 802.3 and parts of IEEE 802.2 support to its architecture. Digital has publicly adopted the IEEE 802.3 standard and committed to both Ethernet and IEEE 802.3 support, collectively known as *CSMA/CD LANs*.

In addition to DECnet, Digital introduced several other products making use of the Ethernet at the data link layer, but deviating from DNA at higher layers and employing Digital developed proprietary protocols and Transport mechanisms. All these protocols, as well as DECnet, coexist and concurrently operate on the same wire, as illustrated by the figure.

Figure 1–1 Several of the Digital developed transport mechanisms

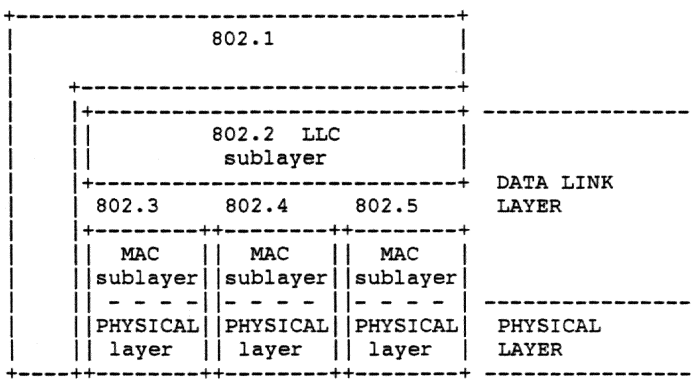


Distributed Systems in general, and Ethernet in particular, constitute the cornerstone of Digital's long range strategy. Products like DECnet, Terminal Servers and other products such as various Local Area Servers and Ethernet based Local Area VAXclusters are expected to significantly enhance Digital's offering in the Distributed Systems market by providing fully distributed solutions to customers' business problems.

1.3 The IEEE 802 family of LAN standards

This family of standards is the effort undertaken by the IEEE to standardize existing popular LAN implementations, such as the Ethernet and the Token Passing based LANs, improving, enhancing and cleaning up various issues. This family of standards constitutes the low level building blocks for other standards organizations such as the ISO, which has adopted the IEEE 802 standards as the LAN Data Link level standards of its OSI - Open System Interconnection model. Currently the IEEE 802 family consists of the following:

Figure 1–2 802 family of standards



1 802.1 - Describes the relationships among the IEEE 802 family of standards and their relationship to the ISO/OSI model.

2 802.2 - Describes the functions, features and protocols of the LLC (Logical Link Control) sublayer of the Data Link layer. The LLC sublayer together with the MAC (Media Access Control) sublayer form the complete Data Link layer. While the LLC sublayer is common to all the access methods, the MAC sublayer is unique to and defined within the access method standard.

3 802.3 - The standard for LANs employing CSMA/CD (Carrier Sense Multiple Access with Collision Detection). The CSMA/CD media access method is the means by which two or more stations share a common bus transmission medium. This is the standard that emerged from the Ethernet.

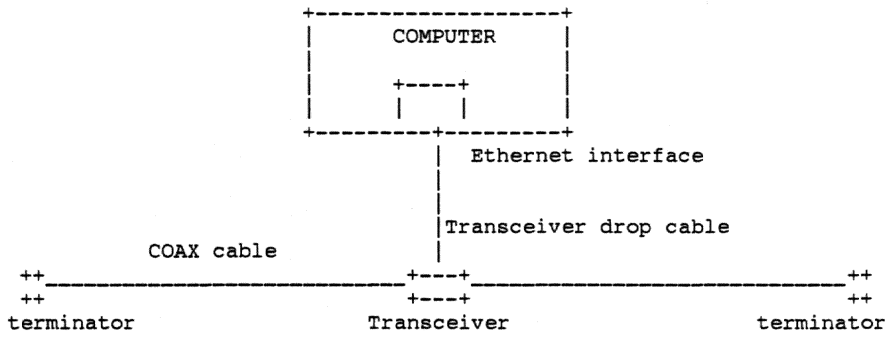
4 802.4 - Describes the elements of the Token Passing Bus access method and its associated physical signaling and media technologies.

5 802.5 - Describes the format and protocols used by the Token Passing Ring MAC sublayer, the physical layer, and the means of attachment to the token passing ring physical medium.

1.4 Ethernet and IEEE 802.3 elements

The Ethernet, which has gained wide acceptance by both large and small corporations, is a high speed (10 Mbps) LAN. The figure shows the main components of the Ethernet network:

Figure 1–3 Ethernet Network Elements



The cable is a low noise, shielded 50 ohm coaxial cable. Over this cable, information is transmitted at the rate of 10 million bits per second. Segments of the cable can be up to 500 meters (546.8 yards) in length and can be extended into longer network lengths by using repeaters. A repeater provides the signal regeneration that is required to strengthen the data transmission signal along the extended length of the cable.

The transceiver, a small electronic device, transmits and receives signals on the coaxial cable, and generally protects against failure and detects electrical interference (referred to as collisions) on the cable. It is connected to the cable using a simple tap and to the interface by means of a transceiver cable which consists of four individual twisted pairs and may be up to 50 meters (54.68 yards) in length.

The terminator is a passive device which fits on both ends of each cable segment, providing proper electrical termination.

Finally, the interface provides the connection to the user or the server station and performs such functions as:

- Data encapsulation/decapsulation (frame assembly/disassembly)
  - handling of source and destination addressing
  - detection of physical channel transmission errors
  - frame delimiting
- Network link management
  - collision avoidance
  - collision handling
- Encoding and decoding of the signal to and from the transceiver

The key element of the Ethernet and IEEE 802.3 specifications is the media access method (rules for using the shared coaxial cable). Commonly referred to as Carrier Sense Multiple Access with Collision Detection (CSMA/CD), it is a simple and efficient means of determining how a station transmits information over a medium that is shared with other stations. In order to transmit information, a station takes the following steps:

1 CARRIER SENSE - Any station wishing to transmit "listens" first. If the cable is busy (i.e. some other station is transmitting) the station waits until the line is clear before transmitting.

2 MULTIPLE ACCESS - Any station wishing to transmit can do so. No central controller is needed to decide who is able to transmit and in what order. This is commonly referred to as distributed control, where all stations on the network are peers with equal access.

3 COLLISION DETECTION - When the cable is free (no other station is transmitting), a station can start transmitting. The transmitting station (or stations) always listens while transmitting in order to detect any other station transmitting on top of its own signal, causing a "collision". In the event of such a collision, where two or more stations are transmitting at the same time, the transmitting stations will continue transmitting for a fixed time to insure that all transmitting stations detect the collision. This is known as the "jam". After the jam, the stations stop transmitting and wait a random period of time before retrying. The range of random wait times increases (by the power of 2) with the number of successive collisions so that collisions can be resolved even if a large number of stations are colliding (this is referred to as the exponential backoff algorithm).

The three most significant characteristics of CSMA/CD based networks are the passive nature of the network, its reliability and expandability. The CSMA/CD media access method enables the network to operate without central control or switching logic. If a station on the network malfunctions, it does not affect the ability of other stations to communicate with each other, nor affect the operation of the network.

A direct result of such a passive network is increased reliability. Total network failure cannot be caused by a single station malfunctioning. A system-wide failure can be caused by a cable malfunction such as an open or short circuit or a continuously transmitting station, and system hardware has built-in checks to detect and correct such situations.

The passive, distributed nature of a CSMA/CD based network also permits easy expansion. Stations can be added to (or deleted from) an existing network without reinitialization or reconfiguration of all other stations. Such a capability supports future growth requirements through simple expansion of the network.

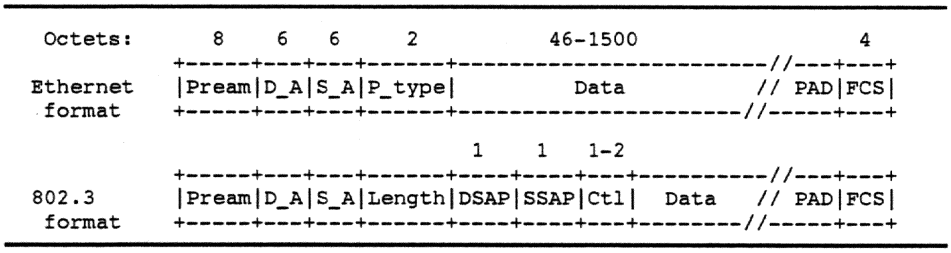
1.5 Ethernet and IEEE 802 differences and coexistence

There are many minor differences in the hardware specifications. Some of the 802.3 differences have special exceptions that allow for Ethernet, others are incompatible. Fortunately, the signal put on the Ethernet cable remains the same.

In terms of software, IEEE 802.3 and Ethernet are not compatible. 802.3 has a length field where Ethernet has a type field. The Ethernet type field is a 16 bit field used to differentiate among different Ethernet users such as DECnet, LAT (the terminal servers protocol) etc. Under the IEEE 802 standards, differentiation among multiple users is part of the 802.2 LLC specification. To that end, an 8 bit field is defined - DSAP (Destination Service Access Point).

The DNA CSMA/CD Data Link Functional Specification (Version 1.0.1, 12 February 1986) allows for the coexistence of Ethernet and IEEE 802.3 frames on the same wire and in the same node. The prerequisite is that Ethernet protocol type field values be **ALWAYS** greater than the maximum data length (1500).

Figure 1–4 DNA CSMA/CD frame formats



Field	Description
Pream	Preamble including the Start Frame Delimiter
D_A	Destination Data Link Address
S_A	Source Data Link Address
P_type	Protocol type field for Ethernet frames
Length	The data length field for IEEE 802.3 frames
DSAP	Destination LLC Service Access Point address for IEEE 802.3 frames
SSAP	Source LLC Service Access Point address for IEEE 802.3 frames
Ctl	LLC Control field for IEEE 802.3 frames
Data	User data
PAD	Padding octets
FCS	Frame Check Sequence

2 Assumptions and goals

2.1 SGEC Basic Assumptions

This paragraph will list the assumptions which led to the design of the SGEC as an internal product. Those assumptions also served as the baseline for the SGEC definition goals.

- Ethernet networks will continue to be used by DEC customers and by DEC engineering community in the future for at least one more decade.
- Current Ethernet VLSI devices do not provide an adequate integration level for Digital products.
- Present Ethernet devices have 60K - 80K transistors, but existing CMOS II technology allows for more than 200K transistors per device.
- Improved device performance in both the Serial Channel interface and the system interface would significantly benefit Digital products.
- VMS software compatibility and support is highly desirable within Digital.
- Ethernet VLSI devices are used in high volumes inside Digital, the estimated numbers are around 150K - 200K devices per year.

2.2 SGEC Project Goals

The following paragraph will list the SGEC design goals. Those goals were derived from the above list of assumptions. They were used to generate the specific list of functionality which was selected for the SGEC.

a. Design an Ethernet communication controller as part of the CVAX chip family. Based on:

- Ethernet networks will continue to be used by DEC customers and by DEC engineering community in the future for at least one more decade.
- Current Ethernet VLSI devices do not provide an adequate integration level for Digital products.
- Ethernet VLSI devices are used in high volumes inside Digital, the estimated numbers are around 150K - 200K devices per year.

b. Design a VLSI Ethernet LAN controller superior in its serial channel features to similar devices already available in the market, or planed in the near future, based on:

- Current Ethernet VLSI devices do not provide an adequate integration level for Digital products.
- Present Ethernet devices have 60K - 80K transistors, but existing CMOS II technology allows for more than 200K transistors per device.

- Improved device performance in both the serial channel interface and the system interface would significantly benefit Digital products.

c. Design a port architecture which will get VMS commitment. Based on:

- VMS software compatibility and support is highly desirable within Digital.

2.3 Basic Definition guidelines

This paragraph will list the definition Guidelines for the SGEC Design.

The set of the SGEC device features was selected out of the envelope of performance which can be designed into an Ethernet device. This set selection was derived from the above two paragraphs stating the SGEC device goals.

2.3.1 System Interface

This section will list the SGEC system interface definition guidelines:

- The SGEC will provide the system designer a two chip solution for 10BASE% Ethernet network connection.
- The device will fit into the CVAX system architecture including 32 bit data and address bus interface and CVAX pin bus timing.
- The SGEC bus transfer rate will match the CVAX pin bus rate and will be up to 20 Mbyte/sec.
- The SGEC will include two 120 byte FIFOs, which will allow a system bus latency of approximately 2 microseconds for data transfers.
- The SGEC will support VAX physical and virtual memory addressing.
- The SGEC will interface to the CPU via a "host communication area" in host memory and via CSR's.

2.3.2 Serial Controller Features

This section will list the SGEC serial channel interface definition guidelines:

- The SGEC will avoid shortcomings in the devices now on the market, such as exponential backoff implementations and coupled serial and system clocks.
- It will perfectly filter 14 addresses or for more than 14 addresses will contain a 512 bit hash mask and one physical address for imperfect addresses filtering.
- The SGEC will automatically discard incoming runt (colliding and too short) frames.
- The SGEC will automatically retransmite outgoing colliding frames.

- The SGEC will support a continuous packet rate of up to 14,000 frames per second.
- The following interframe gaps between *successive, minimum length back-to-back frames* will be allowed in host physical memory interface mode., i.e., will not cause frame loss:

Table 2–1 Minimum interframe gaps physical

Scenario	Minimum gap
Receive following receive	9.6 μSEC
Receive following transmit	4.8 μSEC
Receive following a collision	4.8 μSEC
Transmit following transmit	9.6 μSEC
Transmit following receive	9.6 μSEC
Transmit following a collision	9.6 μSEC

- The following interframe gaps between *successive, minimum length back-to-back frames* will be allowed in host virtual memory interface mode., i.e., will not cause frame loss:

Table 2–2 Minimum interframe gaps virtual

Scenario	Minimum gap
Receive following receive	19.2 μSEC
Receive following transmit	4.8 μSEC
Receive following a collision	4.8 μSEC
Transmit following transmit	19.2 μSEC
Transmit following receive	9.6 μSEC
Transmit following a collision	9.6 μSEC

- The Transmite following a collision numbers, are valid for a backoff_ time = 0, for cases when this time is non zero it will define the transmite following a collision timing.
- The above numbers hold for the following system parameters:

  Maximum DMA latency = 2 μSEC.

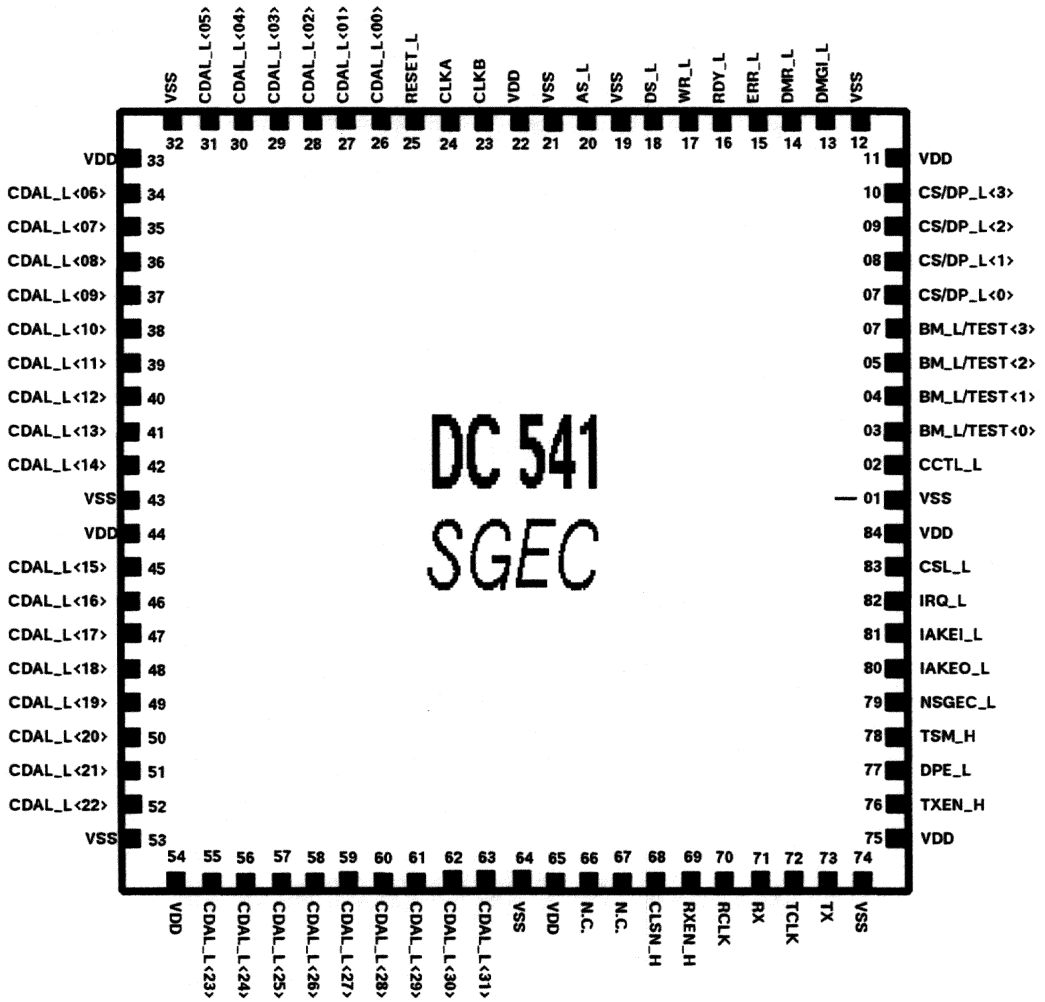
  Burst limit = 4 longwords.

  System clock cycle = 80 NanoSEC.

  Serial line clock cycle = 100 NanoSEC.

3 PINOUT

Figure 3–1 SGEC pinout



Note: The figure is the final pass 1 pinout. It is subject to change in future revisions.

3.1 Pinout tables

The chip will be packaged in an 84-pin fine lead (25 mil) surface mount package.

Table 3–1 SGEC pinout table

Pin	Usage	Width	Description
		CVAX interface pins	
CDAL	IO	32	CVAX Data and Address Lines
BM_L/TEST	IO	4	Byte Mask or Test
CS/DP_L	IO	4	Cycle Status/Parity/Sync/Async
AS_L	IO	1	Address strobe
DS_L	IO	1	Data Strobe
WR_L	IO	1	Write
RDY_L	IO	1	Ready (open drain)
DPE_L	IO	1	Data Parity Enable Signal (open drain)
CCTL_L	O	1	Cache Invalidate Signal (open drain)
ERR_L	I	1	Bus Error
NSGEC_L	O	1	Not SGEC Reference
CSL_L	I	1	Chip select
DMR_L	O	1	DMA Request (open drain)
DMGI_L	I	1	DMA Grant Input
IRQ_L	O	1	Interrupt Request (open drain)
IAKEI_L	I	1	Interrupt Acknowledge Enable Input
IAKEO_L	O	1	Interrupt Acknowledge Enable Output
CLKA,B	I	2	CVAX Clock inputs
Sub total		56	
		Serial interface pins	
RX	I	1	Receive data
RCLK	I	1	Receive clock
RXEN_H	I	1	Receive enable
CLSN_H	I	1	Collision Detect
TX	O	1	Transmit data
TCLK	I	1	Transmit clock
TXEN_H	O	1	Transmit enable
Sub total		7	

Table 3–1 (Cont.) SGEC pinout table

Pin	Usage	Width	Description
		Miscellaneous	
VDD	I	8	+5V Power
VSS	I	9	Ground
TSM_H	I	1	Test Mode
RESET_L	I	1	Reset
Sub total		19	

The following table summarizes the usage of the SGEC's pins.

Table 3–2 Pinout summary

Section	No. of pins	Comments
CP-BUS bus	56	Host bus connection
Serial bus	7	To/from SIA
Power and reset	19	
Not used	2	Reserved for future use
Total	84	

3.2 Pinout Signal Descriptions

For all the pins names, suffix _L means that the pin is asserted when low, and an _H means it is asserted when high. No suffix implies pin can be driven both low and high.

- **CDAL<31:0>** - CVAX Data And Address Lines - (I/O Pins)

  The CVAX Data and Address bus (CDAL) is a 32-bit time multiplexed bus used to carry all data and address information between the SGEC, host CPU and host memory. The strobe control signals AS_L and DS_L determine whether the bus is currently carrying address or data information.

- **BM_L/TEST<3:0>** - Byte Mask/Test pins. - (I/O Pins)

  These pins have dual functions. in normal operation mode they carry byte mask information; in test mode they are used as test pins. Mode selection is done by the TSM_H pin.

  The Byte Mask signals specify which data bytes of the current transfer contain valid information during the data phase of the bus cycle. If BM_L/TEST<3>,BM_L/TEST<2> are asserted, then CDAL<31:16> contain valid data; if BM_L/TEST<1>,BM_L/TEST<0> then CDAL<15:0>; if they are all asserted, then CDAL<31:0>.

During read cycles, the byte masks indicate which bytes of data, and which bits of parity, must be placed on the CDAL and Data Parity lines; if this amounts to less than 32 bits, the other bytes of the CDAL and bits of Data Parity are ignored. During write cycles, the byte masks specify which bytes of the CDAL bus, and which Data Parity bits, contain valid data. The BM_L/TEST<3:0> signals are initially evaluated at the time AS_L is asserted, then each time DS_L is asserted for multiple words transfer cycles.

Note: When the SGEC is accessed as slave, these signal must be "0" as only longword accesses are permitted to SGEC CSR's.

When the TSM_H pin is high, these pins are used as test pins. They may be used to read and write test information from/to the SGEC. Detailed test mode operation is provided in the Chapter 7.

- **CS/DP_L<3:0>** - Cycle Status/Data Parity - (I/O Pins)

CS/DP_L<3:0> are time-multiplexed signals. During the first part of bus cycles, CS/DP_L<2:0>, in conjunction with the WR_L signal, provide status about the current bus cycle. When the SGEC is bus master, it initiates only D-stream read (no lock or modify intent) or write no unlock bus cycles; when it is the bus slave, it responds to only D-stream read (no lock or modify intent), write no unlock, or interrupt acknowledge. Specifically, WR_L and CS/DP_L<2:0> mean the following when AS_L is asserted:

WR_L	CS/DP_L<2:0>	Cycle type
H	L H H	Interrupt Acknowledge
H	H H H	Demand D-stream read (no lock or modify intent)
L	H H H	Write no unlock

When the SGEC is bus master, it uses CS/DP_L<3> to tell the memory controller whether this is a synchronous or an asynchronous bus operation. The SGEC will drive it low for synchronous transfers.

During the second part of bus cycles, CS/DP_L<3:0> provide byte parity for the CDAL bus data. Even parity is checked/generated on even bytes; odd parity on odd bytes. Even parity will drive a Low when there are an even number of "1"'s in the byte's data; odd parity will drive a Low for an odd number of "1"'s. CS/DP_L<3> is the parity signal for CDAL<31:24>, CS/DP_L<2> for CDAL<23:16>, CS/DP_L<1> for CDAL<15:8>, CS/DP_L<0> for CDAL<7:0>. On an SGEC read, the SGEC reads and checks data parity for the bytes specified by BM_L<3:0> if Data Parity Enable (DPE_L) is asserted. On an SGEC write , the SGEC generates data parity for all bytes, irrespective of BM_L<3:0>.

- AS_L - Address Strobe - (I/O Pin)

When the SGEC is the bus slave, the host CPU asserts AS_L to indicate it has placed an address on the CDAL lines. The SGEC latches the CDAL information at that time, and interprets it as a physical address.

When the SGEC chip is bus master (i.e., when it is performing DMA cycles to host memory), AS_L is used to indicate that it has placed a physical address on the CDAL lines.

- **DS_L** - Data Strobe - (I/O Pin)

  DS_L provides the timing control for the data transfer portion of the cycle.

  When the SGEC is the bus slave, in a read cycle the falling edge of DS_L indicates the CDAL lines are free to receive data from the SGEC internal registers; the rising edge indicates that it has been latched by the host CPU and can be removed. In a write cycle, the falling edge indicates the host should place data on the CDAL lines; the rising edge indicates the data may be removed.

  When the SGEC chip is bus master, during a read cycle DS_L is used to indicate the memory controller should place data on the CDAL lines; the rising edge indicates it has been latched by the SGEC and can be removed. In a write cycle, the falling edge indicates the SGEC has placed data on the CDAL lines, and the rising edge indicates the data will be removed.

- **WR_L** - Write - (I/O Pin)

  The Write signal is used to specify the direction of the current bus transfer.

  When the SGEC is the slave, if WR_L is asserted, the bus master (CVAX) will drive the CDAL lines at data time; if WR_L is not asserted the SGEC is expected to supply data.

  When the SGEC is bus master, it will use the Write signal to specify the direction of the current bus transfer. If WR_L is asserted, the SGEC will drive the CDAL lines at data time; if WR_L is not asserted, the SGEC expects to get the data from the bus slave (memory controller).

  In slave mode the SGEC sample the WR_L line at the time AS_L is asserted. In master mode the SGEC drive this line during all the bus cycle time.

- **RDY_L** - Ready - (I/O Pin) - (Open Drain)

  RDY_L is used to synchronize data transfers between the SGEC and host CPU or memory controller. During the data phase of the bus cycle, the bus master must wait for RDY_L to be asserted by the addressed device before terminating the current cycle and latching (or removing) data from the bus.

  When the SGEC is in slave mode, RDY_L assertion signals a CSR access or interrupt cycle completed.

  When the SGEC is the bus master, it waits for the slave (memory controller) to assert RDY_L to indicate transfer completed.

- **DPE_L** - Data Parity Enable - (I/O Pin) - (Open Drain)

  This pin is used to control CP-BUS parity checking.

  During an SGEC master read or slave write DPE_L is asserted by external logic in conjunction with the CDAL data in order to enable parity checking on the incoming CDAL data. When deasserted, the CS/DP_L lines parity information part is ignored.

During an SGEC master write, or slave read or interrupt acknowledge cycles. the DPE_L pin will always be asserted by the SGEC in conjunction with the CDAL data in order to indicate that valid parity information is present.

- **CCTL_L** - Cache invalidate control - (Output Pin) - (Open Drain)

  This pin is used to signal to the host CPU that a memory location is being written to and should initiate a conditional cache invalidate cycle.

- **ERR_L** - Bus Error - (Input Pin)

  This signal is used by external logic to indicate abnormal termination of the current bus cycle. This is typically due to an uncorrectable memory error.

  The SGEC monitors this pin, never asserts it.

- **NSGEC_L** - Not SGEC Reference. - (Output Pin)

  The pin will be asserted when a bus cycle did not address the SGEC. This pin is active only when the CSL_L pin was Low during reset.

- **CSL_L** - Chip Select pin. - (Input Pin)

  This pin is used for addressing the SGEC when the user has elected not to use the internal predefined SGEC addresses or when multiple SGEC's are present on the same CP-BUS.

- **DMR_L** - DMA Request - (Output Pin) - (Open Drain)

  Used to request bus mastership on the CP-BUS bus. Following the assertion of the signal, the host asserts DMGI_L, allowing the SGEC to take over the bus. The SGEC then performs one or more bus cycles and deasserts DMR_L to relinquish the bus.

- **DMGI_L** - DMA Grant Input - (Input Pin)

  This pin is used for bus grant arbitration. If the SGEC has asserted DMR_L, DMGI_L assertion tells the SGEC it acquired bus mastership.

- **IRQ_L** - Interrupt Request - (Output Pin) - (Open Drain)

  This line is used to signal interrupts from the SGEC to the host CPU.

- **IAKEI_L** - Interrupt Acknowledge Enable Input - (Input Pin)

  This pin is used to control interrupt arbitration. Interrupting devices are usually daisy chained with IAKEI_L coming from IAKEO_L of the preceding device in the chain.

- **IAKEO_L** - Interrupt Acknowledge Enable Output - (Output Pin)

  IAKEO_L is used to daisy-chain interrupting devices. It is usually connected to IAKEI_L of the next device in the chain. IAKEO_ L is asserted whenever the SGEC is not the target of an interrupt acknowledge cycle. It permits the next device(s) in the chain to acknowledge the interrupt.

- **CLKA, CLKB** - Clock Inputs - (Input Pin)

  Those two pins are the system clock input pins, they are complementary clock phases, with CMOS level inputs.

Synchronous mode operation requires these clocks come from the **same** source used to clock all other synchronous devices on the CP-BUS. When working asynchronously they can be supplied from a different source.

- **RX** - Receive Data - (Input Pin)

  This pin carries the input receive data from the SIA. The incoming data should be synchronous with the RCLK signal.

- **RCLK** - Receive Clock - (Input Pin)

  This pin carries the recovered receive clock supplied by an external SIA. During idle periods the RCLK pin may be inactive.

- **RXEN_H** - Receive Enable - (Input Pin)

  This pin signals activity on the Ethernet cable to the SGEC. It is asserted when receive data is present on the Ethernet cable and deasserted at the end of a frame. It should be asserted and deasserted synchronously with RCLK.

- **CLSN_H** - Collision Detect - (Input Pin)

  This pin signals collision occurrence on the Ethernet cable to the SGEC. It is asserted or deasserted by the SIA.

- **TX** - Transmit Data - (Output Pin)

  This pin carries the serial output data from the SGEC. The data is synchronized to the TCLK signal.

- **TCLK** - Transmit Clock - (Input Pin)

  This pin carries the transmit clock supplied by an external SIA. This clock should always be active.

- **TXEN_H** - Transmit Enable - (Output Pin)

  This pin signals SGEC transmit in progress to an external SIA.

- **VDD** - Power

  +5V, supplied through eight pins.

- **VSS** - Ground

  Ground, supplied through nine pins.

- **TSM_H** - Test Mode. - (Input Pin)

  This pin is used for selecting the operating mode of the SGEC. When tied to VDD, the SGEC is in test mode and pins BM_L/TEST<3:0> function as test pins. When connected to VSS, BM_L/TEST<3:0> carry the byte mask information.

- **RESET_L** - Reset - (Input Pin)

  Resets the SGEC to its initial state. This signal needs to be at least six clock cycles high. During reset all output pins are tristated and all open drain signals are floated. This signal is also used to synchronize the internal clock phases.

Note: The *NSGEC_L* and *IAKEO_L* are exceptions to this rule at reset they are deasserted and not floated.

4 Host bus protocols

The SGEC uses the host bus to communicate with the host cpu and memory controller (such as the CVAX and CMCTL chips). The SGEC is directly compatible with the *CP-BUS* (CVAX pin bus) and uses a subset of the CVAX chip inputs and outputs. It supports a subset of the CP-BUS cycles (transactions) in either synchronous or asynchronous operating modes. It operates as the bus slave when communicating with the CVAX and as the bus master when communicating with the CMCTL. For detailed timing information see Chapter 9, AC/DC Characteristics.

Note: The SGEC, being CP-BUS compatible, does not require nor checks for the presence of CVAX or CMCTL chips. Although both the CVAX and the CMCTL are mentioned throughout this chapter, they merely represent currently available CP-BUS compatible host cpu and memory controller devices.

Note: The term *clock cycle* used throughout this chapter, refers to the 80ns period specified for the CMOS II CVAX family.

4.1 Bus operating modes

The SGEC operates in either synchronous or asynchronous mode when it is the bus master. A CSR bit is used to select the mode.

When it is the bus slave, it only supports asynchronous mode.

4.1.1 Synchronous mode

When the SGEC is bus master in synchronous mode, CS/DP_L<3> is driven low during the first part of the bus cycle.

Note: Synchronous mode operation gives the best attainable host bus performance.

4.1.2 Asynchronous mode

When the SGEC is in asynchronous mode, all inputs are routed through synchronizers, thus it can take input signals with arbitrary timings. However, the SGEC output signals are always driven as if it were synchronous mode, with the exception that an additional delay cycle is added between successive master DMA transfers.

4.2 Bus slave (CSRs accesses) operation

All host accesses to CSRs in the SGEC are carried out with the SGEC being the slave. A detailed description of the CSRs is contained in Chapter 5, Programming.

The supported CP-BUS cycles (transactions) are:

- Demand D stream read (no lock or modify intent), for host reading a CSR.
- Write no unlock, for host writing a CSR.
- Interrupt acknowledge.

Only single transfers are supported in slave mode.

4.2.1 SGEC addressing

The CSRs addresses are allocated in the CVAX I/O address space. Every SGEC is allocated 16 addresses, one for each CSR. CSRs are longwords and only longword accessible.

The SGEC contains the address decoding logic for a *single* set of CSRs at 20008000 through 2000803C (hex). - hereafter referred to as the *internal address*. When multiple SGECs are to be used in a system, external logic has to perform the address decoding and drive a *chip select* input (pin CSL_L) to the SGEC.

The decision on whether to respond to the internal address or monitor the CSL_L pin, is done at reset time. If pin CSL_L is pulled *low* at reset time, the SGEC will respond to the internal address, else it will monitor the CSL_L input.

When the SGEC is instructed to respond to the internal address, and for CP-BUS cycles other than *interrupt acknowledge*, it also drives an output pin - NSGEC_L. This pin will be asserted whenever the SGEC was **not** addressed. NSGEC_L will be valid within one and a half clock cycles (six phases) of the assertion of AS_L. If NSGEC_L was asserted, it will deassert after AS_L deasserts.

4.2.2 Bus holding policy

The 16 CSRs of the SGEC are subdivided into two blocks:

1 Physical CSRs

CSRs 0-7,15 are physically present in the chip. Access to any of these CSRs will take four to five clock cycles - until RDY_L is asserted.

2 Virtual CSRs

CSRs 8-14 are not physically present and are handled by the on-chip processor. Host access to these CSRs is a two or three stage process.

First, upon a host access the SGEC will assert RDY_L within four to five clock cycles, then, the host must poll the CSR5<DN> bit, which signals that the action, implied by the first CSR access, has completed. If the first CSR access was a read, the host must reissue the read, and only then will it receive valid data.

4.2.3 Host read cycle

A host read cycle takes the following steps:

1. The host initiates a read cycle by asserting AS_L with WR_L deasserted, writing "111" to CS/DP_L<2:0> (*demand D stream read*) and driving the address of the device register to be read onto the CDAL pins.
2. The SGEC latches the address, CS/DP_L<2:0>, BM_L<3:0> and WR_L on the leading edge of AS_L.
3. The SGEC deasserts the NSGEC_L pin, and places data onto CDAL<31:0>. Driving of CDAL pins begins as soon as the address is decoded, so as to not leave them floating. However, the data driven is *arbitrary* and should not be considered valid. Parity data is placed on the CS/DP_L pins and DPE_L is asserted.
4. The SGEC then asserts RDY_L to inform the host that data on the CDAL pins is valid.
5. Finally, after the host deasserts DS_L and AS_L, the SGEC deasserts DPE_L and RDY_L.

A host read cycle takes from four to five clock cycles.

4.2.4 Host write cycle

A host write cycle takes the following steps:

1. The host initiates a write cycle by asserting AS_L, asserting WR_L, writing "111" to CS/DP_L<2:0> (*write no unlock*) and driving CDAL pins with the address of the device register to be written.
2. The SGEC latches the address, CS/DP_L<2:0>, BM_L<3:0> and WR_L on the leading edge of AS_L.
3. The SGEC deasserts the NSGEC_L pin.
4. After DS_L has been asserted, the SGEC latches the data on CDAL<31:0>, CS/DP_L<3:0> and DPE_L.

Note: The BM_L pins must be all "0", otherwise, the SGEC will ignore the written data without any error indication.

5. The SGEC then asserts RDY_L to inform the host that the data has been sampled.
6. Finally, after the host deasserts DS_L and AS_L, the SGEC deasserts RDY_L.
7. If DPE_L was asserted, the SGEC checks the parity data. If a parity error is detected, an interrupt is generated to the host cpu.

A host write cycle takes four to five clock cycles.

4.2.5 Interrupt acknowledge cycle

An interrupt acknowledge cycle follows the same general pattern as a host read cycle.

1 The host initiates an interrupt acknowledge cycle by asserting IAKEI_L, driving the IPL on CDAL<6:2> with WR_L deasserted and writing "011" to the CS/DP_L<2:0> pins.

2 The SGEC responds to an interrupt acknowledge cycle under the following conditions:

- The SGEC had requested an interrupt
- IAKEI_L is asserted
- The IPL driven on CDAL<6:2> matches the SGEC programmed IPL

3 The SGEC then drives CDAL<15:2> with the appropriate interrupt vector (CDAL<31:16,1:0> = "0"), places parity data onto CS/DP_L, asserts DPE_L and asserts RDY_L to indicate to the host that a valid vector address is present on CDAL pins.

4 The host reads the interrupt vector, and resumes the cycle as for a host read cycle. The SGEC releases IRQ_L, RDY_L, DPE_L and CDAL pins.

If IAKEI_L asserts, but one of the other conditions is not met, the SGEC asserts IAKEO_L to pass the interrupt acknowledge to the next device in the interrupt acknowledge daisy chain.

4.3 Bus master (DMA) operation

The following CP-BUS cycles are supported:

- Demand D-stream read (no lock or modify intent)
- Write no unlock

The SGEC supports either *single transfers* or *octaword transfers* in either of the above cycles.

4.3.1 Bus arbitration and holding policy

The SGEC requests host bus mastership by asserting DMR_L, after checking that DMGI_L is not asserted. The first bus cycle starts one to two clock cycles following DMGI_L assertion. The bus is released by deasserting DMR_L.

The amount of time the SGEC will hold the bus is controlled by a programmable parameter - *burst limit*. The burst limit parameter sets an upper limit to the number of longwords which may be transferred before releasing the bus. The SGEC supports burst limits of 1,2,4,8 longwords or *burst limit disable*, in which case the SGEC holds the bus for as long as it needs it, typically until the whole FIFO (120 bytes) completely fills or empties. Table 4–1 specifies the maximum bus holding time versus burst limit size (assuming no CMCTL delays and burst start address in not octaword aligned):

Table 4–1 Maximum bus holding time

Burst limit (longwords)	Holding time (clock cycles)
1	4
2	8
4	16
8	26
Disabled	150 approx.

4.3.2 Single read cycle

In a single read cycle, the SGEC reads one longword from host memory. A single read cycle takes upward of three clock cycles.

The steps in the single read cycle are described in Table 4–2.

Table 4–2 Single read cycle

Clock cycle	Typical phase	Pins actions
1	3	The SGEC drives the address onto CDAL<29:02>. CDAL<31:30> are set "01" to indicate single transfer. WR_L is deasserted. BM_L/TEST<3:0> are all asserted. CS/DP_L<2:0> are set to "111" (*demand D stream read*).
2	1	The SGEC asserts AS_L, indicating that the address is valid.
	2	The SGEC tristates CDAL<31:0>.
	3	The SGEC asserts DS_L, indicating that the CDAL bus is free to receive incoming data.
	4	The SGEC tests for *cycle complete* (RDY_L or ERR_L asserted) once every clock cycle. In a normal, error-free transfer, data is valid on CDAL<31:0>. When RDY_L is asserted, with ERR_L deasserted, the SGEC latches the data from CDAL<31:0>, CS/DP_L<3:0> and DPE_L. Should an error occur (e.g., time out), external logic will respond by asserting ERR_L with RDY_L deasserted. The SGEC will ignore the data on CDAL<31:0>.
3...	1	SGEC deasserts DS_L.
	2	SGEC deasserts AS_L.

If DPE_L was asserted, the SGEC does a parity check by computing the CDAL<31:0> parity and comparing it to the CS/DP_L<3:0> pins. Should a parity error be detected, the SGEC generates an interrupt to the host cpu.

4.3.3 Single write cycle

In a single write cycle, the SGEC writes a single longword to host memory. A single write cycle takes upward of three clock cycles.

The steps in the single write cycle are described in Table 4–3.

Table 4–3 Single write cycle

Clock cycle	Typical phase	Pins actions
1	3	The SGEC drives the address onto CDAL<29:02>. CDAL<31:30> are set to "01" to indicate single longword transfer. CCTL_L and WR_L are asserted. BM_L/TEST<3:0> are asserted as required. CS/DP_L<2:0> are set to 111 (*write no unlock*).
2	1	The SGEC asserts AS_L, indicating that the address is valid.
	3	The SGEC drives CDAL<31:0> with valid data, drives parity data onto CS/DP_L<3:0>, and asserts DS_L and DPE_L. CCTL_L is deasserted.
	4	The SGEC tests for *cycle complete* (RDY_L or ERR_L asserted) once every clock cycle. RDY_L is asserted with ERR_L deasserted. Should an error occur (e.g., time out), external logic will respond by asserting ERR_L with RDY_L deasserted.
3...	1	SGEC deasserts DS_L.
	2	SGEC deasserts AS_L.

4.3.4 Octaword read cycle

In an octaword read cycle, the SGEC reads four consecutive longwords, supplying only the start address. This mode will be used when the burst limit is set to 4 or greater, the SGEC needs four longwords and the start address is octaword aligned.

An octaword read cycle takes upward of ten clock cycles.

The steps in the octaword DMA read cycle, no error, are described in Table 4–4.

In case of an error (ERR_L asserted with RDY_L deasserted) in either of the four longwords transfers, the SGEC aborts the read cycle after completing the current longword transfer, by releasing the bus without completing the transfer of any remaining longwords.

Table 4–4 Octaword read cycle

Clock cycle	Typical phase	Pins actions
1	3	The SGEC drives the address of the first longword onto CDAL<29:02>. This address will always be octaword aligned. CDAL<31:30> are set to "11" to indicate octaword transfer. WR_L is deasserted. BM_L/TEST<3:0> are all asserted. CS/DP_L<2:0> are set to "111" (*demand D stream read*).
2	1	The SGEC asserts AS_L, indicating that the address is valid.
	2	The SGEC releases CDAL<31:0>.
	3	DS_L is asserted, indicating that the CDAL pins are free to receive incoming data.
	4†	The SGEC tests for *transfer complete* (RDY_L or ERR_L asserted) once every clock cycle. In a normal, error-free transfer, data is asserted on CDAL<31:0>. RDY_L is asserted with ERR_L deasserted and the SGEC latches the data from the CDAL<31:0>, CS/DP_L<3:0> and DPE_L pins.
3	1	First longword transfer is finished by deasserting DS_L.
4...	3†	The SGEC reasserts DS_L.
	4†	The SGEC tests again for next *transfer complete* (RDY_L or ERR_L asserted) once every clock cycle and reads the next three longwords from the CDAL pins as it did for the first, finishing each transfer by deasserting DS_L.
9...	1	SGEC deasserts DS_L for the last time.
	2	The octaword read cycle is finished by the SGEC deasserting AS_L.

† The SGEC is capable of initiating a longword transfer once every *two* clock cycles in octaword transfer cycles, even though RDY_L is sampled every cycle.

If DPE_L was asserted, the SGEC does a parity check by computing the CDAL<31:0> parity and comparing it to the CS/DP_L<3:0> pins. Should a parity error be detected, the SGEC generates an interrupt to the host cpu.

4.3.5 Octaword write cycle

In an octaword write cycle, the SGEC writes four consecutive longwords, supplying the start address only. This mode is used if the burst limit is set to 4 or greater, the SGEC needs to write four longwords and the starting address is octaword aligned.

An octaword write cycle takes upward of nine clock cycles.

The steps in the octaword DMA write cycle, no error, are described in Table 4–5. In case of error (ERR_L asserted with RDY_L deasserted) in either of the four longwords transfers, the SGEC will complete the whole octaword write cycle driving the BM_L/TEST<3:0> to all "1", and only then release the bus.

Table 4–5 Octaword write cycle

Clock cycle	Typical phase	Pins actions
1	3	The SGEC drives the address of the first longword onto CDAL<29:02>. This address will always be octaword aligned. CDAL<31:30> are set to "11" to indicate octaword transfer. CCTL_L and WR_L are asserted. BM_L/TEST<3:0> are asserted as required. CS/DP_L<2:0> are set to "111" (*write no unlock*).
2	1	The SGEC asserts AS_L, indicating that the address is valid.
	3	The SGEC drives CDAL<31:0> with valid data, places parity data onto CS/DP_L<3:0> and asserts DS_L and DPE_L. CCTL_L is deasserted.
	4†	The SGEC tests for *transfer complete* (RDY_L or ERR_L asserted) once every clock cycle. In a normal, error-free transfer, RDY_L is asserted with ERR_L deasserted and CMCTL reads the data from the CDAL bus.
3	1	First longword transfer is finished by deasserting DS_L.
4...	3†	The SGEC reasserts DS_L. CCTL_L is reasserted when DS_L asserts for the third longword, and deasserted one clock cycle later.
	4†	The SGEC tests again for next *transfer complete* (RDY_L or ERR_L asserted) once every clock cycle and writes the next three longwords to the CDAL pins as it did for the first, finishing each transfer by deasserting DS_L.
9...	1	SGEC deasserts DS_L for the last time.
	2	The octaword write cycle is finished by the SGEC deasserting AS_L.

† The SGEC is capable of initiating a longword transfer once every *two* clock cycles in octaword transfer cycles, even though RDY_L is sampled every cycle.

5 Programming

The operation of the SGEC is controlled by a program in host memory called the port driver. The SGEC and the port driver communicate through two data structures: *Command and Status Registers (CSRs)* located in the SGEC and mapped in the host I/O address space, and through *descriptors lists and data buffers*, collectively called *Host Communication Area*, in host memory. The CSRs are used for initialization, global pointers, commands and global errors reporting, while the host memory resident structures handle the actions and statuses related to buffer management.

5.1 Programming Overview

The SGEC can be viewed as two independent, concurrently executing processes: *Reception* and *Transmission*. After the SGEC completes its *Initialization* sequence, those two processes alternate between three states: *STOPPED, RUNNING* or *SUSPENDED*. State transitions occur as a result of port driver commands (writing to a CSR) or various external events occurrences. Some of the port driver commands require the referenced process to be in a specific state.

A simple programming sequence of the chip may be summarized as:

1. After power on (or reset), verifying the self test completed successfully.
2. Writing CSRs to set major parameters such as System Base Register, Interrupt Vector, Address Filtering mode and so on.
3. Creating the transmit and receive lists in memory and writing the CSRs to identify them to the SGEC.
4. Placing a setup frame in the transmit list, to load the internal reception address filtering table.
5. Starting the Reception and Transmission processes placing them in the RUNNING state.
6. Waiting for SGEC interrupts. CSR5 contains all the global interrupt status bits.
7. Issuing a *Poll Demand* command, if either of the Reception or Transmission processes enter the SUSPENDED state, after having remedied the suspension cause.

The following sections contain detailed programming and state transitions information.

5.2 Command and Status Registers

The SGEC contains 16 registers, most of which may be accessed by the host while the rest are reserved.

5.2.1 Host access to CSRs

The SGEC's CSRs are located in VAX I/O address space.

The CSRs must be **longword** aligned and can only be accessed using **longword** instructions. The address of CSRx is the base address plus 4x bytes. For example, if the base address is 2000 8000, then the address of CSR2 is 2000 8008. In the following paragraphs, CSRs bits are specified with several access modes. The different access modes for bits are as follows:

Table 5–1 Bit access modes

Bit marked	Meaning
0	Reserved for future expansion - Ignored on Write, Read as "0"
1	Reserved for future expansion - Ignored on Write, Read as "1"
R	Read only, ignored on Write
R/W	Read or Write
W	Write only, unpredictable on Read
R/W1	Read, or Clear by writing a "1". Writing with a "0" has no effect.

In order to save chip real estate, yet not tie up the host bus for extended periods of time, the 16 CSRs are subdivided into two groups:

1 Physical CSRs - 0 through 7, 15.

2 Virtual CSRs - 8 through 14.

The group the CSR is part of, determines the way the host will access it.

5.2.1.1 Physical CSRs

These registers are physically present in the chip. Host access to these CSRs is by a single instruction (e.g., MOVL). There is no host perceivable delay and the instruction completes immediately. Most commonly used SGEC features are contained in the physical CSRs.

5.2.1.2 Virtual CSRs

These registers are not physically present in the SGEC and are incarnated by the on-chip processor. Accesses to SGEC functions implied by these registers may take up to 20 μseconds. So as not to tie up the host bus, virtual CSR access requires several steps by the host.

CSR5<DN> is used to synchronize access to the virtual CSRs. Before accessing a virtual CSR, CSR5<DN> must be checked to be set. After the first virtual CSR access, the SGEC will zero CSR5<DN>. After the SGEC completes the action, it will set CSR5<DN>.

5.2.1.2.1 CSR write

To write to a virtual CSR the host takes the following actions:

1 Issue a write CSR instruction. Instruction completes immediately, but the data is not yet copied by the SGEC.

2 Poll on CSR5<DN>. *No SGEC virtual CSR may be accessed before CSR5<DN> asserts.*

5.2.1.2.2 CSR read

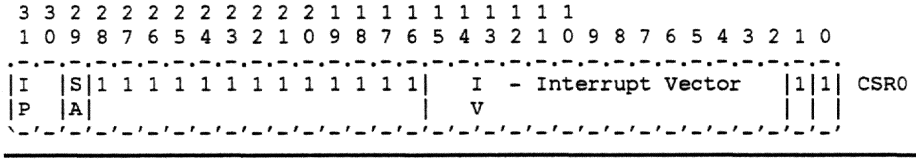
To read a virtual CSR the host takes the following actions:

1. Issue a read CSR instruction. Instruction completes immediately, but no valid data is sent to the host.
2. Poll on CSR5<DN>. *No SGEC virtual CSR may be accessed before CSR5<DN> asserts.*
3. Reissue a read CSR instruction, to the *same* CSR as in step 1. The host receives valid data.

5.2.2 Vector Address, IPL, Sync/Asynch (CSR0)

Since the SGEC may generate an interrupt, on parity errors, during host writes to CSR's, this register **must be the first one written** by the host.

Figure 5–1 CSR0 format



Crucial: A parity error during CSR0 host write may cause a host system crash due to an erroneous Interrupt Vector. To protect against such an eventuality, CSR0 must be written as follows:

1. **Write CSR0.**
2. **Read CSR0.**
3. **Compare value read to value written. In values mismatch, repeat from step 2.**
4. **Read CSR5 and examine CSR5<ME> for pending parity interrupt. Should an interrupt be pending, write CSR5 to clear it.**

Table 5–2 CSR0 bits

Bit	Name	Access	Description
15:00	IV	R/W	Interrupt Vector - During an Interrupt Acknowledge cycle for an SGEC interrupt, this is the value that the SGEC will drive on the host bus CDAL<31:0> pins (CDAL pins <1:0> and <31:16> are set to "0"). Bits <1:0> are ignored when CSR0 is written, and set to "1" when read.
29	SA	R/W	Sync/Asynch - This bit determines the SGEC operating mode when it is the bus master. When set, the SGEC will operate as a synchronous device and when clear, the SGEC will operate as a asynchronous device.

Table 5–2 (Cont.) CSR0 bits

Bit	Name	Access	Description
31:30	IP	R/W	Interrupt Priority - is the VAX interrupt priority level that the SGEC will respond to.

IP	IPL (hex)
00	14
01	15
10	16
11	17

Although the SGEC only has one interrupt request pin, that pin might be wired to any of the four IRQ pins on the host. The value in IP should correspond to the IPL level that the pin is wired to.

5.2.3 Polling Demand (CSR1)

Figure 5–2 CSR1 format

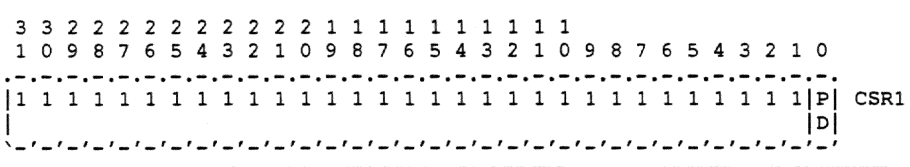


Table 5–3 CSR1 bits

Bit	Name	Access	Description
00	PD	R/W	Polling Demand - Polls the receive list only if it has not previously acquired a free descriptor. Checks the transmit list for frames to be transmitted.

5.2.4 Reserved register (CSR2)

This entire register is reserved.

5.2.5 Descriptor List addresses (CSR3, CSR4)

The two descriptors lists heads address registers are identical in function, one being used for the transmit buffer descriptors and one being used for the receive buffer descriptors. In both cases, the registers are used to point the SGEC to the start of the appropriate buffer descriptor list.

The descriptors lists reside in VAX **physical** memory space and must be **longword** aligned.

Note: **For best performance, it is recommended that the descriptors lists be octaword aligned.**

Initially, these registers **must be written before the respective Start command is given** (see Section 5.2.7), else the respective process will remain in the STOPPED state. New list head addresses are only acceptable while the respective process is in the STOPPED or SUSPENDED states. Addresses written while the respective process is in the RUNNING state, are *ignored* and *discarded*.

If the host attempts to read any of these registers before ever writing to them, the SGEC responds with unpredictable values.

Figure 5–3 Descriptor list addresses format

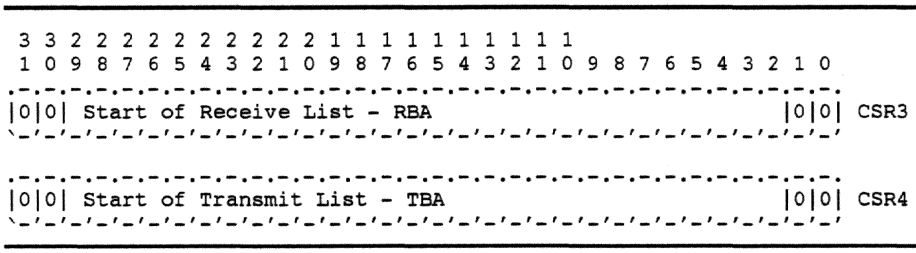


Table 5–4 Descriptor lists addresses bits

Bit	Name	Access	Description
29:00	RBA	R/W	Address of the start of the receive list. This is a 30-bit VAX physical address.
29:00	TBA	R/W	Address of the start of the transmit list. This is a 30-bit VAX physical address.

5.2.6 Status Register (CSR5)

This register contains all the status bits the SGEC reports to the host.

Figure 5–4 CSR5 bits

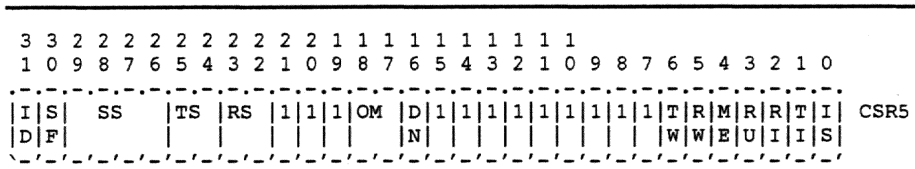


Table 5–5 CSR5 bits

Bit	Name	Access	Description
0	IS	R/W1	Interrupt Summary - The logical "OR" of CSR5 bits 1 through 6.
		Pass1 restriction:	**This bit does not function properly in pass1 parts. It may be fixed for pass2.**
1	TI	R/W1	Transmit Interrupt - When set, indicates one of the following: • Either all the frames in the transmit list have been transmitted (next descriptor owned by the host), or a frame transmission was aborted due to a locally induced error. The port driver must scan down the list of descriptors to determine the exact cause. The Transmission process is placed in the SUSPENDED state. Section 5.4.5 explains the Transmission process state transitions. To resume processing transmit descriptors, the port driver must issue the Poll Demand command. • A frame transmission completed, and TDES1<IC> was set. The Transmission process remains in the RUNNING state, unless the next descriptor is owned by the host or the frame transmission aborted due to an error. In the latter cases, the Transmission process is placed in the SUSPENDED state.
2	RI	R/W1	Receive Interrupt - When set, indicates that a frame has been placed on the receive list. Frame specific status information was posted in the descriptor. The Reception process remains in the RUNNING state.
3	RU	R/W1	Receive buffer Unavailable - When set, indicates that the next descriptor on the receive list is owned by the host and could not be acquired by the SGEC. The Reception process is placed in the SUSPENDED state. Section 5.4.4 explains the Reception process state transitions. Once set by the SGEC, this bit will not be set again until a Poll Demand is issued and the SGEC encounters a descriptor it can not acquire. To resume processing receive descriptors, the host must issue the Poll Demand command.

Table 5–5 (Cont.) CSR5 bits

Bit	Name	Access	Description
4	ME	R/W1	Memory Error - Is set when any of the followings occur: • SGEC is the CP-BUS Master and the ERR_L pin is asserted by external logic (generally indicative of a memory problem). • Parity error detected on an host to SGEC CSR write or SGEC read from memory. When a Memory Error is set, the Reception and Transmission processes are **aborted** and placed in the STOPPED state. **Note: At this point, it is mandatory that the port driver issue a Reset command and rewrite all CSRs.**
5	RW	R/W1	Receive Watchdog Timer interrupt - When set, indicates the Receive Watchdog Timer has timed out, indicating that some other node is babbling on the network. Current frame reception is aborted and RDES0<LE> and RDES0<LS> will be set. Bit CSR5<RI> will also set. The Reception process remains in the RUNNING state.
6	TW	R/W1	Transmit Watchdog Timer interrupt - When set, indicates the transmit watchdog timer has timed out, indicating the SGEC transmitter was babbling. The Transmission process is *aborted* and placed in the STOPPED state.
16	DN	R	Done - When set, indicates the SGEC has completed a requested virtual CSR access. After a reset, this bit is set.
18:17	OM	R	Operating Mode - These bits indicate the current SGEC operating mode as in the following table:

Value	Meaning
00	Normal operating mode.
01	Internal Loopback - Indicates the SGEC is disengaged from the Ethernet wire. Frames from the transmit list are looped back to the receive list, subject to address filtering. Section 5.4.6 explains this mode of operation.
10	External Loopback - Indicates the SGEC is working in full duplex mode. Frames from the transmit list are transmitted on the Ethernet wire and also looped back to the receive list, subject to address filtering. Section 5.4.6 explains this mode of operation.
11	Diagnostic Mode - Explained in Chapter 7.

Table 5–5 (Cont.) CSR5 bits

Bit	Name	Access	Description
23:22	RS	R	Reception process State - Indicates the current state of the Reception process, as follows:

Value	Meaning
00	STOPPED
01	RUNNING
10	SUSPENDED

Section 5.4.4 explains the Reception process operation and state transitions.

25:24	TS	R	Transmission process State - Indicates the current state of the Transmission process, as follows:

Value	Meaning
00	STOPPED
01	RUNNING
10	SUSPENDED

Section 5.4.5 explains the Transmission process operation and state transitions.

29:26	SS	R	Self test Status - The self test completion code according to the following table. Only valid if SF is set.

Value	Meaning
0001	ROM error
0010	RAM error
0011	Address filter RAM error
0100	Transmit FIFO error
0101	Receive FIFO error
0100	Special loopback error

Pass1 info: Self test takes 30 milliseconds to complete.

30	SF	R	Self test Failed - When set, indicates the SGEC self test has failed. The self test completion code bits indicate the failure type.
31	ID	R	Initialization Done - When set, indicates the SGEC has completed the Initialization (reset and self test) sequences, and is ready for further commands. When clear, indicates the SGEC is performing the Initialization sequence and ignore all commands. After the Initialization sequence completes, the Transmission and Reception processes are in the STOPPED state.

5.2.7 Command and Mode Register (CSR6)

This register is used to establish operating modes and for port driver commands.

Figure 5–5 CSR6 format

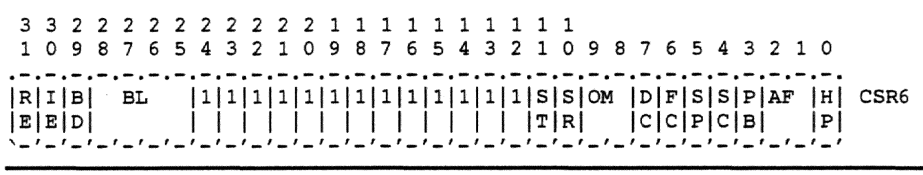


Table 5–6 CSR6 bits

Bit	Name	Access	Description
0	HP	R/W	Hash/Perfect filtering mode - When set, the SGEC will interpret the setup frame as a hash table, and do an imperfect address filtering. The imperfect mode is useful when there are more than 14 multicast addresses to listen to. When clear, the SGEC will do a perfect address filter of incoming frames according to the addresses specified in the setup frame. Refer to the AF bits and Section 5.3.3 for related information. **Note: Toggling this bit invalidates the internal address filtering table. The table is not disturbed but the receive logic will interpret its contents according to the value of the HP bit. The port driver *must* reload it with an appropriate setup frame. See Section 5.3.3.3 for more details.**
2:1	AF	R/W	Address Filtering mode - These bits define the way incoming frames will be address filtered:

Value	Meaning
00	Normal - Incoming frames will be filtered according to the value of the HP bit.
01	Promiscuous - All incoming frames will be passed to the host, regardless of the HP bit value.
10	All Multicast - All incoming frames with multicast address destinations will be passed to the host. Incoming frames with physical address destinations will be filtered according to the value of the HP bit.
11	Unused - Reserved.

Table 5–6 (Cont.) CSR6 bits

Bit	Name	Access	Description
3	PB	R/W	Pass Bad Frames mode - When this bit is set, the SGEC will pass frames that have been damaged by collisions or are too short due to premature reception termination. Both events should have occurred within the collision window (64 bytes), else other errors will be reported. bits SC,SP *must be set* as no stripping will be performed. When clear, these frames will be discarded and never show up in the host receive buffers. **Pass1 restriction: This mode should not be used as it does not work for frames shorter than 14 bytes. Consequently, the SGEC may dead lock.**
4	SC	R/W	Strip CRC Disable mode - When set, the SGEC will transfer CRC bytes, of a received frame, to host receive buffers. When clear, the CRC bytes will not be transferred to the host receive buffers. **This bit does not affect the CRC checking and reporting.** **Note: For IEEE type frames, the CRC bytes will not be moved to host memory. However, for Ethernet type frames, the CRC bytes will be moved to host memory but not reflected in the received frame length RDES0<FL>. Consequently, as any frame type might be arriving, host buffers should be large enough to accommodate the CRC bytes, else the SGEC might use the next buffer.**
5	SP	R/W	Strip Padding Disable mode - When this bit is set, the SGEC will transfer padding bytes, of a received frame, to host receive buffers. When clear, the padding bytes **and CRC bytes** will not be transferred to host receive buffers. **This bit does not affect the CRC checking and reporting.** **Note: In order to strip the padding, the SGEC looks at the frame length field in the receive frame. This field is present in IEEE 802.3 frames, but not in Ethernet frames. The SGEC makes its decision by examining this field and if it is less than 1500, it assumes it is dealing with an IEEE type frame and perform the stripping, if enabled. Should Ethernet type frames with protocol types less than 1500 be expected, stripping of both padding and CRC should be disabled, else frames might be corrupted.** **Stripping of padding bytes means less CP-BUS bandwidth is consumed for frames less than 64 bytes long.**

Table 5–6 (Cont.) CSR6 bits

Bit	Name	Access	Description
6	FC	R/W	Force Collision mode - This bit allows the collision logic to be tested. The chip must be in internal loopback mode for FC to be valid. If FC is set, a collision will be forced during the next transmission attempt. This will result in 16 transmission attempts with Excessive Collision reported in the transmit descriptor.
7	DC	R/W	Disable data Chaining mode - When set, no data chaining will occur in reception; frames, longer than the current receive buffer, will be truncated and RDES0<FS> and RDES0<LS> will always be set. The frame length returned in RDES0<FL> will be the *true* length of the non-truncated frame. It is up to the port driver to compare the frame length with the buffer size, thus determine whether a frame was actually truncated. When clear, frames too long for the current receive buffer, will be transferred to the next buffer(s) in the receive list.
9:8	OM	R/W	Operating Mode - These bits determine the SGEC main operating mode. Changing mode is permitted only when both the Reception and Transmission processes are in the STOPPED state, and ignored otherwise. The port driver must examine CSR5<OM> to verify the new setting took effect.

Value	Meaning
00	Normal operating mode.
01	Internal Loopback - The SGEC will loopback buffers from the transmit list. The data will be passed from the transmit logic back to the receive logic. The receive logic will treat the looped frame as it would any other frame, and subject it to the address filtering and validity check process.
10	External Loopback - The SGEC transmits normally and in addition, will enable its receive logic to its own transmissions. The receive logic will treat the looped frame as it would any other frame, and subject it to the address filtering and validity check process.
11	Diagnostic mode - Explained in the Chapter 7.

Table 5–6 (Cont.) CSR6 bits

Bit	Name	Access	Description
10	SR	R/W	Start/Stop Reception command - When set, the Reception process is placed in the RUNNING state, the SGEC attempts to acquire a descriptor from the receive list and process incoming frames. Descriptor acquisition is attempted from the current position in the list. If no descriptor can be acquired, the Reception process enters the SUSPENDED state. The Start Reception command is honored only when the Reception process is in the STOPPED state. *The first time this command is issued, an additional requirement is that CSR3 must already have been written to, else the Reception process will remain in the STOPPED state.* When cleared, the Reception process is placed in the STOPPED state, after completing reception of the current frame. The next descriptor position in the receive list is saved, and becomes the current position after reception is restarted. The Stop Reception command is honored only when the Reception process is in the RUNNING or SUSPENDED states. Refer to Section 5.4.4 for more information.
11	ST	R/W	Start/Stop Transmission command - When set, the Transmission process is placed the RUNNING state, the SGEC checks the transmit list at the current position for a frame to transmit. If it does not find a frame to transmit, the Transmission process enters the SUSPENDED state. The Start Transmission command is honored only when the Transmission process is in the STOPPED state. *The first time this command is issued, an additional requirement is that CSR4 must already have been written to, else the Transmission process will remain in the STOPPED state.* When cleared the Transmission process is placed in the STOPPED state after completing transmission of the current frame. The next descriptor position in the transmit list is saved, and becomes the current position after transmission is restarted. The Stop Transmission command is honored only when the Transmission process is in the RUNNING or SUSPENDED states. Refer to Section 5.4.5 for more information.
28:25	BL	R/W	Burst Limit mode - Specifies the maximum number of longwords to be transferred in a single DMA burst on the host bus. Permissible values are 1,2,4,8. After Initialization, the burst limit will be set to 1. Only meaningful when BD is clear. Chapter 4 describes host bus operation.
29	BD	R/W	Burst Limit Disable mode - When set, the SGEC may hold the bus for as long as it needs it. When cleared, BL defines the maximum length of a DMA burst. Chapter 4 describes host bus operation.

Table 5–6 (Cont.) CSR6 bits

Bit	Name	Access	Description
30	IE	R/W	Interrupt Enable mode - When set, setting of CSR5 bits 1 through 6 will cause an interrupt to be generated.
31	RE	R/W	Reset command - Upon being set, the SGEC will abort all processes and start the reset sequence. After completing the reset and self test sequence, the SGEC will set bit CSR5<ID>. Clearing this bit has no effect.

5.2.8 System Base Register (CSR7)

This CSR contains the physical starting address of the VAX System Page Table. This register must be loaded by host software before any address translation occurs so that memory will not be corrupted.

Figure 5–6 CSR7 format

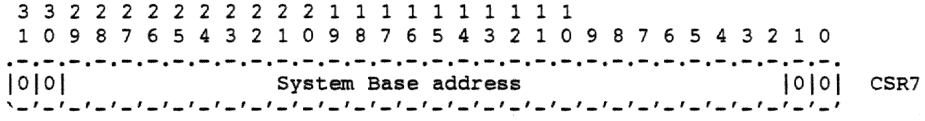


Table 5–7 CSR7 bits

Bit	Name	Access	Description
29:02	SB	R/W	System Base address - The physical starting address of the VAX System Page Table. Not used if VA (Virtual Addressing) is cleared in all descriptors. **This register should be loaded only once after a reset. Subsequent modifications of this register at any other time may cause unpredictable results.**

5.2.9 CSR8

This register is reserved.

5.2.10 Watchdog Timers (CSR9)

The SGEC has two timers that restrict the length of time in which the chip can receive or transmit.

Figure 5–7 CSR9 format

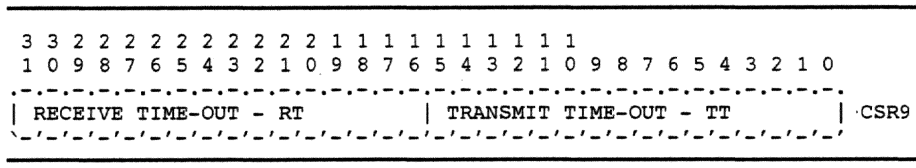


Table 5–8 CSR9 bits

Bit	Name	Access	Description
15:00	TT	R/W	TRANSMIT WATCHDOG TIME-OUT - The Transmit Watchdog Timer protects the network against babbling SGEC transmissions, on top of any such circuitry present in transcievers. If the transmitter stays on for $TT * 16$ cycles of the serial clock, the SGEC will cut off the transmitter and set the CSR5<TW> bit. If the timer is set to zero, it will never time-out. The value of TT is an unsigned integer. With a 10 MHz serial clock, this provides a range of 1.6μs to 100ms. The default value is 12500 corresponding to 20ms.
31:16	RT	R/W	RECEIVE WATCHDOG TIME-OUT - The Receive Watchdog Timer protects the host cpu against babbling transmitters on the network. If the receiver stays on for $RT * 16$ cycles of the serial clock, the SGEC will cut off reception and set the CSR5<RW> bit. If the timer is set to zero, it will never time-out. The value of RT is an unsigned integer. With a 10 MHz serial clock, this provides a range of 1.6μs to 100ms. The default value is 12500 corresponding to 20ms.
		Pass1 restriction:	**A value less than 45 *must not* be programmed as the SGEC will lock.**

These watchdog timers are enabled by default. These timers will assume the default values after hardware or software resets.

5.2.11 CSR10

This register is reserved.

5.2.12 Revision Number and Missed Frame Count (CSR11)

This register contains a missed frame counter and SGEC identification information.

Figure 5–8 Revision Number and Missed Frame Count (CSR11) format

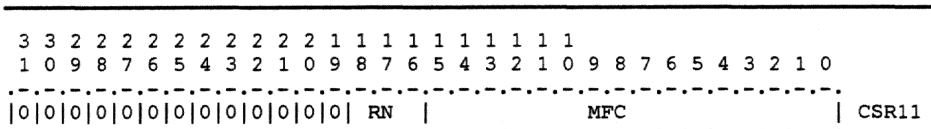


Table 5–9 CSR11 bits

Bit	Name	Access	Description
15:00	MFC	R	Missed Frame Count - Counter for the number of frames that were discarded and lost because host receive buffers were unavailable. The counter pins at all "1" and is cleared when read by the host.
18:16	RN	R	Chip Revision Number - This stores the revision number for this particular SGEC.
			Pass1 info: RN is set to 1.

5.2.13 Diagnostic Registers (CSR12, 13, 14, 15)

These registers are described in Chapter 7, Diagnostics and Testing.

5.3 Descriptors and buffers format

The SGEC transfers frame data to and from receive and transmit buffers in host memory. These buffers are pointed to by descriptors which are also resident in host memory.

There are two descriptor lists: one for receive and one for transmit. The starting address of each list is written into CSRs 3 and 4 respectively. A descriptor list is a forward-linked (either implicitly or explicitly) list of descriptors, the last of which may point back to the first entry, thus creating a ring structure. Explicit chaining of descriptors, through setting xDES1<CA> is called *Descriptor Chaining*. The descriptor lists reside in VAX *physical* memory address space.

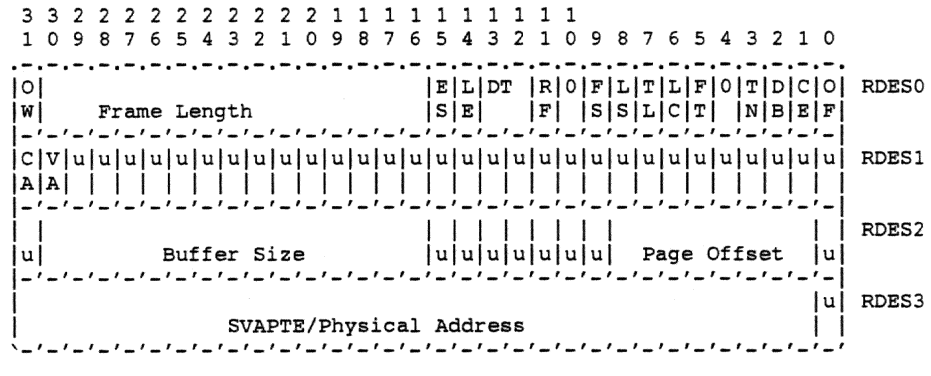
Note: **The SGEC first reads the descriptors, ignoring all unused bits regardless of their state. The only word the SGEC writes back, is the first word (xDES0) of each descriptor. Unused bits in xDES0 will be written as "0". Unused bits in xDES1 - xDES3 may be used by the port driver and the SGEC will never disturb them.**

A data buffer can contain an entire frame or part of a frame, but it cannot contain more than a single frame. Buffers contain only data; buffer status is contained in the descriptor. The term *Data Chaining* is used to refer to frames spanning multiple data buffers. Data Chaining can be enabled or disabled, in reception, through CSR6<DC>. Data buffers reside in VAX memory space, either physical or virtual.

5.3.1 Receive descriptors

The receive descriptor format is shown in Figure 5–9, and described in the following paragraphs.

Figure 5–9 Receive descriptor format



5.3.1.1 RDES0 word

RDES0 word contains received frame status, length and descriptor ownership information.

Note: With the exception of RDES0<OW> and RDES0<FS>, all RDES0 bits are valid only if the current descriptor buffer contains the last segment of a received frame - RDES0<LS> set.

Table 5–10 RDES0 bits

Bit	Name	Description
00	OF	Overflow - When set, indicates received data in this descriptor's buffer was corrupted due to internal FIFO overflow. This will generally occur if SGEC DMA requests are not granted before the internal receive FIFO fills up.
01	CE	CRC Error - When set, indicates that a CRC error has occurred on the received frame. All incoming frames are CRC checked, regardless of the strip CRC or padding functions.
02	DB	Dribbling Bits - When set, indicates the frame contained a non-integer multiple of eight bits. This error will be reported only if the number of dribbling bits in the last byte is greater than two. The CRC check is performed independent of this error, however, only whole bytes are run through the CRC logic. **Consequently, received frames with up to seven dribbling bits will have this bit set, but if CE (or other error indicators) are not set, they should be considered valid.**
03	TN	Translation Not Valid - When set, indicates that a translation error occurred when the SGEC was translating a VAX virtual buffer address. It will only set if RDES1<VA> was set. The Reception process remains in the RUNNING state and attempts to acquire the next descriptor.
05	FT	Frame Type - When set, indicates the frame is an Ethernet type frame. When clear, indicates the frame is an IEEE 802.3 type frame.

Table 5–10 (Cont.) RDES0 bits

Bit	Name	Description
06	LC	Late Collision - When set, indicates the frame was damaged by a collision that occurred after the collision window has passed.
07	TL	Frame Too Long - When set, indicates the frame length exceeds the maximum Ethernet specified size of 1518 bytes.
08	LS	Last Segment - When set, indicates this buffer contains the last segment of a frame and status information is valid. **Note: The last buffer of a frame may be devoid of any data.**
09	FS	First Segment - When set, indicates this buffer contains the first segment of a frame.
11	RF	Runt Frame - When set, indicates this frame was damaged by a collision or premature termination before the collision window had passed. Runt frames will only be passed on to the host if (CSR6<PB>) is set.
13:12	DT	Data Type - Indicates the type of data the buffer contains, according to the following table: **Value** — **Meaning** 00 — Normal received frame 01 — Internally looped back frame 10 — Externally looped back frame
14	LE	Length Error - When set, indicates one of the following: • The frame segment does not fit within the current buffer and the SGEC does not own the next descriptor. The frame is truncated. • The Receive Watchdog timer expired. CSR5<RW> is also set.
15	ES	Error Summary - The logical "OR" of RDES0 bits OF,CE,TN,LC,TL,LE,RF.
30:16	FL	Frame Length - The length in bytes of the received frame.
31	OW	Own bit - When set, indicates the descriptor is owned by the SGEC. When cleared, indicates the descriptor is owned by the host. The SGEC clears this bit upon completing processing of the descriptor and its associated buffer.

5.3.1.2 RDES1 word

Table 5–11 RDES1 bits

Bit	Name	Descriptor
30	VA	Virtual Addressing - When set, RDES3 is interpreted as a SVAPTE (System Virtual Address of Page Table Entry). The SGEC uses RDES3 and RDES2<Page Offset> to perform a VAX virtual address translation process to obtain the physical address of the buffer. When clear, RDES3 is interpreted as the actual physical address of the buffer.
31	CA	Chain Address - When set, RDES3 is interpreted as another descriptor's VAX physical address. This allows the SGEC to process multiple, non-contiguous descriptor lists and explicitly "chain" the lists. Note that contiguous descriptors are implicitly chained.

5.3.1.3 RDES2 word

Table 5–12 RDES2 bits

Bit	Name	Descriptor
08:00	PO	Page Offset - The byte offset of the buffer within the page. Only meaningful if RDES1<VA> is set.
		Note: Receive buffers must be word aligned.
30:16	BS	Buffer Size - The size, in bytes, of the data buffer.
		Pass1 restriction: When Data Chaining is enabled (CSR6<DC> clear), buffer size must be 256 bytes or greater. While permitted, smaller buffers may cause overflow errors.

5.3.1.4 RDES3 word

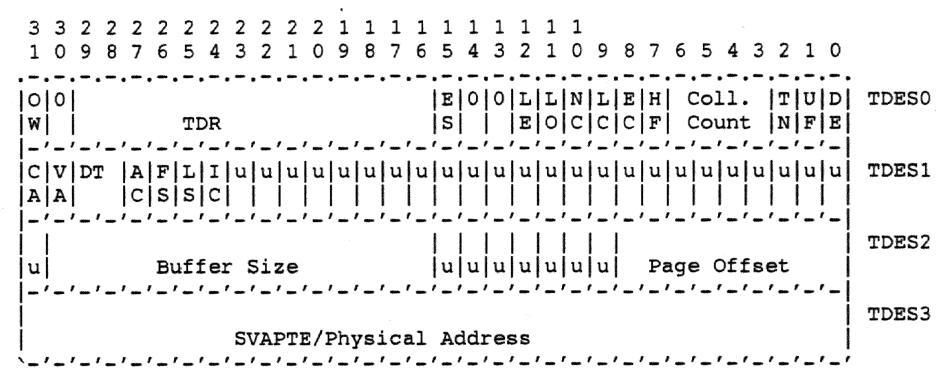
Table 5–13 RDES3 bits

Bit	Name	Descriptor
31:00	SV/PA	SVAPTE/Physical Address - When RDES1<VA> is set, RDES3 is interpreted as the System Virtual Address of Page Table Entry and used in the virtual address translation process. When RDES1<VA> is clear, RDES3 is interpreted as the physical address of the buffer. When RDES1<CA> is set, RDES3 is interpreted as the VAX physical address of another descriptor.
		Note: Receive buffers must be word aligned.

5.3.2 Transmit descriptors

The transmit descriptor format is shown in Figure 5–10, and described in the following paragraphs.

Figure 5–10 Transmit descriptor format



0 - SGEC writes as "0"
u - Ignored by the SGEC on read, never written

5.3.2.1 TDES0 word

TDES0 word contains transmitted frame status and descriptor ownership information.

Table 5–14 TDES0 bits

Bit	Name	Description
00	DE	Deferred - When set, indicates that the SGEC had to defer while trying to transmit a frame. This condition occurs if the channel is busy when the SGEC is ready to transmit.
01	UF	Underflow Error - When set, indicates that the transmitter has truncated a message due to data late from memory. UF indicates that the SGEC encountered an empty transmit FIFO while in the midst of transmitting a frame. The Transmission process enters the SUSPENDED state and sets CSR5<TI>.
02	TN	Translation Not Valid - When set, indicates that a translation error occurred when the SGEC was translating a VAX virtual buffer address. It may only set if TDES1<VA> was set. The Transmission process enters the SUSPENDED state and sets CSR5<TI>.
06:03	CC	Collision Count - A four bit counter indicating the number of collisions that occurred before the transmission attempt succeeded or failed. A count of zero indicates that there were no collisions or that the frame was aborted after 16 collisions (the cases can be distinguished by examining TDES0<EC>.)
07	HF	Heartbeat Fail - When set, indicates Heartbeat Collision Check failure (the transceiver failed to return a collision pulse as a check after the transmission. Some transceivers do not generate heartbeat, and so will always have this bit set. If the transceiver does support it, it indicates transceiver failure.)
08	EC	Excessive Collisions - When set, indicates that the transmission was aborted because 16 successive collisions occurred while attempting to transmit the current frame.
09	LC	Late Collision - When set, indicates frame transmission was aborted due to a late collision.

Table 5–14 (Cont.) TDES0 bits

Bit	Name	Description
10	NC	No Carrier - When set, indicates the carrier signal from the transceiver was not present during transmission (possible problem in the transceiver or transceiver cable). Meaningless in internal loopback mode (CSR5<OM> = 1).
11	LO	Loss of Carrier - When set, indicates loss of carrier during transmission (possible short circuit in the Ethernet cable). Meaningless in internal loopback mode (CSR5<OM> = 1).
12	LE	Length Error - When set, indicates one of the following: • The SGEC encountered a descriptor it did not own, or a chain descriptor (TDES1<CA> = 1), in the middle of data chained descriptors (a frame spanning multiple buffers). • Zero length buffer in the middle of data chained descriptors. • Wrong data type (TDES1<DT> not equal 0) in the middle of data chained descriptors. • Incorrect pairing of TDES1<FS> and TDES1<LS>. The Transmission process enters the SUSPENDED state and sets CSR5<TI>.
15	ES	Error Summary - The logical "OR" of UF, TN, EC, LC, NC, LO and LE.
29:16	TDR	Time Domain Reflectometer - This is a count of bit times (1 bit time = 100 ns on 10BASE5 networks), and is useful for locating a fault on the cable using the velocity of propagation (about 5 ns / meter) on the cable. Only valid if TDES0<EC> is also set. Two such aborts (Excessive Collisions) in a row and with the same or similar (within 20) TDR values indicate a possible cable short (when also TDES0<LO> is set) or open (TDES0<LO> clear).
31	OW	Own bit - When set, indicates the descriptor is owned by the SGEC. When cleared, indicates the descriptor is owned by the host. The SGEC clears this bit upon completing processing of the descriptor and its associated buffer.

5.3.2.2 TDES1 word

Table 5–15 TDES1 bits

Bit	Name	Descriptor
24	IC	Interrupt on Completion - When set, the SGEC will set CSR5<TI> after this frame has been transmitted. To take effect, this bit must be set in the descriptor where LS is set.
25	LS	Last Segment - When set, indicates the buffer contains the last segment of a frame.
26	FS	First Segment - When set, indicates the buffer contains the first segment of a frame.

Table 5–15 (Cont.) TDES1 bits

Bit	Name	Descriptor
27	AC	Add CRC disable - When set, the SGEC will not append the CRC to the end of the transmitted frame. To take effect, this bit must be set in the descriptor where FS is set.
29:28	DT	Data Type - Indicates the type of data the buffer contains, according to the following table:

Value	Meaning
00	Normal transmit frame data
10	Setup frame - Explained in Section 5.3.3.
11	Diagnostic frame - Explained in Chapter 7.

30	VA	Virtual Addressing - When set, TDES3 is interpreted as a SVAPTE (System Virtual Address of Page Table Entry). The SGEC uses TDES3 and TDES2<Page Offset> to perform a VAX virtual address translation process to obtain the physical address of the buffer. When clear, TDES3 is interpreted as the actual physical address of the buffer.
31	CA	Chain Address - When set, TDES3 is interpreted as another descriptor's VAX physical address. This allows the SGEC to process multiple, non-contiguous descriptor lists and explicitly "chain" the lists. Note that contiguous descriptors are implicitly chained.

5.3.2.3 TDES2 word

Table 5–16 TDES2 bits

Bit	Name	Descriptor
08:00	PO	Page Offset - The byte offset of the buffer within the page. Only meaningful if TDES1<VA> is set.

Note: Transmit buffers may start on arbitrary byte boundaries.

Table 5–16 (Cont.) TDES2 bits

Bit	Name	Descriptor
30:16	BS	Buffer Size - The size, in bytes, of the data buffer. If this field is 0, the SGEC will skip over this buffer and ignore it. The frame size is the sum of all BS fields of the frame segments (between and including the descriptors having TDES1<FS> and TDES1<LS> set).

Pass1 restriction: Buffer sizes must be set according to the following table:

Position (within data chained descriptors)	TDES1<FS> state	TDES1<LS> state	Range of buffer sizes (bytes)
First	1	0	1 to 64
Intermediary	0	0	256 at least
Last	0	1	1 at least
First and only	1	1	Any

Deviation from these rules, while permitted, may result in underflow errors.

Note: If the port driver wishes to suppress transmission of a frame, this field must be set to 0 in all descriptors comprising the frame and prior to the SGEC acquiring them. If this rule is not adhered to, corrupted frames might be transmitted.

5.3.2.4 TDES3 word

Table 5–17 TDES3 bits

Bit	Name	Descriptor
31:01	SV/PA	SVAPTE/Physical Address - When TDES1<VA> is set, TDES3 is interpreted as the System Virtual Address of Page Table Entry and used in the virtual address translation process. When TDES1<VA> is clear, TDES3 is interpreted as the physical address of the buffer. When TDES1<CA> is set, TDES3 is interpreted as the VAX physical address of another descriptor.

Note: Transmit buffers may start on arbitrary byte boundaries.

5.3.3 Setup frame

A setup frame defines SGEC Ethernet destination addresses. These addresses will be used to filter all incoming frames. The setup frame is *never* transmitted over the Ethernet, nor looped back to the receive list. While the setup frame is being processed, the receiver logic will temporarily disengage from the Ethernet wire - around 50μseconds. The setup frame size is *always* 128 bytes and must be wholly contained in a single transmit buffer. There are two types of setup frames:

1 Perfect Filtering addresses (14) list

2 Imperfect Filtering hash bucket (512) heads + one physical address

5.3.3.1 First setup frame

A setup frame must be *queued* (**placed in the transmit list with SGEC ownership**) to the SGEC before the Reception process is started, except for when the SGEC operates in promiscuous reception mode.

5.3.3.2 Subsequent setup frame

Subsequent setup frames may be queued to the SGEC while the Reception process is in the RUNNING, SUSPENDED or STOPPED (except when changing filtering mode, see Section 5.3.3.3) state, nor does it affect the state of the Reception process. The only requirement for the setup frame to be processed, is that the Transmission process be in the RUNNING state. The setup frame will be processed after all preceding frames have been transmitted and after the current frame reception, if any, is completed.

5.3.3.3 Changing filtering mode

When switching filtering mode from prefect to imperfect (or vice versa), the following steps must be taken:

1. A Stop Reception (CSR6<SR>) command must be issued (unless the Reception process is already in the STOPPED state).
2. The driver must *verify* the Reception process is STOPPED by repeatedly examining CSR5<RS>.
3. Toggle CSR6<HP>.
4. Queue a setup frame and wait for indication that it has been processed.
5. Start the Reception process with a Start Reception (CSR6<SR> command.

5.3.3.4 Setup frame descriptor

The setup frame descriptor format is shown in Figure 5–11, and described in the following paragraphs.

Figure 5–11 Setup frame descriptor format

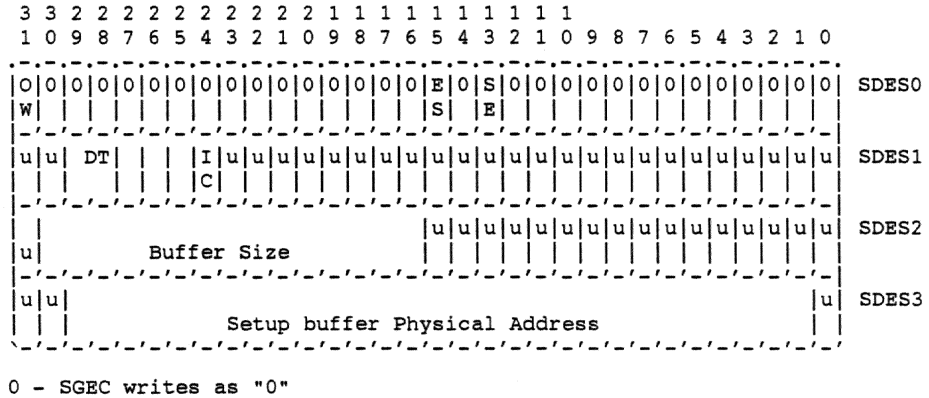


Table 5–18 Setup frame descriptor bits

Word	Bit	Name	Description
SDES0	13	SE	Setup Error - When set, indicates the setup frame buffer size in not 128 bytes.
	15	ES	Error Summary - Set when SE is set.
	31	OW	Own bit - When set, indicates the descriptor is owned by the SGEC. When cleared, indicates the descriptor is owned by the host. The SGEC clears this bit upon completing processing of the descriptor and its associated buffer.
SDES1	24	IC	Interrupt on Completion - When set, the SGEC will set CSR5<TI> after this setup frame has been processed.
	29:28	DT	Data Type - Must be 2 to indicate setup frame.
SDES2	30:16	BS	Buffer Size - Must be 128.
SDES3	29:1	PA	Physical Address - Physical address of setup buffer.
			Note: Setup buffer must be word aligned.

5.3.3.5 Perfect Filtering setup frame buffer

This section describes how the SGEC interprets a setup frame buffer when CSR6<HP> is clear.

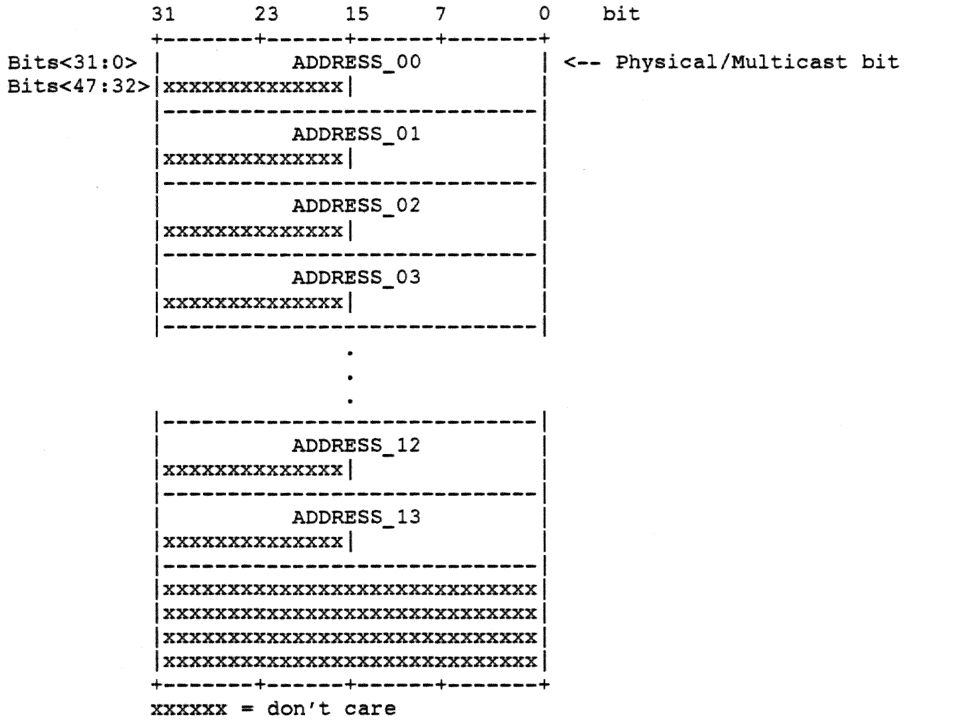
The SGEC can store 14 - full 48 bits Ethernet - destination addresses. It will compare the addresses of any incoming frame to these, and reject those which do not match.

The setup frame *must always* supply all 14 addresses. Any mix of physical and multicast addresses can be used. Unused addresses should be duplicates of one of the valid addresses. The addresses are formatted as shown in the figure below.

Figure 5–12 Perfect Filtering setup frame buffer format

Figure 5–12 Cont'd. on next page

Figure 5–12 (Cont.) Perfect Filtering setup frame buffer format



The low-order bit of the low-order bytes is the address's multicast bit.

Example 5–1 illustrates a Perfect Filtering Setup buffer (fragment).

Example 5–1 Perfect filtering buffer

```
Ethernet addresses to be filtered:
1   A8-09-65-12-34-76
    09-BC-87-DE-03-15
     .
     .
     .

Setup frame buffer fragment:
2   126509A8
    00007634
    DE87BC09
    00001503
     .
     .
     .
```

1 Two Ethernet addresses written according to the DEC STD 134 specification for address display.

2 Those two addresses as they would appear in the buffer.

5.3.3.6 Imperfect Filtering setup frame buffer

This section describes how the SGEC interprets a setup frame buffer when CSR6<HP> is set.

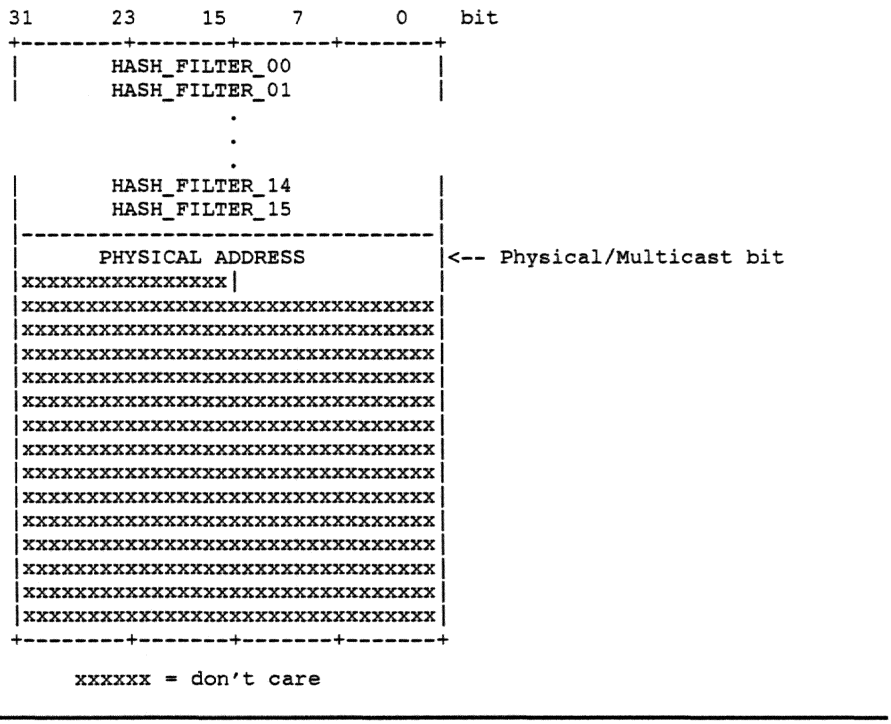
The SGEC can store 512 bits, serving as hash bucket heads, and one *physical* 48 bit Ethernet address. Incoming frames with multicast destination addresses will be subjected to the imperfect filtering. Frames with physical destination addresses will be checked against the single physical address.

For any incoming frame with a **multicast** destination address, the SGEC applies the standard Ethernet CRC function (see (6-1) to the first six bytes containing the destination address, then uses the least significant nine bits of the result, as a bit index into the table. If the indexed bit is set, the frame is accepted. If it is cleared, the frame is rejected.

This filtering mode is called imperfect, because multicast frames not addressed to this station may slip through, but it will still cut down on the number of frames the host will be presented with.

The format for the hash table and the physical address is shown below:

Figure 5–13 Imperfect Filtering setup frame format



Bits are sequentially numbered from right to left and down the table. For example, if CRC(destination address)<8:0> = 33, the SGEC will examine bit #1 in the second longword.

Example 5-2 illustrates an Imperfect Filtering Setup frame buffer and Example 5-3 shows a C program to compute the hash bucket heads and create the resultant Setup frame buffer.

Example 5–2 Imperfect filtering buffer

```
Ethernet addresses to be filtered:
❶   25-00-25-00-27-00
    A3-C5-62-3F-25-87
    D9-C2-C0-99-0B-82
    7D-48-4D-FD-CC-0A
    E7-C1-96-36-89-DD
    61-CC-28-55-D3-C7
    6B-46-0A-55-2D-7E

❷   A8-12-34-35-76-08

Setup frame buffer:
❸   00000000
    10000000
    00000000
    00000000
    00000000
    40000000
    00000080
    00100000
    00000000
    10000000
    00000000
    00000000
    00000000
    00010000
    00000000
    00400000
❹   353412A8
    00000876
```

❶ Ethernet multicast addresses written according to the DEC STD 134 specification for address display.

❷ An Ethernet physical address.

❸ The first part of an Imperfect filter Setup frame buffer with set bits for the ❶ multicast addresses.

❹ The second part of the buffer with the ❷ physical address.

Example 5–3 Imperfect filtering Setup frame buffer creation C program

```
#include <stdio>

unsigned int imperfect_setup_frame[128/4],   /* The setup buffer - 128   */
      /* bytes      */
  address[2],
  crc[33];   /* CRC residue vector     */

main()
{
    int i, hash;
/*              */
/* This program accepts 48 bits Ethernet addresses and builds a Setup frame
/* buffer for imperfect filtering.         */
/*              */
/* Addresses must be entered in hexadecimal. The multicast bit is the least
/* significant bit of the least significant digit of the first 32 bits.
/* Non-multicast addresses are ignored.          */
/*               */
/* Input is terminated by keying CTRL/Z after which the program prints out
/* the buffer.            */
/*              */
main_loop:

/* Prompt user for the Ethernet address          */
    printf("\n\n Enter the first 32 bits (HEX) - ");
    if (scanf("%x", &address[0]) == EOF)
 {

     printf("\n\n Imperfect Setup buffer printout\n");
     for (i=0;  i < 128/4;  i++)
  printf("%08X\n", imperfect_setup_frame[i]);
     exit(1);
 }
    printf("\n Enter the remaining 16 bits (HEX) - ");
    scanf("%x",&address[1]);

/* Ignore non multicast addresses         */
     if ((address[0] & 1) == 0)
  goto main_loop;

/* Compute the hash function          */
    hash = address_crc(address[0],address[1]);

/* Set the appropriate bit in the Setup buffer        */
    imperfect_setup_frame[hash/32] =
 imperfect_setup_frame[hash/32] | 1 << hash%32;

    goto main_loop;
}

int address_crc( unsigned int lsb32 , unsigned int msb16)
{
    int j,hash = 0;

/* Set CRC to all 1's           */

    for (j=0;  j < 33;  j++)
 crc[j] = 1;

/* Compute the address CRC by running the CRC 48 steps       */

    for (j=0;  j < 32;  j++)
 nextstate(lsb32 & 1<<j ? 1 : 0);
    for (j=0;  j < 16;  j++)
 nextstate(msb16 & 1<<j ? 1 : 0);

/* Extract 9 least significant bits from the CRC residue      */
```

Example 5–3 Cont'd. on next page

Example 5–3 (Cont.) Imperfect filtering Setup frame buffer creation C program

```
    for (j=24;  j < 33;  j++)
 hash = hash<<1 | crc[j];

    return hash;
}

nextstate(dat)
int dat;
{
  int i,mean;
  mean = crc[32] ^ dat;
  for(i=32;i>=2;i--) crc[i]=crc[i-1];
  crc[27] = crc[27] ^ mean;
  crc[24] = crc[24] ^ mean;
  crc[23] = crc[23] ^ mean;
  crc[17] = crc[17] ^ mean;
  crc[13] = crc[13] ^ mean;
  crc[12] = crc[12] ^ mean;
  crc[11] = crc[11] ^ mean;
  crc[9] = crc[9] ^ mean;
  crc[8] = crc[8] ^ mean;
  crc[6] = crc[6] ^ mean;
  crc[5] = crc[5] ^ mean;
  crc[3] = crc[3] ^ mean;
  crc[2] = crc[2] ^ mean;
  crc[1] = mean;
}
```

5.4 SGEC operation

5.4.1 Hardware and Software Reset

The SGEC responds to two types of reset commands: a hardware reset through the RESET_L pin, and a software reset command triggered by setting CSR6<RE>. In **both cases**, the SGEC **aborts** all ongoing processing and starts the Reset sequence. The SGEC restarts and reinitializes all internal states and registers. *No internal states are retained, no descriptors are owned and all the host visible registers are set to "0", except where otherwise noted.*

Note: **The SGEC does not explicitly disown any owned descriptors; so descriptors Own bits might be left in a state indicating SGEC ownership.**

The following table indicates the CSR fields which are not set to "0" after reset:

Field	Value
CSR3	Unpredictable
CSR4	Unpredictable
CSR5<DN>	1
CSR6<BL>	1
CSR7	Unpredictable
CSR9	RT = TT = 12500

After the reset sequence completes, the SGEC executes the self test procedure to do basic sanity checking. After the self test completes, the SGEC sets the Initialization Done flag CSR5<ID>. The self test completion status bits CSR5<SF> and CSR5<SS> indicate whether the self test failed and the failure reason.

Pass1 info: Self test takes 30 milliseconds to complete.

If the self test completes successfully, the SGEC is ready to accept further host commands. Both the Reception and Transmission processes are placed in the STOPPED state.

Successive reset commands (either hardware or software) may be issued. The only restriction is that SGEC CSRs should not be accessed during a 1μsecond period following the reset. Access during this period will result in a CP-BUS timeout error. Access to SGEC CSRs during the self test are permitted; however, only CSR5 reads should be performed.

5.4.2 Interrupts

Interrupts are generated as a result of various events. CSR5 contains all the status bits which may cause an interrupt, provided CSR6<IE> is set. The port driver must clear the interrupt bits (by writing a "1" to the bit position), to enable further interrupts from the same source.

Interrupts are *not queued*, and if the interrupting event reoccurs *before* the port driver has responded to it, no additional interrupts will be generated. For example, CSR5<RI> indicates *one or more* frames were delivered to host memory. The port driver should scan *all* descriptors, from its last recorded position up to the first SGEC owned one.

An interrupt will only be generated *once* for simultaneous, multiple interrupting events. It is the port driver responsibility to scan CSR5 for the interrupt cause(s). The interrupt will not be *regenerated*, unless a *new* interrupting event occurs *after* the host acknowledged the previous one, and provided the port driver *cleared* the appropriate CSR5 bit(s). For example, CSR5<TI> and CSR5<RI> may both set, the host acknowledges the interrupt and the port driver begins executing by reading CSR5. Now CSR5<RU> sets. The port driver writes back its copy of CSR5, clearing CSR5<TI> and CSR5<RI>. After the host IPL is lowered below the SGEC level, another interrupt will be delivered with the CSR5<RU> bit set.

Should the port driver clear *all* CSR5 set interrupt bits before the interrupt has been acknowledged, the interrupt will be suppressed.

5.4.3 Startup procedure

A sequence of checks and commands must be performed by the port driver to prepare the SGEC for operation.

1. Wait for the SGEC to complete its Initialization sequence by polling on CSR5<ID> and CSR5<SF> (refer to Section 5.2.6 for details).
2. Examine CSR5<SF> to find out whether the SGEC passed its self test. If it did not, it should be replaced (refer to Section 5.2.6 for details).
3. Write CSR0 to establish system configuration dependent parameters (refer to Section 5.2.2 for details).
4. If the port driver intends to use VAX virtual addresses, CSR7 must be written to identify the System Page Table to the SGEC (refer to Section 5.2.8 for details).
5. If the port driver wishes to change the default settings of the watchdog timers, it must write to CSR9 (refer to Section 5.2.10 for details).
6. Port driver must create the transmit and receive descriptors lists, then write to CSR3 and CSR4 to provide the SGEC with the starting address of each list. The first descriptor on the transmit list will usually contain a setup frame (refer to Section 5.2.5 for details).
7. Write CSR6 to set global operating parameters and start the Transmission and Reception processes. The Reception and Transmission processes enter the RUNNING state and attempt to acquire descriptors from the respective descriptors lists and begin processing incoming and outgoing frames (refer to Section 5.2.7 for details). The Reception and Transmission processes are independent of each other and can be started and stopped separately.

Caution: If address filtering (either perfect or imperfect) is desired, the Reception process should only be started after the Setup frame has been processed.

8. The port driver now waits for any SGEC interrupts. If either the Reception or Transmission processes were SUSPENDED, the port driver must issue the Poll Demand command after it has rectified the suspension cause.

5.4.4 Reception process

While in the RUNNING state, the Reception process polls the receive descriptor list, attempting to acquire free descriptors. Incoming frames are processed and placed in acquired descriptors' data buffers, while status information is written to the descriptor RDES0 words. The SGEC always tries to acquire an extra descriptor in anticipation of incoming frames. Descriptor acquisition is attempted under the following conditions:

- Immediately after being placed in the RUNNING state through setting of CSR6<SR>.
- In response to a Poll Demand command if the SGEC was in the SUSPENDED state.
- The SGEC begins writing frame data to a data buffer pointed to by the current descriptor.

- The last acquired descriptor chained (RDES1<CA> set) to another descriptor.
- A virtual translation error was encountered RDES0<TN> while the SGEC was doing the address translation.

As incoming frames arrive, the SGEC strips the preamble bits and stores the frame data in the receive FIFO. Concurrently, it performs address filtering according to CSR6 fields AF, HP and its internal filtering table. If the frame fails the address filtering, it is ignored and purged from the FIFO. Frames which are shorter than 64 bytes, due to collision or premature termination are also ignored and purged from the FIFO, unless CSR6<PB> is set.

After 64 bytes have been received, the SGEC begins transferring the frame data to the buffer pointed to by the current descriptor. If Data Chaining is enabled (CSR6<DC> clear), the SGEC will write frame data overflowing the current data buffer into successive buffer(s). The SGEC sets the RDES0<FS> and RDES0<LS> in the first and last descriptors, respectively, to delimit the frame. Descriptors are released (RDES0<OW> bit cleared) as their data buffers fill up or the last segment of a frame has been transferred to a buffer.

The SGEC sets RDES0<LS> and the RDES0 status bits in the last descriptor it releases for a frame. After the last descriptor of a frame is released, the SGEC sets CSR5<RI>.

This process is repeated until the SGEC encounters a descriptor flagged as owned by the host. After filling up all previously acquired buffers, the Reception sets CSR5<RU> and enters the SUSPENDED state. The position in the receive list is retained. Any incoming frames while in this state will cause the SGEC to increment the Missed Frames Counter (CSR11<MFC>). To reinitiate processing the port driver must issue the Poll Demand command.

Note: **The SGEC *does not* automatically poll the descriptors lists and the port driver *must* explicitly issue a Poll Demand command after rectifying the suspension cause.**

The following table summarizes the Reception process state transitions and resulting actions:

Table 5–19 Reception process state transitions

From state	Event	To state	Action
STOPPED	Start Reception command	RUNNING	Receive polling begins from last list position or from the the list head if this is the first Start command issued, or if the receive descriptor list address (CSR3) was modified by the port driver.
RUNNING	SGEC attempts acquisition of a descriptor owned by the host	SUSPENDED	CSR5<RU> is set when the last acquired descriptor buffer is consumed. Position in list retained.

Table 5–19 (Cont.) Reception process state transitions

From state	Event	To state	Action
RUNNING	Stop Reception command	STOPPED	Reception process is STOPPED after the current frame, if any, is completely transferred to data buffer(s). Position in list retained.
RUNNING	Memory or host bus parity error encountered	STOPPED	Reception is cut off and CSR5<ME> is set.
RUNNING	Reset command	STOPPED	Reception is cut off.
SUSPENDED	Poll Demand command	RUNNING	Receive polling resumes from last list position or from the list head if CSR3 was modified by the port driver.
SUSPENDED	Stop Reception command	STOPPED	None.
SUSPENDED	Reset command	STOPPED	None.

5.4.5 Transmission process

While in the RUNNING state, the Transmission process polls the transmit descriptor list for any frames to transmit. Frames are built and transmitted on the Ethernet wire. Upon completing frame transmission (or giving up), status information is written to the TDES0 words. Once polling starts, it continues (in sequential or descriptor chained order) until the SGEC encounters a descriptor flagged as owned by the host, or an error condition. At this point, the Transmission process is placed in the SUSPENDED state and CSR5<TI> is set.

CSR5<TI> will also be set after completing transmission of a frame which has TDES1<IC> set in its last descriptor. In this case, the Transmission process remains in the RUNNING state.

Frames may be data chained and span several buffers. Frames must be delimited by TDES1<FS> and TDES1<LS> in the first and last descriptors, respectively, containing the frame. While in the RUNNING state, as the Transmission process starts, it first expects a descriptor with TDES1<FS> set. Frame data transfer from the host buffer to the internal FIFO is initiated. Concurrently, if the current frame had TDES1<LS> clear, the Transmission process attempts to acquire the next descriptor, expecting TDES1<FS> and TDES1<LS> to be clear indicating an intermediary buffer, or TDES1<LS> to be set, indicating the end of the frame. After the last buffer of the frame has been transmitted, the SGEC writes back final status information to the TDES0 word of the descriptor having TDES1<LS> set, optionally sets CSR5<TI> if TDES1<IC> was set, and repeats the process with the next descriptor(s). Actual frame transmission begins *after at least 72 bytes* have been transferred to the internal FIFO, or *a full frame is contained* in the FIFO. Descriptors are released (TDES0<OW> bit cleared) as soon as the SGEC is through processing a descriptor.

Transmit polling suspends under the following conditions:

- the SGEC reaches a descriptor with TDES0<OW> clear. To resume, the port driver must give descriptor ownership to the SGEC and issue a Poll Demand command.

- The TDES1<FS> and TDES1<LS> are incorrectly paired or out of order. TDES0<LE> will be set.
- A frame transmission is given up due to a locally induced error. The appropriate TDES0 bit is set.

The Transmission process enters the SUSPENDED state and sets CSR5<TI>. Status information is written to the TDES0 word of the descriptor causing the suspension. The position in the transmit list, in all of the above cases, is retained. The retained position is that of the *descriptor following the last descriptor closed (set to host ownership) by the SGEC.*

Note: The SGEC *does not* automatically poll the descriptors lists and the port driver *must* explicitly issue a Poll Demand command after rectifying the suspension cause.

The following table summarizes the Transmission process state transitions:

Table 5–20 Transmission process state transitions

From state	Event	To state	Action
STOPPED	Start Transmission command	RUNNING	Transmit polling begins from the last list position or from the head of the list if this is the first Start command issued, or if the transmit descriptor list address (CSR4) was modified by the port driver.
RUNNING	SGEC attempts acquisition of a descriptor owned by the host	SUSPENDED	CSR5<TI> is set. Position in list retained.
RUNNING	Out of order delimiting flag (TDES0<FS> or TDES0<LS>) encountered.	SUSPENDED	TDES0<LE> and CSR5<TI> are set. Position in list retained.
RUNNING	Frame transmission aborts due to a locally induced error (refer to Table 5–14 for details).	SUSPENDED	Appropriate TDES0 and CSR5<TI> bits are set. Position in list retained.
RUNNING	Stop Transmission command	STOPPED	Transmission process is STOPPED after the current frame, if any, is transmitted. Position in list retained.
RUNNING	Transmit watchdog expires	STOPPED	Transmission is cut off and CSR5<TW> is set. Position in list retained.
RUNNING	Memory or host bus parity error encountered	STOPPED	Transmission is cut off and CSR5<ME> is set.
RUNNING	Reset command	STOPPED	Transmission is cut off.
SUSPENDED	Poll Demand command	RUNNING	Transmit polling resumes from last list position or from the list head if CSR4 was modified by the port driver.
SUSPENDED	Stop Transmission command	STOPPED	None.
SUSPENDED	Reset command	STOPPED	None.

5.4.6 Loopback operations

The SGEC supports two loopback modes:

- Internal loopback

  This mode is generally used to verify correct operations of the SGEC internal logic. While in this mode, the SGEC will take frames from the transmit list and loop them back, internally, to the receive list. The SGEC is disengaged from the Ethernet wire while in this mode.

- External loopback

  This mode is generally used to verify correct operations up to the Ethernet cable. While in this mode, the SGEC will take frames from the transmit list and transmit them on the Ethernet wire. Concurrently, the SGEC listens to its own transmissions and places incoming frames in the receive list.

Note: Caution should be exercised in this mode as transmitted frames are placed on the Ethernet wire. Furthermore, the SGEC does not check the origin of any incoming frames, consequently , frames not necessarily originating from the SGEC might make it to the receive buffers.

In either of these modes, all the address filtering and validity checking rules apply. The port driver needs to take the following actions:

1. Place the Reception and Transmission processes in the STOPPED state. The port driver must wait for any previously scheduled frame activity to cease. This is done by polling the TS and RS fields in CSR5.
2. Write to CSR6<OM> according to the desired loopback mode.
3. Prepare appropriate transmit and receive descriptors lists in host memory. These may follow the existing lists at the point of suspension, or may be new lists which will have to be identified to the SGEC by appropriately writing CSR3 and CSR4.
4. Place the Transmission and Reception processes in the RUNNING state through Start commands.
5. Respond and process any SGEC interrupts, as in normal processing.

To restore normal operations, the port driver must execute above step #1, then write the OM field in CSR6 with "00".

Pass1 restriction: Loopback frames are limited to 64 bytes.

5.4.7 DNA CSMA/CD counters and events support

This section describes the SGEC features that support the port driver in implementing and reporting the specified counters and events.

Table 5–21 CSMA/CD counters

Counter	SGEC feature
Seconds since last zeroed	No support.
Octets received	Port driver must add up the RDES0<FL> fields of all successfully received frames.
Octets sent	Port driver must add up the TDES2<BS> fields of all successfully transmitted buffers.
Frames received	Port driver must count the successfully received frames in the receive descriptors list.
Frames sent	Port driver must count the successfully transmitted frames in the transmit descriptors list.
Multicast octets received	Port driver must add up the RDES0<FL> fields of all successfully received frames with multicast address destinations.
Multicast frames received	Port driver must count the successfully received frames with multicast address destinations.
Frames sent, initially deferred	Port driver must count the successfully transmitted frames with TDES0<DE> set.
Frames sent, single collision	Port driver must count the successfully transmitted frames with TDES0<CC> equal to 1.
Frames sent, multiple collisions	Port driver must count the successfully transmitted frames with TDES0<CC> greater than 1.
Send failures	Port driver must count the transmit descriptors having TDES0<ES> set. Other TDES0 bits indicate the specific error with the following exceptions: • Remote Failure to Defer error is flagged as a late collision - TDES0<LC>. • Frame Too Long is not reported by the SGEC.
Collision detect check failed	Port driver must count the transmit descriptors having TDES0<HF> set.
Receive failures	Port driver must count the receive descriptors having RDES0<ES> set. Other RDES0 bits indicate the specific error.
Unrecognized frame destination	No support.
Data overrun	Port driver must count the receive descriptors having RDES0<OF> set.
System buffer unavailable	CSR11<MFC> (refer to Table 5–9).
User buffer unavailable	Not applicable.

CSMA/CD specified events can be reported by the port driver based on the above table. The Initialization Failed event is reported through CSR5<SF>.

6 Serial Interface

6.1 Basic Serial Operation

The SGEC support the full DEC STD 134B frame encapsulation and MAC. It will function in a send and receive half duplex mode system. The SGEC will function in either transmit or receive mode at any instant in time, except for when it is in the loopback modes which operate in full duplex.

Before transmission the SGEC checks that there is no contention for the network bus. In addition to listening for a clear line before transmitting, the SGEC handles collisions in a predetermined way. Should two nodes attempt to transmit at the same time, the signals will collide and the data on the line will be garbled. When transmitting the SGEC listens while transmitting and detect the collision. If present, the SGEC continues to transmit for a predetermined length of time to "Jam" the network, insuring that all nodes have recognized the collision. The SGEC then delay transmission a random amount of time according to the "truncated binary backoff" algorithm implemented in the SGEC, before attempting to transmit again. This minimizes the possibility of collision on retransmission.

Note: **All frequency and timing information in this chapter, are is for 10Mbit/sec serial operation, the bit time equivalent will be given in parenthesis.**

6.1.1 Frame Format

The SGEC transmits or receive information in frames. The SGEC recognizes and transmit DEC STD 134B frames.

6.1.1.1 Ethernet Format Types

Ethernet standards now have three main standard documents, which slightly differ from each other. In this chapter Ethernet will be used as a generic name for the type of network. The specific standard which will be referred is the DEC STD 134B Document. This document is the DEC merge of the three old Ethernet standards. The old Three company Ethernet STD, the DEC STD 134A and the IEEE/802.3 will not be referenced at all.

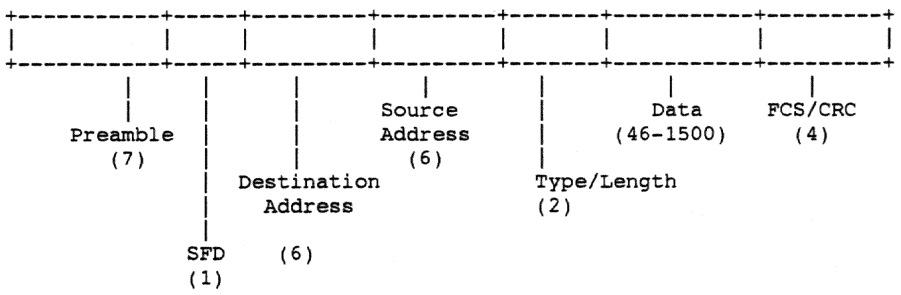
A DEC STD 134B frame consists of a preamble, an SFD, two address fields, a type/length field, a data field, and a frame check sequence (FCS). Each field has a specific format which is described below. A DEC STD 134B frame has a minimum length of 64 bytes and a maximum length of 1518 bytes exclusive of the preamble.

The IEEE/802.3 frame is generally the same as the DEC STD 134B frame. They are different in the type/length field:

1 The IEEE/802.3 has a frame length field with valid data length of 1 to 1500 bytes, the DEC STD 134B recognize values which are greater than 1500 and interpret them as type fields. No type fields smaller than 1500 are allowed in the DEC STD 134B

The DEC STD 134B frame format is shown below:

Figure 6–1 DEC STD 134B Frame Format



Note: The field length in bytes is shown in parentheses.

6.1.1.2 Detailed frame format

Preamble: The preamble is a 7 byte field consisting of 56 alternating "1" and "0" beginning with a "1".

SFD - Start Frame Delimiter: The SFD is a 1 byte field consisting of 6 alternating "1" and "0" beginning with a "1". and terminated by a "11"

This field is identical for the DEC STD 134B and IEEE/802.3 frame format.

Destination Address: The Destination Address is a 6-byte field containing either a specific station address, the broadcast address, or a multicast (logical) address to which this frame is directed.

This field is identical for the DEC STD 134B and IEEE/802.3 frame format.

Source Address: The Source Address is a 6-byte field containing the specific station address from which this frame originated.

This field is identical for the DEC STD 134B and IEEE/802.3 frame format.

Length/Type field: This field consists of two bytes. For DEC STD 134B frames this field is interpreted as length field if smaller than 1500. As a length field this quantity is the number of data bytes in the frame.

If this field is greater than 1500 it is interpreted as a type field. As a type field this field define the type of Protocol of the frame.

For IEEE/802.3 frames this field is the length field defining the data length in bytes with values from 1 to 1500.

Data Field: The Data field consists of 46 to 1500 bytes of information which are fully transparent in the sense that any arbitrary sequence of bytes may occur.

The DEC STD 134B format allows a shorter data field which is specified by the length field. Padding has to be added, upon transmit, to fill the data field up to 46 bytes.

Frame Check Sequence: The Frame Check Sequence (FCS) field is a 32-bit cyclic redundancy check (CRC) value computed as a function of the Destination Address Field, Source Address Field, Type Field, and Data Field. The FCS is appended to each transmitted frame, and used at reception to determine if the received frame is valid.

The CRC polynomial, as specified in the DEC STD 134B specification, is:

$$FCS(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + \quad (6\text{–}1)$$

$$X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X + 1$$

This field is identical for the DEC STD 134B and IEEE/802.3 frame format.

6.1.2 Ethernet Reception Addressing

The SGEC may be setup to recognize any one of the Ethernet receive address groups described below. Each group is separate and distinct from the other groups.

1 Fourteen Address Perfect Filtering

The SGEC provides support for the perfect filtering of up to 14 Ethernet physical or multicast addresses. Any mix of addresses may be used for this perfect filter function of the SGEC. The fourteen addresses are issued in setup frames to the SGEC.

2 One Physical Address, Unlimited Multicast Addresses Imperfect Filtering.

The SGEC provides support for one single physical address to be perfectly filtered with an unlimited number of multicast addresses to be imperfectly filtered. This case supports the needs of applications which wish one single physical address to be filtered as the station address, but also need to enable reception of more than 14 multicast addresses, yet not suffer the overhead of using pass-all-multicast mode. The single Physical address, for perfect filtering, and a 512 bit mask, for imperfect filtering using a hash algorithm are issued in a setup frame to the SGEC. Upon hash hits, the SGEC delivers the received frame.

3 Promiscuous Ethernet Reception

The SGEC provides support for reception of all frames on the network regardless of their destination. This function is controlled by a CSR bit. Use of this group is typically for network monitoring.

4 Group 1 (above) and Reception of All Multicast Ethernet Addresses

This group augments receive address group 1 above with the addition of receiving all frames on the Ethernet with a Multicast Address.

6.1.3 Collision Detection and Implementation

The Ethernet CSMA/CD network access algorithm is completely implemented within the SGEC. In addition to listening for a clear line before transmitting, the SGEC will handle collisions in a predetermined way as defined by the standard. Should two transmitters attempt to seize the line at the same time, they will collide and the data on the line will be garbled. When transmitting the SGEC will listen while it transmits, detect the collision, and then continue to transmit for a predetermined length of time to "jam" the network and ensure that all nodes have recognized the collision. The transmitting SGEC will then delay a random amount of time according to the Ethernet "truncated binary backoff" algorithm in order that the colliding nodes do not try to repeatedly access the network at the same time. Up to 16 attempts to access the network are made by the SGEC before reporting back an error due to excessive collisions.

6.1.4 Clock Generator

The SGEC serial clocking is derived from an external clock source. Use of an external clock enables varying the serial clock frequency independetly of the system clock and thereby vary the serial line speeds. The supported range of line speeds is from 1 Mhz to 10 Mhz.

6.1.5 Watchdog timers

The SGEC contains two separately programmable watchdog timers for receive and transmit. These are 16 bits counters capable of counting for up to 100ms on 10Mbps networks.

6.1.6 Transmit Mode

In the transmit mode, the SGEC initiates a DMA cycle to access data from a transmit buffer. It prefaces the data with a preamble and SFD pattern, and calculates and appends a 32-bit CRC, if enabled.

After a frame is assembled the SGEC waits for the internal Transmite machine to allow transmission on the network, then it serializes the data and output it to the external SIA.

6.1.7 Receive Mode

In the Receive mode the decoded data and clock are fed to the SGEC from an external SIA. The data is deserialized by the receive machine and fed into the internal FIFO. As the data is received the address is checked by the SGEC and a CRC is calculated and then compared to the CRC checksum at the end of the frame. If the calculated CRC does not agree with the Frame CRC, an error bit is set in the receive descriptor. The host processor is notified of all received frames, including those with CRC errors or exccesive dribbling errors. Runt frames are not delivered to the host unless the SGEC is programmed to do so.

6.2 Detailed Transmission Operation

This section will describe the detailed transmission operation as supported by the SGEC. The specific control register definitions, setup frame definitions, and mechanics for host processor software to manipulate the transmit list (i.e. descriptors and buffers) can be found in Chapter 5, Programming.

6.2.1 Transmission Initiation

The host CPU initiates a transmission by storing the entire information content of the frame to be transmitted in one or more buffers in memory. The host processor software prepares a companion transmit descriptor, also in host memory, for the transmit buffer and then signals the SGEC to take it. Once the SGEC has been notified of this transmit list, the SGEC starts to move the data bytes from the host memory to the internal transmit FIFO.

When the Transmit FIFO has adequately filled or when there is a full frame buffered in the transmit FIFO, the SGEC begins to encapsulate the frame. This transmit encapsulation is performed by the Transmit state machine which delays the actual transmission of the data onto the network until the network has been idle for the minimum IPG time (9.6μs).

6.2.2 Frame Encapsulation

The transmit data stream consists of the Preamble, four information fields, and the CRC which is computed in real time by the SGEC chip and automatically appended to the frame at the end of the serial data, if enabled.

The preamble and CRC encapsulation supports DEC STD 134B frame format.

For an outgoing frame the Destination Address, Source Address, Type/Length Field and Data Field are prepared, by the host processor, in the buffer memory prior to initiating transmission by the host CPU. The SGEC chip encapsulates these fields into an Ethernet frame by inserting a preamble before these information fields and appends padding and optionally a CRC after the information fields.

6.2.3 Initial Deferral

The SGEC device constantly monitors the line and is prepared to initiate a transmission any time the host CPU request it. Actual transmission of the data onto the network will only occur if the network has been idle for 9.6μs IPG time and any backoff time requirements have been satisfied.

The IPG time is divided into two parts, IPS1 and IPS2. They are equal respectively to 6.0μs and 3.6μs. In the first part of the IPG, the IPS1 time, the SGEC will monitor the network for idle condition. If carrier will be sensed on the serial line, during this time, the SGEC will deffer and wait until the line will be idle again to restart the IPS1 time count. In the second part of the IPG, the IPS2 time, the SGEC will continue to count the time even though a carrier will be sensed on the network, and will thus force

collision on the network. This is done to assure fairness in the access to the serial line between all the network stations.

6.2.4 Collision

When concurrent transmissions from two or more Ethernet nodes occur (collision), the SGEC chip halts the transmission of the data bytes in the Transmit FIFO and transmits a Jam pattern consisting of AAAAAAAA hex. At the end of the Jam transmission, the SGEC chip begins the Backoff wait period.

Scheduling of retransmission is determined by a controlled randomization process called Truncated Binary Exponential Backoff. The delay is an integer multiple of slot times. The number of slot times to delay before the n*th* retransmission attempt is chosen as a uniformly distributed random integer r in the range:

$0 \leq r < 2^k$

where k = min (n, N) and N = 10

When 16 attempts have been made at transmission and all have been terminated due to collision, the SGEC sets an error status bit and issues an interrupt to the host, if enabled.

NOTE: The jam pattern is a fixed pattern which is not compared with the actual frame CRC. This may cause at a very low probability, a jam pattern which is equal to the CRC.

6.2.5 Watchdog Timer

This watchdog timer will cut out transmission after a programmable delay. This provides a checking mechanism to prevent babbling.

The value used for the time delay for the watchdog timer is programmable, thus providing a mechanism for the host processor to disable or set the timer. The timer starts counting at the beginning of each transmission. If the last bit of the frame is transmitted before the timer expires or there is a collision, the timer is reset and ready for the next transmission. If the timer expires before the transmission ends, transmission is aborted. The watchdog timer can be programmed to count intervals between 1.6μs and 100 milliseconds in increments of 1.6 microseconds. A default value of 20ms is used for Ethernet/IEEE 802.3 networks.

6.2.6 Terminating Transmission

Transmission terminates under the following conditions:

1. Normal: The frame has been transmitted successfully. When the last byte is serialized, the pad and CRC are optionally appended and transmitted, thus concluding frame transmission.
2. Underflow: Transmit data is not ready when needed for transmission. Underflow status bit is set.
3. Excessive Collisions: If a collision occurs for the 15*th* consecutive time, the Excessive Collisions status bit is set.

4 Watchdog timer Expired: If the timer expire while transmission is still ongoing than the programmed interval, transmission will be cut off, and a CSR bit will be set.

5 Memory error: This is a generic error indicating either a host bus timeout or a host memory error. A CSR bit is set.

6 Descriptor error: This is a generic error indicating any problem with the host descriptors list. It may be a translation error, a length error or non proper descriptor control bits.

7 Late collision: If a collision occurs past the collision window, transmission is cut off and a Late Collision bit will be set.

At the completion of every frame transmission, status information about the frame, is written into the Transmit descriptor. In an event of an error concerning the operation of the transmite machine itself, status information will also be written in CSR5.

6.2.7 Transmit parameters values

1 Defer time - IPS1 + IPS2 - 96 Bit Time, 9.6μs for 10Mhz serial rate.

2 IPS1 - 60 Bit Time, 6.0μs for 10Mhz serial rate.

3 IPS2 - 36 Bit Time, 3.6μs for 10Mhz serial rate.

4 Slot time interval - 512 Bit Time, 51.2μs for 10Mhz serial rate.

5 Attempts limit - 16.

6 Backoff limit - 10.

7 Watch dog timer, programmable, units: multiples of 1.28μs, default 16ms, range 1.2μs - 80,000μs.

8 Append CRC on frame transmission, programmable, (yes or no).

6.3 Detailed Receiving Operation

This section will describe the detailed reception operation as supported by the SGEC. The specific control register definitions, setup frame definitions, and mechanics for host processor software to manipulate the receive list (i.e. descriptors and buffers) can be found in a chapter on programming.

6.3.1 Initiating Reception

The SGEC continuously monitors the network when reception is enabled (See CSR definitions). When activity is recognized by a preamble being detected on the Receive data lines, the SGEC synchronizes itself to the incoming data stream during the preamble, waits for the SFD, and then examines the destination address field of the frame. Depending on the address match mode specified, the SGEC will either recognize the frame as being addressed to itself, or abort the frame reception.

6.3.2 Preamble Processing

The preamble as defined by the DEC STD 134B is up to 64 bits (8 bytes) long. The SGEC allow any arbitrary preamble length, it expects at least 6 preamble bits before looking for the "11" end of preamble indicator. If the SGEC chip receives a "00" before receiving the "11" in the preamble, reception is aborted. The frame is not received, and the SGEC waits until the carrier drops and rises again, then begins monitoring the network for a new preamble sequence.

6.3.3 Address Matching

Ethernet addresses consist of two 6-byte fields, one field for the source address and one for the destination address. The first bit of the destination address signifies whether it is a physical address or a multicast/broadcast address.

First Bit	Address
0	Station Address (Physical)
1	Multicast/Broadcast Address (logical)

, the SGEC will filter the frame based on the group of Ethernet Receive Address filtering that has been enabled.

If the frame address passes the filter, then the SGEC will remove the Preamble and deliver the frame to host processor memory.

If, however, the address does not pass the filter, then as soon as the mismatch is recognized the SGEC will terminate reception. In this case, no data is sent to the host memory nor is any receive buffer consumed.

In addition to the four groups of Ethernet Receive Address filtering, an SGEC CSR permits the reception to be explicitly disabled or enabled.

6.3.4 Frame decapsulation

The SGEC checks the CRC bytes of all received frames before releasing the frame to the host processor. CRC (optional) removal is performed for both Ethernet and IEEE 802.3 frames.

Optionally, the SGEC will strip padding off IEEE 802.3 formatted frames.

6.3.5 Terminating Reception

Reception of a specific frame is terminated when any of the following conditions occur:

1. Normal Termination: The carrier sense line goes inactive, this indicates that traffic is no longer present on the Ethernet cable.
2. Overflow: The receive DMA for some reason is not able to empty the Receive FIFO into host processor memory as rapidly as it is filled, and an error occurs as frame data is lost. Overflow status bit will be set.

3 Watchdog timer Expired: If the timer expire reception will be cut off and a CSR bit will be set.

4 Collision: Either a normal or a late collision occurred. In the latter case, Late Collision status bit will be set.

5 Memory error: An error has occurred on either the host bus or in the host memory. A CSR bit will be set.

6 Descriptor error: An error has occurred on the definition of the descriptor for reception.

6.3.6 Frame Reception Conditions

Upon terminating reception, the SGEC will determine the status of the received frame and load it into the Receive Status word in the buffer descriptor. An interrupt will be issued if enabled. The SGEC may report the following conditions at the end of frame reception:

1 Overflow: The SGEC receive FIFO overflowed.

2 CRC Error: The 32-bit CRC transmitted with the frame did not match that calculated upon reception. The CRC check is always done and is independent of any other errors.

3 Dribbling bits Error: This indicates the frame did not end on a byte boundary. The SGEC signals dribbling bits error only if it detects more than two dribbling bits. Only *whole bytes* are run through the CRC check. This means that although up to seven dribbling bits may have occurred, framing error signaled, the frame might nevertheless have been correctly received.

4 Frame Too Short (Runt frame): A frame containing less than 64 bytes of information was received (including CRC). Reception of such runt frames is optionally selectable. The SGEC defaults to inhibit reception of runts.

5 Frame Too Long : A frame containing more than 1500 bytes of information was received Reception of such long frames is completed with an error indication.

6 Late collision Error: A frame collision occurred after 64 bytes of information were received. Reception of such frames is completed , an error bit will be set on the descriptor.

7 Descriptor error: An error was found in one of the receive descriptors, which disabled the proper reception of an incoming frame.

6.3.7 Frame reception programmable quantities

- Enable/Disable reception of runt frames.
- Receive Address Filtering :
  1. Fourteen Addresses Perfect Filtering.
  2. One Physical Address Perfectly Filtered with 512 bits Mask for Imperfect Hash Filter for Multicast Addresses.
  3. Promiscuous mode.
  4. Fourteen Addresses Perfect and All Multicast Addresses.
- Watchdog timer count.
- Enable/disable CRC stripping on reception.
- Enable/disable pad stripping off IEEE 802.3 formatted frames.

7 Diagnostics and Testing

The SGEC supports two levels of testing features.

The first level includs diagnostics features which may be activated without taking the SGEC out of the system. They will need some different software set up but will give more information on the chip without changing the hardware set up.

The second level allows more thorough testing by switching the SGEC to work in diagnostic mode. All those features will be described in this chapter.

7.1 SGEC Operational mode diagnostics features.

Extensive on chip diagnostics is provided by the SGEC. Error in the self test are recorded as flags in the CSRs and should be examined by the CPU before starting operations.

This paragraph lists the summary of diagnostics features that the SGEC will support in operation mode.

7.1.1 SGEC internal Self test

The SGEC includes a self test which is performed after Reset, this test checks some internal parts of the SGEC and after the test completion a report is given in the Status register.

The following hardware blocks of the SGEC are tested in the self test and their functionality is reported in CSR5.

The Internal ROM, RAM, Transmit FIFO, Receive FIFO and the Address Recognition RAM. After testing those blocks the SGEC perform an internal local Loopback test, to check the serial channel functionality.

7.1.2 Time Domain Reflectometer

A Time Domain Reflectometer is incorporated into the SGEC to aid locating faults in the Ethernet cable. Short and opens manifest themselves in reflections which are sensed by the TDR.

7.1.3 SGEC Loopback modes

There are two SGEC Loopback modes, internal and external Loopback. In all types of device Loopback supported by the SGEC it is the responsibility of the host software to build the frame to transmit and to provide a receive buffer for the looped data to be returned to the host processor.

The SGEC Loopback modes are described in Chapter 5.

7.2 SGEC Diagnostic mode features.

This paragraph will list the functions that the SGEC will support in diagnostic mode. Those functions will only be accessible after the TSM pin was set to test mode, thus they mostly will be used for debugging and production testing and less in on board diagnostics:

The following diagnostics features are available on the SGEC:

1 Diagnostic CSR's.

2 Serial access to all the SGEC internal registers via test pins.

3 The ability to load code patches to the internal quip via test pins.

4 Monitor mode.

5 Dump and load internal SGEC address space.

7.2.1 Diagnostic CSR's.

Four CSR's are used for diagnostics purposes, their operation is as follow:

7.2.1.1 Reserved register (CSR12)

This register is reserved for future diagnostics

7.2.1.2 Breakpoint Address Register (CSR13)

This register is virtual CSR. It contains the breakpoint address that will cause the internal CPU to jump to a patch address.

Figure 7–1 CSR13 format

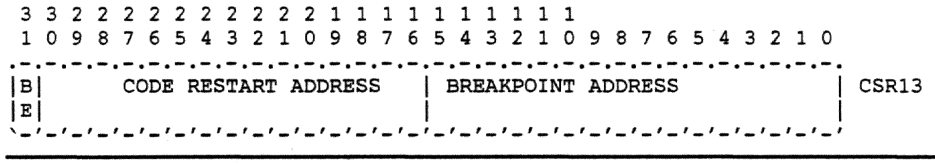


Table 7–1 CSR13 bits

Bit	Name	Access	Description
15:0	BPA	R/W	Breakpoint Address - Define the internal processor address at which the program will halt and jump to the RAM loaded code.
30:16	CRA	R/W	Code restart address - Define the first address in the internal ROM that the internal processor is supposed to jump to after a breakpoint occurred.
31	BE	R/W	Breakpoint enable.

Note: This register in conjunction with the Write address space diagnostics descriptors allow the testing of software patches.

7.2.1.3 Reserved Register (CSR14)

This register is reserved for future diagnostic purposes.

7.2.1.4 Diagnostic mode and status Register (CSR15)

This register is a phisical CSR. It contains the bits which will select the internal test block operation mode.

Figure 7–2 CSR15 format

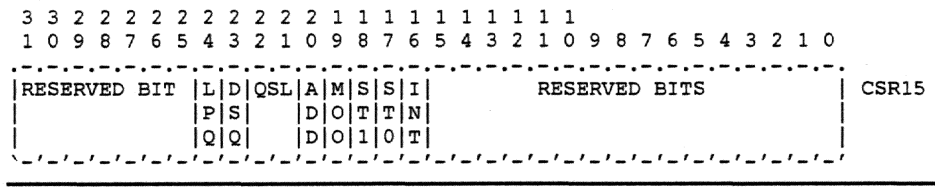


Table 7–2 CSR15 bits

Bit	Name	Access	Description
15:0	RES	R/W	Reserved bits - for future use, will erad as 1
16	INT	R/W	Interrupt bit - This bit will set the internal level 14 interrupt.
17	ST0	R/W	Status 0 bit - This bit is a general popose status bit which may be set or reset by a external control. It may be used for diagnostics programs control.
18	ST1	R/W	Status 1 bit - This bit is a general popose status bit which may be set or reset by a external control. It may be used for diagnostics programs control.
19	MON	R/W	Monitor bit - This bit will select the tests block mode of operation. When set to one it will be in monitor mode and when set to zero it will be in serial test mode.
20	ADB	R/W	Address data space - This bits will define the whether the monitor function will apply to the address or data space which will be available on the external test pins BM_L/TEST<3:0>
22:21	QSL	R/W	Quad select bits - This bits will define the specific four bits of the address or data space which will be available on the external test pins BM_L/TEST<3:0>
23	DSQ	R/W	Disable Quip bit - This bit is used to disable the Quip operation, for control purposes.
24	LPQ	R/W	Loopback Quip bit - This bit is used to put the Quip in a loop on instruction status, in this mode the Quip will indefinitly execute a specific instruction.
31:25	RES	R/W	Reserved - will read as 1

7.2.2 Serial access to the SGEC via test pins.

The four test pins may be used to load and read serial information from the internal SGEC ADDRESS SPACE. The pins BM_L/TEST<3:0> will be allocated to test pins when TSM pin is set to 1. In this mode those pins will work as a serial mechanism to load and read data from the SGEC internal bus by bypassing the SGEC internal controller.

The following assignment IS valid :

BM_L/TEST<0> - Serial test data in.

BM_L/TEST<1> - Serial operation strobe signal.

BM_L/TEST<2> - Serial load clock envelope signal.

BM_L/TEST<3> - Serial test data out.

This hardware block allowS reading and writing to any internal register in the following way:

Reading internal registers:

To perform this operation the required internal address is loaded serialy into the serial address register and then the strobe pin is set to high for one clock cycle. As a result the data on the specific address will be loaded internally to the data register. Shifting the data 16 more bits will send this data to the outside world.

Writing internal registers:

To perform this operation the required internal address and data is loaded serialy into the serial address register and data register by a 31 cycle load signal. then the strobe pin is set to high for one clock cycle. As a result the data on data register will be loaded to the specific address listed on the address register. The following figure will show the specific internal organization.

Figure 7–3 SGEC test loop hardware.

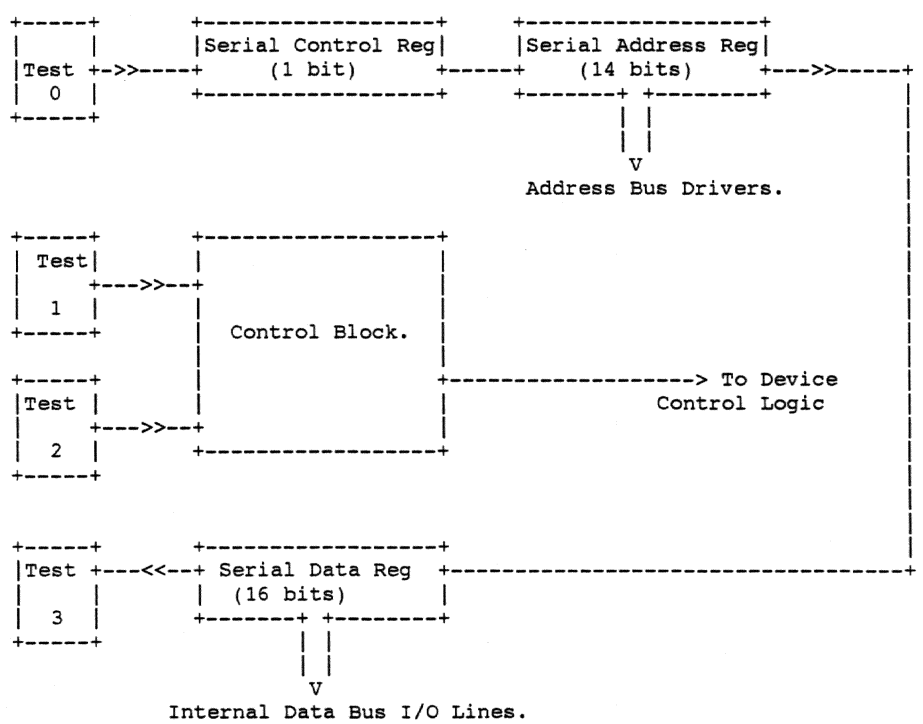


Figure 7–3 Cont'd. on next page

Figure 7–3 (Cont.) SGEC test loop hardware.

7.2.2.1 Serial Address Register

This register will store the serial loaded address. It will be a 14 bit shift register connected to the internal address bus.

Figure 7–4 Serial Address register

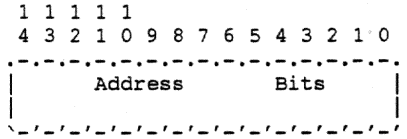


Table 7–3 Serial Address Register

Bit	Name	Access	Description
14:0	AD	Serial	Internal address bits

7.2.2.2 Serial Control Register

This register will include the control bits. It will be a one bit control register.

Figure 7–5 Serial control register

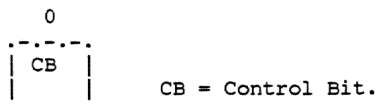


Table 7–4 Serial control register

Bit	Name	Access	Description
0	RWB	Serial	Read write bit , when 1 set to read when 0 set to write.

7.2.2.3 Serial Data Register

This register will be an internal data register latch. It will be a 16 bit input output serial register.

Figure 7–6 Serial Data Register

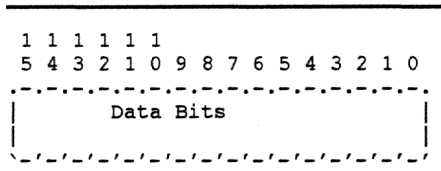


Table 7–5 Serial Data register bits

Bit	Name	Access	Description
15:0	DB	Serial	DATA bits - the internal SGEC data bits

7.2.3 Performing code Patches

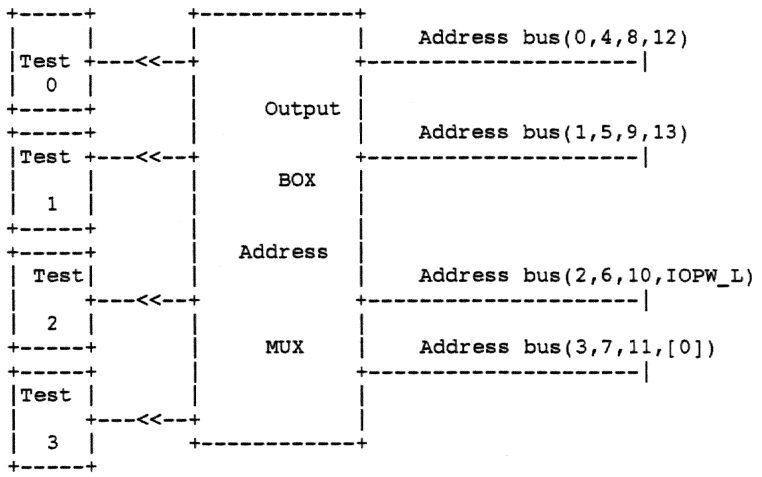
Code patches can be done in the SGEC via two mechanism. The first is the load address space, and the second is the serial test block load mechanism.

7.2.4 Monitoring of the internal Busses

7.2.4.1 Monitoring of the internal Processor address bus

The four test pins may be used to monitor the SGEC code sequence by getting on them the SGEC address lines. This will be controlled by CSR15.

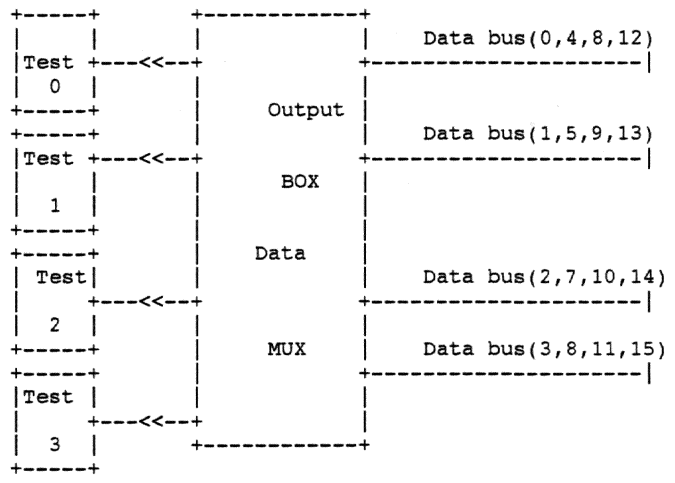
Figure 7–7 SGEC address monitor hardware.



7.2.4.2 Monitoring of the internal Processor Data bus

The four test pins may be used to monitor the SGEC internal data bus by getting on them the SGEC internal data lines. This will be controlled by CSR15.

Figure 7–8 SGEC data bus monitor hardware.



7.2.5 Diagnostics frame

A diagnostics frame may be used in the SGEC to load and dump internal address spaces. The Diagnostics frame is *never* transmitted over the Ethernet, nor looped back to the receive list. The diagnostics frame must be wholly contained in a single transmit buffer. There are two types of Diagnostics frames:

1 Diagnostics Dump Address space.

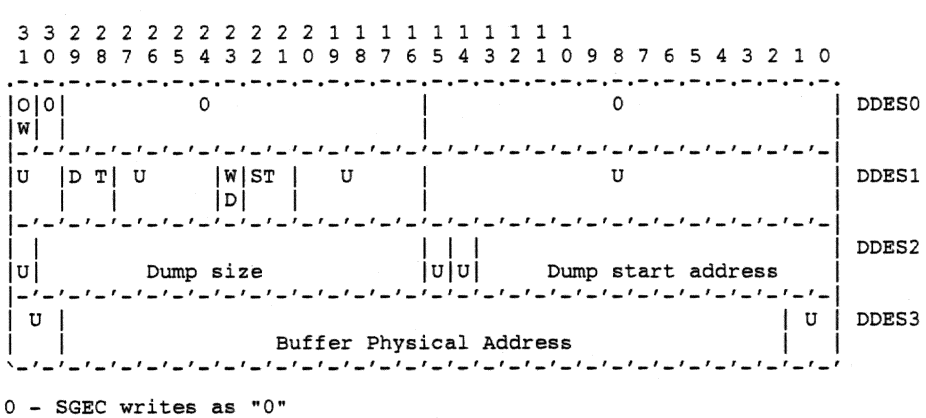
2 Diagnostics Read Address space.

A Diagnostics frame may be given to the SGEC while the Reception process is in the RUNNING, SUSPENDED or STOPPED state, nor does it affect the state of the Reception process. The only requirement for the diagnostics frame to be processed, is that the Transmission process be in the running state. The setup frame will be processed after the current frame reception, if any, is completed. While the diagnostics frame is being processed, the receiver logic will temporarily disengage from the Ethernet wire. The diagnostics frame will be controlled by the following descriptor:

The diagnostic frames are only proceed when the SGEC Operation mode is placed in **Diagnostic** mode CSR6<OM> = <11>.

A dump frame must never be placed inside a multi_buffer frame. If its occurs, the Tx process stops the frame transmission and enters the SUSPENDED state as for a descriptor error.

Figure 7–9 Diagnostic frame descriptor format



0 - SGEC writes as "0"
U - Ignored by the SGEC on read, never written

Table 7–6 Diagnostic descriptor

Word	Bit	Name	Description
DDES0	31	OW	Own bit - When set, indicates the descriptor is owned by the SGEC. When cleared, indicates the descriptor is owned by the host. The SGEC clears this bit upon completing processing of the descriptor and its associated buffer.
DDES1	22:21	ST	SGEC dump Type - Select the SGEC dump type:

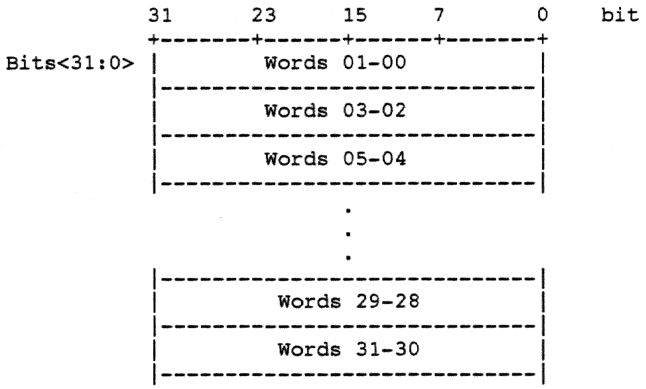
Value	Meaning
00	ROM/RAM/Registers dump
01	Rx Fifo data dump
10	Tx Fifo data dump

DDES1	23	WD	Read/Write Dump - When set (WRITE), the host data will be download into the SGEC. When reset (READ), the SGEC data will be dumped into the host diagnostic buffer.
	29:28	DT	Data type - For Diagnostic frames those bits should be 11
DDES2	13:00	DA	Dump start Address - The start address of the transfer into/from the SGEC internal memory.
	30:16	DS	Dump Size - The size, in word of the memory data transfer.
			Note: The associated buffer must be equal or greater than the dump size.If this is not the case, the dump destination memory (host or SGEC) will be corrupted.
DDES3	29:02	PA	Diagnostic buffer Physical Address -
			Note: Diagnostic buffer may be word aligned.

7.2.5.1 Address Dump Diagnostics frame

This section describes how the SGEC will interpret a diagnostics frame when a dump set up packet will be sent. The Dump buffer must be word aligned. It will contain after the operation the data dumped from the internal Address space. This can be used to dump the internal ROM, RAM or any other internal register.

Figure 7–10 Address Dump Diagnostics frame format

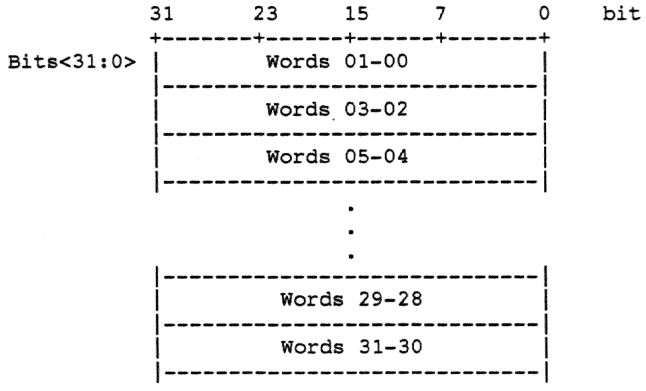


7.2.5.2 Address load Diagnostics frame

This section describes how the SGEC will interpret a diagnostics load frame when it is sent to the chip.

The format for the load address space table is shown below:

Figure 7–11 Address Load Diagnostics frame format



Bits are sequentially numbered from right to left and down the table.

8 System Configurations

The SGEC device can be integrated into a system in three main different system configurations:

1 CVAX host bus system.

2 GHIDRA local bus system.

3 Other host bus system configuration.

8.1 CVAX host bus system

This configuration is the generic configuration for system based on the 32 bit Digital Microprocessor family. In this configuration the SGEC device will reside directly on the CVAX CP-BUS.

This mode of operation can be divided into two sub modes which differ slightly in their application space:

1 CVAX host bus with SGEC in synchronous mode.

2 CVAX host bus with SGEC in asynchronous mode.

8.1.1 CVAX host bus with SGEC in synchronous mode

This is the highest performance configuration. In this configuration the SGEC will use the same CLKA and CLKB signals as the CVAX, and will work synchronously with the CVAX bus.

It will have a 32 bit multiplexed address and data bus and will be able to do the VAX virtual memory address translation.

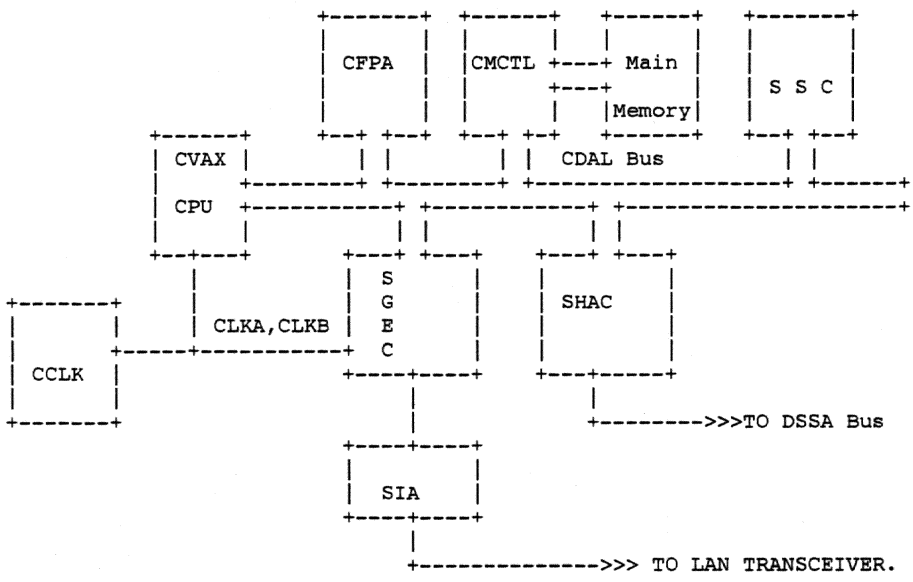
The command and status registers will be transferred between the SGEC and the CVAX via a simple slave interface, while the data blocks will be DMAed directly by the SGEC to main memory buffers.

No glue will be needed to connect the device to the CVAX CP-BUS.

To complete A network connection the system will need in addition to the SGEC an SIA to drive the Transceiver cable and an External Tranceiver.

The following figure is a typical system connection scheme for this mode:

Figure 8–1 Typical SGEC CVAX Host synchronous system configuration



8.1.2 CVAX host bus with SGEC in asynchronous mode

This mode main design goal is to allow for the SGEC to be connected to CVAX at different frequencies either because of faster CVAX CPU chips or the need to use bus buffers for the CVAX bus.

In this mode the SGEC will reside on the CVAX bus asynchronously using a different clock.

In this mode the SGEC will be driven by a separate clock chip. As different clock are used the SGEC will work asynchronously with the processor.

It will have a 32 bit multiplexed address and data bus and will be able to do the VAX virtual memory address translation.

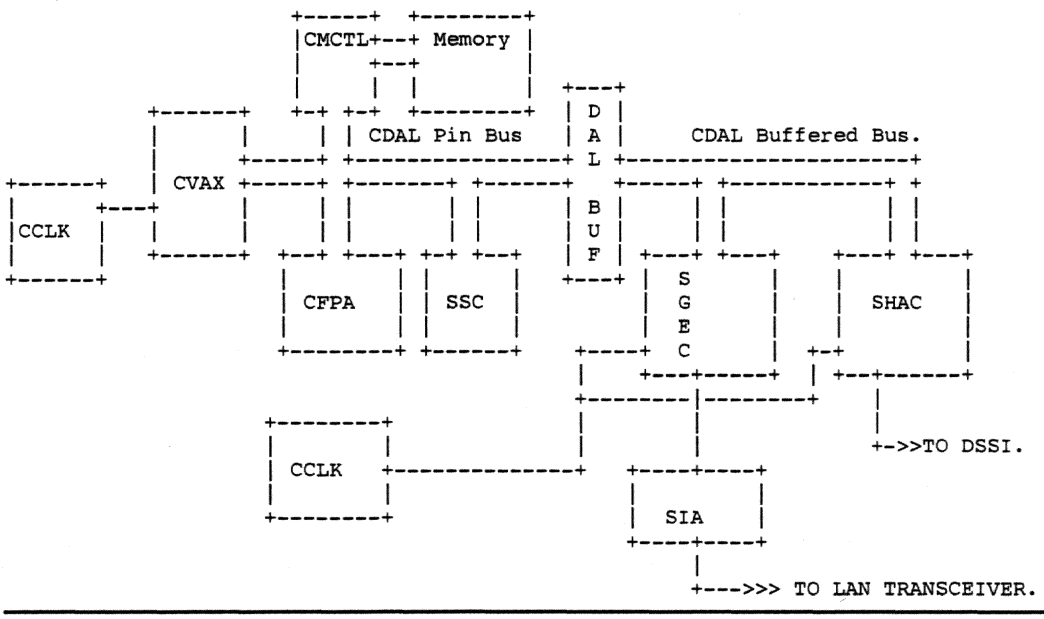
The control and status registers will be transferred between the SGEC and the CVAX via a simple slave interface, while the data blocks will be DMAed directly by the SGEC to main memory buffers.

No glue will be needed to connect the device to the CVAX buffered pin bus. An SSC device will be needed on the CP-Bus to syncronize the Rdy, Err and Reset Signals.

To Complete a full network connection the system will need in addition to the SGEC an SIA chip to drive the Tranceiver cable and a Transceiver.

The following figure is a typical system connection scheme in this mode:

Figure 8–2 Typical SGEC CVAX Host asynchronous system configuration



8.2 GHIDRA bus with SGEC in synchronous mode

This mode main design goal is to be used in high performance systems like the RIGEL where buffering is needed between the system bus and the peripherals.

In this configuration the SGEC will reside on the GHIDRA local bus.

Note: It is assumed that the GHIDRA is identical to the CMCTL, when viewed from the 32 bits (CP-Bus) bus side.

In this mode the SGEC will use the same clock as the GHIDRA chip and will work synchronously with the GHIDRA. It will be connected VIA the 32 bit multiplexed address and data bus.

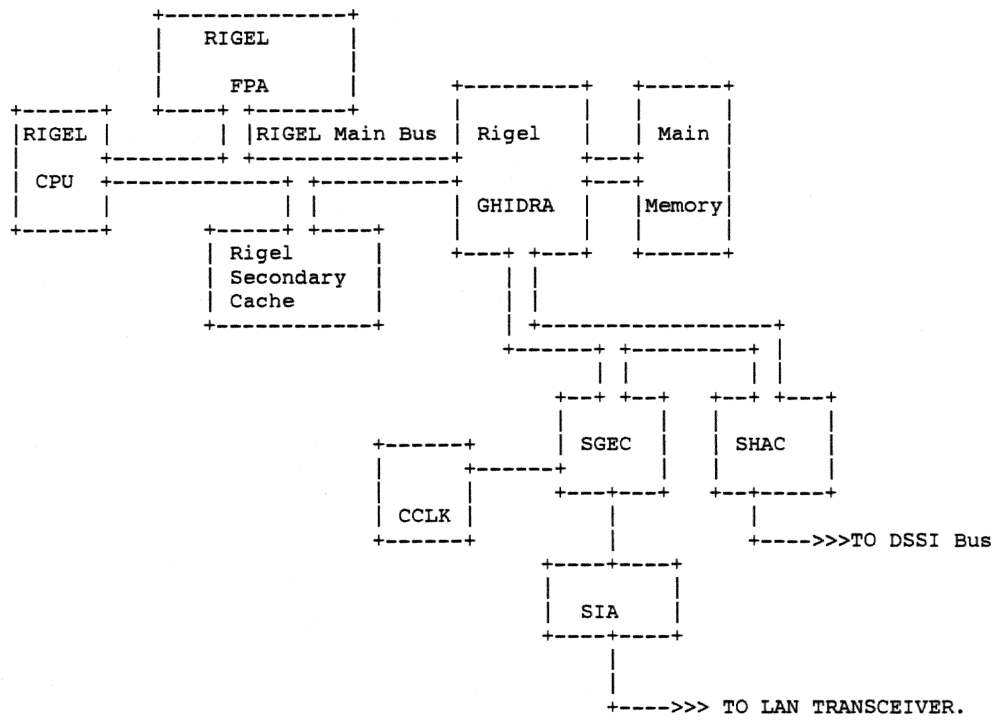
The command and status registers will be transferred between the SGEC and the RIGEL via the window capability of the GHIDRA chip while the data blocks will be transferred by the SGEC via the GHIDRA chip to the main memory buffers.

No glue will be needed to connect the device to the local GHIDRA CP-Bus.

To Complete a full network connection the system will need in addition to the SGEC an SIA to drive the Tranceiver cable and a Transceiver.

The following figure shows the connection scheme:

Figure 8–3 GHIDRA local bus configuration



8.3 Other host bus configuration

The device may also be used for the 32 bit non Digital processor, such as the Intel 80386, and the Motorola 68020, or with other Digital processors not pin compatible to the CP-Bus, such as the μVAX chip.

In this configuration the SGEC will not reside directly on the Processor bus. It will need external glue logic such as TTL multiplexer and transceivers. The control for these multiplexors and transceivers can be derived from the SGEC's bus control signals.

In this mode the SGEC will need a clock chip to drive its timing and it will work asynchronously with the processor.

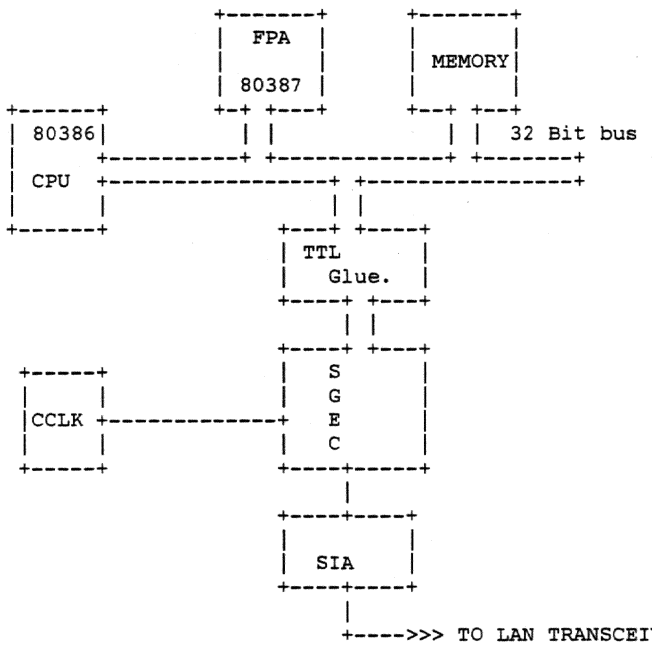
It will have a 32 bit multiplexed address and data bus and will be used in physical memory mode.

The control and status registers will be transferred between the SGEC and the processor via slave memory transfers. Data blocks will be transferred by the SGEC to main memory by the DMA channel.

The serial LAN connection will need an SIA and a Transceiver to complete a fatwire Ethernet capability.

The following figure is a system connection scheme:

Figure 8–4 Block Diagram for 80386 System



8.4 SGEC serial line configurations

This paragraph will show the various way in which the SGEC can be connected to an Ethernet serial line. For all the three configurations the SGEC will need an external SIA to drive the transceiver lines.

The serial line mode of operation can be divided into three sub modes which differ slightly in their application space:

1 SGEC on 10BASE5 (fatwire) Ethernet line.

2 SGEC on 10BASE2 (DTE) line.

3 SGEC on twisted pair Ethernet line.

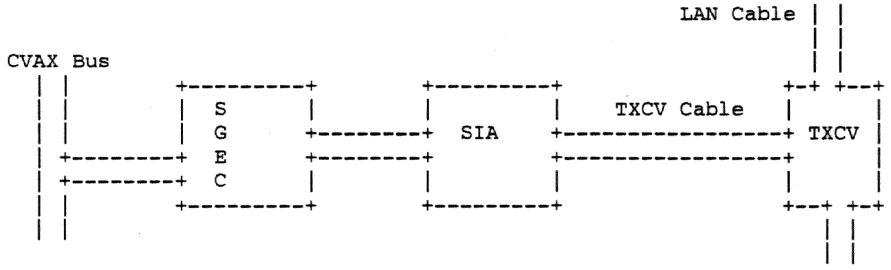
8.4.1 SGEC configuration on 10BASE5 (fatwire) Ethernet line.

In this configuration the SGEC will be used on a full fatwire 2.5Km Ethernet network.

The SGEC will do part the data link Layer protocol for the serial LAN connection and will need an external SIA to drive the full 50m Transceiver cable. It will also need and a Transceiver to connect to the coax cable.

The following figure is a typical system connection scheme:

Figure 8–5 SGEC configuration on fatwire Ethernet line.



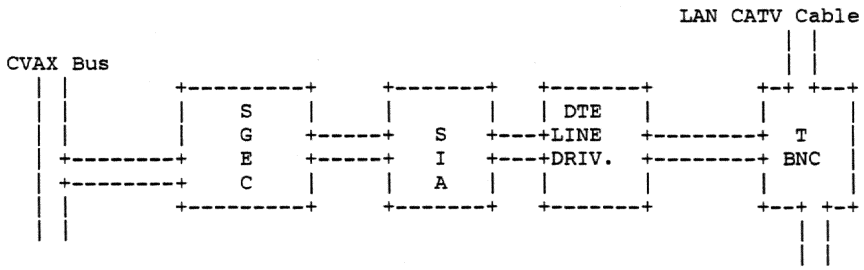
8.4.2 SGEC configuration on 10BASE2 DTE line.

In this configuration the SGEC will be used with an External SIA to drive only a DTE Transceiver on the same board. This will allow working only with up to 185m DTE cables.

The SGEC will do part of the Data link layer protocol and for the serial LAN connection will need an external SIA and a DTE driver to drive the DTE cable.

The following figure is a typical system connection scheme:

Figure 8–6 SGEC configuration on DTE line.



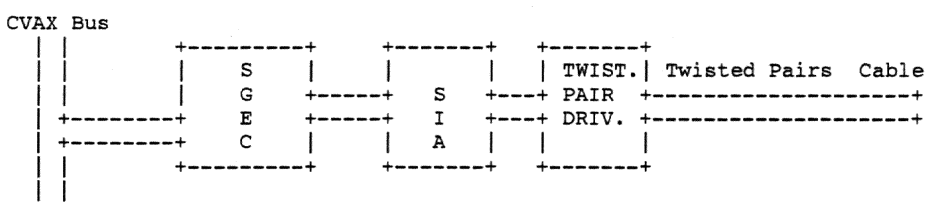
8.4.3 SGEC configuration on twisted pair Ethernet line.

This is the lowest cost configuration in term of the serial line . In this configuration the SGEC will need an external SIA and a twisted pairs line driver to connect to the Network. This will allow working with DEC 10 MHZ twisted pairs or Starlan configuration.

The SGEC will do part of the data link layer protocol for the serial LAN connection and will need an external SIA and line driver to drive the twisted pair cable.

The following figure is a typical system connection scheme:

Figure 8–7 SGEC configuration on twisted pair Ethernet line.



9 AC/DC Characteristics

9.1 Absolute Maximum Ratings

This table defines the maximum rating for the SGEC storage and operation.

Table 9-1 SGEC absolute maximum ratings

No.	Parameter	Value
1	Storage Temperature Range	-55 C to +125 C
2	Operating Temperature Range	0 C to +125 C
3	DC Supply Voltage Range	-0.5 V to +7.0 V
4	Input/Output voltage applied	-0.5 V to +7.0 V

9.2 Electrical Characteristics

This table shows the specified electrical characteristics for the SGEC.

Table 9-2 SGEC Electrical characteristics table

No.	Parameter	Value
1	Specified Temperature Range	0 C to +70 C
2	Specified Supply Voltage Range	+4.50 V to +5.50 V

This table shows the specified electrical characteristics for the SGEC.

Table 9-3 SGEC Electrical characteristic table

Symbol	Paramter	Min	Max	Units	Test condition
Vih	High level input voltage	2.0		V	
Vil	Low level input voltage		0.8	V	
Voh	High level output voltage	2.4		V	Ioh = -400 uA
Vol	Low level output voltage		0.4	V	Iol = 2.0 mA, CL = 100Pf
Vihm	High level input voltage (MOS)	90% VDD		V	Ioh = -100 uA, CL= 100pF
Vilm	Low level input voltage (MOS)		10% VDD	V	Iol = 1.0 mA, Cl = 100 pF
Iil	Input leakage current	-10	10	uA	0<Vin<VDD
Iol	Output leakage current	-10	10	uA	0< Vin<VDD
Icc	Active supply current		500	mA	Iout = 0, Ta = 0c

Table 9–3 (Cont.) SGEC Electrical characteristic table

Symbol	Paramter	Min	Max	Units	Test condition
Cin	Input capacitance		5	pF	
Cout	Output capacitance		10	pF	
Cio	Input/Output capacitance		10	pF	

This table shows the specified electrical characteristics for the SGEC.

Table 9–4 SGEC Electrical Signal Summary

Signal Name	Signal Type	Pin Number	Applicable Tests					
			Vih	Vil	Voh	Vol	Iil	Iol
CDAL<31>	IO	63	X	X	X	X	X	X
CDAL<30>	IO	62	X	X	X	X	X	X
CDAL<29>	IO	61	X	X	X	X	X	X
CDAL<28>	IO	60	X	X	X	X	X	X
CDAL<27>	IO	59	X	X	X	X	X	X
CDAL<26>	IO	58	X	X	X	X	X	X
CDAL<25>	IO	57	X	X	X	X	X	X
CDAL<24>	IO	56	X	X	X	X	X	X
CDAL<23>	IO	55	X	X	X	X	X	X
CDAL<22>	IO	52	X	X	X	X	X	X
CDAL<21>	IO	51	X	X	X	X	X	X
CDAL<20>	IO	50	X	X	X	X	X	X
CDAL<19>	IO	49	X	X	X	X	X	X
CDAL<18>	IO	48	X	X	X	X	X	X
CDAL<17>	IO	47	X	X	X	X	X	X
CDAL<16>	IO	46	X	X	X	X	X	X
CDAL<15>	IO	45	X	X	X	X	X	X
CDAL<14>	IO	42	X	X	X	X	X	X
CDAL<13>	IO	41	X	X	X	X	X	X
CDAL<12>	IO	40	X	X	X	X	X	X
CDAL<11>	IO	39	X	X	X	X	X	X
CDAL<10>	IO	38	X	X	X	X	X	X
CDAL<09>	IO	37	X	X	X	X	X	X
CDAL<08>	IO	36	X	X	X	X	X	X
CDAL<07>	IO	35	X	X	X	X	X	X
CDAL<06>	IO	34	X	X	X	X	X	X
CDAL<05>	IO	31	X	X	X	X	X	X
CDAL<04>	IO	30	X	X	X	X	X	X

Table 9–4 (Cont.) SGEC Electrical Signal Summary

Signal Name	Signal Type	Pin Number	Applicable Tests					
			Vih	Vil	Voh	Vol	Iil	Iol
CDAL<03>	IO	29	X	X	X	X	X	X
CDAL<02>	IO	28	X	X	X	X	X	X
CDAL<01>	IO	27	X	X	X	X	X	X
CDAL<00>	IO	26	X	X	X	X	X	X
RESET_L	I	25	X	X			X	
CLKA *	I	24	X	X			X	
CLKB *	I	23	X	X			X	
AS_L	IO	20	X	X	X	X	X	X
DS_L	IO	18	X	X	X	X	X	X
WR_L	IO	17	X	X	X	X	X	X
RDY_L	IO	16	X	X	X	X	X	X
ERR_L	I	15	X	X			X	
DMR_L	O	14			X	X		X
DMGI_L	I	13	X	X			X	
CS/DP_L<3>	IO	10	X	X	X	X	X	X
CS/DP_L<2>	IO	09	X	X	X	X	X	X
CS/DP_L<1>	IO	08	X	X	X	X	X	X
CS/DP_L<0>	IO	07	X	X	X	X	X	X
BM_L/TEST<3>	IO	06	X	X	X	X	X	X
BM_L/TEST<2>	IO	05	X	X	X	X	X	X
BM_L/TEST<1>	IO	04	X	X	X	X	X	X
BM_L/TEST<0>	IO	03	X	X	X	X	X	X
CCTL_L	O	02			X	X		X
CSL_L	I	83	X	X			X	
IRQ_L	O	82			X	X		X
IAKEI_L	I	81	X	X			X	
IAKEO_L	O	80			X	X		X
NSGEC_L	O	79			X	X		X
TSM_H	I	78	X	X			X	
DPE_L	IO	77	X	X	X	X	X	X
TXEN_H	I	76	X	X			X	
TX	O	73			X	X		X
TCLK	I	72	X	X			X	
RX	I	71	X	X			X	
RCLK	I	70	X	X			X	
RXEN_H	I	69	X	X			X	

Table 9–4 (Cont.) SGEC Electrical Signal Summary

Signal Name	Signal Type	Pin Number	Applicable Tests					
			Vih	Vil	Voh	Vol	Iil	Iol
CLSN_H	I	68	X	X			X	

* CLKA and CLKB should be tested with Vihm and Vilm.

9.3 SGEC SYSTEM BASIC TIMING

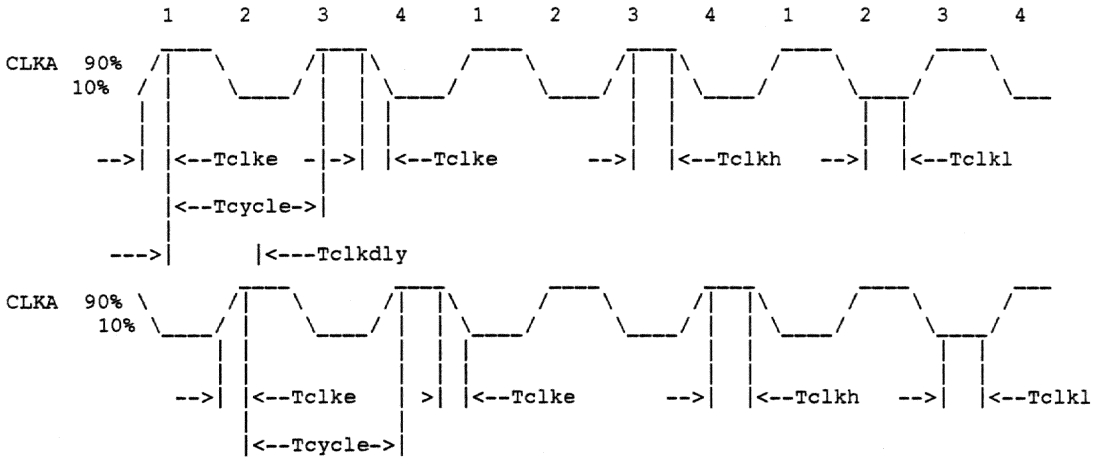
****
QUALIFICATION: These are all PRELIMINARY timing parameters.
****

9.3.1 CVAX Clock In CLKA,CLKB

Those two inputs supply basic clock timing to the chip, when working with a CVAX host. These are nominally a 25 Mhz square wave.

This table show the specified clocks waveforms for the SGEC.

Figure 9–1 SGEC CLKA/CLKB timing



This table show the specified timing characteristics for the SGEC clock inputs.

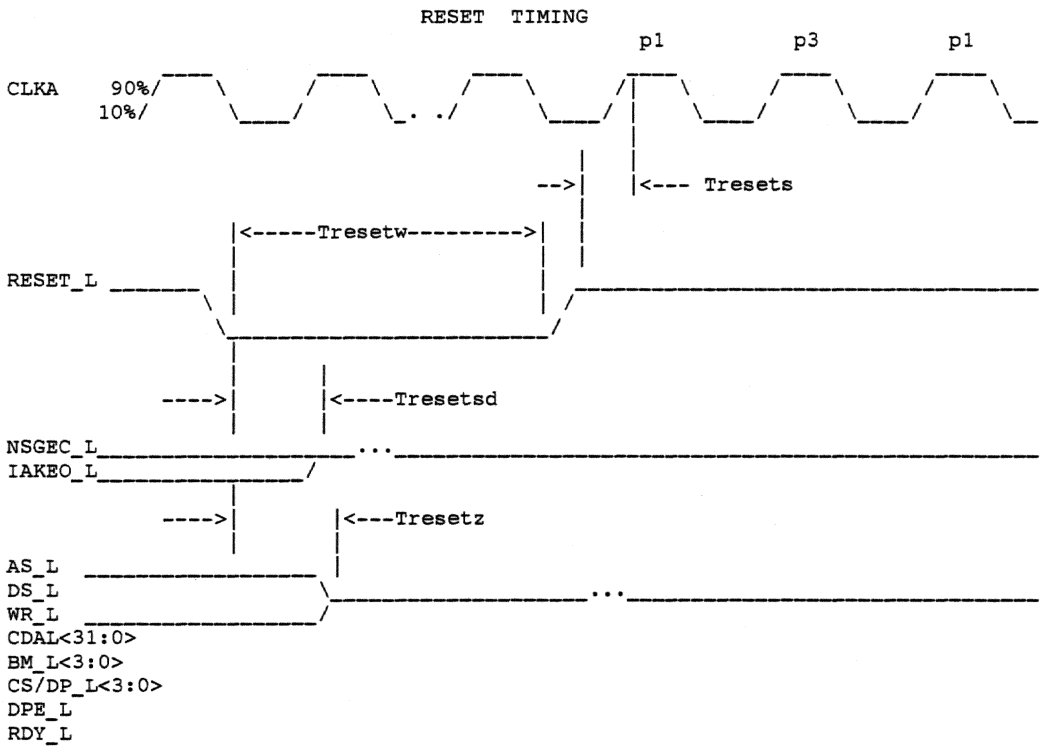
Table 9–5 SGEC CLKA CLKB Timing

Symbol	Definition	Min	Max	Units
Tclke	External clock edge rate	0	8.0	ns
Tcycle	External clock cycle	40.0	TBS	ns
Tclkh	External clock high	12.0	20.0	ns
Tclkl	External clock low	12.0	20.0	ns
Tclkdly	Clock A to clock B delay	18.0	22.0	ns

9.3.2 SGEC RESET pin timing

This input supplies the Reset timing signal to the chip. CLKA and CLKB must be supplied while assertion of RESET_L.

Figure 9–2 SGEC RESET Timing



This table list the SGEC Reset timing.

Table 9–6 SGEC RESET Timing

Symbol	Definition	Min	Max	Units
Tresetw	Reset assertion width	8*Tcycle		ns
Tresetd	Strobe inactive delay from reset	0	120	ns
Tresetz	Bus tristate time from reset	0	120	ns
Tresets	Reset input setup prior to p1	18	Tcycle - 10	ns

9.4 SGEC slave mode timing

****
QUALIFICATION: These are all PRELIMINARY timing parameters.
****

The SGEC operates in slave mode while the host CPU accesses CSRs or acknowledges interrupts.

9.4.1 CPU Read Cycle Timing

This paragraph shows the SGEC timing diagrams and tables for slave Read cycle to the SGEC by the host CPU.

Figure 9–3 SGEC slave read cycle Timing

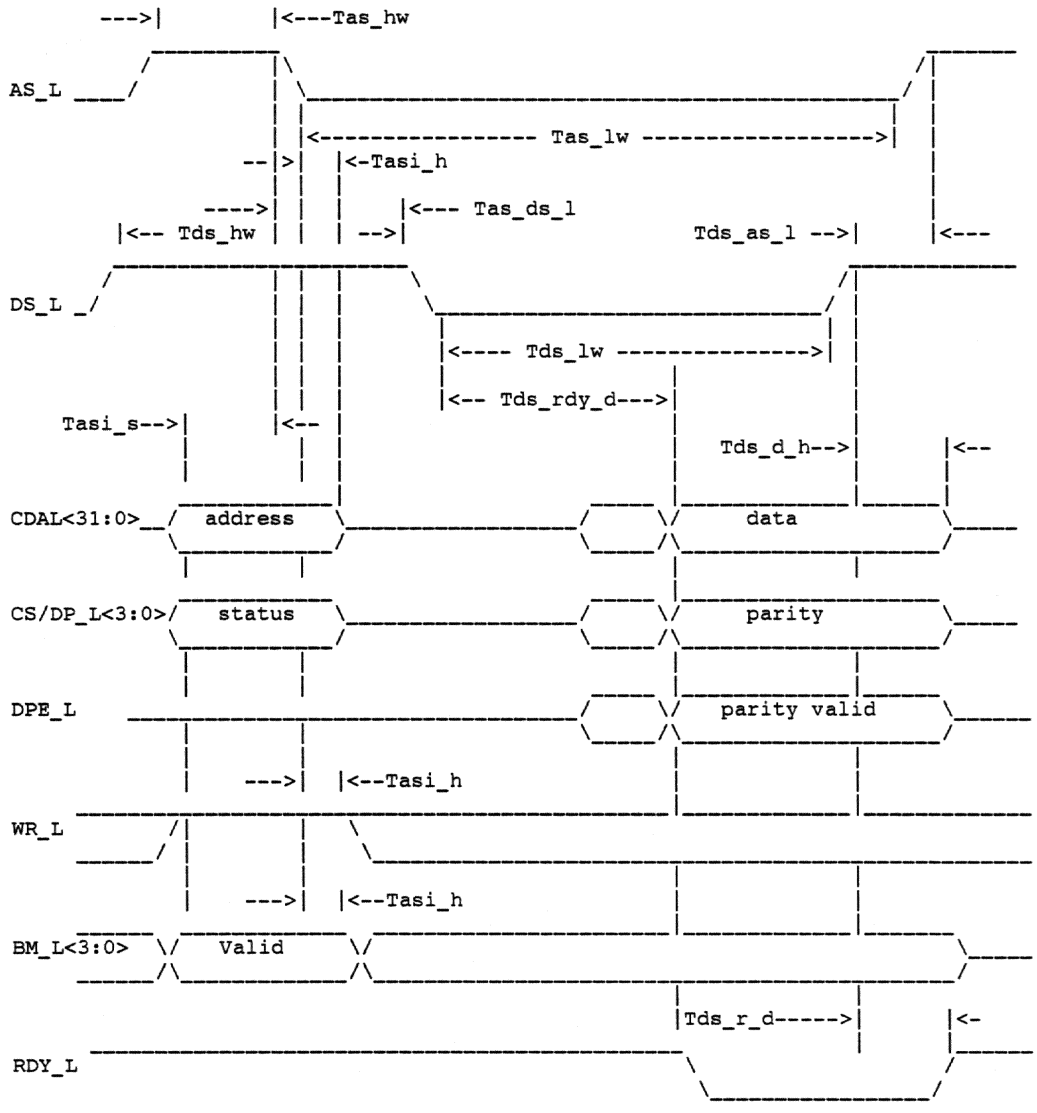


Figure 9–3 Cont'd. on next page

Figure 9–3 (Cont.) SGEC slave read cycle Timing

Table 9–7 SGEC slave read cycle Timing table

Symbol	Definition	Min	Max	Units
Tas_hw	AS high	50		ns
Tas_lw	AS low	240	320	ns
Tasi_h	Address,WR,BM,CS to AS hold time	10		ns
Tasi_s	Address,WR,BM,CS to AS setup time	18		ns
Tas_ds_l	AS to DS delay	40		ns
Tds_hw	DS high	100		ns
Tds_lw	DS low	140	220	ns
Tds_as_l	DS to AS delay	0		ns
Tds_d_h	DS to DATA,Parity	0		ns
Tds_rdy_d	DS to RDY delay	100	180	ns
Tds_r_d	DS to RDY deassertion delay	0	22	

9.4.2 Interrupt acknowledge cycle Timing

This paragraph shows the SGEC timing diagrams and tables for interrupt acknowledge cycle.

Figure 9–4 SGEC Interrupt acknowledge Timing

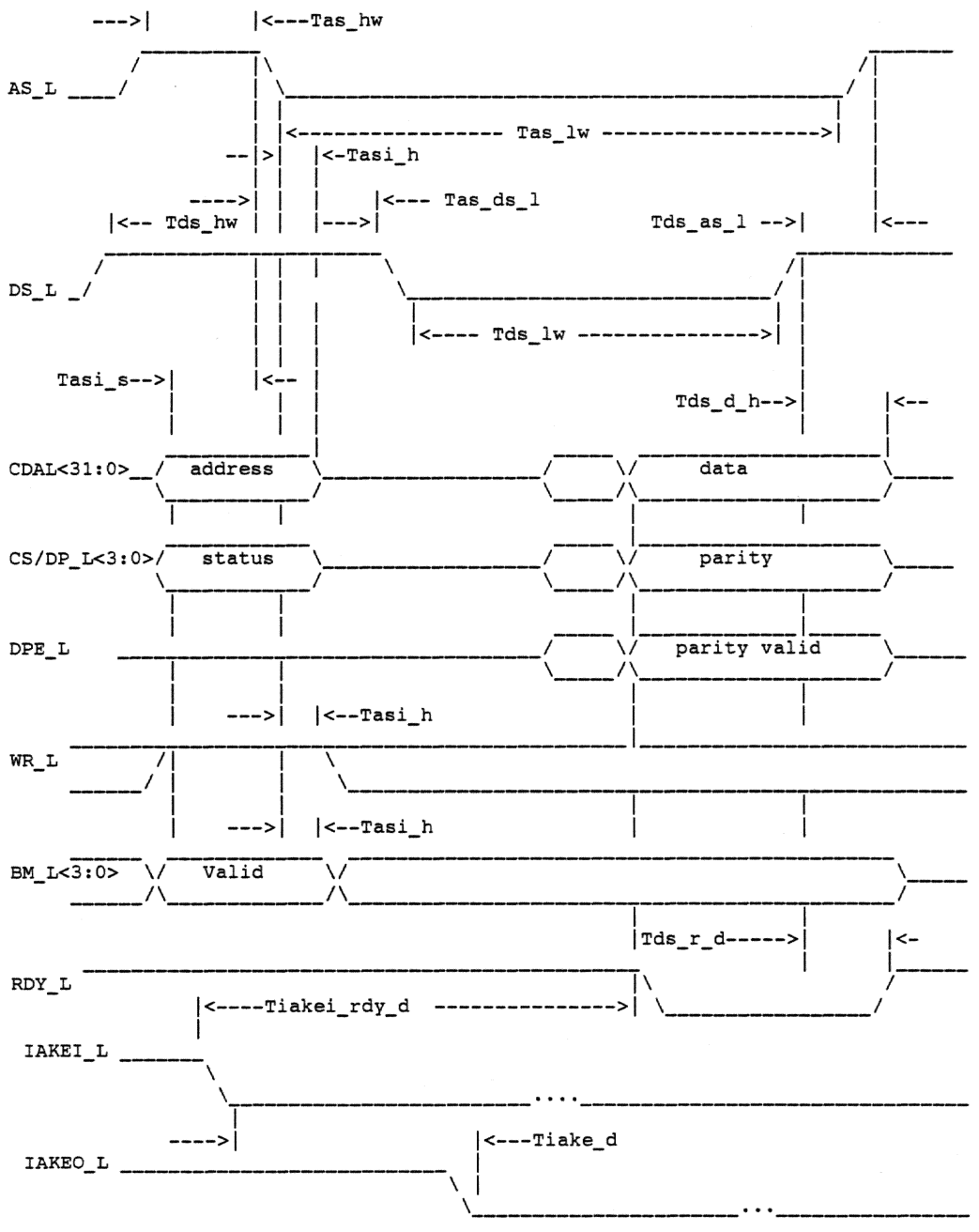


Figure 9–4 Cont'd. on next page

Figure 9–4 (Cont.) SGEC Interrupt acknowledge Timing

Table 9–8 SGEC slave read cycle,interrupt acknowledge cycle Timing table

Symbol	Definition	Min	Max	Units
Tas_hw	AS high	50		ns
Tas_lw	AS low	240		ns
Tasi_h	Address,WR,BM,CS to AS hold time	10		ns
Tasi_s	Address,WR,BM,CS to AS setup time	18		ns
Tas_ds_l	AS to DS delay	40		ns
Tds_hw	DS high	100		ns
Tds_lw	DS low	140		ns
Tds_as_l	DS to AS delay	0		ns
Tds_d_h	DS to DATA,Parity	0		ns
Tiakei_rdy_d	IAKEI to RDY delay (when the SGEC responses to the interrupt acknowledge cycle).	100	180	ns
Tds_r_d	DS to RDY deassertion delay	0	22	
Tiake_d	IAKEI to IAKEO assertion delay (when the SGEC propogates the IAKEI signal)	140	340	ns

9.4.3 CPU Write Cycle

In a host CPU write cycle, it outputs information to The SGEC.

Figure 9–5 CPU write cycle for SGEC in slave mode timing

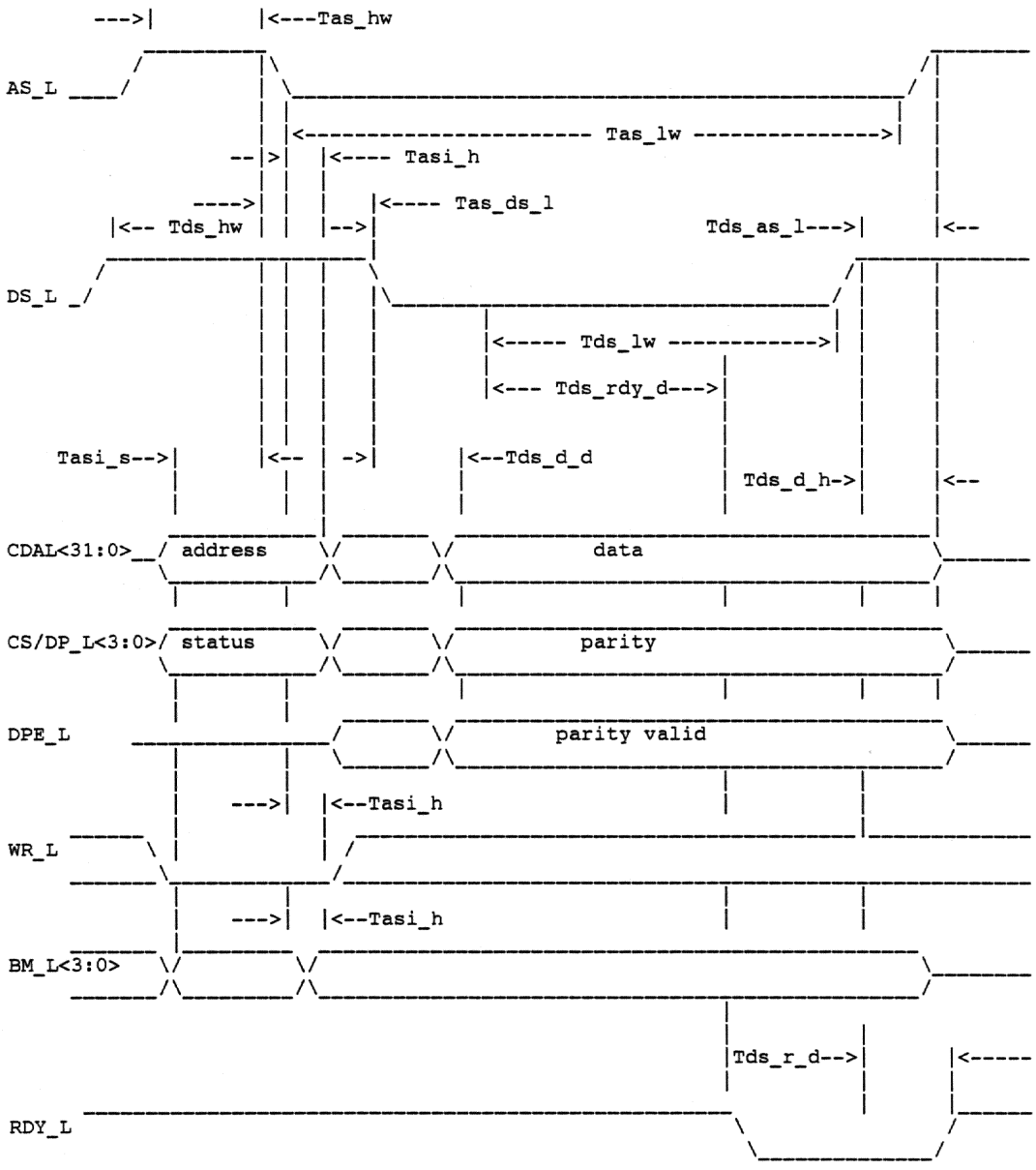


Table 9–9 CPU write cycle Timing

Symbol	Definition	Min	Max	Units
Tas_hw	AS high	50		ns

Table 9-9 (Cont.) CPU write cycle Timing

Symbol	Definition	Min	Max	Units
Tas_lw	AS low	240	320	ns
Tasi_h	Address,WR,BM,CS to AS hold time	10		ns
Tasi_s	Address,WR,BM,CS to AS setup time	18		ns
Tas_ds_l	AS to DS delay	40		ns
Tds_hw	DS high	100		ns
Tds_ lw	DS low	140	220	ns
Tds_as_l	DS to AS delay	0		ns
Tds_rdy_d	DS to RDY delay	100	180	ns
Tds_r_d	DS to RDY deassertion delay	0	22	
Tds_d_d	DS to DATA delay		20	ns
Tds_d_h	DS to DATA hold time	0		ns

9.4.4 NSGEC timing

This diagram shows the timing for the NSGEC_L output. The NSGEC_L signal is asserted when the following occurs:

- A bus cycle doesn't address the SGEC.
- Not during interrupt acknowledge cycle.
- The SGEC selected to work in its internal address.

Figure 9–6 NSGEC timing

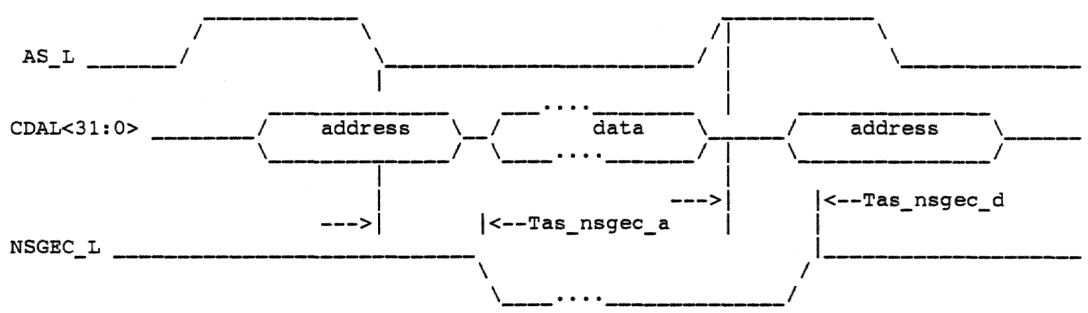


Table 9–10 NSGEC timing

Symbol	Definition	Min	Max	Units
Tas_nsgec_a	AS to NSGEC assertion delay	100	180	ns
Tas_nsgec_d	AS to NSGEC deassertion delay		20	ns

9.5 SGEC MASTER MODE TIMING

****
QUALIFICATION: These are all PRELIMINARY timing parameters.
****

9.5.1 DMA Grant Cycle

The SGEC can request mastership of the CP-BUS and related control signals to transfer incoming and outcoming data by DMA

Figure 9–7 External DMA cycle timing - Acquiring the CP - bus

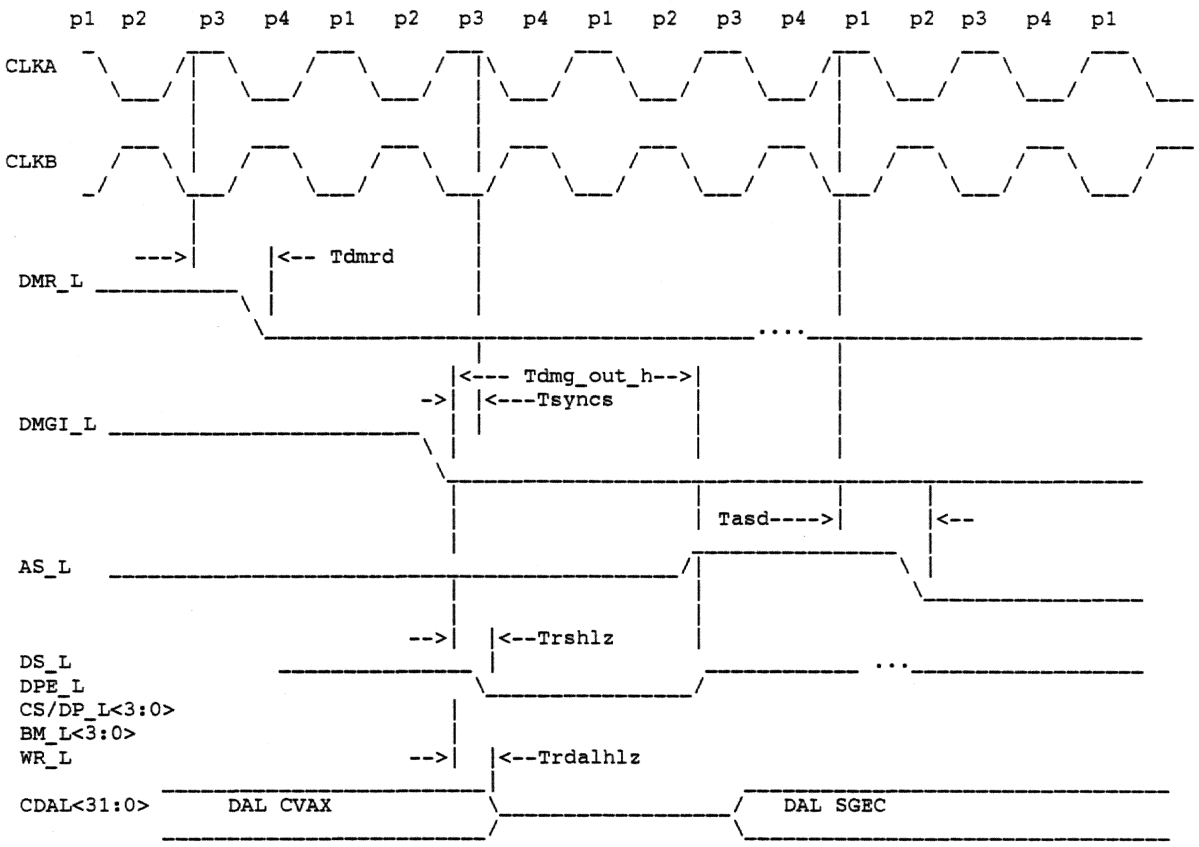


Table 9–11 External DMA cycle timing table - acquiring the CP - bus

Symbol	Definition	Min	Max	Units
Tdmrd	DMR delay	0	18	ns
Tsyncs)	Asynchronousr input setup	12		ns
Tasd	AS strobe assertion delay	0	13.5	ns
Tdmg_out_h	DMGI to SGEC outputs High delay	100	140	ns
Trshlz	Required tri-state		0	ns
Trdalhlz	Required CDAL tri-state		0	ns

Figure 9–8 External DMA cycle timing - Releasing the CP-BUS

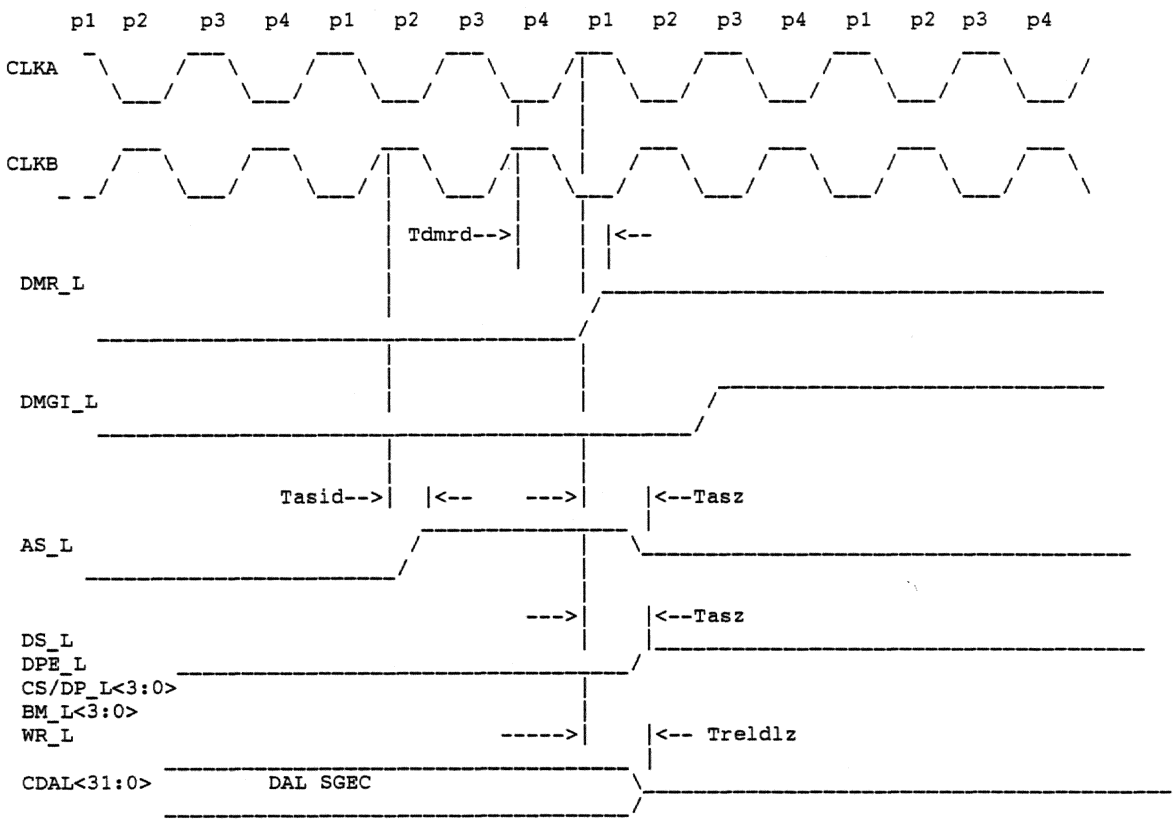


Table 9–12 External DMA cycle timing table - releasing the CP-BUS

Symbol	Definition	Min	Max	Units
Tdmrd	DMR delay	0	18	ns
Tasid	AS strobe deassertion delay	0	18	ns

Table 9–12 (Cont.) External DMA cycle timing table - releasing the CP-BUS

Symbol	Definition	Min	Max	Units
Tasz	Tri-state delay		40	ns
Treldlz	CDAL tri-state		18	

9.5.2 Single Transfer SGEC Read Cycle

In a single transfer SGEC read cycle, the SGEC reads one longword from the main memory. A single transfer read cycle requires a minimum of four clock phases (nominally 160 ns) and may last longer, in increments of two clock phases (nominally 80 ns).

Figure 9–9 Single Transfer SGEC read Cycle

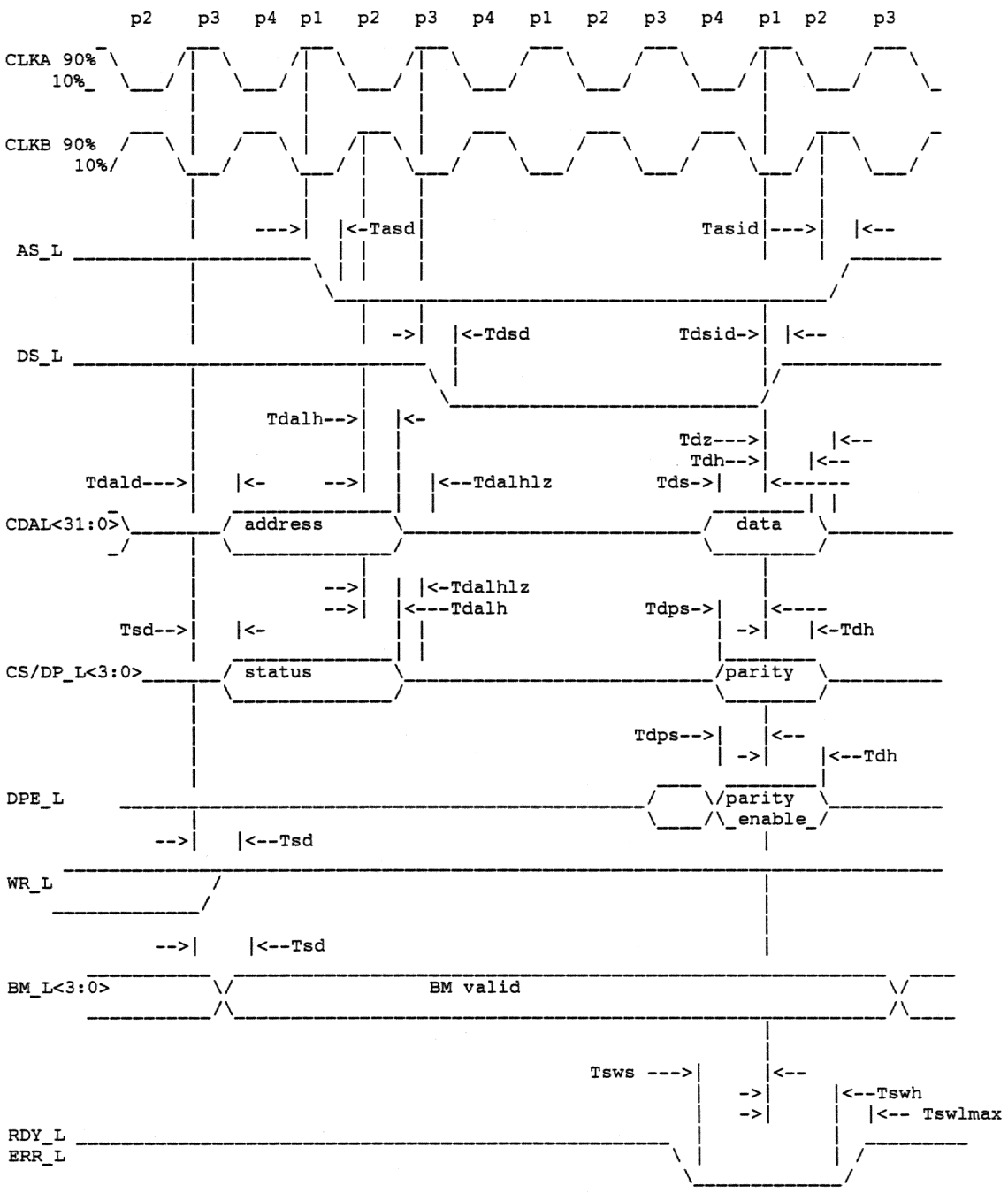


Figure 9–9 Cont'd. on next page

Figure 9–9 (Cont.) Single Transfer SGEC read Cycle

Whenever ERR_L is asserted, DS_L and AS_L remain asserted one additional cycle before the deassertion.

In asynchronus mode, the SGEC waits one additional cycle before starting the next transfer.

Table 9–13 Single Transfer SGEC read Cycle timing table

Symbol	Definition	Min	Max	Units
Tasd	AS strobe assertion delay	0	13.5	ns
Tasid	AS strobe deassertion delay	0	18	ns
Tdsd	DS strobe assertion delay	0	18	ns
Tdsid	DS strobe deassertion delay	0	18	ns
Tdalh	CDAL hold	4.5		ns
Tdald	CDAL drive	0	18	ns
Tdalhlz	CDAL tri-state	0	18	ns
Tdz	Required CDAL tri-state	40		ns
Tdh	Required CDAL hold	4		ns
Tds	Required CDAL setup	20		ns
Tdps	Required Parity setup	16		ns
Tsd	General strobe assertion delay	0	18	ns
Tsws	RDY/ERR sample window setup	13.5		ns
Tswh	RDY/ERR sample window hold	4.5		ns
Tswlmax	RDY/ERR maximum assertion		36	ns

9.5.3 Octaword Transfer SGEC Read Cycle

In an octaword transfer SGEC read cycle, the SGEC reads four longwords (quadword) from main memory. An octaword transfer SGEC read cycle requires a minimum of eighteen clock phases (nominally 240 ns) and may last longer. Each longword transfer may be independently stretched in increments of two clock phases (nominally 80 ns).

Figure 9–10 Octaword Transfer SGEC Read Cycle

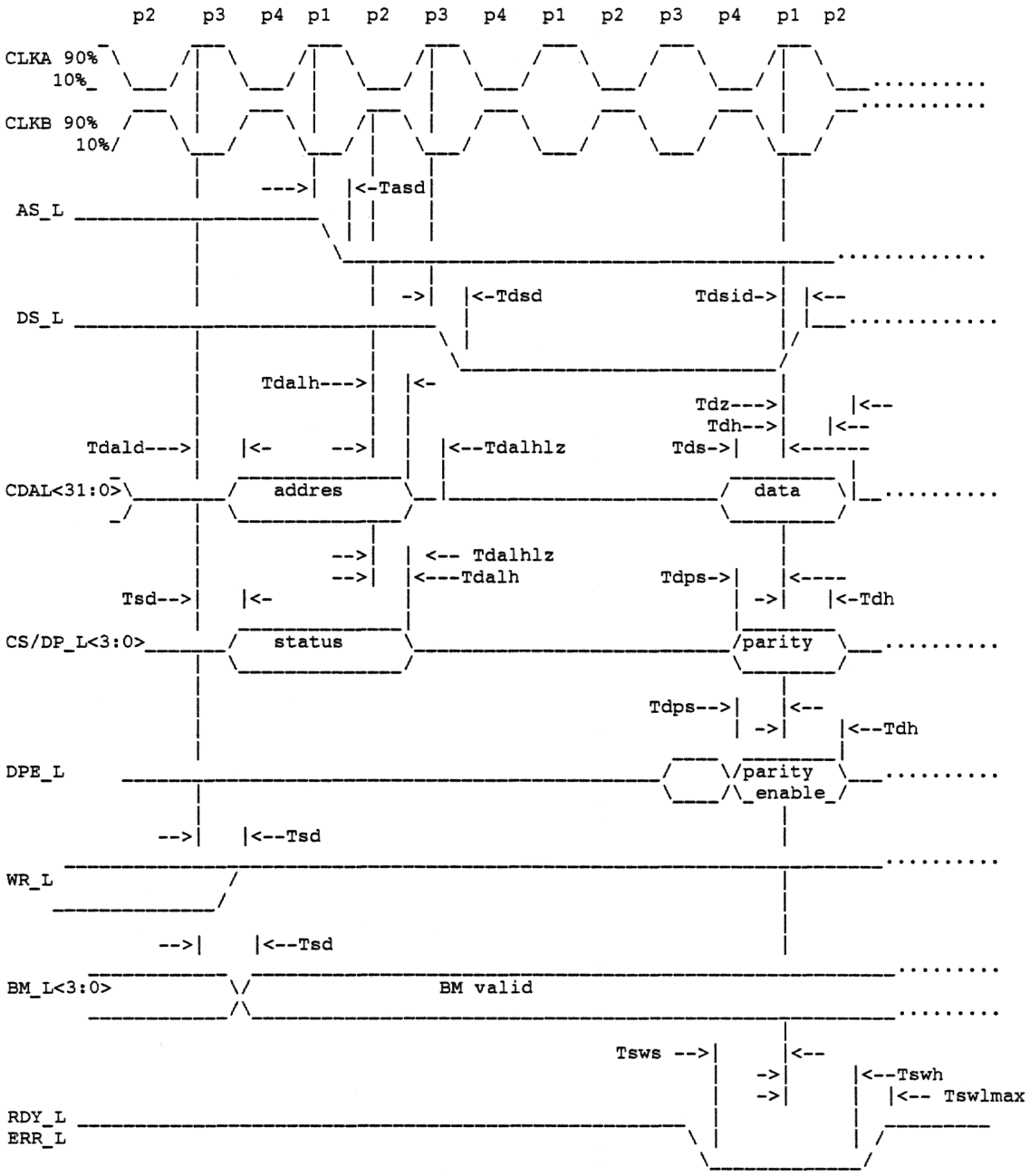
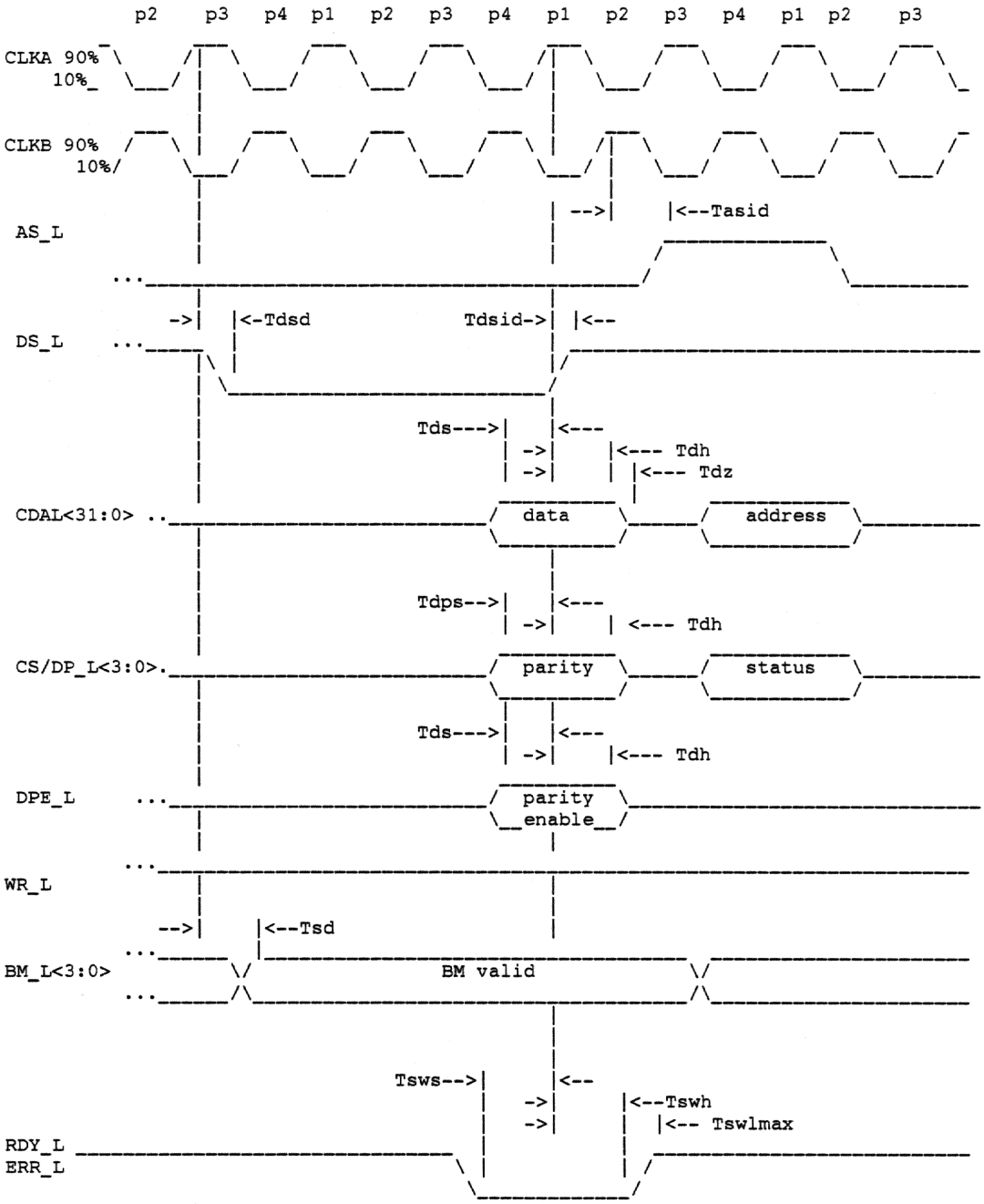


Figure 9–10 Cont'd. on next page

Figure 9–10 (Cont.) Octaword Transfer SGEC Read Cycle



Whenever ERR_L is asserted, DS_L and AS_L remain asserted one additional cycle before the deassertion.

In asynchronus mode, the SGEC waits one additional cycle before starting the next transfer.

Table 9–14 Octaword Transfer SGEC Read Cycle timing table

Symbol	Definition	Min	Max	Units
Tasd	AS strobe assertion delay	0	13.5	ns
Tasid	AS strobe deassertion delay	0	18	ns
Tdsd	DS strobe assertion delay	0	18	ns
Tdsid	DS strobe deassertion delay	0	18	ns
Tdalh	CDAL hold	4.5		ns
Tdald	CDAL drive	0	18	ns
Tdalhlz	CDAL active drive delay	0	18	ns
Tdz	Required CDAL tri-state	40		ns
Tdh	Required CDAL hold	4		ns
Tds	Required CDAL setup	20		ns
Tdps	Required Parity setup	16		ns
Tsd	General strobe assertion delay	0	18	ns
Tsws	RDY/ERR sample window setup	13.5		ns
Tswh	RDY/ERR sample window hold	4.5		ns
Tswlmax	RDY/ERR maximum assertion		36	ns

9.5.4 Single Transfer SGEC Write Cycle

In a single transfer SGEC write cycle, the SGEC writes one longword to the main memory. A single transfer write cycle requires a minimum of four clock phases (nominally 160 ns) and may last longer, in increments of two clock phases (nominally 80 ns).

Figure 9–11 Single Transfer SGEC write Cycle

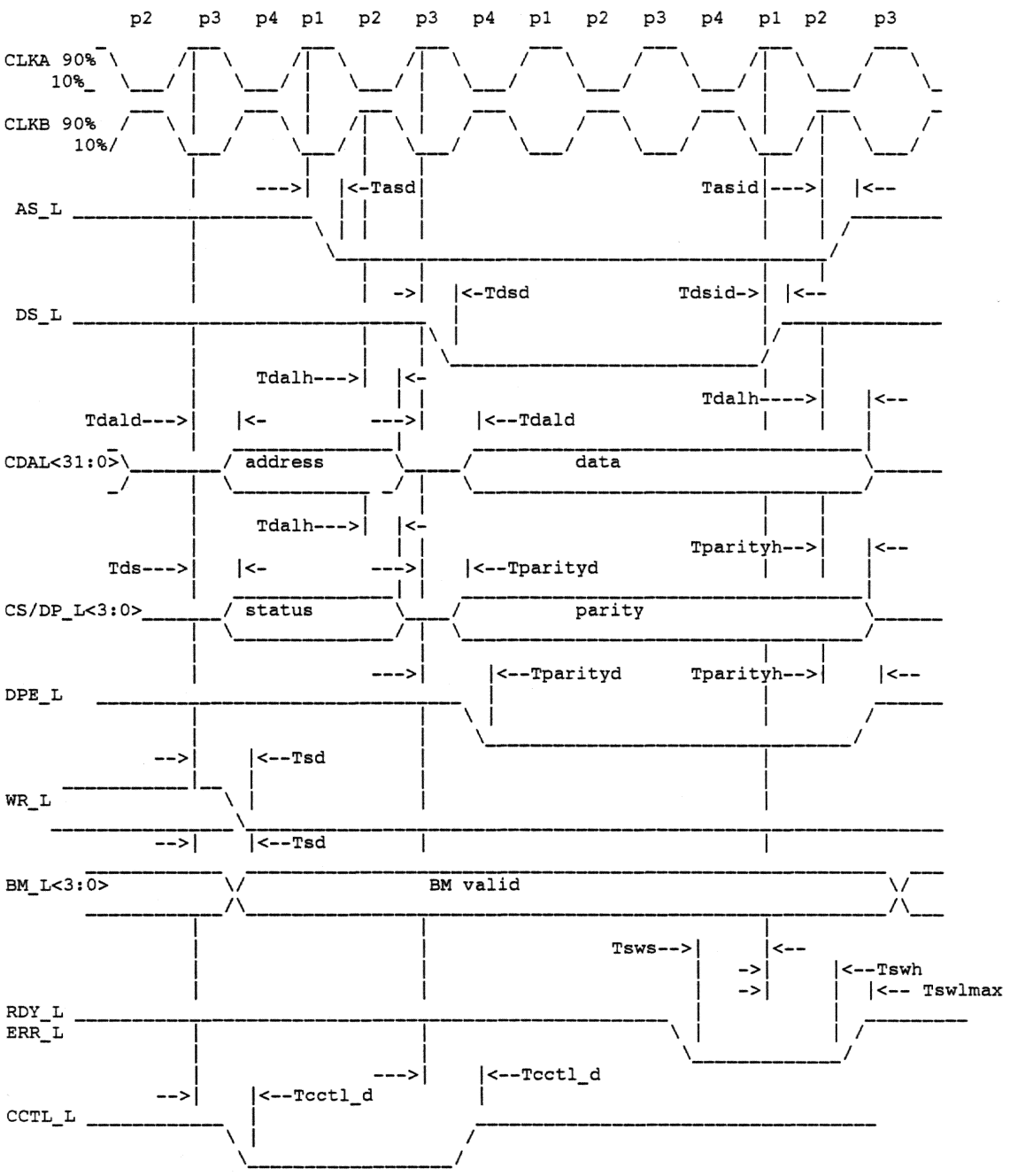


Figure 9–11 Cont'd. on next page

Figure 9–11 (Cont.) Single Transfer SGEC write Cycle

Whenever ERR_L is asserted, DS_L and AS_L remain asserted one additional cycle before the deassertion.

In asynchronus mode, the SGEC waits one additional cycle before starting the next transfer.

Table 9–15 Single Transfer SGEC write Cycle timing table

Symbol	Definition	Min	Max	Units
Tasd	AS strobe assertion delay	0	13.5	ns
Tasid	AS strobe deassertion delay	0	18	ns
Tdsd	DS strobe assertion delay	0	18	ns
Tdsid	DS strobe deassertion delay	0	18	ns
Tdalh	CDAL hold	4.5		ns
Tdald	CDAL drive	0	18	ns
Tdalhlz	CDAL active drive delay	0	18	ns
Tparity_d	Parity delay	0	30	ns
Tparity_h	Parity hold	4.5		ns
Tsd	General strobe assertion delay	0	18	ns
Tcctl_d	CCTL_L delay	0	18	ns
Tsws	RDY/ERR sample window setup	13.5		ns
Tswh	RDY/ERR sample window hold	4.5		ns
Tswlmax	RDY/ERR maximum assertion		36	ns

9.5.5 Octaword Transfer SGEC Write Cycle

In an octaword transfer SGEC DMA write cycle, the SGEC writes four longwords (quadword) to main memory. An octaword transfer SGEC write cycle requires a minimum of eighteen clock phases (nominally 240 ns) and may last longer. Each longword transfer may be independently stretched in increments of two clock phases (nominally 80 ns).

Figure 9–12 Octaword Transfer SGEC Write Cycle

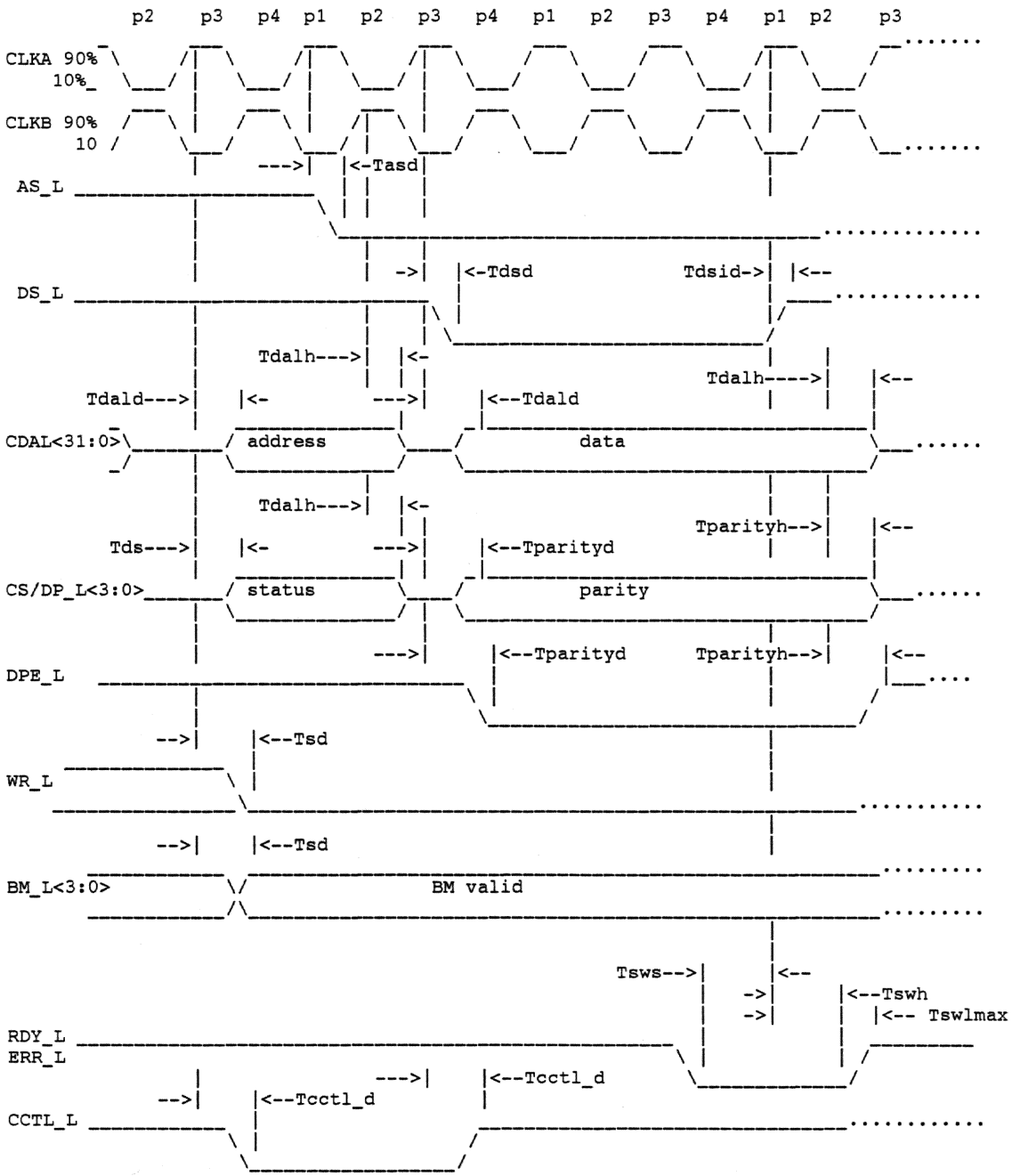
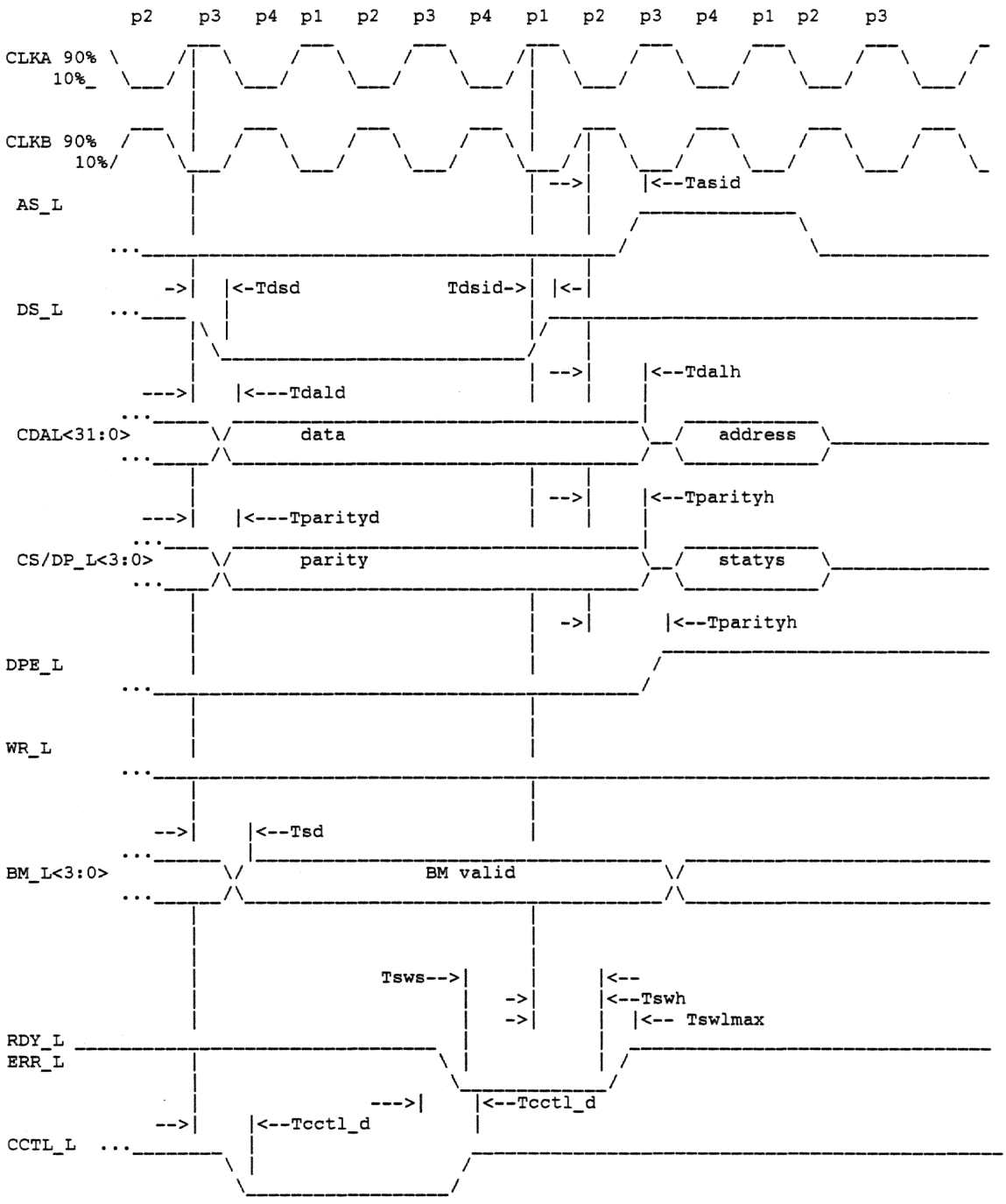


Figure 9–12 Cont'd. on next page

Figure 9–12 (Cont.) Octaword Transfer SGEC Write Cycle



Whenever ERR_L is asserted, DS_L and AS_L remain asserted one additional cycle before the deassertion. CCTL_L is reasserted when DS_L asserts for the third longword.

In asynchronus mode, the SGEC waits one additional cycle before starting the next transfer.

Table 9–16 Octaword Transfer SGEC Write Cycle timing table

Symbol	Definition	Min	Max	Units
Tasd	AS strobe assertion delay	0	13.5	ns
Tasid	AS strobe deassertion delay	0	18	ns
Tdsd	DS strobe assertion delay	0	18	ns
Tdsid	DS strobe deassertion delay	0	18	ns
Tdalh	CDAL hold	4.5		ns
Tdald	CDAL drive	0	18	ns
Tdalhlz	CDAL active drive delay	0	18	ns
Tparity_d	Parity delay	0	30	ns
Tparity_h	Parity hold	4.5		ns
Tsd	General strobe assertion delay	0	18	ns
Tcctl_d	CCTL delay	0	18	ns
Tsws	RDY/ERR sample window setup	13.5		ns
Tswh	RDY/ERR sample window hold	4.5		ns
Tswlmax	RDY/ERR maximum assertion		36	ns

9.6 SGEC serial interface timing

****
QUALIFICATION: These are all PRELIMINARY timing parameters.
****

This paragraph specifies the serial interface timing. The serial clock is nominally a 10Mhz square wave.

9.6.1 Receive clock and Transmit clock timing

Figure 9–13 Receive clock timing

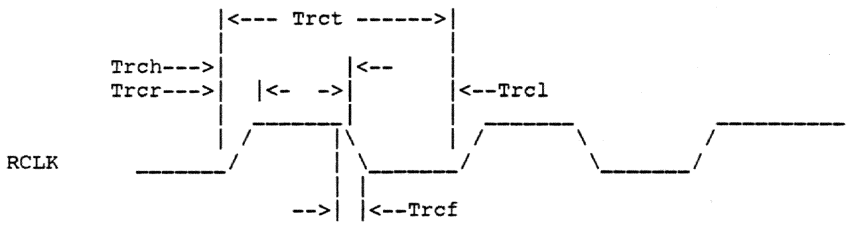
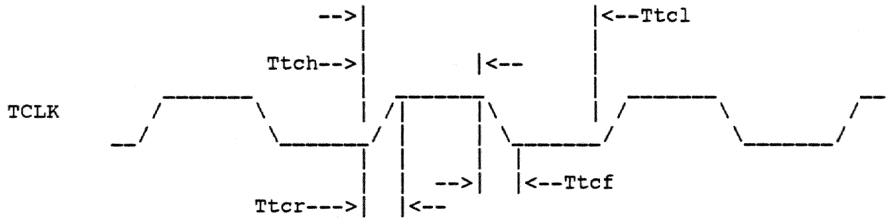


Figure 9–14 Receive clock and Transmit clock timing



This table show the specified timing characteristics for the Transmit and receive clocks.

Table 9–17 Transmit and Receive clock Timing

Symbol	Definition	Min	Typ	Max	Units
Trct	RCLK cycle time	82	100	118	ns
Trch	RCLK high time	38	50		ns
Trcl	RLCK low time	38	50		ns
Trcr	RCLK rise time	0	2.5	8	ns
Trcf	RCLK fall time	0	2.5	8	ns
Ttct	TCLK cycle time	99	100	101	ns
Ttcl	TCLK low time	45	50	55	ns

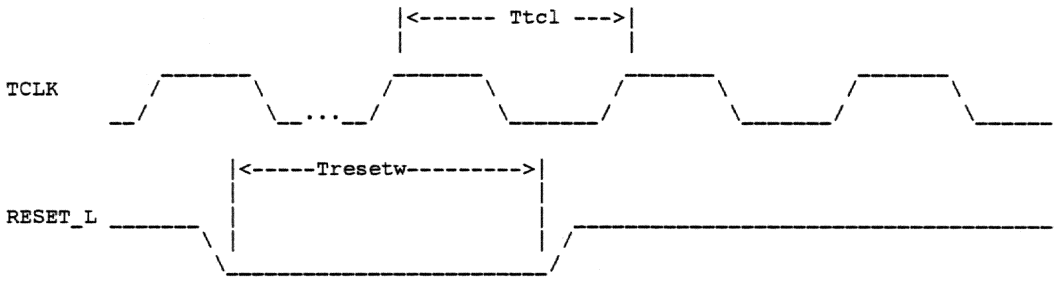
Table 9–17 (Cont.) Transmit and Receive clock Timing

Symbol	Definition	Min	Typ	Max	Units
Ttch	TCLK high time	45	50	55	ns
Ttcr	TCLK rise time	0	2.5	8	ns
Ttcf	TCLK fall time	0	2.5	8	ns

9.6.2 SGEC RESET pin timing

This input supplies the Reset timing signal to the chip. CLKA and CLKB must be supplied while assertion of RESET_L.

Figure 9–15 SERIAL RESET Timing



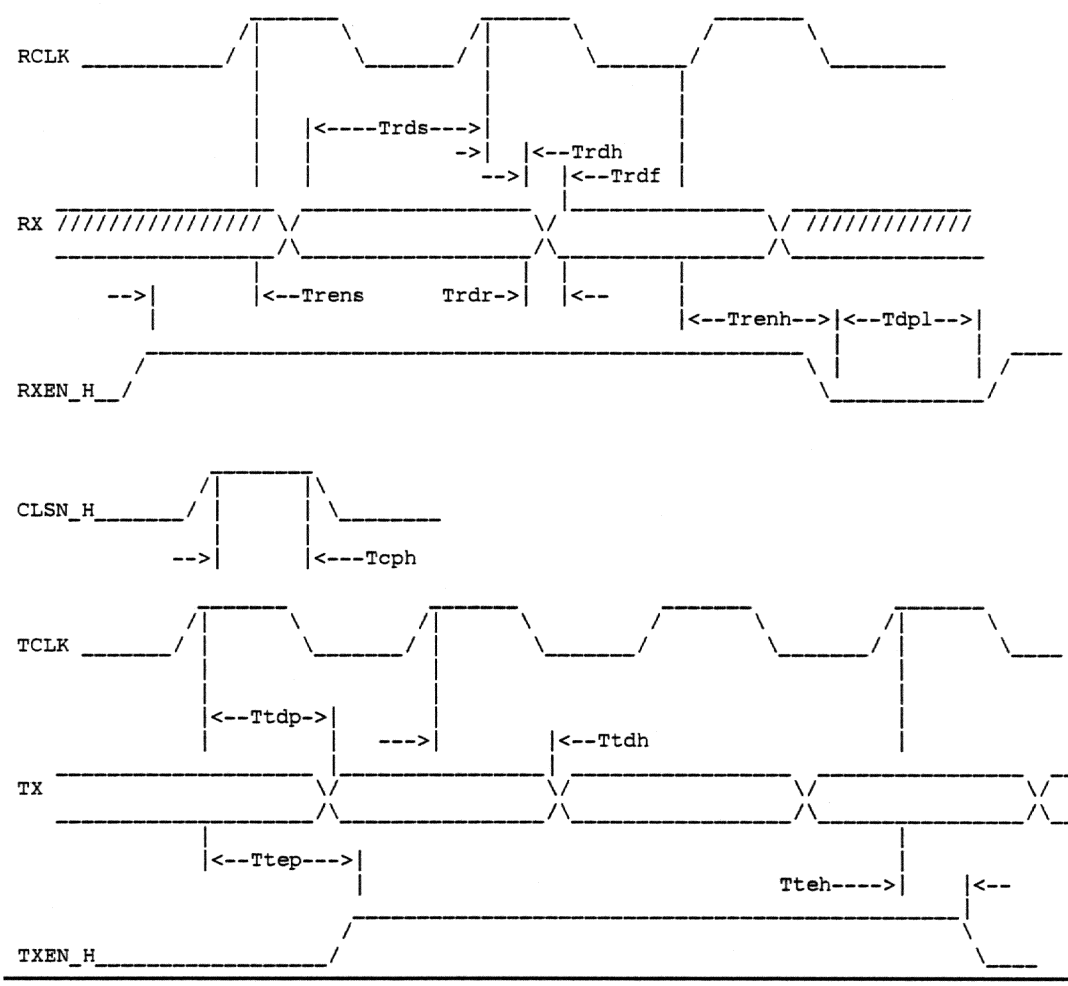
This table list the SERIAL reset timing

Table 9–18 SGEC RESET Timing

Symbol	Definition	Min	Max	Units
Tresetw	Reset assertion width	4Ttcl = 400		ns
Ttcl	TCLK cycle time	99	101	nS

9.6.3 Serial link timing

Figure 9–16 Serial link timing



This table show the specified timing characteristics for the SGEC clock inputs.

Table 9–19 Serial link Timing

Symbol	Definition	Min	Max	Units
Ttep	TXEN propogation delay		95	ns
Tteh	TXEN hold time	5		ns
Ttdp	TX propogation delay		95	ns
Ttdh	TX hold time	5		ns
Trdr	RX data rise time	0	8	ns
Trdf	RX data fall time	0	8	ns
Trdh	RX data hold time	5		ns
Trds	RX data setup time	60		ns
Tdpl	RXEN low time	120		ns
Tcph	CLSN high time	80		ns
Trens	RXEN setup time	40		ns
Trenh	RXEN hold time	40		ns

9.6.4 SGEC timing for 100ns and 60ns clock cycles

Table 9-20 SGEC timing - 100ns

Symbol	Definition	Min	Max	Units
Tclke	External clock edge rate	0	10.0	ns
Tcycle	External clock cycle	50.0	TBS	ns
Tclkh	External clock high	15.0	25.0	ns
Tclkl	External clock low	15.0	25.0	ns
Tclkdly	Clock A to clock B delay	23.0	27.0	ns
Tresetw	Reset assertion width	8*Tcycle		ns
Tresetd	Strobe inactive delay from reset	0	150	ns
Tresetz	Bus tristate time from reset	0	150	ns
Tresets	Reset input setup prior to p1	20	Tcycle - 12	nS
Tas_hw	AS high	60		ns
Tas_lw	AS low	300	400	ns
Tasi_h	Address,WR,BM,CS to AS hold time	12.5		ns
Tasi_s	Address,WR,BM,CS to AS setup time	20		ns
Tas_ds_l	AS to DS delay	50		ns
Tds_hw	DS high	120		ns
Tds_lw	DS low	175	275	ns
Tds_as_l	DS to AS delay	0		ns
Tds_d_h	DS to DATA,Parity	0		ns
Tds_rdy_d	DS to RDY delay	125	225	ns
Tds_r_d	DS to RDY deassertion delay	0	27.5	
Tiake_d	IAKEI to IAKEO assertion delay	175	425	ns
Tds_d_d	DS to DATA delay		25	ns
Tds_d_h	DS to DATA hold time	0		ns
Tas_nsgec_a	AS to NSGEC assertion delay	125	225	ns
Tas_nsgec_d	AS to NSGEC deassertion delay		25	ns
Tnsgec_lw	NSGEC assertion width	125	325	ns
Tdmrd	DMR delay	0	22.5	ns
Tsyns	Asynchronousr input setup	15		ns
Tsynh	Asynchronous input hold	15		ns
Tsynf	Asynchronous input fall time		15	ns
Tasd	AS strobe assertion delay	0	16	ns
Trshlz	Required tri-state		0	ns
Trdalhlz	Required CDAL tri-state		0	ns
Tasid	AS strobe deassertion delay	0	20	ns
Tasz	Tri-state delay		50	ns
Treldlz	CDAL tri-state		20	

Table 9–20 (Cont.) SGEC timing - 100ns

Symbol	Definition	Min	Max	Units
Tdsd	DS strobe assertion delay	0	20	ns
Tdsid	DS strobe deassertion delay	0	20	ns
Tdalh	CDAL hold	5		ns
Tdald	CDAL drive	0	20	ns
Tdalhlz	CDAL tri-state	0	20	ns
Tdz	Required CDAL tri-state	50		ns
Tdh	Required CDAL hold	5		ns
Tds	Required CDAL setup	25		ns
Tdps	Required Parity setup	20		ns
Tsd	General strobe assertion delay	0	20	ns
Tsws	RDY/ERR sample window setup	15		ns
Tswds	RDY/ERR deassertion setup	5		ns
Tswh	RDY/ERR sample window hold	5		ns
Tswlmax	RDY/ERR maximum assertion		45	ns
Tparity_d	Parity delay	0	37.5	ns
Tparity_h	Parity hold	5		ns
Tcctl_d	CCTL delay	0	22.5	ns

Table 9–21 SGEC timing - 60ns

Symbol	Definition	Min	Max	Units
Tclke	External clock edge rate	0	6.0	ns
Tcycle	External clock cycle	30.0	TBS	ns
Tclkh	External clock high	9.0	15.0	ns
Tclkl	External clock low	9.0	15.0	ns
Tclkdly	Clock A to clock B delay	13.5	16.5	ns
Tresetw	Reset assertion width	8*Tcycle		ns
Tresetd	Strobe inactive delay from reset	0	90	ns
Tresetz	Bus tristate time from reset	0	90	ns
Tresets	Reset input setup prior to p1	14	Tcycle - 8	nS
Tas_hw	AS high	37.5		ns
Tas_lw	AS low	180	240	ns
Tasi_h	Address,WR,BM,CS to AS hold time	8		ns
Tasi_s	Address,WR,BM,CS to AS setup time	13.5		ns
Tas_ds_l	AS to DS delay	30		ns
Tds_hw	DS high	75		ns
Tds_lw	DS low	105	165	ns
Tds_as_l	DS to AS delay	0		ns
Tds_d_h	DS to DATA,Parity	0		ns
Tds_rdy_d	DS to RDY delay	75	135	ns
Tds_r_d	DS to RDY deassertion delay	0	16.5	
Tiake_d	IAKEI to IAKEO assertion delay	103	257	ns
Tds_d_d	DS to DATA delay		17	ns
Tds_d_h	DS to DATA hold time	0		ns
Tas_nsgec_a	AS to NSGEC assertion delay	75	135	ns
Tas_nsgec_d	AS to NSGEC deassertion delay		17	ns
Tnsgec_lw	NSGEC assertion width	75	195	ns
Tdmrd	DMR delay	0	13.5	ns
Tsyns	Asynchronousr input setup	9		ns
Tsynh	Asynchronous input hold	9		ns
Tsynf	Asynchronous input fall time		9	ns
Tasd	AS strobe assertion delay	0	10	ns
Trshlz	Required tri-state		0	ns
Trdalhlz	Required CDAL tri-state		0	ns
Tasid	AS strobe deassertion delay	0	13.5	ns
Tasz	Tri-state delay		30	ns
Treldlz	CDAL tri-state		13.5	
Tdsd	DS strobe assertion delay	0	13.5	ns
Tdsid	DS strobe deassertion delay	0	13.5	ns

Table 9–21 (Cont.) SGEC timing - 60ns

Symbol	Definition	Min	Max	Units
Tdalh	CDAL hold	4		ns
Tdald	CDAL drive	0	13.5	ns
Tdalhlz	CDAL tri-state	0	13.5	ns
Tdz	Required CDAL tri-state	30		ns
Tdh	Required CDAL hold	3		ns
Tds	Required CDAL setup	15		ns
Tdps	Required Parity setup	12		ns
Tsd	General strobe assertion delay	0	13.5	ns
Tsws	RDY/ERR sample window setup	10		ns
Tswds	RDY/ERR deassertion setup	4		ns
Tswh	RDY/ERR sample window hold	4		ns
Tswlmax	RDY/ERR maximum assertion		27	ns
Tparity_d	Parity delay	0	22.5	ns
Tparity_h	Parity hold	4		ns
Tcctl_d	CCTL delay	0	13.5	ns

A References

1 William Stallings. Local Networks. Macmillan Publishing Company - May 1984

2 Computer Networks. Prentice Hall Inc - April 1981

3 Introduction to local area networks. Digital Press - Edited 1982

4 Network - a description of Digital LAN support. Digital Press - Edited 1982

5 G. R. Davis. The Local Network Handbook. McGraw Hill - May 1982

6 DEC Standard 134 B - 1988

7 The Ethernet Blue Book. Intel, Xerox and Digital - May 1982

8 The IEEE 802.3 Standard. IEEE 802.* Committee - 1985

9 AMD 7900 Data Sheet. AMD - Edited 1984

10 AMD 7902 Data Sheet. AMD - Edited 1984

11 The CVAX data sheet

12 The CMCTL data sheet

13 The CCLK data sheet

14 80386 CPU data sheet. Intel - 1986

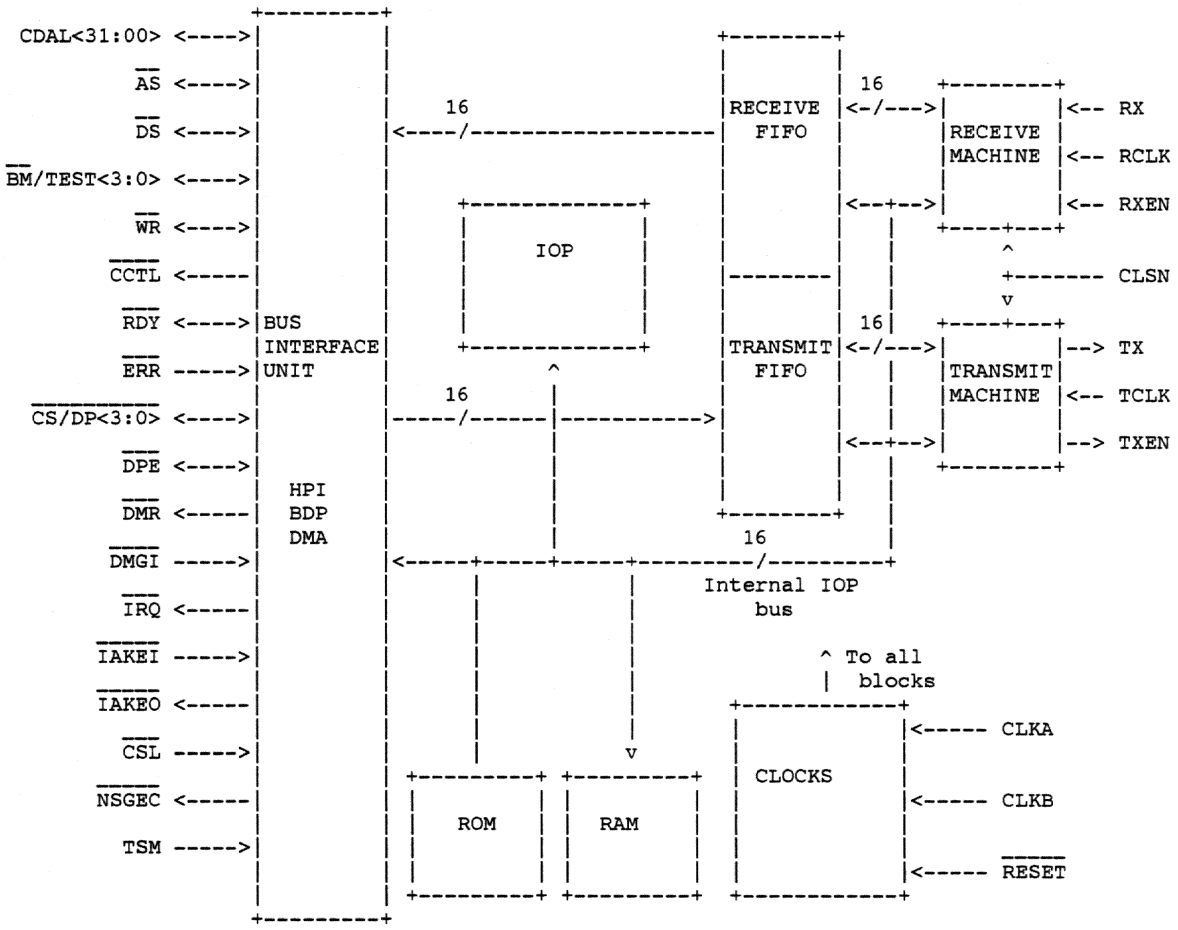
B SGEC internal block diagram

The following is a list of the main blocks in the SGEC:

Short name	Name	Description
HPI	Host Pin Interface	A bus interface unit which takes care of all internal signals for interfacing to the host system bus.
BDP	Bus Data Path Unit	Data path interface unit which passes the data between the internal and external buses.
DMA	Direct Memory Access Unit	3 DMA channels which control the transfer of data between the SGEC and main memory. One RX channel, one TX channel and one control channel. The channels can operate with either physical or virtual addresses.
RAM	Code RAM	A 256 word RAM for control and status bits, and special purpose logic for supporting and testing the internal CPU.
IOP	Processor	An internal 16 bit processor which controls the internal operation of the device, the DMA initialization and the buffer management.
ROM	Code ROM	A 3K word ROM storing the internal code.
FIFO	FIFO	Two 120 byte deep, word-organized, first-in-first-out (FIFO) memories. One stores data to be transmitted and the other stores data that has been received.
RXM	Receive Machine	An interface between the serial line and the Receive data FIFO. The RXM is in charge of the data link layer functions such as Address recognition and filtering, CRC check framing and packet decapsulation.
TXM	Transmit machine	An interface between the serial line and Transmit Data FIFO. The TXM is in charge of the frame generation and CRC generation.

SGEC internal block diagram

Figure B–1 SGEC Block Diagram



C Open issues

Table C-1 summarizes the open issues for the pass2 part:

Table C-1 Open issues

Issue	Explanation
Received IEEE frames	Currently, the SGEC ignores the IEEE Data Length field, except when programmed to strip pad/CRC. An incoming frame whose actual length does not match the Data Length field is not truncated nor error flagged. Is this acceptable?
MOP BOOT message	Should the SGEC detect the MOP BOOT message and optionally trigger a reboot?
Separate Receive and Transmit interrupts	LANBridge request to expedite processing.
Global VAX memory addressing	Currently not supported, should it be?