pdp11

DUV11
line interface
technical manual

digital

EK-DUV11-TM-001

DUV11
line interface
technical manual

digital equipment corporation • maynard, massachusetts

Preliminary Edition, April 1977
1st Edition, August 1977

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

CONTENTS

Page

CHAPTER 1 INTRODUCTION

1.1 SCOPE 1-1
1.2 DATA COMMUNICATION TECHNIQUES 1-1
1.2.1 Pulse Coding 1-1
1.2.2 Pulse Code Transmission 1-1
1.2.2.1 Asynchronous Serial Transmission 1-2
1.2.2.2 Synchronous Serial Transmission 1-3
1.2.2.3 Isochronous Serial Transmission 1-4
1.3 COMMUNICATION SYSTEMS 1-4
1.3.1 Synchronous Systems 1-4
1.3.2 Computer Application 1-6
1.4 GENERAL DESCRIPTION 1-6
1.5 SPECIFICATIONS 1-8
1.5.1 Environmental 1-8
1.5.2 Electrical 1-9
1.5.3 Performance 1-9
1.5.3.1 Baud Rates for Synchronous Communications 1-9
1.5.3.2 Baud Rates for Isochronous Communications 1-9
1.6 ENGINEERING DRAWINGS 1-9
1.6.1 Basic Signal Names 1-9
1.6.2 Flip-Flop Signal Names 1-10

CHAPTER 2 INSTALLATION

2.1 INSTALLATION 2-1
2.1.1 Mounting the DUV11 in the Computer 2-1
2.1.2 Installing the Modem Cable Harness 2-2
2.1.3 Installing DUV11 to Null Modem 2-3
2.1.4 Q BUS and Interrupt Vector Address Assignments 2-6
2.1.5 Jumper Functions 2-7
2.1.6 Option Switches 2-8
2.2 INITIAL TESTING 2-8

CHAPTER 3 DEVICE REGISTERS AND INTERRUPT REQUESTS

3.1 SCOPE 3-1
3.2 DEVICE REGISTERS 3-1
3.2.1 Register Address Assignments 3-1
3.2.2 Register Title and Bit Assignments 3-1
3.2.2.1 Title Assignments 3-1
3.2.2.2 Bit Assignments 3-2
3.3 INTERRUPT REQUESTS 3-12

CONTENTS (CONT)

CHAPTER 4 THEORY OF OPERATION

4.1 SCOPE 4-1
4.2 INITIALIZATION AND PROGRAMMING 4-1
4.3 OVERALL DATA FLOW 4-1
4.4 FUNCTIONAL BLOCK DESCRIPTION 4-2
4.4.1 Address Comparator and Command Decoder 4-2
4.4.2 Data Multiplexer 4-2
4.4.3 Modem Interface Logic 4-2
4.4.4 Receiver Logic 4-2
4.4.5 Transmitter Logic 4-5
4.4.6 Interrupt Control Logic 4-5
4.5 DETAILED FUNCTIONAL DESCRIPTION 4-5
4.5.1 Address Comparator (Engineering Drawing D1) 4-5
4.5.2 Command Decoder (DC004 Chip as Shown on Engineering Drawing D1) 4-5
4.5.3 Data Multiplexer (Engineering Drawing D2) 4-5
4.5.4 Modem Interface Logic 4-5
4.5.5 Receiver Control Logic 4-6
4.5.6 Transmitter Control Logic 4-13
4.5.7 Interrupt Control Logic 4-19
4.5.8 Clear Logic 4-19
4.5.9 Clock Control Logic 4-19
4.5.10 +12 to -12 Power Converter 4-19
4.5.11 Maintenance Indicators 4-19

CHAPTER 5 PROGRAMMING REQUIREMENTS AND RECOMMENDATIONS

5.1 INTRODUCTION 5-1
5.2 PROGRAMMING THE TRANSMITTER IN THE SYNCHRONOUS MODE 5-1
5.2.1 Loading the PARCSR 5-1
5.2.2 Handshaking Sequence 5-1
5.2.3 Enabling the Transmitter 5-3
5.2.4 Detecting the Last Character of the Message 5-3
5.2.5 Transmitting Initial Sync Characters to Establish Synchronization 5-4
5.2.6 Transmitting Sync Characters to Maintain Synchronization 5-4
5.3 PROGRAMMING THE RCVR IN THE INTERNAL SYNCHRONOUS MODE 5-5
5.4 PROGRAMMING THE RCVR IN THE EXTERNAL SYNCHRONOUS MODE 5-6
5.5 PROGRAMMING THE XMTR IN THE ISOCHRONOUS MODE 5-6
5.5.1 Loading the PARCSR 5-6
5.5.2 Enabling the XMTR 5-6
5.6 PROGRAMMING THE RCVR IN THE ISOCHRONOUS MODE 5-6

CONTENTS (CONT)

CHAPTER 6 MAINTENANCE

6.1 SCOPE 6-1
6.2 MAINTENANCE PHILOSOPHY 6-1
6.3 PREVENTIVE MAINTENANCE 6-1
6.4 TEST EQUIPMENT REQUIRED 6-1
6.5 CORRECTIVE MAINTENANCE 6-1
6.5.1 Maintenance Modes 6-2
6.5.1.1 System Test Mode 6-2
6.5.1.2 Internal Loop Mode 6-2
6.5.1.3 External Loop Mode 6-7

APPENDIX A REPRESENTATIVE MODEM FACILITIES AVAILABLE

APPENDIX B LSI INTEGRATED CIRCUIT DESCRIPTIONS

B.1 INTRODUCTION B-1
B.2 PR1472B SYNCHRONOUS RECEIVER (P/SAR) B-1
B.2.1 Synchronous Mode Operation B-9
B.3 PT1482B SYNCHRONOUS TRANSMITTER (P/SAT) B-11
B.3.1 Synchronous Mode Operation B-11
B.4 DC003 INTERRUPT CHIP B-21

APPENDIX C INTEGRATED CIRCUITS

FIGURES

Figure No.	Title	Page
1-1	Asynchronous Technique Format	1-2
1-2	Synchronous Format	1-3
1-3	Typical Communications System	1-7
1-4	DUV11 (M7951) Major Components	1-8
1-5	Flip-Flop Signal Names	1-10
2-1	DUV11-DA Mounted in H9270	2-1
2-2	BC05C-25 Cable Harness	2-2
2-3	DUV11 to Modem Connection	2-3
2-4	DUV11 to Null Modem Connection	2-3
2-5	Null Modem Connector (H312A)	2-4
2-6	Null Modem (H312A) Jumper Connections	2-5
2-7	Modem Test Connection Installation	2-9
3-1	DUV11 Register Configurations and Bit Assignments	3-2
3-2	Receiver Status Register (RXCSR)	3-3
3-3	Receiver Data Buffer (RXDBUF)	3-6
3-4	Parameter Status Register (PARCSR)	3-8
3-5	Transmitter Status Register (TXCSR)	3-9

FIGURES (CONT)

3-6 Transmitter Data Buffer (TXDBUF) 3-12
4-1 DUV11 Functional Block Diagram 4-3
4-2 Receiver Internal Timing Diagram 4-7
4-3 Receiver External Synchronous Timing Diagram 4-9
4-4 Receiver Isochronous Timing Diagram 4-11
4-5 Transmitter Synchronous Timing Diagram 4-15
4-6 Transmitter Isochronous Timing Diagram 4-17
4-7 External Loop Maintenance Mode Interconnection Diagram 4-20
5-1 DUV11 to Modem Interface Diagram 5-2
5-2 Handshaking Sequence Timing Diagram 5-2
6-1 Maintenance Diagram 6-3
B-1 PR1472B Programmable Synchronous Receiver (P/SAR) B-1
B-2 P/SAR Pin Connections B-2
B-3 Synchronous Timing Example (P/SAR) B-10
B-4 PT1482B Programmable Synchronous Transmitter (P/SAT) B-12
B-5 P/SAT Pin Connections B-12
B-6 Synchronous Timing Example (P/SAT) B-19
B-7 DC003 Logic Symbol Diagram B-21
B-8 DC003 Timing Diagram (Section A Only) B-25
B-9 DC003 Timing Diagram (Sections A & B) B-27

TABLES

Table No.	Title	Page
1-1	Representative Message Codes	1-4
1-2	Computer Communications Applications	1-6
2-1	Signal List for Jumper Connections of Null Modem H312A	2-5
2-2	Guide for Setting Switches to Select Device Address	2-6
2-3	Guide for Setting Switches to Select Vector Address	2-7
2-4	Switch Assignments	2-8
3-1	DUV11 Register Address Assignments	3-1
3-2	Receiver Status Register Bit Description	3-4
3-3	Receiver Data Buffer Bit Description	3-7
3-4	Parameter Status Register Bit Description	3-8
3-5	Transmitter Status Register Bit Description	3-10
3-6	Transmitter Data Buffer Bit Description	3-12
6-1	Test Equipment Required	6-2
B-1	P/SAR Signal Mnemonics	B-3
B-2	P/SAR Signals	B-4
B-3	Sync Mode Control Definition	B-10
B-4	P/SAT Signal Mnemonics	B-13
B-5	P/SAT Signals	B-14
B-6	SYNC Mode Control Definitions	B-20
B-7	DC003 Signals	B-22

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual provides a complete description of the DUV11 Line Interface including installation, theory of operation, programming and maintenance. The material is presented with the understanding that the reader is familiar with basic digital computer theory.

This chapter contains introductory information. Data communication techniques and systems are discussed. The DUV11 is presented in terms of its general and physical description and specifications. Also, an explanation of engineering drawing conventions is provided.

1.2 DATA COMMUNICATION TECHNIQUES

There are several techniques used for the transfer of data communication signals. Each has its particular advantages and disadvantages.

1.2.1 Pulse Coding

Standard data communication messages are sent in some form of pulse code. There are several varieties of pulse codes used in the transferral of data in digital form. Binary signals, by their very nature, are natural elements for digital data codes. Such codes are said to be in binary format.

A formatted binary code can represent different symbols only by allowing sufficient binary elements for each symbol. If we think of one binary digit (or bit) representing each symbol, we have only two choices: one symbol represented by the on state, the other represented by the off state. With such an arrangement, we could let the on or one state represent no and the off or zero state represent yes. While it would be difficult with such an arrangement, we could convey messages of a very limited nature from a remote station (such as the answer to "Is the temperature at your station over 70° F?").

If, instead of using one binary digit for our character, we use two, we have more characters to choose from. Our choice for a 1-bit code was limited to two: 0 or 1. Our choice for a 2-bit code is four: 00, 01, 10, or 11. If we choose a 3-bit code, our choice is eight: 000, 001, 010, 011, 100, 101, 110, and 111. It can be shown that for a code with a character makeup of n bits, the number of characters available will be 2^n.

In communications parlance, instead of calling these codes 1-bit codes, 2-bit codes, etc., they are called 1-level codes, 2-level codes, etc. Although any arbitrary meaning can be assigned to a code character, it is more practical for the majority of operations to let the characters represent numbers, punctuation marks, spaces, and letters of the alphabet. In addition to these, some special codes use characters for other meanings.

1.2.2 Pulse Code Transmission

In order to transmit code characters, it is necessary to arrange their elements in a way that will allow their reception without uncertainty.

There are two basic techniques of serial data transmission: asynchronous and synchronous. These two techniques, as well as a third, isochronous, will be discussed in the following paragraphs.

1.2.2.1 Asynchronous Serial Transmission – This technique enables data to be transferred as it becomes available. This is possible by framing each data character with a begin signal (START bit) and an end signal (STOP bit), so that the equipment receiving the data (the interface receiver) knows when a data character is being presented on the communication line and when the line is inactive.

Hence, each character consists of three parts: a START bit, the data bits, and a STOP bit (Figure 1-1). A START bit is a line state (usually a zero) that lasts for 1 bit time. The data bits represent the actual binary character being transferred. In many applications the characters are 8 bits long with the least significant bit being sent out and received first. A STOP bit is a line state (usually a one) that lasts for 1, 1.42, or 2 bit times; it indicates that character transmission is complete. The STOP bit enables the interface receiver to check synchronization after each character transmission. If the STOP bit is not received properly, i.e., it is not presented on the line immediately after the last data bit, the character received is considered erroneous and retransmission is necessary.

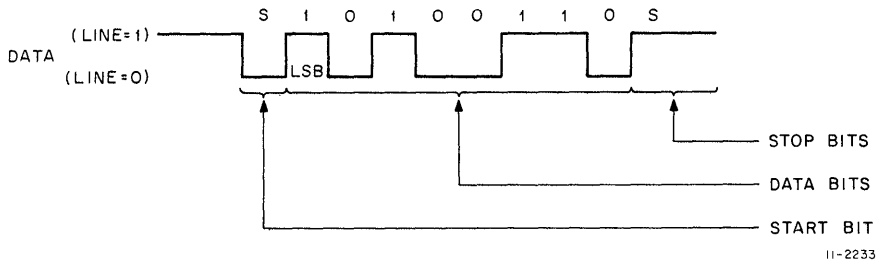


Figure 1-1 Asynchronous Technique Format

Clocking for the interface transmitter and interface receiver during asynchronous transmission is provided by two different sources that are asynchronous to one another. The transmitter clock is enabled when data is available for transmission and clocks the character onto the line. The receiver clock is enabled when a START bit is detected on the line and samples the data bits as they are presented on the line. The receiver is also equipped with a counter that counts the character bits received. When a complete character and a STOP bit are received (the receiver must know the number of bits per character), the receiver clock is disabled until the next START bit is detected.

The asynchronous serial data transmission technique has the following advantages:

1. Can be generated easily by electromechanical equipment (e.g., Teletype® keyboard)
2. Can be used easily to drive mechanical equipment (e.g., Teletype printer)
3. Characters can be sent asynchronously (as they become available) because each character has its own synchronizing information.

The disadvantages of the asynchronous serial transmission technique are:

1. Separate timing is required for both transmitter and receiver.
2. It is distortion sensitive because the receiver depends on incoming signal sequences to become synchronized. Any distortion in these sequences will affect the reliability with which the character is assembled

®Teletype is a registered trademark of Teletype Corporation

3. Speed is limited because a reasonable margin between characters must be built-in to accommodate distortion.

4. It is inefficient because at least 10 bit times are required to send 8 bits of data. If a 2 bit time STOP bit is used, it takes 11 bit times to transfer 8 bits of data.

1.2.2.2 Synchronous Serial Transmission – This technique does not use START and STOP bits to accomplish synchronization. Instead, the entire block of data (message) is preceded on the line by a synchronizing code. When the interface receiver recognizes this code (henceforth referred to as sync characters), it locks in and, using a counter, assembles the data characters which follow. Hence, as in the asynchronous technique, the receiver must know the number of bits per character.

This technique requires that the clock for the interface transmitter be identical to the clock used at the receiver. The clock signal is provided to the transmitter and receiver on lines separate from the data line. At the transmitter, the clock signal serves to clock the data onto the line. At the receiver, the clock signal gates the data in. Figure 1-2 illustrates the timing for a synchronous communication system using modems.

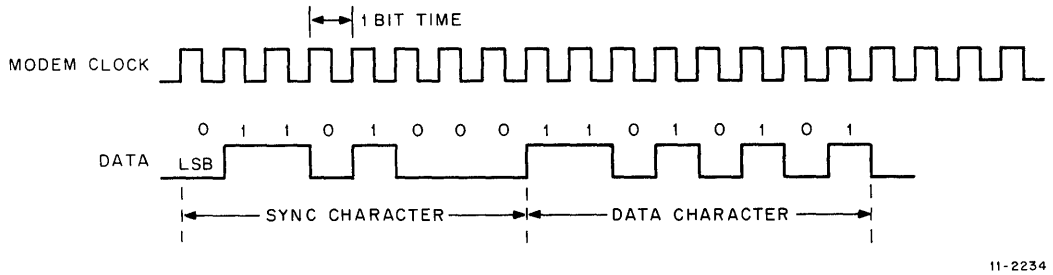


Figure 1-2 Synchronous Format

As shown in Figure 1-2, the modem provides the clock, the transmitter presents the data to the line on the positive going edge of the clock, and the receiver samples the data on the negative going edge. If the transmitter pauses at any time and fails to inhibit the clock, the receiver will continue to sample the line, synchronization is lost, and the remainder of the message will be erroneous.

The advantages of the synchronous serial data transmission technique are:

1. Modem timing sources can be used for both transmitter and receiver.

2. If modem timing is used, interface receiver does not require clock-synchronizing logic as does the asynchronous technique.

3. It is highly efficient because there are no bit times wasted with the use of START and STOP bits. All bits on the line are data with the exception of the sync characters at the beginning of the bit stream.

4. Low distortion sensitivity because the timing is provided along with the data.

5. Higher speeds are achievable because of the low distortion sensitivity.

The disadvantages of the synchronous serial data transmission technique are:

1. Characters must be sent synchronously, not asynchronously (asynchronous transmission is desirable for most real-time and mechanical applications).

2. One bit time added to or missing from the data-bit stream can cause the entire message to be faulty.

3. The common-carrier equipment required to accommodate this mode of operation is more expensive than the equipment required for asynchronous modes of operation.

4. Mechanical equipment cannot transmit or receive this format directly.

1.2.2.3 Isochronous Serial Transmission – This technique is essentially the transmission of asynchronous data over a synchronous modem. Character synchronization is achieved via START and STOP bits; a common timing source is used for both the transmitter and receiver.

The isochronous technique does have advantages over the asynchronous technique. Clocking for isochronous operations emanates from the modems and is synchronous to the data; hence, the receiver does not require clock-synchronizing logic and distortion sensitivity is low, making higher speeds possible.

1.3 COMMUNICATION SYSTEMS

1.3.1 Synchronous Systems – Synchronous modulator-demodulators (modems) have permitted a higher rate of data transmission than asynchronous modems over a voice grade facility. The nature of these transmission techniques has also resulted in higher efficiency by eliminating the need for synchronizing information with every character.

Most synchronous modems supply all the timing necessary to receive each bit as it is made available from the modem. The difficulty in designing a synchronous modem interface is to design the capability of communicating in the message formats used in synchronous communications.

Table 1-1 Representative Message Codes

Character	Meaning	Function
**SYN	Synchronizing signal	Establish character framing
**SOH	Start of heading signal	Precedes block message heading characters
**STX	Start of text signal	Precedes block of text characters
**ETX	End of text signal	Terminates a block of characters started with STX
**ACK	Acknowledge signal	*Affirmative acknowledgment of message received
**NAK	Negative acknowledge signal	*Negative acknowledgment of message received

*ACK and NAK are sent by the station that received the message to the station that originated the message.
**Software protocol

It is not the purpose of this manual to discuss the format for synchronous communication in detail. However, a brief description of these formats is outlined to facilitate the reader's understanding of synchronous interface design.

Because the synchronous transmission technique provides only bit recovery timing, there must be a way to establish character framing and message framing. This is accomplished by using codes (usually ASCII) that are assigned for synchronous message formatting purposes. Representative message codes are listed in Table 1-1.

A typical message that might be sent between two devices (a terminal and a processor) follows.

Terminal To Processor

SYN
SYN
SYN
SOH

User Terminal
No. 4

STX

Req. Balance
of Account
No. 14325

ETX
BCC (check character)

Idle Line

Processor To Terminal

SYN
SYN
SYN
ACK
SYN
SYN
SYN
SOH

To Terminal
No. 4

STX

Balance is
$100

ETX
BCC (check character)

Idle Line

Terminal To Processor

SYN
SYN
SYN
ACK

Idle Line

1.3.2 Computer Application – Electronic computers are often connected into communication systems to help transmit and process digital data. By using computer systems to concentrate data from many low-speed terminals over one voice grade facility, significant improvements can be made in the efficiency of a data communication system. Since most long-range communication systems are connected through common carrier facilities, a communication system using a computer should be interfaced to the correct type facility. There are two basic types of common carrier facilities to which computers must be interfaced: asynchronous serial and synchronous serial. We have already pointed out the advantages and disadvantages of these two types of facilities. Table 1-2 shows typical speeds and applications of these two techniques based on these advantages and disadvantages.

As shown in Table 1-2, there are three basic communication applications to be solved by the computer communications engineer:

Low speed terminal equipment, such as Teletypes
Medium speed terminal equipment
Intercomputer communications.

Table 1-2 Computer Communications Applications

Speed	Asynchronous	Synchronous
Low 0 to 300 baud	Electromechanical terminals such as keyboard printers and teletypes.	Operations tend to be asynchronous at these speeds.
Medium 300 to 3000 baud	Unbuffered terminals such as paper tape readers and punches, card readers and line printers.	Buffered terminals such as displays, buffered card readers, and line printer configurations.
High 5000 baud and up	Not frequently used.	Intercomputer communications.

1.4 GENERAL DESCRIPTION

The DUV11 is a single line, program controlled, double buffered communication interface. The purpose of this interface is to establish a data communication line between an LSI-11 computer (a parallel input/output device) and a Bell 201 or equivalent modem (a serial input/output device). The DUV11 provides serial-to-parallel and parallel-to-serial data conversion, EIA*-to-TTL (transistor-transistor logic) and TTL-to-EIA voltage level conversion and modem control for full or half duplex communication systems.

The DUV11 is compatible with all LSI-11 family computers and the Bell 201 synchronous modem or equivalent. DUV11-DA is the only version and is completely contained on the M7951 quad integrated circuit module. This module can be easily mounted in any standard LSI-11 series backplane. A typical communication system using the DUV11 is shown in Figure 1-3.

Interface operation is entirely program controlled. The mode of operation (synchronous or isochronous), character length (5, 6, 7, or 8 bits plus parity if selected), parity enable and sense (odd or even), sync character configuration, and duplex mode (full or half) are all selected via the program.

*EIA RS232C – A standardized set of signal characteristics (time duration, voltage, and current) specified by the Electronic Industries Association.

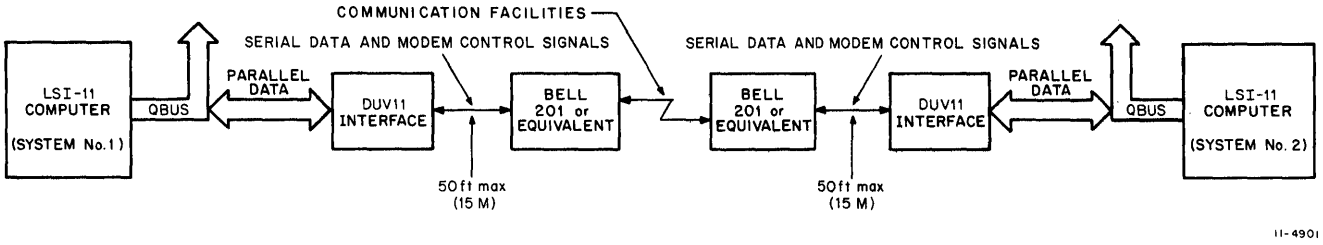


Figure 1-3 Typical Communications System

The interface has the following capabilities:

1. Handles synchronous and isochronous communication data
2. Operates in half duplex or full duplex mode
3. Handles variable length characters (5, 6, 7, or 8 bits plus parity)
4. Generates a parity bit (odd or even) which is transmitted with the data character to the modem
5. Verifies received character parity (odd or even)
6. Inhibits the transmitter data output for maintenance purposes
7. Controls the modem.

In line with these capabilities, the interface performs the following operations:

1. Converts parallel data inputs (from the computer) to serial data outputs (to the modem)
2. Converts serial data inputs (from the modem) to parallel data outputs (to the computer)
3. Inhibits receiver operation when transmitting in the half duplex mode
4. Establishes synchronization prior to allowing received data to be transferred to the computer
5. Provides control signals to the modem and monitors modem status lines
6. Generates interrupt requests to the program in response to any one of the following conditions:
    a. Synchronized data received from the modem
    b. Transmitter ready to accept another character for transmission
    c. Modem status change
    d. Sync (fill) character being transmitted to the modem.

All DUV11 operating power is provided by the mounting panel in which it is installed. For proper operation, the module requires +5 V at 1.2 A (max) and +12 V at 0.45 A (max).

The H9270 or equivalent mounting panel connects the DUV11 to the LSI-11 (Q BUS). All Q BUS input/output signals enter and leave the module via the mounting panel pins. Refer to Chapter 2 for Q BUS to mounting panel connection. Figure 1-4 shows the major DUV11 components; the rocker switches which are used to select the interface Q BUS address, the SAT (Synchronous/Asynchronous Transmitter) chips and option switches. (A complete description of the option switches is provided in Table 2-1.)

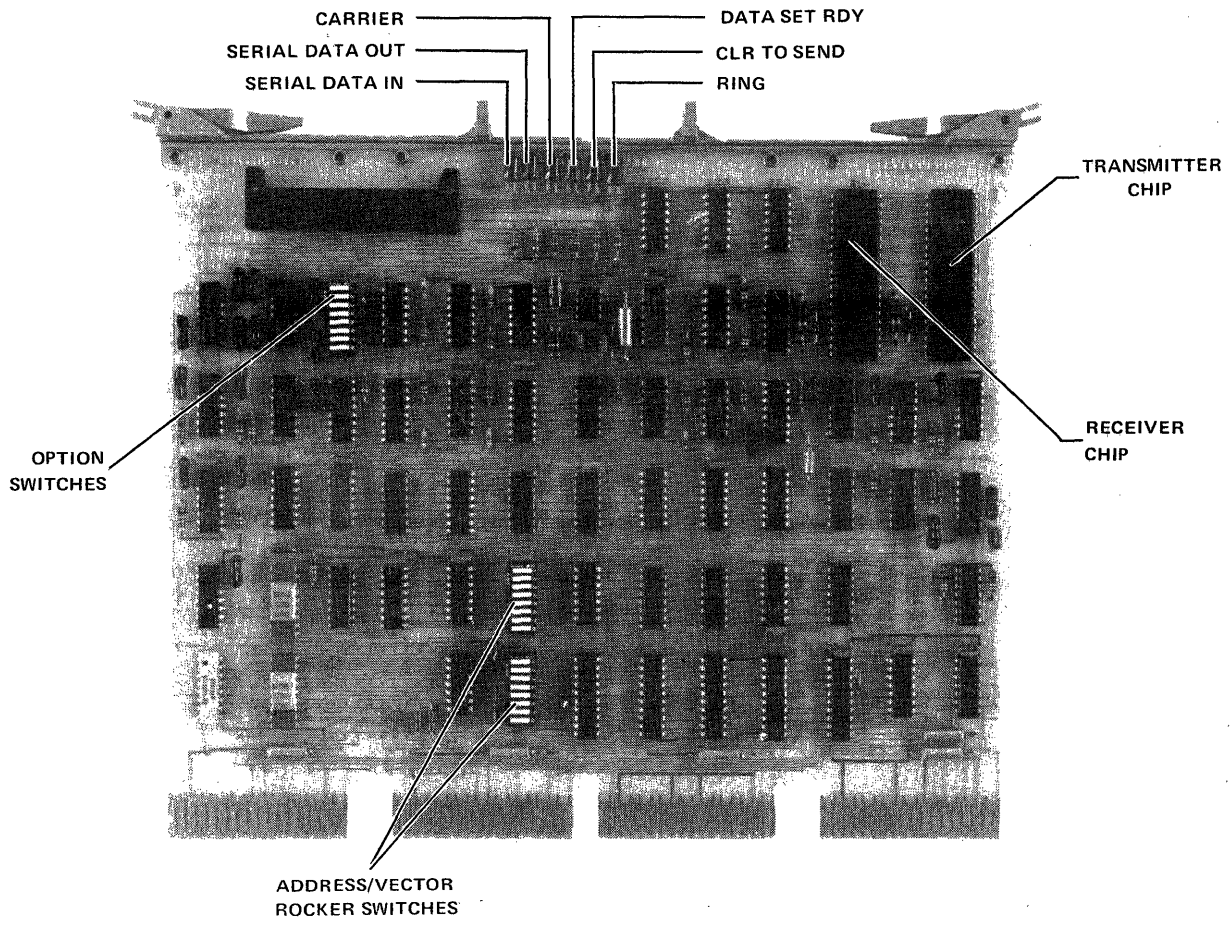


Figure 1-4 DUV11 (M7951) Major Components

1.5 SPECIFICATIONS

Environmental, electrical and performance specifications for the DUV11 are contained in the following paragraphs.

1.5.1 Environmental

Ambient temperature	5° to 50° C (41° to 122° F)
Relative humidity	10% to 95% (without condensation) with max wet bulb 32° C (90° F) and min dewpoint 2° C (36° F)

1.5.2 Electrical

DC voltage requirements	+5 V @ 1.2 A max +12 V @ 0.45 A max

Electrical characteristics

Electrical characteristics of this interface meet EIA standard RS-232C and LSI-11 Q BUS interface specifications.

1.5.3 Performance

The following paragraphs discuss the baud rate limitations of the DUV11 and related program response time.

1.5.3.1 Baud Rates for Synchronous Communications – EIA/CCITT* baud rate (10K baud maximum) is limited by modem and data set interface level converters. Even though the DUV11 can receive and transmit at a high rate, it may in most cases be impractical. Since the service of the data buffers relies solely on the program, little time, if any, would be left for other events. This problem would be compounded if the interface were operating in the full duplex mode.

1.5.3.2 Baud Rates for Isochronous Communications – EIA/CCITT baud rate (10K baud maximum) is limited by data set interface level converters.

1.6 ENGINEERING DRAWINGS

A complete set of engineering drawings is provided with each interface. The general logic symbols used on these drawings are described in the *DEC Logic Handbook*. Specific symbols and conventions are also included in the LSI-11 system manuals. The following paragraphs describe the signal nomenclature used in the drawing set.

1.6.1 Basic Signal Names

Signal names in the DUV11 print set are in the following form:

SOURCE (ASSERTION) SIGNAL NAME (STATE) POLARITY

SOURCE indicates the drawing number of the print from which the signal originates. The drawing number of a print is located in the lower right hand corner of the print title block (D1, D2, D3, D4, D5, and D6).

ASSERTION, normally blank (indicating true assertion), however the ~ (not, negate) symbol, may be used when appropriate.

SIGNAL NAME is the proper name of the signal. The names used on the print are also used in this manual for correlation between the two.

STATE is present when the signal source is a flip-flop, it is either (0) or (1).

POLARITY is either H or L to indicate the voltage level of the signal: H means +3 V; L means ground.

*CCITT – the Consultive Committee International Telegraph and Telephone is an advisory committee established under the United Nations to recommend worldwide standards.

For example, the signal

D5 TX DONE H

originates on sheet 5 of the drawings and is read "when TX DONE is true, this signal is at +3 V."

Q BUS signal lines carry a dual source indicator. These signal names represent a bidirectional wire-ORed bus; as a result multiple sources for a particular bus signal exist.

1.6.2 Flip-Flop Signal Names

Flip-flop signal names add an extra dimension. Although flip-flops have only two outputs, four signal names are possible (Figure 1-5). The two real outputs are RX DONE (1) H on pin 5 and RX DONE (0) H on pin 6. The two additional outputs are simply the two real outputs reidentified. RX DONE (1) L is electrically the same as RX DONE (0) H and RX DONE (0) L is electrically the same as RX DONE (1) H.

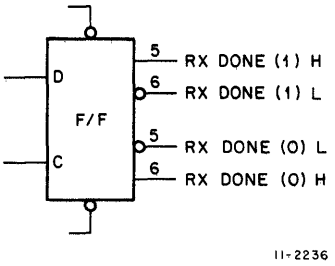


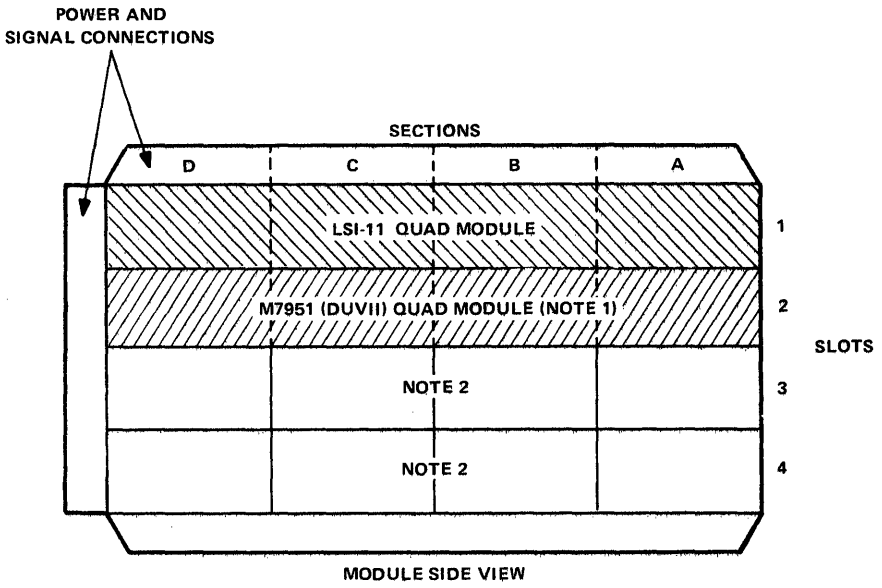
Figure 1-5 Flip-Flop Signal Names

CHAPTER 2
INSTALLATION

2.1 INSTALLATION

2.1.1 Mounting the DUV11 in the Computer

There is one DUV11 installation configuration. This is where the DUV11-DA interfaces with the Bell 201 synchronous modem or equivalent. In this configuration the DUV11-DA can be mounted in the H9270, H9273 or equivalent LSI-11 backplane (Figure 2-1).



NOTES:
1. Usually mounted in slot 2 but could be in slot 3 or 4.
2. LSI-11 options can be mounted in any section or sections of slots 3 and 4.

11-4902

Figure 2-1 DUV11-DA Mounted in H9270

2.1.2 Installing the Modem Cable Harness

The BC05C-25 cable harness (Figure 2-2) is used to connect the DUV11-DA to the Bell 201 modem. To install the cable, refer to Figure 2-3 and proceed as follows:

1. Position the Berg connector such that the connector name and pin number markings are visible and made fully and squarely with the Berg connector on the M7951 module.

2. Align the cinch connector to the receptacle located on the rear of the modem.

3. Mate the cinch connector and tighten the two hold-down screws using a flat blade screwdriver.

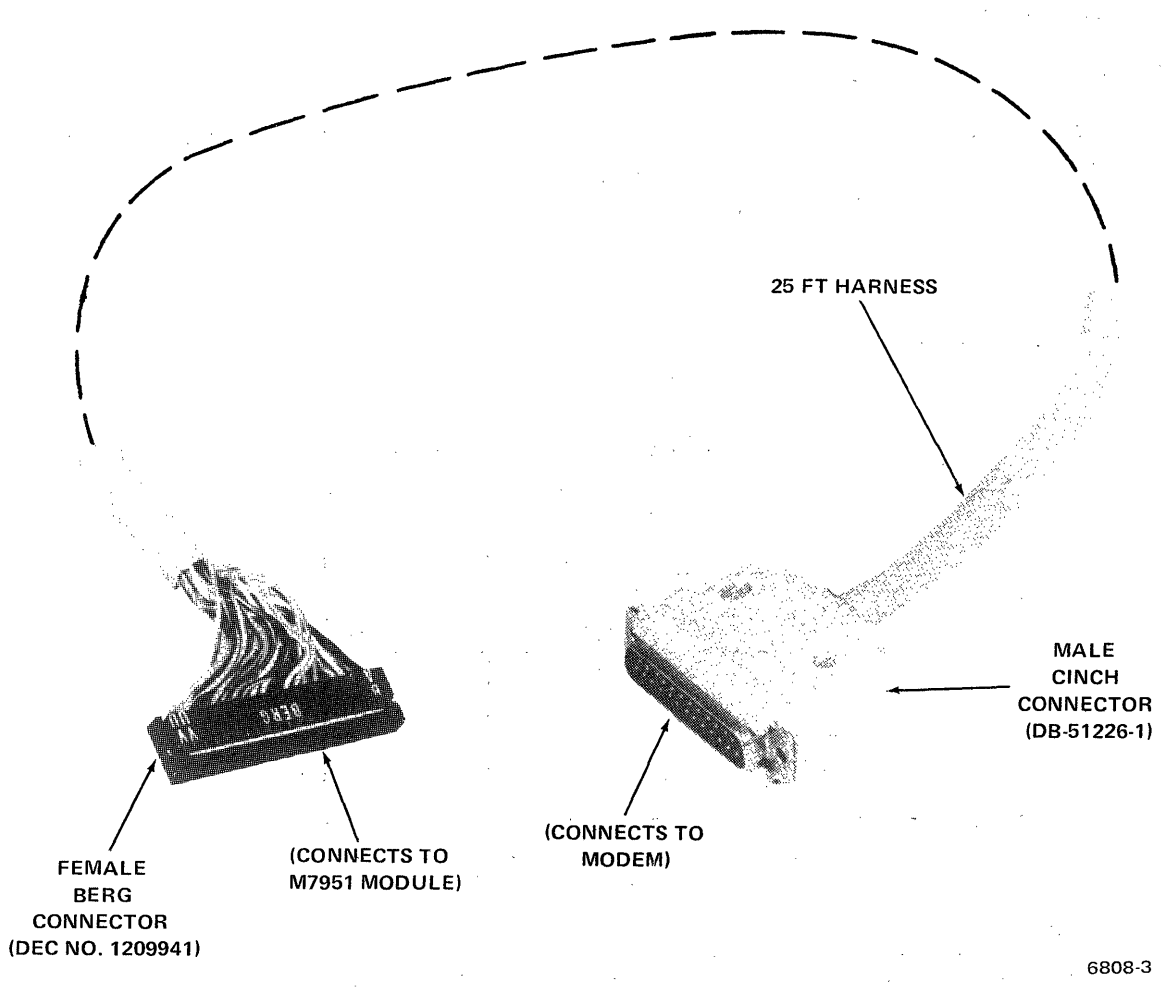


Figure 2-2 BC05C-25 Cable Harness

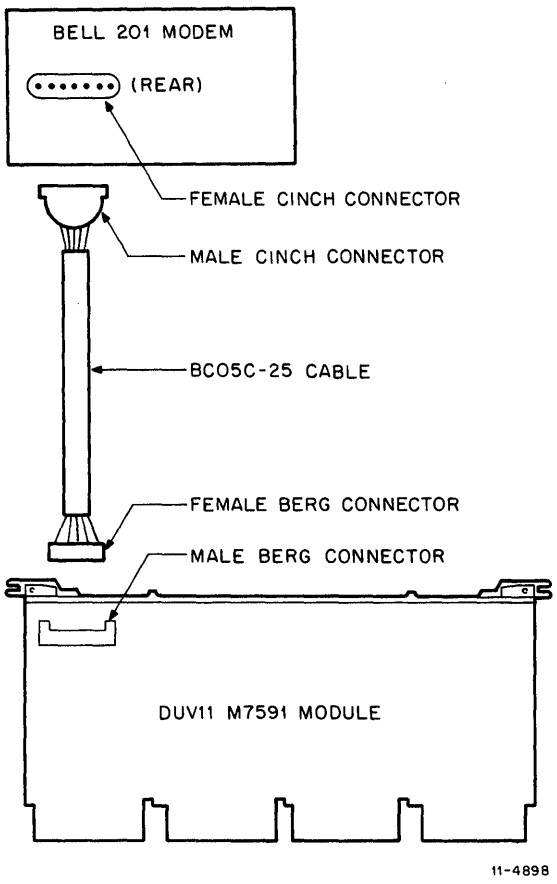


Figure 2-3 DUV11 to Modem Connection

2.1.3 Installing DUV11 to Null Modem

When running two systems back-to-back (without Bell 201), a null modem connector, part number H312A, is used. This set-up is shown in Figure 2-4.

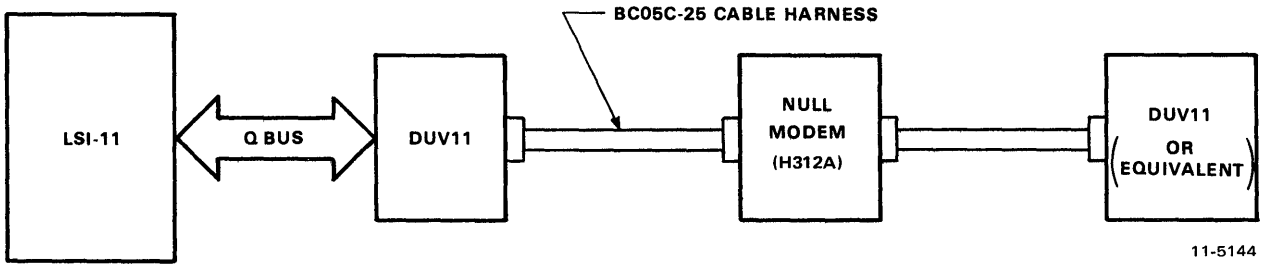


Figure 2-4 DUV11 to Null Modem Connection

The DUV11 connected to section A of the null modem (Figure 2-5) provides the clock source. This DUV11 has option switch 5 set to ON, and switch 7 set to OFF. Connection to section B of the null modem by other than a DUV11 is allowed providing the following is true:

1. The device only takes one DEC 1489 (IC type) input unit load each at the SCT and SCR leads.

2. The device must be compatible with the same series modem.

Jumper wires are connected as illustrated in Figure 2-6, and a jumper connection list is provided in Table 2-1.

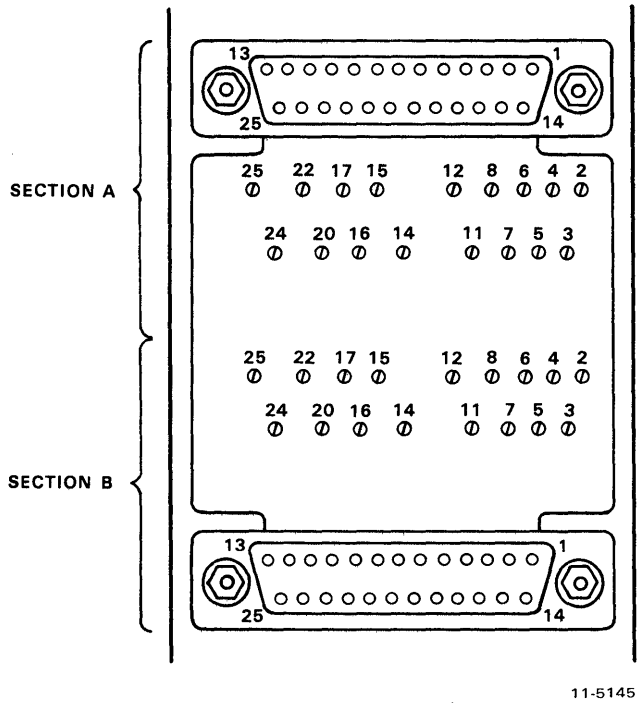


Figure 2-5 Null Modem Connector (H312A)

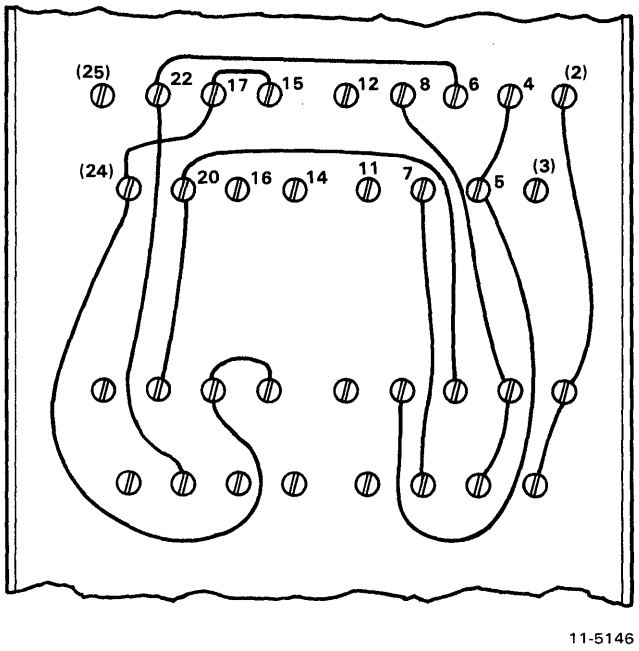


Figure 2-6 Null Modem (H312A) Jumper Connections

Table 2-1 Signal List for Jumper Connections of Null Modem H312A

Section A			Section B	
Signal	**Pin**		**Signal**	**Pin**
EXT CLK	24			
SCR	17	→	SCR	17
SCT	15	→	SCT	15
RING IND	22			
DSR	6	→	DTR	20
			RING IND	22
DTR	20	→	DSR	6
REQ TO SD	4			
CLR TO SD	5	→	CARRIER DET	8
			REQ TO SD	4
CARRIER DET	8	→	CLR TO SD	5
SIG GND	7	→	SIG GND	7
TRANS DATA	2	→	REC DATA	3
REC DATA	3	→	TRANS DATA	2
GND	1	→	GND	1 (connected internally)

2.1.4 Q BUS and Interrupt Vector Address Assignments

The Q BUS and interrupt vector addresses must be determined prior to operating the DUV11. The Q BUS address is switch selectable as are the interrupt vector addresses (Figure 1-4 for location).

The Q BUS address (also referred to as the device address) is controlled by ten rocker switches contained in two dip switch banks E38 and E39, located in the address comparator logic. The position of these switches determines the required address state (0 or 1) of bus address bits 12–03. If a rocker switch is set to ON the switch contacts are closed and an address state of 1 is required on the related address bit to address the DUV11. Hence, electrically the DUV11 can have any device address within the range of 760000 to 777777; however, Digital Equipment Corporation software requires that the device address fall within the floating address range of 760010 to 763776. The device address is set to 160010 (760010) at the factory to facilitate manufacturing testing. The switch setting for address selection is given in Table 2-2.

NOTE

If a device address is selected which falls outside the floating address range, the software must be modified accordingly.

Table 2-2 Guide for Setting Switches to Select Device Address

Module	E38								E39		
Switch No.	1	2	3	4	5	6	7	8	1	2	Device
Bit No.	12	11	10	9	8	7	6	5	4	3	Address
										ON	760010
									ON		760020
									ON	ON	760030
								ON			760040
								ON		ON	760050
								ON	ON		760060
								ON	ON	ON	760070
							ON				760100
						ON					760200
						ON	ON				760300
					ON						760400
					ON		ON				760500
					ON	ON					760600
					ON	ON	ON				760700
				ON							761000
			ON								762000
			ON	ON							763000
		ON									764000

NOTES

1. **ON means switch closed to respond to logical 1 on the Q BUS.**
2. **Switch numbers are physical in switch package at E38 and E39.**

The interrupt vector addresses are also floating and are set to 770_8 at the factory to facilitate manufacturing testing. If it is necessary to change the vector address, simply change the six vector select switches contained in one dip switch bank E39 as required. These switches control vector address bits 08–03, hence, vector addresses can be generated within the range of 000 to 774; however software requires that the vector address fall within the floating address range of 300 to 777. The switch setting for vector address selection is given in Table 2-3.

NOTE

If a vector address is selected which falls outside the floating address range, the software must be modified accordingly.

Table 2-3 Guide for Setting Switches to Select Vector Address

Switch No.	3	4	5	6	7	8	Vector
Bit No.	8	7	6	5	4	3	Address
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON		ON	350
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400
	ON		ON				500
	ON	ON					600
	ON	ON	ON				700

NOTES

1. **ON means switch closed to produce a logical 1 on the Q BUS.**
2. **Switch numbers are physical positions in switch package at E39.**

The address and vector selection switch banks E38 and E39 respectively are shown on engineering drawing D1.

2.1.5 Jumper Functions

Jumpers are used in the DUV11 to increase flexibility and to provide optional input/output points for the EIA signals via the backplane. This is an expansion feature and is not implemented to the basic DUV11-DA.

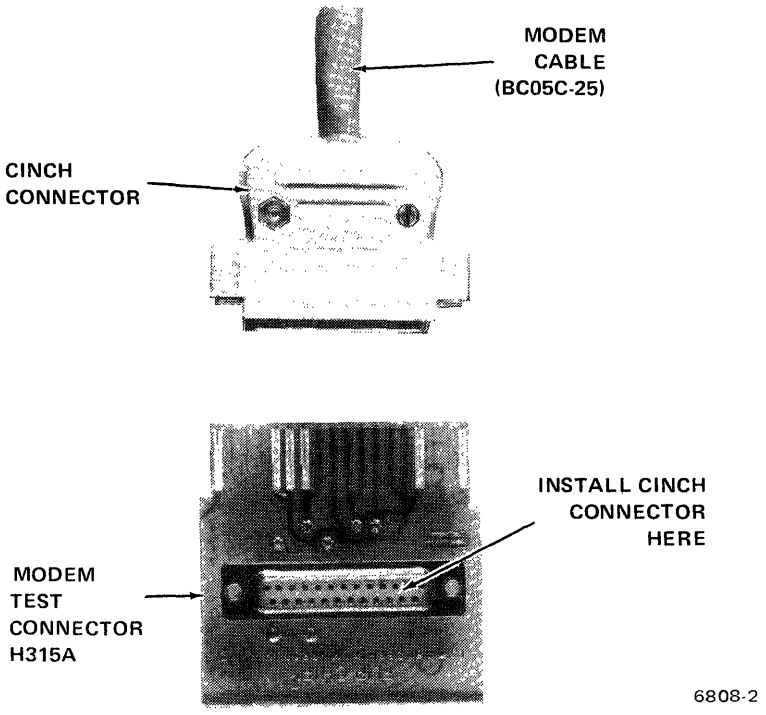


Figure 2-7 Modem Test Connection Installation

CHAPTER 3
DEVICE REGISTERS AND INTERRUPT REQUESTS

3.1 SCOPE

This chapter provides a complete description of the DUV11 device registers and the interrupt requests employed to service those registers.

3.2 DEVICE REGISTERS

All software control of the DUV11 is performed by means of five device registers. These registers have been assigned bus addresses and can be read or loaded (with the exceptions noted) using any LSI-11 instruction referring to their addresses. Address assignments can be changed via the rocker switches to correspond to any address within the floating address range of 160010 to 163776.

3.2.1 Register Address Assignments

The five device registers and associated DUV11 addresses are listed in Table 3-1. Note that these registers are byte addressable.

Table 3-1 DUV11 Register Address Assignments

Register	Mnemonic	Address	Program Capability
Receiver Status Register	RXCSR	16XXX0	Read/Write
Receiver Data Buffer	RXDBUF	16XXX2	Read Only
Parameter Status Register	PARCSR	16XXX2	Write Only
Transmitter Status Register	TXCSR	16XXX4	Read/Write
Transmitter Data Buffer	TXDBUF	16XXX6	Write Only

XXX = Selected in accordance with floating device address scheme.

3.2.2 Register Title and Bit Assignments

Each of the five device registers plays a specific role in controlling and monitoring DUV11 operation. Register titles, bit titles, and read/write capability labeling are intended to facilitate the programmer's understanding of the purpose of each register relative to interface operation and to simplify software preparation.

3.2.2.1 Title Assignments – Register titles and functions are listed below:

1. RXCSR – Programmed and monitored (read/write) to control the RCVR (receiver) portion of the interface; to communicate interface status, requests, and supervisory data to the modem; and to monitor status and supervisory data inputs from the modem.

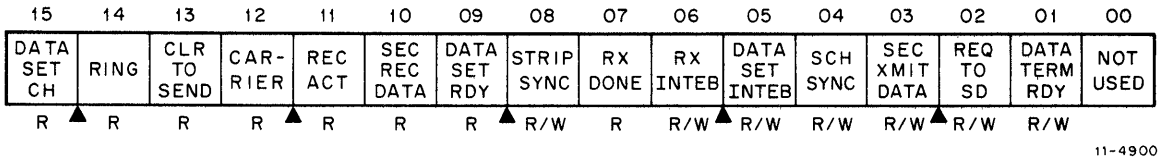
2. RXDBUF – Monitored (read only) to detect interface RCVR status flags and RCVR parallel data outputs.

3. PARCSR – Programmed (write only) to establish the overall operating parameters of the DUV11, i.e., the mode of operation (synchronous or isochronous), word length (5, 6, 7, or 8 bits plus parity), parity (enabled or disabled), parity sense (odd or even), and sync character configuration.

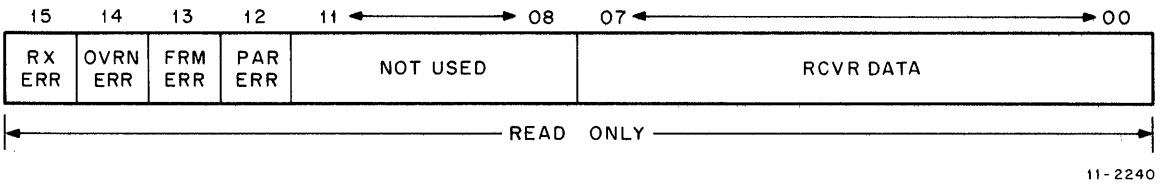
4. TXCSR – Programmed and monitored (read/write) to control the XMTR (transmitter) portion of the interface, to control the resetting and initialization of the interface, and to control and monitor the maintenance mode operation of the interface.

5. TXDBUF – Programmed (write only) to provide parallel data to the interface XMTR for serial transmission to the modem.

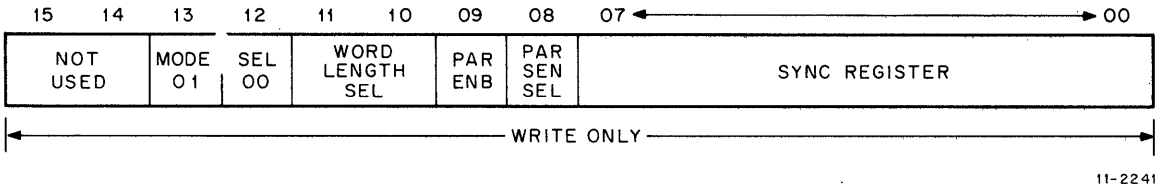
3.2.2.2 Bit Assignments – Bit assignments for the five DUV11 registers are shown in Figure 3-1. The bit names indicate the function of the bit. The bits that are defined as not used or write-only are always read as 0. In the same respect, attempts to program the not used bits or read-only bits have no effect on the bit.



Receiver Status Register (RXCSR)

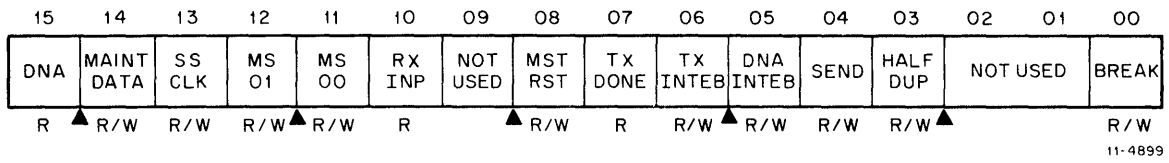


Receiver Data Buffer (RXDBUF)

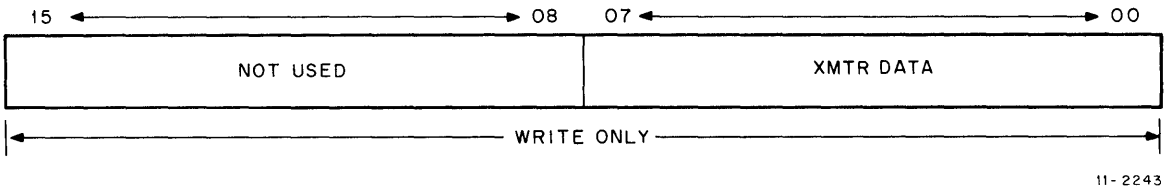


Parameter Status Register (PARCSR)

Figure 3-1 DUV11 Register Configurations and Bit Assignments (Sheet 1 of 2)



Transmitter Status Register (TXCSR)



Transmitter Data Buffer Register (TXDBUF)

Figure 3-1 DUV11 Register Configurations and Bit Assignments (Sheet 2 of 2)

The following figures and tables describe register content. Figures 3-2 through 3-6 illustrate the register formats. Tables 3-2 through 3-6 list bit descriptions.

The mnemonic INIT is used frequently in the tables and refers to the initialization signal generated by the processor. The processor will issue an INIT signal for any one of the following conditions:

1. A programmed RESET instruction is processed.
2. The processor GO function is activated.
3. The power fail sequence occurs.

During a power fail sequence, INIT is asserted when power is going down and again when power is coming up.

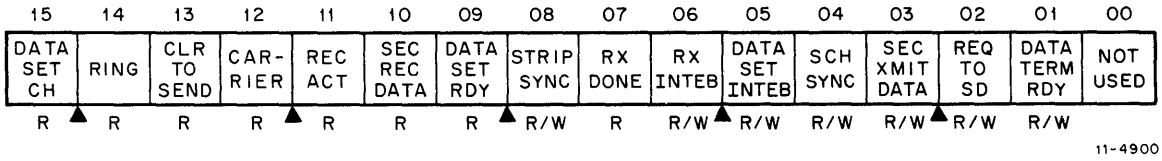


Figure 3-2 Receiver Status Register (RXCSR)

Table 3-2 Receiver Status Register Bit Description

Bit	Name	Description
15	DAT SET CH (Data Set Change)	When set, this bit indicates a modem status change. This bit is set by a transition of any of the following lines: • Ring • Clear To Send • Carrier • Secondary Received Data • Data Set Ready If bit 05 of this register is set, the setting of this bit will cause a RCVR interrupt. Read-only bit; cleared by INIT, master reset, and the DTI SEL 0 (RXCSR read strobe).
14	RING (Ring)	This bit reflects the state of the modem ring line. When set, this bit indicates that a ring signal is being received from the modem. Read-only bit.
13	CLR TO SD (Clear to Send)	This bit reflects the state of the clear to send line from the modem. When set, this bit indicates that the modem is ready to accept data from the interface for transmission. Read-only bit.
12	CARRIER (Carrier)	This bit reflects the state of the modem carrier. When set, this bit indicates the carrier is up. Read-only bit.
11	REC ACT (Receiver Active)	When the internal synchronous mode is selected, this bit is set when the proper number of contiguous sync characters (either 1 or 2, normally set for 2) have been received. If external synchronous or isochronous mode is selected, this bit follows the state of the search sync bit (bit 04 of this register). Refer to Paragraph 5.3 for RCVR synchronization information. Read-only; cleared by INIT, master reset, and SCH SYNC (1) H (search sync) making 1 to 0 transition.
10	SEC RCV DAT (Secondary Receive Data)	This bit reflects the state of the secondary receive data line from the modem. This bit provides a receive channel for supervisory data from the modem to the processor. Read-only bit.

Table 3-2 Receiver Status Register Bit Description (Cont)

Bit	Name	Description
09	DAT SET RDY (Data Set Ready)	This bit reflects the state of the data set ready line from the modem. When set, this bit indicates that the modem is powered up and ready. Read-only bit.
08	STRIP SYNC (Strip sync)	This bit determines whether sync characters received from the modem are to be presented to the program for reading. When this bit is set, receive characters that match the contents of the sync register do not cause a RCVR interrupt provided no errors are detected, i.e., bit 15 of the RXDBUF is clear. Read/write bit; cleared by INIT and master reset.
07	RX DONE (Receiver Done)	This bit is set when synchronization has been achieved and a character has been loaded into the RXDBUF, provided the STRIP SYNC bit is not set. If the STRIP SYNC bit is set and the received character is a sync character without errors, i.e., bit 15 of the RXDBUF is clear, this bit will not be set. When set, this bit will cause a RCVR interrupt request provided bit 06 of this register is set. Read-only bit; cleared by INIT, master reset, and the DTI SEL 2 (RXDBUF read strobe).
06	RX INTEB (Receiver Interrupt Enable)	When set, allows a RCVR interrupt request to be generated when the RX DONE bit is set. Read/Write bit; cleared by INIT and master reset.
05	DAT SET INTEB (Data Set Interrupt Enable)	When set, allows a RCVR interrupt request to be generated when the DAT SET CH bit is set.
04	SCH SYNC (Search Sync)	When set in the internal synchronous mode, enables the RCVR synchronization logic and causes the RCVR to start comparing incoming data bits to the contents of the sync register in an attempt to recognize a sync character. When set in the isochronous mode, enables the RX DONE flag generation logic. When set in the external synchronous mode, enables the RX DONE flag generation logic and causes the RCVR to start framing incoming characters. Read/write bit; cleared by INIT and master reset.

Table 3-2 Receiver Status Register Bit Description (Cont)

Bit	Name	Description
03	SEC XMIT (Secondary Transmit Data)	This bit reflects the state of the secondary transmit data line to the modem. This bit provides a transmit channel for supervisory data from the processor to the modem. Read/write bit; cleared by INIT and master reset.
02	REQ TO SD (Request to Send)	When set, this bit causes the request to send line to the modem to be asserted. The request to send line is a control lead to the modem. This line must be asserted before the interface can transmit data to the modem. Read/write bit, optionally cleared by INIT and master reset.
01	DATA TERM RDY (Data Terminal Ready)	When set, this bit indicates the interface is powered up, programmed, and ready to receive data from the modem. Setting this bit causes the data terminal ready line to the modem to be asserted. The data terminal ready line is a control lead for the modem communication channel. When asserted, it permits the interface to be connected to the channel. Read/write bit; optionally cleared by INIT and master reset.

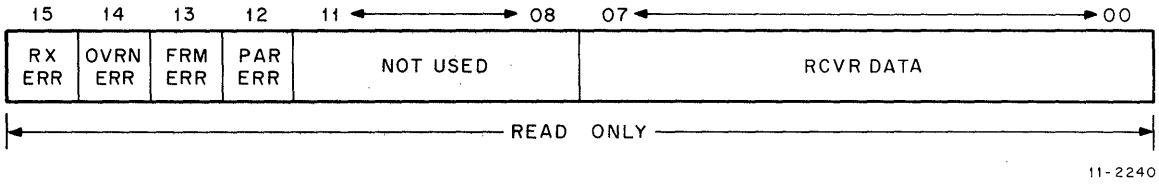


Figure 3-3 Receiver Data Buffer (RXDBUF)

Table 3-3 Receiver Data Buffer Bit Description

Bit	Name	Description
15	RX ERR (Receiver Error)	This bit is set whenever one of the three receiver error bits is set (logical OR of bits 14, 13, and 12). Read-only bit; cleared only when bits 14, 13, and 12 are cleared.
14	OVRN ERR (Overrun Error)	When set, this bit indicates that the processor has failed to service the RX DONE flag within the time required to load another character into the RXDBUF, i.e., (1/baud rate) × (bits per character) seconds. Hence, the previous character was overwritten (lost). This condition indicates the loss of at least one character. Read-only bit; cleared by INIT, master reset, and DTI SEL 2 (RXDBUF read strobe).
13	FRM ERR (Framing Error)	When set, indicates that character received was not followed by a valid STOP bit. This error only occurs in the isochronous mode of operation. Read-only bit; cleared by INIT, master reset, and DTI SEL 2.
12	PAR ERR (Parity Error)	When set, indicates that the parity of the received character does not agree with the parity programmed (odd or even). If parity is not programmed, this bit is always cleared. Read-only bit; cleared by INIT, master reset, and DTI SEL 2.
07–00	RCVR DATA (Receiver Data)	This register holds the received character for transfer to the program. The buffer is right justified for 5, 6, 7, or 8 bits. If parity is received it is also loaded into the buffer at the next vacant higher order bit position. Therefore, if a 5-bit character plus parity is framed by the RCVR, the parity bit would be loaded into bit position 05 in the RXDBUF and presented to the program for reading. If an 8-bit character plus parity is framed, the parity bit would not be presented to the program for reading. Read-only buffer; cannot be cleared, INIT or master reset sets the buffer to all ones. Reading the RDXBUF causes the RXDONE bit in the RXCSR to clear.

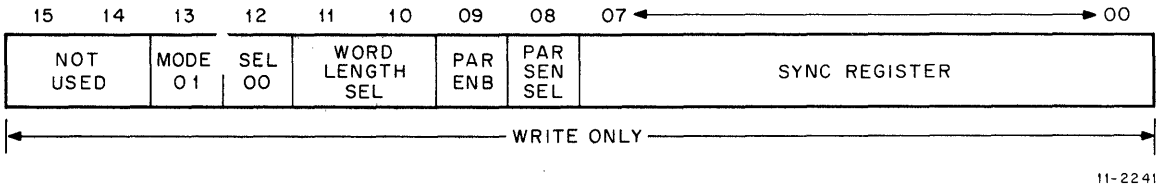


Figure 3-4 Parameter Status Register (PARCSR)

Table 3-4 Parameter Status Register Bit Description

Bit	Name	Description
13 and 12	MODE SEL (Mode Select)	These bits control the mode of operation. Modes are selected as follows: Mode — Bit 13 — Bit 12 Internal Synchronous — 1 — 1 External Synchronous — 1 — 0 Isochronous — 0 — 0 Illegal (Not Used) — 0 — 1 Write-only bits.
11 and 10	WORD LEN SEL (Word Length Select)	These bits control the length of characters received and transmitted by interface. Word length (not including parity) is selected as follows: Bits per Character — Bit 11 — Bit 10 5 — 0 — 0 6 — 0 — 1 7 — 1 — 0 8 — 1 — 1 Write-only bits.
09	PAR ENB	If this bit is set, parity for each character will be (parity enable) generated by the XMTR and checked by the RCVR. If character length is less than eight bits, the parity bit for received data is loaded into the RXDBUF for reading by the program. If bad parity is detected at the RCVR, the parity error flag is set (bit 12 of the RXDBUF). Write-only bit.

Table 3-4 Parameter Status Register Bit Description (Cont)

Bit	Name	Description
08	PAR SEN SEL (Parity Sense Select)	When the parity enable bit (bit 09 of this register) is set, the sense of the parity (odd or even) is controlled by this bit. When this bit is set, even parity is generated by the XMTR and checked for by the RCVR (the program does not have to provide a parity bit to the XMTR). When this bit is cleared, odd parity is generated and checked. Write-only bit.
07–00	Sync Register	This register contains the sync character. The sync character is used by the RCVR to detect received sync characters and thereby achieve synchronization. The sync character is used as a fill character by the XMTR when operating in the synchronous mode. Fill characters are operating in the synchronous mode. Fill characters are transmitted when the program fails to provide characters to the XMTR fast enough to maintain continuous transmission, i.e., (1/baud rate) × (bits per character) seconds – 1/2 (bit time).

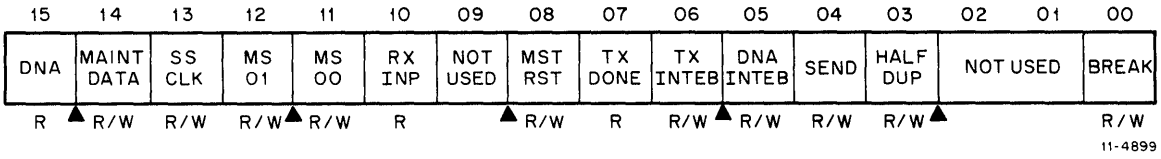


Figure 3-5 Transmitter Status Register (TXCSR)

Table 3-5 Transmitter Status Register Bit Description

Bit	Name	Description
15	DNA (Data Not Available)	This bit is set by the XMTR when a fill character is transmitted. This applies only to the synchronous mode of operation and is caused by late program response to a TX DONE interrupt request. The processor response to TX DONE must be within (1/baud rate) × (bits per character) seconds - 1/2 (bit time). If not, the fill character is transmitted. If bit 05 of this register is set, setting this bit causes an XMTR interrupt request. Read-only bit; cleared by INIT, master reset, and DTI SEL 4 (TXCSR read strobe).
14	MAINT DATA (Maintenance Data)	This bit is used in the internal loop and external loop maintenance modes by the diagnostic program to simulate serial input to the RCVR. Refer to Chapter 6 for more detailed information on the use of this bit. Read/write bit; cleared by INIT or master reset.
13	SS CLK (Single Step Maintenance Clock)	This bit is used in the internal loop and external loop maintenance modes by the diagnostic program to simulate the XMTR and RCVR clocks. Refer to Chapter 6 for more detailed information on the use of this bit. Read/write bit; cleared by INIT or master reset.
12 and 11	MS01/MS00 (Maintenance Mode Select 01 & 00)	These bits are used to select the normal mode of operation or one of three maintenance modes. Modes are selected as follows: Mode — Bit 12 — Bit 11 Normal — 0 — 0 Internal Maintenance Loop — 0 — 1 External Maintenance Loop — 1 — 0 System Test — 1 — 1 Refer to Chapter 6 for more detailed information on the maintenance modes and their use. Read/write bits; cleared by INIT and master reset.

Table 3-5 Transmitter Status Register Bit Description (Cont)

Bit	Name	Description
10	RX INP (Receiver Input)	This bit monitors the RCVR input in the internal loop and external loop maintenance modes. Read-only.
08	MSTRST (Master Reset)	This bit is used to generate a CLR (clear) pulse, which initializes the registers and the XMTR and RCVR and inhibits the BRPLY L (bus reply) signal. Refer to Chapter 4 for more detailed information on the effects of the CLR pulse. This bit remains at a (1) for only 3 μs after being set Read/write.
07	TX DONE (Transmitter Done)	This bit is set by INIT and master reset and when the first bit of the character contained in the XMTR register is placed on the XMTR output line. If bit 06 of this register is set when this bit is set, an XMTR interrupt request is generated. Read-only bit; cleared by LD TXDBUF (TXDBUF load strobe).
06	TX INTEB (Transmitter Interrupt Enable)	When set, this bit allows an XMTR interrupt request to be generated by the TX DONE bit. Read/write bit; cleared by INIT and master reset.
05	DNA INTEB (Data Not Available Interrupt Enable	When set, this bit allows a XMTR interrupt request to be generated by the DNA bit. Read/write bit; cleared by INIT and master reset.
04	SEND (Send)	When set, this bit enables the XMTR and transmission will start when a character is loaded into the TXDBUF. This bit must remain set until the entire message is transmitted. If not, transmission of the character currently in the XMTR register is completed and the XMTR will enter the idle state. Read/write bit; cleared by INIT and master reset.
03	HALF DUP (Half Duplex)	When this bit is set, operation will be in the half duplex mode. In this mode the RCVR is disabled whenever bit 04 of this register is set. Read/write bit; cleared by INIT and master reset.

Table 3-5 Transmitter Status Register Bit Description (Cont)

Bit	Name	Description
00	BREAK (Break)	When this bit is set, the serial XMTR output D5 SERIAL DATA OUT H is held in the space (constant low) condition; otherwise, operation is normal. This bit is used by the diagnostic program in the internal loop or external loop maintenance modes to inhibit the XMTR output while inputting data to the RCVR via bit 14 of this register. Read/write bit; cleared by INIT and master reset.

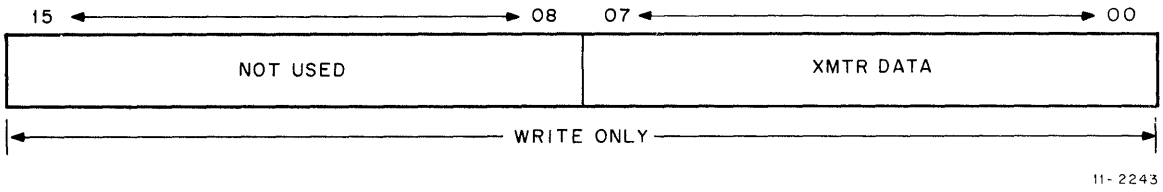


Figure 3-6 Transmitter Data Buffer (TXDBUF)

Table 3-6 Transmitter Data Buffer Bit Description

Bit	Name	Description
07–00	XMTR DATA (Transmitter Data)	This register is loaded by the program with the character to be transmitted. Character length is from 5 to 8 bits. The character is right-hand justified. If a parity bit is enabled, it is generated by the interface. Write-only bits; an INIT or master reset places all ones in this register.

3.3 INTERRUPT REQUESTS

The DUV11 uses interrupts to gain control of the bus, thereby causing the processor to branch to a service subroutine.

The interface uses two interrupt vectors: one for the RCVR section and one for the XMTR section. If simultaneous RCVR and XMTR interrupt requests occur, the RCVR has priority.

Both the XMTR and RCVR sections of the interrupt control logic handle interrupt requests from two sources. A XMTR interrupt request is generated by the setting of the TX DONE bit or the DNA bit provided the TX INTEB and the DNA INTEB bits are set. A RCVR interrupt request is generated by setting the RXDONE bit or the DAT SET CH bit, provided the RX INTEB and DAT SET INTEB bits are set.

The DUV11 interrupt vector addresses are floating. The vector addresses can be changed via switches E39-3 to E39-8 in the interrupt control logic.

NOTE

If the DUV11 interrupt vector address is changed, all DEC programs or other software referring to the interrupt vector addresses must also be changed.

CHAPTER 4
THEORY OF OPERATION

4.1 SCOPE

This chapter contains both general data flow and specific logic interactions that allow the DUV11 interface to function. As the discussions develop, frequent reference will be made to the DUV11 engineering drawing set provided with each unit.

4.2 INITIALIZATION AND PROGRAMMING

Before the DUV11 interface can begin to handle data, it must be initialized and programmed. Initializing the interface prepares it to be programmed. All registers are initialized, all flip-flops are cleared, and the RCVR and XMTR are forced to the idle state. When the RCVR is in the idle state, the RXDBUF (receiver data buffer) is set to all 1s, the RCVR sync register is cleared, and the RCVR timing and control logic and output flags are cleared. When the XMTR is in the idle state, the XMTR output is a constant MARK (high), the XMTR timing and control logic is cleared, and the XMTR output flags are set.

Programming the DUV11 establishes its operating parameters. General operating parameters are controlled by the PARCSR (parameter status register), while specific operating parameters pertaining directly to the RCVR, XMTR, and maintenance circuitry are controlled by the RXCSR (receiver status register) and the TXCSR (transmitter status register). The PARCSR is programmed to select the mode of operation (isochronous, internal synchronous, or external synchronous), word length (5, 6, 7, or 8 bits plus parity), (enable or disable), parity sense (odd or even), and sync character configuration. The RXCSR is programmed to enable or disable the RCVR data handling logic, strip sync logic and interrupt logic, and to communicate interface status, requests and supervisory data to the modem. The TXCSR is programmed to select the maintenance mode (normal, internal loop, external loop, and system test); drive the maintenance clock; provide a maintenance data input; reset and initialize the overall interface; enable or disable the XMTR data handling logic, data output logic, and interrupt logic; and select the interface duplex mode (half or full).

4.3 OVERALL DATA FLOW

Once the interface is programmed, data communication can commence. Data communication can be initiated by the program or by the modem operator. The program initiates communication simply by loading a character into the TXDBUF. The XMTR then outputs that character to the modem, which transmits it to the modem at a remote station. The modem operator initiates data communication by dialing a remote station on the modem. The modem at the remote station detects the call and responds by asserting ring to its own interface. The interface then generates a RCVR interrupt which causes the processor to branch to an interrupt service subroutine. The service subroutine directs the processor to execute the handshaking sequence and load a character into the TXDBUF. If the XMTR is enabled [SEND (1) H asserted], the XMTR begins to output the character to the modem and asserts TX DONE H to request the next character of the message. The modem transmits the character to the modem that placed the call. If more characters are to be transmitted, the program responds to the TX DONE H flag and loads the next character into the TXDBUF. When transmission of the current character is complete, transmission of the next character begins. When all characters comprising the message have been loaded into the TXDBUF and TX DONE H is asserted, the program clears SEND (1) H.

As soon as transmission of the current character is complete, the XMTR output marks (constant high). Note that TX DONE H will not change state after SEND (1) H is cleared.

If during message transmission, the program fails to load the TXDBUF before current character transmission is complete, one of two operations will result, depending on the mode of operation. If the XMTR is programmed for the synchronous mode, a sync character will be output to maintain synchronization with the RCVR (synchronous mode requires continuous transmission). If the isochronous mode is programmed, the XMTR will simply pause until the next character is loaded into the TXDBUF and then resume operation.

Data reception is initiated when input data is provided to the RCVR, provided SCH SYNC(1) H is asserted. Before the RCVR can begin framing characters for reading by the program, however, REC ACT(1) H must assert indicating that the RCVR at the receiving station is synchronized with the XMTR at the sending station. Once REC ACT(1) H asserts, the RCVR frames the very next character, transfers the character to the RXDBUF, and asserts RX DONE(1) H. This assertion causes a RCVR interrupt request to be generated. The processor branches to an interrupt service subroutine and ultimately reads the RXDBUF. If the program fails to read the RXDBUF before the next character is framed and transferred to the RXDBUF, the character previously framed is lost and OVRN ERR H (overrun error) is asserted.

4.4 FUNCTIONAL BLOCK DESCRIPTION

The DUV11 can be divided into six functional blocks, each performing a specific task within the interface. A brief description of each of these blocks is provided in the following paragraphs (Figure 4-1).

4.4.1 Address Comparator and Command Decoder

This block provides the actual interface with the LSI-11 Q BUS. Preset address selection rocker switches are compared to the addressing lines from the Q BUS. If the addresses compare, information in the form of controls and data are exchanged by transceivers within this functional block.

Control of data to and from the QDL BUS of the DUV11 to the Q BUS linking the LSI-11 is under the gating of the command decoder. The command decoder receives its controls from the Q BUS via the address comparator and direct connection.

4.4.2 Data Multiplexer

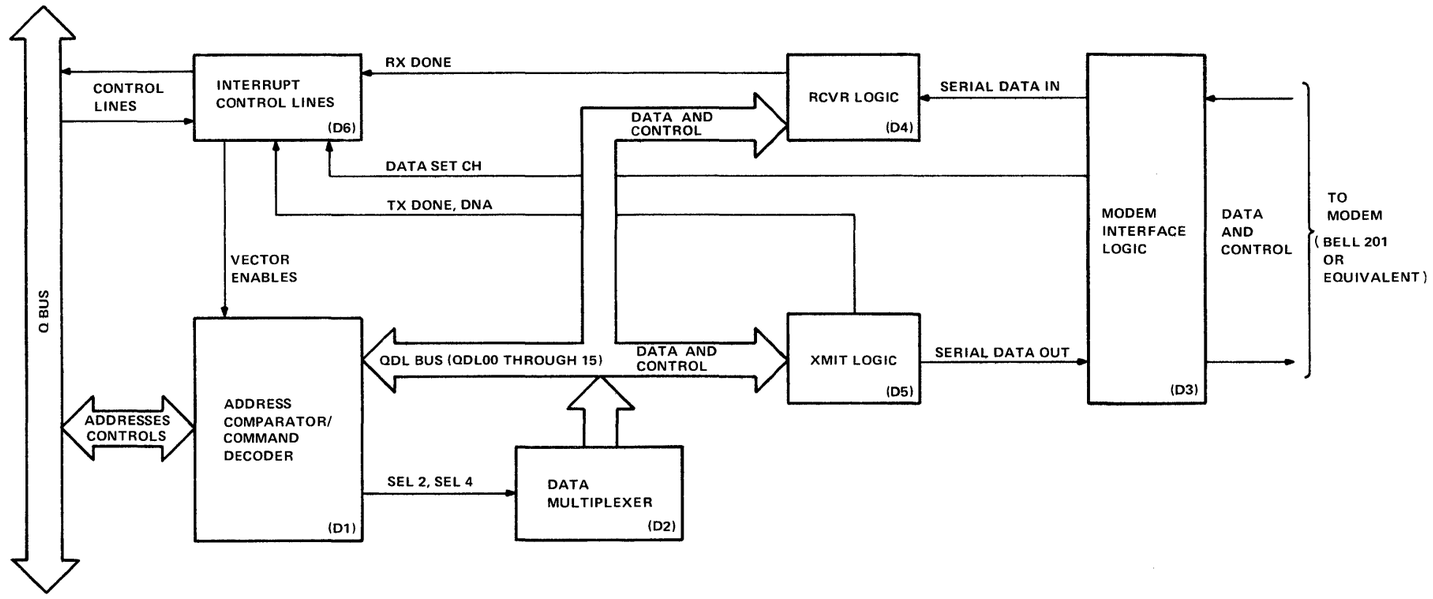
The data multiplexer controls the data and status information to the transceivers which is outputted onto the Q BUS. The multiplexer receives status data from the modem interface logic, the receiver logic and transmitter logic. This information is released to the QDL BUS for transfer to the transceivers under control of the command decoder.

4.4.3 Modem Interface Logic

This block contains the EIA level converters which convert the logic level signals to the voltage levels of the Bell 201 modem. This block contains the transmit data line to the modem and serial data in, as well as access to all the modem control signals.

4.4.4 Receiver Logic

The logic necessary to receive the serial data from another communications system and convert it to parallel data is contained in this block. This includes the receiving section of the parameter control status register, the receiver control status register, the receiver data buffer and other associated receiver logic. This block contains the SAR chip.



NOTE:
( ) indicates engineering drawing sheet of logical block.

11-5151

Figure 4-1 DUV11 Functional Block Diagram

4.4.5 Transmitter Logic

The logic necessary to change the parallel data from the Q BUS to serial data for transmission over communication lines is contained in this block. This includes the transmission section of the parameter control status register, the transmitter control status register, the transmitter data buffer and other associated transmitter logic.

4.4.6 Interrupt Control Logic

The interrupt control logic enables the DUV11 to become bus master, and causes a program interrupt to an interrupt address vector. When an interrupt request is generated the interrupt control logic is enabled, the bus is requested and granted, the interrupt is identified and acknowledged, the processor branches to the subroutine identified by the vector address and then services the interrupt.

4.5 DETAILED FUNCTIONAL DESCRIPTION

The following paragraphs contain further details on the signal flow and functions of the major components comprising the DUV11.

4.5.1 Address Comparator (Engineering Drawing D1)

The address comparator logic is made up of the bus transceivers and address/vector rocker switches. The rocker switches are set before operating the DUV11. When the LSI-11 addresses the DUV11, the bus transceivers compare the preset address with the address on the Q BUS (BDAL 00 through 15 as shown on engineering drawing D1). If they compare, the MATCH signal is asserted which enables the command decoder (DC004 chip). Information then received at the transceivers is passed from the Q BUS to the QDL BUS (QDL 00 through QDL 15) under control of the command decoder. Signal INWDB H enables the transceivers to receive data from the Q BUS and place that data onto the QDL BUS. This signal originates from the Q BUS as BDIN L (engineering drawing D6), which is driven to become DIN L. DIN L is applied to the command decoder and is output as INWD L when MATCH is asserted by the address comparator. INWD L is then gated to become INWDB L. Similarly, the signals SEL 0 L, SEL 2 L, and SEL 4 L which are functions of QDL 00, QDL 01 and QDL 02, when MATCH is asserted to the command decoder, are gated to become EN QDL TO BDAL. This signal enables data from the QDL BUS which is applied to the transceivers to pass on to the Q BUS.

During an interrupt sequence the address comparator circuitry provides passage of the preset interrupt vector address to the Q BUS.

4.5.2 Command Decoder (DC004 Chip as Shown on Enginering Drawing D1)

The command decoder logic controls the flow of data into the status registers within the DUV11 and the passage of status information and data back out to the CPU.

The signals which enable the registers of the DUV11 such as LD PARCSR, LD TXDBUF etc., are generated by gating the outputs of the command decoder (refer to engineering drawing D1). This logic receives bits 00 through 02 from the QDL BUS. When the address comparator outputs MATCH, these bus bits cause the command decoder logic to output the proper select signal. For example if the control logic selector asserts SEL 6 L along with OUTLB L the resultant gated output is LD TXDBUF (1) L, which causes the transmitter data buffer to load parallel data from the QDL BUS.

4.5.3 Data Multiplexer (Engineering Drawing D2)

As mentioned earlier, the data multiplexer controls the passage of DUV11 status signals and data to the bus transceivers for output to the CPU. Two signals, SEL 2 L and SEL 4 L enable the selection of status signals and data which will pass on to the QDL BUS. A truth table containing these enables and resultant outputs are shown in the legend at the top of engineering drawing D2.

4.5.4 Modem Interface Logic

The modem interface logic contains level converters to change the logic level signals to the operating voltage levels of the Bell 201 modem. All logic signals ranging from 2.4 to 3.5 V are converted to +6 V. All ground (0 V) logic signals are converted to -6 V. This circuitry is shown on engineering drawing D3.

4.5.5 Receiver Control Logic

The receiver circuitry contains the synchronous/asynchronous receiver chip (SAR) and its supportive logic. Within the SAR, serial data received from the modem is converted to parallel data for output onto the QDL BUS. Parameter data is supplied via the QDL BUS. PARCSR (1) L loads this data into SAR (engineering drawing D4). Having stored these parameters, the receiver detects the serial received character, accomplishes synchronization, frames the received character, detects errors, raises the RXDONE flag and holds the framed character (for program reading) until the next character is framed.

Once the RCVR logic is enabled, it operates as programmed. The SCH SYNC input enables the RCVR logic. The contents of the PARCSR determine:

1. Mode of operation (internal synchronous, external synchronous, or isochronous)
2. Length of character to be framed (5, 6, 7, or 8 bits plus parity)
3. Parity (enabled or disabled)
4. Parity sense (odd or even)
5. Sync character configuration.

The method of achieving synchronization is the principle difference between the modes of operation.

1. In the internal synchronous mode, two contiguous sync characters must be recognized by the RCVR logic to achieve synchronization. Once synchronization is achieved, the RCVR starts framing on the very next character bit. The received characters must arrive at the RCVR in a continuous serial bit stream or synchronization will be lost.

2. The external synchronous mode is designed for use with communication equipment which accomplishes synchronization external to the DUV11 interface. The external synchronization logic prohibits RCVR operation by inhibiting the assertion of SCH SYNC until synchronization with the XMTR has been achieved. When external synchronization is achieved, SCH SYNC asserts, forcing the RCVR logic to the synchronized state. The RCVR then starts framing immediately, beginning with the very next character bit.

3. In the isochronous mode, each received character is preceded by a start bit and succeeded by a stop bit, which serves to synchronize the RCVR. In this mode, the receiver simply does not start framing until it recognizes a start bit. It then frames the character following the start bit and looks for a stop bit. If a stop bit is not detected, the character received is considered invalid, flagged as such, and held for reading by the program. Hence, in the isochronous mode, characters need not be preceded by sync characters and need not arrive contiguously at the RCVR.

The strip synchronization character (STRIP SYNC) input determines whether received sync characters are to be permitted to set the RX DONE flag. If STRIP SYNC is asserted, all sync characters are discarded provided no errors are detected.

For an illustration of receiver timing involved in internal and external synchronous and isochronous modes of operation refer to Figures 4-2, 4-3, and 4-4. For a more detailed description of the SAR chip refer to Appendix B.

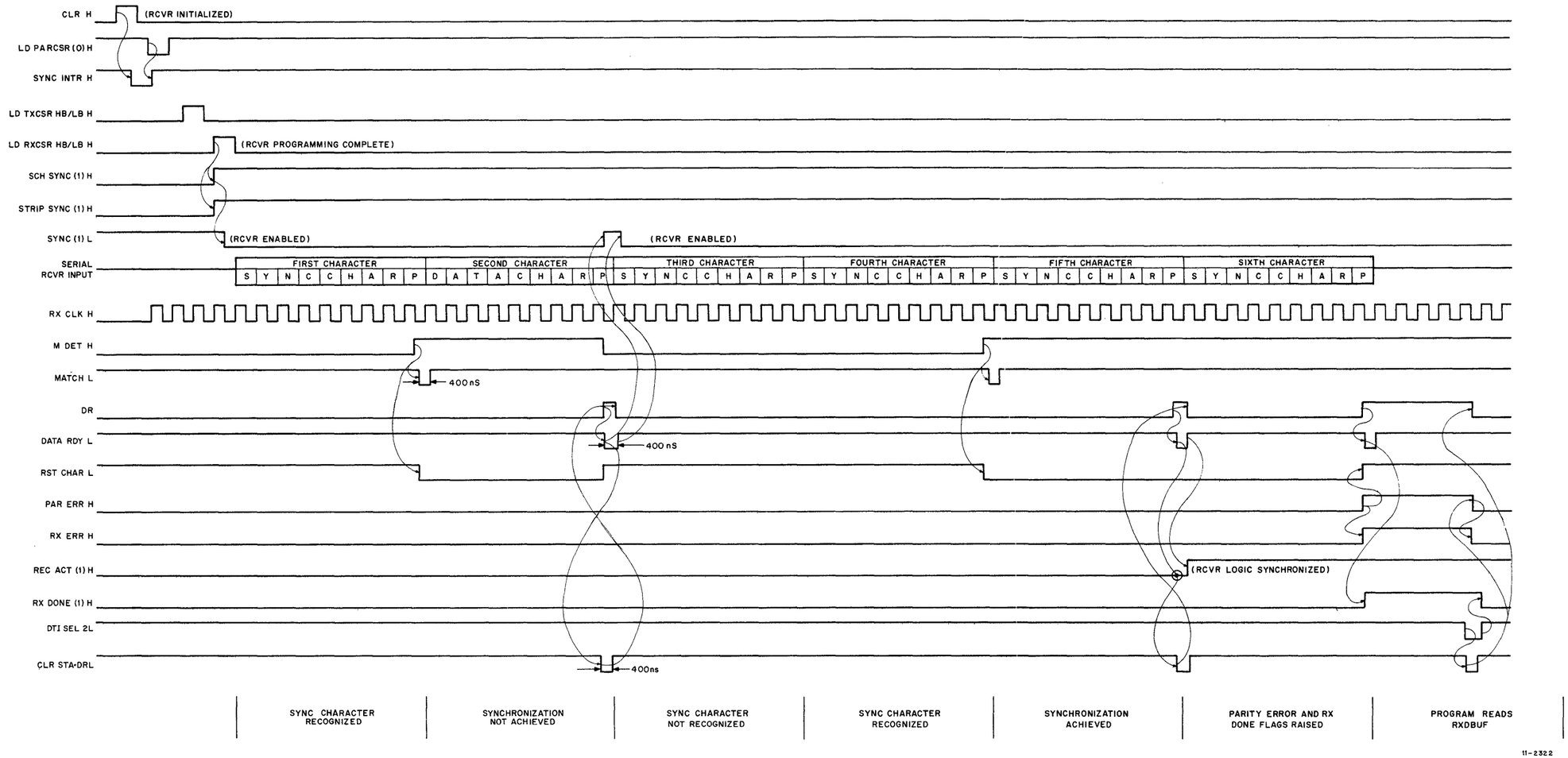


Figure 4-2 Receiver Internal Timing Diagram

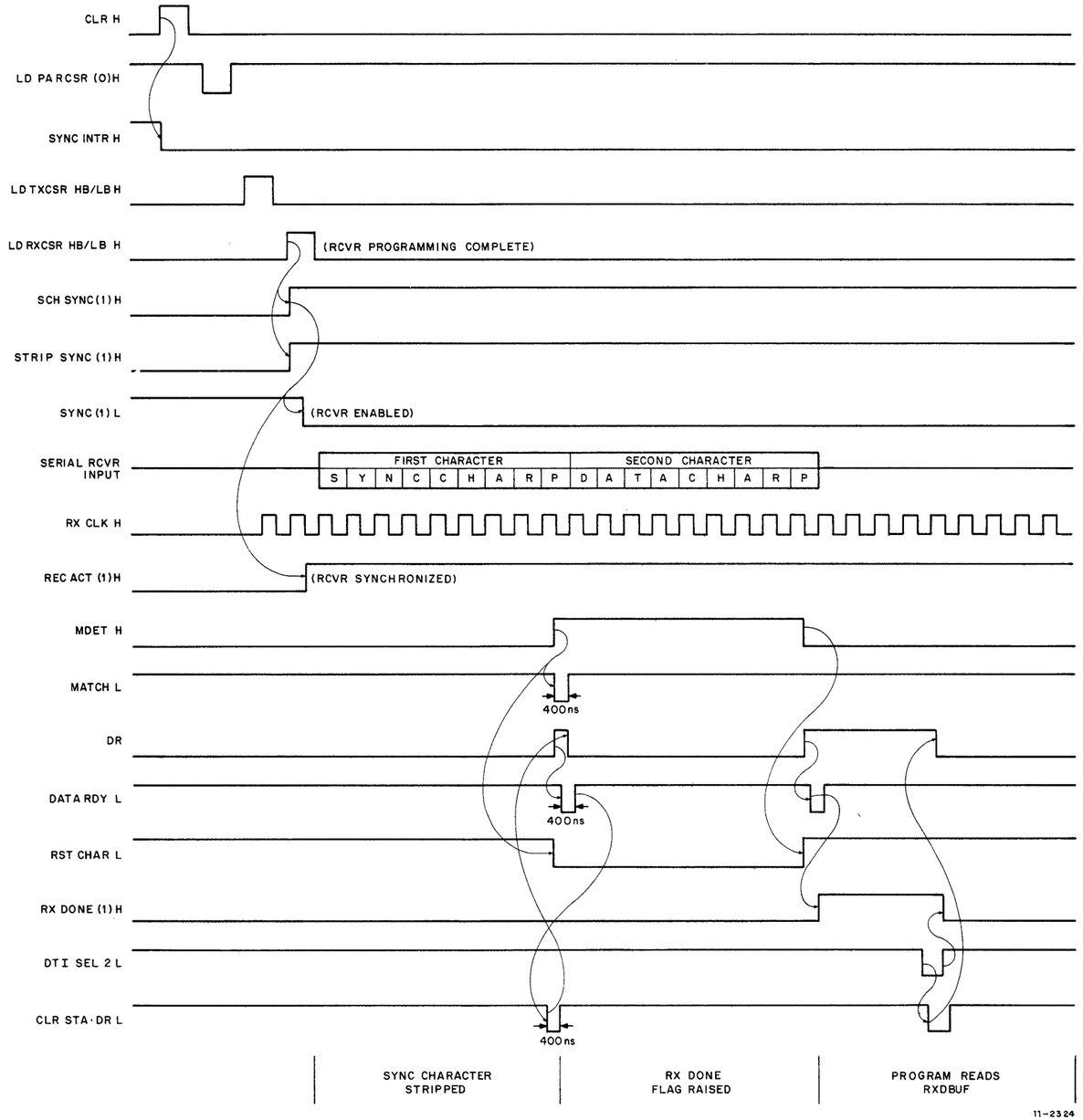


Figure 4-3 Receiver External Synchronous Timing Diagram

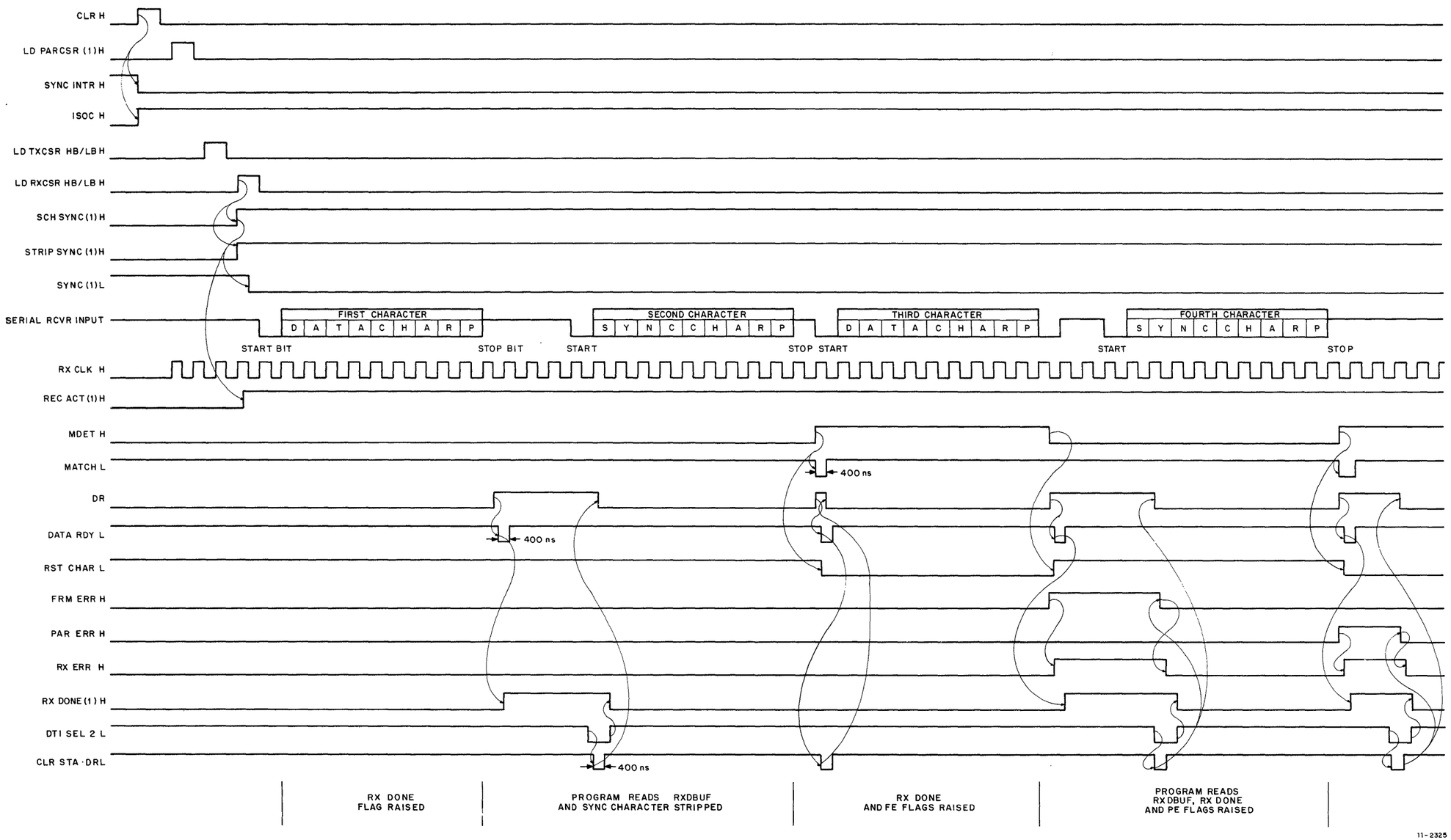


Figure 4-4 Receiver Isochronous Timing Diagram

4.5.6 Transmitter Control Logic

The transmitter circuitry contains the synchronous/asynchronous transmitter chip (SAT) and its supportive logic. The SAT accepts parallel characters from the program, raises the TX DONE flag to request the next character, and serially outputs the current character to the modem. Before transmitter operation can begin, the transmitter logic must be initialized and the PARCSR and TXCSR registers programmed (engineering drawing D5).

The high order bits from the QDL BUS are loaded into the TXCSR when signal LD TXCSR HB H is asserted. The low order bits are loaded into the TXCSR when LD TXCSR LB H is asserted. The signal LD PARCSR (1) L asserted enables parameter data into the SAT.

The signal SEND (1) H enables the transmitter logic. Once the transmitter is enabled, it operates as programmed. The contents of the PARCSR determine:

1. Mode of operation (synchronous or isochronous)
2. Length of character to be transmitted (5, 6, 7, or 8 bits plus parity)
3. Parity (enabled or disabled)
4. Parity sense (odd or even)
5. Sync character configuration (used as fill character in synchronous mode).

There are distinct differences between the two modes of operation:

1. In the synchronous mode, the XMTR receives a parallel transmit character from the program, generates parity if programmed, serially outputs the character plus parity to the modem, and raises the TX DONE flag to request the next character. If the program fails to provide the next character before transmission of the current character is complete, the XMTR outputs fill characters to maintain continuous transmission until another data character is provided. Whenever a fill character is transmitted the data not available (DNA) flag is raised to notify the program of fill character transmission.

2. In the isochronous mode, the XMTR receives a parallel transmit character from the program, generates parity if programmed, outputs a start bit, serially outputs the character plus parity, outputs a stop bit, and raises the TX DONE flag to request the next character. However, in the isochronous mode, if the program fails to provide the next character before transmission of the current character is complete, the XMTR simply pauses until the next character is provided. Hence, the DNA flag is never used in the isochronous mode.

The BREAK input inhibits the XMTR output. Whenever the TXCSR BREAK bit is set, the BREAK input to the XMTR logic asserts and inhibits the XMTR output. This input enables the program to inhibit the XMTR output, while inputting data directly to the RCVR via the RCVR input select logic in the internal and external loop maintenance modes.

For an illustration of transmitter timing involved in synchronous and isochronous modes of operation refer to Figures 4-5 and 4-6. For a more detailed description of the SAT chip refer to Appendix B.

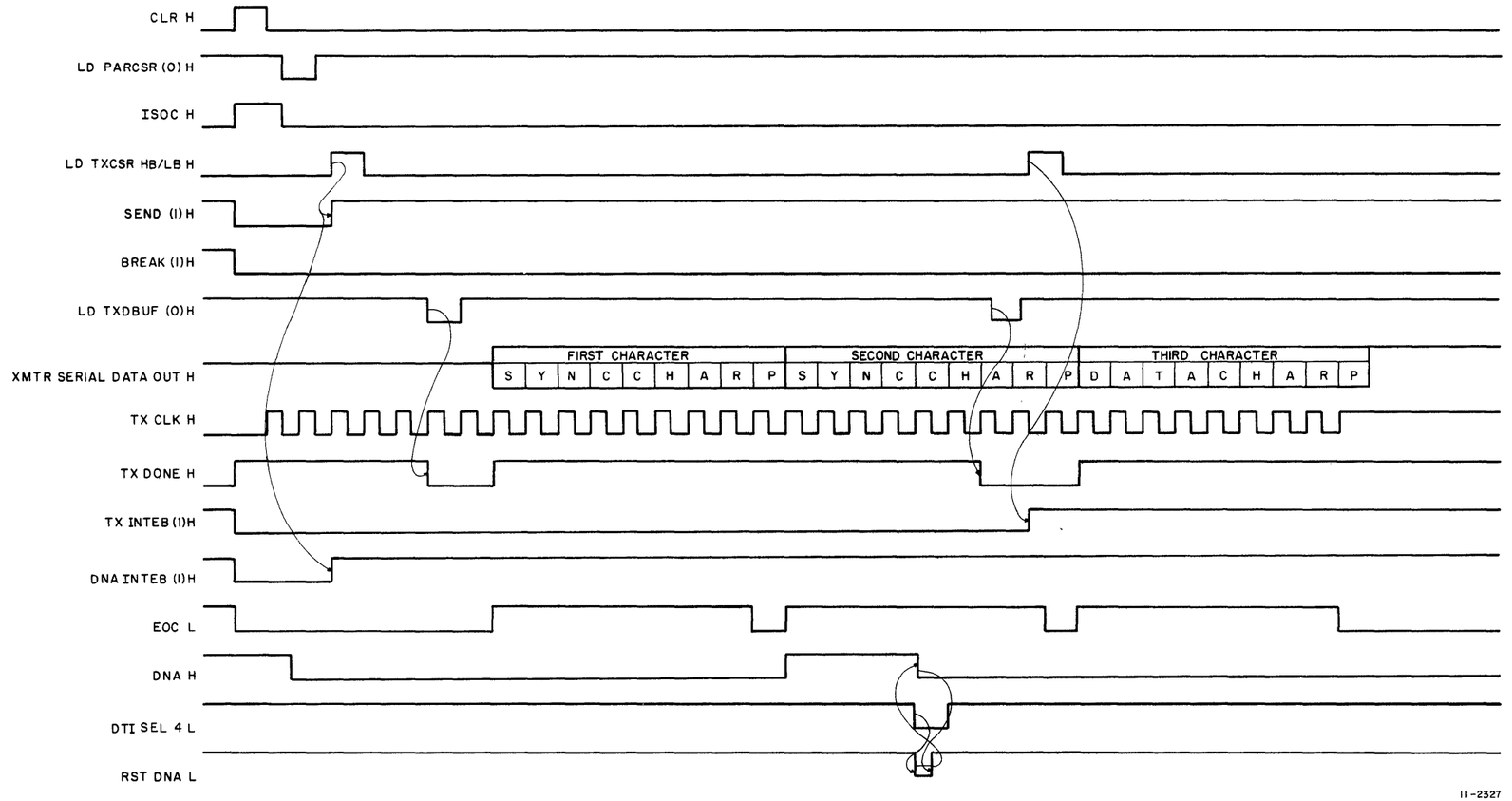


Figure 4-5 Transmitter Synchronous Timing Diagram

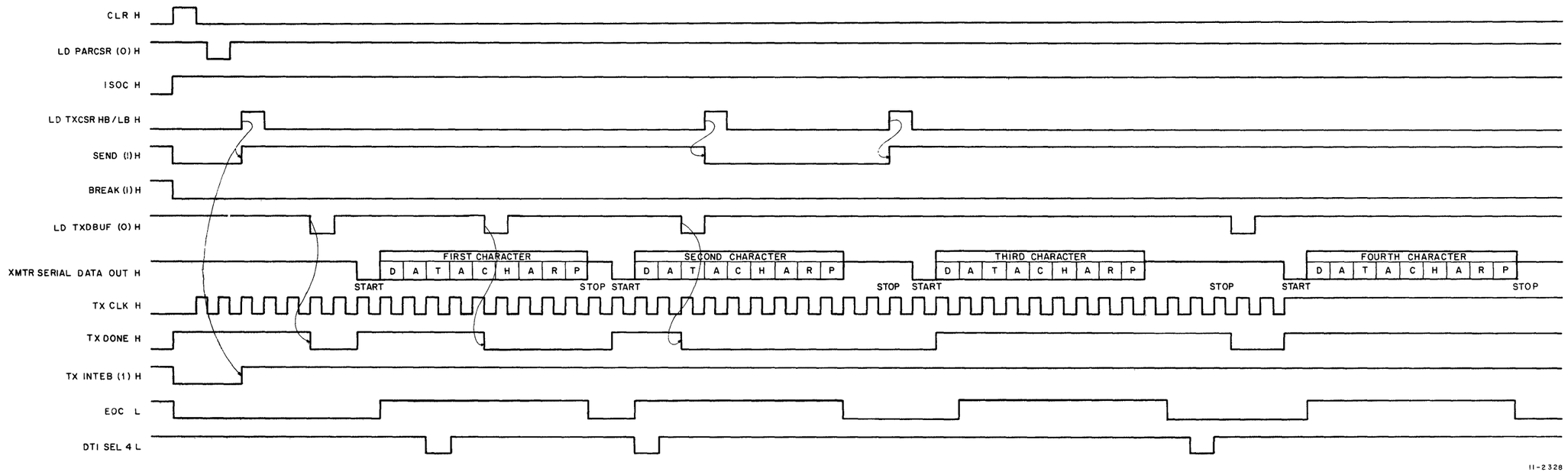


Figure 4-6 Transmitter Isochronous Timing Diagram

4.5.7 Interrupt Control Logic

The interrupt control logic consists of two DC003 chips and associated driving circuitry. When the interrupt control logic receives either RXDONE (1) H, TXDONE (1) H, DATA SET CH (1) H or DNA H with their associated interrupt enable signal, it generates BIRQ L (interrupt request) to the processor (engineering drawing D6). The processor responds with BIAKI L (interrupt acknowledge in) which searches the logic for the originator of the interrupt. If the interrupt was not originated at the DUV11 the signal BIAKO L (interrupt acknowledge out) is passed through with no action taken. If the DUV11 had originated the request EN VEC to BUS H is asserted and depending on the particular interrupt EN UPPER VEC H may also be asserted. This signal asserted then causes the addressing logic to load, onto the Q BUS, the contents of the preset vector address rocker switches. The processor will then perform the preprogrammed subroutine for that interrupt vector address. For a more detailed description of DC003 refer to Appendix B.

4.5.8 Clear Logic

The clear logic generates clear (CLR) and optional clear (OPT CLR) which initialize all DUV11 logic. As shown at the bottom of engineering drawing D3, the INIT signal or MSTRST asserted will activate the clear signals. INIT is a function of BINIT which is received by the interface whenever the computer activates the go function, the processor executes a reset instruction, or the power fail sequence occurs. The clear logic outputs are asserted as long as the BINIT signal remains low. MSTRST is program controlled and is generated by setting bit 08 of the TXCSR. When bit 08 of the TXCSR is set and LD TXCSR HB goes low, a 3 μs one-shot asserts MSTRST and the clear signals remain active for the duration of the one-shot.

The OPT CLR output resets RXCSR bits 1, 2, and 3 and thereby clears the control lines to the modem. By not selecting SW1 option switch, OPT CLR is disabled allowing the DUV11 to be cleared without having to repeat the handshaking sequence. BRPLY is also inhibited as long as CLR is asserted.

4.5.9 Clock Control Logic

The clock control logic decodes the maintenance mode select bits and assigns the transmitter and receiver clocks. There are three possible clock sources, the modem, the programmable SS CLK (single step clock) and the system test clock. (engineering drawing D5.) If the normal operating mode is decoded, the modem clocks are selected. MS00 (0) H is asserted enabling the modem clock inputs (TRS CLK and REC CLK). If the internal loop or external loop maintenance mode is decoded, the SS CLK is selected. This program controlled clock can be operated very slowly to facilitate trouble-shooting. In the internal loop mode, MS00 (1) H is asserted enabling the SS CLK (1) H. In the external loop mode, MS01 (1) H and MS00 (0) H are asserted enabling SS CLK (0) H, TRS CLK and REC CLK. SS CLK (0) H drives CLK EXT, which is routed to the modem test connector, looped back and applied to the TRS CLK and REC CLK inputs (Figure 4-7). If the system test mode is decoded, the system test clock is selected. This output provides an asynchronous clocking source for the system test mode. MS01 (1) H and MS00 (0) H are asserted enabling the internal system test clock to drive the transmitter and receiver. In this mode, the modem clock inputs (TRS CLK and REC CLK) are inhibited. When the DUV11 is transmitting in the half duplex mode, REC CLK is inhibited. HALF DUP (0) L and SEND (0) L go high in this condition, inhibiting REC CLK from reaching the receiver.

4.5.10 +12 to -12 Power Converter

As shown on engineering drawing D6, circuitry is provided to produce -12 Vdc for use by the EIA drivers, the SAT and the SAR chips. A 600 KHz clock is used to switch +12 V into a capacitor network to produce approximately -20 V unregulated. This unregulated voltage is then regulated to -12 V at the output of two twin zener diode networks. The zeners keep the -12 V to within ±5%.

4.5.11 Maintenance Indicators

Indicators in the form of light emitting diodes are provided to display data lines and modem control states for maintenance purposes. Any of the following lines asserted will cause its respective LED to illuminate; RING H, CLR TO SEND H, DATA SET RDY H, CARRIER H, SERIAL DATA OUT H, and SERIAL DATA IN H. These indicators are shown on Figure 1-4 and engineering drawing D6.

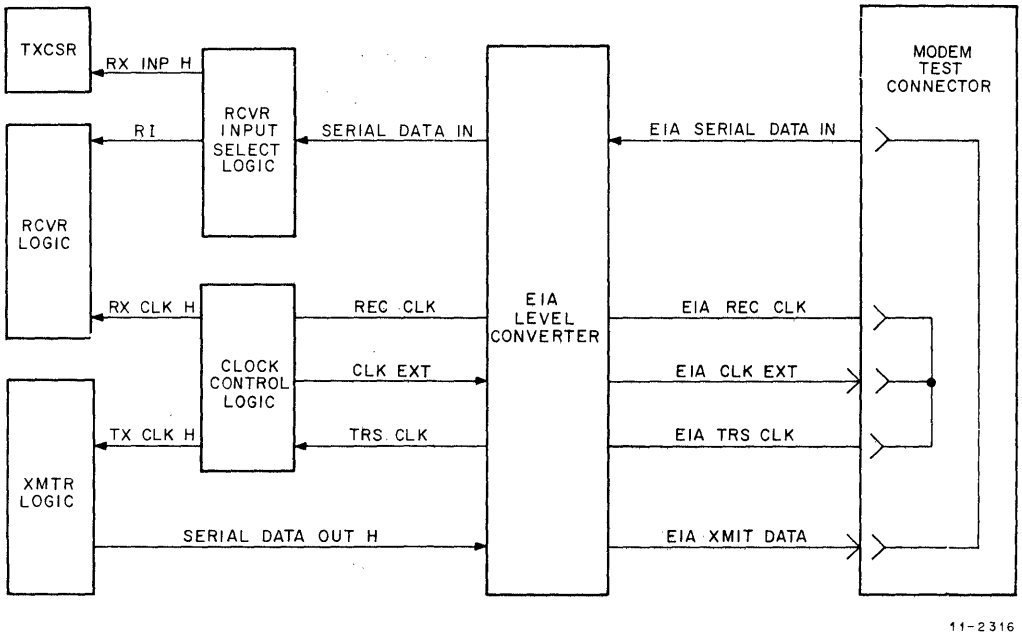


Figure 4-7 External Loop Maintenance Mode Interconnection Diagram

CHAPTER 5
PROGRAMMING REQUIREMENTS AND RECOMMENDATIONS

5.1 INTRODUCTION

To program the DUV11 in the most efficient manner, the programmer must fully understand the control signal and timing requirements for the device. The following paragraphs discuss DUV11 operation from a programming point of view and describe recommended programming methods. It is beyond the scope of this manual to provide detailed programming information. For more detailed information on programming in general, refer to the *Paper-Tape Software Programming Handbook* DEC-11-GGPB-D, and the individual program listings.

5.2 PROGRAMMING THE TRANSMITTER IN THE SYNCHRONOUS MODE

5.2.1 Loading the PARCSR

Once the transmitter is initialized via the BUS INIT pulse or MSTRST, the PARCSR register must be programmed (loaded) to select the mode of operation (synchronous in this case), character length, and parity. At this point the sync register will contain all ones. Before any necessary handshaking is done with the modem, the program must load the sync register with the desired character. When the sync register is loaded, the character will be used for both XMTR and RCVR operation.

5.2.2 Handshaking Sequence

Handshaking sequences serve to establish the data communications channel. This is necessary when the interface is connected to a modem. If the interface is connected to something other than a modem, e.g., a limited distance adapter, handshaking may not be required; the program simply initiates data communication by loading a character into the TXDBUF.

If a handshaking sequence is necessary, the program must be written accordingly. The following paragraphs explain a typical handshaking sequence.

The handshaking sequence is initiated when the modem at one data communication station places a call to a modem at another data communication station. A call may be placed simply by pressing the modem ring button if only two stations are linked in the communication system or dialing-up station 1 on the modem at station 2, if more than two stations are linked.

Once initiated, the handshaking sequence will be executed as programmed. Figure 5-1 illustrates a DUV11 to modem interface; Figure 5-2 illustrates the handshaking sequence.

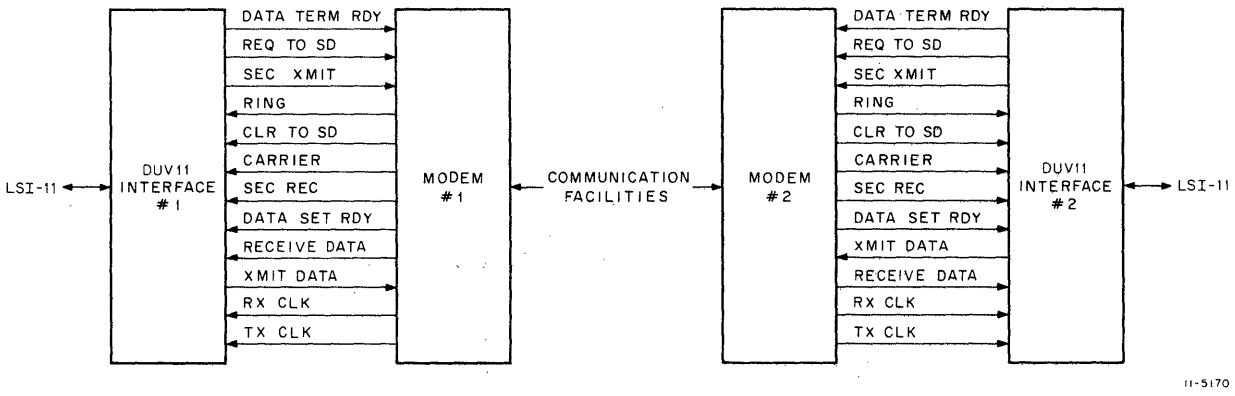


Figure 5-1 DUV11 to Modem Interface Diagram

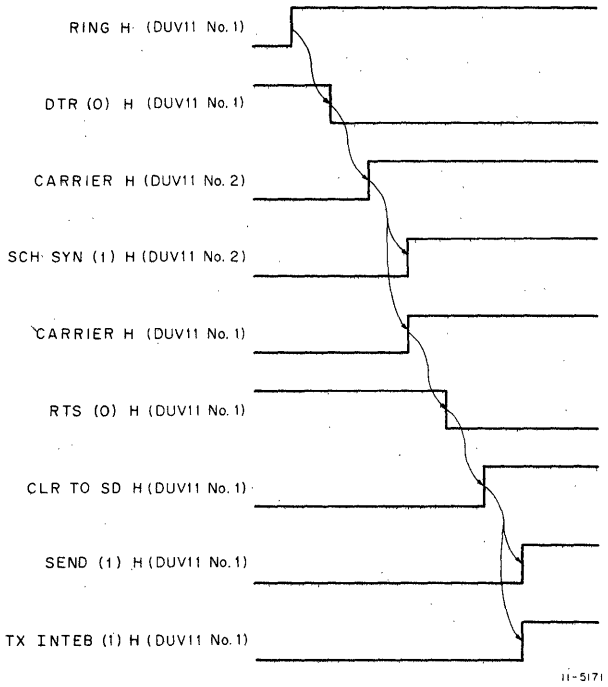


Figure 5-2 Handshaking Sequence Timing Diagram

When modem 2 places a call to modem 1:

1. Modem 1 asserts ring to DUV11 1.
2. DUV11 1 asserts DATA TERM RDY (data terminal ready).
3. Modem 1 sends CARRIER to modem 2.
4. Modem 2 asserts CARRIER to DUV11 2 and sends CARRIER back to modem 1.
5. Modem 1 then asserts CARRIER to DUV11 1 and SCH SYNC (search sync) bit is set at DUV11 2 to enable the RCVR.
6. DUV11 1 asserts REQ TO SD (request to send) to modem 1.
7. Modem 1 asserts CLR TO SD (clear to send) to DUV11 1.
8. The SEND and TX INTEB (XMTR interrupt enable) bits are set at DUV11 1 to enable the XMTR.

Note that the modem DATA SET RDY (data set ready) output must be asserted before any data communication can actually take place. The DATA SET RDY line indicates that the modem is powered up and conditions are go.

Supervisory data may also be transmitted simultaneously with the normal communication data. The SEC XMIT (secondary transmit) and SEC REC (secondary receive) lines provide a supervisory data communication channel.

All data communications can be terminated by simply clearing the data terminal ready bit in the RXCSR.

5.2.3 Enabling the Transmitter

Once handshaking is complete, the program can assert the SEND bit in the TXCSR. When SEND is asserted, the XMTR is enabled but will not start transmitting data until the first character is loaded into the TXDBUF. If SEND is cleared during transmission, the character currently being transmitted will be completed, the transmit line will go to a mark hold state, the internal XMTR logic will enter the idle state, and synchronization with the RCVR will be lost. When SEND is cleared, there is no guarantee that the TX DONE bit will be asserted when current character transmission is complete.

5.2.4 Detecting the Last Character of the Message

When it is necessary to know when the entire message has been transmitted, the DUV11 may be programmed as follows:

1. Just prior to loading the last character of the message into the TXDBUF, clear the TX DONE INTEB bit and set the DNA INTEB bit.
2. When the last character is loaded into the register, the TX DONE bit will set but will not cause an interrupt request.
3. After the last character is transmitted, the transmitter will transmit the sync character and assert DNA, which causes an interrupt request.
4. The DNA interrupt is notification to the program that the entire message has been transmitted.

5.2.5 Transmitting Initial Sync Characters to Establish Synchronization

The transmission of initial sync characters can be accomplished in one of two ways:

1. The program may arrange its data buffer such that the required number of sync characters precede any messages. In this case, the sync register may or may not contain the sync character. If the sync register is not loaded, it will contain all ones subsequent to a BUS INIT or MSTRST.

   Assuming that any necessary handshaking has been completed and that SEND had been asserted, the program can commence transmission by loading a sync character into the TXDBUF. When the first data bit is transferred to the communication line, the TX DONE bit will be asserted. If the TX INTEB bit is set, an interrupt request will be generated and the program must load another sync character into the TXDBUF.

   If the sync character was not initially loaded into the sync register, then synchronization cannot be guaranteed unless the program response time to the TX DONE bit is less than (1/baud rate × bits per char) seconds – 1/2 (bit time). This can be verified by the absence of the DNA bit in the TXCSR.

2. The program can also enable transmission of initial sync characters from the sync register. Assuming any necessary handshaking is complete and SEND is asserted, the program loads the sync register with a sync character, sets the DNA INTEB bit, and clears the TX INTEB bit. The program then loads a sync character into the TXDBUF and transmission begins. The TX DONE interrupt is inhibited so the contents of the sync register are transferred to the XMTR register upon the completion of transmission of the first sync character.

The second sync character is then transmitted and a DNA interrupt is generated notifying the program. The program then allows the transmission of sync characters to continue by simply monitoring the DNA until the desired number have been transmitted. Note that DNA is reset each time the program reads the TXCSR and set again when the first bit of the next sync character is placed on the communication line.

NOTE

It is suggested that a minimum of 5 sync characters be transmitted. In systems that are prone to error because of lost synchronization, as many as 12 sync characters may be desirable.

When the desired number of sync characters have been transmitted, the program sets the TX INTEB bit, thereby enabling the TX DONE interrupt, and responds to the interrupt by loading a message character into the TXDBUF.

5.2.6 Transmitting Sync Characters to Maintain Synchronization

After synchronization has been achieved, it can be maintained by the program by inserting sync characters into the message or by ignoring the TX DONE bit, thereby allowing sync characters from the sync register to be transmitted.

If the latter method is chosen, it can be programmed in one of two ways. The first way would be to set the DNA INTEB bit and clear the TX INTEB bit. The program would then ignore the TX DONE bit and the XMTR would transmit a sync character and assert DNA. The program would monitor the DNA bit and, when the desired number of sync characters are transmitted, set the TX INTEB bit thereby enabling the TX DONE interrupt. The program would then respond to the TX DONE interrupt by loading a message character into the TXDBUF, thereby terminating the transmission of sync

characters. The second way would be to clear the TX INTEB and DNA INTEB bits for a given period of time during message transmission thereby allowing sync characters from the sync register to be transmitted.

NOTE

The SEND bit in the TXCSR must remain set for the duration of the message; any on to off transition will cause the XMTR to enter an idle state after completion of current character transmission.

5.3 PROGRAMMING THE RCVR IN THE INTERNAL SYNCHRONOUS MODE

Once the program has completed any necessary handshaking (Paragraph 5.2.2), the receiver logic can be enabled. The program enables the receiver logic by setting the SCH SYNC (search sync) bit in the RXCSR. Assuming a sync character has been loaded into the sync register (this must be done in the internal synchronous mode), the receiver begins to compare incoming character bits with the character held in the sync register.

NOTE

For the receiver to become synchronized with XMTR either one or two contiguous sync characters must be received. The number of sync characters required is SWITCH selectable. The standard configuration requires two sync characters.

Though the DUV11 may be switched to synchronize on two contiguous sync characters, there is a situation which, if it develops, will prevent RCVR, synchronization on only two contiguous sync characters. If, while the DUV11 is searching for synchronization, it recognizes a sync character that is not followed contiguously by a second sync character, the RCVR internal logic resets, thereby inhibiting the RCVR bit detection logic for two bit times. Should the first bits of a proper sync character sequence occur during that two bit time period, the RCVR will fail to achieve synchronization.

When two contiguous sync characters are received, the REC ACT (receiver active) bit is set and any characters received after that will cause RX DONE interrupt requests, provided the RX INTEB bit is set and the STRIP SYNC bit is cleared.

NOTE

The SCH SYNC bit must remain set for the duration of the message. If not, the character being received at the time of the on to off transition will be lost along with synchronization.

If the programmer wishes the RCVR to discard all sync characters after synchronization is achieved, the STRIP SYNC bit in the RXCSR must be set. The STRIP SYNC bit inhibits the RX DONE interrupt whenever a sync character is received with no errors; however, the sync character is still held in the RXDBUF until the next character is received.

If the program fails to read the RXDBUF in response to a RX DONE interrupt, overrun errors will occur. When the RXDBUF is not serviced in the time required to receive the next character, i.e., (1/baud rate × bits per character) seconds, the character presently being held in the RXDBUF is overwritten by the next received character and the OVRN ERR (overrun error) bit is set in the RXCSR.

NOTE

The information in the following paragraph must be strictly adhered to or RCVR synchronization problems will be encountered.

If the DUV11 is configured to achieve synchronization on two contiguous sync characters then receiver operation may be terminated (after the entire message is received) by simply clearing the SCH SYNC bit in the RXCSR. However, if only one character is required to achieve synchronization, receiver termination is a little more complex. If the SCH SYNC bit is cleared while a sync character is present in the RXDBUF, false synchronization will occur when the receiver is enabled (SCH SYNC bit set) to receive the next message. The program must ensure that this does not happen by transmitting a pad character, i.e., a non-sync character, immediately after the transmission of the terminating control character.

5.4 PROGRAMMING THE RCVR IN THE EXTERNAL SYNCHRONOUS MODE

The external synchronous mode enables the RCVR logic to set to the synchronize state immediately upon the assertion of the SCH SYNC (1) H input. This mode is designed for use with communication equipment capable of accomplishing synchronization external to the DUV11. When the program sets the SCH SYNC bit, the REC ACT bit sets and the RCVR starts framing characters on the very next bit received. When the selected number of bits are received, the received character is transferred into the RXDBUF and the RX DONE bit is set causing an interrupt request. All other features and parameters of the internal synchronous mode apply to this mode also.

5.5 PROGRAMMING THE XMTR IN THE ISOCHRONOUS MODE

5.5.1 Loading the PARCSR

Once the XMTR is initialized via BUS INIT or MSTRST, the PARCSR must be programmed to select the mode of operation (isochronous in this case), character length, and parity. It is not necessary to load the sync register in this mode as sync characters are not required to achieve synchronization and the transmitter is not required to transmit continuously.

5.5.2 Enabling the XMTR

When the required handshaking is complete, the program sets the SEND and TX INTEB bits and loads a character into the TXDBUF. The XMTR adds the START and STOP bits and transmits the character to the modem. As soon as the first character bit is placed on the communication line by the XMTR, the TX DONE bit is asserted and remains asserted until the XMTR services the TXDBUF or clears the SEND bit.

5.6 PROGRAMMING THE RCVR IN THE ISOCHRONOUS MODE

RCVR operation is initiated by the assertion of SCH SYNC. When the program sets the SCH SYNC bit, the REC ACT bit sets and the RCVR starts framing characters upon receipt of the START bit from the XMTR. When the selected number of character bits are received, the RCVR tests the line for a valid STOP bit, transfers the received character into the RXDBUF (minus the start and stop bits), and sets the RX DONE bit. If the STOP bit is not detected, the FRM ERR (framing error) bit is also set. If the program fails to service the RXDBUF before the next character is framed, the OVRN ERR bit is set.

CHAPTER 6
MAINTENANCE

6.1 SCOPE
This chapter lists required test equipment and provides a complete description of DUV11 preventive and corrective maintenance procedures.

6.2 MAINTENANCE PHILOSOPHY
Basically, DUV11 maintenance consists of preventive and corrective maintenance procedures, diagnostic programs, and a maintenance log. The preventive maintenance procedures are performed regularly in an attempt to detect any deterioration due to aging and any damage caused by improper handling of the module. The corrective maintenance procedures are performed to isolate and repair faults in module circuitry only after it has been determined that the module is faulty. The maintenance log is used to record all maintenance activities for future reference and analysis; hopefully, the log will facilitate future maintenance action and aid in detecting any component failure pattern that may develop.

6.3 PREVENTIVE MAINTENANCE
Preventive maintenance consists of tasks performed at periodic intervals to ensure proper equipment operation and minimum unscheduled downtime. These tasks consist of running diagnostics, visual inspection, operational checks, and replacement of marginal components.

NOTE
There will be no scheduled PM specifically for the DUV11-DA. Preventive maintenance should be done in conjunction with scheduled system PMs.

The preventive maintenance schedule depends on the environmental and operating conditions that exist at the installation site. Under normal conditions, recommended preventive maintenance consists of inspection and cleaning every 600 hours of operation or every 4 months, whichever occurs first. However, relatively extreme conditions of temperature, humidity, dust, and/or abnormally heavy work loads demand more frequent maintenance. In any case, the diagnostic programs should be run once per week as part of the normal preventive maintenance schedule.

6.4 TEST EQUIPMENT REQUIRED
Maintenance procedures for the DUV11 require the standard test equipment and diagnostic programs listed in Table 6-1, in addition to standard hand tools, cleaners, test cables, and probes.

6.5 CORRECTIVE MAINTENANCE
The corrective maintenance procedures are designed to aid the maintenance technician in isolating and repairing faults within the DUV11 module. Hence, the technician must be otherwise equipped to determine that the DUV11 is, in fact, at fault.

Table 6-1 Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 453
X10 Probes (2)	Tektronix	P6008
Module Extender	DIGITAL	W984 (Quad Height)
Modem Test Connector	DIGITAL	H315A
Diagnostic (Maindecs)	DIGITAL	MAINDEC-11-DZDUQ through MAINDEC-11-DZDUV

The diagnostic programs comprise the basic tool used by the technician to isolate faults. The diagnostics exercise the DUV11 in three distinct maintenance modes and provide printouts indicating the results. The printouts point the technician to a particular logic area such as the XMTR or RCVR logic. The technician uses standard test equipment (scope and probe) to further isolate the fault to a specific circuit component.

6.5.1 Maintenance Modes

The three maintenance modes are:

1. System Test
2. Internal Loop
3. External Loop.

6.5.1.1 System Test Mode – This mode is selected by the system test diagnostic program. The system test diagnostic exercises all devices and interfaces connected to the Q BUS and is run with the DUV11 connected to the modem. The following operations are performed to exercise the DUV11 (Figure 6-1):

1. The system test clock located within the DUV11 is enabled [MS01 (1) H and MS00 (1) H asserted] and provides clock pulses to the RCVR and XMTR.

2. The XMTR and RCVR are enabled [SEND (1) H and SCH SYNC (1) H asserted].

3. A character is loaded into the TXDBUF.

4. The XMTR output (SERIAL DATA OUT H) is routed to the RCVR via the RCVR input select logic.

5. The program monitors the RX DONE and the RXDBUF for errors.

6.5.1.2 Internal Loop Mode – This mode is designed to isolate the faults within the DUV11 to one of the following logic areas:

1. XMTR
2. RCVR
3. DNA
4. TX DONE
5. RX DONE
6. Synchronization.

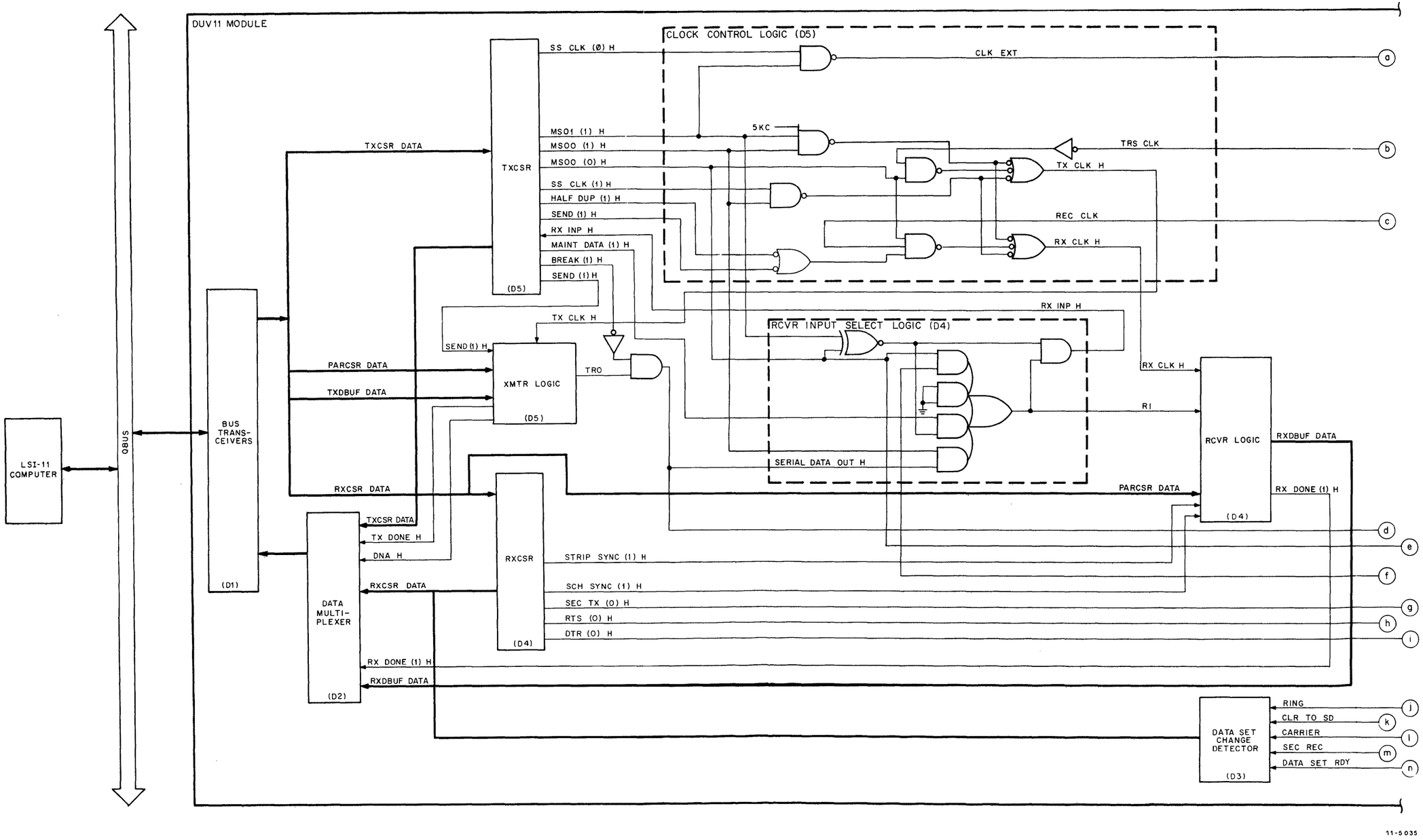


Figure 6-1 Maintenance Diagram
(Sheet 1 of 2)

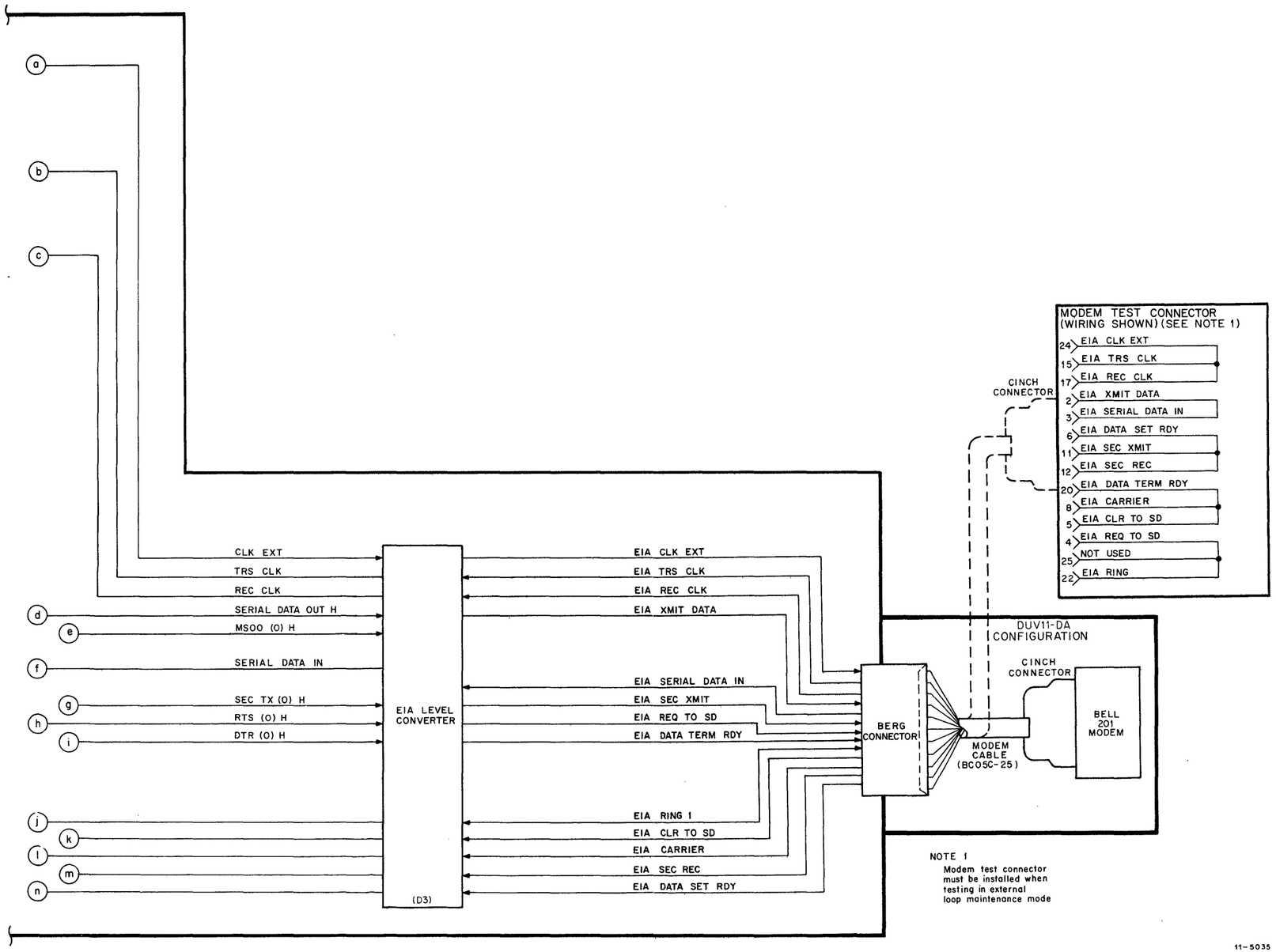


Figure 6-1 Maintenance Diagram
(Sheet 2 of 2)

The internal loop maintenance mode enables the program to exercise the interface logic without physically disconnecting the interface from the modem. This is made possible by maintenance mode logic that electrically inhibits the clock and data channels [MS00 (0) H cleared] between the interface and the modem. Note, however, that the modem control lines are not inhibited; therefore, care must be taken when this mode is programmed not to activate any of the modem control lines.

When the internal loop maintenance mode is programmed, the maintenance mode select bits (MS01, MS00) establish the required operating conditions as follows (Figure 6-1 and engineering drawings D4 and D5):

1. MS00 (0) H is cleared thus inhibiting the modem clock inputs (TRS CLK and REC CLK), the modem input to the RCVR input select logic (SERIAL DATA IN), and the XMTR output to the modem (SERIAL DATA OUT H).

2. MS01 (1) H and MS00 (0) H are cleared thus enabling the program input to the RCVR via the RCVR input select logic [MAINT DATA (1) H] and the RX INP H input to the TXCSR.

NOTE

When programming the internal loop maintenance mode, ensure that SERIAL DATA OUT H is disabled (BREAK bit set) whenever the MAINT DATA (1) H input to the RCVR input select logic is active.

3. MS00 (1) H is asserted thus enabling the programmable single step clock input [SS CLK (1) H] to drive the RCVR and XMTR and the XMTR output to the RCVR via the RCVR input select logic (SERIAL DATA OUT H).

Once the operating conditions are established, the program performs the following operations:

1. The single step clock is programmed (by alternately setting and clearing the SS CLK bit) to provide clock pulses to the RCVR and XMTR.

2. The RCVR and XMTR are enabled.

3. A character is loaded into the TXDBUF.

4. The XMTR then serially outputs the character to the RCVR via the SERIAL DATA OUT H line.

The program then monitors the RX INP bit, the RX DONE bit, and the RXDBUF for errors. To further isolate any errors that may be detected, the program sets the BREAK bit and inputs data directly to the RCVR via the MAINT DATA (1) H line.

6.5.1.3 External Loop Mode – This mode is designed to isolate faults occurring in the cabling connecting the DUV11 to the modem, as well as faults within the DUV11 level converters and data set change detector logic. Before this mode can be executed the interface must be physically disconnected from the modem and the modem test connector (H315A) installed at the modem end of the BC05C modem cable. Figure 6-1 illustrates the proper installation of the modem test connector.

When the external loop maintenance mode is programmed, the maintenance mode select bits establish the required operating conditions as follows (Figure 6-1 and engineering drawings D4 and D5):

1. MS00 (0) H is asserted thus enabling the TRS CLK and REC CLK inputs to the clock control logic, the SERIAL DATA IN input to the RCVR input select logic and the XMTR output to the modem test connector (SERIAL DATA OUT H).

2. MS01 (1) H and MS00 (0) H are asserted thus enabling the program input to the RCVR via the RCVR input select logic [MAINT DATA (1) H] and the RX INP H input to the TXCSR.

NOTE

When programming the external loop maintenance mode, care must be taken to ensure that SERIAL DATA OUT H is disabled (break bit set) whenever the MAINT DATA (1) H input to the RCVR input select logic is active.

3. MS01 (1) H is asserted thus enabling the programmable single step clock input [SS CLK (0) H] to drive the RCVR and XMTR via CLK EXT output to the modem test connector.

Once the operating conditions are established, the program performs the following operations to check out the modem cabling.

1. The single step clock is programmed to activate the EIA CLK EXT output which is looped back by the modem test connector and applied to the TRS CLK and REC CLK input lines.

2. The RCVR and XMTR are enabled.

3. A character is loaded into the TXDBUF.

4. The XMTR then serially outputs the character to the modem test connector, which loops it back to the interface where it is applied to the RCVR via the SERIAL DATA IN line.

The program then monitors the RX INP bit, the RX DONE bit, and the RXDBUF for errors. To further isolate any errors that may be detected, the program sets the BREAK bit and inputs data directly to the RCVR via the MAINT DATA (1) H line.

To check out the modem control lines, the program individually sets and clears the modem control bits (bits 01, 02, and 03 in the RXCSR) and monitors the modem control lines and the DATA SET CH bit for errors.

2.1.6 Option Switches

The DUV11 contains a set of switches which control additional system functions and optional features. Table 2-4 lists these switches (all contained in switch bank E55), and explains their use.

Table 2-4 Switch Assignments

Switch Number*	Function
SW1	Optional Clear – Switch ON enables CLR OPT, which is used to clear RXCSR bits 03, 02, and 01.
SW2	Secondary Transmit – Switch ON enables secondary data channel between the modem and DUV11.
SW3	Secondary Receive – Switch ON enables secondary data channel between the modem and DUV11.
SW4	Sync Characters – Switch ON enables the receiver to synchronize internally upon receiving one sync character. The normal condition of receiving two sync characters exists when SW4 is off.
SW5	Special Feature – Switch ON allows external clock to be internally generated, used when a modem is not being utilized.
SW6	Special Feature – Optional feature is switched ON for program control of data rate selection.
SW7	Maintenance Clock – Switch ON enables the clock that is used for maintenance purposes only.
SW8	Not Used.

*All switches are located on component reference designation E55.

2.2 INITIAL TESTING

The DUV11-DA must be tested prior to placing the unit into operation. For initial test procedures, refer to the engineering specification, A-SP-DUV11-0-2, provided with each DUV11 delivered.

NOTE

Before running diagnostics on interface, disconnect the modem cable (BC05C-25) from the rear of the modem and install the modem test connector H315A as shown in Figure 2-7.

Testing may be performed without removing the BC05C-25 cable from the modem. However, in this mode the EIA line receivers and drivers cannot be tested.

APPENDIX A
REPRESENTATIVE MODEM FACILITIES AVAILABLE

Manufacturer	Model	Speed (Maximum)	Half or Full Duplex	Sync or Async	Type of Line	Comments
Bell System	103A	300 baud	Full Duplex	Async	DDD	
Bell System	103E	300 baud	Full Duplex	Async	DDD	Similar to 103A
Bell System	103F	300 baud	Full Duplex	Async	Private	
Bell System	113A	300 baud	Full Duplex	Async	DDD	Originate Only
Bell System	113B	300 baud	Full Duplex	Async	DDD	Answer Only
Bell System	201A	2000 baud	Either	Sync	DDD	Full Duplex on 2 calls
Bell System	201B	2400 baud	Either	Sync	Private	
Bell System	202B	1800 baud	Either	Async	DDD	
Bell System	202C	1200 baud	Either	Async	DDD	Full Duplex on 2 calls
Bell System	202D	1800 baud	Either	Async	Private	
Bell System	205B	600 baud 1200 baud 2400 baud	Full Duplex	Sync	Private	
Bell System	202E Series	1200 baud	Trans Only	Async	DDD Private	
Bell System	301B	40,800 baud	Either	Sync	Private Wire Band	
Bell System	303B, C, D, E	19,000 to 230,400 baud	Either	Sync	Private Wide Band	
Bell System	811B	110 baud	Either	Async	TWX Network	
Western Union	118-1A	180			Telegraph	
Western Union	1601-A	600			Voice	
Western Union	2121-A	1200			Voice Broad Band	
Western Union	2241-A	2400	Either	Either	Broad Band	
Western Union	100	200	Either	Async	Voice	
Western Union	100	2400	Either	Async	Voice	
Western Union	300	18,000 40,000	Either	Sync	Broad Band	
Rixon	FM-12	1200	Either	Either	Voice Bell 4A	
Rixon	Sebit 48	4800	Either	Sync	Voice Bell 4C	
General Electric	TDM 220	2400	Either	Either	Private Bell 4B	

APPENDIX B
LSI INTEGRATED CIRCUIT DESCRIPTIONS

B.1 INTRODUCTION

LSI integrated circuits (ICs) shown in the engineering drawings for the DUV11 are covered in this appendix. These descriptions are intended as maintenance aids for troubleshooting to the IC level.

B.2 PR1472B SYNCHRONOUS RECEIVER (P/SAR)

The P/SAR is a programmable receiver that interfaces variable length, serial-to-parallel data channel. The receiver converts a serial data stream into parallel characters with a format compatible with all standard synchronous, asynchronous, or isochronous data communications media.

Figure B-1 is a block diagram of the P/SAR. The P/SAR internal control memory, programmable from the device terminals, consists of a control register and a match-character holding register. Contiguous synchronous serial characters are compared in a programmable match-character holding register, character synchronized and assembled.

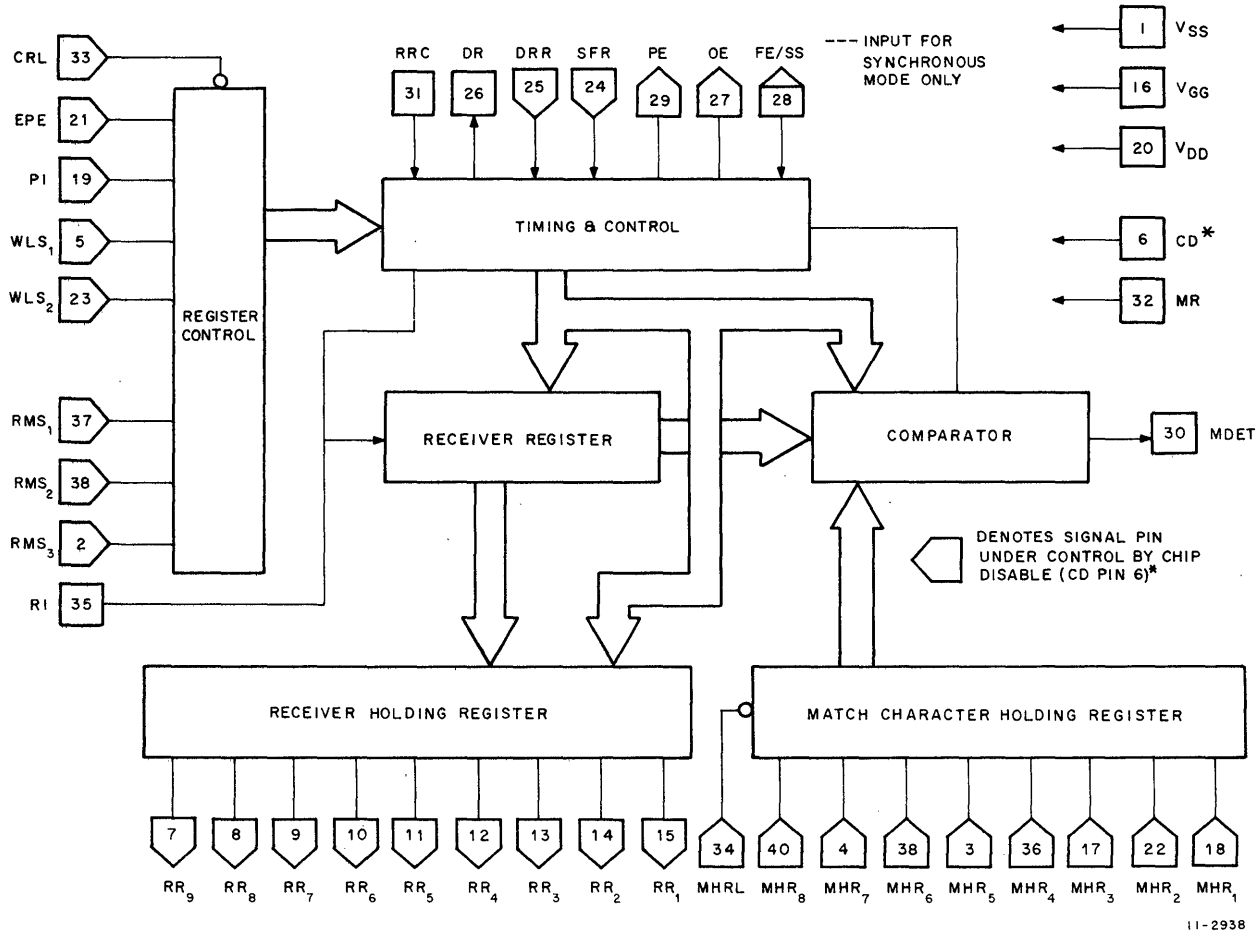


Figure B-1 PR1472B Programmable Synchronous Receiver (P/SAR)

The receiver holding register, a buffer storage register with an associated data received flag, provides an entire serial character time for servicing (unloading) the receiver. The match-character holding register, in conjunction with the comparator, compares the serial data stream, provides an output when the input bit pattern matches the contents of the match-character holding register and causes character synchronization. A master reset is provided.

P/SAR signal mnemonics are listed in Table B-1 and described in detail in Table B-2. Pin connections are shown in Figure B-2.

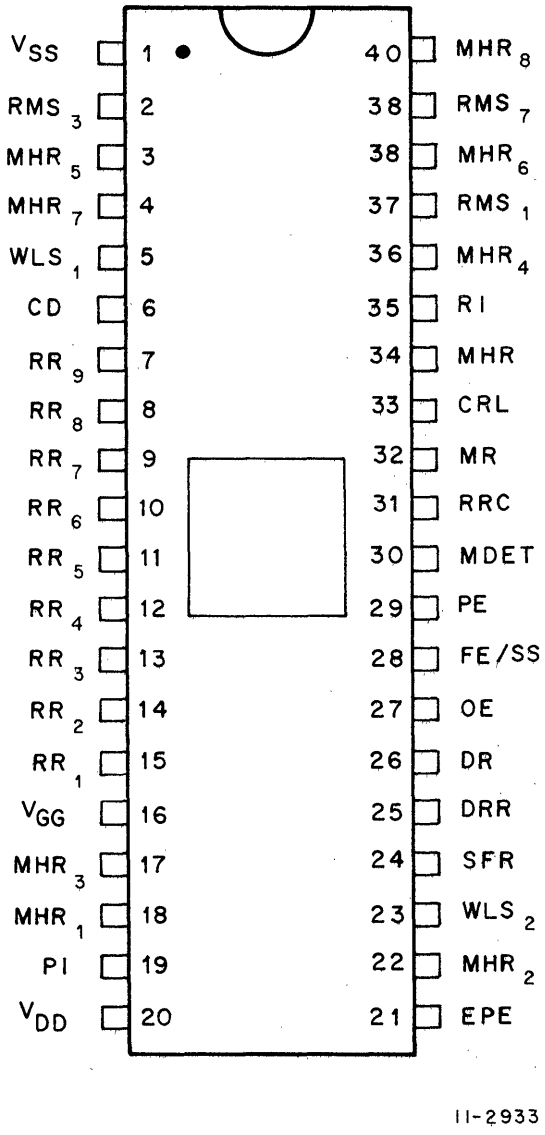


Figure B-2 P/SAR Pin Connections

Table B-1 P/SAR Signal Mnemonics

Input/Output Name	Input/Output Symbol
Power Supply	VSS, VDD, VGG
Receiver Mode Select	RMS_1, RMS_2, RMS_3
Match-Character Holding Register	MHR_1–MHR_8
Word Length Select	WLS_1–WLS_2
Chip Disable	CD
Receiver Holding Register Data	RR_1–RR_9
Parity Inhibit	PI
Even Parity Enable	EPE
Status Flag Reset	SFR
Data Received Reset	DRR
Data Received	DR
Overrun Error	OE
Framing Error	FE
Sync Search	SS
Parity Error	PE
Match Detect	MDET
Receiver Register Clock	RRC
Master Reset	MR
Control Register Load	CRL
Match-Character Holding Register	MHRL
Load Receiver Input	RI

Table B-2 P/SAR Signals

Pin Number	I/O Name	Symbol	Function
1	V_{SS} POWER SUPPLY	V_{SS}	+5 V Supply
37, 39, 2	RECEIVER MODE SELECT	RMS_1,RMS_2, RMS_3	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables RMS_1, RMS_2, and RMS_3 inputs. The Receiver Mode Select Inputs, in conjunction with the Control Register Load Strobe selects the Receiver operating mode. RMS_1, RMS_2, and RMS_3 are left high (connected internally to V_{IH} via a pull-up resistor) to select the sync-internal operating mode.
18, 22 17, 36, 3 38, 4, 40	MATCH-CHARACTER HOLDING REGISTER DATA	MHR_1,MHR_2, MHR_3,MHR_4, MHR_5,MHR_6, MHR_7,MHR_8	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs to the match-character holding register and load strobe, MHRL. Parallel 8-bit characters are input into the match-character holding register with the MHRL strobe (pin 34). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. These inputs are switch selectable to the appropriate input voltage.
5, 23	WORD LENGTH SELECT	WLS_1,WLS_2	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs of the control register and load strobe, CRL. Parallel 8-bit characters are input into the control register with the CRL strobe (pin 33), WLS_1 and WLS_2 select the transmitted character length from five to eight bits defined by the following truth table. WLS_1 / WLS_2 / Selected Word Length V_{IL} V_{IL} 5 bits V_{IL} V_{IH} 6 bits V_{IH} V_{IL} 7 bits V_{IH} V_{IH} 8 bits WLS_1 and WLS_2 are switch selectable to the appropriate input voltage.

Table B-2 P/SAR Signals (Cont)

Pin Number	I/O Name	Symbol	Function
6	CHIP DISABLE	CD	This line controls the disable associated with busable inputs and tristate outputs. A high-level input voltage, V_{IH}, applied to this line disables inputs and removes drive from push-pull output buffers causing them to float. Drivers of disables outputs are not required to sink or source current. The I/O lines controlled by chip disable are defined below. Input Lines / Tristate Output Lines CRL / PE EPE / FE PI / OE WLS_1–WLS_2 / RR_1–RR_8 RMS_1–RMS_3 DRR SFR MHRL MHR_1–MHR_8
7–15	RECEIVER HOLDING REGISTER DATA OUTPUT	RR_9–RR_1	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the receiver holding register outputs, RR_1–RR_9. The parallel data character, including parity (RR_9), appears on these lines. Program control selection of a word length less than eight bits will cause the most significant bits of the character to be forced to a low-level output voltage, V_{OL}. The character will be right justified RR_1 (pin 15) is the least significant bit of the character.
16	V_{GG} POWER SUPPLY	V_{GG}	–12 V Supply.
19	PARITY INHIBIT	PI	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the EPE and PI inputs.

Table B-2 P/SAR Signals (Cont)

Pin Number	I/O Name	Symbol	Function
21	EVEN PARITY ENABLE	EPE	The even parity enable input and parity inhibit input to the control register, in conjunction with the control register load strobe, select even, odd or no parity to be verified by the receiver. A high-level input voltage, V_{IH}, applied to EPE selects even parity if a low-level input voltage, V_{IL}, selects odd parity if a low-level input voltage is applied to parity inhibit. PI and EPE are switch selectable to the appropriate input voltage. PI — EPE — Selected Parity V_{IL} — V_{IL} — ODD V_{IL} — V_{IH} — EVEN V_{IH} — X — NONE X – either V_{IL} or V_{IH}. When programmed, the appropriate parity is verified following the last data bit of a character.
24	STATUS FLAG RESET	SFR	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the SFR input. A low-level input voltage, V_{IL}, applied to this line resets the PE and OE status flags.
25	DATA RECEIVED RESET	DRR	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the SFR input. A low-level input voltage, V_{IL}, applied to this line resets the DR flag.
26	DATA RECEIVED FLAG	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the receiver holding register. When operating in the synchronous mode, the first SYN character, when located and transferred to the receiver holding register, will not cause DR to go to a high-level output voltage, V_{OH}, but will cause MDET to go to a high-level output voltage. Character transfer to the receiver holding register occurs in the center of the last bit of a synchronous character, at which time this flag is updated.

Table B-2 P/SAR Signals (Cont)

Pin Number	I/O Name	Symbol	Function
27	OVERRUN ERROR FLAG	OE	A low-level input voltage. V_{IL}, applied to CD (pin 6) enables the OE output. A high-level output voltage, V_{OH}, indicates that the previously received character was not read (DR line not reset) and was, therefore, lost before the present character was transferred to the receiver holding register. This transfer occurs in the center of the last bit of a received synchronous character, at which time this flag is updated.
28	FRAMING ERROR/ SYN SEARCH	FE/SS	FE/SS is a two-way (I/O) bus. When programmed for the SYNCHRONOUS MODE, this line is an input and is not under control of CD. This line should be driven by a tristate or an open collector device. If programmed for INTERNAL CHARACTER SYNCHRONIZATION, a transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, initiates the automatic internal SYN character search operation. Prior to initiation of this operation, the receiver holding register is transparent so that its contents are identical to that of the RECEIVER REGISTER. Upon receipt of a SYN character, (previously loaded into the match-character holding register during initialization), the receiver holding register becomes non-transparent, the MATCH DETECT output (MDET) goes to a high-level output voltage, V_{OH}, but, the data received (DR) flag does not assume a high-level output voltage, V_{OH}. The P/SAR is now in character synchronization. Subsequent SYN or data character will be transferred to the RECEIVER HOLDING REGISTER as they are assembled (at the center of the last bit) and the DR FLAG will be raised. A transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, causes the P/SAR to lose character synchronization and forces the receiver holding register to become transparent.

Table B-2 P/SAR Signals (Cont)

Pin Number	I/O Name	Symbol	Function
29	PARITY ERROR FLAG	PE	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the PE output. Parity, if programmed, is verified upon receipt of the center of the parity bit which is the last bit of a synchronous character. If a parity error exists, the associated PE register is set to a high-level output voltage, V_{OH}.
30	MATCH DETECT FLAG	MDET	A high-level output voltage, V_{OH}, indicates that the contents of the receiver register are identical to the contents of the match-character holding register. This flag is set to a high-level output voltage, V_{OH}, at the center of the last bit of a synchronous character.
31	RECEIVER REGISTER CLOCK	RRC	This fifty percent duty cycle clock provides the basic receiver timing. The negative transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, shifts data into the RECEIVER REGISTER at a bit rate determined by RMS_1, RMS_2, and RMS_3. Synchronous operation requires that this negative transition occur at the center of each data bit.
32	MASTER RESET	MR	A high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets the contents of the receiver holding register to a high-level output voltage, V_{OH}, resets the contents of the match-character holding register, the MDET, DR, PE, FE, and OE outputs to a low-level output voltage, V_{OL}, but does not effect the contents of the control register.
33	CONTROL REGISTER LOAD STROBE	CRL	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the CRL input. A low-level input voltage, V_{IL} applied to this line enables inputs to dc D type Latches of the control register and loads it with control bits (EPE, PI, RMS_1, RMS_2, RMS_3, WLS_1, WLS_2). This line is hard-wired to a low-level input voltage, V_{IL}.

Table B-2 P/SAR Signals (Cont)

Pin Number	I/O Name	Symbol	Function
34	MATCH CHARACTER HOLDING REGISTER LOAD STROBE	MHRL	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the MHRL input. A low-level input voltage, V_{IL}, applied to this line enables input to dc D Type latches of the match-character holding register and loads it with the match-character register data, MHR_1–MHR_8. A high-level voltage, V_{IH}, applies to this line disables the match-character holding register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}.
35	RECEIVER INPUT	RI	The serial input data stream received on this line enters the receiver register determined by the character length and parity programmed.

B.2.1 Synchronous Mode Operation

Synchronous data appears as a continuous bit stream of contiguous characters at the input to the receiver with no start or stop bits. Character synchronization (the framing of this continuous bit stream into characters of a predetermined fixed length), must be accomplished by a comparison of this bit stream and a synchronization sequence. The P/SAR is designed to accommodate internal or external character synchronization by program control. Internal character synchronization is used by the DUV11.

An example of synchronous timing is shown in Figure B-3. Device operation is programmed subsequent to being forced into its idle state. The P/SAR will enter a defined idle state when the master reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the receiver holding register is set to a high-level output voltage and all output flags are reset to a low-level output voltage. The MR also causes the contents of the match-character holding register to be reset to a low-level voltage.

The control register is loaded by hard-wiring CRL to a low-level input voltage, which defines the internal synchronous mode of operation and times one clock rate selection, character length and selected parity if required. Table B-3 illustrates all programmable synchronous formats.

Character synchronization from the data stream requires receiver recognition of specific bit pattern(s) which define the relative position of synchronous characters in the data stream and subsequent character assembly.

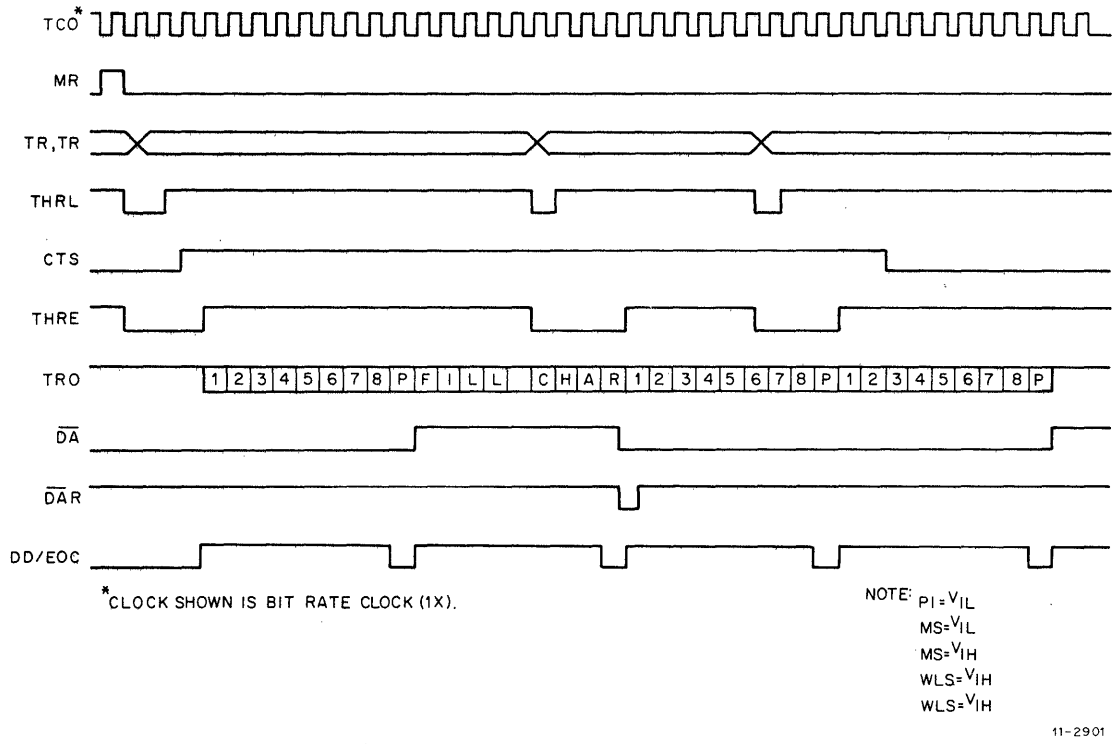


Figure B-3 Synchronous Timing Example (P/SAR)

Table B-3 Sync Mode Control Definition

Control					Character Format	
RMS3	WLS2	WLS1	PI	EPE	Data Bits	Parity Bit Checked
1	0	0	0	0	5	Odd
1	0	0	0	1	5	Even
1	0	0	1	X	5	None
1	0	1	0	0	6	Odd
1	0	1	0	1	6	Even
1	0	1	1	X	6	None
1	1	0	0	0	7	Odd
1	1	0	0	1	7	Even
1	1	0	1	X	7	None
1	1	1	0	0	8	Odd
1	1	1	0	1	8	Even
1	1	1	1	X	8	None
Sets to SYNC Mode						

(When RMS_1 = 1, the receiver operates in the internal character SYNC mode.)

Programmed for internal character synchronization, with a high-level input voltage on the sync search line, the receiver holding register is transparent and its contents are identical to the receiver register. The data stream, gated into the receiver input (RI) by the negative transition of the receiver register clock (RRC), shifts through the receiver register and is compared with the preprogrammed character in the match-character holding register.

A match, indicated by a high-level output voltage on match detect (MDET), returns the receiver holding register to its non-transparent state and initializes timing and control logic, but does not set the data received flag to a high-level output voltage. The character following the match will be transferred to the receiver holding register at the receipt of the center of its last bit and the data received flag is set to a high-level output voltage. Depending on line discipline, this last character may also be a synchronizing character, in which case, MDET will continue to be a high-level output voltage when the data received flag is set. Therefore, sequence verification can be performed by the system. Selection of a word length of less than eight bits causes the most significant bits of the character to be forced to a low level output voltage.

If programmed, parity is verified upon receipt of the center of the parity bit which is the last bit of synchronous character. For word lengths less than eight bits, the parity bit appears immediately to the left of the last bit in the character. If a parity error exists, the associated PE register is set to a high-level output voltage.

Transfer of a character to the receiver holding register sets the associated data received register flag (DR) to a high-level output voltage. If the data received register flag has already been set to a high-level output voltage and has not been cleared by external logic, the transfer of a character to the receiver holding register causes the previous character to be lost (written over) and is alerted by overrun error flag, which is a high-level output voltage. In normal operation, the data received flag is reset by DRR when the receiver holding register is serviced (unloaded). The status flags, PE and OE, are also provided with an external reset SFR. A low-level input voltage on sync search during the negative transition of the RRC causes character synchronization to be lost and initiates transparency of the receiver holding register.

B.3 PT1482B SYNCHRONOUS TRANSMITTER (P/SAT)

The P/SAT is a programmable transmitter that interfaces variable-length, parallel-input data to a serial channel. The transmitter converts parallel characters into a serial data stream with a format compatible with all standard synchronous, asynchronous or isochronous data communications media.

Figure B-4 is a block diagram of the P/SAT. The P/SAT internal control memory, programmable from the device terminals, consists of a control register and a fill (idle) character holding register. Contiguous, serial characters are transmitted, in the synchronous mode, with the automatic insertion of a programmable fill (idle) character during the absence of parallel input data.

The transmitter holding register, a buffer storage register with an associated transmitter holding register empty flag, provides an entire character time for servicing (loading) the transmitter (shift) register. Under internal logic control, the (P/SAT) multiplexer loads data from the transmitter holding register or the fill (idle) character holding register into the transmitter register. A master reset is provided.

P/SAT signal mnemonics are listed in Table B-4 and are described in detail in Table B-5. Pin connections are shown in Figure B-5.

B.3.1 Synchronous Mode Operation

Synchronous transmission requires that characters (programmably variable from 5 to 8 data bits plus parity) are contiguous with no start or stop bits. Since the requirement that characters are contiguous does not imply that the system servicing the transmitter always has ample time to load the transmitter holding register, it is necessary that a character be transmitted when data has not been loaded into the transmitter holding register. This character is defined as the fill or idle character and a separate register has been provided to load this character upon initialization. The fill character holding register is loaded by strobing the fill character holding register load (FHRL) line to a low-level input voltage.

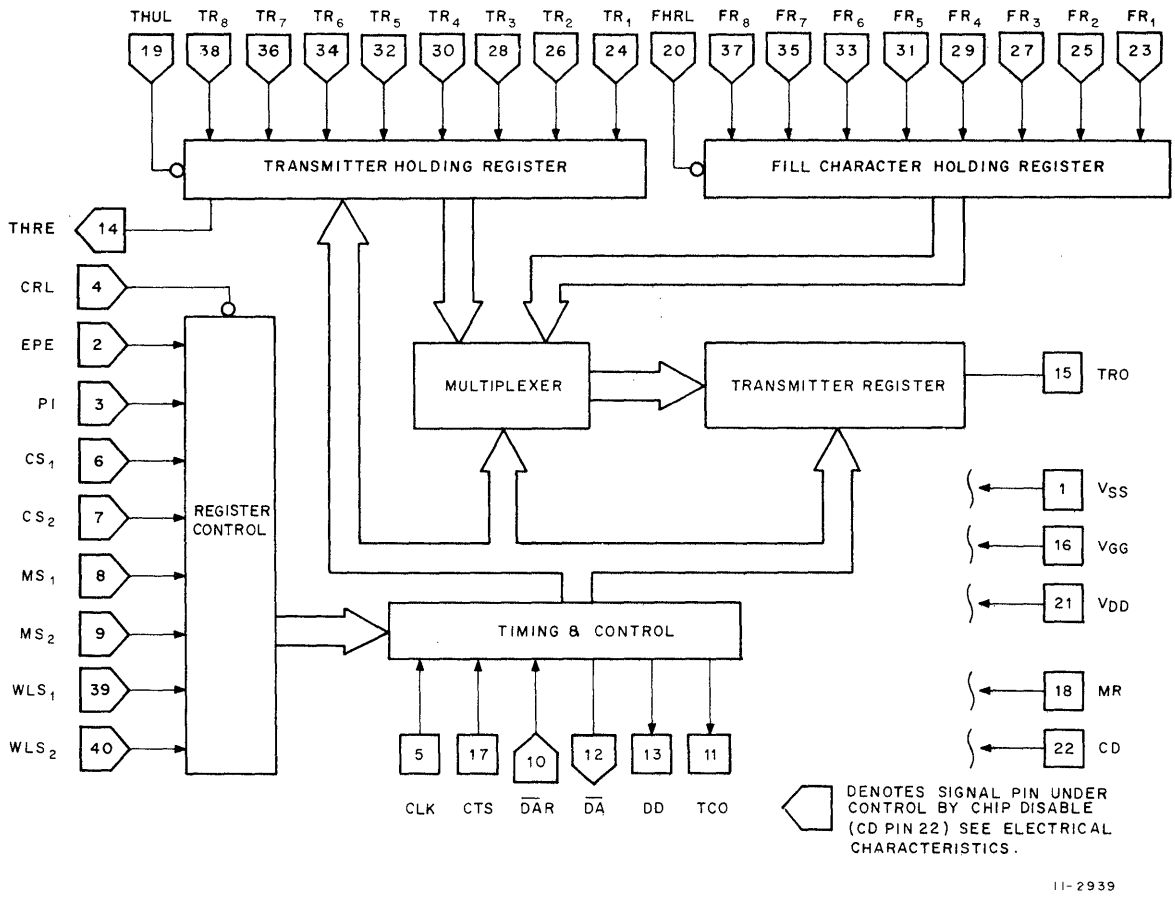


Figure B-4 PT1482B Programmable Synchronous Transmitter (P/SAT)

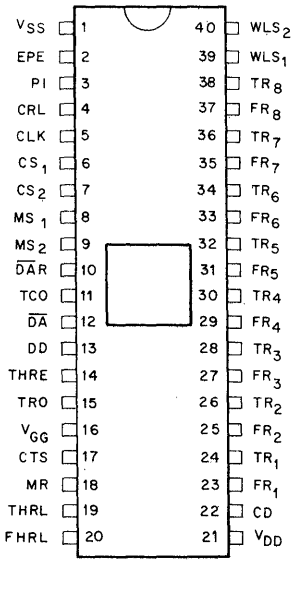


Figure B-5 P/SAT Pin Connections

Table B-4 P/SAT Signal Mnemonics

Input/Output Name	Input/Output Symbol
Power Supply	V_{SS}, V_{DD}, V_{GG}
Even Parity Enable	EPE
Parity Inhibit	PI
Control Register Load	CRL
Clock	CLK
Clock Rate Select	CS_1–CS_2
Mode Select	MS18–MS_2
Data Not Available Reset	DAR
Transmitter Clock Out	TCO
Data Not Available	DA
Data Delimit/End of Character	DD/EOC
Transmitter Holding Register Empty	THRE
Transmitter Register Output	TRO
Clear-To-Send	CTS
Master Reset	MR
Transmitter Holding Register Load	THRL
Fill-Character Holding Register Load	FHRL
Chip Disable	CD
Fill-Character Holding Register Data	FR_1–FR_8
Transmitter Holding Register Data	TR_1–TR_8
Word Length Select	WLS_1–WLS_2

Table B-5 P/SAT Signals

Pin Number	I/O Name	Symbol	Function
1	V_{SS} POWER SUPPLY	V_{SS}	+5 V Supply
2	EVEN PARITY ENABLE	EPE	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the EPE and PI inputs.
3	PARITY INHIBIT	PI	The even parity enable input and the parity inhibit input to the control register load strobe, select even, odd or no parity to be generated by the transmitter. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage is applied to parity inhibit. PI and EPE are switch selectable to the appropriate input voltage. PI EPE Selected Parity V_{IL} V_{IL} ODD V_{IL} V_{IH} EVEN V_{IH} X NONE X – either V_{IL} or V_{IH}. When programmed, the appropriate parity is generated following, and is contiguous with, the last data bit of a character.
4	CONTROL REGISTER LOAD STROBE	CRL	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the CRL input. A low-level input voltage, V_{IL}, applied to this line enables dc latches of the control register and loads it with control bits (EPE, PI, CS_1, CS_2, MS_1, MS_2, WLS_1, WLS_2). This line is hard-wired to a low-level input voltage V_{IL}.
5	TRANSMITTER REGISTER CLOCK	TRC	This is a 50 percent duty cycle clock. The positive going edge of this clock shifts data out of the transmitter register at a times one rate bit as determined by the control bits CS_1 and CS_2, and provides the basic time reference for all device functions.

Table B-5 P/SAT Signals (Cont)

Pin Number	I/O Name	Symbol	Function
6–7	CLOCK RATE SELECT	CS_1–CS_2	A low-level input voltage, V_{IL}, applied to CD enables the CS_1 and CS_2 inputs. These two lines select the internal clock rate divider ratio to produce the transmitter bit rate defined by the truth table below: CS_2 / CS_1 / Selected Clock Input Rate V_{IL} / V_{IL} / 1 × Bit Rate V_{IL} / V_{IH} / 16 × Bit Rate V_{IH} / V_{IL} / 32 × Bit Rate V_{IH} / V_{IH} / 64 × Bit Rate These lines are hard-wired to a low-level input voltage.
8–9	MODE SELECT	MS_1–MS_2	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the MS_1 and MS_2 inputs. These lines select the transmitter operating mode.
10	DATA NOT AVAILABLE RESET	DAR	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the DAR input. A low-level input voltage, V_{IL}, applied to this line resets the data not available flag.
11	TRANSMITTER CLOCK OUTPUT	TCO	This output is a clock at the transmitted bit rate. The negative going edge of this clock corresponds to the center of each transmitted data bit. The positive going edge corresponds to the start of each data bit transition. All waveforms in this specification are referenced to TCO.
12	DATA NOT AVAILABLE FLAG	DA	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the DA input. A high-level output voltage, V_{OH}, on this line indicates that a fill-character has been transmitted, since a character was not loaded into the transmitter holding register by the center of the last bit of a synchronous character.

Table B-5 P/SAT Signals (Cont)

Pin Number	I/O Name	Symbol	Function
13	DATA DELIMIT/ END OF CHARACTER	DD/EOC	A low-level output voltage during synchronous transmission indicates that the last bit of a character is being transmitted.
14	TRANSMITTER HOLDING REGISTER EMPTY	THREE	A low-level input voltage applied to CD (pin 22) enable the THRE input. A high-level output voltage, V_{OH}, on this line indicates the transmitter holding register is empty and has transferred its contents to the transmitter register and may be loaded with a new character. This line goes to a low-level output voltage, V_{OL}, when THRE goes to a low-level input voltage, V_{IL}.
15	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the transmitter holding register are serially shifted out as an NRZ waveform on this line provided that a character was loaded into the transmitter holding register prior to DA flag (in synchronous mode). If a character was not loaded prior to a DA flag, the contents of the fill-character register are transmitted as the next character.
16	V_{GG} POWER SUPPLY	V_{GG}	-12 V supply
17	CLEAR-TO-SEND	CTS	The clear-to-send control initiates or disables transmission as a function of the state of this line. A high-level input voltage, V_{IH}, initiates serial data transmission provided a character has been loaded into the transmitter holding register. A low-level input voltage, V_{IL}, applied to this line during transmission allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.
18	MASTER RESET	MR	The rising edge of a high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets THRE, the contents of the fill-character holding register, and TRO to a high-level output voltage, V_{OH}.

Table B-5 P/SAT Signals (Cont)

Pin Number	I/O Name	Symbol	Function
19	TRANSMITTER HOLDING REGISTER LOAD STROBE	THRL	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the THRL input. A low-level input voltage, V_{IL}, applied to this line enables dc latches of the transmitter holding register and loads it with the transmitter holding register data and forces THRE to a low-level output voltage, V_{OL}. A high-level input voltage, V_{IH}, applied to this line disables the transmitter holding register.
20	FILL-CHARACTER HOLDING REGISTER	FHRL	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the FHRL input. A low-level input voltage, V_{IL}, applied to this line enables dc latches of the fill-character holding register and loads it with the fill-character register data, FR_1–FR_8. A high-level input voltage, V_{IH}, applied to this line disables the control register. This line may be strobed or hardwired to a low-level input voltage, V_{IL}.
21	V_{DD} POWER SUPPLY	V_{DD}	Ground.
22	CHIP DISABLE	CD	This line controls the disconnect associated with busable inputs and tristate outputs. A high-level input voltage, V_{IH}, applied to this line removes drive from push-pull outputs causing them to float. Drivers of disabled inputs are required to sink or source current. The I/O lines controlled by chip disable are defined below. Input Lines — Tristate Output Lines CRL — DA EPE — THRE PI CS_1–CS_2 MS_1–MS_2 DAR THRL FHRL FR_1–FR_8 TR_1–TR_2 WLS_1–WLS_2

Table B-5 P/SAT Signals (Cont)

Pin Number	I/O Name	Symbol	Function
23, 25 27, 29 31, 33 35, 37	FILL-CHARACTER HOLDING REGISTER DATA INPUTS	FR_1–FR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the fill-character holding register and associated load strobe, FHRL. Parallel 8-bit characters are input into the fill-character holding register with the FHRL strobe (pin 20). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2) only the least significant bits are accepted. These inputs are switch selectable to the appropriate input voltage. During synchronous transmission, the fill-character is transmitted if a character was not loaded into the transmitter holding register prior to a DA flag; i.e., the transmitter holding register did not contain a character at the center of the last bit being transmitted from the transmitter register. A high-level input voltage, V_{IL}, will cause a high-level output voltage, V_{OH}, to be transmitted, least significant bit (FR_1) to most significant bit (FR_n) order.
24, 26 28, 30 32, 34 36, 38	TRANSMITTER HOLDING REGISTER DATA INPUTS	TR_1–TR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs to the transmitter holding register and associated load strobe, THRL. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. A high-level output voltage, V_{IH}, will cause a high-level output voltage to be transmitted, least significant bit (TR_1) to most significant bit (TR_n) order.
39–40	WORD LENGTH	WLS_1–WLS_2	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the control register and load strobe, CRL. Parallel 8-bit characters are input into the control register with the CRL strobe (pin 4), WLS and WLS select the transmitted character length from five to eight bits defined by the following truth table.

Table B-5 P/SAT Signals (Cont)

Pin Number	I/O Name	Symbol	Function
			WLS_2 WLS_1 Selected Word Length V_{IL} V_{IL} 5 bits V_{IL} V_{IH} 6 bits V_{IH} V_{IL} 7 bits V_{IH} V_{IH} 8 bits WLS_1 and WLS_2 are switch selectable to the appropriate input voltage.

The P/SAT will enter a defined idle state when the MR is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the transmitter register output continues to mark, the transmitter holding register flag is set to a high-level output voltage, the data delimit/end of character (DD/EOC) flag is set to a low-level output voltage, and the contents of the fill character holding register are forced to a high-level voltage.

An example of synchronous timing is shown in Figure B-6. The control register is loaded by hard-wiring CRL to a low-level input voltage which defines synchronous mode of operation, character length, selected parity if required, and the times one clock rate selection. Table B-6 illustrates all the programmable synchronous character formats.

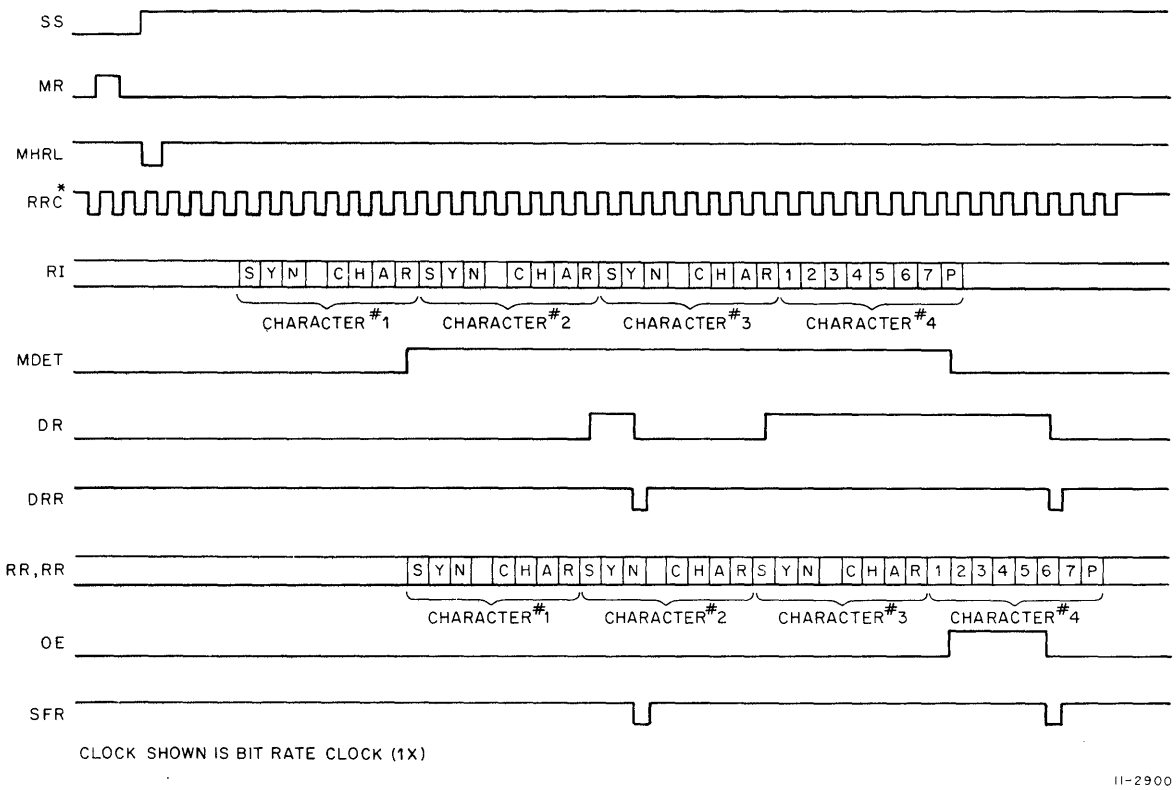


Figure B-6 Synchronous Timing Example (P/SAT)

Table B-6 SYNC Mode Control Definition

Control						Character Format	
MS2	MS1	WLS2	WLS1	PI	EPE	Data Bits	Added Parity Bit
1	0	0	0	0	0	5	Odd
1	0	0	0	0	1	5	Even
1	0	0	0	1	X	5	None
1	0	0	1	0	0	6	Odd
1	0	0	1	0	1	6	Even
1	0	0	1	1	X	6	None
1	0	1	0	0	0	7	Odd
1	0	1	0	0	1	7	Even
1	0	1	0	1	X	7	None
1	0	1	1	0	0	8	Odd
1	0	1	1	0	1	8	Even
1	0	1	1	1	X	8	None
Sets to SYNC mode							

The character transferred into the transmitter register (from the transmitter holding register or the fill character holding register) is determined at the center of the last bit of the character being transmitted.

If, at this time, no character has been loaded into the transmitter holding register, the fill character is loaded into the transmitter register at the end of the bit being transmitted and a data not available (DNA) flag is set to a high-level output voltage. This fill character is loaded into the transmitter holding register, at which time, the DNA flag is reset, the fill character will be completed and the newly-loaded synchronous character will follow contiguously.

A high-level output voltage, on the THRE flag indicates that the transmitter holding register is empty and may be loaded with a character. Data on the inputs of the transmitter holding register is loaded when the transmitter holding register load (THRL) line is strobed to a low-level output voltage. This data must be stable prior to THRL going to a high-level input voltage, since this register is a set of dc latches which are enabled by THRL.

If the clear-to-send (CTS) line is at a low-level input voltage, or if the transmitter register is in the process of transmitting a character, the character in the transmitter holding register will not be transferred down to the transmitter register and the THRE flag will remain at a low-level output voltage.

Raising the CTS line to a high-level input voltage, or completion of transmission of a character from the transmitter register, causes the automatic transfer of the character in the transmitter holding register to the transmitter register which forces the THRE flag to be set to high-level output voltage. The selected parity is added to the data during the transfer to the transmitter register and serial transmission is initiated as an NRZ waveform. A low-level input voltage applied to CTS during transmission allows completion of that character only, after which the device enters the idle state and the output will continue to mark until a high-level input voltage is applied.

The data delimit/end of character flag has been provided to indicate the transmission of serial data on the transmitter register output.

The data delimit/end of character flag is defined as a low-level output voltage during transmission of the last bit of a synchronous character and when the P/SAT is in the idle state.

B.4 DC003 INTERRUPT CHIP

The interrupt chip as shown in Figure B-7 is an 18 pin, 300 center, dip device that provides the circuits to perform an interrupt transaction in a computer system that uses a pass-the-pulse type arbitration scheme. The device is used in peripheral interfaces and provides two interrupt channels labeled A and B, with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or high-drive-open-collector outputs, which allows the device to directly attach to the computer systems bus. Maximum current required from the V_{cc} supply is 140 mA.

Signal mnemonics are listed in Table B-7. Timing diagrams are illustrated in Figures B-8 and B-9.

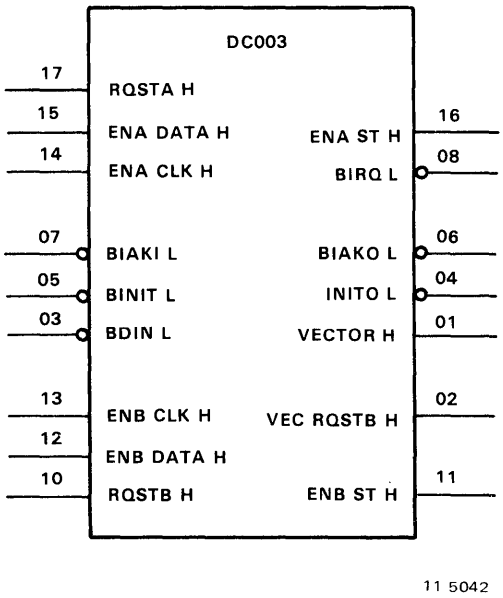


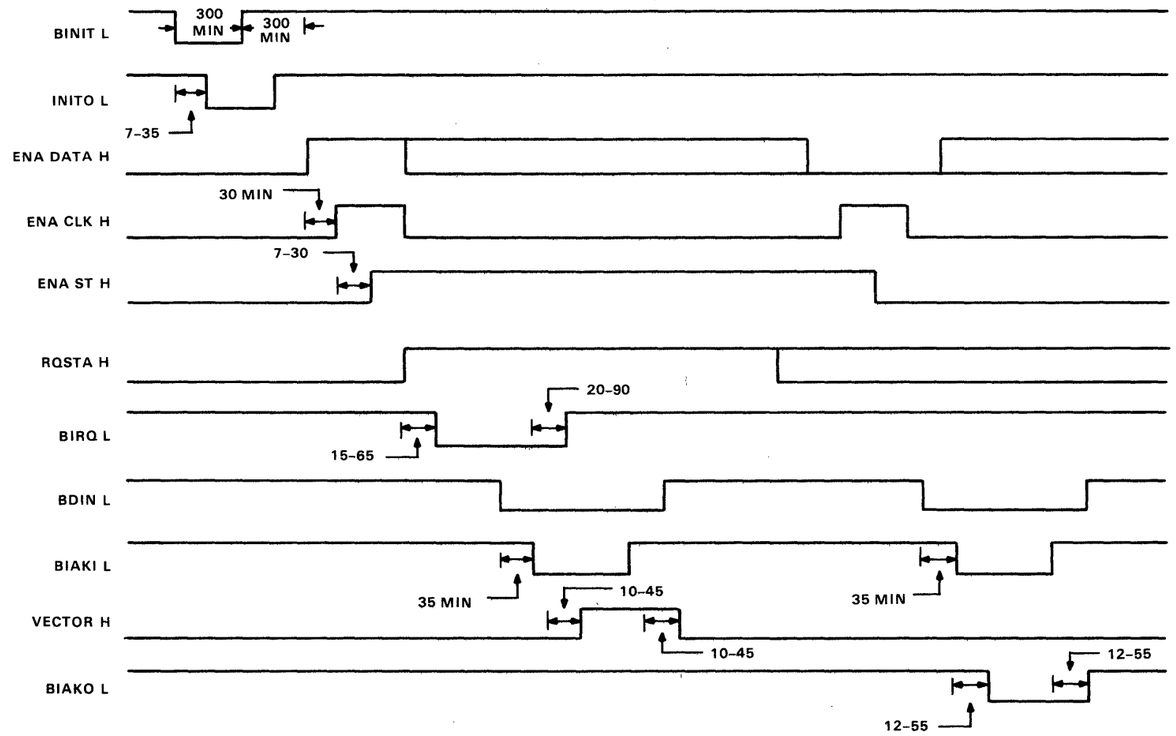
Figure B-7 DC003 Logic Symbol Diagram

Table B-7 DC003 Signals

Pin Number	I/O Name	Symbol	Function
1	INTERRUPT VECTOR GATING SIGNAL	VECTOR H	This signal should be used to gate the appropriate vector address onto the bus and to form the bus signal called BRPLY L.
2	VECTOR REQUEST B SIGNAL	VEC RQSTB H	When asserted indicates RQST B service vector address is required. When unasserted indicates RQST A service vector address is required. VECTOR H is the gating signal for the entire vector address; VEC RQST B H is normally bit 2 of the address.
3	BUS DATA IN	BDIN L	The BDIN signal always precedes a BIAK signal.
4	INITIALIZE OUT	INITO L	This is the buffered BINIT L signal used in the device interface for general initialization.
5	BUS INITIALIZE	BINIT L	When asserted, this signal brings all driven lines to their unasserted state (except INITO L).
6	BUS INTERRUPT ACKNOWLEDGE	BIAKO L	This signal is the daisy-chained signal that is passed by all devices not requesting interrupt service (see BIAKI L). Once passed by a device, it must remain passed until a new BAIKI L is generated.
7	BUS INTERRUPT ACKNOWLEDGE	BIAKI L	This signal is the processor's response to BIRQ L true. This signal is daisy-chained such that the first requesting device blocks the signal propagation while non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.

Table B-7 DC003 Signals (Cont)

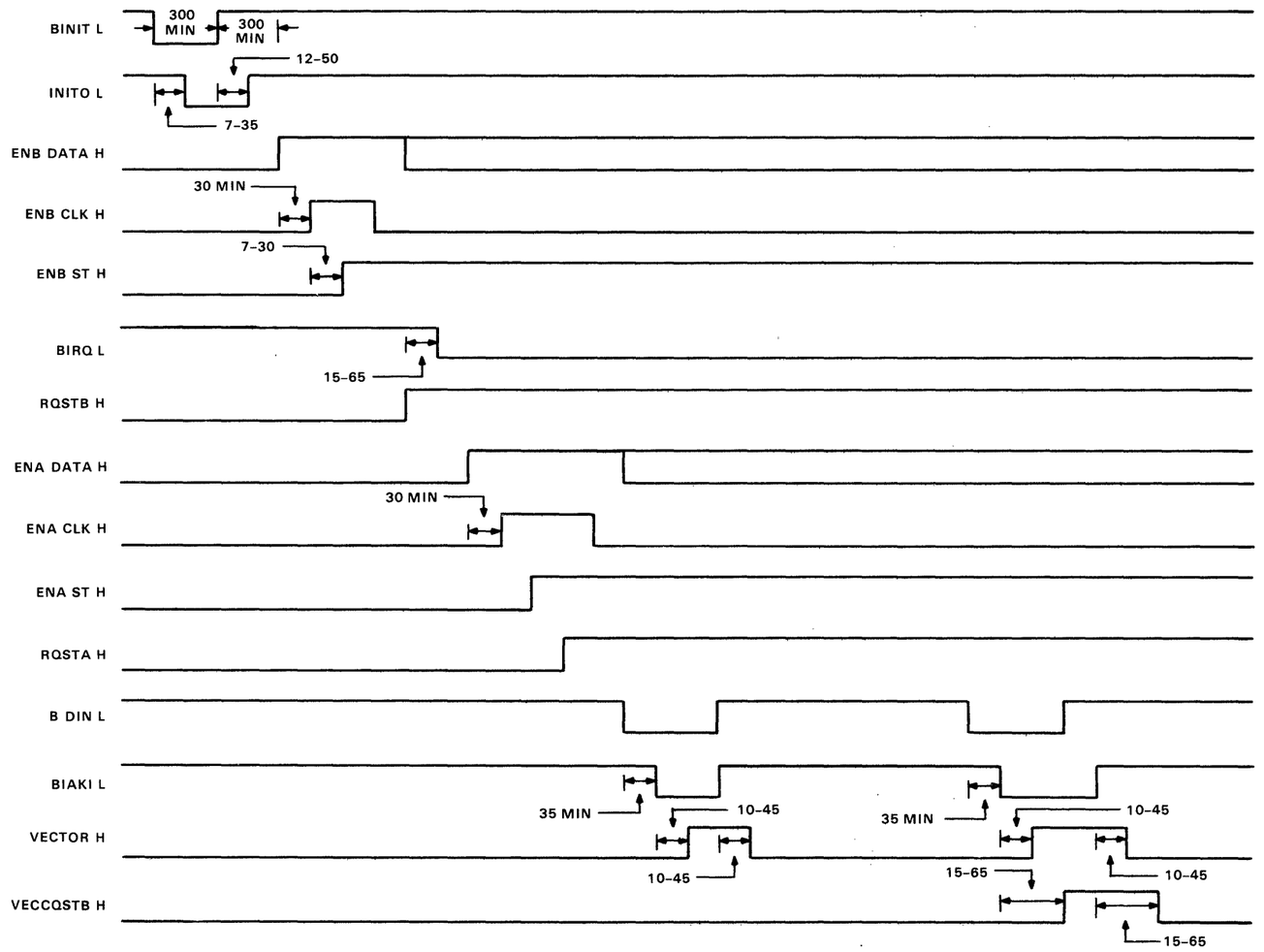
Pin Number	I/O Name	Symbol	Function
8	ASYNCHRONOUS BUS INTERRUPT REQUEST	BIRQ L	The request is generated by a true RQST signal along with the associated true interrupt enable signal. The request is removed after the acceptance of the BDIN L signal and on the leading edge of the BAIKI L signal or the removal of the associated interrupt enable or due to the removal of the associated request signal.
17 10	DEVICE INTERRUPT REQUEST SIGNAL	RQSTA H REQSTB H	When asserted with the enable A flip-flop asserted will cause the assertion of BIRQ L on the bus. This signal line normally remains asserted until the request is serviced.
16 11	INTERRUPT ENABLE	ENA ST H ENB ST H	This signal indicates the state of the interrupt enable A internal flip-flop which is controlled by the signal line ENA DATA H and the ENA CLK H clock line.
15 12	INTERRUPT ENABLE	ENA DATA H ENB DATA H	The level on this line, in conjunction with the ENA CLK H signal, determines the state of the internal interrupt enable A flip-flop. The output of this flip-flop is monitored by the ENA ST H signal.
14 13	INTERRUPT ENABLE	ENA CLK H ENB CLK H	When asserted (on the positive edge), interrupt enable A flip-flop assumes the state of the ENA DATA H signal line.



NOTE: All speeds in nanoseconds.

11-5043

Figure B-8 DC003 Timing Diagram
(Section A Only)



NOTE: All speeds in nanoseconds.

11-5041

Figure B-9 DC003 Timing Diagram
(Sections A & B)

APPENDIX C
INTEGRATED CIRCUITS

The following pages contain reference information for integrated circuits used within DUV11. Logic diagrams, and truth tables in most cases shown. The integrated circuits found in this appendix are:

74LS74
74LS174
74LS175
74LS253
DC004
DC005

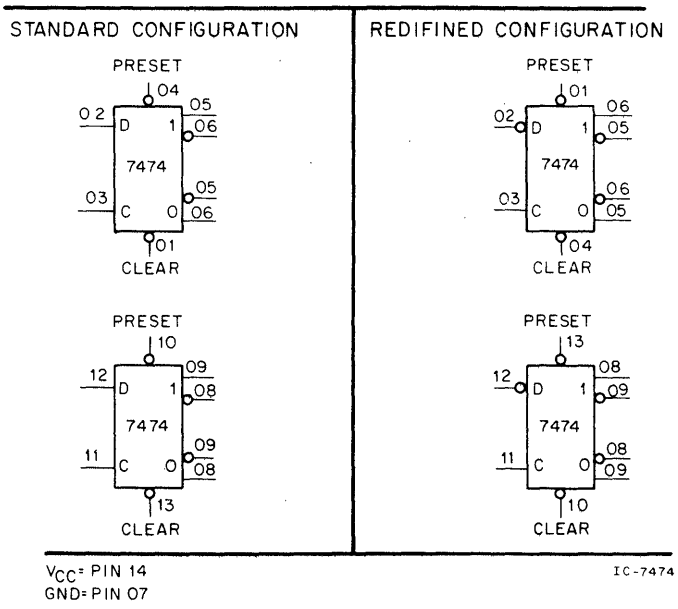
In the case of the DC004 protocol chip and DC005 transceiver, a pictorial of the chip with pin designations is provided.

74LS74 D-TYPE FLIP-FLOP

TRUTH TABLE FOR
7474 STANDARD CONFIGURATION
(EACH FLIP-FLOP)

t_n			t_n+1	
Preset Pin 4(10)	Clear Pin 1(13)	D Input Pin 2(12)	1 Side Pin 5	0 Side Pin 6
High	High	Low	Low	High
High	High	High	High	Low
High	Low	X	Low	High
Low	High	X	High	Low
Low	Low	X	High	High

t_n = bit time before clock pulse.
t_n+1 = bit time after clock pulse.
X = irrelevant



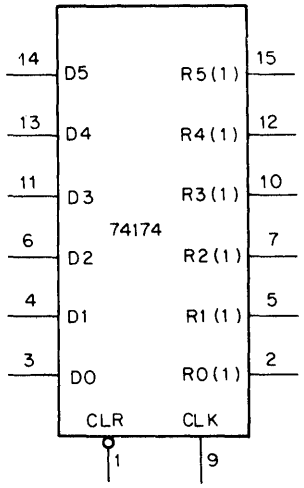
Note: 7474 is shown. LS only signifies low power Schottky.

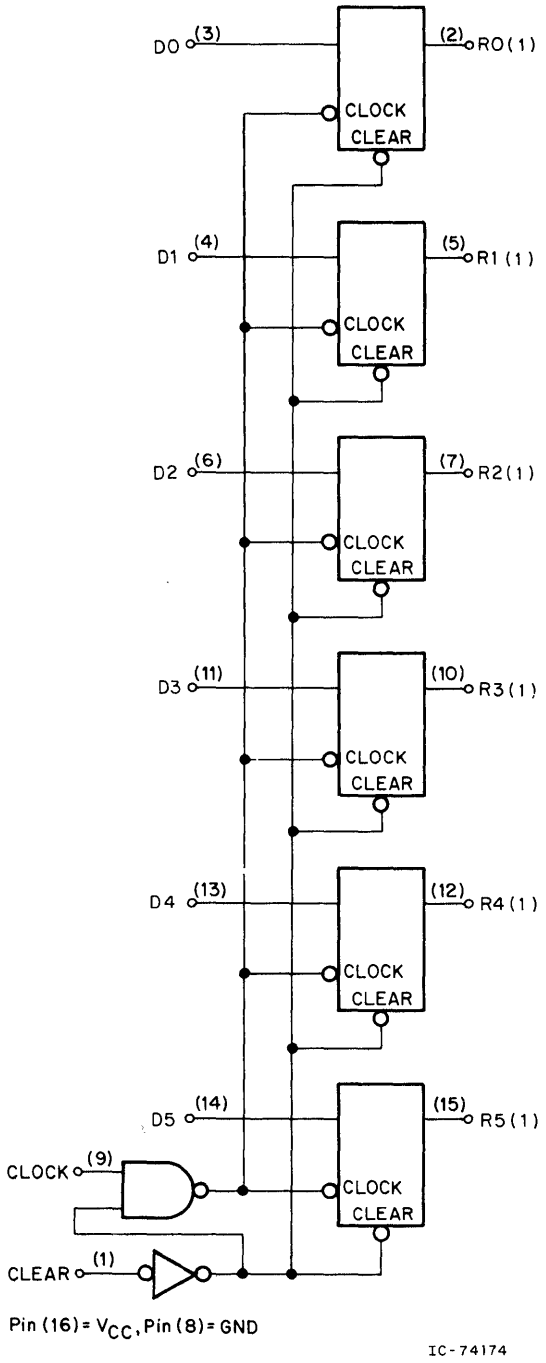
74LS174 HEX D FLIP-FLOP REGISTER

TRUTH TABLE

INPUT t_n D	OUTPUT t_{n+1} R(1)
H	H
L	L

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.





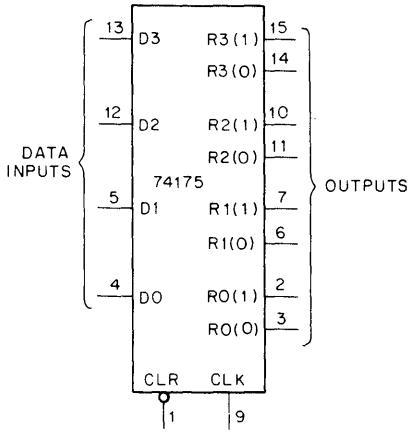
Note: 74174 is shown. LS only signifies low power Schottky.

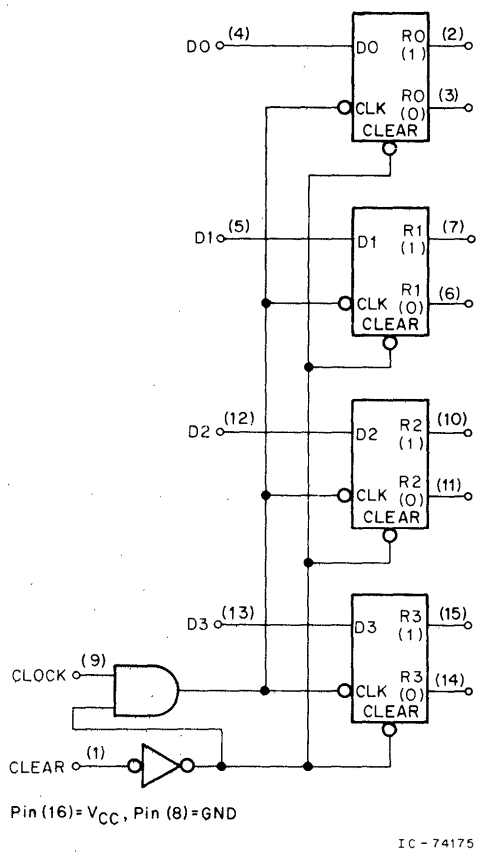
74LS175 QUAD STORAGE REGISTER

TRUTH TABLE

INPUT t_n	OUTPUTS t_{n+1}
D	R(1) R(0)
H	H L
L	L H

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

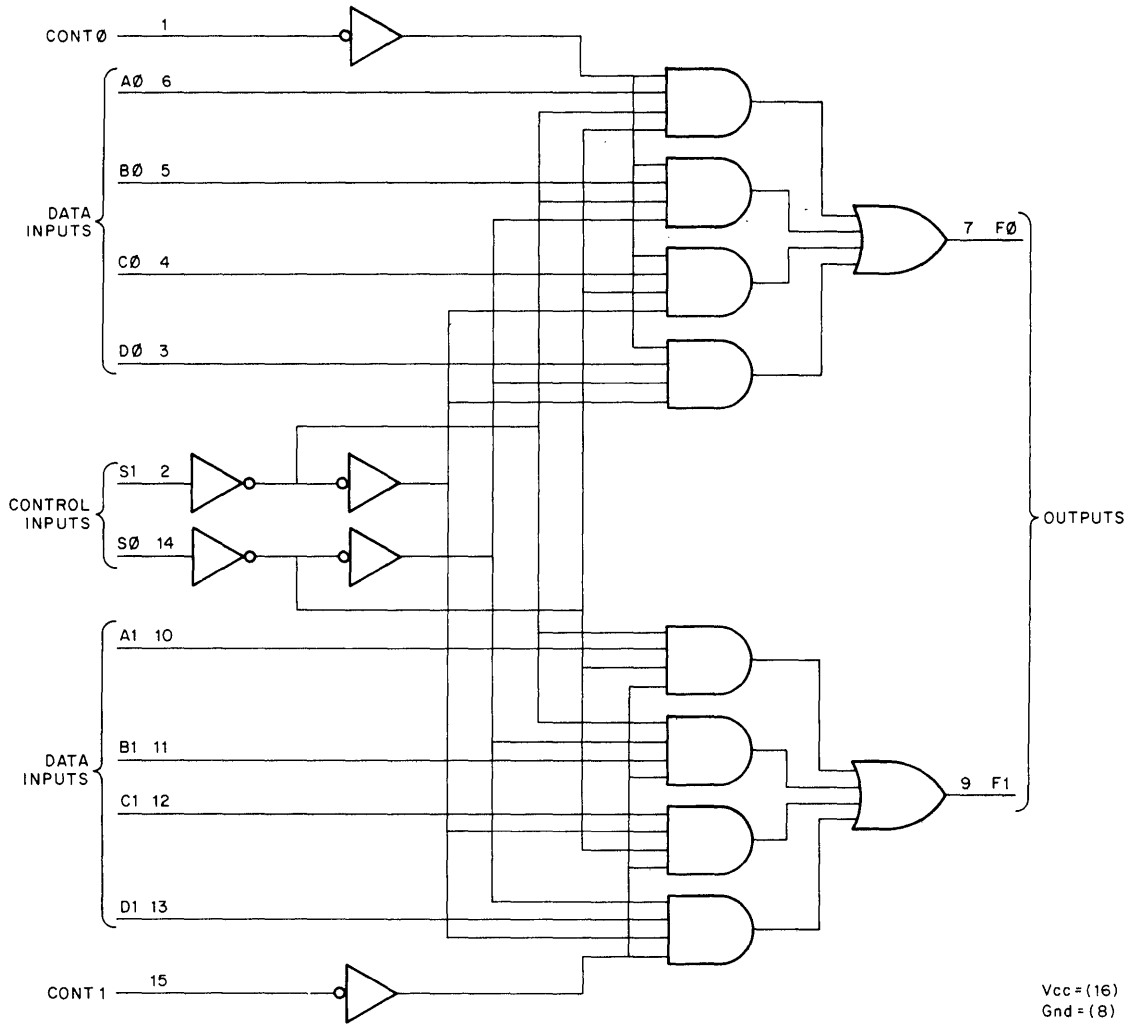




Note: 74175 is shown. LS only signifies low power Schottky.

74LS253 4:1 MULTIPLEXER

The 74LS253 is a dual, 4-line to 1-line data selector/multiplexer.



LOGIC DIAGRAM

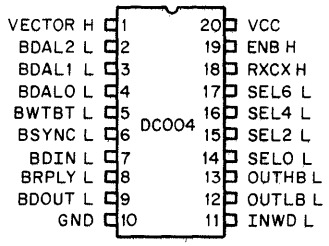
S1	S0	An	Bn	Cn	Dn	CONTn	Fn
X	X	X	X	X	X	HI	Z
LO	LO	LO	X	X	X	LO	LO
LO	LO	HI	X	X	X	LO	HI
LO	HI	X	LO	X	X	LO	LO
LO	HI	X	HI	X	X	LO	HI
HI	LO	X	X	LO	X	LO	LO
HI	LO	X	X	HI	X	LO	HI
HI	HI	X	X	X	LO	LO	LO
HI	HI	X	X	X	HI	LO	HI

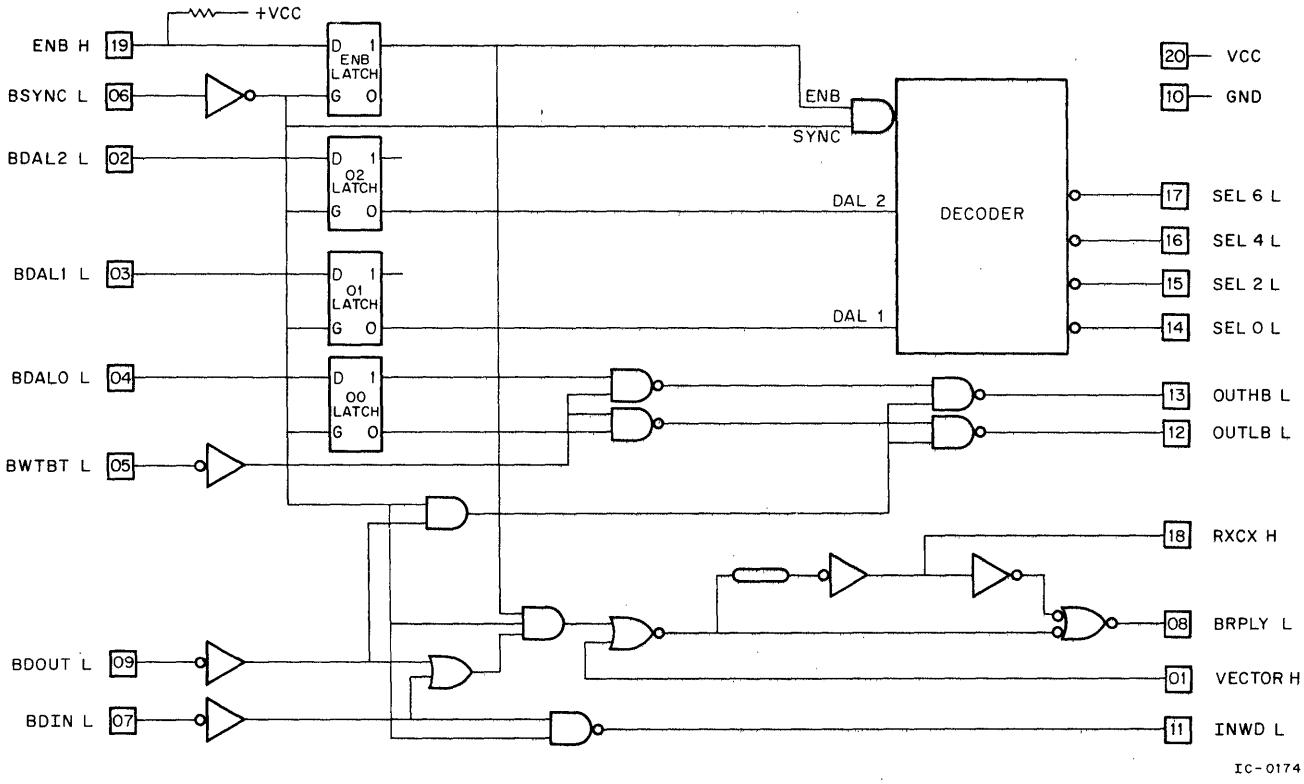
X = DON'T CARE
Z = HI IMPEDANCE

TRUTH TABLE

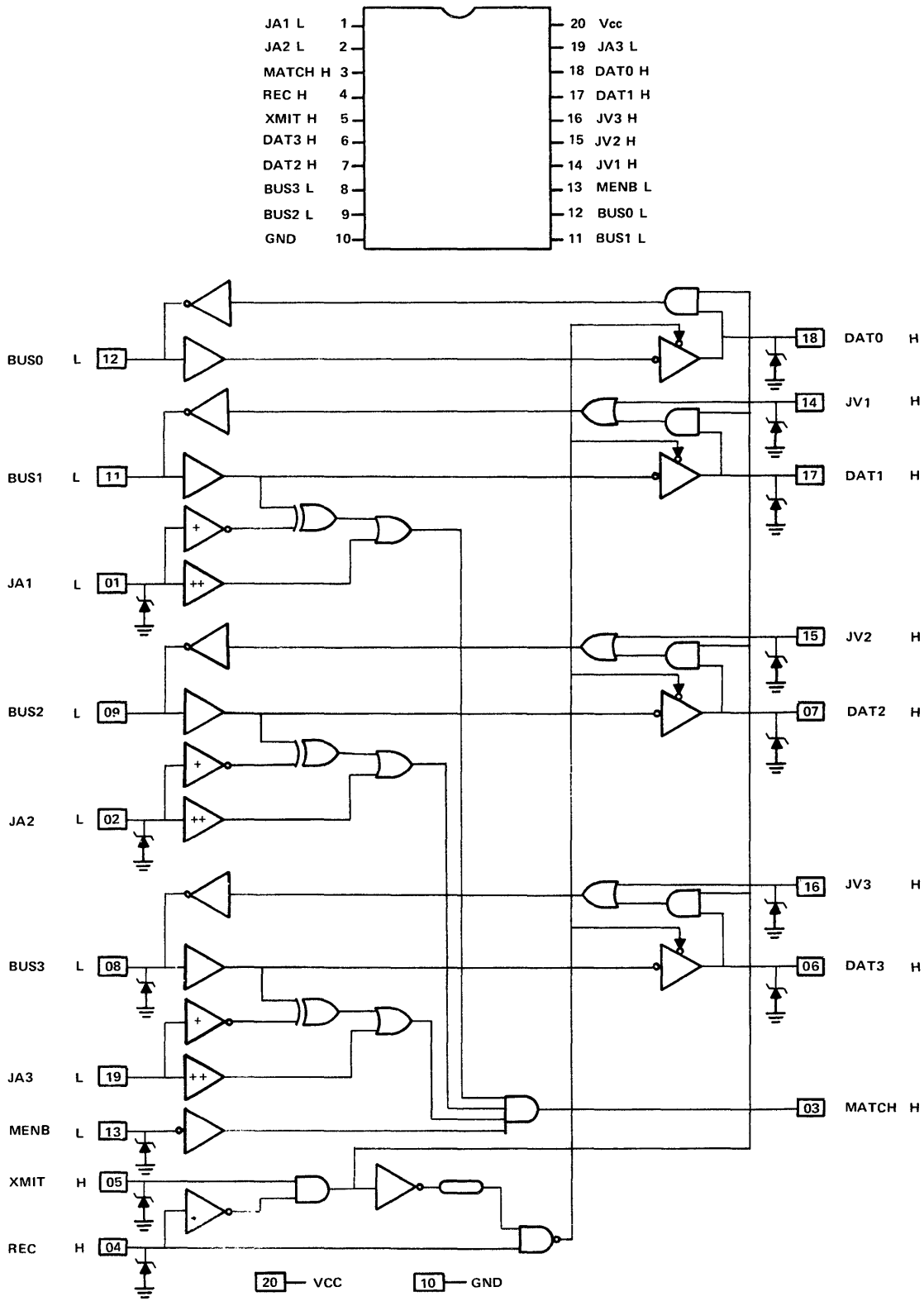
IC-74LS253

DC004 PROTOCOL CHIP





DC005 BUS TRANSCEIVER



IC-DC005

Reader's Comments

DUV11 LINE INTERFACE
TECHNICAL MANUAL
EK-DUV11-TM-001

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults do you find with the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

Would you please indicate any factual errors you have found. _____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

— — — — — — — — — — — Fold Here — — — — — — — — — —

— — — — — — — — — — Do Not Tear - Fold Here and Staple — — — — — — — —

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

Digital Equipment Corporation
Technical Documentation Department
Digital Park, PK3-2
Maynard, Massachusetts 01754

digital

digital equipment corporation

Printed in U.S.A.