DEC-8L-D4BA-D

MC8/L
MEMORY EXTENSION CONTROL OPTION FUNCTIONAL DESCRIPTION

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INTRODUCTION

An additional 4096 (4K) core memory can be added to the standard PDP-8/L 4K core memory to yield the maximum storage capacity of 8192 words. Figure 1 shows the MC8/L modules and their locations in the BA08 Peripheral Expander and Figure 2 illustrates the Memory Extension Control organization, and it's relationship to the standard memory. The Memory Extension Control is placed in the BA08 Peripheral Expander Cabinet as shown in Figure 2. Transfer of MC8/L control and data signals occurs mainly through the special signal cables and connectors. The PDP-8/L I/O BUS is connected to the BA08. Some of the I/O BUS signals are used by the MC8/L option; however, other options make use of this bus so it must be supplied.

The following paragraphs describe the use of the MC8/L control logic, and the Memory Extension Control instruction set. It is assumed that the reader understands the memory timing, read, write, inhibit and sense elements of the basic memory system described in Volume I, Chapter 4, of the PDP-8/L Maintenance Manual. The memory system elements described above are identical to those in the expanded 4K core memory; therefore, maintenance and operation are the same.

LOGIC DESCRIPTION

Instruction Field Register (IF)

This 1-bit register determines the memory field to be used for storage and retrieval of program instructions. The IF register can be loaded directly by pressing LOAD ADDR with the INST FIELD key raised, or by the program through the Instruction Buffer (IB) register. All program executed transfers of the IF come from the IB. The content of the INST FIELD key is loaded directly into the IF and the IB by manual operation of the LOAD ADDR key. When a JMP or JMS instruction is executed, the content of the IB is transferred into the IF.

When an interrupt occurs, the content of the IF is transferred to the Save Field (SF) register. At the end of the interrupt subroutine the IF status is restored through the IB from the SF by execution of the RMF instruction.

When the CIF instruction is executed (refer to Memory Extension Control Instruction Descriptions in this section) the content of MB08 is transferred to the IB; the content of the IB is transferred to the IF at the execution of a JMP or JMS instruction. During the time between the CIF instruction and the JMP or JMS, program interrupts are inhibited.

Data Field Register (DF)

This 1-bit register determines the field used for data storage and retrieval. The DF can be loaded from three discrete sources: MB08, the Save Field (SF1), and the DATA FIELD key.

Initially, the DF is loaded from the DATA FIELD key by manual operation of the LOAD ADDR key. While the program is running, a CDF (change data field) instruction can be used to alter the content of the DF to permit selection of the other memory field. Bit 08 of the CDF instruction contains the desired field address (either 0 or 1). Once loaded, the content of the DF remains unchanged until altered; either manually by LOAD ADDR and the asserted DATA FIELD key, or under program control by a CDF instruction.

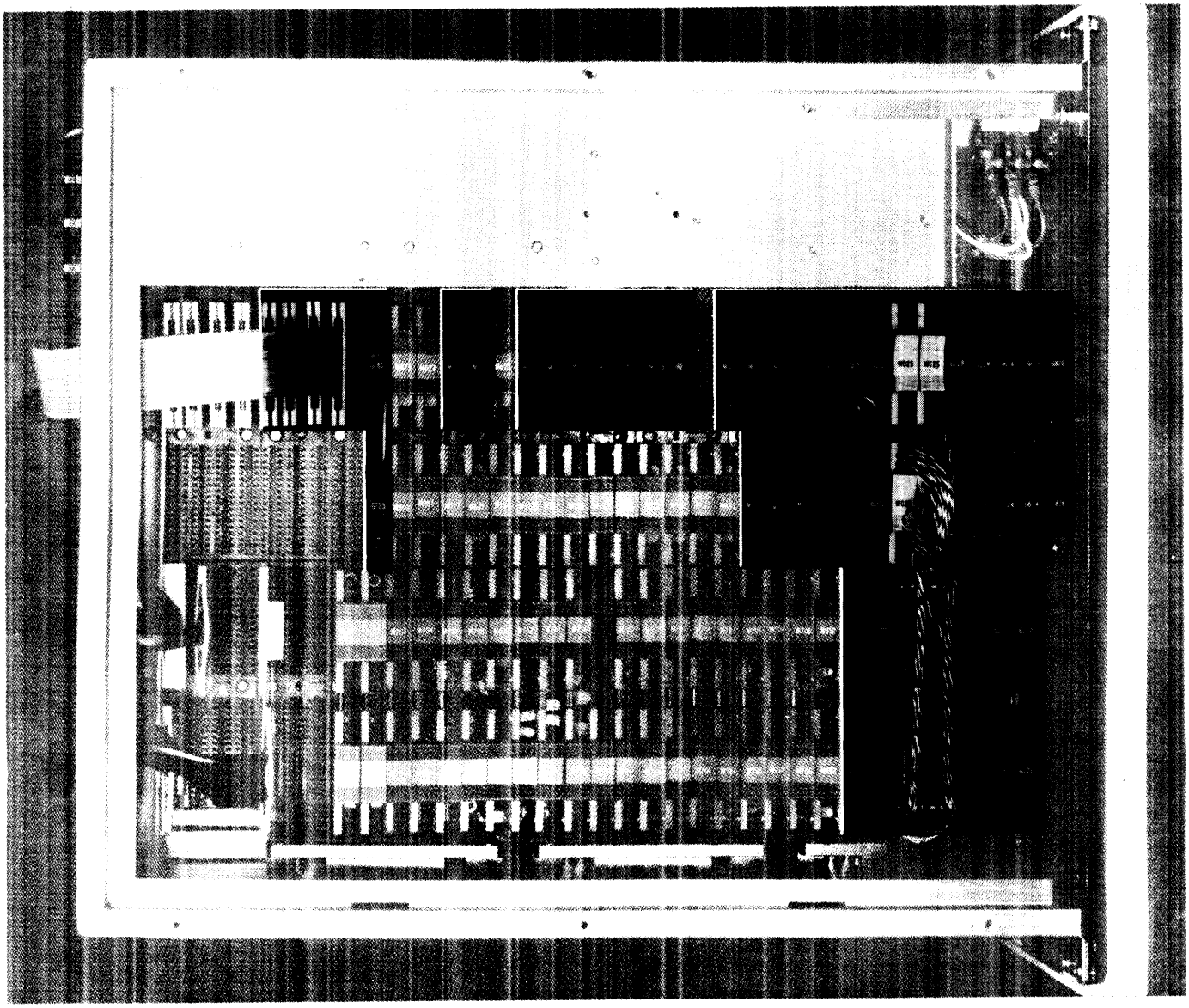


Figure 1 Memory Extension Control in the BA08 Peripheral Expander

During a program-interrupt operation, the content of the DF is automatically stored in the Save Field register (SF1) and is restored to the DF upon completion of the interrupt subroutine by the RMF instruction.

Instruction Buffer Register (IB)

This 1-bit register provides input buffering for data transfers made into IF under program control. Manual transfers are made directly into IF and, simultaneously, into IB. This transfer of data into both registers is necessary to prevent inadvertent changing of the content of IF. The output of IB is loaded into IF at the execution time of every JMP or JMS instruction strobes the output of IB into IF.

Save Field Register (SF)

This 2-bit register provides temporary storage for the content of both IF and DF during a program interrupt. This is necessary to permit IF and DF to be cleared so the program interrupt subroutine can start in field 0. At the conclusion of the interrupt subroutine, an RMF instruction loads the content of SF0 into IB for subsequent transfer into IF, and the content of SF1 into DF. The last instruction in the subroutine (JMP10) completes the transfer from IB, to IF.

Break Field Register (BF)

This 1-bit register determines the field to be used for storage and retrieval of data transfers from I/O devices using the data break facility. The BF is loaded from the EXT DATA ADD line by BTP2 of the cycle before a data break is initiated.

Extended Address (EA) Field Selection

The EA flip-flop (drawing D-BS-MC8-L-2) allows access to either memory field. The flip-flop outputs, $\overline{EA}$ (for field 0, the standard core memory) and EA (for the extended memory) enable each memory timing generator when at a high logic level.

The EA extended address field enable flip-flop can be activated from one of three sources: the the IF register, the DF register, or the BF register. The IF register is gated to the EA flip-flop except during a break cycle or an indirectly referenced data handling instruction (AND, TAD, ISZ and DCA). In addition, when the LOAD ADDR and the INST FIELD keys are operated, the IF is gated to EA to generate the memory field enable level. The DF register is gated to EA when any indirectly-addressed memory reference instruction other than JMP or JMS is executed (AND, TAD, ISZ or DCA). The BF decoder allows the BF to generate the memory field select code during a break cycle.

Interrupt Inhibit

The interrupt inhibit (drawing D-BS-MC8L-2) logic disables the INT OK (drawing D-BS-PDP-8-L-7) level in the processor from the time a CIF instruction is decoded until a JMP or JMS command finishes the CIF instruction. This prevents operation of an interrupt before the field is changed. Interrupt synchronization is restored after the IF is loaded from the IB, allowing further program interrupt to occur.

MEMORY EXTENSION CONTROL INSTRUCTION DESCRIPTIONS

The following paragraphs describe the basic microinstruction set necessary to control program execution with the Memory Extension Control option. See Table 1 Basic IOT Microinstruction Set for the MC8/L.

Table 1
Basic IOT Microinstruction Set for the MC8/L

Mnemonic Program Interrupt	Octal	Operation
CDF	62N1	Change to Data Field N. The data field register is loaded with the selected field number (0 or 1). All subsequent memory requests for operands are automatically switched to that data field until the data field number is changed by a new CDF command, or during a program interrupt. MB8 = > DF
CIF	62N2	Change Instruction Field. The instruction buffer register is loaded with the selected field number (0 or 1). The next JMP or JMS instruction causes the new field to be entered. MB8 => IB.
RDF	6214	Read Data Field. The content of the data field register is transferred into bit 8 of the AC. Bits 6 and 7 are cleared, all other bits of the AC are not affected. DF = > AC8
RIF	6224	Same as RDF, except reads the instruction field. IF = > AC8
RIB	6234	Read Interrupt Buffer. The instruction field and data field, stored in the same field during an interrupt, are read into AC 8 and 11 respectively. SF0 = > AC8 SF1 = > AC11
RMF	6244	Restore Memory Field, Used to exit from a program interrupt.

Change Data Field (CDF)

This instruction (octal code 62N1, where N is the octal number of the field to which control is changing, N is 0_8 for field 0, and 1_8 for field 1) is used prior to storing or retrieving data with any indirectly-addressed memory-reference instruction other than JMP or JMS. This instruction is generated by combining BIOP1 and MB03 through MB07 levels (drawing D-BS-MC8-L-2).

Change Instruction Field (CIF)

This instruction (octal code 62N2, where N is the octal number of the field to which the program is changing) is executed prior to JMP or JMS instruction. The 62N2 instruction allows MB08 (N = MB06 a 0, MB07 a 0 and MB08 either a 0 for field 0 or 1 for field 1) to be loaded into the IB by combining it with BMB09 (0) to enable the IB flip-flop data input and clocking the clock input with LOAD IB. The

content of IB is then transferred to the IF when the next JMP or JMS command is executed (LOAD IF active).

Restore Memory Field (RMF)

This instruction (octal code 6244) restores the contents of the SF to the DF and IB registers. The conclusion of an interrupt subroutine (JMP I 0) loads the IF from the IB. $\overline{\text{RMF}}$ (drawing D-BS-MC8-L-2) allows bit SF1 to be loaded into the DF. The content of the IB is transferred to the IF by executing a JMP or JMS instruction.

Read Interrupt Buffer (RIB)

This instruction (octal code 6234) allows storing that same field in memory if the power failure option is installed. This instruction reads the contents of the 2-bit SF register into the AC on the $\overline{\text{ACI08}}$ and $\overline{\text{ACI11}}$ lines (drawing D-BS-MC8-L-2). These lines activate the INPUT BUS 08 and 11 lines in the processor.

Execution of the RIB instruction generates AC LOAD and AC ENABLE in the processor which allows transfer of the data on INPUT BUS 08 and 11 to the accumulator. AC LOAD (drawing D-BS-PDP8-L-6) is generated by I/O ENABLE and I/O STROBE as a result of performing this IOT (6234) command. I/O ENABLE also produces AC ENABLE (drawing D-BS-PDP8-L-4).

Read Data Field (RDF)

This instruction (octal code 6214) reads the contents of the DF flip-flop onto the $\overline{\text{ACI08}}$ line. The data is transferred to accumulator bit AC08 in the same manner as with the RIB instruction.

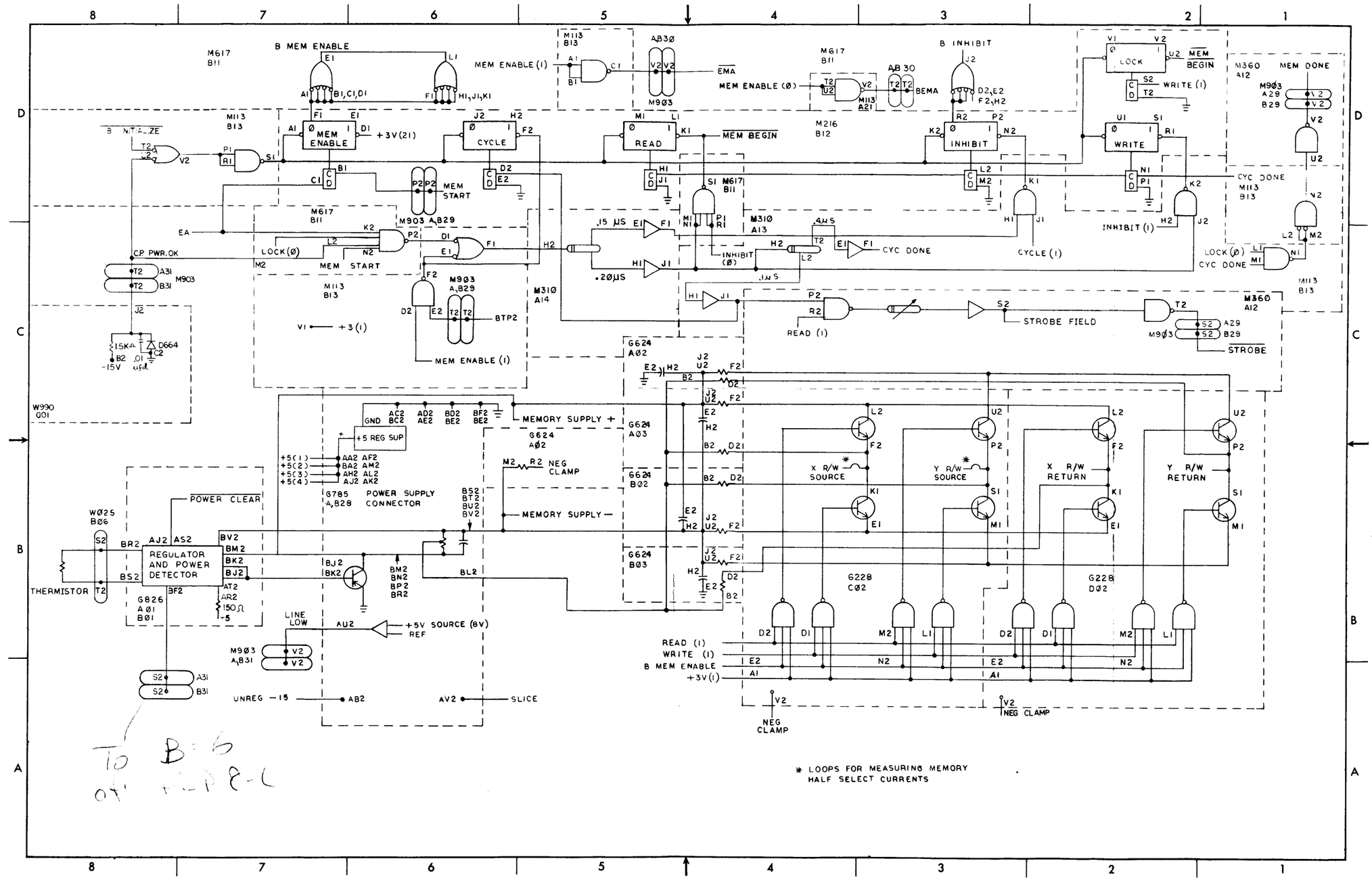
Read Instruction Field (RIF)

This instruction (octal code 6224) reads the contents of the IF flip-flop onto the ACI08 line. The data is transferred through the INPUT BUS 08 line to bit AC08 in the same manner as the RDF.

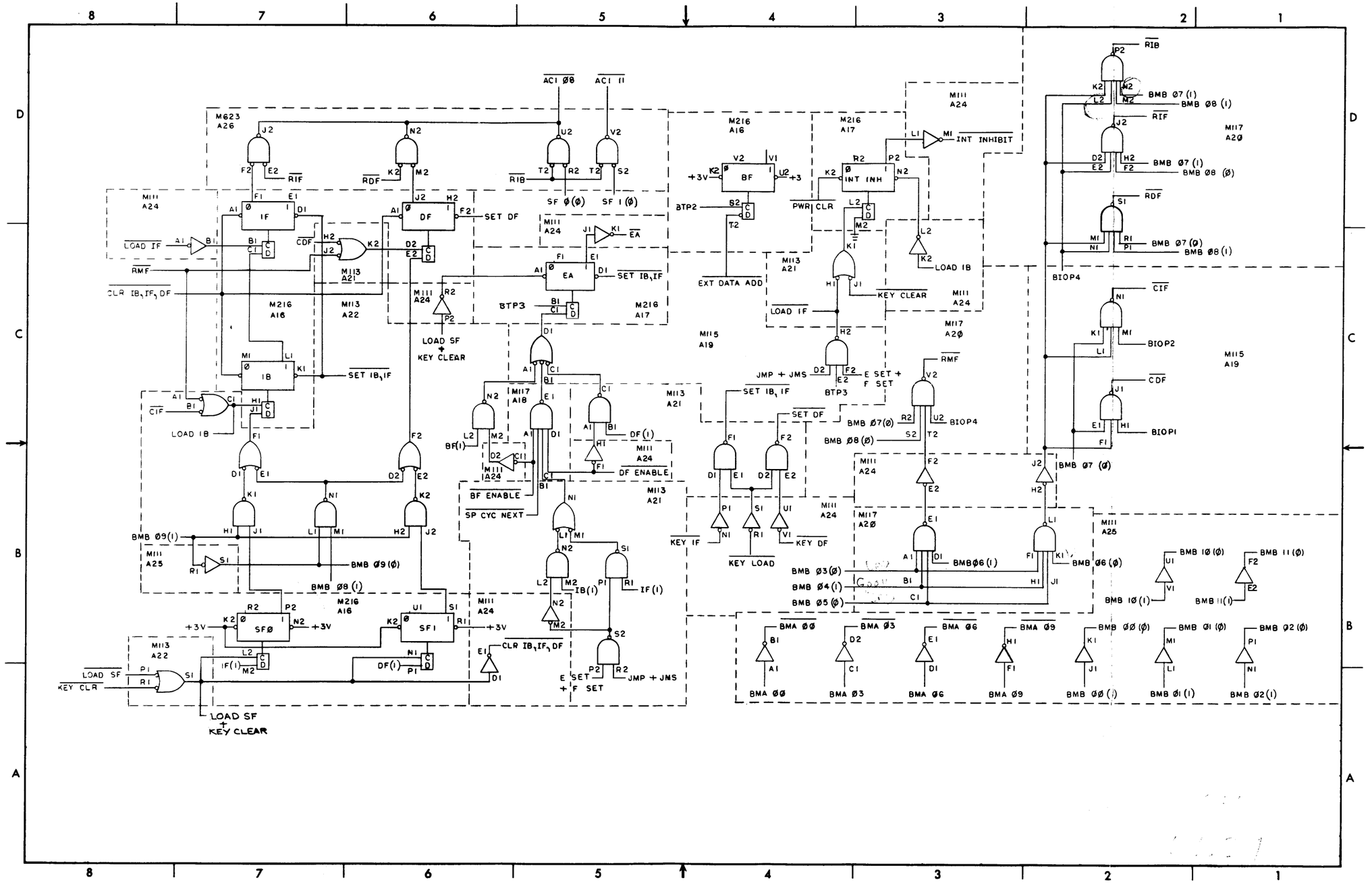
ENGINEERING DRAWINGS

The following drawings pertaining to the MC8/L option are contained in this section.

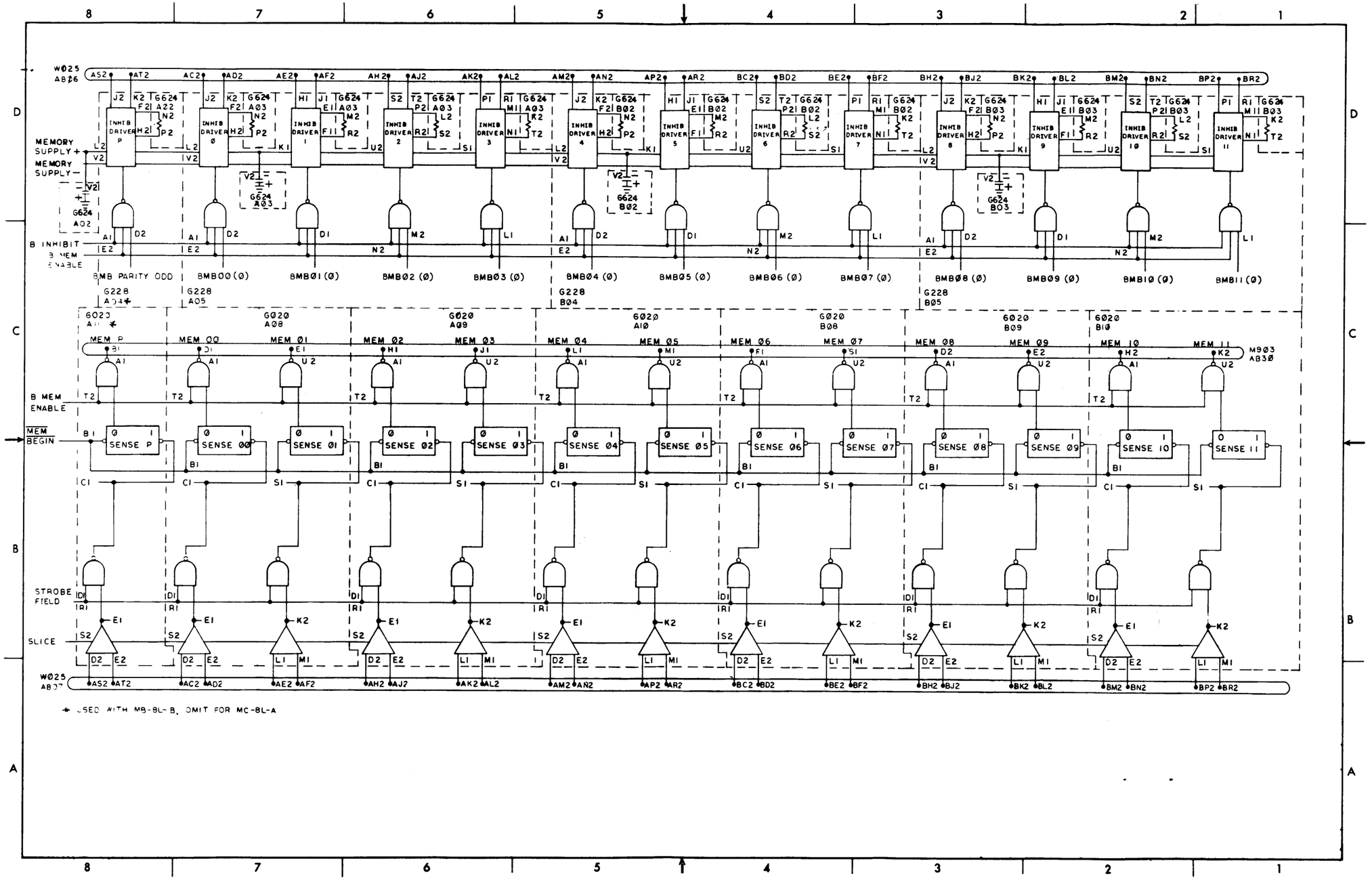
Drawing Number	Title
D-BS-MC8-L-1	Memory Control
D-BS-MC8-L-2	Memory Extension Control
D-BS-MC8-L-3	Sense Amp and Inhibit Drivers
D-CS-MC8-L-4	X-Axis Selection
D-CS-MC8-L-5	Y-Axis Selection
D-IC-MC8-L-6	Special Signal Connectors
D-UA-BC08A-0-0	BC08A Cable



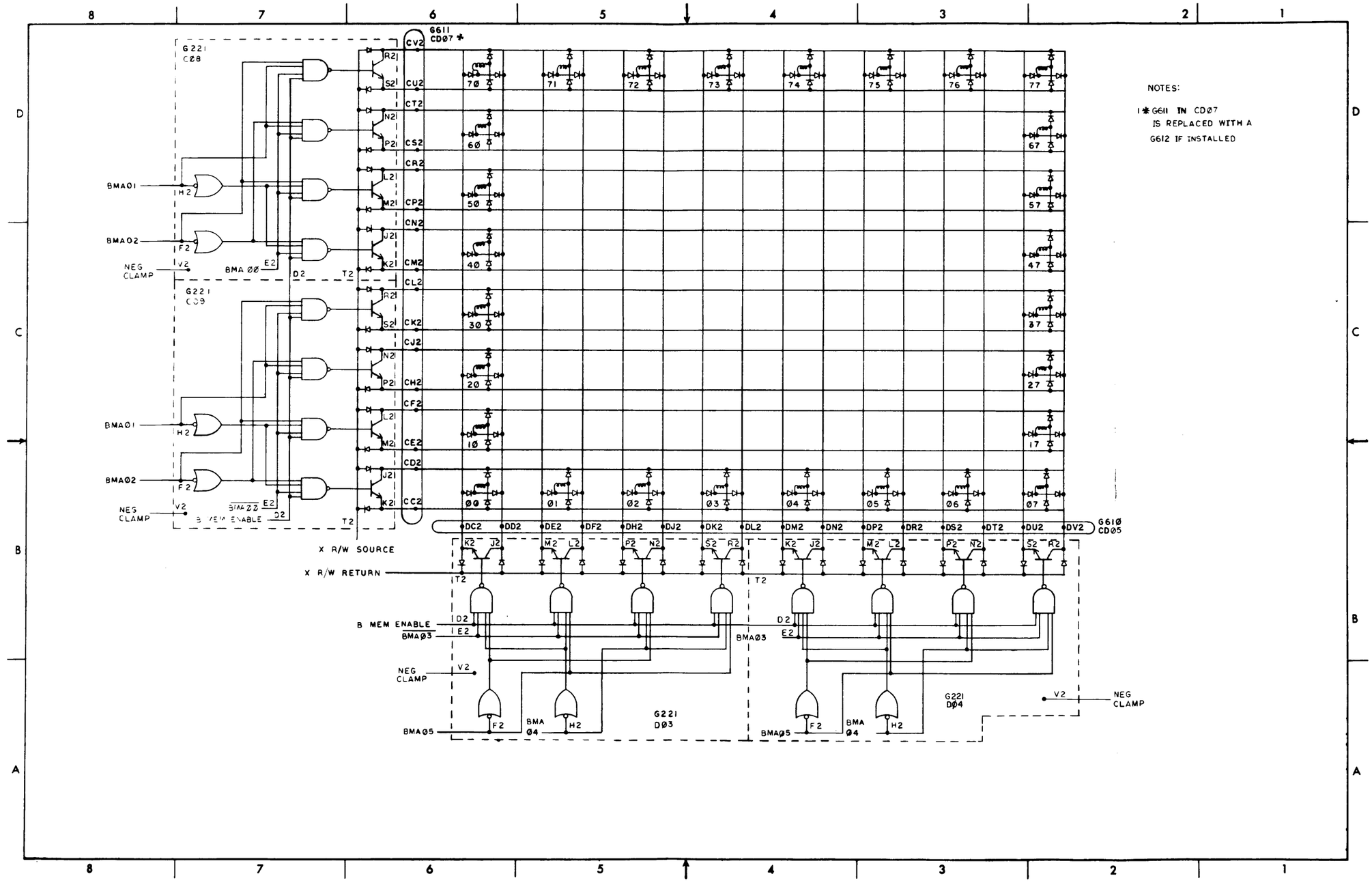
D-BS-MC8-L-1 Memory Control



D-BS-MC8-L-2 Memory Extension Control



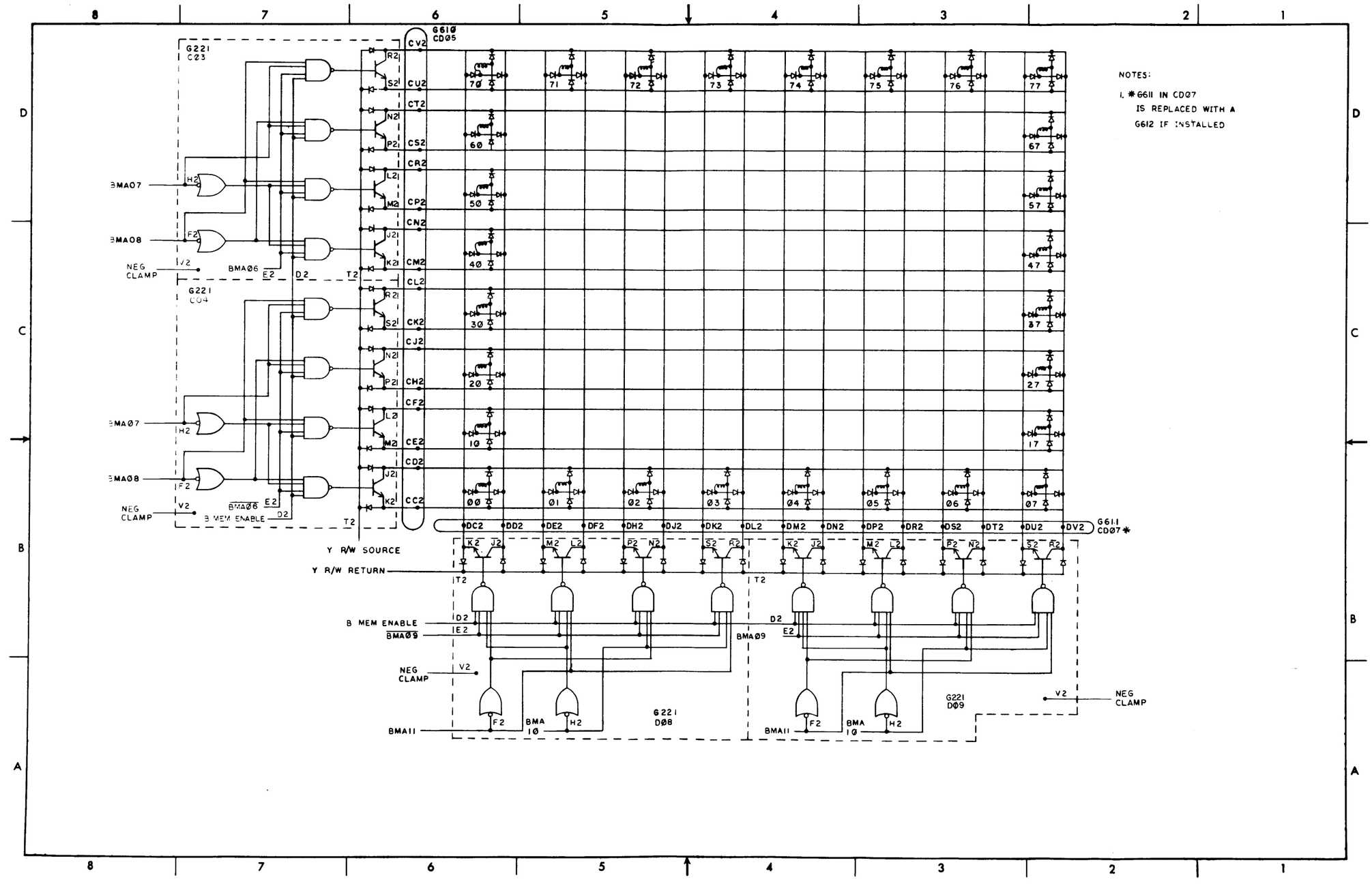
D-BS-MC8-L-3 Sense Amp and Inhibit Drivers



NOTES:

1 * G611 IN CDØ7 IS REPLACED WITH A G612 IF INSTALLED

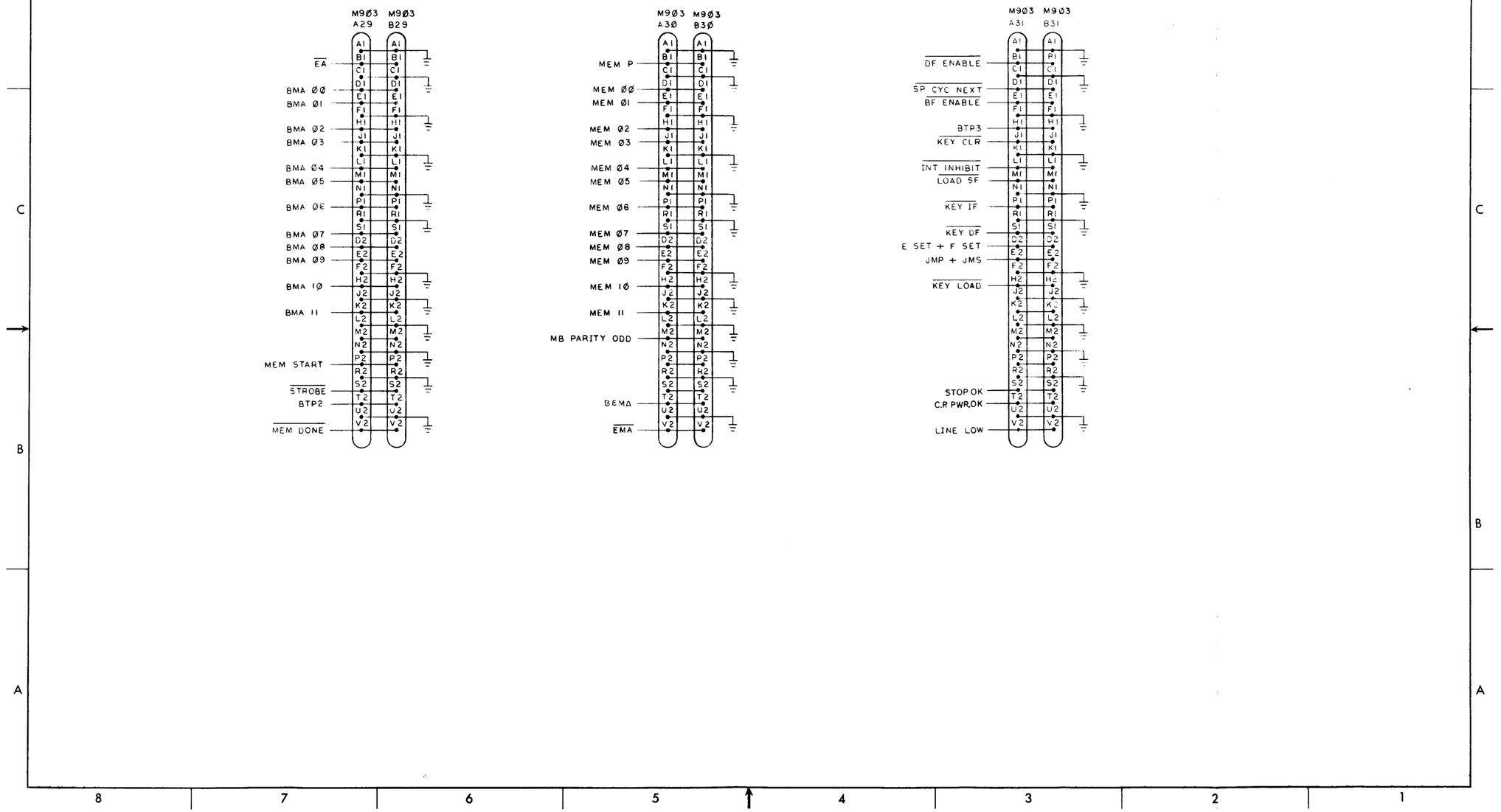
D-CD-MC8-L-4 X-Axis Selection



NOTES:

1. *G611 IN CD07 IS REPLACED WITH A G612 IF INSTALLED

D-CS-MC8-L-5 Y-Axis Selection



D-IC-MC8-L-6 Special Signal Connectors

PART NO.	DIM "A"
BCØ8A-1	1 FT
BCØ8A-2	2 FT
BCØ8A-3	3 FT
BCØ8A-4	4 FT
BCØ8A-5	5 FT
BCØ8A-6	6 FT
BCØ8A-7	7 FT
BCØ8A-8	8 FT
BCØ8A-9	9 FT
BCØ8A-10	10 FT
BCØ8A-11	3 /2 FT

SEE NOTE #2

NOTES:

1. ATTACH ITEM #5 (TAPE) TO ITEM #3 (FLEX PRINT CLAMP) THEN ASSEMBLE ITEM #3 TO ITEM #1 (FLIP CHIP) WITH ITEM #2 OR #6 (EYELETS).
2. FLEXPRINT IS TO BE CUT TO THE FOLLOWING LENGTHS, PRIOR TO FABRICATION:
   FLEXPRINT "A" – DIM "A" PLUS 1¾ INCHES
   FLEXPRINT "B" – DIM "A" PLUS [illegible]
   FLEXPRINT "C" – DIM A PLUS [illegible]
3. P1 IS WIRED TO P2 ON THE SAME PINS, EXAMPLE: P1-A1 IS WIRED TO P2-A1 AND P1-B2 IS WIRED TO P2-B2 AND SO ON.
4. TOLERANCES: (STD. CABLE)

0 TO 2½ FT	± ½ INCH
2'7" TO 5 FT	± 1 INCH
5'1" TO 10 FT	± 2 INCHES

5 FLEXPRINT "C" (TEST) IS NOT ELECTRICALLY CONNECTED