138-139

ANALOG-TO-DIGITAL CONVERTER MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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CONTENTS

ILLUSTRATIONS

INTRODUCTION

The purpose of this instruction manual is to aid personnel in the operation of the Type 138-139 Multiplexed Analog-to-Digital Converter. This manual includes a complete description of system logic and general procedures for operating and calibrating the system.

A brief summary of system application is presented in Section 1, General Description. This section also lists system specifications and physical characteristics.

Section 2, System Operation, describes in general terms the logical organization of the system at block diagram level, explaining how the system is used, both as an adjunct to a computer and as a separate device. This section also explains data format, timing, and use of system controls and indicators.

Section 3, System Logic, describes the conversion process and gives a complete logical description of system hardware.

Section 4, Circuit Description, describes the function, specifications and circuit theory of all DEC system modules used in the 138-139 system.

Section 5, Adjustment and Calibration, includes the procedures necessary for periodic checks and adjustments of certain Digital modules.

Section 6, Pertinent Documents, lists supporting Digital literature and includes the engineering drawings for the 138-139 system. The logic diagrams and replacement schematics included at the end of this section are explained in Sections 3 and 4, respectively.

SECTION 1

GENERAL DESCRIPTION

The Type 138-139 system is a general purpose analog-to-digital converter capable of transforming up to 64 time-shared analog voltages to binary numbers. The design of the system permits unusual flexibility of operation. The unit is equipped to function either as an adjunct to a Digital computer or as a separate, self-contained device. The length of the converted data word, conversion time and accuracy, and multiplexer capacity can be varied by the operator to allow optimum use of the system consistent with his requirements; channel selection is under program control.

The program selects a channel by providing a channel address to the multiplexer control. Two methods of selection are available: one uses an instruction to select a specific channel; the other uses an instruction to index the address already contained in the multiplexer address register. In the latter case, the multiplexer returns to zero upon command to advance from the final channel. Sequenced operation may be short cycled when the number of channels used is less than the maximum.

After selecting a channel, the program must initiate the conversion (however, an option is available which causes a single conversion to follow automatically after each channel selection). If the system is used as a separate device, the instructions must be replaced by equivalent pulses. When a conversion is initiated, the Type 138 converts the input from the selected channel to a binary number of 6 to 11 bits. The selected input may be sampled as many times as desired between address changes. A status level indicates the end of each conversion.

SYSTEM OPERATING SPECIFICATIONS

Resolution	6 to 11 bits, with monotonicity
Increment per bit	156 mv (6-bit word) to 4.8 mv (11-bit word)
Analog input range	0 to -10 v
Digital output range	-2^{n-1} to $+2^{n-1}-1$ (n = selected word length)

SYSTEM OPERATING SPECIFICATIONS (continued)

Output notation	2's complement 1 = -3 v, 0 = 0 v 0 v in = greatest negative digital output -10 v in = greatest positive digital output
Temperature range	±5°C around room temperature
Maximum conversion rate	111 kc (6 bits) to 11.3 kc (11 bits)
Conversion time in microseconds	

Max. Switching Point Error	Number of Bits 6	7	8	9	10	11
±.05%	48	56	64	72	80	88
±.1%	30	35	40	45	50	55
±.2%	18	21	24	27	30	33
±.4%	15	17 1/2	20	22 1/2	25	27 1/2
±.8%	12	14	16	18	20	22
±1.6%	9	10 1/2	12	13 1/2	15	16 1/2

NOTE: Conversion error = maximum switching point error ±1/2 LSB

Control Inputs

Clear	Amplitude.....-2.5 v to -4 v
Index	Pulse width.....>60 nsec
Convert	Fall time.....<0.5 μsec

NOTE: Clear must precede readin by at least 1 μsec.

Readin	Amplitude.....-2.5 v to -4 v
	Pulse width .....>60 nsec
	Fall time.....<0.5 μsec
	Pulse load.....1 unit

Multiplexer address inputs	6 standard Digital logic levels 0 and -3 v with 0 v assertion (optional: -3 v assertion)

PHYSICAL CHARACTERISTICS

Construction	Two standard Digital 25-position mounting panels (aluminum). Indicator and connector panels are aluminum.
Modules	Standard Digital system plug-in modules; series 1000, 4000, and 6000.
Power equipment	Power Supply 728 or 722
Logic	Solid state. Transistors and diodes operating with static logic levels (0 and -3 vdc).
Dimensions	All panels and power supply 722 are standard rack-mounting size: 5 1/4" high, 19" wide
Weight	60 lbs

Power Requirements

Line voltage input	105 to 125 volts, 60 cycle ±0.5 cycles, single phase

EQUIPMENT LIST

The multiplexed analog-to-digital converter is housed in two standard Digital mounting panels. Each panel can hold 25 standard Digital plug-in logic modules. If the system is mounted for use with a Digital computer, a 728 Power Supply is mounted on the plenum door at the rear of the containing bay. For use as a separate device, the system is provided with a 722 Power Supply for rack-mounting.

The following list includes all plug-in modules required by the multiplexed analog-to-digital converter. Numbers in parentheses indicate optional modules. All circuits listed are described in Section 4.

Type	Quantity
Delay 1304	1
Delay Line 1310	1
Difference Amplifier 1572	1

	Quantity
12-bit DAC 1574	1
Multiplexer 1578 (four switches per module)	1-16
Reference Supply 1704	1
Binary-Octal Decoder 4150	2
7-Bit Counter 4222	1
Serial-to-Parallel Assembler 4226	3
Delay 4301	1 (1)
Pulse Amplifier 4604	1
Pulse Amplifier 4606	1 (1)
Level Amplifier 4679	3
Inverter 6102	3 (1)
Inverter 6106	1
Flip-Flop 6202	1
Crystal Clock 6403	1

SIGNAL CONNECTIONS

The connector panel contains two 50-pin receptacles for the analog inputs. The 64 channels are connected to pins 1-32 of each connector. At the left side of each logic panel is a 22-pin Amphenol connector. Pin designations are as follows:

Type 138 (upper panel)				Type 139 (lower panel)			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A	GND	N	ADB_8'	A	MAI_5'	N	MAR_0'
B	Power Clr	P	ADB_9'	B	MAI_4'	P	N.C.
C	ADB_0'	R	ADB_{10}'	C	MAI_3'	R	IMC 7
D	ADB_1'	S	ADB_{11}'	D	MAI_2'	S	GND

Type 138 (upper panel)

Pin	Signal	Pin	Signal
E	ADB_2'	T	FLAG
F	ADB_3'	U	GND
H	ADB_4'	V	Start Conv.
J	ADB_5'	W	Conv. Done
K	ADB_6'	X	GND
L	N.C.	Y	RCB
M	ADB_7'	Z	GND

Type 139 (lower panel)

Pin	Signal	Pin	Signal
E	MAI_1'	T	SMC 10
F	MAI_0'	U	GND
H	MAR_5'	V	SMC 7
J	MAR_4'	W	GND
K	MAR_3'	X	N.C.
L	MAR_2'	Y	N.C.
M	MAR_1'	Z	N.C.

SECTION 2

SYSTEM OPERATION

Figure 2-1 is a block diagram of the Type 138-139 Multiplexed Analog-to-Digital Converter. The figure shows the 139 Multiplexer Control (including an array of multiplexer switches) at the left; the 138 Analog-to-Digital Converter at the right. Control inputs to the system are the four pulses shown at the lower left. These pulses govern both multiplexer channel selection and initiation of analog-to-digital conversion. If the system is used with a DEC computer, these pulses are provided by instructions in the program. Otherwise, the user must provide a program of pulses with the required specifications.

To select a specific channel, the program must first clear the address register and then transfer a 6-bit address into it(with a computer both clear and readin are included in a single instruction). The program may, however, select only an initial channel and then sequence through following channels by indexing MAR (the multiplexer address register). In either case, the address is decoded to select a single analog input channel out of a possible 64 in an 8 x 8 array of multiplexer switches. The analog signal on the selected input channel is then applied to the converter.

After selecting a channel, the program initiates each conversion by pulsing the convert input. As many conversions as are desired may be performed on a single channel between address changes.

The analog-to-digital converter uses the successive approximation method to produce a binary number representative of an analog signal at its input terminal. Converter components include a precision reference source which supplies a voltage equal to the full-scale analog input, an internal digital-to-analog converter (ladder network), a serial-to-parallel assembler, a comparator, and a timing unit. The successive approximation method is initiated as the assembler instructs the digital-to-analog converter to generate a voltage equal to one-half the maximum value. This voltage, together with the analog input, is applied to a comparator whose output indicates whether the analog signal is in the upper or the lower half of the range. At the next timing pulse, the assembler causes the digital-to-analog converter to generage a voltage equal

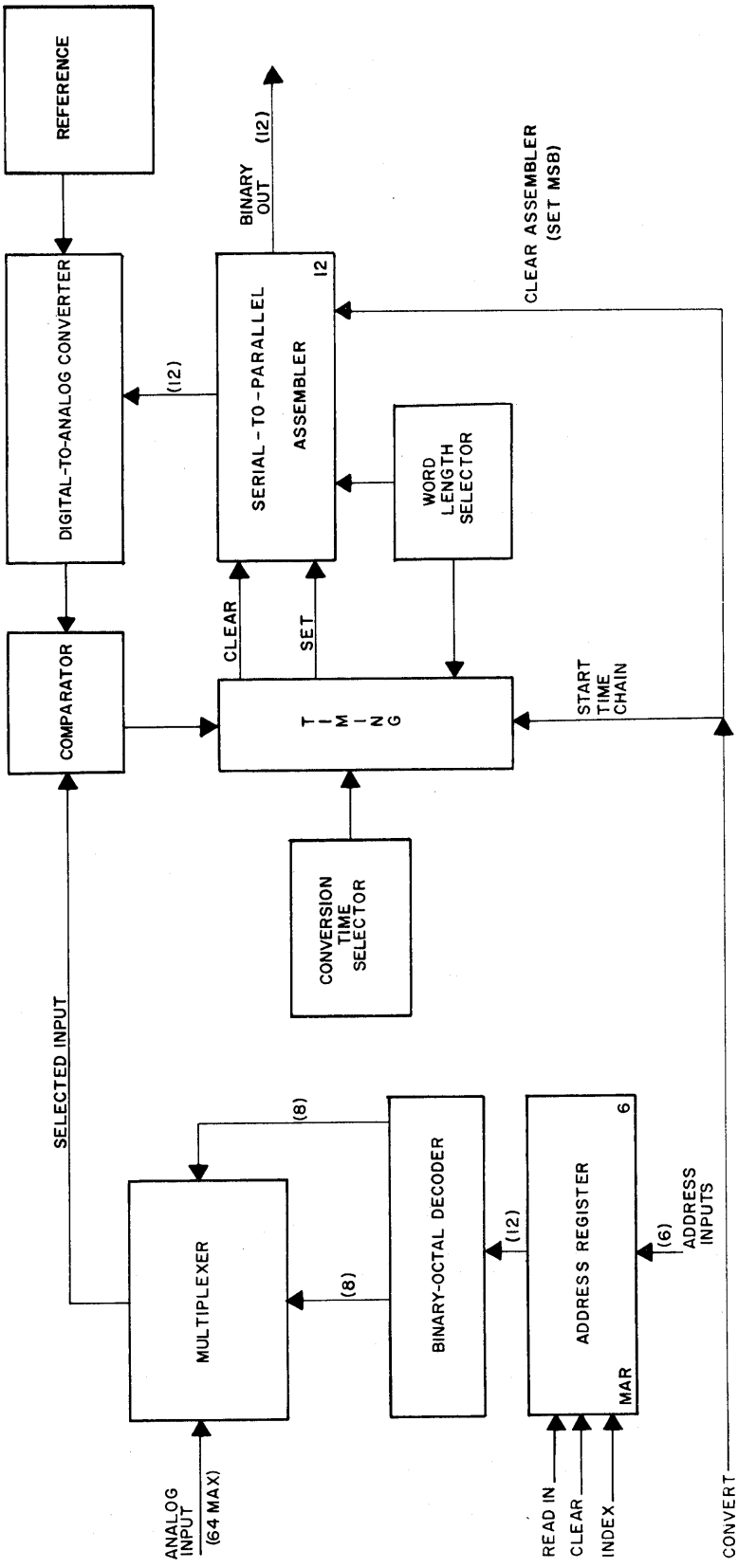


Figure 2-1 Analog-to-Digital Converter

either to one-fourth full scale or three-fourths full scale, depending upon the result of the first comparison. The comparator then indicates which quarter of the range contains the analog voltage.

In each following step, the possible range is divided in half. An N-bit conversion, therefore, requires N steps. The length of the binary output word, as well as the time per comparison may be varied by the operator with two panel switches (Figure 2-2). The switch at the left selects the number of bits (6 to 11); the SPEED/ACCURACY switch selects the maximum allowable switching point error (± .05% to ± 1.6%). Total conversion time depends upon the setting of both switches as listed in System Operating Specifications (Section 1).

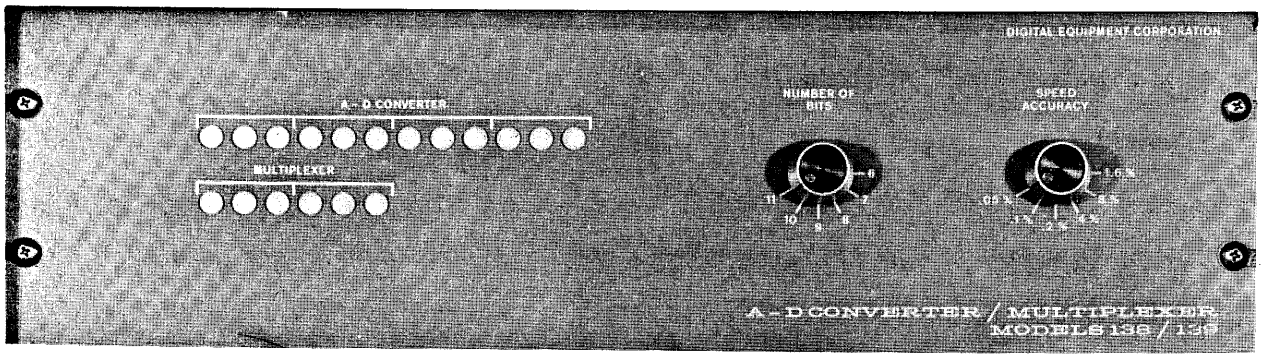


Figure 2-2 Control Panel

The panel also includes two sets of neon indicator registers. The top line of 12 indicators displays the converter output in 2's complement binary; the lower 6 indicators display the address of the selected analog channel.

NUMBER SYSTEM

The output of the analog-to-digital converter is a signed binary number with 2's complement representation for negative numbers. Maximum system resolution is one part in 2048. A - 10 volt input corresponds to the largest positive digital output; a 0 volt input results in the largest negative output. To generate the correct signed output from the unsigned assembler magnitude, the most significant bit of the output data word is complemented, as follows:

Analog Input	Assembler	Binary Output
0 v	111111...	100000...
-5 v	011111...	000000...
-10 v (less one LSB)	000000...	011111

The converter output is a binary number of 6 to 11 bits with ones represented by standard Digital negative logic levels.

PROGRAMMING WITH PDP-1, PDP-4, OR PDP-5

With the addition of the multiplexed analog-to-digital converter, four in-out transfer instructions are added to the PDP-1 computer repertoire, five to the PDP-4 and six to the PDP-5. These instructions are executed in 5 microseconds for PDP-1, 8 microseconds for PDP-4, 12 microseconds for PDP-5). The instructions control channel selection (either by providing a complete address of by indexing the previous address), initiate the conversion, and sample the digital output.

All conversions must be initiated by the program separately from channel selection. Any number of conversions may be initiated between address changes. After initiating a conversion, the programmer must be careful not to sample the output or change the address until the entire conversion is complete. Consequently, a need-a-completion-pulse flip-flop is added to PDP-1, and the program must wait for the return. A status bit is included so the program may determine the origin of the pulse if several devices are operating simultaneously. With PDP-4 and PDP-5 the program should wait for the converter flag (status bit) to go on.

PDP-1 Instructions

Select Multiplexer Channel . . . . . scv Instruction Code 72KN47

Select channel KN, that is, the channel addressed by bits 6 to 11 of the instruction word.

Index Multiplexer Channel . . . . . icv Instruction Code 720060

Index MAR to address the next channel in sequence. If MAR already addresses the final channel, the instruction returns it to channel 0.

Convert A-D . . . . . cad Instruction Code 720040

Initiate a conversion on the channel selected by MAR.

Read Converter Buffer . . . . . rcb Instruction Code 720031

Transfer the converter binary output into bits 0 through 11 of the computer in-out register and clear the converter status bit.

PDP-4 Instructions

Select Multiplexer Channel . . . . . adsm Instruction Code 701103

Select the channel addressed by bits 12 to 17 of the accumulator.

Index Multiplexer Channel . . . . . adim Instruction Code 701201

Index MAR to address the next channel in sequence. If MAR already addresses the final channel, the instruction returns it to channel 0. The accumulator must be clear when this instruction is given unless the converter includes an option which obviates this requirement.

Convert A-D . . . . . adsc Instruction Code 701304

Initiate a conversion on the channel selected by MAR.

Skip on Converter Flag . . . . . adsf Instruction Code 701301

Skip if the converter flag is on, indicating that the converter contains binary information not yet read in.

Read Converter Buffer . . . . . adrb Instruction Code 701312

Transfer the converter binary output to bits 0 through 11 of the accumulator. An option is available which allows the instruction to clear the converter flag.

PDP-5 Instructions

Select Multiplexer Channel . . . . . adsc Instruction Code 6543

Select the Multiplexer channel which is indicated by bits 6 through 11 of the accumulator.

Index Multiplexer Channel . . . . . adic Instruction Code 6544

Index the MAR to address the next channel in sequence. If the MAR already addresses the final channel, the instruction returns to channel zero.

Clear Multiplexer Channel . . . . . adcc Instruction Code 6541

Clear MAR to address channel zero.

Convert A-D . . . . . adcv Instruction Code 6532

Initiate a conversion on the channel selected by the MAR.

Skip-On Converter Flag . . . . . adsf Instruction Code 6531

Skip if the converter flag is on, indicating that the converter contains binary information not yet read in.

Read Converter Buffer . . . . . adrb Instruction Code 6534

Transfer the converter binary output to bits 0 through 11 of the accumulator. Clear the converter flag.

OPERATION WITH OTHER EQUIPMENT

The clear, readin, index, and convert pulses, which control the multiplexed analog-to-digital converter, must fulfill the specifications listed in Section 1. Furthermore, there are certain timing restrictions on the programming of these pulses.

To select a channel, clear must precede readin by at least 1 microsecond, and the address input levels must be asserted at least 2 microseconds before readin. The maximum interval between pulses is dependent upon external control requirements; the multiplexer must be off from clear to 1 microsecond after readin. The maximum available off-interval is 0.2 second.

To sequence the MAR, the address inputs must be negated at least 2 microseconds before index unless the system includes the option which eliminates this requirement. Following index, the multiplexer remains off for the same length of time as when selecting a single address (that is, for 1 microsecond longer than the clear-readin interval). If analog source impedances are sufficiently low, convert may occur within a few hundred nanoseconds after multiplexer turn on. However, for high source impedances, convert must be delayed from 1 to 2 microseconds. An optional feature allows any address change to initiate a conversion, in which case the hardware provides an appropriate delay.

After initiating a conversion, no input pulse should occur until after the conversion is complete. Total conversion time is a function of switch settings as listed in System Operating Specifications (Section 1).

When the status level (flag) changes from 0 to -3 volts, the external controlling device may sample the digital output. One option provides a completion pulse in addition to the level change. Another allows the sampling pulse to clear the assembler, turning off the converter flag. This positive pulse must have the same characteristics as the other control inputs. Either an address change or another conversion may be initiated immediately after sampling.

SECTION 3

SYSTEM LOGIC

This chapter provides a detailed logical description of the multiplexed analog-to-digital converter. The system may be divided into two sections: the Type 139 Multiplexer Control and the Type 138 Analog-to-Digital Converter. The former, together with the multiplexer switch matrix, selects the desired analog channel and connects it to the converter input. The latter transforms the selected analog information to a digital word.

Three logic diagrams found at the end of Section 6 are referred to throughout this section. Digital's numbering system for these engineering drawings is as follows: The first two letters, BS, stand for block schematic; the second, D, indicates the size of the drawing; the third, 138 or 139, specifies the system to which the drawing pertains; and the last group, 01 or 02, gives the drawing number.

Engineering drawing BS-D-139-02 shows the multiplexer control logic, including a multiplexer address register (MAR), two binary-octal decoders, and a 5 megacycle carrier generator. The carrier and the decoder outputs are applied to the analog multiplexer (BS-D-139-01), which may contain from 2 to 64 switches, arranged in an 8 x 8 matrix. The decoder at the right in BS-D-138-01 selects a single row of switches according to the three less significant MAR bits. The second decoder selects a single column according to the three more significant bits. When the 5 megacycle carrier is present in the matrix, the switch at the intersection of the two asserted decoder outputs connects the single connected analog line to the common output from all switches, which is itself connected to the analog input of the analog-to-digital converter.

The 10 megacycle clock (upper left, BS-D-139-02) complements a 6202 Flip-Flop. The signal is applied to the multiplexer matrix to drive the third diode input on all switches. The logical gating is transformer-coupled to the switch for complete dc isolation. The 5 megacycle carrier couples the switch gating levels to the secondary of the selected switching transformer. A complete description of the Type 1578 Multiplexer Switch is included in Section 4.

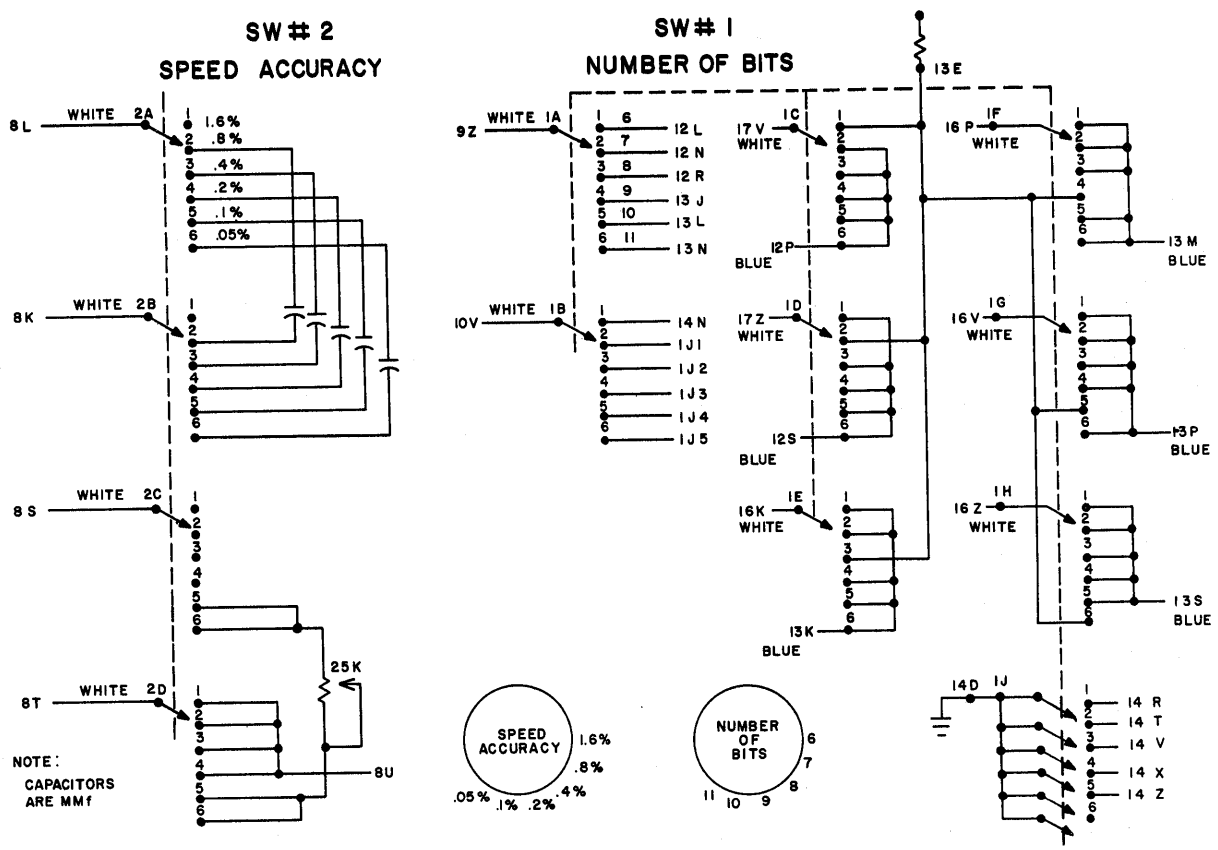


Figure 3-1 Control Panel Switches

Multiplexer address control inputs are shown at the left in drawing BS-D-139-02. Single addressing is initiated by clear, which clears MAR via a 4604 Pulse Amplifier. Pulse length is expanded to 1 microsecond to allow MAR carries to die out. Clear also triggers a 4301 Delay whose level output immediately inhibits the 5 megacycle carrier to protect the multiplexer switches and to isolate the converter during switching. The length of this delay can be varied from 2.5 microseconds to 0.2 second, according to external control requirements (lengths for use with PDP-1 and PDP-4 are 3.3 and 3.0 microseconds).

During the delay interval, readin loads a new address into MAR by performing a ones transfer on the multiplexer address inputs (bottom, BS-D-139-02). An optional inverter module is shown below them, for use when input assertion level must be -3 vdc. Each half of the

register is then separately decoded by a 4150 Binary-Octal Decoder, and the two asserted levels select the appropriate row and column in the multiplexer matrix. At the end of the delay interval, the carrier is restored to the array.

A second 4301 Delay (optional) may be driven by the terminating pulse of the first delay to initiate conversion automatically. This makes possible a variable delay between multiplexer turn on and the start of conversion. (A delay is sometimes necessary when the selected analog signal requires time to charge line capacitance, that is, when its driving source impedance is high). Note: This option can not be used with PDP-1.

To address channels sequentially, index increments the number in MAR by complementing the least significant bit. The pulse also triggers the carrier inhibiting delay to protect the multiplexer array during the address change as previously described. During indexing, the MAR address inputs are unused and must be negated at least 2 microseconds before indexing begins.

When the number of switches required is less than the full complement of 64, it is possible to short-cycle the counter by connecting the two decoder outputs corresponding to the highest numbered channel directly to the AND gate shown at the lower left in BS-D-139-02. When the number in MAR is the address of the final channel, the capacitor-diode gate at the 1 input of flip-flop FF (left end, 4222 module) is thereby enabled. The next index then sets the flip-flop, clearing the counter. When all 64 switches are used, this flip-flop has no function and its output may be disconnected.

When it is inconvenient to negate multiplexer address inputs before indexing, an optional 4606 Pulse Amplifier with a capacitor-diode gate input may be used to short-cycle the counter (this amplifier is shown immediately to the right of the inverter AND gate). It is then unnecessary to apply index to the address input gates; instead it is applied directly to the 4606 whose output is connected to the MAR clear input. The FF output is then disconnected, and the state of the MAR address inputs may be disregarded during indexing.

The Type 138 Analog-to-Digital Converter is shown in BS-D-138-01. As outlined in Section 2, the converter uses the successive approximation method to generate a binary number proportionl to an input voltage. An internal voltage, derived from a 1704 Precision -10 Volt Reference Supply, is generated in binary-weighted steps by a digital-to-analog converter (top, BS-D-138-01). The digital-to-analog is controlled by signals from a digital register

(AD) with gatable 1 and 0 inputs. The distribution register, which determines the next step to be taken, is directly below the AD register. The comparator is in the upper left of the figure; the control timing loop at the lower left. Panel switches controlling word length and conversion accuracy are also shown at lower left.

The distribution register, SH, shifts a single one from left to right at each time pulse. The position of the one determines the next step taken. At the start of conversion, convert clears AD and SH, with the exception of AD_0 and SH_0, which are set. Convert also triggers the timing loop. MSB input F of the 1574 Ladder is now disabled while all other inputs are enabled, since their associated level amplifiers are driven by the 0 AD outputs. The digital-to-analog voltage supplied to the 1572 Comparator is therefore slightly less than half full-scale (approximately -5 volts). The comparator output at F is 0 vdc if the digital-to-analog voltage at P is positive with respect to the analog input voltage at N. If P is relatively negative, pin F is also negative.

The convert pulse entering the time chain is twice delayed: first by a 1 millisecond Type 1310 Delay Line; then by a Type 1304 One-Shot. The 1304 Delay may be varied with the 6-position SPEED/ACCURACY front panel switch. Delay times of 1.5, 2, 2.5, 3, 5, and 8 microseconds per bit correspond to maximum comparator switching point errors of ±1.6, ±0.8, ±0.4, ±0.2, ±0.1, and ±0.05 per cent. The 1304 terminating pulse generates a set pulse which is applied to the AD 1 input gates and to the shift register. Since SH_0 is 1, AD_1 is set, and a 1 is shifted into SH_1.

The 1304 terminating pulse also generates clear concurrently with set if the comparator output is at ground, indicating that the ladder output is lower (that is, more positive) than the analog input. Clear is applied to the 0 input gates of the AD register. If it is present during the first step, AD_0 is cleared, restoring the MSB voltage increment to the digital-to-analog converter and increasing the digital-to-analog output to three-fourths full-scale. AD_0 remains set if clear is absent (digital-to-analog inputs F and H would then both be disabled resulting in one-fourth full-scale output at E).

The level output termination of the 1304 Delay is gated with AD_i^0 (the LSB selected by SW1) to recycle the time chain. The next set pulse then sets AD_2; AD_1 either remains set or is cleared, depending upon comparator output. The 1 in SH_1 is now shifted to SH_2; enabling

set and clear inputs ot AD_3 and AD_2, respectively. This procedure is repeated until AD_i is set. Since AD_i gates the 1304 output level termination via SW1A, further time pulses are now inhibited; the remaining pulse present in the chain then sets AD_{i+1}. The 0 output of this flip-flop is connected through the output buffer, to SW1B to an inverter for use as a converter status bit (-3 volts = conversion complete).

When SW1 is set for N-bit conversion, tne converter output is N bits. The pulse amplifier shown to the right of tne status inverter in BS-D-138-01 develops an optional completion pulse. Another optional PA at lower left allows the assembler, and hence, the converter status bit, to be cleared without also converting.

SECTION 4

CIRCUIT DESCRIPTION

This chapter describes the 17 circuits used in the multiplexed analog-to-digital converter. Schematic diagrams of the circuits described here are grouped in order by type number at the end of the manual. No figure reference is made in this chapter, but reference to the applicable schematic is implied.

INVERTERS AND DIODES

The Type 138-139 unit uses two 10-megacycle inverter modules, Types 6102 and 6106, and a binary-octal diode matrix, Type 4150. Each inverter module includes a -3 vdc supply and has a clamped load associated with each inverter transistor. The 6102 contains nine inverters with emitters grounded internally. The base and collector of each inverter are available at the module connector. The 6106 contains six inverters; the base, collector and emitter are available at the connector. In both types, optional internal jumpers may connect clamped loads to individual inverter outputs (actual connections made are shown on the logic drawings). Delay through a 6000 series inverter is approximately 12 nanoseconds. Both inverter types may be used either as level gates or as pulse gates, and both are driven by Digital Standard Negative Levels and Pulses.

Inverter transistors are operated either in saturation or in cutoff. The collector-emitter impedance of a saturated transistor is very low; at cutoff, it is very high. Consequently, if the emitter is at ground and the collector is connected to a -3 vdc clamped load, the collector output level or pulse is inverted with respect to the base input.

Base input loading is determined by the 3K base resistor. When an inverter emitter is grounded, a saturating current of 1 milliampere flows through the transistor when -3 vdc is present at its base. A base bypass capacitor is provided at each input to provide overdriving current which speeds transistor switching. When the base is at ground, the 68K resistor to +10 vdc supplies I_{CO} to ensure good dc cutoff. This resistor also prevents accidental transistor turn on by noise pulses.

The diode in the clamped load limits the negative voltage at the inverter outputs, supplying whatever current is needed to maintain the output at -3 vdc. This current is a maximum of 8 milliamperes under no-load conditions, and decreases to zero as the current drawn from the external load increases to 8 milliamperes. The value of the clamped load resistor thus determines the maximum external load current at which the inverter may maintain a regulated -3 vdc output.

The -3 vdc supply is established by four 0.75 vdc forward voltage drops across four series connected 1N645 Silicon Diodes. The 560-ohm resistor for this supply accepts enough current to maintain the -3 vdc even under minimum load conditions.

The 4150 Binary-Octal Decoder contains a diode matrix and eight inverter outputs, each with a -3 vdc clamped load. The diode matrix is driven by the 1 and 0 outputs of three flip-flops (a given flip-flop contains a ONE when its 1 output is at -3 vdc). The input to each inverter transistor is a 3-diode positive AND gate. The 0 vdc output of a gate is uniquely asserted when the proper combination of ones and zeros is present in the three associated flip-flops. The binary input is thus represented by eight discrete output levels. When all flip-flops are ZERO, the output of the leftmost gate on the schematic (with inputs connected to the 1 outputs of all three flip-flops) is at ground. The outputs of all other diode gates are at -3 vdc. At any time, therefore, all 4150 Inverter outputs are at ground except the one driven by the satisfied diode input gate.

FLIP-FLOPS

The Type 138-139 unit uses three types of flip-flops. One of these, the 10-megacycle series Type 6202, contains one buffered flip-flop. The Type 4222 is a 1-megacycle flip-flop module, wired internally as a 7-bit counter. The Type 4226 (also 1 megacycle) contains two 4-bit flip-flop registers, which function as a combination buffer and shift register, and three pulse inverters.

Seven-Bit Counter

This module contains seven flip-flops, each with readin gates, and two pulse inverters. One inverter clears the flip-flops; the other drives the gates. Both outputs of flip-flop A are brought out to the connector to provide carry output. Flip-flops B to G each have only one output

connector pin. The selected flip-flop output is connected to the associated pin by an internal jumper. Complement-type capacitor-diode input circuitry is provided for each flip-flop.

The following description refers to the pulse gate having level input terminal W, but applies equally to the other gates on the module. The circuit is activated by applying a Digital Standard Negative Pulse to readin terminal Y. This pulse is inverted by transistor Q16; the resulting positive pulse is applied to the pulse gate comprising diode D40 and the capacitor-resistor combination at the D40 anode. The pulse rising edge is differentiated by the capacitor and may, if the gate is enabled by ground level at W, be applied through D40 to the flip-flop input. The sharp negative spike caused by differentiation of the pulse trailing edge is discharged through the resistor. A negative level (-3 vdc) at W disables the gate by providing dc back bias to D40.

A logical delay is built into the circuit to prevent race problems. Because of this delay, the ground enabling level must be presented at least 1 microsecond before the arrival of the input pulse.

Readin input Y accepts a Digital Standard 0.4-microsecond Negative Pulse. Clear input Z accepts a negative 1-microsecond 2.5-volt pulse (as may be obtained from a Type 4604 Pulse Amplifier). The longer clear pulse is necessary to allow carry pulses in the counter to die out. The start of the clear pulse must precede the count by at least 1 microsecond. Count input X accepts a Digital Standard 0.4-microsecond Positive Pulse, or a positive step of 3 volts with rise time less than 0.2 microseconds. An assertion level must be present at least 2 microseconds before readin; a negation level must be present at least 2 microseconds before readin. Maximum operating frequency of the 4222 Counter is 1 megacycle.

The module is connected internally as a counter by jumpering the complement input of each flip-flop to the 1 output of the preceding flip-flop. For example, if the counter is initially clear, a count pulse input at X complements FFG to ONE because the gate is enabled by ground at the Q14 collector. The 1 output of this flip-flop (-3 vdc) is applied to the complement input of F. When the second count pulse arrives at X, G returns to ZERO, so its 1 output rises to ground. This positive-going transition is coupled through the complement gate of F and is applied to the Q12 base, setting F. The count may continue in this manner until the counter recycles to all zeros or is cleared by a negative 1-microsecond pulse at Z. The count may be begun with any desired number, using the parallel readin gates and pulse input Y.

The orange components on the circuit board contain one of two combinations of passive elements (as shown on the schematic).

Serial-to-Parallel Assembler 4226

This module contains two 4-bit flip-flop registers and three pulse inverters. Transistors Q1 to Q8 make up a buffer register whose bits may be conditionally set or cleared to form the successive approximation of an analog voltage. Transistors Q9 to Q12 and Q16 to Q19 form a shift register which programs the buffer register. The orange components on the etched circuit board contain one of two combinations of passive elements (as shown on the schematic).

The 4226 module accepts three Digital Standard 0.4-microsecond Negative Pulses at pins H, Y, and Z. The preset and read ones inputs are applied through inverters to both registers. The read zeros input, pin Y, is applied through an inverter to the 0 input gates of the buffer register only. Both inputs (U and W) and both outputs (T and X) of the shift register are available, allowing the register to be linked with other modules to form a continuous register of any desired length. When the 4226 is used as the initial 4-bit section of the serial-to-parallel assembler register in the Type 138, the set input gates, pins V and W, are therefore baised off by -3 vdc clamped loads at F and E.

Internal jumpers are provided on the module to allow the preset input to set up any desired initial condition; in the 138 unit this input clears the buffer register except for the most significant bit, which is set.

The 0 output of each flip-flop in the shift register is applied to the input gating of two buffer register flip-flops, in particular to the 0 input gate of one buffer flip-flop and the 1 input gate of the next. In its usual application, a single one is shifted down the shift register, each shift enabling a pair of buffer flip-flops. A subsequent read ones pulse at Z sets the buffer flip-flop whose 1 input is enabled by the shift register; if a read zeros pulse occurs, it clears the buffer flip-flop whose 0 input is enabled. The read ones pulse also shifts the 1 in the shift register to the next bit. The process is then repeated with the next set of read pulses.

The 4226 flip-flops are similar in design to those of the 4222, except for the number of access terminals and method of interconnection.

Flip-Flop 6202

This module contains a single buffered flip-flop, two inverters, and a standard -3 vdc supply. The usual -3 vdc load is omitted, since adequate loading is provided through the collector resistors of the nonconducting transistors.

Inputs to the Type 6202 Flip-Flop are direct set, direct clear, 0 in, 1 in, and two complement inputs (N, P, T, E, J, and L respectively). The set and clear inputs accept 40-nanosecond, 2.5-volt positive pulses. The four remaining inputs must be driven by pulse gate collectors. The minimum 6000 series interpulse spacing is 100 nanoseconds (10 megacycles).

Outputs are 0 out, 1 out, and two carry pulse outputs (F, R, H, and M respectively). The carry output at H is a Digital Standard 40-nanosecond Negative Pulse and is produced by a complement input pulse at J. Carry output M is identical to H; the pulse occurs on a complement input at L.

When the flip-flop contains 0, F is quiescent at -3 vdc and R is grounded; Q3 is saturated and Q4 is cut off until the flip-flop is set by an incoming trigger pulse. The trigger is applied to Q3 via 1 input E or either complement input (the Q4 base is unaffected by a complement pulse when the flip-flop is 1). When Q3 is cut off by the set input pulse, the negative transition at its collector is coupled through R11 and C9 to the Q4 base. Q4 then conducts so its collector rises to ground. This level is coupled through R13 and C14, back to the Q3 base, maintaining Q3 at cutoff. The flip-flop is now quiescent in the ONE state. Transistors Q2 and Q5 drive the 0 and 1 outputs respectively.

To trigger the 6202 with negative-going input pulses, inputs are applied through pulse inverters such as Q1 and Q6. The Q1 collector (X) is normally jumpered to 1 input E, while Q6 collector U is connected to 0 input P. The inputs are held at -3 vdc by clamped loads D3-R4 and D22-R21. Capacitors C5 and C17 and associated resistors ac-couple positive pulses to the base input diodes.

Input gates Q1 and Q6 may be inhibited by applying -3 vdc to their emitters. Ground levels at these points allow the flip-flop to be set by a Digital Standard 40 nanosecond Negative Pulse at Y. A pulse at V clears the flip-flop. The set pulse at Y, for example, is inverted at Q1 and coupled through C5, D7, and D9 to the Q3 base.

Capacitors C12 and C13 synchronize the change in flip-flop outputs during switching and ensure at least a 30 nanosecond delay between flip-flop and output buffer switching. If these capacitors were not present, the 0 output would tend to change before the 1 output when the flip-flop was set. This lag would occur because Q2 would turn on directly with Q3 cutoff. However, Q5 would not cut off until Q4 had saturated. To avoid this condition, C13 delays the Q2 saturation by sharing the driving current from Q3. C12, on the other hand, accelerates Q5 cutoff by coupling the positive transition at the Q2 collector to the Q5 base. When the flip-flop is cleared, the functions of C12 and C13 are reversed; C12 shares the driving current to the Q5 base and C13 speeds Q2 turn off.

The Type 6202 Flip-Flop is complemented when a positive pulse arrives at either J or L from the collector of a pulse gate. Since both complement circuits function in the same manner, the following description, including pin J, applies equally to the description including pin L.

Assume that the flip-flop initially contains 0. Since Q3 is on and Q4 off at this time, T1 terminal 5 is ground and T1 terminal 8 is -3 vdc.

When a complement pulse arrives at J, it is coupled to the T1 secondary as a positive-going pulse from ground at terminal 6 and as a positive-going pulse from -3 volts at terminal 7. Because pulse height does not exceed 3 volts, the pulse at 7 is unable to forward bias D8 and therefore cannot reach the Q4 base. The pulse at 6, however, is positive with respect to ground and pulls up the Q4 base. The flip-flop consequently changes state by the previously described method.

T1 contains a third secondary winding with one side, terminal 4, at ground. This winding is phased so that a negative-going pulse from ground appears at terminal 3 (output H) as a consequence of the positive pulse at J. This output signal is a Digital Standard 40-nanosecond Negative Pulse. R8 and D6 are included to clamp the overshoot of T1, which prevents spurious pulses at the transformer secondary.

An indicator driver output is provided at S; when the flip-flop contains ONE, -3 vdc is supplied to the indicator transistor. R22 limits output current to 1 milliampere and prevents the line capacitance from loading the flip-flop.

The 6202 used in the 139 unit is driven at a 10 megacycle rate by Clock 6403 to supply a 5 megacycle carrier to the analog-to-digital multiplexer array.

PULSE CIRCUITS

The system includes two pulse amplifiers and one crystal clock. Both the 4604 and 4606 Pulse Amplifiers are 1 megacycle types; the 6403 Crystal Clock is set at a frequency of 10 megacycles.

Pulse Amplifier 4604

This module contains three identical pulse amplifiers which provide amplified and standardized pulses to any width between 0.4 and 1 microsecond. Each pulse amplifier has two control pins for determining output pulse width. When these control terminals are left open circuited, the unit amplifies all input signals to Digital Standard 0.4-microsecond Pulses at pulse repetition frequencies up to 1 megacycle. When the control terminals are shorted together, the unit standardizes inputs to produce 1-microsecond pulses at any rate up to 330 kilocycles (one amplifier is connected in this manner in the 139 unit). Any pulse width between 0.4 and 1 microsecond is obtainable by connection of an appropriate external capacitor between the two control terminals. Maximum pulse rate frequency varies with the pulse width from 330 kilocycles to 1 megacycle.

The first pulse amplifier includes transistors Q1 to Q3, with inputs at E and F, and outputs at J and H. The second PA comprised Q4 to Q6, with inputs M-N and outputs S-T. The third includes Q7 to Q9, with inputs Y-Z and outputs V-X. Control terminals for the three amplifiers are K-L, P-R, and U-W, respectively.

Inputs E, N, and Z accept negative-going signals with an amplitude of 2.5 to 4 volts, fall time less than 0.5 microseconds, and width greater than 60 nanoseconds. Inputs F, M, and Y accept positive-going signals with the same characteristics. The following description of the circuit including Q1 to Q3 applies equally to all three pulse amplifiers.

The pulse amplifier comprises a monostable multivibrator (Q1 and Q2), and an output pulse amplifier (Q3). Capacitor-diode C4-D2 couples a negative input at E to the Q2 base; C3-D23 couples a positive input to the Q10 base. This transistor inverts the positive input; the resulting negative pulse at its collector is applied directly to the Q2 base. An appropriate pulse at either input thus provides a negative pulse at this point. The negative pulse triggers the multivibrator generating a negative output pulse. This pulse is amplified by the Q3 circuit; the output is negative at J if H is grounded, or positive at H if J is grounded.

Quiescently, Q1 is on; Q2 and Q3 are off. Base current for Q1 flows through R1 to the -3 vdc supply, holding Q1 in saturation. Voltage divider R7-R9 maintains a small positive voltage at the Q2 base, keeping Q2 cut off. D1 clamps the Q2 collector to -3 vdc. Voltage divider R8-R10-R13 biases the Q3 base positive, holding it off. The Q3 collector potential is approximately -7 volts, as determined by voltage divider R11-R14. No current flows in the T1 primary, and no voltage exists across the secondary.

When a negative pulse appears at input E, C4 differentiates its leading edge generating a negative pulse at the D2 cathode. D2 is now forward biased, so the signal appears at the Q2 base. As Q2 turns on, its collector voltage jumps from -3 volts to ground. This positive step is coupled by C2 (or C1 in parallel with C2, if pins K and L are jumpered) to the Q1 base. Q1 now cuts off and its collector potential drops to -3 volts. R7 holds Q2 on at this time, even though the input pulse is ended. The multivibrator remains in this state until the coupling capacitance (C2, or C1 and C2) from the Q2 collector to the Q1 base discharges. This discharge time is proportional to the capacitance; it is either 0.4 microseconds (if C2 only is used) or 1 microsecond (if C1 and C2 are both used). At the end of the appropriate interval, Q1 turns on, cutting Q2 off, as the multivibrator returns to its quiescent state.

The negative pulse generated at the Q1 collector turns on Q3. The Q3 collector now rises to ground, placing approximately 7 volts across the T1 primary. R11, R14, and C6 stabilize the voltage at T1 terminal 1; so the primary voltage does not diminish appreciably during the pulse. The secondary output voltage is proportional to the primary voltage. The pulse terminates when the multivibrator returns to its quiescent state, cutting off Q3. D5 and R12 damp the T1 primary overshoot, and D4 clips the overshoot at -15 volts to prevent excessive voltage at the collector.

A positive pulse at F, inverted by Q10, triggers the same chain of events to produce an output pulse across J and H.

Pulse Amplifier 4606

This module contains three identical pulse amplifiers which produce Digital Standard 0.4-microseconds, 2.5-volt Pulses. Each circuit comprises a monostable multivibrator and an output pulse amplifier. Inputs as narrow as 70 nanoseconds trigger the circuit. Maximum operating frequency is 1 megacycle.

Each pulse amplifier accepts three inputs: a positive pulse; a negative pulse; and a gated negative pulse. All pulse inputs represent one unit of pulse load. Either pulses or level changes may be used at any input. When level changes are used, a change in only one direction at a given terminal produces an output; that is, a positive-going change at F generates a pulse, while a negative-going change at the same terminal does not.

The gated pulse input is enabled by applying a Digital Standard -3 volt Level to the gate level input. This level must be present for at least 1 microsecond before the pulse arrives.

Each pulse amplifier delivers a Digital Standard 2.5-volt, 0.4-microsecond Pulse when an input pulse appears at any of the three pulse input terminals. Either positive or negative pulse outputs are available; the unused output is grounded.

The first pulse amplifier includes Q1 to Q4, with inputs E, F, and K and outputs H and J. The second comprises Q5 to Q8, with inputs at M, N, and S and outputs P and R. The third is made up of Q9 to Q12, with inputs at U, V, and Y and outputs W and X. The module also contains a -3 vdc supply, derived from the -15 volt input with diodes D28 to D31.

The 4606 Pulse Amplifier circuitry is identical to that of the 4604 with three exceptions: First, the 4606 has no provision for varying output pulse width; second, it includes capacitor-diode input gates; and third, it includes clamped loads, which may be connected directly to the positive pulse input with an internal jumper.

A capacitor-diode gate produces an output pulse in the presence of both a pulse and a level input. For example, in order to couple a negative pulse at K to the Q2 base, a Digital Standard -3 volt Level must be present at L. When this level is at ground, the potential at the junction of C5 and R13 is near 0 vdc. Since the D6-C6 junction is quiescently at -3 vdc, a negative pulse at K cannot sufficiently forward bias D6. A -3 volt level at L, however, results in 0 volts across D6, so that a negative pulse at K is coupled through D6 and C6 to the Q2 base.

D8 and R15 form a clamped load to -3 vdc which may be connected with an internal jumper to the positive input line.

Crystal Clock 6403

This module contains a crystal oscillator, an oscillator output rectifier, and an output pulse amplifier. The crystal oscillator includes Q1 and Q2; Q3 is the rectifier. The pulse amplifier contains Q4 and Q5, and transformers T1 to T3. The 6403 generates Digital Standard 40 nanosecond Pulses, either positive or negative, at a frequency determined by the oscillator crystal. This frequency may be between 5 and 10 megacycles; in the Type 139 units the crystal is series resonant at 10 megacycles. Negative pulses may be obtained at E or positive pulses at F; the unused pin must be grounded.

Positive feedback from the Q2 collector to the Q1 base via crystal CR-1 sustains oscillations at the resonant frequency. The oscillator output is taken from the Q2 collector. Since the impedance of CR-1 is minimum at resonance, the positive feedback is maximum at that frequency, that is, 10 megacycles.

The parallel resonant circuit L1-C2, tuned in the vicinity of 10 megacycles, helps to stabilize the circuit gain and makes it possible to tune the oscillator through a narrow band about the crystal resonant frequency.

Zener diode D7 in series with D6 stabilizes the -4.65 vdc oscillator supply, making it effectively independent of supply variations. Three other voltages are derived from the Zener voltage by means of R7 to R10: -1, -1.3, and -3 vdc. Noise appearing on any of the four voltages is bypassed to ground through capacitors C3 to C6. R2 is the collector load resistor for Q1 and is returned to -6.8 vdc.

The sinusoidal Q2 collector output feeds the Q3 emitter. This 10-megacycle signal is also averaged by R5-C5 to provide a dc level at the Q3 base, which is clamped so it can become no more negative than -3.3 vdc.

When Q3 conducts, its collector rises from -6.8 vdc to the sine wave average level. This voltage transition appears across the T1 primary, resulting in a negative pulse at the Q4 base, driving it rapidly into saturation, and grounding the Q4 collector. Q4 thus places 7.5 volts across the T2 primary. The duration of this pulse is dependent, not upon the duration of the pulse at the T1 secondary, but upon the time necessary for the T2 primary voltage to decay across R14 (approximately 40 nanoseconds). This pulse is further amplified and shaped by Q5 and is coupled through T3 to outputs F and E.

A series-connected diode and resistor are included across each transformer primary to prevent ringing.

DELAY CIRCUITS

The 138-139 system contains three types of delay circuits: two monostable multivibrators and one delay line.

Delay 1304

This module contains an input pulse gate (Q1), a monostable multivibrator (Q2, Q3), an output level amplifier (Q4), and an output pulse amplifier (Q5). When input terminal X is grounded either directly or through the inverter, level output J switches from its quiescent ground level to -3 volts for a predetermined interval, then returns to ground. At this final level transition, a pulse is generated at either E or F, depending on the pulse polarity desired. The delay interval is determined primarily by the capacitor connection (three capacitors are available internally or an external capacitor may be used). When U and T are jumpered, an internal potentiometer may be used for delay adjustment. Circuit recovery time is equal to 20% of the maximim delay available for a given capacitor connection.

A Digital 70 nanosecond Negative Pulse applied to input Y triggers the delay circuit if Z is enabled by a ground level. An external pulse gate may also trigger the delay directly at X. Following the delay period, a Digital 70 nanosecond Pulse is generated at either E or F. If E is grounded, a positive pulse appears at F; if F is grounded, a negative pulse appears at E.

Using only internal components, the delay may be varied from 0.25 microseconds to 500 microseconds in three ranges. With U jumpered to T, potentiometer R5 varies the delay within any range. With no other external connection, C3 provides the minimum range. Other ranges are selected by jumpering H to N or M, thereby adding C4 or C5 into the multivibrator circuit. Delay ranges for these connections are as follows:

None	0.25 to 2.5 μsec
H-N	2.5 to 35 μsec
H-M	35 to 500 μsec

If external delay control is desired, a potentiometer may be connected between pins S and T. Higher delay ranges may be added by connecting an external capacitor between pins L and K.

In the quiescent state Q1, Q3, and Q5 are off; Q2 and Q4 are on. Q1 is held off by a ground level at its base or -3 vdc at its emitter. A current of 2.5 milliamperes flows from -3 vdc through D15, R20, the T1 primary, and R7 to the -15 vdc supply; 5.5 milliamperes flows from the -3 vdc supply through D2, R21, and R7 to -15 volts. The resulting 8 milliamperes through R7 maintain the Q1 collector at about -4 vdc.

Since a steady state current is flowing in the T1 primary at this time, no voltage appears across the secondary. Current flowing from the Q2 base through R3 and the parallel combination R5-R6 (when T is connected to U) holds Q2 on.

When the 1304 Delay is triggered by a pulse at X or Y, the resulting 4-volt drop across the T1 primary is coupled to its secondary winding. Terminal 4 now goes negative, as current through the primary increases linearly from the quiescent value of 2.5 milliamperes to 8 milliamperes. During this increase, the voltage across the primary at first remains nearly constant because of the clamping action of D2 and R21. When the T1 primary begins to draw more than 8 milliamperes, however, the negative-going level at terminal 2 back biases D2, removing R21 from the primary circuit. As the resistance of the primary circuit is thus increased, the primary voltage tends to decrease more rapidly. C2, however, provides an ac shunt to R7, which times the primary current to generate the proper pulse width into trigger diode D1.

This negative pulse at T1 terminal 4 is coupled through D1 to the Q3 base. Q3 then turns on and its collector rises to ground. The low forward resistance of D5 and D6 shunts the T2 primary, so no current flows in its secondary. As Q3 turns on, the junction of D4 and R12 rises to ground, turning off Q4. The output level at J then drops to -3 vdc, indicating the start of the delay interval.

The ground at the Q3 collector is applied through D5 to pin H. It is, in turn, coupled to the Q2 base by either C3, C4, or C5 (depending upon the connections made to H). Q2 is now cut off and its collector drops to -3 vdc. R4 then draws base current from Q3, holding Q3 on even after the pulse at T1-4 ends.

The monostable multivibrator comprising Q2 and Q3 remains in this state (Q2 off and Q3 on) for the time interval required to charge the capacitance in the Q2 base circuit. The RC time constant which determines this interval depends upon the capacitors in use and the resistance of R3 in series with the parallel combination R5-R6.

When the time delay capacitors have charged to a sufficiently negative voltage, Q2 turns on. The rise in Q2 collector voltage is now coupled through R4 and C6 to the Q3 base, cutting it off, which causes the T2 primary current to fall to its quiescent level. The resulting negative pulse in the T2 secondary is applied to the Q5 base, turning it on. The pulse amplifier made up of Q5 and T3 generates a Digital Standard 70-nanosecond Pulse across outputs E and F. This PA output circuit is similar to that of the 4604 module with one exception; C8 in the 1304 tunes the T3 circuit to give the correct output pulse width. When the transformer voltage has dropped to zero, the output pulse ends.

As Q3 turns off, the junction of D4 and R12 returns to -3 vdc, turning on Q4. Level output J therefore returns to ground, indicating the end of the delay.

Delay Line 1310

This module contains a delay line which provides up to 1 microsecond of delay in 50-nanosecond steps, plus an inverter driven by the delay line output. The emitter and collector of the inverter are brought to the external connector and therefore are available for logical gating.

If a Digital Standard 70 nanosecond Negative Pulse is applied to pin X, a pulse to ground appears, after a predetermined delay, at inverter output E. A clamped load is usually connected to E (or some electrically equivalent point) to hold it negative while the inverter is off. The circuit may also be used to delay level transitions.

The delay interval is determined by external connections made at pins J to W, which are connected to taps on the delay line. These taps allow delays of from .05 to 1.00 microsecond in multiples of .05 microseconds. To decrease the number of pins required, only part of the line is tapped in .05-microsecond increments; the remainder provides .2 microsecond steps.

To select a given delay, two jumpers are required: one selects a multiple of .2 microseconds; the other adds a multiple of .05 microseconds (either delay may be zero). The former is selected by one of the following jumper connections:

U to N	.00 μsec
V to P	.20 μsec
V to R	.40 μsec
W to S	.60 μsec
W to T	.80 μsec

The additional miltiple of .05 microseconds is selected by one of the following jumper connections:

H to N	.00 μsec
H to M	.05 μsec
H to L	.10 μsec
H to K	.15 μsec
H to J	.20 μsec

To the figures listed above, add 20 nanoseconds for the delay across the inverter. For example, to produce a total delay of exactly .97 microseconds, jumper W to T and H to K (.80 + .15 + .02 = .97).

When the circuit is quiescent, R1 furnishes cutoff current to hold Q1 off. Terminating resistors R2 and R3 prevent signal reflections from the ends of the delay line. By attenuating the short-delay output signals, R4 and R5 compensate for the attenuation of long-delay signals traversing a greater line length. D1 isolates the input from reflections caused by mismatch at the output tap.

Delay 4301

This module contains an input pulse gate (Q1), a monostable multivibrator (Q2 and Q3), an output level amplifier (Q4), and an output pulse amplifier (Q5). When input pin X is grounded by a Digital 0.4 microsecond Pulse, either directly or through the pulse gate, another 0.4-microsecond pulse is generated at output E or F after a predetermined delay. If E is grounded, a positive pulse appears at F; if F is grounded, a negative pulse appears at E.

In addition to the pulse output at E or F, the 4301 produces a level output at J. This output, quiescently at ground, falls to -3 vdc during the delay interval. Using only internal components, the delay may be varied from 2.5 microseconds to 200 milliseconds in five ranges. Potentiometer R7 can be used to vary the delay within any range by jumpering U to T. With no other external connection, C4 provides the minimum range. Other ranges are selected by jumpering H to either N, M, P, or R, thereby adding one of C5 to C8 into the multivibrator circuit. C4 provides a delay of 2.5 to 25 microseconds. The additional values of capacitance (C5 to C8) each increase the range by a factor of approximately 10.

Circuit recovery time is 20 per cent of the maximum delay in the selected range. If external fine control of the delay interval is desired, a potentiometer may be connected between S and T. Larger delay ranges can be achieved by connecting an additional capacitor between L and K.

When the circuit is quiescent, current from the Q2 base flows through R6 and the parallel combination R7-R8, holding Q2 on. The Q2 collector voltage is close to ground; so voltage divider R4-R9 holds Q3 off. Voltage divider R13-R14 holds the Q3 collector at about -6 vdc. No voltage exists across either the primary or secondary of T2.

Since Q4 is saturated by current through R13 and R14, level output J is at ground. The Q5 base is grounded through the T2 secondary, so Q5 is held off. The output pulse amplifier remains in its quiescent state and no output occurs across E and F.

The 4301 delay is triggered by grounding pin X, either directly or by means of a -2.5 volt, 0.4-microsecond pulse applied through Y to the Q1 base. If the Q1 emitter is grounded at Z, enabling this input gate, the transistor saturates, grounding its collector (X).

Terminal 2 of the T1 primary is now driven positive with respect to T1-1, and an increasing current flows through the primary. C2 bypasses the primary to prevent triggering by spurious noise pulses. The increasing current in the primary produces a negative voltage at secondary terminal 4. D1 couples this negative voltage to the Q3 base, turning Q3 on. The resulting ground at the Q3 collector is coupled through D7 and the parallel combination of C9 and R14 to the Q4 base, cutting this transistor off. The output level at J then drops to -3 vdc, indicating the start of the delay interval.

The ground at the Q3 collector is also applied through D5, R10, D6, and the selected delay capacitance back to the Q2 base. Q2 is therefore immediately cut off and its collector drops. R4 now draws base current from Q3, holding Q3 on even after the termination of the pulse from T1-4.

The monostable multivibrator remains in this state (Q2 off and Q3 on) for the time interval required to charge the capacitance in the Q2 base circuit. The RC time constant which determines this interval depends on the capacitor in use, plus the resistance of R6 in series with the parallel combination R7-R8.

When the time delay capacitors have charged to a sufficiently negative voltage, Q2 turns on. The consequent rise at the Q2 collector is now coupled through R4 and C3 to the Q3 base,

cutting off Q3. The current in the T2 primary therefore falls to its quiescent level, resulting in a negative pulse at T2-3. This pulse is applied to the Q5 base, turning Q5 on.

The pulse amplifier comprising Q5 and T3 then generates a Digital Standard 0.4-microsecond Pulse across outputs E and F. Operation of the pulse amplifier circuit is similar to that of the Type 1304.

When Q3 turns off, its collector voltage goes negative turning Q4 on. J therefore returns to ground concurrently with the output pulse E or F, indicating the end of the delay interval.

ANALOG-TO-DIGITAL CIRCUITS

Five special circuits implement the analog-to-digital conversion process in the multiplexed analog-to-digital converter. Up to 16 Type 1578 Multiplexer Switch modules select a single input from up to 64 channels. The selected input is matched against a sequence of precise voltages generated by an internal Digital-to-Analog Converter (ladder) Type 1574, in conjunction with a precision Power Supply Type 1704 and a set of Type 4679 Level Amplifiers. The fifth module, Difference Amplifier Type 1572, compares the internally generated voltage with the analog input.

Multiplexer Switch 1578

This module contains four identical multiplexer switches, each capable of switching a single analog input. Each circuit comprises a high speed inverter-amplifier, a 5-megacycle switch transformer, and a double-emitter output transistor that performs the analog switching operation.

The input to each circuit is controlled by a 4-input negative AND gate. Three inputs accept Standard Digital Logic Levels. A single multiplexer switch is enabled when these three inputs are negative (One input, M, is not required by the system and hence is open circuited.) The fourth input receives a 5 megacycle, 0 to -3 volt square wave from the output of a Type 6202 Flip-Flop driven by a Type 6403 Clock.

Four outputs of a single decoder are applied to gate inputs F, H, J, and K; a second decoder provides a gate signal at L that is common to all four switches. The carrier input is pin E. Pins R, T, X, and Z are the analog inputs; the selected analog output appears at P, S, W, or Y. An internal source of -3 vdc is derived from the -15 vdc supply. The following description of the switch with analog input R applies equally to the remaining three.

During quiescent operation (switch off), the output of the gate formed by D3, D4, D5, and D6 is close to ground potential, since at least one input is at ground. The Q2 base is therefore maintained at approximately +1.5 volts by R2, D1, and D2, holding Q2 off and open circuiting the T1 primary. The floating circuit driven by the T1 secondary is inactive at this time, resulting in a zero base-collector potential at Q1. Consequently, an effective open circuit exists between the two emitters of Q3.

When a switch is selected by the decoding matrix, negative logic levels appear at three of its gate inputs. The 5 megacycle carrier at E then activates the switch through the fourth input. The square wave is amplified and inverted by Q2 and is applied to the T1 primary. As the primary switches at a 5 megacycle rate (R3 and D7 are connected across it to prevent ringing), a corresponding ac signal is developed across its secondary. This signal is rectified by D8 and D9 to produce a dc level, positive with respect to the center tap, that is applied to the Q1 base. L1 and R4 are included to improve switching characteristics. The base-collector junction of Q1 is now forward biased, which is the condition necessary for conduction between the two Q1 emitters. Since the entire secondary circuit of the transformer is floating, the analog signal at pin R is transferred, through the double-emitter junction of Q1, to output P without significant alteration. During this period, the junction impedance is no greater than 50 ohms. The switch is deactivated when any of the three AND gate inputs returns to ground potential.

Level Amplifier 4679

This module contains four identical switching circuits that accept Digital Standard -3 and 0 vdc Levels and provide outputs of 0 and -10 vdc. Maximum operating frequency is 1 megacycle. Maximum total transition times are 0.2 microseconds for output rise and fall. K, P, V, and Z are the amplifier inputs; J, N, U, and Y, the outputs. The following discussion of the amplifier with input K applies equally to the remaining three.

When a ground level is applied to Q1 and Q2 via K, zero bias exists across their emitter-base junctions; so both transistors are nonconducting. The Q1 collector is pulled toward -15 vdc by its load resistor R4. Since pin J is connected to some voltage between 0 and -10 vdc through an external resistive load, a current path is established through this load, the Q9 emitter-base junction, D1, and R4 to -15 volts. Q9 is thus saturated by the ground at K, effectively placing the negative reference voltage at E across the output load resistance.

When -3 vdc is applied to K, both Q1 and Q2 saturate. The Q2 emitter is brought out separately at F, which must be connected either to chassis ground or to analog ground. The Q1 and Q2 collectors both rise to ground, placing 0 volts at output J and allowing R10 to pull the Q9 base positive by 0.75 vdc (the drop across D1). Q9 is now firmly cut off.

Since variations in transistor parameters may cause small differences in output impedance between upper and lower transistors, small resistances are placed in series with the lower transistor output. These provide a means for matching transistor output impedances. Additional lugs are provided on the circuit board so the resistors may be individually bypassed with jumpers, if desired. In the 138 unit, the constant series resistance remaining is trimmed out by the potentiometers in the ladder.

The 4679 output impedance may be measured and adjusted by jumpering the three negative-output resistors and making the measurements outlined in steps 1 and 2 below. V_g, V_n, V_1, and V_2 are in millivolts. R_g and R_n are in ohms.

1. Ground the level amplifier input to produce analog ground at the output.

   a. Connect a 1M resistor from the output to -10 v. Measure ground offset voltage V_g between the amplifier output terminal and analog ground.

   b. Repeat a, using a 3K resistor from output to -10 v and measuring the voltage V_1 between output and ground.

   c. Calculate ground output resistance R_g as

$$R_g = 0.3\ (V_1 - V_g).$$

2. Connect the level amplifier input to -3 vdc, producing the -10 v reference level at the output.

   a. Connect a 1M resistor from the amplifier output to ground and measure negative voltage V_n between the output and -10 v reference.

   b. Repeat with a 3K resistor from output to ground, measuring voltage V_2 between output and reference.

   c. Calculate R_n, the resistance for negative output, as

$$R_n = 0.3\ (V_2 - V_n).$$

If the difference between R_n and R_g exceeds 0.5 ohms, add an appropriate amount to R_n by removing one or more jumpers. Then repeat steps 2b and 2c to recheck R_n. The V_n value obtained in the first measurement is valid in the recheck.

Level amplifier 4679 should have these output characteristics:

V_g	-3.2 to -9.7 mv
V_n	0.3 to 3.2 mv
R_g and R_n	3 to 9 ohms
$\lvert R_g - R_n \rvert$, maximum	0.5 ohms

Digital-to-Analog Converter 1574

This module contains 25 precision metal film resistors and 9 potentiometers. It operates as a voltage divider (ladder) network to convert the digital output of a flip-flop buffer to an analog signal. The Type 1574 is constructed of 0.5% metal film resistors; nine 5% potentiometers are included for adjustment of the eight most significant ladder bits and the bias input. Input impedance is 3000 ohms or greater; output impedance is 1000 ohms ±.35% when the bias terminal is not used.

The bottom of the schematic shows 14 inputs to the module. All inputs except W and Z must be returned to a voltage. (W functions as an input only when the ladder is operated as a bipolar network.) The 138 unit uses the ladder as a 12-bit unipolar converter with logic levels F to U. W and Z provide a means of calibrating the zero endpoint of the ladder; Z is connected directly to +10 volts, and W is connected to the same point through a large resistance (See Section 5, Adjustment and Calibration).

The combined series-parallel resistance to the right of any ladder node point, up to and including the junction at output E, is 1000 ohms (R10 not included). When the reference voltage is applied to a given input, the voltage contribution of that bit to the summing junction is equal to the sum of all lower order bit contributions plus the least significant bit. If the bits are numbered from 1 to 12 (left to right), then n^{th} bit will contribute $(1/2)^n$ of its input level to the output. For example, output due to an input of V volts at F is V/2; from input H, V/4; etc.

Potentiometers are included in the 1574 module for two reasons. First, they allow adjustment of the ladder for any variation in fixed resistor values. Second, they make it possible to compensate for any variation in level amplifier output impedance. No potentiometers are required by lesser weighted bits because their values are selected to compensate for amplifier output impedance, and offset is divided in each case by bit weight. However, changes in amplifier output impedance become significant at the higher order bits. For example, if total impedance at R11 changes by as little as 4 ohms, an error of almost a bit could appear at the ladder output.

Difference Amplifier 1572

This module contains a high gain difference amplifier with a matched, dual npn transistor differential input stage. The circuit provides outputs of 0 and -3 vdc for a minimum differential input signal of less than 1 millivolt (although common mode effects may shift the switching region within a 3 millivolt range). When the input voltage difference is less than this value, output voltages are a function of input. The input voltage range is from 0 to -10 volts. The more positive of the pair of inputs draws approximately 1.5 microamperes. The more negative input draws approximately 1.0 microampere.

The difference amplifier circuit comprises two symmetrical networks: Q3 left, Q1, Q5, Q7; and Q3 right, Q4, Q6, Q8. An adjustable current sync, Q2, maintains a selected constant current through the 1572 input circuitry.

Distribution of current flow through the input circuitry is dependent upon the magnitude and polarity of the differential voltage at N and P. If differential input voltages is zero (N and P at the same voltage), and the zero-set potentiometer R4 is correctly adjusted, the currents through each leg are equal. Consequently, equal voltages exist at the Q5 and Q6 bases. This voltage is proportional to the current flowing into the sync and is adjustable by common level potentiometer R1.

When the differential input exceeds a few tenths of a millivolt, the voltages at F and W are either ground or -3 vdc, depending on input polarity. For N more positive than P, W is ground; when P is more positive, F is ground.

Assume a differential input in excess of 5 millivolts with P more positive. Input stage collector current remains relatively constant with respect to current through Q1 and Q4, because the Q1 and Q4 base currents are small compared to current through R3 and R6. However, the Q4 base

is more negative than the Q1 base because of slightly increased conduction through Q3 right. Emitter follower Q4 couples this voltage decrement to the Q6 base; Q1 similarly couples the complementary voltage increment to Q5.

Conduction through Q6 now increases, pulling the Q5-Q6 common emitter junction negative by emitter follower action and driving Q5 even further toward cutoff. The negative-going transistion at the Q5 collector drives Q7 into saturation, resulting in ground level at F.

The rise at the Q6 collector turns off Q8; its collector voltage thus falls to -3 volts (determined by the D11 clamp). D9 similarly clamps the Q7 collector when input polarity is reversed. Nominal current flow into each Q3 collector is 100 to 200 microamperes. Since this transistor has a minimum β of 100, input current is approximately 1 to 2 microamperes. A test should be made if it is suspected that the input current exceeds this maximum value, since conversion accuracy can be directly affected. The 1572 module meets this specification as originally supplied; however, conditions of shock or aging may cause input current to increase.

To measure input current, apply ground and -10 vdc to the amplifier input terminals. With a microammeter, measure the input current at each terminal. Then repeat with reversed dc input polarity. As an alternative to the use of a microammeter, reasonably accurate current measurements may be made using a dc millivoltmeter to measure the drop across a 10K resistor inserted in series with each amplifier input. A 10 millivolt drop is equivalent to 1 microampere.

Typical common mode rejection of the 1572 is 3 millivolts equivalent input offset for 10 volts common mode signal change at the input (approximately 70 decibles) and at $\pm 20°C$ temperature change. An amplifier that has drifted far outside this ratio for any reason impairs the accuracy of the comparison.

The common mode rejection test is done with a setup similar to that for the balance adjustment (Section 5). It should be performed at a low audio input frequency. Using a 3 millivolt peak-to-peak sinusoidal input, vary the bias from 0 to -10 volts, and observe the output waveforms on a scope. Although the rectangular waves become asymmetrical away from the -5 volt bias level, they should continue to switch in sync with the input as the bias is varied. There may be additional switchings caused by noise on the low amplitude input; however, if the major switching points are in sync, the amplifier meets the common mode rejection specifications.

Reference Supply 1704

This module is a -10 vdc, shunt regulated, reference voltage supply. It is used primarily as a precision voltage source in digital-to-analog and analog-to-digital applications. In the Type 138 unit, it supplies a reference voltage to the Type 4679 Level Amplifiers, which in turn drive the ladder network.

The Type 1704 output voltage is adjustable in a 3 millivolt range about -10 vdc. At this voltage, the maximum output current is 90 milliamperes for current flowing out of pin E, and 40 milliamperes for current flowing into E. The peak-to-peak ripple is less than 0.1 millivolt. For temperature variations between 15 and 35°C, output fluctuation is less than 1 millivolt. Output voltage change is less than 0.1 millivolt from 0 to full load. Input power is -15 volts at 250 milliamperes.

The 1704 output voltage at E is maintained at its preset value regardless of normal supply or load variations. Current through R21, connecting the -15 vdc supply with the output, is varied in response to these external changes to maintain E at the required voltage. The current through this resistor is determined by parallel control transistors Q5 and Q6, in response to signals from the error sensing circuitry. A reference Zener diode, D1, and three differential amplifier stages, Q1, Q2, and Q3-Q4, sense and amplify minute changes in the -10 volt output. This error signal drives the bases of Q5 and Q6, causing negative feedback in a direction which reduces the error signal at the sensing point.

D1, a stable Zener diode with a small temperature coefficient, is connected between pin T and the base of Q1 left, holding this point at precisely -6.2 vdc. Sense inputs T and Z are connected to ground and to the -10 volt bus. For best accuracy, these connections should be made at points close to the load, to eliminate errors due to IR drop in the lines between the supply and the point at which it is used. When the sense lines are remotely wired in this way, a 100 microfarad capacitor should be connected across them at the load.

Potentiometer R2 is adjusted during initial testing so that current through D1 conforms closely to the manufacturer's specification for optimum Zener current. This current can be monitored during calibration by observing the voltage across the 0.1% resistor R1 at Y and Z. This should be 3.175 volts.

The first two stages of the reference amplifier contain SDA-1 dual transistors, used here because of their low drift characteristics. When a load change or a fluctuation of the -15 volt supply appears across sense terminals T and Z, the change is reflected at the center tap of potentiometer R9 and therefore at the base of Q1 right. Since the base of Q1 left is held constant by D1, a difference voltage is generated at the Q1 collectors. This voltage is coupled directly to the Q2 bases; the further amplified difference voltage at the Q2 collectors is applied to the bases of Q3 and Q4. The output of the differential amplifier string is taken from the Q4 collector and passed through a relatively long time-constant integrator, C1, to slow the response time of the feedback amplifier and to prevent oscillation. The resulting signal drives the Q5 and Q6 bases, increasing or decreasing current flow to maintain the pin E voltage at its proper value.

For example, in the presence of an increased load, E attempts to go positive. The resulting positive voltage change at the base of Q1 right is inverted by Q1, again by Q2 and a third time by Q4, reducing the potential at the Q5 and Q6 bases. As the Q5-Q6 collector-emitter current is thus reduced, E is pulled negative by the -15 volt supply through R21 until the error voltages across the Q1 bases approach zero. If external load requirements are reduced, resulting in a negative transition at E, Q5 and Q6 are turned on harder by the process just described, pulling E positive.

Coarse and fine potentiometers R9 and R7, respectively, may be used to adjust the output voltage at E (or at the load) by varying that portion of the output which is fed back into the amplifier. The function of silicon diode D2 is similar to that of a battery; it allows Q5 and Q6 to be completely cut off if required for proper regulator function. Also, by permitting a reduced emitter resistance for Q5 and Q6, it increases regulator speed.

Test points N and M are used to check the operation of Q5 and Q6. Under normal operating conditions, the voltage at these points should be within 5% of each other; if either transistor fails to conduct, however, its emitter will be approximately 3/4 volt more positive than E.

SECTION 5

ADJUSTMENT AND CALIBRATION

Four analog-to-digital converter modules may require adjustment. Two of these, Reference Supply 1704 and Difference Amplifier 1572, should be checked regularly. The 1574 Ladder adjustments are set upon installation and should not need readjustment under normal circumstances. However, should there be any damage to the analog modules, or should the system be subjected to mechanical shock (which could jar pot settings) or extreme temperature changes, use the methods described in this section for recalibration. A fourth module, the 4301 Delay, may require readjustment if external control requirements change. All module locations are shown in Figure 5-1.

TEST EQUIPMENT

The following equipment is recommended for adjustment and calibration of the multiplexed A-D converter:

A single-frequency sine wave source, between 30 and 1000 cps. The output should be floating and the amplitude should be variable from 2 to 20 millivolts. The 110 volt, 60 cps line may be used directly for this source (suitably stepped down).

A source of 5 ±0.5 volts for biasing the output of the sine wave source.

A dual-trace oscilloscope having a vertical sensitivity of at least 5 mv/cm.

LADDER 1574

The Type 1574 module requires adjustment if it has been subjected to a drastic change in temperature, a mechanical shock sufficient to change trimpot settings, or after replacement or repair of associated 4679 Level Amplifiers. The level amplifier offset voltage should also be measured after replacement or repair (Section 4).

The 1574 Ladder has trimpot adjustments (R2 to R9) in the eight legs associated with input bits 0 to 7 (the R1-R10 leg is used only for adjustment purposes). The open-circuit analog voltage output from any one of these bits should be one LSB greater than the sum of all lesser

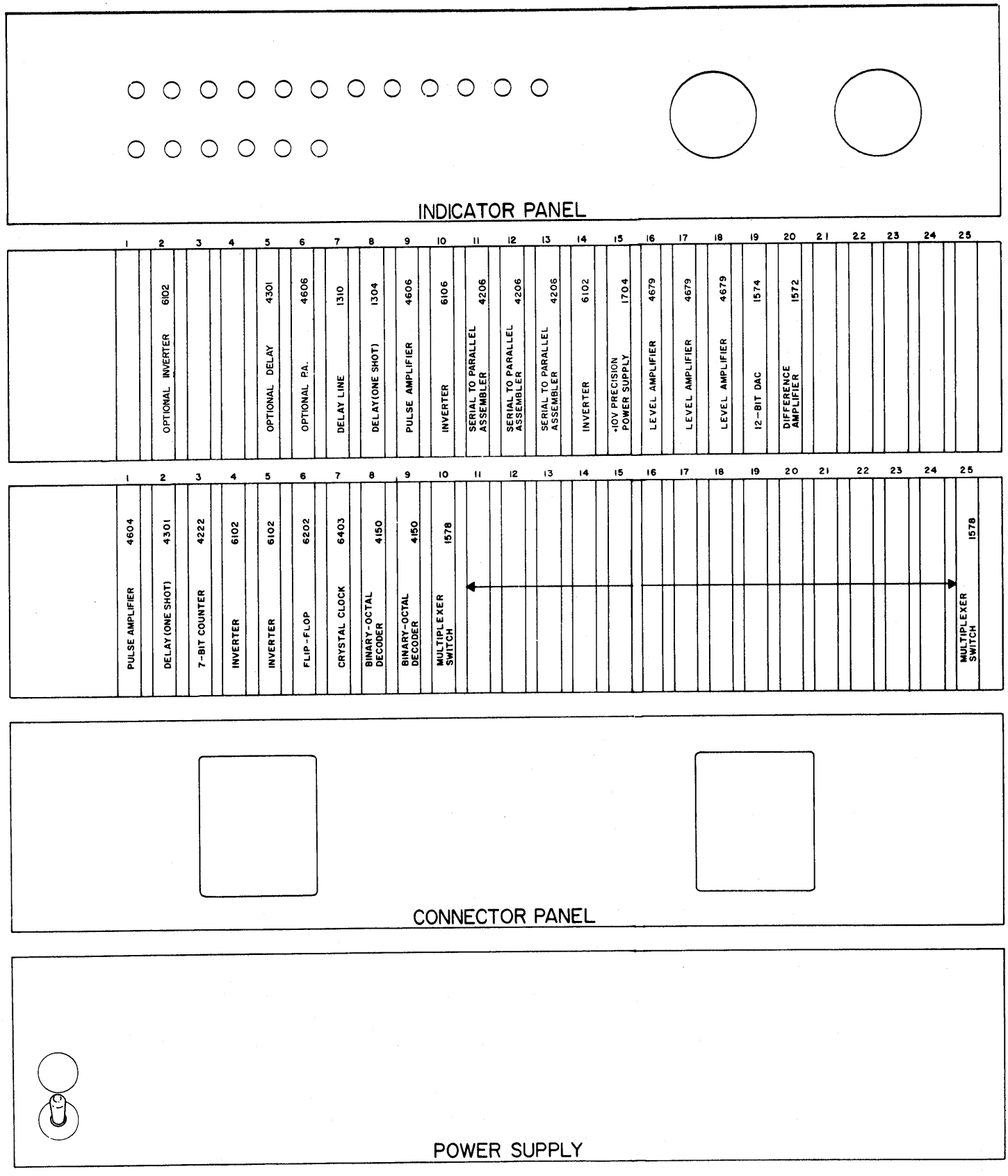


Figure 5-1 Equipment Layout and Module Location

bit contributions. The ladder is calibrated by adjusting each trimpot, starting with the least significant adjustable bit, to obtain the required voltage for each step. This LSB-MSB adjustment sequence obviates compensation for control interaction.

The procedure outlined below is valid for calibration on the bench. The program loop for testing a given bit alternates between a 1 in that bit with all zeros in lesser bits, and the complement. All greater bits are 0 for both states. Thus, the bit 7 test words are:

Pin	F-N	P	R-U
State 1	0	1	0
State 2	0	0	1

The bit 6 test is:

Pin	F-M	N	P-U
State 1	0	1	0
State 2	0	0	1

and so forth. As seen at the latter, the test words for bit 0 are:

Pin	F	H-U
State 1	1	0
State 2	0	1

An oscilloscope, ac-coupled to the ladder output at pin E and analog ground, shows a rectangular wave whose peak-to-peak amplitude corresponds to the increment of the bit under test. The scope vertical preamplifier should be set to a sensitivity of at least 5 mv/cm and calibrated with an external reference so the LSB value of 2.4 millivolts can be observed.

Since sensitivity of trimpot motion increases with bit significance, it is possible accidently to invert the relative values of the output when adjusting one of the greater bits. Synced to the ladder output, the scope would not show this. If such a mistake is noticed, it can be corrected by readjusting the pot for zero difference and then trimming in the direction of decreasing resistance. An unwitting inversion, however, results in -2 LSB error. To avoid this possibility, program the test numbers (or delay one) so the duration is different, making the display asymmetrical. Each polarity can then be associated with a particular width.

Since the ladder trimpots are wire wound, it is necessary to ensure that they are adjusted to a stable position, so that the slider arm is not resting on a single wire and able to jump away, possibly in the wrong direction. Therefore, after trimming, tap the pot once or twice noting the change in output, if any. If it is then required, retrim to another stable position closer to the ideal value.

End point calibrations may be made on the ladder in the following manner: calibrate the scope 0 vdc position and observe the ladder output at E with ladder inputs F to U at ground. This output may be zeroed by varying the resistor connected to ladder input W between 1 and 5 megohms (increase the value if the zero point is high, decrease it if low). The full scale point may be checked by returning ladder inputs F to U to the -10 volt reference and observing the ladder output at E. This point may then be adjusted to -10 volts with the fine voltage control of the 1704 reference supply.

Since the end point calibrations interact, it is difficult to align both perfectly while maintaining linearity. A somewhat more convenient method is to adjust the zero and half-full scale points for optimum fit, which permits closer control over the lower-weighted (and therefore more error sensitive) bits.

DIFFERENCE AMPLIFIER 1572

The 1572 Difference Amplifier has two adjustments which should be checked every three weeks: common level R1; and zero set R4. Proper settings are determined as follows:

1. Remove the module, apply power and connect the inputs of the dualtrace oscilloscope to the amplifier outputs at pins F and W, with scope ground at pin D. Using the ungrounded sine wave source, apply to inputs N and P at 10 millivolt, 30 to 1000 cps signal, biased to -5 volts.

2. With both scope traces synced to a single input, the amplifier outputs appear as two roughly complementary square waves. Adjust R1 for optimum symmetry of pin W output, then adjust R4 for optimum symmetry of the pin F output. To improve the resolution of this adjustment, repeat it with the audio input amplitude reduced to 5 millivolts. It may be necessary to repeat the adjustment sequence several times as the two controls are not independent.

Although the balance adjustment just described is the only one that need normally be performed on the 1572, two useful tests, input current drain and common-mode rejection, can be made if difficulty is suspected (see Section 4).

REFERENCE SUPPLY 1704

The 1704 Reference Supply has both a coarse and a fine output voltage adjustment. These two potentiometers determine the output voltage by regulating the amount of amplifier feedback. A single adjustment of R7, the fine potentiometer, is usually sufficient to correct the full scale point of the 1574 ladder. The coarse control, R9, is used for larger output voltage corrections.

The 1704 output should be checked weekly to ensure that the digital-to-analog reference voltage is correct. Allow the supply to warm up for a few minutes before starting this check.

DELAYS

The 4301 One-Shot Delay, located in the 139 unit, inhibits multiplexer operation from the application of the clear pulse to 1 microsecond after readin. This delay is usually preadjusted to conform with the customer's control requirements; however, if these requirements change at a later date, the 4301 delay interval may be adjusted as follows:

An approximation of the desired delay is obtained by connecting pin H to one of the four internal capacitors. If pin H is unconnected, the delay range is 2.5 to 25 microseconds. Connection of H to N, M, P, or R successively increases the delay by approximate factors of ten. By installing an additional external capacitor across L and K, the delay range may be further extended.

The 4301 Delay may be calibrated by applying a train of Digital Standard 0.4 microsecond negative Pulses to pin Y (or positive pulses to X) and observing the delay time at J with the scope. The pulse source may be used as the scope trigger.

The delay capacitors for the 1304 Delay and the Type 138 unit are selected with the SPEED-ACCURACY switch on the indicator panel. Fine adjustment of the two longest delay intervals (positions 5 and 6, Figure 3-1) is possible with a 25K trimpot, located on switch 2.

SECTION 6

PERTINENT DOCUMENTS

PUBLICATIONS

The following documents serve as source material and complement the information in this manual. These publications are available at the nearest Digital office or from:

Customer Relations Department
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts

a. Digital Modules Catalog, A-705. Thisbook contains information pertaining to the functions and specifications of the various modules and accessories comprising the 138-139 system.

b. Silicon Modules 6000 Series, C-6000, describes the specifications and functions of Digital's silicon system modules.

c. Analog <-> Digital Conversion Handbook, E-5100, gives comprehensive information on all phases of conversion.

d. PDP-1 Handbook, F-15D, gives programming information for the 138-139 when used with the PDP-1.

e. PDP-4 Handbook, F-45, gives basic IOT programming information.

f. PDP-5 Handbook, F-55, describes programming a converter with the PDP-5.

ENGINEERING DRAWINGS

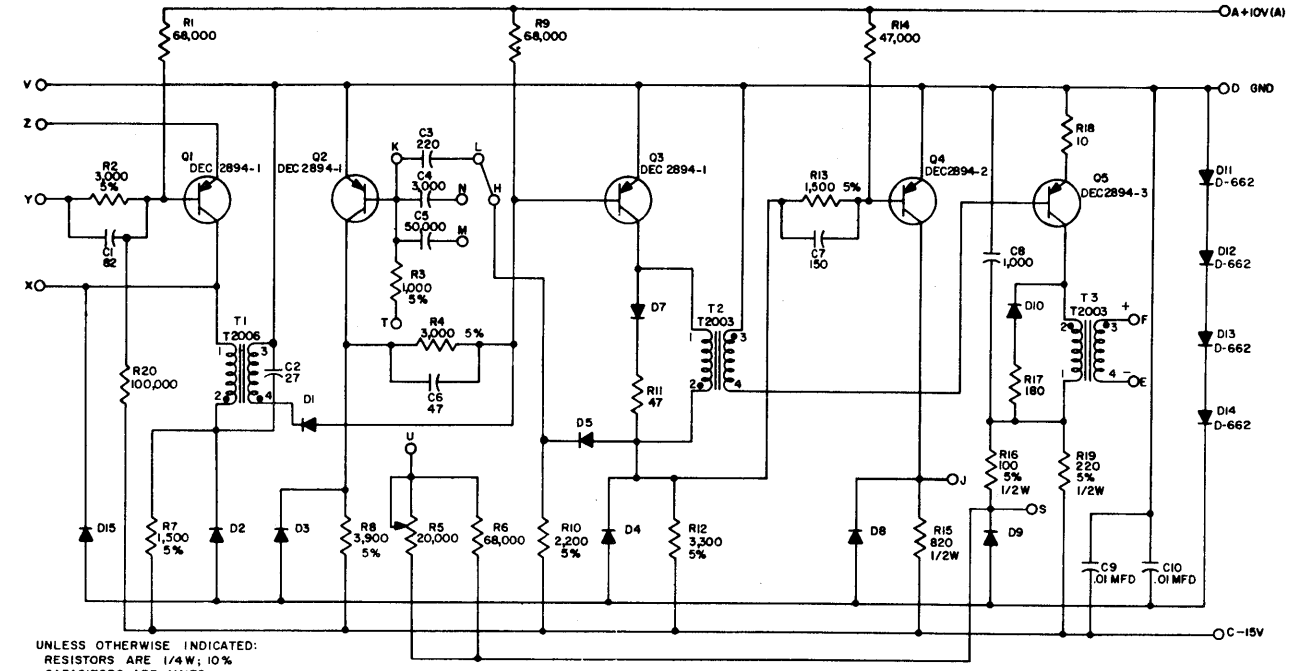
The engineering drawings in the following list are included in this manual as an aid to understanding and maintaining the 138-139 system. Where the book differs from the drawings supplied with the machine, the latter should be presumed correct.

Module Schematics

Delay	RS-1304
Delay Line	RS-1310
Difference Amplifier	RS-1572
12-Bit Digital to Analog Converter	RS-1574
Multiplexer Switch	RS-15780
-10V Precision Power Supply	RS-1704
Binary to Octal Decoder	RS-4150
7-Bit Counter with Readin Gates	RS-4222
Serial to Parallel Assembler	RS-4226
Delay	RS-4301
Pulse Amplifier	RS-4604
Pulse Amplifier	RS-4606
Level Amplifier	RS-4679
Inverter	RS-6102
Inverter	RS-6106
Flip-Flop	RS-6202
Crystal Clock	RS-6403

Logic Drawings

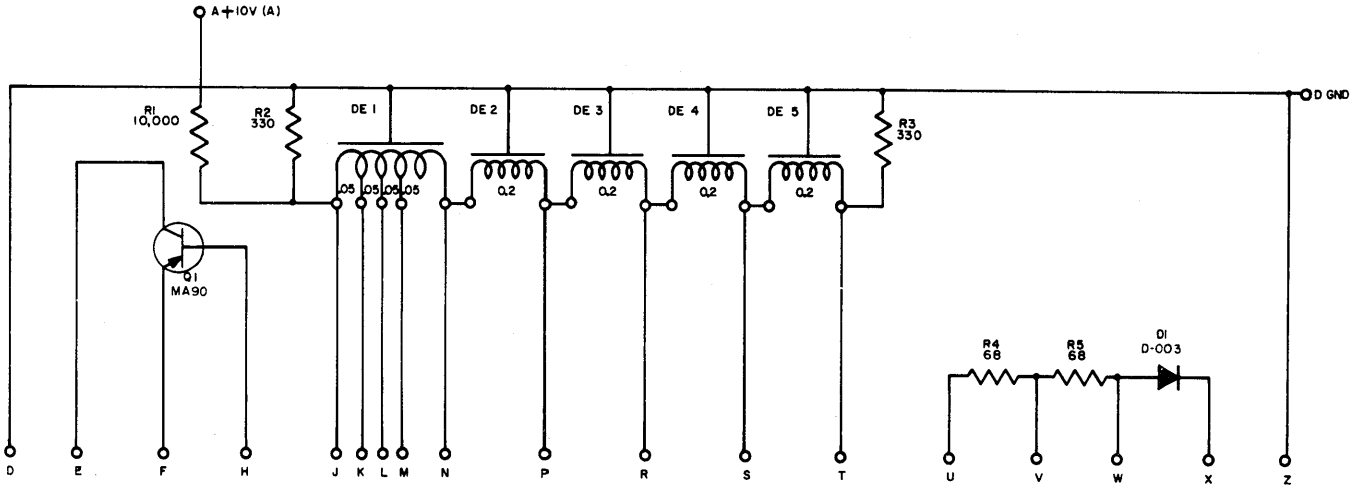
Analog-to-Digital General Purpose	BS-D-138-01
Analog Multiplexer	BS-D-139-01
Multiplexer Control	BS-D-139-02



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-1	DEC2894		
DEC2894-2	DEC2894		
DEC2894-3	DEC2894		
D-662	IN645		
D-664	IN914		

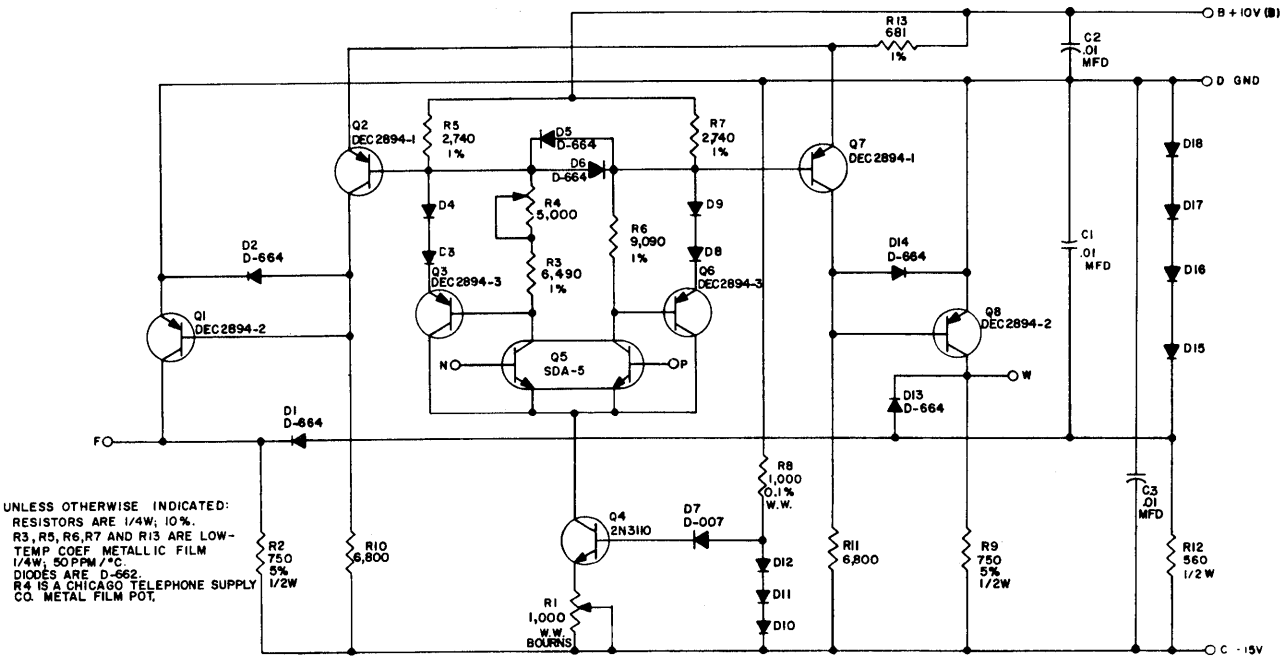
Delay RS-1304



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W; 10%
DE1= TECHNITROL 0.2 μ sec DELAY LINE 330 OHMS TAPPED AT 0.05 μ sec. INTERVAL
DE2= DE5 TECHNTROL 0.2 μ sec. DELAY LINE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MA90	2N2481		
D-003	IN994		

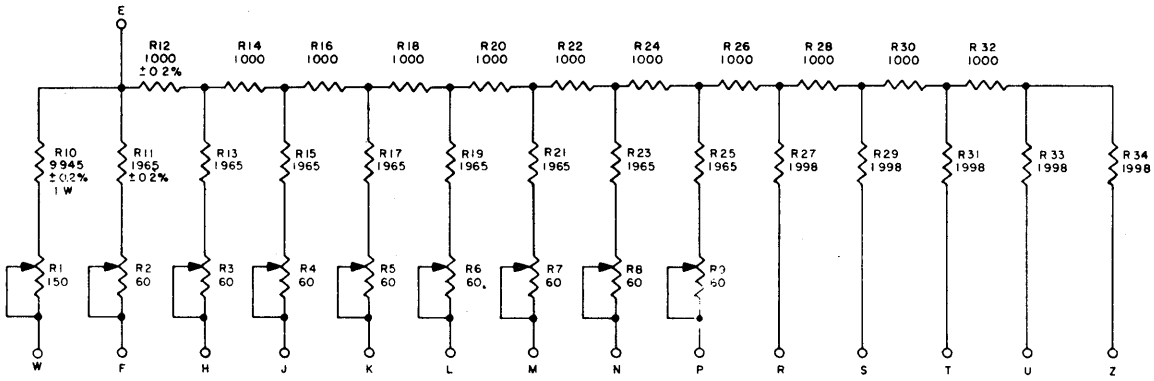
Delay Line RS-1310



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%.
R3, R5, R6, R7 AND R13 ARE LOW-TEMP COEF METALLIC FILM 1/4W, 50 PPM/°C.
DIODES ARE D-662.
R4 IS A CHICAGO TELEPHONE SUPPLY CO. METAL FILM POT.

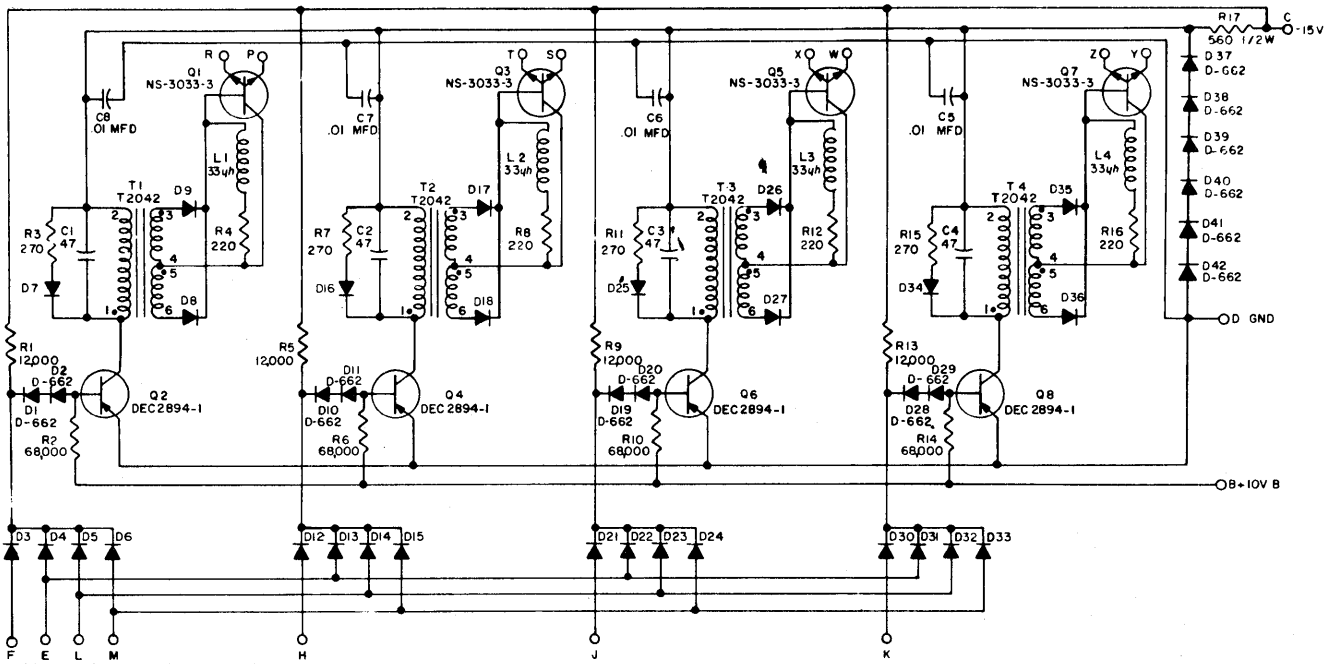
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-1	DEC2894	D-662	1N645
DEC2894-2	DEC2894	D-664	1N914
DEC2894-3	DEC2894	D-007	1N277
2N3110	2N3110		
SDA-5	2N2060		

Difference Amplifier RS-1572



UNLESS OTHERWISE INDICATED
RESISTORS ARE ACI METAL FILM 0.5%, 1/2W
R10 - R18 ± 10 ppm/°C
R19 - R22 ± 50 ppm/°C
R23 - R34 ± 150 ppm/°C
POTENTIOMETERS: DAYSTROM TYPE 510, ±5%, ±50 ppm/°C
R1: RESOLUTION OF .55%, MAX. END RESISTANCE OF 2Ω
R2 - R9: RESOLUTION OF .6%, MAX. END RESISTANCE OF 0.5Ω

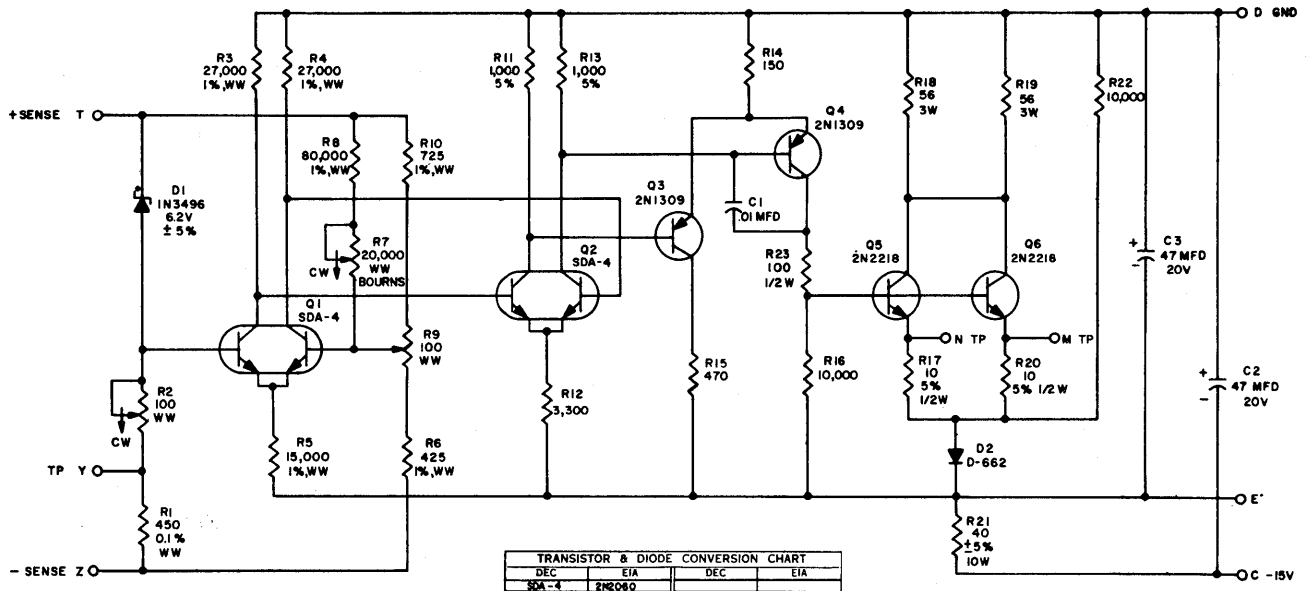
12-Bit Digital-to-Analog Converter RS-1574



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664
CAPACITORS ARE MMFD

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D-662	IN645		
DEC2894-1	DEC2894		
NS-3033-3	3N70		
D-664	IN914		

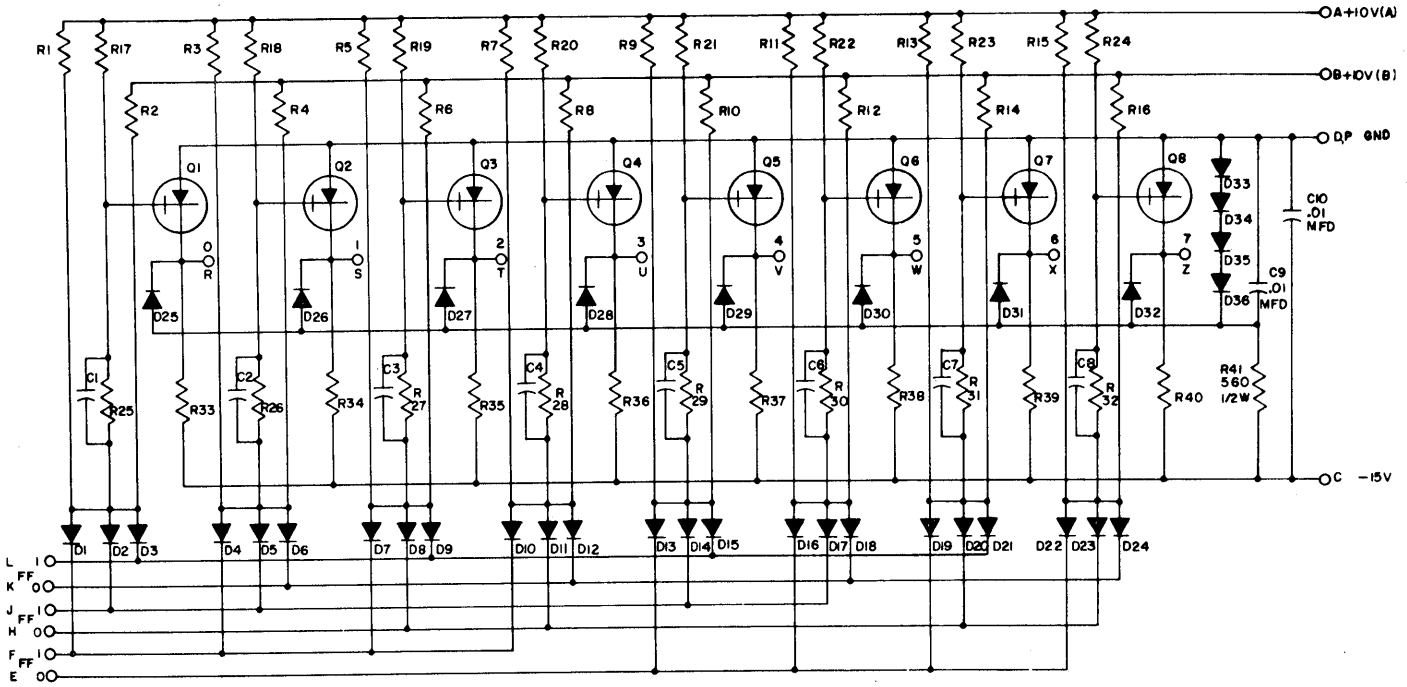
Multiplexer Switch RS-15780



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
SDA-4	2N2060		
2N1309	2N1309		
2N2218	2N2218		
D-662	IN645		
IN5498	IN3498		

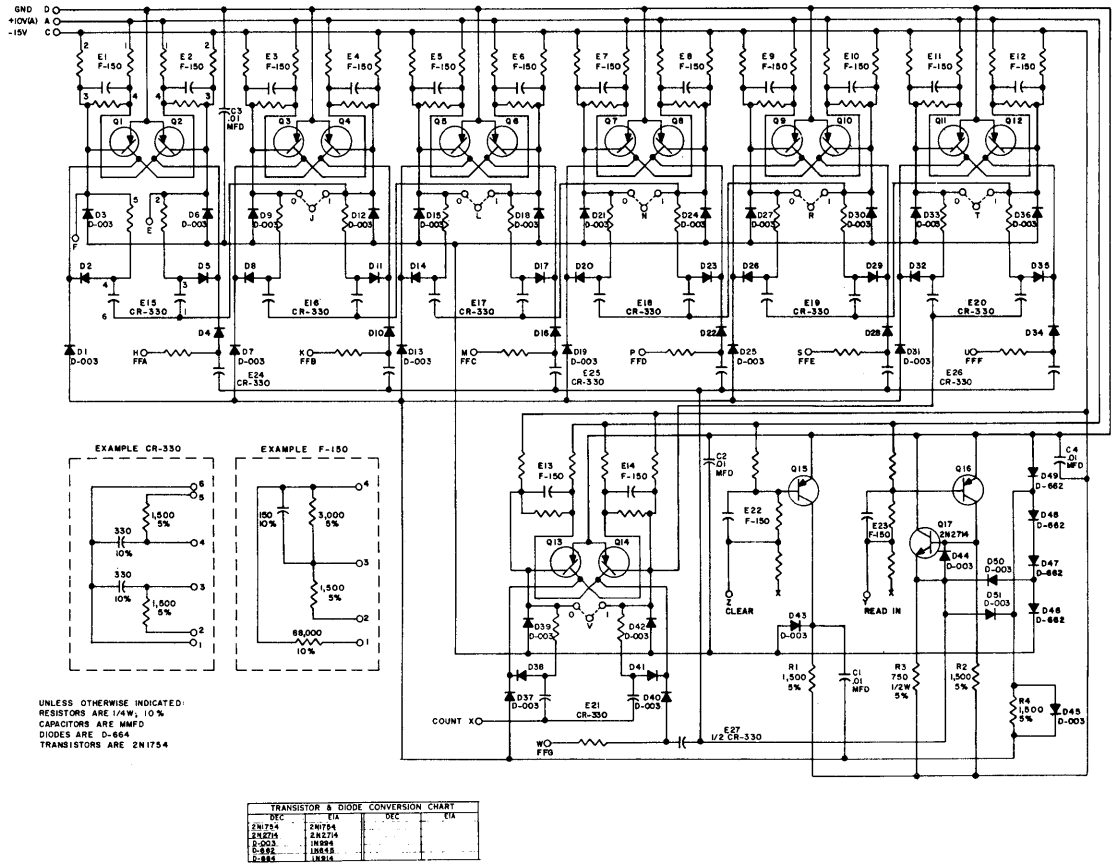
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
R10, R6 AND R1 ARE DAVEN 3 PPM TYPE 1195
R3, R4, R5 AND R8 ARE DAVEN 20 PPM TYPE 1283
R2, R9, ARE 50 PPM DAYSTRUM TRANSITRIM

-10v Precision Power Supply RS-1704



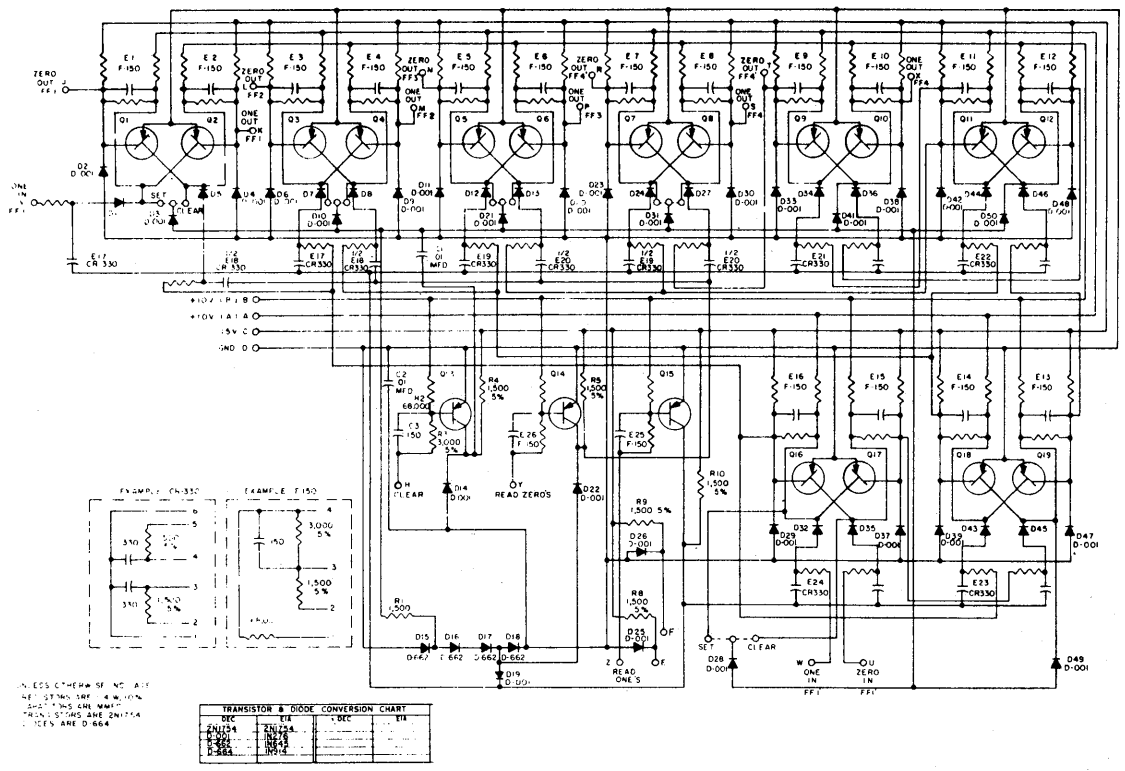
Q1-Q8 ARE 2N1305 : D1-D32 ARE IN276
D33-D36 ARE IN645 : R1-R16 ARE 27,000, 1/4W, 10%
R17-R24 ARE 56,000, 1/4W, 10% : R25-R32 ARE 2,200, 1/4W, 5 %
R33-R40 ARE 1,500, 1/4W, 5 % : C1-C8 ARE .001 MFD

Binary-to-Octal Decoder RS-4150

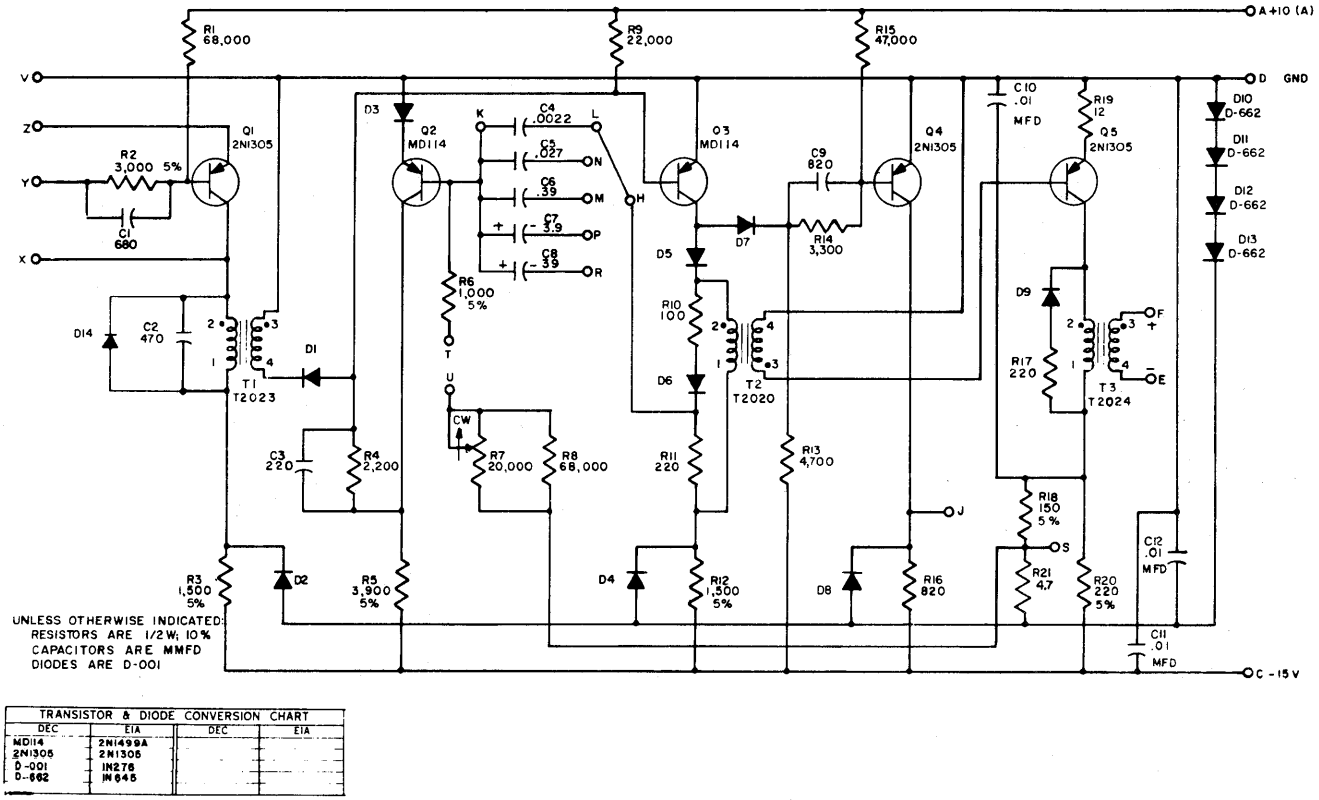


TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N1754	2N1754		
2N2714	2N2714		
D-003	IN998		
D-662	IN645		
D-664	IN914		

7-Bit Counter with Readin Gates RS-4222

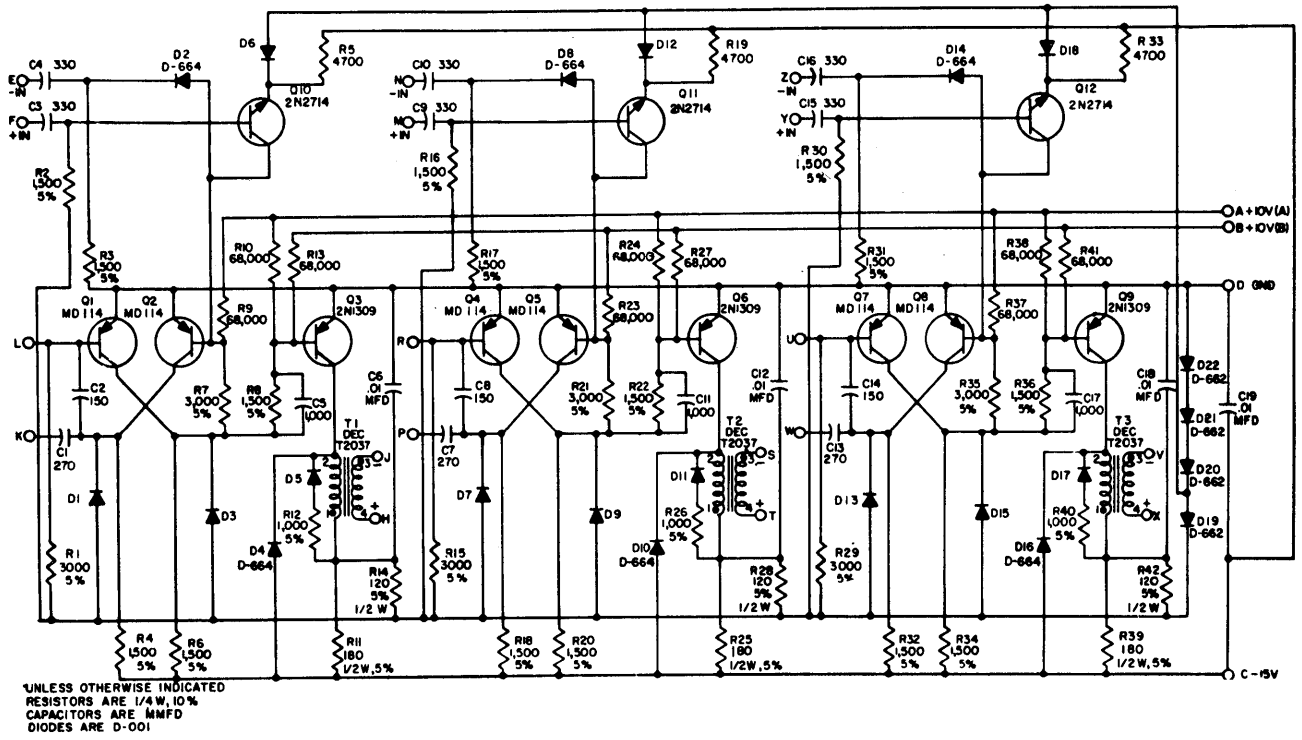


Serial-to-Parallel Assembler RS-4226



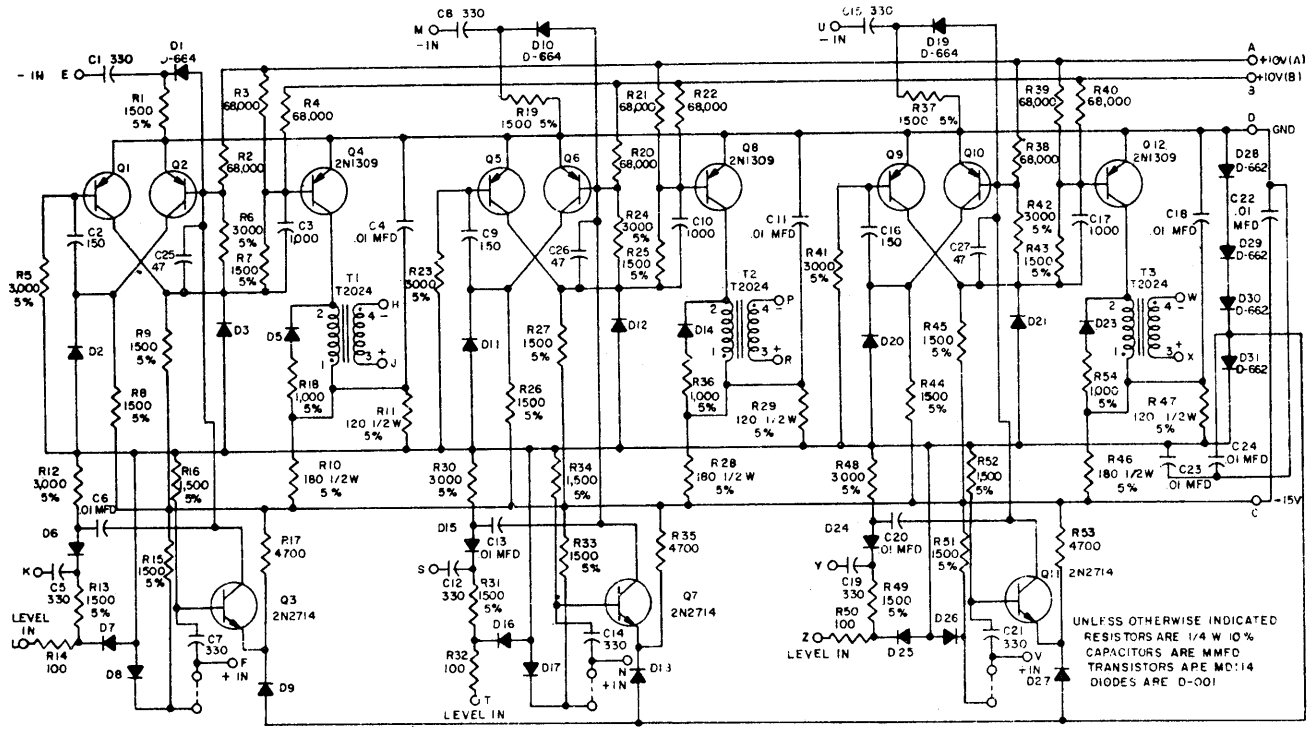
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N1499A		
2N1305	2N1305		
D-001	IN276		
D-662	IN645		

Delay RS-4301



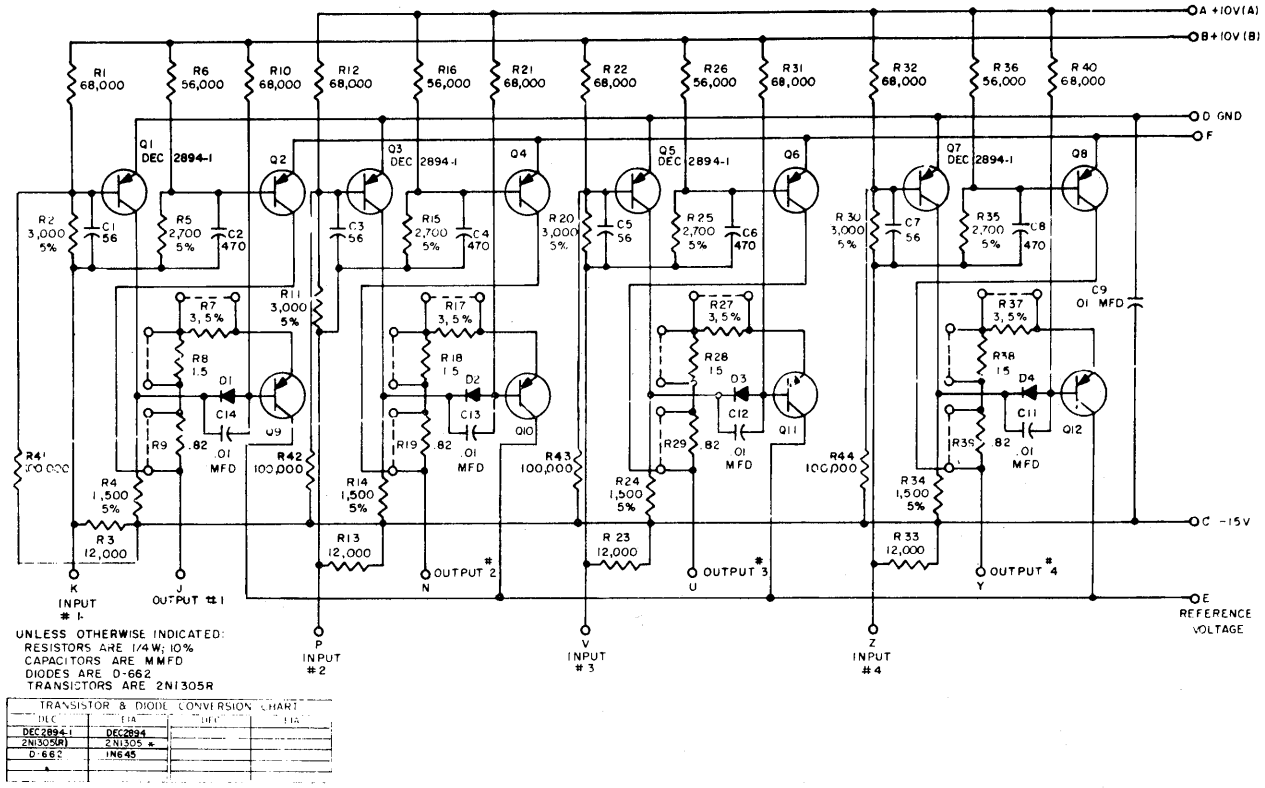
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N2714	2N2714	D-664	IN914
MD114	2N1699A		
2N1309	2N1309		
D-001	IN276		
D-662	IN645		

Pulse Amplifier RS-4604



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N699A	D-664	IN914
2N2714	2N2714		
2N1309	2N1309		
D-001	IN276		
D-662	IN645		

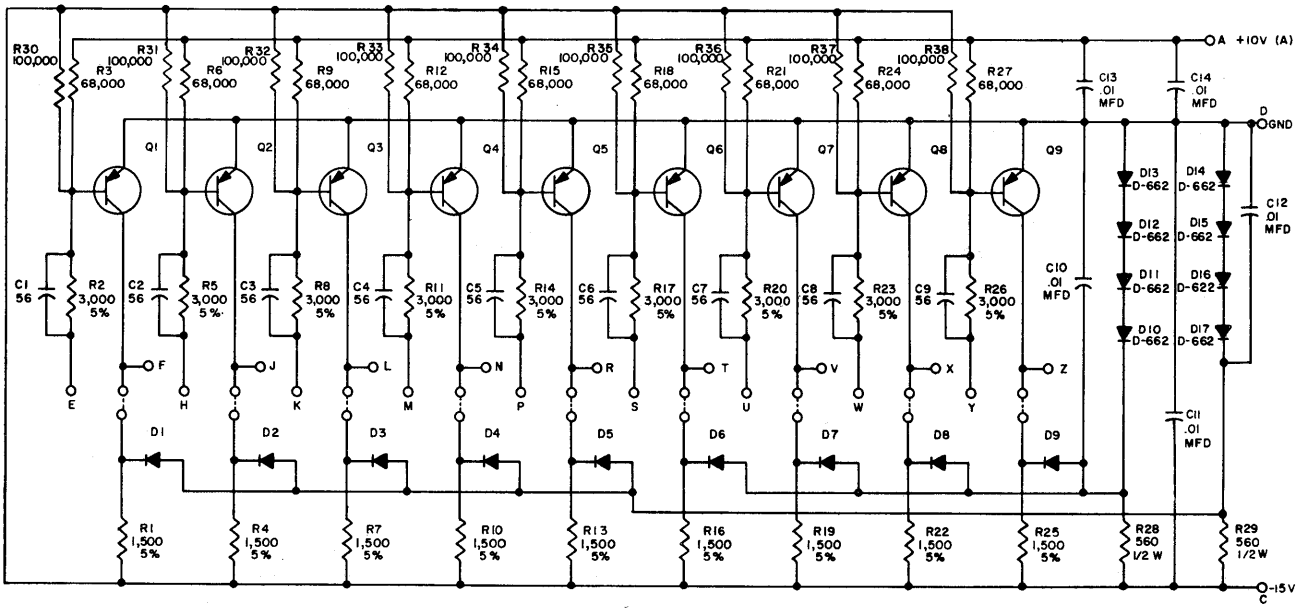
Pulse Amplifier RS-4606



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-662
TRANSISTORS ARE 2N1305R

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-I	DEC2894		
2N1305(R)	2N1305 *		
D-662	IN645		

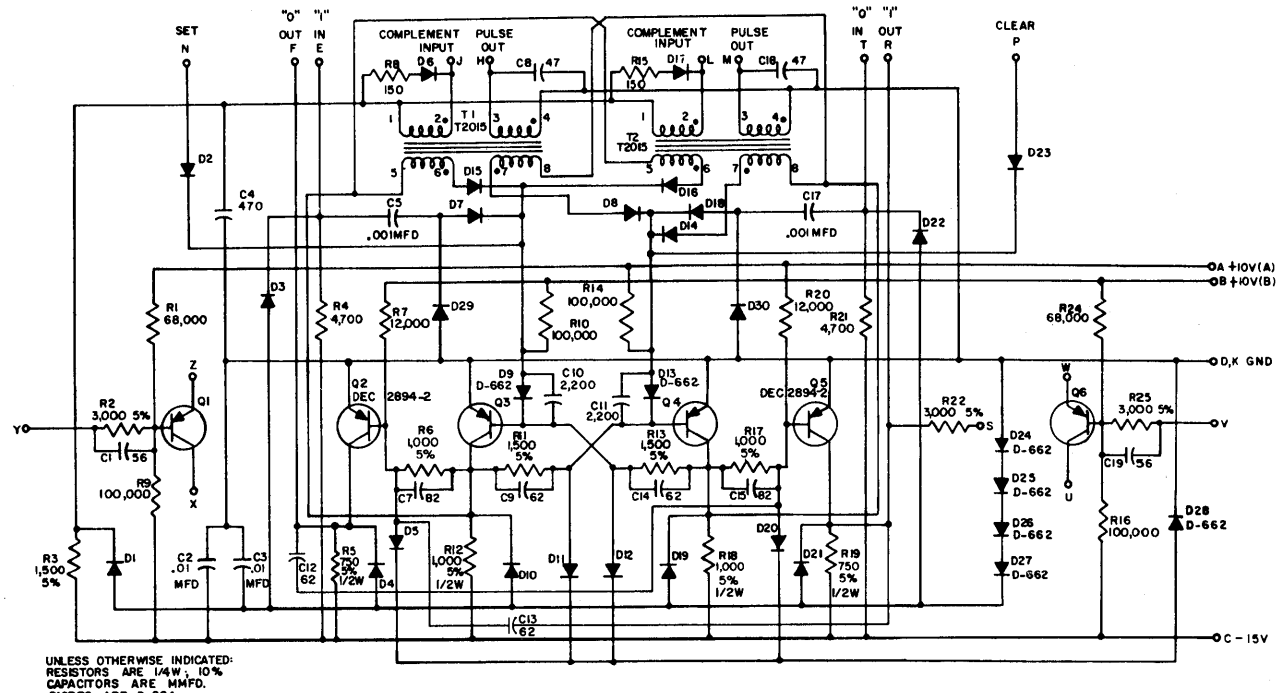
Level Amplifier RS-4679



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 2894-I
DIODES ARE D-664

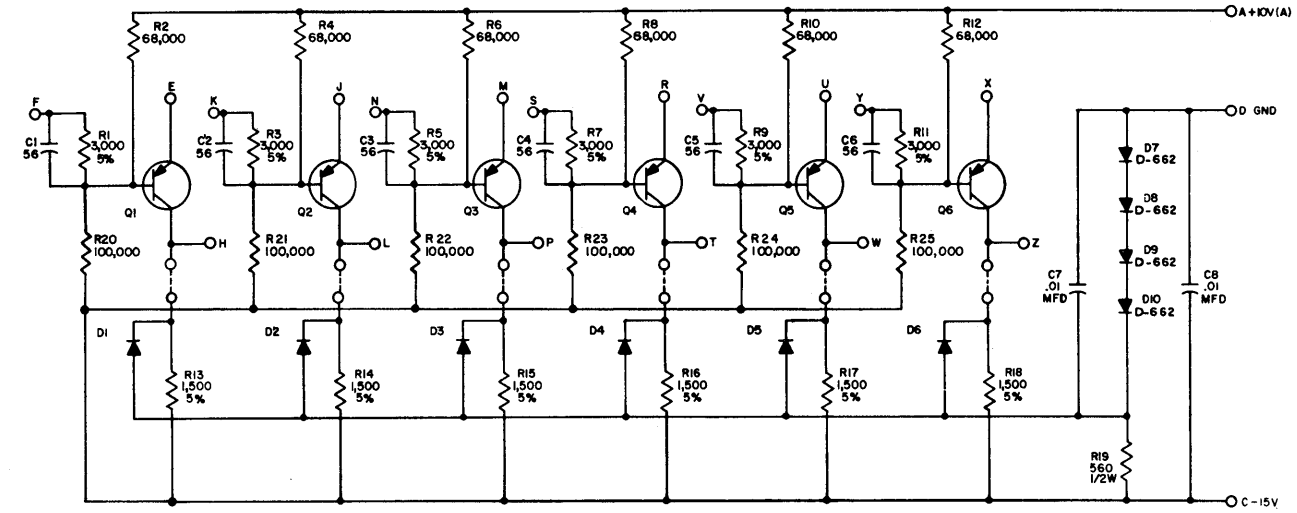
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-I	2N2894		
D-664	IN914		
D-662	IN645		

Inverter RS-6102



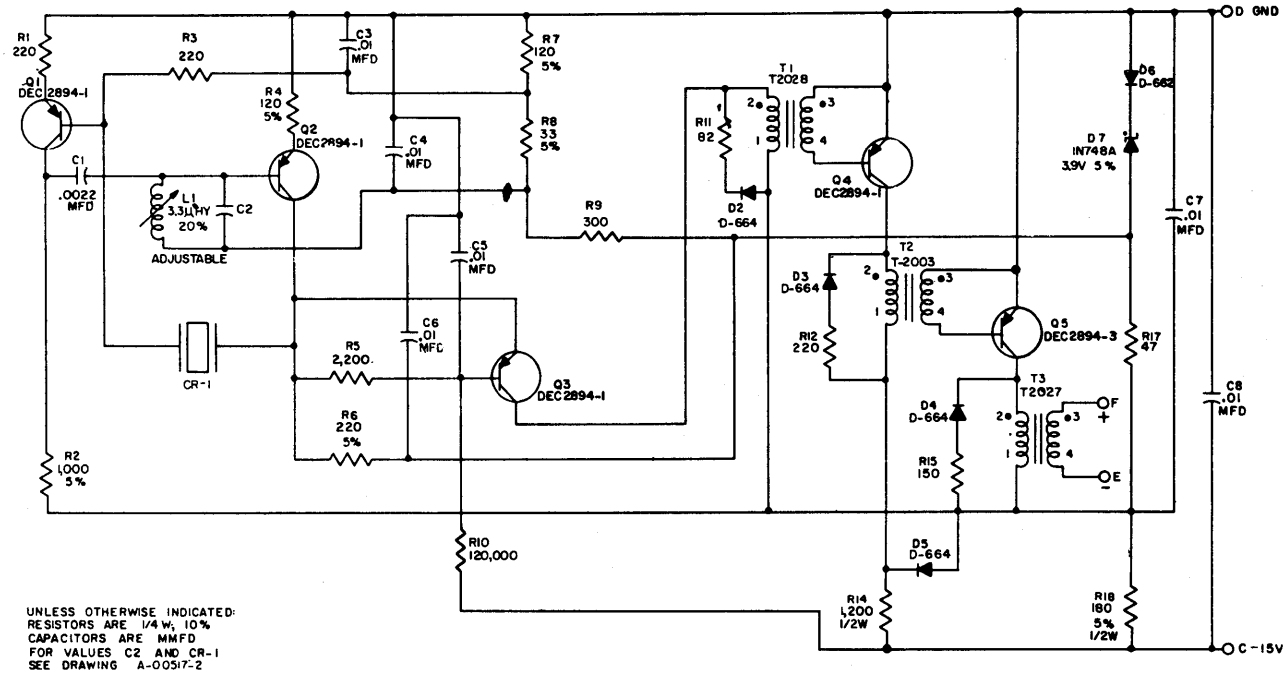
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-1	DEC 2894		
DEC 2894-2	DEC 2894		
D-664	IN914		
D-662	IN645		

Inverter RS-6106



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-1	2N2894		
D-664	IN914		
D-662	IN645		

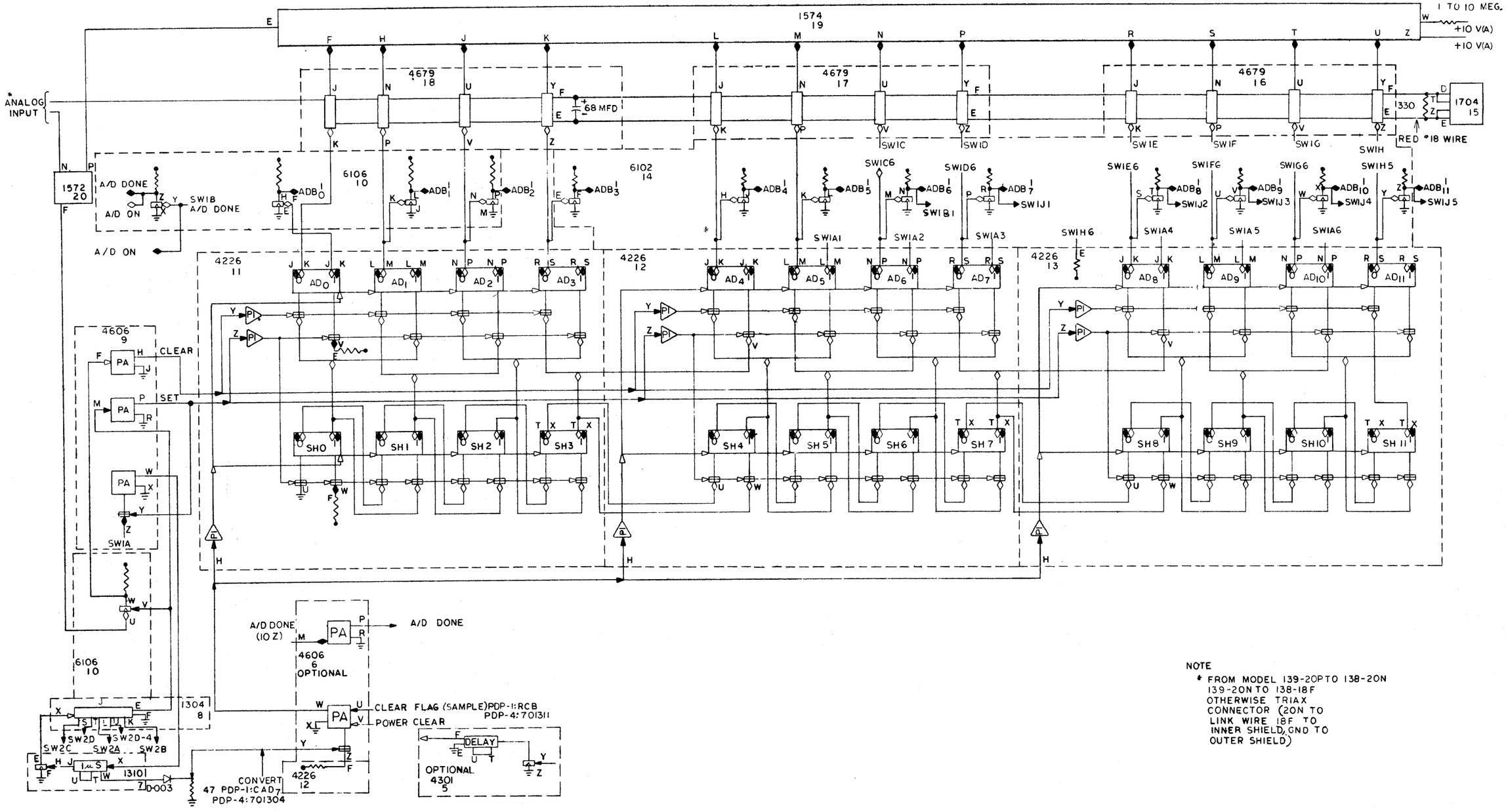
Flip-Flop RS-6202



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
FOR VALUES C2 AND CR-1
SEE DRAWING A-00517-2

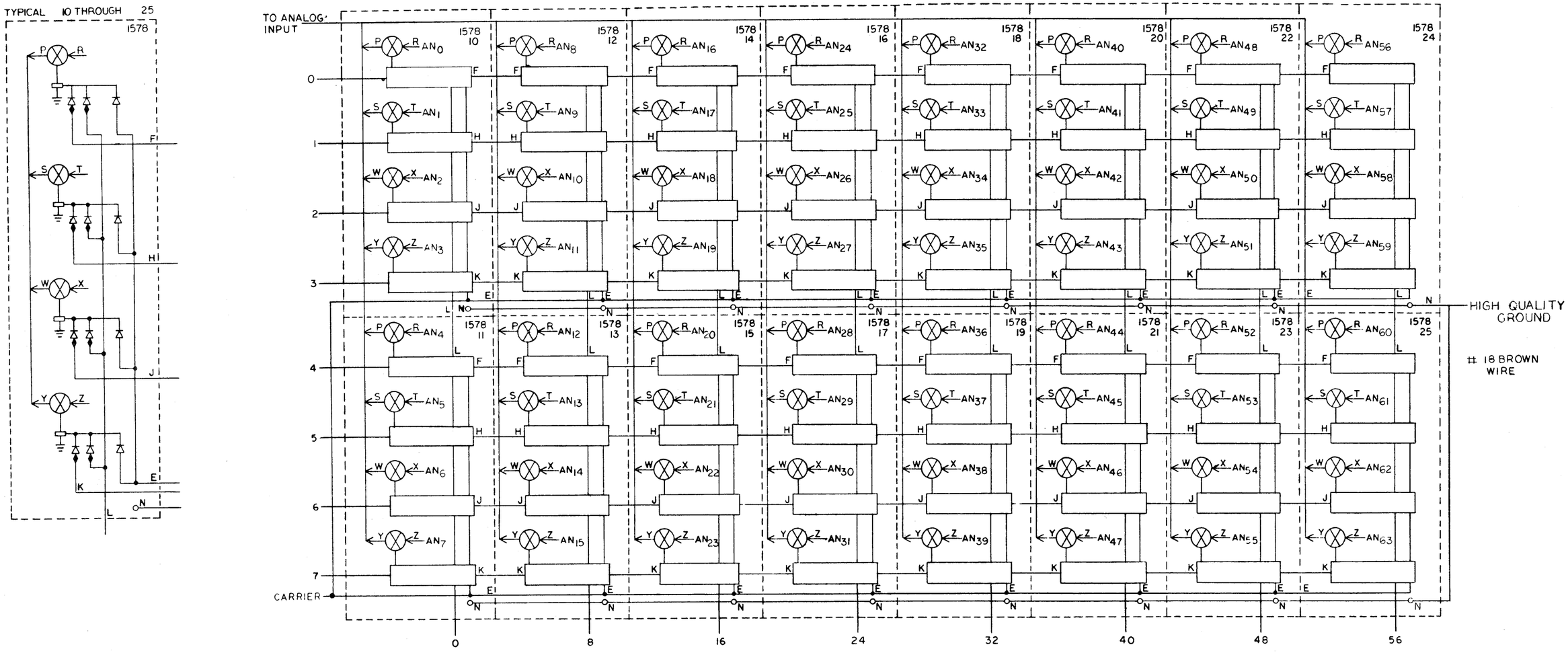
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-1	DEC2894		
DEC2894-3	DEC2894		
D-662	IN648		
D-664	IN914		
IN748A	IN748A		

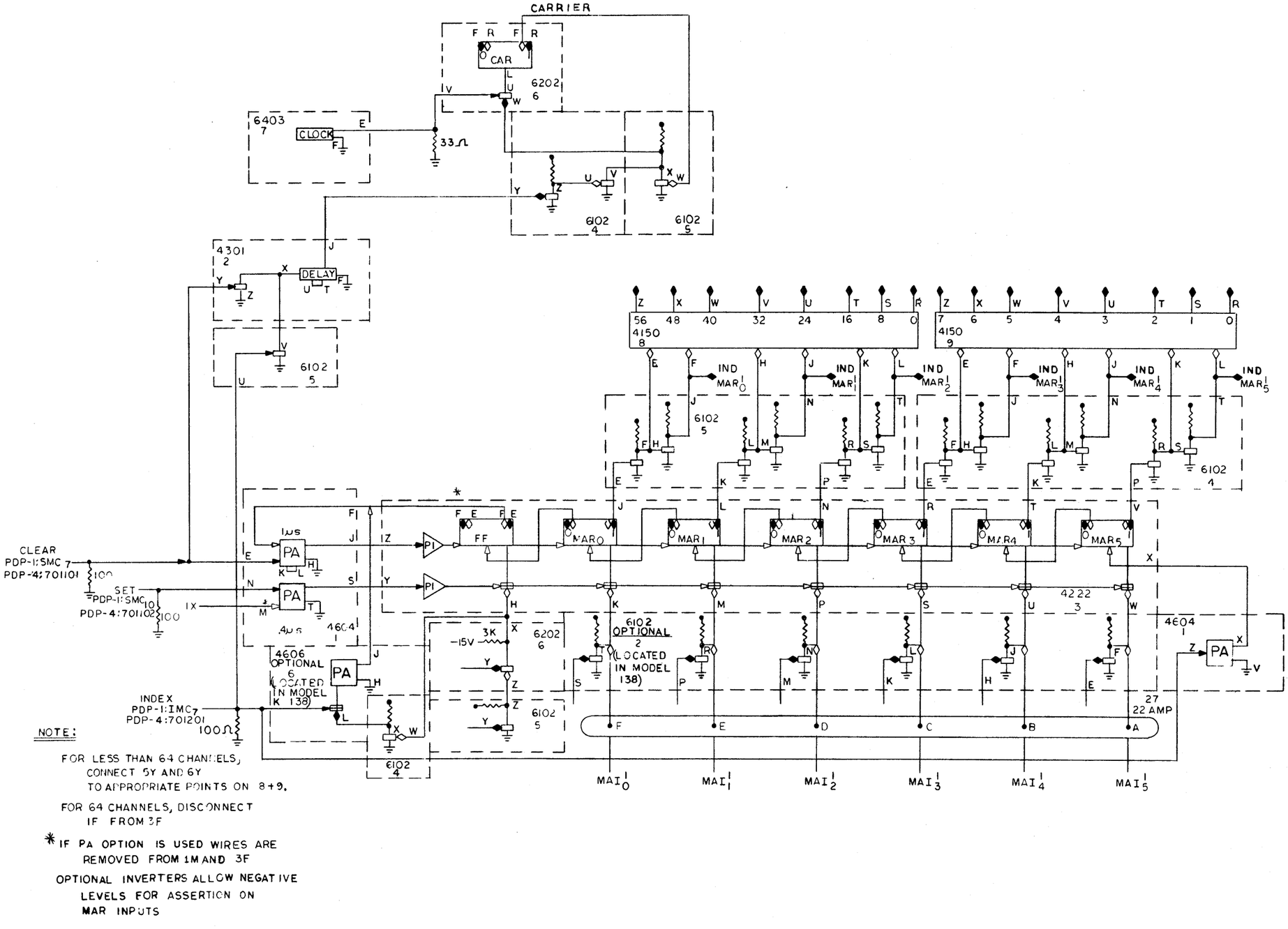
Crystal Clock RS-6403



NOTE

* FROM MODEL 139-20PTO 138-20N
139-20N TO 138-18F
OTHERWISE TRIAX
CONNECTOR (20N TO
LINK WIRE 18F TO
INNER SHIELD, GND TO
OUTER SHIELD)


TYPICAL 10 THROUGH 25
1578
TO ANALOG INPUT
HIGH QUALITY GROUND
18 BROWN WIRE
CARRIER
0
8
16
24
32
40
48
56



NOTE:

FOR LESS THAN 64 CHANNELS, CONNECT 5Y AND 6Y TO APPROPRIATE POINTS ON 8+9.

FOR 64 CHANNELS, DISCONNECT IF FROM 3F

* IF PA OPTION IS USED WIRES ARE REMOVED FROM 1M AND 3F

OPTIONAL INVERTERS ALLOW NEGATIVE LEVELS FOR ASSERTION ON MAR INPUTS

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