Digital Equipment Corporation
Maynard, Massachusetts

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DEC-8E-HR2B-D-KM8

KM8-E MEMORY EXTENSION and TIME-SHARE OPTION MANUAL

The information in this preliminary manual will become, in its final form, a part of the *PDP-8/E Maintenance Manual, Volume 2.*

PRELIMINARY

1st Preliminary Edition November 1971

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SECTION 1 INTRODUCTION

1.0 MEMORY EXTENSION AND TIME SHARE GENERAL DESCRIPTION

The KM8-E option generates a three-bit address for the extended memory address lines allowing the use of more than 4K memory and when required is used as a prerequisite in a time sharing system.

All logic is contained on one QUAD size module designated M837 which plugs directly into the OMNIBUS. All signals entering and leaving the module are via the OMNIBUS.

1.1 MEMORY EXTENSION GENERAL DESCRIPTION

The Memory Extension hardware is a requirement whenever more than 4K of memory is to be addressed. Except for Data Break devices, the Memory Extension is the only means by which extended memory addresses can be applied to the three extended memory address lines called EMA 0-2. Memory is divided into 4K fields starting with field 0 for the basic 4K memory up to field 7 when up to 32K memory is employed. Each 4K memory receives and decodes the EMA signals. This provides the addressing capability of up to 32,768 memory locations. There are two types of fields - the Instruction Field (which acts as an extension to the PC and direct argument addresses) and the Data Field (which augments the address of indirectly obtained arguments). When the programmer desires to use one field for instructions and a different field for data, he directs the corresponding field address to either the Instruction Field Register or the Data Field Register contained on the KM8-E option. The field addresses are applied to the EMA lines by specific instructions and conditional logic. Safeguards are provided so that during unplanned events such as interrupts and data breaks, no field addresses are lost. Program instructions allow any field address to be stored. This is significantly important to the programmer desiring to nest interrupts on time-share.

1.1.1 The Memory Extension

A simplified block diagram showing the basic transfer paths dealing with memory addressing and field addressing is shown in Figure 1. The KM8-E is the only route by which fields above field 0 may be selected. The only exception to this is the data break device which has the capability of selecting its own memory field. The programmer has two methods by which memory fields may be selected. One method is via the Console Switch Register and the second method is via an IOT instruction. In either event, the field information is loaded into the appropriate register in the extension control. The extension control automatically responds to the appropriate instructions and major states by placing the contents of the correct field register onto the EMA lines.

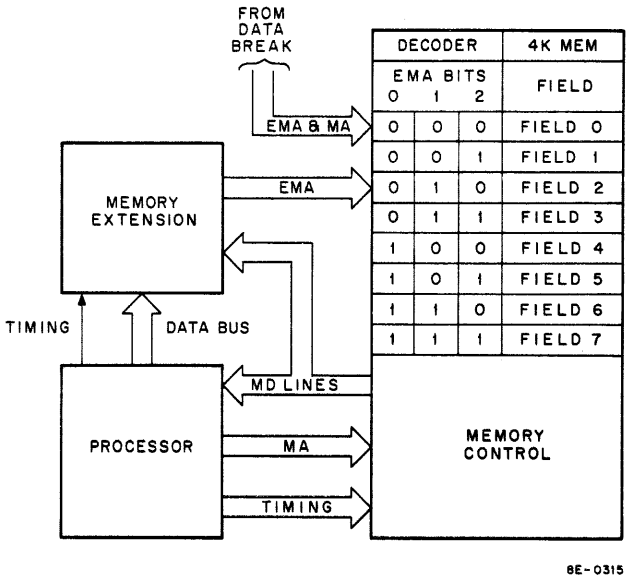

Figure 1 Memory Extension Simplified Block Diagram

1.2 TIME-SHARE GENERAL DESCRIPTION

The Time Share portion of the KM8-E is used only when a Time Sharing system is to be employed. The KM8-E module contains a jumper in the Inhibit Logic which prevents the operation of the time share function. Therefore, unless this jumper is to be removed from the module, the reader need not be concerned with the time share description in this manual.

The KM8-E Memory Extension and Time Share option provides the necessary additional hardware for a general purpose time sharing system. This option, coupled with a time sharing program, such as TSE, and 8K or more of core, allows up to 24 users to independently run programs such that the appearance is created that each user has the computer to himself.

As a system, the user can be considered operating in one of three levels: a) not logged-in level, b) monitor level, and c) user level. A typical system is illustrated in Figure 2. The user interface to the system is the KL8-E Teleprinter Control. The monitor program performs a dominant role in controlling the operation between the processor and the KM8-E option and between the users and the processor.

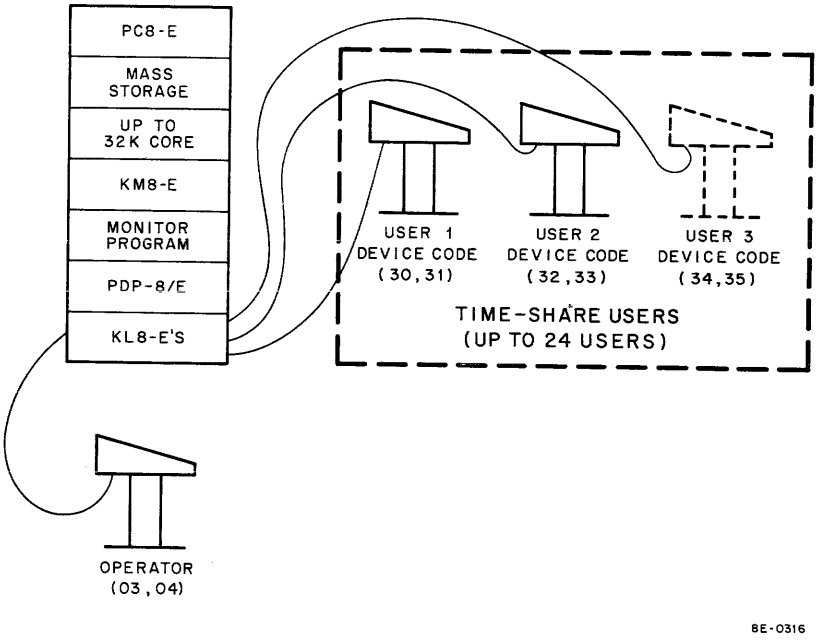

Figure 2 Typical Time-Share System

Monitor is a complex of subprograms used to coordinate the operations of various programs and user consoles. Monitor allocates the time and services of the computer to various users; it grants a slice of processing (computing) time to each job, and schedules jobs in sequential order to make the most use out of the mass storage device. Monitor handles user requests for hardware operations (reader, punch etc.), swaps (moves) programs between memory and mass storage, and manages the user's private files. Thus, the primary time sharing capability is provided by the system monitor and the PDP-8/E processor. However, certain additional hardware not provided by the PDP-8/E processor is required to accommodate the special requirements of time sharing and extended addressing capability.

For more information on the monitor and user programming, refer to Chapter 10 of Introduction to Programming - Digital Equipment Corporation.

1.3 EXTENDED MEMORY AND TIME-SHARE SUMMARY

As a memory extension control, the KM8-E provides:

a. the hardware to allow the programmable selection of the extended memory field (fields 1 through 7); allowing the extended addressing capability of the processor from a basic system of 4096 addresses to an extended memory system up to 32,768 addresses,

b. the hardware to prevent an interrupt or data break from interferring with the extended addressing scheme,

c. the hardware to save and restore a field return address.

As a time-share control, the KM8-E provides:

a. the hardware to distinguish between user and monitor modes,

b. the hardware to trap certain instructions, causing an interrupt and placing the time-share system in monitor mode,

c. the ability to establish user mode.

1.4 SOFTWARE

The following programs are used in the operation of time sharing and memory extension operations:

a. System Programs

1. TSE Time-Sharing Monitor (DEC-T8-MRFB)

TSE (Time Sharing System for the PDP-8/E computer) is a general purpose, stand-alone, time-sharing system. TSE offers each of up to 24 users a comprehensive library of programs that provide facilities for compiling, assembling, editing, loading, saving, calling, debugging, and running user programs on-line.

b. Diagnostic Programs

1. Extended Memory Address Test (MAINDEC-8E-D1FA)

This program tests all of memory (up to 32K) not occupied by the program to verify that each location can be uniquely addressed.

2. Extended Memory Checkerboard (MAINDEC-8E-D1BA)

This diagnostic program is designed to provide worst-case half-select noise conditions in order to determine the operational status of core memory. The patterns generate worst-case noise conditions in all used fields of a PDP-8/E equipped with at least 8K of core memory.

3. Extended Memory Control and Time Share Test (MAINDEC-8E-D1HA)

This program tests the Extended Memory Control and Time Share Option logic for proper operation. The program exercises and tests the control IOT's Time-Share instruction trapping, the ability to address all field, program interrupt, and auto-index.

1.5 COMPANION DOCUMENTS

The following documents and publications are necessary in the operation, installation, and maintenance of this option:

a. DEC PDP-8/E & PDP-8/M Small Computer Handbook - 1972

b. PDP-8/E Maintenance Manual - Volume 1

c. DEC Introduction to Programming

d. DEC Engineering drawing, Memory Extension and Time Share option, number KM8-E

e. Extended Memory Address Test, MAINDEC-8E-D1FA-D

f. Extended Memory Control and Time Share Test, MAINDEC-8E-D2HA-D

SECTION 2 INSTALLATION AND CHECKOUT

2.0 GENERAL REQUIREMENTS

The KM8-E Memory Extension and Time Share Option is installed by on-site DEC Field Service Personnel. No attempt should be made by customers to unpack, inspect, install, checkout, or service the equipment.

2.1 INSTALLATION

Perform the following procedures to install the KM8-E option:

1. Remove the module from the shipping container,
2. Inspect the module for any apparent damage,
3. Connect the module to a convenient OMNIBUS slot.

2.2 CHECKOUT

Perform the following procedures to checkout the KM8-E option:

1. Verify that the extended memory modules have been installed,
2. Verify that the corresponding jumpers have been installed to reflect the appropriate memory fields,
3. Perform acceptance tests provided in Paragraph 2.3, Chapter 2 of Volume 1,
4. Load MAINDEC-8E-D1FA Extended Memory Address Test. This program tests all of memory (up to 32K) not occupied by the program to verify that each location can be uniquely addressed.
5. Load MAINDEC-8E-D1BA. This diagnostic program provides worst-case half-select noise conditions and verifies the operational status of core memory.
6. Load MAINDEC-8E-D1HA Extended Memory Control and Time Share Test. This program tests the Extended Memory Control and Time-Share option logic for proper operation. The program exercises and tests the control IOT's, Time-Share instruction trapping, (if time-share is implemented) the ability to address all fields, program interrupt, and auto-index.
7. Make proper entry on user's log that the acceptance test for the KM8-E option was performed satisfactorily.

SECTION 3 SYSTEM DESCRIPTION

3.0 INTRODUCTION

The system description of the Memory Extension and Time Share option is given in terms of the functional operation. From the functional point of view, instructions which make either the Memory Extension or Time Share portion do something must be considered as well as the philosophy of why the events happen as they do. The system description is therefore, a composite treatment of the hardware, represented in block diagram form, and of the flow of events, represented in flow diagram form. The events as they happen in the Memory Extension and Time Share option are fully considered and the events within the processor are only partially considered. Such areas as Major Register gating and how the processor functions are completely described in Volume 1 of this Maintenance Manual.

3.1 BLOCK DIAGRAM DESCRIPTION

A block diagram representing all of the functional elements of the Memory extension and Time Share option is illustrated in Figure 3. The logic can be considered divided into three groups - the control (located on the left portion of the illustration), the Instruction Field Registers (located in the center of the illustration) and the Data Field Registers (located in the far right of the illustration). The only interface is the OMNIBUS. Therefore, all signals entering and leaving the block diagram are directed from and to the OMNIBUS. Data paths between the Memory Extension and Time Share option and the processor is via the DATA BUS. Data is directed to the console status indicators via the DATA BUS during TS1 for the purpose of informing the operator of which instruction and data fields have been addressed. When the Data Field and/or the Instruction Field are to be stored in memory, the data path is the DATA BUS to the AC register. A DCA instruction is then used to store the information in memory. The data paths between the processor and the Memory Extension and Time Share option is via the DATA BUS or the MD lines.

Special inhibiting features are designed into this option. For example, during a data break operation where some peripheral such as a disk is being operated, control lines such as CPMA Disable prevent the transmission of data to the EMA lines. For the case of Programmed Interrupt, the logic provides the means of holding back an interrupt until a CIF, RMF, or RTF instruction has been completely processed.

Another design feature is trap logic that signals monitor whenever certain instructions are used by the user.

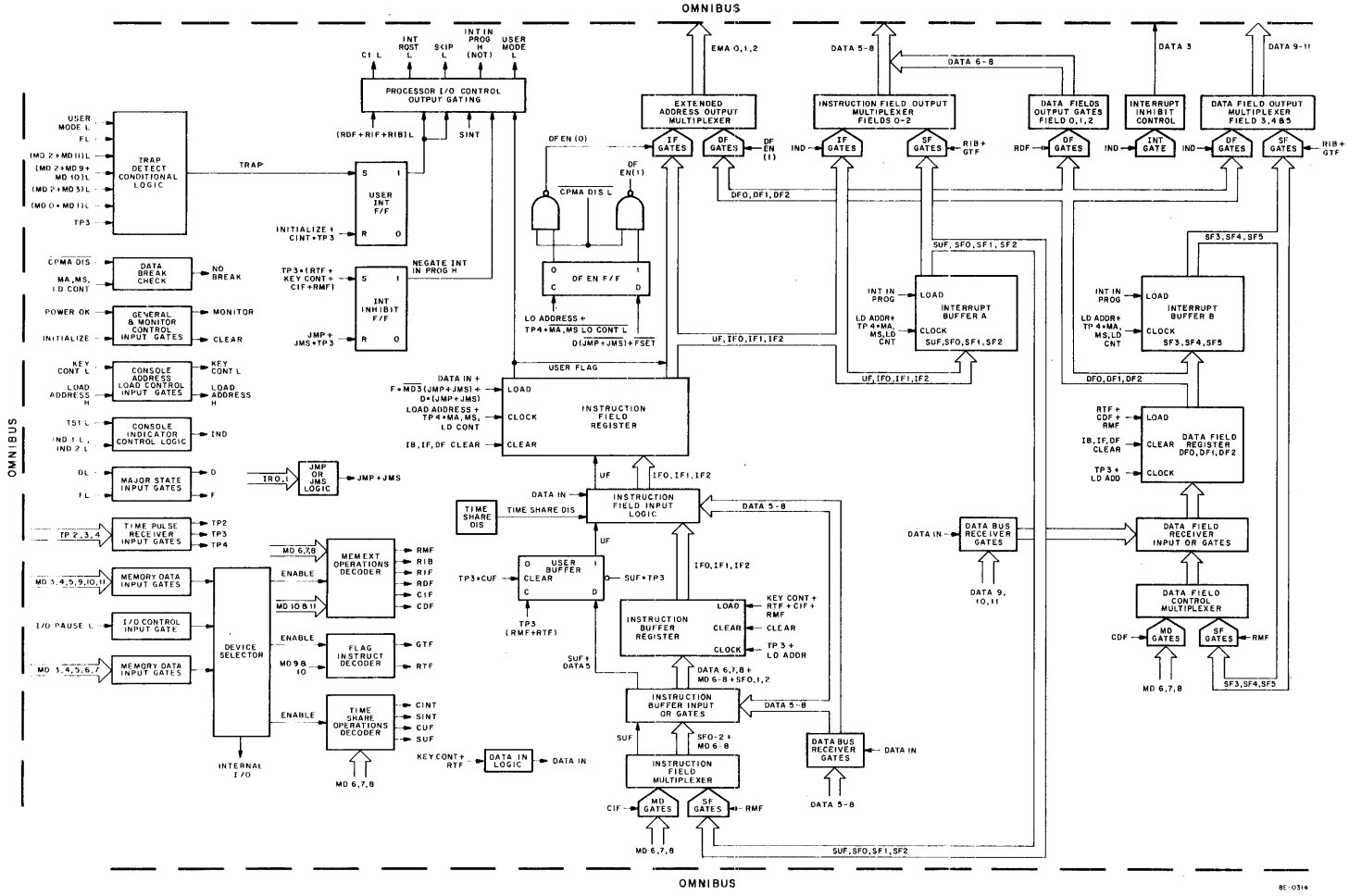

Figure 3 Memory Extension & Time Share Control System Block Diagram

3.1.1 Control Logic

The control logic (refer to Figure 3) for the Memory Extension and Time Share option contains elements similar to most I/O devices. These are the Device Selector Logic, Operations Decoders, the C1, INT RQST and SKIP signal lines. Therefore, before the operation of this option begins, an IOT instruction addressed to this option is required. The INT RQST and SKIP lines are directly controlled by the USER INT flip-flop which functions to detect a TRAP signal. This signals monitor that a TRAP has been detected. Monitor evaluates and takes appropriate action. The USER MODE L control signal is used in the processor to prevent the processor from responding to HLT, OSR and IOT instructions. The Int Inhibit flip-flop serves to ground the INT IN PROG line, thereby preventing an interrupt from occurring whenever instruction field changes are being processed.

For the user not desiring to use the Time Share portion of the option, a simple jumper on the module prevents the User Flag from being loaded. The instructions used with the Memory Extension and Time Share option are given in Table 1. For detailed explanation of each instruction, refer to the KM8-E memory option description in Chapter 7 of the PDP-8/E and PDP-8/M Small Computer Handbook - 1972.

Table 1
KM8-E Extended Memory and Time Share Option Instructions

MEMORY EXTENSION OPERATIONS	
Data Field and Instruction Field Operations	
RMF	(Restore Memory Field)
RIB	(Read Interrupt Buffer)
Data Field Operations	
CDF	(Change to Data Field)
RDF	(Read Data Field)
Instruction Field Operations	
RIF	(Read Instruction Field)
CIF	(Change to Instruction Field)
FLAG OPERATIONS	
GTF	(Get The Flags)
RTF	(Restore The Flags)
TIME SHARE OPERATIONS	
CINT	(Clear User Interrupt)
SINT	(Skip on User Interrupt)
CUF	(Clear User Flag)
SUF	(Set User Flag)

3.1.2 Instruction Field Registers and Controls

The Instruction Field Registers and Controls function to receive new instruction field from any one of three sources: a) Memory Data Lines; b) DATA BUS; c) the Interrupt Buffer. The main registers are the Instruction Buffer Register and the Instruction Field Register. The output lines of the Instruction Field Register are connected to the Extended Address Output Multiplexer and when selected address the Instruction Field by means of a combination of 3 bits on the EMA lines.

The simplified blocks (see Figure 3), concerned with the Instruction Field Register and Instruction Field Operation represents the flow of data, the necessary gating and the primary control signals to enable the gating, loading, clocking, etc. They function to select either the Save Field, the DATA BUS, or the Memory Data Lines as an input and output this information to either the Extended Address Output Multiplexer or to the DATA BUS. The flow of data is from the bottom to the top of the illustration. When the contents of the Interrupt Buffer are transferred to the Instruction Field Register, a RMF instruction gates the Save Field bits through the Instruction Field Multiplexer. When the contents of the Instruction Register was previously stored in some memory location, the CIF instruction gates bits MD6-8 through the Instruction Field Multiplexer.

The DATA BUS Receiver Gates function to receive the data from the AC Register or from the console Switch Register. During TS3 of the FETCH state, the contents of the AC are applied to the DATA BUS while the KM8-E Operations Decoder is decoding the RTF instruction. RTF immediately gates bits 5-8 into the Instruction Buffer Input OR Gates. This information may have been fetched from memory during the previous memory cycle or may have been inputted from the console Switch Register.

The contents of either the MD lines or the Save Field are gated through the Instruction Field Multiplexer by instruction RMF or CIF. The Instruction Buffer Input OR Gates in turn apply either Data 5-8, MD6-8 or the Save Field to the Instruction Buffer Register and applies the User Flag obtained from the Save Field to the User Buffer. The purpose of the Instruction Buffer is to prevent the logic from prematurely loading the Instruction Field Register.

If a CIF, RTF or RMF instruction is issued, the actual change of field does not take place until the next JMP instruction has been completed or until the Execute cycle of a JMS instruction has been entered.

The new Instruction Field is first loaded into the Instruction Buffer and then the transfer is made from the Instruction Buffer to the Instruction Register. It is loaded at TP4 so that memory is not disturbed.

Although data is available for input to the Instruction Buffer Register and the User Buffer, loading does not occur until the loading lines are asserted. For loading the Instruction Buffer, signal line KEY CONT must be grounded or one of the three loading instructions - RTF, CIF, RMF must be asserted

(grounded) and clocked in by TP3. Manual loading of data at the console Switch Register creates LD ADDR for the Instruction Buffer Clock input and KEY CONT for the buffer loading. Bits IF 0-2 representing one of eight possible instruction fields are on the buffer output lines when the buffer is loaded. The Instruction Field Input logic receives IF 0-2 and the User Flag. IF 0-2 bits are then OR'd with DATA 5-8 unless the operator is manually loading data into the Switch Register or an RTF instruction is executed. These conditions allow only DATA 5-8 to enter the Instruction Field Register. The User Flag is inhibited if the TIME SHARE DIS signal is asserted.

The program loading of the Instruction Field Register is accomplished by a directly addressed JMP or JMS instruction at the end of FETCH or by a JMP or JMS at the end of DEFER or by an RTF instruction. The manual loading is accomplished by signal KEY CONT developed when the operator loads data into the console switch register. The clocking for the programmed loading occurs at TP4 and for manual input occurs any time.

Once the Instruction Field Register is loaded, the contents are ready to be loaded into either the Extended Address Output Multiplexer or the Interrupt Buffer.

3.1.3 Interrupt Buffer A

The Interrupt Buffer A functions to save the contents of the Instruction Field when an interrupt occurs. Signal INT IN PROG H loads the User Flag and IF 0-2 bits at TP4. When the interrupt has been serviced and the Memory Extension is again activated, the contents of the Interrupt Buffer are inputted to the Instruction Field Multiplexer by an RMF instruction and the field change sequence of events will be repeated. Should the programmer wish to nest interrupts, he may store the contents of the Interrupt Buffer using the GTF instruction (or RIB instruction). The machine may be restored to its original condition using the RTF (or CIF and CDF) instruction.

3.1.4 Data Field Register and Controls

The Data Field Register and controls function to receive a new data field from any one of three sources: a) Memory Data Lines; b) DATA BUS; c) the Interrupt Buffer. The output lines of the Data Field Register are connected to the Extended Address Output Multiplexer and when selected address the Data Field by means of a combination of 3 bits on the EMA lines.

The simplified blocks (see Figure 3) concerned with the Data Field Register and Data Field Register operation represent the flow of data, the necessary gating and the primary control signals to enable the gating, loading, clocking, etc. They function to select either the Save Field, the DATA BUS, or the Memory Data Lines as an input and output this information to the EMA lines or the DATA BUS.

The flow of data is from the bottom to the top of the illustration. When the contents of the Interrupt Buffer are transferred to the Data Field Register, a RMF (Restore Memory Field) instruction gates the Save Field bits through the Data Field Control Multiplexer. When a CDF (Change Data Field) instruction is executed, bits MD 6-8 are gated through the Data Field Control Multiplexer.

The DATA BUS Receiver Gates receive the data from the AC Register or from the Console Switch Register. During TS3 of the FETCH state, the contents of the AC are applied to the DATA BUS while the KM8-E Flag Instruction Decoder is decoding the RTF instruction. RTF gates bits 9 through 11 into the Data Field Register.

The contents of either the MD lines or the Interrupt Buffer (RMF instruction) are gated through the Data Field control Multiplexer. At TP3, the new Data Field is loaded into the Data Field Register.

3.1.5 Interrupt Buffer B

The Interrupt Buffer B saves the contents of the Data Field whenever an Interrupt occurs. Signal INT IN PROG H loads the Data Field bits DF 0-2 at TP4. When the interrupt has been serviced and the memory extension is to be activated, the Data Field is restored to the Data Field Register by instruction RMF.

3.1.6 Extended Memory Addressing Output Control

The three EMA 0-2 lines address any one of 8 memory fields. When any combination of these lines are grounded, the result is a selected memory field. The Extended Address Output Multiplexer with the DF EN flip-flop determines whether the EMA bits will be the data field or the instruction field (see Figure 3). A simplified flow diagram illustrating the conditions which determine the selection is shown in Figure 4.

Beginning at the top of the flow diagram, the logic tests for a JMP or JMS instruction. If the JMP or JMS instruction is activated, the Instruction Field may be addressed. Otherwise, the logic tests the DEFER state. The DF EN flip-flop is clocked by TP4 or signal LD ADDRESS if the field is applied at the console switches. If a data break is in operation, the extended address will not at that time be applied to the EMA lines. As soon as data break ends, the Extended Address Output Multiplexer will be enabled to either gate the Instruction Field or Data Field bits out to the EMA lines and thereby select a memory field.

The rule for usage of the Data Field is as follows: If the current instruction is an AND, TAD, ISZ, DCA or EAE instruction, and if the processor is currently in the DEFER state, the next EXECUTE cycle will use the Data Field. All other machine cycles which are not Data Break cycles use the Instruction Field.

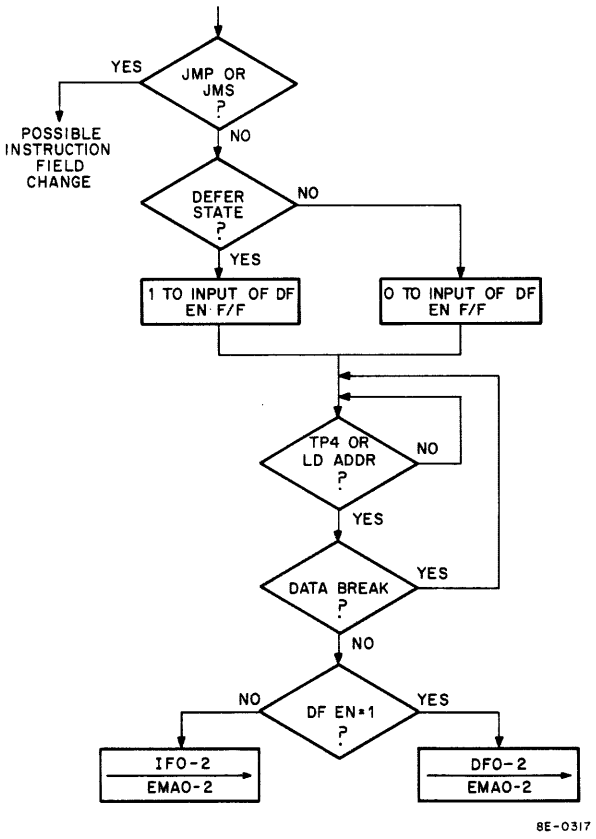

Figure 4 Extended Memory Addressing Flow Diagram

Notice that the DEFER state is tested at the end of the current processor cycle. The decision of whether the processor is to go to the EXECUTE state or the FETCH state is clearly indicated in Figure 3-17 in Volume 1 of this Maintenance Manual. The same type of decisions which determine if the next state is to be EXECUTE or FETCH determine if the Instruction Field or Data Field is to be addressed.

3.2 OPERATING FUNCTIONS

The following paragraphs provide some examples of the KM8-E operation. These descriptions reflect the flow of events for illustrative purposes and do not reflect the method by which this option is to be programmed.

3.2.1 Status Operation

Occasionally the user will want to select the STATUS position on the console selector switch. When he does this, signal IND will be generated at the start of TS1 and remain until TS2. Signal IND is used in the Memory Extension and Time Share logic to gate the contents of the IF and DF Registers through the Output Multiplexers and on to the DATA BUS. Refer to the system block diagram given in Figure 3 and to Figure 5 for the bit arrangement illustrating the status. Only bits 3 and 5 through 11 represent the status of the Memory Extension and Time Share control.

Bit 3 represents the interrupt status of the Interrupt Inhibit flip-flop. Signal INT INHIBIT is generated at TP3 whenever an RTF, KEY CONT, CIF, or RMF signal is asserted and negated at TP3 whenever a JMP or JMS instruction occurs. This prevents any memory field from being lost during a program interrupt. Thus, whenever bit 3 of the status indicator is illuminated, indicating a program interrupt inhibiting condition, the processor has not started a JMP or JMS instruction since the last Instruction Field change instruction was performed. When the IF and DF registers are loaded and signal INT IN PROG H is asserted, the contents of the registers are then loaded into the Interrupt Buffers at TP4.

Bits 5 through 8 represent the contents of the Instruction Field in the IF Register and bits 9 through 11 represent the contents of the Data Field in the (DF) Register.

3.2.2 Interrupt Buffer Transfer to Memory and Restoration

A simplified explanation of how the Interrupt Buffers could be stored in memory and restored to the Instruction Field and Data Field Registers is illustrated in Figure 6 and Figure 7. A Read Interrupt Buffer (RIB) or Get Flags (GTF) instruction creates the necessary gating signals to allow the Instruction Field and Data Field to pass through the corresponding output Multiplexers and be applied to the Data Bus. The same instruction grounds the C1 line which causes the contents of the DATA BUS to be loaded

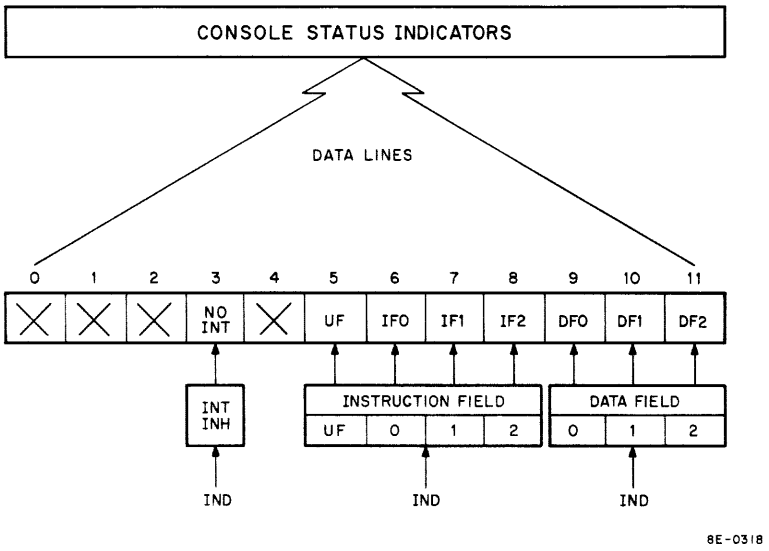

Figure 5 IF and DF Displayed Status During TS1

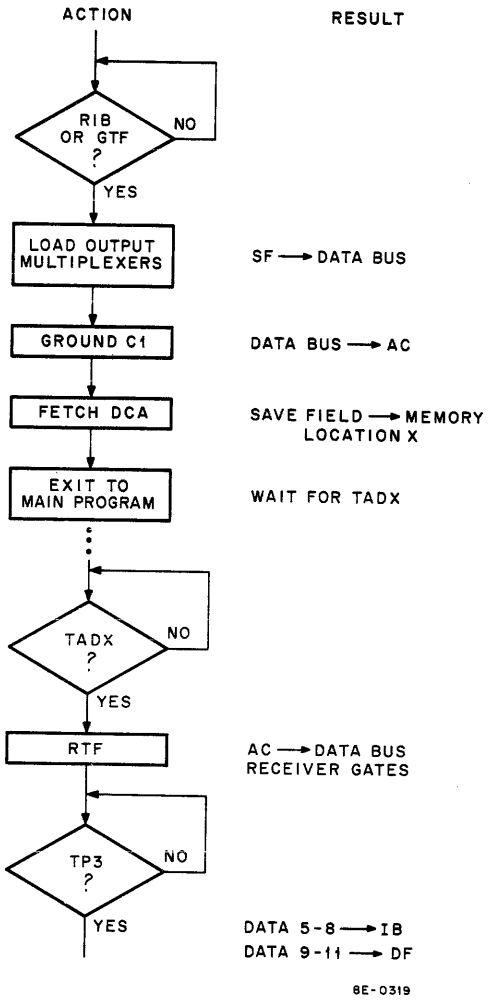

Figure 6 Interrupt Buffer Transfer to Memory and Restoration Flow Diagram

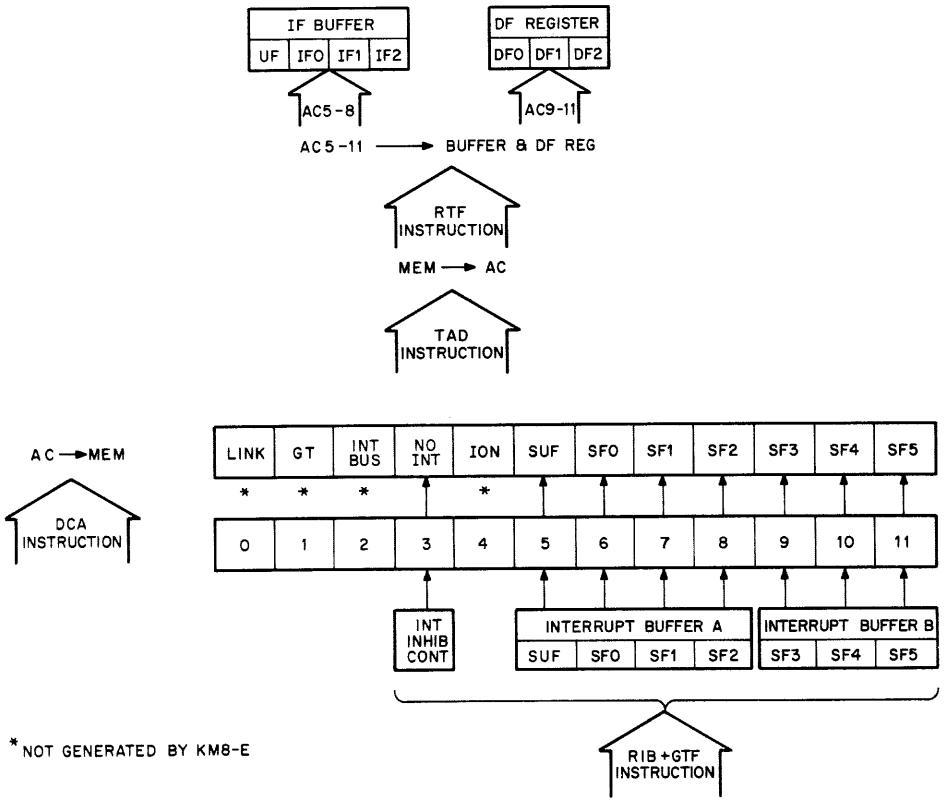

Figure 7 Interrupt Buffer Transfer to Memory and Restoration

into the AC Register. A DCA instruction transfers the contents of the AC Register to the corresponding addressed memory location. The next time the field is to be addressed, the TAD instruction returns the data to the AC Register and an RTF instruction allows the corresponding bits to be loaded into the Instruction Buffer and Data Field Registers at TP3. The addition of PC, AC and MQ handling will allow nesting of interrupts.

3.2.3 Instruction Field Register Loading Operation

The Instruction Field Register Loading operation is illustrated in the Instruction Field Register Loading Flow Diagram given in Figure 8. The first four decision blocks represent a "go" condition if any one of the blocks contain a status of "yes". For example, signal KEY CONT is developed whenever the operator depresses the EXTD ADDR LOAD key. The corresponding clock input is signal LD ADDR. If the loading of the Instruction Field Register is under program control, the next 3 conditions are tested. A restore flag instruction will allow the Instruction Field Register to be loaded at TP4. Otherwise the major states are tested. If the processor is in the FETCH state and not doing an RTF instruction, signal JMP or JMS is tested and finally MD3L is tested. When MD3H is present (indicating direct addressing), the Instruction Field Register will be loaded at TP4. Otherwise, a DEFER state with JMP or JMS is tested. Note that the Instruction Field Register will not be loaded during a Data Break. The clock input is set at TP4 to assure that there is no address mixup during the current memory cycle.

3.2.4 Time-Share Operation of the System

Because much of the logic is shared between the time share operation and the memory extension operation, it may not be obvious what logic is specifically dedicated to the time share function.

The time share portion operates in two modes as denoted by the User Flag (UF) flip-flop (refer to the system block diagram presented in Figure 3). When the UF flip-flop is in the logic 1 state, the system is operating in the user mode and a user program is running in the central processor. When the UF flip-flop is in the logic 0 state, the system is operating in the executive mode and the time-sharing monitor is in control of the central processor.

The four instructions developed by the Time-Share operations Decoder are used by the monitor in the executive mode and are never used by a user program. The Trap Logic is a monitoring device to assure the system that the user is programming valid instructions. When signal TRAP is developed, both the INT RQST and the SKIP lines are grounded. Monitor then takes over and examines the invalid instruction and determines what action must be taken.

The User Flag (UF) also plays an important role in monitoring for valid instructions. When the UF is a one, signal USER MODE L is developed and the grounded line which goes to the processor inhibits

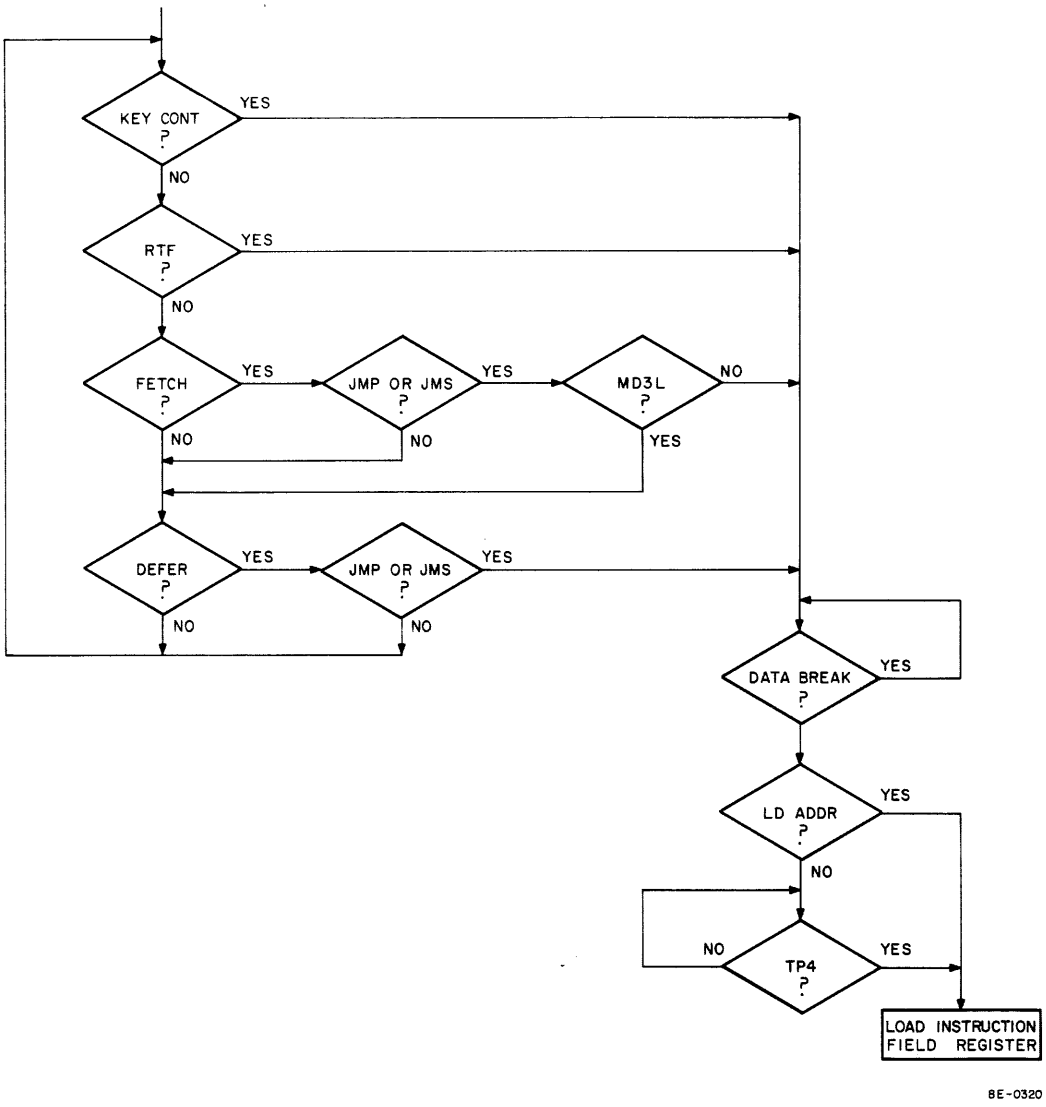

Figure 8 Instruction Register Loading Flow Diagram

signal STOP and signal I/O PAUSE. The processor is operating in the executive mode during the time that memory extension or time-sharing instructions are being processed. The User Mode begins when an SUF instruction has been completed. This sets the User Buffer flip-flop and inhibits the processor interrupt until the next JMP or JMS instruction. At the conclusion of either of these instructions, the User Flag is transferred into the Instruction Field Register. At that time, the User Flag signal is applied to the Processor I/O Control Output Gating where signal USER MODE L is developed.

The following is a summary concerning valid and trapped instructions:

FUNCTION NORMALLY:

- AND
- TAD
- ISZ
- DCA
- JMP
- JMS
- most OPERATES

TRAPPED INSTRUCTIONS:

HLT	Monitor Return. Machine must not stop because all users would be shut down.
OSR, LAS	Requires special action via Teleprinter. A user does not have his own Switch Register.
IOT	Requires interpretation (usually a device code change) by the monitor. For example, any user can use a KSF instruction (octal 6031). If executed by the computer, this instruction would test the flag of the console TTY. (the operator). However, the monitor alters this instruction by changing the middle 6 bits to the device code of the User's TTY.

SECTION 4 DETAILED LOGIC DESCRIPTION

This information will be supplied at a later date.

SECTION 5 MAINTENANCE

The general procedures concerning preventive and corrective maintenance are given in Volume 1, Chapter 4 of the Maintenance Manual. When corrective Maintenance is required, the technician should use the maintenance programs given in Section 2 of this option manual to determine the nature of the problem. The option schematic, drawing number E-CS-M737-0-1 must be referred to for IC locations and pin numbers. Test points have been provided on the module to facilitate troubleshooting.

SECTION 6 SPARES

This information will be supplied at a later date.

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