

DRWA DEC/X11 SYSTEM EXERCISER MODULE
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.REM -

IDENTIFICATION

PRODUCT CODE: AC-F004A-MC
PRODUCT NAME: CXDRWA0 DR11-W MODULE
PRODUCT DATE: SEPTEMBER 1979
MAINTAINER: DEC/X11 SUPPORT GROUP

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1. ABSTRACT

DRW IS AN IOMOD THAT EXERCISES ONE DR11-W. THE DEVICE IS EXERCISED USING THE MAINTENANCE MODE TO TRANSFER A 16 WORD BUFFER. MAINTENANCE MODE IS INTERNAL WRAP-AROUND LOGIC WHICH ELIMINATES THE NEED FOR A USER DEVICE OR PHYSICAL CABLE.

2. REQUIREMENTS

HARDWARE: ONE DR11-W INTERFACE
STORAGE: DRW REQUIRES:
1. DECIMAL WORDS: 287
2. OCTAL WORDS: 0437
3. OCTAL BYTES: 1076

3. PASS DEFINITION

ONE PASS OF DRW CONSISTS OF TRANSFERRING ONE 16 WORD BLOCK OF DATA 77000(8) TIMES

4. EXECUTION TIME

ONE PASS OF DRW RUNNING ALONE ON A PDP11/04 PROCESSOR TAKES APPROXIMATELY 85 SECONDS.

5. CONFIGURATION REQUIREMENTS

DEFAULT PARAMETERS:

DEVADR: 172410, VECTOR: 124, BR1: 5, DEVCNT: 1

REQUIRED PARAMETERS:

NONE

6. DEVICE/OPTION SET-UP

INSTALL DR11-W (NO PHYSICAL CABLE IS NECESSARY)

7. MODULE OPERATION

TEST SEQUENCE:

A: SET UP VECTOR AND DEVICE REGISTERS
R: GENERATE READ-WRITE BUFFER

- C. GENERATE CHECK BUFFER
- D. TRANSFER 16 WORDS IN MAINT. MODE
- E. COMPARE DATA IN/OUT - REPORT ERRORS
- F. REPEAT 77000 TIMES
- G. SIGNAL END OF PASS, RESTART AT A.

IF DEVICE FAILS TO INTERRUPT, AN ERROR MESSAGE WILL OCCUR AND THE PROGRAM WILL REQUEST THAT THE MODULE BE DROPPED.

8. OPERATION OPTIONS

NONE

9. NON STANDARD PRINTOUTS

NONE: ALL PRINTOUTS HAVE THE STANDARD FORMATS DESCRIBED IN THE DEC/X11 DOCUMENT.

10.0 READ-WRITE BUFFER DESCRIPTION

SUBROUTINE LODBUF LOADS DRBUF WITH AN INCREMENTING PATTERN (0123...15). WHEN XFERS ARE COMPLETE, DRBUF WILL BE MODIFIED TO 023...4. DUE TO THE ALTERNATING DATA-DATE SEQUENCE CHARACTERISTIC OF DR11-W MAINTENANCE MODE.

11.0 CHECK BUFFER DESCRIPTION

SUBROUTINE LODCHK LOADS CHKBUF WITH MODIFIED PATTERN DESCRIBED IN 10.

12.0 BURST OPERATION

CHARACTERISTIC OF DR11-W MAINTENANCE MODE OPERATION, THE XFERS ARE MADE IN ALTERNATING SINGLE CYCLE & BURST MODE FASHION. FOR THE FIRST FOUR XFERS THE DR11-W REQUESTS THE BUS ONLY ONCE, AND DOES NOT RELEASE IT UNTIL THE END OF THE FOURTH XFER. THE NEXT FOUR XFERS SEES THE DR11-W REQUESTING & RELEASING THE BUS FOR EACH XFER. THIS ALTERNATING ACTION CONTINUES FOR SUBSEQUENT XFERS.

000000
000000
; DR11-W DEC/X11 EXERCISER MODULE
; IOMOD <DRWA> 172410 124500 77000 165
; MODULE 140000 DRWA 172410 124500 77000 165
; TITLE DRWA DEC/X11 SYSTEM EXERCISER MODULE
; DDXCOM 23 MAY-78

000000
000000
000005
000006
000010
040527 040
; *****
; BEGIN: ASCII / ;MODULE NAME;
; MODNAM: BYTE / ;OPEN TO KEEP TRACK OF WBUF USAGE
; ADDR: 172410+0 ;1ST DEVICE ADDR.
; VECTOR: 124+0 ;1ST DEVICE VECTOR.

000012* 240
000013* 000
000014* 000001
000016* 000000
000020* 000000
000022* 000000
000024* 000000

000026* 140000
000030* 000224
000032* 000224
000034* 000000
000036* 077000
000040* 000000
000042* 000000
000044* 000000
000046* 000000
000050* 000000
000052* 000000
000054* 000000
000056* 000000
000060* 000000
000062* 000000
000064* 000000
000066* 000000
000070* 000000
000072* 000000
000074* 000000
000076* 000000
000100* 000000
000102* 000000
000104* 000000
000106* 000000
000110* 000000
000112* 000276
000114* 000000
000116* 000000
000120* 000000
000122* 000165
000040

```
BR1: .BYTE PRTV5+0 ;1ST BR LEVEL.
BR2: .BYTE PRTV0+0 ;2ND BR LEVEL.
DVID1: 0+1 ;DEVICE INDICATOR 1.
SR1: OPEN ;SWITCH REGISTER 1.
SR2: OPEN ;SWITCH REGISTER 2.
SR3: OPEN ;SWITCH REGISTER 3.
SR4: OPEN ;SWITCH REGISTER 4.
*****
STAT: 140000 ;STATUS WORD.
INLT: START ;MODULE START ADDR.
SPOINT: MODSP ;MODULE STACK POINTER.
PASCNT: 0 ;PASS COUNTER.
ICDNT: 77000 ;LOC TO COUNT ITERATIONS PER PASS=77000
SOPCNT: 0 ;LOC TO COUNT ITERATIONS
HRDCNT: 0 ;LOC TO SAVE TOTAL SOFT ERRORS
SOPPAS: 0 ;LOC TO SAVE TOTAL HARD ERRORS
HRDPAS: 0 ;LOC TO SAVE SOFT ERRORS PER PASS
SYSCNT: 0 ;LOC TO SAVE HARD ERRORS PER PASS
RANNUM: 0 ;# OF SYS ERRORS ACCUMULATED
CONFIG: 0 ;HOLDS RANDOM # WHEN RAND MACRO IS CALLED
RES1: 0 ;RESERVED FOR MONITOR USE
RES2: 0 ;RESERVED FOR MONITOR USE
SVRO: OPEN ;LOC TO SAVE R0.
SVR1: OPEN ;LOC TO SAVE R1.
SVR2: OPEN ;LOC TO SAVE R2.
SVR3: OPEN ;LOC TO SAVE R3.
SVR4: OPEN ;LOC TO SAVE R4.
SVR5: OPEN ;LOC TO SAVE R5.
SVR6: OPEN ;LOC TO SAVE R6.
CSRA: OPEN ;ADDR OF CURRNT CSR.
SADR: OPEN ;ADDR OF GOOD DATA, OR
ACSR: OPEN ;CONTENTS OF CSR.
WASADR: OPEN ;ADDR OF BAD DATA, OR
ASTAT: OPEN ;STATUS REG CONTENTS.
ERRTYP: 0 ;TYPE OF ERROR
ASR: OPEN ;EXPECTED DATA.
AWS: OPEN ;ACTUAL DATA.
RSTRT: RSTRT ;RSTRT ADDRESS AFTER END OF PASS
WDTO: OPEN ;WORDS TO MEMORY PER ITERATION
WDRP: OPEN ;WORDS FROM MEMORY PER ITERATION
INTF: OPEN ;# OF INTERRUPTS PER ITERATION
IDNUM: 165 ;MODULE IDENTIFICATION NUMBER=165
.REPT SPSIZ ;MODULE STACK STARTS HERE.
.NLIST
.LIST 0
.ENDR
```

000224*
210
211
212
213
214
215 000224*

```
MODSP: *****
;THIS MODULE TESTS THE DR-11W DIRECT MEMORY ACCESS INTERFACE
;INITIALIZATION FOR (DMA) DR-11W
START:
```

216 000224* 016705 177556
217 000230* 010567 000526
218 000234* 005725
219 000236* 010567 000522
220 000240* 010567 000516
221 000244* 010567 000512
222 000250* 005725
223 000252* 010567 000512
224 000254* 000000
225 000260* 010567 177524
226 000264* 010567 000502
227 000270* 005725
228 000272* 010567 000476
229
230
231
232
233
234 000276* 012767 077000 000440
235 000304* 104407 000000
236 000310* 104407 000000
237 000314* 012777 177750 000440
238 000322* 012767 000776 000424
239 000330* 104415 000000 000754
240 000336* 016777 000414 000420
241 000344* 005077 000416
242 000350* 012777 177777 000412
243 000356* 055777 000376 000402
244 000364* 012777 000512 000400
245 000372* 116777 177414 000374
246 000400* 005077 000342
247 000404* 004767 000244
248 000410* 004767 000202
249 000414* 012767 000010 000330
250 000422* 005077 000322
251 000426* 052777 010000 000332
252 000434* 052777 000501 000324
253
254
255
256 000442* 104407 000000
257 000446* 104407 000000
258 000452* 005767 000270
259 000456* 001402
260 000460* 001677 000420
261 000464* 005367 000260
262 000470* 001364
263 000472* 005367 000254
264 000476* 104361
265 000500* 104403 000000 000702
266 000506* 104410 000000
267
268
269
270 000512* 005267 000230
271 000516* 042777 000100 000242

```
MOV ADDR,R5 ;GET 1ST ADDRESS
MOV R5,RCR ;SET UP WORD COUNT REG.POINTER
TST (R5)+ ;MAKE CERTAIN REG. CAN BE ACCESSED
MOV R5,BAR ;SET UP BUS ADDRESS REG. POINTER
TST (R5)+ ;ACCESS REG.
MOV R5,CSR ;SET UP CONTROL STATUS REG. POINTER
TST (R5)+ ;ACCESS REGISTER
MOV R5,RDR ;SET UP DATA BUFFER REG. POINTER
TST (R5)+ ;ACCESS REG.
MOV R5,DRVEC0 ;LOAD DEVICE VECTOR
MOV R5,DRVEC0 ;SETUP DEV VECTOR PCOUNTER
TST (R5)+ ;ACCESS REGISTER
MOV R5,DRVEC2 ;SETUP PRIORITY POINTER
; DEVICE SERVICE CODE
RESTRT: MOV #77000,INTPSC ;TIMER FOR WHEN TO END PASS
CONT: BREAKS,BEGIN ;TEMPORARY RETURN TO MONITOR...
BREAKS,BEGIN ;THEN CONTINUE AT NEXT INSTRUCTION.
MOV #20,SMCR ;SIXTEEN WORD TRANSFER
MOV DRB00,VA ;SETUP BASE ADDRESS
CETPAS,BEGIN,VA ;GET PHYSICAL ADDRESS FROM 16-BIT VA
MOV PAC,BAR ;SET UP REAL ADDR.
CLR @CSR ;CLEAR THE CSR
MOV #1,@RDR ;SET UP DATA
BIS FA,@CSR ;SET EXTENDED MEM. BITS
MOV #DRIR,@DRVEC0 ;SET VECTOR TO SERVICE ROUTINE
MOVB BR1,@DRVEC2 ;SET PRIORITY
CLR INTFLG ;CLEAR INTERRUPT FLAG
JSR PC,LDBBUF ;GENERATE READ AND WRITE BUFFER
JSR PC,LDDCHK ;GENERATE CHECKING BUFFER
MOV #10,TMRCNT ;SET UP INTERRUPT LOUP
CLR TMR ;SETUP TIMER COUNTER
BIS #10000,@CSR ;MAINTENANCE MDDR
BIS #501,@CSR ;IE,CYCLE,AND GO
; WAIT FOR INTERRUPT CODE
TIMER: BREAKS,BEGIN ;TEMPORARY RETURN TO MONITOR...
BREAKS,BEGIN ;THEN CONTINUE AT NEXT INSTRUCTION.
TST INTFLG ;DID INTERRUPT OCCUR?
BEQ IS ;IF NOT CONTINUE IN TIMER
JMP CHECK ;IF YES,GO CHECK DATA
DEC TMR ;COUNT MORE TIME;IS TMR FINISHED
BNE TIMER ;IF NOT,BREAK AGAIN
DEC TMRCNT ;DECREASE OVERALL COUNT
BPL TMR ;GE AGAIN IF MORE TIME
MSGNS,BEGIN,HUNG ;ASCII MESSAGE CALL WITH COMMON HEADER
ENDS,BEGIN
; INTERRUPT SERVICE CODE
DRIR: INC INTFLG ;INTERRUPT HAS OCCURRED
BIC #100,@CSR ;CLEAR INTERRUPT ENABLE
```

```

272 000524* 000002
273
274
275
276 000526* 012701 000776*
277 000530* 012703 000010
278 000536* 012703 001036*
279 000542* 022123
280 000544* 001003
281 000546* 005302
282 000550* 003374
283 000552* 000415
284 000554* 016767 000206 177320
285 000562* 014167 177322
286 000566* 010167 177312
287 000572* 014167 177310
288 000576* 010167 177300
289
290 000602* 104404 000000*
291 000606*
292 000606* 104413 000000*
293
294 000612* 000167 177466
295
296
297
298 000616* 012702 001036*
299 000622* 005001
300 000624* 005003
301 000626* 010322
302 000630* 005001
303 000632* 062701 000002
304 000636* 020127 000020
305 000644* 001188
306 000644* 005207
307 000646* 062703 000002
308 000652* 000765
309
310
311 000654* 012701 000776*
312 000660* 005002
313 000662* 005021
314 000664* 005202
315 000666* 020277 000020
316 000672* 001402
317 000674* 010221
318 000676* 000772
319 000700* 000207
320
321 000702* 000706*
322 000704* 177777
323 000706* 042045 053105 041511
324 000714* 020105 040506 046111
325 000720* 042105 052040 020117
326 000730* 047111 042524 051122
327 000736* 050125 022524 000

```

```

RTI ;RETURN TO CODE WHERE INTERRUPT OCCURRED
;DATA CHECK CODE
CHECK: MOV #DRBUF,R1 ;GET THE BUFFER ADDRESS
MOV #8,R2 ;LOAD THE COUNTER
MOV #CHKBUF,R3 ;GET CHECK BUFFER ADDRESS
1$: CMP (R1),(R3)+ ;ARE THE TWO SEQUENTIAL WORDS EQUAL?
BNE 2$ ;NO, REPORT AN ERROR
DEC R2 ;DONE THE WHOLE BUFFER?
BGT 1$ ;NO, KEEP CHECKING
BGT 2$ ;YES,CHECK FOR ENDPASS
MOV CSR,ACSR ;ADDRESS OF CONTROL STATUS REGISTER
MOV -(R1),AWAS ;ACTUAL DATA
MOV R1,WASADR ;ADDRESS OF ACTUAL DATA
MOV -(R1),ASR ;CORRECT DATA
MOV R1,SBADR ;ADDRESS OF CORRECT DATA
;*****
DATERS BEGIN ;DATA ERROR!!!
;*****
DONE: ENDTLS,BEGIN ;SIGNAL END OF ITERATION.
JMP CONT ;MONITOR SHALL TEST END OF PASS
;ELSE DO IT AGAIN

LDCHK: MOV #CHKBUF,R2 ;LOAD CHKBUF WITH INCREMENTING
CLR R1 ;MODIFIED PATTERN
1$: MOV R3,(R2)+
MOV R3,(R2)+
ADD #1,R1
CMP R1,#20 ;ARE WE FINISHED?
BNE 2$ ;NO
RTS ;YES
2$: ADD #2,R3
BR 1$

LDDBUF: MOV #DRBUF,R1 ;LOAD DRBUF WITH INCREMENTING PATTERN
CLR R2
CLR (R1)+
1$: INC R2
CMP R2,#20 ;ARE WE DONE?
BEQ LDEXIT ;YES
MOV R2,(R1)+ ;NO,CONTINUE
LDEXIT: BR 1$
PC

HUNG: FAIL
177777
FAIL: -ASCIZ ;%DEVICE FAILED TO INTERRUPT%

```

```

328 000744* 000744*
329 000744* 000000
330 000746* 000000
331 000750* 000000
332 000752* 000000
333 000754* 000000
334 000756* 000000
335 000760* 000000
336 000762* 000000
337 000764* 000000
338 000766* 000000
339 000770* 000000
340 000772* 000000
341 000774* 000000
342 000776* 000020
343 001036* 000020
344 000001 000001

```

```

EVEN
INTPSC: OPEN
INTFLG: OPEN ;COUNTS FOR WHEN TO ENDPASS
TMR: OPEN
TMRCNT: OPEN
VI: OPEN
PA: OPEN
EA: OPEN
MCR: OPEN
BAR: OPEN
CSR: OPEN
BDR: OPEN
DRVEC0: OPEN
DRVEC2: OPEN
DRBUF: .BLKW 20
CHKBUF: .BLKW 20
.END

```


STAT	000026R	168#		
SVR0	000062R	183#		
SVR1	000064R	184#		
SVR2	000066R	185#		
SVR3	000070R	186#		
SVR4	000072R	187#		
SVR5	000074R	188#		
SVR6	000076R	189#		
SYSCNT	000052R	178#		
TIME	000422R	249#		
TIMER	000442R	255#	262	264
TMR	000750R	249#	261*	331#
TMRcnt	000752R	248#	263*	332#
TRDPFD=	000022	210#		
VA	000754R	237#	238	333#
VECTOR	000010R	159#	225	
WASADR	000104R	193#	286*	
WCR	000762R	217#	236*	336#
WDFR	000116R	200#		
WDT0	000114R	199#		
XPLAG	000005R	157#		
.	= 001076R	328#	342#	343#

. ABS. 000000 000
001076 001

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

XDRWAO, XDRWAO/SOL/CRF:SYM=DDXCOM, XDRWAO
RUN-TIME: 11.2 SECONDS
RUN-TIME RATIO: 11/3=3.7
CORE USED: 7K (13 PAGES)