

## IDENTIFICATION

Product Code: AC-8898E-MC  
Product Name: CZLACE0 LA36 TERM (DL11 & KL11)  
Date Created: August 1978  
Maintainer: DIAGNOSTIC GROUP  
Authors: Robert W. Baker  
R. Quenneville  
Ralph A. Schaubert  
John V. Chatalian

The information in this document is subject to change without notice and should not be construed as a commitment by Digital Equipment Corporation. Digital Equipment Corporation assumes no responsibility for any errors that may appear in this manual.

The software described in this document is furnished to the purchaser under a license for use on a single computer system and can be copied (with inclusion of Digital's copyright notice) only for use in such system, except as may otherwise be provided in writing by Digital.

Digital Equipment Corporation assumes no responsibility for the use or reliability of its software on equipment that is not supplied by Digital.

Copyright (C) 1974, 1977, 1978 by Digital Equipment Corporation

HISTORY

1.0 DECO CZL  
AC-E-0)

1.1.0 Closed Problem Report AA3318

1.1.1 It was reported that a DL11-A operated at 110 baud caused failure in the AREAD routine because the 200 msec. delay is not of sufficient duration to allow setting of the Receiver Register Status "DONE" bit through the Maintenance bit facility. The time delay was increased from 200 to 600 msec.

1.2.0 Closed Problem Report AA3643

1.2.1 Tests 56, 57, 60, 61, 62, 63, 64, 65, and 66 do not run properly when run on an LSI-11. This problem was resolved by changing the branch after the CHAIN command to go back to test for the LSI-11 switch in order to effect the appropriate action during each test.

1.2.2 Second time-out in Test 64 allows excessive wait for operator response. The time delay was reduced from "177777" to "600".

1.2.3 Common routine TYPE does not save the contents of R0 resulting in the loss of this information and consequent failure. Instructions were included to save the contents of R0 on entry into the routine and to restore them upon exit.

1.2.4 Loss of stack contents for non-LSI-11 computers due to incorrect sequence of instructions in Test 65 was also reported in Problem Report AA3803. Refer to 1.3.1.

1.3.0 Closed Problem Report AA3803

1.3.1 Testing of non-LSI-11 computer  
s results in the program hanging  
up because the stack gets popped awa  
y in Test 65. The branch  
after the test for the LSI-11 switch in Test 6  
5 should go to  
the CHAIN command for proper exit from the test for n  
on-LSI-11  
machines. This change supersedes the change released in DEP  
0  
MD-11-DZLAC-D-1.

## TABLE OF CONTENTS

1.0	ABSTRACT
2.0	REQUIREMENTS
2.1	Equipment and Assignments
2.2	Storage
2.3	Preliminary Programs
2.4	Additional Programs
3.0	LOADING PROCEDURE AND INITIALIZATION
4.0	STARTING PROCEDURE
4.1	Startin
4.2	Addresses
4.3	Switch Register Control With I/O Tests
4.4	Switch Register Control Without I/O Tests
4.5	Keyboard Control With I/O Tests
4.6	Keyboard Control Without I/O Tests
5.0	OPERATING PROCEDURE
5.1	Switch Register Control
5.2	Keyboard Control
6.0	TEST DESCRIPTIONS
6.1	Printing Tests
6.1.1	Test0 - Data Path Test
6.1.2	Test1 - Printable Character Test
6.1.3	Test2 - Non-printable Character Test
6.1.4	Test3 - Carriage Return Test
6.1.5	Test4 - Multiple Line Feed Test
6.1.6	Test5 - Single Line Feed Test
6.1.7	Test6 - Backspace Test
6.1.8	Test7 - Overprint Test
6.1.9	Test8 - Printing Frequency Sweep Test
6.1.10	Test9 - Ribbon Feed Test
6.1.11	Test10 - Printer Bell Test
6.1.12	Test11 - Life Test

6.2 Echo Tests  
6.2.1 Test20 - Character Echo Test  
6.2.2 Test21  
- Line Echo Test, Fast Rate  
6.2.3 Test22 - Line Echo Test, Slow Rate  
6.2.4 Test23 - Character/Code Echo Test  
6.2.5 Test24 - Selected Pat  
tern Echo Test  
6.2.6 Test25 - Bell Echo Test  
6.4 Standard I/O Tes  
ts

## 1.0 ABSTRACT

This diagnostic is divided into three basic sections:

1. A check of the console terminal interface logic.
2. A check of the printing characteristics and control logic.
3. An echo portion designed to check the keyboard and to aid in the diagnosis of terminal problems.

Patterns used by the printing tests were chosen for ease of visual verification. The echo tests were designed for maximum flexibility, with Test 24 allowing any desired pattern to be used.

## 2.0 REQUIREMENTS

## 2.1 EQUIPMENT AND ASSIGNMENTS

The diagnostic is written to run on all models of the PDP-11 computer with either a KL11 or DL11 console terminal interface. The diagnostic is preset to test up to 16 additional terminals (on DL11's) assigned between addresses 776500 and 776676. This preset quantity (16) and pre-set address (776500) can be changed by depositing the quantity in DLNR and the starting address in DLADR. For example, to allow for up to 31 additional terminals, the address 775610 could be placed into DLADR and the octal equivalent of 31, i.e., (37) would be placed into DLNR. The number of additional DL11's actually tested will be adjusted automatically downward based upon the first DL11 address (within the implied range) found to be unresponsive. Thus if there is no DL11 present to match the address in DLADR only the console terminal will be tested. Therefore, all DL11's in excess of the console terminal must have contiguous address assignments with the lowest address corresponding

ponding to the value in DLADR.

The console terminal (assigned standard) can be reassigned by placing the address of its receiver status register into CONNADD and its receiver interrupt vector into CONVEC. This reassignment can be made to a terminal within the set of terminals implied by DLNR and DLADR without adverse effect. Note that a terminal with a slower speed (if any) will determine the speed at which all of the terminals are tested. Such a terminal should generally be excluded from the test, or tested separately. (Refer to the symbol definitions in the listing for the above mentioned locations.)

## 2.2 STORAGE

The diagnostic program uses all of 4K of memory with exception of the area used by the absolute loader.

### 2.3 PRELIMINARY PROGRAMS

Any applicable PDP-11 diagnostics should be run on the processor. If any errors are encountered during the interface check, refer to the appropriate interface diagnostic for further help in locating the problem if needed.

### 2.4 ADDITIONAL PROGRAMS

This diagnostic is for verification of basic terminal functions only. If the terminals under test have hardware options installed run diagnostic MAINDEC-11-DZLAF-A, the LA36 TERMINAL OPTIONS TEST.

### 3.0 LOADING PROCEDURE AND INITIALIZATION

Load the LA36 diagnostic program tape following normal procedures. Before starting the program, refer to the description of the routine "DLY". Time delays used by the program are a function of the CPU model and memory type and should be set-up before running the diagnostic. The routine is preset for a PDP-11/05 with core memory. Refer to Section 2.1 for non-standard terminal addresses and for testing multiple DL11 interfaces.

If a hardware switch register does not exist, the program will use the contents of location 176 as the value of the switches. Therefore, be sure to load location 176 with the switch value before starting the program when not using hardware switches.

If the CPU is an LSI-11, 11/03 be sure to set switch register bit 9 to a 1. Special tests are run on the DLV11 interface.



#### 4.0 STARTING PROCEDURE

##### 4.1 STARTING ADDRESSES

200(8) = Run with Switch Register Control  
- perform Console T

terminal I/O tests.

204(8) = Run with Switch Register Control

- skip Console Terminal I/O tests.

210(8) = Run with Keyboard

Control

- perform Console Terminal I/O tests.

214  
(8) = Run with Keyboard Control

- skip Console Terminal I/O tests.

#### 4.2 Switch Register Control With I/O Tests

- A. Set the switch register to 200(8) and press the load address switch.
- B. Set switch register bit 9 to a 1 if the processor is an LSI-11, 11/03. Refer to Section 5.1.5.
- C. Set the switch register bits 7-0 equal to the paper width in terms of the number of columns (octal). Refer to Section 5.1.8.
- D. Set the switch register bit 8 equal to 0 or 1 and press the start switch. A message will be printed indicating the number of DL11's being tested. Refer to Section 5.1.6.
- E. If bit 8 were zero when starting, the Printer tests are executed sequentially, after the entire series of I/O tests are executed.
- F. If bit 8 was set when the start switch was pressed, the entire series of I/O tests will be executed and the CPU will halt at location SELHLT. The program will then be waiting for control via the switch register.

#### 4.3 Switch Register Control - Without I/O Tests

Same as Section 4.2 except in step A, set the switch register to 204(8).

PAGE 7

#### 4.4 Keyboard Control - With I/O Tests

- A. Set the switch register to 210(8) and press the load address switch.
- B. Set the switch register bits 7-0 equal to the paper width in terms of the number of columns (octal). Refer to Section 5.1.8.
- C. Set switch register bit 9 to a 1 if the processor is an LSI-11/03. Refer to Section 5.1.5.
- D. Set switch 8 and press the start switch. A message will be printed indicating the number of DL11's being tested. Refer to Section 5.1.6.
- E. If bit 8 was zero when starting, the printer tests are executed sequentially after the entire series of I/O tests are executed.
- F. If bit 8 were set when the start switch was pressed, the entire series of I/O tests will be executed followed by the select test message. The program will then be waiting for a test selection via any terminal keyboard. Refer to Section 5.2.

#### 4.5 Keyboard Control - Without I/O Tests

Same as Section 4.4 except in step A, set the switch register to 214 (8).

#### 5.0 OPERATING PROCEDURE

The program can be controlled in either of two methods: by the con-

sole switch register or from the keybo  
ard of the terminal(s) under  
test.

## 5.1 SWITCH REGISTER CONTROL

The various switches and their functions are listed below. Switches may be changed and set as desired except as noted in the specific switch descriptions. Refer to the detailed switch descriptions for further, more complete information.

SWITCH NUMBER	DESCRIPTION
15 T AT END OF TEST	1(up) = HALT 0(down) = CONTINUE TEST SEQUENCE
14 ERROR	1(up) = CONTINUE ON ERROR 0(down) = HALT ON ERROR
13	1(up) = DRIVE ONLY CONSOLE TERMINAL 0(down) = DRIVE ALL TERMINALS
11 INDIVIDUAL TEST	1(up) = LOOP ON INDIVIDUAL TEST 0(down) = NORMAL TEST SEQUENCE
9 ALL OTHER PDP-11'S	1(up) = CPU TYPE IS AN LSI-11, 11/03 0(down) = ALL OTHER PDP-11'S
8	1(up) = RUN TEST ONCE AND HALT 0(down) = LOOP ON TEST SEQUENCE
5-0 TEST NUMBER SELECTION	
7-0 ART-UP	NUMBER OF COLUMNS AT START

## 5.1.1 Switch 15

With switch 15 in the up position, the program will halt at the end of the current test. Replacing switch 15 to the down position and press-

ing CONTINUE will continue the normal test operation. Dur  
ing the  
halt, any of the control switches may be changed or set as desired.

#### 5.1.2 Switch 14

Placing switch 14 in the up position will cause the pro  
gram to contin-  
ue on errors during any of the I/O tests only. With switch 1  
4 down,  
the program will halt (at ERRHLT) on any errors during the I-O tests  
with the location of the error in R0. Pressing CONTINUE will cause  
the pro  
gram to continue if switch 14 is down. With switch 14 up,  
pressing contin  
ue will cause the program to loop on the error.

NOTE

Error halts can occur only during the I/O tests. The terminal is connected to a serial line and there is no error information returned to the program from the terminal. Therefore the program cannot report errors occurring in the terminal. Errors detected during the interface tests will result in halts as described above.

5.1.3 Switch 13

Placing switch 13 in the down position will cause the driving of all multiple terminals during the Printer tests only. If switch 13 is up, only the console terminal is driven.

\*\* Note: Switch 13 should only be changed when the program is waiting for a test selection.

5.1.4 Switch 11

Placing switch 11 up at any time will cause the program to loop on the current test as long as switch 11 remains up. Replacing switch 11 down will cause the program to resume normal operation at the completion of the test.

5.1.5 Switch 9

Placing switch 9 up at the start of the test will cause an automatic change in the DELAY timing, and the execution of special DLV11 I/O tests. The DLV11 has no maintenance mode and will cause th

e program  
to hang if tested as a DL11.

#### 5.1.6 Switch 8

With switch 8  
in the down position the program will continue to loop  
through the present t  
est sequence. Placing switch 8 up will cause the  
program to halt (at SELHLT) a  
t the completion of the current test.  
After the halt, set the control switc  
hes as desired and set switches 5  
to 0 to the next desired test number, and the  
n press CONTINUE to start  
the test.



When starting the diagnostic the operator can select a specific test rather than automatically starting the printing test sequence by setting switch 8 up before starting the diagnostic. Upon completion of the I/O test sequence (if being run) the program will either halt at SELHLT waiting for a test selection via the switch register or print the select test message and wait for a test selection from any keyboard. Refer to Section 4 for further information.

#### 5.1.7 Switches 5 to 0

Switches 5 to 0 are used to select specific tests when under switch register control. Test numbers are always in octal.

#### 5.1.8 Switches 7 to 0 (at start-up only)

At start-up only, switches 7 to 0 are used to set the desired maximum number of columns the diagnostic is to test. If the number set is greater than 132(10) or less than 30(10), the program will default to 132(10). The value set must be in octal form. Thus, for normal operation leave switches 7 to 0 down to test the full 132(10) columns.

## 5.2 KEYBOARD CONTROL

The program will be under keyboard control whenever the diagnostic is started at location 210 or 214. Switches on the console switch register will have no effect when under terminal control except for switch 15. The I/O tests cannot be selected when under keyboard control.

To stop a test at any time, type the "RUBOUT" or "DELETE" key on any keyboard. Any terminal may stop the test and select the next test if switch 13 is down. When a test is stopped by typing a "RUBOUT" or "DELETE", the test will terminate and the following message will be typed:

SELECT TEST NUMBER

At this time, type the desired test number followed by any one of the following control characters:

. (period) = Run the selected test once and return for another test selection.

L = Loop on the selected test until a "RUBOUT" is typed.

S = Start the test sequence with the selected test. continue to loop on the printing test sequence until a "RUBOUT" is typed.

The "L" or "S" may be either upper or lower case, but the test number must always be a 2 digit octal number. The test number and terminator are echoed by the program, thus each character will be printed twice if the terminal is in half duplex. For all echo tests, the "L" and "S" will only run the test once (the same as if typing a period). For

all option tests, the "S" will only run the test once (the same as if typing a period), however, typing an "L" will cause the program to loop on the selected test. If an error is detected in the test selection (illegal test number or control character), a question mark is printed and the message will be repeated.



characters are printed in groups of three with three groups per line, separated by three spaces between groups. The first column will contain all ASCII codes from 040 to 077. Column two will contain all ASCII codes from 100 to 137 - primarily the capital letter set. The last column will contain all ASCII codes from 140 to 176 - primarily the small letter set.

With the Auto Line Feed Option set to produce an automatic line feed after every carriage return, there will be a blank line between each printed line.

EXAM  
 PLE:

			AAA	'''
B	bbb		AAA	aaa
		###	BR	
		\$\$\$	CCC	ccc
EE	eee	%%%	DDD	ddd
		^^^	E	
		(((	FFF	fff
HHH	hhh	)))	GGG	ggg
		+++	III	iii
		)))	JJJ	)))
KKK	kkk	+++		
		///	LLL	lll
		---	MMM	mmm
NNN	nnn	...		
		///	OOO	ooo
		000	PPP	ppp
QQQ	qqq	111		
		222	RRR	rrr
		333	SSS	sss
4	TTT	44		
		ttt	UUU	uuu
		555	VVV	vvv
		666		
77	WWW	7		
		www	XXX	xxx
		888	YYY	yyy
		999		
:::	ZZZ	zzz		
		)))	[[[	
		(((	\\	
		===	]]	
]		>>>		
		???		

6.1.3 Test 2 - Non-printable Character Test

This test checks all non-printable characters that have no control function in the LA36 terminal or the LA36 options (such as CR, LF, BS,

& BEL).  
First the ASCII code will be printed followed by the mnemonic  
after a few separating spaces. Following the mnemonic, the actual  
control character will be sent three times and nothing should happen  
at the printer. This pattern is repeated three times on a line,  
until all of the non-printing characters have been tested.

With the Auto Line Feed Option set to produce an automatic  
line feed after every received carriage return, there will be a blank line  
between each printed line.





EXAMPLE:

```
0 0 0 0 0 0 0 0 0
      X  X  X  X  X  X  X
        X  X  X  X  X  X
          X  X  X  X
            X
```

6.1.5 Test 4 - Multiple Line Feed Test

This test checks the line feed capability of the printer by sending various groups of line feeds interspaced with reference lines. The number printed as the reference line indicates the number of line feeds that follow. The first and last lines also contain a string of dashes as reference points for measuring the total distance between the two dashed lines, i.e., 63(10) lines.

With the Auto Line Feed Option set to produce an automatic line feed after every carriage return, the number printed will indicate one less than the number of line feeds (the number of blank lines) that follow. The total distance between the two dashed lines will then be 69 lines.

EXAMPLE:

```
----- 01-----  
-----  
02  
04  
  
08  
  
16 \ 15 Blank Line  
32 /  
31 \ 31 Blank Lines  
00-----
```

### 6.1.6 Test 5 - Single Line Feed Test

This test is designed to check the timing of single line feeds and the capability of doing line feeds in all columns. Two reference lines are used by this test (and Test 6) which also can be used to easily check the number of columns the printer is printing.

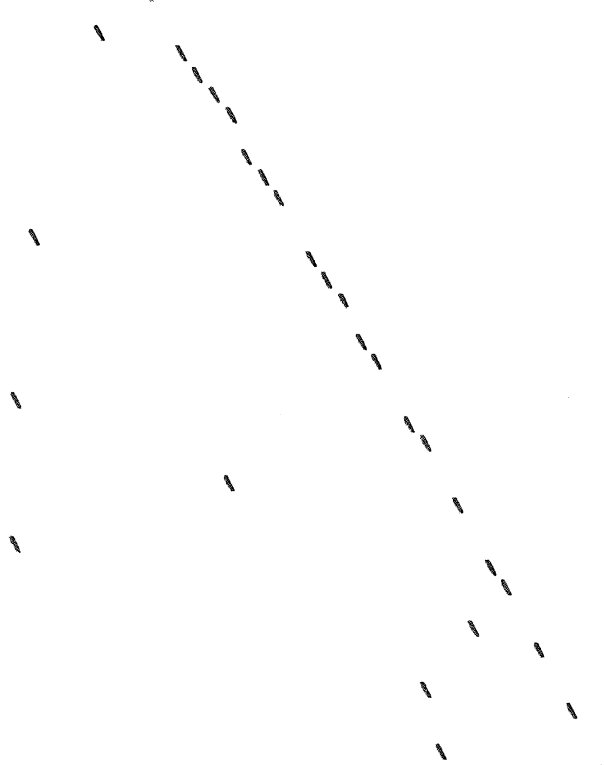
The first reference line contains 130(10) zeroes followed by two 2's if testing 132(10) columns. If less than 132 columns, the line will contain 0's for two less than the maximum number of columns followed by the two 2's. This reference line is a quick check for 132(10) columns if testing the full 132(10) columns. The second reference line prints a string of numbers ( 1 to 9 & 0 ) repeated to the maximum column. This line, again, can be used as a quick check of the number of columns.

The line feed test is accomplished by: printing the first reference line of 0's and two 2's; then either sending 60(10) 3's, if testing 132(10) columns, or waiting 1.8 seconds for an LCV, if testing less than 132(10) columns. If testing 132(10) columns, nothing should happen, except for an LCV, at the end of the line. The 3's should be lost and never printed. After the LCV, with the print head at the extreme right, a carriage return - line feed will be sent followed by repeated backslashes "\" and linefeeds to print a diagonal line down the paper. When a backslash is printed in the maximum column, a carriage return will be sent immediately after the line feed and the second reference line of sequential numbers will be printed. After completing the line, a carriage return - line feed will be sent and the program will wait one second for the carriage return function to complete. After the delay, the reference line will be repeated, the last line being guaranteed to be correct. Any timing problems

during th  
e line feeds will show as misprints or missing characters  
during the first  
16(10) characters of the middle reference line.  
Also, any paper feed pro  
blems will cause misalignment of the slashes  
forming the diagonal line.

EXAMP  
LE:

0000000000000000000000000000000022



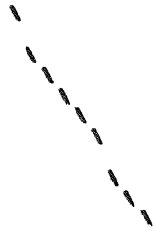
123456789012345678901234567890  
123456789012345678901234567890

With the Auto Line Feed Option set to produce an automatic line feed after every received carriage return, there will be a blank line every

place a  
carriage return is executed.

EXAMPLE:

0000000022



1234567890

1234567890

6.1.7 Test 6 - Backspace Test

This test is designed to test the print timing as in Test 5 as well as the backward and forward movement of the print solenoid head.

The test consists of the same first reference line as in Test 5 then a carriage return-line feed. A full line is then printed using the following pattern:

Forward Slash "/"  
Backspace  
Back Slash "\"

This pattern produces a line of all X's. The two slashes should cross exactly at the middle, producing the X character. When the line is completed a carriage return-line feed is sent and the last two reference lines are printed as in Test 5. Any timing problems will show in the first 16(10) characters of the middle reference line; again as in Test 5.

With the Auto Line Feed Option set  
to produce an automatic line feed  
after every received carriage return,  
there will be a blank line  
between each printed line.

EXAMPLE:

```
0000000000000000000000000000022  
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
123456789012345678901234567890  
123456789012345678901234567890
```



6.1.8 Test 7 - Overprint Test

This test is designed to check the spacing and repeatable printing characteristics of the printer. Three rows of characters are each overprinted two times. The rows consist of the following characters alternated across the line:

Row 1		M-SP
Row 2	SP-a	
Row 3	&-SP	

The resulting pattern will be a checkerboard pattern and the overprinted characters should be aligned properly with the initial characters.

EXAMPLE:

```

      M
M M M M M M M M M M M M M M
      @ @ @ @ @ @ @ @ @ @ @ @ @ @ @ @
& & & & & & & & & & & & & & &

```

With the Auto Line Feed Option set to produce an automatic line feed after every received carriage return, the lines will not be overprinted. There will be three lines of each character with a blank line between each group of characters. The characters in each group should be in the same columns.

EXAMPLE:

```

      M M M M M M M M M M
M M M M M M M M M M M M
      M M M M M M M M M M
@ @ @ @
      @ @ @ @ @ @ @ @ @ @ @
      @ @ @ @ @ @ @ @ @ @ @

```

١٢  
١٣  
١٤  
١٥  
١٦  
١٧  
١٨  
١٩  
٢٠  
٢١  
٢٢  
٢٣  
٢٤  
٢٥  
٢٦  
٢٧  
٢٨  
٢٩  
٣٠  
٣١  
٣٢  
٣٣  
٣٤  
٣٥  
٣٦  
٣٧  
٣٨  
٣٩  
٤٠  
٤١  
٤٢  
٤٣  
٤٤  
٤٥  
٤٦  
٤٧  
٤٨  
٤٩  
٥٠  
٥١  
٥٢  
٥٣  
٥٤  
٥٥  
٥٦  
٥٧  
٥٨  
٥٩  
٦٠  
٦١  
٦٢  
٦٣  
٦٤  
٦٥  
٦٦  
٦٧  
٦٨  
٦٩  
٧٠  
٧١  
٧٢  
٧٣  
٧٤  
٧٥  
٧٦  
٧٧  
٧٨  
٧٩  
٨٠  
٨١  
٨٢  
٨٣  
٨٤  
٨٥  
٨٦  
٨٧  
٨٨  
٨٩  
٩٠  
٩١  
٩٢  
٩٣  
٩٤  
٩٥  
٩٦  
٩٧  
٩٨  
٩٩  
١٠٠



With the  
Auto Line Feed Option set to produce an automatic line feed  
after every received carriage return, there will be a blank line  
between each printed line.

EXAMPLE:

X  
X  
X  
X  
X  
X  
X

6.1.11 Test 12 - Printer Bell Test

This test checks the printer bell buffer to insure that eight bells are distinctly heard, even when sent at the maximum transfer rate. The program sends 8 bell codes at the maximum rate to the printer then waits 2.5 seconds to allow the operator to hear the bells.

6.1.12 Test 17 - Life Test

This test runs continuously and is run as an individual, special test. It is not part of the standard printing test sequence.

This test prints 2 lines of each printable character and then repeats continuously. The second line of each character is overprinted 4 times to conserve paper. At the end of each complete pass through the character set, a message is printed indicating the number of passes executed. If any character (except "Rubout") is typed on the keyboard during this test, the pattern will change and restart with the typed character. This will only happen if keyboard control is in use.

EXAMPLE:

AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA  
AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA  
AA  
BBBBBBBBBBBBBBBBBBBBBBBBBBBBBB  
BBBBBBBBBBBBBBBBBBBBBBBBBB

If the Auto Line Feed Option is set to produce an automatic line feed after every received carriage return, the test will print six lines of each character with a blank line between the first and second lines as well as between each group of characters.

EXAMPLE:

AAAAAAAAAAAAAAAA

AAAAAAAAAAAAAAAA  
AAAAAAAAAAAAAAAA  
AAAAAAAAAAAAAAAA

AAAAAAAAAAAAAAAA  
AAAAAAAAAAAAAAAA

BBBBBBBBBBBBBBBB

BBBBBBBBBBBBBBBB  
BBBBBBBBBBBBBBBB  
BBBBBBBBBBBBBBBB

BBBBBBBBBBBBBBBB  
BBBBBBBBBBBBBBBB

## 6.2 ECHO TESTS

These tests are designed as a test of the keyboard and an aid in isolating troubles within the terminal. At the beginning of each test, the test number will be printed indicating which test is being executed. Typing a "RUBOUT" or "DELETE" at any time, whether in keyboard control or not, will exit the current Echo test and print a test termination message. If in keyboard control, the select test message will be printed and the program will await a test selection as usual. In switch register control, the program will halt (at SELLHLT) waiting for control via the switch register. A detailed description of each test follows:

## 6.2.1 Test 20 - Character Echo Test

This test is designed to operate the terminal in a simulated local mode. Any character typed on the keyboard (except a "rubout") will be echoed to the printer.

If the LA36 terminal is in half duplex with the Auto Line Feed Option available, typing a carriage return may cause a garbled response on the terminal during this test.

## 6.2.2 Test 21 - Line Echo Test, Fast Rate

This test continually sends full lines of any character up to the maximum column width. The test prints a "0" character when started until a key is typed on the keyboard. The program will then send the typed character until another character is typed or the test is terminated by typing a "rubout". The characters are transmitted at the maximum rate with a carriage return-line feed inserted after

every 132(10)  
printable characters.

If the LA36 is in half duplex when running this test, characters may be lost or garbled whenever a character is typed on the keyboard.

With the Auto Line Feed Option set to produce an automatic line feed after every carriage return, there will be a blank line between each printed line.

### 6.2.3 Test 22 - Line Echo Test, Slow Rate

This test is identical to Test 21 except a delay of 1.8 seconds is inserted between each character to allow the print head to perform an LCV between characters.



## 6.2.4 Test 23 - Character/Code Echo Test

This test will print the octal code received by the processor followed by the character or the mnemonic of the character every time a key is pressed on the keyboard. The parity of the received code will be indicated as either odd or even. Allow sufficient time between characters for the line to be printed.

With the Auto Line Feed Option set to produce an automatic line feed after every received carriage return, there will be a blank line between each printed line.

EXAMPLE:

	301	A	ODD
	263	3	ODD
VEN	215	CR	E
	240	SP	EVEN

## 6.2.5 Test 24 - Selected Pattern Echo Test

This test is designed to give maintenance the flexibility to choose their own patterns for isolating any specific problems which may arise in the field.

Type any characters (except control-C and rubout) and each character will be echoed as typed. A maximum of 256(10) characters may be inputted. No carriage returns or line feeds are inserted by the program, all characters must be inputted by the operator. To terminate the input string type a control-C, the program will then continually echo the inputted pattern. To stop the printing, type control-C. The program will stop printing the pattern and will wait for either another pattern input terminated by a control-C, or the same pattern may be used again by typing control-C. To exit the test at any time, type a "rubout".

When any options are available, be careful what characters or character sequences are selected.

#### 6.2.6 Test 25 - Bell Echo Test

This test is designed to test the bell on column 64 if typing has occurred on the line. The test prints a message:

```
TYPE ANY PRINTABLE CHAR  
ACTER AND LISTEN FOR BELL .....
```

After the test message is printed, type any printable character on the keyboard. The character will be echoed and the bell should ring. The message will then be typed again. Type the "rubout" key to terminate the test at any time.

#### 6.4 STANDARD I/O TESTS

These tests are designed as a brief check of the console terminal interface logic. Each check is structured as an independent test and the switch register control \$ may be used. A description of each test is given in the program listing.

Any errors encountered during the I/O tests will cause a halt at location "ER RHLT" if switch 14 is down.

CZLACEO LA36 TERM (DL11 & KL11) MACRO M1110 25-AUG-78 10:13  
TABLE OF CONTENTS

1-	1900	SWITCH REGISTER OPTIONS
2-	4500	SPECIAL OPERATIONAL INFORMATION
3-	6700	SYSTEM EQUATES
4-	13500	TRAP CATCHER & STARTING ADDRESSES
5-	19100	SYMBOL DEFINITIONS
7-	100	PROGRAM INITIALIZATION & CONTROL
13-	46300	COMMON ROUTINES USED BY LA36 TESTS
26-	100	I/O LOGIC TESTS
42-	100	LA36 PRINTER TESTS
55-	100	LA36 ECHO TESTS
62-	100	MISC. DIAGNOSTIC MESSAGES

400  
500  
600  
700  
800  
900  
1000  
1100  
1200  
1300  
1400  
1500  
1600  
1700  
1800  
1900  
2000  
2100  
2200  
2300  
2400  
2500  
2600  
2700  
2800  
2900  
3000  
3100  
3200  
3300  
3400  
3500  
3600  
3700  
3800  
3900  
4000  
4100  
4200  
4300

```

        .TITLE CZLACE0 LA36 TERM (DL11 & KL11)
        LA36 DIAGNOSTIC (DL11 & KL11 INTERFACE)
        AUTHORS:  ROBERT W. BAKER
                   R. QUENNEVILLE
                   RALPH A. SCHAUBER
                   JOHN V. CHATAKIAN
        COPYRIGHT 1974,1977,1978 DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754

        .SBTTL SWITCH REGISTER OPTIONS
        SWITCH      POSITION      FUNCTION
        15          UP (1)       HALT AT COMPLETION OF CURRENT TEST
                   DOWN (0)     CONTINUE NORMAL TEST SEQUENCE
        14          UP (1)       CONTINUE ON ERROR
                   DOWN (0)     HALT ON ERROR
        13          UP (1)       DRIVE ONLY CONSOLE TERMINAL
                   DOWN (0)     DRIVE ALL TERMINALS
        11          UP (1)       LOOP ON INDIVIDUAL TEST
                   DOWN (0)     NORMAL TEST SEQUENCE
        09          UP (1)       CPU TYPE IS AN LSI-11, PDP-11/03
                   DOWN (0)     ALL OTHER PDP-11 CPUs
        08          UP (1)       HALT TO SELECT TEST AT END OF CURRENT TEST
                   DOWN (0)     LOOP ON TEST SEQUENCE
        05-00      TEST # SELECTION
        07-00      # OF COLUMNS AT START-UP
    
```

4500  
4600  
4700  
4800  
4900  
5000  
5100  
5200  
5300  
5400  
5500  
5600  
5700  
5800  
5900  
6000  
6100  
6200  
6300  
6400  
6500

```

        .SBTTL SPECIAL OPERATIONAL INFORMATION
        1.-- THE STANDARD CONSOLE TERMINAL INTERRUPT VECTOR AND REGISTER
              ADDRESSES ARE USED. TO REDEFINE THE LOCATION OF THE CONSOLE
              TERMINAL THE SYMBOLIC LOCATIONS "CONADD" AND "CONVEC" SHOULD
              BE CHANGED BEFORE START UP.
        2.-- BEFORE START UP REFER TO THE DESCRIPTION OF THE ROUTINE "DLY".
              TIMING IS A FUNCTION OF THE PDP-11 MODEL AND MEMORY TYPE AND
              SHOULD BE SET UP BEFORE RUNNING THE DIAGNOSTIC.
        3.-- IF CPU IS A PDP-11/03, LSI-11 SET SWITCH REGISTER
              BIT 09 TO A 1. SPECIAL TESTS ARE RUN ON THE DLV11.
        4.-- SYSTEMS WITHOUT A HARDWARE SWITCH REGISTER SHOULD USE
              MEMORY LOCATION 176 AS A SOFTWARE SWITCH REGISTER.
        5.-- THIS DIAGNOSTIC IS FOR VERIFICATION OF BASIC TERMINAL
              FUNCTIONS ONLY. IF THE TERMINAL UNDER TEST HAS HARDWARE
              OPTIONS INSTALLED RUN DIAGNOSTIC MAINDEC-11-DZLAF-A, THE
              LA36 TERMINAL OPTIONS TEST.
    
```

```

SYSTEM EQUATES
6700
6800
6900
7000
7100
7200
7300
7400
7500
7600
7700
7800
7900
8000
8100
8200
8300
8400
8500
8600
8700
8800
8900
9000
9100
9200
9300
9400
9500
9600
9700
9800
9900
10000
10100
10200
10300
10400
10500
10600
10700
10800
10900
11000
11100
11200
11300
11400
11500
11600
11700
11800
11900
12000
12100
12200
12300

```

```

000000
000001
000002
000003
000004
000005
000006
000007
177776
000001
000002
000003
000004
000010
000016
000040
000100
000200
000300
001000
002000
004000
008000
010000
020000
040000
080000
100000
200000
400000
800000
004000
008000
005726
006340
000200
000300
001000
001000
104000
104001
104002
104003
104004
104005
104006
104007
104010
104011
104012
104013

```

```

.SBRTL SYSTEM EQUATES

REGISTER EQUATES
R0=*0
R1=*1
R2=*2
R3=*3
R4=*4
R5=*5
SP=*6
PC=*7
PSW=177776

SYSTEM EQUATES
BIT0=1
BIT1=2
BIT2=4
BIT3=10
BIT4=16
BIT5=40
BIT6=100
BIT7=200
BIT8=400
BIT9=1000
BIT10=2000
BIT11=4000
BIT12=8000
BIT13=16000
BIT14=32000
BIT15=64000
DPS=0
SCOPSW=BIT14
NITRSW=BIT11
DPS2=7226
PRTV7=340
PRTV4=200
ACRLF=200
LST11=BIT9

PROGRAM TRAP EQUATES
TYPE=EMT+0
ERRDR=EMT+1
EHALT=EMT+2
STRDRV=EMT+3
STPCNV=EMT+4
CHAIN=EMT+5
CHALT=EMT+6
TVPEM=EMT+7
DELAY=EMT+10
TTVCL=EMT+11
CRLF=EMT+12
SCRFLF=EMT+13

```

```

;SCOPE SWITCH
;TEST LOOP SWITCH
;POP STACK ONCE
;POP STACK TWICE
;PRIORITY LEVEL DEFINITIONS

;FLAG FOR LSI-11,11/03

```

```

SYSTEM EQUATES
12400
12500
12600
12700
12800
12900
13000
13100
13200
13300

```

```

104014
104015
104016
104017
104020
104021
104022
104023
104024
104025

```

```

LF=EMT+14
PINTC=EMT+15
PRTHDR=EMT+16
PRNT=EMT+17
READ=EMT+20
AREAD=EMT+21
CR=EMT+22
RDASC=EMT+23
FORWD=EMT+24
READC=EMT+25

```

```

13500
13700
13800 000000
13900 000000
14000
14100
14200
14300 000000 000002
14400 000002 000000
14500 000004 000006
14600 000006 000000
14700 000010 000012
14800 000012 000000
14900 000014 000018
15000 000016 000000
15100 000020 000022
15200 000022 000000
15300 000024 000026
15400 000026 000000
15500 000030 002722
15600 000032 000340
16300
16400
16500
16600 000042 000000
16700
16800
16900
17000 000046 000046
17100
17200
17300
17400 000052 010000
17500
17600
17700
17800 000174 000000
17900 000176 000000
18000
18100 000200 000167 000604
18200 000204 000167 000526
18300 000210 000167 000320
18400 000214 000167 000552
18500
18600
18700
18800
18900 000600 000000

        .SBTTL TRAP CATCHER & STARTING ADDRESSES
        .ENABL  ARS,AMA
        .ASECT

        .=-0
        .+2
        MACHER: HALT ;UNASSIGNED TRAP
        .+2
        HALT ;SP OVERFLOW, BUS ERROR TRAP
        .+2
        HALT ;RESERVED INSTRUCTION TRAP
        .+2
        HALT ;TRACE TRAP
        .+2
        HALT ;TRAP TO CALL IOX
        .+2
        HALT ;POWER FAIL TRAP
        EMTINT ;EMT TRAP
        PRIV7

        .=-42
        0
        .=-46
        LOGICAL
        .=-52
        010000
        .=-174

DISPREG: .WORD 0 ;SOFTWARE DISPLAY
SWREG:   .WORD 0 ;SOFTWARE SWITCH REGISTER

        JMP START ;START UP WITH I/O TESTS RUNNING
        JMP START+1 ;START UP, SKIP ALL I/O TESTS
        JMP START+2 ;START UP, TERMINAL CONTROL WITH I/O TESTS
        JMP START+3 ;START UP TERMINAL CONTROL WITHOUT I/O TESTS

        .=-600
        SPBOT: 0 ;BOTTOM OF STACK
    
```

```

19100
19200
19300
19400
19500 000602 177560
19600 000604 000600
19700 000606 176500
19800
19900
20000
20100
20200 000610 000020
20300 000612 177560
20400 000614 177562
20500 000616 177564
20600 000620 177566
20700 000622 000000
20800 000624 000000
20900 000626 000000
21000 000630 000000
21100 000632 000000
21200 000634 000000
21300 000636 000000
21400 000640 000000
21500 000642 000000
21600 000644 000000
21700 000646 000000
21800 000650 000000
21900 000652 000000
22000 000654 000000
22100 000656 000000
22200 000660 000000
22300 000662 000000
22400 000664 000000
22500 000666 000000
22600 000670 000000
22700 000672 0000251
22800 000674 000000
22900 000676 000000
23000 000700 000000
23100 000702 000000
23200 000704 000000
23300 000706 000000
23400 000710 000000
23500 000712 000000
23600 000714 177570
23700 000716 000000

        .SBTTL SYMBOL DEFINITIONS
        ;
        ;
        CONADD: 177560 ;ADDR OF CONSOLE RECEIVER STATUS REG
        CONVEC: 60 ;CONSOLE TERMINAL INTERRUPT VECTOR
        DLADR: 176500 ;ADDRESS OF FIRST DL11, DEFAULT TO DL11-A,B
        ;IF DL11-C,D,E, THEN
        ;SET TO 175610 FOR FIRST 16 (OF 31) OR
        ;SET TO 176000 FOR LAST 16 (OF 31)
        ;OR SET OTHER DESIRED START ADDRESS
        ;# OF DL11'S TO BE INITIALLY ASSUMED
        DLNR: 16 ;CONSOLE RECEIVER STATUS REG
        TKS: 177562 ;CONSOLE RECEIVER BUFFER
        TKB: 177562 ;CONSOLE RECEIVER STATUS REG
        TPS: 177564 ;CONSOLE TRANSMITTER STATUS REG
        TPB: 177566 ;CONSOLE TRANSMITTER BUFFER
        TKVTR: 60 ;C-T RECEIVER INTERRUPT VECTOR
        TKLVL: PRTY4 ;C-T RECEIVER PRIORITY LEVEL
        TPVTR: 64 ;C-T TRANSMITTER INTERRUPT VECTOR
        PTLVL: PRTY4 ;C-T TRANSMITTER PRIORITY LEVEL
        PTDL: OPEN ;ADDRESS OF FIRST ACTIVE DL11
        CNTLSW: OPEN ;CONSOLE TERMINAL CONTROL SWITCH
        RTNNO: OPEN ;CONTAINS CURRENT TEST NUMBER
        NXTST: OPEN ;CONTAINS ADDRESS OF NEXT TEST
        SCOPTR: OPEN ;CONTAINS ADDRESS OF TEST SCOPE ENTRY
        PRGID: OPEN ;CONTAINS TEST PROGRAM INDICATORS
        CRBWF: OPEN
        CTRA: OPEN
        WIDTH: OPEN ;CURRENT PAPER WIDTH, BINARY
        LEVEL: OPEN ;LEVEL OF EXECUTION
        DLCNT: OPEN ;# OF MULTIPLE DL11'S
        ICTR: OPEN ;I/O TEST ITERATION COUNT
        REPT: OPEN ;TEMP STORAGE FOR TESTS E021 & E022
        BRCTR: OPEN ;COUNTER FOR ROUTINE "READA"
        COUNT3: OPEN ;COUNTER FOR ROUTINE "PRINTC"
        XCSR: OPEN ;ADDRESS OF MULTIPLE DL11 STATUS
        TIMER: 251 ;# MSEC COUNTER FOR ROUTINE "DELAY"
        SPNTR: OPEN ;COUNTER FOR TEST ROUTINE "PT3"
        CURTST: OPEN ;ADDRESS OF CURRENT TEST
        TEMPCH: OPEN ;TEMP STOR FOR ECHO TESTS
        PARTV: OPEN ;PARITY FLAG FOR RECEIVED CHAR
        PCHAR: OPEN ;CHAR CODE WITH PARITY BIT
        LFCNT: OPEN ;COUNTER FOR TEST ROUTINE "PT4"
        INCHK: OPEN ;CHECK FOR INPUT FLAG
        TEMP: OPEN ;TEMPORARY WORKING STORAGE
        SR: 177570 ;SW REG ADDRESS
        CNTR: OPEN ;TIME COUNTER FOR LSI-11 TESTS
    
```

23900

PROGRAM INITIALIZATION & CONTROL

.SBTTL PROGRAM INITIALIZATION & CONTROL

```

100
300
400
500
900
100
800
900 000720 005767 177730
1100 000722 011400
1200 000730 005740
1300 000732 000000
1400 000734 000000
1500 000736 012767
1600 000744 012767 177777 004324
1700 000752 000424
1800 000762 012767 104006 000726
1900 000762 012767 005320 004300
2000 000770 000415
2100 000772 012767 104011 000716
2200 001000 012767 177777 004262
2300 01006 000406
2400 001010 012767 005320 004252
2500 001016 012767 104006 000654
2600 001024 012766 000600
2700 001030 016746 176752
2800 001034 016746 176744
2900 001040 012767 001054 176736
3000 001046 005777 177642
3100 001052 000411
3200 001054 012767 000176 177632
3300 001062 012766
3400 001064 104000
3500 001066 014424
3600 001070 012767 000202 177574
3700 001076 012667 176702
3800 001102 012667 176700
3900 001106 005067 177576
4000 001112 012767 000006 176664
4100 001120 005067 177520
4200 001124 005067 177504
4300 001130 005067 177520
4400 001134 012767 003460 176662
4500 001142 004767 002542

```

```

;*****
;COMMON HALT---WHEN IN SWITCH REGISTER CONTROL THE CPU
;WILL BE ADVANCED TO THIS COMMON HALT WHERE
;A NEW TEST WILL BE EXPECTED TO BE STARTED
;*****
CHLT:  TST    LEVEL      ;TEST CURRENT LEVEL
      BEQ    SELHLT    ;BRANCH IF 0, DO NOT HALT
      MOV    RSP,RO    ;PUT ADDRESS OF CALLER INTO RO
      TST    -(RO)
      HALT
SELHLT: RTI          ;RETURN FROM INTERRUPT
START1: MOV    #CHALT,WAIF ;FORCE END OF I/O TESTS
      MOV    #177777,ATOX ;FORCE SR CONTROL
      BR     STARTX
START2: MOV    #TTYCTL,WAIF ;FORCE TERMINAL CONTROL
      MOV    #ATI,ATOX    ;FORCE ALL I/O TESTS
      BR     STARTX
START3: MOV    #TTYCTL,WAIF ;FORCE TERMINAL CONTROL
      MOV    #177777,ATOX ;FORCE END OF I/O TESTS
      BR     STARTX
START:  MOV    #ATI,ATOX   ;FORCE ALL I/O TESTS
      MOV    #CHALT,WAIF  ;FORCE SR CONTROL
STARTX: MOV    #SP00,SP   ;SET STACK POINTER
      MOV    0,-(SP)     ;SAVE CURRENT VECTOR
      MOV    #105,4      ;SET UP TIMEOUT VECTOR
      TST    RSR         ;TRY TO REFERENCE HARDWARE SW REG
      BR     11$        ;BRANCH IF NO TIMEOUT TRAP OCCURS
      MOV    #SWREG,SR   ;POINT TO SOFTWARE SWITCH REGISTER
      CMP    (SP)+,(SP)+ ;RESTORE STACK
      TYPE   NOSWR      ;TELL OPERATOR TO USE SOFTWARE
      MOV    #202,TIMER  ;SWITCH REG AT LOC 176
      MOV    (SP)+,4    ;ADJUST TIMER FOR LSI-11
      MOV    (SP)+,6    ;RESTORE TIMEOUT VECTOR
      MOV    #6,WACHER  ;ALLOW INPUT CHECKING
      MOV    #6,WACHER  ;CLEAN UP
      CLR    PRGID      ;INITIALIZE PROGRAM FLAGS
      CLR    CNTLSW     ;INITIALIZE TERMINAL CONTROL SWITCH
      CLR    LEVEL      ;INITIALIZE LEVEL
      MOV    #PFA,24    ;SET ADDR POWER FAIL ROUTINE
      JSR    PC,CONIT   ;SET UP CONSOLE TERMINAL ADDRESS

```



```
4700 ;*****  
4800 ;READ THE PAPER WIDTH, NUMBER OF COLUMNS  
4900 ;FROM SWITCH REGISTER POSITIONS 0-7. SAVE AND  
5000 ;CONVERT TO 3 ASCII CHARACTERS. A WIDTH GT 132  
5100 ;OR LT 30 COLUMNS (DECIMAL) WILL BE ABORTED TO 132.  
5200 ;THE SWITCHES MAY BE CHANGED ONCE THE PROGRAM TITLE OR THE DL11 COUNT  
5300 ;MESSAGE HAS STARTED TO PRINT.  
5400 ;*****  
5500  
5600 001146 017701 177542      MOV     RSR,R1      ;PUT (SR) INTO R1  
5700 001152 022701 177400      BIC     R1,#17400,R1 ;SAVE ONLY BITS 0-7  
5800 001156 020127 000204      CMP     R1,#204     ;TEST NO. COLUMN GT 132  
5900 001162 003103              RGT     R1,#35     ;COLUMNS GT 132, DEFAULT TO 132  
6000 001164 020127 000035      1S:    CMP     R1,#35     ;CHECK IF NO. COLUMNS LT 30  
6100 001170 011062              BHL     R1,#35     ;NOT LT 30 NOR GT 132  
6200 001172 012701 000204      2S:    MOV     #204,R1  ;COLUMNS LT 30 OR GT 132, DEFAULT  
6300 001176 010167 000450      3S:    MOV     R1,WIDTH  ;SAVE NO. COLUMNS IN WIDTH  
6400 001202 012700 014127      MOV     #RDR,R0    ;ADDR TO STORE ASCII COLUMN VALUE  
6500 001206 012702 000003      MOV     #3,R2      ;DO A 3 CHAR. CONVERSION  
6600 001212 104023              BTOASC  ;CONVERT NO. COLUMNS TO ASCII  
6700 001214 000461              BR      5S         ;  
6800 001216 000410              BR      5S         ;  
6900 001220 012700 000000      5S:    MOV     #0,R0     ;TRANSMIT A  
7000 001224 012700 000000      PRINTC ;NULL CODE  
7100 001226 104007              TYPEM   ;TYPE PROGRAM TITLE FIRST TIME RUN  
7200 001230 013676              STARTM  ;  
7300 001232 012767 000240 17754  MOV     #NOP,4S
```

```
7500 ;*****  
7600 ;THIS NEXT PART CHECKS THE PRESENCE OF DL11-A OR DL11-C  
7700 ;STARTING AT 776500 A MESSAGE WILL BE PRINTED INDICATING THE NUMBER  
7800 ;PRESENT. THE PRINTER DIAGNOSTIC WILL ADDRESS EACH OF  
7900 ;THE MULTIPLE DL11S IN THE SYSTEM IF SWITCH 13 IS DOWN (0).  
8000 ;*****  
8100  
8200 001240 012767 001320 176536 6S:  MOV     #END2A,MACHER ;INITIALIZE TIME OUT TRAP  
8300 001246 016700 177334      DLADR,R0 ;ADDRESS OF FIRST DL11 TO RO  
8400 001252 016701 177332      MOV     DLNR,R1   ;SET DL CHECK COUNT  
8500 001256 005067 177374      CLR     DLCNT    ;INITIALIZE DLCNT  
8600 001262 005410              TST     (R0)      ;IS DL PRESENT?  
8700 001264 012767 001332 176512 END3:  MOV     #END2,MACHER ;YES, RESET TIME OUT TRAP  
8800 001272 010067 177334      MOV     R0,FSTDL ;STORE ADDRESS OF FIRST DL11  
8900 001278 000401              BR      2S       ;CONTINUE  
9000 001300 005710              TST     (R0)      ;IS DL11 PRESENT  
9100 001302 062700 000010      ADD     #10,R0   ;POINTER AND DL11 ADDRESS  
9200 001306 005067 177344      INC     DLCNT   ;INCREMENT COUNT OF DL11'S  
9300 001312 005307              DEC     R1       ;DECREMENT DL CHECK COUNT, DONE?  
9400 001314 001407              BEQ     END4     ;BRANCH IF DONE  
9500 001316 000770              BR      1S       ;CHECK PRESENCE OF NEXT DL11  
9600 001320 005301              DEC     R1       ;DONE DL CHECK?  
9700 001324 001404              BEQ     END2A   ;YES, EXIT  
9800 001324 062700 000010      ADD     #10,R0   ;NO, CHECK NEXT DL  
9900 001330 000754              BR      END3     ;CONTINUE  
10000 001332 022656              POPSP2 ;DL11 NOT PRESENT  
10100 001334 016700 177316 END4:  MOV     DLCNT,R1  ;GET # DL11'S  
10200 001340 012700 014064      MOV     #DL11S1,R0 ;ADR OF ASCII CHAR STORAGE  
10300 001344 012702 000002      MOV     #2,R2    ;# OF ASCII CHARS  
10400 001350 104023              BTOASC  ;CONVERT NUMBER  
10500 001352 104023              TYPEM   ;TYPE MESSAGE  
10600 001354 014051              DL11S  ;  
10700  
10800 ;*****  
10900 ;EXECUTE THE STRING OF CONSOLE TERMINAL I/O TESTS  
11000 ;THEN EITHER HALT AT LOCATION SELHL1 OR CONTINUE WITH  
11100 ;PRINTER TESTS AS A FUNCTION OF SR BIT 9.  
11200 ;*****  
11300  
11400 001356 005067 177254      CLR     RTNNO    ;SET ROUTINE NO = 0  
11500 001362 005067 177266      CLR     LEVEL    ;SET LEVEL = 0  
11600 001366 026727 003676 177777  CMP     ATOX,#17777 ;SEE IF I/O IS TO BE SKIPPED  
11700 001374 001515              BEQ     SKIP     ;  
11800 001376 012767 005266 177234  MOV     #ATO,NXTST ;ADDRESS OF FIRST I/O TEST  
11900 001404 104024              FORWD  ;SET UP TEST PARAMETERS  
12000 001406 000177 177264      JMP     @CURIST  ;GO TO I/O TEST ROUTINE
```

```

12200
12300
12400
12500
12600
12700
12800
12900
13000
13100
13200
13300
13400
13500
13600
13700
13800
13900
14000
14100
14200
14300
14400
14500
14600
14700
14800
14900
15000
15100
15200
15300
15400
15500
15600
15700
15800
15900
16000
16100
16200
16300
16400
16500
16600
16700
16800
16900
17000
17100
17200
17300
17400
17500
17600
17700
17800
001412 032767 000001 177214 CHAINN: BIT #1,CNTLSW ;CHECK IF TERMINAL CONTROL
001420 001401 ;BEQ IS ;BRANCH IF NOT
001422 104011 ;TIVCTL ;GO TO TERMINAL CONTROL
001424 177214 1S: ;PRGID ;TEST ERROR BIT IN PRGID
001426 100016 ;RPL 3S ;BRANCH IF ERROR BIT NOT SET
001428 040000 177254 ;SCOPSW,MSR ;ERROR CHECK IF SCOPE OPTION ON
001430 032777 ;RT ;BRANCH IF NO SCOPING
001432 177777 177172 ;#-1,SCOPTR ;YES, CHECK IF OK TO SCOPE THIS TEST
001434 001407 ;BEQ 2S ;BRANCH IF NOT OK
001436 022767 ;CMP #SCOPTR,MSR ;PUT ADDR OF SCOPE ENTRY INTO STACK
001438 001403 ;BEQ ;GO TO SCOPE ENTRY IN TEST
001440 000002 177164 ;RTI ;CLEAR ERROR IND. IN PRGID
001442 100000 ;BIC #BIT5,PRGID ;CHECK LEVEL
001444 177156 2S: ;TEST ;BRANCH IF LEVEL=0
001446 177162 3S: ;LEVEL ;TEST LOOP SWITCH ON (=1)
001448 000002 ;BEQ 5S ;BRANCH IF NO LOOP TEST
001450 032777 ;RTI ;GO BACK TO TEST
001452 001405 ;BEQ ;DECREMENT TEST ITERATION COUNT
001454 177146 4S: ;ICTR ;GO TO TEST
001456 001407 ;BEQ 0S ;CHECK IF COUNT=0
001458 000002 ;RTI ;NOT ZERO, REPEAT TEST
001460 000002 000400 177170 5S: ;BIT #BIT8,MSR ;TEST IF SEQUENCE TEST (BIT8)
001462 000002 ;BEQ ;BRANCH TO NEXT TEST IF BIT8=0
001464 000002 ;RTI ;WAIT FOR MORE INPUT
001466 000002 000146 6S: ;JMP POPSP2 ;POP 2 OFF STACK
001468 000002 ;RTI ;THIS FORMERLY WAS RESET
001470 000002 177152 CHAINN: ;NOP ;CHECK SR
001472 100003 ;TST ;BRANCH IF NO HALT WANTED
001474 177066 ;RPL ;CURRENT TEST NUMBER TO RO
001476 000002 ;MOVB ;HALT (NOT FOR TEST SELECTION)
001478 177076 1S: ;HALT ;TEST THE CURRENT LEVEL
001480 001420 ;BEQ 3S ;BRANCH IF 0

```

```

17900
18000
18100
18200
18300
18400
18500
18600
18700
18800
18900
19000
19100
19200
19300
19400
19500
19600
19700
19800
19900
20000
20100
20200
20300
20400
20500
20600
20700
20800
20900
21000
21100
21200
21300
21400
21500
21600
21700
21800
21900
22000
22100
22200
22300
22400
22500
001560 012767 000006 176216 ;MOV #6,WACHER ;CLEAN UP
001566 012706 000600 ;MOV #SPROT,SP ;SET UP STACK POINTER
001572 104024 177777 177036 ;FORWD ;SET UP VALUES FOR NEXT TEST
001574 001004 ;CMP #-1,NXTST ;END OF I/O TESTS (=1)
001576 104024 005266 177026 ;BNE ;BRANCH IF NOT END
001578 012767 ;MOV #ATO,NXTST ;TEST TO FIRST I/O TEST
001580 104024 ;FORWD ;SET UP VALUES FOR NEXT TEST
001582 022777 177777 177012 2S: ;JMP #CURTST ;GO TO TEST
001584 001004 ;CMP #-1,NXTST ;END OF I/O TESTS (=1)
001586 000002 000400 177056 SKIP: ;BNE ;BRANCH IF NOT
001588 032777 ;BIT #BIT8,MSR ;TEST IF WANT TEST SELECTION RIGHT AWAY
001590 000200 176776 ;NEXT1 ;BRANCH IF NOT
001592 000372 176764 ;BIS #BIT7,PRGID ;BYPASS SCOPING
001594 000006 176122 NEXT: ;MOV #PTO,NXTST ;BROD TESTING, GO TO PRINTER TESTS
001596 000600 ;MOV #6,WACHER ;CLEAN UP
001598 104024 ;FORWD ;SET UP STACK POINTER
001600 000177 177002 ;JMP #CURTST ;SET UP NEXT TEST PARAMETERS
001602 005267 176754 NEXT1: ;INC LEVEL ;GO TO ROUTINE
19900
20000
20100
20200
20300
20400
20500
20600
20700
20800
20900
21000
21100
21200
21300
21400
21500
21600
21700
21800
21900
22000
22100
22200
22300
22400
22500
001700 104006 000006 176074 WAITF: CHALT ;OR TIVCTL IF START WAS AT 210
001702 012706 000600 ;MOV #6,WACHER ;CLEAN UP
001704 176774 ;MOV #SPROT,SP ;SET UP STACK POINTER
001706 177777 ;MOV #8,RO ;GET CURRENT SW REG
001708 042700 177700 ;BIC #17700,RO
001710 020027 000037 ;CMP RO,#37 ;TEST IF PROC NO. IS I/O TEST
001712 176706 ;BLS ;BRANCH IF EQ OR LT 37. AN ECHO OR PRINTER
001714 000403 ;PRGID ;I/O TEST, CLEAR PRGID
001716 000200 176676 1S: ;BIS #BIT7,PRGID ;BYPASS SCOPING
001718 006100 2S: ;ROL ;CLEAR C BIT
001720 016057 002524 176660 ;RO ;GET PROGRAM ADDRESS OUT OF
001722 176654 001700 ;MOV #PRGTAB(RO),NXTST ;PROGRAM ADDRESS TABLE
001724 000002 ;CMP #NXTST,#WAITF ;TEST IF LEGAL TEST NO.
001726 104024 ;BEQ ;BRANCH IF ILLEGAL
001728 176700 ;FORWD ;SET UP TEST PARAMETERS
001730 000177 ;JMP #CURTST ;GO TO TEST

```



```

32800                                ;TESTC--CHECKS THAT THE INPUTTED CHARACTER IS BETWEEN 0 AND 7 INCLUSIVE
32900                                ;
33000 002460 026727 176214 000060 TESTC: CMP      TEMPCH,#60 ;CHECK IF NUMERIC AND EQ OR GT 0
33100 002466 193061                BHS      IS          ;BRANCH IF OK
33200 002470 000207                RTS      PC          ;ERROR RETURN
33300 002472 026727 176202 000067 1S:  CMP      TEMPCH,#67 ;CHECK IF EQ OR LT 7
33400 002500 191461                RTS      PC          ;BRANCH IF OK
33500 002502 000207                RTS      PC          ;ERROR RETURN
33600 002504 062716 000002 2S:  ADD      #2,OSP ;SET UP RETURN ADDRESS
33700 002510 016700                MOV      TEMPCH,R0 ;GET CHAR
33800 002514 042700                BIC      #177770,R0 ;SAVE ONLY THE DIGIT
33900 002520 000207                RTS      PC          ;NORMAL RETURN
    
```

```

34100 002522 007372                PRGTAB: PTO ;DATA PATH TEST
34200 002524 007372                PT1 ;PRINTER CHARACTER TEST
34300 002526 007570                PT2 ;NON-PRINTING CHARACTER TEST
34400 002530 010164                PT3 ;CARRIAGE RETURN TEST
34500 002532 010304                PT4 ;MULTIPLE LINE FEED TEST
34600 002534 010462                PT5 ;SINGLE LINE FEED TEST
34700 002536 010666                PT6 ;STICKSPACE TEST
34800 002540 011054                PT7 ;OVERPRINT TEST
34900 002542 011266                PT10 ;PRINTING FREQUENCY SWEEP TEST
35000 002544 011474                PT11 ;RIBBON FEED TEST
35100 002546 011456                PT12 ;PRINTER BELL TEST
35200 002550 001700                WAITF ;SPARE
35300 002552 001700                WAITF ;SPARE
35400 002554 001700                WAITF ;SPARE
35500 002556 001700                WAITF ;SPARE
35600 002560 011546                PT17 ;LIFE TEST
35700 002562 012116                EO20 ;CHARACTER ECHO TEST
35800 002564 012166                EO21 ;LINE ECHO TEST, FAST RATE
35900 002566 012254                EO22 ;LINE ECHO TEST, SLOW RATE
36000 002570 012476                EO23 ;CHARACTER/CODE ECHO TEST
36100 002572 013020                EO24 ;SELECTIVE PATTERN ECHO TEST
36200 002574 013566                EO25 ;BELL ECHO TEST
36300 002576 001700                WAITF ;SPARE
36400 002600 001700                WAITF ;SPARE
36500 002602 001700                WAITF ;SPARE
36600 002604 001700                WAITF ;SPARE
36700 002606 001700                WAITF ;SPARE
36800 002610 001700                WAITF ;SPARE
36900 002612 001700                WAITF ;SPARE
37000 002614 001700                WAITF ;SPARE
37100 002616 001700                WAITF ;SPARE
37200 002620 001700                WAITF ;SPARE
37300 002622 005256                AT0 ;I/O TEST NO. 40
37400 002624 005352                AT1 ;I/O TEST NO. 41
37500 002626 005352                AT2 ;I/O TEST NO. 42
37600 002630 005404                AT3 ;I/O TEST NO. 43
37700 002632 005436                AT4 ;I/O TEST NO. 44
37800 002634 005526                AT5 ;I/O TEST NO. 45
37900 002636 005664                AT6 ;I/O TEST NO. 46
38000 002640 005674                AT7 ;I/O TEST NO. 47
38100 002642 005744                AT10 ;I/O TEST NO. 50
38200 002644 006002                AT11 ;I/O TEST NO. 51
38300 002646 006042                AT12 ;I/O TEST NO. 52
38400 002650 006116                AT13 ;I/O TEST NO. 53
38500 002652 006176                AT14 ;I/O TEST NO. 54
38600 002654 006252                AT15 ;I/O TEST NO. 55
38700 002656 006362                AT16 ;I/O TEST NO. 56
38800 002660 006430                AT17 ;I/O TEST NO. 57
38900 002662 006500                AT20 ;I/O TEST NO. 60
39000 002664 006572                AT21 ;I/O TEST NO. 61
39100 002666 006672                AT23 ;I/O TEST NO. 63
39200 002670 007000                AT25 ;I/O TEST NO. 65
39300 002672 007112                AT24 ;LSI TEST NO. 64
39400 002674 007212                AT25 ;LSI TEST NO. 65
39500 002676 007370                AT26 ;LSI TEST NO. 66
39600 002700 001700                WAITF ;SPARE
39700 002702 001700                WAITF ;SPARE
    
```

```

39800 002704 001700          WAITF          ;SPARE
39900 002710 001700          WAITF          ;SPARE
40000 002710 001700          WAITF          ;SPARE
40100 002712 001700          WAITF          ;SPARE
40200 002714 001700          WAITF          ;SPARE
40300 002716 001700          WAITF          ;SPARE
40400 002720 001700          WAITF          ;SPARE
40500
40600
40700
40800
40900
41000
41100 002722 011646          ;*****
41200 002724 162716          ;EMTINT -----SERVICE ROUTINE FOR TRAPS THROUGH
41300 002730 017616          ;*****
41400 002734 121627          ;*****
41500 002740 011402          ;*****
41600 002742 000000          ;*****
41700 002744 000776          ;*****
41800 002746 000776          ;*****
41900 002750 004112          ;*****
42000 002754 062716          ;*****
42100 002760 017616          ;*****
42200 002764 005046          ;*****
42300 002766 000000          ;*****
42400 002768 000000          ;*****
42500 002774 000136          ;*****
42600
42700
42800 002776 003076          ;*****
42900 002778 003320          ;*****
43000 003002 003346          ;*****
43100 003004 003356          ;*****
43200 003006 003366          ;*****
43300 003010 001412          ;*****
43400 003012 000720          ;*****
43500 003014 003164          ;*****
43600 003016 003436          ;*****
43700 003022 003214          ;*****
43800 003024 003142          ;*****
43900 003026 003216          ;*****
44000 003030 004524          ;*****
44100 003032 003236          ;*****
44200 003034 004112          ;*****
44300 003036 004112          ;*****
44400 003040 003640          ;*****
44500 003042 003226          ;*****
44600 003044 004006          ;*****
44700 003046 003562          ;*****
44800 003050 004204          ;*****
44900 003052 003072          ;*****
45000 003054 003072          ;*****
45100 003056 003072          ;*****
45200 003060 003072          ;*****
45300 003062 003072          ;*****
45400 003064 003072          ;*****

```

```

45500 003066 003072          SPARE          ;SPARE EMT
45600 003072 000000          SPARE          ;SPARE EMT
45700 003074 000776          SPARE: HALT      ;HALT IF TRAP TO UNDEFINED
45800                                     BR          ;EMT IS ATTEMPTED.
45900
46000
46100
46200
46300
46400
46500
46600
46700
46800
46900
47000
47100
47200
47300
47400
47500
47600
47700
47800
47900
48000
48100 003076 010046          ;*****
48200 003100 016601          ;*****
48300 003104 062766          ;*****
48400 003114 011100          ;*****
48500 003116 100403          ;*****
48600 003120 001004          ;*****
48700 003122 012600          ;*****
48800 003124 000002          ;*****
48900 003126 104013          ;*****
49000 003130 000771          ;*****
49100 003132 104017          ;*****
49200 003134 110077          ;*****
49300 003140 000765          ;*****
49400
49500
49600 003142 104017          ;*****
49700 003144 112777          ;*****
49800 003152 104017          ;*****
49900 003154 112777          ;*****
50000 003162 000002          ;*****

```

```

50200 ;XXXXXXXXXX
50300 ;
50400 ;TYPM---MULTI TYPE-A COMMON ROUTINE TO OUTPUT
50500 ; A MESSAGE ON ALL DL11S IF THE MULTI TEST
50600 ; SWITCH (BIT 13) IS RESET. THIS ROUTINE IS USED BY
50700 ; THE PRINTER TESTS TO TYPE HEADINGS IF A UNIT
50800 ; IS NOT READY, THE CHARACTER WILL NOT BE TYPED.
50900 ;XXXXXXXXXX
51000 ;
51100 003164 011601 000002 TYPM: MOV (SP),R1 ;GET POINTER TO ADDR OF MESC
51200 003166 062716 ADD #2,R1 ;GET CHAR
51300 003172 011101 MOV (R1),R1 ;ADDR OF MESC TO R1
51400 003174 112100 MOVB (R1)+,R0 ;GET CHAR
51500 003176 100402 BMT 2,S ;BRANCH IF WANT AUTO CR-LF
51600 003200 001003 BNE 3,S ;CONTINUE IF NOT NULL
51700 003202 000000 RTI ;RETURN
51800 003204 104015 CRLF ;YES SEND CR-LF
51900 003206 000772 BR 1,S ;SET CHAR
52000 003210 104015 PRINTC ;PRINT CHAR
52100 003212 000770 BR 1,S ;GO GET NEXT CHAR.
52200 ;
52300 003214 104022 $CRLF: CR ;SEND CR
52400 003216 012700 $LF: MOV #12,R0 ;SET LF CHAR
52500 003222 104015 PRINTC ;SEND IT
52600 003224 000002 RTI ;RETURN TO CALLER
52700 ;
52800 003226 012700 000015 $CR: MOV #15,R0 ;SET CR CHAR
52900 003232 104015 PRINTC ;SEND IT
53000 003234 000002 RTI ;RETURN
53100 ;
53200 ;*****
53300 ;ROUTINE TO PRINT TEST HEADER
53400 ;*****
53500 ;
53600 003236 012700 000000 $PRHDR: MOV #0,R0 ;TRANSMIT
53700 003242 104015 PRINTC ;NULL CODE
53800 003244 104007 TYPMSG ;PRINT MESSAGE
53900 003246 014110 HDMMSG ;
54000 003254 006200 RTNNO,R0 ;GET TEST NUMBER
54100 003256 006200 ASR ;GET FIRST DIGIT
54200 003258 006200 RO ;
54300 003260 006200 ASR ;
54400 003262 006200 RO ;
54500 003264 177770 BIT #17770,R0 ;MASK FIRST DIGIT
54600 003266 062700 ADD #60,R0 ;MAKE ASCII
54700 003272 104015 PRINTC ;PRINT DIGIT
54800 003274 016700 MOV RTNNO,R0 ;GET TEST NUMBER AGAIN
54900 003276 177770 BIT #17770,R0 ;MASK LAST DIGIT
55000 003278 042700 BIC #777,R0 ;MAKE SET
55100 003300 062700 ADD #60,R0 ;MAKE ASCII
55200 003302 104015 PRINTC ;PRINT DIGIT
55300 003304 016700 MOV RTNNO,R0 ;GET TEST NUMBER AGAIN
55400 003306 177770 BIC #777,R0 ;MAKE SET
55500 003308 104015 PRINTC ;PRINT DIGIT
55600 003310 104015 CRLF ;CR-LF
55700 003312 104014 LF ;BLANK LINE
55800 003314 104014 RTI ;RETURN
55900 003316 000002
    
```

```

55800 ;*****
55900 ;ERRA-- COMMON ERROR RETURN FROM I/O TESTS. HALTS
56000 ; WITH ADDRESS OF ERROR IN R0. TO CONTINUE
56100 ; ON SAME TEST BIT NOT HALTING ON ERROR
56200 ; SET THE SCOPE BIT (14) = 1 AND PRESS CONTINUE
56300 ;*****
56400 ;
56500 003320 032777 040000 175366 ERR: BIT #SCOPSW,@SR ;CHECK SCOPE SWITCH
56600 003322 001404 BEQ 1,S ;BRANCH IF NO SCOPE
56700 003330 005767 TST PRGID ;SCOPING WANTED, FIRST ERROR?
56800 003332 100001 BPL 1,S ;BRANCH AND HALT ON FIRST ERROR
56900 003334 100001 BPL 1,S ;SCOPING WANTED, FIRST ERROR?
57000 003336 100001 RTI ;SCOPE EXIT
57100 003340 052767 100000 175276 $S: BIS #BIT15,PRCID ;SET ERROR INDICATOR
57200 003342 011600 EHLT: MOV @SP,R0 ;ADDRESS OF CALL INTO R0
57300 003344 005740 TST -(R0) ;
57400 003352 000000 HALT ;
57500 003354 000002 ERRHLT: RTI ;RETURN TO TEST FOLLOWING CALL
57600 ;
57700 ;*****
57800 ;
57900 ;$STLSPV--- THIS ROUTINE SETS UP KEYBOARD INTERRUPT
58000 ; VECTOR AND PRIORITY. CALLING SEQUENCE
58100 ;
58200 ;
58300 ; STRDRV ;LOCATION OF NEW INTERRUPT VECTOR
58400 ; AT20C
58500 ;*****
58600 ;
58700 003356 017667 000000 000012 $STLSRV: MOV @SP,STPRA+2 ;SET RETURN ADR AND VECTOR
58800 003364 062716 ADD #2,ASP ;
58900 003370 016701 175226 MOV TR4,R1 ;
59000 003374 012721 000000 STPRA: MOV #0,(R1)+ ;
59100 003400 016721 175220 MOV TR4,R1 ;
59200 003404 000002 RTI ;
59300 ;
59400 ;*****
59500 ;
59600 ;$STLSPV-- THIS ROUTINE SETS UP PRINTER INTERRUPT
59700 ; VECTOR AND PRIORITY CALLING SEQUENCE
59800 ;
59900 ;
60000 ; STPCHV ;LOCATION OF NEW INTERRUPT VECTOR
60100 ; AT35E
60200 ;*****
60300 ;
60400 003406 017667 000000 000012 $STLSPV: MOV @SP,STPPA+2 ;SET RETURN ADR AND VECTOR
60500 003414 062716 ADD #2,ASP ;
60600 003420 016701 175202 MOV TR4,R1 ;
60700 003424 012721 000000 STPPA: MOV #0,(R1)+ ;
60800 003430 016721 175174 MOV TR4,R1 ;
60900 003434 000002 RTI ;RETURN TO CALLER
    
```

61200  
 61300  
 61400  
 61500  
 61600  
 61700  
 61800  
 61900  
 62000  
 62100  
 62200  
 62300  
 62400  
 62500  
 62600  
 62700  
 62800  
 62900  
 63000  
 63100  
 63200  
 63300  
 63400  
 63500  
 63600  
 63700  
 63800  
 63900  
 64000 003436 010146  
 64100 003440 016701  
 64200 003444 005301 175226  
 64300 003446 001376  
 64400 003450 005300  
 64500 003452 011372  
 64600 003454 011601  
 64700 003456 000002

```

*****
DELAY--A COMMON ROUTINE TO DELAY PROCESSING
A GIVEN NUMBER OF MSEC.
CALLING SEQUENCE:
MOV #5,R0 ;R0 CONTAINS THE NUMBER OF MSEC DELAY DESIRED
DELAY
THE DELAY IS EFFECTED BY THE EXECUTION OF THE LOOP;
IS: DEC R1
BNE IS

SINCE THE EXECUTION TIMES OF THE POP11 LINE DOES VARY FROM
MACHINE TO MACHINE, THE VALUE AT SYMBOLIC LOCATION
"TIMER" MUST BE CHANGED TO THE APPROPRIATE VALUE AS SHOWN BELOW
BEFORE STARTING THE DIAGNOSTIC. "TIMER" IS INITIALIZED
FOR AN 11/05,11/10(=251).
MACHINE 05&10 35&40 15&20 LSI&03 BIPOLAR 11/45 & 11/70 CORE
MOS
LOOP: DEC R1 3.4 1.99 2.3 -30 -51 -90
BNE LOOP 2.5 1.76 2.8 -60 -98 1.13
TIME= 5.9USEC 2.75 4.9 7.7 .90USEC 1.49USEC 2.03USEC
SET TIMER 251 554 314 202 2127 1237 755
XXXXXXXXXX
DLY: MOV R1,-(SP) ;SAVE R1
IS: MOV TIMER,R1 ;MOV 1 MSEC LOOP CNT TO R1
DS: DEC R1 ;DECREMENT COUNT
BNE DS ;BRANCH IF NOT ZERO
DEC R0 ;DEC NO. OF MSEC DELAY
BNE IS ;DELAY AGAIN IF NOT ZERO
MOV (SP)+,R1 ;ALL DONE RESTORE R1
RTI
    
```

64900  
 65000  
 65100  
 65200  
 65300  
 65400  
 65500

```

*****
PFail--POWER FAIL ROUTINE
SAVE ALL REGISTERS AND SET RESTART ADDRESS
INTO LOCATION 24
RESTART--POWER FAIL RECOVERY
    
```

100 ; RESTORE ALL REGISTERS AND GO TO START

```

200 ;*****
300
400 003460 010946 PFAIL: MOV R0,-(SP)
500 003462 010146 MOV R1,-(SP)
600 003464 010246 MOV R2,-(SP)
700 003466 010346 MOV R3,-(SP)
800 003470 010446 MOV R4,-(SP)
900 003472 010546 MOV R5,-(SP)
1000 003474 016748 MOV R6,-(SP)
1100 003500 010667 MOV SP,SAVR6 ;SAVE STACK POSITION
1200 003504 012767 MOV #RESTRT,24 ;STORE RESTART ADDRESS
1300 003512 000900 HALT
1400 003514 000000 SAVR6: .WORD 0
1500 003516 104007 RESTRT: .TYPEM
1600 003520 003552 1S
1700 003522 016706 MOV SAVR6,SP ;RESTORE STACK POINTER
1800 003526 012667 MOV (SP),R4 ;RESTORE PFAIL ADDRESS
1900 003532 012605 MOV (SP),R5
2000 003534 012604 MOV (SP),R4
2100 003536 012603 MOV (SP),R3
2200 003540 012602 MOV (SP),R2
2300 003542 012601 MOV (SP),R1
2400 003544 012600 MOV (SP),R0
2500 003546 000167 JMP START
2700 003552 200 120 117 1S: .ASCIZ <ACRLF>/POWER/<ACRLF>
003555 127 105 122
003560 200 000
2800 .EVEN
    
```





```

10600 ;*****
10700 ;
10800 ;BINARY TO ASCII CONVERSION (1 TO 5 ASCII CHARACTERS)
10900 ;CALLING SEQUENCE
11000 ;
11100 ;MOV ADDRESS OF LOC. TO STORE FIRST ASCII CHAR. INTO R0
11200 ;MOV BINARY NUMBER TO BE CONVERTED INTO R1
11300 ;MOV NUMBER TO BE CONVERTED AS A POWER OF TEN INTO R2
11400 ;
11500 ;*****
11600 004006 010267 000060 SBTASC: MOV R2,CNVCTR ;SAVE TEN POWER
11700 004015 006672 ;
11800 004014 062702 004100 ADD #ADTENP,R2 ;CALCULATE ADDRESS OF
11900 ;
12000 004020 014267 000052 1S: CLR -(R2),TENPWR ;STARTING TEN POWER
12100 004024 005067 000044 MOV DIGIT,TENPWR ;POWER OF TEN VALUE TO TEN PWR
12200 004030 166701 000042 2S: SUB TENPWR,R1 ;CLEAR CURRENT DIGIT
12300 004034 103403 ;SUBTRACT TEN POWER FROM BINARY VALUE
12400 004035 005267 3S: BCS 3S ;BRANCH IF END
12500 004035 005267 BR DIGIT ;
12600 004044 066701 000026 ADD TENPWR,R1 ;RESTORE SUBTRACTED VALUE
12700 004050 062767 000016 ADD #60,DIGIT ;CONVERT (DIGIT) TO ASCII
12800 004052 065267 000060 MOV#R DIGIT,(R0)+ ;PUT ASCII CHAR INTO USER BUFFER
12900 004053 065267 000004 DEC CNVCTR ;FINISHED ALL CHARS. CALLED FOR
13000 004056 001354 BNE 1S ;BRANCH IF NOT FINISHED
13100 004070 000002 RTI ;YES, EXIT
13200 004070 000002 ;
13300 004074 000000 CNVCTR: .WORD 0 ;CONVERSION CHARACTER COUNT
13400 004076 000000 DIGIT: .WORD 0 ;CONVERTED CHARACTER
13500 004076 000000 TENPWR: .WORD 0 ;CURRENT TEN POWER
13600 004106 000001 000012 000144 ADTENP: .WORD 1.,10.,100.,1000.,10000.
13600 004106 001750 023420 ;

```

```

13800 ;XXXXXXXXXX
13900 ;
14000 ;READ-- A COMMON ROUTINE WHICH CHECKS THE KEYBOARD
14100 ;DONE FLAG & SETS A FLAG INDICATING CHAR PARITY
14200 ;
14300 ;
14400 ;XXXXXXXXXX
14500 004112 004767 177572 SREAD: JSR PC,CONIT ;RESET CONSOLE ADR AND VECTORS
14600 004116 005767 174534 DLENT TST ;CHECK IF MULTI DL11'S AVAILABLE
14700 004122 016730 174526 174534 1S: BEQ SREADC ;NONE, WAIT FOR CONSOLE INPUT
14800 004132 016767 174474 174530 MOV COUNT,COUNT3 ;SET DL11 COUNT
14900 004140 105777 174524 2S: FTDL,XCSR ;ADDRESS OF FIRST DL11 INTO XCSR
15000 004144 106000 ;TEST IF ANY INPUT
15100 004146 016700 174516 BPL 3S ;CONTINUE IF NO INPUT
15200 004152 004767 177536 JSR PC,CONSET ;SET THIS DL11 AS CONSOLE
15300 004156 000415 ;
15400 004160 005367 174502 3S: BR READ1 ;READ CHAR AND RETURN
15500 004164 001304 DEC COUNT3 ;DECREMENT DL11 COUNT
15600 004166 062767 000010 174474 ADD #0,XCSR ;TEST CONSOLE WHEN DONE DL11'S
15700 004174 000767 174410 4S: BR 4S ;NEXT DL11 ADDRESS
15800 004202 103550 174402 TSTB #0,XCSR ;CONTINUE
15900 004204 105777 174402 SREADC: TSTR #TKS ;CHECK CONSOLE
16000 004210 103375 BPL SREADC ;WAIT, NO INPUT
16100 004212 116767 174376 174460 READ1: MOVB #TKB,TEMPCH ;CHECK KEYBOARD DONE FLAG
16200 004220 042767 174454 174456 MOVB #7740,PCHAR ;BRANCH IF NOT SET
16300 004226 116767 174440 174441 BIC #TEMPCH,PARITY+1 ;SAVE CHARACTER
16400 004234 042767 177600 174430 MOVB #177600,TEMPCH ;SAVE CODE WITH PARITY BIT
16500 004252 027277 174424 000004 CMP #TEMPCH,#4 ;MASK UNWANTED BITS
16600 004256 001715 BEQ SREAD ;SAVE CHAR WITH PARITY BIT
16700 004260 012700 000011 MOV #11,R0 ;MAKE IT 7 BIT ASCII
16800 004264 042767 000377 174410 1S: BIC #77,PARITY ;DISREGARD EOT
16900 004272 005360 ;
17000 004274 001406 BEQ SREAD ;SET SHIFT COUNT
17100 004276 106367 174401 DEC RO ;CLEAR PARITY FLAG
17200 004304 103373 174372 2S: ASLB #PARITY+1 ;DECREMENT SHIFT COUNT
17300 004310 006770 BCC 1S ;EXIT IF DONE
17400 004312 000002 BR PARITY ;CONTINUE IF BIT WAS ZERO
17500 ;CHANGE PARITY FLAG IF BIT WAS ONE
17600 ;CONTINUE
17700 ;SET, RET. TO CALLER
17800 ;
17900 ;XXXXXXXXXX
18000 ;
18100 ;PRINT-- A COMMON ROUTINE TO CHECK THE PRINTER READY FLAG
18200 ;
18300 ;
18400 ;XXXXXXXXXX
18500 ;
18600 004314 105777 174276 SPRNT: TSTB #TPS ;CHECK PRINTER READY FLAG
18700 004320 100375 BPL SPRNT ;BRANCH IF NOT SET
18800 004322 000002 RTI ;SET, RETURN

```

```

19000
19100
19200
19300
19400
19500
19600
19700
19800
19900
20000
20100 004324 016767 174252 174360 $PRTC: CONADD,TEMP ;SET CONSOLE ADR
20200 004332 062767 000004 174352 1S: ADD #4,TEMP
20300 004340 105777 174346 BPT #TEMP
20400 004344 100165 BPL 1S ;WAIT FOR CONSOLE READY
20500 004346 062767 000002 174336 ADD #2,TEMP ;SET ADR
20600 004354 010077 174332 MOV R0,ATEMP ;LOAD CONSOLE PRINTER BUFFER
20700 004360 032777 020000 174326 BIT #BIT13,RSR ;CHECK SW 13
20800 004366 061003 BNE 2S ;SEND ALL TERMS IF SW13 DOWN
20900 004370 005767 174262 TST DLCONT ;CHECK IF MULTIPLE DL11'S
21000 004374 001002 BNE 3S ;CHECK FOR INPUT IF THERE
21100 004376 000167 000432 JMP 18S
21200 004402 016767 174250 174256 2S: MOV DLCONT,COUNT3 ;PUT NO. DL11'S INTO COUNT3
21300 004410 016767 174216 174252 3S: MOV FSRDL,XCSR ;ADDR OF FIRST DL INTO XCSR
21400 004416 005767 174266 4S: INCX #XCSR ;CHECK FOR INPUT?
21500 004422 001140 BNE 13S
21600 004424 026077 174206 000020 CMP RTNNO,#20 ;PRINTING TEST?
21700 004432 002004 BNE 5S ;BRANCH IF NOT
21800 004434 032767 104011 175236 CMP #TVCTL,WAITF ;KEYBOARD CONTROL?
21900 004442 001130 BNE 13S ;SKIP INPUT CHECK IF NOT
22000 004444 105777 174220 TSTR #XCSR ;TEST IF ANY INPUT
22100 004452 062767 000002 174210 ADD #2,XCSR ;CONTINUE IF NO INPUT
22200 004460 017767 174204 174212 MOV #XCSR,TEMPCH ;SET BUFFER ADDRESS
22300 004466 032757 174200 000003 BIC #17600,TEMPCH
22400 004474 001006 BNE 6S ;CHECK IF CONTROL-C
22500 004502 026727 174126 000024 CMP RTNNO,#24 ;CONTINUE IF NOT
22600 004512 061002 JMP 6S ;CHECK IF TEST 24
22700 004520 026727 000420 000177 6S: JMP #TEMPCH,#177 ;CONTINUE IF NOT CONTROL-C
22800 004526 001427 BEQ 9S ;CHECK IF RUBOUT
22900 004530 026727 174102 000017 CMP RTNNO,#17 ;YES, CHECK TEST NUMBER
23000 004534 001003 BNE 7S ;TEST 17?
23100 004540 016703 174134 MOV TEMPCH,R3 ;BRANCH IF NOT
23200 004544 000461 BR 12S ;SAME CHARACTER
23300 004546 026727 174064 000021 7S: CMP RTNNO,#21 ;CONTINUE
23400 004554 016767 174116 174076 MOV TEMPCH,REPT ;BRANCH IF NOT
23500 004564 000451 BR 12S ;SAME CHARACTER
23600 004566 026727 174044 000022 8S: CMP RTNNO,#22 ;CONTINUE
23700 004574 016767 174076 174056 MOV TEMPCH,REPT ;BRANCH IF NOT
23800 004604 000441 BR 12S ;SAME CHARACTER
23900 004606 026727 174024 000021 9S: CMP RTNNO,#21 ;CHECK IF TEST 21
24000 004614 001002 BNE 10S ;NO, CHECK IF TEST 22
24100 004616 022826 POPSP2 ;ADJUST STACK

```

```

24700 004620 012700 000036 MOV #30.,R0 ;DELAY FOR HALF DUPLEX
24800 004626 104007 DELAY 10S
24900 004630 014272 TVSPW ;YES, TEST 21
25000 004632 104005 ECDEND ;PRINT TERMINATION MESSAGE
25100 004634 000167 CHAIN ;CHAIN TO NEXT TEST
25200 004636 000167 095334 000022 10S: JMP E021A ;REPEAT TEST IF LOOP ON TEST SW SET
25300 004640 000167 173772 000022 10S: MOV RTNNO,#22 ;CHECK IF TEST 22
25400 004646 000167 BNE 11S ;SAME CHARACTER
25500 004650 022826 POPSP2 ;ADJUST STACK
25600 004654 104007 MOV #30.,R0 ;DELAY FOR HALF DUPLEX
25700 004656 104007 DELAY 10S
25800 004660 104007 TVSPW ;YES, PRINT TERMINATION MESSAGE
25900 004662 014272 ECDEND
26000 004664 000167 CHAIN
26100 004666 000167 005340 000024 11S: JMP E022A ;CHAIN TO NEXT TEST
26200 004672 026727 173740 000024 11S: CMP RTNNO,#24 ;REPEAT TEST IF LOOP ON TEST SW SET
26300 004700 001133 BNE 22S ;TEST 24?
26400 004702 072829 POPSP2 ;WAIT FOR NEXT TEST IF NOT TEST 24
26500 004704 000167 006244 000036 12S: MOV TERM ;RESET STACK
26600 004710 012700 000036 12S: MOV #30.,R0 ;TERMINATE TEST
26700 004714 104010 DELAY 10S ;DELAY FOR HALF DUPLEX
26800 004716 000167 173756 MOV TEMPCH,R0 ;SET NEW CHARACTER
26900 004722 000167 BPT 14S ;CONTINUE
27000 004724 062767 000002 173736 13S: ADD #2,XCSR ;SET STATUS ADDRESS IN XCSR
27100 004732 062767 000002 173730 14S: ADD #2,XCSR
27200 004740 015767 173536 173744 MOV CONADD,TEMP ;CHECK IF CONSOLE TERMINAL
27300 004746 062767 000004 173736 ADD #4,TEMP ;IS THIS DL
27400 004754 026767 173732 173706 CMP TEMP,XCSR
27500 004762 001420 BEQ 17S
27600 004764 105172 173700 TSTR #XCSR ;TEST PRINTER READY
27700 004766 000167 000002 173670 15S: BPT 18S ;WAIT FOR READY
27800 004772 062767 000002 173670 15S: ADD #2,XCSR ;SET XCSR TO PRINTER BUFFER
27900 005000 010077 173664 MOV R0,#XCSR ;LOAD CHARACTER INTO BUFFER
28000 005004 003167 173656 DEC COUNT3 ;DECREASE COUNT OF DL11'S
28100 005010 003167 BEQ 18S ;ALL DONE, EXIT
28200 005012 062767 000002 173650 16S: ADD #2,XCSR ;GO TEST NEXT DL11 READY FLAG
28300 005020 000167 173772 173636 17S: JMP 4S ;SET XCSR TO PRINTER BUFFER
28400 005022 062767 000002 173636 17S: ADD #2,XCSR ;SET XCSR TO PRINTER BUFFER
28500 005034 005767 173650 000020 18S: TST 18S ;DO NOT LOAD BUFFER
28600 005040 001141 BNE 26S ;NO, BRANCH
28700 005042 022004 173570 000020 CMP RTNNO,#20 ;PRINTING TEST?
28800 005050 002004 BNE 19S ;BRANCH IF NOT
28900 005052 022767 104011 174620 CMP #TVCTL,WAITF ;KEYBOARD CONTROL?
29000 005060 001101 BNE 26S ;SKIP INPUT CHECK IF NOT
29100 005066 100076 173514 19S: TSTR #CONADD ;TEST IF ANY INPUT
29200 005070 016767 173506 173614 BPL #TEMP ;BRANCH IF NONE
29300 005076 062767 000002 173606 19S: MOV CONADD,TEMP ;SET ADR
29400 005104 112767 173602 173566 MOV #TEMP,TEMPCH
29500 005112 042767 173500 173560 BIC #17600,TEMPCH ;MASK UNWANTED BITS
29600 005120 026727 173594 000003 BNE 21S ;CHARACTER = CONTROL-C?
29700 005126 001113 173502 000024 21S: CMP RTNNO,#24 ;TEST 24?
29800 005130 026727 173502 000024 21S: BNE 21S ;CONTINUE IF NOT
29900 005140 012700 000036 20S: MOV #30.,R0 ;DELAY FOR HALF DUPLEX
30000 005144 104010 DELAY 10S

```

30400	005146	104012				CRLF			;SEND CR-LF
30500	005150	022626				POPSP2			;RESET STACK
30600	005152	000167	005650			JMP	EO248		;RETURN TO TEST
30700	005156	026727	173516	000177	21S:	CMP	TEMPCH,#177		;CHECK IF RUBOUT
30800	005164	001006				SNE	23S		;BRANCH IF NO
30900	005166	000607				BR	0S		
31000	005170	012767	000001	173436	22S:	MOV	#1,CNTLSW		;CLEAR LOOP AND SEQUENCE BITS
31100	005176	000167	174660			JMP	#VIB		;GO HALT FOR NEXT TEST
31200	005102	010086			23S:	MOV	R0-(SP)		;SAVE R0
31300	005204	012700	000036			MOV	#30,R0		;DELAY FOR HALF DUPLEX
31400	005210	104010				DELAY			
31500	005212	012900				MOV	(SP)+,R0		;RESTORE R0
31600	005214	012900	173416	000017		CMP	R1NO,#17		;CHECK IF TEST 17
31700	005222	001002				SNE	24S		;BRANCH IF NOT TEST 17
31800	005224	016703	173450			MOV	TEMPCH,R3		;STORE INPUTTED CHARACTER
31900	005230	026727	173402	000021	24S:	CMP	R1NO,#21		;CHECK IF TEST 21
32000	005236	001003				SNE	25S		;BRANCH IF NOT TEST 21
32100	005240	016767	173434	173414		MOV	TEMPCH,REPT		;STORE INPUTTED CHARACTER
32200	005246	026727	173364	000022	25S:	CMP	R1NO,#22		;CHECK IF TEST 22
32300	005254	001003				SNE	26S		;BRANCH IF NOT TEST 22
32400	005256	016767	173416	173376	26S:	MOV	TEMPCH,REPT		;STORE INPUTTED CHARACTER
32500	005264	000002				RTI			;RETURN TO TEST
32600									

32800

```

I/O LOGIC TESTS
. SBTTL I/O LOGIC TESTS
;*****
; ONLY THE CONSOLE TERMINAL IS TESTED.
; UPON COMPLETION, THE CPU WILL EITHER HALT IF SR
; BIT8 IS - 1 AND AWAIT FURTHER INSTRUCTIONS OR CONTINUE
; AND EXECUTE THE PRINTER TESTS CONTINUOUSLY
; IF AN I/O TEST FAILS, THE CPU WILL HALT AT ERRHLT
; WITH THE ADDRESS OF THE ERROR IN RO (LOC 77700). PRESSING
; THE CONTINUE SWITCH WILL CAUSE THE I/O TEST TO
; CONTINUE WITH THE NEXT TEST. HOWEVER IF SWITCH 14
; WERE SET, OR IS SET BEFORE THE CONTINUE SWITCH IS
; PRESSED, THE FAILED TEST WILL LOOP ON ITSELF
; WITHOUT FURTHER HALTS
;*****
; AT0-- TEST #40--TESTS THE ABILITY TO REFERENCE THE
; RECEIVER STATUS WORD (TKS) WITHOUT TRAPPING.
;*****
AT0: 40 ;TEST NUMBER
ATOK: AT1 ;NEXT TEST
10. ;ITERATION COUNT
1S ;SCOPE ENTRY
MOV #3S, MACHERR ;SET UP MACHINE ERROR TRAP
TST @TKS ;REFERENCE RECEIVER STATUS WORD
2S: CHAIN @TKS ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
3S: ERROR 2S ;TRAPPED WHEN REFERENCING
; RECEIVER STATUS WORD (TKS)
;*****
; AT1--TEST #41--TESTS THE ABILITY TO REFERENCE THE
; RECEIVER BUFFER (TKB) WITHOUT TRAPPING.
;*****
AT1: 41 ;TEST NUMBER
AT2 ;NEXT TEST
10. ;ITERATION COUNT
1S ;SCOPE ENTRY
MOV #3S, MACHERR ;SET UP MACHINE ERROR TRAP
TST @TKB ;REFERENCE RECEIVER BUFFER
2S: CHAIN @TKB ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
3S: ERROR 2S ;TRAPPED WHEN REFERENCING
; RECEIVER BUFFER (TKB)

```

```

I/O LOGIC TESTS
;*****
; AT2--TEST #42--TESTS THE ABILITY TO REFERENCE THE
; TRANSMITTER STATUS WORD (TPS) WITHOUT TRAPPING.
;*****
AT2: 42 ;TEST NUMBER
AT3 ;NEXT TEST
10. ;ITERATION COUNT
1S ;SCOPE ENTRY
MOV #3S, MACHERR ;SET UP MACHINE ERROR TRAP
TST @TPS ;REFERENCE TRANSMITTER STATUS WORD
2S: CHAIN @TPS ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
3S: ERROR 2S ;TRAPPED WHEN REFERENCING
; TRANSMITTER STATUS WORD
;*****
; AT3-- TEST #43--TESTS THE ABILITY TO REFERENCE THE
; TRANSMITTER BUFFER (TPB) WITHOUT TRAPPING.
;*****
AT3: 43 ;TEST NUMBER
AT4 ;NEXT TEST
10. ;ITERATION COUNT
1S ;SCOPE ENTRY
MOV #3S, MACHERR ;SET UP ERROR TRAP
TST @TPB ;REFERENCE TRANSMITTER BUFFER
2S: CHAIN @TPB ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
3S: ERROR 2S ;TRAPPED WHEN REFERENCING
; TRANSMITTER BUFFER.

```

```

*****
;AT4-- TEST #44--TESTS THE ABILITY TO SET AND CLEAR THE
;RECEIVER INTERRUPT ENABLE BIT.
*****
      8100
      8200
      8300
      8400
      8500
      8600 005436 000044
      8700 005440 005526
      8800 005442 000012
      8900 005444 005460
      9000 005446 012746 000340
      9100 005452 012746 005460
      9200 005456 052777
      9300 005460 052777 000100 173124
      9400 005466 032777 000100 173116 1S:
      9500 005474 001002
      9600 005476 104001
      9700 005500 000410
      9800 005502 042777 000100 173102
      9900 005510 032777 000100 173074 3S:
      1000 005516 001401
      1010 005520 104001
      1020 005522 104005
      1030 005524 000755
      1040
      1050
      1060
      1070
      1080
      1090
      1100 005526 000045
      1110 005530 005604
      1120 005532 060112
      1130 005534 005550
      1140 005536 012746 000340
      1150 005542 012746 005550
      1160 005546 052777
      1170 005550 052777 000100 173034 1S:
      1180 005556 052777 173034 3S:
      1190 005562 001775
      1200 005564 000005
      1210 005566 000005
      1220 005574 001401 000100 173016 2S:
      1230 005576 104001
      1240 005600 104005
      1250 005602 000762

*****
;AT5-- TEST #45--CHECKS THAT THE RECEIVER INTERRUPT
;ENABLE BIT CAN BE CLEARED WITH RESET INSTRUCTION.
*****
      AT5: 45
           AT6
           10.
           IS
           MOV #PRTV7,-(SP)
           MOV #1,-(SP)
           RTS
           BIT #BIT6,@TKS
           BIT #BIT6,@TKS
           BNE 3S
           ERROR 5S
           BIC #BIT6,@TKS
           BIT #BIT6,@TKS
           BEQ 5S
           ERROR 5S
           CHAIN 1S
           BR 1S
           ;TEST NUMBER
           ;NEXT TEST
           ;ITERATION COUNT
           ;SCOPE ENTRY
           ;SET PRIORITY 7
           ;SET INTERRUPT ENABLE BIT
           ;CHECK IF BIT IS SET
           ;BRANCH IF SET
           ;NOT SET, ERROR
           ;CHAIN TO NEXT TEST
           ;CLEAR INTERRUPT ENABLE BIT
           ;CHECK IF BIT IS CLEARED
           ;BRANCH IF CLEARED
           ;NOT CLEARED, ERROR
           ;CHAIN TO NEXT TEST
           ;DO TEST AGAIN

*****
;AT6-- TEST#46--TESTS THE ABILITY TO SET AND CLEAR
;TRANSMITTER INTERRUPT ENABLE BIT.
*****
      AT6: 46
           AT7
           10.
           IS
           MOV #PRTV7,-(SP)
           MOV #1,-(SP)
           RTS
           BIT #BIT6,@TPS
           BIT #BIT6,@TPS
           BNE 2S
           ERROR 3S
           BIC #BIT6,@TPS
           BIT #BIT6,@TPS
           BEQ 3S
           ERROR 3S
           CHAIN 1S
           BR 1S
           ;TEST NUMBER
           ;NEXT TEST
           ;ITERATION COUNT
           ;SCOPE ENTRY
           ;SET PRIORITY TO 7
           ;SET INTERRUPT ENABLE BIT
           ;BE SURE PRINTER IS DONE WITH DL11S1 MESSAGE
           ;BEFORE ALLOWING FOLLOWING RESET.
           ;RESET
           ;TEST INTERRUPT ENABLE BIT
           ;BRANCH IF CLEARED
           ;STILL SET, ERROR
           ;CHAIN TO NEXT ROUTINE
           ;REPEAT TEST

*****
;AT7-- TEST #47--TESTS THE ABILITY TO CLEAR TRANSMITTER
;INTERRUPT ENABLE BIT WITH RESET INSTRUCTION.
*****
      AT7: 47
           AT10
           10.
           IS
           MOV #PRTV7,-(SP)
           MOV #1,-(SP)
           RTS
           BIT #BIT6,@TPS
           RESET
           BIT #BIT6,@TPS
           BEQ 2S
           ERROR 2S
           CHAIN 1S
           BR 1S
           ;TEST NUMBER
           ;NEXT TEST
           ;ITERATION COUNT
           ;SCOPE ENTRY
           ;SET PRIORITY TO 7
           ;SET INTERRUPT BIT
           ;RESET
           ;CHECK IF BIT IS CLEARED
           ;BRANCH IF CLEARED
           ;ERROR, RESET DID NOT CLEAR BIT
           ;CHAIN TO NEXT ROUTINE
           ;REPEAT TEST

```

```

*****
;AT6-- TEST#46--TESTS THE ABILITY TO SET AND CLEAR
;TRANSMITTER INTERRUPT ENABLE BIT.
*****
      12700
      12800
      12900
      13000
      13100
      13200 005604 000046
      13300 005606 005674
      13400 005610 000012
      13500 005612 005626
      13600 005614 012746 000340
      13700 005620 012746 005626
      13800 005624 060002
      13900 005626 052777 000100 172762 1S:
      14000 005634 032777 000100 172754
      14100 005642 001002
      14200 005644 104001
      14300 005646 000410
      14400 005650 042777 000100 172740 2S:
      14500 005656 032777 000100 172732
      14600 005664 001401
      14700 005666 104001
      14800 005670 104005
      14900 005672 000755
      1500
      1510
      1520
      1530
      1540
      1550
      1560 005674 000047
      1570 005676 005744
      1580 005700 000012
      1590 005702 005716
      1600 005704 012746 000340
      1610 005710 012746 005716
      1620 005714 001401
      1630 005716 052777 000100 172672 1S:
      1640 005724 000005
      1650 005736 032777 000100 172662
      1660 005738 001401
      1670 005736 104001
      1680 005740 104005
      1690 005742 000765

*****
;AT7-- TEST #47--TESTS THE ABILITY TO CLEAR TRANSMITTER
;INTERRUPT ENABLE BIT WITH RESET INSTRUCTION.
*****
      AT7: 47
           AT10
           10.
           IS
           MOV #PRTV7,-(SP)
           MOV #1,-(SP)
           RTS
           BIT #BIT6,@TPS
           RESET
           BIT #BIT6,@TPS
           BEQ 2S
           ERROR 2S
           CHAIN 1S
           BR 1S
           ;TEST NUMBER
           ;NEXT TEST
           ;ITERATION COUNT
           ;SCOPE ENTRY
           ;SET PRIORITY TO 7
           ;SET INTERRUPT BIT
           ;RESET
           ;CHECK IF BIT IS CLEARED
           ;BRANCH IF CLEARED
           ;ERROR, RESET DID NOT CLEAR BIT
           ;CHAIN TO NEXT ROUTINE
           ;REPEAT TEST

```

```

17100
17200
17300
17400
17500
17600 005744 000050
17700 005746 006002
17800 005750 000012
17900 005752 005753
18000 005754 032777 001000 172732 1S: BIT #LSI11,@SR ;TEST NUMBER
18100 005762 001005 ;NEXT TEST
18200 005764 000005 ;ITERATION COUNT
18300 005766 105777 172624 ;SCOPE ENTRY
18400 005772 100401 ;SKIP TEST IF AN LSI-11
18500 005774 104001 ;RESET
18600 005776 104005 ;CHECK TRANSMIT READY BIT
18700 006000 000765 ;BRANCH IF SET
;ERROR, RESET DID NOT SET READY BIT
;CHAIN TO NEXT TEST
;DO AGAIN
;*****
;AT10-- TEST #50--CHECKS THAT RESET SETS THE TRANSMITTER
;READY BIT AND THAT THE READY BIT CAN BE READ RELIABLY.
;*****
AT10: 50 ;TEST NUMBER
AT11 ;NEXT TEST
10- ;ITERATION COUNT
1S ;SCOPE ENTRY
BIT #LSI11,@SR ;SKIP TEST IF AN LSI-11
2S ;RESET
BNE ;CHECK TRANSMIT READY BIT
RESET ;BRANCH IF SET
TSTB @TPS ;ERROR, RESET DID NOT SET READY BIT
2S ;CHAIN TO NEXT TEST
ERROR ;DO AGAIN
CHAIN 1S ;DO AGAIN
BR 1S ;DO AGAIN
;*****
;AT11-- TEST #51--TESTS THAT THE TRANSMITTER READY RESETS
;BY LOADING THE TRANSMITTER BUFFER.
;*****
AT11: 51 ;TEST NUMBER
AT12 ;NEXT TEST
10- ;ITERATION COUNT
1S ;SCOPE ENTRY
MOV #226,R0 ;DELAY 150 MSEC.
DELAY ;RESET
RESET ;LOAD TRANSMITTER BUFFER
CLR @TPB ;CHECK TRANSMIT READY BIT
TSTB @TPS ;BRANCH IF CLEARED
2S ;NOT CLEARED, ERROR
ERROR ;CHAIN TO NEXT TEST
CHAIN 1S ;REPEAT TEST
BR 1S ;REPEAT TEST

```

```

20800
20900
21000
21100
21200
21300 006042 000052
21400 006044 005772
21500 006046 000012
21600 006050 006056
21700 006054 104004
21800 006054 006112
21900 006056 000005
22000 006060 005077 172532
22100 006064 005046 006074
22200 006066 012746
22300 006072 000002 000100 172514
22400 006074 052777
22500 006102 000240
22600 006104 104001
22700 006106 104005
22800 006110 000762
22900 006112 022572
23000 006114 000774
23100
23200
23300
23400
23500
23600
23700 006116 000035
23800 006122 000012
23900 006124 006132
24000 006126 104004
24100 006130 006170
24200 006132 012746 172472
24300 006136 012746 006144
24400 006142 000002
24500 006144 005077 172446
24600 006150 052777 006100 172440
24700 006156 000240
24800 006160 005077 172432
24900 006164 104005
25000 006166 000761
25100 006170 022626
25200 006172 104001
25300 006174 000771
25400
;*****
;AT12-- TEST #52--CHECKS THAT THE TRANSMIT READY BIT CAN
;CAUSE AN INTERRUPT
;*****
AT12: 52 ;TEST NUMBER
AT13 ;NEXT TEST
10- ;ITERATION COUNT
1S ;SCOPE ENTRY
STPCHV ;SET UP TRANSMITTER INTERRUPT VECTOR
TO 4S ;SET CHAIN COMMENT
RESET ;DISABLE TRANSMIT INTERRUPT
;SEE CHAIN COMMENT
CLR @TPS ;SET PRIORITY TO ZERO
-(SP)
MOV #2S,-(SP)
RTI
RTI #RIT6,@TPS ;ENABLE TRANSMIT INTERRUPT
NOP
ERROR ;TRANSMIT READY DID NOT CAUSE INTERRUPT
CHAIN ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
POPSP2 3S ;INTERRUPT OCCURRED, CLEAN STACK
BR 3S ;CHAIN TO NEXT TEST
;*****
;AT13-- TEST #53--TESTS THAT THE TRANSMIT READY DOES NOT CAUSE AN
;INTERRUPT WHEN THE PROCESSOR IS AT THE SAME LEVEL
;*****
AT13: 3S ;TEST NUMBER
AT14 ;NEXT TEST
10- ;ITERATION COUNT
1S ;SCOPE ENTRY
STPCHV ;SET UP TRANSMIT INTERRUPT
VECTOR TO 4S ;SET PROCESSOR TO SAME LEVEL AS XMITTER
MOV TPLVL,-(SP)
#2S,-(SP)
2S: CLR @TPS ;DISABLE TRANSMITTER INTERRUPTS
#RIT6,@TPS ;ENABLE TRANSMITTER INTERRUPTS
3S: CLR @TPS ;OK, NO INTERRUPT OCCURRED
BR ;CHAIN TO NEXT TEST
CHAIN 1S ;REPEAT TEST
POPSP2 ;INTERRUPT OCCURRED, ERROR, CLEAN
ERROR ;UP STACK
BR 3S ;CHAIN TO NEXT TEST

```

```

I/O LOGIC TESTS
25600
25700
25800
25900
26000
26100
26200 006176 000954
26300 006200 006262
26400 006202 000012
26500 006204 006212
26600 006206 104004
26700 006210 006250
26800 006212 005077 172400
26900 006216 016746 172406
27000 006222 162716 006240
27100 006226 012746 006234
27200 006232 000002
27300 006234 052777 000100 172354 25:
27400 006236 006240
27500 006244 104001
27600 006246 000401
27700 006248 000000
27800 006250 006249 172340
27900 006256 104005
28000 006260 000754

;*****
;AT14-- TEST#54--TESTS THAT THE TRANSMIT READY DOES CAUSE AN
; INTERRUPT WHEN THE PROCESSOR IS AT A PRIORITY LEVEL
; ONE LOWER THAN THE TRANSMIT INTERRUPT REQUEST LEVEL
;*****
AT14: 54 ;TEST NUMBER
      AT15 ;NEXT TEST
      10- ;ITERATION COUNT
      15 ;SCOPE ENTRY
      STPCHV ;SET UP TRANSMIT INTERRUPT
      35 ;VECTOR TO 35
      CLR @TPS ;DISABLE TRANSMIT INTERRUPTS
      MOV TPLV, -(SP) ;SET PROCESSOR PRIORITY ONE
      SUB #40, (SP) ;LEVEL LOWER THAN TRANSMITTER
      MOV #25, -(SP)
      RTI
      BIS #BIT6, @TPS ;ENABLE TRANSMITTER INTERRUPTS
      NOP
      ERROR ;NO INTERRUPT, ERROR
      BR 45 ;CHAIN TO NEXT TEST
      POPSP2 ;INTERRUPT OCCURED, CLEAN STACK
      CLR @TPS ;DISABLE TRANSMITTER INTERRUPTS
      CHAIN ;CHAIN TO NEXT TEST
      BR 15 ;REPEAT TEST
  
```

```

I/O LOGIC TESTS
28200
28300
28400
28500
28600
28700
28800 006262 000955
28900 006264 006362
29000 006266 000012
29100 006270 006272
29200 006272 104004
29300 006274 006334
29400 006276 005077 172314
29500 006300 005046 006312
29600 006304 012746
29700 006310 000002
29800 006312 052777 000100 172276 25:
29900 006320 006240
30000 006322 104001
30100 006324 005077 172266 35:
30200 006330 104005
30300 006332 000757
30400 006334 012777 006354 172264 45:
30500 006342 012716 006350
30600 006346 000002
30700 006350 000240
30800 006352 000764
30900 006354 022626
31000 006356 104001
31100 006360 000761
31200
31300
31400
31500
31600
31700 006362 000956
31800 006364 006330
31900 006366 000012
32000 006370 006372
32100 006372 032777 001000 172314 15:
32200 006400 001011 35
32300 006402 012700 007226
32400 006406 104010
32500 006410 104011 25:
32600 006412 000005
32700 006414 052777 172172
32800 006420 100001
32900 006422 104001
33000 006424 104005 35:
33100 006426 000761 15

;*****
;AT15-- TEST#55--TESTS THAT THE TRANSMIT READY DOES NOT
; REINTERRUPT AFTER AN RTI WHEN THE READY BIT HAS
; BEEN RESET.
;*****
AT15: 55 ;TEST NUMBER
      AT16 ;NEXT TEST
      10- ;ITERATION COUNT
      15 ;SCOPE ENTRY
      STPCHV ;SET TRANSMIT INTERRUPT VECTOR
      45 ;TO 45
      CLR @TPS ;DISABLE TRANSMITTER INTERRUPTS
      CLR -(SP) ;SET PROCESSOR PRIORITY TO ZERO
      MOV #25, -(SP)
      RTI
      BIS #BIT6, @TPS ;ENABLE TRANSMITTER INTERRUPTS
      NOP
      ERROR ;ERROR1, TRANSMITTER FAILED TO INTERRUPT
      CLR @TPS ;DISABLE TRANSMITTER INTERRUPTS
      CHAIN ;CHAIN TO NEXT TEST
      BR 15 ;REPEAT TEST
      MOV #6, @TPVTR ;INTERRUPT OCCURED, CHANGE INTERRUPT
      MOV #55, @SP ;VECTOR TO 65 AND RETURN TO 55
      RTI ;RETURN FROM INTERRUPT
      NOP
      BR 35 ;CHAIN TO NEXT TEST
      POPSP2 ;ERROR2, TRANSMITTER REINTERRUPTED
      ERROR 35 ;AFTER RTI WITH READY BIT LEFT ON.
      BR 35 ;CLEAN STACK, CHAIN TO NEXT TEST.

;*****
;AT16--TEST#56--CHECKS THAT RESET CLEARS THE RECEIVER DONE BIT
;*****
AT16: 56 ;TEST NUMBER
      AT17 ;NEXT TEST
      10- ;ITERATION COUNT
      15 ;SCOPE ENTRY
      BIT #LSI11, @SR ;SKIP TEST IF LSI-11
      BNE 35
      MOV #226, R0
      DELAY 150 MSEC ;DELAY 150 MSEC
      AHEAD ;ENABLE RECEIVER
      RESET ;RESET
      TSTB @TKS ;TEST DONE BIT
      BPL 35 ;BRANCH IF DONE IS CLEARED
      ERROR ;NOT CLEARED, ERROR
      CHAIN ;CHAIN TO NEXT TEST
      BR 15 ;REPEAT TEST
  
```



```

I/O LOGIC TESTS
33300 ;*****
33400 ;AT17-- TEST#57--CHECKS THAT REFERENCING THE RECEIVER BUFFER
33500 ;CAUSES THE DONE BIT.
33600 ;*****
33700
33800 006430 000057 AT17: 57 ;TEST NUMBER
33900 006432 006500 AT20 ;NEXT TEST
34000 006434 000012 10- ;ITERATION COUNT
34100 006436 006440 1$ ;SCOPE ENTRY
34200 006440 032777 001000 172246 1$: BIT #LSI11,@SR ;CHECK FOR LSI-11
34300 006446 001212 BNE 3$ ;SKIP TEST IF SET
34400 006450 012700 000226 MOV #226,R0
34500 006454 104010 DELAY ;DELAY 150 MSEC
34600 006456 104021 AREAD ;ENABLE RECEIVER
34700 006460 105777 172130 2$: TSTB @TKR ;REFERENCE RECEIVER BUFFER
34800 006464 105777 172122 TSTB @TKS ;TEST DONE BIT
34900 006470 100001 BPL 3$ ;BRANCH IF NOT SET
35000 006472 104001 ERROR ;DONE BIT IS SET, ERROR
35100 006474 104005 CHAIN ;CHAIN TO NEXT TEST
35200 006476 000760 BR 1$ ;REPEAT TEST
35300 ;*****
35400 ;AT20-- TEST#60--CHECK THAT THE RECEIVER DONE BIT IS ABLE TO
35500 ;CAUSE AN INTERRUPT.
35600 ;*****
35700
35800 006500 000060 AT20: 60 ;TEST NUMBER
35900 006502 006572 AT21 ;NEXT TEST
36000 006504 000012 10- ;ITERATION COUNT
36100 006506 006510 1$ ;SCOPE ENTRY
36200 006510 104003 STRDRV ;SET UP RECEIVER INTERRUPT
36300 006512 006564 4$ ;VECTOR TO 4$
36400 006514 032777 001000 172172 1$: BIT #LSI11,@SR ;CHECK FOR LSI-11
36500 006516 012700 000226 BNE 3$ ;SKIP TEST IF SET
36600 006524 104010 MOV #226,R0
36700 006530 104010 DELAY ;DELAY 150 MSEC
36800 006534 104021 AREAD ;ENABLE RECEIVER
36900 006536 172052 2$: CLR @TKS ;DISABLE RECEIVER INTERRUPTS
37000 006540 005046 CLR -(SP) ;SET PROCESS STATUS TO ZERO
37100 006542 012746 006550 MOV #3$,-(SP)
37200 006546 000001 RTI ;ENABLE RECEIVER INTERRUPT
37300 006550 052777 000100 172034 3$: BIS #RIT6,@TKS ;ERROR, RECEIVER FAILED TO INTERRUPT
37400 006556 104001 NOP ;NO INTERRUPT OCCURRED
37500 006560 104001 ERROR ;CHAIN TO NEXT TEST
37600 006562 004001 BR 5$ ;OK, CLEAN STACK
37700 006564 022626 CHAIN ;CHAIN TO NEXT TEST
37800 006566 104005 BR 1$ ;REPEAT TEST
38000 006570 000751 BR 1$ ;REPEAT TEST
    
```

```

I/O LOGIC TESTS
38200 ;*****
38300 ;AT21-- TEST#61--TESTS THAT THE RECEIVER DONE DOES NOT CAUSE AN
38400 ;INTERRUPT WHEN THE PROCESSOR IS AT THE SAME LEVEL AS
38500 ;THE RECEIVER'S INTERRUPT REQUEST LEVEL.
38600 ;*****
38700
38800 006572 000061 AT21: 61 ;TEST NUMBER
38900 006574 006672 AT22 ;NEXT TEST
39000 006576 000012 10- ;ITERATION COUNT
39100 006600 006606 1$ ;SCOPE ENTRY
39200 006602 104003 STRDRV ;SET RECEIVER VECTOR TO 5$
39300 006604 006664 4$ ;VECTOR TO 4$
39400 006606 032777 001000 172100 1$: BIT #LSI11,@SR ;CHECK FOR LSI-11
39500 006614 001017 000226 BNE 4$ ;SKIP TEST IF SET
39600 006616 012700 MOV #226,R0
39700 006622 104010 DELAY ;DELAY 150 MSEC
39800 006624 104021 AREAD ;ENABLE RECEIVER
39900 006626 005077 171760 2$: CLR @TKS ;ENABLE RECEIVER INTERRUPTS
40000 006632 016746 171766 MOV @TKLVL,-(SP) ;SET PROCESSOR PRIORITY TO SAME LEVEL AS RECEIVER
40100 006636 016746 006644 MOV #3$,-(SP)
40200 006642 000001 RTI ;ENABLE RECEIVER INTERRUPTS
40300 006644 052777 000100 171740 3$: BIS #RIT6,@TKS ;ERROR, RECEIVER INTERRUPTED, CLEAN STACK
40400 006646 006740 NOP ;NO INTERRUPT OCCURRED
40500 006654 005077 171732 4$: CLR @TKS ;CHAIN TO NEXT TEST
40600 006660 104005 BR 5$ ;OK, NO INTERRUPT OCCURRED
40700 006662 000751 CHAIN ;CHAIN TO NEXT TEST
40800 006664 022626 BR 1$ ;REPEAT TEST
40900 006666 104005 ERROR ;ERROR, RECEIVER INTERRUPTED, CLEAN STACK
41000 006670 000771 BR 4$ ;BRANCH 4$
    
```

```

I/O LOGIC TESTS
41200 ;*****
41300 ;AT22-- TEST#62--TESTS THAT THE RECEIVER DONE DOES CAUSE AN
41400 ; INTERRUPT WHEN THE PROCESSOR IS AT A PRIORITY ONE
41500 ; LEVEL LOWER THAN THE RECEIVER'S INTERRUPT
41600 ; REQUEST LEVEL
41700 ;*****
41800
41900 006672 000062 AT22: 62 ;TEST NUMBER
42000 006674 007000 AT23 ;NEXT TEST
42100 006676 000012 10. ;ITERATION COUNT
42200 006700 006006 1S ;SCOPE ENTRY
42300 006702 104003 STRDRV ;SET RECEIVER INTERRUPT
42400 006704 006766 4S ;VECTOR TO 4S
42500 006706 032777 001000 172000 1S: BIT #LSI11,RSR ;CHECK FOR LSI11
42600 006714 001025 000226 BNE 5S ;SKIP TEST IF SET
42700 006716 012700 MOV #226,R0
42800 006722 104010 DELAY ;DELAY 150 MSEC
42900 006724 104021 AREAD ;ENABLE RECEIVER
43000 006726 005077 171660 CLR ;SET RECEIVER INTERRUPTS
43100 006732 016746 2S: MOV #TKS ;DISABLE READER INTERRUPTS
43200 006736 012744 006744 MOV #LVL,-(SP) ;SET PROCESSOR PRIORITY ONE LEVEL
43300 006742 000002 RTI ;
43400 006744 000100 000040 171024 3S: BIS #40,PSW ;LOWER THAN READER
43500 006752 055497 000100 171632 BIS #BIT6,@TKS ;ENABLE INTERRUPTS
43600 006760 000240 NOP ;
43700 006762 104001 ERROR ;FAILED TO INTERRUPT
43800 006764 000401 BR ;CHAIN TO NEXT TEST
43900 006766 022626 4S: POPSP2 5S ;OK, CLEAN STACK
44000 006770 005077 171616 CLR @TKS ;DISABLE RECEIVER INTERRUPTS
44100 006774 104005 BR ;CHAIN TO NEXT TEST
44200 006776 000743 BR 1S ;REPEAT TEST

```

```

I/O LOGIC TESTS
44400 ;*****
44500 ;AT23-- TEST#63--CHECKS THAT THE RECEIVER DONE DOES NOT
44600 ; REINTERRUPT AFTER RTI INSTRUCTION WHEN DONE
44700 ; BIT IS LEFT SET.
44800 ;*****
44900
45000 007000 000063 AT23: 63 ;TEST NUMBER
45100 007002 007112 AT24 ;NEXT TEST
45200 007004 000012 1S ;ITERATION COUNT
45300 007006 007010 1S ;SCOPE ENTRY
45400 007010 032777 001000 171676 1S: BIT #LSI11,RSR ;CHECK FOR LSI-11
45500 007016 001015 000226 BNE 3S ;SKIP TEST IF SET
45600 007020 012700 MOV #226,R0
45700 007024 104010 DELAY ;DELAY 150 MSEC
45800 007026 104021 AREAD ;ENABLE RECEIVER
45900 007030 104003 STRDRV ;SET RECEIVER INTERRUPT
46000 007032 007064 4S ;VECTOR TO 4S
46100 007034 005077 171552 CLR @TKS ;DISABLE RECEIVER INTERRUPTS
46200 007040 052777 000100 171544 BIS #BIT6,@TKS ;ENABLE RECEIVER INTERRUPT
46300 007046 000240 NOP ;
46400 007050 104001 ERROR ;NO INTERRUPT, ERROR
46500 007052 005077 171534 CLR @TKS ;DISABLE RECEIVER INTERRUPTS
46600 007056 000005 RESET ;RESET AFTER LAST INTERRUPT
46700 007060 104005 CHAIN ;CHAIN TO NEXT TEST
46800 007062 000752 RR 1S ;REPEAT TEST
46900 007064 012777 007104 171530 4S: MOV #C,@TKVTR ;INTERRUPT OK, CHANGE VECTOR TO 6S
47000 007072 012714 007100 171530 4S: MOV #C,@SP ;CHANGE RET ADDR TO 5S
47100 007076 000002 RTI ;RETURN
47200 007080 000240 5S: NOP ;
47300 007102 000763 6S: POPSP2 3S ;OK, NO ADDITIONAL INTERRUPT
47400 007104 022626 ERROR ;ERROR, ADDITIONAL INTERRUPT
47500 007106 104001 BR 3S ;CHAIN TO NEXT TEST
47600 007110 000760 BR 3S ;CHAIN TO NEXT TEST

```

```

47800
47900
48000
48100
48200
48300
48400
48500 007112 000064
48600 007114 007212
48700 007116 000001
48800 007120 007172
48900 007124 032777 001000 171564 1$: BIT #LSI11,@SR
49000 007130 001426 171454 1$: BEQ 55
49100 007132 005777 171454 1$: TST @TKS
49200 007136 001401 171454 2$: BEQ 25
49300 007140 104001 000600 171454 2$: ERROR #600,RO
49400 007142 012700 000030 171454 2$: MOV #30,CNTR
49500 007146 012787 000030 171454 2$: TYPE #600,RO
49600 007154 104000 000030 171454 2$: OPMSG #30,CNTR
49700 007156 014401 000030 171454 2$: DELAY #600,RO
49800 007160 104010 000030 171454 2$: TSTR @TKS
49900 007162 105477 000030 171454 2$: BNE 3$
50000 007166 104077 000030 171454 2$: DEC CNTR
50100 007170 005367 000030 171454 2$: BEQ 4$
50200 007174 001403 000030 171454 2$: MOV #600,RO
50300 007176 013700 000030 171454 2$: BR 3$
50400 007202 008766 000030 171454 2$: ERROR #3$
50500 007204 104001 000030 171454 2$: CHAIN 1$
50600
50700 007206 104005 000030 171454 2$: BR 1$
50800 007210 000744

```

```

51000
51100
51200
51300
51400
51500 007212 000065
51600 007214 007270
51700 007216 000001
51800 007220 007222
51900 007222 032777 001000 171464 1$: BIT #LSI11,@SR
52000 007230 001415 171354 1$: BEQ 65
52100 007232 105777 171354 2$: TSTR @TKS
52200 007236 001001 171354 2$: BNE 3$
52300 007240 104001 000100 171336 2$: ERROR #BIT6,@TKS
52400 007242 104003 000100 171336 2$: STRDRV 5$
52500 007244 007262 000100 171336 2$: BIC #BIT6,@TKS
52600 007246 052777 000100 171336 2$: NOP
52700 007254 000240 000100 171336 2$: NOP
52800 007256 000240 000100 171336 2$: ERROR
52900 007260 104001 000100 171336 2$: POPSP2
53000 007262 022626 000100 171336 2$: CHAIN
53100 007264 104005 000100 171336 2$: CHAIN
53200
53300 007266 000755

```

```
53500 ;*****  
53600 ;AT26--TEST#66--CHECK THAT READING TKB CLEARS DONE BIT  
53700 ; AND THAT DONE CLEARED DOES NOT CAUSE AN INTERRUPT  
53800 ;*****  
53900  
54000 007270 000066 AT26: 66 ;TEST NUMBER  
54100 007272 177777 -1 ;LAST TEST  
54200 007274 000001 1 ;ITERATION COUNT  
54300 007276 007300 ;SCOPE ENTRY  
54400 007300 032777 001000 171406 1$: BIT #LSI11,@SR ;SKIP TEST IF NOT AN LSI-11  
54500 007306 001422 171276 2$: BEQ 5$ ;MAKE SURE DONE IS STILL SET  
54600 007310 105777 BNE 3$  
54700 007314 001001 ERROR ;RECEIVER DONE NOT SET  
54800 007316 104001 MOV @TKB,CNTR ;READ DATA BUFFER  
54900 007320 112757 171270 171370 3$: TSTB @TKS ;CHECK THE DONE BIT  
55000 007326 105777 171260 RPI 4$ ;OK  
55100 007332 100001 ERROR ;READING DATA BUFFER DID NOT CLEAR DONE  
55200 007334 104001 STRDRV ;SET RECEIVER INTERRUPT  
55300 007336 104003 6$ ;VECTOR TO 6$  
55400 007340 007364 000100 171242 4$: BIS #BIT6,@TKS ;ENABLE INTERRUPT  
55500 007342 052757 6$  
55600 007350 000240 NOP  
55700 007352 000240 CLR @TKS ;OK- CLEAN UP  
55800 007354 005077 171232 5$: CHAIN RR ;EXIT TESTS  
55900 007360 104005 RR 1$  
56000 007362 000746 6$: ERROR 1$ ;DLV INTERRUPTED WITH DONE CLEAR  
56100 007364 104001 POPSP2 ;CLEAN UP THE STACK  
56200 007366 022526 RR ;EXIT TESTS  
56300 007370 000771
```

56500

LA36 PRINTER TESTS

100  
110  
120  
130  
140  
150  
160  
170  
180  
190  
200  
210  
220  
230  
240  
250  
260  
270  
280  
290  
300  
310  
320  
330  
340  
350  
360  
370  
380  
390  
400  
410  
420  
430  
440

007372 000000  
007374 007446  
007376 104016  
007400 104007  
007402 014127  
007404 012703  
007410 012702 000044  
007414 010300  
007416 016791 171230  
007422 104015  
007424 000300  
007426 005301  
007430 001374  
007432 004303  
007434 104012  
007436 005302  
007440 001365  
007442 104005  
007444 000757

```

.SBTTL LA36 PRINTER TESTS
; THE LA36 PRINTER TESTS WILL BE EXECUTED IN A
; CONTINUOUS LOOP OUTPUTTING TO ALL MULTIPLE DL11'S
; IF SR BIT 8 IS SET TO ZERO AT START UP TIME. IF
; BIT 8 IS SET TO 1 AT START UP THEY MAY BE EXECUTED
; INDIVIDUALLY ONCE OR CONTINUALLY LOOPEP, OR
; BECOME THE FIRST OF THE ENTIRE SEQUENCE OF PRINTER
; TESTS. REFERENCE INSTRUCTIONS IN THE INTRODUCTION
; FOR PROPER MODE OF OPERATION.
;XXXXXXXXXX
PTO -- DATA PATH TEST---FOUR LINES OF ALTERNATING
; "*" AND "U" ARE PRINTED OUT TO THE GIVEN PAPER
; WIDTH. THE PATTERN WILL APPEAR AS FOLLOWS.
;
; *U*U*U*U*U
; U*U*U*U*U*
; *U*U*U*U*U
; U*U*U*U*U*
;XXXXXXXXXX
PTO: 0 ;TEST NUMBER
PT1 ;NEXT TEST
PRTHDR ;PRINT COLUMN # MESC
TYPEM
HDRQ
1S: MOV #4,R1 ;SET FIRST CHAR PAIR
MOV #4,R2 ;SET LINE COUNT
2S: MOV #3,R0 ;SET CHAR PAIR
MOV WIDTH,R1 ;SET COLUMN COUNT
3S: PRINTC ;PRINT CHAR
SWAB R0 ;SET NEXT CHAR
DEC R1 ;DEC COLUMN COUNT
RNE 3S ;FINISH LINE
SWAB R3 ;SET NEXT LINE START CHAR
CRLF ;SEND CR-LF
DEC R2 ;DEC LINE COUNT
RNE 2S ;FINISH TEST
CHAIN ;ALL DONE EXIT
BR 1S ;REPEAT TEST
    
```

LA36 PRINTER TESTS

4600  
4700  
4800  
4900  
5000  
5100  
5200  
5300  
5400  
5500  
5600  
5700  
5800  
5900  
6000  
6100  
6200  
6300  
6400  
6500  
6600  
6700  
6800  
6900  
7000  
7100  
7200  
7300  
7400  
7500  
7600  
7700  
7800  
7900  
8000  
8100  
8200

007446 000001  
007450 007570  
007452 104016  
007454 012701 000040  
007460 012702 000100  
007464 012703 000140  
007470 110100  
007472 004267 000042  
007476 110200  
007500 004767 000034  
007504 012704  
007510 110300 000003  
007512 104015  
007514 005304  
007516 001375  
007520 104012  
007522 104012  
007524 105123  
007526 020327 000200  
007532 104015  
007534 104005  
007536 000746  
007540 012704 000003  
007544 104015  
007546 005304  
007550 001375  
007552 012700 000040  
007556 104015 000040  
007560 012700  
007564 104015  
007566 000207

```

;XXXXXXXXXX
PT1 -- PRINTER CHARACTER TEST --- PRINTS ALL PRINTABLE CHARACTERS
;XXXXXXXXXX
PT1: 1 ;TEST NUMBER
PT2 ;NEXT TEST
PRTHDR
1S: MOV #40,R1 ;SPACE TO R1
MOV #10,R2 ;A TO R2
MOV #140,R3 ;A TO R3
2S: MOVB R1,R0 ;CHAR TO R0
JSP PC,SPSP ;SEND TWO SPACES
MOVB R2,R0 ;NEXT CHAR TO R0
JSP PC,SPSP ;SEND TWO SPACES
MOV #3,R4 ;PRINT COUNT TO R4
MOVB R3,R0 ;THIRD CHAR TO R0
3S: PRINTC ;PRINT THE CHAR
DEC R4 ;THREE TIMES?
RNE 3S ;BRANCH IF NOT
CRLF ;CARRIAGE RETURN LINE FEED
CMPR (R1)+,(R2)+ ;NEXT CHARACTERS
BLD 2S ;CHECK IF ALL DONE
CHAIN ;BRANCH TO NEXT TEST
BR 1S ;REPEAT TEST
SPSP: MOV #3,R4 ;PRINT COUNT TO R4
1S: PRINTC ;PRINT CHAR
DEC R4 ;THREE TIMES?
RNE 3S ;BRANCH IF NOT
MOV #40,R0 ;SPACE TO R0
SP2: PRINTC ;SEND A SPACE
MOV #40,R0 ;SPACE TO R0
SPC: PRINTC #40,R0 ;SEND ANOTHER
RTS PC ;RETURN
    
```

```

8400
8500
8600
8700
8800
8900
9000
9100
9200
9300
9400
9500
9600
9700 007570 000002
9800 007572 010164
9900 007574 104016
10000 007576 012701 007676
10100 007602 012703 010137
10200 007604 012702 000003
10300 007612 012704 000010
10400 007616 121327 000055
10500 007624 001422
10600 007628 104015
10700 007626 104015
10800 007630 005304
10900 007632 001371
11000 007634 104015
11100 007636 012704 000003
11200 007642 104015
11300 007644 005304
11400 007648 001371
11500 007650 005302
11600 007652 001404
11700 007654 104015
11800 007656 104015 177672
11900 007662 000753
12000 007664 104015
12100 007666 000747
12200 007668 104015
12300 007670 104015
12400 007674 000740
12500
12600
12700
12800
007676 060 060 060
007701 040 040 040
007703 060 060 060
007707 060 061 040
007712 040 123 117
007715 110 060 060
007723 125 040 040
007726 060 060 066
007731 040 040 040
007737 060 062 064
007742 040 104 114

```

```

;XXXXXXXXXX
;PT2 -- NON-PRINTING CHARACTER TEST. THIS TEST
;PRINTS THE OCTAL CODE FOLLOWED BY THE MNEMONIC
;OF ALL NON-PRINTING CHARACTERS, FOLLOWING EACH
;MNEMONIC, THE PRINTER IS DRIVEN BY THE NON-PRINTING
;CODE (000 THROUGH 037 PLUS 177)
;ALL CONTROL CHARACTERS (INCLUDING THOSE FOR OPTIONS
;WILL BE SKIPPED, REFER TO THE DOCUMENT FOR A LIST OF THOSE
;TESTED.
;XXXXXXXXXX
PT2: 2 ;TEST NUMBER
PT3 ;NEXT TEST
PRTHDR ;PRINT TEST HEADER
15: MOV #IDEZ,R1 ;ADDR OF IDENT TO R1
MOV #NPCODE,R3 ;ADDR OF NON-PRINT-CODES TO R3
25: MOV #3,R2 ;NO. OF ID'S PER LINE TO R2
35: MOV #16,R4 ;NO. OF CHARS PER ID TO R4
45: CMPB (R3),#55 ;ZERO TERMINATOR IN NP TABLE?
BEQ 75 ;BRANCH IF YES
MOVB (R1)+,R0 ;GET ID CHARACTERS
PRINTC ;AND PRINT A
DEC R4 ;GROUP OF
BNE 45 ;8 CHARACTERS
MOV (R3)+,R0 ;GET NP CODE FROM TABLE
PRINTC ;AND
55: PRINTC ;TRY TO PRINT IT
DEC R4 ;THREE
BNE 55 ;TIMES
DEC R2 ;MORE TO GO ON THIS LINE ?
BEQ 65 ;BRANCH IF NO
JSP PC,SP2 ;SEND 3 SPACES
PRINTC
BR 35 ;BRANCH TO CONTINUE LINE
65: CRLF 25 ;GO DO NEXT LINE
RR 75: CRLF ;
CHAIN 15 ;CHAIN TO NEXT TEST
BR

```

```

LA36 PRINTER TESTS
007745 105 060 062
007750 061 040 046
007753 104 103 061
007757 070 062 062
13000 007761 040 104 062 .ASCII /022 DC2023 DC3024 DC4/
007764 103 062 060
007767 062 063 040
007772 063 064 103
007775 060 060 060
010000 064 040 040
13100 010003 104 103 064 .ASCII /025 NAK026 SYN027 ETR/
010006 060 062 065
010011 060 040 116
010014 101 113 060
010017 062 066 040
010022 040 123 104
010025 060 131 103
010030 116 060 062
010033 105 040 102
13200 010036 060 063 060 .ASCII /030 CAN031 EM 032 SUB/
010041 060 040 103
010044 101 116 060
010047 063 061 040
010052 060 105 063
010055 040 060 115
010060 062 040 040
13300 010063 123 125 102 .ASCII /034 FS 035 GS 036 RS /
010066 060 063 064
010071 040 040 106
010074 123 040 060
010077 063 065 040
010105 040 107 123
010110 040 060 063
010113 122 123 040
13400 010116 066 063 067 .ASCII /037 US 177 DEL /
010121 040 040 125
010124 123 040 061
010127 067 067 040
010132 040 104 105
13500 010137 000 006 006 NPCODE: .BYTE 0,2,6,20,21,22,23,24
010142 020 021 022
010145 023 024
13600 010147 027 .BYTE 25,25,27,30,31,32,34,35
010152 030 032
010155 034 035
13700 010157 036 037 177 .BYTE 36,37,177,55
010162 055 .EVEN

```

```

14000
14100
14200
14300
14400
14500
14600
14700
14800
14900
15000
15100
15200
15300
15400 010164 000003
15500 010166 010304
15600 010170 104016
15700 010172 010450
15800 010176 170476
15900 010202 000117
16000 010206 104015
16100 010210 005361
16200 010212 001404
16300 010214 004767 177340
16400 010220 005301
16500 010222 001367
16600 010224 104022
16700 010226 012767 000001 170440
16800 010234 016701 170434
16900 010240 004767 177314
17000 010244 005301
17100 010246 001374
17200 010250 012700 000130
17300 010254 104022
17400 010256 104022
17500 010260 002767 000002 170406
17600 010266 026767 170402 170356
17700 010276 104014
17800 010278 104014
17900 010300 104015
18000 010302 000733
;XXXXXXXXXX
PT3 -- CARRIAGE RETURN TEST
;
; THE LINE CONSISTS OF A STRING OF O'S AND
; Y'S. FIRST, THE O'S ARE PRINTED OUT TO THE LAST
; COLUMN WITH A SPACE SEPARATING EACH. THEN THE
; CARRIAGE IS SPACED TO THE FIRST BLANK SPACE, AN X
; IS PRINTED AND THEN RETURNED TO THE MARGIN. THIS
; PROCESS IS CONTINUED UNTIL ALL SPACES BETWEEN
; THE ZEROES HAVE BEEN FILLED.
;XXXXXXXXXX
PT3: 3 ;TEST NUMBER
PT4 ;NEXT TEST
PRTHDR ;TYPE HEADER
1S: CLR SPCNT ;CLEAR SPACE COUNTER
MOV WIDTH,R1 ;POSITION COUNTER TO R1
2S: MOV #117,R0 ;"O" TO R0
PRINTC ;PRINT THE "O"
DEC R1 ;DECREMENT POSITION COUNTER
BNE 0 ;BRANCH IF 0
SEND SPACE ;SEND SPACE
3S: DEC R1 ;DECREMENT POSITION COUNTER
BNE 25 ;BRANCH IF NOT ZERO
SEND A CR ;SEND A CR
4S: MOV #1,SPCNT ;SPACE COUNTER SET TO 1
MOV SPCNT,R1 ;NO. OF SPACES TO R1
5S: JSR PC,SPC ;SEND SPACE
RNE R1 ;DECREMENT SPACE COUNTER
MOV #130,R0 ;BRANCH IF NOT ZERO
PRINTC ;"X" INTO R0
ADD ;PRINT "X"
CMP SPCNT,WIDTH ;INCREMENT SPACE COUNT BY 2
BLO 4S ;COMPARE POSITION COUNTER WITH COLM. COUNT
LF ;BRANCH IF LOWER
CHAIN ;SEND LF
BR 1S ;RETURN TO NEXT TEST
;REPEAT TEST

```

```

18200
18300
18400
18500
18600
18700
18800
18900
19000
19100
19200 010304 000004
19300 010306 010462
19400 010310 104016
19500 010312 012767 000001 170366
19600 010320 016701 170326
19700 010324 012702 010444
19800 010330 004767 000060
19900 010334 016701 170346
20000 010340 104014
20100 010342 005301
20200 010344 001374
20300 010346 006367 170334
20400 010352 022767 000100 170326
20500 010360 001406
20600 010362 112200
20700 010364 104015
20800 010366 112200
20900 010370 104015
21000 010372 104022
21100 010374 000757
21200 010376 016701 170250
21300 010402 004767 000008
21400 010406 104014
21500 010410 104005
21600 010412 000737
21700 010414 112200
21800 010416 104015
21900 010420 112200
22000 010422 104015
22100 010424 005741
22200 010426 015700 000137
22300 010432 104015
22400 010434 005301
22500 010436 001375
22600 010440 104022
22700 010442 000207
22800
22900 010444 060 061 060
010447 062 061 064
010452 060 070 061
010455 066 063 062
010460 060 060
;XXXXXXXXXX
PT4 -- MULTIPLE LINE FEED TEST -- 63 LINE FEEDS ARE
SENT WITH A REFERENCE LINE AT THE START AND END.
A NUMBER IS PRINTED WHICH INDICATES THE NUMBER OF LINE
FEEDS THAT WILL BE ISSUED BEFORE THE NEXT
NUMBER OR REFERENCE LINE IS PRINTED.
;XXXXXXXXXX
PT4: 4 ;TEST NUMBER
PRTHDR ;NEXT TEST
1S: MOV #1,LFCNT ;LINE FEED COUNT TO 1
MOV WIDTH,R1 ;COLUMN COUNT TO R1
2S: JSR #LINE3,R2 ;ADDR OF NUMBER FIELD TO R2
MOV LFCNT,R1 ;PRINT REFERENCE LINE
3S: LF ;LINE FEED COUNT TO R1
DEC R1 ;SEND LF
RNE 3S ;DECREMENT COUNTER
ASL LFCNT ;BRANCH IF NOT VET 0
CMP #BIT6,LFCNT ;DOUBLE LINE FEED COUNT
REQ 4S ;TEST IF COUNT IS 32
MOV #R2+,R0 ;BRANCH IF =32, END
PRINTC ;NUMBER TO R0
MOV #R2+,R0 ;NUMBER TO R0
PRINTC ;PRINT IT
BR 2S ;PRINT CR
4S: MOV WIDTH,R1 ;DRIVE THE LINEFEEDS
JSR PC,REF ;COLUMN COUNT TO R1
LF ;SEND END REFERENCE LINE
CHAIN ;ADVANCE PAPER
BR 1S ;REPEAT TEST
REF: MOV #R2+,R0 ;NUMBER TO R0
PRINTC ;PRINT IT
MOV #R2+,R0 ;NUMBER TO R0
PRINTC ;PRINT IT
1S: TST -(R1) ;DECREASE COUNTER BY 2
MOV #131,R0 ;DASH (-) TO R0
PRINTC ;PRINT CR
DEC R1 ;DECREMENT COLUMN COUNTER
RNE 1S ;BRANCH IF NO ZERO
CR ;PRINT CR
RTS PC ;RETURN
LINE3: -ASCII /01020408163200/

```

```

;XXXXXXXXXX
;PT5-- SINGLE LINE FEED TEST -- TESTS THE LINE FEED
;CAPABILITY FROM ALL COLUMNS.
;XXXXXXXXXX
PT5: 5 ;TEST NUMBER
PT6 ;NEXT TEST
PRTHDR ;TYPE HEADER
MOV WIDTH,R1 ;COLUMN COUNT TO R1
RST -(R1) ;DECREASE BY 2
MOV #60,R0 ;"0" TO R0
PRINTC ;SEND 0
DEC R1 ;DECREMENT COLUMN COUNTER
BNE #62,R0 ;BRANCH IF NOT ZERO
MOV #62,R0 ;SEND A 2
PRINTC ;SEND A SECOND TWO
CMP WIDTH,#132. ;COMPARE COLUMN COUNT
BEQ #5 ;BRANCH IF EQ 132
MOV #3410,R0 ;DELAY 1.8 SEC
DELAY 1.8 SEC
BR 5S
3S: MOV #63,R0 ;3'S TO R0
MOV #100,R1 ;64 TO COUNTER
PRINTC ;SEND CHARACTER
RST ;DECREMENT COUNT
BNE #4S ;BRANCH IF NOT ZERO
5S: CRLF ;SEND A CR,LF
MOV WIDTH,R1 ;NO. COLUMNS TO R1
MOV #134,R0 ;BACKSLASH TO R0
PRINTC ;SEND IT
LF ;PRINT LF
DEC R1 ;DECREMENT COUNTER
BNE #6S ;BRANCH IF NOT ZERO.
CR ;SEND CR
JSR PC,PT5AL ;SEND REF LINE #1
CRLF ;SEND A CR,LF
DELAY 1 SEC
BR 5S
6S: MOV WIDTH,R1 ;COLUMN COUNT TO R1
PRINTC ;"0" TO R0
RST ;PRINT 0
DEC R1 ;DECREMENT COUNTER
REQ 2S ;BRANCH IF=0
INR R0 ;INCREMENT CHARACTER
CMP R0,#71 ;COMP CHAR TO "0"
BLS #1S ;BRANCH IF LOWER OR SAME
MOV #60,R0 ;RESET CHAR TO "0"
BR 1S ;CONTINUE
RTS PC ;FINISHED, RETURN TO CALLER

```

```

;XXXXXXXXXX
;PT6-- BACKSPACE TEST -- A REFERENCE LINE SUCH AS IN
;TEST PT5 IS PRINTED. THE SECOND LINE CONSISTS
;OF PRINTING A BACKSLASH, BACKSPACE AND FORWARD
;SLASH COMBINATION OUT TO THE GIVEN COLUMN WIDTH.
;THE LINES ARE THEN FOLLOWED BY THE SAME TWO REFERENCE
;LINES AS PRINTED IN TEST PT5.
;XXXXXXXXXX
PT6: 6 ;TEST NUMBER
PT7 ;NEXT TEST
PRTHDR ;PRINT HEADER
TYPEM ;PRINT COLUMN # MESC
HDR0 ;PRINT COLUMN # MESC
MOV WIDTH,R1 ;COLUMN COUNT TO R1
RST -(R1) ;DECREMENT BY 2
MOV #60,R0 ;"0" TO R0
PRINTC ;SEND 0
DEC R1 ;DECREMENT COLUMN COUNTER
BNE #62,R0 ;BRANCH IF NOT ZERO
MOV #62,R0 ;SEND A "2"
PRINTC ;SEND A SECOND "2"
CMP WIDTH,#132. ;COMPARE COLUMN COUNT
BEQ #3S ;COMPARE COLUMN COUNT
MOV #3410,R0 ;DELAY 1.8 SEC
DELAY 1.8 SEC
BR 3S
3S: MOV #63,R0 ;3'S TO R0
MOV #100,R1 ;64 TO CHAR COUNT
PRINTC ;SEND CHAR
DEC R1 ;DECREMENT CHAR COUNT
BNE #4S ;CONTINUE IF NOT DONE
5S: CRLF ;SEND A CR,LF
MOV WIDTH,R1 ;COLUMN COUNT TO R1
MOV #134,R0 ;BACKSLASH TO R0
PRINTC ;SEND IT
MOV #10,R0 ;BACKSPACE TO R0
PRINTC ;SEND IT
MOV #57,R0 ;FORWARD SLASH TO R0
PRINTC ;SEND IT
DEC R1 ;END OF PAPER
BNE #6S ;BRANCH IF NO
CR ;SEND CR
JSR PC,PT5AL ;SEND REF LINE #1
CRLF ;SEND A CR,LF
DELAY 1 SEC
BR 5S
6S: MOV WIDTH,R1 ;COLUMN COUNT TO R1
PRINTC ;SEND IT
MOV #57,R0 ;FORWARD SLASH TO R0
PRINTC ;SEND IT
DEC R1 ;END OF PAPER
BNE #6S ;BRANCH IF NO
CR ;SEND CR
JSR PC,PT5AL ;SEND SECOND REF LINE
CRLF ;SEND A CR,LF
CHAIN TO NEXT TEST
RR 1S ;REPEAT TEST

```



```

34000
34100
34200
34300
34400
34500
34600
34700
34800
34900
35000
35100 011154 000007
35200 011156 011266
35300 011160 104016
35400 011162 012703 000002
35500 011165 016701 167560
35600 011168 012700 000115
35700 011172 104015
35800 011176 104015
35900 011100 005301
36000 011104 014767 176450
36100 011110 005301
36200 011112 001367
36300 011120 000002
36400 011120 001003
36500 011122 104022
36600 011124 005303
36700 011126 001404
36800 011130 005703
36900 011132 001373
37000 011134 104013
37100 011136 005723
37200 011140 016701 167506
37300 011144 004767 176410
37400 011150 005301
37500 011152 001404
37600 011154 012700 000100
37700 011160 104015
37800 011162 005301
37900 011164 001367
38000 011166 023703 000002
38100 011172 001003
38200 011174 104022
38300 011176 005303
38400 011200 004767
38500 011202 005703
38600 011204 001373
38700 011206 104013
38800 011210 005723
38900 011212 016701 167434
39000 011216 012700 000046
39100 011222 104015
39200 011224 005301
39300
39400 011226 001404
39500 011230 004767 176324
39600 011234 005301

;XXXXXXXXXX
;PT7-- OVERPRINT TEST-- A ROW OF ALTERNATING M'S AND
; SPACES ARE PRINTED, OUT TO THE LAST COLUMN AND OVERPRINTED TWICE.
; A SECOND LINE OF ALTERNATING SPACES AND "M'S" IS THEN
; SENT 3 TIMES AS THE FIRST LINE. THIS IS FOLLOWED
; BY A THIRD AND FINAL LINE OF ALTERNATING "L'S"
; AND SPACES.
;XXXXXXXXXX
PT7: 7 ;TEST NUMBER
PT10 ;NEXT TEST
PRTHOR ;PRINT MESSAGE
1S: MOV #2,R3 ;2 COUNT TO R3
2S: MOV WIDTH,R1 ;NO OF COLUMNS TO R1
3S: MOV #115,R0 ;"M" TO R0
PRINTC ;SEND IT
DEC R1 ;END OF LINE
BEQ 4S ;BRANCH IF YES
JSP PC,SPC ;SEND SPACE
DEC R1 ;END OF LINE?
BNE 3S ;BRANCH IF NO
4S: CMP #2,R3 ;TEST R3
BEQ 5S ;BRANCH IF NOT FIRST TIME
DEC R3 ;DECREASE LINE COUNTER
5S: CR ;REPEAT LINE
TST R3 ;THIRD TIME?
BNE 5S ;BRANCH IF NOT
CRLF ;NEXT LINE
7S: TST (R3)+ ;REPEAT COUNTER TO R3
MOV WIDTH,R1 ;COLUMN COUNT TO R1
JSP PC,SPC ;SEND SPACE
8S: DEC R3 ;DECREASE COLUMN COUNT
BEQ 9S ;BRANCH IF 0, END OF LINE
MOV #100,R0 ;"L" TO R0
PRINTC ;SEND IT
DEC R1 ;DECREASE COLUMN COUNT
BNE 8S ;BRANCH IF NOT 0 (NOT END)
9S: CMP #2,R3 ;END OF LINE, FIRST TIME?
BNE 10S ;BRANCH IF NOT
10S: CR ;SEND CR
DEC R3 ;DECREASE LINE COUNTER
BNE 11S ;REPEAT LINE
11S: TST R3 ;TEST IF THIRD REPEAT
BNE 10S ;BRANCH IF NOT
CRLF ;END NEXT LINE
12S: TST (R3)+ ;LINE REPEAT COUNTER TO R3
MOV WIDTH,R1 ;COLUMN COUNT TO R1
MOV #46,R0 ;"M" TO R0
PRINTC ;SEND IT
DEC R1 ;DECREASE COLUMN COUNT
14S: BEQ 14S ;BRANCH IF END
15S: JSP PC,SPC ;SEND SPACE
DEC R1 ;DECREASE COLUMN COUNT

```

```

LA36 PRINTER TESTS
39700 011236 001367
39800 011240 022703 000002
39900 011244 001003
40000 011246 104022
40100 011250 005303
40200 011252 000757
40300 011254 005703
40400 011256 001373
40500 011260 104013
40600 011262 104015
40700 011264 000676

14S: BNE 13S ;BRANCH IF NOT END
15S: CMP #2,R3 ;TEST IF FIRST TIME
BNE 16S ;BRANCH IF =2, FIRST TIME
CR ;SEND CR
DEC R3 ;DECREASE REPEAT COUNTER
16S: BR 12S ;PRINT LINE AGAIN
TST R3 ;TEST IF END, R3=0
BNE 15S ;BRANCH IF NOT END
CRLF ;SEND CR,LF
CHAIN ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST

```

```

40900 ;XXXXXXXXXX
41000 ;PT10-- PRINTING FREQUENCY TEST-- 120 H'S ARE PRINTED ON 4 LINES
41100 ; 30 PER LINE. THE TEST IS SUCH THAT BETWEEN THE FIRST AND SECOND
41200 ; LINE A 30 MSEC DELAY IS INTRODUCED. THIS DELAY IS THEN INCREASED
41300 ; BETWEEN CHARACTERS OUT TO 60 CHARACTERS IN AN EXPONENTIAL
41400 ; MANNER. THE DELAY IS THEN DECREASED IN THE SAME MANNER OUT TO THE
41500 ; 120TH CHARACTER. THIS DELAY IS CALCULATED AS FOLLOWS;
41600 ;
41700 ; NEW DELAY = OLD DELAY [+ OR -] (OLD DELAY/16 + OLD DELAY/128 )
41800 ;XXXXXXXXXX
41900
42000
42100 011266 000010
42200 011270 011424
42300 011272 104016
42400 011274 012701 000036
42500 011300 012702 000170
42600 011304 012767 000036 000010
42700 011312 012700 000110
42800 011316 104015
42900 011320 012700 000036
43000 011324 104010
43100 011330 005302
43200 011332 005302
43300 011334 001430
43400 011336 016704 177760
43500 011340 006204
43600 011342 006204
43700 011344 006204
43800 011346 006204
43900 011350 006204
44000 011352 006204
44100 011354 006204
44200 011356 006204
44300 011360 006204
44400 011362 006204
44500 011364 022702 000074
44600 011370 003403
44700 011372 109745 177724
44800 011374 009745
44900 011400 005677 177716
45000 011404 000742
45100 011406 104010
45200 011410 000036
45300 011414 000746
45400 011416 104012
45500 011420 104005
45600 011422 000724

```

```

45900 ;XXXXXXXXXX
46000 ;PT11-- RIBBON FEED TEST-- THIS TEST PRINTS A SINGLE COLUMN OF X'S
46100 ; (24 LINES) DOWN THE LEFT MARGIN OF THE PAGE.
46200 ; VISUALLY CHECK THE RIBBON FEED MECHANISM FOR PROPER OPERATION.
46300 ;XXXXXXXXXX
46400
46500
46600
46700
46800 011424 000011
46900 011426 011456
47000 011430 104016 000030
47100 011432 012700 000130
47200 011436 012700
47300 011442 104015
47400 011444 104012
47500 011446 005301
47600 011450 005301
47700 011452 104005
47800 011454 000766
47900
48000
48100
48200 ;XXXXXXXXXX
48300 ;PT12-- PRINTER BELL TEST-- THE LAST TEST IN THE
48400 ; PRINTER TEST SEQUENCE. THIS TEST OUTPUTS
48500 ; EIGHT BELL SIGNALS TO THE PRINTER
48600 ;
48700 ;XXXXXXXXXX
48800
48900
49000
49100 011456 000012
49200 011460 007372
49300 011462 104016
49400 011464 012701 000010
49500 011470 012700 000007
49600 011474 104015
49700 011476 005301
49800 011500 001375
49900 011502 012700
50000 011504 104014 003720
50100 011510 104010
50200 011512 013700 000042
50300 011516 001405
50400 011518 002240
50500 011522 004710
50600 011524 000240
50700 011526 002240
50800 011530 002240
50900 011532 104005
51000 011534 000753

```

```

51200
51300
51400
51500
51600
51700
51800
51900
52000
52100
52200
52300 011536 000017
52400 011540 011536
52500 011542 000167
52600 011546 000177
52700 011550 011536
52800 011552 000336
52900 011556 016704 167070
53000 011562 012767 000001 000322
53100
53200
53300
53400
53500
53600
53700
53800
53900
54000
54100
54200
54300
54400
54500
54600
54700
54800
54900
55000
55100
55200
55300
55400
55500
55600
55700
55800
55900
56000
56100
56200
56300
56400
56500
56600
56700
56800

```

```

;XXXXXXXXXX
;PT17-- LIFE TEST
; THIS TEST PRINTS 2 FULL LINES OF EACH PRINTABLE
; CHARACTER AND OVERPRINTS THE SECOND LINE 4 TIMES.
; THIS TEST IS CONTINUOUS RUNNING ONCE INITIATED,
; LOOPING AUTOMATICALLY ON ITSELF.
; END OF PASS COUNT IS CLEARED WHENEVER TEST IS RESTARTED
;XXXXXXXXXX
PT17B: 17 ;TEST NUMBER
PT17B ;NEXT TEST
JMP PT17D ;CONTINUE
PT17: 17 ;TEST NUMBER
PT17B ;NEXT TEST
CLR PASCNT ;CLEAR PASS COUNT
MOV WIDTH,R4 ;INITIALIZE R4
MOV #1,DIRTN ;AND DIRECTION OF PRECESS
PRTHDR ;PRINT COLUMN # MESC
TYPEM ;SET START CHAR
HRO ;DO 31 TIMES
PT17D: #41,R3 ;BRANCH IF NOT DONE
INC PASCNT ;START OVER
CMP PASCNT,#31 ;SET MESC ADDR
BNE 20S ;# TO CONVERT
MOV #1,PASCNT ;CONVERT PASCNT TO ASCII
MOV #PASMES,R0 ;SET COLUMN COUNT
MOV PASCNT,R1 ;GET CHARACTER
MOV #2,R2 ;TIME TO INSERT PASS # ?
BTOASC ;SEND CHAR
1S: MOV WIDTH,R1 ;DECREMENT COUNT
MOV R3,R0 ;BRANCH IF NOT DONE
JSR PC,CRPOS ;ADJUST R4 POINTER
PRINTC R1 ;SEND CR
DEC R1 ;DONE OVERPRINTS ?
BGT 2S ;NO, CONTINUE
PC,ADJR4 ;ADJUST R4 POINTER
RLF ;SEND LF
MOV #5,R2 ;SET NEXT CHAR
MOV WIDTH,R1 ;DONE CHAR SET ?
MOV R3,R0 ;NO, CONTINUE
JSR PC,CRPOS ;ADJUST R4 POINTER
PRINTC R3 ;SET OVERPRINT COUNT
DEC R1 ;SET COLUMN COUNT
BGT 4S ;GET CHARACTER
PC,ADJR4 ;TIME TO INSERT PASS # ?
RLF ;SEND CHAR
MOV #5,R2 ;DECREMENT COUNT
MOV WIDTH,R1 ;BRANCH IF NOT DONE
MOV R3,R0 ;SEND CR
JSR PC,CRPOS ;DONE OVERPRINTS ?
PRINTC R2 ;NO, CONTINUE
DEC R1 ;ADJUST R4 POINTER
BGT 4S ;SEND LF
PC,ADJR4 ;SET NEXT CHAR
INC R3 ;DONE CHAR SET ?
CMP #177,R3 ;NO, CONTINUE
BNE 1S ;ADJUST R4 POINTER
JSR PC,ADJR4 ;TO RETAIN VISUAL ALIGNMENT
JSR PC,ADJR4 ;THROUGH END OF PASS

```

```

56900 011754 104007
57000 011756 014023
57100 011760 000705
57200 011762 000705
57300

```

```

TYPEM ;TYPE END OF PASS MESC
ENDPAS ;REPEAT TEST
CHAIN PT17D
BR

```

57500								
57600	011764	020401		CKPOS:	CMP	R4,R1		;IS IT TIME TO INSERT PASS # ?
57700	011766	001020			BNE	1\$		;BRANCH IF NO
57800	011770	012700	000040		MOV	#40,R0		;PRINT A SPACE
57900	011774	104015			PRINTC			
58000	011776	116700	002040		MOVB	PASMES,R0		;PRINT MSG OF PASS COUNT
58100	012002	104015			PRINTC			
58200	012004	116700	002033		MOVB	PASMES+1,R0		
58300	012010	104015			PRINTC			
58400	012012	012700	000040		MOV	#40,R0		;PRINT A SPACE
58500	012016	104015			PRINTC			
58600	012020	162701	000003		SUB	#3,R1		;ADJUST R1 3 POSITIONS
58700	012024	062716	000002		ADD	#2,(SP)		;ADJUST RETURN PC OVER PRINTC
58800	012030	000207		1\$:	RTS	PC		
58900								
59000	012032	005767	000054	ADJR4:	TST	DIRTN		;TEST DIRECTION OF PRECESS
59100	012036	010103			BNE	1\$		;BR IF LEFT
59200	012040	005204			INC	R4		;INCREASE POSITION CNTR
59300	012042	020467	166504		CMP	R4,WIDTH		;IS R4 > WIDTH ?
59400	012046	101420			BLOS	3\$		;BR IF NOT GREATER
59500	012050	012704	166576		MOV	WIDTH,R4		;CHANGE DIRECTION
59600	012054	005304			DEC	R4		; TO
59700	012056	012767	000001 000026		MOV	#1,DIRTN		; LEFT.
59800	012064	000411			BR	3\$		
59900	012066	005304		1\$:	DEC	R4		;DECREASE POSITION CNTR
60000	012070	020427	000004		CMP	R4,#4		;LESS THAN 4 ?
60100	012074	002401			BLT	3\$		;BR IF YES
60200	012076	006404			BR	3\$		;ELSE EXIT
60300	012100	012704	000005	2\$:	MOV	#5,R4		;SET R4 TO POS 5
60400	012104	005027	000002	3\$:	CLR	DIRTN		;CHANGE DIRECTION TO RIGHT
60500	012110	000207			RTS	PC		;EXIT
60600								
60700	012112	000000		DIRTN:	.WORD	0		;DIRECTION OF PRECESS (0=LEFT)
60800								
60900	012114	000000		PASCNT:	.WORD	0		

61100

```

LA36 ECHO TESTS
100
200
300
400
500
600
700
800
900
1000
1100
1200
1300 012116 000020
1400 012120 012166
1500 012122 104016
1600 012124 104020
1700 012125 012700
1800 012126 104010
1900 012134 022767
2000 012142 001405
2100 012143 104017
2200 012146 166444
2300 012154 000763
2400 012156 104007
2500 012160 014272
2600 012164 000757
2700
2800
2900
3000
3100
3200
3300
3400
3500
3600
3700
3800
3900 012166 000021
4000 012170 012224
4100 012172 104016
4200 012174 117777
4300 012202 016702
4400 012206 016700
4500 012213 104015
4600 012214 005302
4700 012216 003373
4800 012220 104012
4900 012222 000767

.SRTTL LA36 ECHO TESTS
;XXXXXXXXXX
;E020-- CHARACTER ECHO TEST-- ALL PRINTABLE AND
;NON-PRINTING CHARACTERS TYPED ON THE KEYBOARD
;ARE USED TO DRIVE THE PRINTER, ONE CHARACTER AT
;A TIME. A "RUBOUT" WILL CAUSE THE TEST TO BE
;TERMINATED.
;XXXXXXXXXX
E020: 20 ;TEST NUMBER
ED21 ;NEXT TEST
PRTHDR ;TYPE HEADER
1S: READ ;GO WAIT FOR KEYBOARD INPUT
MOV #30.,R0 ;DELAY FOR HALF DUPLEX
DELAY ;
CMP #177,TEMPCH ;CHECK IF RUBOUT
BEQ 2S ;BRANCH IF YES
PRNT ;NO, CHECK PRINTER READY
MOVH @TKB,@TPB ;READY, ECHO CHARACTER
2S: 1S ;PRINT TERMINATION MESSAGE
;TYPEM
;E0END
;CHAIN 1S ;CHAIN TO NEXT TEST
;BR ;REPEAT TEST
;XXXXXXXXXX
;E021-- LINE ECHO TEST, FAST RATE-- THIS TEST WILL
;CAUSE THE CONTINUAL PRINTING OF "0" AT THE MAXIMUM
;RATE UNTIL EITHER ANOTHER CHARACTER IS SELECTED
;BY PRESSING A KEY ON THE KEYBOARD OR TERMINATION BY THE
;RUBOUT.
;XXXXXXXXXX
E021: 21 ;TEST NUMBER
ED22 ;NEXT TEST
PRTHDR ;TYPE HEADER
E021A: MOV #60,REPT ;CHARACTER TO BE REPEATED (0)
1S: MOV WIDTH,R2 ;SET COLUMN COUNT
2S: MOV REPT,R0 ;GET CHAR
PRINTC ;PRINT CHAR
DEC R2 ;DEC COLUMN COUNT
DEC 2S ;FINISH LINE
CRLF ;SEND A CR AND LF
BR 1S

```

```

LA36 ECHO TESTS
5100
5200
5300
5400
5500
5600
5700
5800
5900 012224 000022
6000 012226 012476
6100 012230 104016
6200 012232 012767
6300 012240 016702
6400 012244 016700
6500 012250 104015
6600 012252 005302
6700 012254 001404
6800 012256 012700
6900 012262 104010
7000 012264 000767
7100 012266 104012
7200 012270 000763

;XXXXXXXXXX
;E022-- LINE ECHO TEST, SLOW RATE-- SAME AS E021 EXCEPT
;THAT A DELAY IS INTRODUCED BETWEEN CHARACTERS
;TO PRODUCE A LCV ACTION
;XXXXXXXXXX
E022: 22 ;TEST NUMBER
ED23 ;NEXT TEST
PRTHDR ;TYPE HEADER
E022A: MOV #60,REPT ;LOAD 0 AS INITIAL CHARACTER
1S: MOV WIDTH,R2 ;SET COLUMN COUNT
2S: MOV REPT,R0 ;GET CHAR
PRINTC ;PRINT CHAR
DEC R2 ;DEC COLUMN COUNT
BEQ 3S ;BRANCH IF DONE LINE
DELAY #3410,R0 ;DELAY 1.8 SEC.
BP 2S ;OUTPUT NEW CHAR.
3S: CRLF ;SEND A CR AND LF
BR 1S

```

LA36 ECHO TESTS					
7400	012272	116	125	114	MONIC: .ASCII /NUL /
7500	012275	040			
7600	012276	123	117	110	.ASCII /SOH /
7700	012303	140			
7800	012305	040	124	130	.ASCII /STX /
7900	012306	105	124	130	.ASCII /ETX /
8000	012311	040			
8100	012313	105	117	124	.ASCII /EOT /
8200	012315	040			
8300	012316	105	116	121	.ASCII /ENQ /
8400	012321	040			
8500	012323	103	103	113	.ASCII /ACK /
8600	012325	040			
8700	012326	102	105	114	.ASCII /BEL /
8800	012333	040	123	040	.ASCII /RS /
8900	012335	040	124	040	.ASCII /HT /
9000	012336	110			
9100	012342	114	106	040	.ASCII /LF /
9200	012345	040			
9300	012346	126	124	040	.ASCII /VT /
9400	012353	040	106	040	.ASCII /FF /
9500	012355	040			
9600	012356	103	122	040	.ASCII /CR /
9700	012363	040	117	040	.ASCII /SO /
9800	012365	040			
9900	012366	123	111	040	.ASCII /SI /
10000	012372	040	114	105	.ASCII /DLE /
10100	012375	040			
10200	012376	104	103	061	.ASCII /DC1 /
10300	012401	040	103	062	.ASCII /DC2 /
10400	012405	040	103	063	.ASCII /DC3 /
10500	012412	040	103	064	.ASCII /DC4 /
	012415	040			
	012416	116	101	113	.ASCII /NAK /
	012421	040			
	012422	123	131	116	.ASCII /SYN /
	012425	040			
	012426	105	124	102	.ASCII /ETB /
	012433	040	101	116	.ASCII /CAN /
	012435	040			
	012436	105	115	040	.ASCII /EM /

LA36 ECHO TESTS					
10600	012441	040	125	102	.ASCII /SUB /
10700	012446	123	123	103	.ASCII /ESC /
10800	012453	040	123	040	.ASCII /FS /
10900	012455	106	123	040	.ASCII /GS /
11000	012456	107			
11100	012461	040	123	040	.ASCII /RS /
11200	012465	122	123	040	.ASCII /US /
11300	012466	125			
11400	012471	040	120	040	.ASCII /SP /
	012472	123			
	012475	040			
					.EVEN



```

LA36 ECHO TESTS
;XXXXXXXXXX
;E024-- SELECTED PATTERN ECHO TEST-- SELECT 1 TO 256
; CHARACTERS- EACH WILL BE ECHOED
; AND STORED UNTIL THE CNTL/C IS SELECTED.
; AT THAT TIME ALL CHARACTERS WILL BE PRINTED AS
; A CONTINUOUS STRING UNTIL EITHER THE RRUOUT IS
; SELECTED TO TERMINATE OR THE CNTL/C IS SELECTED
; AGAIN. A TERMINATING CNTL/C FOLLOWED BY ANOTHER
; CNTL/C WILL ALWAYS CAUSE THE LAST INPUTTED STRING TO
; BE PRINTED. A TERMINATING CNTL/C FOLLOWED BY A CHARACTER OTHER THAN A
; RRUOUT WILL CAUSE A NEW STRING TO BE INPUTTED.
;XXXXXXXXXX
20200
20300
20400
20500
20600
20700
20800
20900
21000
21100
21200
21300
21400
21500 013020 000024
21600 013024 013566
21700 013024 104016
21800 013026 005000
21900 013030 012702 013164
22000 013034 104020
22100 013036 012700
22200 013042 104010
22300 013044 022767 000177 165626
22400 013052 001440
22500 013054 012702 000003 165616
22600 013062 001413
22700 013064 020127 000400
22800 013070 103367
22900 013072 116922 165692
23000 013076 005201
23100 013100 104017
23200 013102 116777 165572 165510
23300 013110 000751
23400
23500
23600
23700 013112 020227 013164
23800 013116 001463
23900 013120 116722 165554
24000 013124 104010
24100 013126 012702 013164
24200 013132 022727 000003
24300 013136 001433
24400 013140 112200
24500 013142 005177 000003
24600 013146 005177
24700 013150 104015
24800 013152 000772
24900 013154 104007
25000 013156 014272
25100 013160 104605
25200 013162 000721
25300 013164 000003
25400 013166
;
;SECTION TO OUTPUT CONTINUOUS STRING
;OUTPUT:
;CMP R2,#BUFR ;CHECK IF POINTER IS AT START OF TABLE
;REQ 15 ;YES, BRANCH
;MOVB TEMPCH,(R2)+ ;NO, STORE ^C IN TABLE
;SCPLF ;SEND A CR LF
;MOV #BUFR,R2 ;BUFFER ADDRESS TO R2
;CMP (R2),#3 ;CHECK IF CHAR IS ^C
;REQ ED246 ;YES, LOOK FOR INPUT AGAIN
;MOVB (R2),#R0 ;GET CHARACTER
;REQ R0,#3 ;DONE STRING?
;PRINTC ;RESTART STRING
;BR 15 ;PRINT CHAR
;TERM: TYPEN 2S ;CONTINUE
;ECHOEND ;OUTPUT TERMINATION MESSAGE
;CHAIN ;CHAIN TO NEXT TEST
;BR E024B ;REPEAT TEST
;BUFR: 3 ;INITIALIZE FIRST CHAR AS CNTL-C IN TABLE
; ;256 CHARACTER BUFFER
;BLKB 256.

```

```

LA36 ECHO TESTS
;XXXXXXXXXX
;E025-- BELL ECHO TEST-- A MESSAGE IS PRINTED AND
; THE TEST WAITS FOR SOME PRINTABLE CHARACTER
; TO BE SELECTED ON THE KEYBOARD (GT040). THIS
; TEST IS VALID ONLY IF THE PAPER WIDTH IS GT 64
; COLUMNS- IF LTR & COLUMNS AN ILLEGAL BELL TEST
; MESSAGE IS PRINTED.
;XXXXXXXXXX
25600
25700
25800
25900
26000
26100
26200
26300
26400
26500
26600
26700 013566 000025
26800 013570 012116
26900 013572 104016
27000 013574 026727 165052 000101
27100 013602 103367
27200 013604 104007
27300 013606 014145
27400 013610 000482
27500 013612 104000
27600 013614 014145
27700 013616 104020
27800 013620 012760 000036
27900 013624 026727
28000 013626 104010 165046 000040
28100 013634 103770
28200 013636 022767 000177 165034
28300 013640 104010
28400 013646 104017
28500 013650 116777 165024 164742
28600 013656 104013
28700 013660 000754
28800 013662 104007
28900 013664 014245
29000 013666 104007
29100 013670 014272
29200 013672 104005
29300 013674 000737
;
;E025:
;E020 ;TEST NUMBER
;PTHDR ;NEXT TEST HEADER
;PRINTC ;PRINT HEADER
;REQ WIDTH,#101 ;TEST IF COLUMN COUNT IS EQ,GT 64
;REQ 4S ;BRANCH IF NOT
;TYPEN ;TYPE TEST MESSG
;BR 3S ;WAIT FOR CHAR
;TYPEN ;TYPE TRST MESSG ON TERM CHAR RCVD ON
;REQ ED25MA ;WAIT FOR OPERATOR RESPONSE
;READ #30,#R0 ;DELAY FOR HALF DUPLEX
;DELAY
;CMP TEMPCH,#40 ;TEST IF PRINTABLE
;REQ 3S ;BRANCH IF NON-PRINTABLE
;CMP #177,TEMPCH ;CHECK IF CHAR IS RRUOUT
;REQ 5S ;BRANCH IF YES
;PRINTC ;CHECK IF PRINTER IS READY
;SCPLF ;PRINT CHAR. (BELL SHOULD SOUND)
;BR 2S ;REPEAT
;TYPEN ;TYPE ERROR MESSAGE
;E025MB ;REPEAT TEST
;ECHOEND ;PRINT TERMINATION
;CHAIN ;EXIT TO NEXT TEST
;BR 1S ;REPEAT TEST

```





014135	114	125	115	
014140	116	123	200	
014143	012	000		
1200 014145	124	133	120	E025MA: .ASCII /TYPE ANY PRINTABLE CHARACTER /
014146	105	040	101	
014153	116	131	040	
014156	120	122	111	
014164	105	124	103	
014167	040	103	110	
014172	101	122	101	
014177	103	040	105	
014200	103	040		
1300 014202	101	116	104	.ASCIZ /AND LISTEN FOR BELL...../
014205	040	114	111	
014210	123	124	105	
014213	116	040	106	
014216	117	122	040	
014221	102	105	114	
014224	114	056	056	
014232	056	056	056	
014235	056	056	056	
014240	056	056	056	
1400 014245	200	116	117	E025MB: .ASCIZ <ACRLF>/NOT ENOUGH COLUMNS/<ACRLF>
014250	124	040	105	
014253	116	117	125	
014256	105	117	040	
014261	103	117	114	
014264	125	115	116	
014267	103	200	000	
1500 014275	110	117	040	E025MC: .ASCIZ <ACRLF>/ECHO TEST TERMINATED/<ACRLF>
014300	124	105	123	
014303	104	040	124	
014306	105	123	124	
014311	111	116	101	
014314	124	105	104	
014317	200	000		
1600 014321	040	040		E023M: .ASCII / / / ;MSG FOR TEST E024
1700 014323	040	040		LINE5A: .ASCIZ / / <ACRLF>
014326	040	040		
014327	040	040		
014335	040	040		
014340	000			
1900 014341	209	017	012	MESG3: .ASCIZ <ACRLF><1><12>/SELECT TEST NUMBER /
014344	105	103	124	
014347	105	103	124	
014352	040	124	105	
014359	122	123	040	
014363	102	123	115	
014366	040	105	122	
2000 014371	105	000	000	EVEN: .ASCII /EVEN/
014374	116	126	105	

2100 014375	117	104	104	ODD: .ASCII /ODD /
014400	040			
2200 014401	124	131	120	OPMSG: .ASCIZ /TYPE ANY CHARACTER/
014404	105	040	101	
014407	116	131	040	
014412	103	110	101	
014420	124	105	103	
014423	000		122	
2300 014424	125	123	105	NOSWR: .ASCIZ /USE SOFTWARE SWITCH REG AT MEMORY ADDR 176/<7>
014427	140	123	117	
014432	106	124	127	
014435	101	122	105	
014440	040	123	127	
014443	111	124	127	
014446	110	040	122	
014451	105	107	040	
014454	101	124	040	
014457	115	105	115	
014462	117	122	131	
014465	040	101	104	
014470	104	122	040	
014473	067	067	066	
014476	009	000		
2400				
2500				
2600	000001			.END

ACRFL = 000200	CHAINN 001412	EO25HA 014145	PRCTAB 002522	START3 000772
ADJBR4 012032	CHAINV 001534	EO25MR 014245	PRINTC= 104015	STLSRV 003406
ADJENP 004100	CHALT = 104006	ERR 003320	PRNT = 104017	STLSRV= 003356
AREAD = 104021	CHLT 000720	ERRHLT = 003354	PRTHDR= 104016	STPCHV= 104004
AT0 = 002296	CKPOS 011764	ERRR = 104001	PRV4 = 000200	STPA 003374
AT1 = 005320	CNTLSW 000634	ERRR1 = 104001	PRV7 = 000340	STRDRV= 104003
AT10 005744	CNTR 000716	FORWD = 104024	PSW = 177776	STRDRV= 104003
AT11 006002	CNVCTR 004072	FORWDA 003614	PTD 007472	STRN 012560
AT12 006042	CNADD 000602	FORWDB 003622	PT1 007448	SWREG 000176
AT13 006116	CNIT 003710	FSTDL 000632	PT10 011266	TEMP 000712
AT14 006176	CONSET 003714	HDRMSC 014113	PT11 011424	TEMPCH 000700
AT15 006262	CONVEC 000604	HERE 011532	PT12 011456	TEMPWR 000476
AT16 006282	CONVT3 014055	ICTR 000660	PT17A 011464	TERM 013154
AT17 006430	CR = 104055	ICTR 000660	PT17B 011546	TESTC 002460
AT2 = 005352	CRBUF = 000646	IDEZ 000776	PT17D 011576	TIMR 000672
AT20 005500	CRLF = 104012	INCHK 000710	PT2 007570	TKB 000614
AT21 005572	CRRA 000650	LEVEL 000654	PT3 010164	TKLVL 000624
AT22 005672	CRTST 000676	F = 104014	PT3 010164	TKS 000612
AT23 005700	DELAY = 104010	LFCNT 000706	PTA 010304	TKVTR 000642
AT24 005712	DIGIT 004074	LINE3 010444	PTS 010462	TMB 000620
AT25 005722	DIRTH 012112	LINES 014323	PT5AL 010630	TPBS 004004
AT26 005770	DISPRE 000174	LOGYCA 014327	PT6 010666	TPLVL 000630
AT3 = 005404	DLADR 000606	LS111 = 001000	PT7 011054	TPS 000616
AT4 = 005436	DLCMT 000656	MONIC 000004	READ = 104020	TPSS 004002
AT5 = 005436	DLNR 000610	MESG3 014341	READC = 104025	TPVTR 000620
AT6 = 005604	DLY = 003436	MG24 013010	READI = 004212	TTVCTL= 104011
AT7 = 005674	DL11S 014051	MG25 013014	REP 010414	TTY1 001776
BIT0 = 000000	DL11S1 014064	MONIC 013014	REPT 000662	TTYB 002062
BIT1 = 000000	EOGPHD = 104002	MOVNUM 012736	RTNND 000636	TYP 003076
BIT10 = 002000	EHLT = 003346	NEXT 001654	SAVR6 003514	TYPE = 104000
BIT11 = 004000	EMTINT 022722	NEXT1 001674	SCOPSW= 040000	TYPEM = 104007
BIT12 = 010000	EMTAB 022776	HITRSW= 004000	SCOPR 000642	TYPM 003164
BIT13 = 020000	ENPAS 014023	NOSMR 014424	SCRLF = 104013	WIF 001700
BIT14 = 040000	END2 001332	NPCODE 010137	SELHLT 000734	WIDTH 000652
BIT15 = 100000	END2A 001320	NXTST 000640	SEK 01630	XCSR 000670
BIT2 = 000004	END3 01262	ODD 014375	SKP 000674	XREAD 003640
BIT3 = 000010	END4 011334	OPFN = 000000	SKRET 03072	XRTASC 004006
BIT4 = 000020	EO20 012116	OPMSG 014401	SPPROT 000600	SCR 003226
BIT5 = 000040	EO21 012166	OUTPUT 013112	SPC 007560	SCRFL 003214
BIT6 = 000100	EO21A 012174	PARTY 000702	SPCNT 000674	SPRWD 003562
BIT7 = 000224	EO22 012224	PASNT 012114	SPSP 007532	SF 003216
BIT8 = 000400	EO22A 012232	PASNES 014042	SR 000714	SPRDR 003336
BIT9 = 001000	EO23 012476	PCHAR 000704	SR 000714	SPRNT 004314
BRCR 000654	EO23M 014321	PFAIL 003460	START 01010	SPRTC 004324
BTASC = 104023	EO24 013020	POPSP = 005726	STARTM 013676	SREAD 004112
BUFR = 013164	EO24B 013026	POPSP2= 022626	STARTX 001024	SREADC 004204
CHAIN = 104005	EO25 013566	PRGD 000644	START1 000736	SSCRLF 003142
			START2 000754	

- ABS. 014500 000  
 000000 001  
 ERRORS DETECTED: 0

VIRTUAL MEMORY USED: 2846 WORDS ( 12 PAGES)  
 DYNAMIC MEMORY: 3844 WORDS ( 14 PAGES)  
 ELAPSED TIME: 00:00:52  
 CZLACE.BIN,CZLACE.LST/-SP=CZLACE.MAC