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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DCMFA-B4-D  
PRODUCT NAME: COMBINED MS-11 (MOS PARITY) AND MF11-LP,MA11-P (CORE)  
PARITY MEMORY TESTS (SUPERSEDES DCMS-A-D)  
DATE CREATED: MAY 11, 1973  
MAINTAINER: DIAGNOSTIC GROUP  
AUTHOR: JIM KAPADIA  
MCO DATE: SEPTEMBER 16, 1974

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34 1.0 ABSTRACT  
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36 THIS PROGRAM LOCATES THE PARITY MEMORY REGISTERS FOR BOTH THE  
37 CORE AND MOS PARITY MEMORIES AND PERFORMS A CHECK OF THE BITS IN EACH.  
38 IT THEN CREATES A MAP SHOWING THE MEMORY CONTROLLED BY EACH PARITY  
39 REGISTER, THE PARITY REGISTERS AND THE MEMORY ARE THEN TESTED USING  
40 THE INFORMATION IN THE MAP.  
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42 2.0 REQUIREMENTS  
43  
44 2.1 EQUIPMENT  
45  
46 PDP-11 WITH MF11-LP OR MA11-P PARITY MEMORY (CORE), MS-11 (MOS) PARITY MEMORY  
47  
48 2.2 STORAGE  
49  
50 THE PROGRAM REQUIRES 4K OF MEMORY.  
51 3.0 LOADING PROCEDURE  
52  
53 LOAD PROGRAM INTO MEMORY USING ABS LOADER.  
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55 4.0 STARTING PROCEDURE  
56  
57 4.1 STARTING ADDRESSES  
58  
59 200= NORMAL (WORST CASE) TESTING  
60 210= ROUTINE TO RESTORE THE LOADER  
61 220= ROUTINE TO SCAN FOR BAD PARITY  
62 230= RESTART OF NORMAL TESTING- USES PREVIOUS MAP OF PARITY MEMORY  
63  
64 4.2.1 PROGRAM AND/OR OPERATOR ACTION  
65  
66 LOAD STARTING ADDRESS.  
67 SET DESIRED SWITCH REGISTER SETTINGS (SEE 5.1- ALL DOWN FOR WORST CASE).  
68 PRESS START.  
69 IF SA 200 OR RESTART ADDRESS 230 IS USED, THE BELL WILL RING AT THE  
70 COMPLETION OF EACH PASS AND END PASS= XXX WILL BE TYPED (WHERE XXX  
71 IS THE NUMBER OF PASSES COMPLETED SINCE THE PROGRAM WAS LAST STARTED).  
72 IF SA 210 OR SA 220 IS USED, THE PROGRAM WILL HALT WHEN DONE.  
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5.0 OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

SW 15=1 OR UP -- HALT ON ERROR  
SW 14=1 OR UP -- SCOPE LOOP  
SW 13=1 OR UP -- INHIBIT PRINTOUT  
SW 11=1 OR UP -- INHIBIT ITERATIONS  
SW 10=1 OR UP -- HALT AFTER LOCATING BAD PARITY BEFORE CORRECTING IT  
(USED IN PARITY SCAN ROUTINE ONLY)  
SW 09=1 OR UP -- HALT AFTER THE PARITY MEMORY MAP HAS BEEN PRINTED  
(ALLOWS MANUAL CHANGES TO FORCE TESTING OF MEMORY  
THAT WAS NOT LOCATED)  
SW 08=1 OR UP -- HALT AT END OF PASS (IF HALTED ELSEWHERE, THE  
PROGRAM MAY BE RELOCATED TO BANK 1, BAD PARITY MAY  
EXIST IN MEMORY, AND/OR WRITE WRONG PARITY MAY  
BE SET)

5.2 SUBROUTINE ABSTRACTS

5.2.1 BEGIN SA 200, RESTART 230

5.2.2 SCOPE

THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUBTEST IN THE INSTRUCTION SECTION. IT RECORDS THE STARTING ADDRESS OF EACH SUBTEST AS IT IS BEING ENTERED. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUBTEST THAT THE SCOPE LOOP IS REQUESTED FOR. IF SCOPE LOOP IS NOT REQUESTED, THERE WILL BE 64 ITERATIONS OF THAT SUBTEST BEFORE THE NEXT SUBTEST IS ENTERED (EXCEPT IN THOSE ROUTINES WHERE IMAX IS CHANGED). SWITCH 11 ON A ONE INHIBITS ITERATION OF SUBTESTS.

5.2.3 ERROR HANDLERS (ERRST,ERRP,ERR)

THESE ROUTINES ARE CALLED VIA EMTS TO PRINT OUT ERROR INFORMATION. (SEE 6.0 FOR DESCRIPTION OF ERROR INFORMATION)

5.2.4 PSCAN (SCAN MEMORY FOR BAD PARITY)

THIS ROUTINE READS ALL LOCATIONS IN MEMORY AND PRINTS OUT THE PHYSICAL ADDRESSES (18 BITS) OF THOSE LOCATIONS CONTAINING BAD PARITY. IT IS UTILIZED WITHIN THE PROGRAM WHILE EXERCISING MEMORY IF A PARITY ERROR OCCURS UNEXPECTEDLY, AND MAY ALSO BE CALLED USING STARTING ADDRESS 220.

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5.2.5 \$TYPE (ASCII MESSAGE TIMEOUT ROUTINE)

THIS IS THE STANDARD TIMEOUT ROUTINE, ALLOWING PATCHING TO UTILIZE OUTPUT DEVICES OTHER THAN THE ASR 33. \$NULL CONTAINS THE VALUE TO BE USED AS A FILLER CHARACTER, AND \$FILLS CONTAINS A NUMBER INDICATING THE NUMBER OF FILLER CHARACTERS REQUIRED. TPS AND TPB CONTAIN THE STATUS AND BUFFER REGISTER ADDRESSES OF THE OUTPUT DEVICE.

5.2.6 TRAPCATCHER

THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION 0 DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS AND INTERRUPTS TO THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE NEXT LOCATION. THE NEXT LOCATION IS LOADED WITH A HALT (000000). THUS AN ILLEGAL TRAP OR INTERRUPT WILL CAUSE A HALT AT THE TRAP LOCATION PLUS TWO.

IF A HALT OCCURS IN THE TRAP OR INTERRUPT AREA, EXAMINE REGISTER SIX. IT WILL CONTAIN THE CURRENT STACK ADDRESS. THE CONTENTS OF THE CURRENT STACK ADDRESS IS THE VALUE OF THE LOCATION COUNTER WHEN THE TRAP OR INTERRUPT OCCURRED.

5.3 PROGRAM AND/OR OPERATOR ACTION

5.3.1 ALTERING THE PARITY MEMORY MAP

IF THE MAP TYPED AT RUN TIME DOES NOT AGREE WITH THE HARDWARE PRESENT THE MAP CAN MANUALLY BE CHANGED TO ALLOW TESTING OF PARITY MEMORY THAT THE MAPPER DID NOT FIND. SETTING SWITCH 9 TO A 1 WILL CAUSE THE PROGRAM TO HALT AFTER THE MAP IS TYPED. AFTER THE HALT, MODIFY THE MAP AS DESIRED (SEE THE DESCRIPTION IN THE LISTING- THE MAP BEGINS AT LOCATION 600). THEN PRESS CONTINUE. THE NEW MAP WILL BE PRINTED, AND IF SW9 IS STILL SET THE PROCESS WILL BE REPEATED. IF SW9 IS NOT SET, THE PROGRAM WILL TEST PARITY MEMORY USING THE NEW MAP.

5.3.2 STOPPING THE PROGRAM

BECAUSE THE PROGRAM RELOCATES ITSELF TO BANK 1 WHILE TESTING BANK 0, A SWITCH IS PROVIDED TO HALT THE PROGRAM AT THE END OF A PASS. SETTING THIS SWITCH (SW9) WILL CAUSE THE PROGRAM TO HALT IN BANK 0 AT THE END OF THE CURRENT PASS (AFTER OUTPUTTING THE END OF PASS MESSAGE).

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6.0 ERRORS

6.1 ERROR PRINTOUTS

THERE ARE THREE TYPES OF ERROR MESSAGES USING COMBINATIONS OF THE FOLLOWING ERROR TYPE ROUTINES.

PC=ZZZZZZ PC OF FAILING ERROR CALL. REFER TO THIS ADDRESS IN THE LISTING FOR AN EXPLANATION OF THE ERROR.

ICNT=YYYYYY CURRENT ITERATION COUNT OF FAILING TEST.  
MPR=XXXXXX ADDRESS OF PARITY REGISTER UNDER TEST.  
MPR DATA=VVVVVV CONTENTS OF PARITY REGISTER UNDER TEST.  
TEST LOC=XXXXXX MEMORY LOCATION UNDER TEST  
S/B: XXXXXX CONTENTS OF MEMORY LOCATION SHOULD BE.  
WAS: XXXXXX CONTENTS OF MEMORY LOCATION WAS.

6.2 DETERMINING ADDRESS OF TEST LOCATION WHEN KT11 IS PRESENT

IN MOST OF THE SUBTESTS, IF A KT11 IS PRESENT IT IS USED. IN ALL CASES IN THIS PROGRAM, WHEN THE KT11 IS ON, KERNEL PAGE 0 IS USED TO REFERENCE BANK 0 AND KERNEL PAGE 7 IS USED TO REFERENCE THE EXTERNAL BANK. IN MOST CASES, KERNEL PAGE 1 IS USED TO REFERENCE THE MEMORY CURRENTLY UNDER TEST. SINCE THE USE OF THE MEMORY MANAGEMENT OPTION IS SIMILAR THROUGHOUT THE PROGRAM, IT IS EASY TO DETERMINE THE ACTUAL (PHYSICAL) MEMORY ADDRESS BEING TESTED.

TO CALCULATE A PHYSICAL ADDRESS, ADD THE STARTING ADDRESS OF THE BANK BEING TESTED TO THE OFFSET WHICH GIVES THE ADDRESS WITHIN THE BANK. SINCE IN THIS PROGRAM ALL RELOCATED MEMORY TESTING IS DONE THRU KERNEL PAGE 1, KERNEL PAGE ADDRESS REGISTER 1 (ADDRESS 772342) WILL ALWAYS CONTAIN THE STARTING ADDRESS OF THE BANK. ACTUALLY, KERNEL PAGE ADDRESS REGISTER 1 (KPAR1) CONTAINS JUST THE TOP 12 BITS OF THE BANK STARTING ADDRESS. ADDING TWO ZEROES (OCTAL) TO THE RIGHT OF THIS VALUE WILL GIVE YOU THE FULL 18 BIT ADDRESS OF THE BANK. THE VIRTUAL ADDRESS USED TO REFERENCE THIS BANK UNDER TEST WILL ALWAYS START WITH 001 (BINARY, TOP 3 OF 16 BITS). THIS REFERENCES PAGE 1. THE LOWER 13 BITS GIVE THE ADDRESS WITHIN THE BANK- ADD THEM TO THE STARTING ADDRESS OF THE BANK TO GET THE FULL 18 BIT PHYSICAL ADDRESS.

FOR EXAMPLE, AN ERROR COMMENT MAY SAY "R1 CONTAINS THE ADDRESS OF THE TEST LOCATION (VIRTUAL THRU KERNEL PAGE 1 IF KT11 PRESENT)." R1 MIGHT CONTAIN 32000, AND KERNEL PAGE ADDRESS REGISTER 1 (LOCATION 772342) MIGHT CONTAIN 2400. FIRST GET THE STARTING ADDRESS OF THE BANK BY ADDING 2 ZEROES TO THE RIGHT OF THE NUMBER IN KPAR1. THUS THE VALUE 2400 INDICATES THAT THE BANK STARTS AT 240000. SECOND, CALCULATE THE OFFSET WITHIN THE BANK. THE VIRTUAL ADDRESS 32000 BREAKS DOWN INTO 1(TOP 3 BITS) WHICH REFERENCES KPAR1, AND 12000 (LOWER 13 BITS) WHICH IS THE OFFSET. THE OFFSET (12000) TO THE BANK

DCMFA,B MACY11,624 18-JUN-73 15:38 PAGE 6  
DCMFAB

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ADDRESS (240000) TO GET THE ACTUAL PHYSICAL ADDRESS BEING TESTED  
(252000).

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6.3 ERROR RECOVERY

IN GENERAL, TEST FAILURES WILL PRINTOUT AN ERROR MESSAGE AND CONTINUE. IF THE HALT ON ERROR SWITCH IS SET, HITTING CONTINUE WILL RECOVER. IF THE PROGRAM HANGS UP IN A LOOP, THE ERROR IS LIKELY TO BE A SIGNAL WHICH WAS NEVER RECEIVED. IF A HALT OCCURS IN THE TRAP AND VECTOR AREA THE PROGRAM MUST BE RESTARTED. IF THE PROGRAM HALTS IN THE MAIN FLOW, CONSULT THE LISTING IF NO MESSAGE IS TYPED OUT.

6.4 ERRORS WHILE TESTING BANK ZERO (ERROR PC VALUES ABOVE 20000)

TEST20 AND TEST21 CHECK BANK 0 IF IT HAS PARITY MEMORY. TO DO THIS, THE CODE IS RELOCATED TO AND EXECUTED FROM BANK 1. THE ERROR PRINTOUTS WILL THUS GIVE THE PC IN BANK 1 OF THE ERROR CALL. SINCE ALL LOCATIONS HAVE BEEN MOVED UP 20000, SUBTRACT 20000 FROM THE ERROR PC TO GET THE ADDRESS IN THE LISTING WHICH CORRESPONDS TO THE PRINTOUT.

7.0 RESTRICTIONS

7.1 STARTING PROCEDURE

PROGRAM MUST BE LOADED INTO LOWER 4K OF MEMORY.

7.2 OPERATING RESTRICTION- AVOID USING THE "HALT" SWITCH

IF THE PROGRAM IS HALTED AT A RANDOM POINT DURING EXECUTION, SEVERAL PROBLEMS MAY ARISE. THE PROGRAM MAY BE RELOCATED TO BANK 1 AT THE TIME IT IS STOPPED, IN WHICH CASE NONE OF THE STANDARD STARTING ADDRESSES WILL WORK. WRITE WRONG PARITY MAY BE SET, IN WHICH CASE YOU MAY ENTER BAD PARITY WHILE PATCHING. AND MEMORY MAY CONTAIN BAD PARITY SINCE YOU MAY BE IN THE MIDDLE OF A TEST WHICH UTILIZES WRITE WRONG PARITY. IT IS THEREFORE STRONGLY RECOMMENDED THAT YOU HALT THE PROGRAM VIA THE "HALT AT END OF PASS" SWITCH (SW8) OR THE "HALT ON ERROR" SWITCH (SW15) RATHER THAN VIA THE HALT/ENABLE SWITCH.

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8.0 MISCELLANEOUS

8.1 EXECUTION TIME

EXECUTION TIME DEPENDS ON THE AMOUNT OF PARITY MEMORY UNDER TEST.  
IT TAKES ABOUT 1 MINUTE TO TEST 24K OF PARITY MEMORY (1 PASS).

8.2 STACK POINTERS

THE KERNEL STACK POINTER IS INITIALIZED TO 510.

9.0 PROGRAM DESCRIPTION

THIS PROGRAM FIRST LOCATES MA11 & MF11 CORE PARITY AND MS-11 MOS PARITY CONTROL  
REGISTERS BY ADDRESSING EACH POSSIBLE REGISTER ADDRESS AND CHECKING THOSE WHICH  
DO NOT TIME OUT. ON DETECTING THE PRESENCE OF A PARITY REGISTER  
THE PROGRAM CHECKS IF IT IS A CORE PARITY OR A MOS PARITY REGISTER  
AND ACCORDINGLY STORES THIS INFORMATION IN AN INDICATOR(INDC0-INDC15)  
THE ADDRESSES OF THE REGISTERS ARE RECORDED  
AND OUTPUT TO THE CONSOLE DEVICE, AND THEN THE REGISTERS ARE  
CHECKED TO SEE THAT THE CORRECT BITS ARE R/W. RESET IS USED TO TEST  
THE EFFECT OF INIT. PARITY MEMORY IS THEN LOCATED BY SETTING WRITE  
WRONG PARITY IN ALL REGISTERS AND WRITING AND READING THE FIRST 4  
ADDRESSES IN EACH 4K. EACH TIME A PARITY REGISTER RECORDS A PARITY  
ERROR, THE MAP IS ALTERED TO INDICATE THAT THAT REGISTER  
CONTROLS THE MEMORY BEING ADDRESSED. THE FINAL MAP IS PRINTED AND  
THEN THE PARITY CONTROL LOGIC IS CHECKED USING THE PARITY MEMORY  
FOUND. SEVERAL PATTERNS ARE WRITTEN INTO EACH PARITY MEMORY  
LOCATION TO SEE THAT NO PARITY ERRORS ARE CREATED. FINALLY, EACH  
BYTE OF PARITY MEMORY IS WRITTEN WITH BOTH GOOD AND BAD PARITY TO  
SHOW THAT THE PARITY BITS CAN BE TOGGLED AND SENSED.  
SINCE THIS IS A COMBINED DIAGNOSTIC, AS FAR AS POSSIBLE  
COMMON TESTS ARE USED FOR BOTH CORE AND MOS. ONLY WHERE THE  
MOS CONTROLLER DEFERS FUNCTIONALLY FROM THE CORE, THE  
INDICATOR IS CHECKED FOR MOS OR CORE AND THE MEMORY  
IN QUESTION IS TESTED ACCORDINGLY.  
A DETAILED EXPLANATION OF THE MAP IS GIVEN IN THE LISTING  
(PAGE 9-12).  
THE DISPLAY REGISTER CONTAINS THE NUMBER OF THE TEST  
BEING EXECUTED.

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419 000536 000000 WAS: 0 ;ACTUAL VALUE FOUND
420 000540 000000 TRDATA: 0
421 000542 000000 MPROK: 0
422 000544 000000 PASCNT: 0 ;PASS COUNT
423 000546 000000 TBANK: 0
424 000550 000000 MEMUT: 0
425 000552 000000 MOKT: 0 ;SET TO INDICATE NO K111 PRESENT
426 000554 000000 HIWORD: 0
427 000556 000000 LOWFLG: 0
428 000560 000000 ODDFLG: 0 ;IF SET INDICATES TESTING HIGH BYTE
429 ;OF MEMORY LOCATION
430 000562 000000 TEMP: 0
431 000564 000000 MTYFG: 0 ;SET TO INDICATE MAP OF PARITY MEMORY
432 ;ALREADY TYPED
433 000566 000000 RELOC: 0
434
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436
437 ;MEMORY PARITY CONTROL REGISTER ADDRESSES
438 ;THE LEAST SIGNIFICANT BIT IN THE DEVICE ADDRESS IS SET TO A ONE(1)
439 ;IF THE CONTROL IS FOUND NOT TO BE PRESENT, THE MEMORY PRESENT UNDER
440 ;CONTROL OF EACH CONTROLLER IS REPRESENTED BY 2 OCTAL WORDS, EACH BIT
441 ;REPRESENTS A 4K BLOCK, I.E. BIT0= 0-4K, BIT1= 4-8K, BIT15= 60-64K.
442 ;THE LOW BYTE OF THE LAST WORD FOR EACH REGISTER INDICATES THE OFFSET (0,2,4,OR 6)
443 ;FOR THE FIRST ADDRESS THAT ACTUALLY CORRESPONDED TO THE REGISTER, THE HIGH BYTE GETS
444 ;SET TO 1 TO INDICATE THAT A MEMORY ADDRESS HAS BEEN FOUND FOR THAT REGISTER.
445 ;FOR EXAMPLE, SAY THAT MPRO AND MPR1 EXIST, CONTROLLING INTERLEAVED MEMORY
446 ;FROM 0 TO 16K, AND THAT MPRO CONTRLS THE ADDRESSES ENDING IN 0 AND 4.
447 ;THE MAP WOULD THEN LOOK AS FOLLOWS:
448 ; MPRO: 172100 ;BIT 0 IS CLEAR SINCE REGISTER IS PRESENT
449 ; 17 ;REGISTER CONTROLS 1ST 16K (=4 BANKS)
450 ; 0
451 ; 400 ;LOW BYTE SHOWS THAT FIRST ADDRESS
452 ; ;ENDS IN 0 (OCTAL)
453 ; ;HIGH BYTE CONTAINS A 1 TO INDICATE
454 ; ;THAT AN ADDRESS WAS FOUND
455 ; MPR1: 172102 ;BIT 0 IS CLEAR SINCE REGISTER IS PRESENT
456 ; 17 ;REGISTER CONTROLS 1ST 16K
457 ; 0
458 ; 402 ;LOW BYTE INDICATES THAT THE FIRST
459 ; ;MEMORY ADDRESS ENDS IN 2 (OCTAL)
460 ; ;HIGH BYTE CONTAINS A 1 TO INDICATE
461 ; ;THAT AN ADDRESS WAS FOUND
462 ;THE REST OF THE MAP WOULD APPEAR AS IN THE LISTING
463
464 000570 172101 MPRO: 172100+1 ;PARITY STATUS REGISTERS
465 000572 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
466 000574 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
467 000576 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
468 000600 172103 MPR1: 172102+1
469 000602 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
470 000604 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
471 000606 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
472 000610 172105 MPR2: 172104+1

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473 000612 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
474 000614 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
475 000616 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
476 000620 172107 MPR3: 172106+1
477 000622 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
478 000624 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
479 000626 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
480 000630 172111 MPR4: 172110+1
481 000632 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
482 000634 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
483 000636 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
484 000640 172113 MPR5: 172112+1
485 000642 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
486 000644 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
487 000646 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
488 000650 172115 MPR6: 172114+1
489 000652 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
490 000654 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
491 000656 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
492 000660 172117 MPR7: 172116+1
493 000662 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
494 000664 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
495 000666 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
496 000670 172121 MPR8: 172120+1
497 000672 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
498 000674 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
499 000676 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
500 000700 172123 MPR9: 172122+1
501 000702 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
502 000704 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
503 000706 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
504 000710 172125 MPR10: 172124+1
505 000712 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
506 000714 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
507 000716 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
508 000720 172127 MPR11: 172126+1
509 000722 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
510 000724 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
511 000726 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
512 000730 172131 MPR12: 172130+1
513 000732 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
514 000734 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
515 000736 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
516 000740 172133 MPR13: 172132+1
517 000742 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
518 000744 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
519 000746 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
520 000750 172135 MPR14: 172134+1
521 000752 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
522 000754 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL
523 000756 000000 0 ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
524 000760 172137 MPR15: 172136+1
525 000762 000000 0 ;0-64K PARITY MEM UNDER THIS CONTROL
526 000764 000000 0 ;64-124K PARITY MEM UNDER THIS CONTROL

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527 000766 000000          0          ;ADDRESS RESPONSE THIS CONTROL (0,2,4,6)
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529 000770 000000          TRZG1 0          ;PARITY REGISTER UNDER TEST
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542 000772 000000          INDC01 0          ;CORE-MOS PARITY INDICATOR FOR MPR
543 000774 000000          INDC11 0          ;CORE-MOS PARITY INDICATOR FOR MPR1
544 000776 000000          INDC21 0          ;CORE-MOS PARITY INDICATOR FOR MPR2
545 001000 000000          INDC31 0          ;CORE-MOS PARITY INDICATOR FOR MPR3
546 001002 000000          INDC41 0          ;FOR MPR4
547 001004 000000          INDC51 0          ;FOR MPR5
548 001006 000000          INDC61 0          ;FOR MPR6
549 001010 000000          INDC71 0          ;FOR MPR7
550 001012 000000          INDC81 0          ;FOR MPR8
551 001014 000000          INDC91 0          ;FOR MPR9
552 001016 000000          INDC101 0         ;FOR MPR10
553 001020 000000          INDC111 0         ;FOR MPR11
554 001022 000000          INDC121 0         ;FOR MPR12
555 001024 000000          INDC131 0         ;FOR MPR13
556 001026 000000          INDC141 0         ;FOR MPR14
557 001030 000000          INDC151 0         ;FOR MPR15
558 001032 000000          RESRVD1 0
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561 001034 070032          RESVC1 70032      ;BIT POSITIONS WHICH ARE RESERVED
562 001036 077772          RESVM1 77772      ;FOR FUTURE USE IN PARITY REGISTERS
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568 001040 125325          ;PARITY PATTERNS
569 001042 152652          PARPAT1 125325    ;EVEN, ODD BYTES
570 001044 052452          152652           ;ODD, EVEN
571 001046 025125          052452           ;EVEN, ODD
572 001050 102070          025125           ;ODD, EVEN
573 001052 072527          102070           ;EVEN, EVEN
574 001054 177777          072527           ;ODD, ODD
575 001056 107030          177777           ;EVEN, EVEN
576 001060 152525          107030           ;ODD, ODD
577 001062 000000          152525           ;ODD, EVEN
578 001064 000000          0                ;EXTRA PATTERN AREA
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582 001066 000000          ;THIS IS A MAP OF THE TOTAL MEMORY PRESENT IN THE SYSTEM.
583 001070 000000          MEML1 0           ;0-64K MEM PRESENT IN 4K CONTIGUOUS BLOCKS
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585
586 001072 000000          MEMH1 0           ;64-124 MEM PRESENT IN 4K CONTIGUOUS BLOCKS
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601 001100 177564          ;THIS IS A MAP OF THE TOTAL PARITY MEMORY PRESENT IN THE SYSTEM.
602 001102 177566          PMEML1 0         ;0-64K PARITY MEMORY PRESENT
603 001104 000           ;(IN 4K CONTIGUOUS BLOCKS)
604 001105 002           PMEMH1 0         ;64-124K PARITY MEMORY PRESENT
605 001106 000           ;(IN 4K CONTIGUOUS BLOCKS)
606 001107 000           PMEMX1 0         ;TEMP TO HOLD CONTENTS OF EITHER
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;ROUTINE TO TYPE ASCII MESSAGES, MESSAGE MUST TERMINATE WITH A 0 BYTE.
;THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.
;NOTE1: #NULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.
;NOTE2: #FILLS CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.

        .=1100
TPS:    177564          ;PRINTER STATUS REGISTER ADDRESS
TPB:    177566          ;PRINTER BUFFER REGISTER ADDRESS
#NULL:  .BYTE 0        ;CONTAINS NULL CHARACTER FOR FILLS
#FILLS: .BYTE 2        ;CONTAINS # OF FILLER CHARACTERS REQUIRED
#TPFLG: .BYTE 0        ;"TERMINAL AVAILABLE" FLAG (0=YES)
        .BYTE 0        ;RESERVED

608 001110 105767 177772  #TYPE: TST# #TPFLG          ;IS THERE A TERMINAL?
609 001114 001401          BEQ 68              ;BR IF YES
610 001116 000000          HALT              ;HALT HERE IF NO TERMINAL
611 001120 010046          MOV RO, -(SP)     ;SAVE RO
612 001122 017600 000002  #2(SP),RO         ;GET ADDRESS OF ASCII STRING
613 001126 112046          MOV#B (RO)+, -(SP) ;PUSH CHARACTER TO BE TYPED ONTO STACK
614 001130 001005          BNE 2#           ;BR IF IT ISN'T THE TERMINATOR
615 001132 005726          TST (SP)+        ;IF TERMINATOR POP IT OFF THE STACK
616 001134 012600          MOV (SP)+, RO    ;RESTORE RO
617 001136 062716 000002  7#1: ADD #2, (SP)   ;ADJUST RETURN PC
618 001142 000002          RTI              ;RETURN
619 001144 004767 000026  2#1: JSR PC, 5#    ;GO TYPE THIS CHARACTER
620 001150 122726 000012  3#1: CMPB #12, (SP)+ ;CHECK IF THE CHARACTER TYPED
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        BNE 1#           ;WAS A LINE FEED
        MOV #NULL, -(SP) ;GO GET NEXT CHARACTER IF NOT LINE FEED
        #2(SP),RO        ;GET # OF FILLER CHARACTERS NEEDED
        #AND THE NULL CHARACTER
        DECB 1((SP)      ;DOES A NULL NEED TO BE TYPED?
        JSR PC, 5#      ;BR IF NO--GO POP THE NULL OF THE STACK
        BR 4#           ;GO TYPE A NULL
        #LOOP
        TST# #TPS      ;WAIT UNTIL PRINTER IS READY
        BPL 5#         ;LOAD CHARACTER TO BE
        MOV# 2(SP), #TPB ;TYPED INTO DATA REGISTER
        RTS PC

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635
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639 001214 000000 SCNFLG: 0 ;SCNFLG GETS SET IF USING
640 ;SCAN ROUTINE (SA=220)
641 001216 000000 KTSTART: 0
642 001220 000000 ADRTYP: 0
643 001222 177600 PDRTAB: 177600
644 001224 172200 172200
645 001226 172300 PDREND: 172300
646 001230 172300 KPDR0: 172300 ;KERNEL PAGE DESCRIPTOR REGISTER ADDRESSES
647 001232 172302 KPDR1: 172302
648 001234 172304 KPDR2: 172304
649 001236 172316 KPDR7: 172316
650 001240 172340 KPAR0: 172340 ;KERNEL PAGE ADDRESS REGISTER ADDRESSES
651 001242 172342 KPAR1: 172342
652 001244 172344 KPAR2: 172344
653 001246 172356 KPAR7: 172356
654 001250 000000 SPSAV: 0 ;REGISTER SAVE LOCATIONS
655 001252 000000 ROSAV: 0
656 001254 000000 RISAV: 0
657 001256 000000 R2SAV: 0
658 001260 000000 R3SAV: 0
659 001262 000000 R4SAV: 0
660 001264 000000 R5SAV: 0
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665
666 001266 012706 000510 ;ROUTINE TO RESTART WITHOUT RETYPING MAP AFTER TEST HAS BEEN RUNNING
667 001272 012767 000001 177264 RSTART: MOV *STKPT,SP ;SET UP STACK POINTER
668 001300 005067 177240 MOV #1,MTYFG ;SET FLAG TO INDICATE MAP HAS BEEN TYPED
669 001304 012737 015304 000024 CLR PASCNT ;INITIALIZE PASS COUNT
670 001312 012737 000340 000026 MOV #PWRDN,##24
671 001320 005067 177164 CLR TSTX
672 001324 005037 177776 CLR #*PS ;CLEAR PROCESSOR STATUS REGISTER
673 001330 012737 000006 000004 MOV #6,##4
674 001336 005037 000006 CLR #*6
675 001342 000167 000416 JMP BEGIN
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680 ;ROUTINE TO SCAN ALL MEMORY FOR BAD PARITY AND TYPE 18 BIT ADDRESSES OF BAD
681 ;LOCATIONS
682 001346 012706 000510 SCAN: MOV *STKPT,SP ;SETUP STACK POINTER
683 001352 005767 177134 TST FTITLE ;IF TITLE HAS BEEN PRINTED, REGISTERS
684 ;HAVE ALREADY BEEN LOCATED- GO
685 ;AND LOCATE IF NOT ALREADY DONE
686 001356 001006 BNE SCANB ;BRANCH, REGISTERS HAVE ALREADY BEEN LOCATED
687 001360 005267 177630 INC SCNFLG ;INCREMENT SCNFLG
688 001364 000167 000120 JMP START1 ;GO TO LOCATE THE REGISTERS

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689 001370 005067 177620 SCAN: CLR SCNFLG ;RETURN HERE AFTER LOCATING THE REGISTERS
690 001374 004767 007760 SCANB: JSR PC,MAPMEM ;SETUP MEMORY MAP
691 001400 004767 012462 JSR PC,PSCAN ;SCAN FOR BAD PARITY
692 001404 104000 TYPE ;TYPE MESSAGE "BAD PARITY SCAN COMPLETE"
693 001406 017055 PSMJG
694 001410 005767 177136 TST NOKT
695 001414 001002 BNE .+6
696 001416 005037 177572 CLR #*SRO ;TURN OFF RT11 IF PRESENT
697 001422 000000 HALT ;END OF PARITY SCAN
698 001424 000750 BR SCAN
699
700
701
702
703 ;NORMAL STARTUP
704 001426 012706 000510 START: MOV *STKPT,SP ;SET UP STACK POINTER
705 001432 005067 177126 CLR MTYFG ;CLEAR FLAG WHICH INDICATES MAP TYPED
706 001436 005067 177102 CLR PASCNT ;INITIALIZE PASS COUNT
707 001442 012737 015304 000024 MOV #PWRDN,##24 ;SETUP POWER FAIL RETURN
708 001450 012737 000340 000026 MOV #340,##26
709 001456 005067 177026 CLR TSTX
710 001462 005767 177024 18: TST FTITLE ;IS TITLE PRINTED YET?
711 001466 001010 BNE START1 ;YES, SKIP OVER
712 001470 004767 012160 JSP PC,SAVLDR ;COPY LOADER TO LOWER 4K
713 001474 005267 177012 INC FTITLE ;SET FLAG
714 001500 104000 TYPE ;TYPE TITLE "MEMORY PARITY TEST
715 001502 016622 HTIT ;MAINDEC=11-DCMFA"
716 001504 104000 TYPE ;TYPE "LOADERS SAVED IN BANK 0.
717 001506 017110 HLDNSV ;TO RESTORE LOADERS, USE SA 210"
718
719
720
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722
723 ;SEARCH FOR PARITY REGISTERS PRESENT AND TYPE ADDRESSES OF THOSE FOUND
724 ;FAILURE TO LOCATE A REGISTER INDICATES THAT THE ADDRESS TIMED OUT OR THAT
725 ;BITS 5-7 IN THE REGISTER DID NOT SET
726 001510 104000 START1: TYPE ;TYPE "MEMORY PARITY REGISTERS PRESENT ARE:"
727 001512 016372 MPRAS
728 001514 005067 177022 CLR MPROK ;CLEAR MPR FLAG
729 001520 012702 000570 MOV #MPRO,R2 ;SET UP POINTERS
730 001524 012703 000772 MOV #INDCO,R3 ;POINTER TO CORE-MOS
731 001530 012737 001670 000004 MOV #GMPRB,##4 ;SET UP TIMEOUT TRAP RETURN
732 001536 005037 000006 CLR #*6
733 001542 042712 000001 GMPRA: BIC #1,(2) ;CLEAR FLAG BIT IN TABLE
734 001546 005062 000002 CLR 2(R2) ;INITIALIZE LOCATIONS IN THE TABLE
735 001552 005062 000004 CLR 4(R2)
736 001556 005062 000006 CLR 6(R2)
737 001562 005772 000000 TST #0(2) ;DOES THIS MPR EXIST? (IF NO, TIMES OUT)
738 001566 052772 000340 000000 BIS #340,0(2) ;YES- IS IT AN MF11-LP OR MA11-P CORE PARITY REG
739 001574 032772 000340 000000 BIT #340,0(2)
740 001602 001414 BEQ 18 ;NO, IS IT A MOB=11 PARITY REGISTER? BRANCH
741 001604 011267 176704 MOV (2),TEMPX ;YES- PRINT REGISTER ADDRESS
742 001610 004567 013154 JSR R5,OACNV ;(GET ASCII)

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743 001614 000514          TEMPX
744 001616 017202          MPRCOR
745 001620 000006          6
746 001622 104000          TYPE
747 001624 017202          MPRCOR          ;(TYPE ADDRESS)
748 001626 012713 000001  MOV      #1,(R3)          ;SET INDICATOR FOR CORE PARITY
749 001632 000413          BR      28
750 001634 011267 176654 18: MOV      (2),TEMPX          ;IT IS A MOS REGISTER, PRINT ADDRESS
751 001640 004567 013124  JSR      RS,DACNV          ;(GET ASCII)
752 001644 000514          TEMPX
753 001646 017243          MPRMOS
754 001650 000006          6
755 001652 104000          TYPE
756 001654 017243          MPRMOS          ;(TYPE ADDRESS)
757 001656 012713 177777  MOV      #-1,(R3)          ;SET INDICATOR FOR MOS PARITY
758 001662 005267 176654 28: INC      MPROR          ;SET MPR REGISTER PRESENT FLAG
759 001666 009403          BR      GMPRC          ;SKIP NEXT
760 001670 022626          GMPRB: CMP      (SP)+,(SP)+          ;RESTORE STACK POINTER
761 001672 052712 000001  BIS      #1,R2          ;SET FLAG INDICATING REGISTER NOT PRESENT
762 001676 062702 000010  GMPRC: ADD      #10,R2          ;UPDATE POINTER
763 001702 005723          TST      (R3)+
764 001704 020227          CMP      R2,#TREG          ;DONE YET?
765 001710 002714          BLT     GMPRA          ;NO, LOOP
766 001712 012737 000006 000004 MOV      #0,#4          ;YES, RESTORE TRAPCATCHER
767 001720 005767 177270  TST      SCNF LG          ;ARE YOU IN THE ROUTINE TO SCAN
768                                ;MEMORY FOR BAD PARITY-(SCAN)
769 001724 001402          BEQ     GMPRD          ;NO,BRANCH TO CARRY ON NORMALLY
770 001726 000167 177436  JMP      SCANA          ;YES, GO BACK TO THE MEMORY
771                                ;SCAN ROUTINE
772 001732 005767 176604  GMPRD: TST      MPROR          ;ANY PARITY REGISTERS PRESENT?
773 001736 001012          BNE     BEGIN          ;YES- GO TEST CONTROLS PRESENT
774 001740 104000          NOREG: TYPE          ;NU- TYPE *NG PARITY REGISTER FOUND*
775 001742 016555          MTR
776 001744 005737 000042  TST      #42          ;LOADED BY MONITOR?
777 001750 001402          BEQ     +6          ;NO, BRANCH
778 001752 000167 007322  JMP      LOGICAL          ;YES- EXIT, NO REGISTERS PRESENT
779 001756 000000          HALT
780 001760 000167 177442  JMP      START          ;NO REGISTERS TO TEST
781                                ;IF CONTINUED, TRY AGAIN
782 001764 012767 002010 014034 BEGIN: MOV      #TEST1+2,RETURN          ;SETUP SCOPE RETURN
783 001772 012767 000100 014022  MOV      #100,IMAX          ;MAXIMUM ITERATION COUNT
784 002000 012737 000006 000004  MOV      #6,#4          ;RESTORE TRAPCATCHER IN TIMEOUT VECTOR
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793 002006 104001          TEST1: SCOPE
794 002010 012737 000001 177570  MOV      #1,@DISPLY          ;LOAD TEST NUMBER INTO THE DISPLAY
795 002016 012700 000570  MOV      #MPRO,R0          ;LOAD ADDRESS OF TABLE INTO R0
796 002022 012704 000772  MOV      #INDCO,R4          ;LOAD ADDRESS OF INDICATOR IN R4

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797 002026 032710 000001 18: BIT      #1,R0          ;IS THIS REGISTER PRESENT?
798 002032 001042          BNE     48          ;NO- BRANCH TO GET NEXT ADDRESS
799 002034 011001          MOV      #R0,R1          ;YES- LOAD R1 WITH ADDRESS OF
800                                ;PARITY REGISTER
801 002036 022714 000001  CMP      #1,(R4)          ;IS THIS REGISTER CORE?
802 002042 001004          BNE     58          ;NO
803 002044 016767 176764 176760  MOV      RESV C,RESRVD          ;YES, CORE, STORE RESERVED BITS
804 002052 000403          BR      +10
805 002054 016767 176756 176750 58: MOV      RESV M,RESRVD          ;MOS, STORE RESERVED BITS
806 002062 012702 000001  MOV      #1,R2          ;LOAD R2 WITH VALUE OF FIRST BIT
807                                ;TO BE TESTED
808 002066 005011          CLR     #R1          ;INITIALIZE PARITY REGISTER
809 002070 011167 176674  MOV      #R1,TREG          ;READ CONTENTS OF PARITY REGISTER
810 002074 046767 176732 176666  RIC      RESRVD,TREG          ;CLEAR BITS WHICH ARE RESERVED
811 002102 001401          BEQ     +4          ;CHECK OTHER BITS- BRANCH IF OK
812 002104 104002          ERROR          ;CLEAR INSTRUCTION DID NOT INITIALIZE
813                                ;ALL USED BITS IN PARITY REGISTER
814                                ;TO ZERO (R1 CONTAINS ADDRESS OF
815                                ;FAILING REGISTER)
816 002106 030267 176720 28: BIT      R2,RESRVD          ;IS THIS BIT RESERVED?
817 002112 001010          BNE     36          ;YES- DON'T TEST IT SINCE IT
818                                ;MAY BE ZERO OR ONE
819 002114 010211          MOV      R2,#R1          ;NO- SET THIS BIT IN THE PARITY REGISTER
820 002116 011103          MOV      #R1,R3          ;READ AND SAVE CONTENTS OF PARITY REGISTER
821 002120 005011          CLR     #R1          ;CLEAR PARITY REGISTER
822 002122 046703 176704  BIC      RESRVD,R3          ;CLEAR BIT LOCATIONS THAT ARE
823                                ;RESERVED
824 002126 020203          CMP      R2,R3          ;CHECK REST
825 002130 001401          BEQ     +4          ;BRANCH IF OK
826 002132 104002          ENROP          ;PARITY REGISTER WHOSE ADDRESS IS IN R1
827                                ;WAS INCORRECT AFTER THE VALUE IN R2
828                                ;WAS WRITTEN INTO IT, ACTUAL CONTENTS
829                                ;(WITH UNUSED BITS CLEARED) IS IN R3
830 002134 006302          ASL     R2          ;ROTATE BIT TO BE TESTED
831 002136 103363          RCC     28          ;IF NOT DONE WITH ALL BIT POSITIONS
832                                ;GO TEST THIS ONE
833 002140 062700 000010 48: ADD      #10,R0          ;MOVE R0 TO POINT TO NEXT POSSIBLE ADDRESS
834 002144 005724          TST      (R4)+
835                                ;OF A PARITY REGISTER
836 002146 020027 000770  CMP      R0,#TREG          ;AT END OF TABLE?
837 002152 002725          BLT     18          ;NO, BRANCH
838 002154 005067 176610  CLR     TREG
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845 002160 104001          TEST2: SCOPE
846 002162 012737 000002 177570  MOV      #2,@DISPLY          ;LOAD TEST NUMBER INTO THE DISPLAY
847 002170 005067 013626  CLR     IMAX          ;DON'T ITERATE TEST
848 002174 012700 000570  MOV      #MPRO,R0          ;LOAD POINTER
849 002200 012703 000772  MOV      #INDCO,R3          ;POINTER TO INDICATOR
850 002204 032710 000001 18: BIT      #1,R0          ;IS THIS PARITY REGISTER PRESENT?

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851 002210 001012          BNE 58          ;NO BRANCH
852 002212 022713 000001  CMP  #1,(R3)   ;IS THIS CORE OR MOS PARITY REGISTER?
853 002216 001404          BEQ  68          ;NO- BRANCH
854 002220 012770 100015 000000  MOV  #100015,0(R0) ;MOS-SET ALL DEFINED BITS TO 1
855 002226 000403          BR  .+10
856 002230 012770 107745 000000 68: MOV  #107745,0(R0) ;CORE- SET ALL DEFINED BITS TO 1
857 002236 062700 000010 58: ADD  #10,R0    ;MOVE POINTER TO POINT TO NEXT MPR ADDRESS
858 002242 005723          TST  (R3)+     ;INCREMENT POINTER TO INDICATOR
859
860 002244 020027 000770          CMP  R0,#TREG  ;OF A PARITY REGISTER
861
862
863 002250 002755          BLT  18          ;NO- CONTINUE
864 002252 105767 176630          TSTB STPFLG   ;YES- TERMINAL AVAILABLE?
865 002256 001003          RNE  48          ;NO- BRANCH
866 002260 105777 176614          TSTB STPS     ;YES- WAIT FOR TERMINAL TO FINISH
867 002264 100375          BPL  .-4
868 002266 000005          RESET
869 002270 012700 000570 48: MOV  #MPR0,R0  ;ISSUE INIT
870 002274 012703 000772          MOV  #INDCO,R3 ;LOAD ADDRESS OF THE TABLE
871 002300 032710 000001 28: BIT  #1,0R0   ;POINTER TO INDICATOR
872 002304 001030          BNE  38          ;IS THIS PARITY REGISTER PRESENT?
873 002306 022713 000001  CMP  #1,(R3)   ;NO- BRANCH
874 002312 001012          BNE  78          ;IS THIS A CORE PAR REGISTER?
875 002314 017002 000000          MOV  0(R0),R2 ;NO, BRANCH
876 002320 005070 000000          CLR  R(R0)     ;YES, GET CONTENTS OF REGISTER
877 002324 042702 077772          BIC  #77772,R2 ;MAKE SURE THAT WMP AND AE ARE CLEAR
878
879 002330 005702          TST  P2        ;MASK RESERVED BITS FOR CORE PAR
880 002332 001401          BEQ  .+4       ;ITY REGISTER, BITS 5-11(ADDRS
881 002334 104002          ERROR        ;BITS) ARE ALSO MASKED
882
883
884
885 002336 000411          BR  38-4       ;CHECK, IF REST WERE CLEARED
886 002340 017002 000000 78: MOV  0(R0),R2 ;CORE PARITY REGISTER WHOSE ADDRESS IS
887 002344 005070 000000          CLR  0(R0)     ;POINTED TO BY R0 WAS INCORRECT
888 002350 046702 176462          BIC  #05VM,R2 ;AFTER A RESET WAS ISSUED- CONTENTS
889 002354 005702          TST  R2        ;SAVED IN R2 WITH UNUSED BITS MASKED
890 002356 001401          BEQ  .+4
891 002360 104002          ERROR
892
893
894
895
896 002362 005070 000000          CLR  0(R0)     ;MOS, GET CONTENTS OF REGISTER
897 002366 062700 000010 38: ADD  #10,R0   ;MAKE SURE THAT WMP AND AE ARE CLEAR
898
899 002372 005723          TST  (R3)+     ;MASK RESERVED BITS FOR MOS PAR REG
900 002374 020027 000770          CMP  R0,#TREG ;CHECK REST
901 002400 002737          BLT  28        ;RESET DID CLEAR ALL BITS
902
903
904

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905 ;MAP CORRESPONDENCE BETWEEN PARITY REGISTERS AND MEMORY, AND TYPE RESULTS
906 ;NOTE THAT IF PARITY MEMORY IS NOT LOCATED CORRECTLY BY THIS SUBTEST
907 ;IT IS DUE TO ONE OF THE FOLLOWING FAILURES:
908 ; -SETTING WRITE WRONG PARITY DID NOT CAUSE BAD PARITY TO BE WRITTEN
909 ; -PARITY GENERATE OR DETECT LOGIC FAILED
910 ; -PARITY ERROR BIT FAILED TO SET
911 ; -PARITY BITS IN MEMORY LOCATION FAILED (I.E. BIT STUCK AT GOOD PARITY VALUE)
912 ;NOTE THAT SETTING SWITCH REGISTER SWITCH 9 WILL CAUSE A HALT AFTER THE MAP
913 ;IS TYPED, IF YOU WISH TO CHANGE THE MAP TO ISOLATE THE CAUSE OF A MAPPING
914 ;FAILURE, YOU CAN DO THIS ONCE THE PROCESSOR IS HALTED. SEE THE DESCRIPTION
915 ;IN THE LISTING (PRECEDING THE MAP TAG #MPR# AT LOCATION 600) FOR THE MEANING
916 ;OF THE MAP CONTENTS, AFTER MAKING THE DESIRED CHANGES, PRESS CONTINUE. THE NEW
917 ;MAP WILL BE TYPED AND IF SWITCH 9 IS LEFT SET THE PROCESS WILL BE REPEATED.
918 ;IF SWITCH 9 IS NOT LEFT SET THE PROGRAM WILL PROCEED TO TEST THE PARITY MEMORY
919 ;AND REGISTERS AS RECORDED IN THE NEW MAP.
920 ;*****
921 002402 104001          TEST3: SCOPE
922 002404 012737 000003 177570  MOV  #3,0#DISPLY ;LOAD TEST NUMBER INTO THE DISPLAY
923 002412 005767 176146          TST  #TYFG    ;IF MAPPING HAS ALREADY BEEN DONE
924 002416 001044          BNE  TEST4    ;SKIP SUBTEST
925 002420 004767 010740          JSR  #7,CLRPAR ;MAP MEMORY
926 002424 004767 006730          JSR  #7,MAPMEM ;FIND PARITY MEMORY AND CORRESPONDING
927 002430 004767 007252          JSR  #7,MAPREG ;REGISTERS USING WRITE WRONG PARITY
928
929
930 002434 005067 176432          CONT3: CLR  PHEML ;WITHOUT ACTION ENABLE SET
931 002440 005067 176430          CLR  PHEMH    ;INITIALIZE LOCATIONS INDICATING
932 002444 012701 000570          MOV  #MPR0,R1 ;TOTAL PARITY MEMORY PRESENT
933 002450 032711 000001 18: BIT  #1,0R1
934 002454 001006          BNE  28
935 002456 056167 000002 176406  BLS  2(R1),PHEML ;FLAG EXISTING PARITY MEMORY (LOW 64K)
936 002464 056167 000004 176402  BLS  4(R1),PHEMH ;FLAG EXISTING PARITY MEMORY (HIGH 64K)
937 002472 062701 000010 28: ADD  #10,R1
938 002476 020127 000770          CMP  R1,#TREG
939 002502 103762          BLO  18
940 002504 004767 007712          JSR  #7,MAP   ;TYPE MAP
941 002510 005267 176050          INC  #TYFG    ;INDICATE MAPPING DONE
942 002514 032737 001000 177570  BIT  #BIT9,0#SR ;SWITCH 9 SET?
943 002522 001402          BEQ  .+6       ;NO- BRANCH
944 002524 000000          HALT        ;YES- SWITCH 9 SET INDICATING HALT
945
946 002526 000742          BR  CONT3    ;AFTER TYPING PARITY MEMORY MAP
947
948
949
950 ;*****
951 ;SHOW THAT ASSERT PB WORKS CORRECTLY FOR EACH REGISTER
952 ;SHOW THAT NO TRAP OCCURS IF ACTION ENABLE (AE) IS NOT SET
953 ;SHOW THAT SETTING AE WITH ERROR ALREADY SET DOESN'T CAUSE A TRAP
954 ;NOTE THAT IF A KILL IS PRESENT, IT IS USED DURING THIS SUBTEST
955 ;*****
956 002530 104001          TEST4: SCOPE
957 002532 012737 000004 177570  MOV  #4,0#DISPLY ;LOAD TEST NUMBER INTO THE DISPLAY
958 002540 012767 000100 013254  MOV  #100,IMAX ;CLEAR ALL PARITY REGISTERS
959 002546 004767 010612          JSR  #7,CLRPAR

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1067
1068 003062 032701 000001          BIT      #1,R1          ;(VIRTUAL THRU KERNEL PAGE 1 IF K11 IS PRESENT)
1069 003066 001403          BEQ      ,+10         ;IF NO MEMORY WAS FOUND TO CORRESPOND
1070 003070 104002          ERROR    ,+10         ;ODD ADDRESS IS RETURNED-BRANCH IF OK
1071                                     ;MAP INDICATES NO PARITY MEMORY IS
1072                                     ;CONTROLLED BY THIS REGISTER
1073                                     ;RO POINTS TO THE ADDRESS OF THE
1074                                     ;PARITY REGISTER
1074 003072 000167 177744          JMP      LOP6         ;AFTER ERROR, CHECK FOR NEXT REGISTER
1075 003076 012770 000004 000000    MOV      #WMP,@(R0)   ;INITIALIZE LOCATION UNDER TEST
1076 003104 011111          MOV      @R1,@R1      ;INITIALLY CLEAR PARITY REGISTER
1077                                     ;R2 CONTAINS VALUE TO BE LOADED
1078 003106 005711          TST     @R1           ;INTO MEMORY
1079 003110 042770 000004 000000    BIC     #WMP,@(R0)   ;WRITE VALUE INTO LOW BYTE
1080 003116 011111          MOV      @R1,@R1      ;READ WORD TO CHECK PARITY
1081 003120 005711          TST     @R1           ;CHECK PARITY REGISTER
1082 003122 005770 000000          TST     @(R0)         ;CHECK PARITY REGISTER
1083 003126 100401          BMI     ,+4           ;BRANCH IF ERROR NOT SET
1084 003130 104002          ERROR    ,+4           ;PARITY ERROR SET WHEN VALUE IN R2 WAS
1085                                     ;WRITTEN AND READ BACK FROM LOW BYTE OF
1086                                     ;LOCATION WHOSE ADDRESS IS CONTAINED IN
1087                                     ;R1 (WMP WAS NOT SET)
1088 003132 005070 000000          CLR     @(R0)         ;CLEAR ERROR BIT
1089 003136 000741          BR      LOP6         ;REINITIALIZE TEST LOCATION
1090 003140 005767 175406          TST     NOKT         ;REINITIALIZE VALUE TO BE USED
1091 003144 001002          BNE     ,+6           ;INCREMENT VALUE TO BE LOADED
1092 003146 005037 177572          CLR     @*SRO        ;LOOP UNTIL ALL VALUES HAVE BEEN USED
1093
1094
1095
1096
1097
1098
1099
1100
1101 003152 104001          TEST6:  MOV      #6,@DISPLY ;LOAD TEST NUMBER INTO THE DISPLAY
1102 003154 012737 000006 177570    JSR     @7,CLRPAR    ;CLEAR ALL PARITY REGISTERS
1103 003162 004767 010176          TST     NOKT         ;K11 PRESENT?
1104 003166 005767 175360          BNE     1$           ;NO, BRANCH
1105 003172 001004          JSR     @7,WRALL     ;YES- MAP IT (KERNEL 0 TO BANK 0, RW;
1106 003174 004767 010064          JSR     @7,MAP1      ;KERNEL 7 TO EXTERNAL BANK, RW; KERNEL 1 RW)
1107 003200 004767 010230          AND     ANDTURN ON  ;AND TURN IT ON
1108
1109 003204 012700 000570          1$:   MOV      #MPRO,R0 ;SETUP TO FIND REGISTERS PRESENT
1110 003210 032710 000001          LOOP6: BIT     #1,R0   ;IS THIS REGISTER PRESENT?
1111 003214 001406          BEQ     TST6         ;YES- BRANCH TO TEST IT
1112 003216 062700 000010          LOP6:  ADD     #10,R0  ;NO- CHECK FOR ANOTHER ONE
1113 003222 020027 000770          CMP     R0,@TREG
1114 003226 103770          BLO    LOOP6
1115 003230 000523          BR      DONE6
1116
1117 003232 004767 010242          TST6:  JSR     @7,LOCATM ;BRANCH TO DONE IF ALL REGISTERS
1118                                     ;HAVE BEEN TESTED
1119                                     ;LOCATE MEMORY CORRESPONDING TO
1120                                     ;THIS REGISTER- R1 SHOULD BE RETURNED
1121                                     ;CONTAINING THE ADDRESS OF THE FIRST
1122                                     ;LOCATION CONTROLLED BY THIS REGISTER

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1121
1122 003236 032701 000001          BIT      #1,R1          ;(VIRTUAL THRU KERNEL PAGE 1 IF K11 PRESENT)
1123 003242 001403          BEQ      ,+10         ;IF NO MEMORY WAS FOUND TO CORRESPOND
1124 003244 104002          ERROR    ,+10         ;ODD ADDRESS IS RETURNED-BRANCH IF OK
1125                                     ;MAP INDICATES NO PARITY MEMORY IS
1126                                     ;CONTROLLED BY THIS REGISTER
1127                                     ;RO POINTS TO THE ADDRESS OF THE
1128 003246 000167 177744          JMP      LOP6         ;PARITY REGISTER
1129                                     ;AFTER ERROR, CHECK FOR NEXT REGISTER
1130
1131
1132 003252 005011          ;FIRST SHOW THAT IF THE PARITY REGISTER IS CLEARED INITIALLY,
1133 003254 005070 000000          ;PARITY ERROR DOESN'T SET
1134 003260 005002          CLR     @R1           ;INITIALIZE LOCATION UNDER TEST
1135                                     ;INITIALLY CLEAR PARITY REGISTER
1136 003262 110211          1$:   MOVVB   R2,@R1      ;R2 CONTAINS VALUE TO BE LOADED
1137 003264 005711          TST     @R1           ;INTO MEMORY
1138 003266 005770 000000          TST     @(R0)         ;WRITE VALUE INTO LOW BYTE
1139 003272 100006          BPL     5$           ;READ WORD TO CHECK PARITY
1140 003274 104002          ERROR    ,+6           ;CHECK PARITY REGISTER
1141                                     ;BRANCH IF ERROR NOT SET
1142                                     ;PARITY ERROR SET WHEN VALUE IN R2 WAS
1143                                     ;WRITTEN AND READ BACK FROM LOW BYTE OF
1144                                     ;LOCATION WHOSE ADDRESS IS CONTAINED IN
1145                                     ;R1 (WMP WAS NOT SET)
1146 003276 005070 000000          CLR     @R1           ;CLEAR ERROR BIT
1147 003302 005011          CLR     @R2           ;REINITIALIZE TEST LOCATION
1148 003304 005002          CLR     R2           ;REINITIALIZE VALUE TO BE USED
1149 003306 000402          BR      2$           ;INCREMENT VALUE TO BE LOADED
1150 003310 105202          5$:   INCB    R2         ;LOOP UNTIL ALL VALUES HAVE BEEN USED
1151 003312 001363          BNE     1$           ;WRITE ALL VALUES INTO HIGH BYTE
1152 003314 110261          2$:   MOVVB   R2,@R1      ;READ WORD TO CHECK PARITY
1153 003320 005711          TST     @R1           ;CHECK PARITY REGISTER
1154 003322 005770 000000          TST     @(R0)         ;CHECK PARITY REGISTER
1155 003326 100002          BPL     ,+6           ;BRANCH IF ERROR NOT SET
1156 003330 104002          ERROR    ,+6           ;PARITY ERROR SET WHEN VALUE IN R2
1157                                     ;WAS WRITTEN AND READ BACK FROM HIGH BYTE
1158                                     ;OF LOCATION WHOSE ADDRESS IS CONTAINED
1159                                     ;IN R1 (WMP WAS NOT SET)
1160                                     ;INCREMENT VALUE TO BE LOADED
1161                                     ;LOOP UNTIL ALL VALUES HAVE BEEN USED
1162
1163 003332 000402          BR      6$           ;TEST PARITY GENERATE AND DETECT LOGIC BY SETTING WRITE WRONG PARITY AND
1164 003334 105202          INCB   R2           ;WRITING EACH POSSIBLE VALUE TO THE LOW BYTE, THEN TO THE HIGH BYTE
1165 003336 001366          BNE     2$           ;INITIALIZE LOCATION UNDER TEST
1166 003338 005011          6$:   CLR     @R1           ;INITIALIZE VALUE TO BE WRITTEN
1167 003340 005002          CLR     R2           ;INITIALIZE VALUE TO BE WRITTEN
1168 003342 005070 000004 000000    MOV      #WMP,@(R0)   ;SET WRITE WRONG PARITY
1169 003344 012770          MOVVB   R2,@R1      ;WRITE WRONG PARITY IN LOW BYTE
1170 003346 005070 000000          CLR     @R1           ;CLEAR WRITE WRONG PARITY, AND CLEAR
1171                                     ;PARITY ERROR IF SET
1172 003348 005711          TST     @R1           ;READ BACK WRONG PARITY
1173 003350 005770 000000          TST     @(R0)         ;PARITY ERROR SET?
1174 003352 100402          BMI     ,+6           ;YES-BRANCH
1175 003354 005070 000000          ERROR    ,+6           ;PARITY ERROR DID NOT SET WHEN THE
1176                                     ;LOCATION UNDER TEST WAS WRITTEN
1177                                     ;AND READ BACK WITH WRITE WRONG PARITY

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1175                                     ;SET, R0 POINTS TO ADDRESS OF PARITY
1176                                     ;REGISTER, R1 CONTAINS ADDRESS OF LOCATION
1177                                     ;BEING TESTED (VIRTUAL, THRU KERNEL
1178                                     ;PAGE 1 IF KT11 IS PRESENT), R2
1179                                     ;CONTAINS THE VALUE WRITTEN
1180 003372 000402                                BR    .+6          ;EXIT LOOP AFTER ERROR
1181 003374 105202                                INCB   R2         ;INCREMENT DATA
1182 003376 001362                                RNE    38        ;LOOP TILL DONE WITH ALL VALUES
1183 003400 005011                                CLR    0R1       ;REINITIALIZE LOCATION TO CLEAR BAD PARITY
1184 003402 005070 000000                       CLR    0(R0)     ;CLEAR ERROR IF SET
1185 003406 005711                                TST    0R1       ;READ LOCATION, WHICH SHOULD NOW HAVE
1186                                     ;GOOD PARITY
1187 003410 005770 000000                       TST    0(R0)     ;PARITY ERROR SET?
1188 003414 100001                                BPL    .+4       ;NO, BRANCH
1189 003416 104002                                ERROR                                     ;GOOD PARITY WAS NOT RESTORED BY
1190                                     ;WRITING INTO THE LOCATION WITH
1191                                     ;WRITE WRONG PARITY CLEARED
1192 003420 012770 000004 000000 481            MOV    ##WP,0(R0) ;SET WRITE WRONG PARITY
1193 003426 110261 000001                        MOVB   P2,1(K1)  ;WRITE WRONG PARITY IN HIGH BYTE
1194 003432 005070 000000                       CLR    0(R0)     ;CLEAR WRITE WRONG PARITY AND PARITY
1195                                     ;ERROR IF SET
1196 003436 005711                                TST    0R1       ;READ BACK WRONG PARITY
1197 003440 005770 000000                       TST    0(R0)     ;PARITY ERROR SET?
1198 003444 100402                                BMI    .+6       ;YES-BRANCH
1199 003446 104002                                ERROR                                     ;PARITY ERROR DID NOT SET WHEN THE LOCATION
1200                                     ;UNDER TEST WAS WRITTEN AND READ BACK WITH
1201                                     ;WRITE WRONG PARITY SET, R0 POINTS
1202                                     ;TO THE ADDRESS OF THE PARITY REGISTER.
1203                                     ;THE VALUE IN P2 WAS WRITTEN INTO THE HIGH
1204                                     ;BYTE OF THE LOCATION WHOSE ADDRESS IS IN R1
1205                                     ;(VIRTUAL THRU KERNEL PAGE 1 IF KT11 PRESENT)
1206                                     ;THEN THE PARITY REGISTER WAS
1207                                     ;CLEARED AND THE WORD WAS READ BACK
1208 003450 000402                                BR    .+6          ;EXIT LOOP AFTER ERROR
1209 003452 105202                                INCB   R2         ;INCREMENT DATA
1210 003454 001361                                RNE    48        ;LOOP TILL DONE WITH ALL VALUES
1211 003456 005011                                CLR    0R1       ;CLEAR BAD PARITY IN TEST LOCATION
1212 003460 005070 000000                       CLR    0(R0)     ;CLEAR PARITY ERROR BIT IF SET
1213 003464 005711                                TST    0R1       ;READ LOCATION, WHICH SHOULD NOW
1214                                     ;HAVE GOOD PARITY
1215 003466 005770 000000                       TST    0(R0)     ;CHECK PARITY ERROR BIT
1216 003472 100001                                BPL    .+4       ;BRANCH IF CLEAR
1217 003474 104002                                ERROR                                     ;WRITING INTO LOCATION WHEN WRITE
1218                                     ;WRONG PARITY WAS NOT SET DID NOT
1219                                     ;WRITE GOOD PARITY
1220 003476 000647                                BR    LUP6       ;GO CHECK FOR ANOTHER PARITY REGISTER
1221 003500 005767 175046                       DONE6: TST    NOKT
1222 003504 001002                                BNE    .+6
1223 003506 005037 177572                       CLR    ##SR0
1224                                     ;TURN OFF KT11 IF PRESENT
1225
1226
1227                                     ;*****
1228                                     ;SHOW THAT SETTING PARITY ERROR AFTER SETTING ACTION ENABLE WON'T CAUSE A TRAP

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1229                                     ;*****
1230 003512 104001                                TEST7: SCOPE
1231 003514 012737 000007 177570                MOV    #7,0(DISPLAY) ;LOAD TEST NUMBER INTO THE DISPLAY
1232 003522 004767 007636                       JSR    %7,CLRPAR   ;INITIALLY CLEAR ALL PARITY REGISTERS
1233 003526 012737 003622 000114                MOV    TRP7,##PARVEC ;SETUP PARITY TRAP RETURN
1234 003534 005037 000116                       CLR    ##PARVEC+2
1235 003540 012700 000570                                MOV    #MPRO,R0    ;SETUP TO GET ADDRESS OF REGISTER PRESENT
1236 003544 032710 000001                                LUP7: BIT    #1,0R0
1237 003550 001406                                BEQ    TST7        ;BRANCH TO TEST REGISTER
1238 003552 062700 000010                                LOOP7: ADD   #10,R0
1239 003556 020027 000770                                CMP    R0,#TRREG
1240 003562 103770                                BLO   LUP7
1241 003564 000412                                BR    DONE7        ;BRANCH IF DONE TESTING ALL REGISTERS
1242 003566 012770 000001 000000                TST7: MOV    #AE,0(R0) ;SET ACTION ENABLE
1243 003574 052770 100000 000000                BIS    #PERR,0(R0) ;SET PARITY ERROR
1244 003602 000240                                NOP                                     ;SHOULD NOT TRAP
1245 003604 005070 000000                                CLR    0(R0)     ;CLEAR PARITY REGISTER
1246 003610 000760                                BR    LOOP7       ;GO CHECK NEXT REGISTER
1247 003612 012737 000116 000114                DONE7: MOV    #PAKVEC+2,##PARVEC
1248 003620 000405                                RR    TEST10
1249 003622 104002                                TRP7: ERRJRP
1250                                     ;TRAP OCCURRED WHEN PARITY ERROR BIT
1251                                     ;WAS SET VIA A BIS INSTRUCTION
1252                                     ;WITH ACTION ENABLE ALREADY SET.
1253                                     ;R0 POINTS TO THE ADDRESS OF THE
1254                                     ;PARITY REGISTER
1255 003624 022626                                CMP    (SP)+,(SP)+ ;RESTORE STACK POINTER
1256 003626 005070 000000                                CLR    0(R0)     ;CLEAR PARITY REGISTER
1257 003632 000747                                BR    LOOP7
1258
1259
1260                                     ;*****
1261                                     ;SHOW THAT REPEATED PARITY ERRORS WILL CAUSE REPEATED TRAPS IF ACTION
1262                                     ;ENABLE IS SET AND PARITY ERROR IS LEFT SET.
1263                                     ;SHOW THAT THE ERROR ADDRESS BITS (11-5) TRACK (ONLY FOR CORE PARITY REGISTERS)
1264                                     ;*****
1265 003634 104001                                TEST10: SCOPE
1266 003636 012737 000010 177570                MOV    #10,##DISPLAY ;LOAD TEST NUMBER INTO THE DISPLAY
1267 003644 004767 007514                       JSR    %7,CLRPAR   ;INITIALLY CLEAR ALL PARITY REGISTERS
1268 003650 005767 174676                       TST    NOKT       ;KT11 PRESENT?
1269 003654 001004                                BNE    18         ;NO- BRANCH
1270 003656 004767 007402                       JSR    %7,RRALL    ;YES- INITIALLY MAP ALL PAGES NR
1271 003662 004767 007546                       JSR    %7,MAP1     ;MAP KERNEL 0 TO BANK 0,RW
1272                                     ;KERNEL 7 TO THE EXTERNAL BANK, RW
1273                                     ;MAKE KERNEL PAGE 1 RW AND TURN ON THE KT11
1274 003666 012700 000570                                18: MOV    #MPRO,R0
1275 003672 012702 000772                                MOV    #INDCO,R2
1276 003676 032710 000001                                LUP10: BIT    #1,0R0
1277 003702 001407                                BEQ    TST10      ;BRANCH TO TEST REGISTER IF PRESENT
1278 003704 062700 000010                                LOOP10: ADD  #10,R0
1279 003710 005722                                TST   (R2)+
1280 003712 020027 000770                                CMP    R0,#TRREG
1281 003716 103767                                BLO   LUP10
1282 003720 000507                                BR    DONE10     ;BRANCH IF ALL REGISTERS HAVE BEEN TESTED

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1283	003722	004767	007552	TST10:	JSR	%7,LOCATM	
1284	003726	032701	000001		BIT	#1,R1	;ERROR RETURN INDICATED?
1285	003732	001403			BEQ	+.10	;BRANCH IF NO
1286	003734	104002			ERROR		;MAP INDICATES THERE IS NO MEMORY
1287							;CORRESPONDING TO THIS REGISTER
1288							;RO POINTS TO THE ADDRESS OF
1289							;THE PARITY REGISTER
1290	003736	000167	177742		JMP	LOOP10	
1291	003742	012770	000004 000000		MOV	#WNP,%(RO)	;SET WRITE WRONG PANITY
1292	003750	011111			MOV	#R1,%R1	;WRITE WRONG PANITY IN FIRST LOCATION
1293	003752	016161	004000 004000		MOV	4000(R1),4000(R1)	;WRITE WRONG PANITY IN SECOND LOCATION
1294	003760	012770	000001 000000		MOV	#AE,%(RO)	;SET ACTION ENABLE AND CLEAR REST
1295	003766	012737	004020 000114		MOV	#TRP10,%#PARVEC	;SETUP PARITY TRAP RETURN
1296	003774	012767	000010 000152		MOV	#10,COUNT	;SETUP COUNTER TO EXECUTE INSTRUCTION 1
1297							; (INST1) TEN TIMES
1298	004002	005711		INST1:	TST	#R1	;READ WRONG PANITY WITH AE SET- SHOULD

1299							
1300	004004	104002			ERROR		;TRAP TO TRP10
1301							;NO PARITY TRAP OCCURRED. RO POINTS TO
1302							;ADDRESS OF THE PARITY REGISTER BEING
1303	004006	000441			BR	CONT10	;TESTED.
1304	004010	005761	004000	INST2:	TST	4000(R1)	;READ WRONG PARITY FROM S&COND ADDRESS
1305							;WITH AE SET- SHOULD TRAP TO TRP10A
1306	004014	104002			ERROR		;NO PARITY TRAP OCCURRED. RO POINTS TO
1307							;THE ADDRESS OF THE PARITY REGISTER
1308							;BEING TESTED
1309	004016	000435			BR	CONT10	
1310	004020	005367	000130	TRP10:	DEC	COUNT	;HAS PARITY TRAP OCCURRED TEN TIMES?
1311	004024	001413			BEQ	1#	;YES- BRANCH
1312	004026	022712	000001		CMP	#1,(R2)	;IS THIS A CORE PAR REG?
1313	004032	001005			BNE	2#	;NO, BRANCH (NO ERROR
1314							;ADDRESS BITS FOR MOS PAR
1315	004034	032770	000040 000000		BIT	#BITS,%(RO)	;IF ERROR ADDRESS BITS ARE TRACKING,
1316							;BIT 5 SHOULD BE CLEAR (ONLY FOR CORE PARITY)
1317	004042	001401			BEQ	+.4	
1318	004044	104002			ERROR		;PARITY ERROR ADDRESS BITS INCORRECT
1319							;RO POINTS TO THE ADDRESS OF THE PANITY
1320							;REGISTER. R1 CONTAINS THE ADDRESS
1321							;REFERENCED TO CAUSE A PARITY TRAP
1322							; (VIRTUAL IF K11 IS PRESENT)
1323	004046	012716	004002	2#:	MOV	#INST1,%SP	;GO EXECUTE INSTRUCTION 1 AGAIN
1324	004052	000002			RTI		
1325	004054	012737	004070 000114	1#:	MOV	#TRP10A,%#PARVEC	;CHANGE PARITY TRAP RETURN
1326	004062	012716	004010		MOV	#INST2,%SP	;GO EXECUTE INSTRUCTION 2
1327	004066	000002			RTI		
1328	004070	022712	000001	TRP10A:	CMP	#1,(P2)	;IS THIS A CORE REG?
1329	004074	001005			BNE	1#	;NO, BRANCH
1330	004076	032770	000040 000000		BIT	#BITS,%(RO)	;PARITY TRAP OCCURRED- CHECK PARITY
1331							;ERROR ADDRESS BITS
1332	004104	001001			BNE	+.4	;BRANCH IF OK (IF THE PARITY ERROR
1333							;ADDRESS BITS TRACKED, BIT 5 WILL BE SET)
1334	004106	104002			ERROR		;PARITY ERROR ADDRESS BITS INCORRECT
1335							;RO POINTS TO THE ADDRESS OF THE
1336							;PARITY REGISTER, THE ADDRESS REFERENCED
1337							;TO CAUSE THE ERROR WAS THAT IN
1338							;R1 PLUS 4000 (OCTAL).
1339	004110	022626		1#:	CMP	(SP)+,(SP)+	
1340	004112	012737	000116 000114	CONT10:	MOV	#PARVEC+2,%#PARVEC	;RESTORE TRAPCATCHER
1341	004120	005070	000000		CLR	%(RO)	;CLEAR PARITY REGISTER
1342	004124	005511			ADC	#R1	;CLEAR BAD PARITY
1343	004126	005561	004000		ADC	4000(R1)	
1344	004132	005070	000000		CLR	%(RO)	;CLEAR PARITY ERROR BIT IF SET
1345	004136	000662			BR	LOOP10	
1346	004140	005767	174406	DONE10:	TST	NOKT	
1347	004144	001002			BNE	1#	
1348	004146	005037	177572		CLR	#SRC	
1349	004152	000401			BR	TEST11	;TURN OFF K111 IF PRESENT
1350	004154	000000		COUNT:	0		
1351							
1352							

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1359 004156 104001
1360 004160 012737 000011 177570
1361 004166 004767 007172
1362 004172 005767 174354
1363 004176 001004
1364 004200 004767 007060
1365 004204 004767 007224
1366
1367 004210 012700 000570
1368 004214 012703 000772
1369 004220 032710 000061
1370 004224 001003
1371 004226 022713 000001
1372 004232 001407
1373
1374 004234 062700 000010
1375 004240 005723
1376 004242 020027 000770
1377 004246 103764
1378 004250 000443
1379 004252 004767 007222
1380
1381 004256 032701 000001

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*****
;IF MULTIPLE PARITY ERRORS OCCUR DURING ONE INSTRUCTION (WITH ACTION ENABLE
;NOT SET) THE ERROR ADDRESS BITS WILL RECORD THE LAST ERROR (ONLY FOR CORE PARITY
;REGISTERS)
*****
TEST11: SCOPE
        MOV     #11, @DISPLY      ;LOAD TEST NUMBER INTO THE DISPLAY
        JSR    %7, CLRPAR        ;INITIALLY CLEAR ALL PARITY REGISTERS
        TST    NOKT              ;KT11 PRESENT?
        BNE   1$                ;NO- BRANCH
        JSR    %7, NRALL         ;YES, MAP KERNEL PAGE 0 TO BANK 0, RW
        JSR    %7, MAP1         ;MAP KERNEL PAGE 7 TO THE EXTERNAL BANK, RW
        JSR    %7, MAP1         ;SET KERNEL PAGE 1 RW AND TURN ON KT11
        MOV    #MPRO, R0         ;SETUP TO GET ADDRESSES OF REGISTERS PRESENT
        MOV    #INDCO, R3
LUP11:  BIT    #1, @R0
        BNE   LOOP11            ;IF THIS REG NOT PRESENT, SKIP
        CMP    #1, (R3)         ;IS THIS A CORE PAR REG?
        BEQ   TEST11           ;YES, THEN TEST IT
        ADD    #10, R0          ;IF NOT CORE, SKIP THIS REGISTER
        TST   (R3)+
        CMP   R0, %FREG
        BLO  LUP11
        BR   DONE11
TST11:  JSR    %7, LOCATM       ;BRANCH OUT IF ALL REGISTERS HAVE BEEN TESTED
        BIT   #1, R1           ;GET THE ADDRESS OF A MEMORY LOCATION
        ;CORRESPONDING TO THIS PARITY REGISTER
        ;ERROR RETURN INDICATED?

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1382 004262 001403
1383 004264 104002
1384
1385
1386 004266 000167 177742
1387 004272 010102
1388 004274 062702 010000
1389 004300 012770 000004 000000
1390 004306 011111
1391 004310 011212
1392 004312 005070 000000
1393 004316 021112
1394
1395 004320 005770 000000
1396 004324 100401
1397 004326 104002
1398
1399
1400 004330 032770 000100 000000
1401
1402
1403 004336 001001
1404 004340 104002
1405
1406
1407
1408
1409 004342 005070 000000
1410 004346 005511
1411 004350 005512
1412 004352 005070 000000
1413 004356 000726
1414 004360 005767 174166
1415 004364 001002
1416 004366 005037 177572
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1425 004372 104001
1426 004374 012737 000012 177570
1427 004402 004767 006756
1428 004406 005767 174140
1429 004412 001004
1430 004414 004767 006644
1431 004420 004767 007010
1432
1433 004424 012700 000570
1434 004430 012702 000772
1435 004434 032710 000001

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        BEQ   .+10              ;BRANCH IF NOT
        ERROR
        JMP   LOOP11
        MOV   R1, R2
        ADD  #10000, R2
        MOV  #WWP, @ (R0)
        MOV  @R1, @R1
        MOV  @R2, @R2
        CLR  @ (R0)
        CMP  @R1, @R2
        TST  @ (R0)
        BMI .+4
        ERROR
        BIT  #BIT6, @ (R0)
        BNE .+4
        ERROR
        CLR  @ (R0)
        ADC  @R1
        ADC  @R2
        CLR  @ (R0)
        BR   LOOP11
DONE11: TST  NOKT
        BNE .+6
        CLR  @%SRO              ;TURN OFF KT11 IF PRESENT

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*****
;SHOW THAT IF AN INSTRUCTION DOING A DATIP GETS A PARITY ERROR,
;THE ORIGINAL DATA IS REWRITTEN IF ACTION ENABLE IS SET, AND IS
;ALTERED IF ACTION ENABLE IS CLEAR
*****
TEST12: SCOPE
        MOV     #12, @DISPLY      ;LOAD TEST NUMBER INTO THE DISPLAY
        JSR    %7, CLRPAR        ;INITIALLY CLEAR ALL PARITY REGISTERS
        TST    NOKT              ;KT11 PRESENT?
        BNE   1$                ;NO- BRANCH
        JSR    %7, NRALL         ;YES, MAP KERNEL 0 TO BANK 0, RW
        JSR    %7, MAP1         ;MAP KERNEL 7 TO THE EXTERNAL BANK, RW
        JSR    %7, MAP1         ;SET KERNEL 1 RW AND TURN ON KT11
        MOV    #MPRO, R0         ;SETUP TO GET ADDRESSES OF REGISTERS PRESENT
        MOV    #INDCO, R2
LUP12:  BIT    #1, @R0

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1436 004440 001003      BNE    LOOP12      ;SKIP, IF THIS REG NOT PRESENT
1437 004442 022712 000001  CMP    #1,(R2)    ;REG PRESENT, IS IT CORE?
1438 004446 001407      BEQ    TST12      ;YES, DO* THIS TEST
1439                                ;SKIP, IF THIS REG IS NOT CORE
1440 004450 062700 000010      LOOP12: ADD   #10,R0
1441 004454 005722      TST   (R2)+
1442 004456 020027 000770      CMP   R0,#TREG
1443 004462 103764      BLO  LUP12
1444 004464 000474      BR   DONE12
1445                                ;BRANCH TO DONE IF ALL REGISTERS
1446 004466 004767 007006      TST12: JSR   #7,LOCATM ;HAVE BEEN TESTED
1447                                ;LOCATE MEMORY CORRESPONDING TO THIS
1448                                ;REGISTER
1448 004472 032701 000001      BIT   #1,R1      ;ERROR RETURN INDICATED?
1449 004476 001403      BEQ   .+10       ;NO- BRANCH
1450 004500 104002      ERROR  ;NO MEMORY IN MAP CORRESPONDING TO
1451                                ;THIS REGISTER, R0 POINTS TO
1452                                ;THE ADDRESS OF THE PARITY REGISTER
1453 004502 000167 177742      JMP   LOOP12
1454 004506 012737 004542 000114  MOV   #TRP12,0#PARVEC ;SET UP PARITY TRAP RETURN
1455 004514 012770 000004 000000  MOV   #WNP,0(R0)      ;SET WRITE WRONG PARITY
1456 004522 012711 125252  MOV   #125252,0R1    ;WRITE WRONG PARITY IN TEST LOCATION
1457 004526 012770 000001 000000  MOV   #AE,0(R0)      ;SET ACTION ENABLE AND CLEAR
1458                                ;WRITE WRONG PARITY
1459 004534 005211      INC   0R1          ;DO DATIP,DATO WITH ACTION ENABLE
1460                                ;SET- SHOULD ABORT ON DATIP AND
1461                                ;RESTORE ORIGINAL DATA
1462 004536 104002      ERROR  ;NO ABORT OCCURRED ON READING LOCATION
1463                                ;WHICH SHOULD CONTAIN BAD PARITY
1464                                ;(WITH AE SET).
1465                                ;R0 POINTS TO ADDRESS OF PARITY REGISTER.
1466                                ;R1 CONTAINS ADDRESS OF TEST LOCATION
1467                                ;(VIRTUAL THRU KERNEL PAGE 1 IF KT11 IS
1468                                ;PRESENT)
1469 004540 000440      TRP12: BR   CONT12
1470 004542 005070 000000      CLR   0(R0)
1471 004546 021127 125252  CMP   0R1,#125252
1472 004552 001401      BEQ   .+4
1473 004554 104002      ERROR  ;PARITY TRAP OCCURRED- CLEAR PARITY REGISTER
1474                                ;ORIGINAL DATA RESTORED?
1475                                ;YES, BRANCH
1476                                ;NO- DATIP WHICH GOT A PARITY ERROR
1477                                ;TRAP ALTERED CONTENTS OF LOCATION
1478                                ;READ. ADDRESS OF TEST LOCATION IS IN R1
1479                                ;(IF KT11 IS PRESENT, ADDRESS IN R1
1480                                ;IS VIRTUAL THRU KERNEL PAGE 1)
1481                                ;R0 POINTS TO ADDRESS OF PARITY REGISTER
1482                                ;MAKE SURE PARITY ERROR SET WHEN
1483                                ;DATA WAS REREAD IN THE ABOVE CMP
1484                                ;DATIP WHICH GOT A PARITY ERROR TRAP
1485                                ;ALTERED THE PARITY OF THE LOCATION READ
1486                                ;R1 CONTAINS ADDRESS OF TEST LOCATION
1487                                ;(VIRTUAL THRU KERNEL 1 IF KT11 PRESENT)
1488                                ;RESTORE STACK POINTER
1489                                ;SET WRITE WRONG PARITY AND CLEAR
1490                                ;PARITY ERROR
1491                                ;REWRITE DATA WITH WRONG PARITY
1492                                ;CLEAR PARITY REGISTER
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1502 004632 005770 000000      TST   0(R0)
1503 004636 100001      BPL   .+4
1504 004640 104002      ERROR  ;DATIP, DATO TO A LOCATION CONTAINING BAD
1505                                ;PARITY WITHOUT AE SET LEFT INCORRECT
1506                                ;DATA. R0 POINTS TO THE ADDRESS OF
1507                                ;THE PARITY REGISTER. R1 CONTAINS THE
1508                                ;ADDRESS OF THE TEST LOCATION (VIRTUAL
1509                                ;THRU KERNEL PAGE 1 IF KT11 IS PRESENT)
1510                                ;CHECK PARITY ERROR BIT
1511                                ;IS PRESENT)
1512                                ;CLEAR PARITY REGISTER
1513                                ;CLEAR LOCATION TO RESTORE GOOD PARITY
1514                                ;CLEAR PARITY ERROR IF SET
1515                                ;GO CHECK FOR ANOTHER PARITY
1516                                ;REGISTER
1517                                ;RESTORE TRAPCATCHER
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1528 004676 104001      TEST13: SCOPE
1529 004700 012737 000013 177570  MOV   #13,0#DISPLY ;LOAD TEST NUMBER INTO THE DISPLAY
1530 004706 004767 006492      JSR   #7,CLRPAR
1531 004712 005767 173634      TST   NOKT
1532 004716 001004      BNE   18
1533 004720 004767 006340      JSR   #7,NRALL
1534 004724 004767 006504      JSR   #7,MAP1
1535                                ;REGISTER
1536 004730 012700 000570      18:   MOV   #MPRO,R0 ;SETUP TO GET ADDRESSES OF REGISTERS PRESENT
1537 004734 032710 000001      LUP13: BIT   #1,0R0
1538 004740 001406      BEQ   TST13
1539                                ;IF THIS REGISTER IS PRESENT, GO
1540                                ;TEST IT
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1490 004606 012737 000116 000114  MOV   #PARVEC+2,0#PARVEC ;RESTORE TRAPCATCHER
1491 004614 005211      INC   0R1          ;SINCE AE IS CLEAR, INSTRUCTION SHOULD
1492                                ;COMPLETE AND SHOULD CLEAR BAD PARITY
1493 004616 005070 000000      CLR   0(R0)
1494 004622 022711 125253  CMP   0R1,#125253,0R1 ;COMPLETE AND SHOULD CLEAR BAD PARITY
1495 004626 001401      BEQ   .+4         ;CLEAR PARITY ERROR BIT
1496 004630 104002      ERROR  ;CHECK DATA
1497                                ;DATIP, DATO TO A LOCATION CONTAINING BAD
1498                                ;PARITY WITHOUT AE SET LEFT INCORRECT
1499                                ;DATA. R0 POINTS TO THE ADDRESS OF
1500                                ;THE PARITY REGISTER. R1 CONTAINS THE
1501                                ;ADDRESS OF THE TEST LOCATION (VIRTUAL
1502                                ;THRU KERNEL PAGE 1 IF KT11 IS PRESENT)
1503                                ;CHECK PARITY ERROR BIT
1504                                ;IS PRESENT)
1505                                ;CLEAR PARITY REGISTER
1506                                ;CLEAR LOCATION TO RESTORE GOOD PARITY
1507                                ;CLEAR PARITY ERROR IF SET
1508                                ;GO CHECK FOR ANOTHER PARITY
1509                                ;REGISTER
1510                                ;RESTORE TRAPCATCHER
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1528 004676 104001      TEST13: SCOPE
1529 004700 012737 000013 177570  MOV   #13,0#DISPLY ;LOAD TEST NUMBER INTO THE DISPLAY
1530 004706 004767 006492      JSR   #7,CLRPAR
1531 004712 005767 173634      TST   NOKT
1532 004716 001004      BNE   18
1533 004720 004767 006340      JSR   #7,NRALL
1534 004724 004767 006504      JSR   #7,MAP1
1535                                ;REGISTER
1536 004730 012700 000570      18:   MOV   #MPRO,R0 ;SETUP TO GET ADDRESSES OF REGISTERS PRESENT
1537 004734 032710 000001      LUP13: BIT   #1,0R0
1538 004740 001406      BEQ   TST13
1539                                ;IF THIS REGISTER IS PRESENT, GO
1540                                ;TEST IT
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1544                                     JTESTED
1545 004756 004767 006516          TST13: JSR      87,LOCATM      JLOCATE MEMORY CORRESPONDING TO THIS
1546                                     JREGISTER, AND IF K11 IS PRESENT
1547                                     JMAP KERNEL 1 TO THAT MEMORY
1548 004762 032701 000001          BIT      #1,R1      JERROR RETURN INDICATED?
1549 004766 001403                    BEQ      .+10      JNO= BRANCH
1550 004770 104002          ERROR                                     JMAP INDICATES NO MEMORY WAS FOUND
1551                                     JCORRESPONDING TO THIS REGISTER
1552                                     JRO POINTS TO THE ADDRESS OF THE
1553                                     JPARITY REGISTER
1554 004772 000167 177744          JMP      LOOP13
1555 004776 012737 005032 000114          MOV      #TRP13,0#PARVEC      JSETUP PARITY TRAP RETURN
1556 005004 012770 000004 000000          MOV      #WNP,0(R0)          JSET WRITE WRONG PARITY
1557 005012 012711 125252          MOV      #125252,0R1        JWRITE WRONG PARITY
1558 005016 012770 000001 000000          MOV      #AE,0(R0)          JSET ACTION ENABLE AND CLEAR
1559                                     JWRITE WRONG PARITY
1560 005024 005711                    TST      0R1          JDATA WITH ACTION ENABLE SET SHOULD
1561                                     JABORT LEAVING DATA UNCHANGED
1562 005026 104002          ERROR                                     JNO ABORT ON READING BAD PARITY
1563                                     JWITH ACTION ENABLE SET, RO POINTS
1564                                     JTO THE ADDRESS OF THE PARITY REGISTER,
1565                                     JR1 CONTAINS THE ADDRESS OF THE TEST
1566                                     JLOCATION (VIRTUAL THRU KERNEL PAGE
1567                                     J1 IF K11 IS PRESENT).
1568 005030 000434                    BR       CONT13
1569 005032 005070 000000          TRP13: CLR      0(R0)          JABORT OCCURRED AS EXPECTED- CLEAR REGISTER
1570 005036 021127 125252          CMP      0R1,#125252        JORIGINAL DATA RESTORED?
1571 005042 001401                    BEQ      .+4          JYES, BRANCH
1572 005044 104002          ERROR                                     JDATA WHICH GOT A PARITY ERROR ALTERED
1573                                     JTHE CONTENTS OF THE LOCATION ADDRESSED,
1574                                     JR1 CONTAINS THE ADDRESS OF
1575                                     JMEMORY BEING TESTED- IF K11 IS
1576                                     JPRESENT, ADDRESS IN R1 IS VIRTUAL)
1577                                     JRO POINTS TO THE ADDRESS OF THE
1578                                     JPARITY REGISTER
1579 005046 005770 000000          TST      0(R0)          JCHECK PARITY REGISTER
1580 005052 100401                    BMI      .+4          JBRANCH IF PARITY ERROR SET
1581 005054 104002          ERROR                                     JPARITY ERROR NOT SET AFTER READING
1582                                     JDATA WITH BAD PARITY
1583                                     JRO POINTS TO THE ADDRESS OF THE PARITY
1584                                     JREGISTER, R1 CONTAINS THE ADDRESS
1585                                     JOF THE TEST LOCATION (VIRTUAL THRU
1586                                     JKERNEL PAGE 1 IF K11 PRESENT)
1587 005056 022626          CMP      [SP]+,[SP]+
1588 005060 012770 000004 000000          MOV      #WNP,0(R0)          JRESTORE STACK POINTER
1589 005066 012711 125252          MOV      #125252,0R1        JSET WRITE WRONG PARITY, CLEAR PARITY ERROR
1590 005072 005070 000000          CLR      0(R0)          JREWRITE DATA WITH WRONG PARITY
1591 005076 012737 000116 000114          MOV      #PARVEC+2,0#PARVEC JCLEAR PARITY REGISTER
1592 005104 005711                    TST      0R1          JRESTORE TRAPCATCHER
1593                                     JDATA TO LOCATION WITH BAD PARITY
1594                                     JAE NOT SET-INSTRUCTION SHOULD COMPLETE
1595 005106 005070 000000          CLR      0(R0)          JCLEAR PARITY ERROR BIT
1596 005112 022711 125252          CMP      #125252,0R1        JCHECK DATA
1597 005116 001401                    BEQ      .+4
1598 005120 104002          ERROR                                     JDATA TO LOCATION WITH BAD PARITY

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1598                                     JWITHOUT ACTION ENABLE SET LEFT INCORRECT DATA
1599                                     JR1 CONTAINS THE ADDRESS OF THE TEST
1600                                     JLOCATION (VIRTUAL THRU KERNEL PAGE 1
1601                                     JIF K11 IS PRESENT). RO POINTS TO THE
1602                                     JADDRESS OF THE PARITY REGISTER.
1603 005122 005070 000000          CONT13: CLR      0(R0)          JCLEAR PARITY REGISTER
1604 005126 005011                    CLP      0R1          JCLEAR LOCATION
1605 005130 005070 000000          CLR      0(R0)          JCLEAR PARITY ERROR IF SET
1606 005134 000702          BK      LOOP13          JGO CHECK FOR ANOTHER PARITY
1607                                     JREGISTER
1608 005136 012737 000116 000114          DONE13: MOV     #PARVEC+2,0#PARVEC JRESTORE TRAPCATCHER
1609 005144 005767 173402          TST      #NKT
1610 005150 001002                    BNE     .+6
1611 005152 005037 177572          CLR      0#SR0          JTURN OFF K11 IF PRESENT
1612
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1616                                     J*****
1617                                     JCHECK PARITY MEMORY WITH SERIES OF PATTERNS FROM 4K TO 20K
1618                                     JENABLE PARITY TRAP
1619                                     J*****
1620 005156 104001          TEST14: SCUPE
1621 005160 012737 000014 177570          MOV      #14,0#DISPLY      JLOAD TEST NUMBER INTO THE DISPLAY
1622 005166 005067 010630          CLR      IMAX              JDON'T ITERATE THE REST OF THE SUBTESTS
1623 005172 004767 006166          JSR      PC,CLRPAR        JCLEAR ALL PARITY REGISTERS
1624 005176 012737 005500 000114          MOV      #TRP14,0#PARVEC      JSETUP PARITY TRAP RETURN
1625 005204 012767 000002 173306          MOV      #2,BITPT          JINITIALIZE BANK INDICATOR TO BANK 1
1626 005212 012767 020000 173276          MOV      #20000,ADRPT       JINITIALIZE MEMORY STARTING ADDRESS
1627 005220 036767 173274 173644          LOOP14: BIT     BITPT,PMEML   JDOES THIS 4K HAVE PARITY?
1628 005226 001012                    BNE     TST14             JYES, TEST IT
1629 005230 062767 020000 173260          LUP14: ADD     #20000,ADRPT    JNO= UPDATE MEMORY ADDRESS
1630 005236 006367 173256          ASL      BITPT            JUPDATE BIT POINTER
1631 005242 022767 000200 173250          CMP      #200,BITPT        JTHIS 20K DONE?
1632 005250 003363          BGT      LOOP14          JNO, BRANCH TO SEE IF NEXT 4K
1633                                     JSHOULD BE TESTED
1634 005252 000443                    BR       DONE14          JYES, EXIT
1635 005254 012704 001040          TST14: MOV     #PARPAT,R4    JINITIALIZE PATTERN POINTER
1636 005260 016767 173232 173242          MOV      ADRPT,HIADR       JSET UPPER LIMIT FOR THIS 4K
1637 005266 062767 020000 173234          ADD     #20000,HIADR
1638 005274 016705 173216          MOV      ADRPT,R5
1639 005300 005025                    CLR     (5)+             JINITIALLY CLEAR CORE BLOCK UNDER TEST
1640 005302 020567 173222          CMP      R5,HIADR
1641 005306 103774                    BLO     2#
1642 005310 012701 000570          MOV      #MPRO,R1          JINITIALIZE TO SET AE IN ALL REGISTERS
1643 005314 032711 000001          3#1: BIT     #1,0R1
1644 005320 001003                    BNE     .+10
1645 005322 012771 000001 000000          MOV      #AE,0(R1)         JSET ACTION ENABLE IF REGISTER IS PRESENT
1646 005330 062701 000010          ADD     #10,R1
1647 005334 020127 000770          CMP      R1,#TREG
1648 005340 103765                    BLO     3#
1649 005342 004767 000024          4#1: JSR      87,TPCORE     JGO TO ROUTINE TO EXERCISE THIS 4K
1650 005346 005724                    TST     (4)+
1651 005350 005714                    TST     (4)              JWITH THE CURRENT PATTERN

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1652 005352 001373 BNE 4# ;NO, LOOP
1653 005354 004767 006004 JSR PC,CLRPAR ;YES, CLEAR ALL PARITY REGISTERS
1654 005360 000723 BR LUP14 ;UPDATE AND CHECK NEXT 4K
1655 005362 012737 000116 000114 DONE14: MOV #PARVEC+2,#PARVEC ;RESTORE TRAP CATCHER
1656 005370 000473 BR TEST15 ;GO TO NEXT TEST
1657
1658 ;ROUTINE TO WRITE AND CHECK EACH LOCATION IN 4K (STARTING AT ADDRESS
1659 ;IN ADRPT) WITH VALUE POINTED TO BY R4
1660 005372 016705 173120 TPCORE: MOV ADRPT,R5 ;SETUP R5 TO ADDRESS MEMORY
1661 ;LOCATION BEING CHECKED
1662 005376 011415 1# MOV (4),(5) ;WRITE PATTERN INTO MEMORY
1663 005400 011567 173132 MOV (5),WAS ;READ TEST LOCATION
1664 005404 021467 173126 CMP (4),WAS ;DATA OK?
1665 005410 001401 BEQ .+4 ;YES= BRANCH
1666 005412 104002 ERROR ;DATA INCORRECT IN LOCATION WHOSE
1667 ;ADDRESS IS IN R5. R4 POINTS TO THE
1668 ;DATA WRITTEN.
1669 005414 005725 TST (5)+ ;UPDATE ADDRESS POINTER
1670 005416 020567 173106 CMP R5,HIADR ;THIS 4K DONE?
1671 005422 103765 BLO 1# ;NO, BRANCH TO TEST NEXT LOCATION
1672 005424 005067 173340 CLR TREG ;YES, DID ANY PARITY ERRORS OCCUR
1673 ;WITHOUT TRAPPING?
1674 005430 012701 000570 MOV #MPRO,R1
1675 005434 032711 000001 2# BIT #1,(R1)
1676 005440 001003 BNE .+10
1677 005442 005771 000000 TST @R1
1678 005446 100406 BMI 3# ;YES= BRANCH
1679 005450 062701 000010 ADD #10,R1
1680 005454 020127 000770 CMP R1,#TREG
1681 005460 103765 BLO 2#
1682 005462 000207 RTS #7 ;NO, RETURN
1683 005464 011167 173300 3# MOV @R1,TREG ;STORE ADDRESS OF REGISTER GETTING ERROR
1684 005470 104004 ERRORS ;PARITY ERROR SET (WITH AE SET) AND
1685 ;NO TRAP OCCURRED. TREG CONTAINS
1686 ;ADDRESS OF PARITY REGISTER WHICH
1687 ;HAS ERROR BIT SET.
1688 005472 004767 006370 JSR #7,PSCAN ;SCAN FOR PARITY ERRORS AND PRINT
1689 ;1# BIT ADDRESSES OF THOSE FOUND,
1690 ;AFTER REPORTING EACH ERROR CLEAR IT
1691 005476 000207 RTS #7
1692
1693 ;PARITY TRAP SERVICE (NO TRAPS TO 114 SHOULD OCCUR IN THIS SUBTEST)
1694 TRP14: CLR TREG
1695 005500 005067 173264 MOV #MPRO,R1 ;FIND PARITY REGISTER INDICATING PARITY ERROR
1696 005504 012701 000570 1# BIT #1,(R1)
1697 005510 032711 000001 BNE .+10
1698 005514 001003 TST @R1
1699 005516 005771 000000 BMI 2# ;BRANCH IF PARITY ERROR SET
1700 005522 100407 ADD #10,R1
1701 005524 062701 000010 CMP R1,#TREG
1702 005530 020127 000770 BLO 1#
1703 005534 103765 ERPOP ;PARITY TRAP TO 114 OCCURRED DURING
1704 005536 104002 BR 3# ;TEST 14 BUT NO REGISTERS HAVE
1705 ;PARITY ERROR SET

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1706 005542 011167 173222 2# MOV @R1,TREG ;STORE ADDRESS OF REGISTER GETTING ERROR
1707 005546 104004 ERRORS ;PARITY TRAP TO 114 OCCURRED DUE TO
1708 ;PARITY ERROR WHILE EXERCISING MEMORY
1709 ;R1 POINTS TO THE ADDRESS OF THE
1710 ;PARITY REGISTER HAVING PARITY ERROR
1711 ;BIT SET
1712 005550 004767 006312 JSR #7,PSCAN ;SCAN FOR BAD PARITY AND TYPE 1# BIT ADDRESSES
1713 ;OF LOCATIONS FOUND BAD
1714 005554 022626 3# CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
1715 005556 000207 RTS #7 ;RETURN (FROM JSR TO TPCORE) TO
1716 ;CHECK NEXT PATTERN
1717
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1720 ;*****
1721 ;CHECK PARITY MEMORY WITH SERIES OF PATTERNS ABOVE 28K
1722 ;ENABLE PARITY ERROR TRAPPING
1723 ;*****
1724 005560 104001 TEST15: SCOPE
1725 005562 012737 000015 177570 MOV #15,#DISPLY ;LOAD TEST NUMBER INTO THE DISPLAY
1726 005570 005767 172756 TST NOKT ;KT11 PRESENT?
1727 005574 001402 BEQ .+6 ;YES= BRANCH
1728 005576 000167 000424 JMP TEST16 ;NO, SKIP TEST
1729 005602 004767 005556 JSR PC,CLRPAR ;CLEAR ALL PARITY REGISTERS
1730 005606 004767 005452 JSR #7,NRALL ;MAP KERNEL 0 TO BANK 0,RW
1731 005612 004767 005616 JSR #7,MAP1 ;MAP KERNEL 7 TO THE EXTERNAL BANK
1732 ;SET KERNEL 1 RW AND TURN ON KT11
1733 005616 012777 001600 173416 MOV #1600,#KPAR1 ;MAP KERNEL PAGE 1 TO BEGINNING OF 28-32K
1734 005624 005067 172726 CLR LOWFLG ;CLEAR FLAG TO INDICATE CHECKING LOWER 64K
1735 005630 016767 173236 MOV PMENH,PMEMX
1736 005636 012737 006146 000114 MOV #TRP15,#PARVEC ;SETUP PARITY TRAP RETURN
1737 005644 012767 000200 172646 MOV #200,BITPT ;INITIALIZE BIT POINTER
1738 005652 036767 172642 173216 LOOP15: BIT BITPT,PMEMX ;DOES THIS 4K HAVE PARITY?
1739 005660 001022 BNE TST15 ;YES, BRANCH TO TEST IT
1740 005662 062777 000200 173352 LOP15: ADD #200,#KPAR1 ;NO= MAP TO NEXT 4K
1741 005670 006367 172624 ASL BITPT ;UPDATE BIT POINTER
1742 005674 103366 BCC LOOP15 ;BRANCH IF NOT DONE WITH 64K
1743 005676 005767 172654 TST LOWFLG ;DONE WITH 128K?
1744 005702 001051 BNE DONE15 ;YES, BRANCH
1745 005704 005267 172646 INC LOWFLG ;NO, SET FLAG INDICATING UPPER 64K
1746 005710 016767 173160 173160 MOV PMENH,PMEMX ;SETUP PARITY MAP WORD
1747 005716 012767 000001 172574 MOV #1,BITPT ;SETUP BIT POINTER FOR UPPER 64K
1748 005724 000752 BR LOOP15 ;CONTINUE
1749 005726 012704 001040 TST15: MOV #PARPAT,R4 ;INITIALIZE PATTERN POINTER
1750 005732 012767 020000 172556 MOV #20000,ADRPT ;INITIALIZE VIRTUAL ADDRESS OF MEMORY
1751 ;BEING TESTED
1752 005740 012705 020000 MOV #20000,R5
1753 005744 005025 2# CLR (5)+ ;INITIALLY CLEAR CORE BLOCK UNDER TEST
1754 005746 020527 040000 CMP R5,#40000
1755 005752 103774 BLO 2#
1756 005754 012701 000570 MOV #MPRO,R1 ;INITIALIZE TO SET ACTION ENABLE IN ALL
1757 ;PARITY REGISTERS
1758 005760 032711 000001 3# BIT #1,@R1
1759 005764 001003 BNE .+10

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1760 005766 012771 000001 000000      MOV      *AE,0(R1)      ;SET ACTION ENABLE IF THIS REGISTER
1761                                     ;IS PRESENT
1762 005774 062701 000010      ADD      #10,R1
1763 006000 020127 000770      CNP     R1,*TREG
1764 006004 103765      BLO     38
1765 006006 004767 000030      JSR     #7,TPCORX    ;EXERCISE THIS 4K
1766 006012 005724      TST     (4)+         ;UPDATE PATTERN
1767 006014 005714      TST     (4)         ;LAST PATTERN?
1768 006016 001373      BNE     48           ;NO, LOOP
1769 006020 004767 005340      JSP     PC,CLRPAR    ;YES, CLEAR ALL PARITY REGISTERS
1770 006024 000716      BR      LOP15        ;UPDATE AND CHECK NEXT 4K
1771 006026 005037 177572      CLR     #BRO        ;TURN OFF KT11 WHEN DONE
1772 006032 012737 000116      MOV     *PARVEC+2,0#PARVEC ;RESTORE TRAPCATCHER
1773 006040 000472      BR      TEST16      ;GO TO NEXT TEST
1774
1775 ;PARITY MEMORY TEST ROUTINE USING KT11 AND TESTING MEMORY ABOVE 28K
1776 ;WRITES AND CHECKS EACH LOCATION IN 4K USING KERNEL PAGE 1 MAPPED TO CURRENT BANK
1777 006042 000240      TPCORX1 NOP
1778 006044 012705 020000      MOV     #20000,R5   ;SETUP R5 TO POINT TO THE LOCATION
1779                                     ;UNDER TEST (VIRTUAL ADDRESS)
1780 006050 011415      18:    MOV     (4),(5) ;WRITE PATTERN
1781 006052 011567 172460      MOV     (5),WAS    ;READ TEST LOCATION
1782 004056 021467 172454      CNP     (4),WAS    ;DATA OK?
1783 006062 001401      BEQ     .+4        ;YES- BRANCH
1784 006064 104002      ERROR
1785                                     ;NO- DATA INCORRECT IN LOCATION WHOSE
1786 ;VIRTUAL ADDRESS IS IN R1 (GOES THRU
1787 ;KERNEL PAGE 1). R4 POINTS TO
1788 ;THE VALUE WRITTEN.
1789 006070 020527 040000      TST     (5)+       ;UPDATE ADDRESS POINTER
1790 006074 103765      CNP     R5,#40000  ;THIS 4K DONE?
1791 006076 005067 172666      BLO     18         ;NO, BRANCH TO TEST NEXT LOCATION
1792                                     ;YES, CHECK TO SEE IF ANY PARITY
1793 ;ERRORS OCCURRED WITHOUT TRAPPING
1794 006102 012701 000570      MOV     #MPRO,R1   ;IS THIS PARITY REGISTER PRESENT?
1795 006106 032711 000001      BIT     #1,(R1)
1796 006112 001003      BNE     .+10       ;NO, GET NEXT ONE
1797 006114 005771 000000      TST     0(R1)     ;YES- DID ERROR SET?
1798 006120 100406      BMI     38         ;YES- BRANCH
1799 006122 062701 000010      ADD     #10,R1    ;NO- GET NEXT REGISTER
1800 006126 020127 000770      CNP     R1,*TREG
1801 006132 103765      BLO     28
1802 006134 000207      RTS     #7         ;NO ERRORS- EXIT
1803 006136 011167 172626      MOV     #R1,TREG  ;STORE ADDRESS OF REGISTER GETTING ERROR
1804 006142 104004      ERRORS
1805                                     ;PARITY ERROR SET (AE ALREADY SET)
1806                                     ;AND NO TRAP OR TIMEOUT OCCURRED
1807 006144 000207      RTS     #7         ;R1 POINTS TO THE ADDRESS OF THE
1808                                     ;PARITY REGISTER
1809
1810 ;PARITY TRAP SERVICE (NO TRAPS TO 114 SHOULD OCCUR IN THIS SUBTEST)
1811 006146 005067 172616      TRP15: CLR     TREG
1812 006152 012701 000570      MOV     #MPRO,R1
1813 006156 032711 000001      18:    BIT     #1,(R1) ;LOCATE PARITY REGISTER INDICATING ERROR
1814 006162 001003      BNE     .+10

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1814 006164 005771 000000      TST     0(R1)
1815 006170 100407      BMI     28         ;BRANCH IF PARITY ERROR IS SET
1816 006172 062701 000010      ADD     #10,R1
1817 006176 020127 000770      CNP     R1,*TREG
1818 006202 103765      BLO     16
1819 006204 104002      ERROR
1820                                     ;TRAP TO 114 OCCURRED DURING TEST 15 BUT
1821 ;NO PARITY REGISTERS HAVE PARITY ERROR SET
1822 006206 000405      BR      38
1823 006210 011167 172554      MOV     #R1,TREG  ;STORE ADDRESS OF REGISTER GETTING ERROR
1824 006214 104004      ERRORS
1825                                     ;PARITY TRAP TO 114 OCCURRED DUE TO
1826 ;PARITY ERROR WHILE EXERCISING MEMORY
1827 006216 004767 005644      JSR     #7,PSCAN   ;"TREG" CONTAINS ADDRESS OF PARITY REGISTER
1828                                     ;HAVING PARITY ERROR BIT SET
1829 ;SCAN MEMORY FOR BAD PARITY AND PRINT 18
1830 ;BIT ADDRESSES OF LOCATIONS FOUND
1831 ;CLEAR BAD PARITY IN EACH AFTER
1832 ;REPORTING IT
1833 006222 022626      38:    CNP     (SP)+,(SP)+ ;RESTORE STACK POINTER
1834 006224 000207      RTS     #7         ;RETURN (FROM JSR TO TPCORX) TO
1835                                     ;TEST NEXT PATTERN
1836
1837 ;*****
1838 ;FORCE WRONG PARITY IN EACH BYTE OF PARITY MEMORY FROM 4K TO 28K
1839 ;WRITE WRONG PARITY AND READ IT BACK WITH ACTION ENABLE SET, MAKING
1840 ;SURE THAT A TRAP OCCURS. THEN WRITE GOOD PARITY AND MAKE SURE THAT
1841 ;NO TRAP OCCURS WHEN IT IS READ. MAKE SURE THAT THE ERROR ADDRESS BITS
1842 ;(PARITY REGISTER BITS 5-11) ARE CORRECT.
1843 ;*****
1844 006226 104001      TEST16: SCOPE
1845 006230 012737 000016 177570      MOV     #16,#DISPLY ;LOAD TEST NUMBER INTO THE DISPLAY
1846 006236 012737 006804 000114      MOV     #TRP16,0#PARVEC ;SET UP TRAP RETURN
1847 006244 012767 000002 172246      MOV     #2,BITPT    ;INIT 4K BIT POINTER TO BANK 1
1848 006252 012767 020000 172236      MOV     #20000,ADRPT ;INIT MEMORY STARTING ADDRESS
1849 006260 036767 172234 172604      18:    BIT     BITPT,PMEML ;DOES THIS 4K HAVE PARITY?
1850 006268 001012      BNE     38         ;YES, BRANCH TO TEST IT
1851 006270 062767 020000 172220      28:    ADD     #20000,ADRPT ;NO, UPDATE MEMORY ADDRESS BY 4K
1852 006276 006367 172216      ASL     BITPT     ;UPDATE BIT POINTER
1853 006302 022767 000200 172210      CNP     #200,BITPT ;THIS 28K DONE?
1854 006310 003363      BGT     18         ;NO, CHECK NEXT 4K
1855 006312 000421      BR      DONE16    ;YES, EXIT
1856 006314 016767 172176 172206      38:    MOV     ADRPT,HIADR ;SET UPPER LIMIT THIS 4K
1857 006322 062767 020000 172200      ADD     #20000,HIADR
1858 006330 004767 005030      JSR     #7,CLRPAR  ;CLEAR ALL PARITY REGISTERS
1859 006334 016705 172156      MOV     ADRPT,R5
1860 006340 005025      58:    CLR     (5)+     ;CLEAR BANK UNDER TEST
1861 006342 020567 172162      CNP     R5,HIADR
1862 006346 103774      BLO     58
1863 006350 004767 000020      68:    JSR     #7,MWP16 ;GO WRITE WRONG PARITY IN EACH BYTE
1864 006354 000745      BR      28         ;UPDATE AND CHECK NEXT 4K
1865 006356 004767 005002      DONE16: JSR     #7,CLRPAR ;CLEAR ALL PARITY REGISTERS IF DONE
1866 006362 012737 000116 000114      MOV     #PARVEC+2,0#PARVEC ;RESTORE TRAP CATCHER
1867 006370 000167 000472      JNP     TEST17    ;GO TO NEXT TEST

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1866
1869
1870 ;WRITE WRONG PARITY TEST ROUTINE - TESTS EACH BYTE IN 4K
1871 ;USING SAME DATA VALUE, WRITES AND CHECKS PARITY IN WRONG STATE
1872 ;AND THEN IN CORRECT STATE TO PROVE THAT PARITY BITS TOGGLE
1873 WWP16: MOV ADDRPT,R5 ;SET TEST ADDRESS POINTER
1874 CLR ODDFLG ;INDICATE TESTING LOW BYTE
1875 MOV #125253,SHDSE ;STORE DATA FOR USE BY ERROR TYPEOUT ROUTINE
1876 WWP16A: MOV #125253,WR5 ;INITIALIZE TEST LOCATION
1877 MOV #MPRO,R1 ;SETUP TO LOAD PARITY REGISTERS
1878 BIT #1,(1)
1879 BNE .+10
1880 MOV #WWP+AE,@(R1) ;SET WRITE WRONG PARITY AND ACTION
1881 ;ENABLE IF THIS PARITY REGISTER
1882 ;IS PRESENT
1883 ADD #10,R1
1884 CMP R1,#TREG
1885 BLO 18
1886 TST ODDFLG ;WRITING HIGH BYTE?
1887 BMI 28 ;YES, BRANCH
1888 MOV #253,WR5 ;NO, WRITE WRONG PARITY IN LOW BYTE
1889 MOV #MPRO,R1 ;THIS CODE CLEARS WWP BIT IN ALL
1890 BIT #1,(1) ;PARITY REGISTERS
1891 BNE .+10
1892 BIC #WWP,@(R1)
1893 ADD #10,R1
1894 CMP R1,#TREG
1895 BLO 58+4
1896 TST ODDFLG ;TESTING HIGH OR LOW BYTE?
1897 BMI 68 ;BRANCH,IF HIGH BYTE
1898 BIC #377,WR5 ;DETECT WRONG PARITY WITH DATIP-
1899 ;SHOULD TRAP TO TRP16 BEFORE DOING THE DATOB
1900 BR 38 ;WRITE WRONG PARITY IN HIGH BYTE
1901 MOV #252,1(R5)
1902 BIC #377,1(R5) ;DETECT WRONG PARITY WITH DATIP-
1903 ;SHOULD TRAP TO TRP16 BEFORE DOING THE DATOB
1904 MOV #MPRO,R1 ;NO TRAP OCCURRED- SETUP TO CLEAR
1905 ;AE AND WWP
1906 BIT #1,@R1
1907 BNE .+10
1908 BIC #WWP+AE,@(R1) ;CLEAR AE AND WWP IN ALL PARITY REGISTERS
1909 ADD #10,R1
1910 CMP R1,#TREG
1911 BLO 48
1912 ERROR
1913 ;ERROR, NO TRAP AFTER WRITING AND
1914 ;READING WRONG PARITY IN LOCATION
1915 ;WHOSE ADDRESS IS IN R5 (AE AND WWP
1916 ;WERE SET IN ALL PARITY REGISTERS)
1917 ;TESTING LOW BYTE IF ODDFLG IS POSITIVE
1918 ;TESTING HIGH BYTE IF ODDFLG IS NEGATIVE
1919 ;NOTE THAT AE AND WWP WERE CLEARED
1920 ;BEFORE TYPING THE ERROR PRINTOUT
1921 006602 000517 BR CN16

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1922 ;WHEN WRONG PARITY DATA IS READ BACK SHOULD ENTER HERE VIA TRAP TO 114
1923 TRP16: MOV #MPRO,R1 ;PARITY TRAP OCCURRED- FIRST CLEAR
1924 TRP16A: BIT #1,@R1 ;WWP AND AE IN ALL REGISTERS
1925 BNE .+10
1926 BIC #AE+WWP,@(R1)
1927 ADD #10,R1
1928 CMP R1,#TREG
1929 BLO TRP16A
1930 MOV #MPRO,R1 ;FIND THE REGISTER THAT SENSED THE ERROR
1931 MOV #LNDC0,R3
1932 CLR TREG
1933 BIT #1,@R1 ;DOES THIS CONTROL EXIST?
1934 BNE 28 ;NO, BRANCH
1935 TST @R1 ;YES- IS ERROR SET?
1936 BPL 28 ;NO, BRANCH
1937 TST TREG ;YES- WAS IT SET IN ANY OTHER REGISTER ALSO?
1938 BEQ .+4 ;NO- BRANCH
1939 ERROR ;ERROR SET IN MORE THAN ONE PARITY REGISTER
1940 ;AFTER WRITING WRONG PARITY IN LOCATION
1941 ;WHOSE ADDRESS IS IN R5
1942 006676 036761 171616 000002 BIT R1PT,2(R1) ;DOES MAP INDICATE THIS PARITY REGISTER
1943 ;CONTROLS THIS MEMORY?
1944 BNE .+4 ;YES, BRANCH
1945 006706 104002 ERROR ;PARITY REGISTER RESPONDED TO MEMORY
1946 ;NOT INCLUDED IN ITS MAP
1947 ;PARITY REGISTER'S ADDRESS IS POINTED
1948 ;TO BY R1. ADDRESS OF LOCATION CAUSING
1949 ;PARITY ERROR IS IN R5
1950 MOV R3,R4
1951 MOV @R1,TREG ;STORE REGISTER ADDRESS
1952 ADD #10,R1
1953 TST (R3)+
1954 CMP R1,#TREG
1955 BLO 18 ;BRANCH UNTIL ALL THE PARITY
1956 ;REGISTERS HAVE BEEN CHECKED
1957 MOV (R3),WAS ;SAVE DATA FROM LOCATION UNDER TEST
1958 CMP #125253,WR5 ;DID BIC CHANGE DATA?
1959 BEQ .+4 ;NO, CONTINUE
1960 ERRORP ;DATA WAS MODIFIED BY THE BIC WHICH
1961 ;GOT A PARITY ERROR TRAP- SINCE PARITY ERROR
1962 ;TRAP OCCURRED, COMMENTS SHOULD NOT HAVE
1963 ;BEEN MODIFIED. R5 CONTAINS ADDRESS
1964 ;OF TEST LOCATION, "TREG" CONTAINS
1965 ;ADDRESS OF PARITY REGISTER SENSING
1966 ;ERROR
1967 006746 005787 172016 TST TREG ;WAS PARITY ERROR SET IN ANY REGISTERS?
1968 006752 001002 BNE 38 ;YES- BRANCH
1969 006754 104002 ERROR ;PARITY TRAP OCCURRED ON READING
1970 ;WRONG PARITY (WITH AE SET) BUT NO
1971 ;REGISTERS HAD PARITY ERROR BIT SET.
1972 ;R5 CONTAINS THE ADDRESS OF THE
1973 ;TEST LOCATION.
1974 006756 000420 BR 48
1975 006760 022714 000001 38: CMP #1,(R4)

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1976 006764 001015 BNE 48
1977 006766 017701 171776 MOV #TREG,R1 ;GET PARITY REGISTER CONTENTS
1978 006772 042701 170037 BIC #170037,R1 ;MASK OFF ALL BUT ERROR ADDRESS BITS
1979 006776 010502 MOV R5,R2 ;GET ADDRESS OF LOCATION UNDER TEST
1980 007000 042702 003777 BIC #3777,R2 ;POSITION BITS IN R2
1981 007004 000302 SWAB R2
1982 007006 006302 ASL R2
1983 007010 006302 ASL R2
1984 007012 020102 CMP R1,R2 ;PARITY ERROR ADDRESS BITS CORRECT?
1985 007014 001401 BEQ .+4
1986 007016 104003 ERRORP ;ERROR ADDRESS BITS (PARITY REGISTER
;BITS 11-5) ARE INCORRECT. R5 CONTAINS
;THE ADDRESS OF THE TEST LOCATION.
;TREG* CONTAINS THE ADDRESS OF THE
;PARITY REGISTER DETECTING THE ERROR
1991 007020 022626 481 CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
1992 007022 011515 CNT161 MOV (5),(5) ;RESTORE TEST LOCATION TO FIX BAD PARITY
1993 007024 005077 171740 CLR ;CLEAR ERROR BIT IN PARITY REGISTER
1994 007030 005715 TST #R5 ;READ LOCATION TO SEE IF PARITY IS GOOD
1995 007032 005777 171732 TST #TREG ;IS PARITY ERROR SET?
1996 007036 100001 BPL .+4 ;NO- BRANCH
1997 007040 104002 ERRORP ;WRITING LOCATION WITH WRITE WRONG PARITY
1998 ;CLEAR DIDN'T CLEAR BAD PARITY
1999 ;R5 CONTAINS ADDRESS OF THE TEST
2000 ;LOCATION. TREG* CONTAINS THE ADDRESS
2001 ;OF THE PARITY REGISTER DETECTING
2002 ;THE ERROR
2003 007042 005167 171512 CN161 CUM ODDFLG ;TOGGLE BYTE INDICATOR
2004 007046 100401 BHI .+4 ;BRANCH IF READY TO TEST HIGH BYTE
2005 007050 005725 TST (5)+ ;UPDATE ADDRESS POINTER
2006 007052 020567 171452 CMP R5,HIADR ;THIS 4K DONE?
2007 007056 103401 BLO 18 ;NO, TEST NEXT LOCATION
2008 007060 000207 RTS #7 ;RETURN TO TEST NEXT BANK
2009 007062 000167 177324 181 JMP WWP16A

;*****
;FORCE WRONG PARITY IN EACH BYTE OF PARITY MEMORY ABOVE 20K
;WRITE WRONG PARITY AND READ IT WITH ACTION ENABLE SET, MAKING SURE
;THAT A TRAP OCCURS, THEN WRITE AND READ THE SAME LOCATION WITH GOOD PARITY
;(USING SAME DATA) TO SHOW THAT THE PARITY BIT TOGGLES, MAKE SURE THAT
;THE ERROR ADDRESS BITS (PARITY REGISTER BITS 5-11) ARE CORRECT.
;*****
TEST17: SCOPE
2021 007070 012737 000017 177570 MOV #17,#DISPLY ;LOAD TEST NUMBER INTO THE DISPLAY
2022 007076 005767 171450 TST NOKT ;KIT11 PRESENT?
2023 007102 001402 BEQ .+6 ;YES, BRANCH
2024 007104 000167 000636 JMP XFR1 ;NO, SKIP TO NEXT TEST
2025 007110 004767 004250 JSR PC,CLHPAR ;CLEAR ALL PARITY REGISTERS
2026 007114 012737 007456 000114 MOV #TRP17,#PARVEC ;SETUP FOR PARITY TRAP
2027 007122 012767 000200 171370 MOV #200,BITPT ;INITIALIZE 4K BIT POINTER
2028 007130 004767 004130 JSR #7,NRALL ;INITIALIZE ALL PAGES TO NON-RESIDENT
2029 007134 004767 004274 JSR #7,MAP1 ;MAP KERNEL 0 TO BANK 0,RW; KERNEL 7

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2030 ;TO THE EXTERNAL BANK, RW. TURN ON
2031 ;THE KIT11 AND MAKE KERNEL 1 RW
2032 007140 012777 001600 172074 MOV #1600,#KPAR1 ;INITIALIZE KERNEL PAGE 1 TO 20K
2033 007146 005067 171404 CLR LOWFLG ;CLEAR FLAG TO INDICATE TESTING LOWER 64K
2034 007152 016767 171714 171716 MOV PMENH,PMENX
2035 007160 012767 000002 000366 MOV #2,INDX17 ;SETUP OFFSET TO CHECK LOWER 64K OF MAPS
2036 007166 036767 171326 171702 181 BIT BITPT,PMENX ;DOES THIS 4K HAVE PARITY?
2037 007174 001025 BNE 36 ;YES, BRANCH TO TEST IT
2038 007176 062777 000200 172036 281 ADD #200,#KPAR1 ;NO, MAP TO NEXT 4K
2039 007204 006367 171310 ASL BITPT ;UPDATE BIT POINTER
2040 007210 103366 BCC 16 ;GO CHECK TO SEE IF THIS 4K HAS PARITY
2041 007212 005767 171340 TST LOWFLG ;END OF 120K?
2042 007216 001025 BNE DONE17 ;YES, EXIT
2043 007220 005267 171332 INC LOWFLG ;NO. SET FLAG TO INDICATE SHIFT TO
2044 007224 016767 171644 171644 MOV PMENH,PMENX ;HIGH 64K AND CHANGE MAPS
2045 007232 012767 000001 171260 MOV #1,BITPT
2046 007240 012767 000004 000306 MOV #4,INDX17 ;SETUP OFFSET TO CHECK UPPER 64K OF MAPS
2047 007246 000747 BR 18
2048 007250 012705 020000 381 MOV #20000,R5
2049 007254 005025 581 CLR (5)+ ;CLEAR BANK UNDER TEST
2050 007256 020527 040000 CMP R5,#40000
2051 007262 103774 BLO 56
2052 007264 004767 000020 681 JSR #7,WWP17 ;GO WRITE WRONG PARITY AND CHECK IT
2053 007270 000742 BR 28 ;UPDATE AND CHECK NEXT 4K
2054 007272 005037 177572 DONE17 CLR #88R0 ;TURN OFF KIT11 WHEN DONE
2055 007276 012737 000116 000114 MOV #PARVEC+2,#PARVEC ;RESTORE TRAP CATCHER
2056 007304 000167 000436 JMP XFR1 ;GO TO SETUP FOR NEXT TEST
2057
2058 ;WRITE WRONG PARITY TEST ROUTINE TO TEST MEMORY ABOVE 20K
2059 007310 012705 020000 WWP17: MOV #20000,R5 ;SET TEST ADDRESS POINTER
2060 007314 005067 171240 CLR ODDFLG ;CLEAR FLAG TO INDICATE TESTING LOW BYTE
2061 007320 012767 125253 171206 MOV #125253,SHDB ;STORE DATA FOR USE BY ERROR TYPEOUT ROUTINE
2062 007326 012715 125253 WWP17A: MOV #125253,OR5 ;INITIALIZE LOCATION
2063 007332 012701 000570 MOV #MPK0,R1 ;INITIALIZE REGISTER ADDRESS POINTER
2064 007336 032711 000001 181 BIT #1,(1) ;DOES THIS CONTROL EXIST?
2065 007342 001003 BNE .+10 ;NO. GET NEXT
2066 007344 012771 000005 000000 MOV #WP+AE,#(R1) ;YES- SET WRITE WRONG PARITY
2067 ;AND ACTION ENABLE
2068 007352 062701 000010 ADD #10,R1
2069 007356 020127 000770 CMP R1,#TREG ;ALL REGISTERS SETUP?
2070 007362 103765 BLO 18 ;NO- LOOP
2071 007364 005767 171170 TST ODDFLG ;YES- TESTING HIGH BYTE?
2072 007370 100405 BHI 28 ;YES, BRANCH
2073 007372 112715 000253 MOV #253,OR5 ;NO, WRITE WRONG PARITY IN LOW BYTE
2074 007376 142715 000377 BIC #377,OR5 ;DETECT WRONG PARITY WITH DATIP-
;SHOULD TRAP TO TRP17 BEFORE DOING THE DATOB
2075
2076 007402 000406 BR 36
2077 007404 112765 000252 000001 281 MOV #252,1(R5) ;WRITE WRONG PARITY IN HIGH BYTE
2078 007412 142765 000377 000001 BIC #377,1(R5) ;DETECT WRONG PARITY WITH DATIP
;SHOULD TRAP TO TRP17 BEFORE DOING THE DATOB
2079
2080 007420 012701 000570 381 MOV #MPK0,R1 ;IF NO TRAP, CLEAR AE AND WWP IN ALL
2081 007424 032711 000001 481 BIT #1,#R1 ;PARITY REGISTERS
2082 007430 001003 BNE .+10
2083 007432 042771 000005 000000 BIC #AE+WWP,#(R1)

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2084 007440 062701 000010 ADD #10,R1
2085 007444 020127 000770 CMP R1,#TREG
2086 007450 103765 BLO 48
2087 007452 104002 ERROR ;NO TRAP AFTER WRITING AND READING
2088 ;WRONG PARITY WITH AE SET= VIRTUAL
2089 ;ADDRESS OF LOCATION IS IN R5
2090 ;(MAPPED THRU KERNEL PAGE 1)
2091 ;WROTE LOW BYTE IF ODDFLG IS POSITIVE
2092 ;WROTE HIGH BYTE IF IT IS NEGATIVE
2093 ;NOTE THAT WWP AND AE WERE CLEARED
2094 ;BEFORE ERROR PRINTOUT
2095 007454 000512 BR CNT17
2096
2097 ;WHEN WRONG PARITY DATA IS READ BACK, SHOULD ENTER HERE VIA TRAP TO 114
2098 TRP171 MOV #MPRO,R1 ;PARITY TRAP OCCURRED= BEFORE CHECKING
2099 007462 032711 000001 TRP171A BIT #1,#R1 ;IT, CLEAR WWP AND AE IF ALL REGISTERS
2100 007466 001003 BNE .+10
2101 007470 042771 000005 000000 BIC #AE+WWP,#(R1)
2102 007476 062701 000010 ADD #10,R1
2103 007502 020127 000770 CMP R1,#TREG
2104 007506 103765 BLO TRP17A
2105 007510 012701 000570 MOV #MPRO,R1 ;FIND REGISTER THAT SENSED THE ERROR
2106 007514 012703 000772 MOV #INDCO,R3 ;SETUP PTR TO INDICATOR
2107 007520 005067 171244 CLR TREG
2108 007524 032711 000001 181 BIT #1,#R1 ;DOES THIS CONTROL EXIST?
2109 007530 001017 BNE 28 ;NO, BRANCH
2110 007532 005771 000000 TST #(R1) ;YES= IS ERROR SET?
2111 007536 100014 BPL 28 ;NO, BRANCH
2112 007540 005767 171224 TST TREG ;YES= WAS IT SET IN ANY OTHER REGISTER ALSO?
2113 007544 001401 BEQ .+4 ;NO= BRANCH
2114 007546 104002 ERROR ;ERROR SET IN MORE THAN ONE PARITY REGISTER
2115 ;AFTER READING WRONG PARITY IN LOCATION
2116 ;WHOSE VIRTUAL ADDRESS IS IN R5
2117 007550 036761 170744 000002 BIT BITPT,2(R1) ;DOES MAP INDICATE THAT THIS REGISTER
2118 ;CONTROLS THIS MEMORY?
2119 007554 INDX17=.+2
2120 007556 001001 BNE .+4 ;YES= BRANCH
2121 007560 104002 ERROR ;PARITY REGISTER RESPONDED TO MEMORY
2122 ;NOT INCLUDED IN ITS MAP, R1 POINTS TO
2123 ;THE PARITY REGISTER'S ADDRESS, R5
2124 ;CONTAINS VIRTUAL ADDRESS OF THE LOCATION
2125 ;BEING TESTED (MAPPED THRU KERNEL
2126 ;PAGE 1)
2127 007562 011167 171202 MOV #R1,TREG ;STORE REGISTER ADDRESS
2128 007566 010304 MOV R3,R4 ;STORE PTR TO INDICATOR
2129 007570 062701 000010 281 ADD #10,R1
2130 007574 005723 TST #(R3)+ ;INCREMENT PTR TO INDICATOR
2131 007576 020127 000770 CMP R1,#TREG
2132 007602 103750 BLO 18 ;LOOP UNTIL ALL THE PARITY REGISTERS
2133 ;HAVE BEEN CHECKED
2134 007604 011567 170726 MOV (5),#AS ;SAVE CONTENTS OF LOCATION UNDER TEST
2135 007610 022715 125253 CMP #125253,#R5 ;DID BICB CHANGE DATA?
2136 007614 001401 BEQ .+4 ;NO, CONTINUE
2137 007616 104002 ERROR ;DATA WAS MODIFIED BY THE BICB WHICH

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2138
2139
2140
2141
2142
2143
2144 007620 005767 171144 TST TREG
2145 007624 001003 BNE 38
2146 007626 104002 ERROR ;GOT A PARITY ERROR TRAP= SINCE PARITY
2147 ;TRAP OCCURRED, CONTENTS SHOULD NOT
2148 ;HAVE BEEN MODIFIED, R5 CONTAINS TEST
2149 ;LOCATION ADDRESS (VIRTUAL, MAPPED THRU
2150 ;KERNEL PAGE 1). "TREG" CONTAINS ADDRESS OF
2151 ;PARITY REGISTER DETECTING PARITY ERROR
2152 007630 000423 BR 48 ;WAS PARITY ERROR SET IN ANY REGISTER?
2153 007632 001022 BNE 48 ;YES= BRANCH
2154 007634 022714 000001 381 CMP #1,(R4) ;PARITY TRAP OCCURRED ON READING
2155 007640 001017 BNE 48 ;WRONG PARITY WITH AE SET BUT NO
2156 ;REGISTER HAS THE PARITY ERROR BIT
2157 ;SET. R5 CONTAINS VIRTUAL ADDRESS
2158 ;OF THE TEST LOCATION (MAPPED THRU
2159 ;KERNEL PAGE 1)
2160 007642 017701 171122 MOV #TREG,R1
2161 007646 042701 170037 BIC #170037,R1
2162 007652 010502 MOV R5,R2
2163 007654 042702 163777 BIC #163777,R2
2164 007660 000302 #WAB R2
2165 007662 006302 ASL R2
2166 007664 006302 ASL R2
2167 007666 067702 171350 ADD #KPAR1,R2
2168 007672 020102 CMP R1,R2 ;PARITY ERROR ADDRESS BITS CORRECT?
2169 007674 001401 BEQ .+4 ;PARITY ERROR ADDRESS BITS (PARITY
2170 007676 104004 ERROR8 ;REGISTER BITS 11-5) INCORRECT
2171 ;"TREG" CONTAINS ADDRESS OF PARITY
2172 ;REGISTER, R5 CONTAINS THE VIRTUAL
2173 ;ADDRESS OF THE TEST LOCATION
2174 ;(MAPPED THRU KERNEL PAGE 1)
2175 ;RESTORE STACK POINTER
2176 007700 022626 481 CMP (SP)+,(SP)+
2177 007702 011515 CNT171 MOV (5),(5)
2178 007704 005077 171060 CLR #TREG
2179 007710 005715 TST #R5
2180 007712 005777 171052 TST #TREG
2181 007716 100001 BPL .+4 ;READ LOCATION TO SEE IF PARITY IS GOOD
2182 007720 104002 ERROR ;IS PARITY ERROR SET?
2183 ;NO, BRANCH
2184 ;WRITING LOCATION WITH WRITE WRONG
2185 ;PARITY CLEAR DIDN'T CLEAR BAD PARITY
2186 ;"TREG" CONTAINS THE ADDRESS OF THE
2187 ;PARITY REGISTER, R5 CONTAINS THE
2188 ;VIRTUAL ADDRESS OF THE TEST LOCATION
2189 ;(MAPPED THRU KERNEL PAGE 1)
2190 007722 006167 170632 COM ODDFLG
2191 007726 100401 BMI .+4 ;TOGGLE BYTE INDICATOR
2192 007730 005725 TST (5)+ ;BRANCH IF HIGH BYTE NOT YET TESTED
2193 007732 020527 040000 CMP R5,#40000 ;UPDATE ADDRESS POINTER
2194 ;THIS 4K DONE?

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2192 007736 103401          BLO 18          ;NO,TEST NEXT LOCATION
2193 007740 000207          RTS 17          ;YES, RETURN TO CHECK FOR NEXT
2194                                ;BANK TO BE TESTED
2195 007742 000167 177360 18: JMP WWP17A      ;GO AND TEST NEXT LOCATION
2196 007746 104001 XFR1: SCOPE
2197 ;IF THE FIRST BANK (BANK 0) IS PARITY MEMORY, SETUP TO TEST IT
2198 ;COPY THE FIRST 4K TO THE SECOND 4K, MOVE THE STACK POINTER TO BANK 1,
2199 ;AND THEN JUMP TO THE COPY OF TEST20 IN BANK 1
2200 007750 032767 000001 171114 BIT #1,PHEML ;IS FIRST 4K PARITY?
2201 007756 001002          BNE .+6        ;BRANCH IF YES
2202 007760 000167 001254          JMP DONE        ;NO- DONE WITH TEST
2203 007764 032767 000002 171074 BIT #2,MENL    ;IS THERE A SECOND 4K(BANK 1)?
2204 007772 001002          BNE .+6        ;YES, BRANCH
2205 007774 000167 001240          JMP DONE        ;NO, EXIT
2206 010000 005037 177776          CLR @#PS      ;CLEAR STATUS REGISTER
2207 010004 004767 003354          JSR #7,CLKPAR ;CLEAR ALL PARITY REGISTERS
2208 010010 012700 010008          MOV #10000,R0 ;R0 IS COUNTER TO MOVE 4K
2209 010014 005001          CLR R1        ;R1 POINTS TO LOCATION IN BANK 0
2210 010016 011161 020000 18: MOV @R1,20000(R1) ;COPY FROM BANK 0 TO BANK 1
2211 010022 005721          TST (R1)+     ;MOVE POINTER
2212 010024 005300          DEC R0        ;DONE WITH 4K?
2213 010026 001373          BNE 18        ;NO- BRANCH
2214 010030 062706 020000          ADD #20000,SP ;YES, MOVE STACK POINTER TO POINT TO BANK 1
2215 010034 012767 030114 025764 MOV #TEST20+20010,RETURN+20000 ;UPDATE SCOPE RETURN IN BANK 1
2216 010042 062767 020000 023144 ADD #20000,ERRA1+20000 ;UPDATE ADDRESSES USED IN ERROR TYPEOUT
2217 010050 062767 020000 023140 ADD #20000,ERRA2+20000
2218 010056 062767 020000 023142 ADD #20000,ERRA3+20000
2219 010064 062767 020000 023136 ADD #20000,ERRA4+20000
2220 010072 062767 020000 023140 ADD #20000,ERRA5+20000
2221 010100 000167 020010          JMP TEST20+20010 ;GO TO TEST 20 IN BANK 1
2222
2223
2224
2225
2226 ;*****
2227 ;IF FIRST 4K IS PARITY MEMORY, CHECK IT WITH A SERIES OF PATTERNS
2228 ;THIS SUBTEST IS RUN IN BANK 1 (20000 ABOVE THE ADDRESSES IN THE LISTING)
2229 ;*****
2229 010104 013746 177776 TEST20: MOV @#PS,-(SP) ;THESE 2 LINES DO THE SAME AS A SCOPE WITHOUT
2230 010110 004767 005614          JSR PC,SCOPEC ;USING AN EMT
2231 010114 012737 000020 177570 MOV #20,@#DISPLAY ;LOAD TEST NUMBER INTO THE DISPLAY
2232 010122 004767 003236          JSR #7,CLKPAR ;CLEAR ALL PARITY REGISTERS
2233 010126 012704 021040          MOV #PARPAT+20000,R4 ;INITIALIZE PATTERN POINTER
2234 010132 005005          CLR R5        ;INITIALLY CLEAR BANK 0
2235 010134 005025 18: CLR (5)+
2236 010136 020527 020000          CMP R5,#20000
2237 010142 103774          BLO 18
2238 010144 012737 030352 000114 MOV #TRP20+20000,@#PARVEC ;SETUP TRAP RETURN
2239 010152 012701 020570          MOV #MPRO+20000,R1 ;SETUP TO SET ACTION ENABLE IN ALL
2240                                ;PARITY REGISTERS PRESENT
2241 010156 032711 000001 28: BIT #1,R1
2242 010162 001003          BNE .+10
2243 010164 012771 000001 000000 MOV #AE,@(R1) ;SET ACTION ENABLE IF REGISTER IS PRESENT
2244 010172 062701 000010          ADD #10,R1
2245 010176 020127 020770          CMP R1,#TREG+20000

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2246 010202 103765          BLO 28          ;BRANCH UNTIL ALL REGISTER ADDRESSES
2247                                ;HAVE BEEN CHECKED
2248 010204 004767 000022 38: JSR #7,CKBK0 ;EXERCISE THIS 4K
2249 010210 005724          TST (4)+      ;UPDATE PATTERN
2250 010212 005714          TST (4)       ;LAST PATTERN?
2251 010214 001373          BNE 38        ;NO, LOOP
2252 010216 004767 003142 DONE20: JSR PC,CLKPAR ;CLEAR ALL PARITY REGISTERS
2253 010222 012737 000116 000114 MOV #PARVEC+2,@#PARVEC ;RESTORE TRAP CATCHER
2254 010230 000526          BR TEST21     ;GO TO NEXT TEST
2255
2256 ;PARITY MEMORY TEST ROUTINE
2257 ;WRITES AND CHECKS EACH LOCATION IN BANK 0 (EXCEPT 114 AND 116)
2258 ;WITH VALUE POINTED TO BY R4
2259 010232 005005          CLR R5        ;SET ADDRESS POINTER
2260 010234 011415 18: MOV (4),(5) ;WRITE PATTERN
2261 010236 021415          CMP (4),(5)   ;DATA OK?
2262 010240 001404          BEQ .+12     ;YES- BRANCH
2263 010242 013746 177776          MOV @#PS,-(SP) ;SETUP TO DO ERROR CALL VIA JSR
2264 010246 004767 002672          JSR PC,ERK    ;ERROR- DATA INCORRECT IN LOCATION
2265                                ;WHOSE ADDRESS IS IN R5. R4 POINTS
2266                                ;TO THE VALUE WRITTEN.
2267 010252 005725          TST (5)+     ;UPDATE ADDRESS POINTER
2268 010254 020527 000114          CMP R5,#114  ;DON'T CHANGE CONTENTS OF 114 AND 116
2269 010260 001002          BNE .+6
2270 010262 062705 000004          ADD #4,R5
2271 010266 020527 020000          CMP R5,#20000 ;HAS THE WHOLE BANK BEEN TESTED WITH
2272                                ;THIS PATTERN?
2273 010272 103760          BLO 18        ;NO, BRANCH TO TEST NEXT LOCATION
2274 010274 005067 010470          CLR TREG+20000 ;YES, DID ANY PARITY ERROR BITS SET?
2275 010300 012701 020570          MOV #MPRO+20000,R1
2276 010304 032711 000001 28: BIT #1,(1)
2277 010310 001003          BNE .+10
2278 010312 005771 000000          TST @R1
2279 010316 100406          BMI 38
2280 010320 062701 000010          ADD #10,R1
2281 010324 020127 020770          CMP R1,#TREG+20000
2282 010330 103765          BLD 28
2283 010332 000207          RTS #7        ;NO- RETURN
2284 010334 013746 177776 38: MOV @#PS,-(SP) ;SETUP TO DO ERROR CALL VIA JSR
2285 010340 004767 002600          JSR PC,ERK    ;ERROR- PARITY ERROR BIT SET AND NO
2286                                ;PARITY TRAP OCCURRED
2287                                ;(AE WAS SET) - R1 POINTS TO ADDRESS
2288                                ;OF PARITY REGISTER
2289 010344 022626          CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
2290 010346 000167 177644          JMP DONE20
2291
2292 ;PARITY TRAP SERVICE (NO TRAPS TO 114 SHOULD OCCUR IN THIS SUBTEST)
2293 TRP20: CLR TREG+20000
2294 010356 012701 020570          MOV #MPRO+20000,R1 ;FIND THE REGISTER RECORDING A PARITY ERROR
2295 010362 032711 000001 18: BIT #1,(R1)
2296 010366 001003          BNE .+10
2297 010370 005771 000000          TST @R1
2298 010374 100412          BMI 28        ;BRANCH IF ERROR IS SET
2299 010376 062701 000010          ADD #10,R1

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2300 010402 020127 020770      CMP      R1,#TREG+20000
2301 010406 103765              BLO      18
2302 010410 013746 177776      MOV      @#PS,=(SP)
2303 010414 004767 002524      JSR      PC,ERR
2304
2305 010420 000430              BR        58
2306 010422 017102 000000      281     MOV      @R1,R2
2307 010426 005003              CLR      R3
2308 010430 005071 000000      381     CLR      @R1
2309 010434 005713              TST      @R3
2310 010436 005771 000000      TST      @R1
2311 010442 100413              BMI      48
2312 010444 005723              TST      (R3)+
2313 010446 020327 020000      CMP      R3,#20000
2314 010452 103766              BLO      38
2315 010454 010271 000000      MOV      R2,@R1
2316 010460 013746 177776      MOV      @#PS,=(SP)
2317 010464 004767 002454      JSR      PC,ERR
2318
2319
2320
2321
2322 010470 000404              BR        58
2323 010472 013746 177776      481     MOV      @#PS,=(SP)
2324 010476 004767 002442      JSR      PC,ERR
2325
2326
2327
2328
2329 010502 022626              581     CMP      (SP)+,(SP)+
2330 010504 000207              RTS      #7
2331
2332
2333
2334
2335
2336
2337
2338
2339
2340
2341 010506 013746 177776      *****
2342 010512 004767 005212      TEST21: MOV  @#PS,=(SP)
2343 010516 012737 000021 177570  JSR      PC,SCOPEC
2344 010524 004767 002634      MOV      #21,@DISPLY
2345 010530 005005              JSR      PC,CLRPAR
2346 010532 005025              CLR      R5
2347 010534 020527 020000      181     CLR      (R5)+
2348 010540 103774              CMP      R5,#20000
2349
2350
2351
2352
2353 010542 005005              BLO      18
*****
;FORCE WRONG PARITY IN EACH LOCATION IN BANK 0
;NOTE THAT THIS SUBTEST IS EXECUTED IN BANK 1 (20000 ABOVE ADDRESSES
;IN THE LISTING), MAKE SURE THAT WRONG PARITY IN EACH BYTE CAN BE DETECTED,
;AND THAT WHEN GOOD PARITY IS WRITTEN AND READ NO PARITY ERROR IS DETECTED.
;CHECK ERROR ADDRESS BITS (PARITY REGISTER BITS 5-11)
*****
;WRITE WRONG PARITY TEST ROUTINE
;USING SAME DATA VALUE, WRITES AND CHECKS PARITY IN WRONG STATE
;AND THEN IN CORRECT STATE TO PROVE THAT PARITY BITS TOGGLE
WNP21: CLR      R5
;SET TEST ADDRESS POINTER

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2354 010544 005067 170010      CLR      ODDFLG
2355 010550 012767 125253 167756  MOV      #125253,SHDBE
2356 010556 012715 125253      WNP21A: MOV      #125253,R5
2357 010562 012701 020570      MOV      @#PRO+20000,R1
2358
2359 010566 032711 000001      181     BIT      #1,(1)
2360 010572 001003              BNE      .+10
2361 010574 012771 000004 000000  MOV      #WNP,@R1
2362 010602 062701 000010      ADD      #10,R1
2363 010606 020127 020770      CMP      R1,#TREG+20000
2364 010612 103765              BLO      18
2365 010614 005767 167740      TST      ODDFLG
2366 010620 100404              BMI      28
2367 010622 112715 000253      MOV      #253,R5
2368 010626 005715              TST      (R5)
2369 010630 000405              BR        38
2370 010632 112765 000051 000001 281     MOV      #252,(R5)
2371 010640 105765 000001      TSTB   1(R5)
2372 010644 012701 020570      381     MOV      #PRO+20000,R1
2373 010650 012703 000772      MOV      #INDCO,R3
2374 010654 032711 000001      481     BIT      #1,@R1
2375 010660 001003              BNE      .+10
2376 010662 042771 000004 000000  BIC      #WNP,@R1
2377 010670 062701 000010      ADD      #10,R1
2378 010674 020127 020770      CMP      R1,#TREG+20000
2379 010700 103765              BLO      48
2380 010702 012701 020570      MOV      #PRO+20000,R1
2381 010706 005067 170056      TREG
2382 010712 032711 000001      LOOP21: BIT      #1,@R1
2383 010716 001024              BNE      58
2384 010720 005771 000000      TST      @R1
2385 010724 100021              BPL      58
2386 010726 005767 170036      TST      TREG
2387 010732 001404              BEQ      .+12
2388 010734 013746 177776      MOV      @#PS,=(SP)
2389 010740 004767 002200      JSR      PC,ERR
2390
2391
2392 010744 032761 000001 000002  BIT      #1,2(R1)
2393
2394 010752 001004              BNE      .+12
2395 010754 013746 177776      MOV      @#PS,=(SP)
2396 010760 004767 002160      JSR      PC,ERR
2397
2398
2399
2400
2401 010764 011167 170000      881     MOV      @R1,TREG
2402 010770 062701 000010      ADD      #10,R1
2403 010774 005723              TST      (R3)+
2404 010776 020127 020770      CMP      R1,#TREG+20000
2405 011002 103743              BLO      LOOP21
2406
2407 011004 005767 167760      TST      TREG
;STORE REGISTER ADDRESS
;CHECKED
;WAS PARITY ERROR SET IN ANY REGISTER?

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2408	011010	001005		BNE	68		YES= BRANCH
2409	011012	013746	177776	MOV	0*PS,=(SP)		NO= SETUP TO DO ERROR CALL VIA A JSR
2410	011016	004767	002122	JSR	PC,ERR		ERROR= NO REGISTER HAS PARITY ERROR
2411							SET AFTER READING WRONG PARITY IN LOCATION
2412							WHOSE ADDRESS IS IN R5
2413	011022	000423		BR	78		
2414	011024	022713	000001	681 CMP	#1,(R3)		IS THIS A CORE PAR REG?
2415	011030	001020		BNE	78		NO, BRANCH(MOS PAR REG DOES NOT
2416							STORE ADDR BITS OF PAR ERROR)
2417	011032	017701	167732	MOV	@TREG,R1		GET PARITY REGISTER CONTENTS
2418	011036	042701	170037	BIC	#170037,R1		MASK ALL BUT ERROR ADDRESS BITS
2419	011042	010502		MOV	R5,R2		GET ADDRESS OF LOCATION UNDER TEST
2420	011044	042702	003777	MOV	#3777,R2		POSITION BITS IN R2
2421	011050	000302		8*AB	R2		

2422	011052	006302		ASL	R2		
2423	011054	006302		ASL	R2		
2424	011056	020102		CMP	R1,R2		PARITY ERROR ADDRESS BITS CORRECT?
2425	011060	001404		BEQ	78		BRANCH IF YES
2426	011062	013746	177776	MOV	0*PS,=(SP)		NO= SETUP TO DO ERROR CALL VIA A JSR
2427	011066	004767	002052	JSR	PC,ERR		ERROR= ADDRESS BITS (PARITY REGISTER
2428							BITS 5-11) INCORRECT- ADDRESS OF PARITY
2429							REGISTER IS CONTAINED IN LOCATION "TREG"
2430							ADDRESS OF TEST LOCATION IS IN R5
2431	011072	011515		781 MOV	@R5,@R5		RESTORE TEST LOCATION TO FIX BAD PARITY
2432	011074	005077	167670	CLR	@TREG		CLEAR ERROR BIT IN PARITY REGISTER
2433	011100	005715		TST	@R5		READ LOCATION TO SET IF PARITY IS GOOD
2434	011102	005777	167662	TST	@TREG		CHECK PARITY ERROR BIT
2435	011108	100004		BPL	.*+12		BRANCH IF NOT SET
2436	011110	013746	177776	MOV	0*PS,=(SP)		SETUP TO DO ERROR CALL VIA A JSR
2437	011114	004767	002024	JSR	PC,ERR		ERROR= WRITING LOCATION WITH WRITE
2438							WRONG PARITY CLEAR DIDN'T CLEAR BAD
2439							PARITY (ADDRESS OF LOCATION IS IN R5)
2440							"TREG" +20000 CONTAINS THE ADDRESS
2441							OF THE PARITY REGISTER
2442	011120	005167	167434	CUM	ODDFLG		TOGGLE BYTE INDICATOR
2443	011124	100401		8*1	.*+4		BRANCH IF HIGH BYTE NOT YET TESTED
2444	011126	005725		TST	(R5)+		UPDATE ADDRESS POINTER
2445	011130	020527	020000	CMP	R5,#20000		THIS 4K DONE?
2446	011134	103610		BLO	W*P21A		LOOP TILL ALL 4K HAS BEEN TESTED
2447	011136	004767	002222	JSR	PC,CLRPAR		CLEAR ALL PARITY REGISTERS
2448	011142	013746	177776	MOV	0*PS,=(SP)		SETUP TO CALL SCOPE VIA JSR
2449	011146	004767	004556	JSR	PC,SCOPEC		SCOPE
2450							
2451							ICOPY SECOND 4K BANK BACK TO FIRST 4K AND RETURN TO FIRST 4K BANK
2452	011152	012700	010000	XFR2: MOV	#10000,R0		R0 IS USED AS A COUNTER
2453	011156	005001		CLR	R1		R1 POINTS TO THE CURRENT LOCATION
2454	011160	016111	020000	18: MOV	20000(R1),@R1		ICOPY BANK 1 TO BANK 0
2455	011164	005721		TST	(R1)+		
2456	011166	005300		DEC	R0		
2457	011170	001373		BNE	18		
2458	011172	162706	020000	SUB	#20000,SP		RESTORE STACK POINTER
2459	011176	162737	020000	013214 SUB	#20000,@ERRA1		
2460	011204	162737	020000	013216 SUB	#20000,@ERRA2		
2461	011212	162737	020000	013226 SUB	#20000,@ERRA3		
2462	011220	162737	020000	013230 SUB	#20000,@ERRA4		
2463	011226	162737	020000	013240 SUB	#20000,@ERRA5		
2464	011234	000137	011240	JMP	@DONE		RETURN TO BANK 0
2465							
2466							
2467							
2468							
2469							
2470							
2471	011240	012737	000116	000114 DONE: MOV	#PARVEC+2,@PARVEC		RESTORE TRAPCATCHER
2472	011246	012706	000510	MOV	#STKPT,SP		REINITIALIZE STACK POINTER
2473	011252	004767	002106	JSR	#7,CLRPAR		CLEAR ALL PARITY REGISTERS
2474	011256	005267	167262	INC	PASCNT		KEEP TRACK OF PASSES COMPLETED
2475	011262	004567	003502	JSR	R5,DACNV		

2476	011266	000544				PASCNT			
2477	011270	016733				NPCNT			
2478	011272	000006				6			
2479	011274	104000				TYPE			
2480	011276	016715				MPGEND			;TYPE BELL, "END PASS#" AND PASS COUNT
2481	011300	013705	000042		LOGICAL:	MOV	R#42,R5		;LOADED BY MONITOR?
2482	011304	001405				BEQ	CONT		;BRANCH IF NO
2483	011306	000005				RESET			;SETUP FOR MONITOR EXIT
2484	011310	004715				JSR	7,(5)		
2485	011312	000240				NOP			
2486	011314	000240				NOP			
2487	011316	000240				NOP			
2488	011320	032737	000400	177570	CONT:	BIT	#BIT0,#SR		;SWITCH 8 SET?
2489	011326	001401				BEQ	,+4		
2490	011330	000000				HALT			;HALT AT END OF PASS SET
2491	011332	105767	167550			TSTB	STPFLG		
2492	011336	001006				BNE	18		;IF NO TERMINAL, SKIP
2493	011340	105777	167534			TSTB	STPS		;WAIT FOR TTY TO FINISH SO THAT RESET
2494	011344	100375				BPL	,-4		;DON'T CLOBBER THE BELL

2495	011346	112777	000000	167526		MOV#	#0,STPB		;OUTPUT A NULL
2496	011354	000167	170404		18:	JMP	BEGIN		
2497									
2498									
2499									
2500									
2501									
2502									
2503									
2504	011360	012737	011564	000004	MAPMEM:	MOV	#MAPMB,#4		;SET NO MEM MANAGEMENT TRAP
2505	011366	005737	177572			TST	#SR0		;IS KI PRESENT? (TIMEOUT IF NO)
2506									
2507									
2508	011372	005067	167154		MAPMA:	CLR	WORT		;INDICATE KI11 PRESENT
2509	011376	004767	001662			JSR	#7,NRALL		;INITIALLY SET ALL PAGES NONRESIDENT, BANK 0
2510	011402	004767	002026			JSR	#7,MAP1		;MAP KERNEL 0 TO BANK 0, RW
2511									;MAP KERNEL 7 TO THE EXTERNAL BANK, RW
2512									;MAP KERNEL 1 RW, AND TURN ON KI11
2513	011406	005067	167134			CLR	TBANK		
2514	011412	012767	177777	167446		MOV	#177777,MEHL		;SET UP CORE MAPS
2515	011420	012767	077777	167442		MOV	#777777,MEH		
2516	011426	012767	000001	167064		MOV	#1,BITPT		;SET UP 4K POINTER
2517	011434	012767	001066	167106		MOV	#MEHL,MEMUT		
2518	011442	012737	011552	000004		MOV	#58,#4		;SET UP FOR TIME OUTS
2519	011450	016777	167072	167564	28:	MOV	TBANK,#KPAR1		;MAP KERNEL PAGE 1 TO BANK BEING TESTED
2520	011456	005737	021000			TST	#21000		;1ST K PRESENT?
2521	011462	005737	025000			TST	#25000		;2ND K PRESENT?
2522	011466	005737	031000			TST	#31000		;3RD K PRESENT?
2523	011472	005737	035000			TST	#35000		;4TH K PRESENT?
2524	011476	062767	000200	167042	38:	ADD	#200,TBANK		;UPDATE TEST ADDRESS
2525	011504	006367	167010			ASL	BITPT		;UPDATE BANK POINTER
2526	011510	103008				BCC	48		;BRANCH IF NOT DONE WITH 64K SECTION
2527	011512	012767	000001	167000		MOV	#1,BITPT		;YES, DO MEMH(64-124K)
2528	011520	012767	001070	167022		MOV	#MEH,MEMUT		
2529	011526	022767	007600	167012	48:	CMP	#7600,TBANK		;EXTERNAL BANK YET?
2530	011534	003345				BGT	28		;NO, NOT YET
2531	011536	005037	177572			CLR	#SR0		;YES- DISABLE KI11
2532	011542	012737	000006	000004		MOV	#6,#4		;RESTORE TRAPCATCHER
2533	011550	000207				RTS	#7		;RETURN
2534	011552	046777	166742	166770	58:	BIC	BITPT,#MEMUT		;TIMEOUT OCCURRED-CLEAR BIT TO INDICATE
2535									;4K BLOCK NOT PRESENT
2536	011560	022626				CMP	(SP)+,(SP)+		;ADJUST STACK
2537	011562	000745				BR	38		;CHECK NEXT BLOCK
2538									
2539									
2540	011564	012767	000001	166760		MOV	#1,NRAT		;NO KI PRESENT - MAP MAX OF 28K IN 4K CONTIGUOUS BLOCKS
2541	011572	022626				CMP	(SP)+,(SP)+		;SET FLAG TO INDICATE KI11 NOT PRESENT
2542	011574	012737	011674	000004		MOV	#38,#4		;RESTORE STACK POINTER
2543	011602	012767	000177	167256		MOV	#177,MEHL		;SET UP TIMEOUT RETURN
2544	011610	005067	167254			CLR	MEMH		;INITIALIZE MAP
2545	011614	012767	000001	166676		MOV	#1,BITPT		;SETUP 4K POINTER
2546	011622	005001				CLR	R1		;INITIALIZE BANK ADDRESS
2547	011624	005761	001000		18:	TST	1000(1)		;1ST K PRESENT
2548	011630	005761	005000			TST	5000(1)		;2ND K PRESENT

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2549 011634 005761 011000          TST      11000(1)          ;3RD K PRESENT
2550 011640 005761 018000          TST      15000(1)          ;4TH K PRESENT
2551 011644 062701 020000          ADD      #20000,R1        ;UPDATE TEST ADDRESS
2552 011650 006367 166644          ASL      BITPT            ;UPDATE POINTER TO NEXT 4K
2553 011654 022767 000200 166636  CMP      #200,BITPT       ;28K CHECKED YET?
2554 011662 003360                    BGT      1#              ;NO, CHECK NEXT 4K BLOCK
2555 011664 012737 000006 000004    MOV      #6,##4
2556 011672 000207                    RTS      #7
2557 011674 046767 166620 167164 3#; BIC      BITPT,MEWL       ;TIMEOUT OCCURRED- CLEAR BIT TO
2558                                ;INDICATE 4K BLOCK NOT PRESENT
2559 011702 022626                    CMP      (SP)+,(SP)+      ;ADJUST STACK POINTER
2560 011704 000757                    BR       2#
2561
2562
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2566
2567 011706 013767 001066 166634  MAPREGI MOV    #MEML,MEMUT      ;LOAD MAP OF MEMORY PRESENT IN LOWER 64K
2568 011714 012767 000001 166576    MOV      #1,BITPT        ;INITIALIZE 4K POINTER
2569 011722 012767 000001 167266    MOV      #1,KTSTART      ;INDICATE KT11 NOT IN USE
2570 011730 005067 166632          CLR      RELOC
2571 011734 005067 166606          CLR      TBANK           ;INITIALIZE ADDRESS OF TEST BANK
2572 011740 005067 166610          CLR      HIWORD         ;CLEAR FLAG TO INDICATE FIRST 64K
2573                                ;BEING CHECKED
2574 011744 005067 167250          CLR      ADRTYP
2575
2576
2577
2578
2579 011750 012702 000570          ;SET WRITE WRONG PARITY IN ALL REGISTERS PRESENT
2580 011754 032712 000001          ;THEN WRITE TEST LOCATION VIA DATO AND READ TEST LOCATION VIA DATI
2581 011760 001003                    ;THEN CLEAR WRITE WRONG PARITY IN ALL REGISTERS
2582 011762 012772 000004 000000  MAPR:  MOV    #MPRO,R2      ;LOAD ADDRESS OF TABLE
2583 011770 062702 000010          1#; BIT    #1,(2)          ;IS THIS REGISTER PRESENT?
2584 011774 020227 000770          ;NO, GET NEXT ONE
2585 012000 103765                    ;YES, SET WRITE WRONG PARITY AND CLEAR REST
2586 012002 016703 166540          MOV      #MWP,#(2)
2587 012006 066703 167206          ADD      #10,R2
2588 012012 011313                    ;DONE WITH TABLE?
2589 012014 005713                    ;BRANCH IF NOT
2590 012016 012702 000570          MOV      TBANK,R3        ;LOAD ADDRESS OF 4K BANK UNDER TEST
2591 012022 032712 000001          ADD      ADRTYP,R3      ;ADD ADDRESS OFFSET (EITHER 0,2,4,OR 6)
2592 012026 001003                    ;WRITE WRONG PARITY
2593 012030 042772 000004 000000  TST      (3),(3)         ;READ WRONG PARITY
2594                                ;CLEAR WRITE WRONG PARITY IN ALL
2595 012036 062702 000010          ;PARITY REGISTERS
2596 012042 020227 000770          ADD      #10,R2
2597 012046 103765                    CMP      R2,#TREG
2598 012050 012702 000560          BLO      2#
2599 012054 062702 000010          MAPRC: MOV    #MPRO-10,R2 ;INIT FOR ERROR CHECKS
2600 012060 020227 000770          1#; ADD      #10,R2
2601 012064 002031                    CMP      R2,#TREG
2602 012066 032712 000001          BGE      MAPRD          ;BRANCH IF DONE WITH TABLE
2603                                ;IS THIS REGISTER PRESENT?

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2603 012072 001370                    BNE      1#              ;NO, GET NEXT ADDRESS
2604 012074 005772 000000          TST      #R(2)           ;YES, DID THIS CONTROLLER GET A
2605                                ;PARITY ERROR?
2606 012100 100365                    BPL      1#              ;NO, CHECK NEXT
2607 012102 005767 166446          TST      HIWORD         ;YES, WHICH 64K IS UNDER TEST?
2608 012106 001004                    BNE      2#              ;BRANCH IF UPPER 64K
2609 012110 056762 166404 000002  BIS      BITPT,2(2)      ;SET BIT IN MAP FOR THIS PARITY REGISTER
2610 012116 000403                    BR       3#
2611 012120 056762 166474 000004 2#; BIS      BITPT,4(2)      ;SET BIT IN MAP FOR THIS PARITY REGISTER
2612 012126 105762 000007          3#; TSTB     7(2)         ;IS THIS THE FIRST ADDRESS FOUND FOR
2613                                ;THIS PARITY REGISTER?
2614 012132 001005                    BNE      4#              ;NO, BRANCH
2615 012134 116762 167060 000006  MOV      ADRTYP,6(2)     ;YES, RECORD LOW BYTE OF ADDRESS (0,2,4,OR 6)
2616 012142 105262 000007          INCB     7(2)           ;INDICATE AN ADDRESS HAS BEEN FOUND FOR
2617                                ;THIS REGISTER
2618 012146 000742                    4#; BR       1#
2619 012150 011313                    MAPRD: MOV    #R3,R3      ;CLEAR BAD PARITY
2620 012152 062767 000002 167040  ADD      #2,ADRTYP      ;CHECK FIRST 4 ADDRESSES IN EACH 4K
2621 012160 026727 167034 000010  CMP      ADRTYP,#10
2622 012166 001402                    BEQ      1#              ;BRANCH IF FIRST 4 ADDRESSES TESTED
2623 012170 000167 177554                    ;IF NOT, GO TEST NEXT ONE
2624 012174 005767 166354          1#; MAPRB   HIWORD         ;IS LOWER MEMORY DONE?
2625 012200 001021                    MAPRE  MAPRE           ;YES, BRANCH
2626 012202 026727 166312 000100  CMP      BITPT,#100     ;DONE WITH 1ST 28K?
2627 012210 103015                    BHS     MAPRE           ;YES, BRANCH
2628 012212 062767 020000 166326  ADD      #20000,TBANK   ;NO- ADD 4K TO ADDRESS
2629 012220 006367 166274          ASL      BITPT          ;SHIFT BIT POINTER
2630 012224 005067 166770          CLR      ADRTYP        ;START WITH FIRST ADDRESS IN BANK
2631 012230 036767 166264 166312  BIT      BITPT,MEMUT    ;DOES THIS 4K BLOCK EXIST?
2632 012236 001756                    BEQ      1#              ;NO- BRANCH
2633 012240 000167 177504                    ;YES, TEST IT
2634 012244 005767 166302          MAPRE: TST    #OKT      ;KT11 PRESENT?
2635 012250 001401                    BEQ      #+4            ;YES, BRANCH
2636 012252 000207                    RTS      #7              ;NO, DONE
2637 012254 005767 166736          TST     #ISTART        ;KT11 ALREADY ON?
2638 012260 001417                    BEQ      1#              ;YES, BRANCH
2639 012262 012767 020000 166256  MOV      #20000,TBANK   ;NO, INIT TBANK TO SELECT KERNEL PAGE 1
2640 012270 012767 001400 166270  MOV      #1400,RELOC    ;SET UP FOR ACCESS TO 28K BANK
2641 012276 004767 000762          JSR     #7,RRALL       ;INITIALLY MAP ALL PAGES NR, BANK 0
2642 012302 004767 001126          JSR     #7,MAP1        ;MAP KERNEL 0 TO BANK 0, RW
2643                                ;MAP KERNEL 7 TO THE EXTERNAL BANK, RW
2644                                ;SET KERNEL 1 RW AND TURN ON KT11
2645 012306 005067 166704          CLR      KTSTART       ;INDICATE KT11 NOW IN USE
2646 012312 012737 000001 177572  MOV      #1,#SRO        ;TURN ON KT11
2647 012320 006367 166174          1#; ASL      BITPT        ;SHIFT BANK INDICATOR
2648 012324 103011                    BCC     2#              ;BRANCH IF FIRST 64K NOT DONE
2649 012326 012767 000001 166164  MOV      #1,BITPT      ;IF FIRST 64K DONE, SETUP FOR
2650 012334 013767 001070 166206  MOV      #MEMH, MEMUT   ;SECOND 64K
2651 012342 012767 000001 166204  MOV      #1,HIWORD      ;INDICATE NOW TESTING HIGH 64K
2652 012350 062767 000200 166210  ADD      #200,RELOC
2653 012356 022767 007600 166202  CMP      #7600,RELOC
2654 012364 003003                    BGT     3#              ;UP TO EXTERNAL BANK YET?
2655 012366 005037 177572          CLR     #SRO           ;NO, CONTINUE
2656 012372 000207                    RTS     #7              ;YES, TURN OFF KT11 AND EXIT

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2657 012374 036767 166120 166146 381 BIT BITPT, MEMUT ;IS THIS 4K PRESENT?
2658 012402 001746 BEQ 18 ;NO- BRANCH
2659 012404 016777 166156 166630 MOV RELOC, RKPARI ;YES, MAP PAGE 1 TO THIS BANK
2660 012412 005067 166602 CLR ADRTYP
2661 012416 000167 177326 JMP MAPRB ;GO TEST FOR PARITY MEMORY
2662
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2668
2669 012422 004767 000736 TMAP: JSR R7, CLRPAR ;CLEAR ALL PARITY REGISTERS PRESENT
2670 012426 104000 TYPE ;TYPE "THE PARITY REGISTERS CONTROL MEMORY
2671 012430 016440 MMAP ;AS FOLLOWS:"
2672 012432 012701 000560 MOV R0, R1 ;SET UP POINTER
2673 012436 062701 000010 TMAP: ADD R1, R1
2674 012442 020127 000770 CMP R1, #TREG ;DONE WITH MAP?
2675 012446 002136 BGE TMAPX ;YES, BRANCH
2676 012450 005067 166100 CLR HIWORD
2677 012454 005067 166042 CLR TRFLG ;INITIALIZE TRANSITION FLAG (USED TO
2678 ;FIGURE MEMORY LIMITS)
2679 012460 005067 166040 CLR TYFLG ;INITIALIZE TO INDICATE NOTHING TYPED FOR
2680 ;THIS REGISTER YET
2681 012464 012767 177774 166034 MOV R4, TYCOR
2682 012472 016167 000002 166016 MOV 2(1), ADRTPT ;GET LOW 64K MEMORY MAP WORD
2683 012500 012767 000001 166012 MOV R1, BITPT ;INITIALIZE 4K POINTER
2684 012506 032711 000001 BIT R1, (1) ;DOES THIS CONTROL EXIST?
2685 012512 001331 BNE TMAPA ;NO, GET ADDRESS OF NEXT ONE
2686 012514 011167 165774 MOV (1), TEMPX ;YES, PRINT ITS ADDRESS
2687 012520 004567 002244 JSR R5, OACNV
2688 012524 000514 TEMPX
2689 012526 016607 MPRAD
2690 012530 000006 6
2691 012532 104000 TYPE
2692 012534 017001 MX1
2693 012536 104000 TYPE
2694 012540 016607 MPRAD
2695 012542 062767 000004 165756 TMAPB: ADD R4, TYCOR ;KEEP TRACK OF # OF K OF CORE
2696 012550 036767 165744 165740 BIT BITPT, ADRTPT ;DOES THIS PARITY REGISTER CONTROL THIS 4K?
2697 012556 001424 BEQ TMAPC ;NO- BRANCH
2698 012560 005767 165736 TST TRFLG ;YES, DOES IT CONTROL PREVIOUS 4K?
2699 012564 001043 BNE TMAPD ;YES- DON'T TYPE IT
2700 012566 012767 000001 165726 MOV R1, TRFLG ;NO- SET FLAG INDICATING TRANSITION
2701 012574 004567 002276 JSR R5, BDCNV ;CONVERT K CORE TO ASCII
2702 012600 000526 TYCOR
2703 012602 016507 MTYCOR
2704 012604 000003 3
2705 012606 104000 TYPE ;TYPE "CONTROLS", AND ADDRESS OF CORE
2706 012610 017020 MX2
2707 012612 104000 TYPE
2708 012614 016507 MTYCOR
2709 012616 104000 TYPE
2710 012620 016514 NDASH
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2711 012622 005267 165676 INC TYFLG ;INDICATE TYPED
2712 012626 000422 BR TMAPD
2713 012630 005767 165666 TMAPC: TST TRFLG ;DID THIS PARITY REGISTER CONTROL PREVIOUS 4K?
2714 012634 001417 BEQ TMAPD ;NO, SKIP PRINTING
2715 012636 005067 165660 CLR TRFLG ;YES, TRANSITION OCCURRED- CLEAR FLAG
2716 012642 004567 002230 JSR R5, BDCNV ;CONVERT K CORE TO ASCII
2717 012646 000526 TYCOR
2718 012650 016507 MTYCOR
2719 012652 000003 3
2720 012654 104000 TYPE
2721 012656 016507 MTYCOR ;TYPE RIGHT AND RETURN
2722 012660 104000 TYPE
2723 012662 016522 MK
2724 012664 104000 TYPE
2725 012666 016517 MCR
2726 012670 005267 165630 INC TYFLG ;INDICATE TYPED
2727 012674 006367 165620 TMAPD: ASL BITPT ;UPDATE BIT POINTER TO NEXT 4K
2728 012700 103320 BCC TMAPB ;TEST NEXT 4K IF NOT DONE WITH 1ST 64K
2729 012702 005767 165646 TST HIWORD ;64-124K DONE?
2730 012706 001405 BEQ 18 ;NO, BRANCH
2731 012710 005767 165610 TST TYFLG ;YES, WAS ANY PARITY MEMORY
2732 ;FOUND FOR THIS REGISTER?
2733
2734
2735 012714 001260 BNE TMAPA ;NO PARITY MEMORY WAS FOUND FOR THIS
2736 012716 104002 ENPROR ;REGISTER- EITHER WRITE WRONG PARITY
2737 ;FAILED, PARITY ERROR GENERATE OR
2738 ;DETECT FAILED, OR THE PARITY ERROR
2739 ;BIT FAILED TO SET
2740 012720 000646 BR TMAPA
2741 012722 016167 000004 165566 181 MOV 4(1), ADRTPT ;UPDATE TO MAP WORD FOR THE UPPER 64K
2742 012730 012767 000001 165562 MOV R1, BITPT ;RESET BIT POINTER
2743 012736 005267 165612 INC HIWORD ;INDICATE LOW 64K DONE
2744 012742 000677 BR TMAPB ;LOOP
2745 012744 000207 TMAPX: RTS R7 ;RETURN WHEN DONE
2746
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2755 012746 012767 016063 000266 ERRST: MOV R0, ERRB ;SETUP TO TYPE MPR ADDRESS AND CONTENTS
2756 012754 012767 177777 000262 MOV R1, ERBX ;NO- LOCATION AFTER MESSAGE
2757 012762 012767 000240 000296 MOV R2, ERBX+2 ;SETUP DATA
2758 012770 017767 165774 165542 MOV R0, TRDATA ;CONVERT TO ASCII
2759 012776 004567 001766 JSR R5, OACNV
2760 013002 000770 IREG
2761 013004 016072 HTREG
2762 013006 000006 6
2763 013010 004567 001754 JSR R5, OACNV ;CONVERT TO ASCII
2764 013014 000540 TRDATA
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2873 013422 020102          CMP    R1,R2
2874 013424 103767          BLO   18
2875 013426 012602          MOV   (SP)+,R2
2876 013430 012601          MOV   (SP)+,R1
2877 013432 000207          RTS   47
2878
2879
2880
2881          ;ROUTINE TO MAP KERNEL 0 TO BANK 0 READ/WRITE.
2882          ;KERNEL 1 READ/WRITE BUT BANK MAPPED BY CALLING ROUTINE,
2883          ;AND KERNEL 7 TO EXTERNAL BANK, READ/WRITE
2884 013434 012777 077406 165566 MAP1:  MOV   #77406,#KPDRO
2885 013442 012777 077406 165562          MOV   #77406,#KPDRI
2886 013450 012777 077406 165560          MOV   #77406,#KPDRI
2887 013456 012777 007600 165562          MOV   #7600,#KPAR7
2888 013464 005077 165550          CLR   #KPAR0
2889 013470 012737 000001 177572          MOV   #1,#SRO
2890 013476 000207          RTS   47
2891
2892
2893
2894          ;ROUTINE TO LOCATE THE FIRST PARITY MEMORY ADDRESS (ABOVE BANK 0)
2895          ;CORRESPONDING TO A GIVEN PARITY REGISTER-REQUIRES THAT THE ROUTINES
2896          ;MAPMEM AND MAPREG HAVE ALREADY BEEN RUN
2897          ;TO USE, PUT THE ADDRESS OF THE ADDRESS OF THE REGISTER IN R0 (I.E. POINT TO
2898          ;TO MAP TABLE)-THE DESIRED ADDRESS IS RETURNED IN R1, USING KERNEL PAGE 1 IF
2899          ;KT11 IS PRESENT
2900 013500 010246          LOCATM: MOV   R2,=(SP)
2901 013502 012702 000200          MOV   #200,R2
2902 013506 012701 000002          MOV   #2,R1
2903 013512 005767 165034          18:  TST   NOKT          ;SKIP USE OF BANK 0
2904 013516 001403          BEQ   38
2905 013520 022701 000200          CMP   #200,R1          ;KT11 PRESENT?
2906 013524 101420          BLOS  48
2907
2908          ;YES, BRANCH
2909          ;NO, CHECK ONLY FOR MEMORY IN FIRST 28K
2910          ;IF NO MEMORY FOUND IN 1ST 28K, GIVE
2911          ;ERROR RETURN
2912          ;DOES THIS 4K CORRESPOND TO THIS REGISTER?
2913          ;YES, BRANCH
2914          ;NO, CHECK TO SEE IF NEXT 4K CORRESPONDS
2915 013526 030160 000002          38:  BIT   R1,2(R0)
2916 013532 001021          BNE  LOCAT1
2917 013534 062702 000200          ADD   #200,R2
2918 013540 006301          ASL   R1
2919 013542 103363          BCC   18
2920 013544 012701 000001          MOV   #1,R1
2921 013550 030160 000004          28:  BIT   R1,4(R0)          ;CHECK HIGH 64K
2922 013554 001010          BNE  LOCAT1
2923 013556 062702 000200          ADD   #200,R2
2924 013562 006301          ASL   R1
2925 013564 103371          BCC   28
2926 013566 012701 000001          48:  MOV   #1,R1
2927 013572 012602          MOV   (SP)+,R2
2928 013574 000207          RTS   47
2929 013576 005767 164750          LOCAT1: TST   NOKT          ;NO PARITY MEMORY CORRESPONDS TO
2930 013602 001005          BNE   18
2931 013604 010277 165432          MOV   R2,#KPAR1          ;THIS REGISTER- RETURN WITH EMROR
2932 013610 012701 020000          MOV   #20000,R1          ;INDICATION
2933 013614 000407          BR    28
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2927 013616 010201          18:  MOV   R2,R1          ;SETUP R1 TO REFERENCE 4K BANK
2928 013620 006301          ASL   R1          ;WITHOUT KT11
2929 013622 006301          ASL   R1
2930 013624 006301          ASL   R1
2931 013626 006301          ASL   R1
2932 013630 006301          ASL   R1
2933 013632 006301          ASL   R1
2934 013634 118067 000006 000010 28:  MOVBS 6(R0),LSAV
2935 013642 066701 000004          ADD   LSAV,R1
2936 013646 012602          MOV   (SP)+,R2          ;RESTORE R2
2937 013650 000207          RTS   47          ;AND RETURN
2938 013652 000000          LSAV:  0
2939
2940
2941
2942          ;SAVE LOADER IN TOP OF FIRST 4K
2943 013654 013746 000004          SAVLDR: MOV  ##4,=(SP)          ;SAVE CONTENTS OF TIMEOUT VECTOR
2944 013660 013746 000006          MOV   #6,=(SP)
2945 013664 012737 000006 000004          MOV   #6,#4
2946 013672 012737 000002 000006          MOV   #RTI,#6          ;SETUP TO RTI ON TIMEOUT
2947 013700 010146          MOV   R1,=(SP)          ;SAVE REGISTERS
2948 013702 010246          MOV   R2,=(SP)
2949 013704 012701 157500          MOV   #157500,R1
2950 013710 000261          18:  SEC
2951 013712 005711          TST   #R1
2952 013714 103006          BCC   28
2953 013716 162701 020000          SUB   #20000,R1
2954 013722 020127 020000          CMP   R1,#20000
2955 013726 101370          BHI   18
2956 013730 000410          BR    SAVLDX
2957 013732 012702 017500          28:  MOV   #17500,R2
2958 013736 012122          38:  MOV   (R1)+(R2)+
2959 013740 020227 020000          CMP   R2,#20000
2960 013744 103774          BLO   38
2961 013746 005267 000016          INC   LDRSVD          ;INDICATE LOADER HAS BEEN MOVED TO
2962
2963          ;THE TOP OF THE FIRST 4K
2964 013752 012602          SAVLDX: MOV  (SP)+,R2
2965 013754 012601          MOV   (SP)+,R1
2966 013756 012637 000006          MOV   (SP)+,#6
2967 013762 012637 000004          MOV   (SP)+,#4
2968 013766 000207          RTS   47
2969 013770 000000          LDRSVD: 0
2970
2971
2972          ;ROUTINE TO RESTORE THE LOADER FROM BANK 0 (WHERE IT WAS SAVED) TO THE
2973          ;HIGHEST BANK IN THE FIRST 28K OF MEMORY
2974 013772 005767 177772          RSTLDR: TST   LDRSVD
2975 013776 001431          BEQ   RSTLDX
2976 014000 012737 000006 000004          MOV   #6,#4
2977 014006 012737 000002 000006          MOV   #RTI,#6
2978 014014 012701 157500          MOV   #157500,R1
2979 014020 000261          18:  SEC
2980 014022 005711          TST   #R1          ;IF TIMEOUT, C BIT WILL BE SET

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2981 014024 103006          BCC      28          ;IF NO TIMEOUT, C BIT WILL BE CLEAR
2982 014026 162701 020000    SUB      #20000,R1 ;TIMEOUT OCCURRED, CHECK FOR NEXT
2983 014032 020127 020000    CMP      R1,#20000 ;LOWER BANK
2984 014036 101370          BHI      18
2985 014040 000410          BR       RSTLDX
2986 014042 012702 017500    MOV      #17500,R2
2987 014046 012221 38:    MOV      (R2)+,(R1)+
2988 014050 020227 020000    CMP      R2,#20000
2989 014054 103774          BLO     38
2990 014056 104000          TYPE    ;TYPE MESSAGE "LOADER RESTORED"
2991 014060 017032          LDRMSG
2992 014062 000000          RSTLDX: HALT      ;LOADER HAS BEEN RESTORED
2993 014064 000776          BR      ,-2       ;TO HIGHEST BANK IN FIRST 28K
2994
2995
2996
2997
2998          ;SCAN ALL MEMORY FOR BAD PARITY, TYPE 18 BIT ADDRESSES OF
                ;LOCATIONS FOUND TO BE BAD, AND WRITE INTO LOCATIONS WITH GOOD PARITY
2999 014066 010146          PSCAN: MOV      R1,=(SP) ;STORE REGISTERS AND LOCATIONS TO BE
3000 014070 010246          MOV      R2,=(SP) ;ALTERED
3001 014072 010346          MOV      R3,=(SP)
3002 014074 010446          MOV      R4,=(SP)
3003 014076 013746 000004    MOV      @#4,=(SP)
3004 014102 013746 000006    MOV      @#6,=(SP)
3005 014106 013746 000114    MOV      @#114,=(SP)
3006 014112 013746 000116    MOV      @#116,=(SP)
3007 014116 012737 000006    MOV      #6,@#4 ;SETUP TIMEOUT TRAPCATCHER
3008 014124 005037 000006    CLR     #6
3009 014130 012737 000116    MOV      #116,@#114 ;SETUP PAKITY TRAP TRAPCATCHER
3010 014136 005037 000116    CLR     #116
3011 014142 005767 164404    TST     NOKT ;KTI1 PRESENT?
3012 014146 001513          BEQ     PSCAN1 ;YES, BRANCH
3013 014150 005002          CLR     R2 ;R2 CONTAINS TEST ADDRESS
3014 014152 012703 000001    MOV      #1,R3 ;R3 USED AS A BIT POINTER
3015 014156 004767 177202    JSR     #7,CLRRPAR ;CLEAR ALL PARITY REGISTERS
3016 014162 005712          TST     #R2 ;READ LOCATION TO CHECK FOR BAD PARITY
3017 014164 000240          NOP
3018 014166 012701 000570    MOV      #MPRO,R1 ;SETUP TO SCAN REGISTERS FOR PARITY
3019 ;ERROR SET
3020 014172 032711 000001    38:    BIT      #1,#R1
3021 014176 001003          BNE     ,+10
3022 014200 005771 000000    TST     @ (R1) ;PARITY ERROR SET?
3023 014204 100424          BHI     66 ;YES- BRANCH
3024 014206 062701 000010    ADD     #10,R1 ;NO- CHECK NEXT REGISTER
3025 014212 020127 000770    CMP     R1,#TREG
3026 014216 103765          BLO     36 ;LOOP UNTIL ALL REGISTERS HAVE BEEN CHECKED
3027 014220 062702 000002    ADD     #2,#R2 ;MOVE ADDRESS POINTER
3028 014224 032702 017777    BIT     #17777,R2 ;DONE WITH 4K?
3029 014230 001352          BNE     16 ;NO, CONTINUE
3030 014232 006303          ASL     R3 ;YES, CHECK FOR TESTING NEXT 4K
3031 014234 020327 000200    CMP     R3,#200
3032 014240 103035          BHS    PSCANX ;EXIT IF DONE WITH 28K
3033 014242 030367 164620    BIT     R3,MEML ;IS THIS MEMORY PRESENT?
3034 014246 001343          BNE     16 ;YES, GO TEST IT

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3035 014250 062702 020000    ADD     #20000,R2 ;NO, UPDATE ADDRESS
3036 014254 000766          BR      58 ;LOOP
3037 014256 010267 000110    68:    MOV      R2,PSADRS ;PARITY ERROR OCCURRED
3038 014262 004567 000502    JSR     R5,OACNV ;GET ASCII OF ADDRESS CONTAINING BAD PARITY
3039 014266 014372          PSADRS
3040 014270 016772          MPSEI  6
3041 014272 000006          6
3042 014274 104000          TYPE    ;TYPE MESSAGE "BAD PARITY FOUND IN LOCATION"
3043 014276 016742          MPSEI  ;AND ADDRESS OF FAILING LOCATION
3044 014300 032737 002000 177570    BIT     #2000,@#SR ;SWITCH 10 SET?
3045 014306 001401          BEQ     ,+4 ;NO- CONTINUE
3046 014310 000000          HALT   ;HALT ON BAD PARITY SET
3047 014312 011212          MOV     #R2,#R2 ;WRITE INTO LOCATION- SHOULD
3048 ;CLEAR BAD PARITY
3049 014314 005071 000000    CLR     @ (R1) ;CLEAR CORRESPONDING PARITY REGISTER
3050 014320 005712          TST     #R2 ;READ LOCATION TO SEE IF BAD PARITY WAS
3051 014322 005771 000000    TST     @ (R1) ;CLEARED
3052 014326 100001          BPL     ,+4 ;OK- BRANCH
3053 014330 104002          ERROR ;BAD PARITY DIDN'T CLEAR WHEN LOCATION
3054 ;WAS REWRITTEN
3055 014332 000732          BR      48 ;GO CHECK NEXT LOCATION
3056 014334 004767 177024    PSCANX: JSR     PC,CLRRPAR ;DONE- CLEAR ALL PARITY REGISTERS
3057 014340 012637 000116    MOV     (SP)+,@#116 ;RESTORE LOCATIONS ALTERED
3058 014344 012637 000114    MOV     (SP)+,@#114
3059 014350 012637 000006    MOV     (SP)+,@#6
3060 014354 012637 000004    MOV     (SP)+,@#4
3061 014360 012604          MOV     (SP)+,R4
3062 014362 012603          MOV     (SP)+,R3
3063 014364 012602          MOV     (SP)+,R2
3064 014366 012601          MOV     (SP)+,R1
3065 014370 000207          RTS     #7 ;RETURN
3066 014372 000000          PSADRS: 0
3067 014374 000000          PSCANH: 0
3068
3069
3070
3071
3072          ;SCAN ALL MEMORY FOR BAD PARITY USING KTI1
                ;TYPE 18 BIT ADDRESSES OF LOCATIONS FOUND BAD, AND WRITE GOOD PARITY BACK IN
3073 014376 017746 164640          PSCAN: MOV      @KPA1,=(SP) ;SAVE CONTENTS OF KERNEL PARI
3074 014402 032737 000001 177572    BIT     #1,@#SR0 ;SKIP IF KTI1 IS ALREADY ON
3075 014410 001004          BNE     18
3076 014412 004767 176646    JSR     PC,NRALL ;MAP KERNEL 0 TO BANK 0,RW
3077 014416 004767 177012    JSR     PC,MAP1 ;MAP KERNEL 7 TO THE EXTERNAL BANK, RW
3078 ;MAP KERNEL 1 RW, AND TURN ON KTI1
3079 014422 005067 177746    18:    CLR     PSCANH ;CLEAR FLAG TO INDICATE CHECKING FIRST 64K
3080 014426 005077 164610    CLR     @KPA1 ;INITIALIZE TO BANK 0
3081 014432 012703 000001    PSLOOP: MOV     #1,R3 ;R3 IS USED AS A BIT POINTER
3082 014436 005767 177732    PSLOOP: TST     PSCANH ;TESTING TOP 64K?
3083 014442 001004          BNE     28 ;YES, BRANCH
3084 014444 030367 164416    BIT     R3,MEML ;NO, IS PARITY MEMORY PRESENT IN THIS 4K?
3085 014450 001022          BNE     PSXTST ;YES- GO TEST IT
3086 014452 000403          BR      ;NO- CHECK FOR NEXT 4K
3087 014454 030367 164410    28:    BIT     R3,MEMH ;IS PARITY MEMORY PRESENT IN THIS 4K?
3088 014460 001016          BNE     PSXTST ;YES- GO TEST IT

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3089 014462 062777 000200 164552 PSNXT: ADD #200,0KPAR1 ;NO= MAP TO NEXT 4K
3090 014470 006303 A&L R3
3091 014472 103361 BCC PSLUP ;BRANCH IF NOT END OF 64K
3092 014474 005767 177674 T&T PSCANH ;END OF TOP 64K?
3093 014500 001003 BNE PS&CX1 ;YES, GET READY TO EXIT
3094 014502 005267 177666 INC PSCANH ;NO, SET FLAG INDICATING DONE WITH
3095 ;LOWER 64K
3096 014506 000751 BR PSLOOP
3097 014510 012677 164526 PS&CX1: MOV (SP)+,0KPAR1
3098 014514 000707 BR PSCANX
3099 014516 012702 020000 PS&XT&T: MOV #20000,R2 ;R2 USED AS ADDRESS POINTER
3100 014522 004767 176636 1&1: JSR #7,CL&RPAR ;CLEAR ALL PARITY REGISTERS
3101 014526 005712 T&T #R2 ;READ LOCATION
3102 014530 012701 000570 MOV #MPRO,R1 ;SETUP TO SCAN REGISTERS FOR PARITY ERROR SET
3103 014534 032711 000001 2&1: BIT #1,0R1
3104 014540 001003 BNE .+10
3105 014542 005771 000000 T&T 0(R1) ;PARITY ERROR SET?
3106 014546 100413 B&M 4& ;YES, BRANCH
3107 014550 062701 000010 ADD #10,R1 ;NO, CHECK NL&T
3108 014554 020127 000770 C&M R1,#TREG
3109 014560 103765 BLO 2& ;LOOP UNTIL ALL REGISTERS HAVE BEEN CHECKED
3110 014562 062702 000002 3&1: ADD #2,R2 ;UPDATE TEST ADDRESS POINTER
3111 014566 020227 040000 C&M R2,#40000 ;DONE WITH BANK?
3112 014572 103753 BLO 1& ;NO= LOOP
3113 014574 000732 BR PSNXT ;YES= GO CHECK FOR ANOTHER BANK
3114 014576 010267 177570 4&1: MOV R2,PS&ADRS ;PARITY ERROR OCCURRED= GET 19 BIT
3115 014602 042767 160000 177562 BIC #160000,PS&ADRS ;OCTAL ADDRESS OF BAD LOCATION
3116 014610 005046 CLR -(SP)
3117 014612 017746 164424 MOV 0KPAR1,-(SP)
3118 014616 006316 ASL 0&SP
3119 014620 006316 ASL 0&SP
3120 014622 006316 ASL 0&SP
3121 014624 006316 ASL 0&SP
3122 014626 006316 ASL 0&SP
3123 014630 006166 000002 ROL 2(SP)
3124 014634 006316 ASL 0&SP
3125 014636 006166 000002 ROL 2(SP)
3126 014642 006366 000002 ASL 2(SP)
3127 014646 062667 177520 ADD (SP)+,PS&ADRS
3128 014652 004567 000112 JSR R5,0ACNV ;CONVERT LOW 16 OCTAL BITS TO ASCII
3129 014656 014372 PS&ADRS
3130 014660 016772 MP&SER1
3131 014662 000006 6
3132 014664 116704 002102 MOV&B MP&SER1,R4
3133 014670 062604 002074 ADD (SP)+,R4 ;CHANGE TO ASCII FOR 19 BITS
3134 014672 110467 002074 MOV&B R4,MP&SER1
3135 014676 104000 TYPE ;TYPE ADDRESS OF LOCATION WITH BAD PARITY
3136 014700 016742 MP&SER
3137 014702 032737 002000 177570 BIT #2000,#&SR ;SWITCH 10 SET?
3138 014710 001401 BEQ .+4 ;NO= BRANCH
3139 014712 000000 HALT ;HALT ON BAD PARITY SET
3140 014714 011212 MOV #0R2,0R2 ;REWRITE LOCATION CONTAINING BAD PARITY
3141 014716 005071 000000 CLR 0(R1) ;CLEAR PARITY ERROR BIT
3142 014722 005712 T&T 0R2 ;READ LOCATION TO SEE IF PARITY IS NOW GOOD

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3143 014724 005771 000000 T&T 0(R1) ;CHECK PARITY ERROR BIT
3144 014730 100001 BPL .+4
3145 014732 104002 ERROR ;REWRITING LOCATION DID NOT CLEAR BAD PARITY
3146 014734 000712 BR 3& ;GO TEST NEXT LOCATION
3147
3148
3149
3150
3151 ;PIC ROUTINE TO OUTPUT A SERIES OF ASCII MESSAGES (CALLED VIA JSR R5)
3152 014736 012567 000022 TYP&SX: MOV (R5)+,TYP&SBX ;GET ADDRESS OF MESSAGE
3153 014742 022767 177777 000014 C&M #1,TYP&SBX ;TERMINATOR?
3154 014750 001001 BNE TYP&SAX ;NO, BRANCH
3155 014752 000205 RTS #5 ;YES, RETURN
3156 014754 013746 177776 TYP&SAX: MOV #*PS,-(SP) ;SETUP TO CALL TYPE ROUTINE VIA JSR
3157 014760 004767 164124 JSR PC,#TYPE ;TYPE ASCII MESSAGE
3158 014764 000000 TYP&SBX: OPEN
3159 014766 000763 BR TYP&SX
3160
3161
3162
3163 ;SUBROUTINE FOR OCTAL TO ASCII CONVERSION
3164 014770 013567 000074 0ACNV: MOV 0(S)+,0ACNVX ;GET OCTAL VALUE
3165 014774 012567 000072 MOV (S)+,0ACDST ;GET DESTINATION ADDRESS
3166 015000 012567 000070 MOV (S)+,0ACNT ;GET CONVERT COUNT
3167 015004 066767 000064 ADD 0ACNT,0ACDST ;DEVELOP ADDRESS TO STORE 1ST CHAR.
3168 015012 016746 000052 0ACNV&1: MOV 0ACNVX,-(SP)
3169 015016 042716 177770 BIC #177770,&SP ;ISOLATE LEAST SIGNIFICANT DIGIT
3170 015022 062716 000060 ADD #6,&SP ;CONVERT DIGIT TO ASCII
3171 015026 005367 000040 DEC 0ACDST
3172 015032 112677 000034 MOV&B (SP)+,0ACDST ;STORE ASCII CHARACTER
3173 015036 042767 000007 000024 BIC #7,0ACNVX
3174 015044 006067 000020 ROR 0ACNVX
3175 015050 006067 000014 ROR 0ACNVX
3176 015054 006067 000010 ROR 0ACNVX
3177 015060 005367 000010 DEC 0ACNT ;DONE ALL DIGITS?
3178 015064 001352 BNE 0ACNV&A ;BRANCH IF NOT DONE
3179 015066 000205 RTS ;DONE, EXIT
3180 015070 000000 0ACNVX: OPEN
3181 015072 000000 0ACDST: 0
3182 015074 000000 0ACNT: 0
3183
3184
3185
3186 ;SUBROUTINE FOR BINARY TO DECIMAL ASCII CONVERSION
3187 015076 104005 BDCNV: SAV04 ;SAVE REGS
3188 015100 012700 015254 MOV #DECVAL,#0 ;SET UP ADDR TO STORE DECIMAL ASCII
3189 015104 013501 MOV 0(S)+,R1 ;BINARY VALUE TO R1
3190 015106 012567 000052 MOV (S)+,BDCNV&C ;DESTINATION ADDR TO BDCNV&C
3191 015112 012567 000050 MOV (S)+,BDCNV&D ;CHARACTER COUNT TO BDCNV&D
3192 015116 012702 015242 MOV #ADTENP,R2 ;ADDR OF TEN POWER STRING
3193 015122 012767 000005 000104 MOV #5,CNVCTR ;SET UP FOR 5 POWER CONVERSIONS
3194 015130 012267 000104 BDCNV&1: MOV (2)+,TENP&R ;MOVE POWER OF TEN VALUE
3195 015134 004767 000034 JSR PC,SUBTEN ;PERFORM CONVERSION
3196 015140 005367 000070 DEC CNVCTR ;DONE 5 CONVERSIONS?

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3197 015144 001371 BNE BDCNVA ;BRANCH IF NOT YET 5.  
3198 015146 166700 000014 SUB BDCNVD,%0  
3199 015152 010067 000004 MOV %0,BDCNVB  
3200 015156 004567 000100 JSR R5,BMOVE  
3201 015162 000000 BDCNVB: OPEN  
3202 015164 000000 BDCNVC: OPEN  
3203 015166 000000 BDCNVD: OPEN  
3204 015170 104006 RST04 ;RESTORE REGS AND EXIT  
3205 015172 000205 RTS R5  
3206 015174 005067 000036 SUBTEN: CLR DIGIT  
3207 015200 166701 000034 SUBTNA: SUB TENPWR,R1 ;SUBTRACT TEN POWER FROM BINARY VALUE  
3208 015204 103403 BCS SUBTNB ;BRANCH IF UNSUCCESSFUL SUBTRACTION  
3209 015206 005267 000024 INC DIGIT  
3210 015212 000772 BR SUBTNA  
3211 015214 066701 000020 SUBTNB: ADD TENPWR,R1 ;RESTORE SUBTRACTED VALUE.  
3212 015220 062767 000060 000010 ADD #60,DIGIT ;CONVERT (DIGIT) TO ASCII  
3213 015226 116720 000004 MOVB DIGIT,(0)+ ;MOVE ASCII CHAR TO DECVAL FIELD  
3214 015232 000207 RTS PC ;EXIT  
3215 015234 000000 CNVCTR: OPEN  
3216 015236 000000 DIGIT: OPEN  
3217 015240 000000 TENPWR: OPEN  
3218 015242 023420 ADTENP: 10000.  
3219 015244 001750 1000.  
3220 015246 000144 100.  
3221 015250 000012 10.  
3222 015252 000001 1.  
3223 015254 040 040 040 DECVAL: .BYTE 040,040,040,040,040,040  
3224 015257 040 040 040  
3225  
3226  
3227  
3228 ;SUBROUTINE TO MOVE A VARIABLE NUMBER OF BYTES  
3229 015262 104005 BMOVE: SAVO4 ;SAVE REGS  
3230 015264 012501 MOV (5)+,R1 ;GET FROM ADDRESS  
3231 015266 012502 MOV (5)+,R2 ;GET TO ADDRESS  
3232 015270 012503 MOV (5)+,R3 ;GET COUNT  
3233 015272 112122 BMOVA: MOV8 (1)+,(2)+ ;MOVE BYTE  
3234 015274 005303 DEC R3 ;DECREMENT COUNT  
3235 015276 001375 BNE BMOVA ;BRANCH IF NOT DONE  
3236 015300 104006 RST04 ;RESTORE REGS AND EXIT  
3237 015302 000205 RTS R5  
3238  
3239  
3240  
3241 ;UNEXPECTED POWER FAIL SERVICE  
3242 ;BECAUSE WMP MAY BE SET IN NPR18 AND ALL PROCESSOR REGISTERS  
3243 ;MAY BE IN USE, CONTINUATION AFTER POWER FAIL IS NOT ATTEMPTED.  
3244 ;INSTEAD, THE PROGRAM RESTARTS AFTER A POWER FAILURE  
3245 015304 012737 015350 000024 PWRDN: MOV #PWRUP,#24 ;SET UP FOR POWER UP  
3246 015312 012701 000570 MOV #NPRO,R1  
3247 015316 032711 000001 BIT #1,R1  
3248 015322 001002 BNE #+6  
3249 015324 005071 CLR #R1 ;CLEAR PARIY REGISTERS IN CASE  
3250 015330 062701 000010 ADD #10,R1 ;WMP IS SET
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3251 015334 020127 000770 CMP R1,#TREG  
3252 015340 103766 BLO 18  
3253 015342 010667 163702 MOV SP,SPSAV  
3254 015346 000000 HALT ;POWER DOWN HALT  
3255 015350 012737 015304 000024 PWRUP: MOV #PWRDN,#24 ;SET UP FOR POWER DOWN  
3256 015356 016706 163666 MOV SPSAV,#SP  
3257 015362 005027 000000 CLR #0 ;STALL SO OUTPUT WON'T BE GARBLED  
3258 015366 005367 177772 DEC #-2  
3259 015372 001375 BNE #-4  
3260 015374 104000 TYPE ;TYPE RECOVERY MESSAGE  
3261 015376 016676 #PWRP  
3262 015400 000167 163662 JMP RSTART ;RESTART  
3263  
3264  
3265  
3266 ;EMT HANDLER  
3267 015404 011646 EMTINT: MOV (SP),-(SP) ;GET SAVED PC  
3268 015406 162716 000002 SUB #2,(SP) ;DECREMENT PC BY 2  
3269 015412 017616 000000 MOV #0,(SP),(SP) ;GET CALL  
3270 015416 121667 000050 CMPB (SP),EMTLIM ;CHECK IF CALL WITHIN LIMITS  
3271 015422 101402 BLOS EMTA ;CALL IS NOT WITHIN LIMITS  
3272 015424 000000 HALT  
3273 015426 000776 BR #-2  
3274 015430 006116 EMTA: ROL (SP) ;EMT ARG X 2  
3275 015432 042716 177001 RIC #177001,(SP) ;REMOVE 7 MSB  
3276 015436 062716 015450 ADD #EMTAB,(SP) ;FORM EMT RTN ADDRESS  
3277 015442 017616 000000 MOV #0,(SP),(SP)  
3278 015446 000136 JMP #(SP)+ ;GO TO EMT RETURN  
3279  
3280  
3281 ;EMT DEFINITIONS AND ASSIGNMENTS  
3282 015450 EMTTAB:  
3283 104000 TYPE=EMT+EMTX  
3284 015450 001110 #TYPE  
3285 104001 SCOPE=EMT+EMTX  
3286 015452 015730 SCOPEC  
3287 104002 ERRUR=EMT+EMTX  
3288 015454 013144 EKR  
3289 104003 ERRJRP=EMT+EMTX  
3290 015456 013024 ERFP  
3291 104004 ERRORS=EMT+EMTX  
3292 015460 012746 ERRST  
3293 104005 SAVO4=EMT+EMTX  
3294 015462 015474 SVO4  
3295 104006 RST04=EMT+EMTX  
3296 015464 015562 RS04  
3297 104007 RST05=EMT+EMTX  
3298 015466 013610 RS05  
3299 104010 SAVO5=EMT+EMTX  
3300 015470 015514 SVO5  
3301 015472 000010 EMTLIM: EMTX=1  
3302  
3303  
3304 ;SUBROUTINE TO SAVE REGS 0-4
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3305 015474 012666 177764      SV04:  MOV      (SP)+,-12,(SP)      ;MOVE PC+PS UP STACK
3306 015500 012666 177764      MOV      (SP)+,-12,(SP)
3307 015504 012767 000002 000040  MOV      *RTI,SV05C
3308 015512 000411      BR      SV05B
3309
3310
3311
3312
3313 015514 012767 000240 000030 ;SUBROUTINE TO SAVE REGS 0-5 + PLACE EMT PC IN R5
3314 015522 000400      SV05B: MOV      *NOP,SV05C
3315      BR      SV05A
3316
3317 015524 012666 177762      SV05A: MOV      (SP)+,-14,(SP)
3318 015530 012666 177762      MOV      (SP)+,-14,(SP)
3319 015534 010546      MOV      R5,-(SP)
3320 015536 010446      SV05B: MOV      R4,-(SP)
3321 015540 010346      MOV      R3,-(SP)
3322 015542 010246      MOV      R2,-(SP)
3323 015544 010146      MOV      R1,-(SP)
3324 015546 010046      MOV      %0,-(SP)
3325 015550 024646      CMP      =(SP),=(SP)
3326 015552 000002      SV05C: RTI      ;RTI OR NOP
3327 015554 016605 000020      MOV      16,(SP),R5      ;EMT PC TO R5
3328 015560 000002      RTI
3329
3330
3331
3332
3333 015562 022626      ;SUBROUTINE TO RESTORE REGS 0-4
3334 015564 012600      R504:  CMP      (SP)+,(SP)+
3335 015566 012601      MOV      (SP)+,%0
3336 015570 012602      MOV      (SP)+,R1
3337 015572 012603      MOV      (SP)+,R2
3338 015574 012604      MOV      (SP)+,R3
3339 015576 016646 177764      MOV      (SP)+,R4
3340 015602 016646 177764      MOV      -12,(SP),-(SP)      ;MOVE PC+PS DOWN STACK
3341 015606 000002      MOV      -12,(SP),-(SP)
3342      RTI
3343
3344
3345
3346 015610 010566 000020      ;SUBROUTINE TO RESTORE REGS 0-5
3347 015614 022626      R505B: MOV      R5,16,(SP)      ;SET EMT PC TO R5
3348 015616 012600      CMP      (SP)+,(SP)+
3349 015620 012601      MOV      (SP)+,%0
3350 015622 012602      MOV      (SP)+,R1
3351 015624 012603      MOV      (SP)+,R2
3352 015626 012604      MOV      (SP)+,R3
3353 015630 012605      MOV      (SP)+,R4
3354 015632 016646 177762      MOV      (SP)+,R5
3355 015636 016646 177762      MOV      -14,(SP),-(SP)
3356 015642 000002      MOV      -14,(SP),-(SP)
3357      RTI
3358

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3365
3366 015644 005037 177776      ;ROUTINE TO LOOP THRU A SINGLE INSTRUCTION TEST
3367 015650 000000      ;LOAD THE STARTING ADDRESS OF THE TEST
3368 015652 013767 177570 000146 ;YOU WISH TO RUN (THE ADDRESS OF THE TESTX
3369 015660 062767 000002 000140 ;TAG) AT THE 1ST HALT, SET SWITCH REGISTER
3370 015666 000000      ;OPTIONS AT THE 2ND HALT.
3371 015670 012767 177777 162612 ;NOTE THAT SW11 MUST BE DOWN AFTER THE 2ND HALT
3372 015676 032737 010000 177570 TESTX: CLR      %*PS
3373 015704 001404      HALT
3374 015706 042737 000020 177776      MOV      %*SR,RETURN      ;*WAIT FOR STARTING ADDRESS
3375 015714 000403      ADD      #2,RETURN      ;LOAD STARTING ADDRESS IN RETURN
3376 015716 052737 000020 177776      HALT      ;ADD 2 TO POINT TO INSTRUCTION AFTER
3377 015724 000177 000076      MOV      #-1,TSTX      ;SET SR OPTIONS
3378      BIT      #10000,%*SR      ;SET FLAG
3379      BEQ      ,+12      ;CHECK SW12
3380      BIC      #20,%*PS      ;BRANCH IF NOT SET
3381      BR      ,+10      ;CLEAR TRACE BIT
3382      BIS      #20,%*PS      ;SKIP NEXT INSTRUCTION
3383      JMP      %*RETURN      ;SET TRACE BIT
3384      ;JUMP TO TEST
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3399
3400
3401
3402
3403
3404
3405
3406
3407 016030
3408 016030 005015 041520 020075      ;SCOPE AND/OR ITERATION LOOP FOR EACH TEST 64 TIMES
3409 016036 020040 020040 020040 ;A SETUP ROUTINE SHOULD INITIALIZE RETURN AND IMAX
3410 016044 020040 041511 052116 SCOPECI: BIT      #40000,%*SR      ;TEST SR FOR SCOPE
3411 016052 020075      BNE      SCOPEB      ;YES, SCOPE
3412 016060 020040 020040 020040 BIT      #4000,%*SR      ;NO-TEST FOR ITERATION
3413      BNE      SCOPEX      ;INHIBIT ITERATION
3414      TST      TSTX      ;USING SINGLE SUBTEST STARTUP?
3415      BNE      SCOPEB      ;YES, LOOP
3416      CMP      ICNT,IMAX      ;COMPARE CURRENT COUNT TO MAX NUMBER
3417      BPL      SCOPEG      ;EXIT-DONE
3418      INC      ICNT      ;INCREMENT COUNT
3419      CMP      (6)+,%6      ;REPOSITION STACK
3420      MOV      (6)+,%*PS      ;RESTORE PREVIOUS PROCESSOR STATUS
3421      JMP      %*RETURN      ;REPEAT TEST
3422      SCOPECI: CLR      TSTX      ;IF USING TESTX STARTUP, RETURN TO NORMAL FLOW
3423      CLR      ICNT      ;CLEAR COUNT
3424      MOV      %*6,RETURN      ;SAVE SCOPE RETURN POINTER
3425      RTI      ;RETURN INLINE-NEXT TEST
3426      IMAX: 100      ;ITERATION COUNT
3427      ICNT: 0      ;COUNT LOCATION FOR ITERATION LOOP
3428      RETURN: 0      ;ADDRESS OF LAST TEST
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3413	016062	000									
3414	016063	040	046440	051120	MSTR:	.ASCII	'	MPR=	'		
3415	016070	020075									
3416	016072	020040	020040	020040	MTRG:	.ASCII	'	MPR DATA=	'		
3417	016100	020040	050115	020122							
3418	016106	040504	040524	020075							
3419	016114	020040	020040	020040	MDATA:	.ASCIZ	'				
3420	016122	020040	000								
3421	016125	015	020012	020040	MSTRX:	.ASCII	<15><12>		TEST LOC=	'	
3422	016132	020040	020040	052040							
3423	016140	051505	020124	047514							
3424	016146	036503	040								
3425	016151	040	020040	020040	MSTRX1:	.ASCII	'				
3426	016156	040									
3427	016157	040	027523	035102		.ASCII	'	S/B:	'		
3428	016164	040									
3429	016165	040	020040	020040	MSTRX3:	.ASCII	'				
3430	016172	040									
3431	016173	040	040527	035123		.ASCII	'	WAS:	'		
3432	016200	040									
3433	016201	040	020040	020040	MSTRX5:	.ASCIZ	'				
3434	016206	020040	000								

3435	016211	015	051412	052105	MSETSR:	.ASCIZ	<15><12>	'SET SR OPTIONS'			
3436	016216	051440	020122	050117							
3437	016224	044524	047117	000123							
3438	016232	020054	051120	051505	MCON:	.ASCIZ	'	PRESS CONTINUE'			
3439	016240	020123	047503	052116							
3440	016246	052516	000105								
3441	016252	005015	042523	020124	MMDEV:	.ASCIZ	<15><12>	'SET DEVICE ADDRESS IN SR'			
3442	016260	042504	044526	042503							
3443	016266	040440	042104	042522							
3444	016274	051523	044440	020116							
3445	016302	051123	000								
3446	016305	015	051412	052105	MMADR:	.ASCIZ	<15><12>	'SET MEMORY TEST LOC IN SR'			
3447	016312	046440	046505	051117							
3448	016320	020131	042524	052123							
3449	016326	046040	041517	044440							
3450	016334	020116	051123	000							
3451	016341	015	051412	052105	MMPAT:	.ASCIZ	<15><12>	'SET TEST PATTERN IN SR'			
3452	016346	052040	051505	020124							
3453	016354	040520	052124	051105							
3454	016362	020116	047111	051440							
3455	016370	000122									
3456	016372	005015	046412	046505	MMPRS:	.ASCIZ	<15><12><12>	'MEMORY PARITY REGISTERS PRESENT!<15><12>			
3457	016400	051117	020131	040520							
3458	016406	044522	054524	051040							
3459	016414	043505	051511	042524							
3460	016422	051522	050040	042522							
3461	016430	042523	052116	006472							
3462	016436	000012									
3463	016440	005015	040520	052122	MTHAP:	.ASCIZ	<15><12>	'PARTY REGISTERS CONTROL MEMORY AS!<15><12>			
3464	016446	020131	042522	044507							
3465	016454	052123	051105	020123							
3466	016462	047503	052116	047522							
3467	016470	020114	042515	047515							
3468	016476	054522	040440	035123							
3469	016504	005015	000								
3470	016507	040	020040	000040	MTYCOR:	.ASCIZ	'				
3471	016514	020055	000		MDASH:	.ASCIZ	'=	'			
3472	016517	015	000012		MCR:	.ASCIZ	<15><12>				
3473	016522	000113			MK:	.ASCIZ	'K'				
3474	016524	047516	050040	051101	MT:	.ASCIZ	'NO PARITY MEMORY FOUND!<15><12>				
3475	016532	052111	020131	042515							
3476	016540	047515	054522	043040							
3477	016546	052517	042116	005015							
3478	016554	000									
3479	016555	116	020117	040520	MTR:	.ASCIZ	'NO PARITY REGISTER FOUND!<15><12>				
3480	016562	044522	054524	051040							
3481	016570	043505	052123	051105							
3482	016576	043040	052517	042116							
3483	016604	005015	000								
3484	016607	040	020040	020040	MPRAD:	.ASCIZ	'	<15><12>			
3485	016614	020040	006440	000012							
3486	016622	005015	005015	042515	MTIT:	.ASCIZ	<15><12><15><12>	'MEMORY PARITY TEST - MAINDEC-11-DCMFA-B'			
3487	016630	047515	054522	050040							
3488	016636	051101	052111	020131							

3489	016644	042524	052123	026440		
3490	016652	046440	044501	042116		
3491	016660	041505	030455	026461		
3492	016666	041504	043115	026501		
3493	016674	000102				
3494	016676	005015	047520	042527	MPWRF: ,ASCIZ	<15><12>'POWER FAILED'
3495	016704	020122	040506	046111		
3496	016712	042105	000			
3497	016715	007			MPGEND: ,BYTE	007
3498	016716	005015	047105	020104	,ASCII	<15><12>'END PASS # '
3499	016724	040520	051523	036440		
3500	016732	040				
3501	016733	040	020040	020040	MPCNT: ,ASCIZ	' '
3502	016740	000040				
3503	016742	006415	041012	042101	MP6ER: ,ASCII	<15><15><12>'BAD PAR FOUND IN LOC '
3504	016750	050040	051101	043040		
3505	016756	052517	042116	044440		
3506	016764	020116	047514	020103		
3507	016772	020040	020040	020040	MP6ER1: ,ASCIZ	' '
3508	017000	000				
3509	017001	015	051012	043505	MX1: ,ASCIZ	<15><12>'REGISTER AT '
3510	017006	051511	042524	020122		
3511	017014	052101	000040			
3512	017020	047503	052116	047522	MX2: ,ASCIZ	'CONTROLS '
3513	017026	051514	000040			
3514	017032	005015	047514	042101	LDRMSG: ,ASCIZ	<15><12>'LOADERS RESTORED'
3515	017040	051105	020123	042522		
3516	017046	052123	051117	042105		
3517	017054	000				
3518	017055	015	041012	042101	PSMSG: ,ASCIZ	<15><12>'BAD PARITY SCAN COMPLETE'
3519	017062	050040	051101	052111		
3520	017070	020131	041523	047101		
3521	017076	041440	046517	046120		
3522	017104	052105	000105			
3523	017110	005015	047514	042101	MLDRSV: ,ASCII	<15><12>'LOADERS SAVED IN BANK 0'
3524	017116	051105	020123	040523		
3525	017124	042526	020104	047111		
3526	017132	041040	047101	020113		
3527	017140	060				
3528	017141	015	052012	020117	,ASCIZ	<15><12>'TO RESTORE LOADERS USE SA 210.'
3529	017146	042522	052123	051117		
3530	017154	020105	047514	042101		
3531	017162	051105	020123	051525		
3532	017170	020105	040523	031040		
3533	017176	030061	000056			
3534	017202	020040	020040	020040	MPCOR: ,ASCIZ	' - CORE PARITY REGISTER'<15><12>
3535	017210	020040	020055	047503		
3536	017216	042522	050040	051101		
3537	017224	052111	020131	042522		
3538	017232	044507	052123	051105		
3539	017240	005015	000			
3540	017243	040	020040	020040	MPRMOS: ,ASCIZ	' - MOS PARITY REGISTER'<15><12>
3541	017250	020040	026440	046440		
3542	017256	051517	050040	051101		

3543	017264	052111	020131	042522		
3544	017272	044507	052123	051105		
3545	017300	005015	000			
3546		017304			,EVEN	
3547		000001			,END	



ADRPT	000516	ADRS	077400	ADRTYP	001220	ADTENP	015242
AE	000001	BDCNV	015076	BDCNVA	015130	BDCNVB	015162
BDCNVC	015164	BDCNVD	015166	BEGIN	001764	BITPT	000520
BITO	000001	BIT1	000002	BIT10	002000	BIT11	004000
BIT12	010000	BIT13	020000	BIT14	040000	BIT15	100000
BIT2	000004	BIT3	000010	BIT4	000020	BITS	000040
BIT6	000100	BIT7	000200	BIT8	000400	BIT9	001000
BMDVA	015272	BMOVE	015262	CKBK0	010232	CLPPAR	013364
CMT16	007022	CMT17	007702	CNVCTR	015234	CN16	007042
CONT	011320	CONT10	004112	CON112	004642	COWT13	005122
CONT3	002434	CONT4	002712	COUNT	004154	DECVAL	015254
DIGIT	015236	DISPLA	177570	DISPLY	177570	DONE	011240
DONE10	004140	DONE11	004360	DONE12	004656	DONE13	005136
DONE14	005362	DONE15	006026	DONE16	006356	DONE17	007272
DONE20	010216	DONE4	002756	DONES	003140	DONE6	003500
DONE7	003612	EMTA	015430	EMTIMT	015404	EMTLIM	015472
EMTTAB	015450	EMTX	000011	ERR	013144	ERRA	013166
ERRA1	013214	ERRA2	013216	ERRA3	013226	ERRA4	013230
ERRA5	013240	ERRB	013242	ERRB3	013244	ERRC	013250
ERRD	013262	ERROR	104002	ERRORP	104003	ERRORS	104004
ERRR	013024	ERRST	012746	FTITLE	000512	GMPRA	001542
GMPRB	001670	GMPHC	001676	GMPHD	001732	HIADR	000530
HIWORD	000554	ICMT	016024	IMAX	016022	INDCO	000772
INDC1	000774	INDC10	001016	INDC11	001020	INDC12	001022
INDC13	001024	INDC14	001026	INDC15	001030	INDC2	000776
INDC3	001000	INDC4	001002	INDC5	001004	INDC6	001006
INDC7	001010	INDC8	001012	INDC9	001014	INDX17	007554
INST1	004002	INST2	004010	KPAR0	001240	KPAR1	001242
KPAR2	001244	KPAR7	001246	KPDRO	001230	KPDR1	001232
KPDR2	001234	KPDR7	001236	KTSTAR	001216	LDRMSG	017032
LDRSVD	013770	LQCATM	013500	LQCAT1	013576	LOGICA	011300
LOOP10	003704	LOOP11	004234	LOOP12	004450	LOOP13	004742
LOOP14	005220	LOOP15	005652	LOOP21	010712	LOOP4	002600
LOOP5	003034	LOOP6	003210	LOOP7	003552	LOP15	005662
LOP4	002606	LOP5	003042	LOP6	003216	LOWFLG	000556
LSAV	013652	LUP10	003676	LUP11	004220	LUP12	004434
LUP13	004734	LUP14	005230	LUP7	003544	MAPMA	011372
MAPMR	011564	MAPMEM	011360	MAPRB	011750	MAPRC	012050
MAPPD	012150	MAPRE	012244	MAPREG	011706	MAP1	013434
MCON	016232	MCP	016517	MDASH	016514	MDATA	016114
MEMH	001070	MEML	001066	MEMUT	000550	ME0	016030
MICNT	016054	MK	016522	MLDSV	017110	MMADR	016306
MHDEV	016252	MMPAT	016341	MMPRS	016372	NPC	016036
MPCMT	016733	MPGEND	016715	MPRAD	016607	MPRCOR	017202
MPRMOS	017243	MPROK	000542	MPRO	000570	MPR1	000600
MPR10	000710	MPR11	000720	MPR12	000730	MPR13	000740
MPR14	000750	MPR15	000760	MPR2	000610	MPR3	000620
MPR4	000630	MPRS	000640	MPR6	000650	MPR7	000660
MPR8	000670	MPP9	000700	MPSER	016742	MPSER1	016772
MPPRF	016676	MSETSR	016211	MSTR	016063	MSTRX	016125
MSTR1	016151	MSTRX3	016165	MSTRX5	016201	MT	016524
MTR	016622	MTHAP	016440	MTRMUM	016030	MTR	016555
MTRREG	016072	MTYCOR	016507	MTYFG	000564	MX1	017001
MX2	017020	NOKT	000552	NOP	000240	NOREG	001740

NRALL	013264	OACDST	015072	OACNT	015074	OACNV	014770
OACNVA	015012	OACNVX	015070	ODDFLG	000560	OPEN	000000
PARPAT	001040	PARVEC	000114	PASCNT	000544	PC	0000007
PDREND	001226	PDRTAB	001222	PERR	000000	PMENH	001074
PHEML	001072	PHEMX	001076	PS	177776	PGADRS	014372
PGCAN	014006	PSCANH	014374	PSCANX	014334	PSCAN1	014376
PSCX1	014510	PSLOOP	014432	PSLUP	014436	PMSG	017055
PSNXT	014462	PSXST	014516	PWRDN	015304	PWRUP	015350
RELOC	000566	RESRVD	001032	RESVC	001034	RESYM	001036
RETURN	016026	RSTART	001266	RSTLDR	013772	RSTLDX	014062
RST04	104006	RSTOS5	104007	RS04	015562	RS06	015610
R0	0000000	ROSAV	001252	R1	0000001	RISAV	001254
R2	0000002	R2SAV	001256	R3	0000003	R3SAV	001260
R4	0000004	R4SAV	001262	R5	0000005	R5SAV	001264
R6	0000006	SAVLDR	013654	SAVLDX	013752	SAV04	104005
SAV05S	104010	SCAN	001346	SCANA	001370	SCANB	001374
SCNFLG	001214	SCOPE	104001	SCOPEB	015772	SCOPEC	015730
SCOPEG	016004	SHDBE	000534	SP	0000006	SPBAV	001250
SR	177570	SKO	177572	START	001426	START1	001510
STKPT	000510	SURTEN	015174	SUBTNA	015200	SUBTNB	015214
SV04	015474	SV05A	015524	SV05B	015536	SV05C	015552
SV05S	015514	TBANK	000546	TEMP	000562	TEMPX	000514
TENPWR	015240	TERTX	015644	TEST1	002006	TEST10	003634
TEST11	004156	TEST12	004372	TEST13	004676	TEST14	005156
TEST15	005560	TEST16	006226	TEST17	007066	TEST2	002160
TEST20	010104	TEST21	010406	TEST3	002402	TEST4	002530
TEST5	002776	TEST6	003152	TEST7	003512	TMAP	012422
TMAPA	012436	TMAPB	012542	TMAPC	012630	TMAPD	012674
TMAPEX	012744	TNUM	000022	TPB	001102	TPCORE	005372
TPCORX	000042	TPS	001100	TRDATA	000540	TREG	000770
TRFLG	000522	TRP10	004020	TRP10A	004070	TRP12	004542
TRP13	000532	TRP14	005500	TRP15	006146	TRP16	006604
TRP16A	006610	TRP17	007456	TRP17A	007462	TRP20	010352
TRP4A	002726	TRP4B	002734	TRP4C	002742	TRP7	003622
TSTLOC	000532	TSTX	000510	TST10	003722	TST11	004252
TST12	004466	TST13	004756	TST14	005254	TST15	005726
TST4	002620	TST5	003056	TST6	003232	TST7	003566
TYCOR	000826	TYFLG	000824	TYPE	104000	TYPESX	014754
TYPSBX	014764	TYPSX	014736	WAS	000536	WFP	000004
WFP16	006374	WFP16A	006412	WFP17	007310	WFP17A	007326
WFP21	010542	WFP21A	010556	XFR1	007746	XFR2	011152
WFILLS	001105	WNULL	001104	*TPFLG	001106	*TYPE	001110
.	017304						

# digital

MAINDEC 11-DCMFA-B  
CHANGE ORDER

ORIGINATOR Ron Platukis  
TEL EXT 5171 , DATE 5/8/74  
DISC PROJ NO. E2007517  
COST CENTER NO. 340  
MC 687

MCO NO. 11-DCMFA-00004  
SHEET 1 OF 1  
DATE RECEIVED 9-12-74  
FIRST ISSUE 9-13-74  
FINAL ISSUE 9-16-74

**PROBLEM**

PROGRAM WOULD BOMB OUT AFTER 10 SEC. OF RUNNING, AND TTY WOULD TYPE "U". ALL MEMORY CONTAINED 124325 OR 125325. WRONG CODING WAS CAUSE.

PGM TO BE CHANGED

MD-11-DCMFA-B

DISP CODE 02

**CORRECTION**

A PATCH IN THE LOCATIONS BELOW WILL RECTIFY THE SITUATION. INSTRUCTION CLR TREG+20000 SHOULD READ CLR TREG.

OPTIONS AFFECTED

MA11, MF11, MS11

**BREAK-IN/EFFECTIVITY**

THIS MCO IS EFFECTIVE IMMEDIATELY AND IS GOOD UNTIL NEW REV., AT WHICH TIME IT MUST BE REPLACED.

PRODUCT LINES AFFECTED

11/45

ITEM NO.	DOCUMENT/PART NO.	OLD REV	NEW REV	DISP CODE	DESCRIPTION OF CHANGE			DOCUMENTATION AFFECTED
					LOC	OLD	NEW	
1	MD-11-DCMFA	B	B1	02	10274	5067	5037	<input checked="" type="checkbox"/> DIAGNOSTICS <input type="checkbox"/> TECH MANUAL <input type="checkbox"/> TESTER <input type="checkbox"/> TEST PROG  <input type="checkbox"/> ENG SPEC <input type="checkbox"/> PURCH SPEC  FIELD SERVICE AFFECTED <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> Customer Charge <input type="checkbox"/> Product Line Charge <input type="checkbox"/> PL _____  <input type="checkbox"/> Contact Software Distribution Center for price. <input type="checkbox"/> Information Only
					10276	10470	0770	
					10352	5067	5037	
					10354	10412	0770	

**DISPOSITION CODES**

- 00 - (DELETED)
- 01 - (DELETED)
- 02 - USE PRESENT STOCK UNTIL NEW STOCK AVAILABLE (PHASE IN)
- 03 - REWORK IMMEDIATELY (RETROFIT)
- 04 - (DELETED)
- 05 - (DELETED)
- 06 - DOCUMENT CORRECTION
- 07 - NEW ITEM (THIS ASSEMBLY)
- 08 - (DELETED)
- 09 - SCRAP IMMEDIATELY

*OK*  
1750

**APPROVAL SIGNATURES**

Typewritten / Hand Signature

DIAGNOSTIC ENGR. Bill Kellicker

MFG. ENGR. Bob Christopher

FIELD SERVICE Al Kimmel

PRODUCT ENGR. Dave Ives