

IDENTIFICATION

Product Code: AC-8898E-MC
Product Name: CZLACE0 LA36 TERM (DL11 & KL11)
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PAGE 2

HISTORY

1.0 DECO CZL
AC-E-9

1.1.0 Closed Problem Report AA3318

1.1.1 It was reported that a DL11-A operated at 110 baud caused failure in the AREAD routine because the 200 msec. delay is not of sufficient duration to allow setting of the Receiver Register Status "DONE" bit through the Maintenance bit facility.
The time delay was increased from 200 to 600 msec.

1.2.0 Closed Problem Report AA3643

1.2.1 Tests 56, 57, 60, 61, 62, 63, 64, 65, and 66 do not run properly when run on an LSI-11. This problem was resolved by changing the branch after the CHAIN command to go back to test for the LSI-11 switch in order to effect the appropriate action during each test.

1.2.2 Second time-out in Test 64 allows excessive wait for operator response. The time delay was reduced from "177777" to "600".

1.2.3 Common routine TYPE does not save the contents of R0 resulting in the loss of this information and consequent failure.

Instructions were included to save the contents of R0 on entry into the routine and to restore them upon exit.

1.2.4 Loss of stack contents for non-LSI-11 computers due to incorrect sequence of instructions in Test 65 was also reported in Problem Report AA3803. Refer to 1.3.1.

1.3.0 Closed Problem Report AA3803

1.3.1 Testing of non-LSI-11 computer
s results in the program hanging
up because the stack gets popped awa
y in Test 65. The branch
after the test for the LSI-11 switch in Test 6
5 should go to
the CHAIN command for proper exit from the test for n
on-LSI-11
machines. This change supersedes the change released in DEP
0
MD-11-DZLAC-0-1.

TABLE OF CONTENTS

1.0	ABSTRACT
2.0	REQUIREMENTS
2.1	Equipment and Assignments
2.2	Storage
2.3	Preliminary Programs
2.4	Additional Programs
3.0	LOADING PROCEDURE AND INITIALIZATION
4.0	STARTING PROCEDURE
4.1	Startin
4.2	Addresses
4.3	Switch Register Control With I/O Tests
4.4	Switch Register Control Without I/O Tests
4.5	Keyboard Control With I/O Tests
4.6	Keyboard Control Without I/O Tests
5.0	OPERATING PROCEDURE
5.1	Switch Register Control
5.2	Keyboard Control
6.0	TEST DE SCRIPTIONS
6.1	Printing Tests
6.1.1	Test0 - Data Path Test
6.1.2	Test1 - Printable Character Test
6.1.3	Test2 - Non-printable Character Test
6.1.4	Test3 - Carriage Return Test
6.1.5	Test4 - Multiple Line Feed Test
6.1.6	Test5 - Single Line Feed Test
6.1.7	Test6 - Backspace Test
6.1.8	Test7 - Overprint Test
6.1.9	Test8 - Printing Frequency Sweep Test
6.1.10	Test9 - Ribbon Feed Test
6.1.11	Test10 - Printer Bell Test
6.1.12	Test11 - Life Test

6.2 Echo Tests
6.2.1 Test20 - Character Echo Test
6.2.2 Test21 - Line Echo Test, Fast Rate
6.2.3 Test22 - Line Echo Test, Slow Rate
6.2.4 Test23 - Character/Code Echo Test
6.2.5 Test24 - Selected Pat
tern Echo Test
6.2.6 Test25 - Bell Echo Test
6.4 Standard I/O Tes
ts

1.0 ABSTRACT

This diagnostic is divided into three basic sections:

1. A check of the console terminal interface logic.
2. A check of the printing characteristics and control logic.
3. An echo portion designed to check the keyboard and to aid in the diagnosis of terminal problems.

Patterns used by the printing tests were chosen for ease of visual verification. The echo tests were designed for maximum flexibility, with Test 24 allowing any desired pattern to be used.

2.0 REQUIREMENTS

2.1 EQUIPMENT AND ASSIGNMENTS

The diagnostic is written to run on all models of the PDP-11 computer with either a KL11 or DL11 console terminal interface. The diagnostic is preset to test up to 16 additional terminals (on DL11's) assigned between addresses 776500 and 776676. This preset quantity (16) and pre-set address (776500) can be changed by depositing the quantity in DLNR and the starting address in DLADR. For example, to allow for up to 31 additional terminals, the address 775610 could be placed into DLADR and the octal equivalent of 31, i.e., (37) would be placed into DLNR. The number of additional DL11's actually tested will be adjusted automatically downward based upon the first DL11 address (within the implied range) found to be unresponsive. Thus if there is no DL11 present to match the address in DLADR only the console terminal will be tested. Therefore, all DL11's in excess of the console terminal must have contiguous address assignments with the lowest address correct.

ponding to the value in DLADR.

The console terminal (assigned standard) can be reassigned by placing the address of its receiver status register into CO NADD and its receiver interrupt vector into CONVEC. This reassignment can be made to a terminal within the set of terminals implied by DLNR and DLADR without adverse effect. Note that a terminal with a slower speed (if any) will determine the speed at which all of the terminals are tested. Such a terminal should generally be excluded from the test, or tested separately. (Refer to the symbol definitions in the listing for the above mentioned locations.)

2.2 STORAGE

The diagnostic program uses all of 4K of memory with exception of the area used by the absolute loader.

2.3 PRELIMINARY PROGRAMS

Any applicable PDP-11 diagnostics should be run on the processor. If any errors are encountered during the interface check, refer to the appropriate interface diagnostic for further help in locating the problem if needed.

2.4 ADDITIONAL PROGRAMS

This diagnostic is for verification of basic terminal functions only. If the terminals under test have hardware options installed run diagnostic MAINDEC-11-DZLAF-A, the LA36 TERMINAL OPTIONS TEST.

3.0 LOADING PROCEDURE AND INITIALIZATION

Load the LA36 diagnostic program tape following normal procedures. Before starting the program, refer to the description of the routine "DLY". Time delays used by the program are a function of the CPU model and memory type and should be set-up before running the diagnostic. The routine is preset for a PDP-11/05 with core memory. Refer to Section 2.1 for non-standard terminal addresses and for testing multiple DL11 interfaces.

If a hardware switch register does not exist, the program will use the contents of location 176 as the value of the switches. Therefore, be sure to load location 176 with the switch value before starting the program when not using hardware switches.

If the CPU is an LSI-11, 11/03 be sure to set switch register bit 9 to a 1. Special tests are run on the DLV11 interface.

4.0 STARTING PROCEDURE

4.1 STARTING ADDRESSES

200(8) = Run with Switch Register Control
- perform Console T

terminal I/O tests.

204(8) = Run with Switch Register Control

- skip Console Terminal I/O tests.

210(8) = Run with Keyboard

control

- perform Console Terminal I/O tests.

214
(8) = Run with Keyboard Control

- skip Console Terminal I/O tests.

4.2 Switch Register Control With I/O Tests

A. Set the switch register to 200(8) and press the load address switch.

B. Set switch register bit 9 to a 1 if the processor is an LSI-11, 11/03. Refer to Section 5.1.5.

C. Set the switch register bits 7-0 equal to the paper width in terms of the number of columns (octal). Refer to Section 5.1.8.

D. Set the switch register bit 8 equal to 0 or 1 and press the start switch. A message will be printed indicating the number of DL11's being tested. Refer to Section 5.1.6.

E. If bit 8 were zero when starting, the Printer tests are executed sequentially, after the entire series of I/O tests are executed.

F. If bit 8 was set when the start switch was pressed, the entire series of I/O tests will be executed and the CPU will halt at location SELHLT. The program will then be waiting for control via the switch register.

4.3 Switch Register Control - Without I/O Tests

Same as Section 4.2 except in step A, set the switch register to 204(8).

PAGE 7

4.4 Keyboard Control - With I/O Tests

- A. Set the switch register to 210(8) and press the load address switch.
- B. Set the switch register bits 7-0 equal to the paper width in terms of the number of columns (octal). Refer to Section 5.1.8.
- C. Set switch register bit 9 to a 1 if the processor is an LSI-11/11/03. Refer to Section 5.1.5.
- D. Set switch 8 and press the start switch. A message will be printed indicating the number of DL11's being tested. Refer to Section 5.1.6.
- E. If bit 8 was zero when starting, the printer tests are executed sequentially after the entire series of I/O tests are executed.
- F. If bit 8 were set when the start switch was pressed, the entire series of I/O tests will be executed followed by the select test message. The program will then be waiting for a test selection via any terminal keyboard. Refer to Section 5.2.

4.5 Keyboard Control - Without I/O Tests

Same as Section 4.4 except in step A, set the switch register to 214 (8).

5.0 OPERATING PROCEDURE

The program can be controlled in either of two methods: by the con-

sole switch register or from the keybo
ard of the terminal(s) under
test.

5.1 SWITCH REGISTER CONTROL

The various switches and their functions are listed below. Switches may be changed and set as desired except as noted in the specific switch descriptions. Refer to the detailed switch descriptions for further, more complete information.

SWITCH NUMBER	DESCRIPTION
15 T AT END OF TEST	1(up) = HALT 0(down) = CONTINUE TEST SEQUENCE
14 ERROR	1(up) = CONTINUE ON ERROR 0(down) = HALT ON ERROR
13	1(up) = DRIVE ONLY CONSOLE TERMINAL 0(down) = DRIVE ALL TERMINALS
11 INDIVIDUAL TEST	1(up) = LOOP ON 0(down) = NORMAL TEST SEQUENCE
9 ALL OTHER PDP-11'S	1(up) = CPU TYPE IS AN LSI-11, 11/03 0(down) =
8	1(up) = RUN TEST ONCE AND HALT 0(down) = LOOP ON TEST SEQUENCE
5-0 TEST NUMBER SELECTION	
7-0 ART-UP	NUMBER OF COLUMNS AT START

5.1.1 Switch 15

With switch 15 in the up position, the program will halt at the end of the current test. Replacing switch 15 to the down position and press-

ing CONTINUE will continue the normal test operation. Dur
ing the
halt, any of the control switches may be changed or set as desired.

5.1.2 Switch 14

Placing switch 14 in the up position will cause the pro
gram to contin-
ue on errors during any of the I/O tests only. With switch 1
4 down,
the program will halt (at ERRHLT) on any errors during the I-O tests
with the location of the error in R0. Pressing CONTINUE will cause
the pro
gram to continue if switch 14 is down. With switch 14 up,
pressing contin
ue will cause the program to loop on the error.

NOTE

Error halts can occur only during the I/O tests. The terminal is connected to a serial line and there is no error information returned to the program from the terminal. Therefore the program cannot report errors occurring in the terminal. Errors detected during the interface tests will result in halts as described above.

5.1.3 Switch 13

Placing switch 13 in the down position will cause the driving of all multiple terminals during the Printer tests only. If switch 13 is up, only the console terminal is driven.

** Note: Switch 13 should only be changed when the program is waiting for a test selection.

5.1.4 Switch 11

Placing switch 11 up at any time will cause the program to loop on the current test as long as switch 11 remains up. Replacing switch 11 down will cause the program to resume normal operation at the completion of the test.

5.1.5 Switch 9

Placing switch 9 up at the start of the test will cause an automatic change in the DELAY timing, and the execution of special DLV11 I/O tests. The DLV11 has no maintenance mode and will cause th

e program
to hang if tested as a DL11.

5.1.6 Switch 8

With switch 8
in the down position the program will continue to loop
through the present t
est sequence. Placing switch 8 up will cause the
program to halt (at SELHLT) a
t the completion of the current test.
After the halt, set the control switc
hes as desired and set switches 5
to 0 to the next desired test number, and the
n press CONTINUE to start
the test.

When starting the diagnostic the operator can select a specific test rather than automatically starting the printing test sequence by setting switch 8 up before starting the diagnostic. Upon completion of the I/O test sequence (if being run) the program will either halt at SELHLT waiting for a test selection via the switch register or print the select test message and wait for a test selection from any keyboard. Refer to Section 4 for further information.

5.1.7 Switches 5 to 0

Switches 5 to 0 are used to select specific tests when under switch register control. Test numbers are always in octal.

5.1.8 Switches 7 to 0 (at start-up only)

At start-up only, switches 7 to 0 are used to set the desired maximum number of columns the diagnostic is to test. If the number set is greater than 132(10) or less than 30(10), the program will default to 132(10). The value set must be in octal form. Thus, for normal operation leave switches 7 to 0 down to test the full 132(10) columns.

5.2 KEYBOARD CONTROL

The program will be under keyboard control whenever the diagnostic is started at location 210 or 214. Switches on the console switch register will have no effect when under terminal control except for switch 15. The I/O tests cannot be selected when under keyboard control.

To stop a test at any time, type the "RUBOUT" or "DELETE" key on any keyboard. Any terminal may stop the test and select the next test if switch 13 is down. When a test is stopped by typing a "RUBOUT" or "DELETE", the test will terminate and the following message will be typed:

SELECT TEST NUMBER

At this time, type the desired test number followed by any one of the following control characters:

- . (period) = Run the selected test once and return for another test selection.
- L "RUBOUT" = Loop on the selected test until a "RUBOUT" is typed.
- S = Start the test sequence with the selected test. Continue to loop on the printing test sequence until a "RUBOUT" is typed.

The "L" or "S" may be either upper or lower case, but the test number must always be a 2 digit octal number. The test number and terminator are echoed by the program, thus each character will be printed twice if the terminal is in half duplex. For all echo tests, the "L" and "S" will only run the test once (the same as if typing a period). For

all option tests, the "S" will only run the test once (the same as if typing a period), however, typing an "L" will cause the program to loop on the selected test. If an error is detected in the test selection (illegal test number or control character), a question mark is printed and the message will be repeated.

characters are printed in groups of three with three groups per line, separated by three spaces between groups. The first column will contain all ASCII codes from 040 to 077. Column two will contain all ASCII codes from 100 to 137 - primarily the capital letter set. The last column will contain all ASCII codes from 140 to 176 - primarily the small letter set.

With the Auto Line Feed Option set to produce an automatic line feed after every carriage return, there will be a blank line between each printed line.

EXAM
 PLE:

		!!!	AAA	'''
		BR	aaa
B	bbb	###	CCC	ccc
		\$\$\$	DDD	ddd
EE	eee	%%%	E	
		&&&	FFF	fff
		(((GGG	ggg
HHH	hhh)))	III	iii
		***	JJJ	jjj
		+++		
KKK	kkk	---	LLL	lll
		...	MMM	mmm
NNN	nnn	///	OOO	ooo
		000	PPP	ppp
		111		
QQQ	qqq	222	RRR	rrr
		333	SSS	sss
		44		
4	TTT	ttt	UUU	uuu
		555	VVV	vvv
		666		
		7		
77	WWW	www	XXX	xxx
		888	YYY	yyy
		999		
:::	ZZZ	zzz	[[[
]]]	\\	
		<<<]]	
		===		
]		>>>		
		???		

6.1.3 Test 2 - Non-printable Character Test

This test checks all non-printable characters that have no control function in the LA36 terminal or the LA36 options (such as CR, LF, BS,

& BEL).
First the ASCII code will be printed followed by the mnemonic
after a few separating spaces. Following the mnemonic, the actual
control character will be sent three times and nothing should happen
at the printer. This pattern is repeated three times on a line,
until all of the non-printing characters have been tested.

With the Auto Line Feed Option set to produce an automatic
line feed after every received carriage return, there will be a blank line
between each printed line.

EXAMPLE:

```
006 ACK 001 SOH 002 STX
         020 DLE 021 DC1 022 DC2
         023 DC3 024 DC
4 025 NAK
         026 SYN 027 ETB 030 CAN
SUB 034 FS
         031 EM 032
         035 GS 036 RS 037 US
         177 DEL
```

6.1.4 Test 3 - Carriage Return Test

This test checks the carriage return from all even numbered columns and the spacing of the solenoid head from the left margin. It is also a good check for proper operation of the position decoder.

The test prints a full line of alternating 0's and spaces, starting with a 0. At the end of the line the print head is returned to the left margin in with a carriage return. The spaces are then filled in by spacing the print head out from the left margin to the first space, printing an "X", and executing a carriage return. This pattern is repeated until the line is completed. Check to see that all X's are in the middle of the space between the two zeroes on either side of it.

EXAMPLE:

```
           0X0X0X0X0X0X0X0X0X0X0X0X0X0X0X0X0X0X0X0
X0X0X
```

With the Auto Line Feed Option set to produce an automatic line feed after every received carriage return, this test will print a line of 0's and spaces, then print a diagonal line of X's. To correctly check the encoder, the Auto Line Feed Option should be disabled.

EXAMPLE:

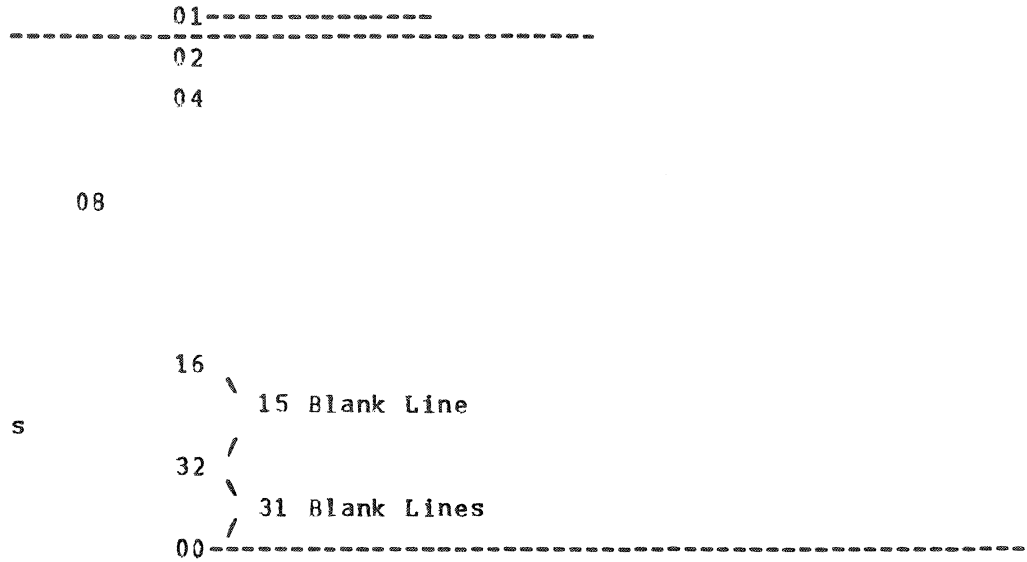
```
0 0 0 0 0 0 0 0 0 0
      X  X  X  X  X  X  X
        X  X  X  X  X  X
          X  X  X  X
            X  X  X
              X  X
                X
```

6.1.5 Test 4 - Multiple Line Feed Test

This test checks the line feed capability of the printer by sending various groups of line feeds interspaced with reference lines. The number printed as the reference line indicates the number of line feeds that follow. The first and last lines also contain a string of dashes as reference points for measuring the total distance between the two dashed lines, i.e., 63(10) lines.

With the Auto Line Feed Option set to produce an automatic line feed after every carriage return, the number printed will indicate one less than the number of line feeds (the number of blank lines) that follow. The total distance between the two dashed lines will then be 69 lines.

EXAMPLE:



6.1.6 Test 5 - Single Line Feed Test

This test is designed to check the timing of single line feeds and the capability of doing line feeds in all columns. Two reference lines are used by this test (and Test 6) which also can be used to easily check the number of columns the printer is printing.

The first reference line contains 130(10) zeroes followed by two 2's if testing 132(10) columns. If less than 132 columns, the line will contain 0's for two less than the maximum number of columns followed by the two 2's. This reference line is a quick check for 132(10) columns if testing the full 132(10) columns. The second reference line prints a string of numbers (1 to 9 & 0) repeated to the maximum column. This line, again, can be used as a quick check of the number of columns.

The line feed test is accomplished by: printing the first reference line of 0's and two 2's; then either sending 60(10) 3's, if testing 132(10) columns, or waiting 1.8 seconds for an LCV, if testing less than 132(10) columns. If testing 132(10) columns, nothing should happen, except for an LCV, at the end of the line. The 3's should be lost and never printed. After the LCV, with the print head at the extreme right, a carriage return - line feed will be sent followed by repeated backslashes "\" and linefeeds to print a diagonal line down the paper. When a backslash is printed in the maximum column, a carriage return will be sent immediately after the line feed and the second reference line of sequential numbers will be printed. After completing the line, a carriage return - line feed will be sent and the program will wait one second for the carriage return function to complete. After the delay, the reference line will be repeated, the last line being guaranteed to be correct. Any timing problems

during th
e line feeds will show as misprints or missing characters
during the first
16(10) characters of the middle reference line.
Also, any paper feed pro
blems will cause misalignment of the slashes
forming the diagonal line.

EXAMP
LE:

0000000000000000000000000000000022

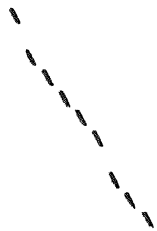
123456789012345678901234567890
123456789012345678901234567890

With the Auto Line Feed Option set to produce an automatic line feed after every received carriage return, there will be a blank line every

place a
carriage return is executed.

EXAMPLE:

0000000022



1234567890

1234567890

6.1.7 Test 6 - Backspace Test

This test is designed to test the print timing as in Test 5 as well as the backward and forward movement of the print solenoid head.

The test consists of the same first reference line as in Test 5 then a carriage return-line feed. A full line is then printed using the following pattern:

Forward Slash "/"
Backspace
Back Slash "\"

This pattern produces a line of all X's. The two slashes should cross exactly at the middle, producing the X character. When the line is completed a carriage return-line feed is sent and the last two reference lines are printed as in Test 5. Any timing problems will show in the first 16(10) characters of the middle reference line; again as in Test 5.

With the Auto Line Feed Option set
to produce an automatic line feed
after every received carriage return,
there will be a blank line
between each printed line.

EXAMPLE:

```
0000000000000000000000000022  
XXXXXXXXXXXXXXXXXXXXXXXXXXXX  
123456789012345678901234567890  
123456789012345678901234567890
```


6.1.8 Test 7 - Overprint Test

This test is designed to check the spacing and repeatable printing characteristics of the printer. Three rows of characters are each overprinted two times. The rows consist of the following characters alternated across the line:

Row 1	M-SP
Row 2	SP-a
Row 3	&-SP

The resulting pattern will be a checkerboard pattern and the overprinted characters should be aligned properly with the initial characters.

EXAMPLE:

```

M M M M M M M M M M M M M M M
  @ @ @ @ @ @ @ @ @ @ @ @ @ @ @
& & & & & & & & & & & & &
  
```

With the Auto Line Feed Option set to produce an automatic line feed after every received carriage return, the lines will not be overprinted. There will be three lines of each character with a blank line between each group of characters. The characters in each group should be in the same columns.

EXAMPLE:

```

M M M M M M M M M M
M M M M M M M M M M
M M M M M M M M M M
  @ @ @ @ @
  @ @ @ @ @ @ @ @ @ @
  @ @ @ @ @ @ @ @ @ @
  
```


6.1.9 Test 10 - Printing Frequency Sweep Test

This test prints the character "H" repeatedly, 30(10) characters per line for four lines. During the first two lines, the time interval between characters is increased from 30(10) milliseconds to 1.8 seconds using the following formula to create a logarithmic increase:

$$28 \quad \text{New Delay} = \text{Old Delay} + \text{Old Delay}/16 + \text{Old Delay}/1$$

The last two lines do just the reverse. The time interval between characters is decreased from 1.8 seconds to 30(10) milliseconds using the following formula to again create a logarithmic decrease:

$$\text{New Delay} = \text{Old Delay} - \text{Old Delay}/16 - \text{Old Delay}/128$$

Look for possible misalignment of the characters or spaces between characters as an indication of timing problems.

With the Auto Line Feed Option set to produce an automatic line feed after every received carriage return, there will be a blank line between each printed line.

EXAMPLE:

```

#####
#####
#####
H   #####
#####

```

6.1.10 Test 11 - Ribbon Feed Test

This test checks the ribbon feed mechanism by printing a single column of 24 lines of X's down the left hand margin of the page. Visually check for proper operation of the ribbon feed mechanism during this test.

With the
Auto Line Feed Option set to produce an automatic line feed
after every received carriage return, there will be a blank line
between each printed line.

EXAMPLE:

X
X
X
X
X
X
X

6.1.11 Test 12 - Printer Bell Test

This test checks the printer bell buffer to insure that eight bells are distinctly heard, even when sent at the maximum transfer rate. The program sends 8 bell codes at the maximum rate to the printer then waits 2.5 seconds to allow the operator to hear the bells.

6.1.12 Test 17 - Life Test

This test runs continuously and is run as an individual, special test. It is not part of the standard printing test sequence.

This test prints 2 lines of each printable character and then repeats continuously. The second line of each character is overprinted 4 times to conserve paper. At the end of each complete pass through the character set, a message is printed indicating the number of passes executed. If any character (except "Rubout") is typed on the keyboard during this test, the pattern will change and restart with the typed character. This will only happen if keyboard control is in use.

EXAMPLE:

AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA
AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA
AA
BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB
BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB
BBBBBB

If the Auto Line Feed Option is set to produce an automatic line feed after every received carriage return, the test will print six lines of each character with a blank line between the first and second lines as well as between each group of characters.

EXAMPLE:

AAAAAAAAAAAAAAAA

AAAAAAAAAAAAAAAA
AAAAAAAAAAAAAAAA
AAAAAAAAAAAAAAAA

AAAAAAAAAAAAAAAA
AAAAAAAAAAAAAAAA

BBBBBBBBBBBBBBBB

BBBBBBBBBBBBBBBB
BBBBBBBBBBBBBBBB
BBBBBBBBBBBBBBBB

BBBBBBBBBBBBBBBB
BBBBBBBBBBBBBBBB

6.2 ECHO TESTS

These tests are designed as a test of the keyboard and an aid in isolating troubles within the terminal. At the beginning of each test, the test number will be printed indicating which test is being executed. Typing a "RUBOUT" or "DELETE" at any time, whether in keyboard control or not, will exit the current Echo test and print a test termination message. If in keyboard control, the select test message will be printed and the program will await a test selection as usual. In switch register control, the program will halt (at SELLHLT) waiting for control via the switch register. A detailed description of each test follows:

6.2.1 Test 20 - Character Echo Test

This test is designed to operate the terminal in a simulated local mode. Any character typed on the keyboard (except a "rubout") will be echoed to the printer.

If the LA36 terminal is in half duplex with the Auto Line Feed Option available, typing a carriage return may cause a garbled response on the terminal during this test.

6.2.2 Test 21 - Line Echo Test, Fast Rate

This test continually sends full lines of any character up to the maximum column width. The test prints a "0" character when started until a key is typed on the keyboard. The program will then send the typed character until another character is typed or the test is terminated by typing a "rubout". The characters are transmitted at the maximum rate with a carriage return-line feed inserted after

every 132(10)
printable characters.

If the LA36 is in half duplex when running this test, characters may be lost or garbled whenever a character is typed on the keyboard.

With the Auto Line Feed Option set to produce an automatic line feed after every carriage return, there will be a blank line between each printed line.

6.2.3 Test 22 - Line Echo Test, Slow Rate

This test is identical to Test 21 except a delay of 1.8 seconds is inserted between each character to allow the print head to perform an LCV between characters.

6.2.4 Test 23 - Character/Code Echo Test

This test will print the octal code received by the processor followed by the character or the mnemonic of the character every time a key is pressed on the keyboard. The parity of the received code will be indicated as either odd or even. Allow sufficient time between characters for the line to be printed.

With the Auto Line Feed Option set to produce an automatic line feed after every received carriage return, there will be a blank line between each printed line.

EXAMPLE:

	301	A	ODD
	263	3	ODD
	215	CR	E
VEN	240	SP	EVEN

6.2.5 Test 24 - Selected Pattern Echo Test

This test is designed to give maintenance the flexibility to choose their own patterns for isolating any specific problems which may arise in the field.

Type any characters (except control-C and rubout) and each character will be echoed as typed. A maximum of 256(10) characters may be inputted. No carriage returns or line feeds are inserted by the program, all characters must be inputted by the operator. To terminate the input string type a control-C, the program will then continually echo the inputted pattern. To stop the printing, type control-C. The program will stop printing the pattern and will wait for either another pattern input terminated by a control-C, or the same pattern may be used again by typing control-C. To exit the test at any time, type a "rubout".

When any options are available, be careful what characters or character sequences are selected.

6.2.6 Test 25 - Bell Echo
Test

This test is designed to test the bell on column 64 if typing has occurred on the line. The test prints a message:

```
TYPE ANY PRINTABLE CHARACTER AND LISTEN FOR BELL .....
```

After the test message is printed, type any printable character on the keyboard. The character will be echoed and the bell should ring. The message will then be typed again. Type the "rubout" key to terminate the test at any time.

6.4 STANDARD I/O TESTS

These tests are designed as a brief check of the console terminal interface logic. Each check is structured as an independent test and the switch register control may be used. A description of each test is given in the program listing.

Any errors encountered during the I/O tests will cause a halt at location "ER RHLT" if switch 14 is down.

CZLACEO LA36 TERM (DL11 & KL11) MACRO M1110 25-AUG-78 10:13
TABLE OF CONTENTS

1-	1900	SWITCH REGISTER OPTIONS
2-	4500	SPECIAL OPERATIONAL INFORMATION
3-	6700	SYSTEM EQUATES
4-	13500	TRAP CATCHER & STARTING ADDRESSES
5-	19100	SYMBOL DEFINITIONS
7-	100	PROGRAM INITIALIZATION & CONTROL
13-	46300	COMMON ROUTINES USED BY LA36 TESTS
26-	100	I/O LOGIC TESTS
42-	100	LA36 PRINTER TESTS
55-	100	LA36 ECHO TESTS
62-	100	MISC. DIAGNOSTIC MESSAGES

400
500
600
700
800
900
1000
1100
1200
1300
1400
1500
1600
1700
1800
1900
2000
2100
2200
2300
2400
2500
2600
2700
2800
2900
3000
3100
3200
3300
3400
3500
3600
3700
3800
3900
4000
4100
4200
4300

```

        .TITLE CZLACE0 LA36 TERM (DL11 & KL11)
;LA36 DIAGNOSTIC (DL11 & KL11 INTERFACE)
;
;AUTHORS:  ROBERT W. BAKER
;          R. QUENNEVILLE
;          RALPH A. SCHAUER
;          JOHN V. CHATALIAN
;
;COPYRIGHT 1974,1977,1978 DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754
;
        .SBTTL SWITCH REGISTER OPTIONS
;SWITCH      POSITION      FUNCTION
;15          UP (1)       HALT AT COMPLETION OF CURRENT TEST
;           DOWN (0)      CONTINUE NORMAL TEST SEQUENCE
;14          UP (1)       CONTINUE ON ERROR
;           DOWN (0)      HALT ON ERROR
;13          UP (1)       DRIVE ONLY CONSOLE TERMINAL
;           DOWN (0)      DRIVE ALL TERMINALS
;11          UP (1)       LOOP ON INDIVIDUAL TEST
;           DOWN (0)      NORMAL TEST SEQUENCE
;09          UP (1)       CPU TYPE IS AN LSI-11, PDP-11/03
;           DOWN (0)      ALL OTHER PDP-11 CPUs
;08          UP (1)       HALT TO SELECT TEST AT END OF CURRENT TEST
;           DOWN (0)      LOOP ON TEST SEQUENCE
;05-00      TEST # SELECTION
;07-00      # OF COLUMNS AT START-UP
    
```

4500
4600
4700
4800
4900
5000
5100
5200
5300
5400
5500
5600
5700
5800
5900
6000
6100
6200
6300
6400
6500

```

        .SBTTL SPECIAL OPERATIONAL INFORMATION
;1.-- THE STANDARD CONSOLE TERMINAL INTERRUPT VECTOR AND REGISTER
;     ADDRESSES ARE USED. TO REDEFINE THE LOCATION OF THE CONSOLE
;     TERMINAL THE SYMBOLIC LOCATIONS "CONADD" AND "CONVEC" SHOULD
;     BE CHANGED BEFORE START UP.
;2.-- BEFORE START UP REFER TO THE DESCRIPTION OF THE ROUTINE "DLY".
;     TIMING IS A FUNCTION OF THE PDP-11 MODEL AND MEMORY TYPE AND
;     SHOULD BE SET UP BEFORE RUNNING THE DIAGNOSTIC.
;3.-- IF CPU IS A PDP-11/03, LSI-11 SET SWITCH REGISTER
;     BIT 09 TO A 1. SPECIAL TESTS ARE RUN ON THE DLV11.
;4.-- SYSTEMS WITHOUT A HARDWARE SWITCH REGISTER SHOULD USE
;     MEMORY LOCATION 176 AS A SOFTWARE SWITCH REGISTER.
;5.-- THIS DIAGNOSTIC IS FOR VERIFICATION OF BASIC TERMINAL
;     FUNCTIONS ONLY. IF THE TERMINAL UNDER TEST HAS HARDWARE
;     OPTIONS INSTALLED RUN DIAGNOSTIC MAINDEC-11-DZLAF-A, THE
;     LA36 TERMINAL OPTIONS TEST.
    
```

SYSTEM EQUATES

```

6700
6800
6900
7000
7100
7200      000000
7300      000001
7400      000002
7500      000003
7600      000004
7700      000005
7800      000006
7900      000007
8000      177776
8100
8200
8300
8400
8500      000001
8600      000002
8700      000004
8800      000010
8900      000040
9000      000100
9100      000200
9200      000400
9300      001000
9400      002000
9500      004000
9600      008000
9700      020000
9800      040000
9900      100000
10000     040000
10100     080000
10200     080000
10300     005776
10400     022826
10500     006340
10600     000200
10700     000500
10800     001000
10900
11000
11100
11200     104000
11300     104001
11400     104002
11500     104003
11600     104004
11700     104005
11800     104006
11900     104007
12000     104010
12100     104011
12200     104012
12300     104913
    
```

.SBRTL SYSTEM EQUATES

REGISTER EQUATES

```

R0=*0
R1=*1
R2=*2
R3=*3
R4=*4
R5=*5
SP=*6
PC=*7
PSW=177776
    
```

SYSTEM EQUATES

```

BIT0=1
BIT1=2
BIT2=4
BIT3=10
BIT4=40
BIT5=40
BIT6=100
BIT7=200
BIT8=200
BIT9=1000
BIT10=2000
BIT11=4000
BIT12=10000
BIT13=20000
BIT14=40000
BIT15=100000
OPR=0
SCOPSW=BIT14
NITRSW=BIT11
POPS=5776
POPS2=22826
PRTY4=340
ACRLF=200
LSI11=BIT9
    
```

```

;SCOPE SWITCH
;TEST LOOP SWITCH
;POP STACK ONCE
;POP STACK TWICE
;PRIORITY LEVEL DEFINITIONS

;FLAG FOR LSI-11,11/03
    
```

PROGRAM TRAP EQUATES

```

TYPE=EMT+0
ERRR=EMT+1
EHALT=EMT+2
STRDRV=EMT+4
STPCNV=EMT+4
CHAIN=EMT+5
CHALT=EMT+6
TYPEM=EMT+7
DELAY=EMT+10
TTVCL=EMT+11
CRLF=EMT+12
SCRLF=EMT+13
    
```

SYSTEM EQUATES

```

12400     104014
12500     104015
12600     104016
12700     104017
12800     104020
12900     104021
13000     104022
13100     104023
13200     104024
13300     104025
    
```

```

LF=EMT+14
PRINCL=EMT+15
PRTHDR=EMT+16
PRNT=EMT+17
READ=EMT+20
AREAD=EMT+21
CR=EMT+22
BPOASC=EMT+23
FORM=EMT+24
READC=EMT+25
    
```

```

13500
13600
13700 000000
13800 000000
13900
14000
14100
14200
14300 000000 000002
14400 000002 000000
14500 000004 000006
14600 000006 000000
14700 000010 000012
14800 000012 000000
14900 000014 000016
15000 000016 000000
15100 000020 000022
15200 000022 000000
15300 000024 000026
15400 000026 000000
15500 000030 002722
15600 000032 000340
15700
15800
15900 000042
16000
16100 000042 000000
16200
16300
16400 000046
16500
16600 000046 011522
16700
16800
16900
17000 000052
17100
17200 000052 010000
17300
17400 000052 010000
17500
17600 000174
17700
17800 000174 000000
17900 000176 000000
18000
18100 000200 000167 000604
18200 000204 000167 000326
18300 000210 000167 000320
18400 000214 000167 000552
18500
18600
18700
18800 000600
18900 000600 000000
    
```

.SBTTL TRAP CATCHER & STARTING ADDRESSES
 ;
 .ENABL ARS,AMA
 .ASECT
 ;
 .=0
 ;UNASSIGNED TRAP
 .+2 HALT ;SP OVERFLOW, BUS ERROR TRAP
 MACHER: .+2 HALT ;RESERVED INSTRUCTION TRAP
 .+2 HALT ;TRACE TRAP
 .+2 HALT ;TRAP TO CALL IOX
 .+2 HALT ;POWER FAIL TRAP
 .EMTINT ;EMT TRAP
 .PRTY7
 ;
 .=42
 0
 ;
 .=46
 LOGICAL
 ;
 .=52
 010000
 ;
 .=174
 DISPREG: .WORD 0 ;SOFTWARE DISPLAY
 SWREG: .WORD 0 ;SOFTWARE SWITCH REGISTER
 ;
 JMP START ;START UP WITH I/O TESTS RUNNING
 JMP START1 ;START UP, SKIP ALL I/O TESTS
 JMP START2 ;START UP TERMINAL CONTROL WITH I/O TESTS
 JMP START3 ;START UP TERMINAL CONTROL WITHOUT I/O TESTS
 ;
 .=600
 SPBOT: 0 ;BOTTOM OF STACK

```

19100
19200
19300
19400
19500 000602 177560
19600 000604 000060
19700 000606 176500
19800
19900
20000
20100
20200 000610 000020
20300 000612 177560
20400 000614 177562
20500 000616 177564
20600 000620 177566
20700 000622 000000
20800 000624 000000
20900 000626 000064
21000 000630 000200
21100 000632 000064
21200 000634 000000
21300 000636 000000
21400 000640 000000
21500 000642 000000
21600 000644 000000
21700 000646 000000
21800 000650 000000
21900 000652 000066
22000 000654 000000
22100 000656 000000
22200 000660 000000
22300 000662 000000
22400 000664 000000
22500 000666 000000
22600 000670 000000
22700 000672 000251
22800 000674 000006
22900 000676 000000
23000 000700 000000
23100 000702 000066
23200 000704 000000
23300 000706 000000
23400 000710 000000
23500 000712 000000
23600 000714 177570
23700 000716 000000
    
```

.SBTTL SYMBOL DEFINITIONS
 ;
 ;
 CONADD: 177560 ;ADDR OF CONSOLE RECEIVER STATUS REG
 CONVEC: 60 ;CONSOLE TERMINAL INTERRUPT VECTOR
 DLADR: 176500 ;ADDRESS OF FIRST DL11, DEFAULT TO DL11-A,B
 ;IF DL11-C,D,E,F THEN
 ;SET TO 176510 FOR FIRST 16 (OF 31) OR
 ;SET TO 176000 FOR LAST 16 (OF 31)
 ;OR SET OTHER DESIRED START ADDRESS
 ;# OF DL11'S TO BE INITIALLY ASSUMED
 DLNR: 16 ;CONSOLE RECEIVER STATUS REG
 TKR: 177562 ;CONSOLE RECEIVER BUFFER
 TKLVL: 177564 ;CONSOLE TRANSMITTER STATUS REG
 TPS: 177564 ;CONSOLE TRANSMITTER BUFFER
 TPB: 177566 ;CONSOLE TRANSMITTER INTERRUPT VECTOR
 TKVTR: 60 ;C.T. RECEIVER PRIORITY LEVEL
 TKLVL: PRTY4 ;C.T. RECEIVER INTERRUPT VECTOR
 TPVTR: 64 ;C.T. TRANSMITTER INTERRUPT VECTOR
 PTLVL: PRTY4 ;C.T. TRANSMITTER PRIORITY LEVEL
 PSTD: OPEN ;ADDRESS OF FIRST ACTIVE DL11
 CNTRL: OPEN ;CONSOLE TERMINAL CONTROL SWITCH
 CNTRL: OPEN ;CONTAINS CURRENT TEST NUMBER
 RNTNO: OPEN ;CONTAINS ADDRESS OF NEXT TEST
 NXTST: OPEN ;CONTAINS ADDRESS OF TEST SCOPE ENTRY
 SCOPT: OPEN ;CONTAINS TEST PROGRAM INDICATORS
 PRGID: OPEN
 CRBUF: OPEN
 CTRA: OPEN
 WIDTH: OPEN
 LEVEL: OPEN ;CURRENT PAPER WIDTH, BINARY
 DL11: OPEN ;LEVEL OF EXECUTION
 DL11: OPEN ;# OF MULTIPLE DL11'S
 ITCR: OPEN ;I/O TEST ITERATION COUNT
 REPT: OPEN ;TEMP STORAGE FOR TESTS E021 & E022
 ERCT: OPEN ;COUNTER FOR ROUTINE "AREA0"
 COUNT3: OPEN ;COUNTER FOR ROUTINE "PRINTC"
 XCSR: OPEN ;ADDRESS OF MULTIPLE DL11 STATUS
 TIMER: 251 ;1/4 SEC COUNTER FOR ROUTINE "DELAY"
 SPCT: OPEN ;COUNTER FOR TEST ROUTINE "pt3"
 CURTST: OPEN ;ADDRESS OF CURRENT TEST
 TPCPH: OPEN ;TEMP STOR FOR ECHO TESTS
 PARTV: OPEN ;PARITY FLAG FOR RECEIVED CHAR
 PCHAR: OPEN ;CHAR CODE WITH PARITY BIT
 LFCNT: OPEN ;COUNTER FOR TEST ROUTINE "pt4"
 INCHK: OPEN ;CHECK FOR INPUT FLAG
 TEMP: OPEN ;TEMPORARY WORKING STORAGE
 SR: 177570 ;SW REG ADDRESS
 CNTR: OPEN ;TIME COUNTER FOR LSI-11 TESTS

23900

PROGRAM INITIALIZATION & CONTROL

.SBTTL PROGRAM INITIALIZATION & CONTROL

```

100
300
400
500
900
100
800
900 000720 005767 177730
1100 000722 011403
1200 000730 005740
1300 000732 000000
1400 000734 000000
1500 000736 012767 177777 004324
1600 000744 012767 104006 000726
1700 000752 004424
1800 000762 012767 104011 000716
1900 000762 012767 005320 004300
2000 000770 004415
2100 000772 012767 104011 000700
2200 001008 012767 177777 004262
2300 001006 004066
2400 001010 012767 005320 004252
2500 001016 012767 104006 000654
2600 001024 012766 000600
2700 001030 016746 176752
2800 001034 016746 176744
2900 001040 012767 001054 176736
3000 001046 005777 177642
3100 001052 004411
3200 001054 012767 000176 177632 10S:
3300 001062 022626
3400 001064 104000
3500 001066 014424
3600 001070 012767 000202 177574
3700 001076 012667 176702 11S:
3800 001102 012667 176700
3900 001106 005067 177576
4000 001112 012767 000006 176664
4100 001120 005067 177520
4200 001124 005067 177504
4300 001130 005067 177520
4400 001134 012767 003460 176662
4500 001142 004767 002542

;*****
;COMMON HALT---WHEN IN SWITCH REGISTER CONTROL THE CPU
; WILL BE ADVANCED TO THIS COMMON HALT WHERE
; A NEW TEST WILL BE EXPECTED TO RE STARTED
;*****
CHLT: TST LEVEL ;TEST CURRENT LEVEL
      BEQ SELHLT ;BRANCH IF 0, DO NOT HALT
      MOV RSP,RO ;PUT ADDRESS OF CALLER INTO RO
      TST ~(R0)
      HALT
SELHLT: RTI ;RETURN FROM INTERRUPT
START1: MOV #CHALT, WAITF ;FORCE END OF I/O TESTS
        MOV #SR, CONTROL ;FORCE SR CONTROL
        BR STARTX
START2: MOV #TYCTL, WAITF ;FORCE TERMINAL CONTROL
        MOV #ATI, ATOX ;FORCE ALL I/O TESTS
        BR START1
START3: MOV #TYCTL, WAITF ;FORCE TERMINAL CONTROL
        MOV #177777, ATOX ;FORCE END OF I/O TESTS
        BR STARTX
START: MOV #ATI, ATOX ;FORCE ALL I/O TESTS
        MOV #CHALT, WAITF ;FORCE SR CONTROL
STARTX: MOV #SP00, SP ;SET STACK POINTER
        MOV @-(SP) ;SAVE CURRENT VECTOR
        MOV #10S, 4 ;SET UP TIMEOUT VECTOR
        TST MSR ;TRY TO REFERENCE HARDWARE SW REG
        BR 11S ;BRANCH IF NO TIMEOUT TRAP OCCURS
        MOV #SWREG, SR ;POINT TO SOFTWARE SWITCH REGISTER
        CMP (SP)+, (SP)+ ;RESTORE STACK
        TYPE ;TELL OPERATOR TO USE SOFTWARE
        NOSWR ;SWITCH REG AT LOC 176
        MOV #202, TIMER ;ADJUST TIMER FOR LSI-11
        MOV (SP)+, 4 ;RESTORE TIMEOUT VECTOR
        MOV (SP)+, 6
        MOV #6, MACHERR ;ALLOW INPUT CHECKING
        CLR INCHK ;CLEAN UP
        CLR PRGID ;INITIALIZE PROGRAM FLAGS
        CLR CNLWSW ;INITIALIZE TERMINAL CONTROL SWITCH
        CLR LEVEL ;INITIALIZE LEVEL
        MOV #PFA, 24 ;SET ADDR POWER FAIL ROUTINE
        JSR PC, CONIT ;SET UP CONSOLE TERMINAL ADDRESS
    
```



```

PROGRAM INITIALIZATION & CONTROL
4700
4800
4900
5000
5100
5200
5300
5400
5500
5600 001146 017701 177542
5700 001152 042701 177400
5800 001156 020127 000204
5900 001162 003123
6000 001164 020127 000035
6100 001170 101002
6200 001172 012701
6300 001172 010167 177450
6400 001202 012700 014127
6500 001206 012702 000003
6600 001312 104273
6700 001314 000461
6800 001216 000410
6900 001220 012700 000000
7000 001226 104007
7100 001226 104007
7200 001230 013676
7300 001232 012767 000240 177754
;*****
;READ THE PAPER WIDTH, NUMBER OF COLUMNS,
;FROM SWITCH REGISTER POSITIONS. SAVE AND
;CONVERT TO 3 ASCII CHARACTERS. A WIDTH GT 132
;OR LT 30 COLUMNS (DECIMAL) WILL BE REPORTED TO 132.
;THE SWITCHES MAY BE CHANGED ONCE THE PROGRAM TITLE OR THE DL11 COUNT
;MESSAGE HAS STARTED TO PRINT.
;*****
MOV R8,R1 ;PUT (SR) INTO R1
BIC #177400,R1 ;SAVE ONLY BITS 0-7
CMP R1,#204 ;TEST NO. COLUMN GT 132
RGT R1,#35 ;COLUMNS GT 132, DEFAULT TO 132
CMP R1,#35 ;CHECK IF NO. COLUMNS LT 30
BHI R1,#35 ;NOT LT 30 NOR GT 132
MOV R1,#204,R1 ;COLUMNS LT 30 OR GT 132, DEFAULT
R1,WIDTH ;SAVE NO. COLUMNS IN WIDTH
MOV #HDRO,R0 ;ADDR TO STORE ASCII COLUMN VALUE
BTOASC #3,R2 ;DO A 3 CHAR. CONVERSION
;CONVERT NO. COLUMNS TO ASCII
BR 5S
BR 6S
MOV #0,P0 ;TRANSMIT A
;NULL CODE
;TYPE PROGRAM TITLE FIRST TIME RUN
;*****
MOV #NOP,4S

```

```

PROGRAM INITIALIZATION & CONTROL
7500
7600
7700
7800
7900
8000
8100
8200 001240 012767 001320 176536 6S: MOV #END2A,WACHER ;INITIALIZE TIME OUT TRAP
8300 001246 016700 177334 MOV DLADR,R0 ;ADDRESS OF FIRST DL11 TO R0
8400 001252 016701 177332 MOV DLNR,R1 ;SET DL CHECK COUNT
8500 001256 005067 177374 CLR DLCNT ;INITIALIZE DLCNT
8600 001262 005710 TST (P0) ;IS DL PRESENT?
8700 001264 012767 001332 176512 END3: MOV #END2,WACHER ;YES, RESET TIME OUT TRAP
8800 001272 010067 MOV R0,FSTDL ;STORE ADDRESS OF FIRST DL11
8900 001276 000401 BR 2S ;CONTINUE
9000 001300 005710 1S: TST (R0) ;IS DL11 PRESENT
9100 001302 062700 #10,R0 ;POINTER AND DL11 ADDRESS
9200 001306 005267 177344 2S: INC DLCNT ;INCREMENT COUNT OF DL11'S
9300 001312 005301 DEC R1 ;DECREMENT DL CHECK COUNT, DONE?
9400 001314 001407 BEQ END4 ;BRANCH IF DONE
9500 001316 000770 BR 1S ;CHECK PRESENCE OF NEXT DL11
9600 001320 005301 END2A: DEC R1 ;DONE DL CHECK?
9700 001324 001404 BEQ END4 ;YES, EXIT
9800 001324 062700 000010 ADD #10,R0 ;NO, CHECK NEXT DL
9900 001330 000754 BR END3 ;CONTINUE
10000 001332 022626 END2: POPSP2 ;DL11 NOT PRESENT
10100 001334 016701 177316 END4: MOV #DL11S1,R0 ;GET # DL11'S
10200 001336 014064 MOV #2,R2 ;ADR OF ASCII CHAR STORAGE
10300 001344 012702 000002 MOV #0,R2 ;# OF ASCII CHARS
10400 001350 104023 BTOASC ;CONVERT NUMBER
10500 001354 014064 TYPE ;TYPE MESSAGE
10600 001354 014064 DL11S
10700
10800
10900
11000
11100
11200
11300
11400 001356 005067 177254 CLR RTNNO ;SET ROUTINE NO = 0
11500 001362 005067 177266 CLR LEVEL ;SET LEVEL = 0
11600 001366 026727 003676 177777 CMP ATOX,#177777 ;SEE IF I/O IS TO BE SKIPPED
11700 001374 001515 BEQ SKIP ;SKIP
11800 001376 012767 005266 177234 MOV #ATO,NXTST ;ADDRESS OF FIRST I/O TEST
11900 001404 104024 FORWD ;SET UP TEST PARAMETERS
12000 001406 000177 177264 JMP @CURTST ;GO TO I/O TEST ROUTINE
;*****
;THIS NEXT PART CHECKS THE PRESENCE OF DL11-A OR DL11-C
;STARTING AT 776500. A MESSAGE WILL BE PRINTED INDICATING THE NUMBER
;PRESENT. THE PRINTER DIAGNOSTIC WILL ADDRESS EACH OF
;THE MULTIPLE DL11S IN THE SYSTEM IF SWITCH 13 IS DOWN (0).
;*****
;*****
;EXECUTE THE STRING OF CONSOLE TERMINAL I/O TESTS
;WHEN EITHER HALT AT LOCATION SELHLR OR CONTINUE WITH
;PRINTER TESTS AS A FUNCTION OF SR BIT 9.
;*****

```

```

12200
12300
12400
12500
12600
12700
12800
12900
13000
13100
13200
13300
13400
13500
13600
13700
13800
13900
14000
14100
14200
14300
14400
14500
14600
14700
14800 001412 032767 000001 177214 CHAINN: BIT #1,CNTLSW ;CHECK IF TERMINAL CONTROL
14900 001420 001401 15: BEQ 15 ;BRANCH IF NOT
15000 001424 104081 TTYCTL ;GO TO TTYCTL CONTROL
15100 001424 002767 177214 1S: TST PRGID ;TEST ERROR BIT IN PRGID
15200 001430 100916 RPL 3S ;BRANCH IF ERROR BIT NOT SET
15300 001430 040000 177254 BIT #5,COPSW,ASR ;ERROR CHECK IF SCOPE OPTION ON
15400 001430 032767 177172 BIC #1,SCOPTR ;BRANCH IF NO SCOPING
15500 001442 022767 177777 CMP #1,SCOPTR ;YES, CHECK IF OK TO SCOPE THIS TEST
15600 001450 001403 BEQ 2S ;BRANCH IF NOT OK
15700 001452 004029 RTI #SCOPTR,ASP ;PUT ADDR OF SCOPE ENTRY INTO STACK
15800 001460 042767 177164 MOV #0,ASP ;GO TO SCOPE ENTRY IN TEST
15900 001466 100000 177156 2S: BIC #BIT15,PRGID ;CLEAR ERROR IND. IN PRGID
16000 001466 002767 177162 3S: TST LEVEL ;CHECK LEVEL
16100 001472 001405 BEQ 4S ;BRANCH IF LEVEL=0
16200 001474 032767 040000 177212 BIT #BITR5W,ASR ;TEST LOOP SWITCH ON (=1)
16300 001502 001405 BEQ 5S ;BRANCH IF NO LOOP TEST
16400 001504 000002 RTI ;GO BACK TO TEST
16500 001506 002767 177146 4S: DEC ICTR ;DECREMENT TEST ITERATION COUNT
16600 001506 000002 BEQ 6S ;BRANCH IF COUNT=0
16700 001514 000002 RTI ;NOT ZERO, REPEAT TEST
16800 001516 032767 000400 177170 5S: BIT #BIT8,ASR ;TEST IF SEQUENCE TEST (BIT8)
16900 001524 001407 BEQ 6S ;BRANCH TO NEXT TEST IF BIT8=0
17000 001526 000146 WAITF ;GO WAIT FOR MORE INPUT
17100 001532 022526 POPS2 ;POP 2 OFF STACK
17200 001534 000240 CHAINV: NOP ;THIS FORMERLY WAS RESET
17300 001536 100003 BPL ASR ;CHECK SR
17400 001536 100003 BPL ASR ;BRANCH IF NO HALT WANTED
17500 001544 167006 MOV# RINNO,RO ;CURRENT TEST NUMBER TO RO
17600 001550 000000 HALT ;HALT (NOT FOR TEST SELECTION)
17700 001552 177076 1S: BEQ LEVEL ;TEST THE CURRENT LEVEL
17800 001552 001420 BEQ 3S ;BRANCH IF 0
    
```

```

*****
CHAINN-- THIS PORTION IS THE COMMON RETURN
FOR ALL THREE CLASSES OF TESTS.

1--IF AN ERROR OCCURRED DURING AN I/O TEST THE
OPERATOR CAN CAUSE THAT TEST TO BE LOOPED
WITHOUT ANY FURTHER ERROR HALTS BY
SETTING THE SCOPE BIT (#1) ON THE SR=1.
SETTING SR BIT #4 TO 0 WILL ALLOW THE
ERROR HALT TO OCCUR AGAIN IF IT STILL EXISTS.

2--IF THE OPERATOR IS IN THE MAINTENANCE
MODE (BIT 8 SET = 1) AT START UP TIME, THE
SELECTED PROGRAM WILL LOOP CONTINUOUSLY
IF SR BIT #1 IS SET=1. IF BIT #1 IS = 0
THEN THE PROGRAM WILL BE ADVANCED TO
THE NEXT TEST IN IT'S CLASS IF BIT 8=0.
AS LONG AS BIT #1 AND
BIT 8 ARE 0, THE CLASS OF TESTS SELECTED
WILL BE CONTINUOUSLY SEQUENCED THROUGH.
IF BIT #1 IS 0 AND BIT 8=1, THEN THE CPU
WILL HALT AT LOCATION SELCT AND WAIT FOR THE
NEXT TEST NUMBER TO BE SET IN THE
***** SWITCH REGISTER.
    
```

```

17900 001560 012767 000006 176216 MOV #6,WACHER ;CLEAN UP
18000 001566 012706 MOV #SPBOT,SP ;SET UP STACK POINTER
18100 001572 104024 FORWD ;SET UP VALUES FOR NEXT TEST
18200 001574 000667 177036 CMP #1,NXTST ;END OF I/O TESTS (=-1)
18300 001602 001004 BNE 2S ;BRANCH IF NOT END
18400 001604 012767 177026 MOV #ATO,NXTST ;SET UP VALUES FOR NEXT TEST
18500 001612 104024 FORWD ;GO TO TEST
18600 001614 032767 177056 2S: JMP @CURTST ;END OF I/O TESTS (=-1)
18700 001620 022767 177777 3S: CMP #1,NXTST ;END OF I/O TESTS (=-1)
18800 001626 001012 BNE NEXT1 ;BRANCH IF NOT
18900 001630 032767 000400 177056 SKIP: BIT #BIT8,ASR ;TEST IF WANT TEST SELECTION RIGHT AWAY
19000 001636 001016 BNE NEXT1 ;BRANCH IF NOT
19100 001640 052767 000200 176776 BIT #BIT7,PRGID ;TEST IF WANT TEST SELECTION RIGHT AWAY
19200 001645 012767 007372 176764 BIC #17,PRGID ;BYPASS SCOPING
19300 001654 012767 000006 MOV #PPO,NXTST ;BYPASS SCOPING, GO TO PRINTER TESTS
19400 001662 012767 000600 NEXT: MOV #6,WACHER ;CLEAN UP
19500 001666 104024 FORWD ;SET UP STACK POINTER
19600 001670 000177 177002 MOV #SPBOT,SP ;SET UP NEXT TEST PARAMETERS
19700 001674 005267 176754 JMP @CURTST ;GO TO ROUTINE
19800
19900
20000
20100
20200
20300
20400
20500
20600
20700
20800
20900 001700 104006 WAITF: CHALT ;OR TTYCTL IF START WAS AT 210
21000 001702 012767 176074 MOV #6,WACHER ;CLEAN UP
21100 001710 012706 MOV #SPBOT,SP ;SET UP STACK POINTER
21200 001714 012706 MOV #R,RO ;GET CURRENT SW REG
21300 001720 042700 177700 BIT #R,RO
21400 001724 020027 000037 CMP #R,#37 ;TEST IF PROG NO. IS I/O TEST
21500 001730 011403 BLOS 1S ;BRANCH IF EQ OR LT 37. AN ECHO OR PRINTER
21600 001732 005367 176706 CLR PRGID ;I/O TEST, CLEAR PRGID
21700 001736 000403 BP 2S
21800 001740 052767 000200 176676 1S: BIS #BIT7,PRGID ;BYPASS SCOPING
21900 001746 000241 CLR C ;CLEAR C BIT
22000 001750 006100 RTI ;GET PROGRAM ADDRESS OUT OF
22100 001752 016057 002522 176660 MOV PRGTAB(RO),NXTST ;PROGRAM ADDRESS TABLE
22200 001760 026727 176654 001700 CMP NXTST,#WAITF ;TEST IF LEGAL TEST NO.
22300 001766 004024 BEQ FORWD ;BRANCH IF ILLEGAL
22400 001770 000177 FORWD ;SET UP TEST PARAMETERS
22500 001772 000177 JMP @CURTST ;GO TO TEST
    
```

```

*****
WAIT FOR FURTHER INSTRUCTIONS:
-LOAD PROGRAM NUMBER INTO BITS 0-5 OF THE SR
-SET SR BIT #11=1 TO LOOP ON SELECTED TEST
-SET SR BIT #11=0 AND BIT #9=0 TO LOOP THROUGH
SEQUENCE OF SELECTED TESTS.
-SET SR BIT #11=0 AND BIT #9=1 TO HALT AGAIN AFTER
EXECUTING TEST ONCE
*****
    
```

```

22700 ;*****
22800 ;TTV1-- THIS SECTION IS USED WHEN THE DIAGNOSTIC IS BEING CONTROLLED BY
22900 ; THE CONSOLE TERMINAL. IT IS EFFECTIVE ONLY WHEN THE DIAGNOSTIC
23000 ; STARTING ADDRESS IS 210 AND SR BIT 6 WAS SET AT START TIME.
23100 ; THE RESPONSE TO THE MESSAGE "SELECT TEST NO." MUST BE THE 2
23200 ; DIGIT OCTAL TEST NUMBER FOLLOWED BY :
23300 ; "S" TO LOOP ON TEST
23400 ; "L" TO LOOP ON SEQUENCE
23500 ; "E" TO EXECUTE TEST ONCE
23600 ; ALL SPACES WILL BE IGNORED. AN ILLEGAL INPUT WILL BE FLAGGED BY A "?"
23700 ; AND THE RETYPING OF THE ABOVE MESSAGE.
23800 ;*****
23900
24000 001776 022626 TTV1: POPSP2 ;POP 2 FROM STACK
24100 002004 109913 TSTB ;TEST IF ANY INPUT
24200 002006 176602 BR ;BRANCH IF NOT
24300 002006 017705 MOV ;GET CHAR
24400 002012 042705 BIC #17760,R5 ;GET CHAR
24500 002018 026527 CMP #177,R5 ;MASK BITS
24600 002022 001064 BNE ;CHECK IF RUBOUT
24700 002024 042767 004400 176602 BIC #4400,CNTLSW ;BRANCH IF NOT
24800 002032 000413 BR TTV1B ;CLEAR LOOP BITS
24900 002032 011401 004000 176572 1s: BIT #NITRSW,CNTLSW ;CHECK IF LOOP ON TEST
25000 002032 011401 BEQ 2S ;BRANCH IF NO LOOP ON TEST
25100 002044 000002 RTI ;LOOP ON TEST
25200 002046 032767 000400 176560 2s: BIT #BITS,CNTLSW ;TEST IF LOOP ON SEQUENCE
25300 002054 011401 BEQ ;BRANCH IF NO LOOP ON SEQUENCE
25400 002054 000164 JMP CHAINV ;CHAIN TO NEXT TEST
25500 002062 012767 177777 176620 TTV1R: MOV #1,NCHK ;CHECK IF YES
25600 002070 012700 MOV #30,,RO ;DELAY FOR HALF DUPLEX
25700 002074 104010 DELAY ;DELAY FOR HALF DUPLEX
25800 002076 104010 PRN ;PRINT
25900 002100 014341 TTYM ;MESSAGE
26000 002102 005067 CLR INCHK ;TYPE MESSAGE
26100 002106 104020 176602 1s: READ ;ALLOW INPUT CHECKING AGAIN
26200 002116 061773 000040 000040 1s: READ TEMPCH,#40 ;WAIT FOR INPUT
26300 002120 012700 BEQ 1S ;TEST IF CHAR IS A SPACE
26400 002120 012700 MOV #30,,RO ;BRANCH IF YES
26500 002126 104010 DELAY ;DELAY FOR HALF DUPLEX
26600 002130 117777 176460 176462 ;READY?
26700 002136 004767 000316 MOVR ;ECHO CHAR
26800 002142 000545 PC,TESTC ;CHECK IF CHAR IS OK
26900 002144 010045 BR ;NO, ERROR
27000 002144 010045 R5 ;OK, PUT CHAR INTO R5
27100 002146 006305 R5,RS ;SHIFT INTO POSITION 5-3
27200 002150 006305 ASL ;SHIFT INTO POSITION 5-3
27300 002154 006305 R5 ;SHIFT INTO POSITION 5-3
27400 002154 006305 ASL ;SHIFT INTO POSITION 5-3
27500 002156 026727 176516 000040 2s: READ ;WAIT FOR NEXT CHAR
27600 002164 001773 000036 CMP ;CHECK IF SPACE
27700 002166 011401 BEQ 2S ;BRANCH IF SPACE
27800 002166 104010 MOV #30,,RO ;DELAY FOR HALF DUPLEX
27900 002174 104010 DELAY ;DELAY FOR HALF DUPLEX
28000 002176 117777 176412 176414 ;READY?
28100 002176 004767 000250 MOVR ;ECHO CHAR
28200 002176 004767 000250 PC,TESTC ;CHECK IF CHAR IS OK
28300 002210 000516 BR ;ERROR IN CHAR
28400 002212 060005 ADD ;OK,RS NOW = OCTAL TEST NO.
    
```

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28400 002214 104020 3s: READ ;WAIT FOR TERMINATION CHARACTER
28500 002216 026727 176456 000040 3s: READ TEMPCH,#40 ;CHECK IF SPACE
28600 002224 001773 000036 BEQ 3S ;BRANCH IF SPACE
28700 002226 012700 MOV #30,,RO ;DELAY FOR HALF DUPLEX
28800 002232 104010 DELAY ;DELAY FOR HALF DUPLEX
28900 002234 104010 PRN ;PRINT
29000 002236 117777 176352 176354 MOVR ;READY?
29100 002244 012767 004001 176362 MOVR #401,CNTLSW ;ECHO CHAR
29200 002252 026727 176422 000114 CMP #401,CNTLSW ;SET BITS 11 & 0
29300 002260 001427 BEQ 5S ;NO, IS IT AN "L" ?
29400 002262 026727 176412 000154 CMP TEMPCH,#114 ;IS THIS AN "L" ?
29500 002266 001427 BEQ 5S ;BRANCH IF YES
29600 002272 026727 176402 000123 CMP TEMPCH,#154 ;CHECK LOWER CASE
29700 002300 001414 BEQ 5S ;BRANCH IF YES
29800 002302 026727 176372 000163 CMP TEMPCH,#123 ;NO, IS IT AN "S" ?
29900 002310 011410 BEQ 4S ;BRANCH IF YES
30000 002312 026727 176362 000056 CMP TEMPCH,#163 ;CHECK LOWER CASE
30100 002320 001052 BNE 4S ;BRANCH IF YES
30200 002322 012767 000001 176304 BR ;NO, IS IT A "." ?
30300 002326 000403 MOV #1,CNTLSW ;NO, ERROR
30400 002332 012767 000401 176274 4s: MOV #401,CNTLSW ;YES SET ONLY BIT 0 IN CONTROL WD
30500 002340 012767 000006 175436 5s: MOV #6,MACHER ;SET BITS 8 & 0
30600 002346 012767 000600 MOV #6,BBOT,SP ;CLEAN UP
30700 002352 000040 000040 CMP #40,SP ;INIT SP
30800 002356 103033 BRHS ;IS THIS AN I/O TEST
30900 002360 020527 000030 CMP #30,SP ;BRANCH IF YES
31000 002364 103007 BRHS ;IS THIS AN OPTION TEST?
31100 002366 020527 000020 CMP #20,SP ;SKIP IF YES
31200 002372 103464 BLO ;IS THIS AN ECHO TEST
31300 002374 012767 000001 176232 MOV #1,CNTLSW ;FORCE ECHO TEST TO A SINGLE RUN
31400 002402 004402 001300 JSR ;LEAVE THIS TERMINAL AS CONSOLE
31500 002404 034767 000200 176226 7s: PC,CONIT ;RESET CONSOLE TERMINAL ADDRESS
31600 002410 052767 000200 176226 7s: BR #017,PRGID ;BYPASS SCORING
31700 002416 000241 CLC ;CLEAR C BIT
31800 002420 006105 R5 ;
31900 002422 016567 MOV PRGTAB(R5),NXTST ;ADDR OF TEST TO NXTST
32000 002430 026727 176210 001700 CMP NXTST,#WAIT ;CHECK IF TEST EXISTS
32100 002436 001403 BEQ ;BRANCH IF NOT
32200 002440 104924 FORWD ;SET UP TEST PARAMETERS
32300 002442 000177 176230 JMP ;GO TO TEST
32400 002446 104917 000077 176142 8s: PRN ;CHECK IF PRINTER IS READY
32500 002450 112777 000077 176142 MOVB #77,ATPR ;SEND A "Z"
32600 002456 000601 BR TTV1B ;TRY AGAIN
    
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32800                                ;TESTC--CHECKS THAT THE INPUTTED CHARACTER IS BETWEEN 0 AND 7 INCLUSIVE
32900                                ;
33000 002460 025727 176214 000060 TESTC: CMP      TEMPCH,#60    ;CHECK IF NUMERIC AND EQ OR GT 0
33100 002466 103061                BHS      IS              ;BRANCH IF OK
33200 002470 000207                RTS      PC              ;ERROR RETURN
33300 002472 026727 176202 000067 1S:  CMP      TEMPCH,#67    ;CHECK IF EQ OR LT 7
33400 002500 101461                RTS      PC              ;BRANCH IF OK
33500 002502 000207                RTS      PC              ;ERROR RETURN
33600 002504 062716 000002 2S:  ADD      #2,OSP        ;SET UP RETURN ADDRESS
33700 002510 016700                MOV      TEMPCH,R0      ;GET CHAR
33800 002514 042700                BIC     #177770,R0     ;SAVE ONLY THE DIGIT
33900 002520 000207                RTS      PC              ;NORMAL RETURN
    
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34100 002522 007372                PRGTAB: PTO           ;DATA PATH TEST
34200 002524 007456                PT1           ;PRINTER CHARACTER TEST
34300 002526 007570                PT2           ;NON-PRINTING CHARACTER TEST
34400 002530 010164                PT3           ;CARRIAGE RETURN TEST
34500 002532 010304                PT4           ;MULTIPLE LINE FEED TEST
34600 002534 010462                PT5           ;SINGLE LINE FEED TEST
34700 002536 010666                PT6           ;BACKSPACE TEST
34800 002540 011054                PT7           ;OVERPRINT TEST
34900 002542 011266                PT10          ;PRINTING FREQUENCY SWEEP TEST
35000 002544 011474                PT11          ;RIBBON FEED TEST
35100 002546 011456                PT12          ;PRINTER BELL TEST
35200 002550 001700                WAITF        ;SPARE
35300 002552 001700                WAITF        ;SPARE
35400 002554 001700                WAITF        ;SPARE
35500 002556 001700                WAITF        ;SPARE
35600 002560 011546                PT17          ;LIFE TEST
35700 002562 012116                EO20         ;CHARACTER ECHO TEST
35800 002564 012166                EO21         ;LINE ECHO TEST, FAST RATE
35900 002566 012254                EO22         ;LINE ECHO TEST, SLOW RATE
36000 002570 012476                EO23         ;CHARACTER/CODE ECHO TEST
36100 002572 013020                EO24         ;SELECTIVE PATTERN ECHO TEST
36200 002574 013566                EO25         ;BELL ECHO TEST
36300 002576 001700                WAITF        ;SPARE
36400 002600 001700                WAITF        ;SPARE
36500 002602 001700                WAITF        ;SPARE
36600 002604 001700                WAITF        ;SPARE
36700 002606 001700                WAITF        ;SPARE
36800 002610 001700                WAITF        ;SPARE
36900 002612 001700                WAITF        ;SPARE
37000 002614 001700                WAITF        ;SPARE
37100 002616 001700                WAITF        ;SPARE
37200 002620 001700                WAITF        ;SPARE
37300 002622 005256                AT0          ;I/O TEST NO. 40
37400 002624 005322                AT1          ;I/O TEST NO. 41
37500 002626 005352                AT2          ;I/O TEST NO. 42
37600 002630 005404                AT3          ;I/O TEST NO. 43
37700 002632 005436                AT4          ;I/O TEST NO. 44
37800 002634 005526                AT5          ;I/O TEST NO. 45
37900 002636 005664                AT6          ;I/O TEST NO. 46
38000 002640 005674                AT7          ;I/O TEST NO. 47
38100 002642 005744                AT10         ;I/O TEST NO. 50
38200 002644 006002                AT11         ;I/O TEST NO. 51
38300 002646 006042                AT12         ;I/O TEST NO. 52
38400 002650 006116                AT13         ;I/O TEST NO. 53
38500 002652 006176                AT14         ;I/O TEST NO. 54
38600 002654 006252                AT15         ;I/O TEST NO. 55
38700 002656 006362                AT16         ;I/O TEST NO. 56
38800 002660 006430                AT17         ;I/O TEST NO. 57
38900 002662 006500                AT20         ;I/O TEST NO. 60
39000 002664 006572                AT21         ;I/O TEST NO. 61
39100 002666 006672                AT22         ;I/O TEST NO. 62
39200 002670 007000                AT23         ;I/O TEST NO. 63
39300 002672 007112                AT24         ;LSI TEST NO. 64
39400 002674 007270                AT25         ;LSI TEST NO. 65
39500 002676 001700                AT26         ;LSI TEST NO. 66
39600 002700 001700                WAITF        ;SPARE
39700 002702 001700                WAITF        ;SPARE
    
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39800 002704 001700      WAITF      ; SPARE
39900 002706 001700      WAITF      ; SPARE
40000 002710 001700      WAITF      ; SPARE
40100 002712 001700      WAITF      ; SPARE
40200 002714 001700      WAITF      ; SPARE
40300 002716 001700      WAITF      ; SPARE
40400 002720 001700      WAITF      ; SPARE
40500
40600
40700
40800
40900
41000
41100 002722 011546      EMTINT:  MOV  R0,-(SP)      ; PUSH STACKED PC TO GET A WORK COPY. (Q)
41200 002724 022716      SUB  #2,R0              ; SUB 2 TO POINT TO CALLING TRAP INSTR.
41300 002730 017616      MOV  @SP,RSP          ; PLACE TRAP INSTR INTO THIS STACK WORK AREA.
41400 002734 121627      CMPB @SP,#35         ; EXAMINE ITS RIGHT SIDE (Q)
41500 002740 101462      BLOS 2S              ; BRANCH IF WITHIN RANGE OF ESTABLISHED TABLE.
41600 002742 000000      HALT                ; ELSE HALT.
41700 002744 000776      BR  1S
41800 002746 006116      2S:  ROL  R0           ; MULT INSTR BY 2 TO GET WORD DISPLACEMENT.
41900 002750 042716      BIC  #177001,RSP     ; STRIP OFF OP CODE AND LS BIT.
42000 002754 002795      ADD  #EMTTAB,RSP    ; ADD IN STARTING ADDRESS OF TABLE.
42100 002760 017616      MOV  @SP,RSP          ; FROM TABLE GET OUT DESIRED POINTER.
42200 002764 005046      CLR  -SP             ; PUSH A ZERO PSW.
42300 002766 007485      MOV  #3$,-(SP)      ; PUSH PC = TO #3$ OF THIS ROUTINE.
42400 002768 016074      RTI  3S             ; DO RTI (POP-POP) TO ESTABLISH THE ZERO PSW.
42500 002774 000136      JMP  R(SP)+         ; JMP TO ROUTINE LEAVING STACK AS FOUND.
42600
42700 002776 003076      EMTTAB: TYP          ; MESSAGE OUTPUT ROUTINE
42800 003078 003076      ERR          ; I/O TEST ERROR ROUTINE
42900 003080 003346      EHLT        ; UNCONDITIONAL HALT
43000 003082 003356      STLSRV     ; KEYBOARD VECTOR/PRIORITY SETUP
43100 003084 003409      STSPV     ; PRINTER VECTOR/PRIORITY SETUP
43200 003086 001412      CHARN     ; COMMON TEST EXIT
43300 003088 000720      CHLT      ; SR BIT 15 HALT
43400 003090 003164      TYPM     ; MESSAGE OUTPUT ROUTINE, MULTI DEVICES
43500 003092 003436      DLY      ; DELAY ROUTINE
43600 003094 003436      TTY1     ; CONSOLE TERMINAL CONTROL
43700 003096 003214      SCRFLF   ; CARRIAGE RETURN-LINE FEED TO ALL DL11'S
43800 003098 003142      SSCRFLF  ; CARRIAGE RETURN-LINE FEED TO CONSOLE
43900 003100 003216      LF       ; LINE FEED ONLY (TO ALL)
44000 003102 004324      PRNCR    ; PRINT CHR
44100 003104 003236      SPRHDR   ; PRINT TEST HEADER
44200 003106 004314      SPRNT    ; PRINTER READY
44300 003108 004112      SREADC   ; READ CHR
44400 003110 003640      READCR   ; READ TEST READ ROUTINE
44500 003112 003226      CR       ; CARRIAGE RETURN ONLY (TO ALL)
44600 003114 004006      SBTASC   ; BINARY TO ASCII CONVERSION
44700 003116 003562      FORDM    ; FORWARD ROUTINE ( BETWEEN TESTS )
44800 003118 003562      READC    ; READ CONSOLE KYBD ONLY
44900 003120 003972      SPARET   ; SPARE EMT
45000 003122 003972      SPARET   ; SPARE EMT
45100 003124 003972      SPARET   ; SPARE EMT
45200 003126 003972      SPARET   ; SPARE EMT
45300 003128 003972      SPARET   ; SPARE EMT
45400 003130 003972      SPARET   ; SPARE EMT

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45500 003066 003072      SPARET   ; SPARE EMT
45600 003070 003072      SPARET   ; SPARE EMT
45700 003074 000900      SPARET:  HALT        ; HALT IF TRAP TO UNDEFINED
45800 003074 000776      BR  SPARET      ; EMT IS ATTEMPTED.
45900
46000
46100
46200
46300
46400
46500
46600
46700
46800
46900
47000
47100
47200
47300
47400
47500
47600
47700
47800
47900
48000
48100 003076 010946      TYP:     MOV  R0,-(SP)      ; SAVE R0
48200 003106 015601      MOV  #2,R1          ; GET POINTER TO ADDR. OF MESG.
48300 003104 062765      ADD  #2,R1
48400 003112 011101      MOV  (R1),R1        ; ADDR. OF MESG TO R1
48500 003114 106100      MOVB (R1),R0        ; GET CHAR
48600 003116 106043      RTI  3S             ; BRANCH IF WANT AUTO CR-LF
48700 003120 001004      BNE  3S             ; PRINT CHAR IF NOT NULL
48800 003122 012600      MOV  (SP)+,R0       ; RESTORE R0
48900 003124 000902      RTI  3S             ; EXIT IF NULL CHAR
49000 003126 104913      SCRFLF  1S          ; YES, SEND CR-LF
49100 003130 000771      BR  3S             ; GET NEXT CHAR
49200 003132 104017      PRNT   1S          ; PRINTER READY?
49300 003134 110977      MOVB  R0,@TPB      ; LOAD PRINTER BUFFER WITH CHAR
49400 003140 000765      BR  1S             ; GO GET NEXT CHAR
49500
49600 003142 104017      SSCRFLF: PRNT      ; PRINTER READY?
49700 003144 112777      MOVB  #15,@TPB     ; SEND CR
49800 003152 104917      PRNT   1S          ; PRINTER READY?
49900 003154 112777      MOVB  #12,@TPB     ; SEND LF
50000 003162 000602      RTI                ; RETURN TO CALLER

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COMMON ROUTINES USED BY LA36 TESTS
50200 ;XXXXXXXXXX
50400 ;
50500 ;TYPM---MULTI TYPE-A COMMON ROUTINE TO OUTPUT
50600 ; A MESSAGE ON ALL DL11S IF THE MULTI TEST
50700 ; SWITCH (BIT 13) IS RESET. THIS ROUTINE IS USED BY
50800 ; THE PRINTER TESTS TO TYPE HEADINGS. IF A UNIT
50900 ; IS NOT READY, THE CHARACTER WILL NOT BE TYPED.
51000 ;XXXXXXXXXX
51200 003164 011601 TYPM: MOV (SP),R1 ;GET POINTER TO ADDR OF MESSG
51300 003166 062716 ADD #2,ASP ;GET CHAR
51400 003172 011101 MOV (R1),R1 ;ADDR OF MESSG TO R1
51500 003174 112100 1S: MOVB (R1)+,R0 ;GET CHAR
51600 003176 100402 BNE 2S ;BRANCH IF WANT AUTO CR-LF
51700 003200 001003 BNE 3S ;CONTINUE IF NOT NULL
51800 003202 000000 RTI ;RETURN
51900 003204 104015 2S: CRLF ;YES SEND CR-LF
52000 003206 000772 BR 1S ;GET CHAR
52100 003210 104015 3S: PRINTC ;PRINT CHAR
52200 003212 000770 BR 1S ;GO GET NEXT CHAR.
52400 003214 104022 SCR: CR ;SEND CR
52500 003216 012700 SLF: MOV #12,R0 ;SET LF CHAR
52600 003222 104015 PRINTC ;SEND IT
52700 003224 000002 RTI ;RETURN TO CALLER
52900 003226 012700 SCR: MOV #15,R0 ;SET CR CHAR
53000 003232 104015 PRINTC ;SEND IT
53100 003234 000002 RTI ;RETURN
53300 ;*****
53400 ;ROUTINE TO PRINT TEST HEADER
53500 ;*****
53700 ;*****
53800 ;*****
54000 003236 012700 000000 SPRHDR: MOV #0,R0 ;TRANSMIT
54100 003242 104015 PRINTC ;NULL CODE
54200 003244 104007 TYPEN ;PRINT MESSAGE
54300 003246 014113 MOV HDMMSG ;*****
54400 003254 006200 175362 RTNNO,R0 ;GET TEST NUMBER
54500 003256 006200 ASR R0 ;GET FIRST DIGIT
54600 003260 005200 R0 ;*****
54700 003262 042700 177770 BIT #177770,R0 ;MASK FIRST DIGIT
54800 003266 062700 ADD #60,R0 ;MAKE ASCII
54900 003272 104015 PRINTC ;PRINT DIGIT
55000 003274 016700 175336 MOV RTNNO,R0 ;GET TEST NUMBER AGAIN
55100 003276 042700 177770 BIT #177770,R0 ;MASK LAST DIGIT
55200 003304 062700 000060 ADD #60,R0 ;MAKE ASCII
55300 003310 104015 PRINTC ;PRINT DIGIT
55400 003314 104015 CRLF ;CR-LF
55500 003316 000002 RTI ;RETURN

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COMMON ROUTINES USED BY LA36 TESTS
55800 ;*****
55900 ;ERRA-- COMMON ERROR RETURN FROM I/O TESTS. HALTS
56000 ; WITH ADDRESS OF ERROR IN R0. TO CONTINUE
56100 ; ON SAME TEST BIT NOT HALTING ON ERROR
56200 ; SET THE SCOPE BIT (14) = 1 AND PRESS CONTINUE
56300 ;*****
56400 ;*****
56500 ;*****
56700 003320 032777 040000 175366 ERR: BIT #SCOPSW,@SR ;CHECK SCOPE SWITCH
56800 003326 001404 BNE 1S ;BRANCH IF NO SCOPE
56900 003330 005767 175310 TST PRCID ;SCOPING WANTED, FIRST ERROR?
57000 003334 100001 BPL 1S ;BRANCH AND HALT ON FIRST ERROR
57100 003336 100007 RTI ;SCOPE EXIT
57200 003340 052767 100000 175276 1S: BIS #BIT15,PRCID ;SET ERROR INDICATOR
57300 003346 011600 EHLT: MOV @SP,R0 ;ADDRESS OF CALL INTO R0
57400 003350 005740 TST -(R0) ;*****
57500 003352 000000 HALT ;*****
57600 003354 000002 ERRHLT: RTI ;RETURN TO TEST FOLLOWING CALL
57700 ;*****
57800 ;*****
58000 ;STLSPV--- THIS ROUTINE SETS UP KEYBOARD INTERRUPT
58100 ; VECTOR AND PRIORITY. CALLING SEQUENCE
58200 ;*****
58300 ;*****
58400 ;*****
58500 ;*****
58600 ;*****
58800 003356 017667 000000 000012 STLSPV: MOV @ (SP),STPRA+2 ;SET RETURN ADR AND VECTOR
58900 003364 062716 ADD #2,ASP ;*****
59000 003370 016701 175276 MOV TR[R1,R1 ;BRANCH AND HALT ON FIRST ERROR
59100 003374 016721 000060 STPRA: MOV #0,(R1)+ ;SCOPE EXIT
59200 003400 016721 175220 MOV TR[LVL,(R1)+ ;SET ERROR INDICATOR
59300 003404 000002 RTI ;*****
59400 ;*****
59500 ;*****
59600 ;*****
59700 ;*****
59800 ;*****
59900 ;*****
60000 ;*****
60100 ;*****
60200 ;*****
60300 ;*****
60400 ;*****
60500 003406 017667 000000 000012 STLSPV: MOV @ (SP),STPPA+2 ;SET RETURN ADR AND VECTOR
60600 003414 062716 ADD #2,ASP ;*****
60700 003420 016701 175276 MOV TR[R1,R1 ;BRANCH AND HALT ON FIRST ERROR
60800 003424 012721 000000 STPPA: MOV #0,(R1)+ ;SCOPE EXIT
60900 003430 016721 175174 MOV TR[LVL,(R1)+ ;SET ERROR INDICATOR
61000 003434 000002 RTI ;RETURN TO CALLER

```

61200
 61300
 61400
 61500
 61600
 61700
 61800
 61900
 62000
 62100
 62200
 62300
 62400
 62500
 62600
 62700
 62800
 62900
 63000
 63100
 63200
 63300
 63400
 63500
 63600
 63700
 63800
 63900
 64000 003436 010146
 64100 003440 016701 175226
 64200 003444 005301
 64300 003446 001376
 64400 003450 005300
 64500 003452 001372
 64600 003454 012601
 64700 003456 000002

```

;*****
;
;DELAY--A COMMON ROUTINE TO DELAY PROCESSING
;A GIVEN NUMBER OF MSEC.
;CALLING SEQUENCE:
;MOV #5,R0 ;R0 CONTAINS THE NUMBER OF MSEC DELAY DESIRED
;DELAY
;
;THE DELAY IS EFFECTED BY THE EXECUTION OF THE LOOP;
;LS: DEC R1
;BNE LS
;
;SINCE THE EXECUTION TIMES OF THE PDP11 LINE DOES VARY FROM
;MACHINE TO MACHINE THE VALUE AT SYMBOLIC LOCATION
;"TIMER" MUST BE CHANGED TO THE APPROPRIATE VALUE AS SHOWN BELOW
;BEFORE STARTING THE DIAGNOSTIC. "TIMER" IS INITIALIZED
;FOR AN 11/05,11/10(=251).
;
;MACHINE 05&10 35&40 15&20 LSI&03 BIPOLAR 11/45 & 11/70 MOS CORE
;
;LOOP: DEC R1 3.4 .99 2.3 -.30 -.51 .90
;BNE LOOP 2.5 1.76 2.6 -.60 -.98 1.13
;TIME= 5.9USEC 2.75 4.9 7.7 .90USEC 1.49USEC 2.03USEC
;SET TIMER 251 554 314 202 2127 1237 755
;XXXXXXXXXX
;
DLY: MOV R1, -(SP) ;SAVE R1
LS: MOV TIMER, R1 ;MOV 1 MSEC LOOP CNT TO R1
;LS: DEC R1 ;DECREMENT COUNT
;BNE LS ;BRANCH IF NOT ZERO
;DEC R0 ;DEC NO. OF MSEC DELAY
;BNE LS ;DELAY AGAIN IF NOT ZERO
;MOV (SP)+, R1 ;ALL DONE RESTORE R1
;RTI
    
```

64900
 65000
 65100
 65200
 65300
 65400
 65500

```

;*****
;
;PFAIL--POWER FAIL ROUTINE
;SAVE ALL REGISTERS AND SET RESTART ADDRESS
;INTO LOCATION 24
;
;RESTART--POWER FAIL RECOVERY
    
```

100 ; RESTORE ALL REGISTERS AND GO TO START

```

200 ;*****
300
400 003460 010946 PFAIL: MOV R0,-(SP)
500 003462 010146 MOV R1,-(SP)
600 003464 010346 MOV R2,-(SP)
700 003466 010346 MOV R3,-(SP)
800 003470 010446 MOV R4,-(SP)
900 003472 010546 MOV R5,-(SP)
1000 003474 016746 MOV R6,-(SP)
1100 003500 010667 MOV SP,SAVR6 ;SAVE STACK POSITION
1200 003504 012767 MOV #RESTRT,24 ;STORE RESTART ADDRESS
1300 003512 000900 HALT
1400 003514 000000 SAVR6: .WORD 0
1500 003516 104007 RESTRT: .TYPEM
1600 003520 003552 .S
1700 003522 016706 MOV SAVR6,SP ;RESTORE STACK POINTER
1800 003526 012667 MOV (SP)+,R4 ;RESTORE PFAIL ADDRESS
1900 003532 012605 MOV (SP)+,R5
2000 003534 012604 MOV (SP)+,R4
2100 003536 012603 MOV (SP)+,R3
2200 003540 012602 MOV (SP)+,R2
2300 003542 012601 MOV (SP)+,R1
2400 003544 012600 MOV (SP)+,R0
2500 003546 000167 JMP START
2700 003552 200 120 117 1S: .ASCIZ <ACRLF>/POWER/<ACRLF>
003555 127 105 122
003560 200 000
2800 .EVEN
    
```


3000					*****
3100					FORWARD--THIS ROUTINE TRANSFERS THE 2 OR 4 ARGUMENTS
3200					FROM THE TEST ROUTINE. THEY ARE;
3300					1- ROUTINE NUMBER
3400					2- ADDRESS OF NEXT TEST
3500					3- ITERATION COUNT (I/O TESTS ONLY)
3600					4- SCOPE ENTRY ADDRESS (I/O TESTS ONLY)
3700					*****
3800					SFORWD: MOV NXTST,R5 ;ADDR OF NEXT TEST TO R5
3900					MOV (R5),R1NNO ;GET NUMBER OF NEXT TEST
4000	003562	016705	175052		MOV (R5),NXTST ;GET ADDR OF FOLLOWING TEST
4100	003566	012567	175044		PRGID,PRGID ;CHECK IF I/O TEST
4200	003572	012567	175042		TSTB FORWDB ;SKIP THE FETCH OF ITER CNT AND SCOPE
4300	003576	105767	175042		BMI FORWDB ;SKIP THE FETCH OF ITER CNT AND SCOPE
4400	003604	012567	175050		MOV (R5),ICTR ;GET ITERATION COUNT
4500	003610	012567	175028		MOV (R5),SCOPTR ;GET SCOPE ENTRY POINT
4600	003614	016567	175056		FORWDA: MOV R5,CURTST ;ENTRY POINT TO TEST IN CUR TST
4700	003620	000002			RTI ;EXIT
4800	003622	012767	177777	175012	FORWDB: MOV #1,SCOPTR ;FORCE NO SCOPE
4900	003630	012767	000001	175022	MOV #1,ICTR ;FORCE ITERATION COUNT OF 1
5000	003636	000766			BR FORWDA

5500					*****
5600					AREAD--A ROUTINE WHICH, THROUGH THE FACILITY OF
5700					THE MAINTENANCE BIT, OUTPUTS TO THE
5800					PRINTER BUFFER AND READS THE KEYBOARD
5900					STATUS DONE IF THE DONE IS NOT SET
6000					WITHIN 600 MSEC, THE CPU WILL HALT WITH
6100					THE LOCATION OF THE ERROR IN RO. PRESS
6200					CONTINUE TO CONTINUE WITH TESTS.
6300					*****
6400					SAREAD: MOV #600,BRCTR ;SET UP 600 MSEC DELAY
6500					BIS #4,TPS ;SET MAINTENANCE BIT
6600	003640	012767	000600	175016	CLR #0,TPB ;LOAD PRINTER BUFFER
6700	003646	052777	000004	174742	1\$: TSTB @TKS ;CHECK DONE BIT
6800	003654	052777	174740		CLR #0,RO ;BRANCH IF DONE
6900	003660	105777	174726		MOV #1,RO ;DONE TO RO
7000	003664	100410			DELAY 1 MSEC
7100	003665	012760	000001		DEC BRCTR ;600 MSEC OVER
7200	003672	104010			BNE 1\$;BRANCH IF NO
7300	003674	005367	174764		2\$: RTI ;TRY AGAIN
7400	003700	001367			RTI ;RETURN TO TEST
7500	003704	104002			*****
7600	003704	000755			CONIT--THIS ROUTINE SETS UP THE DEVICE ADDRESSES
7700	003706	000002			AND INTERRUPT VECTORS FOR THE CONSOLE
7800					TERMINAL.
7900					*****
8000					CONIT: MOV CONADD,RO ;CONSOLE KEYBOARD STATUS ADDR TO RO
8100					CONSET: MOV RO,TKS ;KEYBOARD STATUS ADDRESS (777560) TO TKS
8200	003710	016700	174666		MOV (RO),RO ;INCREMENT RO BY TWO
8300	003714	010067	174672		MOV (RO),TKB ;KEYBOARD DATA ADDR (777562) TO TKB
8400	003720	005720			MOV (RO),TPSS ;INCREMENT RO BY TWO
8500	003722	010967	174666		MOV (RO),TPS ;SAVE TPS OF LAST TERMINAL
8600	003726	005720		000044	MOV (RO),TPS ;PRINTER STATUS ADDR(777564) TO TPS
8700	003730	016767	174662		MOV (RO),TPBS ;INCREMENT RO BY TWO
8800	003736	010067	174654		MOV (RO),TPB ;SAVE TPB OF LAST TERMINAL
8900	003742	005720		000032	MOV (RO),TPB ;PRINTER DATA ADDR (777566) TO TPR
9000	003744	016767	174650		MOV (RO),TPVTR ;KEYBOARD INTERRUPT VECTOR (60) TO TKVTR
9100	003752	010067	174642	174636	MOV (RO),TPVTR ;KEYBOARD INTERRUPT VECTOR (60) TO TKVTR
9200	003756	016767	174622	174636	MOV (RO),TPVTR ;KEYBOARD INTERRUPT VECTOR (60) TO TKVTR
9300	003764	016767	174614	174634	MOV (RO),TPVTR ;KEYBOARD INTERRUPT VECTOR (60) TO TKVTR
9400	003772	052767	000004	174626	ADD #4,TPVTR ;PRINTER INTERRUPT VECTOR (64) TO TPVTR
9500	003776	000207			RTS
9600					*****
9700	004002	000000			TPSS: .WORD 0 ;LAST TERM STATUS REG ADR
9800	004004	000000			TPBS: .WORD 0 ;LAST TERM BUFFER REG ADR

```

10600 ;*****
10700 ;
10800 ;BINARY TO ASCII CONVERSION (1 TO 5 ASCII CHARACTERS)
10900 ;CALLING SEQUENCE
11000 ;
11100 ;MOV ADDRESS OF LOC. TO STORE FIRST ASCII CHAR. INTO R0
11200 ;MOV BINARY NUMBER TO BE CONVERTED INTO R1
11300 ;MOV NUMBER TO BE CONVERTED AS A POWER OF TEN INTO R2
11400 ;BTOASC
11500 ;*****
11600
11700 004006 010267 000060 SBTASC: MOV R2,CNVCTR ;SAVE TEN POWER
11800 004011 006390 ;R2*2
11900 004014 062702 004100 ADD #ADTENP,R2 ;CALCULATE ADDRESS OF
12000 ;STARTING TEN POWER
12100 004020 014267 000052 1S: MOV -(R2),TENPWR ;POWER OF TEN VALUE TO TEN PWR
12200 004024 005067 000044 CLR DIGIT ;CLEAR CURRENT DIGIT
12300 004030 066701 000042 2S: SUB TENPWR,R1 ;SUBTRACT TEN POWER FROM BINARY VALUE
12400 004034 103403 BCS 3S ;BRANCH IF END
12500 004036 005267 000032 INC DIGIT
12600 004042 000779 BR 2S
12700 004044 066701 000026 3S: ADD TENPWR,R1 ;RESTORE SUBTRACTED VALUE
12800 004050 062767 000016 ADD #60,DIGIT ;CONVERT (DIGIT) TO ASCII
12900 004055 000060 MOVB DIGIT,(R0)+ ;PUT ASCII CHAR INTO USER BUFFER
13000 004062 000060 DEC CNVCTR ;FINISHED ALL CHARS. CALLED FOR
13100 004066 001354 BNE 1S ;BRANCH IF NOT FINISHED
13200 004070 000002 RTI ;YES, EXIT
13300 004074 000000 CNVCTR: .WORD 0 ;CONVERSION CHARACTER COUNT
13400 004078 000000 DIGIT: .WORD 0 ;CONVERTED CHARACTER
13500 004076 000000 TENPWR: .WORD 0 ;CURRENT TEN POWER
13600 004100 000001 000012 000144 ADTENP: .WORD 1.,10.,100.,1000.,10000.
13700 004106 001750 023420
    
```

```

13800 ;XXXXXXXXXX
13900 ;
14000 ;READ-- A COMMON ROUTINE WHICH CHECKS THE KEYBOARD
14100 ;DONE FLAG & SETS A FLAG INDICATING CHAR PARITY
14200 ;
14300 ;XXXXXXXXXX
14400
14500 004112 004767 177572 SREAD: JSR PC,CONIT ;RESET CONSOLE ADR AND VECTORS
14600 004116 005767 174534 TST DL11 ;CHECK IF MULTI DL11'S AVAILABLE
14700 004122 001430 BEQ SREADC ;NONE, WAIT FOR CONSOLE INPUT
14800 004124 016767 174526 174534 1S: MOV DL11,COUNT3 ;SET DL11 COUNT
14900 004132 016767 174474 174530 MOV FTDL,XCSR ;ADDRESS OF FIRST DL11 INTO XCSR
15000 004140 105777 174524 2S: TSTB #XCSR ;TEST IF ANY INPUT
15100 004144 100005 BPL #XCSR ;CONTINUE IF NO INPUT
15200 004146 016700 JSR PC,CONSET ;SET THIS DL11 AS CONSOLE
15300 004152 004767 174516 MOV XCSR,R0
15400 004156 000415 BR READ1 ;READ CHAR AND RETURN
15500 004160 005367 174502 3S: DEC COUNT3 ;DECREMENT DL11 COUNT
15600 004164 001404 BEQ 4S ;TEST CONSOLE WHEN DONE DL11'S
15700 004166 062767 000010 174474 ADD #10,XCSR ;NEXT DL11 ADDRESS
15800 004174 000761 BR ;CONTINUE
15900 004176 105777 174410 4S: TSTB #TKS ;CHECK CONSOLE
16000 004202 100350 BPL 1S ;WAIT, NO INPUT
16100 004204 105777 174402 SREADC: TSTR #TKS ;CHECK KEYBOARD DONE FLAG
16200 004210 100375 BPL SREAD ;BRANCH IF NOT SET
16300 004212 117767 174376 174460 READ1: MOVB #TKB,TEMPCH ;SAVE CHARACTER
16400 004220 116767 174454 174456 MOVB TEMPCH,PCHAR ;SAVE CODE WITH PARITY BIT
16500 004226 042767 174400 174450 BIC #7740,PCHAR ;MASK UNWANTED BITS
16600 004234 116767 174440 174441 MOVB TEMPCH,PARITY+1 ;SAVE CHAR WITH PARITY BIT
16700 004242 042767 177600 174430 BIC #17760,TEMPCH ;MAKE IT 7 BIT ASCII
16800 004250 026727 174424 000004 SREAD: MOV #17760,TEMPCH ;DISREGARD EOT
16900 004258 001715 BEQ SREAD
17000 004260 012700 000011 MOV #11,R0 ;SET SHIFT COUNT
17100 004264 042767 174410 1S: BIC #777,PARITY ;CLEAR PARITY FLAG
17200 004272 005306 DEC R0 ;DECREMENT SHIFT COUNT
17300 004274 008406 BEQ 2S ;EXIT IF DONE
17400 004276 106367 174401 ASLB #PARITY+1 ;SHIFT CODE
17500 004302 103373 1S: BCC 1S ;CONTINUE IF BIT WAS ZERO
17600 004304 105167 174372 COMR PARITY ;CHANGE PARITY FLAG IF BIT WAS ONE
17700 004310 000770 BR 1S ;CONTINUE
17800 004312 000002 RTI ;SET, RET. TO CALLER
17900 ;
18000 ;XXXXXXXXXX
18100 ;
18200 ;PRINT-- A COMMON ROUTINE TO CHECK THE PRINTER READY FLAG
18300 ;
18400 ;XXXXXXXXXX
18500
18600 004314 105777 174276 SPRNT: TSTB #TPS ;CHECK PRINTER READY FLAG
18700 004320 100375 BPL #SPRNT ;BRANCH IF NOT SET
18800 004322 000002 RTI ;SET, RETURN
    
```

```

19000
19100
19200
19300
19400
19500
19600
19700
19800
19900
20000
20100
20200
20300
20400
20500
20600
20700
20800
20900
21000
21100
21200
21300
21400
21500
21600
21700
21800
21900
22000
22100
22200
22300
22400
22500
22600
22700
22800
22900
23000
23100
23200
23300
23400
23500
23600
23700
23800
23900
24000
24100
24200
24300
24400
24500
24600
;*****
;PRINTC--SENDS A CHARACTER AT A TIME FIRST TO THE
;CONSOLE DL11 THEN TO ALL MULTIPLE DL11S IF
;SR BIT 13 IS = 0. IF THE REFERENCED PRINTER
;READY BIT IS NOT SET, THE CHARACTER WILL NOT BE
;SENT TO THAT PRINTER. ENTER WITH CHARACTER IN R0.
;CALL: PRINTC
;*****
SPRTC:  MOV    CONADD,TEMP    ;SET CONSOLE ADR
        ADD    #4,TEMP
        TSTR  @TEMP
        BPL  15
        ADD  #2,TEMP
        MOV   R0,@TEMP
        BIT  #RT13,@SR
        BNE  25
        TST  DLCNT
        BNE  18S
        JMP  18S
        MOV   DLCNT,COUNT3
        MOV   FSTDR,XCSR
        TSTR  INCHK
        BNE  13S
        CMP  RTNNO,#20
        BGE  5S
        BCS  #7VCTL,WAITF
        BNE  13S
        TSTR  @XCSR
        BPL  13S
        ADD  #2,XCSR
        MOV   @XCSR,TEMPCH
        BIC  #177600,TEMPCH
        CMP  TEMPCH,#3
        BNE  6S
        CMP  RTNNO,#24
        BNE  6S
        JMP  24S
        CMP  TEMPCH,#177
        BEQ  9S
        CMP  RTNNO,#17
        BNE  7S
        MOV   TEMPCH,R3
        BR   12S
        CMP  RTNNO,#21
        BNE  14S
        MOV   TEMPCH,REPT
        BR   12S
        CMP  RTNNO,#22
        BNE  14S
        MOV   TEMPCH,REPT
        BR   12S
        CMP  RTNNO,#21
        BNE  10S
        POPSP2
;*****
;SET CONSOLE ADR
;WAIT FOR CONSOLE READY
;LOAD CONSOLE PRINTER BUFFER
;CHECK SW 13
;SEND ALL TERMS IF SW13 DOWN
;CHECK FOR MULTIPLE DL11'S
;CHECK FOR INPUT IF THERE
;PUT NO. DL11'S INTO COUNT3
;ADDR OF FIRST DL INTO XCSR
;CHECK FOR INPUT?
;PRINTING TEST?
;BRANCH IF NOT
;KEYBOARD CONTROL?
;SKIP INPUT CHECK IF NOT
;TEST IF ANY INPUT
;CONTINUE IF NO INPUT
;SET BUFFER ADDRESS
;CHECK IF CONTROL-C
;CONTINUE IF NOT
;CHECK IF TEST 24
;CONTINUE IF NOT CONTROL-C
;CHECK IF RBOUOT
;YES, CHECK TEST NUMBER
;TEST 17?
;BRANCH IF NOT
;SAVE CHARACTER
;CONTINUE
;TEST 21?
;BRANCH IF NOT
;SAVE CHARACTER
;CONTINUE
;TEST 22?
;CONTINUE IF NOT
;SAVE CHARACTER
;CONTINUE
;CHECK IF TEST 21
;NO, CHECK IF TEST 22
;ADJUST STACK

```

```

24700
24800
24900
25000
25100
25200
25300
25400
25500
25600
25700
25800
25900
26000
26100
26200
26300
26400
26500
26600
26700
26800
26900
27000
27100
27200
27300
27400
27500
27600
27700
27800
27900
28000
28100
28200
28300
28400
28500
28600
28700
28800
28900
29000
29100
29200
29300
29400
29500
29600
29700
29800
29900
30000
30100
30200
30300
MOV    #30.,R0
DELAY
TYPEM
ECCEND
CHAIN
JMP   E021A
CME  RTNNO,#22
BNE  11S
POPSP2
MOV    #30.,R0
DELAY
TYPEM
ECCEND
CHAIN
JMP   E022A
CMP  RTNNO,#24
BNE  22S
POPSP2
JMP   TERM
MOV   #30.,R0
DELAY
MOV   TEMPCH,R0
BR   14S
ADD  #2,XCSR
ADD  #2,XCSR
MOV   CONADD,TEMP
ADD  #4,TEMP
CMP  TEMP,XCSR
BEQ  17S
TSTR  @XCSR
BPL  15S
ADD  #2,XCSR
MOV   R0,@XCSR
DEC  COUNT3
BEQ  18S
ADD  #2,XCSR
JMP  4S
BR   16S
TSTR  INCHK
BNE  26S
CMP  RTNNO,#20
BGE  19S
BCS  #7VCTL,WAITF
BNE  26S
TSTR  @CONADD
BPL  26S
MOV   CONADD,TEMP
ADD  #2,TEMP
MOV   @TEMP,TEMPCH
BIC  #177600,TEMPCH
CMP  TEMPCH,#3
BNE  21S
CMP  RTNNO,#24
BNE  21S
MOV   #30.,R0
DELAY
;DELAY FOR HALF DUPLEX
;YES, TEST 21
;PRINT TERMINATION MESSAGE
;CHAIN TO NEXT TEST
;REPEAT TEST IF LOOP ON TEST SW SET
;CHECK IF TEST 22
;CHECK IF TEST 24
;ADJUST STACK
;DELAY FOR HALF DUPLEX
;YES, PRINT TERMINATION MESSAGE
;CHAIN TO NEXT TEST
;REPEAT TEST IF LOOP ON TEST SW SET
;TEST 24?
;WAIT FOR NEXT TEST IF NOT TEST 24
;RESET STACK
;TERMINATE TEST
;DELAY FOR HALF DUPLEX
;SET NEW CHARACTER
;CONTINUE
;SET STATUS ADDRESS IN XCSR
;CHECK IF CONSOLE TERMINAL
;IS THIS DL
;TEST PRINTER READY
;WAIT FOR READY
;SET XCSR TO PRINTER BUFFER
;LOAD CHARACTER INTO BUFFER
;DECREASE COUNT OF DL11'S
;ALL DONE, EXIT
;SET XCSR TO NEXT DL11 PRINTER STATUS
;DO TEST NEXT DL11 READY FLAG
;SET XCSR TO PRINTER BUFFER
;DO NOT LOAD BUFFER
;WANT INPUT CHECK?
;NO, BRANCH
;PRINTING TEST?
;BRANCH IF NOT
;KEYBOARD CONTROL?
;SKIP INPUT CHECK IF NOT
;TEST IF ANY INPUT
;BRANCH IF NONE
;SET ADR
;MASK UNWANTED BITS
;CHARACTER = CONTROL-C?
;CONTINUE IF NOT
;TEST 24?
;CONTINUE IF NOT
;DELAY FOR HALF DUPLEX

```

```
30400 005146 104812          CRLF          ;SEND CR-LF
30500 005150 022826          POPSP2       ;RESET STACK
30600 005152 000167          JMP          EQ24B ;RETURN TO TEST
30700 005156 026727          CMP          TEMPCH,#177 ;CHECK IF RUBOUT
30800 005164 001006          BNE          235 ;BRANCH IF NO
30900 005166 000607          BR          95 ;
31000 005170 012767          MOV          #1,CNTLSW ;CLEAR LOOP AND SEQUENCE BITS
31100 005176 000167          JMP          174660 ;GO WAIT FOR NEXT TEST
31200 005202 010046          MOV          R0,-(SP) ;SAVE R0
31300 005204 012700          MOV          #30.,R0 ;DELAY FOR HALF DUPLEX
31400 005210 104010          DELAY ;
31500 005212 012500          MOV ;
31600 005214 173416          CMP          R17 ;CHECK IF TEST 17
31700 005222 001002          BNE          245 ;BRANCH IF NOT TEST 17
31800 005224 016703          MOV          TEMPCH,R3 ;STORE INPUTTED CHARACTER
31900 005230 026727          CMP          R17NO,#21 ;CHECK IF TEST 21
32000 005236 001003          BNE          255 ;BRANCH IF NOT TEST 21
32100 005240 016767          MOV          TEMPCH,REPT ;STORE INPUTTED CHARACTER
32200 005246 026727          CMP          R17NO,#22 ;CHECK IF TEST 22
32300 005254 001003          BNE          265 ;BRANCH IF NOT TEST 22
32400 005256 016767          MOV          TEMPCH,REPT ;STORE INPUTTED CHARACTER
32500 005264 000002          RTI          ;RETURN TO TEST
32600
```

32800

I/O LOGIC TESTS

.SBTTL I/O LOGIC TESTS

```

100
200
300
400
500
600
700
800
900
1000
1100
1200
1300
1400
1500
1600
1700
1800
1900
2000
2100
2200 005266 000040
2300 005270 005320
2400 005272 000012
2500 005274 005304
2600 005276 012767 005314 172500
2700 005300 005777 173302
2800 005310 104005
2900 005312 000774
3000 005314 104001
3100 005316 000774
3200
3300
3400
3500
3600
3700
3800 005320 000041
3900 005322 005353
4000 005324 000012
4100 005326 005336
4200 005330 012767 005346 172446
4300 005336 005777 173252
4400 005342 104005
4500 005344 000774
4600 005346 104001
4700 005350 000774

;*****
;ONLY THE CONSOLE TERMINAL IS TESTED.
;UPON COMPLETION, THE CPU WILL EITHER HALT IF SR
;BITS IS = 1 AND AWAIT FUTURE INSTRUCTIONS OR CONTINUE
;AND EXECUTE THE PRINTER TESTS CONTINUOUSLY
;IF AN I/O TEST FAILS, THE CPU WILL HALT AT ERRHLT
;WITH THE ADDRESS OF THE ERROR IN RO (LOC 77700). PRESSING
;THE CONTINUE SWITCH WILL CAUSE THE I/O TEST TO
;CONTINUE WITH THE NEXT TEST. HOWEVER IF SWITCH 14
;WERE SET, OR IS SET BEFORE THE CONTINUE SWITCH IS
;PRESSED, THE FAILED TEST WILL LOOP ON ITSELF
;WITHOUT FURTHER HALTS
;*****
;ATO-- TEST #40--TESTS THE ABILITY TO REFERENCE THE
;RECEIVER STATUS WORD (TKS) WITHOUT TRAPPING.
;*****
ATO: 40 ;TEST NUMBER
ATX: A71 ;NEXT TEST
10- ;ITERATION COUNT
1S ;SCOPE ENTRY
MOV #3$,MACHERR ;SET UP MACHINE ERROR TRAP
@TKS ;REFERENCE RECEIVER STATUS WORD
2S: CHAIN ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
3S: ERROR 1S ;ERROR TRAPPED WHEN REFERENCING
BR 2S ;RECEIVER STATUS WORD (TKS)

;*****
;AT1--TEST #41--TESTS THE ABILITY TO REFERENCE THE
;RECEIVER BUFFER (TKB) WITHOUT TRAPPING.
;*****
AT1: 41 ;TEST NUMBER
A72 ;NEXT TEST
10- ;ITERATION COUNT
1S ;SCOPE ENTRY
MOV #3$,MACHERR ;SET UP MACHINE ERROR TRAP
@TKB ;REFERENCE RECEIVER BUFFER
2S: CHAIN ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
3S: ERROR 1S ;TRAPPED WHEN REFERENCING
BR 2S ;RECEIVER BUFFER (TKB)

```

I/O LOGIC TESTS

.SBTTL I/O LOGIC TESTS

```

4900
5000
5100
5200
5300
5400 005352 000042
5500 005354 005404
5600 005356 005412
5700 005360 005376
5800 005362 012767 005400 172414
5900 005370 005777 173222
6000 005374 104005
6100 005376 000774
6200 005400 104001
6300 005402 000774
6400
6500
6600
6700
6800
6900
7000 005404 000043
7100 005406 005436
7200 005410 000012
7300 005412 005422
7400 005414 012767 005432 172362
7500 005422 005777 173172
7600 005426 104005
7700 005430 000774
7800 005432 104001
7900 005434 000774

;*****
;AT2--TEST #42--TESTS THE ABILITY TO REFERENCE THE
;TRANSMITTER STATUS WORD (TPS) WITHOUT TRAPPING.
;*****
AT2: 42 ;TEST NUMBER
AT3 ;NEXT TEST
10- ;ITERATION COUNT
1S ;SCOPE ENTRY
MOV #3$,MACHERR ;SET UP MACHINE ERROR TRAP
@TPS ;REFERENCE TRANSMITTER STATUS
2S: CHAIN ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
3S: ERROR 1S ;TRAPPED WHEN REFERENCING
BR 2S ;TRANSMITTER STATUS WORD

;*****
;AT3-- TEST #43--TESTS THE ABILITY TO REFERENCE THE
;TRANSMITTER BUFFER (TPB) WITHOUT TRAPPING.
;*****
AT3: 43 ;TEST NUMBER
AT4 ;NEXT TEST
10- ;ITERATION COUNT
1S ;SCOPE ENTRY
MOV #3$,MACHERR ;SET UP ERROR TRAP
@TPB ;REFERENCE TRANSMITTER BUFFER
2S: CHAIN ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
3S: ERROR 1S ;TRAPPED WHEN REFERENCING
BR 2S ;TRANSMITTER BUFFER.

```

```

I/O LOGIC TESTS
*****
;AT4-- TEST #44--TESTS THE ABILITY TO SET AND CLEAR THE
;RECEIVER INTERRUPT ENABLE BIT.
*****
      8100 ;*****
      8200 ;AT4-- TEST #44--TESTS THE ABILITY TO SET AND CLEAR THE
      8300 ;RECEIVER INTERRUPT ENABLE BIT.
      8400 ;*****
      8500
      8600 005436 000044 AT4: 44 ;TEST NUMBER
      8700 005440 005526 AT5 ;NEXT TEST
      8800 005442 000012 10 ;ITERATION COUNT
      8900 005444 005460 10 ;SCOPE ENTRY
      9000 005446 012746 000340 MOV #PRTV7,-(SP) ;SET PRIORITY 7
      9100 005452 012746 005460 MOV #10,-(SP)
      9200 005456 000000 RTI ;SET INTERRUPT ENABLE BIT
      9300 005460 052777 000100 173124 1S: BIT #BIT6,@TKS ;CHECK IF BIT IS SET
      9400 005466 032777 000100 173116 BIT #BIT6,@TKS ;BRANCH IF SET
      9500 005474 001002 BNE ;NOT SET, ERROR
      9600 005476 104001 BR ;CHAIN TO NEXT TEST
      9700 005500 000410 ERROR 3S ;NOT SET, ERROR
      9800 005502 042777 000100 173102 BIC #BIT6,@TKS ;CLEAR INTERRUPT ENABLE BIT
      9900 005510 032777 000100 173074 BIT #BIT6,@TKS ;CHECK IF BIT IS CLEARED
      10000 005516 001401 BEQ 5S ;BRANCH IF CLEARED
      10100 005520 104001 ERROR 4S ;NOT CLEARED, ERROR
      10200 005522 104005 5S: CHAIN ;CHAIN TO NEXT TEST
      10300 005524 000755 BR 1S ;DO TEST AGAIN
      10400
      10500
      10600 ;*****
      10700 ;AT5-- TEST #45--CHECKS THAT THE RECEIVER INTERRUPT
      10800 ;ENABLE BIT CAN BE CLEARED WITH RESET INSTRUCTION.
      10900 ;*****
      11000
      11100 005526 000045 AT5: 45 ;TEST NUMBER
      11200 005530 005504 AT6 ;NEXT TEST
      11300 005532 000012 10 ;ITERATION COUNT
      11400 005534 005550 10 ;SCOPE ENTRY
      11500 005536 012746 000340 MOV #PRTV7,-(SP) ;SET PRIORITY TO 7
      11600 005542 012746 005550 MOV #10,-(SP)
      11700 005546 000000 RTI ;SET INTERRUPT ENABLE BIT
      11800 005548 052777 000100 173034 1S: BIT #BIT6,@TKS ;BE SURE PRINTER IS DONE WITH DL11S1 MESSAGE
      11900 005556 105777 173034 3S: TSTB @TPS ;BEFORE ALLOWING FOLLOWING RESET.
      12000 005562 001775 BEQ 3S ;RESET
      12100 005564 000005 RESET ;TEST INTERRUPT ENABLE BIT
      12200 005574 001401 BEQ #BIT6,@TKS ;BRANCH IF CLEARED
      12300 005576 104001 ERROR 2S ;STILL SET, ERROR
      12400 005600 104005 CHAIN ;CHAIN TO NEXT ROUTINE
      12500 005602 000762 BR 1S ;REPEAT TEST

```

```

I/O LOGIC TESTS
*****
;AT6-- TEST#46--TESTS THE ABILITY TO SET AND CLEAR
;TRANSMITTER INTERRUPT ENABLE BIT.
*****
      12700 ;*****
      12800 ;AT6-- TEST#46--TESTS THE ABILITY TO SET AND CLEAR
      12900 ;TRANSMITTER INTERRUPT ENABLE BIT.
      13000 ;*****
      13100
      13200 005604 000046 AT6: 46 ;TEST NUMBER
      13300 005606 005674 AT7 ;NEXT TEST
      13400 005610 000012 10 ;ITERATION COUNT
      13500 005612 005626 10 ;SCOPE ENTRY
      13600 005614 012746 000340 MOV #PRTV7,-(SP) ;SET PRIORITY TO 7
      13700 005620 012746 005626 MOV #10,-(SP)
      13800 005624 000000 RTI ;SET INTERRUPT ENABLE BIT
      13900 005626 052777 000100 172762 1S: BIT #BIT6,@TPS ;CHECK THAT BIT IS SET
      14000 005634 032777 000100 172754 BIT #BIT6,@TPS ;BRANCH IF SET
      14100 005642 001002 BNE ;NOT SET, ERROR
      14200 005644 104001 BR ;CHAIN TO NEXT TEST
      14300 005646 000410 ERROR 2S ;NOT SET, ERROR
      14400 005650 042777 000100 172740 BIC #BIT6,@TPS ;CLEAR INTERRUPT ENABLE BIT
      14500 005656 032777 000100 172732 BIT #BIT6,@TPS ;CHECK IF BIT IS CLEARED
      14600 005664 001401 BEQ 3S ;BRANCH IF CLEARED
      14700 005666 104001 ERROR 3S ;NOT CLEARED, ERROR
      14800 005670 104005 CHAIN ;CHAIN TO NEXT TEST
      14900 005672 000755 BR 1S ;DO AGAIN
      15000
      15100 ;*****
      15200 ;AT7-- TEST #47--TESTS THE ABILITY TO CLEAR TRANSMITTER
      15300 ;INTERRUPT ENABLE BIT WITH RESET INSTRUCTION.
      15400 ;*****
      15500
      15600 005674 000047 AT7: 47 ;TEST NUMBER
      15700 005676 005744 AT10 ;NEXT TEST
      15800 005700 000012 10 ;ITERATION COUNT
      15900 005702 005716 10 ;SCOPE ENTRY
      16000 005704 012746 000340 MOV #PRTV7,-(SP) ;SET PRIORITY TO 7
      16100 005710 012746 005716 MOV #10,-(SP)
      16200 005712 000000 RTI ;SET INTERRUPT BIT
      16300 005714 052777 000100 172672 1S: RESET #BIT6,@TPS ;CHECK IF BIT IS CLEARED
      16400 005724 000005 BIT #BIT6,@TPS ;BRANCH IF CLEARED
      16500 005726 032777 000100 172662 BEQ 2S ;ERROR, RESET DID NOT CLEAR BIT
      16600 005734 001401 ERROR ;CHAIN TO NEXT ROUTINE
      16700 005740 104005 CHAIN ;CHAIN TO NEXT ROUTINE
      16800 005742 000765 BR 1S ;REPEAT TEST

```

```

I/O LOGIC TESTS
17100
17200
17300
17400
17500
17600 005744 000050
17700 005746 006002
17800 005750 006012
17900 005752 005762
18000 005754 032777 001000 172732 1S: BIT #LSI11,@SR
18100 005762 001005 2S: BNE
18200 005764 000005 RESET
18300 005766 105777 172624 TESTB @TPS
18400 005772 100401 BMI
18500 005774 104001 ERROR
18600 005776 104005 CHAIN
18700 006000 000765 BR 1S
;*****
;AT10-- TEST #50--CHECKS THAT RESET SETS THE TRANSMITTER
;READY BIT AND THAT THE READY BIT CAN BE READ RELIABLY.
;*****
AT10: 50 ;TEST NUMBER
AT11 ;NEXT TEST
10 ;ITERATION COUNT
1S ;SCOPE ENTRY
BIT #LSI11,@SR ;SKIP TEST IF AN LSI-11
2S ;
BNE ;
RESET ;RESET
TESTB @TPS ;CHECK TRANSMIT READY BIT
BMI ;BRANCH IF SET
ERROR ;ERROR, RESET DID NOT SET READY BIT
CHAIN ;CHAIN TO NEXT TEST
BR 1S ;DO AGAIN
;*****
;AT11-- TEST #51--TESTS THAT THE TRANSMITTER READY RESETS
;BY LOADING THE TRANSMITTER BUFFER.
;*****
AT11: 51 ;TEST NUMBER
AT12 ;NEXT TEST
10 ;ITERATION COUNT
1S ;SCOPE ENTRY
MOV #226,R0 ;DELAY 150 MSEC.
DELAY ;RESET
RESET ;LOAD TRANSMITTER BUFFER
CLR @TPB ;CHECK TRANSMIT READY BIT
TESTB @TPS ;BRANCH IF CLEARED
BPL 2S ;NOT CLEARED, ERROR
ERROR ;CHAIN TO NEXT TEST
CHAIN ;REPEAT TEST
BR 1S ;

```

```

I/O LOGIC TESTS
20800
20900
21000
21100
21200
21300 006042 000052
21400 006044 005772
21500 006046 006012
21600 006050 006056
21700 006052 104004
21800 006054 006112
21900 006056 000005
22000 006060 005077 172532
22100 006064 005046 006074
22200 006066 012746
22300 006072 000002 000100 172514
22400 006074 052777
22500 006102 000240
22600 006104 104001
22700 006106 104005
22800 006110 000762
22900 006112 022572
23000 006114 000774
23100
23200
23300
23400
23500
23600
23700 006116 000035
23800 006120 005772
23900 006122 006012
24000 006124 006132
24100 006126 104004
24200 006130 006170
24300 006132 012746 172472
24400 006136 012746 006144
24500 006142 000002
24600 006144 005077 172446
24700 006150 052777 006100 172440
24800 006156 000240
24900 006160 005077 172432
25000 006164 104005
25100 006166 000761
25200 006170 022626
25300 006172 104001
25400 006174 000771
;*****
;AT12-- TEST #52--CHECKS THAT THE TRANSMIT READY BIT CAN
;CAUSE AN INTERRUPT
;*****
AT12: 52 ;TEST NUMBER
AT13 ;NEXT TEST
10 ;ITERATION COUNT
1S ;SCOPE ENTRY
STPCHV ;SET UP TRANSMITTER INTERRUPT VECTOR
TO 4S ;
;SEE CHAIN COMMENT
RESET ;DISABLE TRANSMIT INTERRUPT
CLR -(SP) ;SET PRIORITY TO ZERO
MOV #2S,-(SP)
RTI
2S: BTR #BIT6,@TPS ;ENABLE TRANSMIT INTERRUPT
NOP
ERROR ;TRANSMIT READY DID NOT CAUSE INTERRUPT
CHAIN ;CHAIN TO NEXT TEST
3S: BR 1S ;REPEAT TEST
4S: POPSP2 3S ;INTERRUPT OCCURRED, CLEAN STACK
;CHAIN TO NEXT TEST
;*****
;AT13-- TEST #53--TESTS THAT THE TRANSMIT READY DOES NOT CAUSE AN
;INTERRUPT WHEN THE PROCESSOR IS AT THE SAME LEVEL
;*****
AT13: 3S ;TEST NUMBER
AT14 ;NEXT TEST
10 ;ITERATION COUNT
1S ;SCOPE ENTRY
STPCHV ;SET UP TRANSMIT INTERRUPT
VECTOR TO 4S ;SET PROCESSOR TO SAME LEVEL AS XMITTER
MOV TPLVL,-(SP)
MOV #2S,-(SP)
2S: CLR @TPS ;DISABLE TRANSMITTER INTERRUPTS
BTR #BIT6,@TPS ;ENABLE TRANSMITTER INTERRUPTS
NOP
3S: CLR @TPS ;OK, NO INTERRUPT OCCURRED
CHAIN ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
4S: POPSP2 ;INTERRUPT OCCURRED,ERROR,CLEAN
;UP STACK
;CHAIN TO NEXT TEST

```

```

I/O LOGIC TESTS
25600
25700
25800
25900
26000
26100
26200 006176 000054
26300 006200 006262
26400 006202 000012
26500 006204 006212
26600 006306 104004
26700 006310 006250
26800 006212 005077 172400
26900 006216 016746 172406
27000 006372 162716 000040
27100 006226 012746 008234
27200 006232 000002
27300 006234 052777 000100 172354 25:
27400 006342 000240
27500 006244 104001
27600 006246 000401
27700 006250 002620
27800 006252 000002 172340
27900 006256 104005
28000 006260 000754

;*****
;AT14-- TEST#54--TESTS THAT THE TRANSMIT READY DOES CAUSE AN
; INTERRUPT WHEN THE PROCESSOR IS AT A PRIORITY LEVEL
; LOWER THAN THE TRANSMIT INTERRUPT REQUEST LEVEL
;*****
AT14: 54 ;TEST NUMBER
      AT15 ;NEXT TEST
      10- ;ITERATION COUNT
      1 ;SCOPE ENTRY
      STPCHV ;SET UP TRANSMIT INTERRUPT
      3 ;VECTOR TO 35
      CLR @TPS ;DISABLE TRANSMIT INTERRUPTS
      TPLVL,-(SP) ;SET PROCESSOR PRIORITY ONE
      SUB #40,(SP) ;LEVEL LOWER THAN TRANSMITTER
      MOV #25,-(SP)
      RTI
      BLS #BIT6,@TPS ;ENABLE TRANSMITTER INTERRUPTS
      NOP
      ERROR ;NO INTERRUPT, ERROR
      BR 45 ;CHAIN TO NEXT TEST
      POPSP2 ;INTERRUPT OCCURED, OK, CLEAN STACK
      45: @TPS ;DISABLE TRANSMITTER INTERRUPTS
      CHAIN ;CHAIN TO NEXT TEST
      BR 15 ;REPEAT TEST

```

```

I/O LOGIC TESTS
28200
28300
28400
28500
28600
28700
28800 006262 000055
28900 006264 006362
29000 006266 000012
29100 006270 006272
29200 006272 104004
29300 006274 006334
29400 006276 005077 172314
29500 006302 005046
29600 006304 012746 006312
29700 006310 000002
29800 006312 052777 000100 172276 25:
29900 006320 000240
30000 006322 104001
30100 006324 005077 172266
30200 006330 104005
30300 006332 0000757
30400 006334 012777 006354 172264 45:
30500 006342 012716 006350
30600 006346 000002
30700 006350 000240
30800 006352 000764
30900 006354 022526
31000 006356 104001
31100 006360 000761
31200
31300
31400
31500
31600
31700 006362 000056
31800 006364 006430
31900 006366 000012
32000 006370 006372
32100 006372 032776 001000 172314 15:
32200 006400 001011
32300 006402 012700 000226
32400 006406 104010
32500 006410 104021
32600 006412 000005
32700 006414 105777 172172
32800 006420 100001
32900 006422 104005
33000 006424 104005
33100 006426 000761

;*****
;AT15-- TEST#55--TESTS THAT THE TRANSMIT READY DOES NOT
; REINTERRUPT AFTER AN RTI WHEN THE READY BIT HAS
; BEEN RESET.
;*****
AT15: 55 ;TEST NUMBER
      AT16 ;NEXT TEST
      10- ;ITERATION COUNT
      1 ;SCOPE ENTRY
      STPCHV ;SET TRANSMIT INTERRUPT VECTOR
      45 ;TO 45
      CLR @TPS ;DISABLE TRANSMITTER INTERRUPTS
      CLR -(SP) ;SET PROCESSOR PRIORITY TO ZERO
      MOV #25,-(SP)
      RTI
      BLS #BIT6,@TPS ;ENABLE TRANSMITTER INTERRUPTS
      NOP
      ERROR ;ERROR1, TRANSMITTER FAILED TO INTERRUPT
      CLR @TPS ;DISABLE TRANSMITTER INTERRUPTS
      CHAIN ;CHAIN TO NEXT TEST
      RR 15 ;REPEAT TEST
      MOV #6,@TPVTR ;INTERRUPT OCCURED, CHANGE INTERRUPT
      MOV #5,@RSP ;VECTOR TO 65 AND RETURN TO 55
      RTI ;RETURN FROM INTERRUPT
      BR 35
      55: NOP 35 ;CHAIN TO NEXT TEST
      65: POPSP2 35 ;ERROR2, TRANSMITTER REINTERRUPTED
      ERROR ;AFTER RTI WITH READY BIT LEFT ON.
      BR 35 ;CLEAN STACK, CHAIN TO NEXT TEST.

;*****
;AT16--TEST#56--CHECKS THAT RESET CLEARS THE RECEIVER DONE BIT
;*****
AT16: 56 ;TEST NUMBER
      AT17 ;NEXT TEST
      10- ;ITERATION COUNT
      1 ;SCOPE ENTRY
      BIT #LSI11,@SR ;SKIP TEST IF LSI-11
      BNE 35
      MOV #226,R0
      25: DELAY 150 MSEC
      AHEAD ;ENABLE RECEIVER
      RESET ;RESET
      TSTB @TKS ;TEST DONE BIT
      BPL 35 ;BRANCH IF DONE IS CLEARED
      ERROR ;NOT CLEARED, ERROR
      CHAIN ;CHAIN TO NEXT TEST
      RR 15 ;REPEAT TEST

```



```

I/O LOGIC TESTS
33300
33400
33500
33600
33700
33800 006430 000057
33900 006432 006500
34000 006434 000012
34100 006436 006436
34200 006440 032777 001000 172246 1$:
34300 006446 001912
34400 006450 012700 000226
34500 006454 104010
34600 006456 104021
34700 006460 105777 172130
34800 006464 105777 172122
34900 006470 100001
35000 006472 104001
35100 006474 104005
35200 006476 000760
35300
35400
35500
35600
35700
35800
35900 006500 000060
36000 006502 006572
36100 006504 000012
36200 006506 006523
36300 006510 104021
36400 006512 006564
36500 006514 032777 001000 172172 1$:
36600 006524 001912 000226
36700 006526 012700
36800 006530 104010
36900 006532 104021
37000 006536 005977 172052
37100 006540 005977
37200 006542 012746 006550
37300 006546 000002
37400 006550 052777 000100 172034 3$:
37500 006552 000240
37600 006560 104001
37700 006562 000401
37800 006564 022626
37900 006566 104005
38000 006570 000751

;*****
;AT17-- TEST#57--CHECKS THAT REFERENCING THE RECEIVER BUFFER
;CLARS THE DONE BIT.
;*****
AT17: 57 ;TEST NUMBER
AT20 ;NEXT TEST
10- ;ITERATION COUNT
1$ ;SCOPE ENTRY
BIT #LSI11,ASR ;CHECK FOR LSI-11
BNE 3$ ;SKIP TEST IF SET
MOV #226,R0
2$: DELAY 150 MSEC
AREAD ;ENABLE RECEIVER
TSTB @TKR ;REFERENCE RECEIVER BUFFER
TSTB @TKS ;TEST DONE BIT
RPL 3$ ;BRANCH IF NOT SET
3$: ERROR ;DONE BIT IS SET, ERROR
CHAIN 1$ ;CHAIN TO NEXT TEST
BR ;REPEAT TEST

;*****
;AT20-- TEST#60--CHECK THAT THE RECEIVER DONE BIT IS ABLE TO
;CAUSE AN INTERRUPT.
;*****
AT20: 60 ;TEST NUMBER
AT21 ;NEXT TEST
10- ;ITERATION COUNT
1$ ;SCOPE ENTRY
STRDRV ;SET UP RECEIVER INTERRUPT
4$ ;VECTOR TO 4$
BIT #LSI11,ASR ;CHECK FOR LSI-11
BNE 5$ ;SKIP TEST IF SET
MOV #226,R0
2$: DELAY 150 MSEC
AREAD ;ENABLE RECEIVER
CLR @TKS ;DISABLE RECEIVER INTERRUPTS
MOV -(SP) ;SET PROCESS STATUS TO ZERO
MOV #3$,-(SP)
RTI
3$: BIT #BIT6,@TKS ;ENABLE RECEIVER INTERRUPT
NOP ;ERROR, RECEIVER FAILED TO INTERRUPT
ERROR ;CHAIN TO NEXT TEST
BR 5$ ;OK, CLEAN STACK
4$: CHAIN ;CHAIN TO NEXT TEST
5$: BR 1$ ;REPEAT TEST

```

```

I/O LOGIC TESTS
38200
38300
38400
38500
38600
38700
38800 006572 000061
38900 006574 006572
39000 006576 000012
39100 006600 006606
39200 006602 104003
39300 006604 032777 001000 172100 1$:
39400 006614 001917 000226
39500 006616 012700
39600 006624 104010
39700 006626 104021
39800 006628 005977 171760
39900 006632 015746 171766
40000 006636 015746 006644
40100 006642 000002
40200 006644 052777 000100 171740 3$:
40300 006654 006240 171732
40400 006656 005977
40500 006660 104005
40600 006662 000751
40700 006664 022626
40800 006666 104001
40900 006668 000751
41000 006670 000771

;*****
;AT21-- TEST#61--TESTS THAT THE RECEIVER DONE DOES NOT CAUSE AN
;INTERRUPT WHEN THE PROCESSOR IS AT THE SAME LEVEL AS
;THE RECEIVER'S INTERRUPT REQUEST LEVEL.
;*****
AT21: 61 ;TEST NUMBER
AT22 ;NEXT TEST
10- ;ITERATION COUNT
1$ ;SCOPE ENTRY
STRDRV ;SET RECEIVER VECTOR TO 5$
5$ ;
BIT #LSI11,ASR ;CHECK FOR LSI-11
BNE 4$ ;SKIP TEST IF SET
MOV #226,R0
2$: DELAY 150 MSEC
AREAD ;ENABLE RECEIVER
CLR @TKS ;ENABLE RECEIVER INTERRUPTS
MOV TKLVL,-(SP) ;SET PROCESSOR PRIORITY TO SAME LEVEL AS RECEIVER
MOV #3$,-(SP)
RTI
3$: BIT #BIT6,@TKS ;ENABLE RECEIVER INTERRUPTS
NOP ;OK, NO INTERRUPT OCCURRED
CHAIN 1$ ;CHAIN TO NEXT TEST
BR ;REPEAT TEST
4$: CHAIN ;CHAIN TO NEXT TEST
5$: ERROR ;ERROR, RECEIVER INTERRUPTED, CLEAN STACK
BR 4$ ;BRANCH 4$

```

```

I/O LOGIC TESTS
41200 ;*****
41300 ;AT22-- TEST#62--TESTS THAT THE RECEIVER DONE DOES CAUSE AN
41400 ; INTERRUPT WHEN THE PROCESSOR IS AT A PRIORITY ONE
41500 ; LEVEL LOWER THAN THE RECEIVER'S INTERRUPT
41600 ; REQUEST LEVEL
41700 ;*****
41800
41900 006672 000062 AT22: 62 ;TEST NUMBER
42000 006674 007006 ;NEXT TEST
42100 006676 000012 ;ITERATION COUNT
42200 006700 006706 ;SCOPE ENTRY
42300 006702 004003 ;SET RECEIVER INTERRUPT
42400 006704 006768 ;VECTOR TO 4S
42500 006706 032777 001000 172000 1S: BIT #LSI11,ASR ;CHECK FOR LSI11
42600 006714 001725 ;BNE #226,R0 ;SKIP TEST IF SET
42700 006716 012700 000226 ;MOV #226,R0
42800 006722 104010 ;DELAY 150 MSEC
42900 006724 104021 ;AREAD ;ENABLE RECEIVER
43000 006726 005077 171660 2S: CLR ;DISABLE RECEIVER INTERRUPTS
43100 006732 016746 171666 ;MOV @TKS, -(SP) ;DISABLE READER INTERRUPTS
43200 006736 012746 006744 ;MOV #35, -(SP) ;SET PROCESSOR PRIORITY ONE LEVEL
43300 006742 000002 ;RTI
43400 006744 162797 000040 171234 3S: SUB #40,PSW ;LOWER THAN READER
43500 006752 052777 000100 171632 ;BIS #B16,@TKS ;ENABLE INTERRUPTS
43600 ;NOP
43700 ;ERROR ;NO INTERRUPT, ERROR
43800 ;BR 5S ;CHAIN TO NEXT TEST
43900 ;POPSP2 5S ;CLEAN STACK
44000 ;CLR @TKS ;DISABLE RECEIVER INTERRUPTS
44100 ;CHAIN 5S ;CHAIN TO NEXT TEST
44200 006776 000743 ;BR 1S ;REPEAT TEST

```

```

I/O LOGIC TESTS
44400 ;*****
44500 ;AT23-- TEST#63--CHECKS THAT THE RECEIVER DONE DOES NOT
44600 ; INTERRUPT AFTER RTI INSTRUCTION WHEN DONE
44700 ; BIT IS LEFT SET.
44800 ;*****
44900
45000 007000 000063 AT23: 63 ;TEST NUMBER
45100 007002 007112 ;NEXT TEST
45200 007004 000012 ;ITERATION COUNT
45300 007006 007010 ;SCOPE ENTRY
45400 007010 032777 001000 171676 1S: BIT #LSI11,@SR ;CHECK FOR LSI-11
45500 007016 001015 000226 2S: BNE #3S ;SKIP TEST IF SET
45600 007020 012700 ;MOV #226,R0
45700 007024 104010 ;DELAY 150 MSEC
45800 007026 104011 ;AREAD ;ENABLE RECEIVER
45900 007030 104003 ;STRDRV ;SET RECEIVER INTERRUPT
46000 007032 007064 ;CLR 4S ;VECTOR TO 4S
46100 007034 005077 171552 ;CLR @TKS ;DISABLE RECEIVER INTERRUPTS
46200 007040 052777 000100 171544 ;BIS #B16,@TKS ;ENABLE RECEIVER INTERRUPT
46300 ;NOP
46400 007050 104001 ;ERROR ;NO INTERRUPT, ERROR
46500 007052 005077 171534 3S: CLR @TKS ;DISABLE RECEIVER INTERRUPTS
46600 007056 000005 ;RESET ;RESET AFTER LAST INTERRUPT
46700 007060 104005 ;CHAIN ;CHAIN TO NEXT TEST
46800 007062 000752 ;BR 4S ;REPEAT TEST
46900 007064 012777 007104 171530 4S: MOV #32,@TKVTR ;INTERUPT OK, CHANGE VECTOR TO 6S
47000 007072 012716 007100 ;MOV #35,@SP ;CHANGE RET ADDR TO 5S
47100 007076 000002 ;RTI ;RETURN
47200 007100 000240 ;BR 5S ;NO ADDITIONAL INTERRUPT
47300 007102 000763 ;BR 6S ;ERROR, ADDITIONAL INTERRUPT
47400 007104 022626 ;POPSP2 3S ;OK, NO ADDITIONAL INTERRUPT
47500 007106 104001 ;ERROR ;ERROR, ADDITIONAL INTERRUPT
47600 007110 000760 ;BR 3S ;CHAIN TO NEXT TEST

```

```

47800 ;*****
47900 ;AT24--TEST#64--HAVE OPERATOR TYPE A CHARACTER ON THE
48000 ;KEYBOARD, THEN CHECK FOR RECEIVER DONE.
48100 ;
48200 ;***** ALLOW 12 SECONDS FOR OPERATOR RESPONSE.
48300 ;
48400
48500 007112 000064 AT24: 64 ;TEST NUMBER
48600 007114 007212 AT25 ;NEXT TEST
48700 007116 000001 1 ;ITERATION COUNT
48800 007120 007172 1 ;SCOPE ENTRY
48900 007122 032777 001000 171564 1$: BIT #LSI11,RSR ;SKIP TEST IF NOT AN LSI-11
49000 007130 001426 BEQ 5$ ;
49100 007132 005777 171454 TST #TKS ;SHOULD BE CLEAR
49200 007136 001401 BEQ 2$ ;
49300 007140 104001 ERROR ;RECEIVER STATUS NOT =0
49400 007142 012700 MOV #600,RO ;1/2 SEC DELAY
49500 007146 012767 000030 171542 2$: MOV #30,CNTR ;SET UP FOR 12 SEC WAIT
49600 007154 104000 TYP ;
49700 007156 014401 OPMSG ;MESSAGE TO TYPE A CHARACTER
49800 007160 104010 DELAY ;1/2 SECOND
49900 007162 105777 TSTR #TKS ;CHECK DONE BIT
50000 007166 104077 171424 #1 ;CONTINUE WAIT
50100 007170 005367 171522 DEC CNTR ;SET - EXIT LOOP
50200 007174 001403 BEQ 4$ ;
50300 007176 012700 MOV #600,RO ;TIME HAS RUN OUT...
50400 007202 000766 BR #3$ ;ANOTHER 1/2 SEC
50500 007204 104001 ERROR ;CONTINUE WAIT
50600 ;NO RECEIVER DONE, OR
50700 007206 104005 5$: CHAIN ;OPERATOR DID NOT RESPOND
50800 007210 000744 BR 1$ ;CHAIN TO NEXT TEST

```

```

51000 ;*****
51100 ;AT25--TEST#65--CHECK THAT RECEIVER DONE CAUSES AN INTERRUPT
51200 ;WHEN BIT 6 (INTERRUPT ENABLE) IS SET.
51300 ;
51400 ;*****
51500 007212 000065 AT25: 65 ;TEST NUMBER
51600 007214 007270 AT26 ;NEXT TEST
51700 007216 000001 1 ;ITERATION COUNT
51800 007220 007222 001000 171464 1$: BIT #LSI11,RSR ;SCOPE ENTRY
51900 007222 032777 BEQ 6$ ;SKIP TEST IF NOT AN LSI-11
52000 007230 001415 171354 2$: TSTR #TKS ;DONE SHOULD BE SET
52100 007232 105777 BEQ 3$ ;
52200 007236 001001 ERROR ;RECEIVER DONE NOT SET
52300 007240 104001 RNE ;SET RECEIVER INTERRUPT
52400 007242 104003 STRDRV 5$ ;VECTOR TO 5$
52500 007244 007262 000100 171336 3$: BIC #BIT6,@TKS ;ENABLE INTERRUPT
52600 007246 052777 NOP ;
52700 007254 000240 BR 4$ ;RECEIVER DID NOT INTERRUPT
52800 007256 000240 NOP ;CLEAN UP THE STACK
52900 007260 104001 4$: ERROR ;
53000 007262 022526 5$: POPSP2 ;
53100 007264 104005 6$: CHAIN ;CHAIN TO NEXT TEST
53200 ;
53300 007266 000755 BR 1$ ;

```

I/O LOGIC TESTS

```

53500 ;*****
53600 ;AT26--TEST#66--CHECK THAT READING TKB CLEARS DONE BIT
53700 ;***** AND THAT DONE CLEARED DOES NOT CAUSE AN INTERRUPT
53800 ;*****
53900
54000 007270 000066 AT26: 66 ;TEST NUMBER
54100 007272 177777 -1 ;LAST TEST
54200 007274 000001 1 ;ITERATION COUNT
54300 007276 007300 ;SCOPE ENTRY
54400 007300 032777 001000 171406 1$: BIT #LSI11,@SR ;SKIP TEST IF NOT AN LSI-11
54500 007306 001422 BEQ 5$ ;MAKE SURE DONE IS STILL SET
54600 007310 105777 171276 2$: TSTB @TKS
54700 007314 001001 BRB 3$
54800 007316 104001 ERROR ;RECEIVER DONE NOT SET
54900 007320 017767 171270 171370 3$: MOV @TKB,CNTR ;READ DATA BUFFER
55000 007322 105777 171260 TSTB @TKS ;CHECK THE DONE BIT
55100 007332 100001 RPL 4$ ;OK
55200 007334 104001 ERROR ;READING DATA BUFFER DID NOT CLEAR DONE
55300 007336 104003 STRDRV ;SET RECEIVER INTERRUPT
55400 007340 007354 6$ ;VECTOR TO 6$
55500 007342 052777 BJS #BIT6,@TKS ;ENABLE INTERRUPT
55600 007350 000240 NOP
55700 007352 000240 CLR
55800 007354 005077 171232 5$: CLR @TKS ;OK- CLEAN UP
55900 007360 104005 CHAIN 1$ ;EXIT TESTS
56000 007362 000746 BR 1$
56100 007364 104001 BR ERROR ;DLV INTERRUPTED WITH DONE CLEAR
56200 007366 022626 POPSP2 ;CLEAN UP THE STACK
56300 007370 000771 BR 5$ ;EXIT TESTS
    
```

I/O LOGIC TESTS

56500

100
200
300
400
500
600
700
800
900
1000
1100
1200
1300
1400
1500
1600
1700
1800
1900
2000
2100
2200
2300
2400
2500
2600 007372 000000
2700 007374 007446
2800 007376 104016
2900 007400 104007
3000 007402 014127
3100 007404 012703
3200 007410 012703 025125
3300 007414 010300 060064
3400 007416 016701 171230
3500 007422 104015
3600 007424 000300
3700 007426 005301
3800 007430 001374
3900 007432 000303
4000 007434 104012
4100 007436 005302
4200 007440 001365
4300 007442 104005
4400 007444 000757

```
.SBTTL LA36 PRINTER TESTS
;
;THE LA36 PRINTER TESTS WILL BE EXECUTED IN A
;CONTINUOUS LOOP OUTPUTTING TO ALL MULTIPLE DL11'S
;IF SR BIT 0 IS SET TO ZERO AT START UP TIME. IF
;BIT 0 IS SET TO 1 AT START UP THEY MAY BE EXECUTED
;INDIVIDUALLY ONCE OR CONTINUALLY LOOPED, OR
;BECOME THE FIRST OF THE ENTIRE SEQUENCE OF PRINTER
;TESTS. REFERENCE INTRUCTIONS IN THE INTRODUCTION
;FOR PROPER MODE OF OPERATION.
;
;XXXXXXXXXX
;PTO -- DATA PATH TEST---FOUR LINES OF ALTERNATING
;   "*" AND "U" ARE PRINTED, OUT TO THE GIVEN PAPER
;   WIDTH. THE PATTERN WILL APPEAR AS FOLLOWS.
;
;   *U*U*U*U*U
;   U*U*U*U*U*
;   *U*U*U*U*U
;   U*U*U*U*U*
;
;XXXXXXXXXX
PTO:  0          ;TEST NUMBER
      PT1       ;NEXT TEST
      PRTHDR    ;
      TYPEN     ;PRINT COLUMN # MESH
      HDRO      ;
1S:   MOV      #U*,R3 ;SET FIRST CHAR PAIR
      MOV      #4,R0  ;SET LINE COUNT
2S:   MOV      R3,R0  ;SET CHAR PAIR
      MOV      WIDTH,R1 ;SET COLUMN COUNT
3S:   PRINTC    ;PRINT CHAR
      SWAB     R0      ;SET NEXT CHAR
      DEC     R1       ;DEC COLUMN COUNT
      RNE     3S      ;FINISH LINE
      SWAB     R3      ;SET NEXT LINE START CHAR
      CRLF    ;SEND CR-LF
      DEC     R2       ;DEC LINE COUNT
      RNE     2S      ;FINISH TEST
      CHAIN   000000  ;ALL DONE, EXIT
      BR      1S      ;REPEAT TEST
```

4600
4700
4800
4900
5000
5100
5200 007446 000001
5300 007450 007570
5400 007452 104016
5500 007454 012701 000040
5600 007460 012702 000100
5700 007464 012703 000140
5800 007470 110100
5900 007472 004767 000042
6000 007476 110200
6100 007500 004767 000034
6200 007504 012704 000003
6300 007510 110300
6400 007512 104015
6500 007514 005304
6600 007516 001375
6700 007520 104012
6800 007522 127122
6900 007524 165723
7000 007526 020327 000200
7100 007532 103756
7200 007534 104005
7300 007536 000746
7400 007540 012704 000003
7500 007544 104015
7600 007546 005304
7700 007550 005303
7800 007552 012700 000040
7900 007556 104015
8000 007560 012700 000040
8100 007564 104015
8200 007566 000207

```
;XXXXXXXXXX
;PT1 -- PRINTER CHARACTER TEST --- PRINTS ALL PRINTABLE CHARACTERS
;XXXXXXXXXX
PT1:  1          ;TEST NUMBER
      PT2       ;NEXT TEST
      PRTHDR    ;
1S:   MOV      #40,R1 ;SPACE TO R1
      MOV      #100,R2 ;A TO R2
      MOV      #140,R3 ;A TO R3
2S:   MOVB    R1,R0   ;CHAR TO R0
      JSR     PC,SPSP ;SEND TWO SPACES
      MOVB    R2,R0   ;NEXT CHAR TO R0
      JSR     PC,SPSP ;SEND TWO SPACES
      MOV     #3,R4   ;PRINT COUNT TO R4
      MOVB    R3,R0   ;THIRD CHAR TO R0
3S:   PRINTC    ;PRINT THE CHAR
      DEC     R4       ;THREE TIMES?
      RNE     3S      ;BRANCH IF NOT
      CRLF    ;CARRIAGE RETURN LINE FEED
      CMPR    (R1)+,(R2)+ ;CHECK IF ALL DONE
      TSTR    (R3)+   ;NEXT CHARACTERS
      BR      1S      ;REPEAT TEST
SPSP: MOV      #3,R4  ;PRINT COUNT TO R4
1S:   PRINTC    ;PRINT CHAR
      DEC     R4       ;THREE TIMES?
      RNE     1S      ;BRANCH IF NOT
SP2:  MOV      #40,R0 ;SPACE TO R0
1S:   PRINTC    ;SEND A SPACE
      MOV     #40,R0  ;SPACE TO R0
      PRINTC    ;SEND ANOTHER
      RTS     PC      ;RETURN
```

```

XXXXXXXXXX
PT2 -- NON-PRINTING CHARACTER TEST. THIS TEST
PRINTS THE OCTAL CODE FOLLOWED BY THE MNEMONIC
OF ALL NON-PRINTING CHARACTERS. FOLLOWING EACH
MNEMONIC, THE PRINTER IS DRIVEN BY THE NON-PRINTING
CODE (000 THROUGH 037 PLUS 177)
ALL CONTROL CHARACTERS (INCLUDING THOSE FOR OPTIONS
WILL BE SKIPPED, REFER TO THE DOCUMENT FOR A LIST OF THOSE
TESTED.
XXXXXXXXXX
PT2: 2 PT3 }TEST NUMBER
      PPTHDR }NEXT TEST
      MOV #IDEZ,R1 }PRINT TEST HEADER
      MOV #NPCODE,R3 }ADDR OF IDENT TO R1
      MOV #3,R2 }ADDR OF NON-PRINT-CODES TO R3
      MOV #19,R4 }NO. OF LINES PER LINE TO R2
      CMPB (R3),#55 }NO. OF CHARS PER ID TO R4
      BEQ 7S }ZERO TERMINATOR IN NP TABLE?
      PRINTC (R1)+,R0 }BRANCH IF YES
      DEC 7S }GET ID CHARACTERS
      BNE 4S }AND PRINT A
      PRINTC }GROUP OF
      DEC 4S }R CHARACTERS
      MOV (R3)+,R0 }GET NP CODE FROM TABLE
      MOV #3,R4 }END
      PRINTC }TRY TO PRINT IT
      DEC R4 }THREE
      BNE 5S }TIMES
      DEC R2 }MORE TO GO ON THIS LINE ?
      BEQ 6S }BRANCH IF NO
      JSP PC,SP2 }SEND 3 SPACES
      PRINTC BR 3S }BRANCH TO CONTINUE LINE
      CRLF BR 2S }GO DO NEXT LINE
      CRLF BR 7S }CHAIN TO NEXT TEST
      CHAIN BR 1S
      BR 1S

12800 007676 060 060 IDEZ: .ASCII /000 NUL001 SOH002 STX/
      007701 040 040 116
      007702 040 040 114
      007707 060 061 060
      007712 040 123 117
      007715 110 060 060
      007723 053 040 130
      007726 060 060 066
12900 007731 040 040 101
      007734 040 113 066
      007737 062 060 040
      007742 040 104 114

```

```

XXXXXXXXXX
PT2: 2 PT3 }TEST NUMBER
      PPTHDR }NEXT TEST
      MOV #IDEZ,R1 }PRINT TEST HEADER
      MOV #NPCODE,R3 }ADDR OF IDENT TO R1
      MOV #3,R2 }ADDR OF NON-PRINT-CODES TO R3
      MOV #19,R4 }NO. OF LINES PER LINE TO R2
      CMPB (R3),#55 }NO. OF CHARS PER ID TO R4
      BEQ 7S }ZERO TERMINATOR IN NP TABLE?
      PRINTC (R1)+,R0 }BRANCH IF YES
      DEC 7S }GET ID CHARACTERS
      BNE 4S }AND PRINT A
      PRINTC }GROUP OF
      DEC 4S }R CHARACTERS
      MOV (R3)+,R0 }GET NP CODE FROM TABLE
      MOV #3,R4 }END
      PRINTC }TRY TO PRINT IT
      DEC R4 }THREE
      BNE 5S }TIMES
      DEC R2 }MORE TO GO ON THIS LINE ?
      BEQ 6S }BRANCH IF NO
      JSP PC,SP2 }SEND 3 SPACES
      PRINTC BR 3S }BRANCH TO CONTINUE LINE
      CRLF BR 2S }GO DO NEXT LINE
      CRLF BR 7S }CHAIN TO NEXT TEST
      CHAIN BR 1S
      BR 1S

13000 007745 105 060 062
      007750 061 040 040
      007753 104 103 061
      007756 060 062 062
      007759 040 040 104
      007764 103 062 060
      007767 062 063 040
      007772 040 104 103
      007775 064 060 062
      010000 064 040 040
      010003 104 103 064
13100 010006 060 062 065
      010011 040 040 116
      010014 101 113 060
      010017 062 066 040
      010022 040 123 131
      010025 116 060 062
      010030 040 040 040
      010033 105 124 102
13200 010036 060 063 060
      010041 040 040 103
      010044 101 116 060
      010047 063 061 040
      010052 040 105 115
      010055 040 060 063
      010060 062 040 040
      010063 123 125 102
13300 010066 060 063 064
      010071 040 040 106
      010074 040 040 066
      010077 063 065 040
      010102 040 107 123
      010105 040 060 063
      010110 066 060 040
      010113 122 123 040
      010116 060 063 067
      010121 040 040 125
      010124 040 061 061
      010127 067 067 040
      010132 040 104 105
      010135 114 040 040
13500 010142 020 021 022 NPCODE: .BYTE 0,2,6,20,21,22,23,24
      010145 023 024
      010147 025 027
13600 010147 025 027 .BYTE 25,25,27,30,31,32,34,35
      010152 030 032
      010155 034 035
13700 010157 036 037 177 .BYTE 36,37,177,55
      010162 055
13800 .EVEN

```

```

14000 ;XXXXXXXXXX
14100 ;
14200 ;PT3 -- CARRIAGE RETURN TEST
14300 ;
14400 ;
14500 ; THE LINE CONSISTS OF A STRING OF O'S AND
14600 ; X'S. FIRST, THE O'S ARE PRINTED OUT TO THE LAST
14700 ; COLUMN WITH A SPACE SEPARATING EACH. THEN THE
14800 ; CARRIAGE IS SPACED TO THE FIRST BLANK SPACE, AN X
14900 ; IS PRINTED AND THEN RETURNED TO THE MARGIN. THIS
15000 ; PROCESS IS CONTINUE UNTIL ALL SPACES BETWEEN
15100 ; THE ZEROES HAVE BEEN FILLED.
15200 ;XXXXXXXXXX
15300 ;
15400 PT3: 3 ;TEST NUMBER
15500 PT4 ;NEXT TEST
15600 PTHDR ;TYPE HEADER
15700 CLR SPCNT ;CLEAR SPACE COUNTER
15800 MOV WIDTH,R1 ;POSITION COUNTER TO R1
15900 #117,R) ;"O" TO RO
16000 PRINTC ;PRINT THE "O"
16100 R1 ;DECREMENT POSITION COUNTER
16200 BGE 3S ;BRANCH IF 0
16300 JSR PC,SPC ;SEND SPACE
16400 DEC R1 ;DECREMENT POSITION COUNTER
16500 BNE 2S ;BRANCH IF NOT ZERO
16600 CR ;SEND A CR
16700 MOV #1,SPCNT ;SPACE COUNTER SET TO 1
16800 MOV SPCNT,R1 ;NO. OF SPACES TO R1
16900 JSR PC,SPC ;SEND SPACE
17000 DEC R1 ;DECREMENT SPACE COUNTER
17100 BNE 5S ;BRANCH IF NOT ZERO
17200 MOV #130,R0 ;"X" INTO R0
17300 PRINTC ;PRINT "X"
17400 CR ;PRINT CR
17500 ADD #2,SPCNT ;INCREMENT SPACE COUNT BY 2
17600 CMP SPCNT,WIDTH ;COMPARE POSITION COUNTER WITH COLM. COUNT
17700 BLO 4S ;BRANCH IF LOWER
17800 LF ;
17900 CHAIN ;SEND LF
18000 BR 1S ;RETURN TO NEXT TEST
;REPEAT TEST

```

```

18200 ;XXXXXXXXXX
18300 ;
18400 ;PT4 -- MULTIPLE LINE FEED TEST -- 63 LINE FEEDS ARE
18500 ; SENT WITH A REFERENCE LINE AT THE START AND END.
18600 ; A NUMBER IS PRINTED WHICH INDICATES THE NUMBER OF LINE
18700 ; FEEDS THAT WILL BE ISSUED BEFORE THE NEXT
18800 ; NUMBER OR REFERENCE LINE IS PRINTED.
18900 ;XXXXXXXXXX
19000 ;
19100 ;
19200 PT4: 4 ;TEST NUMBER
19300 PTHDR ;NEXT TEST
19400 ;TYPE HEADER
19500 MOV #1,LFCNT ;LINE FEED COUNT TO 1
19600 MOV WIDTH,R1 ;COLUMN COUNT TO R1
19700 MOV #LINES,R2 ;ADDR OF NUMBER FIELD TO R2
19800 JSR PC,REF ;PRINT REFERENCE LINE
19900 MOV LFCNT,R1 ;LINE FEED COUNT TO R1
20000 LF ;SEND LF
20100 DEC R1 ;DECREMENT COUNTER
20200 BNE 3S ;BRANCH IF NOT YET 0
20300 ASL LFCNT ;DOUBLE LINE FEED COUNT
20400 CMP #BIT6,LFCNT ;TEST IF COUNT IS 32
20500 BEQ 4S ;BRANCH IF =32, END
20600 MOVB (R2)+,R0 ;NUMBER TO R0
20700 PRINTC ;PRINT IT
20800 MOVB (R2)+,R0 ;NUMBER TO R0
20900 PRINTC ;PRINT IT
21000 CR ;PRINT CR
21100 BR 2S ;DRIVE THE LINEFEEDS
21200 MOV WIDTH,R1 ;COLUMN COUNT TO R1
21300 JSR PC,REF ;SEND END REFERENCE LINE
21400 LF ;ADVANCE PAPER
21500 CHAIN ;
21600 BR 1S ;REPEAT TEST
21700 MOVB (R2)+,R0 ;NUMBER TO R0
21800 PRINTC ;PRINT IT
21900 MOVB (R2)+,R0 ;NUMBER TO R0
22000 PRINTC ;PRINT IT
22100 TST -(R1) ;DECREASE COUNTER BY 2
22200 MOV #137,R0 ;DASH (-) TO R0
22300 PRINTC ;PRINT IT
22400 DEC R1 ;DECREMENT COLUMN COUNTER
22500 BNE 1S ;BRANCH IF NO ZERO
22600 CR ;PRINT CR
22700 RETURN ;RETURN
22800 ;
22900 LINE3: .ASCII /01020408163200/

```

```

LA36 PRINTER TESTS
23100
23200
23300
23400
23500
23600
23700
23800
23900
24000
24100
24200
24300
24400
24500
24600
24700
24800
24900
25000
25100
25200
25300
25400
25500
25600
25700
25800
25900
26000
26100
26200
26300
26400
26500
26600
26700
26800
26900
27000
27100
27200
27300
27400
27500
27600
27700
27800
27900
28000
28100
28200
28300
28400
010462 000005
010464 010666
010466 104916
010470 170156
010474 000060
010476 012700
010502 104915
010504 005301
010506 001375
010510 012700
010514 104915
010516 104915
010520 000204
010522 001404
010530 003410
010534 104910
010536 004877
010540 012700
010544 000063
010550 000100
010552 104915
010554 005301
010556 104912
010560 170066
010570 000134
010572 104914
010574 005301
010576 104915
010600 104922
010602 000022
010606 004767
010610 014910
010614 001750
010616 104910
010618 000006
010622 104912
010624 000720
010626 000720
010630 170016
010634 000061
010640 104915
010642 005301
010644 001407
010646 005200
010650 000071
010654 101771
010656 000060
010662 000766
010664 000207

;XXXXXXXXXX
;PT5-- SINGLE LINE FEED TEST -- TESTS THE LINE FEED
; CAPABILITY FROM ALL COLUMNS.
;XXXXXXXXXX
PT5: 5 ;TEST NUMBER
MOV PT6 ;NEXT TEST
PRTHDR ;PRINT HEADER
MOV WIDTH,R1 ;COLUMN COUNT TO R1
TST -(R1) ;DECREASE BY 2
MOV #60,R0 ;"0" TO R0
PRINTC ;SEND 0
DEC R1 ;DECREMENT COLUMN COUNTER
BNE 25 ;BRANCH IF NOT ZERO
MOV #62,R0 ;SEND A 2
PRINTC ;SEND A SECOND TWO
CMP WIDTH,#132. ;COMPARE COLUMN COUNT
BEQ 35 ;BRANCH IF EQ 132
MOV #3410,R0 ;DELAY 1.8 SEC
DELAY 35
BR 35
MOV #63,R0 ;3'S TO R0
MOV #100,R1 ;64 TO COUNTER
PRINTC ;SEND CHARACTER
DEC R1 ;DECREMENT COUNT
BNE 45 ;BRANCH IF NOT ZERO
CR LF ;SEND A CR, LF
MOV WIDTH,R1 ;NO COLUMNS TO R1
MOV #134,R0 ;BACKSLASH TO R0
PRINTC ;SEND IT
LF ;PRINT LF
DEC R1 ;DECREMENT COUNTER
BNE 65 ;BRANCH IF NOT ZERO
CR ;SEND CR
JSR PC,PTSAL ;SEND REF LINE #1
CR LF ;SEND A CR, LF
DELAY 1 SEC
BR 35
MOV #1750,R0 ;SEND A CR, LF
DELAY 1 SEC
BR 35
MOV #1750,R0 ;SEND A CR, LF
DELAY 1 SEC
BR 35
MOV #61,R0 ;COLUMN COUNT TO R1
PRINTC ;"1" TO R0
DEC R1 ;DECREMENT COUNTER
REQ 25 ;BRANCH IF=0
INC R0 ;INCREMENT CHARACTER
CMG #71 ;COMP CHAR TO "0"
BLOS 15 ;BRANCH IF LOWER OR SAME
MOV #60,R0 ;RESET CHAR TO "0"
BR 15 ;CONTINUE
RTS PC ;FINISHED, RETURN TO CALLER

```

```

LA36 PRINTER TESTS
28600
28700
28800
28900
29000
29100
29200
29300
29400
29500
29600
29700
29800
29900
30000
30100
30200
30300
30400
30500
30600
30700
30800
30900
31000
31100
31200
31300
31400
31500
31600
31700
31800
31900
32000
32100
32200
32300
32400
32500
32600
32700
32800
32900
33000
33100
33200
33300
33400
33500
33600
33700
33800
010666 000006
010670 011054
010672 104916
010674 014917
010676 014917
010700 167746
010704 005741
010706 000060
010712 104915
010714 005301
010716 001375
010720 012700
010724 104915
010726 104915
010730 026727
010734 001404
010740 012700
010744 104910
010746 000407
010750 000063
010754 000100
010760 104915
010762 005301
010764 001375
010766 104915
010770 167656
010774 000134
011000 012700
011002 012700
011006 104915
011010 012700
011014 104915
011016 005301
011020 001365
011022 104914
011024 104922
011026 005301
011032 104917
011034 001750
011040 104910
011046 177562
011050 104912
011052 000712

;XXXXXXXXXX
;PT6-- BACKSPACE TEST -- A REFERENCE LINE SUCH AS IN
; TEST PT5 IS PRINTED. THE SECOND LINE CONSISTS
; OF PRINTING A BACKSLASH, BACKSPACE AND FORWARD
; SLASH COMBINATION OUT TO THE GIVEN COLUMN WIDTH.
; THIS LINE IS THEN FOLLOWED BY THE SAME TWO REFERENCE
; LINES AS PRINTED IN TEST PT5.
;XXXXXXXXXX
PT6: 6 ;TEST NUMBER
PT7 ;NEXT TEST
PRTHDR ;PRINT HEADER
TYPEM ;PRINT COLUMN # MESC
MOV WIDTH,R1 ;COLUMN COUNT TO R1
TST -(R1) ;DECREMENT BY 2
MOV #60,R0 ;"0" TO R0
PRINTC ;SEND 0
DEC R1 ;DECREMENT COLUMN COUNTER
BNE 25 ;BRANCH IF NOT ZERO
MOV #62,R0 ;"2" TO R0
PRINTC ;SEND A "2"
CMP WIDTH,#132. ;SEND A SECOND "2"
BEQ 35 ;COMPARE COLUMN COUNT
MOV #3410,R0 ;DELAY 1.8 SEC
DELAY 35
BR 35
MOV #63,R0 ;3'S TO R0
MOV #100,R1 ;64 TO CHAR COUNT
PRINTC ;SEND CHAR
DEC R1 ;DECREMENT CHAR COUNT
BNE 45 ;CONTINUE IF NOT DONE
CR LF ;SEND A CR, LF
MOV WIDTH,R1 ;COLUMN COUNT TO R1
MOV #134,R0 ;BACKSLASH TO R0
PRINTC ;SEND IT
MOV #10,R0 ;BACKSPACE TO R0
PRINTC ;SEND IT
MOV #57,R0 ;FORWORD SLASH TO R0
PRINTC ;SEND IT
DEC R1 ;END OF PAPER
BNE 65 ;BRANCH IF NO
LF ;BRANCH IF NO
CR ;SEND CR
JSR PC,PTSAL ;SEND REF LINE #1
CR LF ;SEND A CR, LF
DELAY 1 SEC
BR 35
MOV #1750,R0 ;SEND SECOND REF LINE
CR LF ;SEND A CR, LF
CHAIN ;CHAIN TO NEXT TEST
RR 15 ;REPEAT TEST

```



```

34000
34100
34200
34300
34400
34500
34600
34700
34800
34900
35000
35100 011054 000007
35200 011058 011266
35300 011060 104016
35400 011062 012703 000002
35500 011066 016701 167560
35600 011072 012700 000115
35700 011076 104015
35800 011100 005301
35900 011102 001404
36000 011104 004767 176450
36100 011106 013303
36200 011112 001367
36300 011114 022703 000002
36400 011120 012003
36500 011122 104022
36600 011124 005303
36700 011126 000757
36800 011130 005703
36900 011132 013301
37000 011134 104013
37100 011136 005723
37200 011140 016701 167506
37300 011142 024767 176410
37400 011150 005301
37500 011152 001405 000100
37600 011154 012700
37700 011160 104015
37800 011162 005301
37900 011164 001367
38000 011166 022703 000002
38100 011172 004003
38200 011174 104022
38300 011176 005303
38400 011200 006757
38500 011202 005703
38600 011204 001373
38700 011206 104012
38800 011210 005723
38900 011212 016701 167434
39000 011216 012700 000046
39100 011222 104015
39200 011224 005301
39300
39400 011226 001404
39500 011230 004767 176324
39600 011234 005301

```

```

;XXXXXXXXXX
PT7-- OVERPRINT TEST-- A ROW OF ALTERNATING M'S AND
SPACES ARE PRINTED OUT TO THE LAST COLUMN AND OVERPRINTED TWICE.
A SECOND LINE OF ALTERNATING SPACES AND "M" IS THEN
SENT 3 TIMES AS THE FIRST LINE. THIS IS FOLLOWED
BY A THIRD AND FINAL LINE OF ALTERNATING "M"
AND SPACES.
;XXXXXXXXXX
PT7: 7 ;TEST NUMBER
PT10 ;NEXT TEST
PRTHDR ;PRINT MESSAGE
15: MOV #2,R3 ;2 COUNT TO R3
25: MOV WIDTH,R1 ;NO. OF COLUMNS TO R1
35: MOV #15,R0 ;"M" TO R0
PRINTC ;SEND IT
DEC R1 ;END OF LINE
BEQ 45 ;BRANCH IF YES
JSR PC,SPC ;SEND SPACE
DEC R1 ;END OF LINE?
RNE 55 ;BRANCH IF NO
45: CMP #2,R3 ;TEST R3
BNE 65 ;BRANCH IF NOT FIRST TIME
CR ;SEND CR
DEC R3 ;DECREASE LINE COUNTER
BR 25 ;REPEAT LINE
65: TST R3 ;THIRD TIME?
RNE 55 ;BRANCH IF NOT
CRLF ;NEXT LINE
TST (R3)+ ;REPEAT COUNTER TO R3
MOV WIDTH,R1 ;COLUMN COUNT TO R1
CMP PC,SPC ;END SPACE
DEC R1 ;DECREASE COLUMN COUNT
BEQ 95 ;BRANCH IF 0, END OF LINE
MOV #100,R0 ;"M" TO R0
PRINTC ;SEND IT
DEC R1 ;DECREASE COLUMN COUNT
RNE 95 ;BRANCH IF NOT 0 (NOT END)
75: CMP #2,R3 ;END OF LINE, FIRST TIME?
RNE 115 ;BRANCH IF NOT
CR ;SEND CR
DEC R3 ;DECREASE LINE COUNTER
BR 75 ;REPEAT LINE
115: TST R3 ;TEST IF THIRD REPEAT
RNE 105 ;BRANCH IF NOT
CRLF ;DO NEXT LINE
TST (R3)+ ;LINE REPEAT COUNTER TO R3
MOV WIDTH,R1 ;COLUMN COUNT TO R1
MOV #46,R0 ;"M" TO R0
PRINTC ;SEND IT
DEC R1 ;DECREASE COLUMN COUNT
BEQ 145 ;BRANCH IF END
JSP PC,SPC ;SEND SPACE
DEC R1 ;DECREASE COLUMN COUNT

```

```

39700 011236 001367 000002
39800 011240 022703
39900 011244 001404
40000 011246 104022
40100 011250 005303
40200 011252 000757
40300 011254 005703
40400 011256 001373
40500 011260 104012
40600 011262 104005
40700 011264 000676

```

```

145: BNE 135 ;BRANCH IF NOT END
155: CMP #2,R3 ;TEST IF FIRST TIME
RNE 165 ;BRANCH IF =2, FIRST TIME
CR ;SEND CR
DEC R3 ;DECREASE REPEAT COUNTER
BR 125 ;PRINT LINE AGAIN
165: TST R3 ;TEST IF END, R3=0
RNE 155 ;BRANCH IF NOT END
CRLF ;SEND CRLF
CHAIN ;CHAIN TO NEXT TEST
BR 15 ;REPEAT TEST

```

```

40900 ;XXXXXXXXXX
41000 ;
41100 ;PT10-- PRINTING FREQUENCY TEST-- 120 H'S ARE PRINTED ON 4 LINES
41200 ;30 PER LINE. THE TEST IS SUCH THAT BETWEEN THE FIRST AND SECOND
41300 ;30 SEC DELAY IS INTRODUCED. THIS DELAY IS THEN INCREASED
41400 ;BETWEEN CHARACTERS OUT TO 60 CHARACTERS IN AN EXPONENTIAL
41500 ;MANNER. THE DELAY IS THEN DECREASED IN THE SAME MANNER OUT TO THE
41600 ;120TH CHARACTER. THIS DELAY IS CALCULATED AS FOLLOWS:
41700 ;
41800 ; NEW DELAY = OLD DELAY [+ OR -] (OLD DELAY/16 + OLD DELAY/128 )
41900 ;
42000 ;XXXXXXXXXX
42100 PT10: 10 ;TEST NUMBER
42200 011266 000010 ;NEXT TEST
42300 011270 011424 ;TYPE MESSAGE
42400 011272 104016 ;SET R1=30
42500 011274 012700 000036 1S: MOV #36,R1 ;SET CHAR COUNT = 120
42600 011276 012700 000170 ;SET UP DELAY VALUE
42700 011304 012767 000036 2S: MOV #30,R2
42800 011312 012700 000110 ;WH TO R0
42900 011314 104015 000110 ;SEND IT
43000 011316 012760 000036 3S: PRINTC #30,R0
43100 011324 104010 ;DELAY
43200 011326 005301 ;DEC. COUNT OF CHARS PER LINE
43300 011328 005302 4S: BEQ R1,R2 ;BRANCH IF 0, END OF LINE
43400 011330 005302 ;DECREMENT CHAR COUNTER
43500 011334 001430 ;BRANCH IF END
43600 011336 016704 177760 ;GET OLD DELAY
43700 011342 006204 ;CAL 1/16 OF OLD DELAY
43800 011344 006204 ;ASR R4
43900 011346 006204 ;ASR R4
44000 011350 006204 ;ASR R4
44100 011354 006204 ;ASR R4,R5 ;SAVE 1/16 IN R5
44200 011356 006204 ;CAL 1/128 OF OLD DELAY
44300 011360 006204 ;ASR R4
44400 011362 006402 ;ADD #4,R5
44500 011364 006402 000074 ;TEST WHICH HALF OF THE 120 CHARS.
44600 011370 003403 ;BRANCH IF LT OR EQ 60
44700 011372 160567 177724 ;GET 51, DECREASE DELAY BY 34 MEC.
44800 011374 007446 ;GO PRINT AGAIN
44900 011400 060567 177716 5S: ADD R5,R5 ;AT HALF WAY, ADD DELAY OF 34 MEC.
45000 011404 000742 ;GO PRINT AGAIN
45100 011406 104012 6S: BR R5,R5 ;SEND CRLF
45200 011408 104012 000036 ;SET R1=30
45300 011414 007446 ;CRLF #36,R1
45400 011416 104012 7S: BR 45 ;SEND CR,LF
45500 011420 104005 ;CHAIN TO NEXT TEST
45600 011422 000724 ;REPEAT TEST

```

```

45900 ;XXXXXXXXXX
46000 ;
46100 ;PT11-- RIBBON FEED TEST-- THIS TEST PRINTS A SINGLE COLUMN OF X'S
46200 ;(24 LINES) DOWN THE LEFT MARGIN OF THE PAGE.
46300 ;VISUALLY CHECK THE RIBBON FEED MECHANISM FOR PROPER OPERATION.
46400 ;
46500 ;XXXXXXXXXX
46600 ;
46700 PT11: 11 ;TEST NUMBER
46800 011424 000011 ;NEXT TEST
46900 011426 014256 ;TYPE MESSAGE
47000 011430 104216 ;SET R1=24(10), LINE COUNT
47100 011432 012701 000030 1S: MOV #30,R1 ;SET CHAR = X
47200 011436 012700 000130 2S: MOV #130,R0 ;PRINT X
47300 011442 104012 ;SEND CR,LF
47400 011444 005301 ;DECREMENT LINE COUNT
47500 011446 005301 ;CONTINUE IF NOT DONE TEST
47600 011450 001372 ;CHAIN TO NEXT TEST
47700 011454 000768 ;REPEAT TEST
47800 ;
47900 ;
48000 ;
48100 ;XXXXXXXXXX
48200 ;
48300 ;PT12-- PRINTER BELL TEST-- THE LAST TEST IN THE
48400 ;PRINTER TEST SEQUENCE. THIS TEST OUTPUTS
48500 ;EIGHT BELL SIGNALS TO THE PRINTER
48600 ;
48700 ;
48800 ;XXXXXXXXXX
48900 ;
49000 ;
49100 PT12: 12 ;THIS TEST
49200 011456 000112 ;NEXT TEST
49300 011460 007372 ;TYPE HEADER
49400 011464 012701 000010 PT12A: MOV #10,R1 ;COUNTER TO R1
49500 011470 012700 000007 1S: MOV #7,R0 ;BELL TO R0
49600 011474 104015 ;SEND IT
49700 011476 005300 ;DECREMENT COUNT
49800 011500 001375 ;BRANCH IF NOT ZERO
49900 011502 104014 ;LF
50000 011504 012700 000372 ;DELAY 2 SEC BEFORE RESTARTING
50100 011510 104010 000042 ;DELAY
50200 011512 013700 ;CHECK IF UNDER ACT11 OR XXDP
50300 011516 001405 ;CONTINUE TEST SEQUENCE
50400 011520 000746 ;A RESET WAS FORMERLY HERE
50500 011522 004710 LOGICAL: JSR PC,(R0)
50600 011524 000240 ;NOP
50700 011526 000240 ;NOP
50800 011530 000240 ;NOP
50900 011532 124005 ;CHAIN TO NEXT TEST
51000 011534 000753 ;REPEAT TEST

```

```

51200
51300
51400
51500
51600
51700
51800
51900
52000
52100
52200
52300 011536 000017
52400 011540 011536
52500 011542 000167
52600 011546 000117 000030
52700 011550 011536
52800 011552 005067 000336
52900 011556 016704 167070
53000 011562 012767 000001 000322
53100
53200
53300
53400 011576 012763 000041
53500 011602 005267 000306
53600 011606 026727 000302 000031
53700 011614 011993
53800 011618 012700 000001 000270
53900 011624 012700 014042 20S:
54000 011630 016701 000260
54100 011634 012702 000002
54200 011640 104023
54300 011642 016701 167004 1S:
54400 011646 010300
54500 011650 004767 000110 2S:
54600 011654 104015
54700 011656 005301
54800 011660 003377
54900 011662 004767 000144
55000 011666 104012
55100 011670 012702 000005
55200 011674 016701 166752 3S:
55300 011700 010300
55400 011702 004767 000056 4S:
55500 011706 104015
55600 011710 005301
55700 011712 003377
55800 011714 104022
55900 011716 005362
56000 011720 001365 000104
56100 011722 004767
56200 011726 104014
56300 011730 005203
56400 011732 022703 000177
56500 011736 001341
56600 011740 004767 000066
56700 011744 004767 000062
56800 011750 004767 000056

```

```

;XXXXXXXXXX
;PT17-- LIFE TEST
; THIS TEST PRINTS 2 FULL LINES OF EACH PRINTABLE
; CHARACTER AND OVERPRINTS THE SECOND LINE 4 TIMES.
; THIS TEST IS CONTINUOUS RUNNING ONCE INITIATED,
; LOOPING AUTOMATICALLY ON ITSELF.
; END OF PASS COUNT IS CLEARED WHENEVER TEST IS RESTARTED
;XXXXXXXXXX
PT17B: 17 ;TEST NUMBER
PT17B ;NEXT TEST
JMP PT17D ;CONTINUE
PT17: 17 ;TEST NUMBER
PT17B ;NEXT TEST
CLR PASCNT ;CLEAR PASS COUNT
MOV WIDTH,R4 ;INITIALIZE R4
MOV #1,DIRTN ;AND DIRECTION OF PRECESS
PRTHDR ;PRINT COLUMN # MESS
TYPEM ;TYPE END OF PASS MESS
HRO ;REPEAT TEST
MOV #41,R3 ;SET START CHAR
INC PASCNT ;DO 31 TIMES
CMP PASCNT,#31 ;BRANCH IF NOT DONE
BNE 20S ;START OVER
MOV #1,PASCNT ;SET MESS ADDR
MOV #PASMES,R0 ;SET TO CONVERT
MOV PASCNT,R1 ;# TO CONVERT
MOV #2,R2 ;# DIGITS
STOASC ;CONVERT PASCNT TO ASCII
MOV WIDTH,R1 ;SET COLUMN COUNT
MOV R3,R0 ;GET CHARACTER
JSR PC,CRPOS ;TIME TO INSERT PASS # ?
PRINTC ;SEND CHAR
DEC R1 ;DECREMENT COUNT
BGT 2S ;BRANCH IF NOT DONE
JSR PC,ADJR4 ;ADJUST R4 POINTER
MOV #5,R2 ;SET OVERPRINT COUNT
MOV WIDTH,R1 ;SET COLUMN COUNT
MOV R3,R0 ;GET CHARACTER
JSR PC,CRPOS ;TIME TO INSERT PASS # ?
PRINTC ;SEND CHAR
DEC R1 ;DECREMENT COUNT
BGT 4S ;BRANCH IF NOT DONE
CR ;SEND CR
DEC R2 ;DONE OVERPRINTS ?
BNE 3S ;NO, CONTINUE
JSR PC,ADJR4 ;ADJUST R4 POINTER
LF ;SEND LF
INC R3 ;SET NEXT CHAR
CMP #177,R3 ;DONE CHAR SET ?
BNE 1S ;NO, CONTINUE
JSR PC,ADJR4 ;OFFSET POINTER 3 PLACES
JSR PC,ADJR4 ;TO RETAIN VISUAL ALIGNMENT
JSR PC,ADJR4 ;THROUGH END OF PASS

```

```

56900 011754 104007
57000 011756 014023
57100 011760 000705
57200 011762 000705
57300

```

```

TYPEM ;TYPE END OF PASS MESS
ENDPAS
CHAIN
BR PT17D ;REPEAT TEST

```

57500								
57600	011764	020401		CKPOS:	CMP	R4,R1		;IS IT TIME TO INSERT PASS # ?
57700	011766	001020			BNE	1\$;BRANCH IF NO
57800	011770	012700	000040		MOV	#40,R0		;PRINT A SPACE
57900	011774	104015			PRINTC			
58000	011776	187000	002040		MOVB	PASMES,R0		;PRINT MSG OF PASS COUNT
58100	012002	104015			PRINTC			
58200	012004	116700	002033		MOVB	PASMES+1,R0		
58300	012010	104015			PRINTC			;PRINT A SPACE
58400	012012	012700	000040		MOV	#40,R0		
58500	012016	104015			PRINTC			
58600	012020	162701	000003		SUB	#3,R1		;ADJUST R1 3 POSITIONS
58700	012024	082716	000002		ADD	#2,(SP)		;ADJUST RETURN PC OVER PRINTC
58800	012030	000207		1\$:	RTS	PC		
58900								
59000	012032	005767	000054	ADJR4:	TST	DIRTN		;TEST DIRECTION OF PRECESS
59100	012036	011013			BNE	1\$;BR IF LEFT
59200	012040	005204			INC	R4		;INCREASE POSITION CNTR
59300	012042	020467	166504		CMP	R4,WIDTH		;IS R4 > WIDTH ?
59400	012046	101420			BLOS	3\$;BR IF NOT GREATER
59500	012050	016704	166576		MOV	WIDTH,R4		;CHANGE DIRECTION
59600	012054	005304			DEC	R4		; TO
59700	012056	012767	000001 000026		MOV	#1,DIRTN		; LEFT.
59800	012064	000411			BR	3\$		
59900	012066	005304		1\$:	DEC	R4		;DECREASE POSITION CNTR
60000	012070	020427	000004		CMP	R4,#4		;LESS THAN 4 ?
60100	012074	002401			BLT	2\$;BR IF YES
60200	012076	000404			BR	3\$;ELSE EXIT
60300	012100	012704	000005	2\$:	MOV	#5,R4		;SET R4 TO POS 5
60400	012104	005007	000002	3\$:	CLR	DIRTN		;CHANGE DIRECTION TO RIGHT
60500	012110	000207			PC			;EXIT
60600								
60700	012112	000000		DIRTN:	.WORD	0		;DIRECTION OF PRECESS (0=LEFT)
60800								
60900	012114	000000		PASCNT:	.WORD	0		

61100

```

LA36 ECHO TESTS
. SRTTL LA36 ECHO TESTS
XXXXXXXXXX
EO20-- CHARACTER ECHO TEST-- ALL PRINTABLE AND
NON-PRINTING CHARACTERS TYPED ON THE KEYBOARD
ARE USED TO DRIVE THE PRINTER, ONE CHARACTER AT
A TIME. A "RUBOUT" WILL CAUSE THE TEST TO BE
TERMINATED.
XXXXXXXXXX
EO20: 20 ;TEST NUMBER
EO21 ;NEXT TEST
PRTHDR ;TYPE HEADER
1S: READ ;GO WAIT FOR KEYBOARD INPUT
MOV #30.,R0 ;DELAY FOR HALF DUPLEX
DELAY ;
CMP #177,TEMPCH ;CHECK IF RUBOUT
BEQ 2S ;BRANCH IF YES
PRNT ;NO, CHECK PRINTER READY
MOVR @TKB,@TPB ;READY, ECHO CHARACTER
BR 1S ;
2S: PYPFM ;PRINT TERMINATION MESSAGE
ECPEND ;
CHAIN ;CHAIN TO NEXT TEST
BR 1S ;REPEAT TEST
XXXXXXXXXX
EO21-- LINE ECHO TEST, FAST RATE-- THIS TEST WILL
CAUSE THE CONTINUAL PRINTING OF "M" AT THE MAXIMUM
RATE UNTIL EITHER ANOTHER CHARACTER IS SELECTED
BY PRESSING A KEY ON THE KEYBOARD OR TERMINATION BY THE
RUBOUT.
XXXXXXXXXX
EO21: 21 ;TEST NUMBER
EO22 ;NEXT TEST
PRTHDR ;TYPE HEADER
EQ21A: MOV #60,REPT ;CHARACTER TO BE REPEATED (O)
1S: MOV WIDTH,R2 ;SET COLUMN COUNT
2S: MOV REPT,R0 ;SET CHAR
PRINTC ;PRINT CHAR
DEC R2 ;DEC COLUMN COUNT
RGT 2S ;FINISH LINE
CRLF ;SEND A CR AND LF
BR 1S ;

```

```

LA36 ECHO TESTS
XXXXXXXXXX
EO22-- LINE ECHO TEST, SLOW RATE-- SAME AS EO21 EXCEPT
THAT A DELAY IS INTRODUCED BETWEEN CHARACTERS
TO PRODUCE A LCV ACTION
XXXXXXXXXX
EO22: 22 ;TEST NUMBER
EO23 ;NEXT TEST
PRTHDR ;TYPE HEADER
EQ22A: MOV #60,REPT ;LOAD 0 AS INITIAL CHARACTER
1S: MOV WIDTH,R2 ;SET COLUMN COUNT
2S: MOV REPT,R0 ;SET CHAR
PRINTC ;PRINT CHAR
DEC R2 ;DEC COLUMN COUNT
BEQ 3S ;BRANCH IF DONE LINE
MOV #3410,R0 ;
DELAY ;DELAY 1.0 SEC.
BR 2S ;OUTPUT NEW CHAR.
3S: CRLF ;SEND A CR AND LF
BR 1S ;

```

LA36 ECHO TESTS

Address	Hex	Hex	Hex	Hex	Text
7400	012272	116	125	114	MONIC: .ASCII /NUL /
7500	012275	040			
7600	012276	123	117	110	.ASCII /SOH /
7700	012302	123	124	130	.ASCII /STX /
7800	012305	040			
7900	012306	105	124	130	.ASCII /ETX /
8000	012311	040			
8100	012312	105	117	124	.ASCII /EOT /
8200	012315	040			
8300	012316	105	116	121	.ASCII /ENQ /
8400	012321	040			
8500	012322	103	103	113	.ASCII /ACK /
8600	012325	040			
8700	012326	102	105	114	.ASCII /BEL /
8800	012332	102	123	040	.ASCII /RS /
8900	012335	040			
9000	012336	110	124	040	.ASCII /HT /
9100	012341	040			
9200	012342	114	106	040	.ASCII /LF /
9300	012345	040			
9400	012346	126	124	040	.ASCII /VT /
9500	012352	040			
9600	012355	106	106	040	.ASCII /FF /
9700	012356	103	122	040	.ASCII /CR /
9800	012361	040			
9900	012362	123	117	040	.ASCII /SO /
10000	012365	040			
10100	012366	123	111	040	.ASCII /SI /
10200	012372	104	114	105	.ASCII /DLE /
10300	012375	040			
10400	012376	104	103	061	.ASCII /DC1 /
10500	012401	040			
	012405	103	103	062	.ASCII /DC2 /
	012406	040			
	012411	104	103	063	.ASCII /DC3 /
	012412	040			
	012415	104	103	064	.ASCII /DC4 /
	012416	116	101	113	.ASCII /NAK /
	012421	040			
	012422	123	131	116	.ASCII /SYN /
	012425	040			
	012426	105	124	102	.ASCII /ETB /
	012431	040			
	012433	103	101	116	.ASCII /CAN /
	012435	040			
	012436	105	115	040	.ASCII /EM /

LA36 ECHO TESTS

10600	012441	040			
10700	012445	123	125	102	.ASCII /SUB /
10800	012446	105	123	103	.ASCII /ESC /
10900	012451	040			
11000	012455	106	123	040	.ASCII /FS /
11100	012456	107	123	040	.ASCII /GS /
11200	012461	040			
11300	012462	122	123	040	.ASCII /RS /
11400	012465	040			
	012466	125	123	040	.ASCII /US /
	012471	040			
	012475	123	120	040	.ASCII /SP /
	012476	040			
	012477	105			.EVEN

```

11600
11700
11800
11900
12000
12100
12200
12300
12400
12500
12600
12700 012476 000233
12800 012509 013020
12900 012502 104016
13000 012504 104020
13100 012506 012700 000036
13200 012512 104010
13300 012514 026727 166160 000041
13400 012522 103015
13500 012524 004767 000130
13600 012530 116700 166144
13700 012536 006300
13800 012538 006300
13900 012540 062700 012272
14000 012544 004767 000166
14100 012548 104000
14200 012552 014321
14300 012554 000753
14400 012556 026727 166116 000177
14500 012560 014721
14600 012566 012701 013010
14700 012572 116721 166102
14800 012578 112721 000040
14900 012584 112721 000040
15000 012590 112721 000040
15100 012612 004767 000042
15200 012616 012700 013010
15300 012624 004767 000110
15400 012626 000750
15500 012630 004767 000024
15600 012634 012700 013014
15700 012640 104000 000072
15800 012644 104000
15900 012646 014321
16000 012650 104000
16100 012652 104000
16200 012654 104000
16300 012656 000712
16400 012660 012701 000003
16500 012664 014321
16600 012670 062701 000003
16700 012674 016700 166004
16800 012700 042700 177770
16900 012704 062700 000060
17000 012710 110041
17100 012712 005302
17200 012714 001407

```

```

;XXXXXXXXXX
;E023-- CHARACTER CODE TEST-- ANY CHARACTER SELECTED
; WILL BE ECHOED ALONG WITH ITS OCTAL CODE.
; A MNEMONIC WILL BE PRINTED INSTEAD OF THE CHARACTER
; IF IT IS A NON-PRINTING CHARACTER.
; THE PARITY OF THE RECEIVED CODE WILL ALSO BE
; INDICATED AS EITHER EVEN OR ODD.
;XXXXXXXXXX
E023: 23 ;TEST NUMBER
E024 ;NEXT TEST
PRTHDR ;TYPE HEADER
;GO WAIT FOR CHARACTER
;DELAY FOR HALF DUPLEX
1S: READ ;TEST IF CHAR IS PRINTABLE
MOV #30,R0 ;BRANCH IF IT IS
DELAY TEMPCH,#41 ;STORE CODE INTO MESSAGE
PC,STRLN ;GET CODE AGAIN
MOV TEMPCH,R0 ;MULT BY 4
R0 ;ADD ADDR OF MNEMONIC TABLE
ADD #MONIC,R0 ;MOV MNEMONIC TO MESSAGE
JSR PC,MOVNUM ;TYPE CODE AND MNEMONIC
;ADDRESS OF MESSAGE
2S: E023M ;GO WAIT FOR NEXT CHARACTER
;TEST IF CHAR IS A RUBOUT
;BRANCH IF RUBOUT
BP 1S
CMP TEMPCH,#177
REQ 4S
MOV #MG24,R1
MOV TEMPCH,(R1)+
MOV #40,(R1)+
MOV #40,(R1)+
MOV #40,(R1)+
JSR PC,STRLN ;STORE CODE INTO MESSAGE
MOV #MG24,R0 ;ADDR OF CHAR INTO R0
JSR PC,MOVNUM ;MOV CHAR INTO MESSAGE
;TYPE MESSAGE
;RUBOUT, CONVERT AND STOR CODE
4S: JSR PC,STRLN ;ADDR. OF DEL INTO R0
MOV #MG25,R0 ;TYPE MESSAGE
JSR PC,MOVNUM ;ADDR OF MESSAGE
;TYPE MESSAGE
;ADDRESS OF MESSAGE
E023M ;CHAIN TO NEXT TEST
;REPEAT TEST
1S: BR ;COUNT OF 3 TO R2
MOV #3,R2 ;ADDR OF MESC TO R1
MOV #1,R1 ;POINT TO LAST SPACE IN MESC
1S: MOV PCHAR,R0 ;MOVE OCTAL CODE TO R0
BIC #177770,R0 ;SAVE LS OCTAL CHAR
ADD #60,R0 ;MAKE ASCII
MOV #60,(R1) ;MOVE INTO MESC
DEC R2 ;DECREMENT CHAR COUNTER
BEQ 2S ;BRANCH IF 3 MOVED
;XXXXXXXXXX

```

```

17300 012716 006267 165762
17400 012718 006267 165762
17500 012726 006267 165752
17600 012732 000760
17700 012734 000207
17800 012736 012701 014327
17900 012742 012702 000004
18000 012746 112021
18100 012750 005302
18200 012752 001375
18300 012754 105767 165722
18400 012760 001003
18500 012762 012700 014371
18600 012766 000402
18700 012770 012700 014375
18800 012774 012702 000004
18900 013000 112021
19000 013002 005302
19100 013004 001375
19200 013006 000207
19300
19400 013010 040 040 040 MG24: .ASCII / / ;SAVE CHARACTER CODE
013013 040
19500
19600
19700
19800 013014 104 105 114 MG25: .ASCII /DEL / ;MNEMONIC FOR RUBOUT
013017 040
19900
20000 .EVEN

```

```
20200 ;XXXXXXXXXX  
20300 ;E024-- SELECTED PATTERN ECHO TEST-- SELECT 1 TO 256  
20400 CHARACTERS. EACH WILL BE ECHOED  
20500 AND STORED UNTIL THE CNTL/C IS SELECTED.  
20600 AT THAT TIME ALL CHARACTERS WILL BE PRINTED AS  
20700 A CONTINUOUS STRING UNFIL EITHER THE RUBOUT IS  
20800 SELECTED TO TERMINATE OR THE CNTL/C IS SELECTED  
20900 AGAIN. A TERMINATING CNTL/C FOLLOWED BY ANOTHER  
21000 CNTL/C WILL ALWAYS CAUSE THE LAST INPUTTED STRING TO  
21100 BE PRINTED. A TERMINATING CNTL/C FOLLOWED BY A CHARACTER OTHER THAN A  
21200 RUBOUT WILL CAUSE A NEW STRING TO BE INPUTTED.  
21300 ;XXXXXXXXXX  
21400  
21500 013020 000024 E024: 24 ;TEST NUMBER  
21600 013022 013566 E025 ;NEXT TEST  
21700 013024 104016 PPTHDR ;TYPE TEST HEADER  
21800 013026 005001 CLR R1 ;CLEAR CHARACTER COUNT  
21900 013030 012702 013164 MOV #RUBFR,R2 ;ADDRESS OF BUFFER TO R2  
22000 013034 104020 1S: READ ;WAIT FOR INPUT  
22100 013036 012700 000036 MOV #30.,R0 ;DELAY FOR HALF DUPLEX  
22200 013042 104010 DELAY  
22300 013044 022710 000177 165626 CMP #177,TEMPCH ;TEST IF RUBOUT  
22400 013052 001440 BEQ TERM ;BRANCH IF RUBOUT  
22500 013054 012767 000003 165616 CMP #3,TEMPCH ;TEST IF CNTL-C  
22600 013062 014417 BEQ INPUT ;BRANCH IF CNTL-C  
22700 013064 020127 000400 CMP R1,#256. ;YES, CHECK IF CHAR CNT IS EQ, GT 256  
22800 013070 103361 BHIS ;BRANCH IF YES, IGNORE CHAR  
22900 013072 116727 165602 MOVB TEMPCH,(R2)* ;STORE CHAR INTO BUFFER  
23000 013076 005207 INC R1 ;INCREMENT CHARACTER COUNT  
23100 013080 103614 PRNT ;CHECK IF PRINTER READY  
23200 013102 116777 165572 165510 MOVB TEMPCH,ATPB ;ECHO CHAR  
23300 013110 000751 BR 1S ;GO WAIT FOR NEXT CHAR  
23400 ;  
23500 ;SECTION TO OUTPUT CONTINUOUS STRING  
23600 ;  
23700 013112 020227 013164 OUTPUT: CMP R2,#RUBFR ;CHECK IF POINTER IS AT START OF TABLE  
23800 013114 001403 BEQ 1S ;YES, BRANCH  
23900 013120 116722 165554 MOVB TEMPCH,(R2)* ;NO, STORE ^C IN TABLE  
24000 013124 104013 SCPLF ;SEND A CR LF  
24100 013126 012702 013164 1S: MOV #RUBFR,R2 ;BUFFER ADDRESS TO R2  
24200 013132 021477 000003 CMP R2,#3 ;CHECK IF FIRST CHAR IS ^C  
24300 013136 001443 BEQ E024B ;YES, LOOK FOR INPUT AGAIN  
24400 013140 112200 2S: MOVB (R2)+,R0 ;GET CHARACTER  
24500 013142 020627 000003 CMP R0,#3 ;DONE STRING?  
24600 013146 012767 BEQ 1S ;YES, RESTART STRING  
24700 013150 104015 PRINTC ;PRINT CHAR  
24800 013152 000777 BR 2S ;CONTINUE  
24900 013154 104007 TERM: TYPEM ;OUTPUT TERMINATION MESSAGE  
25000 013160 E025MB  
25100 013160 CHAIN ;CHAIN TO NEXT TEST  
25200 013162 000721 BR E024B ;REPEAT TEST  
25300 013164 000003 BUFR: 3 ;INITIALIZE FIRST CHAR AS CNTL-C IN TABLE  
25400 013166 .BLKB 256. ;256 CHARACTER BUFFER
```

```
25600 ;XXXXXXXXXX  
25700 ;E025-- BELL ECHO TEST-- A MESSAGE IS PRINTED AND  
25800 THE TEST WAITS FOR SOME PRINTABLE CHARACTER  
25900 TO BE SELECTED ON THE KEYBOARD (GT040). THIS  
26000 TEST IS VALID ONLY IF THE PAPER WIDTH IS GT 64  
26100 COLUMNS. IF LTES COLUMNS AN ILLEGAL BELL TEST  
26200 MESSAGE IS PRINTED.  
26300 ;XXXXXXXXXX  
26400 ;  
26500 ;  
26600 ;  
26700 013566 000025 E025: 25 ;TEST NUMBER  
26800 013570 012116 E020 ;NEXT TEST HEADER  
26900 013572 104016 PPTHDR ;PRINT HEADER  
27000 013574 026727 165052 000101 1S: WIDTH,#101 ;TEST IF COLUMN COUNT IS EQ,GT 64  
27100 013602 103427 BLD 4S ;BRANCH IF NOT  
27200 013604 104007 TYPEM ;TYPE TEST MESC  
27300 013606 014145 BR ;  
27400 013610 000442 BR 3S ;WAIT FOR CHAR  
27500 013612 104000 TYPE ;TYPE TEST MESC ON TERM CHAR RCVD ON  
27600 013614 014145 E025MA  
27700 013616 104020 3S: READ ;  
27800 013620 012700 000036 MOV #30.,R0 ;WAIT FOR OPERATOR RESPONSE  
27900 013624 104010 DELAY ;DELAY FOR HALF DUPLEX  
28000 013626 026727 165046 000040 CMP TEMPCH,#40 ;TEST IF PRINTABLE  
28100 013634 103770 000177 165034 BLD 3S ;CHECK IF CHAR IS RUBOUT  
28200 013636 022767 000177 165034 BEQ #177,TEMPCH ;BRANCH IF NON-PRINTABLE  
28300 013644 001410 BEQ 5S ;BRANCH IF YES  
28400 013646 104017 PRNT ;CHECK IF PRINTER IS READY  
28500 013650 116777 165024 164742 MOVB TEMPCH,ATPB ;PRINT CHAR. (BELL SHOULD SOUND)  
28600 013656 104013 SCPLF ;SEND A CR LF  
28700 013660 000754 BR 2S ;REPEAT  
28800 013662 104007 4S: TYPEM ;TYPE ERROR MESSAGE  
28900 013664 014245 E025MB  
29000 013666 104007 5S: TYPEM ;PRINT TERMINATION  
29100 013670 014272 E025MB  
29200 013672 104005 CHAIN ;EXIT TO NEXT TEST  
29300 013674 000737 BR 1S ;REPEAT TEST
```


100				.SRTTL	MISC. DIAGNOSTIC MESSAGES
200				STARTM:	.ASCII <7><2><ACRLF><17>/CZLACEO LA36 TERM (DL11 & KL11)/<ACRLF>
300	013676	007	002		
	013701	017	103		
	013704	114	103		
	013707	105	060		
	013712	114	101		
	013715	066	040		
	013718	105	122		
	013723	040	050		
	013726	114	061		
	013731	040	046		
	013734	113	114		
	013737	061	051		
400	013742	114	101		.ASCII /LA36 TERMINAL DIAGNOSTIC/<ACRLF>
	013745	066	040		
	013750	105	122		
	013753	111	116		
	013756	114	040		
	013761	111	101		
	013764	116	117		
	013767	124	111		
	013772	200			
500	013773	064	114		.ASCIZ /DL11 & KL11 INTERFACE/<ACRLF><12>
	013776	061	040		
	014001	040	113		
	014004	061	061		
	014007	115	115		
	014012	101	103		
	014015	101	103		
	014020	200	012		
600	014023	200	012		ENDPAS: .ASCII <ACRLF><12>/END OF PASS /
	014026	116	106		
	014031	117	106		
	014034	120	101		
	014037	123	040		
	014042	060	060		
700	014045	060	200		PASMES: .ASCIZ /0000/<ACRLF><12>
	014050	000			
800	014051	200	103		DL11S: .ASCII <ACRLF>/CONSOLE & /
	014054	116	117		
	014057	114	105		
	014062	046	040		
900	014064	060	040		DL11S1: .ASCIZ /00 DL11'S UNDER TEST/<ACRLF><12>
	014067	104	114		
	014072	061	047		
	014075	040	125		
	014100	104	105		
	014103	040	122		
	014106	040	124		
	014111	012	200		
1000	014113	007	002		HDRMSC: .ASCIZ <7><2><ACRLF><17><12>/TEST #/
	014116	017	012		
	014121	105	124		
	014124	040	043		
1100	014127	060	060		HDR0: .ASCIZ /000 COLUMNS/<ACRLF><12>
	014132	040	103		

```

014135 114 125 115
014140 112 123 200
014143 012 000
1200 014145 124 131 120 E025MA: .ASCII /TYPE ANY PRINTABLE CHARACTER /
014150 116 131 101
014153 116 122 040
014156 120 122 111
014161 116 124 101
014164 116 103 101
014167 040 103 101
014172 101 122 101
014175 103 124 105
014178 103 040
1300 014202 101 114 104 .ASCIZ /AND LISTEN FOR BELL...../
014205 040 114 111
014210 123 124 105
014213 116 122 105
014216 116 122 040
014221 102 105 114
014224 114 056 056
014227 116 056 056
014230 029 056 056
014233 116 056 056
014236 056 056 056
014240 056 000 056
1400 014243 116 116 117 E025MB: .ASCIZ <ACRLF>/NOT ENOUGH COLUMNS/<ACRLF>
014250 124 040 105
014253 116 117 125
014256 103 110 040
014259 103 114 114
014264 125 115 116
1500 014267 123 200 000 E025M: .ASCIZ / / / ;MSG FOR TEST E024
014270 210 115 040 LINE5A: .ASCIZ / /<ACRLF>
014300 124 105 123
014303 124 040 124
014306 105 122 124
014311 111 116 115
014314 124 105 104
014317 200 000
1600 014323 040 040 040
1700 014326 040 040 040
1800 014329 040 040 040
014332 040 040 040
014335 000 000 200
1900 014340 000 017 012 MESG3: .ASCIZ <ACRLF><17><12>/SELECT TEST NUMRER /
014343 200 103 124
014346 116 124 101
014352 040 124 105
014355 123 124 040
014358 103 125 115
014361 103 125 115
014366 040 040 000
2000 014371 105 126 105 EVEN: .ASCII /EVEN/
014374 116

```

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2100 014375 117 104 104 ODD: .ASCII /ODD /
014400 040 131 120 OPMSG: .ASCIZ /TYPE ANY CHARACTER/
2200 014401 124 101 101
014404 105 040 101
014407 116 131 040
014412 103 110 101
014415 122 111 103
014420 124 105 122
014423 000
2300 014424 125 123 105 NOSWR: .ASCIZ /USE SOFTWARE SWITCH REG AT MEMORY ADDR 176/<7>
014427 040 123 117
014432 106 124 105
014435 101 122 105
014440 040 123 127
014443 111 123 103
014446 110 040 122
014451 105 107 040
014454 101 124 040
014457 115 103 115
014462 117 122 131
014465 040 101 104
014470 104 122 040
014473 061 122 066
014476 004 000
2400
2500
2600 000001 .END

```

ACRLF = 000200	CHAIN = 001412	E025MA = 014145	PRCTAB = 002522	START3 = 000772
ADJR4 = 012032	CHAINV = 001534	E025MR = 014245	PRINTC = 104015	STLSRV = 003406
ADTENP = 004100	CHALT = 104006	ERR = 003320	PRNT = 104017	STLSPV = 003356
AREAD = 104021	CHLT = 000720	ERRHLT = 003354	PRTHDR = 104016	STPCRV = 104004
AT0 = 005265	CKPOS = 011764	ERRR = 104301	PRV4 = 000200	STPPA = 003374
AT0X = 005270	CNTLSW = 000634	EVEN = 104301	PRV7 = 000340	STPPA = 003374
AT1 = 005320	CNTR = 000716	FORWD = 104024	PSW = 177775	STRDRV = 104003
AT10 = 005744	CNVCTR = 004072	FORWDA = 003614	PT0 = 007372	STRLN = 012660
AT11 = 005800	CMAADD = 000602	FORWDB = 003622	PT1 = 007446	SWREC = 000176
AT12 = 006042	CONIT = 003710	FSTDL = 000632	PT10 = 011266	TEMP = 000712
AT13 = 006116	CONSET = 003714	HDRMSG = 014113	PT11 = 011424	TEMPCH = 000700
AT14 = 006175	CONVEC = 000604	HDR0 = 014137	PT12 = 011456	TENPWR = 004076
AT15 = 006262	COUNT3 = 000600	HERE = 011532	PT17A = 011464	TERM = 013154
AT16 = 006362	CR = 104032	ICTR = 000660	PT17B = 011546	TESTC = 002460
AT17 = 006430	CRBUF = 000646	IDEZ = 007676	PT17D = 011576	TIMER = 000672
AT2 = 005352	CRFL = 104012	INCHK = 000710	PT2 = 007570	TKB = 000614
AT20 = 006500	CTRA = 000650	LEVEL = 000654	PT3 = 010164	TKLVL = 000624
AT21 = 006572	CURTST = 000676	LF = 104014	PT4 = 010304	TKS = 000612
AT22 = 006672	DELAY = 104010	LFCNT = 000706	PT5 = 010462	TRVTR = 000622
AT24 = 007000	DIGIT = 004074	LINE3 = 010444	PT5AL = 010630	TB = 000620
AT24 = 007112	DIRTN = 012112	LINES = 014323	PT6 = 010666	TBPS = 004004
AT25 = 007212	DISPRE = 000174	LOCISA = 014322	PT7 = 011054	TPLVL = 000630
AT26 = 007270	DLADR = 000606	LSC11 = 001000	READ = 104020	TPS = 000616
AT3 = 005404	DLCNT = 000656	LSI11 = 001000	READC = 104025	TPSS = 004002
AT4 = 005436	DLHR = 000610	MACHR = 000004	READI = 004212	TPTR = 000626
AT5 = 005526	DLV = 003436	MESC3 = 014341	REP = 010414	TTVCTL = 104011
AT6 = 005604	DL11S = 014051	MG24 = 013010	REPT = 000662	TTY1 = 001776
AT7 = 005674	DL11S1 = 014064	MG25 = 013014	RESTR = 000656	TTYB = 002062
BIT0 = 000001	ECODND = 014272	MONIC = 014272	RND = 000630	TYPE = 104000
BIT1 = 000002	EHALT = 104002	MOVNUM = 012736	SAVR6 = 003514	TYPM = 003164
BIT10 = 002000	EMIT = 003346	NEXT = 001654	SCOPSW = 040000	WAITP = 001700
BIT11 = 004000	EMTWT = 002722	NEXT1 = 001674	SCRLF = 104013	WIDTH = 000652
BIT12 = 010000	EMTAB = 002776	NTTRSW = 004000	SELHLT = 000734	XCSR = 000670
BIT13 = 020000	ENDPAS = 014023	NOSMR = 014424	SKIP = 001630	SAREAD = 003640
BIT14 = 040000	END2 = 001332	NPCODE = 010137	SPARET = 003072	SRTASC = 004006
BIT15 = 100000	END2A = 001320	NXTST = 000640	SPROT = 000606	SCRLF = 003216
BIT2 = 000004	END3 = 012162	ODD = 014375	SPC = 007560	SPDRWD = 003562
BIT3 = 000010	END4 = 001334	OPFN = 000000	SPCNT = 000674	SIF = 003216
BIT4 = 000020	EO20 = 012116	OPMSG = 014401	SPSP = 007552	SPRHR = 003216
BIT5 = 000040	EO21 = 012166	OUTPUT = 013112	SR = 000714	SPRNT = 004314
BIT6 = 000100	EO21A = 012174	PARTY = 007072	START = 001010	SPRTC = 004324
BIT7 = 000200	EO22 = 012224	PASNT = 012114	STARTM = 013676	SREAD = 004112
BIT8 = 000400	EO22A = 012232	PASNES = 014042	STARTX = 001024	SREADC = 004204
BIT9 = 001000	EO23 = 012476	PCHAR = 000704	START1 = 000736	SSCRLF = 003142
BRCR = 000664	EO23M = 014321	PFALL = 003460	START2 = 000754	
BTOASC = 104023	EO24 = 013020	POPSP = 005726		
BUF = 013164	EO24B = 013026	POPSP2 = 022626		
CHAIN = 104005	EO25 = 013566	PRCID = 000644		

* ABS. 014500 000
 000000 001
 ERRORS DETECTED: 0

VIRTUAL MEMORY USED: 2846 WORDS (12 PAGES)
 DYNAMIC MEMORY: 3844 WORDS (14 PAGES)
 ELAPSED TIME: 00:00:52
 CZLACE.BIN,CZLACE.LST-SP=CZLACE.MAC