

digital**MAINDEC CHANGE
NOTICE**

CHANGE NO.

11-D8DB- 5

Sheet 1 of 1

AUTHOR J. Friedrich	PROGRAM DATE DEC. 71	PRODUCT LINE PDP-11	MAINDEC NUMBER 11-D8DB
DATE 12/13/71	EXT. 3246		

PROGRAM NAME Synchronous interface diagnosti**DEVICE** PDP-11

ITEM 1-2-3	<p>PROBLEM: This is a composit of all MCN's on this program.</p> <p>A. Eliminates Vector initialization bug.</p> <p>B. Eliminates a "RCV active" problem associated with bus buffered systems.</p> <p>C. Eliminates a software bug discovered when transmitter buffer ECO was implemented.</p> <table border="0"> <tr> <td>CORRECTION:</td> <td>LOCATION</td> <td>FROM</td> <td>TO</td> <td>;RESULT</td> </tr> <tr> <td></td> <td>1266</td> <td>Ø1Ø2Ø3</td> <td>Ø1Ø213</td> <td></td> </tr> <tr> <td></td> <td>3666</td> <td>ØØØØØ4</td> <td>ØØ4ØØ4</td> <td>;Clears "RCV active", "Maintenance Mode".</td> </tr> <tr> <td></td> <td>6ØØ6</td> <td>116777</td> <td>Ø16777</td> <td>;Changes MOV BYTE to MOV WORD</td> </tr> </table>	CORRECTION:	LOCATION	FROM	TO	;RESULT		1266	Ø1Ø2Ø3	Ø1Ø213			3666	ØØØØØ4	ØØ4ØØ4	;Clears "RCV active", "Maintenance Mode".		6ØØ6	116777	Ø16777	;Changes MOV BYTE to MOV WORD																				
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4.	<p>A. 11/45 ONLY.</p> <p>PROBLEM: It appears that at the present level of investigation that there is a "shut down" problem going from one test to the next when running on 11/45. The following patch adds an additional SYNC character to the start up routines.</p> <table border="0"> <tr> <td>CORRECTION:</td> <td>LOCATION</td> <td>FROM</td> <td>TO</td> </tr> <tr> <td></td> <td>7010</td> <td>2</td> <td>3</td> </tr> <tr> <td></td> <td>7476</td> <td>2</td> <td>3</td> </tr> </table> <p>B. Documentation Change.</p> <p>Paragraph 9.1.1 LINE.N LINE NUMBER Halt is at location 1152 no 1052 The reasoning behind developing this scheme of selecting line number and vector address was to force production to configure add-ons as per the key sheet. The routine LINE.N accepts consol switches SW8-SWØ as the vector address of DP11 ZERO (17477Ø) and SW15-SW9 on the octal line number. That is if SW15-SW9 is set to 1 the DP11 address generated is 17476Ø, 2 is 17475Ø, etc.</p>	CORRECTION:	LOCATION	FROM	TO		7010	2	3		7476	2	3																												
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5. 7/18/72	<p>11/05 only -</p> <p>To hear bell make following patch:</p> <table border="0"> <tr> <td>010206:</td> <td>004737</td> <td>017110:</td> <td>105737</td> </tr> <tr> <td>010210:</td> <td>017110</td> <td>017112:</td> <td>177564</td> </tr> <tr> <td>010212:</td> <td>000240</td> <td>017114:</td> <td>100375</td> </tr> <tr> <td></td> <td></td> <td>017116:</td> <td>012737</td> </tr> <tr> <td>017032:</td> <td>004737</td> <td>017120:</td> <td>000207</td> </tr> <tr> <td>017034:</td> <td>017110</td> <td>017122:</td> <td>177566</td> </tr> <tr> <td>017036:</td> <td>000240</td> <td>017124:</td> <td>105737</td> </tr> <tr> <td></td> <td></td> <td>017126:</td> <td>177564</td> </tr> <tr> <td></td> <td></td> <td>017130:</td> <td>100375</td> </tr> <tr> <td></td> <td></td> <td>017132:</td> <td>000207</td> </tr> </table>	010206:	004737	017110:	105737	010210:	017110	017112:	177564	010212:	000240	017114:	100375			017116:	012737	017032:	004737	017120:	000207	017034:	017110	017122:	177566	017036:	000240	017124:	105737			017126:	177564			017130:	100375			017132:	000207
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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-08DB-D
PRODUCT NAME: DP11A SYNCHRONOUS LINE UNIT
DATE CREATED: AUGUST 1971
MAINTAINER: DIAGNOSTIC GROUP
AUTHOR: JOHN FRIEDRICH

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M. C. N. REQUIRED
THIS PROGRAM REQUIRES MCMS
IN ORDER TO WORK PROPERLY

1. ABSTRACT

THIS MAINDEC CONSISTS OF TWO PROGRAMS, FIRSTLY, A DP11A EXERCISER WHICH IS RUN WITH A TEST CONNECTOR (DB25S) IN PLACE OF THE MODEM. THE FUNCTION OF THIS TEST IS TO CHECK OUT THE CABLE (BC01R-25) AND FUNCTIONAL INTERFACE WITH THE MODEM. THIS TEST IS RUN UNDER A SIMULATED (SOFTWARE) CLOCK THAT RUNS AT APPROXIMATELY 54KHZ.

SECONDLY, THERE IS THE PRINCIPLE DIAGNOSTIC FOR THE DP11. THIS PROGRAM RUNS IN THE MAINTENANCE MODE WITH THE 9C01R-25 CABLE REMOVED FROM THE SYSTEM UNIT. THIS TEST PROVIDES COMPLETE DIAGNOSTICS FOR THE DP11-DA AND DP11-CA.

2. REQUIREMENTS

2.1 EQUIPMENT

PDP11/20
DB25S TEST CONNECTOR (IF CABLE TEST IS TO BE RUN)
DP11-DA
DP11-CA (OPTIONAL)

2.2 STORAGE

THIS PROGRAM USES MEMORY TO LOCATION 16774.

3. LOADING PROCEDURE

THIS PROGRAM'S OBJECT TAPE IS PUNCHED IN ABSOLUTE FORMAT. THE ABS LOADER IS USED TO LOAD THE PROGRAM.

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

SWITCH 7 INDICATES TO THE PROGRAM THAT THIS IS THE FIRST PASS OR THAT A NEW DP11 LINE IS TO BE SELECTED FOR TEST (SEE 4.3 OPERATOR ACTION)

SWITCH 8 SELECTS THE DP11-CA OPTION FOR TEST

4.2 STARTING ADDRESSES

200 * START ADDRESS FOR MAINTENANCE MODE DIAGNOSTICS (CABLE MUST BE PULLED FROM THE SYSTEM UNIT)

210 * START ADDRESS FOR BC01R-25 CABLE TEST (DB25S TEST CONNECTOR MUST BE PLUGED IN)

4.3 OPERATOR ACTION

4.3.1 IF SWITCH 7 WAS LEFT UP THE PROGRAM WILL HALT AT LOCATION 1052 AND REQUIRE THE FOLLOWING OPERATOR ACTION:

A) SW0-SW8 MUST BE SET TO THE VECTOR ADDRESS OF THE FIRST DP11.

B) SW9-SW15 MUST BE SET TO THE OCTAL LINE NUMBER OF THE DP11 TO BE TESTED. E.G, THE FIRST DP11 IS LINE 0.

PRESS CONTINUE, ZERO SWITCHES AND RESELECT AS PER 5.1.1 "SWITCH SETTINGS".

ALL DP11 ADDRESSES SHALL BE ASSIGNED FROM 774777 TO 774400 (CONTIGUOUSLY):

I.E.	1ST DP11	774776	XMIT	BUFFER
		774774	XMIT	STATUS
		774773	SYNC	BUFFER
		774772	RCV	BUFFER
		774770	RCV	STATUS
	2ND	774766		
		774764		
		774762		
		774760		
	32ND	774406		
		774404		
		774402		
		774400		

- 4.3.2 FOR CABLE TEST REMOVE BC01R-25 CABLE FROM MODEM AND PLUG THE DB25S TEST CONNECTOR SOCKET INTO THE CABLE.
- 4.3.3 FOR THE MAINTENANCE MODE TEST THE CABLE MUST BE REMOVED FROM THE DEVICE SYSTEM UNIT.
- 5. OPERATING PROCEDURE
 - 5.1.1 SWITCH SETTINGS (APPLICABLE TO BOTH TESTS)
 - SW15 = 1 OR UP ... HALT ON ERROR
 - SW14 = 1 OR UP ... SCOPE LOOP
 - SW13 = 1 OR UP ... INHIBIT PRINTOUT
 - SW11 = 1 OR UP ... INHIBIT ITERATION
- 6. ERRORS
 - 6.1 ERROR PRINTOUT
 - PRINTS ALL ERRORS UNLESS INHIBITED BY SWITCH 13.
 - 6.1.1 ERRORS ARE REPORTED THROUGH AN EMULATOR TRAP TO ERRP. THIS ROUTINE PRINTS THE OCTAL EQUIVALENT OF THE CONTENTS OF THE STACK. FOR EXAMPLE, ASSUME THAT AN ERROR WAS DETECTED IN AN INTERRUPT SERVICE ROUTINE. THE PRINTOUT WOULD BE THE PROGRAM COUNTER PC AND STATUS PS OF THE ERROR REPORT TRAP FOLLOWED BY THE PC AND PS OF THE MAINLINE CODE.

6.2 ERROR RECOVERY

A. IF IN A SCOPE LOOP, RESET SWITCH 14.

B. TO RECOVER FROM HALT ON ERROR, MAKE SURE SW14 IS RESET THEN DEPRESS CONTINUE.

NOTE: SINCE DATA TRANSMISSION MUST BE CONTINUOUS A HALT ON ERROR MAY CAUSE AN AVALANCHE OF ERRORS, IF THIS HAPPENS USE STEP C.

C. RELOAD SA AND START.

7. RESTRICTIONS

7.1 STARTING RESTRICTIONS

SEE 4.1 AND 4.3.1

7.2 OPERATING RESTRICTIONS

7.2.1 CABLE TEST (SA#210) MUST BE RUN WITH DB25S CONNECTOR IN PLACE OF A MODEM.

7.2.2 MAINTENANCE MODE DIAGNOSTIC MUST BE RUN WITH CABLE REMOVED FROM SYSTEM UNIT.

8. MISCELLANEOUS

8.1 EXECUTION TIME

THE PROGRAM RINGS THE TELETYPE BELL APPROXIMATELY EVERY 4 MINUTES.

9. PROGRAM DESCRIPTION

9.1 INITIALIZATION ROUTINES

THE START CODE FOR BOTH THE MAINTENANCE MODE AND THE CABLE TEST INITIALIZES THE PROCESSOR PRIORITY TO LEVEL SEVEN AND SETS THE STACK POINTER TO ADDRESS 1000. CONSOL SWITCH SEVEN IS THEN EXAMINED TO DETERMINE IF THIS IS THE FIRST PASS OR A NEW LINE IS TO BE SELECTED FOR TEST. IF SWITCH SEVEN IS UP TWO SUBROUTINES (CLRVEC,LINE,N) ARE EXECUTED BEFORE THE TEST SECTION IS ENTERED.

9.1.1 CLRVEC, CLEAR-VECTOR-AREA

THE SUBROUTINE "CLEAR-VECTOR-AREA" LOADS THE COMMUNICATION VECTOR AREA WITH ,*2,HALT. THIS CAUSES ANY ILLEGAL INTERRUPTS TO TRAP TO THERE STATUS WORD.

9.1.2 LINE,N; LINE NUMBER

THE FUNCTION OF THIS SUBROUTINE IS TO SAVE SWITCH EIGHT OF THE CONSOL (SW8 SELECTS DP11-CA OPTION) AND WAIT FOR OPERATOR ACTION TO SPECIFY THE LINE NUMBER AND FIRST DP11 VECTOR ADDRESS. WHEN THE PROGRAM HALTS AT LOCATION 001052 SWITCHES SW0 THRU SW8 MUST BE SET TO THE VECTOR ADDRESS OF THE FIRST DP11 AND SWITCHES SW9 THRU SW15 MUST BE SET TO THE OCTAL EQUIVILANT OF THE LINE NUMBER (E.G. THE FIRST LINE IS LINE 0(0) THE TENTH LINE IS LINE 11(8)); FOLLOWING THIS ACTION "CONTINUE" ENTERS THE PROGRAM INTO THE SELECTED TEST SECTION. IF SWITCH SEVEN IS NOT UP WHEN "START" IS DEPRESSED THE PROGRAM ASSUMES THIS A RERUN OF THE SAME HARDWARE CONFIGURATION AND EXECUTES THE TESTS USING THE SAME PPARAMETERS PREVIOUSLY SELECTED.

9.2 MAINTENANCE MODE TESTS

IN AN EFFORT TO OPTIMIZE CORE UTILIZATION MANY OF THE DIAGNOSTIC TEST WERE WRITTEN IN SUBROUTINE FORMAT VERSUS MACROS.

9.2.1 BITST, BIT TEST

THIS SUBROUTINE IS ENTERED WITH A JSR X5, BITST, IMMEDIATELY FOLLOWING THIS INSTRUCTION IS THE BIT SELECTED FOR TEST, THE BIT NUMBER IS FETCHED BY THE SUBROUTINE AND STORED IN LOCATION "BITS", USING A SEQUENCE OF "BIS" "BIT" AND "BIC" INSTRUCTIONS EACH READ/WRITE BIT OF THE TRANSMITTER AND RECEIVER CSR (TCSR, RCSR) IS TESTED TO VERIFY THAT AT LEAST THAT PARTICULAR BIT CAN BE REFERENCED AND IS IN FACT READ/WRITE, NO ATTEMPT IS MADE AT THIS POINT TO CHECK FOR ILLEGITIMATE INTERACTION.

9.2.2 RESET TEST

THIS IS A SIMPLE TEST THAT MERELY WRITES INTO ALL WRITEABLE BITS OF THE TCSR AND RCSR, CHECKS THAT THEY WERE SET, ISSUES "RESET" AND CHECKS THAT ALL BITS THAT ARE SUPPOSED TO BE CLEARED BY RESET WERE.

9.2.3 VALID

THE FUNCTION OF THIS SUBROUTINE IS TO TEST FOR INTERACTION BETWEEN READ/WRITE BITS OF THE TCSR AND RCSR, THIS ROUTINE IS ENTERED WITH A JSR REGISTER FIVE, FOLLOWED BY THE BIT NUMBER, THE SELECTED BIT IS SET AND THEN THE ENTIRE CSR IS COMPARED WITH THE WORD (BITS) USED TO SET THE SELECTED BIT, IF ANY OTHER BIT IS SET AN ERROR IS REPORTED, LOCATION "REG" CONTAINS THE ADDRESS OF THE CSR SELECTED FOR TEST, AN EXAMINATION OF THIS CSR SHOULD REVEAL A BIT SET OTHER THAN THE ONE IN LOCATION "BITS".

9.2.4 CLEAR

THIS SUBROUTINE IS ENTERED THE SAME WAY AS BITST, AND VALID ARE ENTERED, ITS FUNCTION IS TO TEST FOR INTERACTION BETWEEN ANY CSR BITS DURING A BIT CLEAR INSTRUCTION, THIS IS ACCOMPLISHED BY SETTING ALL READ/WRITE BITS OF THE SELECTED CSR AND MAKING A DUPLICATE BIT MAP IN TMPDAT, THEN "BITS" IS USED TO CLEAR A SINGLE BIT IN THE CSR AND TMPDAT, FOLLOWING THIS THE CSR IS COMPARED WITH TMPDAT TO VERIFY THAT ONLY THAT BIT WAS CLEARED.

9.2.5 PRIORITY TESTS

WITH THE PROCESSOR PRIORITY AT LEVEL FIVE "STATUS-INTERRUPT-ENABLE" (SIE) IS SET AND ALL THE BITS THAT SHOULD CAUSE A STATUS INTERRUPT ARE SET INDIVIDUALLY AND COLLECTIVELY SET, SECONDLY SIE IS REMOVED AND THE PROCESSOR PRIORITY IS LOWERED TO FOUR, AGAIN THE CSR BITS THAT CAUSE "STATUS INTERRUPTS" ARE SET AND RESET, FINALLY THE SIE BIT IS SET WHILE THE PROCESSOR PRIORITY IS AT FOUR AND IT IS VERIFIED THAT EACH DISCRETE EVENT THAT SHOULD CAUSE A STATUS INTERRUPT DOES, THIS SEQUENCE TESTS THAT THE DP11 STATUS BITS INTERRUPT AT THE PROPER PROCESSOR PRIORITY, THE NEXT SEQUENCE OF PRIORITY TESTS VERIFY THE TRANSMITTER INTERRUPTS BY LOADING THE TRANSMIT BUFFER, ENABLING THE MAINTENANCE MODE COUNTER AND WAITING FOR AN INTERRUPT, IF NO INTERRUPT IS RECEIVED WITHIN 10 CHARACTER TIMES AN ERROR IS REPORTED.

9.2.6 SYNCHRONIZATION TESTS

THE FIRST SYNC TEST (SRW0) VERIFIES THE READ/WRITE CAPABILITY OF THE SYNC REGISTER 174XX3 AND THE SYNC EXTENSION 174XX7 WHEN THE DP11-CA OPTION EXISTS, THIS IS ACCOMPLISHED BY WRITING AND READING ALL POSSIBLE SYNC CHARACTERS (0 THRU 377(8) FOR THE SYNC REG AND 0 THRU 17(8) FOR THE SYNC EXTENSION),

THE NEXT SYNC TEST (SYNC0) ISSUES TWO OF EVERY POSSIBLE SYNC CHARACTER IN EACH OF THE AVAILABLE CHARACTER LENGTH AND CHECKS THAT TWO OF EACH SYNC RAISES "RECEIVER ACTIVE", THEN THE THIRD SYNC IS TRANSMITTED AS DATA, THIS CHECKS THE CAPABILITY OF THE RECEIVER TO INTERRUPT AND ALSO CHECKS THE RECEIVER BUFFER FOR DATA RECEPTION ACCURACY, THIS TEST IS FIRST RAN BY LOADING THE TRANSMIT BUFFER UNDER SOFTWARE CONTROL THEN IS REPEATED IN THE IDLE MODE, THIS CHECKS THAT EACH AND EVERY POSSIBLE SYNC CHARACTER CAN BE TRANSMITTED IN THE IDLE MODE IN THE EVENT THAT AN ERROR IS DETECTED IN THE LAST TWO SYNC TEST AND THE "HALT-ON-ERROR" SWITCH IS UP A SCOPE LOOP MAY BE RUN, THIS IS ACCOMPLISHED BY REMOVING "HALT-ON-ERROR" SW15, SETTING "SCOPE", INHIBIT PRINT, AND PRESSING CONTINUE, THIS CAUSES INCREMENT INSTRUCTION TO BE SKIPPED AND THEREFORE LOOP ON THE SAME SYNC CHARACTER.

9.2.7 INTERRUPT DRIVEN SEQUENTIAL DATA TEST

SYNC IS ESTABLISHED THROUGH THE TRANSMISSION TWO SYNC CHARACTERS, ONCE SYNC IS ESTABLISHED A BINARY COUNT PATTERN IS TRANSMITTED THE SIZE OF WHICH IS DETERMINED BY THE MAXIMUM CHARACTER SELECTED FOR TEST (8 BITS/CHARACTER OR 12/8 BITS/CHARACTER IF THE CA OPTION EXISTS), AT THE COMPLETION OF THE BINARY COUNT PATTERN "ACTIVE" IS DROPPED AND THE NEXT SHORTEST CHARACTER LENGTH IS SELECTED, THIS TEST IS REPEATED FOR THREE CHARACTER LENGTHS (12,11,10, OR 8,7,6).

FUNCTIONALLY THIS TEST VERIFIES THE CAPABILITY OF THE DP11 TO MAINTAIN SYNC OVER A LONG CHARACTER STRING.

IN THE EVENT THAT AN ERROR IS DETECTED AND "HALT-ON-ERROR" IS UP REMOVE IT, SET "INHIBIT PRINT" AND "SCOPE" AND PRESS CONTINUE, THIS PROCEDURE WILL PREVENT THE BINARY COUNT FROM INCREMENTING AND CAUSES THE INTERRUPT SERVICE ROUTINES TO RUN CONTINUOUSLY.

9.2.8 RANDOM DATA, RANDOM STALL

THIS INTERRUPT DRIVEN TEST TRANSMITS RANDOM DATA FOR A PERIOD OF TIME (0 TO 0.65 SECONDS, 0 TO 260 CHARACTERS) DETERMINED BY A RANDOM GENERATOR. AT THE EXPIRATION OF THE DATA TIME INTERVAL THE "IDLE" MODE IS ENTERED AND SYNC CHARACTERS ARE TRANSMITTED FOR A RANDOM PERIOD OF TIME. WHEN THE IDLE TIME TERMINATES THE DATA MODE IS RESTARTED AND NEW DATA IS TRANSMITTED FOR A NEW TIME INTERVAL.

THIS VERIFIES THAT THE DP11 CAN SWITCH BETWEEN DATA MODE AND IDLE AT RANDOM.

9.2.9 PARITY TEST

THE PARITY TEST CONSISTS OF A TRANSMITTER INTERRUPT SERVICE ROUTINE THAT TRANSMITS A BINARY COUNT PATTERN AND A RECEIVER INTERRUPT SERVICE ROUTINE THAT CALCULATES THE PARITY ON THE EXPECTED DATA, COMPARES THE RECEIVED DATA WITH THE EXPECTED DATA, AND FINALLY TESTS THE PARITY BIT (BIT 12=0 FOR EVEN, 1 FOR ODD).

9.2.10 RECEIVER OVERRUN TEST

THIS TEST TRANSMITS TWO SYNC CHARACTERS TO RAISE "ACTIVE" FOLLOWED BY TWO DATA CHARACTERS. RECEIVER INTERRUPT ENABLE IS NOT SET THEREFORE "RECEIVER OVERRUN" SHOULD SET AND CAUSE A TRANSMITTER STATUS INTERRUPT. THIS SEQUENCE IS REPEATED FOR A FULL BINARY COUNT.

9.2.11 HALF DUPLEX TEST

THE HALF DUPLEX BIT SHOULD PREVENT ANY DATA FROM ENTERING THE RECEIVER WHILE SEND-REQUEST IS UP. TO VERIFY THIS RECEIVER INTERRUPT ENABLE IS SET WHILE THE TRANSMITTER IDLES FOR APPROXIMATELY 30MS. FOR EACH POSSIBLE CHARACTER AVAILABLE IN THE 8 BIT/CHAR SET, ANY DATA ENTRY INTO THE RECEIVER WILL CAUSE A TRAP TO AN ERROR ROUTINE.

9.3 CABLE TEST

THE CABLE TEST REQUIRES THE LEAST AMOUNT OF EFFORT AND THEREFORE CAN BE RUN AS A QUICK CONFIDENCE CHECK. THE OPERATING PROCEDURE IS TO DISCONNECT THE BC01R-25 CABLE FROM THE MODEM AND PLUG IT INTO THE B025S TEST CONNECTOR. FROM THIS POINT ON THE OPERATING PROCEDURE IS THE SAME AS THE MAINTENANCE MODE DIAGNOSTIC. THE PRINCIPLE DIFFERENCE BETWEEN THE CABLE TEST AND THE MAINTENANCE MODE TEST IS THE CLOCK. THE MAINTENANCE MODE TEST RUNS OFF OF A FREE RUNNING 3KHZ MULTI-VIBRATOR WHERE AS THE CABLE TEST OPERATES OFF A SOFTWARE CLOCK. SETTING BIT 3 OF THE TRANSMITTER STATUS RAISES THE CLOCK, CLEARING IT LOWERS THE CLOCK. THE SOFTWARE CLOCK THEREFORE HAS A FREQUENCY RANGE OF ZERO TO 50KHZ. THIS ENABLES THE PROGRAM TO STEP THROUGH THE TRANSMIT-RECEIVE SEQUENCE ONE BIT AT A TIME. IT ALSO VERIFIES THE 10KHZ CABLE SPEC AND 50KHZ LOGIC SPEC.

9.3.1 DELAY N

THE MACRO CALL DELAY, CAUSES THE PROCESSOR TO STAY APPROXIMATELY N TIMES 10 MICROSECONDS.

9.3.2 JLOCK

CLOCK IS THE SUBROUTINE TO RUN THE SOFTWARE CLOCK, IT IS ENTERED BY A JSR X5, CLOCK FOLLOWED BY THE NUMBER OF CYCLES DESIRED, UPON ENTRY THE SUBROUTINE FETCHES THE CYCLE COUNT AND EXAMINE BITS OF SAVS1 TO DETERMINE IF 8 BITS/CHAR OR 12 BITS/CHAR HAVE BEEN SELECTED FOR TEST, IF THE 12 BIT MODE HAS BEEN SELECTED 4 IS ADDED TO THE CLOCK COUNT AND BIT 10 OF THE RECEIVER STATUS IS SET BEFORE EXECUTING THE CLOCKING INSTRUCTIONS, EMBEDDED WITHIN THE CLOCKING INSTRUCTIONS IS TWO MACRO CALLS (DELAY N) TO SLOW DOWN THE CLOCK, WITH DELAY 1 THE SOFTWARE CLOCK RUNS AT APPROXIMATELY 25 KHZ, THIS MACRO ENABLES THE OPERATOR TO SLOW THE CLOCK DOWN TO ALMOST ZERO CPS, THIS CAN BE USEFULL IN DETERMING IF A BUG IF FREQUENCY DEPENDENT.

9.3.3 MCLOCK

THIS MACRO CALL IS ANOTHER SOFTWARE CLOCK, IT WAS WRITTEN FOR CODE THAT IS INDEPENDENT OF 12/8 BITS PER CHARACTER OPTION. MCLOCK N EXECUTES N SOFTWARE CYCLES, MCLOCK ALSO HAS THE DELAY MACRO EMBEDDED WITHIN ITS DEFINITION, HOWEVER, BECAUSE IT IS A MACRO THE DELAY INSTRUCTIONS WOULD HAVE TO BE MODIFIED EACH TIME THE MACRO IS CALLED.

9.3.4 REE

REE IS A UTILITY SUBROUTINE TO REINITIALIZE THE DP11 STATUS REGISTER, INTERRUPT VECTOR AND SELECT THE 12/8 BITS PER CHARACTER MODE. THE ENTRY REGISTER IS R5, THE ADDRESS TO WHICH THIS SUBROUTINE RETURNS IS A FUNCTION OF THE NUMBER OF BITS PER CHARACTER SELECTED FOR TEST, IF 8 BITS PER CHARACTER IS SELECTED THE SUBROUTINE RETURNS TO AN INSTRUCTION THAT SETS UP THE DATA LIMIT FOR THAT MODE, IF THE TWELVE BIT PER CHARACTER MODE IS SELECTED THE CONTENTS OF REGISTER 5 IS MODIFIED AND SUBROUTINE RETURNS TO THE INSTRUCTION THAT SETS UP THE TWELVE BIT LIMIT.

9.3.5 SYNCHRONIZATION CHARACTER TESTS

FOLLOWING STATUS REGISTER AND VECTOR INITIALIZATION THE CLOCK IS RUN FOR 30 CYCLES TO CLEAR OUT ANY PREVIOUS DATA THAT MAY BE RESIDING IN THE TRANSMIT OR RECEIVE BUFFERS, AT THIS POINT THE "TRANSMITTER DONE" AND "TRANSMITTER INTERRUPT ENABLE" ARE SET CAUSING AN INTERRUPT TO A SYNCHRONIZATION SUBROUTINE, TV18, TV18 LOADS THE TRANSMIT BUFFER WITH A SYNC CHARACTER, UPON RETURN FROM THE INTERRUPT SERVICE ROUTINE THE SOFTWARE CLOCK RUNS FOR 3 CYCLES, THIS SHOULD BE SUFFICIENT TO RAISE "SEND REQUEST"; IF NOT AN ERROR IS REPORTED, THE SOFTWARE CLOCK THEN GENERATOR ENOUGH CYCLES TO TRANSMIT EXACTLY ONE CHARACTER AND EXAMINES "RECEIVE ACTIVE", IF "RECEIVER ACTIVE" IS UP THE RECEIVER IS PREMATURELY ACTIVE AND AN ERROR IS REPORTED, THE NEXT SET OF CYCLES GENERATED IS ONE SHORT OF THE NUMBER REQUIRED TO TRANSMIT A FULL CHARACTER.

AGAIN "RECEIVER ACTIVE" IS TESTED FOR A PREMATURE RESPONSE

ONE MORE CYCLE IS THEN GENERATED AND "ACTIVE" SHOULD BE UP, TO VERIFY THAT IT WAS THE TRANSMITTED DATA THAT RAISED "ACTIVE" AND NOT NOISE A THIRD SYNC IS TRANSMITTED AND CHECKED AS DATA, THE SEQUENCE IS CONTINUED FOR COMPLETE SET OF POSSIBLE SYNC CHARACTERS (1 TO LIMIT), IN EACH OF THE THREE AVAILABLE CHARACTER LENGTHS, THIS SET OF TESTS ALSO HAS THE SCOPE LOOP FACILITY WHERE THE SAME SYNC CHARACTER IS NOT CHANGED IF THE SCOPE SWITCH SW14 IS UP,

9.3.6 SEQUENTIAL DATA

THIS TEST IS THE SAME AS THAT RUN IN THE MAINTENANCE MODE TEST, IT'S PRINCIPLE OBJECTIVE IS TO VERIFY THE 50KHZ SPEC OF THE DP11. THE SOFTWARE CLOCK THAT DRIVES THIS TEST OPERATES AT APPROXIMATELY 56KHZ,

9.3.7 RANDOM DATA, RANDOM IDLE

THIS TEST IS SIMILAR TO THE RANDOM DATA TEST RUN IN THE MAINTENANCE MODE, THE DIFFERENCE IS THAT IN GOING FROM "IDLE" TO "DATA", "ACTIVE" IS DROPPED AND THE RECEIVER RESYNCD,

9.3.8 SEND-REQUEST TEST

IN THIS TEST "SEND REQUEST" IS RAISED BY LOADING THE TRANSMIT BUFFER AND GENERATING 3 CYCLES, IF THE CABLE IS WIRED PROPERLY "SEND REQUEST" SHOULD RAISE "CLEAR-TO-SEND" AND "MODEM READY" (DATA SET READY), THIS TEST IS REPEATED IN THE 8, 7, AND 6 BITS PER CHARACTER MODE.

9.3.9 TERMINAL READY

THE FUNCTION OF THIS TEST IS TO VERIFY THAT WITH THE DB25S TEST CONNECTOR IN PLACE, SETTING "TERMINAL READY" RAISES "CARRIER" AND "RING FLAG", THIS TEST ALSO VERIFIES "RING FLAG" AND "CARRIER DOWN FLAG" INTERRUPT,

JDP11A SYNCHRONOUS MODEM INTERFACE DIAGNOSTIC
 J*****MAINTENANCE MODE*****
 JCOPYRIGHT, DIGITAL EQUIPMENT CORPORATION*****
 JMAYNARD, MASSACHUSETTS 01754
 JPROGRAMMER: JOHN FRIEDRICH

JMAINDEC-11-08DB

JEQUALITIES

100000	BIT15=100000
040000	BIT14=40000
020000	BIT13=20000
010000	BIT12=10000
004000	BIT11=4000
002000	BIT10=2000
001000	BIT9=1000
000400	BIT8=400
000200	BIT7=200
000100	BIT6=100
000040	BIT5=40
000020	BIT4=20
000010	BIT3=10
000004	BIT2=4
000002	BIT1=2
000001	BIT0=1
000000	R0=X0
000001	R1=X1
000002	R2=X2
000003	R3=X3
000004	R4=X4
000005	R5=X5
000006	R6=X6
000006	SP=X6
000007	PC=X7
177776	PS=177776
104000	ERROR=EMT
177570	SWR=177570
104400	SCOPE=TRAP
000240	NOP=240
104001	SAVREG=EMT+1
104002	RESTOR=EMT+2

JTRAP INITIALIZATION

000100	,REPT	100
		,+2
		HALT
	,ENDR	
		,+2
		HALT
		,+2
000000	000002	
000002	000000	
000004	000006	

000006	000000	HALT
000010	000012	,+2
000012	000000	HALT
000014	000016	,+2
000016	000000	HALT
000020	000022	,+2
000022	000000	HALT
000024	000026	,+2
000026	000000	HALT
000030	000032	,+2
000032	000000	HALT
000034	000036	,+2
000036	000000	HALT
000040	000042	,+2
000042	000000	HALT
000044	000046	,+2
000046	000000	HALT
000050	000052	,+2
000052	000000	HALT
000054	000056	,+2
000056	000000	HALT
000060	000062	,+2
000062	000000	HALT
000064	000066	,+2
000066	000000	HALT
000070	000072	,+2
000072	000000	HALT
000074	000076	,+2
000076	000000	HALT
000100	000102	,+2
000102	000000	HALT
000104	000106	,+2
000106	000000	HALT
000110	000112	,+2
000112	000000	HALT
000114	000116	,+2
000116	000000	HALT
000120	000122	,+2
000122	000000	HALT
000124	000126	,+2
000126	000000	HALT
000130	000132	,+2
000132	000000	HALT
000134	000136	,+2
000136	000000	HALT
000140	000142	,+2
000142	000000	HALT
000144	000146	,+2
000146	000000	HALT
000150	000152	,+2
000152	000000	HALT
000154	000156	,+2
000156	000000	HALT
000160	000162	,+2
000162	000000	HALT

000164	000166	,+2
000166	000000	HALT
000170	000172	,+2
000172	000000	HALT
000174	000176	,+2
000176	000000	HALT
000200	000202	,+2
000202	000000	HALT
000204	000206	,+2
000206	000000	HALT
000210	000212	,+2
000212	000000	HALT
000214	000216	,+2
000216	000000	HALT
000220	000222	,+2
000222	000000	HALT
000224	000226	,+2
000226	000000	HALT
000230	000232	,+2
000232	000000	HALT
000234	000236	,+2
000236	000000	HALT
000240	000242	,+2
000242	000000	HALT
000244	000246	,+2
000246	000000	HALT
000250	000252	,+2
000252	000000	HALT
000254	000256	,+2
000256	000000	HALT
000260	000262	,+2
000262	000000	HALT
000264	000266	,+2
000266	000000	HALT
000270	000272	,+2
000272	000000	HALT
000274	000276	,+2
000276	000000	HALT
000300	000302	,+2
000302	000000	HALT
000304	000306	,+2
000306	000000	HALT
000310	000312	,+2
000312	000000	HALT
000314	000316	,+2
000316	000000	HALT
000320	000322	,+2
000322	000000	HALT
000324	000326	,+2
000326	000000	HALT
000330	000332	,+2
000332	000000	HALT
000334	000336	,+2
000336	000000	HALT
000340	000342	,+2

000342 000000
000344 000346
000346 000000
000350 000352
000352 000000
000354 000356
000356 000000
000360 000362
000362 000000
000364 000366
000366 000000
000370 000372
000372 000000
000374 000376
000376 000000

HALT
,+2
HALT
,+2
HALT
,+2
HALT
,+2
HALT
,+2
HALT
,+2
HALT
,+2
HALT
,+2
HALT
HALT

VECTOR INITIALIZATION
.#24

000024 000024
000024 010746
000026 000340

PFAIL
340

POWER FAIL VECTOR
PRIORITY 7

.#30

000030 000030
000032 010220
000034 011102
000036 000340

EMTVEC
340
SCOPEC
340

ERROR REPORT VECTOR
PRIORITY 7
SCOPE LOOP VECTOR
PRIORITY 7

```

000200 000200 000167 000674 ,=200
          000210 000167 012360 ,=210
          001100 000005 ,=1100
001100 000005 BEGIN1 RESET
001102 012706 001100 MOV #BEGIN1,DP
001106 012767 000340 176662 MOV #340,PS
001114 032767 000200 176446 BIT #BIT7,SWR
001122 001404 BEQ BGN0
001124 004767 000142 JSR X7,CLRVEC
          001130 004767 000004 JSR X7,LINE,N
001134 000167 000416 BGN0 JMP BGN1

```

;LINE,N SUBROUTINE TO FETCH THE LINE
 ;NUMBER AND FIRST DP11 VECTOR ADDRESS FROM
 ;THE CONSOL SWITCHES
 ;SW0-SW8=VECTOR ADDRESS OF FIRST DP11
 ;SW9-SW15=LINE NUMBER OF DP11 SELECTED FOR TEST

```

001140 005067 010166 010100 LINE,N CLR ERRCNT
001144 016767 176420 010100 MOV SWR,SAVSR1
001152 000000 HALT

001154 016767 176410 010072 MOV SWR,SAVSR2

001162 005001 CLR R1
001164 116701 010065 MOVB SAVSR2+1,R1
001170 006201 ASR R1
001172 006301 ASL R1
001174 006301 ASL R1
001176 006301 ASL R1
001200 012702 174770 MOV #174770,R2
001204 160102 SUB R1,R2
001206 012703 011224 MOV #DPRS,R3
001212 010223 MOV R2,(R3)+
001214 005722 TST (R2)+
001216 010223 MOV R2,(R3)+
001220 005202 INC R2
001222 010223 MOV R2,(R3)+
001224 005202 INC R2
001226 010223 MOV R2,(R3)+
001230 005722 TST (R2)+
001232 010223 MOV R2,(R3)+
001234 005202 INC R2
001236 010223 MOV R2,(R3)+
001240 016702 010010 MOV SAVSR2,R2
001244 042702 177000 BIC #177000,R2
001250 060102 ADD R2,R2

```

;SET UP CONSOL SWITCH REGISTER

;DB25S CONNECTOR TEST

;SET UP STACK POINTER
 ;SET PROCESSOR PRIORITY = 7
 ;TEST FOR CHANGE IN DP ADRS
 ;BRANCH IF NO CHANGE
 ;LOAD ENTIRE COMMUNICATION VECTOR AREA WITH
 ; ;+2
 ; HALT
 ;FETCH LINE NUMBER FROM SWR
 ;START TEST

;CLEAR ERROR COUNT
 ;SAVE CONSOL SWITCH SETTINGS
 ;SET SWR TO LINE NUMBER
 ;LOW BYTE = FIRST DP VECTOR
 ;HIGH BYTE = LINE NUMBER(8)
 ;SAVE CONSOL SWITCHES

;SAVE LINE NUMBER
 ;CLEAR LSB
 ;SCALE LINE NUMBER TO ADDRESS
 ;MODULO 10(8)

;SET R2 = LINE 0 ADDRESS
 ;MANUFACTURE DEVICE ADDRESS
 ;R3 = ADDRESS OF RCV STATUS ADRS
 ;LOAD RCV STATUS ADRS
 ;INC TO RCV BUFFER ADRS
 ;LOAD RCV BUFFER ADRS
 ;INC TO SYNC BUFFER ADRS
 ;LOAD SYNC ADRS
 ;INC TO XMIT STATUS ADRS
 ;LOAD TRANSMITTER STATUS ADRS
 ;INC TO XMIT BUFFER
 ;LOAD XMIT BUFFER ADRS
 ;INC TO SYNC EXTENTION
 ;LOAD SYNC EXTENSION ADRS
 ;SET UP VECTOR ADDRESS
 ;CLEAR LINE NUMBER FROM VEC ADRS
 ;SET VECTOR ADDRESS TO LINE NUMBER

```

001252 010223      MOV      R2,(R3)+      ;LOAD RCV VECTOR ADRS
001254 005722      TST      (R2)+        ;INC TO NEXT VECTOR
001256 010223      MOV      R2,(R3)+      ;LOAD RCV PRIORITY ADRS
001260 005722      TST      (R2)+        ;INC TO NEXT VECTOR
001262 010223      MOV      R2,(R3)+      ;LOAD XMIT VECTOR ADRS
001264 005722      TST      (R2)+        ;INC TO NEXT VECTOR
001266 010203      MOV      R2,R3        ;LOAD XMIT PRIORITY ADRS
001270 000207      RTS      X7

```

*****CLRVEC*****

;CLRVEC,ROUTINE TO FILL COMMUNICATION VECTOR AREA WITH ,+2,HALT

```

001272 012702 000300  CLRVEC: MOV      #300,R2      ;R2 COMM VECTOR AREA ADRS
001276 012701 000302  MOV      #302,R1        ;INIT R1 WITH ADRS OF HALT
001302 010122  CV1:    MOV      R1,(R2)+      ;MOV ,+2 TO PC
001304 005022  CLR      (R2)+        ;MOV HALT TO PC
001306 022121  CMP      (R1)+,(R1)+   ;INC TO NEXT VECTOR AREA
001310 022701 000776  CMP      #776,R1      ;END OF VECTOR AREA
001314 001372  BNE      CV1          ;NO
001316 000207  RTS      X7          ;RETURN

```

```

;MACR DELAY N          ;WHERE N=TENS OF MICROSECONDS
MOV      #N,CNT      ;SET UP COUNT
DEL=: DEC      CNT      ;TIME OUT
BNE      DEL        ;NO
;ENDM

```

;BITSR,ROUTINE TO TEST READ WRITE BITS OF STATUS
;THIS ROUTINE VERIFIES THAT EACH READ/WRITE BIT
;CAN BE SET AND CLEARED

EXAMINE LOCATIONS
 IBITS: FOR BIT UNDER TEST
 IREG: FOR REGISTER UNDER TEST

001320	012567	000226		BITSTI	MOV	(R5)+,BITS	ISAVE BIT NUMBER
001324	056777	000222	000222		BIS	BITS,@REG	ISET BIT
001332	036777	000214	000214		BIT	BITS,@REG	IIS BIT SET?
001340	001001				BNE	,+4	IYES
001342	104000				ERROR		IREPORT ERROR
001344	046777	000202	000202		BIC	BITS,@REG	ICLEAR BIT
001352	036777	000174	000174		BIT	BITS,@REG	IIS BIT CLEARED
001360	001401				BEQ	,+4	IYES
001362	104000				ERROR		IREPORT ERROR
001364	056777	000162	000162		BIS	BITS,@REG	ISET BIT
001372	036777	000154	000154		BIT	BITS,@REG	IIS BIT SET
001400	001001				BNE	,+4	IYES
001402	104000				ERROR		IREPORT ERROR
001404	005077	000144			CLR	@REG	ICLEAR REG
001410	036777	000136	000136		BIT	BITS,@REG	IIS BIT CLEARED
001416	001401				BEQ	,+4	IYES
001420	104000				ERROR		IREPORT ERROR
001422	052777	000004	007574		BIS	#BIT2,@DPRS	IKEEP CLOCK HUMMING
001430	000205				RTS	X5	

INVALID, ROUTINE TO TEST FOR ANY INTERACTION BETWEEN BITS
 ITHIS ROUTINE CHECKS THAT WHEN EXECUTING A BIT SET INSTRUCTION
 IONLY THE SPECIFIED BIT IS SET

001432	012567	000114		VALIDI	MOV	(R5)+,BITS	IFETCH BIT NUMBER
001436	056777	000110	000110		BIS	BITS,@REG	ISET BIT
001444	026777	000102	000102		CMP	BITS,@REG	IWAS ONLY THAT BIT SET?
001452	001401				BEQ	,+4	IYES
001454	104000				ERROR		IREPORT ERROR
001456	046777	000070	000070		BIC	BITS,@REG	IRESTORE REG
001464	000205				RTS	X5	IRETURN

ICLEAR, ROUTINE TO TEST THAT BIC ONLY CLEARS SPECIFIED BIT

001466	012567	000060		CLEARI	MOV	(R5)+,BITS	IFETCH BIT NUMBER
001472	046777	000054	000054		BIC	BITS,@REG	ICLEAR BIT
001500	046767	000046	007574		BIC	BITS,TMPDAT	ICLEAR MASK
					DELAY	1600,	IDELAY 16 MS
001506	012767	003100	007554		MOV	#1600,,CNT	ISET UP COUNT
	001514			DEL=.			
001514	005367	007550			DEC	CNT	ITIME OUT
001520	001375				BNE	DEL	I NO
001522	026777	007554	000024		CMP	TMPDAT,@REG	IWERE ANY OTHER BITS CLEARED
001530	001401				BEQ	,+4	I NO
001532	104000				ERROR		IREPORT ERROR
001534	056777	000012	000012		BIS	BITS,@REG	IRESTORE REG
001542	056767	000004	007532		BIS	BITS,TMPDAT	IRESTORE MASK
001550	000205				RTS	X5	IRETURN

001552	000000			BITS:	0
001554	000000			REG:	0

```

I
;*****TEST 1: READ/WRITE ALL BITS OF STATUS*****
BGN1: RESET
001556 000005                                MOV     #340,PS                ;SET PROCESSOR STATUS TO 7
001560 012767 000340 176210                 MOV     #BGN1+2,RETURN        ;SET UP SCOPE RETURN
001566 012767 001560 007362                 MOV     #BGN1,PU1+2          ;SET UP PFAIL RETURN ADRS
001574 012767 001556 007230                 MOV     #400,ICOUNT          ;ITERATION = 400
001602 012767 000400 007342                 CLR     @DPTS                ;CLEAR TRANSMITTER STATUS
001610 005077 007416                          CLR     @DPRS                ;CLEAR RECEIVER STATUS
001614 005077 007404                          MOV     #FTINT,@DPTIV        ;SET UP TRANSMITTER TEST VECTOR 1
001620 012777 011472 007416                 MOV     #FRINT,@DPRIV        ;SET UP RECEIVER TEST VECTOR 1
001626 012777 011476 007404                 MOV     #240,@DPRP           ;SET UP RECEIVER PRIORITY=5
001634 012777 000240 007400                 MOV     #240,@DPTP           ;SET UP TRANSMITTER PRIORITY=5
001642 012777 000240 007376                 MOVB   #26,@SYNC            ;CLEAR NOISE FROM SYNC
001650 112777 000026 007352                 BIS     #BIT2,@DPRS          ;SET MAINTENANCE MODE
001656 052777 000004 007340                 ;TO ENABLE INTERNAL CLOCK (3KHZ)
001664 032777 000004 007332                 ;MAINT, SET
001672 001001                                ;YES
001674 104000                                ;REPORT ERROR
BIT     #BIT2,@DPRS
BNE     ,+4
ERROR

```

IAN ILLEGAL INTERRUPT WILL TRAP TO
 IAN ERROR MESSAGE ROUTINE
 SCOPE

001676 104400

001700	012767	000010	007244	MOV	#10,ICOUNT	ISET ITERATION COUNT TO 10
001706	016767	007312	177640	ITEST	ALL READ/WRITE BITS OF RECEIVER STATUS	
001714	004567	177400		MOV	DPRS,REG	I TEST RECEIVER STATUS BITS
001720	000001			JSR	X5,BITST	ISYNC STRIP
001722	104400			BIT0		
001724	004567	177370		SCOPE		
001730	000002			JSR	X5,BITST	IHALF DUPLEX
001732	104400			BIT1		
001734	004567	177360		SCOPE		
001740	000004			JSR	X5,BITST	IMAINTEANCE MODE
001742	104400			BIT2		
001744	004567	177350		SCOPE		
001750	000100			JSR	X5,BITST	IRECEIVER INTERRUPT ENABLE
001752	104400			BIT6		
001754	004567	177340		SCOPE		
001760	000200			JSR	X5,BITST	IDONE
001762	104400			BIT7		
001764	004567	177330		SCOPE		
001770	000400			JSR	X5,BITST	IBITS/CHAR
001772	104400			BIT8		
001774	004567	177320		SCOPE		
002000	001000			JSR	X5,BITST	I" "
002002	104400			BIT9		
002004	004567	177310		SCOPE		
002010	002000			JSR	X5,BITST	I " "
002012	104400			BIT10		
				SCOPE		

IBIT3=MISCELLANEOUS RECEIVE*READ ONLY
 IBIT11=RECEIVE ACTIVE*READ/WRITE ZERO
 IBIT12=PARITY(VRC)*READ ONLY
 IALL OTHER BITS ARE NOT USED

TEST ALL READ/WRITE BITS OF TRANSMITTER STATUS

002014	016767	007212	177532	MOV	DPTS,REG	TEST TRANS STATUS BITS
002022	004567	177272		JSR	X5,BITST	TERMINAL READY R/W
002026	000001			BIT0		
002030	104400			SCOPE		
002032	042777	000004	007164	BIC	#BIT2,@DPRS	SHUT OFF CLOCK FOR IDLE SYNC
002040	004567	177254		JSR	X5,BITST	IDLE SYNC R/W
002044	000002			BIT1		
002046	104400			SCOPE		
002050	052777	000004	007146	BIS	#BIT2,@DPRS	START CLOCK
002056	004567	177236		JSR	X5,BITST	SECONDARY TRANSMIT R/W
002062	000010			BIT3		
002064	104400			SCOPE		
002066	004567	177226		JSR	X5,BITST	STATUS INTERRUPT ENABLE R/W
002072	000040			BIT5		
002074	104400			SCOPE		
002076	004567	177216		JSR	X5,BITST	TRANSMITTER INTERRUPT R/W
002102	000100			BIT6		
002104	104400			SCOPE		
002106	004567	177206		JSR	X5,BITST	DONE
002112	000200			BIT7		
002114	104400			SCOPE		
002116	004567	177176		JSR	X5,BITST	RING FLAG R/W
002122	020000			BIT13		
002124	104400			SCOPE		
002126	004567	177166		JSR	X5,BITST	CARRIER DOWN
002132	100000			BIT15		
002134	104400			SCOPE		
002136	004567	177156		JSR	X5,BITST	RECEIVER OVERUN FLAG R/W
002142	040000			BIT14		
002144	104400			SCOPE		

IRESET TEST
 ISET PROCESSOR PRIORITY TO 7
 ISET ALL WRITE BITS IN T & R STATUS
 IISSUE RESET AND VERIFY ALL BITS THAT ARE
 ITO BE CLEARED BY RESET--WERE

002146	012767	000340	175622	MOV	#340,PS	IPRIORITY = 7
002154	005077	007052		CLR	@DPTS	ICLEAR TRANSMITTER STATUS
002160	005077	007040		CLR	@DPRS	ICLEAR RECEIVER STATUS
002164	052777	000004	007032	BIS	#BIT2,@DPRS	IMAINTEANCE MODE
002172	012777	160353	007032	MOV	#160353,@DPTS	ISET ALL TRANSMITTER STATUS BITS
002200	012777	143707	007016	MOV	#143707,@DPRS	ISET ALL RECEIVER STATUS BITS

INOTE! IF BITS/CHAR BITS ARE SET TO ALL 1'S RCV WILL
 INOT GO ACTIVE

ITEST READ/WRITE BITS OF RECEIVER STATUS

002206	032777	000001	007010	RWRSI	BIT	#BIT0,@DPRS	ISYNC STRIP SET
002214	001001				BNE	,+4	IYES
002216	104000				ERROR		IREPORT ERROR
002220	032777	000002	006776		BIT	#BIT1,@DPRS	IHALF DUPLEX SET
002226	001001				BNE	,+4	IYES
002230	104000				ERROR		IREPORT ERROR
002232	032777	000004	006764		BIT	#BIT2,@DPRS	IMAINTEANCE MODE SET
002240	001001				BNE	,+4	IYES
002242	104000				ERROR		IREPORT ERROR
002244	032777	000100	006752		BIT	#BIT6,@DPRS	IRCV INT ENB SET
002252	001001				BNE	,+4	IYES
002254	104000				ERROR		IREPORT ERROR
002256	032777	000200	006740		BIT	#BIT7,@DPRS	IRECEIVER DONE
002264	001001				BNE	,+4	IYES
002266	104000				ERROR		IREPORT ERROR
002270	032777	000400	006726		BIT	#BIT8,@DPRS	I#BITS/CHAR (LSB)
002276	001001				BNE	,+4	
002300	104000				ERROR		IREPORT ERROR
002302	032777	001000	006714		BIT	#BIT9,@DPRS	I#BITS/CHAR
002310	001001				BNE	,+4	
002312	104000				ERROR		IREPORT ERROR
002314	032777	002000	006702		BIT	#BIT10,@DPRS	I#BITS/CHAR (MSB)
002322	001001				BNE	,+4	
002324	104000				ERROR		IREPORT ERROR

IVERIFY "RECEIVER ACTIVE" IS READ/WRITE ZERO

002326	032777	004000	006670		BIT	#BIT11,@DPRS	IRECEIVER ACTIVE=WRITE ZERO
002334	001401				BEG	,+4	IYES
002336	104000				ERROR		IREPORT ERROR

ITEST ALL READ/WRITE BITS OF THE TRANSMITTER STATUS

002340	032777	000001	006664		BIT	#BIT0,@DPTS	ITERMINAL READY SET
002346	001001				BNE		IYES

002350	104000			ERROR		IREPORT ERROR
002352	032777	000002	006652	BIT	#BIT1,@DPTS	IIDLE SYNC SET
002360	001001			BNE	,+4	IYES
002362	104000			ERROR		IREPORT ERROR
002364	032777	000010	006640	BIT	#BIT3,@DPTS	IMISC TRANSMIT SET
002372	001001			BNE	,+4	IYES
002374	104000			ERROR		IREPORT ERROR

002376	032777	000040	006626	BIT	#BIT5,@DPTS	I STATUS INTERRUPT ENABLE SET
002404	001001			BNE	,+4	IYES
002406	104000			ERROR		I REPORT ERROR
002410	032777	000100	006614	BIT	#BIT6,@DPTS	I TRANSMITTER READY SET GO
002416	001001			BNE	,+4	IYES
002420	104000			ERROR		I REPORT ERROR
002422	032777	020000	006602	BIT	#BIT13,@DPTS	I RING FLAG SET
002430	001001			BNE	,+4	IYES
002432	104000			ERROR		I REPORT ERROR
002434	032777	040000	006570	BIT	#BIT14,@DPTS	I RECEIVER OVERRUN SET
002442	001001			BNE	,+4	IYES
002444	104000			ERROR		I REPORT ERROR
002446	032777	100000	006556	BIT	#BIT15,@DPTS	I CARRIER DOWN FLAG SET
002454	001001			BNE	,+4	IYES
002456	104000			ERROR		I REPORT ERROR

ISSUE "RESET" AND VERIFY ALL BITS ARE CLEARED

002460	000005			RESET		
002462	032777	000001	006534	BIT	#BIT0,@DPRS	I STRIP SYNC CLEAR
002470	001401			BEQ	,+4	IYES
002472	104000			ERROR		I REPORT ERROR
002474	032777	000002	006522	BIT	#BIT1,@DPRS	I HALF DUPLEX CLEAR
002502	001401			BEQ	,+4	IYES
002504	104000			ERROR		I REPORT ERROR
002506	032777	000004	006510	BIT	#BIT2,@DPRS	I MAINTENANCE MODE CLEAR
002514	001401			BEQ	,+4	IYES
002516	104000			ERROR		I REPORT ERROR
002520	032777	000100	006476	BIT	#BIT6,@DPRS	I RCV INT ENB CLEAR
002526	001401			BEQ	,+4	IYES
002530	104000			ERROR		I REPORT ERROR
002532	032777	000400	006464	BIT	#BIT8,@DPRS	
002540	001401			BEQ	,+4	
002542	104000			ERROR		I REPORT ERROR
002544	032777	001000	006452	BIT	#BIT9,@DPRS	
002552	001401			BEQ	,+4	
002554	104000			ERROR		I REPORT ERROR
002556	032777	002000	006440	BIT	#BIT10,@DPRS	
002564	001401			BEQ	,+4	
002566	104000			ERROR		I REPORT ERROR
002570	032777	000200	006426	BIT	#BIT7,@DPRS	I RECEIVER DONE CLEAR
002576	001401			BEQ	,+4	IYES
002600	104000			ERROR		I REPORT ERROR
002602	005777	006416		TST	@DPRS	I RCV STATUS CLEAR
002606	001401			BEQ	,+4	IYES
002610	104000			ERROR		I REPORT ERROR

VERIFY ALL READ/WRITE BITS OF TRANSMITTER STATUS ARE CLEAR

002612	032777	000001	006412	BIT	#BIT0,@DPTS	!TERMINAL READY CLEAR
002620	001401			BEQ	,+4	!YES
002622	104000			ERROR		!REPORT ERROR
002624	032777	000002	006400	BIT	#BIT1,@DPTS	!IDLE SYNC CLEAR
002632	001401			BEQ	,+4	!YES
002634	104000			ERROR		!REPORT ERROR
002636	032777	000004	006366	BIT	#BIT2,@DPTS	!MISC TRANSMIT CLEAR
002644	001401			BEQ	,+4	!YES
002646	104000			ERROR		!REPORT ERROR
002650	032777	000010	006354	BIT	#BIT3,@DPTS	!LSB OF #BITS/CHARACTER CLEAR
002656	001401			BEQ	,+4	!YES
002660	104000			ERROR		!REPORT ERROR
002662	032777	000020	006342	BIT	#BIT4,@DPTS	!MSB OF #BITS/CHAR CLEAR
002670	001401			BEQ	,+4	!YES
002672	104000			ERROR		!REPORT ERROR
002674	032777	000040	006330	BIT	#BIT5,@DPTS	!STATUS INTERRUPT ENABLE CLEAR
002702	001401			BEQ	,+4	!YES
002704	104000			ERROR		!REPORT ERROR
002706	032777	000100	006316	BIT	#BIT6,@DPTS	!TRANSMITTER INTERRUPT ENABLE CLEAR
002714	001401			BEQ	,+4	!YES
002716	104000			ERROR		!REPORT ERROR
002720	032777	020000	006304	BIT	#BIT13,@DPTS	!RING FLAG CLEAR
002726	001401			BEQ	,+4	!YES
002730	104000			ERROR		!REPORT ERROR
002732	032777	040000	006272	BIT	#BIT14,@DPTS	!RX O/RUN CLEAR
002740	001401			BEQ	,+4	!YES
002742	104000			ERROR		!REPORT ERROR
002744	032777	100000	006260	BIT	#BIT15,@DPTS	!CARRIER DOWN CLEAR
002752	001401			BEQ	,+4	!YES
002754	104000			ERROR		!REPORT ERROR

!TEST READY BIT CLEAR BEFORE READY CAN COME UP

002756	012777	160377	006246	MOV	#160377,@DPTS	!LOAD STATUS
002764	000005			RESET		
002766	032777	000200	006236	BIT	#BIT7,@DPTS	!READY CLEARED
002774	001401			BEQ	,+4	!YES
002776	104000			ERROR		!REPORT ERROR
003000	005777	006226		TST	@DPTS	!STATUS CLEAR
003004	001401			BEQ	,+4	!YES
003006	104000			ERROR		!REPORT ERROR

IBIT INTERACTION TEST
 ISET EACH BIT AND VERIFY THAT ONLY THAT BIT IS AFFECTED

IRECEIVER STATUS BIT VALIDITY TEST

003010	016767	006210	176536	VLIDI	MOV	DPRS,REG	I TEST RCV
003016	104400				SCOPE		
003020	004567	176406			JSR	X5,VALID	I STRIP SYNC
003024	000001				BIT0		
003026	104400				SCOPE		
003030	004567	176376			JSR	X5,VALID	I HALF DUPLEX
003034	000002				BIT1		
003036	104400				SCOPE		
003040	004567	176366			JSR	X5,VALID	I MAINTENANCE MODE
003044	000004				BIT2		
003046	104400				SCOPE		
003050	004567	176356			JSR	X5,VALID	I INTERRUPT ENABLE
003054	000100				BIT6		
003056	104400				SCOPE		
003060	004567	176346			JSR	X5,VALID	I DONE
003064	000200				BIT7		
003066	004567	176340			JSR	X5,VALID	I BITS/CHAR
003072	000400				BIT8		
003074	104400				SCOPE		
003076	004567	176330			JSR	X5,VALID	r" "
003102	001000				BIT9		
003104	104400				SCOPE		
003106	004567	176320			JSR	X5,VALID	I " "
003112	002000				BIT10		
003114	104400				SCOPE		

I TRANSMITTER STATUS BIT VALIDITY TEST

003116	016767	006110	176430		MOV	DPTS,REG	I TEST XMIT STATUS
003124	005077	006102			CLR	@DPTS	I CLEAR TRANSMITTER STATUS
003130	004567	176276			JSR	X5,VALID	I TERMINAL READY
003134	000001				BIT0		
003136	104400				SCOPE		
003140	004567	176266			JSR	X5,VALID	I IDLE SYNC
003144	000002				BIT1		
003146	104400				SCOPE		
003150	004567	176256			JSR	X5,VALID	I MISC TRANSMIT
003154	000010				BIT3		
003156	104400				SCOPE		
003160	004567	176246			JSR	X5,VALID	I STATUS ENABLE
003164	000040				BIT5		
003166	104400				SCOPE		
003170	004567	176236			JSR	X5,VALID	I TRANSMITTER ENABLE
003174	000100				BIT6		
003176	104400				SCOPE		
003200	004567	176226			JSR	X5,VALID	I TRANSMITTER DONE
003204	000200				BIT7		
003206	104400				SCOPE		

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003210 004567 176216
003214 020000
003216 104400
003220 004567 176206
003224 040000
003226 104400
003230 004567 176176
003234 100000

JSR X5,VALID IIRING FLAG
BIT13
SCOPE
JSR X5,VALID IRECEIVER OVERRUN
BIT14
SCOPE
JSR X5,VALID ICARRIER DOWN
BIT15

IVERIFY BIT CLEAR ONLY CLEARS SPECIFIED BIT

IBIT INTERACTION TEST
 ISET EACH BIT AND VERIFY THAT ONLY THAT BIT IS AFFECTED

IRECEIVER STATUS BIT VALIDITY TEST

003010	016767	006210	176536	VALIDI	MOV	DPRS,REG	I TEST RCV
003016	104400				SCOPE		
003020	004567	176406			JSR	X5,VALID	I STRIP SYNC
003024	000001				BIT0		
003026	104400				SCOPE		
003030	004567	176376			JSR	X5,VALID	I HALF DUPLEX
003034	000002				BIT1		
003036	104400				SCOPE		
003040	004567	176366			JSR	X5,VALID	I MAINTENANCE MODE
003044	000004				BIT2		
003046	104400				SCOPE		
003050	004567	176356			JSR	X5,VALID	I INTERRUPT ENABLE
003054	000100				BIT6		
003056	104400				SCOPE		
003060	004567	176346			JSR	X5,VALID	I DONE
003064	000200				BIT7		
003066	004567	176340			JSR	X5,VALID	I BITS/CHAR
003072	000400				BIT8		
003074	104400				SCOPE		
003076	004567	176330			JSR	X5,VALID	r" "
003102	001000				BIT9		
003104	104400				SCOPE		
003106	004567	176320			JSR	X5,VALID	i " "
003112	002000				BIT10		
003114	104400				SCOPE		

ITRANSMITTER STATUS BIT VALIDITY TEST

003116	016767	006110	176430		MOV	DPTS,REG	I TEST XMIT STATUS
003124	005077	006102			CLR	DPTS	I CLEAR TRANSMITTER STATUS
003130	004567	176276			JSR	X5,VALID	I TERMINAL READY
003134	000001				BIT0		
003136	104400				SCOPE		
003140	004567	176266			JSR	X5,VALID	I IDLE SYNC
003144	000002				BIT1		
003146	104400				SCOPE		
003150	004567	176256			JSR	X5,VALID	I MISC TRANSMIT
003154	000010				BIT3		
003156	104400				SCOPE		
003160	004567	176246			JSR	X5,VALID	I STATUS ENABLE
003164	000040				BIT5		
003166	104400				SCOPE		
003170	004567	176236			JSR	X5,VALID	I TRANSMITTER ENABLE
003174	000100				BIT6		
003176	104400				SCOPE		
003200	004567	176226			JSR	X5,VALID	I TRANSMITTER DONE
003204	000200				BIT7		
003206	104400				SCOPE		

IRECEIVER TEST SECTION

```

003236 104400          SCOPE
003240 005067 005706 CLR      ICOUNT      ISET ITERATION COUNT TO 1
003244 112777 000026 005756 MOVB    #26,@SYNC    ILOAD SYNC WITH ANYTHING
003252 016767 005746 176274 MOV     DPRS,REG    ITEST RCV STATUS
003260 012767 003707 006014 MOV     #3707,TMPDAT ISTORE STATUS IMAGE
003266 012777 003707 005730 MOV     #3707,@DPRS ISET UP STATUS
003274 012767 003304 005654 MOV     #CREG,RETURN
003302 104400          SCOPE

003304 004567 176136 CREG1   JSR      X5,CLEAR    ISTRIP SYNC
003310 000001          BIT0
003312 104400          SCOPE
003314 004567 176146 JSR      X5,CLEAR    IHALF DUPLEX
003320 000002          BIT1
003322 104400          SCOPE
003324 004567 176136 JSR      X5,CLEAR    IMAINTENANCE MODE
003330 000004          BIT2
003332 104400          SCOPE
003334 004567 176126 JSR      X5,CLEAR    IRECEIVER INT ENB
003340 000100          BIT6
003342 104400          SCOPE
003344 004567 176116 JSR      X5,CLEAR    IRECEIVER DONE
003350 000200          BIT7
003352 104400          SCOPE
003354 004567 176106 JSR      X5,CLEAR    IBITS/CHAR
003360 000400          BIT8
003362 104400          SCOPE
003364 004567 176076 JSR      X5,CLEAR    ) " "
003370 001000          BIT9
003372 104400          SCOPE
003374 004567 176066 JSR      X5,CLEAR    ) " "
003400 002000          BIT10
003402 104400          SCOPE
003404 012767 000012 005540 MOV     #10,,ICOUNT  ISET ITERATION COUNT TO 10
    
```

ITRANSMITTER TEST SECTION

```

003412 005077 005606 CLR     @DPRS      ICLEAR RECEIVER STATUS
003416 052777 000004 005600 BIS     #BIT2,@DPRS  ISET MAINTENANCE MODE
003424 012777 160353 005600 MOV     #160353,@DPTS ISET UP STATUS
003432 012767 163353 005642 MOV     #163353,TMPDAT ISTORE STATUS IMAGE
003440 012767 001130 005622 DELAY   600,      IDELAY 6MS FOR SEND REQUEST
003446 003446          MOV     #600.,CNT  ISET UP COUNT

003446 005367 005616 DEL=.   DEC     CNT      ITIME OUT
003452 001375          BNE    DEL      INO
003454 032777 001000 005550 BIT     #BIT9,@DPTS ISEND REQUEST UP
003462 001001          BNE    ,+4      IYES
003464 104000          ERROR      IREPORT ERROR
    
```

INOTE: "SEND REQUEST" IS SET BY "IDLE SYNC"
) "CLEAR-TO-SEND" IS SET BY MAINTENANCE MODE

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003466	012767	003476	005462	MOV	#CREG2,RETURN	
003474	104400			SCOPE		
003476	016767	005530	176050	CREG21 MOV	DPTS,REG	I TEST TRANS
003504	004567	175756		JSR	X5,CLEAR	I TERMINAL READY
003510	000001			BIT0		
003512	104400			SCOPE		
				I IDLE SYNC		
003514	042767	003002	005560	BIC	#3002,TMPDAT	I CLEARING IDLE SYNC SHOULD CLEAR SEND REQUEST
003522	042777	000002	005502	BIC	#2,@DPTS	I CLEAR IDLE SYNC
				DELAY	1600,	I WAIT FOR "CLEAR-TO-SEND" TO DROP
003530	012767	003100	005532	MOV	#1600, CNT	I SET UP COUNT
	003536			DEL=,		
003536	005367	005526		DEC	CNT	I TIME OUT
003542	001375			BNE	DEL	I NO
003544	026777	005532	005460	CMP	TMPDAT,@DPTS	I IDLE SYNC AND SEND REQUEST CLEAR
003552	001401			BEQ	,04	I YES
003554	104000			ERROR		I REPORT ERROR
003556	052767	003002	005516	BIS	#3002,TMPDAT	I REINSTATE IMAGE
003564	052777	000002	005440	BIS	#2,@DPTS	I REINSTATE STATUS
003572	104400			SCOPE		
003574	004567	175666		JSR	X5,CLEAR	I MISC TRANSMIT
003600	000010			BIT3		
003602	104400			SCOPE		
003604	004567	175656		JSR	X5,CLEAR	I STATUS INTERRUPT ENABLE
003610	000040			BIT5		
003612	104400			SCOPE		
003614	004567	175646		JSR	X5,CLEAR	I TRANSMITTER INTERRUPT ENABLE
003620	000100			BIT6		
003622	104400			SCOPE		
003624	042777	000004	005372	BIC	#BIT2,@DPRS	I MAINT MODE OFF (STOP CLOCK)
003632	042767	002000	005442	BIC	#BIT10,TMPDAT	I CLEAR "CLEAR-TO-SEND"
003640	004567	175622		JSR	X5,CLEAR	I READY
003644	000200			BIT7		
003646	052777	000004	005350	BIS	#BIT2,@DPRS	I MAINT MODE ON
003654	052767	002000	005420	BIS	#BIT10,TMPDAT	I SET "CLEAR-TO-SEND" TEST BIT
003662	104400			SCOPE		
003664	042777	000004	005332	BIC	#BIT2,@DPRS	I SHUT OFF CLOCK
003672	042767	002000	005402	BIC	#BIT10,TMPDAT	I CLEAR -TO -SEND
003700	004567	175562		JSR	X5,CLEAR	I RING FLAG
003704	020000			BIT13		
003706	104400			SCOPE		
003710	004567	175552		JSR	X5,CLEAR	I RECEIVER OVERRUN
003714	040000			BIT14		
003716	104400			SCOPE		
003720	004567	175542		JSR	X5,CLEAR	I CARRIER DOWN
003724	100000			BIT15		
003726	104400			SCOPE		

IPRIORITY TESTS
 IVERIFY THAT THERE ARE NO STATUS INTERRUPTS
 IWHEN PS=5

003730	012767	004000	005214	MOV	#4000,ICOUNT	IITERATION COUNT=4000
003736	012767	000240	174032	MOV	#240,PS	IPRIORITY#5
003744	052777	000004	005252	BIS	#BIT2,@DPRS	ISET MAINTENANCE MODE
003752	052777	000040	005252	BIS	#BIT5,@DPTS	ISTATUS INTERRUPT ENABLE (SIE)
IINTERRUPT WILL TRAP TO ERROR MESSAGE						
003760	052777	010000	005244	BIS	#BIT12,@DPTS	IIRING FLAG
003766	042777	020040	005236	BIC	#20040,@DPTS	ICLEAR CSR
003774	052777	000040	005230	BIS	#BIT5,@DPTS	IINT ENB (STATUS)
004002	052777	040000	005222	BIS	#BIT14,@DPTS	IRECEIVER OVERRUN FLAG
004010	042777	040040	005214	BIC	#40040,@DPTS	ICLEAR CSR
004016	052777	000040	005206	BIS	#BIT5,@DPTS	IINT ENB (STATUS)
004024	052777	100000	005200	BIS	#BIT1,@DPTS	ICARRIER DOWN FLAG
004032	042777	100040	005172	BIC	#100040,@DPTS	ICLEAR CSR

IVERIFY NO TRANSMITTER READY INTERRUPTS

004040	052777	000100	005164	BIS	#BIT6,@DPTS	IEXIT INT ENB
004046	052777	000001	005156	BIS	#BIT0,@DPTS	I NOISE
004054	052777	000002	005150	BIS	#BIT1,@DPTS	I MORE NOISE
004062	052777	000004	005142	BIS	#BIT2,@DPTS	I MORE NOISE
004070	052777	000010	005134	BIS	#BIT3,@DPTS	I MORE NOISE
004076	052777	000020	005126	BIS	#BIT4,@DPTS	I MORE NOISE
004104	042777	000037	005120	BIC	#37,@DPTS	I QUIET!
004112	042777	000100	005112	BIC	#BIT6,@DPTS	
004120	104400			SCOPE		

TEST FOR CONTROL OF STATUS INTERRUPT ENABLE BIT
 NO INTERRUPT VECTOR SHOULD OCCUR IF INT ENB IN NOT SET
 INTERRUPT VECTOR POINTS TO ERROR MESSAGE ROUTINE

```

004122 012767 000200 173646          MOV      #200,PS          ;PRIORITY=4
004130 052777 020000 005074 INTST1: BIS      #BIT13,#DPTS    ;RING FLAG
004136 042777 020000 005066          BIC      #BIT13,#DPTS    ;CLEAR
004144 052777 040000 005060          BIS      #BIT14,#DPTS    ;RECEIVER OVERRUN FLAG
004152 042777 040000 005052          BIC      #BIT14,#DPTS    ;CLEAR
004160 052777 100000 005044          BIS      #BIT15,#DPTS    ;CARRIER DOWN FLAG
004166 042777 100000 005036          BIC      #BIT15,#DPTS
004174 052777 160000 005030          BIS      #160000,#DPTS   ;SET ALL STATUS ERROR BITS
004202 042777 160000 005022          BIC      #160000,#DPTS   ;CLEAR
004210 162767 000040 173560          SUB      #40,PS          ;DECREASE PRIORITY LEVEL
004216 016767 173554 005056          MOV      PS,TMPDAT       ;STORE PROCESSOR STATUS
004224 042767 000017 005050          BIC      #17,TMPDAT      ;CLEAR T,N,Z,V,C
004232 162767 000040 005042          SUB      #40,TMPDAT      ;HAVE ALL PRIORITY LEVELS BEEN TESTED
004240 100333          BPL      INTST1          ;NO
004242 104400          SCOPE                   ;YES
  
```

VERIFY THAT ALL STATUS BITS INTERRUPT AT ALL LEVELS
 EQUAL TO OR LESS THAN 4
 IF THE DEVICE INTERRUPTS SUCCESSFULLY, THE
 INTERRUPT SERVICE ROUTINE WILL RETURN
 THE PROGRAM COUNTER TO THE INSTRUCTION AFTER
 THE ERROR TRAP

```

004244 012777 004300 004772          MOV      #IT2A,#DPTIV    ;SET UP INTERRUPT VECTOR=RTI
004252 012767 000200 173516          MOV      #200,PS        ;PRIORITY=4
004260 052777 000040 004744 INTST2: BIS      #BIT5,#DPTS    ;INT ENB STATUS
004266 052777 020000 004736          BIS      #BIT13,#DPTS    ;RING FLAG
004274 000240          NOP                      ;SHOULD INTERRUPT AFTER NOP
004276 104000          ERROR                    ;REPORT ERROR
004300 042777 020000 004724 IT2A:  BIC      #BIT13,#DPTS    ;CLEAR RING
004306 022626          CMP      (SP)+,(SP)+     ;ADJUST STACK
004310 012777 004336 004726          MOV      #IT2B,#DPTIV    ;SET UP NEXT INTERRUPT VECTOR
004316 042767 000040 173452          BIC      #BIT5,PS        ;SET PRIORITY TO 4
004324 052777 040000 004700          BIS      #BIT14,#DPTS    ;RECEIVER OVERRUN FLAG
004332 000240          NOP                      ;REPORT ERROR
004334 104000          ERROR                    ;CLEAR RCY 0 RUN
004336 042777 040000 004666 IT2B:  BIC      #BIT14,#DPTS    ;ADJUST STACK
004344 022626          CMP      (SP)+,(SP)+     ;SET UP NEXT INTERRUPT VECTOR
004346 012777 004374 004670          MOV      #IT2C,#DPTIV    ;SET PRIORITY TO 4
004354 042767 000040 173414          BIC      #BIT5,PS        ;CARRIER DOWN FLAG
004362 052777 100000 004642          BIS      #BIT15,#DPTS
004370 000240          NOP                      ;REPORT ERROR
004372 104000          ERROR                    ;CLEAR CARRIER DOWN FLAG
004374 042777 100000 004630 IT2C:  BIC      #BIT15,#DPTS    ;ADJUST STACK
004402 022626          CMP      (SP)+,(SP)+     ;FALSE INT TRAP
004404 012777 011472 004632          MOV      #FTINT,#DPTIV   ;YES
004412 104400          SCOPE
  
```

DOES LOADING XMT BUFFER CLEAR XMT DONE

```

004414 012767 000620 004530      MOV      #400,,ICOUNT      ;SET ITERATION COUNT TO 400
004422 005077 004576                CLR      @DPRS             ;CLEAR RCV STATUS
004426 005077 004600                CLR      @DPTS             ;CLEAR XMIT STATUS
004432 052777 000200 004572      BIS      #BIT7,@DPTS      ;DONE
004440 032777 000200 004564      BIT      #BIT7,@DPTS      ;DONE SET
004446 001001                    BNE      ,+4              ;YES
004450 104000                    ERROR                    ;REPORT ERROR
004452 016777 004624 004554      MOV      TMPDAT,@DPTB     ;LOAD BUFFER
004460 032777 000200 004544      BIT      #BIT7,@DPTS      ;DONE CLEARED
004466 001401                    BEQ      ,+4              ;YES
004470 104000                    ERROR                    ;REPORT ERROR
004472 052777 000004 004524      BIS      #BIT2,@DPRS      ;SET MAINTENANCE MODE

```

VERIFY TRANSMITTER READY INTERRUPTS AT LEVEL 4
 IAT 8 BITS PER CHARACTER

```

004500 005077 004526                TST01  CLR      @DPTS      ;CLR STATUS
004504 012777 004564 004532      MOV      #IT3A,@DPTIV     ;TEST PASS VECTOR = RT1 TO IT3A
004512 012767 000200 173256      MOV      #200,PS          ;PRIORITY=4
004520 116777 004556 004506      INTST3: MOVB     TMPDAT,@DPTB ;LOAD XMIT BUFFER
004526 052777 000100 004476      BIS      #BIT6,@DPTS      ;XMIT INT ENB
004534 032777 000200 004470      BIT      #BIT7,@DPTS      ;READY CLEARED BY BUFF LOAD
004542 001401                    BEQ      ,+4              ;YES
004544 104000                    ERROR                    ;REPORT ERROR
004546 012767 004704 004514      DELAY  MOV      #2500,,CNT  ;25 MS
004554 004554                                ;SET UP COUNT
004554 005367 004510      DEL*1  DEC      CNT          ;TIME OUT
004560 001375                                INO
004562 104000                    ERROR                    ;TRANSMITTER FAILED TO INTERRUPT
004564 042777 000100 004440      IT3A1  BIC      #BIT6,@DPTS     ;CLEAR INT ENB
004572 042767 000040 173176      BIC      #BIT5,PS          ;SET PRIORITY TO 4
004600 022626      CMP      (SP)+,(SP)+      ;ADJUST STACK

```

VERIFY READY INTERRUPTS AT LEVEL 4
 IAT 7 BITS PER CHARACTER

```

004602 005077 004424                CLR      @DPTS             ;CLR STATUS
004606 012777 004674 004430      MOV      #IT4A,@DPTIV     ;TEST PASS VECTOR = IT4A
004614 012767 000200 173154      MOV      #200,PS          ;PRIORITY=4
004622 052777 001000 004374      BIS      #BIT9,@DPRS      ;7 BITS/CHARACTER
004630 116777 004446 004376      INTST4: MOVB     TMPDAT,@DPTB ;LOAD XMIT BUFFER
004636 052777 000100 004366      BIS      #BIT6,@DPTS      ;XMIT INT ENB
004644 032777 000200 004360      BIT      #BIT7,@DPTS      ;LOAD BUFFER CLEARED READY

```

```

004652 001401          BEQ      ,+4          )YES
004654 104000          ERROR     )REPORT ERROR
                                DELAY    2500,          )25 MS
004656 012767 004704 004404          MOV      #2500,,CNT          )SET UP COUNT
                                004664
                                DEL=,
004664 005367 004400          DEC      CNT          )TIME OUT
004670 001375          BNE      DEL          )NO
004672 104000          ERROR     )TRANSMITTER FAILED TO INTERRUPT
004674 042777 001000 004322 IT4AI  BIC      #BIT9,@DPRS )CLR 7 BITS/CHAR
004702 042777 000100 004322          BIC      #BIT6,@DPTS )CLEAR INT ENB
004710 042767 000040 173060          BIC      #BIT5,PS      )SET PRIORITY TO 4
004716 022626          CMP      (SP)+,(SP)+ )ADJUST STACK
004720 104400          SCOPE   )YES

```

VERIFY READY INTERRUPTS AT LEVEL 4
AT 6 BITS PER CHARACTER

```

004722 012767 000012 004222          MOV      #10,,ICOUNT      )SET ITERATION COUNT TO 10
004730 012767 000200 173040          MOV      #200,PS         )PRIORITY=4
004736 005077 004270          CLR      @DPTS           )CLR STATUS
004742 012777 005022 004274          MOV      #IT5A,@DPTIV    )TEST PASS VECTOR = IT5A
004750 052777 002000 004246          BIS      #BIT10,@DPRS    )6 BITS/CHARACTER
004756 116777 004320 004250 IQTST5I MOVB    TMPDAT,@DPTB      )LOAD XMIT BUFFER
004764 052777 000100 004240          BIS      #BIT6,@DPTS     )XMIT INT ENB
004772 032777 000200 004232          BIT      #BIT7,@DPTS     )LOAD BUFFER CLEARED READY
005000 001401          BEQ      ,+4          )YES
005002 104000          ERROR     )REPORT ERROR
                                DELAY    2500,          )25 MS
005004 012767 004704 004256          MOV      #2500,,CNT          )SET UP COUNT
                                005012
                                DEL=,
005012 005367 004252          DEC      CNT          )TIME OUT
005016 001375          BNE      DEL          )NO
005020 104000          ERROR     )TRANSMITTER FAILED TO INTERRUPT
005022 042777 002000 004174 IT5AI  BIC      #BIT10,@DPRS    )CLR 6 BITS/CHAR
005030 005077 004176          CLR      @DPTS           )CLEAR STATUS
005034 022626          CMP      (SP)+,(SP)+ )ADJUST STACK
005036 104400          SCOPE

```

TEST SYNC BUFFER IS READ/WRITE

```

005040 005067 004236          SRW0I  CLR      TMPDAT      )CLEAR TEST DATA
005044 005077 004154          CLR      @DPRS           )CLEAR RECEIVER STATUS
005050 105077 004154          CLR      @SYNC          )CLEAR SYNC
005054 105777 004150          TSTB    @SYNC           )
005060 001401          BEQ      ,+4          )BRANCH IF SYNC CLEARED
005062 104000          ERROR     )REPORT ERROR
005064 116777 004212 004136 SRW1I  MOVB    TMPDAT,@SYNC      )LOAD SYNC
005072 126777 004204 004130          CMPB    TMPDAT,@SYNC    )TEST IF LOAD OK
005100 001401          BEQ      ,+4          )BRANCH OK
005102 104000          ERROR     )REPORT ERROR
005104 005267 004172          INC      TMPDAT          )NEXT SYNC

```

```

005110 122767 000400 004164 CMPB #400,TMPDAT ;HAVE ALL SYNC'S BEEN TESTED
005116 001401 BEQ ,+4 ;YES
005120 000761 BR SRW1 ;NO,TEST NEXT SYNC
005122 112777 000026 004100 MOVB #26,@SYNC ;ANY SYNC BUT ALL 1'S
005130 104400 SCOPE
    
```

;READ/WRITE ALL CHARACTERS IN SYNC EXTENSION

```

005132 032767 000400 004112 BIT #BIT0,SAVSR1 ;12 BITS/CHAR
005140 001431 BEQ SY ;NO, BRANCH AROUND TEST
005142 005067 004134 CLR TMPDAT ;LOAD TMPDAT WITH ZEROS
005146 112777 000017 004062 MOVB #17,@SEXT ;LOAD SYNC EXT WITH 1'S
005154 116777 004122 004054 EXT1: MOVB TMPDAT,@SEXT ;LOAD SYNC EXTENSION
005162 127767 004050 004112 CMPB @SEXT,TMPDAT ;DID SYNC LOAD CORRECTLY
005170 001401 BEQ ,+4 ;YES
005172 104000 ERROR ;REPORT ERROR
005174 005267 004102 INC TMPDAT ;NEXT SYNC
005200 022767 000020 004074 CMP #20,TMPDAT ;HAVE ALL SYNC'S BEEN TESTED
005206 001362 BNE EXT1 ;NO, CONTINUE TEST
005210 105077 004022 CLRB @SEXT ;CLEAR SYNC EXT
005214 105777 004016 TSTB @SEXT ;TEST SYNC EXT
005220 001401 BEQ ,+4 ;BRANCH IF SYNC CLEARED
005222 104000 ERROR ;REPORT ERROR
    
```

;***** SYNC TESTS *****

;SYNCHRONIZATION CHARACTER TEST
;ISSUE ALL SYNC CHARACTERS AND VERIFY THAT IT WAS THE
;CORRECT SYNC

```

005224 105077 004006 SY1 CLRB @SEXT ;CLEAR SYNC EXTENSION
005230 005077 003776 CLR @DPTS ;CLEAR TRANSMITTER STATUS
005234 005077 003764 CLR @DPRS ;CLEAR RECEIVER STATUS
005240 012767 000200 172530 MOV #200,PS ;PRIORITY#4
005246 012767 000377 004024 MOV #377,SLIM ;SYNC LIMIT FOR 8BITS/CHAR
005254 012767 000400 004000 MOV #400,BPC ;INDEX TO CHANGE BITS/CHAR
005262 052777 000004 003734 BIS #BIT2,@DPRS ;MAINT MODE
005270 012767 000001 003770 MOV #1,TSYNC ;FIRST SYNC = 1
005276 012777 011476 003734 SYC02: MOV #FRINT,@DPRIV ;SET UP RECEIVER INT VECTOR TO ERROR
SYC2: DELAY 6000 ;10 CHAR TIMES FOR ALL 1'S IN BUFF
MOV #6000, CNT ;SET UP COUNT
DEL=.
005304 012767 013560 003756 DEL=. DEC CNT ;TIME OUT
005312 005367 003752 BNE DEL ;NO
005316 001375 MOVB TSYNC,@SYNC ;LOAD SYNC BUFFER
005320 116777 003742 003702 MOVB @SYNC,TDATA ;STORE SYNC
005326 117677 003676 003752 MOVB TSYNC,@DPTB ;LOAD FIRST SYNC CHAR
005334 116777 003726 003672 BIT #BIT7,@DPTS ;READY FOR NEXT SYNC
005342 032777 000200 003662
    
```

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005350 001774
005352 032777 004000 003644
005360 001401
005362 104000

BEQ ,=6
BIT #BIT11,0DPRS
BEQ ,*4
ERROR

JNO TEST AGAIN
JTEST FOR PREMATURE ACTIVE
JBRANCH IF NOT SET
JPREMATURE ACTIVE

005364	116777	003676	003642		MOVB	TSYNC, @DPTB	ILOAD SECOND SYNC BYTE
005372	012777	005440	003640		MOV	#SYC2A, @DPRIV	ISET UP TEST VECTOR
005400	105777	003626			TSTB	@DPTS	ITRANSMITTER READY
005404	100375				BPL	, -4	INO
005406	016777	003654	003620		MOV	TSYNC, @DPTB	IXMIT 3ED SYNC AS DATA
005414	052777	000100	003602		BIS	#BIT6, @DPRS	IRCV INT ENB
					DELAY	3000,	ISTALL 10 CHARACTER TIMES
005422	012767	005670	003640		MOV	#3000, ,CNT	ISET UP COUNT
	005430			DEL=,			
005430	005367	003634			DEC	CNT	ITIME OUT
005434	001375				BNE	DEL	INO
005436	104000				ERROR		IREPORT ERROR
005440	017767	003562	003634	SYC2A1	MOV	@DPRB, TMPDAT	ISAVE DATA
005446	026767	003630	003612		CMP	TMPDAT, TSYNC	ICORRECT SYNC CHARACTER
005454	001404				BEQ	SYC2B	IYES
005456	042777	000004	003540		BIC	#BIT2, @DPRS	INO, SHUT OFF CLOCK
005464	104000				ERROR		IREPORT ERROR
005466	032777	000200	003530	SYC2B1	BIT	#BIT7, @DPRS	IDONE CLEARED

```

005474 001401 BEQ ,+4 IYES
005476 104000 ERROR IREPORT ERROR
005500 042777 000100 003516 BIC #BIT6,@DPRS ICLEAR REV INT ENB
005506 032777 004000 003510 BIT #BIT11,@DPRS IRECEIVER ACTIVE
005514 001001 BNE ,+4 IYES
005516 104000 ERROR IREPORT ERROR
005520 112777 000026 003502 MOVB #26,@SYNC ICHANGE SYNC
005526 042777 004000 003470 BIC #BIT11,@DPRS ICLEAR RECEIVER ACTIVE
005534 032777 004000 003462 BIT #BIT11,@DPRS IRCV ACTIVE CLEARED
005542 001401 BEQ ,+4 IYES
005544 104000 ERROR IREPORT ERROR
005546 022626 CMP (SP)+,(SP)+ IADJUST STACK
005550 042767 000040 172220 BIC #BIT5,PS ISET PRIORITY TO 4
005556 032767 040000 172004 BIT #BIT14,SWR ITEST FOR SCOPE LOOP
005564 001002 BNE SYC2C IBRANCH AROUND INC IF SCOPE
005566 105267 003474 INCB TSYNC INEXT SYNC
005572 126767 003502 003466 SYC2C1 CMFB SLIM,TSYNC IHAVE ALL SYNC'S BEEN TESTED
005600 001241 BNE SYC2 INO
005602 005067 003460 CLR TSYNC IYES
005606 056777 003450 003410 BIS BPC,@DPRS IDEC BITS/CHAR BY 1 BIT
005614 006267 003460 ASR SLIM IDECREASE #BITS/CHAR
005620 062767 000400 003434 ADD #400,BPC IDEC BITS/CHAR BY 1 BIT
005626 022767 001400 003426 CMP #1400,BP_ IHAVE ALL CHAR SEIZES BEEN TESTED
005634 001220 BNE SYC02 INO
005636 012767 000376 003434 MOV #376,SLIM ISET UP SYNC LIMIT TO 0BITS/CHAR

```

*****SYNC EXTENSION TEST*****

```

005644 032767 000400 003400 S0,EXT1 BIT #BIT8,SAVSR1 IDOES TWELVE BIT OPTION EXIST
005652 001574 BEQ ISYC IBRANCH IF NOT
005654 042777 003400 003342 BIC #3400,@DPRS ICLEAR BITS/CHARACTER
005662 052777 002104 003334 BIS #2104,@DPRS ISET STATUS TO 12 BITS/CHARACTER
005670 012767 000400 003370 MOV #400,TSYNC IFIRST SYNC CHARACTER
005676 105077 003326 CLRB @SYNC ILOAD SYNC BUFFERS WITH 400
005702 112777 000001 003326 MOVB #1,@SEXT ILOAD SYNC BUFFERS WITH 400
005710 012767 007400 003362 MOV #7400,SLIM ISET UP SYNC LIMIT
005716 012767 002000 003336 MOV #2000,BPC ISET # BITS/CHAR TO 12
005724 012777 011476 003306 S1,EXT1 MOV #FRINT,@DPRIV IRCV INTERRUPT VECTOR = ERROR
                                DELAY 6000 IWAIT FOR ALL 1'S
                                MOV #6000,CNT ISET UP COUNT

005732 012767 006000 003330 DEL=, DEC CNT ITIME OUT
                                005740 BNE DEL INO
005740 005367 003324 ITO SHIFT INTO XMIT,RCV BUFS
005744 001375 ICLEAR SYNC EXTENSION
                                CLRB @SYNC ILOAD NEXT SYNC
                                MOVB TSYNC+1,@SEXT ITRANSMIT FIRST SYNC
                                MOV TSYNC,@DPTB IWAIT FOR "DONE"
                                TSTB @DPTB
                                BPL ,+4
                                BIT #BIT11,@DPTS
                                BEQ ,+4
                                ERROR
                                MOV TSYNC,@DPTB ITEST FOR PREMATURE "ACTIVE"
                                TSTB @DPTS INO
                                BPL ,+4 IREPORT ERROR
                                ITRANSMIT SECOND SYNC
                                IWAIT FOR "DONE"

```

```

005746 105077 003256
005752 116777 003311 003256
005760 016777 003302 003246
005766 105777 003240
005772 100375
005774 032777 004000 003230
006002 001401
006004 104000
006006 116777 003254 003220
006014 105777 003212
006020 100375

```

MOV

φ16777

006022	012777	006102	003210	MOV	#S2,EXT,@DPRIV	ISET UP RECEIVER INT VECTOR
006030	052777	000100	003166	BIS	#BIT6,@DPRS	IRCV INTERRUPT ENABLE
006036	016777	003224	003170	MOV	TSYNC,@DPTB	ITRANSMIT 3ED SYNC AS DATA
006044	105777	003162		TSTB	@DPTS	IWAIT FOR "DONE"
006050	102375			BPL	,=4	I
006052	032777	004000	003144	BIT	#BIT11,@DPRS	I TEST FOR ACTIVE
006060	001001			BNE	,+4	I OK
006062	104000			ERROR		I REPORT ERROR
				DELAY	6000,	IWAIT FOR INTERRUPT
006064	012767	013560	003176	MOV	#6000,,CNT	ISET UP COUNT
	006072			DEL=.		
006072	005367	003172		DEC	CNT	ITIME OUT
006076	001375			BNE	DEL	INO
006100	104000			ERROR		I DEVICE FAILED TO INTERRUPT
006102	017767	003120	003172	S2,EXT: MOV	@DPRB,TMPDAT	ISAVE RECEIVED DATA
006110	026767	003152	003164	CMP	TSYNC,TMPDAT	ICOMPARE SYNC
006116	001401			BEG	,+4	IBRANCH IF SYNC OK
006120	104000			ERROR		I REPORT ERROR
006122	022626			CMP	(SP)+,(SP)-	IADJUST STACK
006124	042767	000040	171644	BIC	#BIT5,PS	ILOWER PRIORITY
006132	042777	004000	003064	BIC	#BIT11,@DPRS	ICLEAR ACTIVE
006140	042777	000100	003056	BIC	#BIT6,@DPRS	ICLEAR INT ENB
006146	032767	040000	171414	BIT	#BIT14,SWR	I TEST FOR SCOPE LOOP
006154	001002			BNE	S4,EXT	IBRANCH AROUND INC IF SCOPE
006156	105267	003105		INCB	TSYNC+1	IINC TO NEXT TEST SYNC
006162	126767	003101	003111	S4,EXT: CMPB	TSYNC+1,SLIM+1	IHAVE ALL SYNC'S BEEN TESTED
006170	001404			BEG	S3,EXT	IYES
006172	112777	000026	003030	MOVB	#26,@SYNC	ICHANGE SYNC
006200	000651			BR	S1,EXT	
006202	005067	003060		S3,EXT: CLR	TSYNC	ICLEAR TSYNC
006206	006267	003066		ASR	SLIM	IDECREASE SYNC LIMIT
006212	046777	003044	003004	BIC	BPC,@DPRS	ICLEAR OLD CHAR SIZE
006220	062767	000400	003034	ADD	#400,BPC	IINC BITS/CHAR TO NEXT SIZE
006226	056777	003030	002770	BIS	BPC,@DPRS	ICHANGE BIT MODE
006234	022767	003400	003020	CMP	#3400,BPC	ICHECK CHARACTER SIZE
006242	001230			BNE	S1,EXT	IBRANCH UNTIL ALL SIZES HAVE BEEN TESTED

I IDLE SYNC TEST

I RAISE "ACTIVE" BY IDLEING IN EACH AVAILABLE CHARACTER LENGTH

006244	012767	000012	002700	ISYC1: MOV	#10,,ICOUNT	ISET ITERATION COUNT TO 10
006252	012767	000026	003006	MOV	#26,TSYNC	ILOAD TEST SYNC CHARACTER
006260	005077	002746		CLR	@DPTS	ICLEAR STATUS REGISTERS
006264	005077	002734		CLR	@DPRS	I
006270	016703	002730		MOV	DPRS,R3	IFETCH DEVICE ADRS
006274	005203			INC	R3	ICHANGE ADRS TO HIGH BYTE OF STATUS
006276	052777	000004	002720	BIS	#BIT2,@DPRS	I START MAINTENANCE
006304	012702	006612		MOV	#TAG2,R2	ISET UP CHARACTER LENGTH SELECTOR
				ISYC1: DELAY	6000,	IWAIT FOR ALL 1'S TO SHIFT IN

006310	012767	013560	002752		MOV	#6000, CNT	ISET UP COUNT
	006316			DEL=.			
006316	005367	002746			DEC	CNT	ITIME OUT
006322	001375				BNE	DEL	INO
006324	012777	006406	002706		MOV	#ISYC2, @DPRIV	ILOAD DP RCV INTERRUPT VECTOR
006332	116777	002730	002670		MOVB	TSYNC, @SYNC	ILOAD LOW BYTE OF SYNC
006340	116777	002723	002670		MOVB	TSYNC+1, @SEXT	ILOAD SYNC EXTENSION BITS
006346	016777	002714	002660		MOV	TSYNC, @DPTS	ILOAD XMIT BUFFER
006354	052777	000002	002650		BIS	#BIT1, @DPTS	ISET IDLE SYNC
006362	052777	000100	002634		BIS	#BIT6, @DPRS	ISET RCV INTERRUPT ENABLE
					DELAY	12000.	IWAIT FOR RCV INTERRUPT
006370	012767	027340	002672		MOV	#12000, CNT	ISET UP COUNT
	006376			DEL=.			
006376	005367	002666			DEC	CNT	ITIME OUT
006402	001375				BNE	DEL	INO
006404	104000				ERROR		IREPORT ERROR
006406	017767	002614	002666	ISYC2:	MOV	@DPRB, TMPDAT	ISAVE RCV DATA
006414	000406			ISYC3:	BR	ISYC4	ICONTROL WORD 12 BITS=BR, +2
006416	026767	002660	002642		CMP	TMPDAT, TSYNC	IDOES SYNC CHECK
006424	001401				BEG	, +4	IYES
006426	104000				ERROR		IREPORT ERROR
006430	000411				BR	ISYC5	
006432	105767	002645		ISYC4:	TSTB	TMPDAT+1	IVERIFY ONLY 8 BITS WERE TRANSMITTED
006436	001401				BEG	, +4	I BRANCH IF OK
006440	104000				ERROR		IREPORT ERROR
006442	126767	002634	002616		CMPB	TMPDAT, TSYNC	ICHECK SYNC IN LOW BYTE
006450	001401				BEG	, +4	I BRANCH IF SYNC OK
006452	104000				ERROR		IREPORT ERROR
006454	032777	000200	002542	ISYC5:	BIT	#BIT7, @DPRS	IDID READING RCV BUFF CLR DONE
006462	001401				BEG	, +4	IYES
006464	104000				ERROR		IREPORT ERROR
006466	042777	004000	002530		BIC	#BIT11, @DPRS	ICLEAR ACTIVE
006470	032777	004000	002522		BIT	#BIT11, @DPRS	IACTIVE CLEARED?
006502	001401				BEG	, +4	IYES
006504	104000				ERROR		IREPORT ERROR
006506	042777	000002	002516		BIC	#BIT1, @DPTS	ICLEAR IDLE
006514	042767	000040	171254		BIC	#BITS, PS	ILOWER PRIORITY TO 4
006522	022626				CMP	(SP)+, (SP)+	IADJUST STACK
006524	142213				BIQB	(R2)+, @R3	ICLEAR CHAR LENGTH
006526	132213				BISB	(R2)+, @R3	ISELECT NEXT CHAR LENGTH
006530	020227	006616			CMP	R2, #TAG2+4	IEND OF MODE?
006534	001265				BNE	ISYC1	INO
006536	032767	000400	002506		BIT	#BITS, SAVBR1	ITEST 12 BITS/CHARACTER
006544	001424				BEG	SEQD0	INO
006546	032777	002000	002450		BIT	#BIT10, @DPRS	IEND OF 12 BIT TEST
006554	001020				BNE	SEQD0	IYES
006556	052777	002000	002440		BIS	#BIT10, @DPRS	INO
006564	024242				CMP	-(R2), -(R2)	IADJUST CHAR SELECTION
006566	042777	001400	002430		BIC	#1400, @DPRS	ICLEAR CHAR LENGTH LSB'S
006574	012767	000400	177612		MOV	#400, ISYC3	ICHANGE CONTROL WORD
006602	012767	001426	002456		MOV	#1426, TSYNC	ICHANGE SYNC
006610	000637				BR	ISYC1	
006612	000403			TAG2:	403		ICHARACTER LENGTH SELECTION
006614	001003				1003		ICHARACTER LENGTH SELECTION

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006616 012767 000026 002442 SE0001 MOV #26,TSYNC
006624 012767 000406 177562 MOV #406,ISYC3

IRESTORE TSYNC
IRESTORE CONTROL WORD

*****[INTERRUPT DRIVEN SEQUENTIAL DATA TEST*****

006632	005067	002314		SEQD1	CLR	ICOUNT	ISET ITERATION COUNT TO 1
006636	105077	002374			CLRB	@SEXT	ICLEAR SYNC EXTENTION
006642	012767	000000	002434		MOV	#0, RDATA	IINIT RCV DATA
006650	012767	000000	002430		MOV	#0, TDATA	IINIT XMIT DATA
006656	005077	002342			CLR	@DPRS	IRECEIVER STATUS
006662	005077	002344			CLR	@DPTS	I TRANSMITTER STATUS
006666	052777	000005	002330		BIS	#5, @DPRS	ICLOCK ON + STRIP SYNC
006674	012767	007042	003162		MOV	#RAND, R3*2	ISET UP RETURN ADDRESS
006702	012767	000400	002366		MOV	#400, CHLEN	IC HAR LENGTH INDEX
006710	032767	000400	002334		BIT	#BIT8, SAVSR1	I TEST 12 BIT CHAR MODE
006716	001414				BEQ	SEQD2	IND
006720	012767	010000	002322		MOV	#10000, LIMIT	ISELECT END OF DATA
006726	052777	002000	002270		BIS	#BIT10, @DPRS	ISELECT 12 BITS/CHARACTER
006734	012767	000426	002324		MOV	#426, TSYNC	ISYNC FOR 12 BIT CHAR
006742	105277	002270			INCB	@SEXT	IPLACE MSB OF SYNC IN SYNC EXT
006746	000406				BR	SEQD3	
006750	012767	000400	002272	SEQD2I	MOV	#400, LIMIT	ITEMPORARY CHARACTER LIMIT
006756	012767	000026	002302		MOV	#26, TSYNC	IINIT SYNC STORAGE
006764	012777	011532	002252	SEQD3I	MOV	#TV18, @DPTIV	I TRANSMITTER VECTOR
006772	012777	011652	002240		MOV	#RV18, @DPRIV	IRECEIVER VECTOR
007000	012767	000200	170770		MOV	#200, PS	IPRIORITY#4
007006	012767	000002	002256		MOV	#2, SCNT	ISYNC COUNT#2
007014	116777	002246	002206		MOVB	TSYNC, @SYNC	ILOAD SYNC
007022	052777	000100	002174		BIS	#BIT6, @DPRS	IRCV INT ENB
007030	052777	000340	002174		BIS	#340, @DPTS	I STATUS INT ENB
							ITRANS INT ENB
							ITRANS DONE
007036	000001				WAIT		IWAIT FOR INTERRUPTS
007040	000776				BR	, -2	

*****RANDOM DATA, RANDOM STALL*****

007042	104400			RANDI	SCOPE		
007044	012767	000000	002224		MOV	#0, CHLEN	ISET CHAR LENGTH TO 8 BITS
007052	012767	000026	002206		MOV	#26, TSYNC	ISYNC = 26
007060	116777	002202	002142		MOVB	TSYNC, @SYNC	ILOAD SYNC BUFFER
007066	004767	000100			JSR	X7, AND	IEXECUTE DATA + STALL MODES

IREPEAT PREVIOUS TEST AT 7 BITS/CHAR

007072	012767	000200	002176		MOV	#200, CHLEN	ISET CHAR LENGTH TO 7 BITS
007100	052777	000400	002116		BIS	#BIT8, @DPRS	I7 BITS/CHAR
007106	042777	004000	002110		BIC	#BIT11, @DPRS	ICLEAR ACTIVE
007114	004767	000052		RANDA1	JSR	X7, AND	IEXECUTE DATA + STALL MODES

REPEAT PREVIOUS TEST AT 6 BITS/CHAR

007120	012767	000300	002150	MOV	#300,CHLEN	ISET CHAR LENGTH TO 6 BITS
007126	042777	000400	002070	BIC	#BIT8,@DPRS	
007134	052777	001000	002062	BIS	#BIT9,@DPRS	ISET MODE TO 6 BITS/CHAR
007142	042777	004000	002054	BIC	#BIT11,@DPRS	ICLEAR ACTIVE
007150	004767	000016		RANDB: JSR	X7,AND	IEXECUTE DATA & STALL MODES
007154	042777	007700	002042	LOOP: BIC	#7700,@DPRS	ICLEAR RCV STATUS
007162	042777	160342	002042	BIC	#160342,@DPTS	ICLEAR XMIT STATUS
007170	000511			BR	PARTY	

COMMON DATA AND IOLE SUBROUTINE

007172	012701	015371		AND: MOV	#15371,R1	IPRIME RANDOM # GEN
007176	012702	072414		MOV	#72414,R2	I" " "
007202	012703	004036		MOV	#4036,R3	I" " "
007206	012767	007300	001742	MOV	#STAG,RETURN	ISET UP SCOPE RETURN
007214	042777	004300	002002	BIC	#4300,@DPRS	IRCV INT ENB, RCV ACTIVE
007222	042777	160342	002002	BIC	#160342,@DPTS	IINT ENBS IDLE SYNC, ERRORS
007230	012767	012562	002106	MOV	#BOTTOM,RP	ISET UP RCV POINTER
007236	016767	002102	002076	MOV	RP,TP	ISET UP XMIT POINTER
007244	012777	012220	001766	MOV	#RRRR,@DPRIV	IRCV INT VECTOR
007252	012777	012066	001764	MOV	#RRRT,@DPTIV	IXMIT INT VECTOR
007260	012767	000002	002004	MOV	#2,SCNT	ISYNC COUNT + 2
007266	110267	002014		MOVB	R2,TDATA	IRANDOM DATA
007272	052777	000100	001724	BIS	#100,@DPRS	IRCV INT ENB
007300	016777	001762	001726	STAG: MOV	TSYNC,@DPTS	ILOAD BUFFER
007306	012767	000010	001636	MOV	#10,ICOUNT	ISET ITERATION TO 10
007314	052777	000340	001710	BIS	#340,@DPTS	IXMIT DONE, INT ENB, STATUS ENB
007322	010167	002012		TIM0: MOV	R1,TIME	I"ON" STALL
007326	005367	002006		TIM1: DEC	TIME	I0.6 SEC MAX
007332	001375			BNE	TIM1	
007334	042777	000140	001670	BIC	#140,@DPTS	ITURN OFF INT ENB
007342	052777	000002	001662	BIS	#BIT1,@DPTS	IDLE SYNC
007350	004967	001606		JSR	X5,RNUM	IGENERATE "STALL" TIME
007354	010167	001760		MOV	R1,TIME	IFETCH RANDON STALL TIME
007360	005367	001754		TIM2: DEC	TIME	ICOUNT IDLE TIME
007364	001375			BNE	TIM2	ITIME OUT?
007366	004567	001570		JSR	X5,RNUM	IGENERATE "ON" TIME + SYNC
007372	042777	000002	001632	BIC	#BIT1,@DPTS	ICLEAR IDLE
007400	000240			NOP		
007402	104400			SCOPE		
007404	042777	000100	001612	BIC	#100,@DPRS	ICLEAR RCV INT ENB
007412	000207			RTS	X7	

*****PARITY TEST*****

IVERIFY "PARITY" BIT=1 FOR ODD PARITY AND=0 FOR EVEN

007414	012767	007422	001534	PARTY1	MOV	#PARTY+6,RETURN	ISET UP SCOPE RETURN
007422	012767	000002	001522		MOV	#2,ICOUNT	IITERATION = 10,
007430	012767	001401	002770		MOV	#1401,RPRT1	ILOAD RPRT2WITH BEQ ,+4
007436	012767	000400	001604		MOV	#400,LIMIT	ISET UP CHARACTER LIMIT
007444	005067	001634			CLR	RDATA	ICLR RCV DATA
007450	005067	001632			CLR	TDATA	ICLR XMIT DATA
007454	105077	001556			CLRB	@SEXT	ICLEAR SYNC EXTENTION
007460	012767	000026	001600		MOV	#26,TSYNC	ISET UP SYNC
007466	116777	001574	001534		MOV	TSYNC,@SYNC	IINIT SYNC
007474	012767	000002	001570		MOV	#2,SCNT	I2 SYNC'S
007502	005077	001516			CLR	@DPRS	ICLR RECEIVER STATUS
007506	005077	001520			CLR	@DPTS	ICLR TRANSMITTER STATUS
007512	032767	000400	001532		BIT	#BIT8,SAVSR1	I8/12 BITS/CHAR
007520	001406				BEQ	TY1	I BRANCH IF 8 BITS/CHAR
007522	012767	010000	001520		MOV	#10000,LIMIT	ISET LIMIT TO 12 BITS/CHAR
007530	052777	002000	001466		BIS	#BIT10,@DPRS	ISELECT 12 BIT MODE
007536	012767	000200	170232	TY11	MOV	#200,PS	IPRIORITY = 4
007544	012777	012302	001472		MOV	#TPRTY,@DPTIV	ITRANSMITTER PARITY TEST VECTOR
007552	012777	012372	001460		MOV	#RPRTY,@DPRIV	IRECEIVER PARITY TEST VECTOR
007560	052777	000105	001436		BIS	#105,@DPRS	IRCV INT ENB, STRIP SYNC, CLOCK
007566	052777	000300	001436		BIS	#300,@DPTS	IXMIT INT ENB,DONE
007574	000001			SLP1	WAIT		
007576	000776				BR	SLP	

IRECEIVER OVERRUN TST

007600	104400			OVRUN1	SCOPE		
007602	012767	000002	001342		MOV	#2,ICOUNT	ISET ITERATION COUNT TO 10
007610	012767	000000	001464		MOV	#0,TMPDAT	Istor TEST CHAR IN TMPDAT
007616	105077	001414			CLRB	@SEXT	ICLEAR SYNC EXTENTION
007622	112777	000026	001400		MOV	#26,@SYNC	ILOAD SYNC BUFFER
007630	032767	000400	001414		BIT	#BIT8,SAVSR1	I8/12 BITS/CHAR
007636	001403				BEQ	OR0	I BRANCH IF 8 BITS/CHAR
007640	052777	002000	001356		BIS	#BIT10,@DPRS	ISELECT 12 BITS/CHAR
007646	012777	010010	001370	OR01	MOV	#ORUN,@DPTIV	IXMIT STATUS INT VECTOR=O'RUN
007654	052777	000004	001342		BIS	#BIT2,@DPRS	ITURN ON CLOCK
007662	012767	013560	001400	OR11	DELAY	6000,	IWAIT FOR BCV TO CLEAR
	007670				MOV	#6000,,CNT	ISET UP COUNT
007670	005367	001374		DEL=.	DEC	CNT	ITIME OUT
007674	001375				BNE	DEL	INO
007676	052777	000200	001326		BIS	#BIT7,@DPTS	IDONE
007704	105777	001322			TSTB	@DPTS	I TRANSMIT FIRST SYNC
007710	100375				BPL	,-4	
007712	012777	000026	001314		MOV	#26,@DPTB	
007720	105777	001306			TSTB	@DPTS	
007724	100375				BPL	,-4	
007726	012777	000026	001300		MOV	#26,@DPTB	I TRANSMIT SECOND SYNC
007734	105777	001272			TSTB	@DPTS	
007740	100375				BPL	,-4	
007742	016777	001334	001264		MOV	TMPDAT,@DPTB	I TRANSMIT DATA CHAR #1

```

007750 105777 001256 TSTB @DPTS
007754 100375 BPL ,=4
007756 016777 001320 001250 MOV TMPDAT,@DPTS ;TRANSMIT DATA CHAR #2
007764 052777 000040 001240 BIS #BIT5,@DPTS ;SET STATUS INT ENB
;WAIT FOR O'RUN INTERRUPT
;SET UP COUNT
007772 012767 005670 001270 DELAY 3000;
MOV #3000,;CNT
DEL=,
010000 010000 005367 001264 DEC CNT ;TIME OUT
010004 001375 BNE DEL ;NO
010006 104000 ERROR ;REPORT ERROR, NO O'RUN INT
010010 032777 040000 001214 ORUN: BIT #BIT14,@DPTS ;TEST FOR O'RUN
010016 001001 BNE ,+4 ;BRANCH IF O'RUN CAUSED INT
010020 104000 ERROR ;REPORT ERROR
010022 005077 001204 CLR @DPTS ;CLEAR XMIT STATUS
010026 042777 004000 001170 BIC #BIT11,@DPRS ;CLEAR ACTIVE
010034 022626 CMP (SP)+,(SP)+ ;ADJUST STACK
010036 042767 000040 167732 BIC #BIT5,PS ;LOWER PRIORITY TO 4
010044 005267 001232 INC TMPDAT ;INC TO NEXT DATA
010050 022767 000400 001224 CMP #400,TMPDAT ;TEST FOR END OF DATA
010056 001301 BNE OR1 ;BRANCH IF NOT END
010060 104400 SCOPE

```

HALF DUPLEX TEST

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010062 012767 000620 001062 DUPLX: MOV #400,;ICOUNT ;ITERATION COUNT = 400
010070 005077 001130 CLR @DPRS ;CLEAR RECEIVER STATUS
010074 005077 001132 CLR @DPTS ;CLEAR TRANSMITTER STATUS
010100 052777 000002 001116 BIS #BIT1,@DPRS ;HALF DUPLEX
010106 052777 000100 001110 BIS #BIT6,@DPRS ;INT ENB RCV
010114 052777 000004 001102 BIS #BIT2,@DPRS ;TURN ON CLOCK
010122 012777 011476 001110 MOV #FRINT,@DPRIV ;SETUP TEST VECTOR
010130 005067 001132 CLR TSYNC ;CLR TEST SYNC
010134 012767 000200 167634 MOV #200,PS ;PRIORITY=4
010142 116777 001120 001060 DPLX1: MOVB TSYNC,@SYNC ;LOAD SYNC BUFFER
010150 052777 000002 001054 BIS #BIT1,@DPTS ;IDLE SYNC
;DELAY 20.1 MS
;SET UP COUNT
010156 012767 005670 001104 DELAY 3000;
MOV #3000,;CNT
DEL=,
010164 010164 005367 001100 DEC CNT ;TIME OUT
010170 001375 BNE DEL ;NO
010172 105267 001070 INCB TSYNC ;HAVE ALL SYNC BEEN TESTED
010176 001361 BNE DPLX1 ;NO
010200 012777 000007 001014 MOV #7,@CTPB ;BELL
010206 105777 001006 TSTB @CTPS ;PUNCH DONE?
010212 100375 BPL ,=4 ;NO
010214 000167 171336 JMP BGN1

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EMULATOR ROUTINE

010220	011646			EMTVECI	MOV	@R6,=(R6)	I DUPLICATE PC ON STACK
010222	162716	000002			SUB	#2,@R6	I POINT PC TO EMT INST,
010226	017616	000000			MOV	@(R6),@R6	I MOV EMT INST ONTO STACK
010232	121627	000002			CMPB	@R6,#2	I TEST THAT CALL IS WITHIN LIMITS
010236	101401				BLOS	EMTOK	I BRANCH IF WITHIN LIMITS
010240	104000				ERROR		I REPORT CALL NOT WITHIN LIMITS
010242	006116			EMTOKI	ROL	@R6	I EMT ARGUMENT X 2,
010244	042716	177001			BIC	#177001,@R6	I CLEAR HIGH BYTE
010250	062716	010262			ADD	#EMTAB,@R6	I FORM ADRS OF ROUTINE ADRS
010254	017616	000000			MOV	@(R6),@R6	I PUT ROUTINE ADRS ON STACK
010260	000136				JMP	@(R6)+	I JUMP TO ROUTINE
010262	010270			EMTAB1	ERRP		I ERROR PRINT ROUTINE
010264	000000				B		
010266	000000				B		
010270	010667	001014		ERRPI	MOV	R6,SAVPC	I SAVE STACK POINTER
010274	010046			SAVRI	MOV	R0,=(R6)	I SAVR R0 THRU R5
010276	010146				MOV	R1,=(R6)	
010300	010246				MOV	R2,=(R6)	
010302	010346				MOV	R3,=(R6)	
010304	010446				MOV	R4,=(R6)	
010306	010546				MOV	R5,=(R6)	
010310	016701	000774			MOV	SAVPC,R1	I R1=SAVPC
010314	036727	167250	020000		BIT	SWR,#BIT13	I TEST FOR INHIBIT PRINT OUT
010322	001402				BEQ	ERP0	I BRANCH TO PRINT
010324	000167	000066			JMP	PRINT1	I INHIBIT, RETURN TO MAIN STREAM
010330	105777	000664		ERP0I	TSTB	@CTPS	I READY
010334	100375				BPL	,=4	I NO
010336	012777	000215	000656		MOV	#215,@CTPB	I YES, CR
010344	105777	000650			TSTB	@CTPS	I READY
010350	100375				BPL	,=4	I NO
010352	012777	000212	000642		MOV	#212,@CTPB	I YES, LF
010360	105777	000634			TSTB	@CTPS	I READY
010364	100375				BPL	,=4	I NO
010366	012102			ERP1I	MOV	(R1)+,X2	I FETCH WORD OFF STACK
010370	004767	000054			JSR	X7,PRTAB	I PRINT WORD PC OR PS
010374	105777	000620			TSTB	@CTPS	I SPACE BETWEEN WORDS
010400	100375				BPL	,=4	
010402	012777	000240	000612		MOV	#240,@CTPB	I SPACE
010410	020127	001100			CMP	R1,#BEGIN1	I TEST FOR END OF STACK
010414	001364				BNE	ERP1	I CONTINUE PRINT IF STACK NOT EMPTY
010416	005767	167146		PRINT1I	TST	SWR	I TEST FOR HLT ON ERR
010422	100001				BPL	,+4	
010424	000000				HALT		
010426	005267	000700			INC	ERRCNT	I INC ERROR COUNT
010432	012605			RESTRI	MOV	(R6)+,R5	I RESTOR R5 THRU R0
010434	012604				MOV	(R6)+,R4	
010436	012603				MOV	(R6)+,R3	
010440	012602				MOV	(R6)+,R2	
010442	012601				MOV	(R6)+,R1	
010444	012600				MOV	(R6)+,R0	

010446 000002

RTI RETURN

ISAVREG EMT CALL TO SAVE R0 THRU R5

010450	005067	000252		PRTAB I	CLR	BINCT	
010454	005067	000244			CLR	WGTCT	
010460	012704	010732			MOV	#LIST,X4	I GET LIST ADDRESS
010464	012767	000005	000236		MOV	#5,ASCNT	
010472	012767	000007	000220		MOV	#7,SEVEN	
010500	012767	000001	000214		MOV	#1,DECML	
010506	105777	000506		WAIT1 I	TSTB	@CTPS	
010512	100375				BPL	WAIT1	
010514	005702				TST	X2	
010516	100404				BMI	MINUS	I NEG SIGN PRINT 1
010520	012777	000260	000474		MOV	#260,@CTPB	I POS SIGN PRINT 0
010526	000403				BR	STAR	
010530	012777	000261	000464	MINUS I	MOV	#261,@CTPB	
010536	016703	000156		STAR I	MOV	SEVEN,X3	I PUT MASK IN R3
010542	010267	000150			MOV	X2,TOODLE	I GET READY TO DOODLE NUMBER IN TOODLE
010546	005167	000144			COM	TOODLE	I COMPENSATES FOR COMPLEMENT DURING BIC
010552	046703	000140			BIC	TOODLE,X3	I AND IN OCTAL CHARACTER
010556	001410				BEQ	WRTDC	I ZERO, WRITE 0 IN LIST
010560	066767	000136	000136	MKNUM I	ADD	DECML,WGTCT	I COUNT UP TO
010566	005267	000134			INC	BINCT	I AND RECORD
010572	026703	000126			CMP	WGTCT,X3	I SAME BINARY WEIGHT
010576	001370				BNE	MKNUM	I KEEP COUNTN
010600	062767	000260	000120	WRTDC I	ADD	#260,BINCT	I ADD ASCII PREFIX
010606	016724	000114			MOV	BINCT,(4)*	I WRITE ASCII CHAR IN LIST
010612	066767	000102	000102		ADD	SEVEN,DECML	I EXPAND BINARY WEIGHT
010620	005067	000100			CLR	WGTCT	
010624	005067	000076			CLR	BINCT	
010630	005367	000074			DEC	ASCNT	
010634	001410				BEQ	XLIST	I 5 CHAR IN LIST
010636	012703	000003			MOV	#3,X3	I SET X3 FOR ADD LOOP
010642	066767	000052	000050	MOADD I	ADD	SEVEN,SEVEN	I MAKING SEVENTY BY SEVEN
010650	005303				DEC	X3	
010652	001373				BNE	MOADD	
010654	000730				BR	STAR	I NX SEVEN SET GET NX OCTAL
010656	012767	000005	000044	XLIST I	MOV	#5,ASCNT	I SEND 5 CHAR TO TTY
010664	105777	000330		WAIT2 I	TSTB	@CTPS	
010670	100375				BPL	WAIT2	
010672	014477	000324			MOV	-(4),@CTPB	
010676	005367	000026			DEC	ASCNT	
010702	001401				BEQ	HDFHM	I FINISH PRINTING GET NXT NUM
010704	000767				BR	WAIT2	
010706	105777	000306		HDFHM I	TSTB	@CTPS	
010712	100375				BPL	,=4	
010714	000207				RTS	X7	I HEAD FOR HOME
010716	000000			TOODLE I	0		
010720	000000			SEVEN I	0		
010722	000000			DECML I	0		
010724	000000			WGTCT I	0		

010726	000000			BINCTI	0
010730	000000			ASCNTI	0
010732	000000			LISTI	0
010734	000000				0
010736	000000				0
010740	000000				0
010742	000000				0
010744	000000				0

IPOWER FAIL ROUTINE

010746	012767	010756	167050	PFAILI	MOV	#PWRUP,24	ILOAD PFAIL VECTOR FOR POWER UP
010754	000000				HALT		I
010756	000005			PWRUPI	RESET		IWAIT TTY TO COME UP
010760	012706	001100			MOV	#BEGIN1,SP	IREINIT STACK POINTER
010764	012767	010746	167032		MOV	#PFAIL,24	ILOAD PFAIL VECTOR FOR POWER DOWN
010772	105777	000222			TSTB	@CTPS	IREADY
010776	100375				BPL	,=4	INO
011000	012777	000215	000214		MOV	#215,@CTPB	IYES, CR
011006	105777	000206			TSTB	@CTPS	IREADY
011012	100375				BPL	,=4	INO
011014	012777	000212	000200		MOV	#212,@CTPB	IYES, LF
011022	010702				MOV	PC,X2	ILOAD PC
011024	004767	177420			JSR	X7,PRTAB	IPRINT PFAIL PC
011030	000137	001556		PUP11	JMP	@BGN1	

ISGEN,ROUTINE TO GENERATE A UNIQUE SYNC CHARACTER

011034	112777	000026	000166	SGENI	MOVB	#26,@SYNC	ISET UP FILLER SYNC
					DELAY	3000,	IDELAY 10 CHAR
011042	012767	005670	000220		MOV	#3000,,CNT	ISET UP COUNT
	011050			DEL=.			
011050	005367	000214			DEC	CNT	ITIME OUT
011054	001375				BNE	DEL	INO
011056	004567	000100			JSR	X5,RNUM	IRANDOM #
011062	110167	000200			MOVB	R1,TSYNC	ILOAD SYNC
011066	000207				RTS	X7	

ISCOPE LOOP ROUTINE ENTERED BY USER TRAP

011070	022606			SCOPEB	CMP	(6)+,X6	IREPOSITION THE STACK
011072	012667	166700			MOV	(6)+,PS	IUPDATE STATUS
011076	000177	000054			JMP	@RETURN	ISCOPE RETURN

ISCOPE OR/AND ITERATION LOOP FOR EACH TEST 4000 TIMES

011102	032767	040000	166460	SCOPECI	BIT	#BIT14,SWR	ITEST BR FOR SCOPE
011110	001367				BNE	SCOPEB	IYES SCOPE
011112	032767	004000	166450		BIT	#BIT11,SWR	INO = TEST FOR ITERATION
011120	001013				BNE	SCOPEA	IINHIBIT ITERATION
011122	026767	000026	000022		CMP	SCOPEF,ICOUNT	
011130	001403				BEQ	SCOPEG	IEXIT = DONE
011132	005267	000016			INC	SCOPEF	IINCREMENT COUNT
011136	000754				BR	SCOPEB	ILOOP SOME MORE
011140	005067	000010		SCOPEGI	CLR	SCOPEF	ICLEAR COUNT
011144	011667	000006			MOV	@X6,RETURN	ISAVE SCOPE RETURN POINTER

011150	000002	SCOPEA:	RTI	IRETURN	INLINE-NEXT TEST
011152	004000	ICOUNT:	4000		
011154	000000	SCOPEF:	0	ICOUNT	LOCATION FOR ITERATION LOOP
011156	012576	RETURN:	BEGIN2+2	IAADDRESS	OF LAST TEST
011160	000777		BR	ISCOPE	LOOP FAILURE

IRNUM, PSEUDO RANDOM NUMBER GENERATOR

011162	032767	040000	166400	RNUM1	BIT	#BIT14,SWR	ITEST	FOR SCOPE LOOP
011170	001010				BNE	RNUM1	IEXIT	IF SCOPE
011172	060201				ADD	R2,R1		
011174	005501				ADC	R1		
011176	060102				ADD	R1,R2		
011200	005502				ADC	R2		
011202	060302				ADD	R3,R2		
011204	005502				ADC	R2		
011206	060203				ADD	R2,R3		
011210	005503				ADC	R3		
011212	000205			RNUM1	RTS	X5		

ICONSTANTS, DYNAMIC MEMORY STORAGE AND DEVICE ADDRESSES

011214	177560	CTKSI	177560	ICONSOL	TTY KEYBOARD STATUS
011216	177562	CTKBI	177562	ICONSOL	TTY DATA BUFFER
011220	177564	CTPSI	177564	ICONSOL	TTY PUNCH STATUS
011222	177566	CTPBI	177566	ICONSOL	TTY PUNCH BUFFER

011224	174770	DPRSI	174770	IDP11	RECEIVER STATUS
011226	174772	DPRBI	174772	IDP11	RECEIVER BUFFER
011230	174773	SYNCS	174773	ISYNC	BUFFER
011232	174774	DPTSI	174774	IDP11	TRANSMITTER STATUS
011234	174776	DPTBI	174776	IDP11	TRANSMITTER BUFFER
011236	174777	SEXTI	174777	IDP11	SYNC EXTENSION

011240	000300	DPRVI	300	IDP11	RECEIVER INTERRUPT VECTOR
011242	000302	DPRPI	302	IDP11	RECEIVER PRIORITY
011244	000304	DPTVI	304	IDP11	TRANSMITTER INTERRUPT VECTOR
011246	000306	DPTPI	306	IDP11	TRANSMITTER PRIORITY

011250	000400	LIMITI	400	ICHARACTER	LIMIT
011252	000000	SAVSR1:	0	ISWITCH	REGISTER STORAGE #1
011254	000000	SAVSR2:	0		
011256	000000	CLKCNT:	0	ICOUNT	FOR CLOCK MACRO
011260	000000	ERCOUNT:	0	IERROR	COUNT
011262	000010	BPCI	10	IBITS	PER CHARACTER
011264	000000	SYNCS:	0		
011266	000000	TSYNC:	0	ITEST	SYNC CHARACTER
011270	000000	CNTI	0	IMISC,	COUNTER

011272	000000			SCNTI	0		ISYNC COUNT
011274	000200			LIMTMP:	200		ITEMPORARY LIMIT
011276	000000			CHLEN:	0		ICHAARACTER LENGTH
011300	000000			SLIMI	0		
011302	000000			TMPDAT:	0		ITEMPORARY STORAGE
011304	000000			RDATA:	0		IRECEIVER DATA
011306	000000			TDATA:	0		ITRANSMITTER DATA
011310	000000			SAVPC:	0		ISAVE PC
011312	000000			SAVSP:	0		ISAVE PS
011314	000000			SAVR0:	0		ISAVE R0
011316	000000			SAVR1:	0		ISAVE R1
011320	000000			SAVR2:	0		ISAVE R2
011322	000000			SAVR3:	0		ISAVE R3
011324	000000			SAVR4:	0		ISAVE R4
011326	000000			SAVR5:	0		ISAVE R5
011330	000000			CCI	0		ICHAARACTER COUNT
011332	000000			ERRCNT:	0		
011334	000000			FLAG:	0		
011336	000000			RCNT:	0		
011340	000000			TIME:	0		
011342	000000			TPI	0		ITRANSMITTER TUMBLE TABLE POINTER
011344	000000			RPI	0		IRECEIVER TT POINTER

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I
I INTERRUPT SERVICE ROUTINES
I
I THESE ROUTINES MAY FUNCTION AS:
I 1. ERROR TRAPS FOR FALSE INTERRUPTS
I 2. POINTERS BACK TO THE MAIN LINE FOR VALID INTERRUPTS
I 3. FUNCTIONAL TEST WHICH ARE INTERRUPT DRIVEN

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I VERIFY THAT INTERRUPT RESULTED FROM RING:
011346 022626 TV24: CMP (SP)+,(SP)+

011350 032777 020000 177654 BIT #BIT13,0DPTS ITEST FOR RING
011356 001001 BNE TV24A IBRANCH IF SET
011360 104000 ERROR IREPORT ERROR

011362 042777 020000 177642 TV24A: BIC #BIT13,0DPTS ICLEAR RING FLAG.
011370 032777 020000 177634 BIT #BIT13,0DPTS ITEST IT
011376 001401 BEQ TV24B IBRANCH IF CLEAR.
011400 104000 ERROR IREPORT ERROR

011402 032777 140200 177622 TV24B: BIT #140200,0DPTS INO OTHER STATUS FLAG ON?
011410 001401 BEQ TV24C
011412 104000 ERROR IREPORT ERROR
011414 000167 005334 TV24C: JMP RCD1

I VERIFY THAT INTERRUPT RESULTED FROM 'CARRIER DOWN' FLAG
011420 022626 TV25: CMP (SP)+,(SP)+ ICLEAN UP STACK
011422 032777 100000 177602 BIT #BIT15,0DPTS ITEST FOR 'CARRIER DOWN' FLAG
011430 001001 BNE TV25A IBRANCH IF SET
011432 104000 ERROR IREPORT ERROR

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011434	042777	100000	177570	TV25A:	BIC	#BIT15,@DPTS	ICLEAR 'CARRIER DOWN' FLAG,
011442	032777	100000	177562		BIT	#BIT15,@DPTS	ITEST IT
011450	001401				BEG	TV25B	IBRANCH IF CLEAR,
011452	104000				ERROR		IREPORT ERROR
011454	032777	060200	177550	TV25B:	BIT	#060200,@DPTS	INO OTHER FLAGS ON?
011462	001401				BEG	TV25C	
011464	104000				ERROR		IREPORT ERROR
011466	000167	005330		TV25C:	JMP	BELL	
011472	104001			FTINT:	EMT+1		IREPORT FALSE TRANSMITTER INTERRUPT
011474	000000				HALT		ERROR ROUTINE SHOULD RETURN TO MAINLINE
011476	104001			FRINT:	EMT+1		IREPORT FALSE RECEIVER INTERRUPT
011500	000000				HALT		ERROR ROUTINE SHOULD RETURN TO MAINLINE
011502	062716	000002		TRT1:	ADD	#2,@SP	IADD 2 TO PC TO SKIP OVER HALT
011506	000002				RTI		IPC POINTS TO HALT
011510	022626			TV5:	CMP	(SP)+,(SP)+	IREPOSITION POINTER
011512	000167	173046			JMP	IT3A	IRETURN TO MAINLINE
011516	022626			TV6:	CMP	(SP)+,(SP)+	IADJUST STACK
011520	000167	173150			JMP	IT4A	IRETURN TO MAINLINE
011524	022626			TV7:	CMP	(SP)+,(SP)+	IADJUST STACK
011526	000167	173270			JMP	IT5A	IRETURN TO MAINLINE
011532	016777	177530	177474	TV18:	MOV	TSYNC,@DPTS	IXMIT SYNC
011540	116777	177523	177470		MOVB	TSYNC+1,@SEXT	ILOAD SYNC EXT
011546	005367	177520			DEC	SCNT	IHAVE 2 SYNC'S BEEN XMITED
011552	001003				BNE	T18	INO
011554	012777	011564	177462		MOV	#TV19,@DPTIV	IYES CHANGE VECTOR
011562	000002			T18:	RTI		

ISEQUENTIAL DATA TRANSMISSION ROUTINE

011564	032777	160000	177440	TV19I	BIT	#160000, @DPTS	IANY STATUS ERRORS
011572	001401				BEQ	,+4	INO
011574	104000				ERROR		IREPORT ERROR
011576	032777	000200	177426		BIT	#BIT7, @DPTS	ITRANSMITTER READY
011604	001001				BNE	,+4	IYES
011606	104000				ERROR		IREPORT ERROR
011610	016777	177472	177416		MOV	TDATA, @DPTB	ILOAD BUFFER
011616	032767	040000	169744		BIT	#BIT14, SWR	I TEST FOR SCOPE LOOP
011624	001011				BNE	T19	I BRANCH AROUND INC IF SCOPE
011626	005267	177454			INC	TDATA	I NEXT CHARACTER
011632	026767	177412	177446		CMP	LIMIT, TDATA	I HAVE ALL CHARACTERS
011640	001003				BNE	T19	INO
011642	042777	000140	177362		BIC	#140, @DPTS	IYES, CLEAR INTERRUPTS
011650	000002			T19I	RTI		

I RECEIVE SEQUENTIAL DATA

011652	032777	000100	177344	RV18I	BIT	#BIT6, @DPRS	I RECEIVE DONE
011660	001001				BNE	,+4	IYES
011662	104000				ERROR		IREPORT ERROR
011664	026777	177414	177334		CMP	RDATA, @DPRB	ICORRECT DATA
011672	001404				BEQ	RV18A	
011674	017767	177326	177400		MOV	@DPRB, TMPDAT	I STORE DATA
011702	104000				ERROR		IREPORT ERROR
011704	042777	000001	177312	RV18AI	BIC	#BIT0, @DPRS	ICLEAR STRIP SYNC
011712	032767	040000	169650		BIT	#BIT14, SWR	I TEST FOR SCOPE
011720	001047				BNE	R10	I BRANCH AROUND INC IF SCOPE
011722	005267	177356			INC	RDATA	I NEXT CHARACTER
011726	026767	177316	177350		CMP	LIMIT, RDATA	
011734	001041				BNE	R10	
011736	012767	000000	177340		MOV	#0, RDATA	
011744	012767	000000	177334		MOV	#0, TDATA	
011752	006267	177272			ASR	LIMIT	IDECREASE LIMIT TO 7 BITS
011756	012777	011532	177260		MOV	#TV18, @DPTIV	ISET UP SYNC TRANSMISSION
011764	012767	000004	177300		MOV	#4, SCNT	ISYNC COUNT #4
011772	092777	000001	177224		BIS	#BIT0, @DPRS	ISTRIP SYNC
012000	042777	004000	177216		BIC	#BIT11, @DPRS	ICLEAR RCV ACTIVE
012006	052777	000340	177216		BIS	#340, @DPTS	IINT ENB + DONE
012014	056777	177256	177202		BIS	CHLEN, @DPRS	ICHANGE CHAR LENGTH

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012022	062767	000400	177240		ADD	#400,CHLEN	I DECREASE CHAR LENGTH
012030	022767	001400	177240	R17I	CMP	#1400,CHLEN	I HAVE ALL LENGTHS BEEN TESTED
012036	001401				BEQ	R19	I YES
012040	000002			R18I	RTI		I NO
012042	022626			R19I	CMP	(SP)+,(SP)+	I ADJUST POINTER
012044	005077	177162			CLR	@DPTS	I CLR TRANSMITTER STATUS
012050	005077	177150			CLR	@DPRS	I CLR RECEIVER STATUS
012054	042767	000040	165714		BIC	#BIT5,PS	I PRIORITY = 4
012062	000137	007042		R20I	JMP	@#RAND	I JUMP TO RANDOM DATA TEST

ISYNC ROUTINE FOR RANDOM DATA TEST

ISYNC ROUTINE FOR RANDOM DATA TEST

```

012066 032777 000200 177136 RRR1: BIT #BIT7,@DPTS IREADY
012074 001001 BNE .+4 IYES
012076 104000 ERROR IREPORT ERROR
012100 016777 177162 177126 MOV TSYNC,@DPTB ITRANSMIT SYNC
012106 005367 177160 DEC SCNT I2 SYNC'S
012112 001006 BNE RT2 INO
012114 012777 012132 177122 MOV #RR1,@CPTIV IYES, SET UP DATA TRANSMIT VECTOR
012122 042777 160000 177102 BIC #160000,@DPTS ICLEAR ERROR BITS
012130 000002 RT2: RTI
    
```

IRRR1, RANDOM DATA, SYNC, RANDOM STALL
ITRANSMITTER SERVICE ROUTINE

```

012132 032777 000200 177072 RRT1: BIT #BIT7,@DPTS ITRANSMITTER READY
012140 001001 BNE .+4 IYES
012142 104000 ERROR IREPORT ERROR
012144 004567 177012 JSR X5,RNUM IGENERATE NEXT CHARACTER
012150 010167 177132 MOV R1,TDATA
012154 046767 177116 177124 BIC CHLEN,TDATA IREDUCE DATA TO # BITS/CHAR
012162 016777 177120 177044 MOV TDATA,@DPTB ITRANSMIT CHARACTER
012170 016704 177146 MOV TP,R4 ISET UP TRANSMITTER POINTER
012174 016724 177106 MOV TDATA,(R4)+ IMOV CHARACTER TO TUMBLE TABLE
012200 020427 012572 CMP R4,#TOP IEND OF TUMBLE TABLE
012204 001002 BNE RT1
012206 012704 012562 MOV #BOTTOM,R4
012212 010467 177124 RT1: MOV R4,TP ISAVE TRANSMITTER POINTER
012216 000002 RTI
    
```

IRRRR, RANDOM DATA, RANDOM SYNC, RANDOM STALL, RECEIVER SERVICE

```

012220 017767 177002 177056 RRRR: MOV @DPRB,RDATA ISAVE RECEIVED DATA
012226 016700 177112 MOV RP,R0 ISET UP RECEIVER POINTER
012232 026720 177046 CMP RDATA,(R0)+ IIS DATA CORRECT
012236 001406 BEQ RR1 IYES
012240 026767 177040 177020 CMP RDATA,TSYNC IIF NOT DATA IS IT SYNC
012246 001401 BEQ ERROR IYES
012250 104000 ERROR IREPORT ERROR
012252 005740 TST -(R0) IADJUST TUMBLE TABLE
012254 022700 012572 RR1: CMP #TOP,R0 ITOP OF TUMBLE TABLE
012260 001002 BNE RR2 INO
012262 012700 012562 MOV #BOTTOM,R0 IYES,RAP AROUND
012266 010067 177052 RR2: MOV R0,RP ISAVE RECEIVER POINTER
012272 042777 000001 176724 BIC #BIT0,@DPRS ICLEAR STRIP SYNC
012300 000002 RTI
    
```


TRANSMITTER SERVICE ROUTINES FOR PARITY TEST

```

012302 016777 176760 176724 TPRTYI MOV TSYNC,@DPTB JXMIT SYNC CHARACTER
012310 005367 176756 DEC SCNT JDEC SYNC COUNT
012314 001003 BNE TPRT1 JBRANCH IF LESS THAN 2 SYNCs
012316 012777 012326 176720 MOV #TPRT2,@DPTIV JSET VECTOR TO TRANSMIT DATA
012324 000002 TPRT1I RTI JRETURN TO MAINLINE

012326 032777 160000 176676 TPRT2I BIT #160000,@DPTS JAN Y ERRORS
012334 001401 BEQ ,+4 JNO
012336 104000 ERROR JREPORT ERROR
012340 016777 176742 176666 MOV TDATA,@DPTB JTRANSMIT DATA
012346 005267 176734 INC TDATA JINC TRANSMIT DATA
012352 026767 176730 176670 CMP TDATA,LIMIT JIS UPPER LIMIT REACHED
012360 001401 BEQ TPRT3 JYES, EXIT
012362 000002 RTI JNO, RETURN TO MAINLINE
012364 005077 176642 TPRT3I CLR @DPTS JCLEAR STATUS REGISTER
012370 000002 RTI
    
```

RECEIVER SERVICE ROUTINE FOR PARITY TEST

```

000000 HERE=0

012372 017727 176626 000000 RPRTYI MOV @DPRS,#HERE JSAVE RCV STATUS HERE
012400 017767 176622 176674 MOV @DPRB,TMPDAT JSAVE RCV DATA
012406 026767 176670 176670 CMP TMPDAT,RDATA JCHECK FOR CORRECT DATA
012414 001401 BEQ ,+4 JBRANCH IF DATA OK
012416 104000 ERROR JREPORT ERROR
012420 032767 010000 177750 BIT #BIT12,RPRTY+4 JTEST PARITY
012426 001401 RPRT1I BEQ ,+4 J(RPRT1)=BEQ ,+4 FOR EVEN PARITY
J(RPRT1)=BNE ,+4 FOR ODD PARITY
012430 104000 ERROR JREPORT ERROR
JEXAMIN #HERE FOR STATUS
J TMPDAT FOR DATA
J RPRT1 FOR ODD/EVEN
012432 005267 176646 INC RDATA JINC TO NEXT EXPECTED DATA
012436 005067 176672 CLR FLAG JPARITY FLAG
012442 012767 000020 176666 MOV #16,,RCNT JSET ROTATE COUNT TO 16.
012450 000241 CLC JCLEAR CARRY
012452 006167 176626 RPRT2I ROL RDATA JROTATE DATA
012456 103002 BCC RPRT3 JBRANCH IF BIT IS A "0"
012460 005167 176650 COM FLAG JSET FLAG TO A "1" FOR ODD PARITY
012464 005367 176646 RPRT3I DEC RCNT JDEC ROTATE COUNT
012470 001370 BNE RPRT2 JBRANCH IF 16 BIT WORD NOT CHECKED

JIF FLAG=1 EXPECTED DATA SHOULD CAUSE ODD PARITY
JBIT 12="1"

012472 006167 176606 ROL RDATA JRESTORE EXPECTED DATA
012476 005767 176632 TST FLAG JTEST FOR NEXT PARITY
012502 100404 BML RPRT4 JBRANCH FOR ODD PARITY
012504 052767 000400 177714 BIS #BIT8,RPRT1 JEVEN PARITY=BEQ ,+4
012512 000403 BR RPRT5 J
012514 042767 000400 177704 RPRT4I BIC #BIT8,RPRT1 JODD PARITY=BNE ,+4
    
```

012522	042777	000001	176474	RPRT5:	BIC	#BIT0,@DPRS	ICLEAR SYNC STRIP
012530	026767	176514	176546		CMP	LIMIT,RDATA	IEND OF DATA
012536	001401				BEG	RPRT6	IYES
012540	000002				RTI		INO
012542	005077	176456		RPRT6:	CLR	@DPRS	ICLEAR STATUS
012546	022626				CMP	(SP)+,(SP)+	IADJUST STACK
012550	042767	000040	165220		BIC	#BIT5,PS	ILOWER PRIORITY
012556	000167	175016			JMP	OVRUN	IJUMP TO EVERRUN TEST
012562	000000			BOTTOM:	0		IBOTTOM OF TUMBLE TABLE
012564	000000				0		
012566	000000				0		
012570	000000				0		
012572	000000			TOP:	0		

```

*****PART2 DB25S CONNECTOR TEST SECTION*****
012574 000005          BEGIN2I RESET
012576 012706 001100      MOV      #BEGIN1,SP      ISET UP STACK POINTER
012602 012767 000340 165166  MOV      #340,PS      ISET PROCESSOR PRIORITY = 7
012610 032767 000200 164752  BIT      #BIT7,SWR     ITEST FOR CHANGE IN DP ADRS
012616 001404          BEQ      BGN0A         IBRANCH IF NO CHANGE
012620 004767 166446      JSR      X7,CLRVEC     ILOAD ENTIRE VECTOR AREA WITH
                                I ,+2
                                I HALT
                                IFETCH LINE NUMBER FROM SWR
012624 004767 166310      JSR      X7,LINE,N
012630 000167 000204      BGN0A1  JMP      BGN3

,MACR  DELAY  N          IWHERE N=TENS OF MICROSECONDS
      MOV    #N,CNT      ISET UP COUNT
DEL=,  DEC    CNT        ITIME OUT
      BNE   DEL         INO
,ENDM  IYES

I
IMACRO TO TEST READ/WRITE AND CLEAR CAPABILITY OF
IALL BITS IN XMIT & RCV STATUS
,MACR  BITSR  N,R          IBIT TEST STATUS REG "R" BIT "N"
      BIS    #BIT'N',@DPIR'S  ISET BIT N
      BIT    #BIT'N',@DPIR'S  IBIT N SET?
      BNE    ,+4             IYES
      ERROR  IREPORT ERROR
      BIC    #BIT'N',@DPIR'S  ICLEAR BIT N
      BIT    #BIT'N',@DPIR'S  IBIT CLEAR
      BEQ    ,+4             IYES
      ERROR  IREPORT ERROR
      BIS    #BIT'N',@DPIR'S  ISET BIT N
      BIT    #BIT'N',@DPIR'S
      BNE    ,+4
      ERROR  IREPORT ERROR
      CLR    @DPIR'S         ICLEAR BIT "N" BY CLR
      BIT    #BIT'N',@DPIR'S
      BEQ    ,+4
      ERROR  IREPORT ERROR
,ENDM

```

ICLOCK, SUBROUTINE TO RUN SOFTWARE CLOCK
 INUMBER OF CYCLES IS FETCHED CALL

012634	012567	176416		CLOCKI	MOV	(R5),CLKCNT	IFETCH CLOCK COUNT
012640	032767	000400	176404		BIT	#BIT8,SAVSR1	I12/8 BITS/CHAR
012646	001411				BEQ	CLK	I BRANCH IF 8 BITS/CHAR
012650	052777	002000	176346		BIS	#BIT10,@DPRS	ISELECT 12 BIT MODE
012656	052767	000400	176364		BIS	#BIT8,LIMIT	I9 BIT SYNC
012664	062767	000004	176364		ADD	#4,CLKCNT	I INCREASE CLOCK COUNT
012672	052777	000010	176332	CLKI	BIS	#BITS,@DPTS	ISET CLOCK HIGH
	012700			DEL#.			
012700	016767	000042	176362		MOV	FREQ,CNT	ISET UP DELAY COUNT
012706	005367	176356			DEC	CNT	IDECREMENT COUNT
012712	001372				BNE	DEL	I BRANCH IF NO TIMEOUT
012714	042777	000010	176310		BIC	#BITS,@DPTS	ISET CLOCK LOW
	012722			DEL#.			
012722	016767	000020	176340		MOV	FREQ,CNT	ISET UP DELAY COUNT
012730	005367	176334			DEC	CNT	IDECREMENT COUNT
012734	001372				BNE	DEL	I BRANCH IF NO TIMEOUT
012736	005367	176314			DEC	CLKCNT	
012742	001353				BNE	CLK	
012744	000205				RTS	X5	
012746	000001			FREQI	1		I NORMAL 12,8 US DELAY I PATCH FOR 50 FT CABEL

IMCLOCK, MACRO TO RUN SOFTWARE CLOCK N CYCLES

```

.MACR MCLK N
    MOV #N,CLKCNT
    I CLOCK N TIMES
    I CLOCK COUNT
MCLK#.
```

	BIS	#BITS,@DPTS	ISET CLOCK HIGH
DEL#.			
	MOV	FREQ,CNT	ISET UP DELAY COUNT
	DEC	CNT	IDECREMENT COUNT
	BNE	DEL	I BRANCH IF NO TIMEOUT
	BIC	#BITS,@DPTS	ISET CLOCK LOW
DEL#.			
	MOV	FREQ,CNT	ISET UP DELAY COUNT
	DEC	CNT	IDECREMENT COUNT
	BNE	DEL	I BRANCH IF NO TIMEOUT
	DEC	CLKCNT	
	BNE	MCLK	

```

.ENDM

```

IREE, SUBROUTINE TO REINITIALIZE DP11 FOR NEXT TEST

012750	012767	000200	165020	REEI	MOV	#200,PS	ISET PRIORITY TO 4
012756	005077	176250			CLR	@DPTS	ICLEAR XMIT STATUS
012762	005077	176236			CLR	@DPRS	ICLEAR RCV STATUS
012766	105077	176244			CLRB	@SEXT	ICLEAR SYNC EXTENTION
012772	012767	000001	176266		MOV	#1,TSYNC	I INIT TEST SYNC
013000	012777	011476	176232		MOV	#FRINT,@DPRIV	ISET UP RVI INT VECTOR
013006	012777	011532	176230		MOV	#TV18,@DPTIV	ISET XMIT INT VECTOR TO SYNC

013014 032767 000400 176230
 013022 001405
 013024 062705 000010
 013030 052777 002000 176166
 013036 000205

BIT #BIT8,SAVSR1
 BEQ REE1
 ADD #10,R5
 BIS #BIT10,@DPRS
 REE1: RTS X5
 ;*****TEST 1: CABLE TESTS

!TEST FOR 8/12 BITS/CHAR
 !EXIT IF 8 BITS
 !SET RETURN ADRS FOR 12 BIT LIMIT
 !SET 12 BIT/CHAR MODE
 !RETURN

013040 012767 013054 176110
 013046 012767 000000 176076
 013054 104400
 013056 000005
 013060 112777 000026 176142
 013066 012767 013040 175736
 013074 005077 176132
 013100 105077 176132
 013104 005077 176114
 013110 012777 011472 176126
 013116 012777 011476 176114
 013124 012777 000240 176110
 013132 012777 000240 176106
 013140 004567 177470
 013144 000030

BGN3: MOV #BGN3A,RETURN
 MOV #0,,ICOUNT
 BGN3A: SCOPE
 RESET
 MOVB #26,@SYNC
 MOV #BGN3,PUP1+2
 CLR @DPTS
 CLR @SEXT
 CLR @DPRS
 MOV #FTINT,@DPTIV
 MOV #FRINT,@DPRIV
 MOV #240,@DPRP
 MOV #240,@DPTP
 JSR X5,CLOCK
 30

!SET UP SCOPE RETURN
 !ITERATION = 0;
 !CLEAR NOISE FROM SYNC
 !SET UP PFAIL RETURN ADRS
 !CLEAR TRANSMITTER STATUS
 !CLEAR SYNC EXT
 !CLEAR RECEIVER STATUS
 !SET UP TRANSMITTER TEST VECTOR 1
 !SET UP RECEIVER TEST VECTOR 1
 !SET UP RECEIVER PRIORITY=6
 !SET UP TRANSMITTER PRIORITY=6
 !RUN CLOCK

ISYNCHRONIZATION CHARACTER TEST 8/12 BITS/CHARACTER
 IINTERRUPT ENABLE, COMPARE SYNC, TEST PARITY

213146	004567	177576		JSR	X5,REE	IREINIT FOR TEST
213152	012767	000376	176070	MOV	#376,LIMIT	I8 BIT SYNC LIMIT
213160	000403			BR	,+10	I BRANCH AROUND 12 BIT LIMIT
IFEE WILL ENER HERE IF 12 BITS/CHAR						
213162	012767	007776	176060	MOV	#7776,LIMIT	ISET UP 12 BITS/CHAR LIMIT
213170	012767	013512	003706	MOV	#SSYC4A,SRV5B	ISET UP RCV SERVICE RETURN
213176	012777	011532	176040	SSYC4I	MOV #TV18,@DPTIV	ISET XMIT INT VECTOR TO SYNC
213204	012767	000003	176060	MOV	#3,SCNT	ISYNC COUNT = 3
213212	004567	177416		JSR	X5,CLOCK	IRUN CLOCK
213216	000030			30		
213220	116777	176042	176002	MOVB	TSYNC,@SYNC	ILOAD SYNC BUFFER
213226	116777	176035	176002	MOVB	TSYNC+1,@SEXT	ILOAD SYNC EXT
213234	052777	000100	175742	BIS	#BIT6,@DPRS	IRCV INT ENB
213242	052777	000300	175742	BIS	#300,@DPTS	IXMIT INT ENB
213250	012767	000003	176000	MCLK	3	
	013256			MOV	#3,CLKCNT	ICLOCK COUNT
213256	052777	000010	175746	MCLK#.	BIS #BIT3,@DPTS	ISET CLOCK HIGH
	013264			DEL#.		
213264	016767	177456	175776	MOV	FREQ,CNT	ISET UP DELAY COUNT
213272	005367	175772		DEC	CNT	IDECREMENT COUNT
213276	001372			BNE	DEL	I BRANCH IF NO TIMEOUT
213300	042777	000010	175724	BIC	#BIT3,@DPTS	ISET CLOCK LOW
	013306			DEL#.		
213306	016767	177434	175754	MOV	FREQ,CNT	ISET UP DELAY COUNT
213314	005367	175750		DEC	CNT	IDECREMENT COUNT
213320	001372			BNE	DEL	I BRANCH IF NO TIMEOUT
213322	005367	175730		DEC	CLKCNT	
213326	001353			BNE	MCLK	
213330	032777	001000	175674	BIT	#BIT9,@DPTS	I SEND REQUEST UP?
213336	001001			BNE	,+4	IYES
213340	104000			ERROR		I REPORT ERROR
213342	004567	177266		JSR	X5,CLOCK	IRUN CLOCK
213346	000010			10		
213350	032777	004000	175646	BIT	#BIT11,@DPRS	I RECEIVER ACTIVE
213356	001401			BEQ	,+4	INO
213360	104000			ERROR		I REPORT ERROR
213362	004567	177246		JSR	X5,CLOCK	IRUN CLOCK
213366	000007			7		
213370	032777	004000	175634	BIT	#BIT11,@DPTS	IRCV ACTIVE?
213376	001401			BEQ	,+4	INO
213400	104000			ERROR		I REPORT ERROR
213402	012767	000001	175646	MCLK	1	
	013410			MOV	#1,CLKCNT	ICLOCK COUNT
213410	052777	000010	175614	MCLK#.	BIS #BIT3,@DPTS	ISET CLOCK HIGH
	013416			DEL#.		
213416	016767	177324	175644	MOV	FREQ,CNT	ISET UP DELAY COUNT
213424	005367	175640		DEC	CNT	IDECREMENT COUNT
213430	001372			BNE	DEL	I BRANCH IF NO TIMEOUT
213432	042777	000010	175572	BIC	#BIT3,@DPTS	ISET CLOCK LOW

013440	016767	177302	175622	DEL=.	MOV	FREQ,CNT	ISET UP DELAY COUNT
013446	005367	175616			DEC	CNT	IDECREMENT COUNT
013452	001372				BNE	DEL	IBRANCH IF NO TIMEOUT
013454	005367	175576			DEC	CLKCNT	
013460	001353				BNE	MCLK	
013462	032777	004000	175534		BIT	#BIT11,@DPRS	IRCV ACTIVE?
013470	001001				BNE	,+4	IYES
013472	104000				ERROR		IREPORT ERROR
013474	012777	017044	175536		MOV	#SRV5,@OPRIV	ITEST PASS VECTOR
013502	004567	177126			JSR	%5,CLOCK	IRUN CLOCK
013506	000010				LD		
013510	104000				ERROR		IREPORT ERROR
013512	042777	004000	175504	SSYC4A1	BIC	#BIT11,@DPRS	ICLEAR ACTIVE
013520	042777	000100	175504		BIC	#BIT6,@DPTS	ICLEAR INT ENB
013526	032767	040000	164034		BIT	#BIT14,SWR	ITEST FOR SCOPE LOOP
013534	001220				BNE	SSYC4	IBRANCH IF SCOPE LOOP
013536	112777	000026	175464		MOVB	#26,@SYNC	ICHANGE SYNC
013544	005267	175516			INC	TSYNC	INEXT SYNC, ENTRY FROM INTERRUPT
013550	026767	175474	175510		CMP	LIMIT,TSYNC	IHAVE ALL SYNC'S BEEN TESTED
013556	001207				BNE	SSYC4	

```

;SYNCHRONIZATION CHARACTER TEST 7/11 BITS/CHARACTER
;INTERRUPT ENABLE AND SYNC CHARACTER CHECK
213560 004567 177164 JSR X5,REE ;REINIT DP11
;RETURN HERE IF 8 BITS/CHAR
213564 012767 000176 175456 MOV #176,LIMIT ;17 BIT LIMIT
213572 000403 BR ,+10 ;BRANCH AROUND 12 BITS/CHAR LIMIT
;RETURN HERE IF 12 BITS/CHAR
213574 012767 003776 175446 MOV #3776,LIMIT ;11 BITS/CHAR LIMIT
213602 052777 000400 175414 BIS #BIT8,@DPRS ;17/11 BITS PER CHAR
213610 012767 014132 003266 MOV #SSYC5A,@RV5B ;SET UP RCV SERVICE RETURN
213616 012777 011476 175414 MOV #FRINT,@DPRIV ;FALSE INT TEST VECTOR
213624 012777 011532 175412 SSYC51 MOV #TV18,@DPTIV ;SET XMIT INT VECTOR TO SYNC
213632 012767 000003 175432 MOV #3,SCNT ;XMIT 3 SYNCs
213640 004567 176770 JSR X5,CLOCK ;RUN CLOCK
213644 000024 24
213646 116777 175414 175354 MOVB TSYNC,@SYNC ;LOAD SYNC BUFFER
213654 052777 000300 175350 BIS #300,@DPTS ;XMIT INT ENB
213662 052777 000100 175334 BIS #BIT6,@DPRS ;RCINT ENB
MCLK,
213670 012767 000003 175360 MOV #3,CLKCNT ;CLOCK COUNT
213676 052777 000010 175326 BIS #BIT3,@DPTS ;SET CLOCK HIGH
DEL#,
213704 016767 177036 175356 MOV FREQ,CNT ;SET UP DELAY COUNT
213712 005367 175352 DEC CNT ;DECREMENT COUNT
213716 001372 BNE DEL ;BRANCH IF NO TIMEOUT
213720 042777 000010 175304 BIC #BIT3,@DPTS ;SET CLOCK LOW
DEL#,
213726 016767 177014 175334 MOV FREQ,CNT ;SET UP DELAY COUNT
213734 005367 175330 DEC CNT ;DECREMENT COUNT
213740 001372 BNE DEL ;BRANCH IF NO TIMEOUT
213742 005367 175310 DEC CLKCNT
213746 001353 BNE MCLK
213750 032777 001000 175254 BIT #BIT9,@DPTS ;SEND REQUEST UP?
213756 001001 BNE ,+4
213760 104000 ERROR ;REPORT ERROR
213762 004567 176646 JSR X5,CLOCK ;RUN CLOCK
213766 000007 7
213770 032777 004000 175226 BIT #BIT11,@DPRS ;RECEIVER ACTIVE
213776 001401 BEQ ,+4 ;NO
214000 104000 ERROR ;REPORT ERROR
214002 004567 176626 JSR X5,CLOCK ;RUN CLOCK
214006 000006 6
214010 032777 004000 175214 BIT #BIT11,@DPTS ;RCV ACTIVE?
214016 001401 BEQ ,+4 ;NO
214020 104000 ERROR ;REPORT ERROR
MCLK,
214022 012767 000001 175226 MOV #1,CLKCNT ;CLOCK COUNT
214030 052777 000010 175174 BIS #BIT3,@DPTS ;SET CLOCK HIGH
DEL#,
214036 016767 176704 175224 MOV FREQ,CNT ;SET UP DELAY COUNT
214044 005367 175220 DEC CNT ;DECREMENT COUNT
214050 001372 BNE DEL ;BRANCH IF NO TIMEOUT

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014052	042777	000010	175152		BIC	#BITS,@DPTS	ISSET CLOCK LOW
	014060			DEL=.			
014060	016767	176662	175202		MOV	FREQ,CNT	ISSET UP DELAY COUNT
014066	005367	175176			DEC	CNT	IDECREMENT COUNT
014072	001372				BNE	DEL	IBRANCH IF NO TIMEOUT
014074	005367	175156			DEC	CLKCNT	
014100	001353				BNE	MCLK	
014102	032777	004000	175114		BIT	#BIT11,@DPRS	IRCV ACTIVE?
014110	001001				BNE	,+4	IYES
014112	104000				ERROR		IREPORT ERROR
014114	012777	017044	175116		MOV	#SRV5,@DPRIV	ITEST PASS VECTOR
014122	004567	176506			JSR	X5,CLOCK	IRUN CLOCK
014126	000007				7		
014130	104000				ERROR		IREPORT ERROR
014132	042777	004000	175064	SSYCSAI	BIC	#BIT11,@DPRS	ICLEAR RCV ACTIVE
014140	042777	000100	175064		BIC	#BIT6,@DPTS	ICLEAR XMIT INT ENB
014146	112777	000026	175054		MOVVB	#26,@SYNC	IDUMMY SYNC
014154	032767	040000	163406		BIT	#BIT14,SWR	ITEST FOR SCOPE LOOP
014162	001220				BNE	SSYCS	IBRANCH IF SCOPE
014164	005267	175076			INC	TSYNC	INEXT SYNC
014170	026767	175054	175070		CMP	LIMIT,TSYNC	IHAVE ALL SYNC'S BEEN TESTED
014176	001212				BNE	SSYCS	

ISYNCHRONIZATION CHARACTER TEST 6/10 BITS/CHARACTER
 INTERRUPT ENABLE AND SYNC CHARACTER CHECK

014200	004567	176544			JSR	X5,REE	IREINIT DP11
014204	012767	000075	175036		MOV	#75,LIMIT	I6 BIT LIMIT
014212	000403				BR	,+10	IBRANCH AROUND 10 BIT LIMIT
					IRETURN HERE IF 10 BITS/CHAR		
014214	012767	001775	175026		MOV	#1775,LIMIT	ISSET UP 10 BITS/CHAR
014222	052777	001000	174774		BIS	#BIT9,@DPRS	I6/10 BITS/CHAR
014230	012767	014566	002646		MOV	#SSYCS6A,SRV5B	ISSET UP RCV SERVICE RETURN
014236	012777	011532	175000	SSYCS6I	MOV	#TV18,@DPTIV	ISSET XMIT INT VECTOR TO SYNC
014244	012767	000003	175020		MOV	#3,SCNT	IXMIT 3 SYNC'S
014252	042777	000100	174752		BIC	#BIT6,@DPTS	ICLEAR XMIT INT ENB
014260	042777	004000	174736		BIC	#BIT11,@DPRS	ICLEAR ACTIVE
014266	112777	000026	174734		MOVVB	#26,@SYNC	ICHALGE SYNC
014274	004567	176334			JSR	X5,CLOCK	IRUN CLOCK
014300	000021				21		
014302	116777	174760	174720		MOVVB	TSYNC,@SYNC	ILOAD SYNC BUFFER
014310	052777	000100	174706		BIS	#BIT6,@DPRS	IRCVINT ENB
014316	052777	000300	174706		BIS	#300,@DPTS	IXMIT INT ENB
					MCLK	3	
014324	012767	000003	174724		MOV	#3,CLKCNT	ICLOCK COUNT
	014332			MCLK=.			
014332	052777	000010	174672		BIS	#BITS,@DPTS	ISSET CLOCK HIGH
	014340			DEL=.			
014340	016767	176402	174722		MOV	FREQ,CNT	ISSET UP DELAY COUNT
014346	005367	174716			DEC	CNT	IDECREMENT COUNT
014352	001372				BNE	DEL	IBRANCH IF NO TIMEOUT
014354	042777	000010	174650		BIC	#BITS,@DPTS	ISSET CLOCK LOW
	014362			DEL=.			
014362	016767	176360	174700		MOV	FREQ,CNT	ISSET UP DELAY COUNT
014370	005367	174674			DEC	CNT	IDECREMENT COUNT
014374	001372				BNE	DEL	IBRANCH IF NO TIMEOUT

PALX11	V003	11-AUG-71	17139	PAGE 26-2			
014376	005367	174654		DEC	CLKCNT		
014402	001353			BNE	MCLK		
014404	032777	001000	174620	BIT	#BIT9,@DPTS	ISEND REQUEST UP?	
214412	001001			BNE	,+4		
014414	104000			ERROR		IREPORT ERROR	
214416	004567	176212		JSR	X5,CLOCK	IRUN CLOCK	
014422	000006			6			
014424	032777	004000	174572	BIT	#BIT11,@DPRS	IRECEIVER ACTIVE	
014432	001401			BEG	,+4	INO	
014434	104000			ERROR		IREPORT ERROR	
014436	004567	176172		JSR	X5,CLOCK	IRUN CLOCK	
014442	000005			5			
014444	032777	004000	174560	BIT	#BIT11,@DPTS	IRCV ACTIVE?	
014452	001401			BEG	,+4	INO	
014454	104000			ERROR		IREPORT ERROR	
				MCLK	1		
014456	012767	000001	174572	MOV	#1,CLKCNT	ICLOCK COUNT	
	014464						
014464	052777	000010	174540	MCLK#.	BIS	#BIT3,@DPTS	ISSET CLOCK HIGH
	014472			DEL#.			
014472	016767	176250	174570	MOV	FREQ,CNT	ISSET UP DELAY COUNT	
014500	005367	174564		DEC	CNT	IDECREMENT COUNT	
014504	001372			BNE	DEL	IBRANCH IF NO TIMEOUT	
014506	042777	000010	174516	BIC	#BITS,@DPTS	ISSET CLOCK LOW	
	014514			DEL#.			
014514	016767	176226	174546	MOV	FREQ,CNT	ISSET UP DELAY COUNT	
014522	005367	174542		DEC	CNT	IDECREMENT COUNT	
014526	001372			BNE	DEL	IBRANCH IF NO TIMEOUT	
014530	005367	174522		DEC	CLKCNT		
014534	001353			BNE	MCLK		
014536	032777	004000	174460	BIT	#BIT11,@DPRS	IRCV ACTIVE?	
014544	001001			BNE	,+4	IYES	
014546	104000			ERROR		IREPORT ERROR	
014550	012777	017044	174462	MOV	#SRV5,@DPRIV	ITEST VECTOR	
014556	004567	176052		JSR	X5,CLOCK	IRUN CLOCK	
014562	000006			6			
014564	104000			ERROR		IREPORT ERROR	
014566	042777	004000	174430	SSYC6A:	BIC	#BIT11,@DPRS	
014574	112777	000026	174426	MOVB	#26,@SYNC		
014602	032767	040000	162760	BIT	#BIT14,SWR	ITEST FOR SCOPE LOOP	
014610	001212			BNE	SSYC6	IBRANCH IF SCOPE	
014612	005267	174450		INC	TSYNC	INEXT SYNC	
014616	026767	174426	174442	CMP	LIMIT,TSYNC	IHAVE ALL SYNC'S BEEN TESTED	
014624	001402			BEG	,+6	IYES	
014626	000167	177404		JMP	SSYC6	INO	
014632	104400			SCOPE			

INTERRUPT DRIVEN SEQUENTIAL DATA TEST

Address	Op1	Op2	Op3	Op4	Op5	Op6	Op7
014634	005067	174312		SSEQD1	CLR	ICOUNT	ISET ITERATION COUNT TO 1
014640	105077	174372			CLRB	@SEXT	ICLEAR SYNC EXTENTION
014644	005067	174434			CLR	RDATA	I RECEIVER DATA
014650	005067	174432			CLR	TDATA	I TRANSMITTER DATA
014654	005077	174344			CLR	@DPRS	I RECEIVER STATUS
014660	005077	174346			CLR	@DPTS	I TRANSMITTER STATUS
014664	052777	000001	174332		BIS	#BIT0,@DPRS	I STRIP SYNC
014672	012767	015146	175164		MOV	#R2AND,R20*2	ISET UP RETURN ADDRESS
							I REPLACE #R2AND WITH #SSEQD
							I FOR CONTINUOUS DATA
							I CHAR LENGTH INDEX
							I TEST 12 BIT CHAR MODE
							INO
							I SELECT END OF DATA
							I SELECT 12 BITS/CHARACTER
							I SYNC FOR 12 BIT CHAR
							I PLACE MSB OF SYNC IN SYNC EXT
014700	012767	000400	174370		MOV	#400,CHLEN	I TEMPORARY CHARACTER LIMIT
014706	032767	000400	174336		BIT	#BIT8,SAVSR1	I INIT SYNC STORAGE
014714	001414				BEG	SSEQD2	I TRANSMITTER VECTOR
014716	012767	010000	174324		MOV	#10000,LIMIT	I RECEIVER VECTOR
014724	052777	002000	174272		BIS	#BIT10,@DPRS	I PRIORITY#4
014732	012767	000426	174326		MOV	#426,TSYNC	I SYNC COUNT#4
014740	105277	174272			INCB	@SEXT	I LOAD SYNC
014744	000406				BR	SSEQD3	I RCV INT ENB
014746	012767	000400	174274	SSEQD21	MOV	#400,LIMIT	I STATUS INT ENB
014754	012767	000026	174304		MOV	#26,TSYNC	I TRANS INT ENB
014762	012777	011532	174254	SSEQD31	MOV	#TV16,@DPTIV	I TRANS DONE
014770	012777	011652	174242		MOV	#RV16,@DPRIV	
014776	012767	000200	162772		MOV	#200,PS	
015004	012767	000004	174260		MOV	#4,SCNT	
015012	116777	174250	174210		MOV#B	TSYNC,@SYNC	
015020	052777	000100	174176		BIS	#BIT6,@DPRS	
015026	052777	000340	174176		BIS	#340,@DPTS	
015034	022767	000001	175704		CMP	#1,FREQ	I TEST FOR HIGH SPEED
015042	001010				BNE	SCLK3	I BRANCH IF NOT HIGH SPEED
015044	052777	000010	174160	SCLK21	BIS	#BIT3,@DPTS	I SET CLOCK HIGH
015052	042777	000010	174152		BIC	#BIT3,@DPTS	I SET CLOCK LOW
015060	000771				BR	SCLK2	
015062	000000				HALT		
015064	012767	000001	174164	SCLK31	MCLK	1	I RUN SLOW CLOCK
	015072				MOV	#1,CLKCNT	I CLOCK COUNT
015072	052777	000010	174132	MCLK#.	BIS	#BIT3,@DPTS	I SET CLOCK HIGH
	015100			DEL#.			
015100	016767	175642	174162		MOV	FREQ,CNT	I SET UP DELAY COUNT
015106	005367	174156			DEC	CNT	I DECREMENT COUNT
015112	001372				BNE	DEL	I BRANCH IF NO TIMEOUT
015114	042777	000010	174110		BIC	#BIT3,@DPTS	I SET CLOCK LOW
	015122			DEL#.			
015122	016767	175620	174140		MOV	FREQ,CNT	I SET UP DELAY COUNT
015130	005367	174134			DEC	CNT	I DECREMENT COUNT
015134	001372				BNE	DEL	I BRANCH IF NO TIMEOUT
015136	005367	174114			DEC	CLKCNT	
015142	001353				BNE	MCLK	

015144 000747

BR SCLK3

;*****

;RANDOM DATA RANDOM IDLE

015146	104400			R2ANDI	SCOPE		
015150	005067	173776		CLR	ICOUNT		;ITERATIONS * 1
015154	105077	174056		CLRB	@SEXT		;CLEAR SYNC EXTENTION
015160	012767	177400	174110	MOV	#177400,CHLEN		;SET CHAR LENGTH TO 8 BITS
015166	012767	000026	174072	MOV	#26,TSYNC		;SYNC * 26
015174	116777	174066	174026	MOVB	TSYNC,@SYNC		;LOAD SYNC BUFFER
015202	012701	015371		MOV	#15371,R1		;PRIME RANDOM * GEN
015206	012702	072414		MOV	#72414,R2		
015212	012703	004036		MOV	#4036,R3		
015216	104400			SCOPE			
015220	004767	000112		JSR	X7,A2ND		
015224	104400			SCOPE			

;REPEAT PREVIOUS TEST AT 7 BITS/CHAR

015226	012767	177600	174042	MOV	#177600,CHLEN		;SET CHAR LENGHT TO 7 BITS
015234	052777	000400	173762	BIS	#BIT0,@DPRS		;7 BITS/CHAR
015242	042777	004000	173754	BIC	#BIT11,@DPRS		;CLEAR ACTIVE
015250	104400			R2ANDAI	SCOPE		
015252	004767	000060		JSR	X7,A2ND		
015256	104400			SCOPE			

REPEAT PREVIOUS TEST AT 6 BITS/CHAR

015260	012767	177700	174010	MOV	#177700,CHLEN	ICLEAR CHAR LENGTH TO 6 BITS
015266	042777	000400	173730	BIC	#BIT8,@DPRS	
215274	052777	001000	173722	BIS	#BIT9,@DPRS	ICLEAR MODE TO 6 BITS/CHAR
215302	042777	004000	173714	BIC	#BIT11,@DPRS	ICLEAR ACTIVE
015310	104400			R2=NDBI	SCOPE	
015312	004767	000020		JSR	X7,A2ND	
015316	104400				SCOPE	
015320	042777	007700	173676	L200PI	BIC #7700,@DPRS	ICLEAR RCV STATUS
015326	042777	160343	173676		BIC #160343,@DPTS	ICLEAR XMIT STATUS
015334	000550			BR	SENR	
				ICOMMON	DATA AND IDLE SUBROUTINE	
015336	042777	004300	173660	A2NDI	BIC #4300,@DPRS	IRCV INT ENB, RCV ACTIVE
015344	042777	160342	173660		BIC #160342,@DPTS	IINT ENBS IDLE SYNC, ERRORS
015352	012767	012562	173764		MOV #BOTTOM,RP	IRP = BOTTOM OF TUMBLE TABLE
015360	016767	173760	173754		MOV RP,TP	ICLEAR UP TRANSMIT POINTER
015366	012767	000004	173556		MOV #4,ICOUNT	ITERATIONS = 10
015374	012777	012220	173636		MOV #RRRR,@DPRIV	IRCV INT VECTOR
015402	012777	012066	173634		MOV #RRRT,@DPTIV	IXMIT INT VECTOR
015410	012767	000002	173654		MOV #2,SCNT	ISYNC COUNT = 2
015416	110267	173664		MOV	R2,TDATA	IRANDOM DATA
015422	016777	173640	173604	MOV	TSYNC,@DPTB	ILOAD BUFFER
015430	052777	000100	173566	BIS	#100,@DPRS	IRCV INT ENB
015436	052777	000140	173566	BIS	#140,@DPTS	IXMIT INT ENB
015444	010167	173670		T2IM0I	MOV R1,TIME	I"ON" STALL
				T2IM1I	MCLK	
015450	012767	000001	173600		MOV #1,CLKCNT	ICLOCK COUNT
	013456			MCLK=,		
015456	052777	000010	173546		BIS #BIT3,@DPTS	ICLEAR CLOCK HIGH
	013464			DEL=,		
015464	016767	175256	173576		MOV FREQ,CNT	ICLEAR UP DELAY COUNT
015472	005367	173572			DEC CNT	IDECREMENT COUNT
015476	001372				BNE DEL	IBRANCH IF NO TIMEOUT
015500	042777	000010	173524		BIC #BIT3,@DPTS	ICLEAR CLOCK LOW
	013506			DEL=,		
015506	016767	175234	173554		MOV FREQ,CNT	ICLEAR UP DELAY COUNT
015514	005367	173550			DEC CNT	IDECREMENT COUNT
015520	001372				BNE DEL	IBRANCH IF NO TIMEOUT
015522	005367	173530			DEC CLKCNT	
015526	001353				BNE MCLK	
015530	005367	173604			DEC TIME	ICLEAR 0.6 SEC AVERAGE
015534	001345				BNE T2IM1	
015536	042777	000140	173466		BIC #140,@DPTS	ITURN OFF INT ENB
015544	052777	000002	173460		BIS #BIT1,@DPTS	IDLE SYNC
015552	004567	173404			JSR X5,RNUM	IGENERATE "STALL" TIME
015556	010167	173556			MOV R1,TIME	I
				T2IM2I	MCLK	
015562	012767	000001	173466		MOV #1,CLKCNT	ICLOCK COUNT
	015570			MCLK=,		
015570	052777	000010	173434		BIS #BIT3,@DPTS	ICLEAR CLOCK HIGH
	015576			DEL=,		

015576 016767 175144 173464
015604 005367 173460
015610 001372
015612 042777 000010 173412
015620
015620 016767 175122 173442
015626 005367 173436
015632 001372
015634 005367 173416
015640 001353
015642 005367 173472
015646 001345
015650 004567 173306
015654 000207

DEL = .

MOV FREQ,CNT
DEC CNT
BNE DEL
BIC #BIT3,0DPTS
MOV FREQ,CNT
DEC CNT
BNE DEL
DEC CLKCNT
BNE MCLK
DEC TIME
BNE T2IM2
JSR X5,RNUM
RTS X7

ISET UP DELAY COUNT
IDECREMENT COUNT
IBRANCH IF NO TIMEOUT
ISET CLOCK LOW
ISET UP DELAY COUNT
IDECREMENT COUNT
IBRANCH IF NO TIMEOUT
ICOUNT IDLE TIME
ITIME OUT?
IGENERATE "ON" TIME + SYNC

IOB255 TEST CONNECTOR DISCRETE EVENTS TEST

VERIFY "SEND REQUEST" RAISES "CLEAR-TO-SEND" AND "MODEM READY"
 WHEN TRANSMITTER BUFFER IS LOADED

015656	104400			SENDR1	SCOPE		
015660	012767	000010	173264		MOV	#10,ICOUNT	ITERATIONS = 10
015666	012767	000240	162102		MOV	#240,PS	IPRIORITY=5
015674	005077	173332			CLR	@DPTS	ICLR XMIT STATUS
015700	005077	173320			CLR	@DPRS	ICLR RCV STATUS
015704	004567	174724			JSR	X5,CLOCK	IRUN CLOCK
015710	000010				10		
015712	012777	011472	173324		MOV	#FTINT,@DPTIV	IXMIT ERROR TRAP VECTOR
015720	012777	011476	173312		MOV	#FRINT,@DPRIV	IRCV ERROR TRAP VECTOR
015726	052777	000040	173276		BIS	#BITS,@DPTS	ISTATUS+RDY INT ENB
015734	016777	173346	173272		MOV	TDATA,@DPTB	ILOAD BUFFER
015742	004567	174666			JSR	X5,CLOCK	IRUN CLOCK
015746	000003				3		
015750	032777	001000	173254		BIT	#BIT9,@DPTS	I"SEND REQUEST" ON
015756	001001				BNE	,+4	IYES
015760	104000				ERROR		IREPORT ERROR
015762	032777	002000	173242		BIT	#BIT10,@DPTS	ICLEAR-TO-SEND" UP?
015770	001001				BNE	,+4	IYES
015772	104000				ERROR		IREPORT ERROR
015774	032777	010000	173230		BIT	#BIT12,@DPTS	I"MODEM READY" UP
016002	001001				BNE	,+4	IYES
016004	104000				ERROR		IREPORT ERROR
016006	004567	174622			JSR	X5,CLOCK	IRUN CLOCK
016012	000012				12		
016014	032777	001000	173210		BIT	#BIT9,@DPTS	I"SEND REQUEST" DOWN
016022	001401				BEQ	,+4	IYES
016024	104000				ERROR		IREPORT ERROR
016026	032777	002000	173176		BIT	#BIT10,@DPTS	I"CLEAR-TO-SEND" DOWN
016034	001401				BEQ	,+4	IYES
016036	104000				ERROR		IREPORT ERROR
016040	032777	010000	173164		BIT	#BIT12,@DPTS	I"MODEM READY" DOWN
016046	001401				BEQ	,+4	IYES
016050	104000				ERROR		IREPORT ERROR

PERFORM PREVIOUS TEST AT 7/11 BITS/CHARACTER

016052	012767	000240	161716		MOV	#240,PS	IPRIORITY = 5
016060	005077	173146			CLR	@DPTS	ICLR XMIT STATUS
016064	005077	173134			CLR	@DPRS	ICLR RCV STATUS
016070	012777	011472	173146	SENDR2	MOV	#FTINT,@DPTIV	IXMIT ERROR TRAP VECTOR
016076	012777	011476	173134		MOV	#FRINT,@DPRIV	IRCV ERROR TRAP VECTOR
016104	052777	000400	173112		BIS	#BITS,@DPRS	I7/11 BITS/CHARACTER
016112	052777	000040	173112		BIS	#BITS,@DPTS	ISTATUS+RDY INT ENB
016120	016777	173162	173106		MOV	TDATA,@DPTB	ILOAD BUFFER
016126	004567	174502			JSR	X5,CLOCK	IRUN CLOCK
016132	000003				3		
016134	032777	001000	173070		BIT	#BIT9,@DPTS	I"SEND REQUEST" ON
016142	001001				BNE	,+4	IYES

016144	104000			ERROR		JREPORT ERROR
016146	032777	002000	173056	BIT	#BIT10,@DPTS	I"CLEAR-TO-SEND" UP?
016154	001001			BNE	,*4	IYES
016156	104000			ERROR		JREPORT ERROR
016160	032777	010000	173044	BIT	#BIT12,@DPTS	I"MODEM READY" UP
016166	001001			BNE	,*4	IYES
016170	104000			ERROR		JREPORT ERROR
016172	004567	174436		JSR	X5,CLOCK	JRUN CLOCK
016176	000011			11		
016200	032777	001000	173024	BIT	#BIT9,@DPTS	I"SEND REQUEST" DOWN
016206	001401			BEG	,*4	IYES
016210	104000			ERROR		JREPORT ERROR
016212	032777	002000	173012	BIT	#BIT10,@DPTS	I"CLEAR-TO-SEND"DOWN
016220	001401			BEG	,*4	IYES
016222	104000			ERROR		JREPORT ERROR
016224	032777	010000	173000	BIT	#BIT12,@DPTS	I"MODEM READY" DOWN
016232	001401			BEG	,*4	IYES
016234	104000			ERROR		JREPORT ERROR

JPERFORM PREVIOUS TEST AT 6/10 BITS/CHARACTER

016236	012767	000240	161532	MOV	#240,PS	JPRIORITY = 5
016244	005077	172762		CLR	@DPTS	ICLR XMIT STATUS
016250	005077	172750		CLR	@DPRS	ICLR RCV STATUS
016254	012777	011472	172762	SENDR3: MOV	#FTINT,@DPTIV	I"XMIT ERROR TRAP VECTOR
016262	012777	011476	172750	MOV	#FRINT,@DPRIV	I"RCV ERROR TRAP VECTOR
016270	052777	001000	172726	BIS	#BIT9,@DPRS	I6 BITS/CHARACTER
016276	052777	000040	172726	BIS	#BIT5,@DPTS	I"STATUS+RDY INT ENB
016304	016777	172776	172722	MOV	TDATA,@DPTB	ILOAD BUFFER
016312	004567	174316		JSR	X5,CLOCK	JRUN CLOCK
016316	000003			3		
016320	032777	001000	172704	BIT	#BIT9,@DPTS	I"SEND REQUEST" ON
016326	001001			BNE	,*4	IYES
016330	104000			ERROR		JREPORT ERROR
016332	032777	010000	172672	BIT	#BIT12,@DPTS	I"MODEM READY" UP
016340	001001			BNE	,*4	IYES
016342	104000			ERROR		JREPORT ERROR
016344	004567	174264		JSR	X5,CLOCK	JRUN CLOCK
016350	000010			10		
016352	032777	001000	172652	BIT	#BIT9,@DPTS	I"SEND REQUEST" DOWN
016360	001401			BEG	,*4	IYES
016362	104000			ERROR		JREPORT ERROR
016364	032777	002000	172640	BIT	#BIT10,@DPTS	I"CLEAR-TO-SEND" DOWN
016372	001401			BEG	,*4	IYES
016374	104000			ERROR		JREPORT ERROR
016376	032777	010000	172626	BIT	#BIT12,@DPTS	I"MODEM READY" DOWN
016404	001401			BEG	,*4	IYES
016406	104000			ERROR		JREPORT ERROR

JDB255 TEST CONNECTCONNECTOR TEST

JVERIFY "SEND REQUEST" RAISES "MODEM READY" AND "CLEAR TO SEND"

016410 104400 SCOPE

016412	005077	172606		MORDYI	CLR	@DPRS	ICLEAR RCV STATUS
016416	005077	172610			CLR	@DPTS	ICLEAR XMIT STATUS
016422	016777	172654	172604		MOV	TMPDAT,@DPTB	ILOAD XMIT BUFFER
016430	004567	174200			JSR	X5,CLOCK	
016434	000004				4		
016436	032777	001000	172566		BIT	#BIT9,@DPTS	ISEND REQUEST UP?
016444	001001				BNE	,+4	IYES
016446	104000				ERROR		IREPORT ERROR
016450	032777	002000	172554		BIT	#BIT10,@DPTS	ICLEAR TO SEND?
016456	001001				BNE	,+4	IYES
016460	104000				ERROR		IREPORT ERROR
016462	032777	010000	172542		BIT	#BIT12,@DPTS	IMODEM READY?
016470	001001				BNE	,+4	IYES
016472	104000				ERROR		IREPORT ERROR
016474	104400				SCOPE		

ITERMINAL READY

				ITERM RDY-RAISE "CARRIER" AND "RING FLAG", NO INT ENB	
016476	012767	000240	161272	MOV #240,PS	IPRIORITY = 5
016504	005077	172522		CLR #DPTS	ICLR XMIT STATUS
016510	005077	172510		CLR #DPRS	ICLR RCV STATUS
016514	012777	011472	172510	MOV #FTINT,#DPTS	IERROR TRAP VECTOR
016522	052777	000001	172502	BIS #BIT0,#DPTS	ITERMINAL READY
				DELAY 1500	I15MS PROPOGATION DELAY
016530	012767	001500	172532	MOV #1500,CNT	ISET UP COUNT
	016536				
016536	005367	172526		DEL=, DEC CNT	ITIME OUT
016542	001375			BNE DEL	INO
016544	032777	000001	172460	BIT #BIT0,#DPTS	ITERMINAL READY
016552	001001			BNE ,+4	IYES
016554	104000			ERROR	IREPORT ERROR
016556	032777	004000	172446	BIT #BIT11,#DPTS	ICARRIER
016564	001001			BNE ,+4	IYES
016566	104000			ERROR	IREPORT ERROR
016570	032777	020000	172434	BIT #BIT13,#DPTS	IRING FLAG UP
016576	001001			BNE ,+4	IYES
016600	104000			ERROR	IREPORT ERROR
				ICLEAR TERMINAL READY	
016602	042777	000001	172422	BIC #BIT0,#DPTS	ICLEAR TERMINAL READY
				DELAY 1500	
016610	012767	001500	172452	MOV #1500,CNT	ISET UP COUNT
	016616				
016616	005367	172446		DEL=, DEC CNT	ITIME OUT
016622	001375			BNE DEL	INO
016624	032777	000001	172400	BIT #BIT0,#DPTS	ITERM RDY DOWN
016632	001401			BEG ,+4	IYES
016634	104000			ERROR	IREPORT ERROR
016636	032777	004000	172366	BIT #BIT11,#DPTS	ICARRIER DOWN
016644	001401			BEG ,+4	IYES
016646	104000			ERROR	IREPORT ERROR
016650	032777	100000	172354	BIT #BIT15,#DPTS	I"CARRIER DOWN" FLAG UP
016656	001001			BNE ,+4	IYES
016660	104000			ERROR	IREPORT ERROR
016662	042777	100000	172342	BIC #BIT15,#DPTS	ICLEAR DOWN FLAG
				IVERIFY THAT "RING" AND "CARRIER DOWN" INTERRUPT	
016670	012777	000240	172350	MOV #240,#DPTP	IINTERRUPT PRIORITY 5,
016676	005077	172330		CLR #DPTS	ICLEAR XMIT STATUS
016702	005077	172316		CLR #DPRS	ICLEAR RCV STATUS
016706	012777	011346	172330	MOV #TV24,#DPTIV	IEST PASS VECTOR
016714	012767	000200	161054	MOV #200,PS	IPRIORITY = 4
016722	052777	000040	172302	BIS #BIT5,#DPTS	ISTATUS INTERRUPT ENABLE
016730	052777	000001	172274	BIS #BIT0,#DPTS	ITERMINAL READY
				DELAY 1500	I15,75 MS DELAY
016736	012767	001500	172324	MOV #1500,CNT	ISET UP COUNT
	016744				
016744	005367	172320		DEL=, DEC CNT	ITIME OUT
016750	001375			BNE DEL	INO
016752	104000			ERROR	IREPORT ERROR

				VERIFY "CARRIER DOWN" RAISES INTERRUPT	
016754	012777	011420	172262	RCD11	MOV #TV25,@DPTV INEXT TEST VECTOR
016762	012767	000200	161006		MOV #200,PS
016770	042777	000001	172234		BIC #BIT0,@DPTS ICLEAR TERM, RDY, SHOULD SET 'CARRIER DOWN'.
					DELAY 1500 I15.75MS DELAY
016776	012767	001500	172264		MOV #1500,CNT ISET UP COUNT
	017004			DEL=.	
017004	005367	172260			DEC CNT ITIME OUT
017010	001375				BNE DEL INO
017012	104000				ERROR IREPORT ERROR
017014	046777	060760	172210		BIC BIT15,@DPTS ICLEAR "CARRIER DOWN"
017022	104400			BELL1	
017024	012777	000007	172170		MOV #7,@CTPB IYES, RING BELL
017032	105777	172162			TSTB @CTPS IPUNCH READY
017036	100375				BPL ,=4
017040	000167	173774			JMP BGN3

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)
)INTERRUPT SERVICE ROUTINES FOR DB25S TESTS
)
)THESE ROUTINES MAY FUNCTION AS:
) 1. ERROR TRAPS FOR FALSE INTERRUPTS
) 2. POINTERS BACK TO THE MAIN LINE FOR VALID INTERRUPTS
) 3. FUNCTIONAL TEST WHICH ARE INTERRUPT DRIVEN

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017044	032777	000200	172152	SRV5I	BIT	#BIT7,0DPRS	IRCV DONE
017052	001001				BNE	,+4	
017054	104000				ERROR		IREPORT ERROR
017056	126777	172204	172142		CMPB	TSYNC,0DPRB	ICORRECT SYNC CHARACTER
017064	001401				BEQ	,+4	IYES
017066	104000				ERROR		IREPORT ERROR
017070	022626				CMP	(SP)+,(SP)+	IADJUST STACK
017072	005726				TST	(SP)+	IADJUST STACK FOR CLOCK SUB
017074	042767	000040	160674		BIC	#BIT5,PS	ILOWER PRIORITY
017102	000137				137		IJMP
017104	013512			SRV5BI	SSYC4A		IBACK TO MAINLINE
	000001				.END		

A2ND	015336	DPRP	011242	NOP	000240	RRRR	012220
AND	007172	DPRS	011224	OR0	007646	RRRT	012066
ASCNT	010730	DPTB	011234	OR1	007662	RRT1	012132
BEGIN1	001100	DPTIV	011244	ORUN	010010	RT1	012212
BEGIN2	012574	DPTP	011246	OVRUN	007600	RT2	012130
BELL	017022	DPTS	011232	PARTY	007414	RV18	011652
BGN0	001134	DUPLX	010062	PC	000007R	RV18A	011704
BGN0A	012630	EMTAB	010262	PFAIL	010746	RWBR	002206
BGN1	001556	EMTOK	010242	PRINT1	010416	S0,EXT	005644
BGN3	013040	EMTVEC	010220	PRTAB	010450	S1,EXT	005724
BGN3A	013054	ERCOUN	011240	PS	177776	S2,EXT	006102
BINCT	010726	ERP0	010330	PUP1	011030	S3,EXT	006202
BIT0	000001	ERP1	010366	PWRUP	010756	S4,EXT	006162
BIT1	000002	ERRCNT	011332	R0	000000R	SAVPC	011310
BIT10	002000	ERROR	104000	R1	000001R	SAVR	010274
BIT11	004000	ERRP	010270	R17	012030	SAVR0	011314
BIT12	010000	EXT1	005154	R18	012040	SAVR1	011316
BIT13	020000	FLAG	011334	R19	012042	SAVR2	011320
BIT14	040000	FREQ	012746	R2	000002R	SAVR3	011322
BIT15	100000	FRINT	011476	R20	012062	SAVR4	011324
BIT2	000004	FTINT	011472	R2AND	013146	SAVR5	011326
BIT3	000010	HDFHM	010706	R2ANDA	015250	SAVREG	104001
BIT4	000020	HERE	000000	R2ANDB	015310	SAVCP	011312
BIT5	000040	ICOUNT	011152	R3	000003R	SAV01	011252
BIT6	000100	INTST1	004130	R4	000004R	SAV02	011254
BIT7	000200	INTST2	004260	R5	000005R	SCLK2	015044
BIT8	000400	INTST3	004520	R6	000006R	SCLK3	015064
BIT9	001000	INTST4	004630	RAND	007042	SCNT	011272
BITS	001552	IQTST5	004756	RANDA	007114	SCOPE	104400
BITST	001320	ISYC	006244	RANDB	007150	SCOPEA	011150
BOTTOM	012562	ISYC1	006310	RCD	016676	SCOPEB	011070
BPC	011262	ISYC2	006406	RCD1	016754	SCOPEC	011102
CG	011330	ISYC3	006414	RCNT	011336	SCOPEF	011154
CHLEN	011276	ISYC4	006432	RDATA	011304	SCOPEG	011140
CLEAR	001466	ISYC5	006454	REE	012750	SENDR	015656
CLK	012672	IT2A	004300	REE1	013036	SENDR2	016070
CLKCNT	011256	IT2B	004336	REG	001554	SENDR3	016254
CLOCK	012634	IT2C	004374	RESTOR	104002	SEQ0	006632
CLRVEC	001272	IT3A	004564	RESTR	010432	SEQ00	006616
CNT	011270	IT4A	004674	RETURN	011156	SEQ02	006750
CREG	003304	IT5A	005022	RNUM	011162	SEQ03	006764
CREG2	003476	L200P	015320	RNUM1	011212	SEVEN	010720
CTKB	011216	LIMIT	011250	RP	011344	SEXT	011236
CTKS	011214	LIMTMP	011274	RPRT1	012426	SGEN	011034
CTPB	011222	LINE,N	001140	RPRT2	012452	SLIM	011300
CTPS	011220	LIST	010732	RPRT3	012464	SLP	007574
CV1	001302	LOOP	007154	RPRT4	012514	SP	000006R
DECML	010722	MCLK	015570	RPRT5	012522	SRV5	017044
DEL	017004	MINUS	010530	RPRT6	012542	SRV5B	017104
DPLX1	010142	MKNUM	010560	RPRTY	012372	SRW0	005040
DPRB	011226	MOADD	010642	RR1	012254	SRW1	005064
DPRIV	011240	MORDY	016412	RR2	012266	SSEQD	014634

SSEQD2	014746	TV5	011510
SSEQD3	014762	TV6	011516
SSYC4	013176	TV7	011524
SSYC4A	013512	TY1	007536
SSYC5	013624	VALID	001432
SSYC5A	014132	VLID	003010
SSYC6	014236	WAIT1	010506
SSYC6A	014566	WAIT2	010664
STAG	007300	WGTCY	010724
STAR	010536	WRTOC	010600
START1	000200	XLIST	010656
SWR	177570		
SY	005224		
SYC02	005276		
SYC2	005304		
SYC2A	005440		
SYC2B	005466		
SYC2C	005572		
SYNC	011230		
SYNCNT	011264		
T18	011562		
T19	011650		
T2IM0	015444		
T2IM1	015450		
T2IM2	015562		
TAG2	006612		
TDATA	011306		
TIM0	007322		
TIM1	007326		
TIM2	007360		
TIME	011340		
TMPDAT	011302		
TOODLE	010716		
TOP	012572		
TP	011342		
TPRT1	012324		
TPRT2	012326		
TPRT3	012364		
TPRTY	012302		
TRTI	011502		
TST0	004500		
TSYNC	011266		
TV18	011532		
TV19	011564		
TV24	011346		
TV24A	011362		
TV24B	011402		
TV24C	011414		
TV25	011420		
TV25A	011434		
TV25B	011454		
TV25C	011466		

ERRORS DETECTED: 0

RUN-TIME: 30 SECONDS

5K CORE USED