IDENTIFICATION

PRODUCT CODE:	MAINDEC-11-DCKBN-A1-D
PRODUCT NAME:	11/45 PIRQ INTERUPT TEST
DATE CREATED:	15 MAR 1972
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR:	JOHN ADAMS

1,0 ABSTRACT

THIS IS A TEST OF THE PROGRAM INTERUPT REQUEST
(PIRQ) LOGIC,

2,0 REQUIREMENTS

2,1 EQUIPMENT
BASIC 11/45 SYSTEM

2,2 STORAGE
THIS PROGRAM USES 0 THRU 17500

2,3 PRELIMINARY PROGRAMS
D0AA THRU D0MA

3,0 LOADING PROCEDURE
LOAD PROGRAM USING ABS LOADER

4,0 STARTING PROCEDURE
LOAD ADDRESS 200, PRESS START, THE PROGRAM WILL LOOP
AND RING BELL ON PASS COMPLETION,

5,0 OPERATING PROCEDURE

5,1 SWITCH SETTINGS
NONE

5,2 SUBROUTINE ABSTRACTS

5,2,1 SCOPE
SCOPE IS A MOVE PC,R1 AND STORES THE PC+2 IN R1,

5,2,2 HLT
HLT IS A HALT INSTRUCTION,

6,0 ERRORS
ALL ERRORS WILL CAUSE A HALT
TRAP AND INTERRUPT ERRORS WILL CAUSE A HALT AT VECTOR+2,

6,1 ERROR RECOVERY
PRESS CONTINUE TO PROCEDE TO NEXT TEST

6,2 ERROR LOOPING
TO LOOP ON AN ERROR, PLACE A BRANCH TO THE PREVIOUS SCOPE
INSTRUCTION IN PLACE OF THE HALT INSTRUCTION,
NOTE THAT IF THE ERROR IS INTERMITTANT THAT THE TEST WILL
DROP THRU THE HALT AND PROCEED TO THE NEXT TEST,
THEREFORE, TO LOOP THE TEST CONTINUOSLY REPLACE THE BEQ ,+4
INSTRUCTION IMMEDIATLY PRECEEDING THE HALT WITH A BRANCH
BACK TO THE PREVIOUS SCOPE,

TO LOOP ON TRAP FAILURES, PATCH IN THE FOLLOWING ROUTINE
AT THE ADDRESS OF THE TRAP VECTOR,

```
TRAPVEC:        TRAPVEC+4
TRAPVEC+2:      0
TRAPVEC+4:      012716  ;MOVE SCOPE ADDRESS TO STACK
TRAPVEC+6:      ADDRESS ;ADDRESS OF PREVIOUS SCOPE
TRAPVEC+10:     000006  ;RETURN TO TEST AT SCOPE
```

RESTORE ALL LOCATIONS BEFORE PROCEEDING TO NEXT TEST,

7,0 RESTRICTIONS
NONE

8,0 MISCELLANEOUS
ON TRAP ERRORS THE STACK POINTER(R6) WILL CONTAIN THE ADDRESS WHERE THE TRAP OCCURED.

8,1 EXECUTION TIME
THIS PROGRAM TAKES ABOUT 1 MINUTE.

8,2 STACK POINTER
THIS PROGRAM INITIALY SETS THE STACK POINTER AT 500.

```
     1                                  .TITLE  MAINDEC-11-DCKBN-A PROG INT RQST LOGIC
                                        .NLIST  MC,MD,SEQ
                                        .LIST   ME
                                        .ABS
                                    ;DCKBNA- TESTS THAT PROGRAM INTERRUPT REQUEST (PIRQ) HARDWARE WORKS PROPERLY.
                                    ;THE PIRQ LOGIC 'BOOKS' AN INTERRUPT AND WHEN THE PRIORITY LEVEL FALLS
                                    ;BELOW THAT OF THE REQUEST THE INTERRUPT IS TAKEN.
                                    ;NOTE: IT IS NOT SPECIFIED AS TO WHETHER OR NOT THE NEXT INSTRUCTION IS
                                    ;EXECUTED IF THE 'BOOKED' REQUEST IS GREATER THAN THAT OF THE PROCESSER.

                                    ;STARTING PROCEEDURE
                                    ;       LOAD ADDRESS=200
                                    ;       PRESS START
                                    ;       STACK POINTER IS AT 500
                                    ;       BELL WILL RING WHEN TEST IS COMPLETE

                                    ;EQUATE STATEMENTS
000000                                      R0=%0
000001                                      R1=%1
000002                                      R2=%2
000003                                      R3=%3
000004                                      R4=%4
000005                                      R5=%5
000006                                      SP=%6
000007                                      PC=%7
                                    ;VECTOR ADDRESSES

000004                                      ERRVEC=4
000010                                      RESVEC=10
000014                                      TBITVEC=14
000020                                      IOTVEC=20
000024                                      PFVEC=24
000030                                      EMTVEC=30
000034                                      TRPVEC=34
000064                                      TPVEC=64            ;TELETYPE PRINTER INTERRUPT VECTOR

                                    ;**********************INITIAL STACK POINTER=500**********************

000500                                      STKPTR=500          ;INITIAL STACK POINTER
010701                                      SCOPE=010701        ;MOVE PC TO R1
000000                                      HLT=HALT            ;ERROR HALT
022626                                      POP2=022626         ;POPS TWO WORD OFF THE STACK
                                    ;RESISTER ADDRESSES
177776                                      PSW=177776          ;ADDRESS OF PROCESSOR STATUS
177770                                      UBREAK=177770       ;ADDRESS OF MICRO BREAK REGISTER
177564                                      TPCSR=177564        ;ADDRESS OF TELEPRINTER CONTROL STATUS
177566                                      TPBUF=177566        ;AND DATA BUFFER REGISTER
177570                                      SWR=177570          ;ADDRESS OF CONSOLE SWITCH REGISTER
177570                                      DISPLAY=177570      ;ADDRESS OF CONSOLE DISPLAY REGISTER
                                    ;PSW BIT ASSIGNMENTS
000000                                      PRTY0=0
000040                                      PRTY1=40
000100                                      PRTY2=100
000140                                      PRTY3=140
```



```
000200                                      PRTY4=200
000240                                      PRTY5=240
000300                                      PRTY6=300
000340                                      PRTY7=340
000340                                      PRTY10=340

                                    ;PIRQ BIT ASSIGNMENTS
000000                                      PIR0=0
001000                                      PIR1=1000
002000                                      PIR2=2000
004000                                      PIR3=4000
010000                                      PIR4=10000
020000                                      PIR5=20000
040000                                      PIR6=40000
100000                                      PIR7=100000
100000                                      PIR10=100000
000000                                      PIA0=0
000042                                      PIA1=42
000104                                      PIA2=104
000146                                      PIA3=146
000210                                      PIA4=210
000252                                      PIA5=252
000314                                      PIA6=314
000356                                      PIA7=356

                                    ;MACRO CALLS
```

```
                000000                  ,#0
000000  000002                          ,+2
000002  000000                          HALT
000004  000006                          ,+2
000006  000000                          HALT
000010  000012                          ,+2
000012  000000                          HALT
000014  000016                          ,+2
000016  000000                          HALT
000020  000022                          ,+2
000022  000000                          HALT
000024  000026                          ,+2
000026  000000                          HALT
000030  000032                          ,+2
000032  000000                          HALT
000034  000036                          ,+2
000036  000000                          HALT
000040  000042                          ,+2
000042  000000                          HALT
000044  000046                          ,+2
000046  000000                          HALT
000050  000052                          ,+2
000052  000000                          HALT
000054  000056                          ,+2
000056  000000                          HALT
000060  000062                          ,+2
000062  000000                          HALT
000064  000066                          ,+2
000066  000000                          HALT
000070  000072                          ,+2
000072  000000                          HALT
000074  000076                          ,+2
000076  000000                          HALT
000100  000102                          ,+2
000102  000000                          HALT
000104  000106                          ,+2
000106  000000                          HALT
000110  000112                          ,+2
000112  000000                          HALT
000114  000116                          ,+2
000116  000000                          HALT
000120  000122                          ,+2
000122  000000                          HALT
000124  000126                          ,+2
000126  000000                          HALT
000130  000132                          ,+2
000132  000000                          HALT
000134  000136                          ,+2
000136  000000                          HALT
000140  000142                          ,+2
000142  000000                          HALT
000144  000146                          ,+2
000146  000000                          HALT
```



```
000150  000152                          ,+2
000152  000000                          HALT
000154  000156                          ,+2
000156  000000                          HALT
000160  000162                          ,+2
000162  000000                          HALT
000164  000166                          ,+2
000166  000000                          HALT
000170  000172                          ,+2
000172  000000                          HALT
000174  000176                          ,+2
000176  000000                          HALT
000200  000202                          ,+2
000202  000000                          HALT
000204  000206                          ,+2
000206  000000                          HALT
000210  000212                          ,+2
000212  000000                          HALT
000214  000216                          ,+2
000216  000000                          HALT
000220  000222                          ,+2
000222  000000                          HALT
000224  000226                          ,+2
000226  000000                          HALT
000230  000232                          ,+2
000232  000000                          HALT
000234  000236                          ,+2
000236  000000                          HALT
000240  000242                          ,+2
000242  000000                          HALT
000244  000246                          ,+2
000246  000000                          HALT
000250  000252                          ,+2
000252  000000                          HALT
000254  000256                          ,+2
000256  000000                          HALT
000260  000262                          ,+2
000262  000000                          HALT
000264  000266                          ,+2
000266  000000                          HALT
000270  000272                          ,+2
000272  000000                          HALT
000274  000276                          ,+2
000276  000000                          HALT
000300  000302                          ,+2
000302  000000                          HALT
000304  000306                          ,+2
000306  000000                          HALT
000310  000312                          ,+2
000312  000000                          HALT
000314  000316                          ,+2
000316  000000                          HALT
000320  000322                          ,+2
000322  000000                          HALT
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000324  000326                          ,+2
000326  000000                          HALT
000330  000332                          ,+2
000332  000000                          HALT
000334  000336                          ,+2
000336  000000                          HALT
000340  000342                          ,+2
000342  000000                          HALT
000344  000346                          ,+2
000346  000000                          HALT
000350  000352                          ,+2
000352  000000                          HALT
000354  000356                          ,+2
000356  000000                          HALT
000360  000362                          ,+2
000362  000000                          HALT
000364  000366                          ,+2
000366  000000                          HALT
000370  000372                          ,+2
000372  000000                          HALT
000374  000376                          ,+2
000376  000000                          HALT

        000200                          ,=200
000200  000167  000606                  JMP     START

        001000                          ,=1000
001000  000000          ICNT:   0                       ;PASS COUNT
001002  177772          PI:     177772                  ;PROGRAM INTERRUPT REQUEST REGISTER
001004  177773          PIH:    177773                  ;HIGH (ODD) BYTE
001006  000240          PIRVEC: 240                     ;PROGRAM INTERRUPT REQUEST INTER-
001010  000242          PIRLVL: 242                     ;RUPT VECTOR AND STATUS
001012  005067  177762  START:  CLR     ICNT            ;CLEAR PASS COUNT
001016  012706  000500          MOV     #STKPTR,SP      ;INITIALIZE THE STACK PTR
001022  012706  000500  BEGIN:  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
001026  012767  000340  176742  MOV     #PRTY7,PSW      ;SET PROCESSER PRIORITY=7
001034  016737  177740  177570  MOV     ICNT,@#DISPLAY  ;DISPLAY PASS COUNT
001042  032737  000400  177570  BIT     #400,@#SWR      ;LOAD MICRO BREAK REGISTER
001050  001403                  BEQ     .+10
001052  113737  177570  177770  MOVB    @#SWR,@#UBREAK  ;LOAD MICRO BREAK REG WITH SR0=7

                                ;TEST THAT PROGRAM INTERRUPT REGISTER (PIRQ) CAN BE ACCESSED
001060  012767  001074  176716  T0:     MOV     #T0A,4          ;LOAD ERROR TRAP VECTOR
001066  005777  177710                  TST     @PI             ;REFERENCE PI
001072  000403                  BR      T0B
001074  022626          T0A:    POP2                    ;POP 2 WORDS OFF THE STACK
001076  000000                  HLT                     ;ERROR CP FAILED TO ACCESS PI
001100  000767                  BR      T0              ;LOOP TEST IF ERROR
001102  012767  000006  176674  T0B:    MOV     #6,4            ;RESTORE ERROR TRAP
001110  000400                  BR      T1              ;GO TO NEXT TEST

                                ;TEST THAT PROGRAM INTERRUPT REGISTER CAN BE LOADED AND CLEARED (T1-T7)

001112  010701          T1:     SCOPE
```



```
001114  012767  000340  176654          MOV     #PRTY7,PSW      ;SET PROCESSER PRIORITY=7
001122  012777  001000  177652          MOV     #PIR1,@PI       ;SET PIR=1
001130  017700  177646                  MOV     @PI,R0          ;GET RESULT
001134  022700  001042                  CMP     #PIR1+PIA1,R0   ;CORRECT RESULT?
001140  001401                          BEQ     T1A
001142  000000                          HLT                     ;INCORRECT RESULT
001144  005077  177632          T1A:    CLR     @PI             ;CLEAR PROGRAM INTERRUPT REGISTER
001150  017700  177626                  MOV     @PI,R0          ;GET RESULTS
001154  001401                          BEQ     T2
001156  000000                          HLT                     ;PIRQ DID NOT CLEAR

001160  010701          T2:     SCOPE
001162  012777  002000  177612          MOV     #PIR2,@PI       ;SET PIR=2
001170  017700  177606                  MOV     @PI,R0          ;GET RESULT
001174  022700  002104                  CMP     #PIR2+PIA2,R0   ;CORRECT RESULT
001200  001401                          BEQ     T2A
001202  000000                          HLT
001204  005077  177572          T2A:    CLR     @PI
001210  017700  177566                  MOV     @PI,R0
001214  001401                          BEQ     T3
001216  000000                          HLT

001220  010701          T3:     SCOPE
001222  012777  004000  177552          MOV     #PIR3,@PI
001230  017700  177546                  MOV     @PI,R0
001234  022700  004146                  CMP     #PIR3+PIA3,R0
001240  001401                          BEQ     T3A
001242  000000                          HLT
001244  005077  177532          T3A:    CLR     @PI
001250  017700  177526                  MOV     @PI,R0
001254  001401                          BEQ     T4

001256  000000                          HLT
```

```
001260  010701                  T4:     SCOPE
001262  012777  010000  177512          MOV     #PIR4,@PI
001270  017700  177506                  MOV     @PI,R0
001274  022700  010210                  CMP     #PIR4+PIA4,R0
001300  001401                          BEQ     T4A
001302  000000                          HLT
001304  005077  177472          T4A:    CLR     @PI
001310  017700  177466                  MOV     @PI,R0
001314  001401                          BEQ     T5

001316  000000                          HLT
001320  010701                  T5:     SCOPE
001322  012777  020000  177452          MOV     #PIR5,@PI
001330  017700  177446                  MOV     @PI,R0
001334  022700  020252                  CMP     #PIR5+PIA5,R0
001340  001401                          BEQ     T5A
001342  000000                          HLT
001344  005077  177432          T5A:    CLR     @PI
001350  017700  177426                  MOV     @PI,R0
001354  001401                          BEQ     T6

001356  000000                          HLT
001360  010701                  T6:     SCOPE
001362  012777  040000  177412          MOV     #PIR6,@PI
001370  017700  177406                  MOV     @PI,R0
001374  022700  040314                  CMP     #PIR6+PIA6,R0
001400  001401                          BEQ     T6A
001402  000000                          HLT
001404  005077  177372          T6A:    CLR     @PI
001410  017700  177366                  MOV     @PI,R0
001414  001401                          BEQ     T7

001416  000000                          HLT
001420  010701                  T7:     SCOPE
001422  012777  100000  177352          MOV     #PIR7,@PI
001430  017700  177346                  MOV     @PI,R0
001434  022700  100356                  CMP     #PIR7+PIA7,R0
001440  001401                          BEQ     T7A
001442  000000                          HLT
001444  005077  177332          T7A:    CLR     @PI
001450  017700  177326                  MOV     @PI,R0
001454  001401                          BEQ     T10
001456  000000                          HLT

                                ;TEST THAT RESET CLEARS PIRQ
001460  010701                  T10:    SCOPE
001462  012777  177777  177312          MOV     #-1,@PI         ;SET ALL PIR BITS IN MSH AND
                                                                ;PIA BITS 0 TO 7 IN LSH
001470  017700  177306                  MOV     @PI,R0          ;GET RESULT
001474  022700  177356                  CMP     #177000+PIA7,R0 ;DID ALL CORRECT BITS SET
001500  001401                          BEQ     T10A
001502  000000                          HLT
001504  000005                  T10A:   RESET                   ;RESET
```



```
001506  017700  177270                  MOV     @PI,R0          ;GET RESULT
001512  001402                          BEQ     T11             ;BRANCH IF 0
001514  000000                          HLT                     ;RESET DID NOT CLEAR ALL BITS
001516  000760                          BR      T10             ;LOOP TEST IF RESET FAILS
```

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                                        ;TEST THAT ODD BYTE OF PIRQ CAN BE REFERENCED,
001520  010701                  T11:    SCOPE
001522  112777  000002  177254          MOVB    #2,@PIH         ;LOAD ODD BYTE
001530  117700  177250                  MOVB    @PIH,R0         ;GET ODD BYTE
001534  122700  000002                  CMPB    #2,R0           ;DID ODD BYTE LOAD CORRECTLY
001540  001401                          BEQ     T11A
001542  000000                          HLT
001544  017700  177232          T11A:   MOV     @PI,R0          ;GET PIRQ
001550  022700  001042                  CMP     #PIR1+PIA1,R0   ;COMPARE WORD
001554  001401                          BEQ     T12
001556  000000                          HLT                     ;WORD FAILED

                                        ;TEST THAT EVEN BYTE BITS CANNOT BE 'PROGRAM' SET,
001560  010701                  T12:    SCOPE
001562  005077  177214                  CLR     @PI             ;CLEAR PIRQ
001566  112777  177777  177206          MOVB    #-1,@PI         ;TRY TO SET EVEN BYTE BITS
001574  017700  177202                  MOV     @PI,R0          ;GET RESULT
001600  001401                          BEQ     T13
001602  000000                          HLT                     ;ERROR! PIRQ GOT LOADED

                                        ;TEST THAT 'PIA' BITS DECODE ONLY THE MOST SIGNIFICANT 'SET' BIT

001604  010701                  T13:    SCOPE
001606  012777  001000  177166          MOV     #PIR1,@PI
001614  017700  177162                  MOV     @PI,R0
001620  022700  001042                  CMP     #PIR1+PIA1,R0
001624  001401                          BEQ     .+4
001626  000000                          HLT

001630  052777  002000  177144          BIS     #PIR2,@PI
001636  017700  177140                  MOV     @PI,R0
001642  022700  003104                  CMP     #PIR1+PIR2+PIA2,R0
001646  001401                          BEQ     .+4
001650  000000                          HLT

001652  052777  004000  177122          BIS     #PIR3,@PI
001660  017700  177116                  MOV     @PI,R0
001664  022700  007146                  CMP     #PIR1+PIR2+PIR3+PIA3,R0
001670  001401                          BEQ     .+4
001672  000000                          HLT

001674  052777  010000  177100          BIS     #PIR4,@PI
001702  017700  177074                  MOV     @PI,R0
001706  022700  017210                  CMP     #PIR1+PIR2+PIR3+PIR4+PIA4,R0
001712  001401                          BEQ     .+4
001714  000000                          HLT

001716  052777  020000  177056          BIS     #PIR5,@PI
001724  017700  177052                  MOV     @PI,R0
001730  022700  037252                  CMP     #PIR1+PIR2+PIR3+PIR4+PIR5+PIA5,R0
001734  001401                          BEQ     .+4
001736  000000                          HLT
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```
001740  052777  040000  177034          BIS     #PIR6,@PI
001746  017700  177030                  MOV     @PI,R0
001752  022700  077314                  CMP     #PIR1+PIR2+PIR3+PIR4+PIR5+PIR6+PIA6,R0
001756  001401                          BEQ     .+4
001760  000000                          HLT
001762  052777  100000  177012          BIS     #PIR7,@PI
001770  017700  177006                  MOV     @PI,R0
001774  022700  177356                  CMP     #PIR1+PIR2+PIR3+PIR4+PIR5+PIR6+PIR7+PIA7,R0
002000  001401                          BEQ     T14
002002  000000                          HLT
```

```
                                ;TEST THAT WHEN PROGRAM INTERRUPT OCCURS THAT IT DOES SO AT THE CORRECT
                                ;VECTOR.  IF THE VECTOR IS INCORRECT PROGRAM WILL HALT AT THE INCORRECT VECTOR
                                ;ADDRESS +2.

002004  010701                  T14:    SCOPE
002006  012777  002042  176772          MOV     #T14A,@PIRVEC   ;LOAD INTERRUPT VECTOR AND
002014  012777  000340  176760          MOV     #PRTY7,@PIRLVL  ;PRIORITY LEVEL
002022  012777  001000  176752          MOV     #PIR1,@PI       ;REQUEST AN INTERRUPT AT LEVEL 1
002030  005067  175742                  CLR     PSW             ;ALLOW INTERRUPTS
002034  000240                          NOP
002036  000000                          HLT                     ;INTERRUPT FAILED
002040  000661                          BR      T13             ;LOOP TEST
002042  000240                  T14A:   NOP                     ;INTERRUPTS TO T14A
002044  022626                          POP2
002046  000005                          RESET                   ;CLEAR PIRQ
002050  012767  000340  175720          MOV     #PRTY7,PSW      ;LOCK OUT INTERRUPTS
                                ;TEST THAT PSW GETS LOADED WITH THE WORD FOLLOWING THE VECTOR ADDRESS
                                ;(VECTOR ADDRESS+2).
002056  010701                  T15:    SCOPE
002060  012777  002114  176720          MOV     #T15A,@PIRVEC
002066  012777  000340  176714          MOV     #PRTY7,@PIRLVL
002074  005067  175676                  CLR     PSW             ;CLEAR PSW
002100  012777  001000  176674          MOV     #PIR1,@PI
002106  000240                          NOP
002110  000000                          HLT                     ;ERROR INTERRUPT FAILED
002112  000412                          BR      T16
002114  022626                  T15A:   POP2
002116  016700  175654                  MOV     PSW,R0
002122  022700  000340                  CMP     #PRTY7,R0
002126  001404                          BEQ     T16
002130  000000                          HLT
002132  012767  000340  175636          MOV     #PRTY7,PSW
                                ;TEST THAN AN INTERRUPT OCCURS IF INSTRUCTION FOLLOWING REQUEST
                                ;LOWERS REQUEST LEVEL BELOW CURRENT PROCESSER STATUS LEVEL.
002140  010701                  T16:    SCOPE
002142  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
002146  005077  176630                  CLR     @PI             ;CLEAR PIRQ
002152  012777  002212  176626          MOV     #T16A,@PIRVEC   ;LOAD INTERRUPT VECTOR
002160  012777  000340  176622          MOV     #PRTY7,@PIRLVL  ;AND STATUS
002166  012767  000200  175602          MOV     #PRTY4,PSW      ;SET PROCESSER STATUS EQUAL TO 4
002174  012777  020000  176600          MOV     #PIR5,@PI       ;REQUEST INTERRUPT AT LEVEL 5
002202  005077  176574                  CLR     @PI             ;DISABLE REQUEST
002206  000000                          HLT                     ;ERROR! PROGRAM DID NOT INTERRUPT
002210  000402                          BR      T17             ;GO TO NEXT TEST
002212  022626                  T16A:   POP2
002214  000400                          BR      T17             ;GO TO NEXT TEST

                                ;TEST THAT IF THE INSTRUCTION FOLLOWING A REQUEST RAISES THE PROCESSER PRIORITY
                                ;ABOVE THAT OF THE REQUEST THAT THE REQUEST STILL INTERRUPTS.
002216  010701                  T17:    SCOPE
002220  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
002224  005077  176552                  CLR     @PI             ;CLEAR PIRQ
002230  012777  002274  176550          MOV     #T17A,@PIRVEC   ;LOAD INTERRUPT VECTOR
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002236  012777  000340  176544          MOV     #PRTY7,@PIRLVL  ;AND STATUS
002244  012767  000100  175524          MOV     #PRTY2,PSW
002252  012777  004000  176522          MOV     #PIR3,@PI
002260  012767  000140  175510          MOV     #PRTY3,PSW
002266  000240                          NOP
002270  000000                          HLT                     ;ERROR! PROG, INT, NOT ACK.
002272  000402                          BR      T20
002274  022626                  T17A:   POP2
002276  000400                          BR      T20

        000020                  C=20
        000021                  D=21
        000001                  N=1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY LEVEL (1) IS EQUAL TO THE PROGRAM
                                ;INTERRUPT REQUEST LEVEL (1) THAT NO INTERRUPT OCCURS.
002300  010701                  T20:    SCOPE
002302  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
002306  005077  176470                  CLR     @PI             ;CLEAR PROGRAM INTERRUPT REQUEST REG.
002312  012777  002346  176466          MOV     #T20A,@PIRVEC   ;LOAD INTERRUPT VECTOR &
002320  012777  000340  176462          MOV     #PRTY7,@PIRLVL  ;STATUS
002326  012767  000040  175442          MOV     #PRTY1,PSW      ;SET PROCESSER STATUS EQUAL TO 1
002334  012777  001000  176440          MOV     #PIR1,@PI       ;REQUEST INTERRUPT AT LEVEL 1
002342  000240                          NOP
002344  000401                          BR      T21             ;GO TO NEXT TEST
002346  000000                  T20A:   HLT                     ;PROGRAM INTERRUPTED,STATUS=REQ-
                                                                ;UEST LEVEL=1.

        000002                          N=N+1
        000021                          C=C+1
        000022                          D=D+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY LEVEL (2) IS EQUAL TO THE PROGRAM
                                ;INTERRUPT REQUEST LEVEL (2) THAT NO INTERRUPT OCCURS.
002350  010701                  T21:    SCOPE
002352  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
002356  005077  176420                  CLR     @PI             ;CLEAR PROGRAM INTERRUPT REQUEST REG.
002362  012777  002416  176416          MOV     #T21A,@PIRVEC   ;LOAD INTERRUPT VECTOR &
002370  012777  000340  176412          MOV     #PRTY7,@PIRLVL  ;STATUS
002376  012767  000100  175372          MOV     #PRTY2,PSW      ;SET PROCESSER STATUS EQUAL TO 2
002404  012777  002000  176370          MOV     #PIR2,@PI       ;REQUEST INTERRUPT AT LEVEL 2
002412  000240                          NOP
002414  000401                          BR      T22             ;GO TO NEXT TEST
002416  000000                  T21A:   HLT                     ;PROGRAM INTERRUPTED,STATUS=REQ-
                                                                ;UEST LEVEL=2.

        000003                          N=N+1
        000022                          C=C+1
        000023                          D=D+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY LEVEL (3) IS EQUAL TO THE PROGRAM
                                ;INTERRUPT REQUEST LEVEL (3) THAT NO INTERRUPT OCCURS.
002420  010701                  T22:    SCOPE
002422  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
002426  005077  176350                  CLR     @PI             ;CLEAR PROGRAM INTERRUPT REQUEST REG.
002432  012777  002466  176346          MOV     #T22A,@PIRVEC   ;LOAD INTERRUPT VECTOR &
002440  012777  000340  176342          MOV     #PRTY7,@PIRLVL  ;STATUS
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002446  012767  000140  175322          MOV     #PRTY3,PSW      ;SET PROCESSER STATUS EQUAL TO 3
002454  012777  004000  176320          MOV     #PIR3,@PI       ;REQUEST INTERRUPT AT LEVEL 3
002462  000240                          NOP
002464  000401                          BR      T23             ;GO TO NEXT TEST
002466  000000                  T22A1:  HLT                     ;PROGRAM INTERRUPTED,STATUS=REQ-
                                                                ;UEST LEVEL=3,

        000004                          N=N+1
        000023                          C=C+1
        000024                          D=D+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY LEVEL (4) IS EQUAL TO THE PROGRAM
                                ;INTERRUPT REQUEST LEVEL (4) THAT NO INTERRUPT OCCURS,
002470  010701                  T23:    SCOPE
002472  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
002476  005077  176300                  CLR     @PI             ;CLEAR PROGRAM INTERRUPT REQUEST REG,
002502  012777  002536  176276          MOV     #T23A,@PIRVEC   ;LOAD INTERRUPT VECTOR &
002510  012777  000340  176272          MOV     #PRTY7,@PIRLVL  ;STATUS
002516  012767  000200  175252          MOV     #PRTY4,PSW      ;SET PROCESSER STATUS EQUAL TO 4
002524  012777  010000  176250          MOV     #PIR4,@PI       ;REQUEST INTERRUPT AT LEVEL 4
002532  000240                          NOP
002534  000401                          BR      T24             ;GO TO NEXT TEST
002536  000000                  T23A1:  HLT                     ;PROGRAM INTERRUPTED,STATUS=REQ-
                                                                ;UEST LEVEL=4,

        000005                          N=N+1
        000024                          C=C+1
        000025                          D=D+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY LEVEL (5) IS EQUAL TO THE PROGRAM
                                ;INTERRUPT REQUEST LEVEL (5) THAT NO INTERRUPT OCCURS,
002540  010701                  T24:    SCOPE
002542  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
002546  005077  176230                  CLR     @PI             ;CLEAR PROGRAM INTERRUPT REQUEST REG,
002552  012777  002606  176226          MOV     #T24A,@PIRVEC   ;LOAD INTERRUPT VECTOR &
002560  012777  000340  176222          MOV     #PRTY7,@PIRLVL  ;STATUS
002566  012767  000240  175202          MOV     #PRTY5,PSW      ;SET PROCESSER STATUS EQUAL TO 5
002574  012777  020000  176200          MOV     #PIR5,@PI       ;REQUEST INTERRUPT AT LEVEL 5
002602  000240                          NOP
002604  000401                          BR      T25             ;GO TO NEXT TEST
002606  000000                  T24A1:  HLT                     ;PROGRAM INTERRUPTED,STATUS=REQ-
                                                                ;UEST LEVEL=5,

        000006                          N=N+1
        000025                          C=C+1
        000026                          D=D+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY LEVEL (6) IS EQUAL TO THE PROGRAM
                                ;INTERRUPT REQUEST LEVEL (6) THAT NO INTERRUPT OCCURS,
002610  010701                  T25:    SCOPE
002612  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
002616  005077  176160                  CLR     @PI             ;CLEAR PROGRAM INTERRUPT REQUEST REG,
002622  012777  002656  176156          MOV     #T25A,@PIRVEC   ;LOAD INTERRUPT VECTOR &
002630  012777  000340  176152          MOV     #PRTY7,@PIRLVL  ;STATUS
002636  012767  000300  175132          MOV     #PRTY6,PSW      ;SET PROCESSER STATUS EQUAL TO 6
002644  012777  040000  176130          MOV     #PIR6,@PI       ;REQUEST INTERRUPT AT LEVEL 6
002652  000240                          NOP
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002654  000401                          BR      T26             ;GO TO NEXT TEST
002656  000000                  T25A1:  HLT                     ;PROGRAM INTERRUPTED,STATUS=REQ-
                                                                ;UEST LEVEL=6,

        000007                          N=N+1
        000026                          C=C+1
        000027                          D=D+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY LEVEL (7) IS EQUAL TO THE PROGRAM
                                ;INTERRUPT REQUEST LEVEL (7) THAT NO INTERRUPT OCCURS,
002660  010701                  T26:    SCOPE
002662  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
002666  005077  176110                  CLR     @PI             ;CLEAR PROGRAM INTERRUPT REQUEST REG,
002672  012777  002726  176106          MOV     #T26A,@PIRVEC   ;LOAD INTERRUPT VECTOR &
002700  012777  000340  176102          MOV     #PRTY7,@PIRLVL  ;STATUS
002706  012767  000340  175062          MOV     #PRTY7,PSW      ;SET PROCESSER STATUS EQUAL TO 7
002714  012777  100000  176060          MOV     #PIR7,@PI       ;REQUEST INTERRUPT AT LEVEL 7
002722  000240                          NOP
002724  000401                          BR      T27             ;GO TO NEXT TEST
002726  000000                  T26A1:  HLT                     ;PROGRAM INTERRUPTED,STATUS=REQ-
                                                                ;UEST LEVEL=7,

        000010                          N=N+1
        000027                          C=C+1
        000030                          D=D+1
        000001                  N=1
        000000                  M=0
                                ;TEST THAT WHEN THE PROCESSER PRIORITY (1) IS GREATER THAN THE PROGRAM INT=
                                ;ERRUPT REQUEST LEVEL (0) THAT NO INTERRUPT OCCURS,
002730  010701                  T27:    SCOPE
002732  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
002736  005077  176040                  CLR     @PI             ;CLEAR PIRQ
002742  012777  002776  176036          MOV     #T27A,@PIRVEC)  ;LOAD INTERRUPT VECTOR
002750  012777  000340  176032          MOV     #PRTY7,@PIRLVL  ;AND STATUS
002756  012767  000040  175012          MOV     #PRTY1,PSW      ;SET PROCESSER STATUS EQUAL TO 1
002764  012777  000000  176010          MOV     #PIR0,@PI       ;REQUEST INTERRUPT AT LEVEL 0
002772  000240                          NOP
002774  000401                          BR      T30             ;GO TO NEXT TEST
002776  000000                  T27A1:  HLT                     ;ERROR PROGRAM INTERRUPTED WHEN
                                                                ;STATUS=1, REQUEST LEVEL=0

        000030                          C=C+1
        000031                          D=D+1
        000001                          M=M+1
        000002                          N=N+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY (2) IS GREATER THAN THE PROGRAM INT=
                                ;ERRUPT REQUEST LEVEL (1) THAT NO INTERRUPT OCCURS,
003000  010701                  T30:    SCOPE
003002  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003006  005077  175770                  CLR     @PI             ;CLEAR PIRQ
003012  012777  003046  175766          MOV     #T30A,@PIRVEC)  ;LOAD INTERRUPT VECTOR
003020  012777  000340  175762          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003026  012767  000100  174742          MOV     #PRTY2,PSW      ;SET PROCESSER STATUS EQUAL TO 2
003034  012777  001000  175740          MOV     #PIR1,@PI       ;REQUEST INTERRUPT AT LEVEL 1
003042  000240                          NOP
```

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003044  000401                          BR      T31             ;GO TO NEXT TEST
003046  000000                  T30A1:  HLT                     ;ERROR PROGRAM INTERRUPTED WHEN
                                                                ;STATUS=2, REQUEST LEVEL=1

                000031                  C=C+1
                000032                  D=D+1
                000002                  M=M+1
                000003                  N=N+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY (3) IS GREATER THAN THE PROGRAM INT-
                                ;ERRUPT REQUEST LEVEL (2) THAT NO INTERRUPT OCCURS.
003050  010701                  T31:    SCOPE
003052  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003056  005077  175720                  CLR     @PI             ;CLEAR PIRQ
003062  012777  003116  175716          MOV     #T31A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003070  012777  000340  175712          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003076  012767  000140  174672          MOV     #PRTY3,PSW      ;SET PROCESSER STATUS EQUAL TO 3
003104  012777  002000  175670          MOV     #PIR2,@PI       ;REQUEST INTERRUPT AT LEVEL 2
003112  000240                          NOP
003114  000401                          BR      T32             ;GO TO NEXT TEST
003116  000000                  T31A1:  HLT                     ;ERROR PROGRAM INTERRUPTED WHEN
                                                                ;STATUS=3, REQUEST LEVEL=2

                000032                  C=C+1
                000033                  D=D+1
                000003                  M=M+1
                000004                  N=N+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY (4) IS GREATER THAN THE PROGRAM INT-
                                ;ERRUPT REQUEST LEVEL (3) THAT NO INTERRUPT OCCURS.
003120  010701                  T32:    SCOPE
003122  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003126  005077  175650                  CLR     @PI             ;CLEAR PIRQ
003132  012777  003166  175646          MOV     #T32A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003140  012777  000340  175642          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003146  012767  000200  174622          MOV     #PRTY4,PSW      ;SET PROCESSER STATUS EQUAL TO 4
003154  012777  004000  175620          MOV     #PIR3,@PI       ;REQUEST INTERRUPT AT LEVEL 3
003162  000240                          NOP
003164  000401                          BR      T33             ;GO TO NEXT TEST
003166  000000                  T32A1:  HLT                     ;ERROR PROGRAM INTERRUPTED WHEN
                                                                ;STATUS=4, REQUEST LEVEL=3

                000033                  C=C+1
                000034                  D=D+1
                000004                  M=M+1
                000005                  N=N+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY (5) IS GREATER THAN THE PROGRAM INT-
                                ;ERRUPT REQUEST LEVEL (4) THAT NO INTERRUPT OCCURS.
003170  010701                  T33:    SCOPE
003172  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003176  005077  175600                  CLR     @PI             ;CLEAR PIRQ
003202  012777  003236  175576          MOV     #T33A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003210  012777  000340  175572          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003216  012767  000240  174552          MOV     #PRTY5,PSW      ;SET PROCESSER STATUS EQUAL TO 5
003224  012777  010000  175550          MOV     #PIR4,@PI       ;REQUEST INTERRUPT AT LEVEL 4
003232  000240                          NOP
```



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003234  000401                          BR      T34             ;GO TO NEXT TEST
003236  000000                  T33A1:  HLT                     ;ERROR PROGRAM INTERRUPTED WHEN
                                                                ;STATUS=5, REQUEST LEVEL=4

                000034                  C=C+1
                000035                  D=D+1
                000005                  M=M+1
                000006                  N=N+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY (6) IS GREATER THAN THE PROGRAM INT-
                                ;ERRUPT REQUEST LEVEL (5) THAT NO INTERRUPT OCCURS.
003240  010701                  T34:    SCOPE
003242  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003246  005077  175530                  CLR     @PI             ;CLEAR PIRQ
003252  012777  003306  175526          MOV     #T34A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003260  012777  000340  175522          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003266  012767  000300  174502          MOV     #PRTY6,PSW      ;SET PROCESSER STATUS EQUAL TO 6
003274  012777  020000  175500          MOV     #PIR5,@PI       ;REQUEST INTERRUPT AT LEVEL 5
003302  000240                          NOP
003304  000401                          BR      T35             ;GO TO NEXT TEST
003306  000000                  T34A1:  HLT                     ;ERROR PROGRAM INTERRUPTED WHEN
                                                                ;STATUS=6, REQUEST LEVEL=5

                000035                  C=C+1
                000036                  D=D+1
                000006                  M=M+1
                000007                  N=N+1
                                ;TEST THAT WHEN THE PROCESSER PRIORITY (7) IS GREATER THAN THE PROGRAM INT-
                                ;ERRUPT REQUEST LEVEL (6) THAT NO INTERRUPT OCCURS.
003310  010701                  T35:    SCOPE
003312  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003316  005077  175460                  CLR     @PI             ;CLEAR PIRQ
003322  012777  003356  175456          MOV     #T35A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003330  012777  000340  175452          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003336  012767  000340  174432          MOV     #PRTY7,PSW      ;SET PROCESSER STATUS EQUAL TO 7
003344  012777  040000  175430          MOV     #PIR6,@PI       ;REQUEST INTERRUPT AT LEVEL 6
003352  000240                          NOP
003354  000401                          BR      T36             ;GO TO NEXT TEST
003356  000000                  T35A1:  HLT                     ;ERROR PROGRAM INTERRUPTED WHEN
                                                                ;STATUS=7, REQUEST LEVEL=6

                000036                  C=C+1
                000037                  D=D+1
                000007                  M=M+1
                000010                  N=N+1
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                000000                  N=0
                000001                  M=1
                                        ;TEST THAT WHEN THE PROCESSER PRIORITY (0) IS LESS THAN THE PROGRAM INT-
                                        ;ERRUPT REQUEST LEVEL(1) THAT AN INTERRUPT OCCURS,
003360  010701                  T36:    SCOPE
003362  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003366  005077  175410                  CLR     @PI             ;CLEAR PIRQ
003372  012777  003426  175406          MOV     #T36A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003400  012777  000340  175402          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003406  012767  000000  174362          MOV     #PRTY0,PSW      ;SET PROCESSER STATUS=0
003414  012777  001000  175360          MOV     #PIR1,@PI       ;REQUEST INTERRUPT AT LEVEL1
003422  000240                          NOP
003424  000000                          HLT                     ;ERROR! PROGRAM FAILED TO INTERRUPT
003426  000400                  T36A:   BR      T37             ;GO TO NEXT TEST

                000001                  N=N+1
                000002                  M=M+1
                000037                  C=C+1
                000040                  D=D+1
                                        ;TEST THAT WHEN THE PROCESSER PRIORITY (1) IS LESS THAN THE PROGRAM INT-
                                        ;ERRUPT REQUEST LEVEL(2) THAT AN INTERRUPT OCCURS,
003430  010701                  T37:    SCOPE
003432  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003436  005077  175340                  CLR     @PI             ;CLEAR PIRQ
003442  012777  003476  175336          MOV     #T37A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003450  012777  000340  175332          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003456  012767  000040  174312          MOV     #PRTY1,PSW      ;SET PROCESSER STATUS=1
003464  012777  002000  175310          MOV     #PIR2,@PI       ;REQUEST INTERRUPT AT LEVEL2
003472  000240                          NOP
003474  000000                          HLT                     ;ERROR! PROGRAM FAILED TO INTERRUPT
003476  000400                  T37A:   BR      T40             ;GO TO NEXT TEST

                000002                  N=N+1
                000003                  M=M+1
                000040                  C=C+1
                000041                  D=D+1
                                        ;TEST THAT WHEN THE PROCESSER PRIORITY (2) IS LESS THAN THE PROGRAM INT-
                                        ;ERRUPT REQUEST LEVEL(3) THAT AN INTERRUPT OCCURS,
003500  010701                  T40:    SCOPE
003502  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003506  005077  175270                  CLR     @PI             ;CLEAR PIRQ
003512  012777  003546  175266          MOV     #T40A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003520  012777  000340  175262          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003526  012767  000100  174242          MOV     #PRTY2,PSW      ;SET PROCESSER STATUS=2
003534  012777  004000  175240          MOV     #PIR3,@PI       ;REQUEST INTERRUPT AT LEVEL3
003542  000240                          NOP
003544  000000                          HLT                     ;ERROR! PROGRAM FAILED TO INTERRUPT
003546  000400                  T40A:   BR      T41             ;GO TO NEXT TEST

                000003                  N=N+1
                000004                  M=M+1
                000041                  C=C+1
                000042                  D=D+1
                                        ;TEST THAT WHEN THE PROCESSER PRIORITY (3) IS LESS THAN THE PROGRAM INT-
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                                        ;ERRUPT REQUEST LEVEL(4) THAT AN INTERRUPT OCCURS,
003550  010701                  T41:    SCOPE
003552  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003556  005077  175220                  CLR     @PI             ;CLEAR PIRQ
003562  012777  003616  175216          MOV     #T41A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003570  012777  000340  175212          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003576  012767  000140  174172          MOV     #PRTY3,PSW      ;SET PROCESSER STATUS=3
003604  012777  010000  175170          MOV     #PIR4,@PI       ;REQUEST INTERRUPT AT LEVEL4
003612  000240                          NOP
003614  000000                          HLT                     ;ERROR! PROGRAM FAILED TO INTERRUPT
003616  000400                  T41A:   BR      T42             ;GO TO NEXT TEST

                000004                  N=N+1
                000005                  M=M+1
                000042                  C=C+1
                000043                  D=D+1
                                        ;TEST THAT WHEN THE PROCESSER PRIORITY (4) IS LESS THAN THE PROGRAM INT-
                                        ;ERRUPT REQUEST LEVEL(5) THAT AN INTERRUPT OCCURS,
003620  010701                  T42:    SCOPE
003622  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003626  005077  175150                  CLR     @PI             ;CLEAR PIRQ
003632  012777  003666  175146          MOV     #T42A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003640  012777  000340  175142          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003646  012767  000200  174122          MOV     #PRTY4,PSW      ;SET PROCESSER STATUS=4
003654  012777  020000  175120          MOV     #PIR5,@PI       ;REQUEST INTERRUPT AT LEVEL5
003662  000240                          NOP
003664  000000                          HLT                     ;ERROR! PROGRAM FAILED TO INTERRUPT
003666  000400                  T42A:   BR      T43             ;GO TO NEXT TEST

                000005                  N=N+1
                000006                  M=M+1
                000043                  C=C+1
                000044                  D=D+1
                                        ;TEST THAT WHEN THE PROCESSER PRIORITY (5) IS LESS THAN THE PROGRAM INT-
                                        ;ERRUPT REQUEST LEVEL(6) THAT AN INTERRUPT OCCURS,
003670  010701                  T43:    SCOPE
003672  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
003676  005077  175100                  CLR     @PI             ;CLEAR PIRQ
003702  012777  003736  175076          MOV     #T43A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003710  012777  000340  175072          MOV     #PRTY7,@PIRLVL  ;AND STATUS
003716  012767  000240  174052          MOV     #PRTY5,PSW      ;SET PROCESSER STATUS=5
003724  012777  040000  175050          MOV     #PIR6,@PI       ;REQUEST INTERRUPT AT LEVEL6
003732  000240                          NOP
003734  000000                          HLT                     ;ERROR! PROGRAM FAILED TO INTERRUPT
003736  000400                  T43A:   BR      T44             ;GO TO NEXT TEST

                000006                  N=N+1
                000007                  M=M+1
                000044                  C=C+1
                000045                  D=D+1
                                        ;TEST THAT WHEN THE PROCESSER PRIORITY (6) IS LESS THAN THE PROGRAM INT-
                                        ;ERRUPT REQUEST LEVEL(7) THAT AN INTERRUPT OCCURS,
003740  010701                  T44:    SCOPE
003742  012706  000500                  MOV     #STKPTR,SP      ;INITIALIZE THE STACK POINTER
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003746  005077  175030          CLR     @PI             ;CLEAR PIRQ
003752  012777  004006  175026  MOV     #T44A,@PIRVEC   ;LOAD INTERRUPT VECTOR
003760  012777  000340  175022  MOV     #PRTY7,@PIRLVL  ;AND STATUS
003766  012767  000300  174002  MOV     #PRTY6,PSW      ;SET PROCESSER STATUS=6
003774  012777  100000  175000  MOV     #PIR7,@PI       ;REQUEST INTERRUPT AT LEVEL7
004002  000240                  NOP
004004  000000                  HLT                     ;ERROR! PROGRAM FAILED TO INTERRUPT
004006  000400          T44A:   BR      T45             ;GO TO NEXT TEST

        000007                  N=N+1
        000010                  M=M+1
        000045                  C=C+1
        000046                  D=D+1

                        ;TEST THAT PIRQ REQUESTS AN INTERRUPT AT EACH LEVEL AS THE REQUEST LEVEL
                        ;IS DECREASED,
004010  012706  000500  T45:    MOV     #STKPTR,SP      ;INITIALIZE STACK POINTER
004014  005000                  CLR     %0
004016  012767  000340  173752  MOV     #PRTY7,PSW      ;LOCK OUT INTERRUPTS
004024  012777  177777  174750  MOV     #-1,@PI         ;REQUEST AN INTERRUPT AT ALL LEVELS
004032  012777  004056  174746  MOV     #LEVEL7,@PIRVEC ;LOAD INT' RQST, VECTOR
004040  012777  000340  174742  MOV     #PRTY7,@PIRLVL  ;AND (NEW) STATUS
004046  005067  173724          CLR     PSW             ;ALLOW INTERRUPTS AT ALL LEVELS
004052  000000                  HLT                     ;ERROR! NO INTERRUPT
004054  000566                  BR      T45EX           ;EXIT TEST

004056  012700  100000  LEVEL7: MOV     #PIR7,%0        ;SET INDICATOR BIT IN R0
004062  022777  177356  174712  CMP     #PIR7+PIR6+PIR5+PIR4+PIR3+PIR2+PIR1+PIA7,@PI
004070  001401                  BEQ     .+4             ;IS PIRQ CORRECT?
004072  000000                  HLT                     ;INCORRECT PIRQ
004074  042777  100000  174700  BIC     #PIR7,@PI       ;DELETE REQUEST AT LEVEL 7
004102  012777  004120  174676  MOV     #LEVEL6,@PIRVEC ;SET UP FOR LEVEL 6 REQUEST
004110  022626                  POP2                    ;RESTORE THE STACK
004112  005067  173660          CLR     PSW             ;ALLOW INTERRUPTS
004116  000000                  HLT                     ;ERROR! NO INTERRUPT
004120  052700  040000  LEVEL6: BIS     #PIR6,%0        ;SET INDICATOR BIT
004124  022777  077314  174650  CMP     #PIR6+PIR5+PIR4+PIR3+PIR2+PIR1+PIA6,@PI
004132  001401                  BEQ     .+4             ;IS PIRQ CORRECT?
004134  000000                  HLT                     ;ERROR! INCORRECT PIRQ
004136  042777  040000  174636  BIC     #PIR6,@PI       ;DELETE LEVEL 6 REQUEST
004144  012777  004162  174634  MOV     #LEVEL5,@PIRVEC ;SET UP FOR LEVEL 5 REQUEST
004152  022626                  POP2                    ;RESTORE THE STACK
004154  005067  173616          CLR     PSW             ;ALLOW INTERRUPTS
004160  000000                  HLT                     ;ERROR! NO INTERRUPT

004162  052700  020000  LEVEL5: BIS     #PIR5,%0        ;SET INDICATOR BIT
004166  022777  037252  174606  CMP     #PIR5+PIR4+PIR3+PIR2+PIR1+PIA5,@PI
004174  001401                  BEQ     .+4             ;IS PIRQ CORRECT
004176  000000                  HLT                     ;ERROR! INCORRECT PIRQ
004200  042777  020000  174574  BIC     #PIR5,@PI       ;DELETE LEVEL 5 REQUEST
004206  012777  004224  174572  MOV     #LEVEL4,@PIRVEC ;SET UP FOR LEVEL 4 REQUEST
004214  022626                  POP2                    ;RESTORE THE STACK
004216  005067  173554          CLR     PSW             ;ALLOW INTERRUPTS
004222  000000                  HLT                     ;ERROR! NO INTERRUPT
```



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004224  052700  010000  LEVEL4: BIS     #PIR4,%0        ;SET INDICATOR BIT
004230  022777  017210  174544          CMP     #PIR4+PIR3+PIR2+PIR1+PIA4,@PI
004236  001401                  BEQ     .+4             ;IS PIRQ CORRECT?
004240  000000                  HLT                     ;ERROR! INCORRECT PIRQ
004242  042777  010000  174532          BIC     #PIR4,@PI       ;DELETE LEVEL 4 REQUEST
004250  012777  004266  174530          MOV     #LEVEL3,@PIRVEC ;SET UP FOR LEVEL 3 REQUEST
004256  022626                  POP2                    ;RESTORE THE STACK
004260  005067  173512          CLR     PSW             ;ALLOW INTERRUPTS
004264  000000                  HLT                     ;ERROR! NO INTERRUPT

004266  052700  004000  LEVEL3: BIS     #PIR3,%0        ;SET INDICATOR BIT
004272  022777  007146  174502          CMP     #PIR3+PIR2+PIR1+PIA3,@PI
004300  001401                  BEQ     .+4             ;IS PIRQ CORRECT?
004302  000000                  HLT                     ;ERROR! INCORRECT PIRQ
004304  042777  004000  174470          BIC     #PIR3,@PI       ;DELETE LEVEL 3 REQUEST
004312  012777  004330  174466          MOV     #LEVEL2,@PIRVEC ;SET UP FOR LEVEL 2 REQUEST
004320  022626                  POP2                    ;RESTORE THE STACK
004322  005067  173450          CLR     PSW             ;ALLOW INTERRUPTS
004326  000000                  HLT                     ;ERROR! NO INTERRUPT

004330  052700  002000  LEVEL2: BIS     #PIR2,%0        ;SET INDICATOR BIT
004334  022777  003104  174440          CMP     #PIR2+PIR1+PIA2,@PI
004342  001401                  BEQ     .+4             ;IS PIRQ CORRECT?
004344  000000                  HLT                     ;ERROR! INCORRECT PIRQ
004346  042777  002000  174426          BIC     #PIR2,@PI       ;DELETE LEVEL 2 REQUEST
004354  012777  004372  174424          MOV     #LEVEL1,@PIRVEC ;SET UP FOR LEVEL 1 REQUEST
004362  022626                  POP2                    ;RESTORE THE STACK
004364  005067  173406          CLR     PSW             ;ALLOW INTERRUPTS
004370  000000                  HLT                     ;ERROR! NO INTERRUPT

004372  052700  001000  LEVEL1: BIS     #PIR1,%0        ;SET INDICATOR BIT
004376  022777  001042  174376          CMP     #PIR1+PIA1,@PI
004404  001401                  BEQ     .+4             ;IS PIRQ CORRECT?
004406  000000                  HLT                     ;ERROR! INCORRECT PIRQ
004410  022626                  POP2                    ;RESTORE THE STACK
004412  005077  174364          CLR     @PI             ;CLEAR PROGRAM INT'RQST'REG.
004416  005067  173354          CLR     PSW
004422  022700  177000          CMP     #177000,%0      ;WERE ALL LEVELS SERVICED
004426  001401                  BEQ     .+4
004430  000000                  HLT                     ;ERROR! A LEVEL(S) NOT SERVICED
                                                        ;MISSINGBIT(S) GIVE LEVEL MISSED

004432  000240          T45EX:  NOP
                        ;CHECK THAT PROGRAM INTERRUPT REQUEST TAKE PRECEDENCE
                        ;OVER BUS INTERRUPT (TTY)

004434  010701          T46:    SCOPE
004436  012706  000500          MOV     #STKPTR,%6      ;SET STACK PTR
004442  000237                  SPL     7               ;SET PRIORITY LEVEL 7
004444  012777  004520  174334          MOV     #T46A,@PIRVEC   ;LOAD PIRQ INT VECTOR
004452  012777  000280  174330          MOV     #PRTY4,@PIRLVL  ;ASSUME PRIORITY LEVEL 4 ON INTERRUPT
004460  012737  004522  000064          MOV     #T46B,@#TPVEC   ;LOAD TTY PRINTER INTERRUPT
004466  012737  000200  000066          MOV     #PRTY4,@#TPVEC+2
004474  012737  000100  177564          MOV     #100,@#TPCSR    ;SET IE BIT
```

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004502  012777  010000  174272          MOV     #PIR4,@PI       ;REQUEST INTERRUPT AT LEVEL 4
004510  005037  177776                  CLR     @#PSW           ;ALLOW PIRQ INTERRUPT
004514  000240                          NOP
004516  000000                          HLT                     ;ERROR:NO INTERRUPT
004520  000401                  T46A:   BR      .+4             ;BRANCH OVER HALT WHEN PIRQ INTERRUPTS
004522  000000                  T46B:   HLT                     ;ERROR: TTY INTERRUPTED
004524  005077  174252                  CLR     @PI
004530  005037  177564                  CLR     @#TPCSR
004534  012737  000066  000064          MOV     #TPVEC+2,@#TPVEC

004542  010701                  T47:    SCOPE
004544  000237                          SPL     7               ;SET PRIORITY LEVEL =7
004546  012706  000500                  MOV     #STKPTR,X6      ;SET STACK PTR
004552  012737  004612  000030          MOV     #T47A,@#EMTVEC  ;LOAD EMT TRAP VECTOR
004560  005037  000032                  CLR     @#EMTVEC+2      ;ASSUME PRIORITY LEVEL 0 AFTER EMT
004564  012777  004614  174214          MOV     #T47B,@PIRVEC   ;LOAD PIRQ INTERRUPT VECTOR
004572  012777  000340  174210          MOV     #PRTY7,@PIRLVL  ;ASSUME PRIORITY LEVEL 7 AFTER INT
004600  012777  010000  174174          MOV     #PIR4,@PI       ;BOOK INTERRUPT RQST AT LEVEL 4
004606  104000                          EMT                     ;TRAP ASUME LEVEL 0 AFTER TRAP
004610  000000                          HLT                     ;ERROR: FAILED TO TRAP
004612  000000                  T47A:   HLT                     ;ERROR: PIRQ INT. FAILED AFTER EMT
004614  022726  004612          T47B:   CMP     #T47A,(6)+      ;CHECK RETURN PC ON THE STACK
004620  001401                          BEQ     .+4
004622  000000                          HLT                     ;ERROR: INCORRECT PC ON THE STACK
004624  005726                          TST     (6)+            ;CHECK STATUS ON STACK
004626  001401                          BEQ     .+4
004630  000000                          HLT                     ;ERROR: INCORRECT STATUS ON STACK
004632  005077  174144                  CLR     @PI             ;CLEAR INTERRUPT REQUEST
004636  016777  174146  174142          MOV     PIRLVL,@PIRVEC  ;RESTORE INT VECTOR
004644  005077  174140                  CLR     @PIRLVL
004650  012737  000032  000030          MOV     #EMTVEC+2,@#EMTVEC
004656  010701                          SCOPE

004660  005267  174114          END:    INC     ICNT            ;INCREMENT THE PASS COUNTER
004664  026727  174110  001000          CMP     ICNT,#1000
004672  001402                          BEQ     DONE
004674  000167  174122                  JMP     BEGIN           ;RESTART THE TEST
004700  012767  000007  172660  DONE:   MOV     #7,TPBUF        ;RING THE BELL
004706  105767  172652                  TSTB    TPCSR           ;WAIT FOR BELL TO
004712  100375                          BPL     .-4             ;RING
004714  013702  000042                  MOV     @#42,X2         ;GET DECTAPE MONITOR RETURN ADDRESS
004720  001404                          BEQ     DONE1           ;DO NOT RETURN IF (42)=0
004722  004712                          JSR     7,(2)           ;RETURN TO DECTAPE MONITOR
004724  000240                          NOP                     ;ACT11
004726  000240                          NOP                     ;OVERLAY
004730  000240                          NOP                     ;AREA
004732  000167  174054          DONE1:  JMP     START
        000001                          ,END
```



```
BEGIN   001022          C       = 000045        D       = 000046        DISPLA = 177570
DONE    004700          DONE1     004732        EMTVEC  = 000030        END     004660
ERRVEC  = 000004        HLT     = 000000        ICNT      001000        IOTVEC  = 000020
LEVEL1    004372        LEVEL2    004330        LEVEL3    004266        LEVEL4    004224
LEVEL5    004162        LEVEL6    004120        LEVEL7    004056        M       = 000010
N       = 000007        PC      =%000007        PFVEC   = 000024        PI        001002
PIA0    = 000000        PIA1    = 000042        PIA2    = 000104        PIA3    = 000146
PIA4    = 000210        PIA5    = 000252        PIA6    = 000314        PIA7    = 000356
PIH       001004        PIRLVL    001010        PIRVEC    001006        PIR0    = 000000
PIR1    = 001000        PIR10   = 100000        PIR2    = 002000        PIR3    = 004000
PIR4    = 010000        PIR5    = 020000        PIR6    = 040000        PIR7    = 100000
POP2    = 022626        PRTY0   = 000000        PRTY1   = 000040        PRTY10  = 000340
PRTY2   = 000100        PRTY3   = 000140        PRTY4   = 000200        PRTY5   = 000240
PRTY6   = 000300        PRTY7   = 000340        PSW     = 177776        RESVEC  = 000010
R0      =%000000        R1      =%000001        R2      =%000002        R3      =%000003
R4      =%000004        R5      =%000005        SCOPE   = 010701        SP      =%000006
START     001012        STKPTR  = 000500        SWR     = 177570        TBITVE  = 000014
TPBUF   = 177566        TPCSR   = 177564        TPVEC   = 000064        TRPVEC  = 000034
T0        001060        T0A       001074        T0B       001102        T1        001112
T1A       001144        T10       001466        T10A      001504        T11       001520
T11A      001544        T12       001560        T13       001604        T14       002004
T14A      002042        T15       002056        T15A      002114        T16       002140
T16A      002212        T17       002216        T17A      002274        T2        001160
T2A       001204        T20       002300        T20A      002346        T21       002350
T21A      002416        T22       002420        T22A      002466        T23       002470
T23A      002536        T24       002540        T24A      002606        T25       002610
T25A      002656        T26       002660        T26A      002726        T27       002730
T27A      002776        T3        001220        T3A       001244        T30       003000
T30A      003046        T31       003050        T31A      003116        T32       003120
T32A      003166        T33       003170        T33A      003236        T34       003240
T34A      003306        T35       003310        T35A      003356        T36       003360
T36A      003426        T37       003430        T37A      003476        T4        001260
T4A       001304        T40       003500        T40A      003546        T41       003550
T41A      003616        T42       003620        T42A      003666        T43       003670
T43A      003736        T44       003740        T44A      004006        T45       004010
T45EX     004432        T46       004434        T46A      004520        T46B      004522
T47       004542        T47A      004612        T47B      004614        T5        001320
T5A       001344        T6        001360        T6A       001404        T7        001420
T7A       001444        UBREAK  = 177770        .       = 004736

 ERRORS DETECTED:  0
```