```
                .REM    %
```

IDENTIFICATION

PRODUCT CODE:	AC-F639A-MC
PRODUCT NAME:	CKKFAA0 ROM DIAG(11/44 UBI)
DATE CREATED:	OCT 1979
MAINTAINER:	DIAGNOSTIC ENGINEERING
AUTHOR:	JOHN W. CIUKAJ

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47
48                          HISTORY SECTION
49                          ---------------
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51
52                          (K.KFAAO WAS RELEASED OCT 1979
53
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BOOT ROM DIAGNOSTIC- 11/44

1. OVERVIEW

THE 11/44 BOOT DIAGNOSTIC ROM IS DESIGNED TO PROVIDE DIAGNOSTIC ROUTINES FOR SOME BASIC CPU,CACHE, & MEMORY GO-NO-GO TESTS.

IT MAY BE IMPLEMENTED IN THE FOLLOWING MANNER:

1. AT POWER UP
2. DEPRESSING THE FRONT PANEL BOOT SWITCH
3. ISSUING THE BOOT COMMAND FROM THE MFM CONSOLE
4. LOAD ADDRESS AND START SEQUENCE

THE 11/44 BOOT DIAGNOSTIC IS AN INTEGRAL PART OF THE UBI BOOTSTRAPPING SYSTEM .THE SYSTEM ALLOWS FOR:

A. BOOT OR POWER UP TO MFM CONSOLE WITH BOOT DIAGNOSTIC SELECTED,
B. BOOT OR POWER UP TO MFM CONSOLE WITHOUT BOOT DIAGNOSTIC SELECTED,
C. BOOT OR POWER UP TO PRIMARY BOOTSTRAP ROM WITH BOOT DIAGNOSTIC SELECTED,
D. BOOT OR POWER UP TO PRIMARY BOOTSTRAP ROM WITHOUT BOOT DIAGNOSTIC SELECTED.

2. UBI BOOTSTRAPPING SYSTEM (FIGURE 1)

THE PRIMARY ACTIVATING PROCESSES FOR THE BOOTSTRAP SYSTEM ARE EITHER A POWER UP SEQUENCE OR THE ACTUATING OF THE FRONT PANEL BOOT SWITCH.

TO ACTIVATE THE BOOTSTRAPPING PROCESS ON POWER UP SWITCH S1 (M7095 MODULE) IN THE CPU CONTROL LOGIC MUST BE IN THE ON POSITION. IF THIS SWITCH IS OFF THEN A NORMAL TRAP TO LOCATION 24 TO EXECUTE THE USER POWER UP ROUTINE WILL OCCUR. WHEN THIS SWITCH IS ON, THE CPU MICRO CODE ASSERTS 773024 ON THE BUS, SWITCH E28-1,E28-2 ,TOGETHER WITH E28-3 THRU 10, ON THE UBI WILL DETERMINE WHAT ACTION WILL FOLLOW AS THE POWER UP SEQUENCE CONTINUES.

WHEN THE CONSOLE BOOT SWITCH IS ACTUATED, A SOFTWARE ONLY POWER DOWN FOLLOWED BY A BOOT POWER UP OCCURS. NOTE THAT THE POSITION OF S1 IS IRRELEVANT IN THIS CASE.
773024 WILL BE ASSERTED ON THE UNIBUS ADDRESS LINES. LIKE THE NORMAL POWER UP DESCRIBED ABOVE, SWITCH E28-1, E28-2,TOGETHER WITH E28-3 THRU WILL DETERMINE WHAT ACTION WILL FOLLOW.

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112
113                     (CONSULT SHEET 11 M7098 MODULE FOR SWITCH SETTINGS E28-1
114                      THRU E28-10)
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3. BOOT DIAGNOSTIC ROM

THERE ARE THREE DIFFERENT TYPES OF TESTS INCLUDED IN THE BOOT DIAGNOSTIC ROM :

1. CPU TESTS
2. MEMORY TEST
3. CACHE TEST

THE CPU TESTS ARE TESTS OF MOST UNARY AND DOUBLE OPERAND INSTRUCTIONS USING REGISTER MODES 0,1 AND 4. EXCEPT TESTS THAT USE THE STACK POINTER,MAIN MEMORY IS NOT MODIFIED. IF A FAILURE IS DETECTED,A 'BR .' WILL OCCUR.

THE MEMORY TEST PERFORMS BOTH A DUAL ADDRESSING AND DATA CHECK OF ALL THE AVAILABLE MEMORY FROM ADDRESS 1000 TO 28K WITH CACHE DISABLED. THIS TEST WILL CHANGE ALL OF MEMORY TESTED. WHEN AN ERROR IS DETECTED, 'ERROR' IS PRINTED TO THE CONSOLE,FOLLOWED BY A CPU HALT. MFM CONSOLE MODE WILL BE ENTERED DUE TO THE HALT WITH THE FAILING PC BEING PRINTED. AN MFM CONSOLE 'CONTINUE' WILL ALLOW CONTINUATION OF THE BOOT ROM DIAGNOSTIC. WHEN AN ERROR IS INCURRED, R0 WILL CONTAIN THE ADDRESS AT WHICH THE FAILURE WAS DETECTED . R1 WILL CONTAIN THE FAILING DATA PATTERN AND R0 WILL CONTAIN THE EXPECTED DATA PATTERN.

A CACHE TEST IS PERFORMED TO CHECK BOTH DUAL ADDRESSING AND CACHE DATA MEMORY.THE CACHE DATA STORE AND MAIN MEMORY LOCATIONS WILL BE WRITTEN WITH THEIR OWN ADDRESS. CACHE UPDATES AND HITS USING MAIN MEMORY FROM VIRTUAL ADDRESS 1000 TO HIGHEST AVAILABLE MEMORY LESS THAN 28K ARE ALLOWED. IT MUST BE NOTED THAT THE TEST DOES NOT GUARANTEE THAT DATA RECEIVED IS ACTUALLY COMING FROM CACHE DUE TO THE CACHE CPU CLOCK RESTART OCCURING. TO GET THE CLOSEST ASSURANCE THAT THIS IS HAPPENING,CACHE HITS ARE CHECKED VIA THE 'HIT' MAINTENANCE BIT IN THE CACHE MAINTENANCE REGISTER. WHEN AN ERROR OCCURS AND MFM 'CONTINUE' IS USED,ERROR HANDLING IS SIMILAR TO MEMORY TEST WHEN DATA ERRORS ARE INCURRED. BUT A 'CONTINUE' AFTER A HIT ERROR WILL RESULT WITH THE CACHE TEST BEING ABORTED AND THE BOOT ROM DIAGNOSTIC EXITING.

NOTE: IF CACHE IS NOT FOUND, THE CACHE TEST IS NOT PERFORMED.

4.0 PRINTOUT EXAMPLES

CONDITIONS: THE FOLLOWING EXAMPLES ARE ILLUSTRATIONS
OF TYPEOUTS TO THE TERMINAL WITH THE UBI MICRO SWITCHES
E28-2 THRU 10 SELECTED FOR 'POWERUP/BOOT
TO CONSOLE WITH DIAGNOSTIC' (USW=020)
(SEE FIG. 1)

1. ERROR OCCURS IN BOOT DIAGNOSTIC CACHE TEST WHEN POWERUP OCCURS:

```
ERROR
CONSOLE
17777707  165652
>>>
```

2. ERROR OCCURS WHEN BOOT COMMAND IS ISSUED FROM CONSOLE

```
>>>B
ERROR
CONSOLE
17777707  165652
>>>
```

3. NO ERROR OCCURS; BOOT DIAGNOSTIC RUNS SUCCESSFULLY:

```
>>>B

CONSOLE
17777707  165714
>>>
```

5.0 LOAD ADDRESS AND START PROCEDURE

THE BOOT DIAGNOSTIC MAY BE RUN BY LOADING ADDRESS 165020
USING THE MFM CONSOLE AND STARTING. THE FOLLOWING EXAMPLE EXHIBITS
THIS AND ILLUSTRATES SUCCESSFUL COMPLETION OF THE DIAGNOSTIC.

H 1

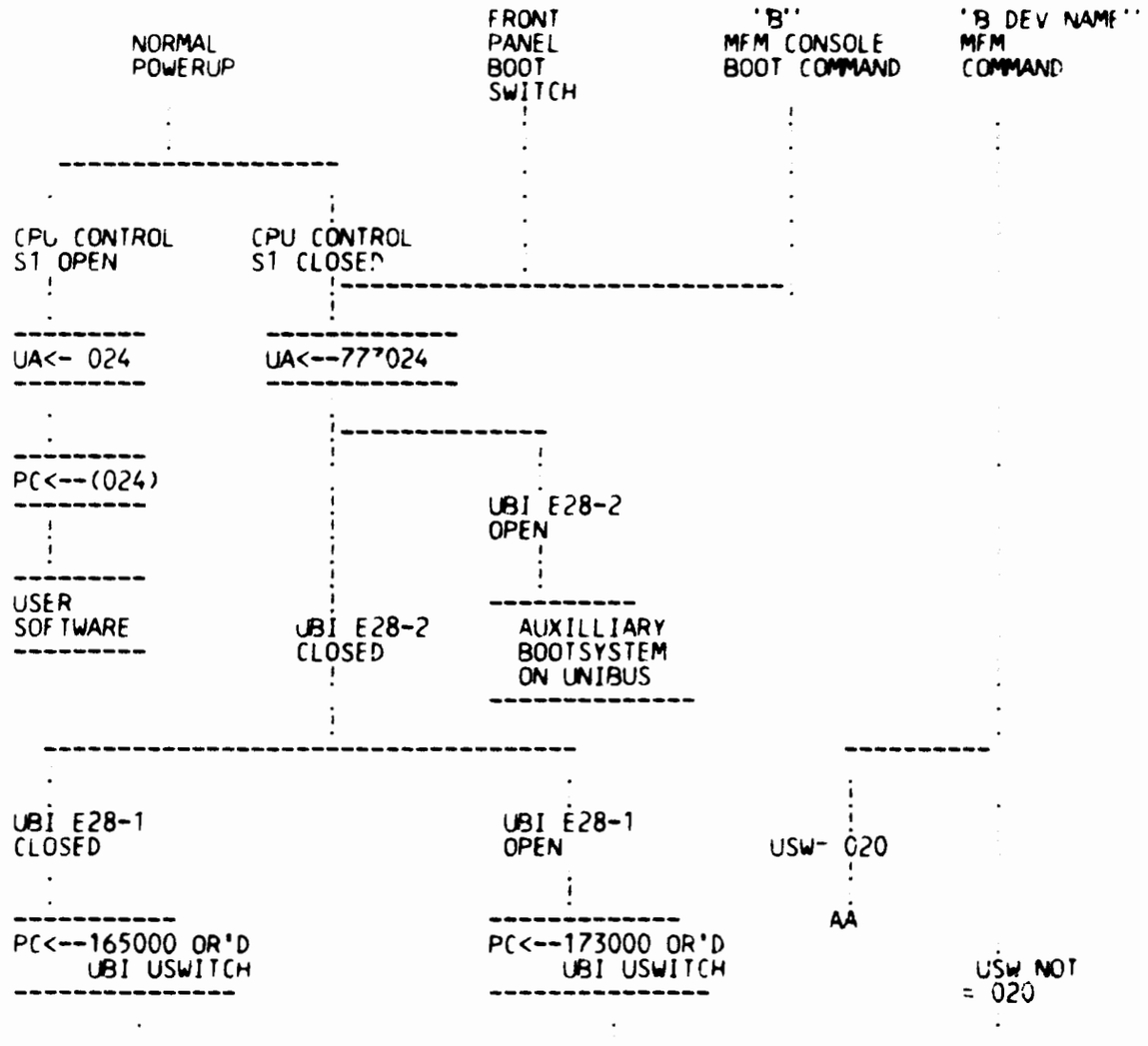
```
223
224
225
226
227
228
229
230
```

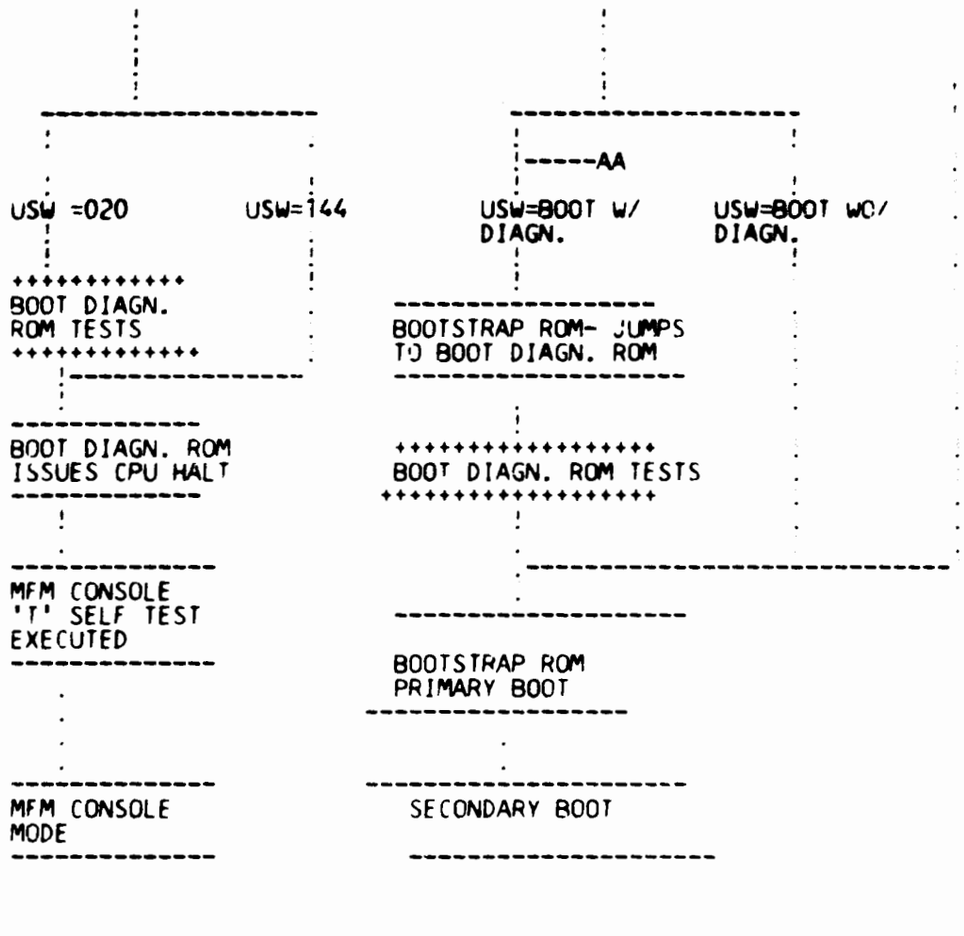
```
>>>S 165020

CONSOLE
17777707  165714
>>>
```

.MAIN. MA M ... B -ASE

11/44 UBI BOOTSTRAP SYSTEM- FIG. 1

NOTES: 1. CLOSED=ON
2. OPEN -OFF
3. USW- UBI E28-3 THRU 10 MICRO SWITCH SETTING (LOCATED ON UBI MODULE)
4. UA- UNIBUS ADDRESS
5. S1 IS LOCATED ON KE44-1 DATA PATH (M7094)




USW =020
USW=144
BOOT DIAGN.
ROM TESTS
BOOT DIAGN. ROM
ISSUES CPU HALT
MFM CONSOLE
'T' SELF TEST
EXECUTED
MFM CONSOLE
MODE
-----AA
USW=BOOT W/
DIAGN.
USW=BOOT W/O
DIAGN.
BOOTSTRAP ROM- JUMPS
TO BOOT DIAGN. ROM
BOOT DIAGN. ROM TESTS
BOOTSTRAP ROM
PRIMARY BOOT
SECONDARY BOOT

```
                                %
                                .ENABL  ABS
000000
          001015                MISS=1015                       ;UNCONDITIONAL BYPASS,FORCE MISS LO
                                                                ;FORCE MISS HI, DISABLE CACHE INTERRUPT
                                                                ;USED FOR CACHE CONTROL REGISTER
          104000                ERROR=104000
          165000                .=165000
165000    012737    177777  000706  ENTBT:  MOV     #-1,@#706               ; BOOT/POWERUP TO PERIPHERAL
                                                                ;ROM WITH DIAGNOSTIC.SET FLAG.
                                                                ;JUMPED TO HERE FROM 165564
165006    000405                        BR      SAVE
165010    005037    000706      START:  CLR     @#706           ;CLEAR FLAG
165014    000402                        BR      SAVE
165016    000240                        NOP
165020    000773                        BR      START           ;ENTRY: BOOT/POWERUP TO CONSOLE WITH DIAGNOSTI
165022    010037    000700      SAVE:   MOV     R0,@#700        ;SAVE R0,R1,R4 CONTENTS.
165026    010137    000702              MOV     R1,@#702
165032    010437    000704              MOV     R4,@#704
165036    012737    165676  000004      MOV     #CPUERR,@#4             ;SETUP FOR ANY CPU ERRORS
165044    012737    000340  000006      MOV     #340,@#6
165052    012737    165736  000030      MOV     #$ERR,@#30      ;SETUP ERROR PRINT ROUTINE
165060    012737    000340  000032      MOV     #340,@#32
                                ;;******************************************************************************
                                        .SBTTL  TEST1   THIS TEST VERIFIES THE UNCONDITIONAL BRANCH
                                ;*
                                ;*      THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
                                ;*      THIS TEST IS ENTERED AND THEY SHOULD REMAIN THAT WAY UPON
                                ;*      THE COMPLETION OF THIS TEST.
                                ;;******************************************************************************
165066                          TST1:

165066    000401                        BR      TST2            ; * BRANCH ALWAYS
165070    000777                        BR .

                                ;;******************************************************************************
                                        .SBTTL  TEST2   TEST "CLR", MODE "0", AND "BMI","BVS","BHI","BLT","BLOS"
                                ;*
                                ;*      THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
                                ;*      THS TEST IS ENTERED. UPON COMPLETION OF THIS TEST THE "SP"
                                ;*      (R6) SHOULD BE ZERO AND ONLY THE "Z" FLIP-FLOP WILL BE SET.
                                ;*
                                ;;******************************************************************************
165072                          TST2:

165072    005006                        CLR     SP              ;N-0,Z=1,V=0,C=0,SP=000000
165074    100404                        BMI     1$              ; V BRANCH IF N=1
165076    102403                        BVS     1$              ; V BRANCH IF V=1
165100    101002                        BHI     1$              ; V BRANCH IF Z AND C ARE BOTH 0
165102    002401                        BLT     1$              ; V BRANCH IF (N XOR V)=1
165104    101401                        BLOS    TST3            ; * BRANCH IF (Z XOR C)=0
165106    000777              1$:       BR .

                                ;;******************************************************************************
                                        .SBTTL  TEST3   TEST "DEC", MODE "0", AND "BPL","BEQ","BGE","BLE"
                                ;*
```

```
                                ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE: R0 = ?, R1 = ?, R2 = ?
                                ;*      R3 = ?, R4 = ?, R5 = ?, SP = 000000
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                                ;*      N = 1, Z = 0, V = 0, AND C = 0
                                ;*      THE REGISTERS AFFECTED BY THE TEST ARE:
                                ;*      SP = 177777
                                ;*
                                ;;**************************************************************************
165110                          TST3:
165110  005306                          DEC     SP              ;N=1,Z=0,V=0,C=0,SP=177777
165112  100003                          BPL     1$              ; V BRANCH IF N=0
165114  001402                          BEQ     1$              ; V BRANCH IF Z=1
165116  002001                          BGE     1$              ; V BRANCH IF (N XOR V)=0
165120  003401                          BLE     TST4            ; * BRANCH IF (Z OR (N XOR V)) 1
165122  000777                  1$:     BR .

                                ;;**************************************************************************
                                        .SBTTL  TEST4   TEST 'ROR, MODE '0', AND 'BVC','BHIS','BNE'
                                ;*
                                ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 1, Z = 0, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE: R0=?, R1=?, R2 = ?
                                ;*      R3 = ?, R4 = ?, R5 = ?, SP = 177777
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                                ;*      N = 0, Z = 0, V = 1, AND C = 1
                                ;*      THE REGISTERS AFFECTED BY THE TEST ARE:
                                ;*      SP = 077777
                                ;*
                                ;;**************************************************************************
165124                          TST4:
165124  006006                          ROR     SP              ;N=0,Z=0,V=1,C=1,SP=077777
165126  102002                          BVC     1$              ; V BRANCH IF V=0
165130  103001                          BHIS    1$              ; V BRANCH IF C=0
165132  001001                          BNE     TST5            ; * BRANCH IF Z=0
165134  000777                  1$:     BR .


                                ;;**************************************************************************
                                        .SBTTL  TEST5   TEST REGISTER DATA PATH
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 0, V = 1, AND C = 1.
                                ;*      THE REGISTERS ARE: R0 = ?, R1 = ?, R2 = ?
                                ;*      R3 = ?, R4 = ?, R5 = ?, SP = 077777.
                                ;:      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0  AND C = 0.
                                ;*      THE REGISTERS ARE LEFT AS FOLLOWS:
                                ;*      R0 = 125252, R1 = 000000, R2 = 125252, R3 = 125252
                                ;*      R4 = 125252, R5 = 125252, AND SP = 125252
                                ;*
                                ;;**************************************************************************
165136                          TST5:
165136  012706  125252                MOV     #125252,SP      ;N=0,Z=0,V=0,C=1,SP=125252
165142  000402                          BR      .+6
165144  000000                          HALT                    ;ENTRY: BOOT/POWERUP TO CONSOLE WITHOUT DIAGNOSTIC
```

```
 165146  000776                         BR      .-2
 165150  010600                         MOV     SP,R0           ;N=0,Z=0,V=0,C=1,R0=125252
 165152  010001                         MOV     R0,R1           ;N=0,Z=0,V=0,C=1,R1=125252
 165154  010102                         MOV     R1,R2           ;N=0,Z=0,V=0,C=1,R2=125252
 165156  010203                         MOV     R2,R3           ;N=0,Z=0,V=0,C=1,R3=125252
 165160  010304                         MOV     R3,R4           ;N=0,Z=0,V=0,C=1,R4=125252
 165162  010405                         MOV     R4,R5           ;N=0,Z=0,V=0,C=1,R5=125252
 165164  160501                         SUB     R5,R1           ;N=0,Z=1,V=0,C=0, AND R1=000000
 165166  002401                         BLT     1$              ; V BRANCH IF (N XOR V)=1
 165170  001401                         BEQ     TST6            ; * BRANCH IF Z=1
 165172  000777                 1$:     BR .

                                ;;*******************************************************************************
                                        .SBTTL  TEST6   TEST 'ROL', 'BCC', 'BLT'
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N   0, Z = 1, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                                ;*      R3 = 125252, R4 = 125252, R45 - 125252, SP = 125252.
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N   0, Z = 0, V = 1, AND C - 1.
                                ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                                ;*      R2 WHICH SHOULD NOW EQUAL 05252'.
                                ;*
                                ;;*******************************************************************************
 165174                         TST6:
 165174  006102                         ROL     R2              ;N=0,Z=0,V=1, =1, AND R2 = 052524
 165176  103001                         BCC     1$              ; V BRANCH IF C=0
 165200  002401                         BLT     TST7            ; * BRANCH IF (N XOR V)-1
 165202  000777                 1$:     BR .


                                ;;*******************************************************************************
                                        .SBTTL  TEST7   TEST 'ADD', 'INC', 'COM', AND 'BCS', 'BLE'
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 0, V = 1, AND C = 1.
                                ;*      THE REGISTERS ARE: R0 = 125252  R1 = 000000, R2 - 052524
                                ;*      R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                                ;*      R3 WHICH NOW EQUALS 000000, AND R1 WHICH IS ALSO 000000
                                ;*
                                ;;*******************************************************************************
 165204                         TST7:
                                                                 ;(R2 = 052524) + (R3 = 125252)
 165204  060203                         ADD     R2,R3           ;N=1,Z=0,V=0,C=0,AND R3=177776
 165206  005203                         INC     R3              ;N=1,Z=0,V=0,C=0, AND R3=177777
 165210  005103                         COM     R3              ;N=0,Z=1,V=0,C=1, AND R3=000000
 165212  060301                         ADD     R3,R1           ;N=0,Z=1,V-0,C=0, AND R1 - 000000
 165214  103401                         BCS     1$              ; V BRANCH IF C-1
 165216  003401                         BLE     TST10           ; * BRANCH IF (Z OR (N XOR V))-1
 165220  000777                 1$:     BR .

                                ;;*******************************************************************************
                                        .SBTTL  TEST10  TEST 'ROR', 'DEC', 'BIS', 'ADD', AND 'BLO'
```

```
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 052524
                        ;*      R3 = 000000, R4 = 125252, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 1, Z = 0, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R4 WHICH SHOULD NOW EQUAL 052525, AND
                        ;*      R1 WHICH SHOULD NOW EQUAL 177777
                        ;*
                        ;;*************************************************************************
165222                  TST10:
165222  006004                  ROR     R4              ;N=0,Z=0,V=1,C=0, AND R4 = 052525
165224  050403                  BIS     R4,R3           ;N=0,Z=0,V=0,C=0, AND R3 = 052525
165226  060503                  ADD     R5,R3           ;N=1,Z=0,V=0,C=0, AND R3 = 177777
165230  005203                  INC     R3              ;N=0,Z=1,V=0,C=0, AND R3 = 000000
165232  103402                  BLO     1$              ; V BRANCH IF C=1
165234  005301                  DEC     R1              ;N=1,Z=0,V=0,C=0, AND R1 = 177777
165236  002401                  BLT     TST11           ; * BRANCH IF (N XOR V)=1
165240  000777          1$:     BR .
                        ;*
                        ;;*************************************************************************
                                .SBTTL  TEST11  TEST "COM", "BIC", AND "BGT", "BLE"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 1, Z = 0, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 177777, R2 = 052524
                        ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 0, V = 1, AND C = 1.
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R0 WHICH SHOULD NOW EQUAL 052525, AND
                        ;*      R1 WHICH SHOULD NOW EQUAL 052524
                        ;*
                        ;;*************************************************************************
165242                  TST11:
165242  005100                  COM     R0              ;N=0,Z=0,V=0,C=1, AND R0   052525
165244  101401                  BLOS    2$              ; * BRANCH IF (Z OR C)=1
165246  000777                  BR .                    ;STOP HERE IF BRANCH FAILED
165250  040001          2$:     BIC     R0,R1           ;N=1,Z=0,V=0,C=1, AND R1 = 125252
165252  060101                  ADD     R1,R1           ;N=0,Z=0,V=1,C=1, AND R1 = 052524
165254  003001                  BGT     1$              ; V BRANCH IF Z AND ( N XOR V) ARE BOTH 0
165256  003401                  BLE     TST12           ; * BRANCH IF (Z OR (N XOR V))=1
165260  000777          1$:     BR .
                        ;;*************************************************************************
                                .SBTTL  TEST12  TEST "SWAB", "CMP", "BIT", AND "BNE", "BGT"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 0, V = 1, AND C = 1.
                        ;*      THE REGISTERS ARE: R0 = 052525, R1 = 052524, R2 = 052524
                        ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N   0, Z = 0, V = 0, AND C = 1.
                        ;*      THE REGISTERS ARE NOW:
                        ;*      R0   052525, R1 = 052125, R2 = 052524, R3 = 000000
```

```
                                ;*      R4 = 052525, R5 = 052525, SP = 125252.
                                ;*
                                ;;*****************************************************************************
165262                          TST12:
165262  000301                          SWAB    R1              ;N=0,Z=0,V=0,C=0, AND R1 = 052125
165264  020127  052125                  CMP     R1,#052125              ;N=0,Z=1,V=0,C=0
165270  001004                          BNE     1$              ; V BRANCH IF Z=0
                                                                ;R4 = 052525 R5 = 125252
165272  030405                          BIT     R4,R5           ;N=0,Z=1,V=0,C=0
165274  003002                          BGT     1$              ; V BRANCH IF Z OR (N XOR V) ARE 0
165276  005105                          COM     R5              ;N=0,Z=0,V=0,C=1, AND R5 = 052525
165300  001001                          BNE     TST13           ; * BRANCH IF Z-1
165302  000777                  1$:     BR .
                                ;;*****************************************************************************
                                        .SBTTL  TEST13  TEST "MOVB", "SOB", "CLR", "TST" AND "BPL", "BNE"
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N - 0, Z - 0, V = 0, AND C = 1.
                                ;*      THE REGISTERS ARE: R0 = 052525, R1 = 052125, R2 - 052524
                                ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP - 125252.
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C - 0.
                                ;*      R0 IS DECREMENTED BY A SOB INSTRUCTION TO 000000
                                ;*      R1 IS CLEARED AND THEN INCREMENTED AROUND TO 000000
                                ;*
                                ;;*****************************************************************************
165304                          TST13:
165304  112700  177401                  MOVB    #177401,R0      ;N=0,Z-0,V=0,C-1, AND R0 - 000001
165310  100001                          BPL     2$              ; * BRANCH IF N=0
165312  000777                  1$:     BR .                    ;STOP IF "BPL" FAILED
165314  077002                  2$:     SOB     R0,1$           ;DO NOT LOOP SINCE (R0 -1)   0
165316  005001                          CLR     R1              ;N=0, Z=1, V-0, C=0, AND R1   000000
165320  005201                  3$:     INC     R1              ;INCREMENT 64K TIMES (2 ** 16)
165322  077002                          SOB     R0,3$           ;LOOP BACK TO "INC" 64K TIMES
165324  005700                          TST     R0              ;N=0,Z-1,V=0,C-0, AND R0 = 000000
165326  001002                          BNE     4$              ; V BRANCH IF Z 0
165330  005701                          TST     R1              ;N=0,Z=1,V=0,C 0, AND R1 - 000000
165332  001401                          BEQ     TST14
165334  000777                  4$:     BR .
                                ;;*****************************************************************************
                                        .SBTTL  TEST14  TEST "JSR", "RTS", "RTI", & "JMP"
                                ;*
                                ;*      THIS TEST FIRST SETS THE STACK POINTER TO 776,
                                ;*      AND THEN VERIFIES THAT "JSR", "RTS", "RTI", AND "JMP"
                                ;*      ALL WORK PROPERLY.
                                ;*
                                ;*      ON ENTRY TO THIS TEST THE STACK POINTER "SP" IS INITIALIZED
                                ;*      TO 00776 AND IS LEFT THAT WAY ON EXIT.
                                ;*
                                ;;*****************************************************************************
165336                          TST14:
165336  012706  000776          11$:    MOV     #776,SP         ;SET UP THE STACK POINTER
165342  004767  000002                  JSR     PC,1$           ;TRY TO JSR TO 1$
165346  000777                  10$:    BR .                    ;THE "JSR" MUST HAVE FAILED
165350  022716  165346          1$:     CMP     #10$,(SP)       ;WAS THE CORRECT ADDRESS PUSHE'
```

```
 614 165354  001401                        BEQ     2$              ;BRANCH IF YES
 615 165356  000777                        BR      .               ;WRONG THING PUSHED ON STACK
 616 165360  012716  165370          2$:   MOV     #3$,(SP)        ;CHANGE THE ADDRESS ON THE STACK
 617 165364  000207                        RTS     PC              ;TRY TO RETURN TO 3$
 618 165366  000777                        BR      .               ;DID NOT RETURN PROPERLY
 619 165370  005046                  3$:   CLR     -(SP)           ;PUSH A ZERO ON THE STACK
 620 165372  012746  165402              MOV     #4$,-(SP)       ;PUSH THE RETURN ADDRESS ON STACK
 621 165376  000002                        RTI                     ;SEE IF AN "RTI" WORKS
 622 165400  000777                        BR      .               ;THE "RTI" FAILED
 623 165402  000137  165410          4$:   JMP     @#5$            ;TRY TO "JMP"
 624 165406  000777                        BR      .               ;THE "JMP" FAILED
 625 165410                          5$:                           ;ADDRESS TO "JMP" TO
 626
 627                                ;;=====================================================================
 628                                        .SBTTL  TEST15  TEST MAIN MEMORY FROM VIRTUAL 001000 TO LAST ADDR.
 629                                ;*
 630                                ;*      THIS TEST WILL TEST MAIN MEMORY WITH THE CACHE DISABLED, FROM
 631                                ;*      VIRTUAL ADDRESS 001000 TO LAST ADDR.
 632                                ;*
 633                                ;*      IN THIS TEST THE REGISTERS ARE INITIALIZED AS FOLLOWS:
 634                                ;*      R0 - 001000, R1 = DATA READ, R2   001000, R3-177746(CACHE CONTROL REGISTER)
 635                                ;*       R5 - LAST MEMORY ADDRESS, SP - 000776
 636                                ;*
 637                                ;*      R4 IS USED AS POINTER FOR ERROR PRINT MESSAGE
 638                                ;*
 639
 640                                ;;=====================================================================
 641 165410                          TST15:
 642 165410  012705  160000              MOV     #160000,R5      ;FIRST GET SIZE OF MEMORY.
 643 165414  005037  000006              CLR     @#6
 644 165420  012737  165426  000004      MOV     #1$,@#4
 645 165426  012706  000776          1$: MOV     #776,SP
 646 165432  005745                      TST     -(R5)
 647                                                             ;IN END,R5 CONTAINS LAST MEM ADDR.
 648
 649 165434                          FIX:
 650 165434  012703  177746              MOV     #177746,R3      ;CACHE CONTROL REGISTER
 651 165440  012737  165466  000004      MOV     #6$,@#4         ;SETUP FOR POTENTIAL TRAP IF CACHE NOT PRESENT
 652 165446  012713  001015              MOV     #MISS,(R3)              ;ACCESS CACHE BY DISABLING CACHE
 653 165452  012737  165662  000114      MOV     #CONT,@#114             ;SET UP PARITY VECTOR
 654 165460  005037  000116              CLR     @#116           ;SET PROCESSOR STATUS WORD TO ZERO
 655 165464  000403                      BR      7$                      ;CACHE MUST BE PRESENT
 656 165466  012737  165676  000004  6$: MOV     #CPUERR,@#4             ;RESTORE TRAP VECTOR
 657
 658 165474  012702  001000          7$: MOV     #1000,R2        ;FIRST ADDRESS STORAGE
 659 165500  010200                      MOV     R2,R0           ;SETUP FORST ADDRESS
 660 165502  010010                  1$: MOV     R0,(R0)         ;LOAD EACH ADDRESS WITH ITS
 661                                                             ;OWN ADDRESS
 662 165504  005720                      TST     (R0)+
 663 165506  020005                      CMP     R0,R5
 664 165510  101774                      BLOS    1$
 665 165512  010200                      MOV     R2,R0           ;SET STARTING ADDRESS IN R0
 666 165514  011001                  2$: MOV     (R0),R1         ;GET THE DATA
 667 165516  020001                      CMP     R0,R1           ;IS IT CORRECT?
 668 165520  001402                      BEQ     3$              ;BRANCH IF YES
 669 165522  104000                      ERROR                   ;GO TO PRINT ROUTINE
 670 165524  000000                      HALT                    ;DATA ERROR ON READING MEMORY LOCATION
```

```
    671
    672 165526  005120          3$:     COM     (R0)+           ;R0 = ADDRESS, R1   DATA RECEIVED, R0   DATA EXPECTED
    673 165530  020005                  CMP     R0,R5           ;COMPLEMENT DATA AND INCREMENT ADDRESS
    674 165532  101770                  BLOS    2$
    675 165534  014001          4$:     MOV     -(R0),R1        ;READ THE DATA (IT SHOULD NOW BE THE
    676                                                         ;COMPLEMENT OF THE ADDRESS)
    677 165536  005101                  COM     R1              ;COMPLEMENT BEFORE CHECKING
    678 165540  020001                  CMP     R0,R1           ;IS THE DATA CORRECT?
    679 165542  001402                  BEQ     5$              ;BRANCH IF YES
    680 165544  104000                  ERROR                   ;GO TO PRINT ROUTINE
    681 165546  000000                  HALT                    ;DATA ERROR ON READING MEMORY LOCATION
    682                                                         ;R0=ADDRESS, R1-DATA RECEIVED, R0=DATA EXPECTED
    683 165550  020002          5$:     CMP     R0,R2
    684 165552  001370                  BNE     4$
    685
```

```
                                ;;*************************************************************************
                                ;       .SBTTL  TEST16  TEST MEMORY WITH THE DATA CACHE ON
                                ;*
                                ;*      THIS TEST CHECKS VIRTUAL MEMORY FROM 001000 THRU LAST ADDRESS
                                ;*      TO INSURE THAT YOU CAN GET HITS ALL THE WAY UP THROUGH MAIN
                                ;*      MEMORY.
                                ;*
                                ;*      UPON ENTRY THE REGISTERS WILL BE SET UP AS FOLLOWS:
                                ;*      R0 = 001000 (ADDRESS), R2 = (FIRST ADDRESS), R3=177746(CACHE CONTROL REGISTER)
                                ;*      R5 = (LAST MEMORY ADDRESS), SP = 776
                                ;*
                                ;*      R4 IS USED AS POINTER FOR ERROR MESSAGE
                                ;*
                                ;;*************************************************************************
165554                          TST16:
165554  012737  165704  000004        MOV     #JUMP,@#4       ;SETUP FOR POSSIBLE TRAP
165562  000402                  BR      .+6
165564  000167  177210          JMP     ENTBT           ;ENTRY: BOOT/POWERUP TO BOOTSTRAP ROM
                                ;               WITH DIAGNOSTIC
165570  005013                  CLR     (R3)            ;ENABLE ALL CACHE; ALLOW FOR CACHE INTERRUPTS
165572  012737  165676  000004        MOV     #CPUERR,@#4     ;RESTORE VECTORS

165600  012702  001000                MOV     #1000,R2        ;SETUP FIRST ADDRESS
165604  010200                  MOV     R2,R0           ;FIRST ADDRESS IS 1000 OCTAL
165606  010010          1$:     MOV     R0,(R0)         ;FILL MEMORY WITH ADDRESSES
165610  005720                  TST     (R0)+
165612  020005                  CMP     R0,R5
165614  101774                  BLOS    1$
165616  010200          2$:     MOV     R2,R0           ;FIRST ADDRESS
165620  005110          3$:     COM     (R0)            ;DOUBLE COMPLEMENT DATA AND
165622  005110                  COM     (R0)            ;MAKE SURE IT IS IN THE CACHE.
165624  021000                  CMP     (R0),R0         ;CREATE READ HIT;
165626  001402                  BEQ     5$              ;BRANCH IF DATA MATCHES
165630  104000                  ERROR                   ;GOTO PRINT ROUTINE
165632  000000                  HALT                    ;DATA DIDN'T MATCH R0 = ADDRESS + 2
165634  005720          5$:     TST     (R0)+           ;READ HIT;CLOCK HIT INFO. INTO MAINTENANCE REGISTER
165636  032737  000400  177750        BIT     #400,@#177750           ;WAS THE LAST MEMORY REFERENCE A HIT
165644  001403                  BEQ     4$              ;BRANCH IF YES
165646  104000                  ERROR                   ;GOTO PRINT ROUTINE
165650  000000                  HALT                    ;HIT FAILED TO OCCUR R0 = ADDRESS + 2
165652  000406                  BR      DSBLCACH        ;ABORT REST OF TEST IF "CONTINUE" PRESSED
165654  020005          4$:     CMP     R0,R5
165656  101760                  BLOS    3$
165660  000411          JUMP0:  BR      JUMP            ;EXIT TEST

165662  104000          CONT:           ERROR                   ;GOTO PRINT ROUTINE
165664  000000                          HALT                    ;STOP HERE IF THERE IS A CACHE PARITY ERROR
                                                        ;OR A MAIN MEMORY PARITY ERROR
                                                        ;CHECK CCR, MEMORY REGISTER AND CPU REGISTER
                                                        ;TO FIND WHICH ONE
165666  000776                          BR      .-2
165670                          DSBLCACH:
165670  012713  001015                MOV     #MISS,(R3)      ;FORCE MISSES IN BOTH GROUPS OF CACHE
165674  000403                  BR      JUMP
```

```
    744  65676  104000                    CPUERR: ERROR                   ;GOTO PRINT ROUTINE
    745 165700  000000                            HALT                    ;TRAP TO ERROR VECOR 4 OCCURRED-CHECK STACK
    746                                                                   ;FOR ORIGIN
    747 165702  000776                            BR      .-2
    748
    749 165704                                  JUMP:
    750 165704  005737  000706                    TST @#706                       ;WAS THE DIAGNOSTIC ENTERED FROM PERIPHERAL
    751                                                                   ;ROM
    752 165710  001002                            BNE 1$                  ;YES
    753 165712  000000                            HALT                    ;HALT TO GET TO 11/44 CONSOLE
    754 165714  000776                            BR      .-2
    755
    756 165716                                  1$:
    757 165716  013700  000700                    MOV     @#700,R0        ;NOW RESTORE ALL NEEDED REGISTERS.
    758 165722  013701  000702                    MOV     @#702,R1        ;AND RETURN TO BOOTSTRAP.
    759 165726  013704  000704                    MOV     @#704,R4
    760 165732  000164  000002                    JMP     2(R4)           ;RETURN TO PERIPHERAL ROM.REGISTER R4
    761                                                                   ;CONTAINS RETURN ADDRESS LOCATION
    762
    763 165736  012704  165762          $ERR:   MOV     #ERRMSG,R4
    764 165742  105737  177564          PUTCHR: TSTB    @#177564
    765 165746  100375                          BPL     PUTCHR
    766 165750  112437  177566                  MOVB    (R4)+,@#177566
    767 165754  105714                          TSTB    (R4)
    768 165756  001371                          BNE     PUTCHR
    769 165760  000002                          RTI
    770
    771 165762     015      012      105 ERRMSG: .ASCIZ  <15><12>/ERROR/
        165765     122      122      117
        165770     122      000
    772                                         .EVEN
    773
    774         165772                          .=165772
    775 165772  000000                          .WORD   0
    776
    777
    778 165774  041460                          .WORD   41460           ;IDENTIFIES ROM AS "C0": C VERSION, REV 0.
    779 165776  124140                          .WORD   124140          ;CONTAINS CRC-16 WORD FOR LAST 255 WORDS.
    780
    781
    782         000001                          .END
```

.MAIN. MACRO M1111 26-SEP-79 10:28 PAGE 8-2
SYMBOL TABLE

```
CONT    165662          FIX     165434          START   165010          TST14   165336          TST4    165124
CPUERR  165676          JUMP    165704          TST1    165066          TST15   165410          TST5    165136
DSBLCA  165670          JUMP0   165660          TST10   165222          TST16   165554          TST6    165174
ENTBT   165000          MISS  = 001015          TST11   165242          TST2    165072          TST7    165204
ERRMSG  165762          PUTCHR  165742          TST12   165262          TST3    165110          $ERR    165736
ERROR = 104000          SAVE    165022          TST13   165304

. ABS.  166000      000
        000000      001
ERRORS DETECTED:  0

VIRTUAL MEMORY USED:  376 WORDS  ( 2 PAGES)
DYNAMIC MEMORY:  2794 WORDS  ( 10 PAGES)
ELAPSED TIME:  00:00:15
.CKKFAA0.SEQ/NL:TOC/CRF=CKKFAA0.P11
```

[illegible]AA CREATED BY MACRO ON [illegible]-FEB-79 AT [illegible] PAGE [illegible]
SYMBOL CROSS REFERENCE CREF

SYMBOL	VALUE	REFERENCES						
CONT	165662	7-653	#8-734					
CPUERR	165676	7-348	7-656	8-728	#8-744			
DSBLCA	165670	8-729	#8-740					
ENTBT	165000	#7-337	8-705					
ERRMSG	165762	8-763	#8-771					
ERROR =	104000	#7-335	7-669	7-680	8-7[illegible]	8-7[illegible]	8-7[illegible]	8-7[illegible]
FIX	165434	#7-649						
JUMP	165704	8-703	8-732	8-74[illegible]	#8-749			
JUMPO	165660	#8-732						
MISS =	001015	#7-332	7-652	8-741				
PUTCHR	165742	#8-764	8-765	8-768				
SAVE	165022	7-340	7-342	#7-345				
START	165010	#7-341	7-344					
TST1	165066	#7-359						
TST10	165222	7-495	#7-512					
TST11	165242	7-519	#7-536					
TST12	165262	7-543	#7-560					
TST13	165304	7-568	#7-584					
TST14	165336	7-595	#7-609					
TST15	165410	#7-641						
TST16	165554	#8-702						
TST2	165072	7-362	#7-373					
TST3	165110	7-380	#7-396					
TST4	165124	7-401	#7-417					
TST5	165136	7-421	#7-439					
TST6	165174	7-452	#7-468					
TST7	165204	7-471	#7-488					
$ERR	165736	7-350	#8-763					