

# UDC11

CONTROL TEST  
MD-11-DZUDB-B

EP-DZUDB-B-DL  
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FICHE 1 OF 1

JUN 1978  
digital  
MADE IN USA



IDENTIFICATION

PRODUCT CODE:       MAINDEC-II-DZ UDB-B-D  
PRODUCT NAME:       UDCII CONTROL TEST  
DATE CREATED:        JANUARY 1973  
MAINTAINER:         DIAGNOSTIC GROUP  
AUTHOR:             R. WHITTON

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DIGITAL EQUIPMENT CORPORATION

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1. ABSTRACT

UDC11 CONTROL TEST TESTS VIRTUALLY ALL OF THE CONTROL LOGIC UP TO THE UDC BUS. MAINTENANCE LOGIC IS USED TO GENERATE UDC INTERRUPTS AND TO SINGLE STEP THE SCAN REGISTER. NOTE: THE UDC BUS CABLE TO THE SYSTEM UNITS CAN BE REMOVED FROM THE CONTROL WHILE THIS TEST IS RUN IF ERRORS RESULT DUE TO INTERRUPT MODULES GENERATING INTERRUPTS. IF THE MODULES GENERATING INTERRUPTS ARE IN THE FIRST FOUR ADDRESSES (000-004), THE MODULES MUST BE REMOVED SINCE REMOVING THE BUS CABLE WILL NOT DISCONNECT THESE MODULES FROM THE UDC BUS.

A POWER FAIL TEST IS INCLUDED. STARTING ADDRESS=000204. THIS TEST WILL TYPE A MESSAGE THAT IT IS WAITING FOR A POWER FAILURE AND WILL TYPE WHICH ONE OF TWO TYPES OF FAILURES OCCUR (UDC DC POWER OR PDP11) WHEN AND IF THEY HAPPEN.

2. REQUIREMENTS

2.1 EQUIPMENT

A. PDP-11  
B. ASR33/39 TELETYPE.  
C. UDC11 CONTROL

THE PROCESSOR AND TELETYPE MUST BE IN OPERATING CONDITION.

THE TELETYPE AND UDC11 CONTROL MUST HAVE THEIR STANDARD PERIPHERAL ADDRESSES, INTERRUPT LEVELS, AND INTERRUPT VECTOR ADDRESSES. REFER TO SECTION 7.2 IF YOUR SYSTEM DOES NOT HAVE STANDARD PERIPHERAL ADDRESSES.

2.2 STORAGE

THIS PROGRAM USES LOCATIONS 000000 THROUGH 012910.

3. LOADING PROCEDURE

THIS PROGRAM'S OBJECT TAPE IS PUNCHED IN ABSOLUTE FORMAT. THE ABS LOADER IS USED TO LOAD THE PROGRAM.

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4: USE PROCEDURE

- A: UDC BUS CABLE MAY BE UNPLUGGED FROM CONTROL
- B: LOAD EITHER ADDRESS 200 FOR CONTROL DIAGNOSTIC OR ADDRESS 204 FOR POWER FAIL TEST;
- C: PRESS START.
- D: THE PROGRAM IDENTIFIES ITSELF, TYPES SETUP INSTRUCTIONS, SR OPTIONS MESSAGE, AND HALTS.
- E: PERFORM SETUP (STEPS A AND B), AND SELECT DESIRED SR OPTIONS, IF ANY. NORMAL SR SETTING IS 000000.

THIS PROGRAM'S SR OPTIONS ARE:

SR15 = 1	HALT ON ERROR
SR14 = 1	ENTER SCOPE MODE
SR13 = 1	INHIBIT ERROR PRINTOUT
SR11 = 1	INHIBIT ITERATION
SR10 = 1	HALT AT END OF TEST CURRENTLY EXECUTING
SR9 = 1	SELECT THE TEST SPECIFIED BY SR7 THROUGH SR2
SR7 THROUGH SR8	= NUMBER OF TEST TO BE SELECTED

SECTION 7.1 GIVES A COMPLETE EXPLANATION OF SR OPTIONS.

- F: PRESS CONT; THE PROGRAM BEGINS EXECUTION.
- G: AT THE END OF EACH PASS THE TELETYPE BELL RINGS ONCE, AND "END" IS TYPED.
- H: REFER TO SECTION 6.2 IF ERROR PRINTOUTS OCCUR.

EXECUTION TIME:

- A: ONE NORMAL ERROR FREE PASS TAKES APPROXIMATELY 1 MINUTES.
- B: ONE SINGLE ITERATION PASS (SR11=1) TAKES ABOUT 10 SECONDS.

\*\*\*\*\*NOTE\*\*\*\*\*

THE SINGLE ITERATION PASS IS A CONVENIENT WAY TO QUICKLY DETERMINE IF ANY SOLID PROBLEMS EXIST. FOR A THOROUGH TEST, THE NORMAL ITERATION PASS SHOULD BE RUN.

4.1 RESTART PROCEDURE

TO RESTART THE PROGRAM WITHOUT GENERATING THE INITIAL PRINTOUTS PROCEED AS FOLLOWS:

- A: LOAD ADDRESS 000210
- B: PERFORM STEP E OF PREVIOUS PROCEDURE.
- C: PRESS START.

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5: PROGRAM AND/OR OPERATOR ACTION

5.1 NORMAL HALTS

LOC 001656 COMMON HALT. THIS HALT IS CONTAINED IN A SUBROUTINE THAT IS CALLED BY THOSE PARTS OF THE PROGRAM THAT REQUIRE THAT THE PROCESSOR STOP. THIS HALT NORMALLY OCCURS UPON COMPLETION OF NON-ERROR PRINTOUTS. THE CONSOLE DATA LIGHTS DISPLAY THE ADDRESS OF INSTRUCTION THAT GENERATED THE HALT REQUEST.

LOC 001330 ROUTINE END HALT. THIS HALT OCCURS UPON COMPLETION OF THE CURRENT TEST ROUTINE IF SA10 IS SET. THE CONSOLE DATA LIGHTS DISPLAY THE NUMBER OF THE TEST JUST COMPLETED.

5.2 NORMAL PRINTOUTS

ALL NON-ERROR PRINTOUTS ARE NORMAL PRINTOUTS. INSTRUCTION, TITLE, AND USER ERROR PRINTOUTS ARE NORMAL PRINTOUTS.

6: ERRORS

ERRORS ARE REPORTED IN THIS PROGRAM BY THE FOLLOWING METHODS:

- A: UNCONDITIONAL ERROR HALTS, OR
- B: ERROR PRINTOUT FOLLOWED BY OPTIONAL ERROR HALT.

6.1 UNCONDITIONAL ERROR HALTS

AN UNCONDITIONAL ERROR HALT WILL OCCUR AT THE ADDRESSES LISTED BELOW IF THROUGH HARDWARE OR SOFTWARE FAILURE, PROGRAM CONTROL IS TRANSFERRED TO AN UNEXPECTED AREA BETWEEN 000000 AND 000376.

000002 RESERVED AREA  
000006 ERROR TRAP  
000012 RESERVED INSTRUCTION TRAP  
000016 DEBUG TRAP  
000022 IOT TRAP  
000026 POWER FAIL TRAP  
000040 THROUGH 000376 - SYSTEM SOFTWARE AND INTERRUPT VECTOR AREA, EXCEPT FOR UDC11 AND IY VECTORS.

TO FIND OUT WHERE THE PROGRAM WAS AT THE TIME THE FAILURE OCCURRED,

- A: EXAMINE CONTENTS OF REGISTER 6; (ADDRESS 177906);
- B: TRANSFER THE CONTENTS OF REG 6 TO THE SR, LOAD ADDRESS AND EXAMINE;
- C: THE DATA SHOWN IN THE DATA LIGHTS IS THE VALUE OF THE PC WHEN THE FAILURE OCCURRED.
- D: LOCATE IN PROGRAM LISTING THE DISPLAYED PC VALUE.

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6.1 CONT'D)

E. THE INSTRUCTION THAT IMMEDIATELY PRECEDES THE ONE REFERENCED BY THE DISPLAYED PC VALUE IS THE INSTRUCTION THAT WAS/WAS BEING EXECUTED WHEN THE FAILURE OCCURRED.

AN UNCONDITIONAL ERROR HALT FAILURE IS AN ABNORMAL CONDITION INDICATING A HARDWARE FAILURE, OR MOST UNLIKELY, A PROGRAM FAILURE. THIS PROGRAM ASSUMES THAT THE PROCESSOR IS IN OPERATING CONDITION IN ORDER TO PERFORM ITS TESTS. ANY FURTHER STEPS REQUIRED TO DIAGNOSE AN UNCONDITIONAL ERROR HALT ARE NOT WITHIN THE SCOPE OF THIS PROGRAM.

6.2 ERROR PRINTOUTS

ERROR PRINTOUTS ARE GENERATED BY THE "ERRN" SUBROUTINE. THE "ERRN" SUBROUTINE IS CALLED BY AN "ERRORN" STATEMENT IN THE PROGRAM LISTING. AN ERROR PRINTOUT LOOKS AS FOLLOWS:

TXXX PC=YYYYY ICNT=ZZZZ. ADDITIONAL ERROR INFORMATION

WHERE:

TXXX IS THE NUMBER OF FAILING ROUTINE (OCTAL).

PC=YYYYY IS THE ADDRESS OF ERROR CALL.

ICNT=ZZZZ. IS THE ITERATION COUNT AT TIME OF FAILURE.

THE ADDITIONAL ERROR INFORMATION FURTHER DESCRIBES THE ERROR. THIS WILL USUALLY BE THE CONTROL AND STATUS REGISTERS.

UDCR=XXXXXX UDSR=XXXXXX

AFTER THE PRINTOUT IS COMPLETED, THE PROGRAM WILL HALT AT COMMON ERROR HALT AT LOC 882442 IF SR19 IS SET.

WHEN AN ERROR PRINTOUT OCCURS:

- A. LOOK UP THE ADDRESS REFERENCED BY PC=YYYYY IN THE LISTING.
- B. OPPOSITE THE PC VALUE IN "ERROR" STATEMENT WILL BE FOUND, AND IN THE COMMENTS SECTION, A DESCRIPTION OF THE ERROR.
- C. AT THE BEGINNING OF THE TEST ROUTINE A DESCRIPTION OF THE TEST WILL BE FOUND.

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7. MISCELLANEOUS

7.I SR OPTIONS

THE STANDARD SR OPTIONS ARE DESCRIBED HERE:

SR15 HALT ON ERROR: WITH SR15 SET TO A I, THE PROGRAM WILL HALT AFTER AN ERROR OCCURS; PRESSING CONT WILL CAUSE PROGRAM TO RESUME OPERATION.

SR14 SCOPE: THIS OPTION CAUSES THE PROGRAM TO REMAIN IN THE CURRENT TEST ROUTINE; WHEN THE OPTION IS REMOVED, THE PROGRAM WILL COMPLETE THE CURRENT ROUTINE, AND WILL THEN GO ON TO THE NEXT ROUTINE.

SR13 INHIBIT ERROR PRINTOUT: THIS OPTION IF SET, WILL REMOVE ALL ERROR PRINTOUTS.

\*\*\*\*\*NDTE\*\*\*\*\*

SCOPE MODE OPERATION IS ACHIEVED BY LOCKING THE PROGRAM IN THE CURRENT ROUTINE, INHIBITING ERROR PRINTOUTS, AND BYPASSING ERROR HALTS.

SR11 INHIBIT ITERATION: SETTING THIS OPTION WILL CAUSE THE PROGRAM TO EXECUTE EACH TEST ONLY ONCE, INSTEAD OF THE NORMAL NUMBER OF ITERATIONS SELECTED FOR EACH TEST. TWO POSSIBLE USES OF THIS OPTION ARE:

- A. QUICK PASS: EACH TEST IS RUN ONLY ONCE.
- B. TO SKIP OVER A FAILING ROUTINE.

SR10 HALT AT END OF CURRENT ROUTINE: WITH THE OPTION SET, THE PROGRAM WILL HALT AT THE END OF EACH TEST, AND DISPLAY IN DATA LIGHTS THE NUMBER OF THE TEST JUST COMPLETED. THREE POSSIBLE USES OF THIS OPTION ARE:

- A. TO STEP THROUGH THE PROGRAM ONE ROUTINE AT A TIME.
- B. WHEN THE PROGRAM HAS BEEN RUNNING FOR A WHILE, TO FIND OUT HOW FAR IT HAS PROGRESSED.
- C. IN CASE OF A BLOW UP, ETC., TO STEP THROUGH ONE TEST AT A TIME UNTIL THE FAILURE REOCCURS; THE ROUTINE FOLLOWING THE PREVIOUSLY COMPLETED ROUTINE WOULD BE THE FAILING ROUTINE.

SR9 SELECT ROUTINE: WITH SR9 SET, THE PROGRAM WILL GO AND EXECUTE THE ROUTINE INDICATED BY SR7 THROUGH SR8, AFTER THE CURRENT ROUTINE HAS BEEN COMPLETED. IF THE OPTION IS REMOVED, THE PROGRAM WILL PROCEED TO EXECUTE THE ROUTINES FOLLOWING THE SELECTED ROUTINE.

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7.2 TESTING UDC11 AT NON-STANDARD ADDRESSES AND/OR VECTORS

THIS PROGRAM CAN TEST THE UDC11 AT NON-STANDARD ADDRESSES AND VECTORS PROVIDED THOSE ADDRESSES AND VECTORS ARE PROVIDED TO THE PROGRAM AS FOLLOWS:

- A: AFTER LOADING PROGRAM REFER TO PROGRAM LISTING AND CHANGE LOCATIONS 001210 THROUGH 001244 TO REFLECT THE NEW UDC11 ADDRESSES AND VECTORS.
- B: IF THE TELETYPE IS ALSO AT NON STANDARD ADDRESSES, CHANGE LOCATIONS 001200 THRU 001206 ALSO.
- C: PROCEED TO USE THE PROGRAM, OR
- D: USING STANDARD DUMP ROUTINES, DUMP OUT THE ENTIRE PROGRAM IN ABSOLUTE FORMAT TO HAVE AN OBJECT TAPE THAT REFLECTS YOUR SYSTEM, OR
- E: DUMP OUT ONLY LOCATIONS 001210 THROUGH 001244 IN ABSOLUTE FORMAT, AND LOAD IT ALSO AFTER LOADING THE MAIN PROGRAM.

8: DESCRIPTION

THIS PROGRAM IS ORGANIZED INTO THREE MAIN SECTIONS:

- A: CONTROL ROUTINE,
- B: TEST ROUTINES,
- C: COMMON SUBROUTINES

8.1 CONTROL ROUTINE

THE CONTROL ROUTINE ASSUMES CONTROL WHEN THE PROGRAM IS STARTED. IT HAS THE FOLLOWING FUNCTIONS:

- A: CONTROL'S SEQUENCE OF TEST ROUTINES,
- B: MONORS AND ACTS ON SR OPTIONS.

THE CONTROL ROUTINE IS CALLED FROM A TEST ROUTINE BY THE "SCOPE" STATEMENT.



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0.2 TEST ROUTINES

THE ACTUAL TESTING IS PERFORMED BY A SET OF TEST ROUTINES THAT ARE NUMBERED SEQUENTIALLY FROM 0 TO 100 (OCTAL). EACH TEST ROUTINE IS PRECEDED BY A TEST HEADER THAT IS USED BY THE CONTROL ROUTINE IN ORDER TO PROPERLY SEQUENCE THROUGH THE TESTS. THE HEADER LOOKS AS FOLLOWS: (EXAMPLE)

```

.....
T201  20          (ROUTINE NUMBER 20)
      T21          (ADDRESS OF NEXT ROUTINE)
      100.        (TEST ITERATION COUNT)
      BAGA        (SCOPE ENTRY POINT)
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THE FIRST 2 ITEMS ARE SELF EXPLANATORY. THE TEST ITERATION COUNT INDICATES TO THE CONTROL ROUTINE THE NUMBER OF TIMES THE TEST SHOULD BE PERFORMED BEFORE GOING ON TO THE NEXT ROUTINE.

THE SCOPE ENTRY POINT INDICATES TO THE CONTROL ROUTINE THE ADDRESS IT SHOULD RETURN TO AFTER THE FIRST ITERATION. THE ADDRESS MAY NOT NECESSARILY POINT TO THE FIRST INSTRUCTION OF THE TEST.

0.3 COMMON SUBROUTINES

ALL SUBROUTINES NEEDED BY EITHER THE CONTROL ROUTINE OR TEST ROUTINES ARE GROUPED TOGETHER. THE MOST SIGNIFICANT SUBROUTINE IS THE "ERRR" SUBROUTINE, WHICH IS CALLED BY AN "ERRORR" STATEMENT AND TYPES THE TEST NUMBER AND PC VALUE WHEN A FAILURE OCCURS.

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100000  
  
000412  
000402  
000424  
000404  
001412  
003412  
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003424  
007000

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.ENDR
.TITLE DZUDB=B CONTROL TEST
.ABS

JUDC=1I CONTROL TEST
JMAINDEC=11-DZUDB=B
JCOPYRIGHT 1971, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.
J    REVISED: JAN, 1973
J    ROBERT A. WHITTON
J
JSTANDARD SR SWITCH OPTION (SWITCH SET TO A 1)
J
J
JISR15 = HALT ON ERROR
JISR14 = SCOPE
JISR13 = INHIBIT ERROR PRINTOUT
JISR12 = INHIBIT TRACE
JISR11 = INHIBIT ITERATIONS
JISR10 = HALT AT END OF CURRENT TEST
JISR9 = SELECT ROUTINE SPECIFIED BY SR7 THROUGH SR8
JISR7 THROUGH SR8 = NUMBER OF TEST ROUTINE TO BE SELECTED
JSYMBOL DEFINITIONS
J
JISR BIT DEFINITIONS
JISR0=1
JISR1=2
JISR2=4
JISR3=10
JISR4=20
JISR5=40
JISR6=100
JISR7=200
JISR8=400
JISR9=1000
JISR10=2000
JISR11=4000
JISR12=10000
JISR13=20000
JISR14=40000
JISR15=100000
J
JIC1=BIT11BIT3BIT0      IMINT,DEF INT,DEF SCAN EN
JIC2=BIT11BIT0         IMINT,DEF INT
JIC3=BIT2BIT4BIT0     IMINT,IMM INT, IMM SCAN EN
JIC4=BIT2BIT0         IMINT,IMM INT
JIC5=BITC1BIT0       IC1+STOP X
JIC6=BITC1BIT9BIT10  IC1+STOP X+Y
JIC7=BITC3BIT0       IC3+STOP X
JIC8=BITC3BIT9BIT10  IC3+STOP X+Y
JIC9=BIT9BIT10BIT11  ISTOP X+Y+WD
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629 000000  
630 000040  
631 000100  
632 000140  
633 000200  
634 000240  
635 000300  
636 000340  
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638 177970  
639 177776  
640 000027  
641 000006  
642  
643 009726  
644 022626  
645 009746  
646 024646  
647 000240  
648 000000  
649 177777  
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655 000000 000002  
656 000002 000000  
657 000004 000006  
658 000006 000000  
659 000010 000012  
660 000012 000000  
661 000014 000016  
662 000016 000000  
663 000020 000022  
664 000022 000000  
665 000024 002432  
666 000026 000340  
667 000030 002650  
668 000032 000340  
669 000034 000036  
670 000036 000000

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PRTY0=0  
PRTY1=40  
PRTY2=100  
PRTY3=140  
PRTY4=200  
PRTY5=240  
PRTY6=300  
PRTY7=340  
|  
SR=177970  
PS=177776  
PC=X7  
SP=X6  
|  
POSP=009726  
POSP2=022626  
PUSH=009746  
PUSH2=024646  
NOP=000240  
OPEN=0  
X=1  
EMTX=0  
TLAST=1  
|  
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MA=0  
MA=2  
HALT  
MA=2  
HALT  
MA=2  
HALT  
MA=2  
HALT  
MA=2  
HALT  
MA=2  
HALT  
PWRFLI PWRDN  
EMTVI E:INT  
PRTY7  
TR=2  
HALT

IPRIORITY LEVEL DEFINITIONS

IPROCESSOR REGISTER DEFINITIONS

IPOP STACK, SAME AS TST (6)+  
IPOP STACK TWICE, SAME AS CMP (6)+,(6)+  
IPUSH STACK, SAME AS TST -(6)  
IPUSH STACK TWICE, SAME AS CMP -(6),-(6)

iUNASSIGNED TRAP

iSP OVERFLOW, BUS ERROR TRAP

iRESERVED INSTRUCTION TRAP

iTRACE TRAP

iTRAP TO CALL IOX

iPOWER FAIL TRAP

iEMT TRAP

iTRAP TRAP

672				
676	000040	000042	.+2	
(1)	000042	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000044	000046	.+2	
(1)	000046	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000050	000052	.+2	
(1)	000052	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000054	000056	.+2	
(1)	000056	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000060	000062	.+2	
(1)	000062	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000064	000066	.+2	
(1)	000066	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000070	000072	.+2	
(1)	000072	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000074	000076	.+2	
(1)	000076	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000100	000102	.+2	
(1)	000102	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000104	000106	.+2	
(1)	000106	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000110	000112	.+2	
(1)	000112	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000114	000116	.+2	
(1)	000116	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000120	000122	.+2	
(1)	000122	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000124	000126	.+2	
(1)	000126	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000130	000132	.+2	
(1)	000132	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000134	000136	.+2	
(1)	000136	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000140	000142	.+2	
(1)	000142	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000144	000146	.+2	
(1)	000146	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000150	000152	.+2	
(1)	000152	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000154	000156	.+2	
(1)	000156	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000160	000162	.+2	
(1)	000162	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000164	000166	.+2	
(1)	000166	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000170	000172	.+2	
(1)	000172	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000174	000176	.+2	
(1)	000176	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000200	000202	.+2	
(1)	000202	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000204	000206	.+2	
(1)	000206	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000210	000212	.+2	

(1)	000212	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000214	000216	:+2	
(1)	000216	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000220	000222	:+2	
(1)	000222	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000224	000226	:+2	
(1)	000226	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000230	000232	:+2	
(1)	000232	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000234	000236	:+2	
(1)	000236	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000240	000242	:+2	
(1)	000242	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000244	000246	:+2	
(1)	000246	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000250	000252	:+2	
(1)	000252	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000254	000256	:+2	
(1)	000256	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000260	000262	:+2	
(1)	000262	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000264	000266	:+2	
(1)	000266	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000270	000272	:+2	
(1)	000272	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000274	000276	:+2	
(1)	000276	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000300	000302	:+2	
(1)	000302	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000304	000306	:+2	
(1)	000306	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000310	000312	:+2	
(1)	000312	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000314	000316	:+2	
(1)	000316	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000320	000322	:+2	
(1)	000322	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000324	000326	:+2	
(1)	000326	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000330	000332	:+2	
(1)	000332	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000334	000336	:+2	
(1)	000336	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000340	000342	:+2	
(1)	000342	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000344	000346	:+2	
(1)	000346	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000350	000352	:+2	
(1)	000352	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000354	000356	:+2	
(1)	000356	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000360	000362	:+2	
(1)	000362	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000364	000366	:+2	

(1)	000366	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000370	000372	.+2	
(1)	000372	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000374	000376	.+2	
(1)	000376	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000400	000402	.+2	
(1)	000402	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000404	000406	.+2	
(1)	000406	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000410	000412	.+2	
(1)	000412	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000414	000416	.+2	
(1)	000416	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000420	000422	.+2	
(1)	000422	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000424	000426	.+2	
(1)	000426	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000430	000432	.+2	
(1)	000432	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000434	000436	.+2	
(1)	000436	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000440	000442	.+2	
(1)	000442	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000444	000446	.+2	
(1)	000446	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000450	000452	.+2	
(1)	000452	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000454	000456	.+2	
(1)	000456	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000460	000462	.+2	
(1)	000462	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000464	000466	.+2	
(1)	000466	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000470	000472	.+2	
(1)	000472	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000474	000476	.+2	
(1)	000476	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000500	000502	.+2	
(1)	000502	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000504	000506	.+2	
(1)	000506	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000510	000512	.+2	
(1)	000512	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000514	000516	.+2	
(1)	000516	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000520	000522	.+2	
(1)	000522	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000524	000526	.+2	
(1)	000526	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000530	000532	.+2	
(1)	000532	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000534	000536	.+2	
(1)	000536	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000540	000542	.+2	

(1)	002542	000020	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002544	000546	,+2	
(1)	002546	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002550	000552	,+2	
(1)	002552	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002554	000556	,+2	
(1)	002556	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002560	000562	,+2	
(1)	002562	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002564	000566	,+2	
(1)	002566	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002570	000572	,+2	
(1)	002572	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002574	000576	,+2	
(1)	002576	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002600	000602	,+2	
(1)	002602	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002604	000606	,+2	
(1)	002606	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002610	000612	,+2	
(1)	002612	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002614	000616	,+2	
(1)	002616	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002620	000622	,+2	
(1)	002622	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002624	000626	,+2	
(1)	002626	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002630	000632	,+2	
(1)	002632	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002634	000636	,+2	
(1)	002636	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002640	000642	,+2	
(1)	002642	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002644	000646	,+2	
(1)	002646	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002650	000652	,+2	
(1)	002652	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002654	000656	,+2	
(1)	002656	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002660	000662	,+2	
(1)	002662	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002664	000666	,+2	
(1)	002666	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002670	000672	,+2	
(1)	002672	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002674	000676	,+2	
(1)	002676	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002700	000702	,+2	
(1)	002702	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002704	000706	,+2	
(1)	002706	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002710	000712	,+2	
(1)	002712	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	002714	000716	,+2	

(1)	000716	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000720	000722	,+2	
(1)	000722	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000724	000726	,+2	
(1)	000726	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000730	000732	,+2	
(1)	000732	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000734	000736	,+2	
(1)	000736	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000740	000742	,+2	
(1)	000742	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000744	000746	,+2	
(1)	000746	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000750	000752	,+2	
(1)	000752	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000754	000756	,+2	
(1)	000756	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000760	000762	,+2	
(1)	000762	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000764	000766	,+2	
(1)	000766	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000770	000772	,+2	
(1)	000772	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS
(1)	000774	000776	,+2	
(1)	000776	000000	HALT	ITRAPPED TO PREVIOUS ADDRESS



678		000200			.0200		
679	000200	000167	001044		JMP	START	IGO TO START OF PROGRAM
680							
681		000204			.0204		
682	000204	000167	002256		JMP	PHRTST	IPOWER FAIL TEST
683							
684		000210			.0210		
685	000210	000167	001064		JMP	GETRDY	IBYPASS INITIAL TYPEOUTS
686		000000			R0=X0		



699 001214 171774  
700 001216 000234  
701 001220 000236  
702 001222 171772  
703 001224 171770  
704 001226 171000  
705 001230 171002  
706 001232 171004  
707 001234 171010  
708 001236 171020  
709 001240 171040  
710 001242 171100  
711 001244 171200  
712 001246 171400

UDSRI 171774  
UTVI 234  
UPLI 236  
MCLKI 171772  
UMODI 171770  
UDCA1I 171000  
UDCA2I 171002  
UDCA3I 171004  
UDCA4I 171010  
UDCA5I 171020  
UDCA6I 171040  
UDCA7I 171100  
UDCA8I 171200  
UDCA9I 171400

IUBCI1 SCAN REGISTER  
IUBCI1 TRAP VECTOR  
IUBCI1 PRIORITY LEVEL  
IUBCI1 MAINTENANCE CLOCK  
IUBCI1 RESERVED MODULE ADDRESS  
IUBCI1 RESERVED MODULE ADDRESS, CLASS 00?  
ICLASS 002  
ICLASS 004  
ICLASS 010  
ICLASS 020  
ICLASS 040  
ICLASS 100  
ICLASS 200  
ICLASS 400

714											
715											
716											
717	001250	012706	001100								
718	001254	009067	002650								
719	001260	104000									
720	001262	003376									
721	001264	009737	000042								
722	001270	001003									
723	001272	104000									
724	001274	003264									
725	001276	104003									
726	001300	012767	004142	002624	GETRDYi	MOV	070,NXTST				
727	001306	012767	000006	176470	GTADYXi	MOV	06,MACHER				
728	001314	012767	000340	176454		MOV	0PRTY7,PS				
729	001322	016777	177672	177666		MOV	UPL,OUTV				
730	001330	009077	177664			CLR	0UPL				
731	001334	012706	001100			MOV	0100,SP				
732	001340	104004				SRESET					
733	001342	002767	000236		GTADYAi	JSR	PC,FORWD				
734	001346	032767	001000	176214		BIT	0019,SR				
735	001354	001002				BNE	GTADYC				
736	001356	000177	002552			JMP	0CURTST				
737	001362	016700	176202		GTADYCi	MOV	SR,X0				
738	001366	042700	177400			BIC	0177400,X0				
739	001372	126700	002532			CMPB	RTNNO,X0				
740	001376	001002				BNE	GTADYD				
741	001400	000177	002530			JMP	0CURTST				
742	001404	022767	177777	002520	GTADYDi	CMF	0-I,NXTST				
743	001412	001353				BNE	GTADYA				
744	001414	104000				TYPE					
745	001416	003356				MINCR?					
746	001420	104003				CHALT					
747	001422	000726				BR	GETRDY				

```

|
| START OF TEST CONTROLLER
|
| STARTI  MOV  0100,SP      ISET BOTTOM OF SP STACK
|          CLR  RTNNO
|          TYPE
|          MTTT
|          TST  0042      IMONITOR LOAD
|          BNE  GETRDY    IYES, SKIP NEXT MESSAGE
|          TYPE
|          MSETSR
|          CHALT
|          MOV  070,NXTST  IADDRESS OF FIRST ROUTINE
|          MOV  06,MACHER  IRESET MACHER TRAP
|          MOV  0PRTY7,PS  ISET PRIORITY 7
|          MOV  UPL,OUTV   IRESET TRAP
|          CLR  0UPL
|          MOV  0100,SP   ISET BOTTOM OF STACK
|          SRESET
|          JSR  PC,FORWD   IISSUE RESET
|          BIT  0019,SR   IROLL FORWARD TO NEXT ROUTINE
|          BNE  GTADYC    ICHECK SELECT ROUTINE SWITCH SET
|          JMP  0CURTST   IBRANCH IF SELECT ROUTINE SWITCH SET
|          MOV  SR,X0     IGO RUN CURRENT ROUTINE
|          BIC  0177400,X0 IGET (SR)
|          CMPB RTNNO,X0  IMASK UNDESIRED BITS
|          BNE  GTADYD    ICOMPARE RTNNO TO (RB)
|          JMP  0CURTST   IBRANCH IF ROUTINE NOT FOUND YET
|          CMF  0-I,NXTST IGO RUN ROUTINE
|          BNE  GTADYA    INO, CHECK FOR LAST ROUTINE
|          TYPE          IBRANCH IF NOT LAST ROUTINE
|          MINCR?       ITYPE INCORRECT RTN SELECTED
|          CHALT
|          BR   GETRDY   ICOMMON HALT
|                          ISTART OVER

```

```

749
750
751
752 001424 012767 000340 177444 CHAINNI MOV @PRTY7,1076
753 001432 009077 177554 CLR @UDCR
754 001436 016767 002464 177430 MOV SCOPTR,1076
755 001444 012706 001074 MOV @1074,SP
756 001450 009267 002450 INC ICNT ;INCREMENT ICNT
757 001454 001002 BNE CHNAC ;BR IF RESULT NOT 0
758 001456 009167 002442 COM ICNT ;RESET ICNT TO -1
759 001462 032767 040000 176100 CHNACI BIT @BIT14,SR ;CHECK FOR SCOPE OPTION
760 001470 001403 BEQ CHNA ;BRANCH IF SCOPE SWR NOT SET
761 001472 016716 002430 CHNABI MOV SCOPTR,(SP) ;SET UP RETURN TO ROUTINE
762 001476 000002 RTI
763
764 001500 032767 004000 176062 CHNAI BIT @BIT11,SR ;TEST INHIBIT ITERATION SWITCH
765 001506 001003 BNE CHNAA ;BRANCH IF INHIBIT ITERATION SW SET
766 001510 009367 002406 DEC ICTR ;DECREMENT ITERATION COUNT
767 001514 001366 BNE CHNAB ;BRANCH IF COUNT NOT 0
768 001516 022626 CHNAAI POPSP2 ;POP STACK POINTER TWICE
769 001520 032767 002000 176042 BIT @BIT10,SR ;IS ROUTINE END HALT SW SET?
770 001526 001403 BEQ CHNB ;BRANCH IF NOT SET
771 001530 016700 002374 MOV RTNNO,X0 ;ROUTINE END HALT, TEST @IN LIGHTS
772 001534 000000 HALT ;CHECK SELECT ROUTINE SWITCH
773 001536 032767 001000 176024 CHNBI BIT @BIT9,SR ;BRANCH IF SELECT RTN SW SET
774 001544 001295 BNE GETRDY ;LIST TEST ?
775 001546 022767 177777 002356 CMP @-1,NXTST ;BRANCH IF NOT LAST TEST
776 001554 001294 BNE GETRDY ;TYPE PROGRAM END BELL
777 001556 104000 TYPE
778 001560 004051 MPBEND
779 001562 013705 000042 MOV @042,X9 ;LINK TO MONITOR
780 001566 001644 BEQ GETRDY ;NO, REPEAT PROGRAM
781 001570 000005 RESET
782 001572 004715 LOGICI JSR X7,(5)
783 001574 000240 NOP
784 001576 000240 NOP
785 001600 000240 NOP
786 001602 000636 BR GETRDY ;GO REPEAT PROGRAM
787
788 ;TEST CONTROLLER
789
790 001604 016705 002322 FORWARDI MOV NXTST,X5 ;ADDRESS OF NEXT ROUTINE
791 001610 012567 002314 MOV (5)+,RTNNO ;GET NEXT ROUTINE NUMBER
792 001614 012567 002312 MOV (5)+,NXTST ;GET ADDRESS ON NEXT "NEXT" ROUTINE
793 001620 012567 002276 MOV (5)+,ICTR ;GET ITERATION COUNT
794 001624 012567 002276 MOV (5)+,SCOPTR ;GET SCOPE LOOP ENTRY POINTER
795 001630 010567 002300 MOV X9,CURTST ;ADDR OF NOW CURRENT TEST TO CURTST
796 001634 012767 000001 002262 MOV @1,ICNT ;PRESET ICNT TO 1
797 001642 000207 RTS PC

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799
800          | ERROR HANDLER
801          |
802 001644 017767 177342 002264 ERRSTI MOV  @UDCR,UDCR?  ISAVE CONTENTS OF UDCR
803 001652 017767 177336 002260      MOV  @UDSR,UDSR?  ISAVE CONTENTS OF UDSR
804 001660 012767 003223 000166      MOV  @MSTR,ERRB
805 001666 009067 000200      CLR  ERRE
806 001672 004567 000240      JSR  %5,OACNV      I CONVERT TO ASCII
807 001676 004136
808 001700 003233      UDCR?
809 001702 000006      MUDCR
810 001704 004567 000226      JSR  %5,OACNV      I CONVERT TO ASCII
811 001710 004140
812 001712 003251      UDSR?
813 001714 000006      MUDSR
814 001716 000421      BR   ERRA=6
815 001720 012767 177777 000126 ERRI  MOV  @=1,ERRB      ISET UP ONE MESSAGE CALL
816 001726 012767 000240 000122      MOV  @240,ERRB+2
817 001734 009067 000132      CLR  ERRE
818 001740 000413      BR   ERRA
819 001742 011667 000106      ERRII MOV  (SP),ERRB     I DEVELOP ADDITIONAL MESSAGE ADDR.
820 001746 017767 000102 000100      MOV  @ERRB,ERRB
821 001754 012767 000002 000110      MOV  @2,ERRE
822 001762 012767 177777 000066      ERRAI MOV  @=1,ERRB+2
823 001770 032767 020000 175572      ERRAI BIT  @BIT13,SR
824 001776 001030      BNE  ERRC
825 002000 011667 000064      MOV  (SP),ERRD     I DEVELOP CALLING ADDR.
826 002004 162767 000002 000056      SUB  @2,ERRD
827 002012 004567 000120      JSR  %5,OACNV      I CONVERT TEST # TO ASCII
828 002016 004130
829 002020 003161      RYNO
830 002022 000003      MNUM
831 002024 004567 000106      JSR  %5,OACNV
832 002030 002070      IGO TO OCTAL TO ASCII CONVERT
833 002032 003174      ERRD      ISOURCE ADDRESS
834 002034 000006      MPC      IDESTINATION ADDRESS
835 002036 004567 000162      JSR  %5,OACNV      I GOF DIGITS TO CONVERT
836 002042 004124      I CONVERT ICNT TO DECIMAL ASCII
837 002044 003212
838 002046 000005
839 002050 104001      TYPES
840 002052 003100      I TYPE#
841 002054 000000      ERRII MOV  @=1,ERRB     I ERROR HEADER
842 002056 177777      ERRII OPEN
843 002060 104017      ERRII OPEN
844 002062 066716 000004      ERRII ADD  ERRE,(SP)  I ADDITIONAL ERROR MESSAGE IF ANY
845 002066 000002
846 002070 000000      ERRII EHALT
847 002072 000000      ERRII ADD  ERRE,(SP)  I GO ERR HALT IF DESIRED

```

```

049
050
051
052 002074 005767 179470
053 002100 100001
054 002102 000000
055 002104 000002
056
057
058
059 002106 104015
060 002110 012567 000016
061 002114 022767 177777 000010
062 002122 001002
063 002124 104014
064 002126 000002
065 002130 104000
066 002132 000000
067 002134 000765

|
| CONDITIONAL ERROR HALT ROUTINE
|
| EHLTI TST SR |CHECK FOR HALT ON ERROR
| BPL EHLTA |BRANCH IF NO HALT DESIRED
| HALT
| EHLTAI RTI

|
| SUBROUTINE TO OUTPUT A SERIES OF ASCII MESSAGES ON TELETYPE PRINTER
|
| TYP5I SAV05S
| MOV (5)+,TYP5B |GET ADDRESS OF MESSAGE TO TYP5B
| CMP #1,TYP5B |CHECK FOR TERMINATOR
| BNE TYP5A |BRANCH IF NOT TERMINATOR
| RST05S
| RTI
| TERMINATOR REACHED, EXIT
| TYP5AI TYPE |CALL ON TYP SUBROUTINE TO TYPE MESSAGE
| TYP5BI OPEN |ADDRESS OF MESSAGE GOES HERE
| BR TYP5+2 |GO PROCESS NEXT MESSAGE

```

```

869
870
871
872 002136 104011
873 002140 013567 000056
874 002144 012501
875 002146 012502
876 002150 060201
877 002152 016703 000044
878 002156 042703 177770
879 002162 062703 000060
880 002166 110341
881 002170 042767 000007 000024
882 002176 006067 000020
883 002202 006067 000014
884 002206 006067 000010
885 002212 003302
886 002214 001356
887 002216 104012
888 002220 000205
889 002222 000000
890
891
892
893 002224 104011
894 002226 012700 002402
895 002232 313501
896 002234 012567 000052
897 002240 012567 000050
898 002244 012702 002370
899 002250 012767 000005 000104
900 002256 012267 000104
901 002262 004767 000034
902 002266 003367 000070
903 002272 001371
904 002274 166700 000014
905 002300 010067 000004
906 002304 004567 000100
907 002310 000000
908 002312 000000
909 002314 000000
910 002316 104012
911 002320 000205

```

```

)
)SUBROUTINE FOR OCTAL TO ASCII CONVERSION
)
OACNVI SAV04
MOV 0(5)+,OACNVX ;GET OCTAL VALUE
MOV (5)+,X1 ;GET DESTINATION ADDRESS
MOV (5)+,X2 ;GET CONVERT COUNT
ADD X2,X1 ;DEVELOP ADDR TO STORE 1ST CHAR.
OACNVAI MOV OACNVX,X3
BIC 0177770,X3 ;ISOLATE LEAST SIGNIFICANT DIGIT
ADD #60,X3 ;CONVERT DIGIT TO ASCII
MOVB X3,-(1) ;STORE ASCII CHARACTER
BIC #7,OACNVX
ROR OACNVX
ROR OACNVX
ROR OACNVX
DEC X2 ;DONE ALL DIGITS?
BNE OACNVA ;BRANCH IF NOT DONE
RST04
RTS X5 ;DONE, EXIT
OACNVXI OPEN
)
)SUBROUTINE FOR BINARY TO DECIMAL ASCII CONVERSION
)
BDCNVI SAV04
MOV #DECVAL,X0 ;SAVE REGS
MOV 0(5)+,X1 ;SET UP ADDR TO STORE DECIMAL ASCII
MOV (5)+,BDCNVC ;BINARY VALUE TO R1
MOV (5)+,BDCNV0 ;DESTINATION ADDR TO BDCNV0
MOV #ADTENP,X2 ;CHARACTER COUNT TO BDCNV0
MOV #5,CNVCTR ;ADDR OF TEN POWER STRING
BDCNVAI MOV (2)+,TENPWR ;SET UP FOR 9 POWER CONVERSIONS
JSR PC,SUBTEN ;MOVE POWER OF TEN VALUE
DEC CNVCTR ;PERFORM CONVERSION
BNE BDCNVA ;DONE 9 CONVERSIONS
SUB BDCNV0,X0 ;BRANCH IF NOT YES
MOV X0,BDCNV0
JSR X5,BMOVE
BDCNVBI OPEN
BDCNVCi OPEN
BDCNVDi OPEN
RST04
RTS X5 ;RESTORE REGS AND EXIT

```



```

913
914 002322 009067 000036      SUBTENI CLR      DIGIT
915 002326 166701 000034      SUBTNAI SUB      TENPWR,X1      ;SUBTRACT TEN POWER FROM BINARY VALUE
916 002332 103403          BCS      SUBTND      ;BRANCH IF UNSUCCESSFUL SUBTRACTION
917 002334 009267 000024          INC      DIGIT
918 002340 000772          BR       SUBTNA
919 002342 066701 000020      SUBTNDI ADD      TENPWR,X1      ;RESTORE SUBTRACTED VALUE.
920 002346 062767 000060 000010      ADD      #60,DIGIT      ;CONVERT (DIGIT) TO ASCII
921 002354 116720 000004          MOVB    DIGIT,(0)+      ;MOVE ASCII CHAR TO DECVAL FIELD
922 002360 000207          RTS     PC              ;EXIT
923 002362 000000      CNVCTRI OPEN
924 002364 000000      DIGITI  OPEN
925 002366 000000      TENPWR; OPEN
926 002370 023420      ADTENPI 10000.
927 002372 001750      1000.
928 002374 000144      100.
929 002376 000012      10.
930 002400 000001      1.
931 002402      040      040 040 040 040 040 040 040 040 040 040
931 002405      040      040 040
932
933      ;SUBROUTINE TO MOVE A VARIABLE NUMBER OF BYTES
934
935 002410 104011      BMOVEI  SAV04          ;SAVE REGS
936 002412 012501          MOV      (5)+,X1      ;GET FROM ADDRESS
937 002414 012502          MOV      (9)+,X2      ;GET TO ADDRESS
938 002416 012503          MOV      (9)+,X3      ;GET COUNT
939 002420 112122      BMOVAI  MOVB    (1)+,(2)+ ;MOVE BYTE
940 002422 005303          DEC      X3           ;DECREMENT COUNT
941 002424 001375          BNE     BMOVA        ;BRANCH IF NOT DONE
942 002426 104012      RST04          ;RESTORE REGS AND EXIT
943 002430 000205          RTS     X5
944
945      ;UNEXPECTED POWER FAIL SERVICE
946
947 002432 012767 002442 175364      PHRDNI  MOV      @PHRUP,PHRPL ;SET UP FOR POWER UP
948 002440 000000          HALT
949 002442 012706 001100      PHRUPI  MOV      @100,SP      ;RESTORE STACK POINTER
950 002446 012767 002432 175350      MOV      @PHRDN,PHRPL    ;SET UP FOR POWER DOWN
951 002454 000005          RESET
952 002456 104000          TYPE      ;TYPE RECOVERY MESSAGE
953 002460 003532          MPWRP
954 002462 000167 176612      JMP     GETRDYX        ;GO TO NEXT TEST

```

```

956
957      | POWER FAIL TEST
958      |
959 002466 012706 001100      | PHRTSTi MOV    @1100,SP      | ISET UP SP AND STATUS
960 002472 012767 002566 175324 |          MOV    @PWRDT,PWRPL | ISET UP FOR POWER DOWN
961 002500 012777 002620 176510 |          MOV    @PWFDC,OUTV
962 002506 012777 000300 176504 |          MOV    @PRTY0,OUPL
963 002514 104000 |          TYPE
964 002516 003453 |          MPWRT
965 002520 012706 001100      | PHUDCi MOV    @1100,SP
966 002524 012777 000036 176460 |          MOV    @J6,UDCR      | ISET UP UDC CONTROL
967 002532 012767 000000 175236 |          MOV    @PRTY0,PS
968 002540 032777 040000 176444 | PHUDCAi BIT    @BIT14,UDCR   | ITEST POWER FAIL BIT
969 002546 001774 |          BEQ    PHUDCA       | IBRANCH IF CLEAR
970 002550 000240 |          NOP
971 002552 000240 |          NOP
972 002554 104000 |          TYPE
973 002556 003571 |          MPUDC              | IERRCR; POWER FAIL BIT SET + NO TRAP
974 002560 000001 |          WAIT
975 002562 000005 |          RESET
976 002564 000755 |          BR
977 002566 012767 002576 175230 | PHADTi MOV    @PWRDT,PWRPL      | ISET UP FOR POWER UP
978 002574 000000 |          HALT
979 002576 012767 002566 175220 | PHAUTi MOV    @PWRDT,PWRPL
980 002604 012706 001100      |          MOV    @1100,SP
981 002610 000005 |          RESET
982 002612 104000 |          TYPE
983 002614 003532 |          MPWRF
984 002616 000740 |          BR
985 002620 032777 040000 176364 | PWFDCi BIT    @BIT14,UDCR   |
986 002626 001404 |          BEQ    PWFDCX
987 002630 104000 |          TYPE
988 002632 003645 |          MPUOK
989 002634 000005 |          RESET
990 002636 000730 |          BR    PHUDC
991 002640 104000 | PHUDCi TYPE
992 002642 003721 |          MPUONG
993 002644 000005 |          RESET
994 002646 000724 |          BR    PHUDC

```

```

996
997
998
999 002650 011646
1000 002652 162716 000002
1001 002656 017616 000000
1002 002662 121667 001232
1003 002666 101402
1004 002670 000000
1005 002672 000776
1006 002674 006116
1007 002676 042716 177001
1008 002702 062716 004060
1009 002706 017616 000000
1010 002712 000136
1011
1012
1013
1014 002714 102015
1015 002716 010500
1016 002720 009740
1017 002722 000000
1018 002724 104014
1019 002726 000002
1020
1021
1022
1023 002730 104013
1024 002732 012700 052925
1025 002736 009100
1026 002740 010067 177770
1027 002744 000005
1028 002746 104016
1029 002750 000002
1030
1031
1032
1033 002752 104015
1034 002754 012500
1035 002756 012701 177742
1036 002762 062701 000300
1037 002766 009301
1038 002770 001376
1039 002772 009300
1040 002774 001372
1041 002776 104014
1042 003000 000002

;
;EMT HANDLER
;
;EMTINTI MOV (SP),-(SP) ;GET SAVED PC
; SUB #2,(SP) ;DECREMENT PC BY 2
; MOV @SP,(SP)
; CMPB (SP),EMTLIM ;CHECK IF CALL WITHIN LIMITS
; BLOS EMTA ;CALL IS NOT WITHIN LIMITS
; HALT
; BR ,=2
; EMTAI ROL (SP) ;EMT ARG X 2
; BIC #177001,(SP) ;REMOVE 7 MSB
; ADD @EMTTAB,(SP) ;FORM EMT RTN ADDRESS
; MOV @SP,(SP)
; JMP @SP+

;
;SUBROUTINE FOR COMMON HALTS
;
;CHLTI SAV09S
; MOV X5,X0 ;DEVELOP ADDRESS OF CALLER
; TST -(0)
; HALT ;HALT, ADDRESS OF CALL INSTRUCTION
; RST09S
; RTI ;IN DATA LIGHTS

;
;SUBROUTINE TO ISSUE RESET
;
;SRSETTI SAV09S
; MOV #52925,X0 ;DATA TO R0
; COM X0
; MOV X0,SRSETT+2
; RESET ;ISSUE RESET, R0 IS DISPLAYED
; RST09S
; RTI

;
;SUBROUTINE TO DELAY A SPECIFIED NUMBER OF MILLISECONDS
;
;DL9I SAV09S
; MOV (5)+,X0 ;DELAY COUNTER TO R0
; MOV #36,X1 ;CONSTANT FOR TRAP TIME
; DL9AI ADD #300,X1 ;1 MSEC COUNT TO R1
; DL9BI DEC X1 ;DECREMENT 1 MSEC COUNT
; BNE DLYB ;BRANCH IF NOT 0
; DEC X0 ;DECREMENT IT
; BNE DLYA ;BRANCH IF NOT DONE DELAYING
; RST09S
; RTI ;EXIT

```

```

1044
1045
1046
1047 003002 012666 177764
1048 003006 012666 177764
1049 003012 012767 000002 000046
1050 003020 000414
1051
1052
1053
1054 003022 012767 000240 000036
1055 003030 000403
1056
1057
1058
1059 003032 012767 000002 000026
1060 003040 012666 177762
1061 003044 012666 177762
1062 003050 010546
1063 003052 010446
1064 003054 010346
1065 003056 010246
1066 003060 010146
1067 003062 010046
1068 003064 024646
1069 003066 000002
1070 003070 016605 000020
1071 003074 000002
1072
1073
1074
1075 003076 022626
1076 003100 012600
1077 003102 012601
1078 003104 012602
1079 003106 012603
1080 003110 012604
1081 003112 016646 177764
1082 003116 016646 177764
1083 003122 000002
1084
1085 003124 010566 000020
1086
1087
1088
1089 003130 022626
1090 003132 012600
1091 003134 012601
1092 003136 012602
1093 003140 012603
1094 003142 012604
1095 003144 012605
1096 003146 016646 177762
1097 003152 016646 177762

|
| SUBROUTINE TO SAVE REGS 0-4
|
SV04I  MOV      (SP)+,-12,(SP)  I MOVE PC+PS UP STACK
      MOV      (SP)+,-12,(SP)
      MOV      #RTI,SV05C
      BR       SV05B

|
| SUBROUTINE TO SAVE REGS 0-5 AND PLACE EMT PC IN R5
|
SV05SI MOV      #NOP,SV05C
      BR       SV05A

|
| SUBROUTINE TO SAVE REGS 0-5
|
SV05I  MOV      #RTI,SV05C      I MOVE PC+PS UP STACK
SV05AI MOV      (SP)+,-14,(SP)
      MOV      (SP)+,-14,(SP)
      MOV      X5,-(SP)
SV05BI MOV      X4,-(SP)
      MOV      X3,-(SP)
      MOV      X2,-(SP)
      MOV      X1,-(SP)
      MOV      X0,-(SP)
      PUSH2
SV05CI RTI
      MOV      16,(SP),X5      I RTI OR NOP
      RTI                      I EMT PC TO R5

|
| SUBROUTINE TO RESTORE REGS 0-4
|
RS04I  POPSP2
      MOV      (SP)+,X0
      MOV      (SP)+,X1
      MOV      (SP)+,X2
      MOV      (SP)+,X3
      MOV      (SP)+,X4
      MOV      -12,(SP),-(SP)  I MOVE PC+PS DOWN STACK
      MOV      -12,(SP),-(SP)
      RTI

|
RS05SI MOV      X5,16,(SP)      I SET EMT PC TO R5

|
| SUBROUTINE TO RESTORE REGS 0-5
|
RS05I  POPSP2
      MOV      (SP)+,X0
      MOV      (SP)+,X1
      MOV      (SP)+,X2
      MOV      (SP)+,X3
      MOV      (SP)+,X4
      MOV      (SP)+,X5
      MOV      -14,(SP),-(SP)  I MOVE PC+PS DOWN STACK
      MOV      -14,(SP),-(SP)

```

```

1098 003156 000002 RTI
1099
1100 I ASCII MESSAGES
1101 I
1102 003160 124 MEOI ,ASCII /T/
1103 003161 040 020040 020040 MNUMI ,ASCII / PC= /
003166 020040 041520 020075
1104 003174 020040 020040 020040 MPDI ,ASCII / IENT= /
003202 020040 041511 052116
003210 020075
1105 003212 020040 020040 027040 MIENTI ,ASCIZ / ;/ <19><12>
003220 009015 000
1106 003223 040 052440 041504 MSRI ,ASCII / UDCR= /
003230 036522 040
1107 003233 040 020040 020040 MUOCRI ,ASCII / UDSR= /
003240 020040 052440 051504
003246 036522 040
1108 003251 040 020040 020040 MUOSRI ,ASCIZ / / <19><12>
003256 020040 006440 000012
1109 003264 042523 020124 051123 MSETSR I ,ASCII / SET SR OPTIONS. NORMAL SR = 000000. /
003272 047440 052120 047511
003300 051516 020056 047516
003306 046522 046101 051440
003314 020122 020075 030060
003322 030060 030060 054
1110 003327 040 044124 047105 ,ASCIZ / THEN PRESS CONTINUE/ <19><12>
003334 050040 042522 051523
003342 041440 047117 044524
003350 052516 006505 000012
1111 003356 047111 040526 044514 MINCRTI ,ASCIZ / INVALID TEST/ <19><12>
003364 020104 042524 052123
003372 006456 000012
1112 003376 009015 042125 026503 MTTI ,ASCIZ <19><12> / UDC=11 CONTROL TEST = MAINDEC=11=0ZUDB-A/ <19><12>
003404 030461 041440 047117
003412 051124 046117 052040
003420 051505 020124 020055
003426 040515 047111 042504
003434 026503 030461 042055
003442 052532 041104 040455
003450 009015 000
1113 003453 015 050012 053517 MPURTI ,ASCIZ <19><12> / POWER FAIL TEST: WAITING FOR POWER FAILURE/ <19><12>
003460 051105 043040 044501
003466 020114 042524 052123
003474 020073 040527 052111
003502 047111 020107 047506
003510 020122 047520 042527
003516 020122 040506 046111
003524 051125 006505 000012
1114 003532 042522 047503 042526 MPURFI ,ASCIZ / RECOVERED FROM POWER FAILURE/ <19><12>
003540 042522 020104 051106
003546 046517 050040 053517
003554 051105 043040 044501
003562 052514 042522 009015
003570 000

```

```
1115 003571      125 041504 050040 MPUDCI ,ASCIZ 'UDC POWER FAIL BIT SET, NO TRAP INITIATED'<15><12>
      003576 053517 051105 043040
      003604 044501 020114 044502
      003612 020124 042523 020124
      003620 047040 020117 051124
      003626 050101 044440 044516
      003634 044524 052101 042105
      003642 005015      000
1116 003645      122 041505 053117 MPUDOKI ,ASCIZ 'RECOVERED FROM UDC EXPANDER POWER FAILURE'<15><12>
      003652 051105 042105 043040
      003660 047522 020115 042125
      003666 020103 054105 040520
      003674 042116 051105 050040
      003702 053517 051105 043040
      003710 044501 052514 042522
      003716 005015      000
1117 003721      124 040522 050120 MPUDNGI ,ASCII 'TRAPPED DUE TO UDC EXPANDER POWER FAILURE;'<15><12>
      003726 042105 042040 042525
      003734 052040 020117 042125
      003742 020103 054105 040520
      003750 042116 051105 050040
      003756 053517 051105 043040
      003764 044501 052514 042522
      003772 020054 005015
1118 003776 047510 042527 042526 ,ASCIZ 'HOWEVER ERROR BIT NOT SET IN STATUS WORD'<15><12>
      004004 020122 051105 047522
      004012 020122 044502 020124
      004020 047516 020124 042523
      004026 020124 047111 051440
      004034 040524 052524 020123
      004042 047527 042122 005015
      004050      000
1119 004051      007
1120 004052 047105 006504 000012 MPGENDI ,BYTE 007
      ,ASCIZ 'END'<15><12>
      ,EVEN
;
; EMT DEFINITIONS AND ASSIGNMENTS
;
EMTTAB;
      TYPE=EMT+EMTX
      ,WORD STYPE
      EMTX=EMTX+I
      TYPES=EMT+EMTX
      ,WORD TYPB
      EMTX=EMTX+I
      ERROR=EMT+EMTX
      ,WORD ERR
      EMTX=EMTX+I
      CHALT=EMT+EMTX
      ,WORD CHLT
      EMTX=EMTX+I
      SRESET=EMT+EMTX
      ,WORD SRESET
      EMTX=EMTX+I
1121
1122
1123
1124
1125 004060
1126      104000
1127 004060 001100
1128      000001
1129      104001
1130 004062 002106
1131      000002
1132      104002
1133 004064 001720
1134      000003
1135      104003
1136 004066 002714
1137      000004
1138      104004
1139 004070 002730
1140      000005
```

1141		104005	SCOPE=EMT+EMTX
1142	004072	001424	,WORD CHAINN
1143		000006	EMTX=EMTX+1
1144		104006	ERROR10EMT+EMTX
1145	004074	001742	,WORD ERR1
1146		000007	EMTX=EMTX+1
1147		104007	ERRORS0EMT+EMTX
1148	004076	001644	,WORD ERRST
1149		000010	EMTX=EMTX+1
1150		104010	DELAY0EMT+EMTX
1151	004100	002752	,WORD DLY
1152		000011	EMTX=EMTX+1
1153		104011	SAVB40EMT+EMTX
1154	004102	003002	,WORD SVB4
1155		000012	EMTX=EMTX+1
1156		104012	RSTB40EMT+EMTX
1157	004104	003076	,WORD RSB4
1158		000013	EMTX=EMTX+1
1159		104013	SAVB50EMT+EMTX
1160	004106	003032	,WORD SVB5
1161		000014	EMTX=EMTX+1
1162		104014	RSTB50EMT+EMTX
1163	004110	003124	,WORD RSB5
1164		000015	EMTX=EMTX+1
1165		104015	SAVB550EMT+EMTX
1166	004112	003022	,WORD SVB55
1167		000016	EMTX=EMTX+1
1168		104016	RSTB50EMT+EMTX
1169	004114	003130	,WORD RSB5
1170		000017	EMTX=EMTX+1
1171		104017	EMALT0EMT+EMTX
1172	004116	002074	,WORD EMLT
1173		000020	EMTX=EMTX+1
1174	004120	000017	EMLI Mi EMTX-1
1175			
1176			STORAGE
1177			
1178	004122	000000	ICTRI OPEN
1179	004124	000000	ICNTI OPEN
1180	004126	000000	SCOPIRi OPEN
1181	004130	000000	RTNNOi OPEN
1182	004132	000000	NXTSTi OPEN
1183	004134	000000	CUATSTi OPEN
1184	004136	000000	UDCRTi OPEN
1185	004140	000000	UDSRTi OPEN

iCURRENT ITERATION COUNT  
iACCUMULATED ITERATION COUNT  
iCURRENT SCOPE POINTER

```

1187 |
1188 | |START OF TEST ROUTINES
1189 | |
1190 | |
1191 | |.....
1192 | 004142 000000 |T0| 0 |ROUTINE NUMBER 0 |
1193 | 004144 004174 | | T1 |ADDRESS OF NEXT ROUTINE |
1194 | 004146 001790 | | 1000, |TEST ITERATION COUNT |
1195 | 004150 004192 | | A1A |SCOPE ENTRY POINT |
1196 | 000000 | | X=X+1 | |
1197 | |.....
1198 | |TEST ABILITY TO REFERENCE UDCR WITHOUT TRAPPING
1199 | 004152 012767 004166 173624 |A1A| MOV @A1B,MACHER |SET UP BUS TRAP ERROR
1200 | 004160 009777 179026 | | TST @UDCR |REFERENCE UDCR
1201 | 004164 104005 | | |OR IF NO TRAP OCCURS
1202 | 004166 104002 |A1B| ERROR |TRAPPED WHEN REFERENCING UDCR
1203 | 004170 022626 | | POPSP2 |
1204 | 004172 104005 | | SCOPE |
1205 | |
1206 | |.....
1207 | 004174 000001 |T1| 1 |ROUTINE NUMBER 1 |
1208 | 004176 004226 | | T2 |ADDRESS OF NEXT ROUTINE |
1209 | 004200 001790 | | 1000, |TEST ITERATION COUNT |
1210 | 004202 004204 | | A2A |SCOPE ENTRY POINT |
1211 | 000001 | | X=X+1 | |
1212 | |.....
1213 | |TEST ABILITY TO REFERENCE UDSR WITHOUT TRAPPING
1214 | 004204 012767 004220 173572 |A2A| MOV @A2B,MACHER |SET UP BUS TRAP ERROR
1215 | 004212 009777 174776 | | TST @UDSR |REFERENCE UDSR
1216 | 004216 104005 | | |OR IF NO TRAP OCCURS
1217 | 004220 104002 |A2B| ERROR |TRAPPED WHEN REFERENCING UDSR
1218 | 004222 022626 | | POPSP2 |
1219 | 004224 104005 | | SCOPE |
1220 | |
1221 | |.....
1222 | 004226 000002 |T2| 2 |ROUTINE NUMBER 2 |
1223 | 004230 004260 | | T3 |ADDRESS OF NEXT ROUTINE |
1224 | 004232 001790 | | 1000, |TEST ITERATION COUNT |
1225 | 004234 004236 | | A3A |SCOPE ENTRY POINT |
1226 | 000002 | | X=X+1 | |
1227 | |.....
1228 | |TEST ABILITY TO REFERENCE UDCA1 WITHOUT TRAPPING
1229 | 004236 012767 004252 173540 |A3A| MOV @A3B,MACHER |SET UP BUS TRAP ERROR
1230 | 004244 009777 174756 | | TST @UDCA1 |REFERENCE UDCA1
1231 | 004250 104005 | | |OR IF NO TRAP OCCURS
1232 | 004252 104002 |A3B| ERROR |TRAPPED WHEN REFERENCING UDCA1
1233 | 004254 022626 | | POPSP2 |
1234 | 004256 104005 | | SCOPE |
1235 | |
1236 | |.....
1237 | 004260 000003 |T3| 3 |ROUTINE NUMBER 3 |
1238 | 004262 004312 | | T4 |ADDRESS OF NEXT ROUTINE |
1239 | 004264 001790 | | 1000, |TEST ITERATION COUNT |
1240 | 004266 004270 | | A4A |SCOPE ENTRY POINT |

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1241          000003          X0X+1          |
1242          |.....|
1243          |TEST ABILITY TO REFERENCE UDCA2 WITHOUT TRAPPING
1244 004270 012767 004304 173506 A4A1 MOV #A4B,MACHER |SET UP BUS TRAP ERROR
1245 004276 009777 174726      TST 0UDCA2 |REFERENCE UDCA2
1246 004302 104005          SCOPE |OR IF NO TRAP OCCURS
1247 004304 104002 A4B1 ERROR |TRAPPED WHEN REFERENCING UDCA2
1248 004306 022626      POPSP2
1249 004310 104005          SCOPE
1250          |
1251          |.....|
1252 004312 000004 T4I 4 |ROUTINE NUMBER 4
1253 004314 004344      T5 |ADDRESS OF NEXT ROUTINE
1254 004316 001790      1000, |TEST ITERATION COUNT
1255 004320 004322      A5A |SCOPE ENTRY POINT
1256          000004          X0X+1          |
1257          |.....|
1258          |TEST ABILITY TO REFERENCE UDCA3 WITHOUT TRAPPING
1259 004322 012767 004336 173494 A5A1 MOV #A5B,MACHER |SET UP BUS TRAP ERROR
1260 004330 009777 174676      TST 0UDCA3 |REFERENCE UDCA3
1261 004334 104005          SCOPE |OR IF NO TRAP OCCURS
1262 004336 104002 A5B1 ERROR |TRAPPED WHEN REFERENCING UDCA3
1263 004340 022626      POPSP2
1264 004342 104005          SCOPE
1265          |
1266          |.....|
1267 004344 000005 T5I 5 |ROUTINE NUMBER 5
1268 004346 004376      T6 |ADDRESS OF NEXT ROUTINE
1269 004350 001790      1000, |TEST ITERATION COUNT
1270 004352 004354      A6A |SCOPE ENTRY POINT
1271          000005          X0X+1          |
1272          |.....|
1273          |TEST ABILITY TO REFERENCE UDCA4 WITHOUT TRAPPING
1274 004354 012767 004370 173422 A6A1 MOV #A6B,MACHER |SET UP BUS TRAP ERROR
1275 004362 009777 174646      TST 0UDCA4 |REFERENCE UDCA4
1276 004366 104005          SCOPE |OR IF NO TRAP OCCURS
1277 004370 104002 A6B1 ERROR |TRAPPED WHEN REFERENCING UDCA4
1278 004372 022626      POPSP2
1279 004374 104005          SCOPE
1280          |
1281          |.....|
1282 004376 000006 T6I 6 |ROUTINE NUMBER 6
1283 004400 004430      T7 |ADDRESS OF NEXT ROUTINE
1284 004402 001790      1000, |TEST ITERATION COUNT
1285 004404 004406      A7A |SCOPE ENTRY POINT
1286          000006          X0X+1          |
1287          |.....|
1288          |TEST ABILITY TO REFERENCE UDCA5 WITHOUT TRAPPING
1289 004406 012767 004422 173370 A7A1 MOV #A7B,MACHER |SET UP BUS TRAP ERROR
1290 004414 009777 174616      TST 0UDCA5 |REFERENCE UDCA5
1291 004420 104005          SCOPE |OR IF NO TRAP OCCURS
1292 004422 104002 A7B1 ERROR |TRAPPED WHEN REFERENCING UDCA5
1293 004424 022626      POPSP2
1294 004426 104005          SCOPE

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1295 |
1296 |.....|
1297 004430 000007 T7i 7 |ROUTINE NUMBER 7
1298 004432 004462 T10 |ADDRESS OF NEXT ROUTINE
1299 004434 001750 1000 |TEST ITERATION COUNT
1300 004436 004440 A8A |SCOPE ENTRY POINT
1301 |.....|
1302 |
1303 |TEST ABILITY TO REFERENCE UDCA6 WITHOUT TRAPPING
1304 004440 012767 004454 173336 A8Ai MOV #A8B,MACHER |SET UP BUS TRAP ERROR
1305 004446 009777 174566 TST @UDCA6 |REFERENCE UDCA6
1306 004452 104005 |SCOPE
1307 004454 104002 A8Bi ERROR |OR IF NO TRAP OCCURS
1308 004456 022626 POPSP2 |TRAPPED WHEN REFERENCING UDCA6
1309 004460 104005 SCOPE
1310 |
1311 |.....|
1312 004462 000010 T10i 10 |ROUTINE NUMBER 10
1313 004464 004514 T11 |ADDRESS OF NEXT ROUTINE
1314 004466 001750 1000 |TEST ITERATION COUNT
1315 004470 004472 A9A |SCOPE ENTRY POINT
1316 |.....|
1317 |
1318 |TEST ABILITY TO REFERENCE UDCA7 WITHOUT TRAPPING
1319 004472 012767 004506 173304 A9Ai MOV #A9B,MACHER |SET UP BUS TRAP ERROR
1320 004500 009777 174536 TST @UDCA7 |REFERENCE UDCA7
1321 004504 104005 |SCOPE
1322 004506 104002 A9Bi ERROR |OR IF NO TRAP OCCURS
1323 004510 022626 POPSP2 |TRAPPED WHEN REFERENCING UDCA7
1324 004512 104005 SCOPE
1325 |
1326 |.....|
1327 004514 000011 T11i 11 |ROUTINE NUMBER 11
1328 004516 004546 T12 |ADDRESS OF NEXT ROUTINE
1329 004520 001750 1000 |TEST ITERATION COUNT
1330 004522 004524 A10A |SCOPE ENTRY POINT
1331 |.....|
1332 |
1333 |TEST ABILITY TO REFERENCE UDCA8 WITHOUT TRAPPING
1334 004524 012767 004540 173252 A10Ai MOV #A10B,MACHER |SET UP BUS TRAP ERROR
1335 004532 009777 174506 TST @UDCA8 |REFERENCE UDCA8
1336 004536 104005 |SCOPE
1337 004540 104002 A10Bi ERROR |OR IF NO TRAP OCCURS
1338 004542 022626 POPSP2 |TRAPPED WHEN REFERENCING UDCA8
1339 004544 104005 SCOPE
1340 |
1341 |.....|
1342 004546 000012 T12i 12 |ROUTINE NUMBER 12
1343 004550 004600 T13 |ADDRESS OF NEXT ROUTINE
1344 004552 001750 1000 |TEST ITERATION COUNT
1345 004554 004556 A11A |SCOPE ENTRY POINT
1346 |.....|
1347 |
1348 |TEST ABILITY TO REFERENCE UDCA9 WITHOUT TRAPPING
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1349 004556 012767 004572 173220 A1IAI MOV #A11B,MACHER ISET UP BUS TRAP ERROR
1350 004564 005777 174456 TST UDCA9 IREFERENCE UDCA9
1351 004570 104005 SCOPE IOK IF NO TRAP OCCURS
1352 004572 104002 A1IBI ERROR ITRAPPED WHEN REFERENCING UDCA9
1353 004574 022626 POPSP2
1354 004576 104005 SCOPE
1355
1356
1357 004600 000013 T13I 13 IROUTINE NUMBER 13
1358 004602 004704 T14 IADDRESS OF NEXT ROUTINE
1359 004604 000144 100. ITEST ITERATION COUNT
1360 004606 004610 B1A ISCOPE ENTRY POINT
1361 000013
1362
1363 I.....
1364 004610 005077 174376 B1AI CLR UDCR ICLEAR UDCR
1365 004614 052777 000001 174370 BIS #BIT0,UDCR ISET UDCR BIT 0
1366 004622 032777 000001 174362 BIT #BIT0,UDCR ISEE IF BIT IS SET
1367 004630 001002 ONE ,+6 IBRANCH IF SET
1368 004632 104002 ERROR IBIT 0 FAILED TO SET
1369 004634 104005 SCOPE
1370 004636 042777 000001 174346 BIC #BIT0,UDCR ICLEAR UDCR BIT 0
1371 004644 032777 000001 174340 BIT #BIT0,UDCR ISEE IF BIT HAS CLEARED
1372 004652 001401 BEQ ,+6 IBRANCH IF BIT IS CLEAR
1373 004654 104002 ERROR IBIT 0 DID NOT CLEAR
1374 004656 052777 000001 174326 BIS #BIT0,UDCR ISET UDCR BIT 0 (RIF)
1375 004664 005777 174356 TST UDCA9 IADDRESS MODULE
1376 004670 032777 000001 174314 BIT #BIT0,UDCR
1377 004676 001001 ONE ,+6
1378 004700 104002 ERROR IRIFF CLEARED BIT 0
1379 004702 104005 SCOPE
1380
1381
1382 004704 000014 T14I 14 IROUTINE NUMBER 14
1383 004706 004704 T15 IADDRESS OF NEXT ROUTINE
1384 004710 000144 100. ITEST ITERATION COUNT
1385 004712 004714 B2A ISCOPE ENTRY POINT
1386 000014
1387
1388 I.....
1389 004714 005077 174272 B2AI CLR UDCR ICLEAR UDCR
1390 004720 052777 000002 174264 BIS #BIT1,UDCR ISET UDCR BIT 1
1391 004726 032777 000002 174256 BIT #BIT1,UDCR ISEE IF BIT IS SET
1392 004734 001002 ONE ,+6 IBRANCH IF SET
1393 004736 104002 ERROR IUDCR BIT 1 FAILED TO SET
1394 004740 104005 SCOPE
1395 004742 042777 000002 174242 BIC #BIT1,UDCR ICLEAR UDCR BIT 1
1396 004750 032777 000002 174234 BIT #BIT1,UDCR ISEE IF BIT IS CLEAR
1397 004756 001401 BEQ ,+6 IBRANCH IF BIT IS CLEAR
1398 004760 104002 ERROR IUDCR BIT 1 FAILED TO CLEAR
1399 004762 104005 SCOPE
1400
1401
1402 004764 000015 T15I 15 IROUTINE NUMBER 15

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1403 004766 009044          T16          ;ADDRESS OF NEXT ROUTINE
1404 004770 000144          100.        ;TEST ITERATION COUNT
1405 004772 004774          B3A         ;SCOPE ENTRY POINT
1406          000015          X=X+1
1407
1408 |-----|
1409 004774 009077 174212 B3A1 CLR      UDCR      ;CLEAR UDCR
1410 005000 052777 000004 174204 BIS      #BIT2,UDCR  ;SET UDCR BIT 2
1411 005006 032777 000004 174176 BIT      #BIT2,UDCR  ;SEE IF BIT IS SET
1412 005014 001002          ONE      ;+6
1413 005016 104002          ERROR
1414 005020 104005          SCOPE
1415 005022 042777 000004 174162 BIC      #BIT2,UDCR  ;CLEAR UDCR BIT 2
1416 005030 032777 000004 174154 BIT      #BIT2,UDCR  ;SEE IF BIT IS CLEAR
1417 005036 001401          BEQ      ;+4
1418 005040 104002          ERROR
1419 005042 104005          SCOPE
1420
1421 |-----|
1422 005044 000016          T161        ;ROUTINE NUMBER 16
1423 005046 000124          T17        ;ADDRESS OF NEXT ROUTINE
1424 005050 000144          100.        ;TEST ITERATION COUNT
1425 005052 000054          B4A         ;SCOPE ENTRY POINT
1426          000016          X=X+1
1427
1428 |-----|
1429 005054 009077 174132 B4A1 CLR      UDCR      ;CLEAR UDCR
1430 005060 052777 000010 174124 BIS      #BIT3,UDCR  ;SET UDCR BIT 3
1431 005066 032777 000010 174116 BIT      #BIT3,UDCR  ;SEE IF BIT IS SET
1432 005074 001002          ONE      ;+6
1433 005076 104002          ERROR
1434 005100 104005          SCOPE
1435 005102 042777 000010 174102 BIC      #BIT3,UDCR  ;CLEAR UDCR BIT 3
1436 005110 032777 000010 174074 BIT      #BIT3,UDCR  ;SEE IF BIT IS CLEAR
1437 005116 001401          BEQ      ;+4
1438 005120 104002          ERROR
1439 005122 104005          SCOPE
1440
1441 |-----|
1442 005124 000017          T171        ;ROUTINE NUMBER 17
1443 005126 000204          T20        ;ADDRESS OF NEXT ROUTINE
1444 005130 000144          100.        ;TEST ITERATION COUNT
1445 005132 000134          B5A         ;SCOPE ENTRY POINT
1446          000017          X=X+1
1447
1448 |-----|
1449 005134 009077 174052 B5A1 CLR      UDCR      ;CLEAR UDCR
1450 005140 052777 000020 174044 BIS      #BIT4,UDCR  ;SET UDCR BIT 4
1451 005146 032777 000020 174036 BIT      #BIT4,UDCR  ;SEE IF BIT IS SET
1452 005154 001002          ONE      ;+6
1453 005156 104002          ERROR
1454 005160 104005          SCOPE
1455 005162 042777 000020 174022 BIC      #BIT4,UDCR  ;CLEAR UDCR BIT 4
1456 005170 032777 000020 174014 BIT      #BIT4,UDCR  ;SEE IF BIT IS CLEAR

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1457 005176 001401          BEQ      ,+4          IBRANCH IF BIT IS CLEAR
1458 005200 104002          ERROR          IUDCR BIT 4 FAILED TO CLEAR
1459 005202 104005          SCOPE
1460
1461 |.....|
1462 005204 000020 T201 20          IROUTINE NUMBER 20
1463 005206 005204 T21  T21          IADDRESS OF NEXT ROUTINE
1464 005210 000144 100.          ITEST ITERATION COUNT
1465 005212 005214 06A          ISCOPE ENTRY POINT
1466 000020 X=X+1          |
1467 |.....|
1468 ITEST THAT UDCR BIT 8 CAN BE SET AND CLEARED
1469 005214 005077 173772 06A1 CLR  UDCR          ICLEAR UDCR
1470 005220 052777 000400 173764 BIS  #BIT8,UDCR      ISET UDCR BIT 8
1471 005226 032777 000400 173756 BIT  #BIT8,UDCR      ISEE IF BIT IS SET
1472 005234 001002          ONE      ,+6          IBRANCH IF SET
1473 005236 104002          ERROR          IUDCR BIT 8 FAILED TO SET
1474 005240 104005          SCOPE
1475 005242 042777 000400 173742 BIC  #BIT8,UDCR      ICLEAR UDCR BIT 8
1476 005250 032777 000400 173734 BIT  #BIT8,UDCR      ISEE IF BIT IS CLEAR
1477 005256 001401          BEQ      ,+4          IBRANCH IF BIT IS CLEAR
1478 005260 104002          ERROR          IUDCR BIT 8 FAILED TO CLEAR
1479 005262 104005          SCOPE
1480
1481 |.....|
1482 005264 000021 T211 21          IROUTINE NUMBER 21
1483 005266 005344 T22  T22          IADDRESS OF NEXT ROUTINE
1484 005270 000144 100.          ITEST ITERATION COUNT
1485 005272 005274 07A          ISCOPE ENTRY POINT
1486 000021 X=X+1          |
1487 |.....|
1488 ITEST THAT UDCR BIT 9 CAN BE SET AND CLEARED
1489 005274 005077 173712 07A1 CLR  UDCR          ICLEAR UDCR
1490 005300 052777 001000 173704 BIS  #BIT9,UDCR      ISET UDCR BIT 9
1491 005306 032777 001000 173676 BIT  #BIT9,UDCR      ISEE IF BIT IS SET
1492 005314 001002          ONE      ,+6          IBRANCH IF SET
1493 005316 104002          ERROR          IUDCR BIT 9 FAILED TO SET
1494 005320 104005          SCOPE
1495 005322 042777 001000 173662 BIC  #BIT9,UDCR      ICLEAR UDCR BIT 9
1496 005330 032777 001000 173654 BIT  #BIT9,UDCR      ISEE IF BIT IS CLEAR
1497 005336 001401          BEQ      ,+4          IBRANCH IF BIT IS CLEAR
1498 005340 104002          ERROR          IUDCR BIT 9 FAILED TO CLEAR
1499 005342 104005          SCOPE
1500
1501 |.....|
1502 005344 000022 T221 22          IROUTINE NUMBER 22
1503 005346 005424 T23  T23          IADDRESS OF NEXT ROUTINE
1504 005350 000144 100.          ITEST ITERATION COUNT
1505 005352 005354 08A          ISCOPE ENTRY POINT
1506 000022 X=X+1          |
1507 |.....|
1508 ITEST THAT UDCR BIT 10 CAN BE SET AND CLEARED
1509 005354 005077 173632 08A1 CLR  UDCR          ICLEAR UDCR
1510 005360 052777 002000 173624 BIS  #BIT10,UDCR     ISET UDCR BIT 10

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1511	005366	032777	002000	173616	BIT	#BIT10,UDCR	ISEE IF BIT IS SET
1512	005374	001002			BNE	,+6	IBRANCH IF SET
1513	005376	104002			ERROR		IUDCR BIT 10 FAILED TO SET
1514	005400	104005			SCOPE		
1515	005402	042777	002000	173602	BIC	#BIT10,UDCR	ICLEAR UDCR BIT 10
1516	005410	032777	002000	173574	BIT	#BIT10,UDCR	ISEE IF BIT IS CLEAR
1517	005416	001401			BEQ	,+4	IBRANCH IF BIT IS CLEAR
1518	005420	104002			ERROR		IUDCR BIT 10 FAILED TO CLEAR
1519	005422	104005			SCOPE		
1520							
1521							
1522	005424	000023			T23I	23	ROUTINE NUMBER 23
1523	005426	009504				T24	ADDRESS OF NEXT ROUTINE
1524	005430	000144				100,	TEST ITERATION COUNT
1525	005432	009434				B9A	SCOPE ENTRY POINT
1526		000023				X=X+1	
1527							
1528							
1529	005434	009077	173552		ITEST THAT UDCR BIT 11 CAN BE SET AND CLEARED		
1530	005440	052777	004000	173544	B9AI	CLR UDCR	ICLEAR UDCR
1531	005446	032777	004000	173536	BIS	#BIT11,UDCR	ISSET UDCR BIT 11
1532	005454	001002			BIT	#BIT11,UDCR	ISEE IF BIT IS SET
1533	005456	104002			BNE	,+6	IBRANCH IF SET
1534	005460	104005			ERROR		IUDCR BIT 11 FAILED TO SET
1535	005462	042777	004000	173522	SCOPE		
1536	005470	032777	004000	173514	BIC	#BIT11,UDCR	ICLEAR UDCR BIT 11
1537	005476	001401			BIT	#BIT11,UDCR	ISEE IF BIT IS CLEAR
1538	005500	104002			BEQ	,+4	IBRANCH IF BIT IS CLEAR
1539	005502	104005			ERROR		IUDCR BIT 11 FAILED TO CLEAR
1540					SCOPE		
1541							
1542	005504	000024			T24I	24	ROUTINE NUMBER 24
1543	005506	009540				T25	ADDRESS OF NEXT ROUTINE
1544	005510	000005				5,	TEST ITERATION COUNT
1545	005512	009514				C1A	SCOPE ENTRY POINT
1546		000024				X=X+1	
1547							
1548							
1549	005514	052777	000001	173470	ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 0		
1550	005522	104004			C1AI	BIS #BIT0,UDCR	ISSET UDCR BIT 0
1551	005524	032777	000001	173460	SRESET		ISSUE RESET TO CLEAR BIT
1552	005532	001401			BIT	#BIT0,UDCR	ISEE IF BIT IS CLEAR
1553	005534	104002			BEQ	,+4	IBRANCH IF BIT IS CLEAR
1554	005536	104005			ERROR		IRESET FAILED TO CLEAR UDCR BIT 0
1555					SCOPE		
1556							
1557	005540	000025			T25I	25	ROUTINE NUMBER 25
1558	005542	009574				T26	ADDRESS OF NEXT ROUTINE
1559	005544	000005				5,	TEST ITERATION COUNT
1560	005546	009550				C2A	SCOPE ENTRY POINT
1561		000025				X=X+1	
1562							
1563							
1564	005550	052777	000002	173434	ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 1		
					C2AI	BIS #BIT1,UDCR	ISSET UDCR BIT 1

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1565 005556 104004          SRESET          ;ISSUE RESET TO CLEAR BIT
1566 005560 032777 000002 173424 BIT #BIT1,UDCR ;SEE IF BIT IS CLEAR
1567 005566 001401 BEQ ,+4 ;BRANCH IF BIT IS CLEAR
1568 005570 104002 ERROR ;RESET FAILED TO CLEAR UDCR BIT 1
1569 005572 104005 SCOPE
1570
1571 |
1572 005574 000026 T26i 26 ;ROUTINE NUMBER 26
1573 005576 009630 T27 ;ADDRESS OF NEXT ROUTINE
1574 005600 000005 S ;TEST ITERATION COUNT
1575 005602 009604 C3A ;SCOPE ENTRY POINT
1576 000026 X=X+1
1577 |
1578 ;TEST THAT RESET INSTRUCTION CLEARS UDCR BIT 2
1579 005604 052777 000004 173400 C3A1 B18 #BIT2,UDCR ;SET UDCR BIT 2
1580 005612 104004 SRESET ;ISSUE RESET TO CLEAR BIT
1581 005614 032777 000004 173370 BIT #BIT2,UDCR ;SEE IF BIT IS CLEAR
1582 005622 001401 BEQ ,+4 ;BRANCH IF BIT IS CLEAR
1583 005624 104002 ERROR ;RESET FAILED TO CLEAR UDCR BIT 2
1584 005626 104005 SCOPE
1585
1586 |
1587 005630 000027 T27i 27 ;ROUTINE NUMBER 27
1588 005632 009664 T30 ;ADDRESS OF NEXT ROUTINE
1589 005634 000005 S ;TEST ITERATION COUNT
1590 005636 009640 C4A ;SCOPE ENTRY POINT
1591 000027 X=X+1
1592 |
1593 ;TEST THAT RESET INSTRUCTION CLEARS UDCR BIT 3
1594 005640 052777 000010 173344 C4A1 B18 #BIT3,UDCR ;SET UDCR BIT 3
1595 005646 104004 SRESET ;ISSUE RESET TO CLEAR BIT
1596 005650 032777 000010 173334 BIT #BIT3,UDCR ;SEE IF BIT IS CLEAR
1597 005656 001401 BEQ ,+4 ;BRANCH IF BIT IS CLEAR
1598 005660 104002 ERROR ;RESET FAILED TO CLEAR UDCR BIT 3
1599 005662 104005 SCOPE
1600
1601 |
1602 005664 000030 T30i 30 ;ROUTINE NUMBER 30
1603 005666 009720 T31 ;ADDRESS OF NEXT ROUTINE
1604 005670 000005 S ;TEST ITERATION COUNT
1605 005672 009674 C5A ;SCOPE ENTRY POINT
1606 000030 X=X+1
1607 |
1608 ;TEST THAT RESET INSTRUCTION CLEARS UDCR BIT 4
1609 005674 052777 000020 173310 C5A1 B18 #BIT4,UDCR ;SET UDCR BIT 4
1610 005702 104004 SRESET ;ISSUE RESET TO CLEAR BIT
1611 005704 032777 000020 173300 BIT #BIT4,UDCR ;SEE IF BIT IS CLEAR
1612 005712 001401 BEQ ,+4 ;BRANCH IF BIT IS CLEAR
1613 005714 104002 ERROR ;RESET FAILED TO CLEAR UDCR BIT 4
1614 005716 104005 SCOPE
1615
1616 |
1617 005720 000031 T31i 31 ;ROUTINE NUMBER 31
1618 005722 009754 T32 ;ADDRESS OF NEXT ROUTINE

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1619 005724 000005          5;          ITEST ITERATION COUNT
1620 005726 000730          C6A          ISCOPE ENTRY POINT
1621          000031          X=X+1
1622          |-----|
1623          ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 5
1624 005730 052777 000040 173254 C6A1  BIS  #BIT5,UDCR  ISET UDCR BIT 5
1625 005736 104004          SRESET      ISSUE RESET TO CLEAR BIT
1626 005740 032777 000040 173244  BIT  #BIT5,UDCR  ISEE IF BIT IS CLEAR
1627 005746 001401          BEQ  ,+4        IBRANCH IF BIT IS CLEAR
1628 005750 104002          ERROR      IRESET FAILED TO CLEAR UDCR BIT 5
1629 005752 104005          SCOPE
1630          |-----|
1631          |-----|
1632 005754 000032          T32i  32          IROUTINE NUMBER 32
1633 005756 000010          T33          IADDRESS OF NEXT ROUTINE
1634 005760 000005          5;          ITEST ITERATION COUNT
1635 005762 000764          C7A          ISCOPE ENTRY POINT
1636          X=X+1
1637          |-----|
1638          ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 6
1639 005764 052777 000100 173220 C7A1  BIS  #BIT6,UDCR  ISET UDCR BIT 6
1640 005772 104004          SRESET      ISSUE RESET TO CLEAR BIT
1641 005774 032777 000100 173210  BIT  #BIT6,UDCR  ISEE IF BIT IS CLEAR
1642 006002 001401          BEQ  ,+4        IBRANCH IF BIT IS CLEAR
1643 006004 104002          ERROR      IRESET FAILED TO CLEAR UDCR BIT 6
1644 006006 104005          SCOPE
1645          |-----|
1646          |-----|
1647 006010 000033          T33i  33          IROUTINE NUMBER 33
1648 006012 000044          T34          IADDRESS OF NEXT ROUTINE
1649 006014 000005          5;          ITEST ITERATION COUNT
1650 006016 000020          C8A          ISCOPE ENTRY POINT
1651          X=X+1
1652          |-----|
1653          ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 7
1654 006020 052777 000200 173164 C8A1  BIS  #BIT7,UDCR  ISET UDCR BIT 7
1655 006026 104004          SRESET      ISSUE RESET TO CLEAR BIT
1656 006030 032777 000200 173154  BIT  #BIT7,UDCR  ISEE IF BIT IS CLEAR
1657 006036 001401          BEQ  ,+4        IBRANCH IF BIT IS CLEAR
1658 006040 104002          ERROR      IRESET FAILED TO CLEAR UDCR BIT 7
1659 006042 104005          SCOPE
1660          |-----|
1661          |-----|
1662 006044 000034          T34i  34          IROUTINE NUMBER 34
1663 006046 000100          T35          IADDRESS OF NEXT ROUTINE
1664 006050 000005          5;          ITEST ITERATION COUNT
1665 006052 000054          C9A          ISCOPE ENTRY POINT
1666          X=X+1
1667          |-----|
1668          ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 8
1669 006054 052777 000400 173130 C9A1  BIS  #BIT8,UDCR  ISET UDCR BIT 8
1670 006062 104004          SRESET      ISSUE RESET TO CLEAR BIT
1671 006064 032777 000400 173120  BIT  #BIT8,UDCR  ISEE IF BIT IS CLEAR
1672 006072 001401          BEQ  ,+4        IBRANCH IF BIT IS CLEAR

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1673 006074 104022 ERROR IRESET FAILED TO CLEAR UDCR BIT 8
1674 006076 104035 SCOPE
1675 |
1676 |.....|
1677 006100 000035 T39I 35 IROUTINE NUMBER 35
1678 006102 006134 T36 IADDRESS OF NEXT ROUTINE
1679 006104 000005 S. ITEST ITERATION COUNT
1680 006106 006110 C10A ISCOPE ENTRY POINT
1681 000035 X=X+1
1682 |.....|
1683 ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 9
1684 006110 052777 001000 173074 C10AI BIS #BIT9,UDCR ISET UDCR BIT 9
1685 006116 104024 SRESET ISSUE RESET TO CLEAR BIT
1686 006120 032777 001000 173064 BIT #BIT9,UDCR ISEE IF BIT IS CLEAR
1687 006126 001401 BEQ ,+4 IBRANCH IF BIT IS CLEAR
1688 006130 104002 ERROR IRESET FAILED TO CLEAR UDCR BIT 9
1689 006132 104035 SCOPE
1690 |
1691 |.....|
1692 006134 000036 T36I 36 IROUTINE NUMBER 36
1693 006136 006170 T37 IADDRESS OF NEXT ROUTINE
1694 006140 000005 S. ITEST ITERATION COUNT
1695 006142 006144 C11A ISCOPE ENTRY POINT
1696 000036 X=X+1
1697 |.....|
1698 ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 10
1699 006144 052777 002000 173040 C11AI BIS #BIT10,UDCR ISET UDCR BIT 10
1700 006152 104004 SRESET ISSUE RESET TO CLEAR BIT
1701 006154 032777 002000 173030 BIT #BIT10,UDCR ISEE IF BIT IS CLEAR
1702 006162 001401 BEQ ,+4 IBRANCH IF BIT IS CLEAR
1703 006164 104002 ERROR IRESET FAILED TO CLEAR UDCR BIT 10
1704 006166 104035 SCOPE
1705 |
1706 |.....|
1707 006170 000037 T39I 37 IROUTINE NUMBER 37
1708 006172 006224 T40 IADDRESS OF NEXT ROUTINE
1709 006174 000005 S. ITEST ITERATION COUNT
1710 006176 006200 C12A ISCOPE ENTRY POINT
1711 000037 X=X+1
1712 |.....|
1713 ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 11
1714 006200 052777 004000 173004 C12AI BIS #BIT11,UDCR ISET UDCR BIT 11
1715 006206 104004 SRESET ISSUE RESET TO CLEAR BIT
1716 006210 032777 004000 172774 BIT #BIT11,UDCR ISEE IF BIT IS CLEAR
1717 006216 001401 BEQ ,+4 IBRANCH IF BIT IS CLEAR
1718 006220 104002 ERROR IRESET FAILED TO CLEAR UDCR BIT 11
1719 006222 104035 SCOPE
1720 |
1721 |.....|
1722 006224 000040 T40I 40 IROUTINE NUMBER 40
1723 006226 006260 T41 IADDRESS OF NEXT ROUTINE
1724 006230 000005 S. ITEST ITERATION COUNT
1725 006232 006234 C13A ISCOPE ENTRY POINT
1726 000040 X=X+1
```

```
1727 | .....  
1728 | ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 12  
1729 006234 052777 010000 172750 C13AI BIS #BIT12,UDCR ISET UDCR BIT 12  
1730 006242 104004 SRESET IISSUE RESET TO CLEAR BIT  
1731 006244 032777 010000 172740 BIT #BIT12,UDCR ISEE IF BIT IS CLEAR  
1732 006252 001401 BEQ ,+4 IBRANCH IF BIT IS CLEAR  
1733 006254 104002 ERROR IRESET FAILED TO CLEAR UDCR BIT 12  
1734 006256 104005 SCOPE  
1735 |  
1736 | .....  
1737 006260 000041 T41i 41 IROUTINE NUMBER 41  
1738 006262 006314 T42 IADDRESS OF NEXT ROUTINE  
1739 006264 000005 S, ITEST ITERATION COUNT  
1740 006266 006270 C14A ISCOPE ENTRY POINT  
1741 000041 X#X+1  
1742 | .....  
1743 | ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 13  
1744 006270 052777 020000 172714 C14Ai BIS #BIT13,UDCR ISET UDCR BIT 13  
1745 006276 104004 SRESET IISSUE RESET TO CLEAR BIT  
1746 006300 032777 020000 172704 BIT #BIT13,UDCR ISEE IF BIT IS CLEAR  
1747 006306 001401 BEQ ,+4 IBRANCH IF BIT IS CLEAR  
1748 006310 104002 ERROR IRESET FAILED TO CLEAR UDCR BIT 13  
1749 006312 104005 SCOPE  
1750 |  
1751 | .....  
1752 006314 000042 T42i 42 IROUTINE NUMBER 42  
1753 006316 006350 T43 IADDRESS OF NEXT ROUTINE  
1754 006320 000005 S, ITEST ITERATION COUNT  
1755 006322 006324 C15A ISCOPE ENTRY POINT  
1756 000042 X#X+1  
1757 | .....  
1758 | ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 14  
1759 006324 052777 040000 172660 C15Ai BIS #BIT14,UDCR ISET UDCR BIT 14  
1760 006332 104004 SRESET IISSUE RESET TO CLEAR BIT  
1761 006334 032777 040000 172650 BIT #BIT14,UDCR ISEE IF BIT IS CLEAR  
1762 006342 001401 BEQ ,+4 IBRANCH IF BIT IS CLEAR  
1763 006344 104002 ERROR IRESET FAILED TO CLEAR UDCR BIT 14  
1764 006346 104005 SCOPE  
1765 |  
1766 | .....  
1767 006350 000043 T43i 43 IROUTINE NUMBER 43  
1768 006352 006404 T44 IADDRESS OF NEXT ROUTINE  
1769 006354 000005 S, ITEST ITERATION COUNT  
1770 006356 006360 C16A ISCOPE ENTRY POINT  
1771 000043 X#X+1  
1772 | .....  
1773 | ITEST THAT RESET INSTRUCTION CLEARS UDCR BIT 15  
1774 006360 052777 100000 172624 C16Ai BIS #BIT15,UDCR ISET UDCR BIT 15  
1775 006366 104004 SRESET IISSUE RESET TO CLEAR BIT  
1776 006370 032777 100000 172614 BIT #BIT15,UDCR ISEE IF BIT IS CLEAR  
1777 006376 001401 BEQ ,+4 IBRANCH IF BIT IS CLEAR  
1778 006400 104002 ERROR IRESET FAILED TO CLEAR UDCR BIT 15  
1779 006402 104005 SCOPE  
1780 |
```

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1781
1782 006404 000044
1783 006406 006430
1784 006410 000012
1785 006412 006414
1786 000044
1787
1788
1789 006414 104004
1790 006416 109777 172572
1791 006422 001401
1792 006424 104007
1793 006426 104005
1794
1795
1796 006430 000045
1797 006432 006694
1798 006434 000062
1799 006436 006440
1800 000045
1801
1802
1803 006440 104004
1804 006442 009777 172554
1805 006446 127727 172542 000040
1806 006454 001402
1807 006456 104007
1808 006460 104005
1809 006462 009777 172534
1810 006466 127727 172522 000100
1811 006474 001402
1812 006476 104007
1813 006500 104005
1814 006502 009777 172514
1815 006506 127727 172502 000140
1816 006514 001402
1817 006516 104007
1818 006520 104005
1819 006522 009777 172474
1820 006526 127727 172462 000200
1821 006534 001402
1822 006536 104007
1823 006540 104005
1824 006542 009777 172454
1825 006546 127727 172442 000240
1826 006554 001402
1827 006556 104007
1828 006560 104005
1829 006562 009777 172434
1830 006566 127727 172422 000300
1831 006574 001402
1832 006576 104007
1833 006600 104005
1834 006602 009777 172414

|.....|
T44i 44 |ROUTINE NUMBER 44 |
      T49 |ADDRESS OF NEXT ROUTINE |
      10: |TEST ITERATION COUNT |
      C17A |SCOPE ENTRY POINT |
      X=X+1 |
|.....|
|TEST THAT INIT CLEARS SCAN REGISTER
C17Ai SRESET
      TSTB 0UDSR |TEST IF SCAN REGISTER = 0
      BEQ ,+6 |BRANCH IF REGISTER = 0
      ERRORS
      SCOPE
|
|.....|
T49i 49 |ROUTINE NUMBER 49 |
      T46 |ADDRESS OF NEXT ROUTINE |
      90: |TEST ITERATION COUNT |
      D1A |SCOPE ENTRY POINT |
      X=X+1 |
|.....|
|TEST THAT X SCAN REG COUNTS CORRECTLY USING MAINT CLOCK
D1Ai SRESET |CLEAR SCAN REGISTER
      TST 0MCLK |GENERATE STROBE
      CMPB 0UDSR,#40 |CHECK COUNT
      BEQ ,+6 |BRANCH IF COUNT CORRECT
      ERRORS |X DID NOT COUNT TO 1
      SCOPE
      TST 0MCLK
      CMPB 0UDSR,#100 |X DID NOT COUNT TO 2
      BEQ ,+6
      ERRORS
      SCOPE
      TST 0MCLK
      CMPB 0UDSR,#140 |X DID NOT COUNT TO 3
      BEQ ,+6
      ERRORS
      SCOPE
      TST 0MCLK
      CMPB 0UDSR,#200 |X DID NOT COUNT TO 4
      BEQ ,+6
      ERRORS
      SCOPE
      TST 0MCLK
      CMPB 0UDSR,#240 |X DID NOT COUNT TO 5
      BEQ ,+6
      ERRORS
      SCOPE
      TST 0MCLK
      CMPB 0UDSR,#300 |X DID NOT COUNT TO 6
      BEQ ,+6
      ERRORS
      SCOPE
      TST 0MCLK

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1035	006606	127727	172402	000340	CMPB	0UDSR,#340	
1036	006614	001402			BEG	,+6	
1037	006616	104007			ERRORS		ix DID NOT COUNT TO 7
1038	006620	104005			SCOPE		
1039	006622	009777	172364		TST	0UDCR	
1040	006626	001402			BEG	,+6	iBRANCH IF CONT REG CLEAR
1041	006630	104007			ERRORS		
1042	006632	104005			SCOPE		
1043	006634	009777	172362		TST	0MCLK	
1044	006640	027727	172346	100000	CMP	0UDCR,#BITIS	iONLY SCAN ERROR SHOULD BE SET
1045	006646	001401			BEG	,+4	
1046	006650	104007			ERRORS		
1047	006652	104005			SCOPE		
1048							
1049							
1050	006654	000046					
1051	006656	007110					
1052	006660	000062					
1053	006662	006664					
1054		000046					
1055							
1056							
1057	006664	104004					
1058	006666	012777	001400	172316	MOV	0BIT9BIT0,0UDCR	iSET STOP X+MAINT
1059	006674	009777	172322		TST	0MCLK	iGENERATE STROBE
1060	006700	127727	172310	000004	CMPB	0UDSR,#4	iCHECK COUNT
1061	006706	001402			BEG	,+6	iBRANCH IF COUNT CORRECT
1062	006710	104007			ERRORS		iY DID NOT COUNT TO 1
1063	006712	104005			SCOPE		
1064	006714	009777	172302		TST	0MCLK	
1065	006720	127727	172270	000010	CMPB	0UDSR,#10	
1066	006726	001402			BEG	,+6	
1067	006730	104007			ERRORS		iY DID NOT COUNT TO 2
1068	006732	104005			SCOPE		
1069	006734	009777	172262		TST	0MCLK	
1070	006740	127727	172250	000014	CMPB	0UDSR,#14	
1071	006746	001402			BEG	,+6	
1072	006750	104007			ERRORS		iY DID NOT COUNT TO 3
1073	006752	104005			SCOPE		
1074	006754	009777	172242		TST	0MCLK	
1075	006760	127727	172230	000020	CMPB	0UDSR,#20	
1076	006766	001402			BEG	,+6	
1077	006770	104007			ERRORS		iY DID NOT COUNT TO 4
1078	006772	104005			SCOPE		
1079	006774	009777	172222		TST	0MCLK	
1080	007000	127727	172210	000024	CMPB	0UDSR,#24	
1081	007006	001402			BEG	,+6	
1082	007010	104007			ERRORS		iY DID NOT COUNT TO 5
1083	007012	104005			SCOPE		
1084	007014	009777	172202		TST	0MCLK	
1085	007020	127727	172170	000030	CMPB	0UDSR,#30	
1086	007026	001402			BEG	,+6	
1087	007030	104007			ERRORS		iY DID NOT COUNT TO 6
1088	007032	104005			SCOPE		

1889	007034	009777	172162		TST	0MCLK	
1890	007040	127727	172150	000034	CMPB	0UDSR,#34	
1891	007046	001402			BEG	,+6	
1892	007050	104007			ERRORS		iy DID NOT COUNT TO 7
1893	007052	104005			SCOPE		
1894	007054	027727	172132	001400	CMP	0UDCR,#BIT0BIT0	IBR IF ONLY STOP X+MAINT SET
1895	007062	001402			BEG	,+6	
1896	007064	104007			ERRORS		
1897	007066	104005			SCOPE		
1898	007070	009777	172126		TST	0MCLK	ISTROBE TO ERROR
1899	007074	027727	172112	101400	CMP	0UDCR,#BIT15:BIT9:BIT0	IONLY SCAN ERR,SIP X,MAINT SET
1900	007102	001401			BEG	,+4	
1901	007104	104007			ERRORS		
1902	007106	104005			SCOPE		
1903							
1904							
1905	007110	000047			T47i	47	ROUTINE NUMBER 47
1906	007112	007244			T50		ADDRESS OF NEXT ROUTINE
1907	007114	000062			50i		TEST ITERATION COUNT
1908	007116	007120			D3A		SCOPE ENTRY POINT
1909		000047			X+X+1		
1910							
1911							
1912	007120	104004			ITEST THAT WD SCAN REG COUNTS CORRECTLY USING MAINT CLK		
1913	007122	012777	003400	172062	D3Ai	SRESET	CLEAR SCAN REGISTER
1914	007130	009777	172066		MOV	0BIT0:BIT9:BIT0	0UDCR ISET SIP X+Y+MAINT
1915	007134	127727	172054	000001	TST	0MCLK	GENERATE STROBE
1916	007142	001402			CMPB	0UDSR,#1	CHECK COUNT
1917	007144	104007			BEG	,+6	BRANCH IF COUNT CORRECT
1918	007146	104005			ERRORS		WD DID NOT COUNT TO 1
1919	007150	009777	172046		SCOPE		
1920	007154	127727	172034	000002	TST	0MCLK	
1921	007162	001402			CMPB	0UDSR,#2	
1922	007164	104007			BEG	,+6	
1923	007166	104005			ERRORS		WD DID NOT COUNT TO 2
1924	007170	009777	172026		SCOPE		
1925	007174	127727	172014	000003	TST	0MCLK	
1926	007202	001402			CMPB	0UDSR,#3	
1927	007204	104007			BEG	,+6	
1928	007206	104005			ERRORS		WD DID NOT COUNT TO 3
1929	007210	027727	171776	003400	SCOPE		
1930	007216	001402			CMP	0UDCR,#BIT0:BIT9:BIT0	
1931	007220	104007			BEG	,+6	BRANCH IF ONLY SIP X+Y+MAINT SET
1932	007222	104005			ERRORS		
1933	007224	009777	171772		SCOPE		
1934	007230	027727	171756	103400	TST	0MCLK	ISTROBE TO ERROR
1935	007236	001401			CMP	0UDCR,#BIT15:BIT0:BIT9:BIT10	
1936	007240	104007			BEG	,+4	IBR IF ONLY SCAN ERROR,SIP X+Y,MAINT SET
1937	007242	104005			ERRORS		
1938					SCOPE		
1939							
1940	007244	000050			T50i	50	ROUTINE NUMBER 50
1941	007246	007334			T51		ADDRESS OF NEXT ROUTINE
1942	007250	000144			100i		TEST ITERATION COUNT

1943	007252	007254			E1A		ISCOPE ENTRY POINT	•
1944		000090			X0X+1			•
1945							.....	
1946					ITEST THAT DEF INT CAN BE GENERATED BY MAINT + DEF INT EN			
1947	007254	012777	000402	171730	E1A1	MOV	#BITC2,0UDCR	ISSET MAINT+DEF INT EN
1948	007262	032777	010000	171722		BIT	#BIT12,0UDCR	ICHECK DEF INT BEING GENERATED
1949	007270	001002				BNE	,+6	IBRANCH IF SET
1950	007272	104007				ERRORS		
1951	007274	104005				SCOPE		
1952	007276	032777	020000	171706		BIT	#BIT13,0UDCR	ICHECK IF IMM INT SET
1953	007304	001402				BEQ	,+6	IBRANCH IF CLEAR
1954	007306	104007				ERRORS		
1955	007310	104005				SCOPE		
1956	007312	042777	000400	171672		BIC	#BIT0,0UDCR	ICLEAR MAINT FLOP
1957	007320	032777	010000	171664		BIT	#BIT12,0UDCR	ICHECK IF DEF INT CLEAR
1958	007326	001401				BEQ	,+4	IBRANCH IF CLEAR
1959	007330	104007				ERRORS		
1960	007332	104005				SCOPE		
1961								
1962							.....	
1963	007334	000091			T511	91	IROUTINE NUMBER 91	•
1964	007336	007442				T52	IADDRESS OF NEXT ROUTINE	•
1965	007340	000012				10:	ITEST ITERATION COUNT	•
1966	007342	007344				E2A	ISCOPE ENTRY POINT	•
1967		000091				X0X+1		•
1968							.....	
1969					ITEST THAT DEF SCAN STARTS AND SETS SCAN ERROR, NO TRAP #S07			
1970	007344	104004			E2A1	SRESET		
1971	007346	012777	000412	171636		MOV	#BITC1,0UDCR	ISSET MAINT,DEF INT,DEF SCAN EN
1972	007354	104010				DELAY		
1973	007356	000001				1	IWAIT 1 MS	
1974	007360	032777	100000	171624		BIT	#BIT15,0UDCR	IDID SCAN ERROR SET?
1975	007366	001002				BNE	,+6	IBRANCH IF BIT IS SET
1976	007370	104007				ERRORS		
1977	007372	104005				SCOPE		
1978	007374	032777	000040	171610		BIT	#BIT5,0UDCR	IDID SCAN ERROR SET DEF DONE?
1979	007402	001002				BNE	,+6	IBRANCH IF BIT IS SET
1980	007404	104007				ERRORS		
1981	007406	104005				SCOPE		
1982	007410	104004				SRESET		
1983	007412	032777	100000	171572		BIT	#BIT15,0UDCR	IDID SCAN ERROR CLEAR?
1984	007420	001402				BEQ	,+6	IBRANCH IF CLEAR
1985	007422	104007				ERRORS		
1986	007424	104005				SCOPE		
1987	007426	032777	000040	171556		BIT	#BIT5,0UDCR	IDID DEF SCAN DONE CLEAR?
1988	007434	001401				BEQ	,+4	IBRANCH IF CLEAR
1989	007436	104007				ERRORS		
1990	007440	104005				SCOPE		
1991								
1992							.....	
1993	007442	000092			T521	92	IROUTINE NUMBER 92	•
1994	007444	007516				T53	IADDRESS OF NEXT ROUTINE	•
1995	007446	000012				10:	ITEST ITERATION COUNT	•
1996	007450	007452				E20A	ISCOPE ENTRY POINT	•

```
1997      000092      X=X+1      i
1998      |
1999      |.....|
2000      007452  104004      E2BAI  SRESET      I INITIALIZE CONTROL
2001      007454  012777  000412  171530      MOV      @BITC1,@UDCR      I SET MAINT,DEF INT,DEF SCAN EN
2002      007462  032777  000001  171522      BIT      @BIT0,@UDCR      I DID RIF SET WITH START SCAN
2003      007470  001402      BEQ      ,+6      I BRANCH IF RIF CLEAR
2004      007472  104007      ERRORS
2005      007474  104005      SCOPE
2006      007476  104010      DELAY      I WAIT FOR SCAN DONE
2007      007500  000001
2008      007502  022777  120452  171502      CMP      @120452,@UDCR      I SCAN ERR,DEF INT,MAINT,DEF SCAN DONE
2009      007510  001001      BNE      ,+4      I DEF SCAN EN,DEF INT EN
2010      007512  104007      ERRORS      I SHOULD ALL BE SET
2011      007514  104005      SCOPE
2012      |
2013      |.....|
2014      007516  000093      T53I  93      I ROUTINE NUMBER 93
2015      007520  007572      T54      I ADDRESS OF NEXT ROUTINE
2016      007522  000012      10:      I TEST ITERATION COUNT
2017      007524  007526      E2CA      I SCOPE ENTRY POINT
2018      000093      X=X+1      |
2019      |
2020      |.....|
2021      007526  104004      E2CAI  SRESET      I INITIALIZE CONTROL
2022      007530  012777  000413  171494      MOV      @BITC1@BIT0,@UDCR      I SET MAINT,DEF INT,DEF SCAN,RIF
2023      007536  032777  000001  171446      BIT      @BIT0,@UDCR      I DID RIF CLEAR WITH START SCAN
2024      007544  001002      BNE      ,+6      I BRANCH IF RIF SET
2025      007546  104007      ERRORS
2026      007550  104005      SCOPE
2027      007552  104010      DELAY
2028      007554  000001
2029      007556  022777  120453  171426      CMP      @120453,@UDCR      I SCAN ERR,D INT,MAINT,D SCAN DONE
2030      007564  001001      BNE      ,+4      I D SCAN EN,D INT EN ALL SET
2031      007566  104007      ERRORS
2032      007570  104005      SCOPE
2033      |
2034      |.....|
2035      007572  000094      T54I  94      I ROUTINE NUMBER 94
2036      007574  007646      T55      I ADDRESS OF NEXT ROUTINE
2037      007576  000012      10:      I TEST ITERATION COUNT
2038      007600  007602      E3A      I SCOPE ENTRY POINT
2039      000094      X=X+1      |
2040      |
2041      |.....|
2042      007602  104004      E3AI  SRESET      I TEST THAT SCAN ERROR SETS SCAN VALUE TO ALL ONES
2043      007604  012777  000416  171400      MOV      @BITC1@BIT2,@UDCR      I SET MAINT,DEF INT,DEF SCAN EN,IMM EN
2044      007612  104010      DELAY      I WAIT 1 MS
2045      007614  000001
2046      007616  127727  171372  000377      CMPB     @UDSR,@377      I CHECK IF SCAN VALUE 377
2047      007624  001402      BEQ      ,+6      I BRANCH IF SCAN = 377
2048      007626  104007      ERRORS
2049      007630  104005      SCOPE
2050      007632  104004      SRESET
```

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2051 007634 100777 171354          TSTB   0UDSR          IDID RESET CLEAR SCAN REGISTER?
2052 007640 001401          BEQ     ,+4          IBRANCH IF CLEARED
2053 007642 104007          ERRORS
2054 007644 104005          SCOPE
2055
2056 |-----|
2057 007646 000055          T59i   95           IROUTINE NUMBER 95
2058 007650 007736          T56           IADDRESS OF NEXT ROUTINE
2059 007652 000144          100.         ITEST ITERATION COUNT
2060 007654 007656          E4A         ISCOPE ENTRY POINT
2061          000055          X=X+1
2062 |-----|
2063 ITEST THAT DEF SCAN START CLEARS SCAN ERROR + DEF SCAN DONE
2064 007656 012777 000412 171326          E4Ai   MOV     @BITC1,0UDCR ISET MAINT,DEF INT+SCAN EN
2065 007664 104010          DELAY
2066 007666 000001          1           IWAIT UNTIL ERROR AND DONE SETS
2067 007670 042777 000012 171314          BIC     @BIT1|BIT3,0UDCR ISET DEF INT EN LOW+HIGH+CLEAR DEF SCAN EN
2068 007676 052777 000002 171306          BIS     @BIT1,0UDCR   ITO CLEAR SCAN EN+DONE
2069 007704 000240          NOP
2070 007706 032777 100000 171276          BIT     @BIT15,0UDCR IWAIT FOR DLY CLEAR DONE
2071 007714 001402          BEQ     ,+4          IDID SCAN ERROR CLEAR?
2072 007716 104007          ERRORS          IBRANCH IF CLEAR
2073 007720 104005          SCOPE
2074 007722 032777 000040 171262          BIT     @BIT9,0UDCR   IDID DEF SCAN DONE CLEAR?
2075 007730 001401          BEQ     ,+4          IBRANCH IF CLEAR
2076 007732 104007          ERRORS
2077 007734 104005          SCOPE
2078
2079 |-----|
2080 007736 000056          T56i   96           IROUTINE NUMBER 96
2081 007740 010064          T57           IADDRESS OF NEXT ROUTINE
2082 007742 000144          100.         ITEST ITERATION COUNT
2083 007744 007746          E5A         ISCOPE ENTRY POINT
2084          000056          X=X+1
2085 |-----|
2086 ITEST THAT DEF SCAN ENABLE WILL INHIBIT SCAN + RIF CLEARS DONE
2087 007746 012777 000403 171236          E5Ai   MOV     @BITC2|BIT8,0UDCR ISET MAINT,RIF+DEF INT
2088 007754 104010          DELAY
2089 007756 000001          1           IWAIT, SCAN SHOULD NOT START
2090 007760 032777 000040 171224          BIT     @BIT9,0UDCR   ICHECK IF DEF SCAN DONE CLEAR
2091 007766 001402          BEQ     ,+4          IBRANCH IF CLEAR
2092 007770 104007          ERRORS
2093 007772 104005          SCOPE
2094 007774 052777 000014 171210          BIS     @BIT3|BIT2,0UDCR ISET DEF SCAN EN,IMM INT
2095 010002 104010          DELAY
2096 010004 000001          1           IWAIT FOR ERROR+DONE
2097 010006 042777 000400 171176          BIC     @BIT8,0UDCR   ICLEAR TO PREVENT NEW SCAN
2098 010014 032777 000001 171170          BIT     @BIT8,0UDCR   IDID RIF STAY SET?
2099 010022 001002          BNE     ,+4          IBRANCH IF SET
2100 010024 104007          ERRORS
2101 010026 104005          SCOPE
2102 010030 009777 171204          TST     0UDCA6          IADDRESS MOD TO RIF
2103 010034 000240          NOP
2104 010036 032777 100040 171146          BIT     @BIT15|BIT9,0UDCR IDID RIF CLEAR ERROR+DONE?
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2105	010044	001401			BEG	.+4		IBRANCH IF CLEAR	
2106	010046	104007			ERRORS				
2107	010050	032777	000001	171134	BIT	#BIT0,0UDCR		IS RIP STILL SET?	
2108	010056	001001			BNE	.+4		IBRANCH IF SET	
2109	010060	104007			ERRORS			ICLEARED IN ERROR	
2110	010062	104005			SCOPE				
2111									
2112									
2113	010064	000057							
2114	010066	010146			T57:	57		IROUTINE NUMBER 57	
2115	010070	001750				T60		IAADDRESS OF NEXT ROUTINE	
2116	010072	010074				1000,		ITEST ITERATION COUNT	
2117		000057				E6A		ISCOPE ENTRY POINT	
2118						X0X+1			
2119									
2120	010074	012777	001412	171110	ITEST THAT Y FAULT CAN BE GENERATED IN DEF MODE, NO TRAPS P9=7	E6A:	MOV	#BIT9,0UDCR	ISSET MAIN?, DEF INT+SCAN, STOP Y
2121	010102	104010					DELAY	IWAIT IMS	
2122	010104	000001							
2123	010106	032777	100000	171076			BIT	#BIT15,0UDCR	ITEST IF SCAN ERROR SET
2124	010114	001002					BNE	.+6	IBRANCH IF SET
2125	010116	104007					ERRORS		
2126	010120	104005					SCOPE		
2127	010122	032777	000040	171062			BIT	#BIT5,0UDCR	ITEST IF DEF DONE SET
2128	010130	001002					BNE	.+6	IBRANCH IF SET
2129	010132	104007					ERRORS		
2130	010134	104005					SCOPE		
2131	010136	042777	000001	171046			BIC	#BIT0,0UDCR	IGENERATE RIP
2132	010144	104005					SCOPE		
2133									
2134									
2135	010146	000060							
2136	010150	010230					T60:	60	IROUTINE NUMBER 60
2137	010152	001750						T61	IAADDRESS OF NEXT ROUTINE
2138	010154	010156						1000,	ITEST ITERATION COUNT
2139		000060						E7A	ISCOPE ENTRY POINT
2140								X0X+1	
2141									
2142	010156	012777	003412	171026	ITEST THAT WD FAULT CAN BE GENERATED IN DEF MODE, NO TRAPS P5=7	E7A:	MOV	#BIT6,0UDCR	ISSET MAIN?, DEF INT+SCAN, STOP WD
2143	010164	104010					DELAY	IWAIT IMS	
2144	010166	000001							
2145	010170	032777	100000	171014			BIT	#BIT15,0UDCR	ITEST IF SCAN ERROR SET
2146	010176	001002					BNE	.+6	IBRANCH IF SET
2147	010200	104007					ERRORS		
2148	010202	104005					SCOPE		
2149	010204	032777	000040	171000			BIT	#BIT5,0UDCR	ITEST IF DEF DONE SET
2150	010212	001002					BNE	.+6	IBRANCH IF SET
2151	010214	104007					ERRORS		
2152	010216	104005					SCOPE		
2153	010220	042777	000001	170764			BIC	#BIT0,0UDCR	IGENERATE RIP
2154	010226	104005					SCOPE		
2155									
2156									
2157	010230	000061							
2158	010232	010310					T61:	61	IROUTINE NUMBER 61
								T62	IAADDRESS OF NEXT ROUTINE

```
2159 010234 001790          1000,          ;TEST ITERATION COUNT
2160 010236 010240          E8A           ;SCOPE ENTRY POINT
2161          000001          X=X+1          ;
2162          ;
2163          ;
2164 010240 012777 007402 170744 ;TEST THAT DEF INT WITH STOP X,Y,WD SET WILL NOT SET ERROR
2165 010246 052777 000010 170736 E8A1  MOV  @BITC2IBITC9,0UDCR  ISET MAINT,DEF INT EN,STOP X+Y+WD
2166 010254 104010          DELAY          ;WAIT FOR SCAN DONE
2167 010256 000001          1
2168 010260 032777 100000 170724 BIT  @BIT15,0UDCR  ;CHECK THAT SCAN ERR DID NOT SET
2169 010266 001402          BEQ  ,+4       ;BRANCH IF CLEAR
2170 010270 104007          ERRORS
2171 010272 104005          SCOPE
2172 010274 032777 000040 170710 BIT  @BIT5,0UDCR  ;CHECK IF DEF SCAN DONE SET
2173 010302 001001          BNE  ,+4       ;BRANCH IF DONE SET
2174 010304 104007          ERRORS
2175 010306 104005          SCOPE
2176          ;
2177          ;
2178 010310 000062          T621  62       ;ROUTINE NUMBER 62
2179 010312 010366          T63       ;ADDRESS OF NEXT ROUTINE
2180 010314 001790          1000,      ;TEST ITERATION COUNT
2181 010316 010320          E9A       ;SCOPE ENTRY POINT
2182          000062          X=X+1          ;
2183          ;
2184          ;
2185 010320 012777 007402 170664 E9A1  MOV  @BITC2IBITC9,0UDCR  ISET MAINT,DEF INT,STP X,Y,WD
```

2197	010326	052777	000010	170656	BIS	#BIT3,0UDCR	ISET DEF SCAN EN
2198	010334	104010			DELAY		IWAIT FOR DONE
2199	010336	000001			1		
2200	010340	109777	170650		TSTB	0UDSR	ITEST FOR SCAN OF 0
2201	010344	001402			BEO	,+6	
2202	010346	104007			ERRORS		
2203	010350	104005			SCOPE		
2204	010352	022777	017452	170632	CHP	#17452,0UDCR	IDEF INT,STP X,Y,W0,MAINT,DEF DONE
2205	010360	001401			BEO	,+6	IDEF SCAN EN,DEF INT
2206	010362	104007			ERRORS		
2207	010364	104005			SCOPE		
2208							
2209					.....		
2210	010366	000063			T63I	63	IROUTINE NUMBER 63
2211	010370	010456				T64	IADDRESS OF NEXT ROUTINE
2212	010372	000144				100,	ITEST ITERATION COUNT
2213	010374	010376				F1A	ISCOPE ENTRY POINT
2214		000063				X+X+1	
2215					.....		
2216					ITEST THAT IMM INT CAN BE GENERATED BY MAINT+IMM INT EN		
2217	010376	012777	000404	170606	F1A1	MOV	#BITC4,0UDCR
2218	010404	032777	020000	170600		BIT	#BIT13,0UDCR
2219	010412	001002				BNE	,+6
2220	010414	104007			ERRORS		IBRANCH IF SET
2221	010416	104005			SCOPE		
2222	010420	032777	010000	170564	BIT	#BIT12,0UDCR	ICHECK IF DEF INT SET
2223	010426	001402			BEO	,+6	IBRANCH IF CLEAR
2224	010430	104007			ERRORS		
2225	010432	104005			SCOPE		
2226	010434	042777	000400	170550	BIC	#BIT0,0UDCR	ICLEAR MAINT
2227	010442	032777	020000	170542	BIT	#BIT13,0UDCR	ICHECK IF IMM INT CLEAR
2228	010450	001401			BEO	,+6	IBRANCH IF CLEAR
2229	010452	104007			ERRORS		
2230	010454	104005			SCOPE		
2231							
2232					.....		
2233	010456	000064			T64I	64	IROUTINE NUMBER 64
2234	010460	010564				T65	IADDRESS OF NEXT ROUTINE
2235	010462	000012				10,	ITEST ITERATION COUNT
2236	010464	010466				F2A	ISCOPE ENTRY POINT
2237		000064				X+X+1	
2238					.....		
2239					ITEST THAT IMM SCAN STARTS AND SETS SCAN ERROR, NO TRAP PS07		
2240	010466	104004			F2A1	SRESET	
2241	010470	012777	000424	170514		MOV	#BITC3,0UDCR
2242	010476	104010				DELAY	ISET MAINT,IMM INT,IMM SCAN EN
2243	010500	000001			1		IWAIT IMS
2244	010502	032777	100000	170502	BIT	#BIT15,0UDCR	IDID SCAN ERROR SET?
2245	010510	001002			BNE	,+6	IBRANCH IF BIT IS SET
2246	010512	104007			ERRORS		
2247	010514	104005			SCOPE		
2248	010516	032777	000200	170466	BIT	#BIT7,0UDCR	IDID SCAN ERROR SET IMM DONE?
2249	010524	001002			BNE	,+6	IBRANCH IF BIT IS SET
2250	010526	104007			ERRORS		

Address	Hex	Dec	Hex	Hex	Code	Comment
2251	010530	104005			SCOPE	
2252	010532	104004			SRESET	
2253	010534	032777	100000	170450	BIT #BIT15,0UDCR	!DID SCAN ERROR CLEAR?
2254	010542	001402			BEG ,+6	!BRANCH IF CLEAR
2255	010544	104007			ERRORS	
2256	010546	104005			SCOPE	
2257	010550	032777	000200	170434	BIT #BIT7,0UDCR	!DID IMM SCAN DONE CLEAR?
2258	010556	001401			BEG ,+6	!BRANCH IF CLEAR
2259	010560	104007			ERRORS	
2260	010562	104005			SCOPE	
2261						
2262						
2263	010564	000005				
2264	010566	010640				
2265	010570	000012				
2266	010572	010574				
2267		000005				
2268						
2269						
2270	010574	104004				
2271	010576	012777	000424	170406		
2272	010604	032777	000001	170400		
2273	010612	001402				
2274	010614	104007				
2275	010616	104005				
2276	010620	104010				
2277	010622	000001				
2278	010624	022777	120624	170360		
2279	010632	001401				
2280	010634	104007				
2281	010636	104005				
2282						
2283						
2284	010640	000006				
2285	010642	010730				
2286	010644	000144				
2287	010646	010650				
2288		000006				
2289						
2290						
2291	010650	012777	000424	170334		
2292	010656	104010				
2293	010660	000001				
2294	010662	042777	000004	170322		
2295	010670	052777	000004	170314		
2296	010676	000240				
2297	010700	017700	170306			
2298	010704	032700	100000			
2299	010710	001402				
2300	010712	104005				
2301	010714	104007				
2302	010716	032700	000100			
2303	010722	001401				
2304	010724	104007				

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2305 010726 104005          SCOPE
2306
2307 |
2308 010730 000067          T67i  67          ;ROUTINE NUMBER 67
2309 010732 011090          T70    T70          ;ADDRESS OF NEXT ROUTINE
2310 010734 000144          100.    ;TEST ITERATION COUNT
2311 010736 010740          F4A    ;SCOPE ENTRY POINT
2312 000067          X=X+1
2313 |
2314 |TEST THAT IMM SCAN ENABLE WILL INHIBIT SCAN + RIF CLEARS DONE
2315 010740 012777 000404 170244 F4Ai  MOV    #BITC4,UDCR ;SET MAIN+IMM INT
2316 010746 104010          DELAY   ;WAIT SCAN SHOULD NOT START
2317 010750 000001          1
2318 010752 032777 000100 170232 BIT    #BIT6,UDCR  ;CHECK IF IMM SCAN DONE CLEAR
2319 010760 001402          BEQ    ,+6        ;BRANCH IF CLEAR
2320 010762 104007          ERRORS
2321 010764 104005          SCOPE
2322 010766 052777 000020 170216 BIS    #BIT4,UDCR  ;SET IMM SCAN ENABLE
2323 010774 104010          DELAY   ;WAIT FOR ERROR AND DONE
2324 010776 000001          1
2325 011000 042777 000400 170204 BIC    #BIT8,UDCR  ;CLEAR TO PREVENT NEW SCAN
2326 011006 052777 000001 170176 BIS    #BIT0,UDCR  ;SET RIF
2327 011014 032777 100200 170170 BIT    #BIT15|BIT9,UDCR ;IS ERROR + DONE STILL SET?
2328 011022 001001          ONE    ,+6        ;BRANCH IF SET
2329 011024 104007          ERRORS ;SETTING RIF FLOP CLEARED ERROR OR DONE
2330 011026 009777 170210 TST    UDCA7      ;ADDRESS MODULE TO RIF
2331 011032 000240          NOP
2332 011034 032777 100200 170190 BIT    #BIT15|BIT9,UDCR ;WAIT FOR DEL CLEAR DONE
2333 011042 001401          BEQ    ,+6        ;DID RIF CLEAR ERROR + DONE
2334 011044 104007          ERRORS ;BRANCH IF CLEAR
2335 011046 104005          SCOPE
2336
2337 |
2338 011050 000070          T70i  70          ;ROUTINE NUMBER 70
2339 011052 011132          T71    T71          ;ADDRESS OF NEXT ROUTINE
2340 011054 001790          1000.  ;TEST ITERATION COUNT
2341 011056 011060          F5A    ;SCOPE ENTRY POINT
2342 000070          X=X+1
2343 |
2344 |TEST THAT Y FAULT CAN BE GENERATED IN IMM MODE, NO TRAPS PS=7
2345 011060 012777 001424 170124 F5Ai  MOV    #BITC7,UDCR ;SET MAIN, IMM INT+SCAN, STOP Y
2346 011066 104010          DELAY   ;WAIT IMS
2347 011070 000001          1
2348 011072 032777 100000 170112 BIT    #BIT15,UDCR ;TEST IF SCAN ERROR SET
2349 011100 001002          ONE    ,+6        ;BRANCH IF SET
2350 011102 104007          ERRORS
2351 011104 104005          SCOPE
2352 011106 032777 000200 170076 BIT    #BIT7,UDCR  ;TEST IF IMM DONE SET
2353 011114 001002          ONE    ,+6        ;BRANCH IF SET
2354 011116 104007          ERRORS
2355 011120 104005          SCOPE
2356 011122 042777 000001 170062 BIC    #BIT8,UDCR  ;GENERATE RIF
2357 011130 104005          SCOPE
2358

```

```

2359
2360 011132 000071
2361 011134 011214
2362 011136 001750
2363 011140 011142
2364 000071
2365
2366
2367 011142 012777 003424 170042
2368 011150 104010
2369 011152 000001
2370 011154 032777 100000 170030
2371 011162 001002
2372 011164 104007
2373 011166 104005
2374 011170 032777 000200 170014
2375 011176 001002
2376 011200 104007
2377 011202 104005
2378 011204 042777 000001 170000
2379 011212 104005
2380
2381
2382 011214 000072
2383 011216 011274
2384 011220 001750
2385 011222 011224
2386 000072
2387
2388
2389 011224 012777 007404 167760
2390 011232 052777 000020 167752
2391 011240 104010
2392 011242 000001
2393 011244 032777 100000 167740
2394 011252 001402
2395 011254 104007
2396 011256 104005
2397 011260 032777 000200 167724
2398 011266 001001
2399 011270 104007
2400 011272 104005
2401
2402
2403 011274 000073
2404 011276 011352
2405 011300 001750
2406 011302 011304
2407 000073
2408
2409
2410 011304 012777 007404 167700
2411 011312 052777 000020 167672
2412 011320 104010

```

```

.....
T71: 71
T72
1000,
F6A
X=X+1
ROUTINE NUMBER 71
ADDRESS OF NEXT ROUTINE
TEST ITERATION COUNT
SCOPE ENTRY POINT

```

```

.....
ITEST THAT WD FAULTY CAN BE GENERATED IN IMM MODE, NO TRAPS PS=7
F6A: MOV #BITC0,0UDCR ISET MAINT, IMM INT+SCAN, STOP WD
      DELAY
      1
      BIT #BIT15,0UDCR ITEST IF SCAN ERROR SET
      BNE ,+6 IBRANCH IF SET
      ERRORS
      SCOPE
      BIT #BIT7,0UDCR ITEST IF IMM DONE SET
      BNE ,+6 IBRANCH IF SET
      ERRORS
      SCOPE
      BIC #BIT2,0UDCR IGENERATE RIF
      SCOPE

```

```

.....
T72: 72
T73
1000,
F7A
X=X+1
ROUTINE NUMBER 72
ADDRESS OF NEXT ROUTINE
TEST ITERATION COUNT
SCOPE ENTRY POINT

```

```

.....
ITEST THAT IMM INT WITH STOP X,Y, WD SET WILL NOT SET ERROR
F7A: MOV #BITC4|BITC9,0UDCR ISET MAINT, IMM INT EN, STP X+Y+WD
      BIS #BIT4,0UDCR ISET IMM SCAN EN
      DELAY
      1
      BIT #BIT15,0UDCR ICHECK THAT SCAN ERROR DID NOT SET
      BEQ ,+6 IBRANCH IF CLEAR
      ERRORS
      SCOPE
      BIT #BIT7,0UDCR ICHECK IF IMM SCAN DONE SET
      BNE ,+6 IBRANCH IF DONE SET
      ERRORS
      SCOPE

```

```

.....
T73: 73
T74
1000,
F8A
X=X+1
ROUTINE NUMBER 73
ADDRESS OF NEXT ROUTINE
TEST ITERATION COUNT
SCOPE ENTRY POINT

```

```

.....
ITEST THAT IMM INT WITH STOP X+Y, WD SET WILL SCAN TO 0
F8A: MOV #BITC4|BITC9,0UDCR ISET MAINT, IMM INT EN, STP X+Y+WD
      BIS #BIT4,0UDCR ISET IMM SCAN EN
      DELAY

```

```

2413 011322 000001          1
2414 011324 109777 167664  TSTB  UDCR          ITEST FOR SCAN ADR OF 0
2415 011330 001402          BEQ    ,+6
2416 011332 104007          ERRORS
2417 011334 104005          SCOPE
2418 011336 022777 027624 167646  CMP    #27624,UDCR  IDEF INT,STOP X+Y+WD,MAINT,IMM DONE
2419 011344 001401          BEQ    ,+4          IDEF SCAN EN,DEF INT+RIF SET
2420 011346 104007          ERRORS
2421 011350 104005          SCOPE
2422
2423
2424 011352 000074          I
2425 011354 011404          T74:  74          IROUTINE NUMBER 74
2426 011356 000031          T75          IADDRESS OF NEXT ROUTINE
2427 011360 011362          25;          ITEST ITERATION COUNT
2428          000074          G1A          ISCOPE ENTRY POINT
2429          X=X+1
2430
2431 011362 104004          ITEST THAT DEF VALID SETS
2432 011364 016701 167622  G1A:  SRESET
2433 011370 012700 001000          MOV    UDCR,X1          IMOVE ADDRESS INT: R0
2434 011374 012777 006412 167610  MOV    #BIT9,X0
2435 011402 050011          MOV    #BITC1|BIT11|BIT10,UDCR  ISET MAINT,DEF INT,SCAN EN
2436 011404 104010          BIS    X0,(1)          ISET STOP X
2437 011406 000001          DELAY
2438 011410 052777 000024 167574  BIS    #BIT2|BIT4,UDCR          ISET IMM + SCAN EN
2439 011416 032777 100000 167570  BIT    #BIT15,UDCR          IDEF VALID SHOULD BE SET
2440 011424 001002          BNE    ,+6          IBRANCH IF DEF VALID SET
2441 011426 104007          ERRORS
2442 011430 104005          SCOPE
2443 011432 104010          DELAY
2444 011434 000001          I
2445 011436 109777 167552  TSTB  UDCR          IIS SCAN 0?
2446 011442 001402          BEQ    ,+6          IBRANCH IF SCAN IS 0
2447 011444 104007          ERRORS
2448 011446 104005          SCOPE
2449 011450 022777 037676 167534  CMP    #37676,UDCR  IIMM+DEF INT,STP X+Y+WD,MAINT
2450 011456 001401          BEQ    ,+4          IIMM+DEF DONE,SCAN EN,INT EN
2451 011460 104007          ERRORS
2452 011462 104005          SCOPE
2453
2454
2455 011464 000075          I
2456 011466 011566          T79:  75          IROUTINE NUMBER 75
2457 011470 000031          T76          IADDRESS OF NEXT ROUTINE
2458 011472 011474          25;          ITEST ITERATION COUNT
2459          000075          G2A          ISCOPE ENTRY POINT
2460          X=X+1
2461
2462 011474 104004          ITEST THAT IMM INT OVERRIDES DEF
2463 011476 016701 167510  G2A:  SRESET
2464 011502 012700 000004          MOV    UDCR,X1          IMOVE ADDRESS I NTO R0
2465 011506 012777 000432 167476  MOV    #BIT2,X0
2466 011514 050011          MOV    #BITC1|BIT2,UDCR          ISET MAINT,DEF INT,SCAN ENABS
2466          BIS    X0,(1)          ISET IMM INT
  
```





```
2521 011734 022777 027624 167250      CMP      #27624,0UDCR      IMM INT,STOP X+Y+WD
2522 011742 001401      BEQ      ,+4              IMINT,IMM DONE,IMM SCAN EN,IMM INT SET
2523 011744 104007      ERRORS
2524 011746 104005      SCOPE
2525 011750 104007      G3ERRXi ERRORS          ITRAPPED WHILE SERVICING TRAP
2526 011752 104005      SCOPE
2527
2528
2529 011754 000100      T100i   100              IROUTINE NUMBER 100
2530 011756 012074      T101    T101              IADDRESS OF NEXT ROUTINE
2531 011760 000144      100.    100.              ITEST ITERATION COUNT
2532 011762 011764      G4A     G4A              ISCOPE ENTRY POINT
2533 000100      X=X+1
2534
2535
2536 011764 012777 012036 167224      G4Ai   MOV      #G4OK,OUTV      IPRIME FOR GOOD RETURN
2537 011772 012777 000000 167220      MOV      #PRTY6,OUPL
2538 012000 012767 000000 165770      MOV      #PRTY6,PS
2539 012006 016701 167200      MOV      UDCR,X1          IMOVE ADDRESS INTO R1
2540 012012 012700 001000      MOV      #BIT9,X0         IPUT STOP X IN R0
2541 012016 012777 006412 167166      MOV      #BITC1IBIT9IBIT1,UDCR
2542 012024 050011      BIS      X0,(1)          ISET STOP X TO STOP SCAN
2543 012026 104010      DELAY
2544 012030 000001      1
2545 012032 104007      ERRORS          ISHOULD TRAP BEFORE GETTING HERE
2546 012034 104005      SCOPE
2547 012036 012777 012070 167152      G40Ki  MOV      #G4ERRX,OUTV     IPRIME FOR SERVICE TRAP
2548 012044 009777 167142      TST      0UDCR           IADDRESS CONTROL TO SEE IF
2549 012050 009777 167140      TST      0UDSR           ITHIS CAUSES SERVICE TRAP
2550 012054 022777 017452 167130      CMP      #17452,0UDCR    IDEF DONE,SCAN EN,INT
2551 012062 001401      BEQ      ,+4              ISTOP X+Y+WD
2552 012064 104007      ERRORS
2553 012066 104005      SCOPE
2554 012070 104007      G4ERRXi ERRORS          ITRAPPED WHILE SERVICING TRAP
2555 012072 104005      SCOPE
2556
2557
2558 012074 000101      T101i   101              IROUTINE NUMBER 101
2559 012076 012204      T102    T102              IADDRESS OF NEXT ROUTINE
2560 012100 000144      100.    100.              ITEST ITERATION COUNT
2561 012102 012104      G5A     G5A              ISCOPE ENTRY POINT
2562 000101      X=X+1
2563
2564
2565 012104 012777 012154 167104      G5Ai   MOV      #G5ERR,OUTV     IPRIME FOR ERROR RETURN
2566 012112 012777 000300 167100      MOV      #PRTY6,OUPL
2567 012120 012767 000300 165650      MOV      #PRTY6,PS          ISET PS=6
2568 012126 016701 167060      MOV      UDCR,X1          IMOVE ADDRESS INTO R0
2569 012132 012700 002000      MOV      #BIT10,X0        IPUT STOP Y IN R0
2570 012136 012777 005424 167046      MOV      #BITC3IBIT9IBIT1,UDCR ISET MAINT,IMM INT,IMM SCAN EN
2571 012144 050011      BIS      X0,(1)          ISET STOP Y TO STOP SCAN
2572 012146 104010      DELAY
2573 012150 000001      1
2574 012152 000402      BR      ,+6              IWAIT,NO TRAP SHOULD OCCUR
                                IBRANCH IF NO TRAP
```

```

2575 012154 104007          G5ERRI  ERRORS          IMM TRAP WHEN PS=6
2576 012156 104005          SCOPE
2577 012160 012777 012202 167030  MOV      @G5OK,OUTV    PRIME FOR GOOD RETURN
2578 012166 012767 000240 165602  MOV      @PRTY5,PS     LOWER PS TO 5
2579 012174 000240          NOP
2580 012176 000240          NOP
2581 012200 104007          ERRORS          INO TRAP PS=5
2582 012202 104005          SCOPE
2583
2584
2585 012204 000102          T1021  102          ROUTINE NUMBER 102
2586 012206 012314          T103          ADDRESS OF NEXT ROUTINE
2587 012210 000144          100,         TEST ITERATION COUNT
2588 012212 012214          G6A         SCOPE ENTRY POINT
2589          000102          X=X+1
2590
2591
2592 012214 012777 012264 166774  ITEST THAT DEF TRAPS AT CORRECT RR LEVEL
2593 012222 012777 000200 166770  G6AI  MOV      @G6ERR,OUTV  PRIME FOR ERROR RETURN
2594 012230 012767 000200 165540  MOV      @PRTY4,DUPL
2595 012236 016701 166750  MOV      @PRTY4,PS     ISET PS=4
2596 012242 012700 001000  MOV      UDCR,X1      MOVE ADDRESS INTO R0
2597 012246 012777 006412 166736  MOV      @BIT0,X0      PUT STOP X IN R0
2598 012254 050011          BIS      X0,(1)       ISET MAINT,DEF INT,SCAN EN
2599 012256 104010          DELAY
2600 012260 000001          1
2601 012262 000402          BR      ,+6
2602 012264 104007          G6ERRI  ERRORS          IDEF TRAPPED WHEN PS=4
2603 012266 104005          SCOPE
2604 012270 012777 012312 166720  MOV      @G6OK,OUTV    PRIME FOR GOOD RETURN
2605 012276 012767 000140 165472  MOV      @PRTY3,PS     LOWER PS TO 3
2606 012304 000240          NOP
2607 012306 000240          NOP
2608 012310 104007          ERRORS          INO TRAP PS=3
2609 012312 104005          SCOPE
2610
2611
2612 012314 000103          T1031  103          ROUTINE NUMBER 103
2613 012316 012410          T104          ADDRESS OF NEXT ROUTINE
2614 012320 001750          1000,        TEST ITERATION COUNT
2615 012322 012324          G7A         SCOPE ENTRY POINT
2616          000103          X=X+1
2617
2618
2619 012324 012777 012404 166664  ITEST THAT DATA TRANSFERS WILL NOT CAUSE FALSE TRAPS
2620 012332 012777 000036 166692  G7AI  MOV      @G7ERR,OUTV  PRIME FOR ERROR RETURN
2621 012340 012767 000000 165430  MOV      @36,UDCR     ISET IMM+DEF INT+SCAN ENAB
2622 012346 012777 177777 166690  MOV      @PRTY0,PS     ISET PS TO 0
2623 012354 000777 166644  MOV      @177777,@UMOD  LOAD UDC BUS WITH ONES
2624 012360 001402          TST      @UMOD        UDC BUS SHOULD BE 0
2625 012362 104007          BEQ      ,+6
2626 012364 104005          ERRORS          SCOPE
2627 012366 000077 166632  CLR      @UMOD        CLEAR UDC BUS
2628 012372 000777 166626  TST      @UMOD

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2629 012376 001401          BEQ      ,+4
2630 012400 104007          ERRORS
2631 012402 104005          SCOPE
2632 012404 104007          G7ERRI  ERRORS          ;DATA TRANSFERS CAUSED TRAP
2633 012406 104005          SCOPE
2634
2635 |
2636 012410 000104          T104:  104          ;ROUTINE NUMBER 104
2637 012412 012506          T105          ;ADDRESS OF NEXT ROUTINE
2638 012414 001750          1000.        ;TEST ITERATION COUNT
2639 012416 012420          G0A          ;SCOPE ENTRY POINT
2640          000104          X=X+1
2641 |
2642 |-----|
2643 012420 012777 012502 166570  ;TEST THAT DATA TRANSFERS WILL NOT CAUSE FALSE TRAPS
2644 012426 012777 000036 166556  G0A:  MOV      #G0ERR,OUTV ;PRIME FOR ERROR RETURN
2645 012434 012767 060000 165334  MOV      #36,UDCR      ;SET IMM+DEF INT AND SCAN ENAB
2646 012442 012777 125252 166554  MOV      #PRTY0,PS     ;SET PS TO 0
2647 012450 005777 166550          MOV      #125252,UMOD ;LOAD UDC BUS WITH PATTERN
2648 012454 001402          TST      UMOD          ;UDC BUS SHOULD BE 0
2649 012456 104007          BEQ      ,+6
2650 012460 104005          ERRORS
2651 012462 012777 052525 166534  MOV      #52525,UMOD  ;LOAD COMPLIMENT PATTERN
2652 012470 005777 166530          TST      UMOD
2653 012474 001401          BEQ      ,+4
2654 012476 104007          ERRORS
2655 012500 104005          SCOPE
2656 012502 104007          G0ERRI  ERRORS          ;DATA TRANSFERS CAUSED TRAP
2657 012504 104005          SCOPE
2658 |
2659 |-----|
2660 012506 000105          T105:  105          ;ROUTINE NUMBER 105
2661 012510 012572          T106          ;ADDRESS OF NEXT ROUTINE
2662 012512 000144          100.         ;TEST ITERATION COUNT
2663 012514 012516          G9A          ;SCOPE ENTRY POINT
2664          000105          X=X+1
2665 |
2666 |-----|
2667 | AND DOES NOT TRAP WITH IMM INT DISABLED
2668 012516 012777 012566 166472  G9A:  MOV      #G0ERR,OUTV ;PRIME FOR ERROR RETURN
2669 012524 012767 000240 165244  MOV      #PRTY5,PS     ;SET PS=5
2670 012532 012777 000412 166452  MOV      #BITC1,UDCR   ;SET MAIN,DEF INT+SCAN EN
2671 012540 104010          DELAY
2672 012542 000001          1
2673 012544 012777 012570 166444  MOV      #G9OK,OUTV   ;PRIME FOR GOOD RETURN
2674 012552 052777 000004 166432  BIS      #BIT2,UDCR   ;ENABLE IMM INT
2675 012560 104010          DELAY
2676 012562 000001          1
2677 012564 104007          ERRORS
2678 012566 104007          G9ERRI  ERRORS          ;NO TRIP WITH IMM INT EN
2679 012570 104005          G9OKI   SCOPE          ;TRAP OCCURRED WITH IMM INT DISABLED
2680 |
2681 |-----|
2682 012572 000106          T106:  106          ;ROUTINE NUMBER 106
```

2683 012574 177777  
2684 012576 000001  
2685 012600 012602  
2686 000106  
2687  
2688  
2689 012602 104005  
2690 000001

TLAST  
1  
EZA  
X=X+1  
|.....|  
DUMMY END TEST  
EZA1 SCOPE  
.END

iADDRESS OF NEXT ROUTINE  
iTEST ITERATION COUNT  
iSCOPE ENTRY POINT  
i

ADTENP	002370	A1A	004152	A1B	004166	A1PA	004524
A10B	004540	A11A	004556	A11B	004572	A2A	004224
A2B	004220	A3A	004236	A3B	004252	A4A	004270
A4B	004304	A5A	004322	A5B	004336	A6A	004354
A6B	004370	A7A	004406	A7B	004422	A8A	004440
A8B	004454	A9A	004472	A9B	004506	BDCNV	002224
BDCNVA	002256	BDCNVB	002310	BDCNVC	002312	BDCNVD	002314
BITC1	000412	BITC2	000402	BITC3	000424	BITC4	000404
BITC5	001412	BITC6	003412	BITC7	001424	BITC8	003424
BITC9	007000	BIT0	000001	BIT1	000002	BIT10	002000
BIT11	004000	BIT12	010000	BIT13	020000	BIT14	040000
BIT15	100000	BIT2	000004	BIT3	000010	BIT4	000020
BIT5	000040	BIT6	000100	BIT7	000200	BIT8	000400
BIT9	001000	BMOVA	002420	BMOVE	002410	B1A	004610
B2A	004714	B3A	004774	B4A	005054	B5A	005134
B6A	005214	B7A	005274	B8A	005354	B9A	005434
CHAINN	001424	CHALT	104003	CHLT	002714	CHNA	001500
CHNAA	001516	CHNAB	001472	CHNAC	001462	CHNB	001536
CNVCTR	002362	CURTST	004134	C1A	005914	C1PA	006110
C11A	006144	C12A	006200	C13A	006234	C14A	006270
C15A	006324	C16A	006360	C17A	006414	C2A	005550
C3A	005604	C4A	005640	C5A	005674	C6A	005730
C7A	005764	C8A	006020	C9A	006054	DECVL	002402
DELAY	104010	D:BIT	002364	DLY	002752	DLVA	002762
DLVB	002766	D1A	006440	D2A	006664	D3A	007120
EMALT	104017	EHLT	002074	EHLTA	002104	EMTA	002674
EMTINT	002650	EMTLM	004120	EMTAB	004060	EMTV	000030
EMTX	000020	ERR	001720	ERRA	001770	ERRB	002054
ERRC	002060	ERRD	002070	ERRE	002072	ERROR	104002
ERRORS	104007	ERROR1	104006	ERRST	001644	ERR1	001742
E1A	007254	E2A	007344	E2BA	007452	E2CA	007526
E3A	007602	E4A	007656	E5A	007746	E6A	010074
E7A	010156	E8A	010240	E9A	010320	FORWD	001604
F1A	010376	F2A	010466	F2BA	010574	F3A	010650
F4A	010740	F5A	011060	F6A	011142	F7A	011224
F8A	011304	GETRDY	001300	GTRDYA	001342	GTRDYC	001362
GTRDYD	001404	GTRDYX	001306	G1A	011362	G2A	011474
G2AA	011576	G2AAER	011630	G3A	011644	G3ERRX	011750
G3OK	011716	G4A	011764	G4ERRX	012070	G4OK	012036
G5A	012104	G5ERR	012154	G5OK	012202	G6A	012214
G6ERR	012264	G6OK	012312	G7A	012324	G7ERR	012404
G8A	012420	G8ERR	012502	G9A	012516	G9ERR	012566
G9OK	012570	ICNT	004124	ICTR	004122	LOGIC	001572
MACHER	000004	MCLK	001222	MEO	003100	MICNT	003212
MINCRT	003356	MPC	003174	MPGEND	004051	MPUDC	003571
MPUDNG	003721	MPUDOK	003645	MPHRF	003532	MPURT	003453
MSETSR	003264	MSTR	003223	MTIT	003376	MTNUM	003161
MUDCR	003233	MUDSR	003251	NOP	000240	NXYSY	004132
OACNV	002136	OACNVA	002152	OACNVX	002222	OPEN	000000
PC	0000007	POPSP	005726	POPSP2	0022626	PRTY0	000000
PRTY1	000040	PRTY2	000100	PRTY3	000140	PRTY4	000200
PRTY5	000240	PRTY6	000300	PRTY7	000340	PS	177776
PUSH	005746	PUSH2	024646	PWFDC	002620	PWFDCX	002640
PWRDN	002432	PWRDT	002566	PWRFL	000024	PWRSTY	002466

PWRUP	002442	PWRUT	002576	PWUDC	002520	PWUDCA	002540
RST04	104012	RST05	104016	RST05S	104014	RSP4	003076
RS05	003130	RS05S	003124	RYNNO	004130	R0	X000000
SAV04	104011	SAV05	104013	SAV05S	104015	SCOPE	104005
SCOPTR	004126	SP	X000000	SR	177570	SRESET	104004
SRSETT	002730	START	001250	SUBTEN	002322	SUBTNA	002326
SUBTNB	002342	SV04	003002	SV05	003032	SV05A	003040
SV05B	003052	SV05C	003066	SV05S	003022	TENPHR	002366
TKB	001204	TKS	001202	TLAST	177777	TP0	001210
TPS	001206	TRPV	000034	TYPE	104000	TPES	104001
TYP5	002106	TYPSA	002130	TYPSB	002132	T0	004142
T1	004174	T10	004462	T100	011754	T101	012074
T102	012204	T103	012314	T104	012410	T105	012506
T106	012572	T11	004514	T12	004546	T13	004600
T14	004704	T15	004764	T16	005044	T19	005124
T2	004226	T20	005204	T21	005264	T22	005344
T23	005424	T24	005504	T25	005540	T26	005574
T27	005630	T3	004260	T30	005664	T31	005720
T32	005754	T33	006010	T34	006044	T39	006100
T36	006134	T37	006170	T4	004312	T40	006224
T41	006260	T42	006314	T43	006350	T44	006404
T45	006430	T46	006654	T47	007110	T5	004344
T50	007244	T51	007334	T52	007442	T53	007516
T54	007572	T55	007646	T56	007736	T59	010064
T6	004376	T60	010146	T61	010230	T62	010310
T63	010366	T64	010456	T65	010564	T66	010640
T67	010730	T7	004430	T70	011050	T71	011132
T72	011214	T73	011274	T74	011352	T75	011464
T76	011566	T77	011634	UDCA1	001226	UDCA2	001230
UDCA3	001232	UDCA4	001234	UDCA5	001236	UDCA6	001240
UDCA7	001242	UDCA8	001244	UDCA9	001246	UDCR	001212
UDCRT	004136	UDBR	001214	UDSRT	004140	UMOD	001224
UPL	001220	UTV	001216	X	000106	ZZA	012602
SFILLS	001201	SNULL	001200	STYPE	001100	.	012604

ERRORS DETECTED: 0

DZUDB-B CONTROL TEST MACY11,623 14-FEB-73 20194 PAGE 36-12  
UDC118, SRC

•,UDC118/N-SYSMAC.SML,UDC118, SRC  
RUN-TIME: 15 28 0 SECONDS  
CORE USED: 8K