

DQ11

INTERRUPT LOGIC TEST
MD-11-DZDQC-C

EP-DZDQC-C-DL-A

NOV 1976

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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-D2100-C-D
PRODUCT NAME: D011 INTERRUPT LOGIC TESTS
DATE: 21 JUNE 1976
MAINTAINER: DIAGNOSTIC GROUP

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1. ABSTRACT

THE FUNCTION OF THE DZ11 DIAGNOSTICS ARE TO VERIFY THAT THE OPTION OPERATES ACCORDING TO SPECIFICATIONS.

THIS TEST CHECKS ALL POSSIBLE INTERRUPTS VERIFYING THAT AN INTERRUPT OCCURS WHEN IT SHOULD AND THAT ONE DOESN'T HAPPEN WHEN IT SHOULDN'T.
ALSO THAT THE INTERRUPTS OCCUR TO THE CORRECT VECTOR.
BASIC NPR FUNCTIONS ARE ALSO INCLUDED IN THIS TEST.

CURRENTLY THERE ARE SEVEN OFF LINE DIAGNOSTICS THAT ARE TO BE RUN IN SEQUENCE TO INSURE THAT IF AN ERROR SHOULD OCCUR IT WILL BE DETECTED AT AN EARLY STAGE AND INSURING THAT DIAGNOSIS OF ERROR WILL BE IMMEDIATE TO PROBLEM.
NOTE: ADDITIONAL DIAGNOSTICS MAY BE ADDED IN THE FUTURE.

THE SEVEN DIAGNOSTICS ARE:

1. DZ00A [REV] BASIC R/W TEST #1
2. DZ00B [REV] BASIC R/W TEST #2
3. DZ00C [REV] BASIC NPR AND INTERRUPT TEST
4. DZ00D [REV] RECEIVER TRANSMITTER EXERCISER TEST
5. DZ00E [REV] MISC. RX AND TX TESTS. PLUS 900 TESTS.
6. DZ00F [REV] CHARACTER DETECT TESTS.
7. DZ00H [REV] CHARACTER LENGTH AND INTERRUPT TESTS.

THERE IS ALSO AN ONLINE TEST TO BE DISCUSSED LATER.
1. DZ00G [REV] ONLINE TEST. (ITEP OVERLAY)

AND A PARAMETER INPUT PROGRAM IS AVAILABLE
1. DZ00G [REV] DZ11 TRIAL PROGRAM (PARAMETER INPUT)

2. REQUIREMENTS

2.1 EQUIPMENT

ANY PDP-11 FAMILY CPU (WITH MINIMUM 4K MEMORY)-WITH OR WITHOUT A HARDWARE SWITCH REGISTER (LOC. 177570)
ASR 33 (C. EQUIVALENT)
DZ11
SYNC MODEM (ONLY REQUIRED FOR ONLINE TEST)

2.2 STORAGE

PROGRAM WILL LOAD AND RUN IN 4K OF MEMORY.

LOCATIONS 1400 THRU 1600 ARE ESPECIALLY TO BE NOTED AND TO BE UNTOUCHED BY OPERATOR AFTER D011 TRIAL PROGRAM HAS BEEN EXECUTED. OR AFTER THE "AUTO SIZING" HAS BEEN DONE.

3. LOADING PROCEEDURE

3.1 METHOD

ALL PROGRAMS ARE IN ABSOLUTE FORMAT AND ARE LOADED USING THE ABSOLUTE LOADER.

ABSOLUTE LOADER STARTING ADDRESS +500

MEMORY *
 SIZE

4K	17
8K	37
12K	57
16K	77
20K	117
24K	137
28K	157

3.1.1 LOAD THE ADDRESS OF ABS. LOADER (LOC.XXX500)

3.1.2 THEN START

4. STARTING PROCEEDURE

- A. LOAD LOC. 200
- B. SET SWR TO ZERO FOR "AUTO SIZING" OR LEAVE
 LEAVE SWR BIT 7=1 TO USE EXISTING PARAMETERS SET UP
 BY D011 TRIAL PROGRAM OR A PREVIOUSLY RUN D011 DIAGNOSTIC
 THAT USED THE "AUTO SIZING".
 ****REFER TO SECTION 4.1 FOR SOFTWARE SWITCH REGISTER OPERATION
 AND OPTIONS.****
 NOTE: THE SOFTWARE SWITCH REGISTER IS LOCATED AT LOC.176
 SOFTWARE DISPLAY REGISTER IS LOCATED AT LOC.174

C. THEN START
 THE PROGRAM WILL TYPE MAINDEC NAME AND PROGRAM NAME
 IF THIS WAS THE FIRST START UP OF THE PROGRAM) AND ALSO
 THE FOLLOWING:

"MAP OF D011 STATUS"

1400	160010
1402	152300
1404	160020
1406	15031C

THE ABOVE IS ONLY AN EXAMPLE!

THIS WOULD INDICATE THE STATUS TABLE STARTING AT ADD.
1400 IN THE PROGRAM. THE STATUS TABLE MUST BE VERIFIED BY THE
USER IF AUTO SIZING IS DONE. FOR INFORMATION OF STATUS
TABLE SEE SECTION 8.4 FOR HELP.

****IF THE SOFTWARE SWITCH REGISTER IS SELECTED THEN THE FOLLOWING
WILL BE TYPED AFTER THE PROGRAM IDENTIFIES ITSELF:
SWR=XXXXXX NEW= (REFER TO SECTION 4.1 FOR OPERATOR'S OPTION)****
NOTE: IF USING THE SOFTWARE SWITCH REGISTER WHEN A HARDWARE
SWITCH REGISTER IS AVAILABLE THE PROGRAM WILL NOT
TYPE OUT THE TITLE.

THE PROGRAM WILL TYPE "R"
AND PROCEED TO RUN THE DIAGNOSTIC

4.1 CONTROL SWITCH SETTINGS

IF THE DIAGNOSTIC IS RUN ON A CPU WITHOUT A SWITCH
REGISTER THEN A SOFTWARE SWITCH REGISTER IS USED WHICH ALLOWS
THE USER THE SAME SWITCH OPTIONS AS THE HARDWARE SWITCH REGISTER.
IF THE HARDWARE SWITCH REGISTER DOES NOT EXIST OR IF ONE DOES
AND IT CONTAINS ALL ONES (177777) THEN THE SOFTWARE SWITCH
REGISTER (LOC. 176) IS USED.

CONTROL:

THIS PROGRAM ALSO SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH
REGISTER (LOC. 176) FROM THE TTY. THIS CAN BE ACCOMPLISHED BY
DOING THE FOLLOWING:

- 1) TYPE CONTROL G (<13>); THIS WILL ALLOW THE TTY TO ENTER DATA INTO
LOC. 176 AT SELECTED POINTS WITHIN THE PROGRAM.
- 2) THE MACHINE WILL THEN TYPE: SWR=XXXXXXNEW= (XXXXXX IS THE COTAL CONTENTS
OF THE SOFTWARE SWITCH REGISTER.)
- 3) AFTER THE "NEW=" HAS BEEN TYPED THEN THE OPERATOR CAN DO ONE
OF THE FOLLOWING AT THE TTY:
 - A) TYPE A NUMBER TO BE LOADED INTO LOC. 176 FOLLOWED BY A <CR>.
(ONLY NUMBERS BETWEEN 0-7 WILL BE ACCEPTED AND ONLY 6 NUMBERS
WILL BE ALLOWED)
IF A <CR> IS THE FIRST KEY DEPRESSED THE SOFTWARE SWITCH
REGISTER CONTENTS WILL NOT BE CHANGED.
 - B) IF A CONTROL U (<1U>) IS DEPRESSED THEN THE PROGRAM WILL SEND YOU
BACK TO STEP 2.

SW 15	SET: HALT ON ERROR
SW 14	SET: LOOP ON CURPENT TEST
SW 13	SET: INHIBIT ERROR PRINT OUT
SW 12	SET: INHIBIT TYPE OUT/BELL ON ERROR.
SW 11	SET: INHIBIT ITERATIONS

SW 10 SET: ESCAPE TO NEXT TEST
 SW 09 SET: LOOP WITH CURRENT DATA
 SW 08 SET: CATCH ERROR AND LOOP ON IT
 SW 07 SET: USE PREVIOUS STATUS TABLE. CLR-DO AUTO SIZE.
 SW 06 SET:
 SW 05 SET:
 SW 04 SET:
 SW 03 SET:
 SW 02 SET: LOCK ON SELECTED TEST
 SW 01 SET: RESTART PROGRAM AT SELECTED TEST
 SW 00 SET: RESELECT DQ11'S DESIRED ACTIVE.

4.1.2 SWITCH REGISTER RESTRICTIONS

SW 00 RESELECT DQ11'S DESIRED ACTIVE.
 PLEASE NOTE THAT A MESSAGE IS TYPED
 OUT FOR SWITCH REGISTER BEING EQUAL TO DQ11'S
 ACTIVE. THIS MEANS IF THE SYSTEM HAS
 FOUR DQ11S; BITS 00,01,02,03 WILL
 BE SET IN LOC "DQACTV". USING THIS
 SWITCH ALTERS THAT LOCATION; THEREFORE
 IF FOUR DQ11S ARE IN THE SYSTEM
 DO NOT SET SWITCHS GREATER THAN
 SW 03 IN THE UP POSITION. THIS WOULD BE
 A FATAL ERROR. DO NOT SELECT MORE ACTIVE
 DQ11S THAN HAS BEEN GIVEN INFORMATION
 ABOUT IN TRIAL PROGRAM.

METHOD: A: LOAD ADDRESS 100
 B: START WITH SW 00=1
 C: PROGRAM WILL TYPE MESSAGE
 D: CONTINUE THE BINARY NUMBER OF DQ11S DESIRED ACTIVE
 EXAMPLE: 1=1 DQ11; 2=2 DQ11; 7=3 DQ11; 17=4 DQ11 37=5 DQ11 ETC.
 E: NUMBER (IF VALID) WILL BE IN DATA LIGHTS (EXCLUDING 11/05, 11/04, 11/34)
 F: CONTINUE WITH ANY OTHER SWITCH SETTINGS DESIRED.

SW 01 IT IS STRONGLY SUGGESTED THAT
 AT LEAST ONE PASS HAS BEEN MADE
 BEFORE TRYING TO SELECT A TEST
 THAT IS NOT IN THE ORDER OF SEQUENCE
 THE REASON BEING IS THAT THE
 PROGRAM HAS TO CLEAR AREAS AND SET
 UP PARAMETERS. ALSO WHEN A TEST IS
 SELECTED ALWAYS START AT THE VERY
 BEGINNING OF THAT TEST.

SW 09 LOOP ON CURRENT DATA:
 THIS SWITCH WILL ONLY WORK IF
 CALL "SCOPI" IS IN THAT TEST.
 THE REASON, BEING THAT MOST TESTS
 DEAL WITH BLOCKS OF DIFFERENT DATA
 TO BE SENT OR RECEIVED ALL AT ONCE
 THUS IN BLOCK DATA; ONE PATTERN CANN'T BE SINGLED OUT.

4.1.3 SWITCH REGISTER PRIORITYS

ERROR SWITCHES

1. SW 12 DELETE PRINT OUT/BELL ON ERROR.
2. SW 13 DELETE ERROR PRINTOUT.
3. SW 15 HALT ON THE ERROR.
4. SW 08 GOTO BEGINNING OF THE TEST.
5. SW 10 GOTO NEXT TEST ON ERROR.

HLT (ERROR) ROUTINE SUPPORTS <↑G> OPERATION

SCOPE SWITCHES

1. SW 09 (IF ENABLED BY "SCOPI")
2. SW 14
3. SW 11

SCOPE ROUTINE WILL SUPPORT <↑G> OPERATION

4.2 STARTING ADDRESS

STARTING ADDRESS IS AT 000200
THERE ARE NO OTHER STARTING ADDRESSES
FOR THE DQ11 DIAGNOSTICS PREVIOUSLY MENTIONED

NOTE: IF ADDRESS 000042 IS NON-ZERO
THE PROGRAM ASSUMES IT IS UNDER
ACT11 OR DDP CONTROL AND WILL ACT ACCORDINGLY
AFTER *ALL* AVAILABLE DQ11'S ARE TESTED
THE PROGRAM WILL RETURN TO "DDP2" OR "ACT-11".

5. OPERATING PROCEDURE

WHEN PROGRAM IS INITIALLY STARTED MESSAGES AS DESCRIBED IN SECTION
FOUR WILL BE PRINTED.

AND PROGRAM WILL BEGIN RUNNING THE
DIAGNOSTIC

5.2 PROGRAM AND/OR OPERATOR ACTION

THE TYPICAL APPROACH SHOULD BE

1. HALT ON ERROR (VIA SW 15=1)
WHEN EVER AN ERROR OCCURS
2. CLEAR SW 15
3. SET SW 14: (LOOP ON THIS TEST)
4. SET SW 13: (INHIBIT ERROR PRINT OUT)

THE TEST NUMBER AND PC WILL BE TYPED OUT AND
POSSIBLY AN ERROR MESSAGE (THIS DEPENDS ON THE TEST)
TO GIVE THE OPERATOR AN IDEA AS TO THE SOURCE OF THE
PROBLEM. IF IT IS NECESSARY TO KNOW MORE INFORMATION
CONCERNING THE ERROR REPORT; LOOK IN THE LISTING
FOR THAT TEST NUMBER WHICH WAS TYPED OUT
AND THEN NOTE THE PC OF THE ERROR REPORT
THIS WAY THE EXACT FUNCTIONING OF THE TEST

CAN BE INTERPEDITED

5. ERRORS

AS DESCRIBED PREVIOUSLY THERE WILL ALWAYS BE A TEST NUMBER AND PC TYPED OUT AT THE TIME OF AN ERROR (PROVIDING SW 13=0 AND SW 12=0). IN MOST CASES ADDITIONAL INFORMATION WILL BE SUPPLIED THE THE ERROR MESSAGE WHICH IS TO GIVE THE OPERATOR AN INDICATION OF THE ERROR.

5.2 ERROR RECOVERY

IF FOR SOME REASON THE DQ11 SHOULD "HANG THE BUS" (GAIN CONTROL OF BUS SO THAT CONSOLE MANUAL FUNCTIONS ARE INHIBITED) AN INIT OR POWER DOWN/UP IS NECESSARY FOR OPERATOR TO REGAIN CONTROL OF CPU. IF THIS SHOULD HAPPEN; LOOK IN LOCATION "TS*NO" (ADDRESS 1222) FOR THE NUMBER OF THE TEST THAT WAS RUNNING AT THE TIME OF THE CATASTROPHIC ERROR. IN THIS WAY THE OPERATOR WILL HAVE AN IDEA AS TO WHAT THE DQ11 WAS DOING AT THE TIME OF THE ERROR.

5.3 ****HALT RECOVERY WHEN USING SOFTWARE SWITCH REGISTER****

IF THE SOFTWARE SWITCH REGISTER IS TO BE CHANGED AFTER A HALT THE THE OPERATOR IS REQUIRED TO TYPE A (<G>) BEFORE DEPRESSING CONTINUE. THE FOLLOWING WILL BE TYPED:
SWR=XXXXXX NEW= (REFER TO SECTION 4.1 FOR OPERATOR OPTION)

7. RESTRICTIONS

7.1 STARTING RESTRICTIONS

SEE SECTION 4. (PLEASE)

7.2 OPERATING RESTRICTIONS

DQ11 TRIAL PROGRAM MUST BE RUN PRIOR TO THE FIRST AND ONLY THE FIRST RUNNING OF ANY DQ11 DIAGNOSTIC
NOTE: IF NO PROGRAM OTHER THAN A DQ11 DIAGNOSTIC WAS LOADED AFTER DQ11 TRIAL OR IF CORE MEMORY HAS NOT BEEN CHANGED; OR IF THERE IS NO DQ11 CONFIGURATION CHANGES; THE DQ11 TRIAL PROGRAM NEED NEVER BE RUN AGAIN. HOWEVER IF ANY OF THE ABOVE HAVE BEEN VIOLATED THE DQ11 TRIAL PROGRAM MUST BE RUN AGAIN BEFORE RUNNING THE DIAGNOSTICS
NOTE: AN ALTERNATIVE TO THE ABOVE IS ATTEMPTING THE "AUTO SIZING" WHEN PROGRAM IS INITIALLY STARTED WITH SW07=0.

9. MISCELLANEOUS

DZDQC MACY11 27(732) 24-SEP-76 10:14 PAGE 9
 DZDQCC.P11

8.1 EXECUTION TIME

8.2 PASS COMPLETE

WHEN THE DIAGNOSTIC HAS COMPLETED
 A PASS THE FOLLOWING IS AN EXAMPLE
 OF THE PRINT OUT TO BE EXPECTED.

END PASS DZDQC-C CSR: 160000 VEC: 300 PASSES: 000001 ERRORS: 000000

NOTE: THE NUMBERS FOR CSR AND VEC ARE
 NOT NECESSARILY THE VALUES FOR THE DEVICE
 THEY ARE ONLY FOR THIS EXAMPLE.

8.3 TST1 (MINI MONITOR)

THE VERY FIRST "TEST" (TST1)
 IS *NOT* A TEST OF THE DQ11 HARDWARE
 IT IS A MINI-MONITOR USED TO CYCLE DQ11 IN THE
 SYSTEM THROUGH THE DIAGNOSTIC.

REMEMBER: TST1 IS NOT A TEST OF DQ11 HARDWARE!!!!!!!

8.4 KEY LOCATIONS

RETURN (1210) CONTAINS THE ADDRESS WHERE PROGRAM WILL
 RETURN WHEN ITERATION COUNT IS REACHED
 OR IF LOOP ON TEST IS ASSERTED.

NEXT (1212) CONTAINS THE ADDRESS OF THE NEXT TEST
 TO BE PERFORMED.

TSTNO (1222) CONTAINS THE NUMBER OF THE TEST NOW
 BEING PERFORMED.

RUN (1272) THE BIT IN "RUN" ALWAYS POINTS ONE
 PAST THE DQ11 CURRENTLY BEING TESTED.

EXAMPLE:

(RUN) 1272/0000000001000000

MEANS THAT DQ11 NO.05 IS THE DQ1. NOW
 RUNNING.

DQCR00-DQCR17

DQST00-DQST17

(1400)-(1476)

THESE LOCATIONS CONTAIN THE INFORMATION
 NEEDED TO TEST UP TO 16 (DECIMAL) DQ11S
 SEQUENTIALY. THEY CONTAIN THE CSR, VECTOR
 AND STATUS CONCERNING THE CONFIGURATION
 OF EACH DQ11.

DQACTV (1500)

EACH BIT SET IN THIS LOCATION INDICATES
 THAT THE ASSOCIATED DQ11 WILL BE TESTED
 IN TURN.

EXAMPLE:

(DQACTV) 1500/000000000000111111

MEANS THAT DQ11 NO. 00,01,02,03,04
 WILL BE TESTED.

EXAMPLE:

(DQACTV) 1500/00000000000010001

MEANS THAT DQ11 NO. 00,04

DQCSR (1506) WILL BE TESTED.
 CONTAINS THE RECEIVER CSR OF THE
 CURRENT DQ11 UNDER TEST.
 DQSTAT (1510) CONTAINS THE STATUS OF THE CURRENT
 DQ11 UNDER TEST.
 BIT 15 SET: TWO SYNC CHARS/ONE SYNC CHAR
 BIT 14 SET: TEST JUMPER INSTALLED/NOT INSTALLED
 BIT 13 SET: BB OPTION INSTALLED/NOT INSTALLED
 BIT 12 SET: BA OPTION INSTALLED/NOT INSTALLED
 BIT 11 SET: ACTIVE ON FIRST NON-SYNC/ACTIVE AFTER NO. OF SYNC
 BIT 10 SET: AB OPTION INSTALLED/NOT INSTALLED
 BIT 09 SET: ODD VRC/EVEN VRC
 BIT 00-08 VECTOR "A" OF DEVICE

8.5 *** METHOD OF AUTO SIZING ***

8.5.1 FINDING THE CONTROL STATUS REGISTER.

WHEN LOOKING FOR THE CSR IT IS NECESSARY TO TAKE CARE
 THAT WHEN A CSR IS FOUND THAT IT IS INDEED A DQ11. THAT
 IS THE METHOD OF MY MADNESS FOR THIS ROUTINE.
 AN ATTEMPT TO CLEAR THE MISC. REGISTER IS TRIED
 IF A TIME-OUT TRAP OCCURES POINTERS ARE UPDATED
 AND ATTEMPTED AGAIN. IF NO TIME-OUT; THE RECEIVER "ACTIVE BIT" (BIT 12)
 IS SET AND A *COMPARE* FOR BOTH SYNC1 AND SYNC 2 IS DONE
 AT THE MISC. REGISTER. IF THEY ARE THERE THIS IS
 A DQ11. THE INFORMATION IS STORED AWAY.

8.5.2 ONE SYNC BIT OR TWO?

SINCE TOO MUCH HARDWARE MUST BE TURNED ON TO SENSE THE
 PRESENTS OF ONE SYNC OR TWO. THE PROGRAM ASSUMES TWO SYNC
 CHARS. NOTE: THIS ASSUMPTION MAY BE ALTERED AFTER AUTO SIZING
 BY ALTERING BIT 15 IN APPRIQATE DQSTXX: LOCATION.

8.5.3 "BB" OPTION INSTALLED?

TO SENSE FOR THE "BB" OPTION THE PROGRAM SELECTS THE
 CHARACTER DET. REGISTER AND THE LOADS IN ALL 1'S; IF
 ANY ONE OR COMBINATION OF BITS ARE SET THE BB OPTION
 IS ASSUMED TO EXIST.

8.5.4 "AB" OPTION INSTALLED?

TO SENSE FOR THE "AB" OPTION THE PROGRAM SELECTS THE
 POLYNOMIAL REGISTER AND WRITES ALL 1'S INTO IT; IF ANY
 ONE OR COMBINATION OF BITS ARE SET THE AB OPTION IS ASSUMED
 TO EXIST.

8.5.5 "BA" OPTION INSTALLED?

TO SENSE FOR "BA" OPTION REQUEST TO SEND AND DATA TERMINAL
 READY ARE SET; IF EITHER ONE OR BOTH ARE SET THE PROGRAM
 ASSUMES THE BA OPTION EXISTS

8.5.6 JUMPER ON END OF CABLE?

THE PROGRAM CHECKS TO SEE IF EITHER OR BOTH CLEAR TO SEND AND CARRIER ARE SET; IF SO THE PROGRAM ASSUMES THE TEST JUMPER IS ON THE END OF THE CABLE.

8.5.7 ACTIVE ON FIRST NON-SYNC?

SINCE TOO MUCH HARDWARE MUST BE TURNED ON TO SENSE FOR WHEN THE DQ11 GOES ACTIVE THE PROGRAM ASSUMES "ACTIVE ON FIRST NON-SYNC". NOTE: THIS CAN BE CHANGED BY ALTERING BIT 11 IN THE APPRIOATE DQSTXX: AFTER AUTO SIZING

8.5.8 SET FOR ODD OR EVEN PARITY?

AS ABOVE TOO MUCH HARDWARE IS NEED TO SENSE WHICH PARITY WAS SELECTED. SO THE PROGRAM ASSEMES ODD PARITY. NOTE: THIS CAN BE CHANGED BY ALTERING BIT 9 IN APPRIO-ATE DQSTXX: LOCATION. AFTER AUTO SIZING

8.5.9 FINDING THE VECTOR.

THE PROGRAM SETS "PRIMARY DONE" "SECONDAY DONE" AND "INTERUPT ENABLE" AND LOOKS FOR AN INTERUPT. IF IT INTERUPTS IT IS PICKED UP AND STORED AWAY. IF NO INTERUPT OCCURES THE PROGRAM ASSUMES VECTOR =300. THIS PROBLEM WILL BE FIXED IN ONE OF THE DIAGNOSTICS AND *AUTO SIZING* SHOULD BE REDONE TO GET THE CORRECT VECTOR.

9. PROGRAM DESCRIPTION

CONTAINED WITHIN LISTING

10. LISTING

FOLLOWING

532
531
530
529
528
527
526
525
524
523
522
521
520
519
518
517
516
515
514
513
512
511
510
509
508
507
506
505
504
503
502
501
500

177320

NON.EX=177320
.ENABLE AMA

:MAINDEC-11-DZDQC-C/<377>/DQ11 INTERRUPT AND NPR LOGIC TEST
:COPYRIGHT 1975, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754

:REVISED 21-JUNE-76 BY S. CARPENTER

: A)SUPPORTS SOFTWARE SWITCH REGISTER
: B)SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH REGISTER
: BY <↑G>.

:STARTING PROCEDURE

:LOAD PROGRAM

:LOAD ADDRESS 000200

:PRESS START

:PROGRAM WILL TYPE "MAINDEC-11-DZDQC-C/<377>/DQ11 INTERRUPT AND NPR LOGIC TEST"

:PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED

:AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE

:AND THEN RESUME TESTING

;SWITCH REGISTER OPTIONS

100000
040000
020000
010000
004000
002000
001000
000400
000100
000040
000020
000010
000004
000002
000001

SW15=100000
SW14=40000
SW13=20000
SW12=10000
SW11=4000
SW10=2000
SW09=1000
SW08=400
SW06=100
SW05=40
SW04=20
SW03=10
SW02=4
SW01=2
SW00=1

=1,HALT ON ERROR
=1,LOOP ON CURRENT TEST
=1,INHIBIT ERROR TYPEOUT
=1,DELETE TYPEOUT/BELL ON ERROR.
=1,INHIBIT ITERATIONS
=1,ESCAPE TO NEXT TEST ON ERROR
=1,LOOP WITH CURRENT DATA
=1,LOOP ON ERROR

:LOCK ON TEST SELECT
:RESTART PROGRAM AT SELECTED TEST
:RESELECT DQ11 DESIRED ACTIVE
:NOTE: THIS MUST NOT EXCEED ORIGINAL COUNT

570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
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606
607
608
609
610
611
612
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616
617
618
619
620
621
622
623
624
625

000000
000001
000002
000003
000004
000005
000006
000007

177570
177570
177776
001200

005746
005726
010046
012600
024646
022626

100000
040000
020000
010000
004000
002000
001000
000400
000200
000100
000040
000020
000010
000004
000002
000001

002000
004000
010000
020000
040000

;REGISTER DEFINITIONS

R0=%0 :GENERAL REGISTER
 R1=%1 :GENERAL REGISTER
 R2=%2 :GENERAL REGISTER
 R3=%3 :GENERAL REGISTER
 R4=%4 :GENERAL REGISTER
 R5=%5 :GENERAL REGISTER
 SP=%6 :PROCESSOR STACK POINTER
 PC=%7 :PROGRAM COUNTER

;LOCATION EQUIVALENCIES

DSWR= 177570 ;HARDWARE SWITCH REGISTER LOC.
 DLIGHTS=177570 ;HARDWARE DISPLAY REGISTER LOC.
 PS=177776 ;PROCESSOR STATUS WORD
 STACK=1200 ;START OF PROCESSOR STACK

;INSTRUCTION DEFINITIONS

PUSH1SP=5746 ;DECREMENT PROCESSOR STACK 1 WORD
 POP1SP=5726 ;INCREMENT PROCESSOR STACK 1 WORD
 PUSHRO=10046 ;SAVE R0 ON STACK
 POPFD=12600 ;RESTORE R0 FROM STACK
 PUSH2SP=24646 ;DECREMENT STACK TWICE
 POP2SP=22626 ;INCREMENT STACK TWICE
 .EQUIV EMT,HLT ;BASIC DEFINITION OF ERROR CALL

BIT15=100000
 BIT14=40000
 BIT13=20000
 BIT12=10000
 BIT11=4000
 BIT10=2000
 BIT9=1000
 BIT8=400
 BIT7=200
 BIT6=100
 BIT5=40
 BIT4=20
 BIT3=10
 BIT2=4
 BIT1=2
 BIT0=1

;DQ11 OPTIONAL DEFINITIONS

ABBIT=2000
 ACTBIT=4000
 BABIT=10000
 BBBIT=20000
 JUMBIT=40000

626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650

001000
100000

00DBIT=1000
SYNBIT=100000

:DQ11 SECONDARY REGISTER DEFINATIONS

000000
000001
000002
000003
000004
000005
000006
000007

RXBA.P=0
RXWC.P=1
TXBA.P=2
TXWC.P=3
RXBA.S=4
RXWC.S=5
TXBA.S=6
TXWC.S=7

;RECEIVER BUS ADDRESS PRIMARY.
;RECEIVER WORD COUNT PRIMARY.
;TRANSMITTER BUS ADDRESS PRIMARY.
;TRANSMITTER BUS ADDRESS PRIMARY.
;RECEIVER BUS ADDRESS SECONDARY.
;RECEIVER WORD COUNT SECONDARY.
;TRANSMITTER BUS ADDRESS SECONDARY.
;TRANSMITTER WORD COUNT SECONDARY.

000010
000011
000012
000013
000014
000015
000016
000017

CHARDT=10
SYNC.=11
MISC.=12
TX.MUX=13
SEQ.=14
RX.BCC=15
TX.BCC=16
POLY.=17

; CHARACTER DETECT REGISTER.
; SYNC REGISTER.
; MISCELLANEOUS REGISTER.
; TRANSMITTER MUX REGISTER.
; SEQUENCE REGISTER.
; RECEIVER BCC REGISTER.
; TRANSMITTER BCC REGISTER.
; POLYNOMIAL REGISTER.

000514	000516	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000516	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000520	000522	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000522	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000524	000526	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000526	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000530	000532	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000532	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000534	000536	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000536	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000540	000542	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000542	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000544	000546	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000546	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000548	000550	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000550	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000552	000554	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000554	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000556	000558	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000558	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000560	000562	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000562	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000564	000566	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000566	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000570	000572	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000572	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000574	000576	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000576	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000600	000602	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000602	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000604	000606	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000606	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000610	000612	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000612	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000614	000616	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000616	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000620	000622	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000622	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000624	000626	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000626	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000630	000632	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000632	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000634	000636	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000636	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000640	000642	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000642	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000644	000646	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000646	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000650	000652	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000652	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000654	000656	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000656	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000660	000662	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000662	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000664	000666	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000666	000000	HALT	: EXAMINE STACK TO FIND CAUSE
000670	000672	.+2	: UNEXPECTED TRAP TO THIS LOCATION
000672	000000	HALT	: EXAMINE STACK TO FIND CAUSE

9075	000674	000676	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9076	000676	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9077	000700	000702	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9078	000702	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9079	000704	000706	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9080	000706	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9081	000710	000712	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9082	000712	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9083	000714	000716	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9084	000716	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9085	000720	000722	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9086	000722	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9087	000724	000726	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9088	000728	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9089	000730	000732	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9090	000732	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9091	000734	000736	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9092	000736	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9093	000740	000742	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9094	000742	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9095	000744	000746	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9096	000746	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9097	000750	000752	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9098	000752	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9099	000754	000756	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9100	000756	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9101	000760	000762	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9102	000762	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9103	000764	000766	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9104	000766	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9105	000770	000772	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9106	000772	000000	HALT	:EXAMINE STACK TO FIND CAUSE
9107	000774	000776	.+2	:UNEXPECTED TRAP TO THIS LOCATION
9108	000776	000000	HALT	:EXAMINE STACK TO FIND CAUSE

965		000220		.=220			
966	000220	012702	001400	CSRMAP:	MOV	#1400,R2	
967	000224	005022			CLR	(R2)+	
968	000226	022702	001512		CMP	#1512,R2	
969	000232	001374			BNE	.-6	
970	000234	005037	001504		CLR	DQNUM	
971	000240	012702	001400		MOV	#1400,R2	
972	000244	012701	160000		MOV	#160000,R1	
973	000250	012737	000614	000004	MOV	#53,2#4	
974	000256	112761	000012	000005	1\$:	MOVB	#12,5(R1)
975	000264	005061	000006		CLR	6(R1)	
976	000270	012711	010000		MOV	#10000,(R1)	
977	000274	022761	030000	000006	CMP	#30000,6(R1)	
978	000302	001071			BNE	2\$	
979	000304	010122			MOV	R1,(R2)+	
980	000306	052712	100000		BIS	#SYNBIT,(R2)	
981	000312	005011			CLR	(R1)	
982	000314	112761	000010	000005	MOVB	#10,5(R1)	
983	000322	012761	177777	000006	MOV	#-1,6(R1)	
984	000330	005761	000006		TST	6(R1)	
985	000334	001402			BEQ	.-+6	
986	000336	052712	020000		BIS	#BBBIT,(R2)	
987	000342	112761	000017	000005	MOVB	#17,5(R1)	
988	000350	012761	177777	000006	MOV	#-1,6(R1)	
989	000356	005761	000006		TST	6(R1)	
990	000362	001402			BEQ	.-+6	
991	000364	052712	002000		BIS	#ABBIT,(R2)	
992	000370	012761	001400	000002	MOV	#1400,2(R1)	
993	000376	032761	001400	000002	BIT	#1400,2(R1)	
994	000404	001402			BEQ	.-+6	
995	000406	052712	010000		BIS	#BABIT,(R2)	
996	000412	032761	030000	000002	BIT	#30000,2(R1)	
997	000420	001402			BEQ	.-+6	
998	000422	052712	040000		BIS	#JUMBIT,(R2)	
999	000426	052712	004000		BIS	#ACTBIT,(R2)	
1000	000432	052712	001000		BIS	#ODDBIT,(R2)	
1001	000436	005722			TST	(R2)+	
1002	000440	005011			CLR	(R1)	
1003	000442	005061	000002		CLR	2(R1)	
1004	000446	005061	000002		CLR	2(R1)	
1005	000452	005061	000004		CLR	4(R1)	
1006	000456	005061	000006		CLR	6(R1)	
1007	000462	005237	001504		INC	DQNUM	
1008	000466	062701	000010	2\$:	ADD	#10,R1	
1009	000472	022701	164000		CMP	#164000,R1	
1010	000476	001267			BNE	1\$	
1011	000500	005037	001500		CLR	DQACTV	
1012	000504	005737	001504		TST	DQNUM	
1013	000510	001434			BEQ	4\$	
1014	000512	013701	001504		MOV	DQNUM,R1	
1015	000516	010137	001276		MOV	R1,SAVNUM	
1016	000522	000241		3\$:	CLC		
1017	000524	006137	001500		ROL	DQACTV	
1018	000530	005237	001500		INC	DQACTV	
1019	000534	005301			DEC	R1	
1020	000536	001371			BNE	3\$	

```

: CLEAR ALL STATUS TABLE
: DO CLEAR
: ALL TABLE DONE
: BR IF MORE TO GO
: SET NUMBER OF DQ11S TO 0
: SET TABLE POINTER
: GET FIRST FLOATING ADDRESS
: SET FOR TIME OUT TRAP--NO DEVICE--
: TRY AND SEL MISC REGISTER
: TRY AND CLEAR MISC REG
: TRY AND SET RX ACTIVE
: LOOK FOR SYNC 1 AND SYNC 2
: THIS IS NOT A DQ11 IF I BRANCH
: NOW THIS IS A DQ11 --STORE CSR
: SET FOR TWO SYNC CHARS
: CLEAR DQ ACTIVE BIT
: SEL CHAR DET REGISTER
: WRITE INTO CHAR DET REG
: WAS THE REGISTER WRITTEN?
: APPARENTLY NO BB OPTION.
: SET FOR BB OPTION
: SEL POLYNO. REGISTER
: WRITE POLYNO. REGISTER
: WAS REG WRITTEN?
: BR IF NO AB OPTION
: SET FOR AB OPTION
: TRY TO SET .DTR. .RS.
: DID ANY OF THEM SET
: BR IF NO BA OPTION
: SET FOR BA OPTION
: DID .CS. .CO. SET
: BR IF NO JUMPER
: SET FOR JUMPER
: SET FOR ACTIVE ON FIRST NON-SYNC
: SET FOR ODD VRC.....
: POP POINTER
: CLEAR RCSR
: CLEAR TCSR
: CLEAR AGAIN
: CLEAR ERROR REG
: CLEAR SEC REG
: UPDATE NUMBER OF DQ11S
: UPDATE CSR POINTER BY 10 .9)
: HAVE ALL FLOATING ADDRESSES BEEN CHECKED??
: BR IF NOT ALL DONE
: ZERO ACTIVE DQ11S
: WERE ANY DQ11S FOUND
: HEY BUDDY. NO DQ11S FOUND IN SYSTEM
: SAVE NUMBER OF DQ11S
: SAVE NUMBER FOR ACT11
: CLEAR CARRY
: **** ACTIVE ADDRESS
: SET BIT 0
: DEC NUMBER OF DQ11S
: BR IF MORE TO GO
  
```

```

1021 000540 012737 000006 000004 MOV #6,J#4 ;RESET TIME OUT VECTOR
1022 000546 013737 001500 011502 MOV DQACTV,SAVACT ;SAVE ACTIVE
1023 000554 012737 000340 000022 MOV #340,J#22 ;SET IOT TRAP PRIO: TO 7
1024 000562 012702 001400 MOV #1400,R2 ;SET TABLE POINTER
1025 000566 012700 000300 MOV #300,R0 ;SET VECTOR START
1026 000572 012701 000302 MOV #302,R1 ;SET VECTOR+2 START
1027 000576 000137 000056 JMP VECMAP ;GO FIND THE VECTORS
1028 000602 104402 4$: TYPE ;TYPE MESSAGE
1029 000604 015125 MERR2 ;I DIDN'T FIND ANY DQ11S. DON'T USE AUTO SIZE.
1030 00060E 005000 CLR R0 ;
1031 000610 000000 HALT ;HOW CAN I TEST NO DQ11S
1032 000612 000776 BR -2 ;DON'T LET OPR HIT CONT. SW
1033 000614 012716 000466 5$: MOV #2$, (SP) ;ENTERED BY TIME OUT TRAP
1034 000620 000002 RTI ;GO HOME.
1035
1036
1037
1038 001000 005377 040515 047111 .=1000
1039 001006 042504 026503 030461 MTITLE: .ASCIZ <377><12> MAINDEC-11-DZDQC-C/<377>/DQ11 INTERRUPT AND NPR LOGIC TEST/<37
1040 001014 042055 042132 041521
1041 001022 041455 042377 030521
1042 001030 020061 047111 042524
1043 001036 051122 050125 020124
1044 001044 047101 020104 050116
1045 001052 020122 047514 044507
1046 001060 020103 042524 052123
1047 001066 000377
1048
1049 001200 .=1200
1050 ;INDIRECT POINTERS
1051
1052 001200 177570 SWR: 177570 ;SWITCH REGISTER POINTER
1053 001202 177570 LIGHTS: 177570 ;DISPLAY REGISTER POINTER
1054 001204 177560 TKCSR: 177560 ;TELETYPE KEYBOARD CONTROL REGISTER
1055 001206 177562 TKDBR: 177562 ;TELETYPE KEYBOARD DATA BUFFER
1056 001210 177564 TPCSR: 177564 ;TELEPRINTER CONTROL REGISTER
1057 001212 177566 TPDBR: 177566 ;TELEPRINTER DATA BUFFER
1058
1059 ;PROGRAM CONTROL PARAMETERS
1060
1061 001214 000000 RETURN: 0 ;SCOPE ADDRESS FOR LOOP ON TEST
1062 001216 000000 NEXT: 0 ;ADDRESS OF NEXT TEST TO BE EXECUTED
1063 001220 000000 LOCK: 0 ;ADDRESS FOR LOCK ON CURRENT DATA
1064 001222 000003 ICOUNT: 3 ;NUMBER OF ITERATIONS THAT CURRENT TEST WILL BE EXECUTED
1065 001224 000000 LPCNT: 0 ;NUMBER OF ITERATIONS COMPLETED
1066 001226 000000 TSTNO: 0 ;NUMBER OF TEST IN PROGRESS
1067 001230 000000 PASCNT: 0 ;NUMBER OF PASSES COMPLETED
1068 001232 000000 ERRCNT: 0 ;TOTAL NUMBER OF ERRORS
1069 001234 000000 LSTERR: 0 ;PC OF LAST ERROR CALL
1070
1071 ;PROGRAM VARIABLES
1072
1073 001236 000000 CHAR1: 0
1074 001240 000000 CHAR2: 0
1075 001242 000000 CHAR3: 0
1076 001244 000000 TEMP1: 0 ;TEMPORARY STORAGE

```

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DZDQCC.P11 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

1077	001246	000000	TEMP2:	0	: TEMPORARY STORAGE
1079	001250	000000	TEMP3:	0	: TEMPORARY STORAGE
1079	001252	000000	TEMP4:	0	: TEMPORARY STORAGE
1090	001254	000000	TEMP5:	0	: TEMPORARY STORAGE
1081	001256	000000	SAVR0:	0	: R0 STORAGE
1092	001260	000000	SAVR1:	0	: R1 STORAGE
1083	001262	000000	SAVR2:	0	: R2 STORAGE
1084	001264	000000	SAVR3:	0	: R3 STORAGE
1085	001266	000000	SAVR4:	0	: R4 STORAGE
1096	001270	000000	SAVR5:	0	: R5 STORAGE
1087	001272	000000	SAVSP:	0	: STACK POINTER STORAGE
1088	001274	000000	SAVPC:	0	: PROGRAM COUNTER STORAGE
1099	001276	000000	SAVNUM:	0	
1090	001300	000001	CREAM:	.BLKW 1	
1091	001302	000000	RUNFLG:	0	
1092	001304	000000	RUN:	0	
1093	001306	000000	RUNCNT:	0	

```

1094
1095
1096
1097 001310 000
1098 001311 000
1099 001312 000
1100 001313 000
1101 000000
1102
1103
1104
1105
1106
1107
1108
1109 001314
1110 104400
1111 001314 013020
1112 104401
1113 001316 013150
1114 104402
1115 001320 013170
1116 104403
1117 001322 013276
1118 104404
1119 001324 013414
1120 104405
1121 001326 013446
1122 104406
1123 001330 013662
1124 104407
1125 001332 013722
1126 104408
1127 001334 013754
1128 104411
1129 001336 013760
1130 104412
1131 001340 015620
1132 104413
1133 001342 015636
1134 104414
1135 001344 014662
1136 104415
1137 001346 014736
1138
1139
1140
1141
1142
1143
1144 001350 000000
1145 001352 000000
1146 001354 000000
1147 001356 000000
1148 001360 000000
1149 001362 000000

;PROGRAM CONTROL FLAGS
INIFLG: .BYTE 0 ;PROGRAM INITIALIZATION FLAG
STFLG: .BYTE 0 ;TEST START FLAG
ERRFLG: .BYTE 0 ;ERROR OCCURED FLAG
LOKFLG: .BYTE 0 ;LOCK ON CURRENT TEST FLAG
$Y=0

;DEFINITIONS FOR TRAP SUBROUTINE CALLS
;POINTERS TO SUBROUTINES CAN BE FOUND
;IN THE TABLE IMMEDIATLY FOLLOWING THE DEFINITIONS

;*****
;*****
;TRPTAB:
SCOPE=TRAP+0 ;CALL TO SCOPE LOOP AND ITERATION HANDLER
SCOPE
SCOPI=TRAP+1 ;CALL TO LOOP ON CURRENT DATA HANDLER
SCOPI
TYPE=TRAP+2 ;CALL TO TELETYPE OUTPUT ROUTINE
TYPE
INSTR=TRAP+3 ;CALL TO ASCII STRING INPUT ROUTINE
INSTR
INSTER=TRAP+4 ;CALL TO INPUT ERROR HANDLER
INSTER
PARAM=TRAP+5 ;CALL TO NUMERICAL DATA INPUT ROUTINE
PARAM
SAVOS=TRAP+6 ;CALL TO REGISTER SAVE ROUTINE
SAVOS
RESOS=TRAP+7 ;CALL TO REGISTER RESTORE ROUTINE
RESOS
CONVRT=TRAP+10 ;CALL TO DATA OUTPUT ROUTINE
CONVRT
CNVRT=TRAP+11 ;CALL TO DATA OUTPUT ROUTINE WITHOUT CR/LF.
CNVRT
MSTCLR=TRAP+12 ;CALL TO ISSUE MASTER CLEAR
MSTCLR
MEMCLR=TRAP+13 ;CALL TO CLEAR ALL SCRATCH PAD MEMORIES
MEMCLR
CKSWR=TRAP+14 ;CALL TO ALLOW SWREG TO BE LOADED FROM TTY
CKSWR
CNTLU=TRAP+15 ;CALL TO ALLOW LOADING OF SWREG FROM TTY
CNTLU

;****
;*****
;*****

;DQ11 VECTOR AND REGISTER INDIRECT POINTERS
DORVEC: 0 ;POINTER TO DQ11 RECEIVER INTERRUPT VECTOR
DQRLVL: 0 ;POINTER TO DQ11 RECEIVER INTERRUPT SERVICE PS
DQTEVC: 0 ;POINTER TO DQ11 TRANSMITTER INTERRUPT VECTOR
DQTLVL: 0 ;POINTER TO DQ11 TRANSMITTER INTERRUPT SERVICE PS
DQRCR: 0 ;POINTER TO DQ11 RECEIVER CONTROL REGISTER
DQRCSH: 0 ;POINTER TO HIGH BYTE OF DQ11 RECEIVER CONTROL REGISTER
    
```


M02

DZDQC MACY11 27(732) 24-SEP-76 10:14 PAGE 26
 DZDQCC.P11 PROGRAM INITIALIZATION AND START UP.

```

1206 001512 012737 000340 177776 .START: MOV #340,PS ;LOCK OUT INTERRUPTS
1207 001520 012706 001200 MOV #STACK,SP ;SET UP STACK
1208 001524 012737 014564 000024 MOV #.PFAIL,@#24 ;SET UP POWER FAIL VECTOR
1209 001532 013737 001504 001276 MOV DQNUM,SAVNUM
1210 001540 105037 001311 CLRB STFLG ;CLEAR START FLAG
1211 001544 005037 001230 CLR PASCNT ;CLEAR PASS CCUNT
1212 001550 105037 001312 CLRB ERRFLG ;CLEAR ERROR FLAG
1213 001554 005037 001302 CLR RUNFLG
1214 001560 012737 001400 001300 MOV #1400,CREAM
1215 001566 005037 001232 CLR ERRCNT ;CLEAR ERROR COJNT
1216 001572 005037 001234 CLR LSTERR ;CLEAR LAST ERROR POINTER
1217 001576 012737 000001 001226 MOV #1,TSTNO ;SET UP FOR TEST 1
1218 001604 012737 001512 001214 MOV #.START,RETURN ;SET UP FOR POWER FAIL BEFORE
1219 ;TESTING STARTS
1220 001612 105737 001310 TSTB INIFLG ;HAS INITIALIZATION BEEN PERFORMED
1221 001616 001075 BNE 12$
1222 001620 104402 001000 TYPE ,MTITLE ;TYPE TITLE MESSAGE
1223 001624 105137 001310 COMB INIFLG ;IF NOT SET FLAG AND DO
1224
1225 001630 012737 177570 001200 MOV #DSWR,SWR ;MOV HARDWARE SWR TO SWR
1226 001636 012737 177570 001202 MOV #DLIGHTS,LIGHTS ;MOV DISPLAY LIGHTS TO LIGHTS
1227 001644 013746 000006 MOV @#6,-(SP) ;SAVE VECTORS
1228 001650 013746 000004 MOV @#4,-(SP)
1229 001654 012737 001674 000004 MCV #64$,@#4 ;SET UP FOR TIMEOUT
1230 001662 022777 177777 177310 CMP #-1,@SWR ;REFERENCE HARDWARE SWITCH REGISTER
1231 001670 001402 BEQ 65$
1232 001672 000407 BR 66$
1233 001674 022526 64$: CMP (SP)+,(SP)+ ;ADJUST STACK
1234 001676 012737 000176 001200 65$: MOV #SWREG,SWR ;POINT TO SOFTWARE SWITCH REG
1235 001704 012737 000174 001202 MOV #DISPREG,LIGHTS ;POINT TO SOFT DISPLAY REG
1236 001712 012637 000004 66$: MOV (SP)+,@#4 ;RESTORE VECTORS
1237 001716 012637 000006 MOV (SP)+,@#6
1238 001722 005737 000042 TST @#42 ;UNDER MONITOR
1239 001726 001005 BNE 67$
1240 001730 022737 000176 001200 CMP #SWREG,SWR ;IS SWREG USED
1241 001736 001001 BNE 67$
1242 001740 104415 CNTLU
1243 001742 105777 177232 67$: TSTB @SWR
1244 001746 100402 BMI .+6
1245 001750 004737 000220 JSR PC,CSRMAP
1246 001754 104402 015412 TYPE ,XHEAD
1247 001760 012737 001400 001244 MOV #1400,TEMP1
1248 001766 017737 177252 001246 MOV @TEMP1,TEMP2
1249 001774 001406 BEQ .+16
1250 001776 104410 CONVRT
1251 002000 015440 XSTATQ
1252 002002 062737 000002 001244 ADD #2,TEMP1
1253 002010 000766 BR .-22
1254 002012 032777 000001 177160 12$: BIT #SW00,@SWR
1255 002020 001424 BEQ 1$
1256 002022 104402 TYPE
1257 002024 015333 MNEW
1258 002026 005000 CLR RG
1259 002030 000000 HALT
1260 002032 104414 CKSWR
1261 002034 027737 177140 001502 CMP @SWR,SAVACT

```


DZDQC MACY11 27(732) 24-SEP-76 10:14 PAGE 27
 DZDQCC.P11 PROGRAM INITIALIZATION AND START UP.

```

1262 002042 101404          BLOS      11$
1263 002044 104402          TYPE
1264 002046 015174          MERR3
1255 002050 000000          HALT
1256 002052 000776          BR        -2
1267 002054 017737 177120 001500 11$:  MOV      @SWR,DQACTV
1268 002062 013700 001500  MOV      DQACTV,R0
1269 002066 000000          HALT
1270 002070 104414          CKSWR
1271 002072 012700 00030C  1$:  MOV      #300,R0
1272 002076 012701 000302  MOV      #302,R1
1273 002102 010120          2$:  MOV      R1,(R0)+
1274 002104 005021          CLR      (R1)+
1275 002106 022021          CMP      (R0)+,(R1)+
1276 002110 022700 001000  CMP      #1000,R0
1277 002114 001372          BNE      2$
1278
1279          :TEST START AND RESTART
1280
1281 002116 012737 000340 177776 .BEGIN:  MOV      #340,PS          ;LOCK OUT INTERRUPTS
1282 002124 012706 001200  MOV      #STACK,SP      ;SET UP STACK
1283 002130 005737 000042  TST      @#42          ;IS PROGRAM UNDER MONITOR CONTROL
1284 002134 001040          BNE      3$
1285 002136 104414          CKSWR          ;CHECK FOR <↑G>
1286 002140 032777 000004 177032  BIT      #BIT2,@SWR      ;CHECK FOR LOCK ON TEST
1287 002146 001411          BEQ      1$
1288 002150 104402 015232          TYPE      ,MLOCK
1289 002154 012737 000240 013046  MOV      #NOP,TTST
1290 002162 012737 000240 013050  MOV      #NOP,TTST+2      ;SET UP TO LOCK
1291 002170 000406          BR        2$
1292 002172 013737 013144 013046 1$:  MOV      BRW,TTST
1293 002200 013737 013146 013050  MOV      BRX,TTST+2      ;LOCK NOT SELECTED, SET JP FOR NORMAL SCOPE LOOP
1294 002206 032777 000302 176764 2$:  BIT      #SW01,@SWR      ;IF SW01=1, GET STARTING PC
1295 002214 001410          BEQ      3$
1296 002216 104403          INSTR
1297 002220 015220          MTSTPC
1298 002222 104405          PARAM
1299 002224 002254          TST1
1300 002226 012442          TLAST
1301 002230 000207          RETURN
1302 002232 001          .BYTE 1
1303 002233 001          .BYTE 1
1304 002234 000403          BR        4$
1305 002236 012737 002254 001214 3$:  MOV      #TST1,RETURN      ;START AT TEST 1
1306 002244 104402 015122 4$:  TYPE      MR          ;TYPE R
1307 002250 000177 176740  JMP      @RETURN          ;START TESTING
1308
1309          : TEST 1
1310          ;*****
1310 002254 012737 000001 001226 1TST1: MOV      #1,TSTNO
1311 002262 012737 002644 001214  MOV      #TST2,RETURN
1312 002270 012737 002644 001216  MOV      #TST2,NEXT
1313 002276 105737 001302  TSTB     RUNFLG          ;IS THIS MY FIRST TIME HERE?
1314 002302 001010          BNE      1$          ;BR IF FLAG IS SET
1315 002304 012737 000001 001304  MOV      #BIT0,RUN          ;SET RUN POINTER.
1316 002312 012737 000020 001306  MOV      #16,RUNCNT      ;SET FOR MAX OF 16 DQ11'S PER S'STEM
1317 002320 105137 001302  COMB     RUNFLG          ;SET RUN FLAG

```

001304	071500	15:	BIT	RUN, DQACTV	: FIND AN ACTIVE DQ11 TO TEST.
001500			ONE	35	: BR IF I FOUND ONE TO TEST.
			TEST	DQACTV	: FIND OUT IF THERE ARE NO DQ11 ACTIVE.
			BEQ	25	: BR TO FATAL ERROR. WHY AM I HERE IF NO ACTIVE DQ11'S???
001304			CCC	RUN	: CLEAR ALL THE CONDITION CODES OF CPU
000004	001300		RCL	#4, CREAM	: UPDATE RUN POINTER
001306			ADD	RUNCNT	: UPDATE ADDRESS POINTER.
			DEC	15	: DEC NUMBER OF TIMES I LOOKED AT ACTIVE.
000020	001306		MOV	#16, RUNCNT	: BR AND KEEP LOOKING.
001500	001300		MOV	#1400, CREAM	: START RESTORING MY POINTERS.
000001	001304		MOV	#1, RUN	: RESTORE ADDRESS POINTER
			BR	15	: RESTORE RUN POINTER.
		25:	TYPE		: KEEP ON TESTING.
			HERE		: ALERT OPERATOR OF FATAL ERROR
			HALT		: NO DQ11 ACTIVE. WHY AM I HERE???
			BR		: YOU MUST RELOAD DQ11 DIAGNOSTIC!!
		33:	RCL		: STICK HERE ON CONT.
001304			RCL	RUN	: CLEAR CPU COND. CODES
001506	001506		MOV	#0, DQCSR	: UPDATE RUN. ACTIVE DQ11 FOUND.
000002	001300		ADD	#2, CREAM	: PLACE ADDRESS OF DQ11 AT DQCSR
001510	001510		MOV	#0, DQSTAT	: UPDATE ADDRESS POINTER
000002	001300		ADD	#2, CREAM	: PLACE STATUS OF DQ11 AT DQSTAT
001506	001300		MOV	DQCSR, DQCSR	: UPDATE ADDRESS POINTER
001510	001300		MOV	DQSTAT, DQSTAT	
001350	001350		BIT	#17700, DQARVEC	
			MOV	DQARVEC, DQARLVL	: GENERATE ADDRESS OF RECEIVER INTERRUPT SERVICE PS
000002	001350		ADD	#2, DQARLVL	
001354	001354		MOV	DQARLVL, DQATVEC	: GENERATE ADDRESS OF TRANSMITTER INTERRUPT VECTOR
000002	001354		ADD	#2, DQATVEC	
001354	001354		MOV	DQATVEC, DQATLVL	: GENERATE ADDRESS OF TRANSMITTER INTERRUPT SERVICE PS
000002	001354		ADD	#2, DQATLVL	
001360	001360		MOV	DQCSR, DQCRSH	
001360	001360		MOV	DQCRSH, DQCRSH	: GENERATE ADDRESS OF HIGH BYTE
001360	001364		MOV	DQCSR, DQTCR	: GENERATE ADDRESS OF TRANSMITTER CONTROL REGISTER
000002	001364		ADD	#2, DQTCR	
001364	001366		MOV	DQTCR, DQERR	: GENERATE ADDRESS OF ERROR REGISTER
000002	001366		ADD	#2, DQERR	
001370	001370		MOV	DQERR, DQERR	: GENERATE ADDRESS OF HIGH BYTE OF ERROR REGISTER
001370	001372		MOV	DQERR, DQERR	
001370	001372		MOV	DQERR, DQERR	: GENERATE ADDRESS OF SECONDARY REGISTER
001370	001374		MOV	DQERR, DQERR	
001370	001374		MOV	DQERR, DQERR	: GENERATE ADDRESS OF HIGH BYTE

:STEP MODE VERIFICATION AND CLOCK LOSS TEST
:SET STEP MODE
:SET RECEIVER GO
:SET TRANSMITTER GO
:EXPECTED RESULTS (AFTER DELAY)
:TRANSMITTER CLOCK LOSS = 1
:RECEIVER CLOCK LOSS = 1
:****NOTE: AS THE "CLOCK UP" OCCURS
:AN "NPR" SHOULD BE EXECUTED.
:THEREFORE IF THE DQ11 IS GOING TO "HANG"
:THE BUS DUE TO NPR'S THIS IS THE
:FIRST TEST IT WILL HAPPEN IN!!****

: TEST 2

ST2: MOV #2, TSTNO
MOV #10, ICOUNT
MOV #TST3, NEXT
MOV #340, PS
MEMCLR
MSTCLR
CLR TEMP1
MOV #10, TEMP2
MOVB #12, DQDRFG
MOV #BIT1, DQDSEC
MOV #BIT12+BIT0, DQDRCSR
MOV #BIT0, DQDTCR
INC DQDSEC
DEC DQDSEC
15: INC TEMP1
BNE #S
DEC BIT12, DQDRCSR
BNE #S
MOV #3, R5
MOVB DQDRR, R4
CMP R5, R4
BEQ #S
HLT 13
25: SCOPE
:TEST LOOP VERIFICATION
:SET STEP MODE AND TEST LOOP
:SET RECEIVER GO
:SET TRANSMITTER GO
:EXPECTED RESULTS (AFTER DELAY)
:TRANSMITTER CLOCK LOSS=0
:RECEIVER CLOCK LOSS=0

:LOCK OUT INTERRUPTS
:CLEAR MEMORY
:INIT DQ11
:ZERO DELAY COUNTER
:DELAY 9 X 65535 TIMES
:SELECT MISC REG
:SET AUTO STEP
:SET RX GO
:SET TX GO
:CLOCK UP
:CLOCK ON
:DO THE DELAY....
:DELAY
:CLEAR RX ACTIVE
:DELAY.....
:DELAY
:SET FOR EXPECTED
:READ THE DQERR REGISTER (SEL4)
:CLOCK LOSS WORKING
:OR IF YES.
:TX AND RX CLOCK LOSS ERROR
:SCOPE THIS TEST.

: TEST 3

ST3: MOV #3, TSTNO
MOV #10, ICOUNT
MOV #TST4, NEXT
MEMCLR
MOV #340, PS ;SET PS =7 LOCK OUT INTERRUPTS

000002 001006
000010 001006
000014 001016
000040 177776
001244
000010 001246
000012 176450
000012 176444
000001 176439
000001 176439
001244
001244
010000 176372
001246
000003
176362
012737 000003 001226
012737 000010 001222
012737 003142 001216
014413
012737 000040 177776

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141 003046 104412
141 003050 005037 001244
141 003054 012737 000010 001246
141 003058 112737 000012 176300
141 003062 012737 000012 176274
141 003066 012737 000001 176254
141 003070 012737 000001 176252
141 003112 005237 001244 15:
141 003116 001375
141 003120 005337 001246
141 003124 001372
141 003128 005005
141 003130 117704 176232
141 003134 001401
141 003138 104013
141 003142 004400 23:

```

```

MSTCLR
CLR TEMP1
MOV #10,TEMP2
MOVB #12,DQREG
MOV #BIT1+BIT3,DQSEC
MOV #BIT0,DQRC5R
MOV #BIT0,DQGTCSR
INC TEMP1
SNE #5
DEC TEMP2
BNE #5

CLR R5
MOVB DQERR,R4
BEQ #5
HLT #5
SCOPE

```

```

:INIT D011
:SET DELAY COUNTER TO 0
:SET FOR 8 X 65535 TIME DELAY
:SELECT MISC REGISTER
:SET TESTLOOP AND AUTO STEP
:SET RX GO.
:SET TX GO.
:
: D
: E
: L
: A
: Y
:SET EXPECTED
:GET ACTUAL
:BR IF LOW BYTE OF DQERR IS C
:D011 ERROR REG NOT C
:SCOPE THIS TEST.

```

E03

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:INDIVIDUAL INTERRUPT ENABLE TESTS
:SET SELECTED INTERRUPT ENABLE
:VERIFY THAT NO INTERRUPT OCCURS

:INTERRUPT LOGIC TEST
:SET CHARACTER DETECT INTERRUPT ENABLE
:VERIFY THAT NO INTERRUPT OCCURS

: TEST 4

:*****

003142 012737 000004 001226
003150 012737 003226 001216
003156 104412
003160 004737 016042
003164 003206
003166 003212
003170 052777 000020 176162
003176 005037 177776
003202 000240
003204 000403
003206 104003
003210 000401
003212 104002
003214 012706 001200
003220 004737 016074
003224 104400

TST4: MOV #4,TSTNO
MOV #TSTS,NEXT
MSTCLR
JSR PC,SETV
IS
JS
BIS #BIT4,DQGRCSR
CLR PS
NOP
BR JS
HLT JS
BR JS
HLT JS
MOV #STACK,SP
JSR PC,RECAT
48: SCOPE

:CLEAR INTERFACE
:SET UP INTERRUPT VECTORS
:RECEIVER WILL INTERRUPT TO 18
:TRANSMITTER WILL INTERRUPT TO 28
:SET CHARACTER DETECT INTERRUPT ENABL
:SET PROCESSOR PRIORITY TO 0
:WINDOW FOR INTERRUPTS
:UNEXPECTED RECEIVER INTERRUPT
:UNEXPECTED TRANSMITTER INTERRUPT
:STORE STACK
:RESTORE TRAPCATCHER
:CHECK FOR ITERATIONS, LOOP

:INTERRUPT LOGIC TEST
:SET RECEIVE DONE INTERRUPT ENABLE
:VERIFY THAT NO INTERRUPT OCCURS

: TEST 5

:*****

003226 012737 000005 001226
003234 012737 003312 001216
003242 104412
003244 004737 016042
003250 003272
003252 003276
003254 052777 000040 176076
003262 005037 177776
003266 000240
003270 000403
003272 104003
003274 000401
003276 104002
003280 012706 001200
003284 004737 016074
003288 104400

TST5: MOV #5,TSTNO
MOV #TSTS6,NEXT
MSTCLR
JSR PC,SETV
IS
JS
BIS #BITS,DQGRCSR
CLR PS
NOP
BR JS
HLT JS
BR JS
HLT JS
MOV #STACK,SP
JSR PC,RECAT
48: SCOPE

:CLEAR INTERFACE
:SET UP INTERRUPT VECTORS
:RECEIVER WILL INTERRUPT TO 18
:TRANSMITTER WILL INTERRUPT TO 28
:SET RECEIVE DONE INTERRUPT ENABL
:SET PROCESSOR PRIORITY TO 0
:WINDOW FOR INTERRUPTS
:UNEXPECTED RECEIVER INTERRUPT
:UNEXPECTED TRANSMITTER INTERRUPT
:RESTORE STACK
:RESTORE TRAPCATCHER
:CHECK FOR ITERATIONS, LOOP

:INTERRUPT LOGIC TEST
:SET ERROR INTERRUPT E. 3LE
:VERIFY THAT NO INTERRUPT OCCURS

: TEST 6

```

149:
148: 003312 012737 000006 001226 *****
147: 003320 012737 003376 001216 *TST6: MOV #6,TSTNO
146: 003326 104412 MSTCLR ;CLEAR INTERFACE
145: 003320 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
144: 003324 003356 1$ ;RECEIVER WILL INTERRUPT TO 1$
143: 003336 003362 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
142: 003340 052777 000010 176016 BIS #BIT3,DDQTCR ;SET ERROR INTERRUPT ENABL
141: 003346 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
140: 003352 000240 NOP ;WINDOW FOR INTERRUPTS
139: 003354 000403 BR 3$
138: 003356 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
137: 003360 000401 BR 3$
136: 003362 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
135: 003364 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
134: 003370 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
133: 003376 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP

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; INTERRUPT LOGIC TEST
; SET DATASET INTERRUPT ENABLE
; VERIFY THAT NO INTERRUPT OCCURS

```

: TEST 7

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132: 003376 012737 000007 001226 *****
131: 003384 012737 003462 001216 *TST7: MOV #7,TSTNO
130: 003392 104412 MSTCLR ;CLEAR INTERFACE
129: 003394 004737 016072 JSR PC,SETV ;SET UP INTERRUPT VECTORS
128: 003396 003442 1$ ;RECEIVER WILL INTERRUPT TO 1$
127: 003398 003446 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
126: 003400 052777 000020 175732 BIS #BIT4,DDQTCR ;SET DATASET INTERRUPT ENABL
125: 003402 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
124: 003404 000240 NOP ;WINDOW FOR INTERRUPTS
123: 003406 000403 BR 3$
122: 003408 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
121: 003410 000401 BR 3$
120: 003412 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
119: 003414 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
118: 003416 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
117: 003418 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP

```

```

; INTERRUPT LOGIC TEST
; SET TRANSMIT DONE INTERRUPT ENABLE
; VERIFY THAT NO INTERRUPT OCCURS

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: TEST 10

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116: 003462 012737 000010 001226 *****
115: 003470 012737 003546 001216 *TST10: MOV #10,TSTNO
114: 003476 104412 MSTCLR ;CLEAR INTERFACE
113: 003484 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
112: 003492 003526 1$ ;RECEIVER WILL INTERRUPT TO 1$
111: 003494 003532 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
110: 003496 052777 000040 175646 BIS #BIT5,DDQTCR ;SET TRANSMIT DONE INTERRUPT ENABL
109: 003498 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
108: 003500 000240 NOP ;WINDOW FOR INTERRUPTS

```



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1547 003524 000403 BR 3$
1548 003526 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1549 003530 000401 BR 3$
1550 003532 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1551 003534 012706 001200 3$: MOV #STACK, SP ;RESTORE STACK
1552 003540 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
1553 003544 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP

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```

: INDIVIDUAL INTERRUPT FLAG TESTS
: SET SELECTED INTERRUPT FLAG
: VERIFY THAT NO INTERRUPT OCCURS

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: INTERRUPT LOGIC TEST
: SET RECEIVE DONE S INTERRUPT FLAG
: VERIFY THAT NO INTERRUPT OCCURS

```

: TEST 11

```

1555 003546 012737 000011 001226 †TST11: MOV #11,TSTNO
1556 003554 012737 003632 001216 MOV #TST12,NEXT
1557 003562 104412 MSTCLR ;CLEAR INTERFACE
1558 003564 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1559 003570 003612 1$ ;RECEIVER WILL INTERRUPT TO 1$
1560 003572 003616 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
1561 003574 052777 000100 175556 BIS #BIT6,JDQRCR ;SET RECEIVE DONE S INTERRUPT FLAG
1562 003602 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1563 003606 000240 NOP ;WINDOW FOR INTERRUPTS
1564 003610 000403 BR 3$
1565 003612 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1566 003614 000401 BR 3$
1567 003616 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1568 003620 012706 001200 3$: MOV #STACK, SP ;RESTORE STACK
1569 003624 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
1570 003630 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP

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: INTERRUPT LOGIC TEST
: SET RECEIVE DONE P INTERRUPT FLAG
: VERIFY THAT NO INTERRUPT OCCURS

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: TEST 12

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1571 003632 012737 000012 001226 †TST12: MOV #12,TSTNO
1572 003640 012737 003716 001216 MOV #TST13,NEXT
1573 003646 104412 MSTCLR ;CLEAR INTERFACE
1574 003650 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1575 003654 003676 1$ ;RECEIVER WILL INTERRUPT TO 1$
1576 003656 003702 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
1577 003660 052777 000200 175472 BIS #BIT7,JDQRCR ;SET RECEIVE DONE P INTERRUPT FLAG
1578 003665 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1579 003672 000240 NOP ;WINDOW FOR INTERRUPTS
1580 003674 000403 BR 3$
1581 003676 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1582 003700 000401 BR 3$
1583 003702 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1584 003704 012706 001200 3$: MOV #STACK, SP ;RESTORE STACK

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1603 003710 004737 016074          JSR    PC,RECAT          ;RESTORE TRAPCATCHER
1604 003714 104400          4$:   SCOPE              ;CHECK FOR ITERATIONS, LOOP
1605
1606          ; INTERRUPT LOGIC TEST
1607          ; SET TRANSMIT DONE S INTERRUPT FLAG
1608          ; VERIFY THAT NO INTERRUPT OCCURS
1609
1610          : TEST 13
1611          :*****
1612 003716 012737 000013 001226  TST13: MOV    #13,TSTNO
1613 003724 012737 004002 001216      MOV    #TST14,NEXT
1614 003732 104412          MSTCLR
1615 003734 004737 016042          JSR    PC,SETV          ;CLEAR INTERFACE
1616 003740 003762          1$    ;SET UP INTERRUPT VECTORS
1617 003742 003766          2$    ;RECEIVER WILL INTERRUPT TO 1$
1618 003744 052777 000100 175412  BIS    #BIT6,DDOTCSR   ;TRANSMITTER WILL INTERRUPT TO 2$
1619 003752 005037 177776          CLR    PS              ;SET TRANSMIT DONE S INTERRUPT FLAG
1620 003756 000240          NOP                    ;SET PROCESSOR PRIORITY TO 0
1621 003760 000403          BR     3$              ;WINDOW FOR INTERRUPTS
1622 003762 104003          1$:   HLT    3          ;UNEXPECTED RECEIVER INTERRUPT
1623 003764 000401          BR     3$
1624 003766 104002          2$:   HLT    2          ;UNEXPECTED TRANSMITTER INTERRUPT
1625 003770 012706 001200          3$:   MOV    #STACK,SP  ;RESTORE STACK
1626 003774 004737 016074          JSR    PC,RECAT        ;RESTORE TRAPCATCHER
1627 004000 104400          4$:   SCOPE              ;CHECK FOR ITERATIONS, LOOP
1628
1629          ; INTERRUPT LOGIC TEST
1630          ; SET RECEIVE DONE S INTERRUPT FLAG
1631          ; VERIFY THAT NO INTERRUPT OCCURS
1632
1633          : TEST 14
1634          :*****
1635 004002 012737 000014 001226  TST14: MOV    #14,TSTNO
1636 004010 012737 004066 001216      MOV    #TST15,NEXT
1637 004016 104412          MSTCLR
1638 004020 004737 016042          JSR    PC,SETV          ;CLEAR INTERFACE
1639 004024 004046          1$    ;SET UP INTERRUPT VECTORS
1640 004026 004052          2$    ;RECEIVER WILL INTERRUPT TO 1$
1641 004030 052777 000200 175326  BIS    #BIT7,DDOTCSR   ;TRANSMITTER WILL INTERRUPT TO 2$
1642 004036 005037 177776          CLR    PS              ;SET RECEIVE DONE S INTERRUPT FLAG
1643 004042 000240          NOP                    ;SET PROCESSOR PRIORITY TO 0
1644 004044 000403          BR     3$              ;WINDOW FOR INTERRUPTS
1645 004046 104003          1$:   HLT    3          ;UNEXPECTED RECEIVER INTERRUPT
1646 004050 000401          BR     3$
1647 004052 104002          2$:   HLT    2          ;UNEXPECTED TRANSMITTER INTERRUPT
1648 004054 012706 001200          3$:   MOV    #STACK,SP  ;RESTORE STACK
1649 004060 004737 016074          JSR    PC,RECAT        ;RESTORE TRAPCATCHER
1650 004064 104400          4$:   SCOPE              ;CHECK FOR ITERATIONS, LOOP
1651
1652          ; INTERRUPT LOGIC TEST
1653          ; SET DATA SET INTERRUPT FLAG
1654          ; VERIFY THAT NO INTERRUPT OCCURS
1655
1656          : TEST 15
1657          :*****
1658 004066 012737 000015 001226  TST15: MOV    #15,TSTNO

```

```

1659 004074 012737 004152 001216      MOV      #TST16,NEXT
1660 004102 104412      MSTCLR
1661 004104 004737 016042      JSR      PC,SETV
1662 004110 004132      1$
1663 004112 004136      2$
1664 004114 052777 100000 175242      BIS      #BIT15,JDQTCR
1665 004122 005037 177776      CLR      PS
1666 004126 000240      NOP
1667 004130 000403      BR      3$
1668 004132 104003      1$: HLT      2
1669 004134 000401      BR      3$
1670 004136 104002      2$: HLT      2
1671 004140 012706 001200      3$: MOV      #STACK,SP
1672 004144 004737 016074      JSR      PC,RECAT
1673 004150 104400      4$: SCOPE

```

```

: INTERRUPT LOGIC TEST
: SET T CLOCK LOSS INTERRUPT FLAG
: VERIFY THAT NO INTERRUPT OCCURS

```

: TEST 16

:*****

```

1680
1681 004152 012737 000016 001226      TST16: MOV      #16,TSTNO
1682 004160 012737 004236 001216      MOV      #TST17,NEXT
1683 004166 104412      MSTCLR
1684 004170 004737 016042      JSR      PC,SETV
1685 004174 004216      1$
1686 004176 004222      2$
1687 004200 052777 000001 175160      BIS      #BIT0,JDQERR
1688 004206 005037 177776      CLR      PS
1689 004212 000240      NOP
1690 004214 000403      BR      3$
1691 004216 104003      1$: HLT      3
1692 004220 000401      BR      3$
1693 004222 104002      2$: HLT      2
1694 004224 012706 001200      3$: MOV      #STACK,SP
1695 004230 004737 016074      JSR      PC,RECAT
1696 004234 104400      4$: SCOPE

```

```

: INTERRUPT LOGIC TEST
: SET R CLOCK LOSS INTERRUPT FLAG
: VERIFY THAT NO INTERRUPT OCCURS

```

: TEST 17

:*****

```

1700
1701
1702
1703
1704 004236 012737 000017 001226      TST17: MOV      #17,TSTNO
1705 004244 012737 004322 001216      MOV      #TST20,NEXT
1706 004252 104412      MSTCLR
1707 004254 004737 016042      JSR      PC,SETV
1708 004260 004302      1$
1709 004262 004306      2$
1710 004264 052777 000002 175074      BIS      #BIT1,JDQERR
1711 004272 005037 177776      CLR      PS
1712 004276 000240      NOP
1713 004300 000403      BR      3$
1714 004302 104003      1$: HLT      3

```

```

: CLEAR INTERFACE
: SET UP INTERRUPT VECTORS
: RECEIVER WILL INTERRUPT TO 1$
: TRANSMITTER WILL INTERRUPT TO 2$
: SET R CLOCK LOSS INTERRUPT FLAG
: SET PROCESSOR PRIORITY TO 0
: WINDOW FOR INTERRUPTS
: UNEXPECTED RECEIVER INTERRUPT

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```

1715 004304 000401          BR      3$
1716 004306 104002          2$:    HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1717 004310 012706 001200        3$:    MOV      #STACK,SP ;RESTORE STACK
1718 004314 004737 016074          JSR      PC,RECAT ;RESTORE TRAPCATCHER
1719 004320 104400          4$:    SCOPE ;CHECK FOR ITERATIONS, LOOP
1720
1721          ; INTERRUPT LOGIC TEST
1722          ; SET T LATENCY INTERRUPT FLAG
1723          ; VERIFY THAT NO INTERRUPT OCCURS
1724
1725          : TEST 20
1726          : *****
1727 004322 012737 000020 001226 1ST20: MOV      #20,TSTNO
1728 004330 012737 004406 001216          MOV      #TST21,NEXT
1729 004335 104412          MSTCLR ;CLEAR INTERFACE
1730 004340 004737 016042          JSR      PC,SETV ;SET UP INTERRUPT VECTORS
1731 004344 004366          1$:    ;RECEIVER WILL INTERRUPT TO 1$
1732 004346 004372          2$:    ;TRANSMITTER WILL INTERRUPT TO 2$
1733 004350 052777 000004 175010        BIS      #BIT2,JDQERR ;SET T LATENCY INTERRUPT FLAG
1734 004356 005037 177776          CLR      PS ;SET PROCESSOR PRIORITY TO 0
1735 004362 000240          NOP ;WINDOW FOR INTERRUPTS
1736 004364 000403          BR      3$
1737 004366 104003          1$:    HLT      3          ;UNEXPECTED RECEIVER INTERRUPT
1738 004370 000401          BR      3$
1739 004372 104002          2$:    HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1740 004374 012706 001200        3$:    MOV      #STACK,SP ;RESTORE STACK
1741 004400 004737 016074          JSR      PC,RECAT ;RESTORE TRAPCATCHER
1742 004404 104400          4$:    SCOPE ;CHECK FOR ITERATIONS, LOOP
1743
1744          ; INTERRUPT LOGIC TEST
1745          ; SET R LATENCY INTERRUPT FLAG
1746          ; VERIFY THAT NO INTERRUPT OCCURS
1747
1748          : TEST 21
1749          : *****
1750 004406 012737 000021 001226 1ST21: MOV      #21,TSTNO
1751 004414 012737 004472 001216          MOV      #TST22,NEXT
1752 004422 104412          MSTCLR ;CLEAR INTERFACE
1753 004424 004737 016042          JSR      PC,SETV ;SET UP INTERRUPT VECTORS
1754 004430 004452          1$:    ;RECEIVER WILL INTERRUPT TO 1$
1755 004432 004456          2$:    ;TRANSMITTER WILL INTERRUPT TO 2$
1756 004434 052777 000010 174724        BIS      #BIT3,JDQERR ;SET R LATENCY INTERRUPT FLAG
1757 004442 005037 177776          CLR      PS ;SET PROCESSOR PRIORITY TO 0
1758 004446 000240          NOP ;WINDOW FOR INTERRUPTS
1759 004450 000403          BR      3$
1760 004452 104003          1$:    HLT      3          ;UNEXPECTED RECEIVER INTERRUPT
1761 004454 000401          BR      3$
1762 004456 104002          2$:    HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1763 004460 012706 001200        3$:    MOV      #STACK,SP ;RESTORE STACK
1764 004464 004737 016074          JSR      PC,RECAT ;RESTORE TRAPCATCHER
1765 004470 104400          4$:    SCOPE ;CHECK FOR ITERATIONS, LOOP
1766
1767          ; INTERRUPT LOGIC TEST
1768          ; SET T NON-EX MEM INTERRUPT FLAG
1769          ; VERIFY THAT NO INTERRUPT OCCURS
1770

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```

1771 : TEST 22
1772 :*****
1773 004472 012737 000022 001226 †TST22: MOV #22,TSTNO
1774 004500 012737 004556 001216 MOV #TST23,NEXT
1775 004506 104412 MSTCLR ;CLEAR INTERFACE
1776 004510 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1777 004514 004536 1$ ;RECEIVER WILL INTERRUPT TO 1$
1778 004516 004542 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
1779 004520 052777 000020 174640 BIS #BIT4,ADQERR ;SET T NON-EX MEM INTERRUPT FLAG
1780 004526 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1781 004532 000240 NOP ;WINDOW FOR INTERRUPTS
1782 004534 000403 BR 3$
1783 004536 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1784 004540 000401 BR 3$
1785 004542 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1786 004544 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
1787 004550 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
1788 004554 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
1789
1790 ; INTERRUPT LOGIC TEST
1791 ; SET R NON-EX MEM INTERRUPT FLAG
1792 ; VERIFY THAT NO INTERRUPT OCCURS
1793
1794 : TEST 23
1795 :*****
1796 004556 012737 000023 001226 †TST23: MOV #23,TSTNO
1797 004564 012737 004642 001216 MOV #TST24,NEXT
1798 004572 104412 MSTCLR ;CLEAR INTERFACE
1799 004574 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1800 004600 004622 1$ ;RECEIVER WILL INTERRUPT TO 1$
1801 004602 004626 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
1802 004604 052777 000040 174554 BIS #BIT5,ADQERR ;SET R NON-EX MEM INTERRUPT FLAG
1803 004612 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1804 004616 000240 NOP ;WINDOW FOR INTERRUPTS
1805 004620 000403 BR 3$
1806 004622 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1807 004624 000401 BR 3$
1808 004626 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1809 004630 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
1810 004634 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
1811 004640 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
1812
1813 ; INTERRUPT LOGIC TEST
1814 ; SET R BCC ERROR INTERRUPT FLAG
1815 ; VERIFY THAT NO INTERRUPT OCCURS
1816
1817 : TEST 24
1818 :*****
1819 004642 012737 000024 001226 †TST24: MOV #24,TSTNO
1820 004650 012737 004726 001216 MOV #TST25,NEXT
1821 004656 104412 MSTCLR ;CLEAR INTERFACE
1822 004660 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1823 004664 004706 1$ ;RECEIVER WILL INTERRUPT TO 1$
1824 004666 004712 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
1825 004670 052777 000100 174470 BIS #BIT6,ADQERR ;SET R BCC ERROR INTERRUPT FLAG
1826 004676 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
    
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1827 004702 000240      NOP      ;WINDOW FOR INTERRUPTS
1828 004704 000403      BR       3$
1829 004706 104003      1$: HLT  3      ;UNEXPECTED RECEIVER INTERRUPT
1830 004710 000401      BR       3$
1831 004712 104002      2$: HLT  2      ;UNEXPECTED TRANSMITTER INTERRUPT
1832 004714 012706 001200      3$: MOV  #STACK, SP ;RESTORE STACK
1833 004720 004737 016074      JSR    PC, RECAT  ;RESTORE TRAPCATCHER
1834 004724 104400      4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
1835
1836      ; INTERRUPT LOGIC TEST
1837      ; SET R VRC ERROR INTERRUPT FLAG
1838      ; VERIFY THAT NO INTERRUPT OCCURS
1839
1840      ; TEST 25
1841      ; *****
1842 004726 012737 000025 001226  †TST25: MOV  #25, TSTNO
1843 004734 012737 005012 001216      MOV  #TST26, NEXT
1844 004742 104412      MSTCLR ; CLEAR INTERFACE
1845 004744 004737 016042      JSR    PC, SETV  ; SET UP INTERRUPT VECTORS
1846 004750 004772      1$:      ; RECEIVER WILL INTERRUPT TO 1$
1847 004752 004776      2$:      ; TRANSMITTER WILL INTERRUPT TO 2$
1848 004754 052777 000200 174404      BIS  #BIT7, @DQERR ; SET R VRC ERROR INTERRUPT FLAG
1849 004762 005037 177776      CLR  PS        ; SET PROCESSOR PRIORITY TO 0
1850 004766 000240      NOP        ; WINDOW FOR INTERRUPTS
1851 004770 000403      BR       3$
1852 004772 104003      1$: HLT  3      ; UNEXPECTED RECEIVER INTERRUPT
1853 004774 000401      BR       3$
1854 004776 104002      2$: HLT  2      ; UNEXPECTED TRANSMITTER INTERRUPT
1855 005000 012706 001200      3$: MOV  #STACK, SP ; RESTORE STACK
1856 005004 004737 016074      JSR    PC, RECAT  ; RESTORE TRAPCATCHER
1857 005010 104400      4$: SCOPE ; CHECK FOR ITERATIONS, LOOP
1858
1859      ; INDIVIDUAL INTERRUPT TESTS
1860      ; SET SELECTED INTERRUPT ENABLE AND FLAG
1861      ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT ADDRESS
1862
1863      ; INTERRUPT LOGIC TEST
1864      ; SET CHARACTER DETECT INTERRUPT ENABLE
1865      ; SET CHARACTER DETECT INTERRUPT FLAG
1866      ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
1867
1868      ; TEST 26
1869      ; *****
1870      ; *****
1871 005012 012737 000026 001226  †TST26: MOV  #26, TSTNO
1872 005020 012737 005102 001216      MOV  #TST27, NEXT
1873 005026 104412      MSTCLR ; CLEAR INTERFACE
1874 005030 004737 016042      JSR    PC, SETV  ; SET UP INTERRUPT VECTORS
1875 005034 005064      1$:      ; RECEIVER WILL INTERRUPT TO 1$
1876 005036 005066      2$:      ; TRANSMITTER WILL INTERRUPT TO 2$
1877 005040 052777 000020 174312      BIS  #BIT4, @DQRCR ; SET CHARACTER DETECT INTERRUPT ENABL
1878 005046 052777 100000 174304      BIS  #BIT15, @DQRCR ; SET CHARACTER DETECT INTERRUPT FLAG
1879 005054 005037 177776      CLR  PS        ; SET PROCESSOR PRIORITY TO 0
1880 005060 000240      NOP        ; WINDOW FOR INTERRUPTS
1881 005062 104000      HLT  0      ; RECEIVER DID NOT INTERRUPT
1882 005064 000401      1$: BR   3$      ; RECEIVER SHOULD INTERRUPT TO THIS LOCATION

```


M03

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 DZDQCC.P11 DQ11 INTERJPT AND NFR LOGIC TESTS.

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1893 005066 104002          2$:  HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1894 005070 012706 001200  3$:  MOV      #STACK,SP    ;RESTORE STACK
1895 005074 004737 016074          JSR      PC,RECAT      ;RESTORE TRAPCATCHER
1896 005100 104400          4$:  SCOPE                    ;CHECK FOR ITERATIONS. LOOP
1897
1898          ; INTERRUPT LOGIC TEST
1899          ; SET RECEIVE DONE INTERRUPT ENABLE
1900          ; SET RECEIVE DONE S INTERRUPT FLAG
1901          ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
1902
1903          ; TEST 27
1904          ; *****
1895 005102 012737 000027 001226  †TST27: MOV      #27,TSTNO
1896 005110 012737 005172 001216      MOV      #TST30,NEXT
1897 005116 104412          MSTCLR                    ;CLEAR INTERFACE
1898 005120 004737 016042          JSR      PC,SETV        ;SET UP INTERRUPT VECTORS
1899 005124 005154          1$:                      ;RECEIVER WILL INTERRUPT TO 1$
1900 005126 005156          2$:                      ;TRANSMITTER WILL INTERRUPT TO 2$
1901 005130 052777 000040 174222      BIS      #BITS,ADQRCR   ;SET RECEIVE DONE INTERRUPT ENABL
1902 005136 052777 000100 174214      BIS      #BIT6,ADQRCR  ;SET RECEIVE DONE S INTERRUPT FLAG
1903 005144 005037 177776          CLR      PS            ;SET PROCESSOR PRIORITY TO 0
1904 005150 000240          NOP                    ;WINDOW FOR INTERRUPTS
1905 005152 104000          HLT      0            ;RECEIVER DID NOT INTERRUPT
1906 005154 000401          1$:  BR      3$          ;RECEIVER SHOULD INTERRUPT TO THIS LOCATION
1907 005156 104002          2$:  HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1908 005160 012706 001200          3$:  MOV      #STACK,SP    ;RESTORE STACK
1909 005164 004737 016074          JSR      PC,RECAT      ;RESTORE TRAPCATCHER
1910 005170 104400          4$:  SCOPE                    ;CHECK FOR ITERATIONS, LOOP
1911
1912          ; INTERRUPT LOGIC TEST
1913          ; SET RECEIVE DONE INTERRUPT ENABLE
1914          ; SET RECEIVE DONE P INTERRUPT FLAG
1915          ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
1916
1917          ; TEST 30
1918          ; *****
1919 005172 012737 000030 001226  †TST30: MOV      #30,TSTNO
1920 005200 012737 005262 001216      MOV      #TST31,NEXT
1921 005206 104412          MSTCLR                    ;CLEAR INTERFACE
1922 005210 004737 016042          JSR      PC,SETV        ;SET UP INTERRUPT VECTORS
1923 005214 005244          1$:                      ;RECEIVER WILL INTERRUPT TO 1$
1924 005216 005246          2$:                      ;TRANSMITTER WILL INTERRUPT TO 2$
1925 005220 052777 000040 174132      BIS      #BITS,ADQRCR   ;SET RECEIVE DONE INTERRUPT ENABL
1926 005226 052777 000200 174124      BIS      #BIT7,ADQRCR  ;SET RECEIVE DONE P INTERRUPT FLAG
1927 005234 005037 177776          CLR      PS            ;SET PROCESSOR PRIORITY TO 0
1928 005240 000240          NOP                    ;WINDOW FOR INTERRUPTS
1929 005242 104000          HLT      0            ;RECEIVER DID NOT INTERRUPT
1930 005244 000401          1$:  BR      3$          ;RECEIVER SHOULD INTERRUPT TO THIS LOCATION
1931 005246 104002          2$:  HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1932 005250 012706 001200          3$:  MOV      #STACK,SP    ;RESTORE STACK
1933 005254 004737 016074          JSR      PC,RECAT      ;RESTORE TRAPCATCHER
1934 005260 104400          4$:  SCOPE                    ;CHECK FOR ITERATIONS. LOOP
1935
1936          ; INTERRUPT LOGIC TEST
1937          ; SET TRANSMIT DONE INTERRUPT ENABLE
1938          ; SET TRANSMIT DONE S INTERRUPT FLAG

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005262 012737 000031 001226
005270 012737 005354 001216
005276 104412
005300 004737 016042
005304 005336
005306 005340
005310 052777 000040 174046
005316 052777 000100 174040
005324 005037 177776
005330 000240
005332 104001
005334 000402

005336 104003
005340 000240
005342 012706 001200
005346 004737 016074
005352 104400

```

:VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
; TEST 31
;*****
TST31: MOV #31,TSTNO
MOV #TST32,NEXT
MSTCLR
JSR PC,SETV
1$
2$
BIS #BIT5,JDQTCR
BIS #BIT6,JDQTCR
CLR PS
NOP
HLT 1
BR 3$

1$: HLT 3
2$: NOP
3$: MOV #STACK,SP
JSR PC,RECAT
4$: SCOPE

;CLEAR INTERFACE
;SET UP INTERRUPT VECTORS
;RECEIVER WILL INTERRUPT TO 1$
;TRANSMITTER WILL INTERRUPT TO 2$
;SET TRANSMIT DONE INTERRUPT ENABL
;SET TRANSMIT DONE S INTERRUPT FLAG
;SET PROCESSOR PRIORITY TO 0
;WINDOW FOR INTERRUPTS
;TRANSMITTER DID NOT INTERRUPT
;WITH TRANSMIT DONE INTERRUPT ENABL AND
;TRANSMIT DONE S INTERRUPT FLAG SET
;UNEXPECTED RECEIVER INTERRUPT
;TRANSMITTER SHOULD INTERRUPT TO HERE
;RESTORE STACK
;RESTORE TRAPCATCHER
;CHECK FOR ITERATIONS. LOOP

```

; INTERRUPT LOGIC TEST
; SET TRANSMIT DONE INTERRUPT ENABLE
; SET TRANSMIT DONE P INTERRUPT FLAG
; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

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; TEST 32
;*****
TST32: MOV #32,TSTNO
MOV #TST33,NEXT
MSTCLR
JSR PC,SETV
1$
2$
BIS #BIT5,JDQTCR
BIS #BIT7,JDQTCR
CLR PS
NOP
HLT 1
BR 3$

1$: HLT 3
2$: NOP
3$: MOV #STACK,SP
JSR PC,RECAT
4$: SCOPE

;CLEAR INTERFACE
;SET UP INTERRUPT VECTORS
;RECEIVER WILL INTERRUPT TO 1$
;TRANSMITTER WILL INTERRUPT TO 2$
;SET TRANSMIT DONE INTERRUPT ENABL
;SET TRANSMIT DONE P INTERRUPT FLAG
;SET PROCESSOR PRIORITY TO 0
;WINDOW FOR INTERRUPTS
;TRANSMITTER DID NOT INTERRUPT
;WITH TRANSMIT DONE INTERRUPT ENABL AND
;TRANSMIT DONE P INTERRUPT FLAG SET
;UNEXPECTED RECEIVER INTERRUPT
;TRANSMITTER SHOULD INTERRUPT TO HERE
;RESTORE STACK
;RESTORE TRAPCATCHER
;CHECK FOR ITERATIONS. LOOP

```

; INTERRUPT LOGIC TEST
; SET ERROR INTERRUPT ENABLE
; SET T CLOCK LOSS INTERRUPT FLAG
; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

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; TEST 33
;*****

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005654 005706 15
005655 005710 25
005656 052777 000010 173476 25 BIS #BIT3,DDQTCR
005657 052777 000010 173476 25 BIS #BIT2,DDQERR
005658 005037 177776 25 CLR PS
005659 000240 25 NOP
005660 104001 25 HLT 1
005661 000402 25 BR 38
005706 104003 45: HLT 3
005710 000240 25: NOP
005712 012706 001200 35: MOV #STACK,SP
005714 004737 016074 35: JSR PC,RECAT
005722 104400 45: SCOPE

```

```

:RECEIVER WILL INTERRUPT TO 15
:TRANSMITTER WILL INTERRUPT TO 25
:SET ERROR INTERRUPT ENABL
:SET T LATENCY INTERRUPT FLAG
:SET PROCESSOR PRIORITY TO 0
:WINDOW FOR INTERRUPTS
:TRANSMITTER DID NOT INTERRUPT
:WITH ERROR INTERRUPT ENABL AND
:T LATENCY INTERRUPT FLAG SET
:UNEXPECTED RECEIVER INTERRUPT
:TRANSMITTER SHOULD INTERRUPT TO HERE
:RESTORE STACK
:RESTORE TRAPCATCHER
:CHECK FOR ITERATIONS, LOOP

```

```

: INTERRUPT LOGIC TEST
: SET ERROR INTERRUPT ENABLE
: SET R LATENCY INTERRUPT FLAG
: VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

: TEST 36

```

005724 012737 000036 001226
005725 012737 006016 001216
005726 104412
005727 004737 016042
005728 006000
005729 006002
005730 052777 000010 173404
005731 052777 000010 173400
005732 005037 177776
005733 000240
005734 104001
005735 000402
006000 104003
006001 000240
006002 012706 001200
006003 004737 016074
006004 104400

```

```

TST36: MOV #36,TSTNO
MOV #TST37,NEXT
MSTCLR
JSR PC,SETV
15
25
25 BIS #BIT3,DDQTCR
25 BIS #BIT3,DDQERR
25 CLR PS
25 NOP
25 HLT 1
25 BR 35
15: HLT 3
25: NOP
35: MOV #STACK,SP
35: JSR PC,RECAT
45: SCOPE

```

```

: CLEAR INTERFACE
: SET UP INTERRUPT VECTORS
: RECEIVER WILL INTERRUPT TO 15
: TRANSMITTER WILL INTERRUPT TO 25
: SET ERROR INTERRUPT ENABL
: SET R LATENCY INTERRUPT FLAG
: SET PROCESSOR PRIORITY TO 0
: WINDOW FOR INTERRUPTS
: TRANSMITTER DID NOT INTERRUPT
: WITH ERROR INTERRUPT ENABL AND
: R LATENCY INTERRUPT FLAG SET
: UNEXPECTED RECEIVER INTERRUPT
: TRANSMITTER SHOULD INTERRUPT TO HERE
: RESTORE STACK
: RESTORE TRAPCATCHER
: CHECK FOR ITERATIONS, LOOP

```

```

: INTERRUPT LOGIC TEST
: SET ERROR INTERRUPT ENABLE
: SET T NON-EX MEM INTERRUPT FLAG
: VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

: TEST 37

```

006006 012737 000037 001226
006007 012737 006110 001216
006008 104412
006009 004737 016042
006010 006072
006011 006074
006012 052777 000010 173312
006013 052777 000020 173306

```

```

TST37: MOV #37,TSTNO
MOV #TST40,NEXT
MSTCLR
JSR PC,SETV
15
25
25 BIS #BIT3,DDQTCR
25 BIS #BIT4,DDQERR

```

```

: CLEAR INTERFACE
: SET UP INTERRUPT VECTORS
: RECEIVER WILL INTERRUPT TO 15
: TRANSMITTER WILL INTERRUPT TO 25
: SET ERROR INTERRUPT ENABL
: SET T NON-EX MEM INTERRUPT FLAG

```

```

006060 005037 177776 CLR PS :SET PROCESSOR PRIORITY TO 0
006064 000240 NOP :WINDOW FOR INTERRUPTS
006066 104001 HLT 1 :TRANSMITTER DID NOT INTERRUPT
006070 000402 BR 3$ :WITH ERROR INTERRUPT ENABL AND
:NON-EX MEM INTERRUPT FLAG SET
006072 104003 1$: HLT 3 :UNEXPECTED RECEIVER INTERRUPT
006074 000240 2$: NOP :TRANSMITTER SHOULD INTERRUPT TO HERE
006076 012706 001200 3$: MOV #STACK,SP :RESTORE STACK
006102 004737 016074 JSR PC,RECAT :RESTORE TRAPCATCHER
006106 104400 4$: SCOPE :CHECK FOR ITERATIONS, LOOP

```

```

: INTERRUPT LOGIC TEST
: SET ERROR INTERRUPT ENABLE
: SET R NON-EX MEM INTERRUPT FLAG
: VERIFY THAT AN INTERRUPT OCCURS TO THE CORPECT VECTOR

```

: TEST 40

```

006110 012737 000040 001226 TST40: MOV #40,TSTNO
006116 012737 006202 001216 MOV #TST41,NEXT
006124 104412 MSTCLR :CLEAR INTERFACE
006126 004737 016042 JSR PC,SETV :SET UP INTERRUPT VECTORS
006132 006164 1$: :RECEIVER WILL INTERRUPT TO 1$
006134 006166 2$: :TRANSMITTER WILL INTERRUPT TO 2$
006136 052777 000010 173220 BIS #BIT3,DDGTCR :SET ERROR INTERRUPT ENABL
006144 052777 000040 173214 BIS #BIT5,DDGERR :SET R NON-EX MEM INTERRUPT FLAG
006152 005037 177776 CLR PS :SET PROCESSOR PRIORITY TO 0
006154 000240 NOP :WINDOW FOR INTERRUPTS
006156 104001 HLT 1 :TRANSMITTER DID NOT INTERRUPT
006162 000402 BR 3$ :WITH ERROR INTERRUPT ENABL AND
:NON-EX MEM INTERRUPT FLAG SET
006164 104003 1$: HLT 3 :UNEXPECTED RECEIVER INTERRUPT
006166 000240 2$: NOP :TRANSMITTER SHOULD INTERRUPT TO HERE
006170 012706 001200 3$: MOV #STACK,SP :RESTORE STACK
006174 004737 016074 JSR PC,RECAT :RESTORE TRAPCATCHER
006200 104400 4$: SCOPE :CHECK FOR ITERATIONS, LOOP

```

```

: INTERRUPT LOGIC TEST
: SET ERROR INTERRUPT ENABLE
: SET R BCC ERROR INTERRUPT FLAG
: VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

: TEST 41

```

006202 012737 000041 001226 TST41: MOV #41,TSTNO
006210 012737 006274 001216 MOV #TST42,NEXT
006216 104412 MSTCLR :CLEAR INTERFACE
006220 004737 016042 JSR PC,SETV :SET UP INTERRUPT VECTORS
006224 006256 1$: :RECEIVER WILL INTERRUPT TO 1$
006226 006260 2$: :TRANSMITTER WILL INTERRUPT TO 2$
006230 052777 000010 173126 BIS #BIT3,DDGTCR :SET ERROR INTERRUPT ENABL
006236 052777 000100 173122 BIS #BIT6,DDGERR :SET R BCC ERROR INTERRUPT FLAG
006244 005037 177776 CLR PS :SET PROCESSOR PRIORITY TO 0
006250 000240 NOP :WINDOW FOR INTERRUPTS
006252 104001 HLT 1 :TRANSMITTER DID NOT INTERRUPT
006254 000402 BR 3$ :WITH ERROR INTERRUPT ENABL AND

```

```

1163
1164 006256 104003 1S: HLT 3 ;R BCC ERROR INTER. JPT FLAG SET
1165 006260 000240 2S: NOP ;UNEXPECTED RECEIVER INTERRUPT
1166 006262 012706 001200 3S: MOV #STACK,SP ;TRANSMITTER SHOULD INTERRUPT TO HERE
1167 006266 004737 016074 JSR PC,RECAT ;RESTORE STACK
1168 006272 104400 4S: SCOPE ;RESTORE TRAPCATCHER
;CHECK FOR ITERATIONS, LOOP

```

```

; INTERRUPT LOGIC TEST
; SET ERROR INTERRUPT ENABLE
; SET R VRC ERROR INTERRUPT FLAG
; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

: TEST 42

```

1176 TST42: MOV #42,TSTNO
1177 006274 012737 000042 001226 MOV #TST43,NEXT
1178 006302 012737 006366 001216 MSTCLR
1179 006310 104412 JSR PC,SETV
1180 006312 004737 016042 1S
1181 006316 006350 2S
1182 006320 006352 BIS #BIT3,DDQTCR ;CLEAR INTERFACE
1183 006322 032777 000010 173034 BIS #BIT7,DDQERR ;SET UP INTERRUPT VECTORS
1184 006330 052777 000200 173030 CLR PS ;RECEIVER WILL INTERRUPT TO 1S
1185 006336 005037 177776 ;TRANSMITTER WILL INTERRUPT TO 2S
1186 006342 000240 ;SET ERROR INTERRUPT ENABL
1187 006344 104001 ;SET R VRC ERROR INTERRUPT FLAG
1188 006346 000402 HLT 1 ;SET PROCESSOR PRIORITY TO 0
;WINDOW FOR INTERRUPTS
;TRANSMITTER DID NOT INTERRUPT
;WITH ERROR INTERRUPT ENABL AND
;R VRC ERROR INTERRUPT FLAG SET
;UNEXPECTED RECEIVER INTERRUPT
;TRANSMITTER SHOULD INTERRUPT TO HERE

```

```

1190 006350 104003 1S: HLT 3
1191 006352 000240 2S: NOP
1192 006354 012706 001200 3S: MOV #STACK,SP
1193 006360 004737 016074 JSR PC,RECAT
1194 006364 104400 4S: SCOPE
;CHECK FOR ITERATIONS, LOOP

```

```

;TEST THAT THE RECEIVER WILL INTERLPT
;BEFORE THE TRANSMITTER WHEN
;THEY ARE BOTH ENABLED AT THE
;SAME TIME.

```

: TEST 43

```

2204 TST43: MOV #43,TSTNO
2205 006366 012737 000043 001226 MOV #TST44,NEXT
2206 006374 012737 006502 001216 MSTCLR
2207 006402 104412 JSR PC,SETV
2208 006404 004737 016042 1S
2209 006410 006454 2S
2210 006412 006456 MOV #340,PS ;INIT DQ11
2211 006414 012737 000340 177776 MOV #240,DDQTCR ;SET THE VECTORS
2212 006422 012777 000240 172734 MOV #240,DDQRCR ;THIS FOR RX
2213 006430 012777 000240 172722 MOV #240,DDQRCR ;THIS FOR TX
2214 006436 000240 ;LOCK OUT INTERRUPTS
2215 006440 005037 177776 CLR PS ;SET TX PRI DONE AND IE
2216 006444 000240 ;SET RX PRI DONE AND IE
2217 006446 000240 ;INTERUPT YET.
2218 006450 104001 ;ZERO PROC. STATUS
2219 006452 104000 HLT 1 ;WAIT ONE INSTR. TIME
;TX AND RX FAILED TO INTERRUPT

```



```

006454 000401 15: BR 35 ;GOOD FOR RX
006456 104002 25: HLT 2 ;TX SHOULD NOT HAVE INTERRUPTED
006460 005077 172674 35: CLR 3DQRCR ;CLEAR RXCSR
006464 005077 172674 CLR 3DQTCR ; CLEAR TX CSR
006470 012706 001200 MOV #STACK,SP ;RESTORE STACK POINTER
006474 004737 016074 JSR PC,RECAT ;RESET VECTORS
006500 104400 SCOPE ;SCOPE THE TEST

```

;VERIFY THAT THE TRANSMITTER INTERRUPTS
;ONLY ONCE WHEN IT IS ENABLED.

: TEST 44

```

006502 012737 000044 001226 TST44: MOV #44,TSTNO
006510 012737 006506 001216 MOV #TST45,NEXT
006516 104412 MSTCLR
006520 004737 016042 JSR PC,SETV
006524 006572 15
006526 006576 25
006530 012737 000340 177776 MOV #340,PS
006536 012777 000240 172620 MOV #240,3DQTCR
006544 012700 177777 MOV #-1,R0
006550 005002 CLR R2
006552 005037 177776 CLR PS
006556 105202 INCB R2
006560 001376 BNE .-2
006562 005700 TST R0
006564 001401 BEQ .+4
006566 104001 HLT 1
006570 104400 SCOPE
006572 104003 15: HLT 3
006574 000002 25: COM R0
006576 005100 BEQ .+4
006600 001401 HLT 2
006602 104002 RTI
006604 000002

```

;VERIFY THAT THE RECEIVER INTERRUPTS
;ONLY ONCE WHEN IT IS ENABLED.

: TEST 45

```

006606 012737 000045 001226 TST45: MOV #45,TSTNO
006614 012737 006712 001216 MOV #TST46,NEXT
006622 104412 MSTCLR ;INIT DQ11
006624 004737 016042 JSR PC,SETV ;GO AND SET VECTORS
006630 006676 15 ;RX TO 15
006632 006706 25 ;TX TO 25
006634 012737 000340 177776 MOV #340,PS ;LOCK OUT INTERRUPTS
006642 012777 000240 172510 MOV #240,3DQRCR ;SET RX PRI DONE AND IE
006650 012700 177777 MOV #-1,R0 ;SET FOR CHECK
006654 005002 CLR R2 ;ZERO COUNTER
006656 005037 177776 CLR PS ;ENABLE INTERRUPTS
006662 105202 INCB R2 ;START COUNTING
006664 001376 BNE .-2 ;LOOP HERE
006666 005700 TST R0 ;IS CHECKER 0

```

```

2275 006670 001401 BEQ .+4 ;BR IF YES
2276 006672 104000 HLT 0 ;EITHER RX DID NOT INTERRUPT; OR MORE THAN ONCE
2277 006674 104400 SCOPE ;SCOPE THE TEST
2278 006676 005100 1$: COM R0 ;CHECK INTERRUPT
2279 006700 001401 BEQ .+4 ;BR IF FIRST TIME HERE
2280 006702 104003 HLT 3 ;RX INTERRUPTED MORE THAN ONCE
2281 006704 000002 RTI ;GO BACK AND DELAY
2282 006706 104002 2$: HLT 2 ;UNEXPECTED TX INTERRUPT
2283 006710 000002 RTI ;RETURN

```

```

;TEST TO SEE IF THE
;DQ11 TRANSMITTER WILL
;INTERUPT AT PS LEVEL
;OF 7 PRIORITY.
;

```

: TEST 46

```

2294 006712 012737 000046 001226 †TST46: MOV #46,TSTNO
2295 006720 012737 007014 001216 MOV #TST47,NEXT
2296 006726 104412 MSTCLR ;INIT DQ11
2297 006730 004737 016042 JSR PC,SETV ;SET VECTORS
2298 006734 006766 1$ ;RX INTERRUPTS TO 1$
2299 006736 006772 2$ ;TX INTERRUPTS TO 2$
2300 006740 012700 177777 MOV #-1,R0 ;SET CHECKER
2301 006744 012737 000340 177776 MOV #340,PS ;SET PRIORITY
2302 006752 012777 000240 172404 MOV #240,DDQTCSR ;SET PRI DONE AND IE
2303 006760 000240 NOP ;
2304 006762 000240 NOP ;
2305 006764 000403 BR 3$ ;CONTINUE TEST
2306 006766 104003 1$: HLT 3 ;UNEXPECTED RX INTERRUPT
2307 006770 000002 RTI ;CONTINUE TEST
2308 006772 005100 2$: COM R0 ;CHECK INTERRUPT
2309 006774 012706 001200 3$: MOV #STACK.SP ;SET STACK POINTER
2310 007000 005700 TST R0 ;CHECK INTERRUPT POINTER
2311 007002 001001 BNE .+4 ;
2312 007004 104002 HLT 2 ;
2313 007006 005077 172352 CLR DDQTCSR ;
2314 007012 104400 SCOPE ;

```

```

;TEST TO SEE IF THE
;DQ11 TRANSMITTER WILL
;INTERUPT AT PS LEVEL
;OF 6 PRIORITY.
;

```

: TEST 47

```

2324 007014 012737 000047 001226 †TST47: MOV #47,TSTNO
2325 007022 012737 007116 001216 MOV #TST50,NEXT
2326 007030 104412 MSTCLR ;INIT DQ11
2327 007032 004737 016042 JSR PC,SETV ;SET VECTORS
2328 007036 007070 1$ ;RX INTERRUPTS TO 1$
2329 007040 007074 2$ ;TX INTERRUPTS TO 2$
2330 007042 012700 MOV #-1,RC ;SET CHECKER

```

```

2331 007046 012737 000300 177776      MOV      #300,PS      ;SET PRICRITY
2332 007054 012777 000240 172302      MOV      #240,SDQTCR ;SET PRI DONE AND IE
2333 007062 000240                NOP
2334 007064 000240                NOP
2335 007066 000403                BR       3$
2336 007070 104003                1$: HLT      3          ;CONTINUE TEST
2337 007072 000002                RTI
2338 007074 005100                2$: COM      RO      ;UNEXPECTED RX INTERUPT
2339 007076 012706 001200        3$: MOV      #STACK,SP ;CONTINUE TEST
2340 007102 005700                TST      RO          ;CHECK INTERUPT
2341 007104 001001                BNE      .+4         ;SET STACK POINTER
2342 007106 104002                HLT      2          ;CHECK INTERUPT POINTER
2343 007110 005077 172250        CLR      SDQTCR
2344 007114 104400                SCOPE
2345
2346                ;TEST TO SEE IF THE
2347                ;DQ11 TRANSMITTER WILL
2348                ;INTERUPT AT PS LEVEL
2349                ;OF 5 PRIORITY.
2350
2351                ;
2352                ;
2353                ;
2354                ; TEST 50
2355                ;*****
2356 007116 012737 000050 001226  TST50: MOV      #50,TSTNO
2357 007120 012737 007220 001216  MOV      #TST51,NEXT
2358 007132 104412                MSTCLR
2359 007134 004737 016042                JSR      PC,SETV    ;INIT DQ11
2360 007140 007172                1$:          ;SET VECTORS
2361 007142 007176                2$:          ;RX INTERUPTS TO 1$
2362 007144 012700 177777                MOV      #-1,RC    ;TX INTERUPTS TO 2$
2363 007150 012737 000240 177776  MOV      #240,PS   ;SET CHECKER
2364 007156 012777 000240 172200  MOV      #240,SDQTCR ;SET PRIORITY
2365 007164 000240                NOP          ;SET PRI DONE AND IE
2366 007166 000240                NOP
2367 007170 000403                BR       3$
2368 007172 104003                1$: HLT      3          ;CONTINUE TEST
2369 007174 000002                RTI          ;UNEXPECTED RX INTERUPT
2370 007176 005100                2$: COM      RO      ;CONTINUE TEST
2371 007200 012706 001200        3$: MOV      #STACK,SP ;CHECK INTERUPT
2372 007204 005700                TST      RO          ;SET STACK POINTER
2373 007206 001001                BNE      .+4         ;CHECK INTERUPT POINTER
2374 007210 104002                HLT      2
2375 007212 005077 172146        CLR      SDQTCR
2376 007216 104400                SCOPE
2377
2378                ;TEST TO SEE IF THE
2379                ;DQ11 TRANSMITTER WILL
2380                ;INTERUPT AT PS LEVEL
2381                ;OF 4 PRIORITY.
2382                ;
2383                ;
2384                ;
2385                ; TEST 51
2386                ;*****
2387 007220 012737 000051 001226  TST51: MOV      #51,TSTNO
2388 007226 012737 007322 001216  MOV      #CHKBA,NEXT
2389 007234 104412                MSTCLR          ;INIT DQ11

```

```

2387 007236 004737 016042 JSR PC,SETV ;SET VECTORS
2388 007242 007274 1$ ;RX INTERRUPTS TO 1$
2389 007244 007300 2$ ;TX INTERRUPTS TO 2$
2390 007246 012700 177777 MOV #-1,RO ;SET CHECKER
2391 007252 012737 000200 177776 MOV #200,PS ;SET PRIORITY
2392 007260 012777 000240 172076 MOV #240,ADQTCR ;SET PRI DONE AND IE
2393 007266 000240 NOP ;
2394 007270 000240 NOP ;
2395 007272 000403 BR 3$ ;CONTINUE TEST
2396 007274 104003 1$: HLT 3 ;UNEXPECTED RX INTERJPT
2397 007276 000002 RTI ;CONTINUE TEST
2398 007300 005100 2$: COM RO ;CHECK INTERRUPT
2399 007302 012706 001200 3$: MOV #STACK,SP ;SET STACK POINTER
2400 007306 005700 TST RO ;CHECK INTERRUPT POINTER
2401 007310 001401 BEQ .+4
2402 007312 104001 HLT 1
2403 007314 005077 172044 CLR ADQTCR
2404 007320 104400 SCOPE

; IF THE DATA SET CONTROL OPTION IS INSTALLED,
; TEST 52 WILL BE EXECUTED

2412 007322 032737 010000 001510 CHKBA: BIT #BABIT,DQSTAT
2413 007330 001435 BEQ CHKCA1

; INTERRUPT LOGIC TEST
; SET DATA SET INTERRUPT ENABLE
; SET DATA SET INTERRUPT FLAG
; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

; TEST 52
; *****
2421 007332 012737 000052 001226 TST52: MOV #52,TSTNO
2422 007340 012737 007426 001216 MOV #TST53,NEXT
2423 007346 104412 MSTCLR
2424 007350 004737 016042 JSR PC,SETV ;CLEAR INTERFACE
2425 007354 007406 1$ ;SET UP INTERRUPT VECTORS
2426 007356 007410 2$ ;RECEIVER WILL INTERRUPT TO 1$
2427 007360 052777 000020 171776 BIS #BIT4,ADQTCR ;TRANSMITTER WILL INTERRUPT TO 2$
2428 007366 052777 100000 171770 BIS #BIT15,ADQTCR ;SET DATA SET INTERRUPT ENABL
2429 007374 005037 177776 CLR PS ;SET DATA SET INTERRUPT FLAG
2430 007400 000240 NOP ;SET PROCESSOR PRIORITY TO 0
2431 007402 104001 HLT 1 ;WINDOW FOR INTERRUPTS
2432 007404 000402 BR 3$ ;TRANSMITTER DID NOT INTERRUPT
2433 007406 104003 1$: HLT 3 ;WITH DATA SET INTERRUPT ENABL AND
2434 007410 000240 2$: NOP ;DATA SET INTERRUPT FLAG SET
2435 007412 012706 001200 3$: MOV #STACK,SP ;UNEXPECTED RECEIVER INTERRUPT
2436 007416 004737 016074 JSR PC,RECAT ;TRANSMITTER SHOULD INTERRUPT TO HERE
2437 007422 104400 4$: SCOPE ;RESTORE STACK
;RESTORE TRAPCATCHER
;CHECK FOR ITERATIONS. LOOP

```

2440 007424 000240 CHKCA1: NOP

:RECEIVER BASIC NPR LOGIC TEST (USING PRIMARY BUS ADDRESS AND CHARACTER COUNT)
:EXPECTED RESULTS
:RECEIVER DONE INTERRUPT OCCURS
:RECEIVER DONE (PRIMARY) = 1
:RECEIVER GO = 0
:RECEIVER P/S = 1
:NO ERROR FLAGS ARE SET
:RECEIVER BUS ADDRESS (PRIMARY) = RBUFF+1
:RECEIVER CHARACTER COUNT (PRIMARY) = 0
:CONTENTS OF RBUFF = 0

: TEST 53

:*****

2456 007426 012737 000053 001226
2457 007434 012737 007450 001214
2458 007442 012737 007752 001216
2459 007450 104413
2460 007452 104412
2461 007454 012737 000340 177776
2462 007462 012737 0000C0 017170
2463 007470 004737 016024
2464 007474 004737 016042
2465 007500 007576
2466 007502 007600
2467 007504 004737 016122
2468 007510 000 000
2469 007512 017166
2470 007514 177777
2471 007516 012777 000040 171634
2472 007524 052777 000001 171626
2473 007532 112777 000012 171630
2474 007540 052777 000020 171624
2475 007546 005037 177776
2476 007552 012737 0020C0 001244
2477 007560 005337 001244
2478 007564 001375
2479 007566 012737 000340 177776
2480 007574 104000
2481 007576 000401
2482 007600 104002
2483 007602 012706 001200
2484 007606 012706 000244
2485
2486
2487 007612 017704 171542
2488 007616 042704 177400
2489 007622 020504
2490 007624 001401
2491 007626 104004
2492 007630 005005
2493 007632 013703 001366
2494 007636 117704 171524
2495 007642 001401

TST53: MOV #53, TSTNO
MOV #99\$, RETURN
MOV #TST54, NEXT
99\$: MEMCLR
1\$: MSTCLR
MOV #340, PS ;LOCK OUT INTERRUPTS
MOV #0, T\$BUFF
JSR PC, SETMNT ;SET MAINTENANCE MODE
JSR PC, SETV ;SET UP INTERRUPT VECTORS
3\$: ;RECEIVER WILL INTERRUPT TO 3\$
4\$: ;TRANSMITTER WILL INTERRUPT TO 4\$
JSR PC, SETBABC ;SELECT RECEIVER BUS ADDRESS (PRIMARY)
.BYTE 0, 0 ;LOAD BUS ADDRESS
RBUFF -1 ;SELECT RECEIVER CHARACTER COUNT (PRIMARY)
;CHARACTER COUNT=1
MOV #BITS, @DQRC5R ;SET RECEIVER PRIMARY INTERRUPT ENABLE
BIS #BIT0, @DQRC5R ;SET RECEIVER GO
MOVB #12, @DQREG ;SELECT MISCELLANEOUS REGISTER
BIS #BIT4, @DQSEC ;FORCE RECEIVER INTERRUPT
CLR PS ;ENABLE INTERRUPTS
MOV #2000, TEMP1 ;SET UP DELAY
2\$: DEC TEMP1 ;WAIT FOR INTERRUPTS AND NPPS
BNE 2\$
MOV #340, PS ;LOCK OUT INTERRUPTS
HLT 0 ;RECEIVER DID NOT INTERRUPT
3\$: BR 5\$
4\$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
5\$: MOV #STACK, SP ;RESTORE PROCESSOR STACK
MOV #244, R5 ;(R5)=EXPECTED DATA IN RECEIVER CONTROL REGISTER
;DONE (PRIMARY)=1, INTERRUPT ENENABLE=1,
;P/S=1
; (R4)=ACTUAL DATA IN RECEIVER CONTROL REGISTER
MOV @DQRC5R, R4 ;CLEAR UNWANTED BITS
BIC #177400, R4 ;ARE EXPECTED AND RECEIVED DATA THE SAME
CMP R5, R4
BEQ 6\$
HLT 4 ;RECEIVER STATUS ERROR
6\$: CLR R5 ;(R5)=EXPECTED DATA IN ERROR REGISTER, 0
MOV @DQERR, R3 ;ADDRESS OF ERROR REGISTER
MOVB @DQERR, R4 ;(R4)=ACTUAL DATA IN ERROR REGISTER
BEQ 7\$

```

2496 007644 104006          HLT      6          ;ERROR FLAG(S) SET
2497 007646 112777 000000 171514 7$:  MOV     #0, @DQREG ;SELECT RECEIVER BUS ADDRESS (PRIMARY,
2498 007654 012702 000000          MOV     #0, R2      ;ADDRESS OF RECEIVER BUS ADDRESS
2499                                ;SECONDARY REGISTER
2500 007660 013703 001372          MOV     DQSEC, R3  ;ADDRESS OF SECONDARY REGISTER
2501 007664 012705 017167          MOV     #RBUF+1, R5 ; (R5)=EXPECTED DATA IN
2502                                ;RECEIVER BUS ADDRESS (PRIMARY) REGISTER,
2503                                ;RBUF+1
2504 007670 017704 171476          MOV     @DQSEC, R4 ; (R4)=ACTUAL DATA IN RECEIVER
2505                                ;BUS ADDRESS REGISTER (PRIMARY)
2506 007674 020504          CMP     R5, R4     ;ARE EXPECTED AND RECEIVED DATA THE SAME
2507 007676 301401          BEQ     10$
2508 007700 104007          HLT     7          ;BUS ADDRESS ERROR
2509 007702 105277 171462 10$:  INCB   @DQREG     ;SELECT CHARACTER COUNT ADD.
2510 007705 005202          INC     R2        ;UPDATE POINTER
2511 007710 012705 000000          MOV     #0, R5    ;SET FOR EXPECTED.
2512 007714 017704 171452          MOV     @DQSEC, R4 ;READ THE ACTUAL.
2513 007720 020504          CMP     R5, R4    ;ARE THEY EQUAL?
2514 007722 001401          BEQ     11$
2515 007724 104010          HLT     10       ;BR IF YES
2516 007726 012705 000000 11$:  MOV     #0, R5    ;CHARACTER COUNT ERROR
2517 007732 012703 017166          MOV     #RBUF, R3 ;SET POINTER.
2518 007736 013704 017166          MOV     RBUF, R4
2519 007742 020504          CMP     R5, R4    ;EQUAL?
2520 007744 001401          BEQ     12$
2521 007746 104011          HLT     11       ;BR IF YES
2522 007750 104400 12$:  SCOPE
2523
2524                                ;TRANSMITTER BASIC NPR LOGIC TEST (USING PRIMARY BUS ADDRESS AND CHARACTER COUNT
2525                                ;EXPECTED RESULTS
2526                                ;
2527                                ;TRANSMITTER DONE INTERRUPT OCCURS
2528                                ;TRANSMITTER DONE (PRIMARY) = 1
2529                                ;TRANSMITTER GO = 0
2530                                ;TRANSMITTER P/S = 1
2531                                ;NO ERROR FLAGS ARE SET
2532                                ;
2533                                ;TRANSMITTER BUS ADDRESS (PRIMARY) = TBUF+1
2534                                ;TRANSMITTER CHARACTER COUNT (PRIMARY) = 0
2535                                ;CONTENTS OF TRANSMITTER BUFFER = 52525
2536
2537                                ; TEST 54
2538                                ;*****
2539 007752 012737 000054 001226 TST54: MOV     #54, TSTNO
2540 007760 012737 007776 001214          MOV     #1$, RETURN
2541 007766 012737 010272 001216          MOV     #TST55, NEXT
2542 007774 104413 99$:  MEMCLR
2543 007776 104412 1$:  MSTCLR
2544 010000 012737 000340 177776          MOV     #340, PS   ;LOCK OUT INTERRUPTS
2545 010006 012737 052525 017170          MOV     #52525, TBUF
2546 010014 004737 016024          JSR     PC, SETMNT ;SET MAINTENANCE MODE
2547 010020 004737 016042          JSR     PC, SETV   ;SET UP INTERRUPT VECTORS
2548 010024 010110 3$:
2549 010026 010112 4$:
2550 010030 004737 016122          JSR     PC, SETBABC ;RECEIVER WILL INTERRUPT TO 3$
2551 010034 002000 .BYTE 2, 0 ;TRANSMITTER WILL INTERRUPT TO 4$
2552 010036 017170 TBUF ;SELECT TRANSMITTER BUS ADDRESS (PRIMARY)
;LOAD BUS ADDRESS
;SELECT TRANSMITTER CHARACTER COUNT (PRIMARY)

```

```

2552 010040 177777 -1 ; CHARACTER COUNT=1
2553 010042 012777 000040 171314 MOV #BITS,ADQTCR ; SET TRANSMITTER PRIMARY INTERRUPT ENABLE
2554 010050 052777 000001 171306 BIS #BIT0,ADQTCR ; SET TRANSMITTER GO
2555 010056 005037 177776 CLR PS ; ENABLE INTERRUPTS
2556 010062 012737 002000 001244 MOV #2000,TEMP1 ; SET UP DELAY
2557 010070 005337 001244 2$: DEC TEMP1 ; WAIT FOR INTERRUPTS AND NPRS
2558 010074 001375 9NE 2$
2559 010076 012737 000340 177776 MOV #340,PS ; LOCK OUT INTERRUPTS
2560 010104 104001 HLT 1 ; TRANSMITTER DID NOT INTERRUPT
2561 010106 000402 BR 5$
2562 010110 104003 3$: HLT 3 ; UNEXPECTED RECEIVER INTERRUPT
2563 010112 000240 4$: NOP
2564 010114 012706 001200 5$: MOV #STACK,SP ; RESTORE PROCESSOR STACK
2565 010120 012705 000244 MOV #244,R5 ; (R5)=EXPECTED DATA IN TRANSMITTER CONTROL REGIS
2566 ; DONE (PRIMARY)=1, INTERRUPT ENEABLE=1,
2567 ; P/S=1
2568 010124 017704 171234 MOV ADQTCR,R4 ; (R4)=ACTUAL DATA IN TRANSMITTER CONTROL REGISTE
2569 010132 042704 177400 BIC #177400,R4 ; CLEAR UNWANTED BITS
2570 010134 020504 CMP R5,R4 ; ARE EXPECTED AND RECEIVED DATA THE SAME
2571 010136 001401 BEQ 6$
2572 010140 040005 HLT 5 ; TRANSMITTER STATUS ERROR
2573 010142 005005 6$: CLR R5 ; (R5)=EXPECTED DATA IN ERROR REGISTER. 0
2574 010144 013703 001366 MOV DQERR,R3 ; ADDRESS OF ERROR REGISTER
2575 010150 117704 171212 MOVB ADQERR,R4 ; (R4)TUAL DATA IN ERROR REGISTER
2576 010154 001401 BEQ 7$
2577 010155 104006 HLT 6 ; ERROR FLAG(S) SET
2578 010160 112777 000002 171202 7$: MOVB #2,ADQREG ; SELECT TRANSMITTER BUS ADDRESS (PRIMARY)
2579 010166 012702 000002 MOV #2,R2 ; ADDRESS OF TRANSMITTER BUS ADDRESS
2580 ; SECONDARY REGISTER
2581 010172 013703 001372 MOV DQSEC,R3 ; ADDRESS OF SECONDARY REGISTER
2582 010176 012705 017171 MOV #TBUF+1,R5 ; (R5)=EXPECTED DATA IN
2583 ; TRANSMITTER BUS ADDRESS (PRIMARY) REGISTER.
2584 ; TBUF+1
2585 010202 017704 171164 MOV ADQSEC,R4 ; (R4)=ACTUAL DATA IN TRANSMITTER
2586 ; BUS ADDRESS REGISTER (PRIMARY)
2587 010206 020504 CMP R5,R4 ; ARE EXPECTED AND RECEIVED DATA THE SAME
2588 010210 001401 BEQ 10$
2589 010212 104007 HLT 7 ; BUS ADDRESS ERROR
2590 010214 105277 171150 10$: INCB ADQREG ; SELECT CHARACTER COUNT ADD.
2591 010220 005202 INC R2 ; UPDATE POINTER
2592 010222 012705 000000 MOV #0,R5 ; SET FOR EXPECTED.
2593 010226 017704 171140 MOV ADQSEC,R4 ; READ THE ACTUAL.
2594 010232 020504 CMP R5,R4 ; ARE THEY EQUAL?
2595 010234 001401 BEQ 11$ ; BR IF YES
2596 010236 104010 HLT 10 ; CHARACTER COUNT ERROR
2597 010240 012705 052525 11$: MOV #52525,R5 ; SET POINTER.
2598 010244 112777 000013 171116 MOVB #13,ADQREG ; SEL TX MUX REG
2599 010252 012702 000013 MOV #13,R2 ; SET FOR ERROR
2600 010256 017704 171110 MOV ADQSEC,R4 ; READ DQSEC
2601 010262 020504 CMP R5,R4 ; WAS CHAR GOOD?
2602 010264 001401 BEQ 12$ ; BR IF OK
2603 010266 104012 HLT 12 ; INCORRECT CHAR.
2604 010270 104400 12$: SCOPE
2605 ;
2606 ; RECEIVER BASIC NPR LOGIC TEST (USING SECONDARY BUS ADDRESS AND CHARACTER COUNT)
2607 ; EXPECTED RESULTS

```


M04

DZDQC MACY11 27(732) 24-SEP-76 10:14 PAGE 52
 DZDQCC.P11 DQ11 INTERRUPT AND NPR LOGIC TESTS.

```

2608 : RECEIVER DONE INTERRUPT OCCURS
2609 : RECEIVER DONE (SECONDARY) = 1
2610 : RECEIVER GO = 0
2611 : RECEIVER P/S = 1
2612 : NO ERROR FLAGS ARE SET
2613 :
2614 : RECEIVER BUS ADDRESS (SECONDARY) = RBUFF+1
2615 : RECEIVER CHARACTER COUNT (SECONDARY) = 0
2616 : CONTENTS OF RBUFF = 0
2617 :
2618 :
2619 : TEST 55
2620 : *****
2621 †TST55: MOV #55,TSTNO
2622 MOV #TST56,NEXT
2623 MSTCLR ;ISSUE A MASTER CLEAR.
2624 JSR PC,SETLOP ;SET TEST LOOP
2625 CLRB #RBUFF,#DQSEC ;SELECT RX 9A PRI.
2626 INCB #DQREG ;SET RX BA
2627 MOV #-1,#DQSEC ;SELECT RX WC PRI.
2628 BIS #BIT12+BIT0,#DQRCR ;SET FOR ONE CHAR.
2629 MOV #7000,R0 ;SET ACTIVE AND GO!!
2630 DEC R0 ;SET FOR TIME OUT DELAY
2631 BNE .-2 ;DELAY.....
2632 MOV #204,R5 ;DONE?
2633 MOV #DQRCR,R4 ;SET EXPECTED. PRI. DONE AND P/S
2634 BIC #177400,R4 ;READ RX CSF.
2635 CMP R4,R5 ;MASK UNWANTED BITS.
2636 BEQ .+4 ;IS IT CORRECT?
2637 HLT 4 ;BR IF YES.
2638 CLR #DQRCR ;RECEIVER STATUS ERROR.
2639 MOV #340,PS ;CLEAR ALL BUT RX P/S
2640 MOV #0,TBUFF ;LOCK OUT INTERRUPTS
2641 1$: MEMCLR ;CLEAR INTERFACE MEI 1ES
2642 JSR PC,SETMNT ;SET MAINTENANCE MOD.
2643 JSR PC,SETV ;SET UP INTERRUPT VECTORS
2644 3$: ;RECEIVER WILL INTERRUPT TO 3$
2645 4$: ;TRANSMITTER WILL INTERRUPT TO 4$
2646 JSR PC,SETBABC ;SELECT RECEIVER BUS ADDRESS (SECONDARY)
2647 .BYTE 4,0 ;LOAD BUS ADDRESS
2648 RBUFF ;SELECT RECEIVER CHARACTER COUNT (SECONDARY)
2649 -1 ;CHARACTER COUNT=1
2650 MOV #BITS,#DQRCR ;SET RECEIVER SECONDARY INTERRUPT ENABLE
2651 BIS #BIT0,#DQRCR ;SET RECEIVER GO
2652 MOVB #12,#DQREG ;SELECT MISCELLANEOUS REGISTER
2653 BIS #BIT4,#DQSEC ;FORCE RECEIVER INTERRUPT
2654 CLR PS ;ENABLE INTERRUPTS
2655 MOV #2000,TEMP1 ;SET UP DELAY
2656 2$: DEC TEMP1 ;WAIT FOR INTERRUPTS AND NPRS
2657 BNE 2$
2658 MOV #340,PS ;LOCK OUT INTERRUPTS
2659 HLT 0 ;RECEIVER DID NOT INTERRUPT
2660 3$: BR 5$
2661 4$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
2662 5$: MOV #STACK,SP ;RESTORE PROCESSOR STACK
2663 MOV #140,R5 ;(R5)=EXPECTED DATA IN RECEIVER CONTROL REGISTER

```

```

2664 ;DONE (SECONDARY)=1, INTERRUPT ENEABLE=1,
2665 ;P/S=1
2666 010544 017704 170610 MOV 3DQRCR,R4
2667 010550 042704 177400 BIC #177400,R4
2668 010554 020504 CMP R5,R4
2669 010556 001401 BEQ 6$
2670 010560 104004 HLT 4
2671 010562 005005 6$: CLR R5
2672 010564 013703 001366 MOV DQERR,R3
2673 010570 117704 170572 MOVB 3DQERR,R4
2674 010574 001401 BEQ 7$
2675 010576 104006 HLT 6
2676 010600 112777 000004 170562 7$: MOVB #4,3DQREG
2677 010606 012702 000004 MOV #4,R2 ;ADDRESS OF RECEIVER BUS ADDRESS (SECONDARY) REGISTER
2678 ;SECONDARY REGISTER
2679 010612 013703 001372 MOV DQSEC,R3 ;ADDRESS OF SECONDARY REGISTER
2680 010616 012705 017167 MOV #RBUF+1,R5 ;(R5)=EXPECTED DATA IN RECEIVER BUS ADDRESS (SECONDARY) REGISTER, RBUF+1
2681
2682
2683 010622 017704 170544 MOV 3DQSEC,R4 ;(R4)=ACTUAL DATA IN RECEIVER BUS ADDRESS REGISTER (SECONDARY)
2684 ;ARE EXPECTED AND RECEIVED DATA THE SAME
2685 010626 020504 CMP R5,R4
2686 010630 001401 BEQ 10$
2687 010632 104007 HLT 7 ;BUS ADDRESS ERROR
2688 010634 105277 170530 10$: INCB 3DQREG
2689 010640 005202 INC R2
2690 010642 012705 000000 MOV #0,R5
2691 010646 017704 170520 MOV 3DQSEC,R4
2692 010652 020504 CMP R5,R4
2693 010654 001401 BEQ 11$
2694 010656 104010 HLT 10 ;CHARACTER COUNT ERROR
2695 010660 012705 000000 11$: MOV #0,R5
2696 010664 012703 017166 MOV #RBUF,R3
2697 010670 013704 017166 MOV RBUF,R4
2698 010674 020504 CMP R5,R4
2699 010676 001401 BEQ QZX
2700 010700 104011 HLT 11
2701 010702 104400 QZX: SCOPE
2702
2703 ; TRANSMITTER BASIC NPR LOGIC TEST (USING SECONDARY BUS ADDRESS AND CHARACTER COUNT)
2704 ; EXPECTED RESULTS
2705 ; TRANSMITTER DONE INTERRUPT OCCURS
2706 ; TRANSMITTER DONE (SECONDARY) = 1
2707 ; TRANSMITTER GO = 0
2708 ; TRANSMITTER P/S = 1
2709 ; NO ERROR FLAGS ARE SET
2710
2711 ; TRANSMITTER BUS ADDRESS (SECONDARY) = TBUF+1
2712 ; TRANSMITTER CHARACTER COUNT (SECONDARY) = 0
2713 ; CONTENTS OF TRANSMITTER BUFFER = 177777
2714
2715 ; TEST 56
2716 ; *****
2717 010704 012737 000056 001226 TST56: MOV #56,TSTNO
2718 010712 012737 010730 001214 MOV #15,RETURN
2719 010720 012737 011330 001216 MOV #TST57,NEXT

```



```

011224 012702 000005      MOV      #6,R2          :ADDRESS OF TRANSMITTER BUS ADDRESS
011230 013703 001372      MOV      @DSEC,R3      :SECONDARY REGISTER
011234 012705 017171      MOV      #TBUF+1,R5    :ADDRESS OF SECONDARY REGISTER
                                : (R5)=EXPECTED DATA IN
                                : TRANSMITTER BUS ADDRESS (SECONDARY) REGISTER,
                                : TBUF+1
011240 017704 170126      MOV      @DSEC,R4      : (R4)=ACTUAL DATA IN TRANSMITTER
                                : BUS ADDRESS REGISTER (SECONDARY)
                                : ARE EXPECTED AND RECEIVED DATA THE SAME
011244 020504      CMP      R5,R4
011246 001401      BEQ     10$
011250 104007      HLT
                                :BUS ADDRESS ERROR
011252 105277 170112 10$: INCB   @DREG
011256 035202      INC     R2
011260 012705 000000      MOV      #0,R5
011264 017704 170102      MOV      @DSEC,R4
011270 020504      CMP      R5,R4
011272 001401      BEQ     11$
011274 104010      HLT
                                :CHARACTER COUNT ERROR
011276 012705 177777 11$: MOV      #177777,R5
011280 112777 000013 170160 MC.B   #13,@DREG
011284 012702 000013      MOV      #13,R2
011288 017704 170052      MOV      @DSEC,R4
011292 020504      CMP      R5,R4
011296 001401      BEQ     12$
011298 104012      HLT
011300 104400 12$: SCOPE

```

```

:RECEIVER NON-EXISTANT MEMORY TIMEOUT TEST
: (USING PRIMARY BUS ADDRESS AND CHARACTER COUNT)
:EXPECTED RESULTS
:
:RECEIVER DONE INTERRUPT OCCURS
:RECEIVER DONE (PRIMARY) = 1
:RECEIVER CS = 0
:RECEIVER PS = 1
:RECEIVER NON EXISTANT MEMORY ERROR FLAG = 1
:
:RECEIVER BUS ADDRESS (PRIMARY) = RBUF+1
:RECEIVER CHARACTER COUNT (PRIMARY) = 0

```

: TEST 57

```

011302 012737 000357 001226 13T57: MOV      #57,TSTNO
011306 012737 011362 001214      MOV      #15,RETURN
011310 012737 011624 001216      MOV      #TST60,NEXT
011314 012737 003340 177776      MOV      #340,PS
                                :LOCK OUT INTERRUPTS
011318 012737 104413 15: MEMCLR :CLEAR INTERFACE MEMORIES
011322 012737 104412      MSTCLR :MASTER CLEAR INTERFACE
011326 004737 016024      JSR     PC.SETMNT     :SET MAINTENANCE MODE
011330 004737 016042      JSR     PC.SETV      :SET UP INTERRUPT VECTORS
011334 011472 3$      JSR     3$           :RECEIVER WILL INTERRUPT TO 3$
011338 011474 4$      JSR     4$           :TRANSMITTER WILL INTERRUPT TO 4$
011342 004737 016122      JSR     PC.SETBABC
011346 000000 140      .BITE  0,140
011350 177320      NON.EX -1
011354 177777      -1
011358 012777 000040 167740      MOV      #BITS,@DRCR :SET RECEIVER PRIMARY INTERRUPT ENABLE

```

```
000000000000 011420 052777 700001 167732 BIS #BIT0,DQRCR :SET RECEIVER GO
000000000000 011426 122777 000012 167734 MOVB #12,DQREG :SELECT MISCELLANEOUS REGISTER
000000000000 011434 052777 000020 167730 BIS #BIT4,DQSEC :FORCE RECEIVER INTERRUPT
000000000000 011442 005037 177776 CLR PS :ENABLE INTERRUPTS
000000000000 011446 012737 002000 001244 MOV #2000,TEMP1 :SET UP DELAY
000000000000 011454 005337 001244 25: DEC TEMP1 :WAIT FOR INTERRUPTS AND MFRS
000000000000 011460 001375 000340 177776 9NE 25 :LOCK OUT INTERRUPTS
000000000000 011462 012737 000340 MOV #340,PS :RECEIVER DID NOT INTERRUPT
000000000000 011470 104000 35: HLT 0
000000000000 011472 000401 45: BR 55
000000000000 011474 104002 55: HLT 2
000000000000 011476 012706 001200 MOV #STACK_SP :UNEXPECTED TRANSMITTER INTERRUPT
000000000000 011502 012705 000244 MOV #244,R5 :RESTORE PROCESSOR STACK
000000000000 011506 017704 167646 MOV DQRCR,R4 : (R4)=EXPECTED DATA IN RECEIVER CONTROL REGISTER
000000000000 011512 042704 177400 BIC #177400,R4 : (R4)=ACTUAL DATA IN RECEIVER CONTROL REGISTER
000000000000 011516 020504 CMP R5,R4 :CLEAR UNWANTED BITS
000000000000 011520 001401 BEQ 65 :ARE EXPECTED AND RECEIVED DATA THE SAME
000000000000 011522 104004 65: HLT 4
000000000000 011524 005005 65: CLR R5 :RECEIVER STATUS ERROR
000000000000 011526 013703 001366 MOV DQERR,R3 : (R5)=EXPECTED DATA IN ERROR REGISTER, 0
000000000000 011532 017704 167630 MOV DQERR,R4 :ADDRESS OF ERROR REGISTER
000000000000 011536 100401 BMI 75 : (R4)=ACTUAL DATA IN ERROR REGISTER
000000000000 011540 104006 HLT 6
000000000000 011542 112777 000000 167620 75: MOVB #0,DQREG :ERROR FLAG(S) NOT SET
000000000000 011550 012702 000000 MOV #0,R2 :SELECT RECEIVER BUS ADDRESS (PRIMARY)
000000000000 011554 013703 001372 MOV DQSEC,R3 :ADDRESS OF RECEIVER BUS ADDRESS
000000000000 011560 012705 177321 MOV #NON.EX+1,R5 :SECONDARY REGISTER
000000000000 011564 017704 167602 MOV DQSEC,R4 :ADDRESS OF SECONDARY REGISTER
000000000000 011570 020504 CMP R5,R4 : (R5)=EXPECTED DATA IN
000000000000 011572 001401 BEQ 105 :RECEIVER BUS ADDRESS (PRIMARY) REGISTER.
000000000000 011574 104007 HLT 7 :RBUF+1
000000000000 011576 105277 167566 105: INCB DQREG : (R4)=ACTUAL DATA IN RECEIVER
000000000000 011602 005202 INC R2 :BUS ADDRESS REGISTER (PRIMARY)
000000000000 011604 012705 000000 MOV #0,R5 :ARE EXPECTED AND RECEIVED DATA THE SAME
000000000000 011610 017704 167556 MOV DQSEC,R4
000000000000 011614 020504 CMP R5,R4
000000000000 011616 001401 BEQ 115
000000000000 011620 104010 HLT 10 :CHARACTER COUNT ERROR
000000000000 011622 104400 115: SCOPE
; TRANSMITTER NON-EXISTANT MEMORY TIMEOUT TEST
; (USING PRIMARY BUS ADDRESS AND CHARACTER COUNT)
; EXPECTED RESULTS
; TRANSMITTER DONE INTERRUPT OCCURS
; TRANSMITTER DONE (PRIMARY) = 1
; TRANSMITTER GO = 0
; TRANSMITTER P/S = 1
; TRANSMITTER NON EXISTANT MEMORY ERROR FLAG = 1
; TRANSMITTER BUS ADDRESS (PRIMARY) = TBUF+1
```

E05

D2000 MACY11 27:732) 24-SEP-76 10:14 PAGE 57
D20000.P11 D011 INTERRUPT AND NPR LOGIC TESTS.

TRANSMITTER CHARACTER COUNT (PRIMARY) = 0

```

:
: TEST 60
: *****
: ST60: MOV #60, TSTNO
: MOV #1$, RETURN
: MOV #TST61, NEXT
: MOV #340, PS
: LOCK OUT INTERRUPTS
: CLEAR INTERFACE MEMORIES
: MASTER CLEAR INTERFACE
: SET MAINTENANCE MODE
: SET UP INTERRUPT VECTORS
: RECEIVER WILL INTERRUPT TO 3$
: TRANSMITTER WILL INTERRUPT TO 4$
1$: MEMCLR
MSTCLR
JSR PC, SETMNT
JSR PC, SETV
3$:
4$:
JSR PC, SETBABC
.BYTE 2, 140
NON.EX -1
MOV #BITS, DDQTCR
BIS #BITC, DDQTCR
CLR PS
MOV #2000, TEMP1
2$: DEC TEMP1
BNE 2$
MOV #340, PS
HLT 1
BR 5$
3$: HLT 3
4$: NOP
5$: MOV #STACK, SP
MOV #244, R5
: RESTORE PROCESSOR STACK
: (R5)=EXPECTED DATA IN TRANSMITTER CONTROL REGIS
: DONE (PRIMARY)=1, INTERRUPT ENABLE=1.
: P/S=1
: (R4)=ACTUAL DATA IN TRANSMITTER CONTROL REGISTE
: CLEAR UNWANTED BITS
: ARE EXPECTED AND RECEIVED DATA THE SAME
6$: HLT 5
CLR R5
: TRANSMITTER STATUS ERROR
: (R5)=EXPECTED DATA IN ERROR REGISTER, 0
: ADDRESS OF ERROR REGISTER
: (R4)TUAL DATA IN ERROR REGISTER
7$: HLT 6
MOVB #2, DDQREG
MOV #2, R2
: ERR?? FLAG(S) NOT SET
: SELECT TRANSMITTER BUS ADDRESS (PRIMARY)
: ADDRESS OF TRANSMITTER BUS ADDRESS
: SECONDARY REGISTER
: ADDRESS OF SECONDARY REGISTER
: (R5)=EXPECTED DATA IN
: TRANSMITTER BUS ADDRESS (PRIMARY) REGISTER.
: TBUF+1
: (R4)=ACTUAL DATA IN TRANSMITTER
: BUS ADDRESS REGISTER (PRIMARY)
: ARE EXPECTED AND RECEIVED DATA THE SAME
8$: MOV DDQSEC, R3
MOV #NON.EX+1, R5
9$: MOV DDQSEC, R4
CMP R5, R4
BEQ 10$
HLT 7
10$: INCB DDQREG

```

```

012064 005202
012066 012705 000000
012072 017704 167274
012076 020504
012100 001401
012102 104010
012104 104400
012106 012737 000061 001226
012114 012737 012140 001214
012122 012737 012272 001216
012130 012737 003340 177776
012136 104413
012140 104412
012142 004737 016024
012146 004737 016122
012152 000 000
012154 017166
012156 177777
012160 052777 000001 167172
012166 177777 000012 167174
012174 052777 000020 167170
012202 012737 002000 001244
012210 105777 167144
012214 100412
012216 005337 001244
012222 001372
012224 017704 167130
012230 042704 177400
012234 012705 000204
012240 104004
012242 104412
012244 032777 000020 167106
012252 001406
012254 005005
012256 017704 167076
012262 042704 177400
012266 104004
012270 104400
012272 012737 000062 001226
012300 012737 012324 001214

```

```

INC R2
MOV #0,R5
MOV @DQSEC,R4
CMP R5,R4
BEQ 11$
HLT 10 ; CHARACTER COUNT ERROR
11$: SCOPE

```

```

;RECEIVER P/S MASTER CLEAR TEST
;EXECUTE 1 NPR CYCLE TO FORCE RECEIVER P/S TO A 1
;ISSUE MASTER CLEAR
;VERIFY THAT RECEIVER P/S WAS CLEARED

```

```

: TEST 61
*****

```

```

TST61: MOV #61,TSTNO
MOV #1$,RETURN
MOV #TST62,NEYT
MOV #340,PS ; LOCK OUT INTERRUPTS.
1$: MEMCLR ; MASTER CLEAR INTERFACE
MSTCLR ; SET MAINTENANCE MODE
JSR PC,SETMNT
JSR PC,SETBABC
.BYTE 0,0
RBUFF -1
BIS #BIT0,@DQRCR
MOVB #12,@DQREG ; SELECT MISC REGISTER
BIS #BIT4,@DQSEC ; FORCE RX NPR
MOV #2000,TEMP1 ; SET FOR TIME OUT
2$: TSTB @DQRCR ; PRIMARY DONE UP
BMI 3$ ; BR IF PRI DONE SET.
DEC TEMP1 ; DELAY
BNE 2$ ; KEEP WAITING
MOV @DQRCR,R4 ; SAVE THE CSR
BIC #177400,R4 ; CLEAR UNWANTED BITS.
MOV #204,R5 ; SET EXPECTED.
HLT 4
3$: MSTCLR
BIT #BIT4,@DQRCR
BEQ 4$
CLR R5
MOV @DQRCR,R4
BIC #177400,R4
HLT 4
4$: SCOPE

```

```

;TRANSMITTER P/S MASTER CLEAR TEST
;EXECUTE 1 NPR CYCLE TO FORCE TRANSMITTER P/S TO A 1
;ISSUE MASTER CLEAR
;VERIFY THAT TRANSMITTER P/S WAS CLEARED

```

```

: TEST 62
*****

```

```

TST62: MOV #62,TSTNO
MOV #1$,RETURN

```



```

3000 012306 012737 012442 001216      MOV      #TST63,NEXT
3001 012314 012737 000340 177776      MOV      #340,PS          ;LOCK OUT INTERUPTS.
3002 012322 104413      MEMCLR
3003 012324 104412      1$:      MSTCLR          ;MASTER CLEAR INTERFACE
3004 012326 004737 016024      JSR      PC,SETMNT      ;SET MAINTENANCE MODE
3005 012332 004737 016122      JSR      PC,SETBABC
3006 012336      002      .BYTE      2,0
3007 012340 017170      TBUF
3008 012342 177777      -1
3009 012344 052777 000001 167012      BIS      #BIT0,DDQTCR
3010 012352 012737 002000 001244      MOV      #2000,TEMP1    ;SET FOR TIME OUT
3011 012350 105777 167000      2$:      TSTB      DDQTCR      ;PRIMARY DONE UP
3012 012354 100412      SMI      3$            ;BR IF PRI DONE SET.
3013 012366 005337 001244      DEC      TEMP1         ;DELAY
3014 012372 001372      BNE      2$           ;KEEP WAITING
3015 012374 017704 166764      MOV      DDQTCR,R1      ;SAVE THE CSR
3016 012400 042704 177400      BIC      #177400,R4     ;CLEAR UNWANTED BITS.
3017 012404 012705 000204      MOV      #204,R5       ;SET EXPECTED.
3018 012410 104005      HLT
3019 012412 104412      3$:      MSTCLR
3020 012414 032777 000320 166742      BIT      #BIT4,DDQTCR
3021 012422 001406      BEQ      4$
3022 012424 005005      CLR      R5
3023 012426 017704 166732      MOV      DDQTCR,R4
3024 012432 042704 177400      BIC      #177400,R4
3025 012436 104005      HLT
3026 012440      4$:      SCOPE
3027
3028      ;TRANSMITTER NPR DATA TEST (STEP MODE)
3029      ;EXECUTE 1 TRANSMITTER NPR CYCLE FOR EACH DATA PATTERN 0-177777
3030      ;VERIFY THAT TRANSMITTER BUFFER CONTAINS THE CORRECT DATA
3031
3032      : TEST 63
3033      :*****
3034      :TST63: MOV      #63,TSTNO
3035      :      MOV      #1$,RETURN
3036      :      MOV      #10,ICOUNT
3037      :      MOV      #.EOP,NEXT
3038      :      MOV      #2$,LOCK
3039      :      MOV      #340,PS          ;LOCK OUT INTERUPTS.
3040      :      MEMCLR          ;CLEAR ALL MEMORIES
3041      :      MSTCLR          ;INITIALIZE DEVICE
3042      :      CLR      ZDATA      ;CLEAR POINTER
3043      :      MOV      #0,R0
3044      :      MOV      DQSEC,R3
3045      :      MOV      #13,R2          ;SET FOR ERROR
3046      :      MSTCLR          ;SET FOR ERROR (TX MUX)
3047      :      JSR      PC,SETSTP      ;GIVE ANOTHER MASTER CLEAR
3048      :      JSR      PC,SETBABC
3049      :      .BYTE      2,0          ;SET BUS ADDR. AND WC
3050      :      TBUF
3051      :      -1
3052      :      MOV      ZDATA,R5      ;SET EXPECTED
3053      :      MOV      R5,TBUF        ;LOAD CHARACTER
3054      :      MOV      #BIT0,DDQTCR  ;SET TX GO.
3055      :      MOV      #2000,TEMP1    ;SET FOR DELAY

```

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DZDQCC.P11 DQ11 INTERRUPT AND NFR LOGIC TESTS.

```
3056 012576 105777 166562 3$: TSTB 2DQTCR ;TX PRI DONE?  
3057 012602 100404 4$ CMI 4$ ;BR IF YES  
3058 012604 005337 001244 DEC TEMP1 ;DELAY  
3059 012610 001372 BNE 3$ ;KEEP DELAYING  
3060 012612 104003 HLT 3 ;TX PRI DONE FAILED TO SET  
3061 012614 112777 000013 166546 4$: MOVB #13,2DQREG ;SELECT TX MUX REG.  
3062 012622 017704 166544 MOV 2DQSEC,R4 ;READ MUX  
3063 012626 020504 CMP R5,R4 ;GOOD CHARACTER?  
3064 012630 001401 BEQ 5$ ;BR IF GOOD  
3065 012632 104012 HLT 12 ;DATA COMPARISON ERROR  
3066 012634 104401 5$: SCOPI ;LOCK ON DATA (SW09=1)  
3067 012636 005237 017172 INC ZDATA ;UPDATE CHARACTER  
3068 012642 005300 DEC R0 ;UPDATE COUNTER  
3069 012644 001332 BNE 2$ ;GO DO MORE CHARACTERS  
3070 012646 104400 6$: SCOPE ;SCOPE THIS TEST.  
3071  
3072 ;END OF PASS  
3073 ;TYPE NAME OF TEST  
3074 ;UPDATE PASS COUNT  
3075 ;CHECK FOR EXIT TO ACT-11  
3076 ;RESTART TEST  
3077  
3078 012650 005037 001234 .EOP: CLR LSTERR ;CLEAR LAST ERROR PC  
3079 012654 005037 001312 CLR ERRFLG ;CLEAR ERROR FLAG  
3080 012660 005237 001230 INC PASCNT ;UPDATE PASS COUNT  
3081 012664 104402 TYPE  
3082 012666 015100 MEPASS  
3083 012670 104402 TYPE  
3084 012672 015261 MCSRX  
3085 012674 104411 CNVRT  
3086 012676 013006 XCSR  
3087 012700 104402 TYPE  
3088 012702 015267 MVECX  
3089 012704 104411 CNVRT  
3090 012706 013014 XVEC  
3091 012710 104402 TYPE  
3092 012712 015275 MPASSX  
3093 012714 104411 CNVRT  
3094 012716 013022 XPASS  
3095 012720 104402 TYPE  
3096 012722 015306 MERRX  
3097 012724 104411 CNVRT  
3098 012726 013030 XERR  
3099 012730 013777 001230 166244 MOV PASCNT,2LIGHTS ;DISPLAY PASS COUNT  
3100 012736 005337 001276 DEC SAVNUM  
3101 012742 001013 BNE RESTRT  
3102 012744 013737 001504 001276 MOV DQNUM,SAVNUM  
3103 012752 013701 000042 MOV #42,R1 ;CHECK FOR ACT-11 OR DDP  
3104 012756 001405 BEQ RESTRT ;IF NOT, CONTINUE TESTING  
3105 012760 000005 RESET  
3106 012762 LOGICAL:  
3107 012762 004711 JSR PC,(R1)  
3108 012764 000240 NOP  
3109 012766 000240 NOP  
3110 012770 000240 NOP  
3111 012772 104414 RESTRT: CKSWR
```

DZDQC MACY11 27(732) 24-SEP-76 10:14 PAGE 61
 DZDQCC.P11 END OF PASS ROUTINE

3112	012774	012737	002254	001214		MOV	#TST1, RETURN
3113	013002	000137	002254			JMP	TST1
3114	013006	000001			XCSR:	1	
3115	013010	006	002			.BYTE	6,2
3116	013012	001360				DQRCSR	
3117	013014	000001			XVEC:	1	
3118	013016	003	002			.BYTE	3,2
3119	013020	001350				DQRVEC	
3120	013022	000001			XPASS:	1	
3121	013024	006	002			.BYTE	6,2
3122	013026	001230				PASCNT	
3123	013030	000001			XERR:	1	
3124	013032	006	002			.BYTE	6,2
3125	013034	001232				ERRCNT	
3126							
3127							
3128							
3129	013036	104414					
3130	013040	032777	040000	166132	.SCOPE:	CKSWR	
3131	013046	001407			TST:	BIT	#BIT14, QSWR
3132	013050	000432				BEQ	1\$
3133	013052	105777	166126			BR	3\$
3134	013056	100027				TSTB	@TKCSR
3135	013060	017700	166122			BPL	3\$
3136	013064	000412				MOV	@TKDBR, R0
3137	013066	032777	004000	166104	1\$:	BR	2\$
3138	013074	001006				BIT	#SW11, QSWR
3139	013076	005237	001224			BNE	2\$
3140	013102	023737	001224	001222		INC	LPCNT
3141	013110	001012				CMP	LPCNT, ICOUNT
3142	013112	105037	001312		2\$:	BNE	3\$
3143	013116	005037	001224			CLRB	ERRFLG
3144	013122	012737	000012	001222		CLR	LPCNT
3145	013130	013737	001216	001214		MOV	#10, ICOUNT
3146	013136	013716	001214		3\$:	MOV	NEXT, RETURN
3147	013142	000002				MOV	RETURN, (SP)
3148	013144	001407			BRW:	RTI	
3149	013146	000432			BRX:	1407	
3150						432	
3151							
3152							
3153	013150	104414					
3154	013152	032777	001000	166020	.SCOPE1:	CKSWR	
3155	013160	001402				BIT	#SW09, QSWR
3156	013162	013716	001220			BEQ	1\$
3157	013166	000002			1\$:	MOV	LOCK, (SP)
3158						RTI	
3159							
3160							
3161	013170	010546			.TYPE:	MOV	R5, -(SP)
3162	013172	017605	000002			MOV	@2(SP), R5
3163	013176	062766	000002	000002		ADD	#2, 2(SP)
3164	013204	005737	014660		1\$:	TST	@RDSW
3165	013210	001004				BNE	300\$
3166	013212	032777	010000	165760		BIT	#SW12, QSWR
3167	013220	001024				BNE	3\$

;SCOPE LOOP AND INTERATION HANDLER

;CHECK FOR FREEZE ON CURRENT DATA

;TELETYPE OUTPUT ROUTINE

3168	013222	105715			300\$:	TSTB	(R5)
3169	013224	100014				BPL	2\$
3170	013226	105777	165756			TSTB	@TPCSR
3171	013232	100375				BPL	.-4
3172	013234	012777	000015	165750		MOV	#15,@TPDDBR
3173	013242	105777	165742			TSTB	@TPCSR
3174	013246	100375				BPL	.-4
3175	013250	012777	000012	165734		MOV	#12,@TPDDBR
3176	013256	105777	165726		2\$:	TSTB	@TPCSP
3177	013262	100375				BPL	2\$
3178	013264	112577	165722			MOVB	(R5)+,@TPDDBR
3179	013270	001345				BNE	1\$
3180	013272	012605			3\$:	MOV	(SP)+,R5
3181	013274	000002				RTI	

;ASCII STRING INPUT ROUTINE

3182							
3183							
3184							
3185	013276	010346			.INSTR:	MOV	R3,-(SP)
3186	013300	010446				MOV	R4,-(SP)
3187	013302	017637	000004	013320		MOV	@4(SP),MSG
3188	013310	062766	000002	000004		ADD	#2,4(SP)
3189	013316	104402			.INST1:	TYPE	
3190	013320	000000			.MSG:	0	
3191	013322	012704	015452			MOV	#INBUF,R4
3192	013326	012703	000007			MOV	#7,R3
3193	013332	105777	165646		1\$:	TSTB	@TKCSR
3194	013336	100375				BPL	1\$
3195	013340	117714	165642			MOVB	@TKDDBR,(R4)
3196	013344	142714	000200			BICB	#200,(R4)
3197	013350	121427	000025			CMPB	(R4),#25
3198	013354	001003				BNE	200\$
3199	013356	104402	015040			TYPE,MCRLF	
3200	013362	000755				BR	.INST1
3201	013364	122427	000015		200\$:	CMPB	(R4)+,#15
3202	013370	001423				BEQ	INSTR2
3203	013372	117777	165610	165612		MOVB	@TKDDBR,@TPDDBR
3204	013400	105777	165604		2\$:	TSTB	@TPCSR
3205	013404	100375				BPL	2\$
3206	013406	005303				DEC	R3
3207	013410	001350				BNE	1\$
3208	013412	000402				BR	.INSTG
3209	013414	010346			.INSTE:	MOV	R3,-(SP)
3210	013416	010446				MOV	R4,-(SP)
3211	013420	104402			.INSTG:	TYPE	
3212	013422	015034				MQM	
3213	013424	005737	014660			TST	@#RDSW
3214	013430	001402				BEQ	400\$
3215	013432	104402	015040			TYPE,MCRLF	
3216	013436	000727			400\$:	BR	.INST1
3217	013440	012604			INSTR2:	MOV	(SP)+,R4
3218	013442	012603				MOV	(SP)+,R3
3219	013444	000002				RTI	

;IS IT <↑G>

;CONVERT ASCII STRING TO OCTAL

3220							
3221							
3222							
3223	013446	010546			.PARAM:	MOV	R5,-(SP)

3224	013450	010446		MOV	R4, -(SP)	
3225	013452	016605	000004	MOV	4(SP), R5	
3226	013456	012537	013652	MOV	(R5)+, LOLIM	
3227	013462	012537	013654	MOV	(R5)+, HILIM	
3228	013466	012537	013656	MOV	(R5)+, DEVADR	
3229	013472	112537	013660	MOVB	(R5)+, LOBITS	
3230	013476	112537	013661	MOVB	(R5)+, ADRCNT	
3231	013502	010566	000004	MOV	R5, 4(SP)	
3232	013506	005005		PARAM1: CLR	R5	
3233	013510	012704	015452	MOV	#INBUF, R4	
3234	013514	122714	000015	CMPB	#15, (R4)	
3235	013520	001420		BEQ	PARERR	
3236	013522	121427	000060	1\$: CMPB	(R4), #6C	
3237	013526	002415		BLT	PARERR	
3238	013530	121427	000067	CMPB	(R4), #67	
3239	013534	003012		BGT	PARERR	
3240	013536	142714	000060	BICB	#60, (R4)	
3241	013542	152405		BISB	(R4)+, R5	
3242	013544	122714	000015	CMPB	#15, (R4)	
3243	013550	001414		BEQ	LIMITS	
3244	013552	006305		ASL	R5	
3245	013554	006305		ASL	R5	
3246	013556	006305		ASL	R5	
3247	013560	000760		BR	1\$	
3248	013562	122714	000015	PARERR: CMPB	#15, (R4)	; IS FIRST CHARACTER A <CR>
3249	013566	001003		BNE	120\$	
3250	013570	005737	014660	TST	#ARDSW	; IS CKSWR ROUTINE BEING USED
3251	013574	001023		BNE	PARTI	
3252	013576	104404		120\$: INSTER		
3253	013600	000742		BR	PARAM1	
3254						
3255						; TEST TO SEE IF NUMBER .S WITHIN LIMITS
3256						
3257	013602	020537	013654	LIMITS: CMP	R5, HILIM	
3258	013606	101365		BHI	PARERR	
3259	013610	020537	013652	CMP	R5, LOLIM	
3260	013614	103762		BLO	PARERR	
3261	013616	133705	013660	BITB	LOBITS, R5	
3262	013622	001357		BNE	PARERR	
3263						
3264						; STORE NUMBER AT SPECIFIED ADDRESS
3265						
3266	013624	013704	013656	1\$: MOV	DEVADR, R4	
3267	013630	010524		MOV	R5, (R4)+	
3268	013632	062705	000002	ADD	#2, R5	
3269	013636	105337	013661	DECB	ADRCNT	
3270	013642	001372		BNE	1\$	
3271	013644	012604		PARTI: MOV	(SP)+, R4	
3272	013646	012605		MOV	(SP)+, R5	
3273	013650	000002		RTI		
3274	013652	000000		LOLIM: 0		
3275	013654	000000		HILIM: 0		
3276	013656	000000		DEVADR: 0		
3277	013660	000000		LOBITS: 0		
3278		013661		ADRCNT=LOBITS+1		
3279						

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3280                                     ;SAVE PC OF TEST THAT FAILED AND RO-R5
3281
3282 013662 016637 000004 001274 .SAV05: MOV     4(SP),SAVPC
3283
3284                                     ;SAVE RO-R5
3285
3286 013670 010537 001270          SV05:  MOV     R5,SAVR5
3287 013674 010437 001266          MOV     R4,SAVR4
3288 013700 010337 001264          MOV     R3,SAVR3
3289 013704 010237 001262          MOV     R2,SAVR2
3290 013710 010137 001260          MOV     R1,SAVR1
3291 013714 010037 001256          MOV     R0,SAVR0
3292 013720 000002          RTI
3293
3294                                     ;RESTORE RO-R5
3295
3296 013722 013700 001256          .RES05: MOV    SAVR0,R0
3297 013726 013701 001260          MOV    SAVR1,R1
3298 013732 013702 001262          MOV    SAVR2,R2
3299 013736 013703 001264          MOV    SAVR3,R3
3300 013742 013704 001266          MOV    SAVR4,R4
3301 013746 013705 001270          MOV    SAVR5,R5
3302 013752 000002          RTI
3303
3304                                     ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
3305
3306 013754 104402          .CONVR: TYPE
3307 013756 015040          MCRLF
3308 013760 010046          .CNVRT: MOV    R0,-(SP)
3309 013762 010146          MOV    R1,-(SP)
3310 013764 010346          MOV    R3,-(SP)
3311 013766 010446          MOV    R4,-(SP)
3312 013770 010546          MOV    R5,-(SP)
3313 013772 017601 000012          MOV    @12(SP),R1
3314 013776 013737 015514 001250          MOV    TEMP,TEMP3
3315 014004 062766 000002 000012          ADD    #2,12(SP)
3316 014012 012137 014174          MOV    (R1)+,WRDCNT
3317 014016 112137 014176          1$:  MOVB  (R1)+,CHRCNT
3318 014022 112137 014177          MOVB  (R1)+,SPACNT
3319 014026 013137 014200          MOV    @2(R1)+,BINWRD
3320 014032 013704 014200          2$:  MOV    BINWRD,R4
3321 014036 113705 014176          MOVB  CHRCNT,R5
3322 014042 012700 015514          MOV    #TEMP,R0
3323 014046 010403          3$:  MOV    R4,R3
3324 014050 042703 177770          BIC    #177770,R3
3325 014054 062703 000060          ADD    #060,R3
3326 014060 110320          MOVB  R3,(R0)+
3327 014062 000241          CLC
3328 014064 006004          ROR    R4
3329 014066 000241          CLC
3330 014070 006004          ROR    R4
3331 014072 000241          CLC
3332 014074 006004          ROR    R4
3333 014076 005305          DEC    R5
3334 014100 001362          BNE   3$
3335 014102 012703 015556          MOV    #MDATA,R3

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 DZDQCC.P11 GENERAL UTILITIES (TYPE OUT, ERROR, SCOPE, ETC.)

3336	014106	114023		4\$:	MOVB	-(R0), (R3)+	
3337	014110	105337	014176		DECB	CHRCNT	
3338	014114	001374			BNE	4\$	
3339	014116	105737	014177		TSTB	SPACNT	
3340	014122	001405			BEQ	6\$	
3341	014124	112723	000040	5\$:	MOVB	#040, (R3)+	
3342	014130	105337	014177		DECB	SPACNT	
3343	014134	001373			BNE	5\$	
3344	014136	105013		6\$:	CLRB	(R3)	
3345	014140	104402			TYPE		
3346	014142	015556			MDATA		
3347	014144	005337	014174		DEC	WRDCNT	
3348	014150	001322			BNE	1\$	
3349	014152	013737	001250 015514		MOV	TEMP3, TEMP	
3350	014160	012605			MOV	(SP)+, R5	
3351	014162	012604			MOV	(SP)+, R4	
3352	014164	012603			MOV	(SP)+, R3	
3353	014166	012601			MOV	(SP)+, R1	
3354	014170	012600			MOV	(SP)+, R0	
3355	014172	000002			RTI		
3356	014174	000000			WRDCNT:	0	
3357	014176	000000			CHRCNT:	0	
3358		014177			SPACNT=	CHRCNT+1	
3359	014200	000000			BINWRD:	0	
3360							; TRAP DISPATCH SERVICE
3361							; ARGUMENT OF TRAP IS EXTRACTED
3362							; AND USED AS OFFSET TO OBTAIN POINTER
3363							; TO SELECTED SUBROUTINE
3364							
3365	014202	011646		.TRPSR:	MOV	(SP), -(SP)	; GET PC OF RETURN
3366	014204	152716	000002		SUB	#2, (SP)	; =PC OF TRAP
3367	014210	017616	000000		MOV	@(SP), (SP)	; GET TRP
3368	014214	006316		TRPOK:	ASL	(SP)	; MULTIPLY TRAP ARG BY 2
3369	014216	042716	177001		BIC	#177001, (SP)	; CLEAR UNWANTED BITS
3370	014222	062716	001314		ADD	#.TRPTAB, (SP)	; POINTER TO SUBROUTINE ADDRESS
3371	014226	017616	000000		MOV	@(SP), (SP)	; SUBROUTINE ADDRESS
3372	014232	000136			JMP	@(SP)+	; GO TO SUBROUTINE
3373							
3374							; ERROR HANDLER
3375							
3376	014234	104414		.HLT:	CKSWR		
3377	014236	032777	010000 164734		BIT	#SW12, @SWR	
3378	014244	001406			BEQ	XBX	
3379	014246	105777	164736		TSTB	@TPCSR	
3380	014252	100003			BPL	XBX	
3381	014254	112777	000207 164730		MOVB	#207, @TPDBR	
3382	014262	032777	020000 164710	XBX:	BIT	#SW13, @SWR	
3383	014270	001074			BNE	HALTS	
3384	014272	021637	001234		CMP	(SP), LSTERR	
3385	014276	001404			BEQ	1\$	
3386	014300	011637	001234		MOV	(SP), LSTERR	
3387	014304	105037	001312		CLRB	ERRFLG	
3388	014310	104406		1\$:	SAVDS		
3389	014312	011605			MOV	(SP), R5	
3390	014314	162705	000002		SUB	#2, R5	
3391	014320	011504			MOV	(R5), R4	

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 DZDQCC.P11 GENERAL UTILITIES (TYPE OUT,ERROR,SCOPE,ETC.)

3392	014322	006304			ASL	R4
3393	014324	061504			ADD	(R5),R4
3394	014326	006304			ASL	R4
3395	014330	042704	177001		BIC	#177001,R4
3396	014334	062704	016744		ADD	#.ERRTAB,R4
3397	014340	012437	014432		MOV	(R4)+,ERRMSG
3398	014344	012437	014444		MOV	(R4)+,DATAHD
3399	014350	011437	014456		MOV	(R4),DATABP
3400	014354	105737	001312		TSTB	ERRFLG
3401	014360	001403			BEQ	TYPMSG
3402	014362	005737	014456		TST	DATABP
3403	014356	001027			BNE	TYPDAT
3404	014370	104402			TYPMSG:	TYPE
3405	014372	015317			MTSTN	
3406	014374	104411			CNVRT	
3407	014376	014556			XTSTN	
3408	014400	104402			TYPE	
3409	014402	015405			MERRPC	
3410	014404	104411			CNVRT	
3411	014406	014550			ERTABO	
3412	014410	104402			TYPE	
3413	014412	015040			MCRLF	
3414	014414	112737	177777	001312	MOVB	#-1,ERRFLG
3415	014422	005737	014432		TST	ERRMSG
3416	014426	001402			BEQ	WRKO.FM
3417	014430	104402			TYPE	
3418	014432	000000			ERRMSG:	0
3419	014434				WRKO.FM:	
3420	014434	005737	014444		TST	DATAHD
3421	014440	001402			BEQ	TYPDAT
3422	014442	104402			TYPE	
3423	014444	000000			DATAHD:	0
3424	014446	005737	014456		TYPDAT:	TST
3425	014452	001402			BEQ	DATABP
3426	014454	104410			CONVRT	RESREG
3427	014456	000000			DATABP:	0
3428	014460	104407			RESREG:	RESOS
3429	014462	005777	164512		HALTS:	TST
3430	014466	100005			BPL	2SWR
3431	014470	010046			PUSHRO	EXITER
3432	014472	016600	000002		MOV	2(SP),R0
3433	014476	000000			HALT	
3434	014500	012600			POPPO	
3435	014502	104414			EXITER:	CKSWR
3436	014504	005237	001232		INC	ERRCNT
3437	014510	032777	000400	164462	BIT	#SW08,2SWR
3438	014516	001007			BNE	1\$
3439	014520	032777	002000	164452	BIT	#SW10,2SWR
3440	014526	001407			BEQ	2\$
3441	014530	013737	001216	001214	MOV	NEXT,RETURN
3442	014536	012706	001200		1\$:	MOV
3443	014542	000177	164446		JMP	#STACK,SP
3444	014546	000002			2\$:	RTI
3445	014550	000001			ERTABO:	1
3446	014552	006	002		.BYTE	6,2
3447	014554	001274			SAVPC	


```

MACY:1 27.732 GENERAL
015030 000176 17777 SWREG
015031 000176 001 .BYTE 0,1
015032 005033 015040 OUT: TYPE,MCRLF
015033 000002 014660 CLR 3RDSW
015034 000002 SWREG: 1
015035 000004 002 .BYTE 6,2
015036 000176 SWREG
015037 057377 000107 SCNTG: .ASCIZ (377) /IG/
015038 051127 051127 020075 SMSWR: .ASCIZ (377) /SWR= /
015039 000040 047040 053535 SMNEW: .ASCIZ / NEW= /
015040 020040 .EVEN
015041 015034 020040 000077 MQM: .ASCIZ '??'
015042 000377 MCRLF: .ASCIZ (377)
015043 050377 051127 043040 MPFAIL: .ASCIZ (377) /PWR FAILED. RESTART AT TEST /
015044 044501 042514 027104
015045 051505 051505 040524
015046 052123 040440 020124
015047 042524 052123 000040
015048 042116 042116 050040 MEPASS: .ASCIZ (377) /END PASS DZDQC /
015049 020123 055104
015050 020102 000040
015051 051120 051120 043017 MR: .ASCIZ (377) /R/
015052 020115 047111 MERR2: .ASCIZ (377) /PROGRAM INDICATES NO DEVICES PRESENT./
015053 040503 042524
015054 047516 042040
015055 041511 051505
015056 042522 042523
015057 000056 043125 MERR3: .ASCIZ (377) /INSUFFICIENT DATA!
015058 044503 047105
015059 040504 040524
015060 051505 020124 MTSTPC: .ASCIZ (377) /TEST PC-/
015061 000055
015062 041517 020113 MLOCK: .ASCIZ (377) /LOCK ON SELECTED TEST.
015063 051440 046105
015064 042524 020104
015065 052123 000
015066 051123 020072 MCSRX: .ASCIZ /CSR: /
015067 041505 020072 MVECX: .ASCIZ /VEC: /
015068 051501 042523 MPASSX: .ASCIZ /P : /
015069 000040
015070 047522 051522 MERRX: .ASCIZ /ERRORS: /
015071 000
015072 052377 051505 M...TN: .ASCIZ (377) (377) /TEST NO: /
015073 047516 020072
015074 042523 020124 MNEW: .ASCIZ (377) /SE SWITCH REG TO DQ11'S DESIRED ACTIVE.
015075 052111 044103

```

```

015346 051040 043505 052040
015354 020117 050504 030461
015362 051447 042040 051505
015370 051111 042105 040440
015378 052103 053111 021105
015404 000000
015405 120000
015412 046777 035103 000040
015420 020106 050101 047440
015428 051440 050504 030461
015436 051523 040524 052524
015440 000000
015443 000002
015444 000006 003
015445 001244
015446 000006 002
015450 001246
015452 000000
015514 000000
015556 000000
015620 000000
015620 112777 000012 163542
015626 012777 000040 163536
015624 000002
015636 105077 163526
015636 012700 000020
015642 152777 000020 163514
015646 142777 000140 163506
015654 005077 163504
015662 105277 163476
015666 005300
015672 001364
015674 105077 163466
015676 105077 163454
015702 012700 000020
015706 112777 000010 163450
015712 005077 163446
015720 112777 000014 163436
015724 005077 163434
015732 105277 163420
015742 005300
015744 001362

```

```

MERRPC: .ASCIZ /PC: /
XHEAD: .ASCIZ <377>/MAP OF DQ11 STATUS/<377>

```

```

.EVEN
XSTAT0: 2
        .BYTE 6,3
        .TEMP1
        .BYTE 6,2
        .TEMP2

```

```

.EVEN
;BUFFERS FOR INPUT-OUTPUT

```

```

INBUF: 0
      = +40
TEMP: 0
     = +40
MDATA: 0
      = +40

```

```

;MASTER CLEAR DQ11 INTERFACE

```

```

.MSTCLR:
MOV    #12, D0REG
MOV    #BITS, D0QSEC
RTI

```

```

;CLEAR INTERFACE MEMORIES

```

```

.MEMCLR:
CLR    D0QREG
MOV    #16, R0
15:   BIS    #BIT4, D0QREG
      BIC    #140, D0QREG
      CLR    D0QSEC
      INCB  D0QREG
      DEC   R0
      BNE   15
      CLR    D0QREG
      CLR    D0QRC5H
MOV    #16, R0
25:   MOV    #10, D0QREG
      CLR    D0QSEC
      MOV    #14, D0QREG
      CLR    D0QSEC
      INCB  D0QRC5H
      DEC   R0
      BNE   25

```

```

3616 015746 105077 163410 CLR B 2DQRC5H
3617 015752 005077 163402 CLR 2DQRC5R
3618 015756 005077 163402 CLR 2DQTC5R
3619 015762 005077 163400 CLR 2DQERR
3620 015766 000002 RTI
;SET STEP MODE
3621 015770 112777 000012 163372 SETSTP: MOV B #12, 2DQREG
3622 015776 052777 000002 163366 BIS #BIT1, 2DQSEC
3623 016004 000207 RTS PC
;SET TEST LOOP
3624 016006 112777 000012 163354 SETLOP: MOV B #12, 2DQREG
3625 016014 052777 000010 163350 BIS #BIT3, 2DQSEC
3626 016022 000207 RTS PC
;SET MAINTENANCE MODE
3627 016024 112777 000012 163336 SETMNT: MOV B #12, 2DQREG
3628 016032 052777 000012 163332 BIS #BIT1+BIT3, 2DQSEC
3629 016040 000207 RTS PC
;SET INTERRUPT VECTORS
3630 016042 011605 SETV: MOV (SP), R5
3631 016044 012577 163300 MOV (R5)+, 2DQRV5C
3632 016050 012777 000340 163274 MOV #340, 2DQRLVL
3633 016056 012577 163272 MOV (R5)+, 2DQTV5C
3634 016062 012777 000340 163268 MOV #340, 2DQTLVL
3635 016070 010516 MOV R5, (SP)
3636 016072 000207 RTS PC
;RESTORE TRAPCATCHER
3637 016074 013777 001352 163246 RECAT: MOV 2DQRLVL, 2DQRV5C
3638 016102 005077 163244 CLR 2DQRLVL
3639 016106 013777 001356 163240 MOV 2DQTLVL, 2DQTV5C
3640 016114 005077 163236 CLR 2DQTLVL
3641 016120 000207 RTS PC
;SET UP BUS ADDRESS AND CHARACTER COUNTS
;FOR SELECTED FUNCTION
3642 016122 011605 SETBABC: MOV (SP), R5
3643 016124 112577 163240 MOV B (R5)+, 2DQREG
3644 016130 152777 000020 163232 BIS B #BIT4, 2DQREG
3645 016136 152577 163226 BIS B (R5)+, 2DQREG
3646 016142 012577 163224 MOV (R5)+, 2DQSEC
3647 016146 142777 000040 163214 BIC B #BIT5, 2DQREG
3648 016154 105277 163210 INCB 2DQREG
3649 016160 012577 163206 MOV (R5)+, 2DQSEC
3650 016164 010516 MOV R5, (SP)
3651 016166 000207 RTS PC
  
```

3672
 3673
 3674
 3675

: TABLE OF ERROR MESSAGES

016170	042522	042503	053111	EM0:	.ASCIZ	/RECEIVER DID NOT INTERRUPT/
016223	124	042522	051516	EM1:	.ASCIZ	/TRANSMITTER DID NOT INTERRUPT/
016261	125	042516	050130	EM2:	.ASCIZ	/UNEXPECTED TRANSMITTER INTEPRUPT/
016322	047125	054105	042520	EM3:	.ASCIZ	/UNEXPECTED RECEIVER INTERRUPT/
016360	042522	042503	053111	EM4:	.ASCIZ	/RECEIVER STATUS ERROR/
016406	051124	047101	046523	EM5:	.ASCIZ	/TRANSMITTER STATUS ERROR/
016437	105	051122	051117	EM6:	.ASCIZ	/ERRJR FLAG(S) SET/
016461	102	051525	040440	EM7:	.ASCIZ	/BUS ADDRESS ERROR/
016503	103	040510	040522	EM10:	.ASCIZ	/CHARACTER COUNT ERROR/
016531	122	041505	044505	EM11:	.ASCIZ	/RECEIVED DATA ERROR/
016555	124	040522	051516	EM12:	.ASCIZ	/TRANSMITTER BUFFER DATA ERROR/
016613	103	047514	045503	EM13:	.ASCIZ	/CLOCK LOSS ERROR/

: TABLE OF DATA HEADERS

016634	042777	050130	041505	DHC:	.ASCIZ	<377>/EXPECTED	RECEIVED	REG ADDRESS/
016675	377	054105	042520	D41:	.ASCIZ	<377>/EXPECTED	RECEIVED	SEC ADR SEC REG/
				.EVEN				

3676
 3677
 3678
 3679
 3680
 3681
 3682
 3683
 3684
 3685
 3686
 3687
 3688
 3689
 3690
 3691
 3692
 3693
 3694
 3695
 3696
 3697
 3698
 3699
 3700
 3701
 3702
 3703
 3704
 3705
 3706
 3707
 3708
 3709

: TABLE OF POINTERS FOR ERROR JUTPUT

.ERRTAB:EMO
 0
 0
 EM1
 0
 0
 EM2
 0
 0
 EM3
 0
 0
 EM4
 DHC
 DHC
 EM5
 DHC
 DHC
 EM6
 DHC
 DHC
 EM7
 DHC
 DHC
 EM10
 DHC
 DHC
 EM11
 DHC
 DHC
 EM12
 DHC

3710	017044	017126			DT3
3711	017046	016613			EM13
3712	017050	016634			DHO
3713	017052	017110			DT2
3714					
3715					
3716					:DATA TABLES FOR ERROR OUTPUT
3717	017054	000003			
3718	017056	006	004		DT0:
3719	017060	001270			3
3720	017062	006	004		.BYTE 6 4
3721	017064	001266			SAVR5
3722	017056	006	004		.BYTE 6 4
3723	017070	001360			SAVR4
3724	017072	000003			DQRCR
3725	017074	006	004		DT1:
3726	017076	001270			3
3727	017100	006	004		.BYTE 6 4
3728	017102	001266			SAVR5
3729	017104	006	004		.BYTE 6 4
3730	017106	001364			SAVR4
3731	017110	000003			DQTCR
3732	017112	003	007		DT2:
3733	017114	001270			3
3734	017116	003	007		.BYTE 3 7
3735	017120	001266			SAVR5
3736	017122	006	000		.BYTE 3 7
3737	017124	001366			SAVR4
3738	017126	000004			DQERR
3739	017130	006	004		DT3:
3740	017132	001270			4
3741	017134	006	004		.BYTE 6 4
3742	017136	001266			SAVR5
3743	017140	006	004		.BYTE 6 4
3744	017142	001372			SAVR4
3745	017144	002	000		DQSEC
3746	017146	001262			.BYTE 2 0
3747	017150	000003			SAVR2
3748	017152	006	004		DT4:
3749	017154	001270			3
3750	017156	006	004		.BYTE 6 4
3751	017160	001266			SAVR5
3752	017162	006	004		.BYTE 6 4
3753	017164	001264			SAVR4
3754	017166	000000			6 4
3755	017170	000000			SAVR3
3756	017172	000000			RBUFF: 0
3757		000001			TBUFF: 0
					ZDATA: 0
					.END

K06

DZDQC MACY11 27(732) 24-SEP-76 10:14 PAGE 77
 DZDQCC.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

LSTERR	001234	1069*	1216*	3078*	3384	338E*	3472*							
MCRLF	015040	3199	3215	3307	3413	3507	3520*							
MCSRX	015261	3084	3547*											
MDATA	015556	3335	3345	3585*										
MEMCLR=	104413	1132*	1382	1416	2459	2541	2641	2720	2722	2741	2921	2896	2963	3002
		3040	3474											
MEPASS	015100	3082	3526*											
MERRPC	015405	3409	3566*											
MERRX	015306	3096	3553*											
MERR2	015125	1029	1332	3530*										
MERR3	015174	1264	3537*											
MISC. =	000012	643*												
MLOCK	015232	1288	3543*											
MNEW	015333	1257	3558*											
MPASSX	015275	3092	3551*											
MPFAIL	015042	3468	3521*											
MQM	015034	3212	3519*											
MR	015122	1306	3529*											
MSTCLR=	104412	1130*	1383	1418	1448	1471	1494	1517	1540	1568	1591	1614	1637	1660
		1683	1706	1729	1752	1775	1798	1821	1844	1873	1897	1921	1945	1971
		1997	2023	2049	2075	2101	2127	2153	2179	2206	2235	2263	2296	2326
		2356	2386	2424	2460	2542	2622	2721	2822	2897	2964	2982	3003	3019
		3041	3046	3473										
MTITLE	001000	1038*	1222											
MTSTN	015317	3405	3555*											
MTSTPC	015220	1297	3541*											
MVECX	015267	3088	3549*											
NEXT	001216	1062*	1312*	1380*	1415*	1447*	1470*	1493*	1516*	1539*	1567*	1590*	1613*	1636*
		1659*	1682*	1705*	1728*	1751*	1774*	1797*	1820*	1843*	1872*	1896*	1920*	1944*
		1970*	1996*	2022*	2048*	2074*	2100*	2126*	2152*	2178*	2205*	2234*	2262*	2295*
		2325*	2355*	2385*	2423*	2458*	2540*	2621*	2719*	2819*	2894*	2961*	3000*	3037*
		3145	3441											
NON.EX=	177320	532*	2829	2861	2904	2935								
ODDBIT=	001000	626*	1000											
OUT	014774	3488	3490	3492	3496	3508*								
PARAM =	104405	1120*	1298	3502										
PARAM1	013506	3232*	3253											
PARERR	013562	3235	3237	3239	3248*	3258	3260	3262						
PARTI	013644	3251	3271*											
PASCNT	001230	1067*	1211*	3080*	3099	3122								
PC =	%000007	581*	953*	1245*	1443*	1460*	1472*	1483*	1495*	150E*	1518*	1529*	1541*	1552*
		1569*	1580*	1592*	1603*	1615*	1626*	1638*	1649*	1661*	1672*	1684*	1695*	1707*
		1718*	1730*	1741*	1753*	1764*	1776*	1787*	1799*	1810*	1822*	1833*	1845*	1856*
		1874*	1885*	1898*	1909*	1922*	1933*	1946*	1959*	1972*	1985*	1998*	2011*	2024*
		2037*	2050*	2063*	2076*	2089*	2102*	2115*	2128*	2141*	2154*	2167*	2180*	2193*
		2207*	2224*	2236*	2264*	2297*	2327*	2357*	2387*	2425*	2439*	2463*	2464*	2467*
		2545*	2546*	2549*	2623*	2642*	2643*	2646*	2742*	2743*	2746*	2823*	2824*	2927*
		2898*	2899*	2902*	2965*	2966*	3004*	3005*	3047*	3048*	3107*	3626*	3632*	3638*
		3648*	3656*	3670*										
PFTAB	014652	3470	3476*											
POLY. =	000017	648*												
POPPO	012600	595*	3434											
PCP1SP=	005726	593*												
POP2SP=	022626	597*												
PS =	177776	587*	940*	1206*	1281*	1381*	1417*	1453*	1476*	1499*	1522*	1545*	1573*	1596*
		1619*	1642*	1665*	1688*	1711*	1734*	1757*	1780*	1903*	1826*	1849*	1879*	1903*

		1927*	1951*	1977*	2003*	2029*	2055*	2091*	2107*	2133*	2159*	2185*	2210*	2214*
		2239*	2243*	2267*	2271*	2301*	2331*	2361*	2391*	2420*	2461*	2475*	2479*	2543*
		2555*	2559*	2639*	2654*	2658*	2739*	2752*	2756*	2820*	2835*	2833*	2895*	2909*
		2912*	2962*	3001*	3029*									
		594#	3431											
		592#												
		596#												
PUSHRO=	010045													
PUSH1S=	005746													
PUSH2S=	024646													
QZX	010702	2699	2701#											
RBUFF	017166	2469	2501	2517	2518	2625	2649	2680	2696	2697	2968	3754#		
RDSW	014660	3164	3213	3250	3484#	3498*	3508*							
RECAT	016074	1460	1483	1506	1529	1552	1580	1603	1626	1649	1672	1695	1718	1741
		1764	1787	1810	1833	1856	1885	1909	1933	1959	1985	2011	2037	2063
		2089	2115	2141	2167	2193	2224	2438	3652#					
RESREG	014460	3425	3428#											
RESTAR	014575	3455	3461#											
RESTR	012772	3101	3104	3111#										
RESOS =	104407	1124#	3428											
RETURN	001214	1061#	1218*	1305*	1307	1311*	2457*	2539*	2718*	2818*	2893*	2960*	2999*	3035*
		3112*	3145*	3146	3441*	3443	3475							
RUN	001304	1092#	1315*	1318	1323*	1329*	1336*							
RUNCNT	001306	1093#	1316*	1325*	1327*									
RUNFLG	001302	1091#	1213*	1313	1317*									
RXBA.P=	000000	632#												
RXBA.S=	000004	636#												
RXWC.P=	000001	633#												
RXWC.S=	000005	637#												
RX.BCC=	000015	646#												
RO	=%000000	574#	931*	933	943*	1025*	1030*	1258*	1268*	1271*	1273*	1275	1276	2241*
		2246	2252*	2269*	2274	2278*	2300*	2308*	2310	2330*	2338*	2340	2360*	2368*
		2370	2390*	2398*	2400	2629*	2630*	2730*	2731*	3043*	3068*	3135*	3291	3296*
		3308	3322*	3326*	3336	3354*	3432*	3599*	3604*	3608*	3614*			
R1	=%000001	575#	931	932*	933	934	972*	974*	975*	976*	977	979	981*	982*
		983*	984	987*	988*	929	992*	993	996	1002*	1003*	1004*	1005*	1006*
		1008*	1009	1014*	1015	1019*	1026*	1272*	1273	1274*	1275	3103*	3107	3290
		3297*	3309	3313*	3316	3317	3318	3319	3353*					
R2	=%000002	576#	941	942*	945*	946	948*	949*	966*	967*	968	971*	979*	990*
		986*	991*	995*	998*	999*	1000*	1001	1024*	2242*	2244*	2270*	2272*	2498*
		2510*	2579*	2591*	2599*	2677*	2689*	2776*	2798*	2796*	2958*	2870*	2932*	2944*
		3045*	3289	3298*										
R3	=%000003	577#	2493*	2500*	2517*	2574*	2581*	2672*	2679*	2696*	2771*	2778*	2953*	2960*
		2927*	2934*	3044*	3185	3192*	3206*	3209	3219*	3288	3299*	3310	3323*	3324*
		3325*	3326	3335*	3336*	3341*	3344*	3352*						
R4	=%000004	578#	1398*	1399	1431*	2487*	2488*	2489	2494*	2504*	2506	2512*	2513	2519*
		2519	2568*	2569*	2570	2575*	2585*	2587	2593*	2594	2600*	2601	2633*	2634*
		2635	2666*	2667*	2668	2673*	2683*	2685	2691*	2692	2697*	2698	2734*	2735
		2765*	2766*	2767	2772*	2782*	2784	2790*	2791	2797*	2798	2847*	2849*	2849
		2854*	2864*	2866	2872*	2873	2921*	2922*	2923	2928*	2938*	2940	2946*	2947
		2978*	2979*	2986*	2987*	3015*	3016*	3023*	3024*	3062*	3063	3186	3191*	3195*
		3196*	3197	3201	3210	3217*	3224	3233*	3234	3236	3238	3240*	3241	3242
		3248	3266*	3267*	3271*	3287	3300*	3311	3320*	3323	3328*	3330*	3332*	3351*
		3391*	3392*	3393*	3394*	3395*	3396*	3397	3398	3399				
R5	=%000005	579#	1397*	1399	1430*	2484*	2489	2492*	2501*	2506	2511*	2513	2516*	2519
		2565*	2570	2573*	2582*	2587	2592*	2594	2597*	2601	2632*	2635	2663*	2669
		2671*	2680*	2685	2690*	2692	2695*	2698	2733*	2735	2762*	2767	2770*	2779*
		2784	2789*	2791	2794*	2798	2844*	2849	2852*	2861*	2866	2871*	2873	2918*
		2923	2926*	2935*	2940	2945*	2947	2980*	2985*	3017*	3022*	3052*	3053	3063

11:12	3153*	
950	1206*	1219
910	3365*	
1100*	3170*	
11:5*	3161*	

G07

ADD	1098	1252	1324	1338	1342	1345	1347	1349	1353	1355	3163	3188	3268	3315	3325
ASL	3337	3393	3396	3369	3392	3394									
EXL	3324	3245	3246												
BYL	990	994	997		1013	1231	1249	1255	1287	1295	1321	1400	1432	2247	2253
BYL	2779	2401	2413		2490	2495	2507	2514	2520	2571	2576	2598	2595	2602	2636
BYL	2774	2686	2693		2699	2736	2768	2773	2785	2792	2799	2850	2867	2874	2924
BYL	2948	2984	3021		3064	3104	3131	3155	3202	3214	3235	3243	3340	3378	3385
BYL	3416	3421	3425		3440										
BYL		1343	1394	2488	2569	2634	2667	2766	2848	2922	2979	2987	3016	3024	3324
BYL	3295	3240	3601												
BYL	980	996	3666												
BYL	1641	1664	1697		995	998	999	1000	1452	1475	1498	1521	1544	1572	1535
BYL	1926	1949	1950		1975	1733	1756	1779	1802	1925	1948	1977	1978	1901	1902
BYL	2131	2132	2157		2158	1976	2001	2002	2027	2028	2052	2054	2079	2080	2105
BYL	2232	2634	2907		2970	2193	2184	2428	2429	2472	2474	2554	2628	2651	2652
BYL	2600	3663	3664			2972	3009	3625	3631	3637					
BYL	996	1254	1286		1294	1318	2412	2993	3020	3130	3137	3154	3166	3277	3382
BYL	3439														
BYL		1262													
BYL		2855	2929	2975	3012	3057									
BYL	989	978	1010		1020	1221									
BYL	1428	2245	2273		2311	2341	2339	1241	1277	1284	1314	1319	1326	1393	1396
BYL	3014	3059	3069		3101	3138	3141	2479	2558	2627	2657	2732	2755	2838	2911
BYL	3234	3338	3243		3248	3383	3403	3165	3167	3179	3198	3207	3249	3251	3262
BYL	3244	3338	3243		3248	3383	3403	3438	3466	3489	3490	3496	3605	3615	
BYL	3169	3171	3174		3177	3194	3205	3380	3430	3492					
BYL	1032	1232	1253		1265	1291	1304	1330	1334	1455	1457	1478	1480	1501	1503
BYL	1526	1547	1549		1575	1577	1598	1600	1621	1623	1644	1646	1667	1669	1690
BYL	1713	1715	1736		1738	1759	1761	1792	1784	1805	1807	1828	1830	1851	1853
BYL	1906	1920	1954		1980	2006	2032	2058	2084	2110	2136	2162	2188	2219	2225
BYL	2065	2395	2433		2481	2561	2660	2758	2841	2914	3172	3136	3200	3209	3216
BYL	3253	3457													
BYL	1335	3329	3331												
BYL	967	970	975		981	1002	1003	1004	1005	1006	1011	1030	1211	1213	1215
BYL	1216	1258	1384		1419	1430	1453	1476	1499	1522	1545	1573	1596	1619	1643
BYL	1665	1688	1711		1757	1780	1803	1826	1849	1879	1903	1927	1951	1973	1990
BYL	2029	2055	2081		2133	2159	2185	2214	2221	2222	2242	2243	2270	2277	2303
BYL	2243	2373	2403		2475	2492	2555	2573	2573	2638	2671	2738	2752	2771	2813
BYL	2852	2908	2926		3022	3042	3078	3079	3142	3232	3464	3471	3472	3508	3613
BYL	3610	3612	3617		3619	3653	3655								
BYL	1210	2624	3142		3344	3387	3598	3606	3607	3616					
BYL	933	950	968		977	1009	1230	1233	1240	1261	1275	1276	1399	3489	3526
BYL	2513	2570	2587		2594	2601	2635	2668	2695	2692	2698	2735	2767	3489	3531
BYL	2798	2849	2873		2922	2940	2947	3062	3140	3257	3259	3384	3489		
BYL	3197	3201	3234		3238	3242	3248	3495							
BYL	2278	2308	2338		2368	2398	3498								
BYL	1317														
BYL	1019	1325	1391	1395	1427	2477	2557	2630	2656	2731	2754	2837	2910	2976	3013
BYL	3258	3268	3100	3206	3333	3347	3604	3614							

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DZDQCC.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

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	2216	2303	2304	2333	2334	2363	2364	2393	2394	2431	2436	2440	2563	2760	2916
	3108	3109	3110												
RESET	3105														
RETURN	1301														
ROL	1017	1323	1336												
ROR	939	3323	3330	3332											
RTI	952	1034	2251	2255	2281	2283	2307	2337	2367	2397	3147	3157	3181	3219	3273
	3292	3302	3355	3444	3509	3593	3620								
RTS	952	3626	3632	3639	3648	3656	3670								
SUB	3366	3390													
TRAP	1110	1112	1114	1116	1118	1120	1122	1124	1126	1128	1130	1132	1134	1136	
TST	941	946	984	989	1001	1012	1239	1283	1320	2246	2274	2310	2340	2370	2400
TSTB	3164	3213	3250	3402	3415	3420	3424	3429	3487						
	1220	1243	1313	2974	3011	3056	3133	3168	3170	3173	3176	3193	3204	3339	3379
	3400	3491													
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	1175	1176	1177	1178	1179	1180	1181	1182	1183	1184	1185	1186	1187	1188	1189
	1190	1191	1192	1193	1194	1195	1196	1197							
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	3115	3118	3121	3124	3446	3449	3477	3511	3511	3573	3575	3719	3720	3722	3725
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.ENABL	533	551													
.END	3757														
.ENDC	1313	1381	1416	1448	1455	1459	1471	1478	1492	1494	1501	1505	1517	1524	1528
	1540	1547	1551	1568	1575	1579	1591	1598	1612	1614	1621	1625	1637	1644	1648
	1660	1667	1671	1683	1690	1694	1706	1713	1717	1729	1736	1740	1752	1759	1763
	1775	1782	1786	1798	1805	1809	1821	1828	1832	1844	1851	1855	1873	1882	1884
	1897	1906	1908	1921	1930	1932	1945	1956	1958	1971	1982	1984	1997	2003	2010
	2023	2034	2036	2049	2060	2062	2075	2086	2088	2101	2112	2114	2127	2138	2140
	2153	2164	2166	2179	2190	2192	2206	2235	2263	2296	2313	2326	2343	2356	2373
	2396	2401	2403	2424	2435	2437	2459	2522	2541	2604	2622	2701	2720	2801	2820
	2876	2895	2950	2962	2990	3001	3027	3038							
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.IF	1312	1380	1415	1447	1455	1470	1478	1493	1501	1516	1524	1539	1547	1567	1575
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	1906	1908	1920	1929	1930	1932	1944	1953	1957	1970	1979	1982	1996	2005	2008
	2022	2031	2034	2048	2057	2060	2074	2083	2086	2100	2109	2112	2126	2135	2139
	2137	2161	2164	2178	2187	2190	2205	2224	2262	2295	2311	2313	2325	2341	2343
	2357	2371	2373	2385	2386	2401	2423	2432	2435	2452	2458	2534	2540	2616	2621
	2713	2719	2814	2819	2889	2894	2961	2971	3000	3010	3037				
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	1636	1637	1644	1659	1660	1667	1682	1683	1690	1705	1706	1713	1729	1729	1736
	1751	1752	1759	1774	1775	1782	1797	1798	1805	1820	1821	1829	1843	1844	1851
	1872	1873	1882	1884	1896	1897	1906	1908	1920	1921	1930	1932	1944	1945	1953
	1958	1970	1971	1979	1984	1996	1997	2005	2010	2022	2023	2031	2036	2048	2049

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DZDQCC.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

.WORD 921 3494

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

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RUN-TIME RATIO: 140/78=1.7
CCRE USED: 24K (47 PAGES)

