DP11

SYNCHRONOUS INTERFACE

MD-11-DZDPA-B

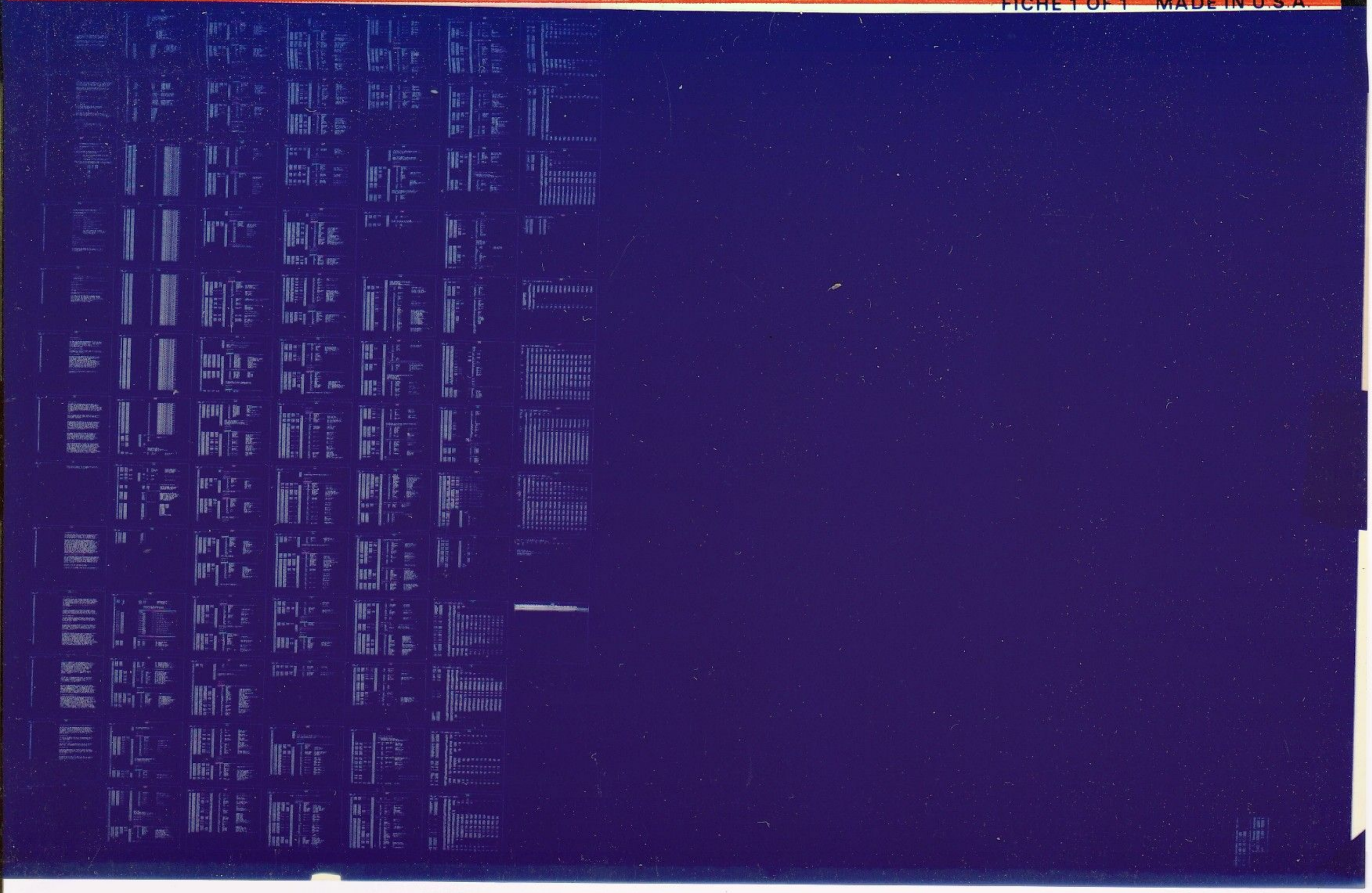
EP-DZDPA-B-DL-A

NOV 1976

digital

FICHE 1 OF 1

MADE IN U.S.A.



.MACRO HELLO

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZDPA-B

PRODUCT NAME: DP11A SYNCHRONOUS LINE UNIT

DATE: APRIL.1976

MAINTAINER: DIAGNOSTIC GROUP

1. ABSTRACT

THIS MAINDEC CONSISTS OF TWO PROGRAMS. FIRSTLY, A DP11A EXERCISER WHICH IS RUN WITH A TEST CONNECTOR (DB25S) IN PLACE OF THE MODEM. THE FUNCTION OF THIS TEST IS TO CHECK OUT THE CABLE (BC01R-25) AND FUNCTIONAL INTERFACE WITH THE MODEM. THIS TEST IS RUN UNDER A SIMULATED (SOFTWARE) CLOCK THAT RUNS AT APPROXIMATELY 54KHZ.

SECONDLY, THERE IS THE PRINCIPLE DIAGNOSTIC FOR THE DP11. THIS PROGRAM RUNS IN THE MAINTENANCE MODE WITH THE BC01R-25 CABLE REMOVED FROM THE SYSTEM UNIT. THIS TEST PROVIDES COMPLETE DIAGNOSTICS FOR THE DP11-DA AND DP11-DA.

2. REQUIREMENTS

2.1 EQUIPMENT

ANY PDP11 FAMILY CPU
DB25S TEST CONNECTOR (IF CABLE TEST IS TO BE RUN)
DP11-DA
DP11-CA (OPTIONAL)

2.2 STORAGE

THIS PROGRAM USES MEMORY TO LOCATION 17500

3. LOADING PROCEDURE

THE PROGRAM MAY BE LOADED LIKE ANY OTHER PROGRAM
SUCH AS: PAPER TAPE,DECTAPE,MAGTAPE,CASSETT,DISK,ETC.
MOST COMMON WILL BE PAPER TAPE LOADING THROUGH
THE USE OF ABSOLUTE LOADER.

3.1 DF11-L TESTING

THIS PROGRAM WILL EXERCISE THE DF11-L.
METHOD: CABLE MUST BE INSERTED INTO DP11,TEST CONNECTOR ON END OF CABLE. SA=210, SET SW00=1,HIT START AND CONT. AS PER 4.3.1.
NOTE: IN THIS TEST AN ERROR WILL CAUSE PRG TO START AT BEGGINING OF TEST

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

SWITCH 7 — SET INDICATES SINGLE DP11 MODE
CLEAR INDICATES CYCLE MODE (MORE THAN ONE)

SWITCH 8 — SET SELECTS THE DP11-CA OPTION FOR TEST

4.2 STARTING ADDRESSES

200 = START ADDRESS FOR MAINTENANCE MODE DIAGNOSTICS (CABLE MUST BE PULLED FROM THE SYSTEM UNIT)

210 = START ADDRESS FOR BC01R-25 CABLE TEST (DB25S TEST CONNECTOR MUST BE PLUGED IN)

4.3 OPERATOR ACTION

4.3.1 IF SWITCH 7 WAS LEFT UP THE PROGRAM WILL HALT WITH THE SWITCH REG IN IN THE DATA LIGHTS. (EXCLUDING 11/05 AND 11/10 CPU) AND REQUIRE THE FOLLOWING OPERATOR ACTION:

A) SW0-SW8 MUST BE SET TO THE VECTOR ADDRESS OF THE FIRST DP11. NOTE FIRST DP11 VECTOR; NOT THE LINE SELECTED UNLESS IT IS LINE 0

B) SW9-SW15 MUST BE SET TO THE OCTAL LINE NUMBER OF THE DP11 TO BE TESTED. E.G. THE FIRST DP11 IS LINE 0.

PRESS CONTINUE. SR IS IN DATA LIGHTS(EXCLUDING 11/05,11/10) RESET SWITCH AS PER 5.1.1"SWITCH SETTINGS". PRESS CONTINUE. THIS STARTS PROGRAM. ALL DP11 ADDRESSES SHALL BE ASSIGNED FROM 774777 TO 774400 CONTIGUOUSLY

I.E.	1ST DP11	774776	XMIT	BUFFER
		774774	XMIT	STATUS
		774773	SYNC	BUFFER
		774772	RCV	BUFFER
		774770	RCV	STATUS
	2ND	774756		
		774764		
		774762		
		774760		
	32ND	774406		
		774404		
		774402		
		774400		

E01

4.3.2 FOR CABLE TEST REMOVE BC01R-25 CABLE FROM MODEM AND PLUG THE DB25S TEST CONNECTOR SOCKET INTO THE CABLE.

4.3.3 FOR THE MAINTENANCE MODE TEST THE CABLE MUST BE REMOVED FROM THE DEVICE SYSTEM UNIT.

5. OPERATING PROCEDURE

5.1.1 SWITCH SETTINGS (APPLICABLE TO BOTH TESTS)

SW15 = 1 OR UP ... HALT ON ERROR

SW14 = 1 OR UP ... SCOPE LOOP FOR WHOLE CURRENT TEST

SW13 = 1 OR UP ... INHIBIT ERROR PRINTOUT

SW12 = 1 OR UP ... INHIBIT ALL PRINTOUT, BELL ON ERROR.

SW11 = 1 OR UP ... INHIBIT ITERATION

SW10 = 1 OR UP ... ESCAPE TO NEXT TEST ON ERROR

SW08 = 1 OR UP ... GO TO TOP OF CURRENT TEST ON ERROR.
NOTE: THIS SWITCH IS VERY IMPORTANT FOR DATA ERRORS IN WHICH THE DP11 CLOCK IS RUNNING. THIS SWITCH MUST BE SET TO A 1 TO STOP AN AVALANCH OF ERRORS.....

6. ERRORS

6.1 ERROR PRINTOUT

PRINTS ALL ERRORS UNLESS INHIBITED BY SWITCH 13 OR SWITCH 12.

ERROR PRINT OUT WILL LOOK LIKE:

TEST NO. XXX LINE NO. XX
PC: XXXXXX

DEPENDING ON THE ERROR AN ADDITIONAL MESSAGE MAY BE TYPED OUT.

6.1.1 AS STATED ABOVE FOR ERRORS THAT ARE CAUSED BY A COMPARISON SUCH AS DATA COMPARISON,REGISTER COMPARISON,ETC. AND INTERUPT ERRORS. THERE WILL BE ADDITIONAL INFORMATION IN THE ERROR REPORT.

6.2 ERROR RECOVERY

A. IF IN A SCOPE LOOP, SET SWITCH 14.

B. TO RECOVER FROM HALT ON ERROR, MAKE SURE SW14 IS SET THEN DEPRESS CONTINUE.

C. IT MAY BE DESIRABLE TO SET SW 13 OR SW 12 IN AN ERROR CONDITION.

7. RESTRICTIONS

7.1 STARTING RESTRICTIONS

SEE 4.1 AND 4.3.1

7.2 OPERATING RESTRICTIONS

7.2.1 CABLE TEST (SA=210) MUST BE RUN WITH DB25S CONNECTOR IN PLACE OF A MODEM.

7.2.2 MAINTENANCE MODE DIAGNOSTIC MUST BE RUN WITH CABLE REMOVED FROM SYSTEM UNIT.

7.2.3 CYCLE MODE. IF SW 07=0 WHEN START IS PRESSED; PROGRAM WILL RUN SELECTED TEST (CABLE OR MAINTENANCE) ASSUMING THAT ALL DP11S IN THE SYSTEM ARE TO BE TESTED. PROGRAM STARTS WITH LINE 0 THEN SENSES FOR NEXT LINE; IF IT EXISTS IT WILL BE TESTED. THIS GOES ON UNTILL A NON-EXISTANT LINE IS FOUND THEN THE PROGRAM STARTS WITH LINE 0 AGAIN.
BASCSR AND BASVEC ARE DEFAULT VALUES. IF YOUR VALUES ARE DIFFERENT PATCH YOUR VALUES IN THERE.

8. MISCELLANEOUS

9. PROGRAM DESCRIPTION

9.1 INITIALIZATION ROUTINES

THE START CODE FOR BOTH THE MAINTENANCE MODE AND THE CABLE TEST INITIALIZES THE PROCESSOR PRIORITY TO LEVEL SEVEN AND SETS THE STACK POINTER TO ADDRESS 1100. CONSOL SWITCH SEVEN IS THEN EXAMINED TO DETERMINE IF THIS IS CYCLE MODE OR SINGLE LINE IS TEST. IF SWITCH SEVEN IS UP TWO SUBROUTINES (CLRVEC,LINE.N) ARE EXECUTED BEFORE THE TEST SECTION IS ENTERED.

9.1.1 CLRVEC, CLEAR-VECTOR-AREA

THE SUBROUTINE "CLEAR-VECTOR-AREA" LOADS THE COMMUNICATION VECTOR AREA WITH .+2,HALT. THIS CAUSES ANY ILLEGAL INTERRUPTS TO TRAP TO THERE STATUS WORD.

9.1.2 LINE.N, LINE NUMBER

THE FUNCTION OF THIS SUBROUTINE IS TO SAVE SWITCH EIGHT OF THE CONSOL (SW8 SELECTS DP11-CA OPTION) AND WAIT FOR OPERATOR ACTION TO SPECIFY THE LINE NUMBER AND FIRST DP11 VECTOR ADDRESS. WHEN THE PROGRAM HALTS;
SWITCHES SW0 THRU SW8 MUST BE SET TO THE VECTOR ADDRESS OF THE FIRST DP11 AND SWITCHES SW9 THRU SW15 MUST BE SET TO THE OCTAL EQUIVILANT OF THE LINE NUMBER (E.G. THE FIRST LINE IS LINE 0(8) THE TENTH LINE IS LINE 11(8)). FOLLOWING THIS ACTION "CONTINUE" ENTERS THE PROGRAM INTO THE SELECTED TEST SECTION. IF SWITCH SEVEN IS NOT UP WHEN "START" IS DEPRESSED THE PROGRAM ASSUMES CYCLE MODE AND WILL START RUNNING WITH LINE 0 THRU ALL LINES. BASCSR AND BASVEC ARE USED AS DEFALT CONDITIONS.

9.2 MAINTENANCE MODE TESTS

IN AN EFFORT TO OPTIMIZE CORE UTILIZATION MANY OF THE DIAGONOSTIC TEST WERE WRITTEN IN SUBRCUTINE FORMAT VERSUS MACROS.

9.2.1 BITST, BIT TEST

THIS SUBROUTINE IS ENTERED WITH A JSR R5, BITST. IM-
MEDIATELY FOLLOWING THIS INSTRUCTION IS THE BIT SELECTED
FOR TEST. THE BIT NUMBER IS FETCHED BY THE SUBROUTINE
AND STORED IN LOCATION "BITS". USING A SEQUENCE OF "BIS" "BIT"
AND "BIC" INSTRUCTIONS EACH READ/WRITE BIT OF THE TRANSMITTER
AND RECEIVER CSR (TCSR,RCSR) IS TESTED TO VERIFY THAT AT LEAST
THAT PARTICULAR BIT CAN BE REFERENCED AND IS IN FACT READ/WRITE.
NO ATTEMPT IS MADE AT THIS POINT TO CHECK FOR ILLEGITIMATE
INTERACTION.

9.2.2 RESET TEST

THIS IS A SIMPLE TEST THAT MERELY WRITES INTO ALL WRITEABLE
BITS OF THE TCSR AND RCSR, CHECKS THAT THEY WERE SET,
ISSUES "RESET" AND CHECKS THAT ALL BITS THAT ARE SUPPOSED TO
BE CLEARED BY RESET-WERE.

9.2.3 VALID

THE FUNCTION OF THIS SUBROUTINE IS TO TEST FOR INTERACTION
BETWEEN READ/WRITE BITS OF THE TCSR AND RCSR. THIS ROUTINE
IS ENTERED WITH A JSR REGISTER FIVE, FOLLOWED BY THE BIT
NUMBER. THE SELECTED BIT IS SET AND THEN THE ENTIRE CSR
IS COMPARED WITH THE WORD (BITS) USED TO SET THE SELECTED
BIT. IF ANY OTHER BIT IS SET AN ERROR IS REPORTED. LOCATION
"REG" CONTAINS THE ADDRESS OF THE CSR SELECTED FOR TEST.
AN EXAMINATION OF THIS CSR SHOULD REVEAL A BIT SET OTHER
THAN THE ONE IN LOCATION "BITS".

9.2.4 CLEAR

THIS SUBROUTINE IS ENTERED THE SAME WAY AS BITST, AND VALID
ARE ENTERED. ITS FUNCTION IS TO TEST FOR INTERACTION
BETWEEN ANY CSR BITS DURING A BIT CLEAR INSTRUCTION.
THIS IS ACCOMPLISHED BY SETTING ALL READ/WRITE BITS
OF THE SELECTED CSR AND MAKING A DUPLICATE BIT MAP IN
TMPDAT. THEN "BITS" IS USED TO CLEAR A SINGLE BIT IN THE
CSR AND TMPDAT. FOLLOWING THIS THE CSR IS COMPARED WITH
TMPDAT TO VERIFY THAT ONLY THAT BIT WAS CLEARED.

9.2.5 PRIORITY TESTS

WITH THE PROCESSOR PRIORITY AT LEVEL FIVE "STATUS-INTERRUPT-
ENABLE" (SIE) IS SET AND ALL THE BITS THAT SHOULD CAUSE A
STATUS INTERRUPT ARE SET INDIVIDUALLY AND COLLECTIVELY SET.
SECONDLY SIE IS REMOVED AND THE PROCESSOR PRIORITY IS LOWERED
TO FOUR. AGAIN THE CSR BITS THAT CAUSE "STATUS INTERRUPTS"
ARE SET AND RESET. FINALLY THE SIE BIT IS SET WHILE THE
PROCESSOR PRIORITY IS AT FOUR AND IT IS VERIFIED THAT
EACH DISCRETE EVENT THAT SHOULD CAUSE A STATUS INTERRUPT
DOES. THIS SEQUENCE TESTS THAT THE DP11 STATUS BITS INTERRUPT
AT THE PROPER PROCESSOR PRIORITY. THE NEXT SEQUENCE OF PRIORITY
TESTS VERIFY THE TRANSMITTER INTERRUPTS BY LOADING THE

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   333                                          TRANSMIT BUFFER, ENABLING THE MAINTENANCE MODE CLOCK AND
   334                                          WAITING FOR AN INTERRUPT.  IF NO INTERRUPT IS RECEIVED WITHIN
   335                                          10 CHARACTER TIMES AN ERROR IS REPORTED.
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9.2.6 SYNCHRONIZATION TESTS

THE FIRST SYNC TEST (TEST 24) VERIFIES THE READ/WRITE CAPABILITY OF THE SYNC REGISTER 174XX3 AND THE SYNC EXTENSION 174XX7 WHEN THE DP11-CA OPTION EXISTS. THIS IS ACCOMPLISHED BY WRITING AND READING ALL POSSIBLE SYNC CHARACTERS (0 THRU 377(8) FOR THE SYNC REG AND 0 THRU 17(8) FOR THE SYNC EXTENSION).

THE NEXT SYNC TEST ISSUES TWO OF EVERY POSSIBLE SYNC CHARACTER IN EACH OF THE AVAILABLE CHARACTER LENGTH AND CHECKS THAT TWO OF EACH SYNC RAISES "RECEIVER ACTIVE". THEN THE THIRD SYNC IS TRANSMITTED AS DATA. THIS CHECKS THE CAPABILITY OF THE RECEIVER TO INTERRUPT AND ALSO CHECKS THE RECEIVER BUFFER FOR DATA RECEPTION ACCURACY. THIS TEST IS FIRST RUN BY LOADING THE TRANSMIT BUFFER UNDER SOFTWARE CONTROL THEN IS REPEATED IN THE IDLE MODE. THIS CHECKS THAT EACH AND EVERY POSSIBLE SYNC CHARACTER CAN BE TRANSMITTED IN THE IDLE MODE IN THE EVENT THAT AN ERROR IS DETECTED IN THE LAST TWO SYNC TEST AND THE "HALT-ON-ERROR" SWITCH IS UP A SCOPE LOOP MAY BE RUN. THIS IS ACCOMPLISHED BY REMOVING "HALT-ON-ERROR" SW15, SETTING "SCOPE", INHIBIT PRINT,SET SW09, AND PRESSING CONTINUE. THIS CAUSES INCREMENT INSTRUCTION TO BE SKIPPED AND THEREFORE LOOP ON THE SAME SYNC CHARACTER.

9.2.7 INTERRUPT DRIVEN SEQUENTIAL DATA TEST

SYNC IS ESTABLISHED THROUGH THE TRANSMISSION TWO SYNC CHARACTERS. ONCE SYNC IS ESTABLISHED A BINARY COUNT PATTERN IS TRANSMITTED THE SIZE OF WHICH IS DETERMINED BY THE MAXIMUM CHARACTER SELECTED FOR TEST (8 BITS/CHARACTER OR 12/8 BITS/CHARACTER IF THE CA OPTION EXISTS). AT THE COMPLETION OF THE BINARY COUNT PATTERN "ACTIVE" IS DROPPED AND THE NEXT SHORTEST CHARACTER LENGTH IS SELECTED. THIS TEST IS REPEATED FOR THREE CHARACTER LENGTHES (12,11,10,OR 8,7,6).

FUNCTIONALLY THIS TEST VERIFIES THE CAPABLIITY OF THE DP11 TO MAINTAIN SYNC OVER A LONG CHARACTER STRING.

IN THE EVENT THAT AN ERROR IS DETECTED AND "HALT-ON-ERROR" IS UP REMOVE IT, SET "INHIBIT PRINT" AND "SCOPE" AND PRESS CONTINUE.

9.2.8 RANDOM DATA, RANDOM STALL

THIS INTERRUPT DRIVEN TEST TRANSMITS RANDOM DATA FOR A PERIOD OF TIME (0 TO 0.65 SECONDS, 0 TO 260 CHARACTERS) DETERMINED BY A RANDOM GENERATOR. AT THE EXPIRATION OF THE DATA TIME INTERVAL THE "IDLE" MODE IS ENTERED AND SYNC CHARACTERS ARE TRANSMITTED FOR A RANDOM PERIOD OF TIME. WHEN THE IDLE TIME TERMINATES THE DATA MODE IS RESTARTED AND NEW DATA IS TRANSMITTED FOR A NEW TIME INTERVAL.
THIS VERIFIES THAT THE DP11 CAN SWITCH BETWEEN DATA MODE AND IDLE AT RANDOM.

9.2.9 PARITY TEST

THE PARITY TEST CONSISTS OF A TRANSMITTER INTERRUPT SERVICE ROUTINE THAT TRANSMITS A BINARY COUNT PATTERN AND A RECEIVER INTERRUPT SERVICE ROUTINE THAT CALCULATES THE PARITY ON THE EXPECTED DATA, COMPARES THE RECEIVED DATA WITH THE EXPECTED DATA, AND FINALLY TESTS THE PARITY BIT (BIT 12=0 FOR EVEN, 1 FOR ODD).

9.2.10 RECEIVER OVERRUN TEST

THIS TEST TRANSMITS TWO SYNC CHARACTERS TO RAISE "ACTIVE" FOLLOWED BY TWO DATA CHARACTERS. RECEIVER INTERRUPT ENABLE IS NOT SET THEREFORE "RECEIVER OVERRUN" SHOULD SET AND CAUSE A TRANSMITTER STATUS INTERRUPT. THIS SEQUENCE IS REPEATED FOR A FULL BINARY COUNT. (000-377)

9.2.11 HALF DUPLEX TEST

THE HALF DUPLEX BIT SHOULD PREVENT ANY DATA FROM ENTERING THE RECEIVER WHILE SEND-REQUEST IS UP. TO VERIFY THIS RECEIVER INTERRUPT ENABLE IS SET WHILE THE TRANSMITTER IDLES FOR APPROXIMATELY 30MS. FOR EACH POSSIBLE CHARACTER AVAILABLE IN THE 8 BIT/CHAR SET. ANY DATA ENTRY INTO THE RECEIVER WILL CAUSE A TRAP TO AN ERROR ROUTINE.

9.3 CABLE TEST

THE CABLE TEST REQUIRES THE LEAST AMOUNT OF EFFORT AND THEREFORE CAN BE RUN AS A QUICK CONFIDENCE CHECK. THE OPERATING PROCEDURE IS TO DISCOUNT THE BC01R-25 CABLE FROM THE MODEM AND PLUG IT INTO THE DB25S TEST CONNECTOR. FROM THIS POINT ON THE OPERATING PROCEEDURE IS THE SAME AS THE MAINTENANCE MODE DIAGNOSTIC. THE PRINCIPLE DIFFERENCE BETWEEN THE CABLE TEST AND THE MAINTENANCE MODE TEST IS THE CLOCK. THE MAINTENANCE MODE TEST RUNS OFF OF A FREE RUNNING 3KHZ MULTIVIBRATOR WHERE AS THE CABLE TEST OPERATES OFF A SOFTWARE CLOCK. SETTING BIT 3 OF THE TRANSMITTER STATUS RAISES THE CLOCK, CLEARING IT LOWERS THE CLOCK. THE SOFTWARE CLOCK THEREFORE HAS A FREQUENCY RANGE OF ZERO TO 56KHZ. THIS ENABLES THE PROGRAM TO STEP THROUGH THE TRANSMIT-RECEIVE SEQUENCE ONE BIT AT A TIME.
IT ALSO VERIFIES THE 10KHZ CABLE SPEC AND 50 KHZ LOGIC SPEC.

9.3.2 CLOCK

CLOCK IS THE SUBROUTINE TO RUN THE SOFTWARE CLOCK. IT IS ENTERED BY A TRAP CALL, CLOCK FOLLOWED BY THE NUMBER OF CYCLES DESIRED. UPON ENTRY THE SUBROUTINE FETCHES THE CYCLE COUNT AND EXAMINE BIT8 OF SAVSR1 TO DETERMINE IF 8 BITS/CHAR OR 12 BITS/CHAR HAVE BEEN SELECTED FOR TEST. IF THE 12 BIT MODE HAS BEEN SELECTED 4 IS ADDED TO THE CLOCK COUNT AND BIT 10 OF THE RECEIVER STATUS IS SET BEFORE EXECUTING THE CLOCKING INSTRUCTIONS. BY CHANGING LOCATION "FREQ" IT IS POSSIBLE TO SLOW DOWN THE CLOCK. WITH FREQ 1 THE SOFTWARE CLOCK RUNS AT APPROXIMATELY 25 KHZ. THIS ENABLES THE OPERATOR TO SLOW THE CLOCK DOWN TO ALMOST ZERO CPS. THIS CAN BE USEFULL IN DETERMING IF A BUG IF FREQUENCY DEPENDENT.

9.3.3 RXCLK

THIS TRAP CALL IS ANOTHER SOFTWARE CLOCK. IT WAS WRITTEN FOR CODE THAT IS INDEPENDENT OF 12/8 BITS PER CHARACTER OPTION. RXCLK N EXECUTES N SOFRWARE CYCLES. RXCLK ALSO HAS "FREQ" EMBEDDED WITHIN ITS DEFINITION. SINCE IT IS A TRAP CALL THE DELAY INSTRUCTIONS CAN BE CHANGED BY CHANGING THE CONTENTS OF "FREQ".

9.3.4 REE

REE IS A UTILITY SUBROUTINE TO REINITIALIZE THE DP11 STATUS REGISTER, INTERRUPT VECTOR AND SELECT THE 12/8 BITS PER CHARACTER MODE. THE ENTRY REGISTER IS R5. THE ADDRESS TO WHICH THIS SUBROUTINE RETURNS IS A FUNCTION OF THE NUMBER OF BITS PER CHARACTER SELECTED FOR TEST. IF 8 BITS PER CHARACTER IS SELECTED THE SUBROUTINE RETURNS TO AN INSTRUCTION THAT SETS UP THE DATA LIMIT FOR THAT MODE. IF THE TWELVE BIT PER CHARACTER MODE IS SELECTED THE CONTENTS OF REGISTER 5 IS MODIFIED AND SUBROUTINE RETURNS TO THE INSTRUCTION THAT SETS UP THE TWELVE BIT LIMIT.

9.3.5 SYNCHRONIZATION CHARACTER TESTS

FOLLOWING STATUS REGISTER AND VECTOR INITIALIZATION THE CLOCK IS RUN FOR 30 CYCLES TO CLEAR OUT ANY PREVIOUS DATA THAT MAY BE RESIDING IN THE TRANSMIT OR RECEIVE BUFFERS. AT THIS POINT THE "TRANSMITTER DONE" AND "TRANSMITTER INTERRUPT ENABLE" ARE SET CAUSING AN INTERRUPT TO A SYNCHRONIZATION SUBROUTINE, TV18. TV18 LOADS THE TRANSMIT BUFFER WITH A SYNC CHARACTER. UPON RETURN FROM THE INTERRUPT SERVICE ROUTINE THE SOFTWARE CLOCK RUNS FOR 3 CYCLES. THIS SHOULD BR SUFFICIENT TO RAISE "SEND REQUEST"; IF NOT AN ERROR IS REPORTED. THE SOFTWARE CLOCK THEN GENERATOR ENOUGH CYCLES TO TRANSMIT EXACTLY ONE CHARACTER AND EXAMINES "RECEIVE ACTIVE". IF "RECEIVER ACTIVE" IS UP THE RECEIVER IS PREMATURELY ACTIVE AND AN ERROR IS REPORTED. THE NEXT SET OF CYCLES GENERATED IS ONE SHORT OF THE NUMBER REQUIRED TO TRANSMIT A FULL CHARACTER.

AGAIN "RECEIVER ACTIVE" IS TESTED FOR A PREMATURE RESPONSE.

ONE MORE CYCLE IS THEN GENERATED AND "ACTIVE" SHOULD BE UP. TO VERIFY THAT IT WAS THE TRANSMITTED DATA THAT RAISED "ACTIVE" AND NOT NOISE A THIRD SYNC IS TRANSMITTED AND CHECKED AS DATA. THE SEQUENCE IS CONTINUED FOR COMPLETE SET OF POSSIBLE SYNC CHARACTERS (1 TO LIMIT), IN EACH OF THE THREE AVAILABLE CHARACTER LENGTHS. THIS SET OF TESTS ALSO HAS THE SCOPE LOOP FACILITY WHERE THE SAME SYNC CHARACTER IS NOT CHANGED IF THE SCOPE SWITCH SW14 IS UP.

9.3.6 SEQUENTIAL DATA

THIS TEST IS THE SAME AS THAT RUN IN THE MAINTENANCE MODE TEST. IT'S PRINCIPLE OBJECTIVE IS TO VERIFY THE 50KHZ SPEC OF THE DP11. THE SOFTWARE CLOCK THAT DRIVES THIS TEST OPERATES AT APPROXIMATELY 56KHZ.

9.3.7 RANDOM DATA, RANDOM IDLE

THIS TEST IS SIMILAR TO THE RANDOM DATA TEST RUN IN THE MAINTENANCE MODE. THE DIFFERENCE IS THAT IN GOING FROM "IDLE" TO "DATA", "ACTIVE" IS DROPPED AND THE RECEIVER RESYNCED.

9.3.8 SEND-REQUEST TEST

IN THIS TEST "SEND REQUEST" IS RAISED BY LOADING THE TRANSMIT BUFFER AND GENERATING 3 CYCLES. IF THE CABLE IS WIRED PROPERLY "SEND REQUEST" SHOULD RAISE "CLEAR-TO -SEND" AND "MODEM READY" (DATA SET READY). THIS TEST IS REPEATED IN THE 8, 7, AND 6 BITS PER CHARACTER MODE.

9.3.9 TERMINAL READY

THE FUNCTION OF THIS TEST IS TO VERIFY THAT WITH THE DB25S TEST CONNECTOR IN PLACE, SETTING "TERMINAL READY" RAISES "CARRIER" AND "RING FLAG". THIS TEST ALSO VERIFIES "RING FLAG" AND "CARRIER DOWN FLAG" INTERRUPT.

.ENDM HELLO

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                                        ;DP11A SYNCHRONOUS MODEM INTERFACE DIAGNOSTIC
                                        ;******MAINTENANCE MODE******
                                        ;COPYRIGHT, DIGITAL EQUIPMENT CORPORATION******
                                        ;MAYNARD, MASSACHUSETTS  01754
                                        ;PROGRAMMER: JOHN FRIEDRICH
                                        ;REVISED BY: JOHN EGOLF



                                        ;MAINDEC-11-DZDPA-B

                                        ;DP11
                                        ;COPYRIGHT JUNE 1973,1976, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754

                                                ;STARTING PROCEDURE
                                                ;LOAD PROGRAM
                                                ;LOAD ADDRESS 000200
                                                ;PRESS START
                                                ;THIS IS FOR THE STATIC TEST
                                                ;LOAD ADDRESS 000210
                                                ;PRESS START
                                                ;THIS IS FOR CABLE TEST
                                                ;FOR MORE INFORMATION SEE THE
                                                ;DOCUMENTATION IN FRONT OF THE LISTING



                                        ;SWITCH REGISTER OPTIONS

                                        SW15=100000             ;=1,HALT ON ERROR
                                        SW14=40000              ;=1,LOOP ON CURRENT TEST
                                        SW13=20000              ;=1,INHIBIT ERROR TYPEOUT
                                        SW12=10000              ;=1,DELETE TYPEOUT,BELL ON ERROR.
                                        SW11=4000               ;=1,INHIBIT ITERATIONS
                                        SW10=2000               ;=1,ESCAPE TO NEXT TEST ON ERROR
                                        SW09=1000               ;=1,LOOP WITH CURRENT DATA
                                        SW08=400                ;=1,LOOP ON ERROR
                                        SW07=200                ;=1,SINGLE SELECTED DP11. =0 CYCLE ALL DP11S
                                        SW06=100
                                        SW05=40
                                        SW04=20
                                        SW03=10
                                        SW02=4
                                        SW01=2
                                        SW00=1
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                                        ;REGISTER DEFINITIONS

000000                                  R0=%0           ;GENERAL REGISTER
000001                                  R1=%1           ;GENERAL REGISTER
000002                                  R2=%2           ;GENERAL REGISTER
000003                                  R3=%3           ;GENERAL REGISTER
000004                                  R4=%4           ;GENERAL REGISTER
000005                                  R5=%5           ;GENERAL REGISTER
000006                                  SP=%6           ;PROCESSOR STACK POINTER
000007                                  PC=%7           ;PROGRAM COUNTER

                                        ;LOCATION EQUIVALENCIES

177570                                  SWR=177570      ;CONSOLE SWITCH REGISTER
177570                                  LIGHTS=177570   ;PDP-11/45 DISPLAY REGISTER
177776                                  PS=177776       ;PROCESSOR STATUS WORD
001050                                  STACK=1050      ;START OF PROCESSOR STACK

                                        ;INSTRUCTION DEFINITIONS

005746                                  PUSH1SP=5746    ;DECREMENT PROCESSOR STACK 1 WORD
005726                                  POP1SP=5726     ;INCREMENT PROCESSOR STACK 1 WORD
010046                                  PUSHR0=10046    ;SAVE R0 ON STACK
012600                                  POPR0=12600     ;RESTORE R0 FROM STACK
024646                                  PUSH.SP=24646   ;DECREMENT STACK TWICE
022626                                  POP.SP=22626    ;INCREMENT STACK TWICE
                                        .EQUIV  EMT,HLT ;BASIC DEFINITION OF ERROR CALL


100000                                  BIT15=100000
040000                                  BIT14=40000
020000                                  BIT13=20000
010000                                  BIT12=10000
004000                                  BIT11=4000
002000                                  BIT10=2000
001000                                  BIT9=1000
000400                                  BIT8=400
000200                                  BIT7=200
000100                                  BIT6=100
000040                                  BIT5=40
000020                                  BIT4=20
000010                                  BIT3=10
000004                                  BIT2=4
000002                                  BIT1=2
000001                                  BIT0=1
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                                                ;TRAPCATCHER FOR ILLEGAL INTERRUPTS
                        000000          .=0
000000  000002          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000002  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000004  000006          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000006  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000010  000012          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000012  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000014  000016          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000016  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000020  000022          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000022  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000024  000026          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000026  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000030  000032          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000032  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000034  000036          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000036  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000040  000042          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000042  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000044  000046          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000046  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000050  000052          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000052  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000054  000056          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000056  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000060  000062          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000062  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000064  000066          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000066  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000070  000072          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000072  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000074  000076          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000076  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000100  000102          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000102  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000104  000106          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000106  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000110  000112          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000112  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000114  000116          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000116  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000120  000122          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000122  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000124  000126          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000126  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000130  000132          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000132  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000134  000136          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000136  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000140  000142          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000142  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000144  000146          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000146  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000150  000152          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000152  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
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E02


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   676  000154  000156                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   677  000156  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   678  000160  000162                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   679  000162  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   680  000164  000166                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   681  000166  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   682  000170  000172                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   683  000172  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   684  000174  000176                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   685  000176  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   686  000200  000202                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   687  000202  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   688  000204  000206                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   689  000206  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   690  000210  000212                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   691  000212  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   692  000214  000216                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   693  000216  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   694  000220  000222                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   695  000222  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   696  000224  000226                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   697  000226  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   698  000230  000232                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   699  000232  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   700  000234  000236                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   701  000236  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   702  000240  000242                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   703  000242  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   704  000244  000246                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   705  000246  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   706  000250  000252                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   707  000252  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   708  000254  000256                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   709  000256  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   710  000260  000262                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   711  000262  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   712  000264  000266                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   713  000266  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   714  000270  000272                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   715  000272  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   716  000274  000276                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   717  000276  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   718  000300  000302                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   719  000302  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   720  000304  000306                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   721  000306  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   722  000310  000312                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   723  000312  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   724  000314  000316                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   725  000316  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   726  000320  000322                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   727  000322  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   728  000324  000326                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   729  000326  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
   730  000330  000332                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   731  000332  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
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 732  000334  000336                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 733  000336  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 734  000340  000342                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 735  000342  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 736  000344  000346                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 737  000346  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 738  000350  000352                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 739  000352  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 740  000354  000356                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 741  000356  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 742  000360  000362                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 743  000362  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 744  000364  000366                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 745  000366  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 746  000370  000372                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 747  000372  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 748  000374  000376                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 749  000376  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 750  000400  000402                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 751  000402  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 752  000404  000406                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 753  000406  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 754  000410  000412                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 755  000412  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 756  000414  000416                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 757  000416  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 758  000420  000422                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 759  000422  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 760  000424  000426                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 761  000426  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 762  000430  000432                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 763  000432  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 764  000434  000436                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 765  000436  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 766  000440  000442                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 767  000442  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 768  000444  000446                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 769  000446  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 770  000450  000452                  +2            ;UNEXPECTED TRAP TO THIS LOCATION
 771  000452  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 772  000454  000456                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 773  000456  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 774  000460  000462                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 775  000462  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 776  000464  000466                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 777  000466  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 778  000470  000472                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 779  000472  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 780  000474  000476                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 781  000476  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 782  000500  000502                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 783  000502  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 784  000504  000506                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 785  000506  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
 786  000510  000512                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 787  000512  000000                HALT            ;EXAMINE STACK TO FIND CAUSE
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   788  000514  000516                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   789  000516  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   790  000520  000522                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   791  000522  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   792  000524  000526                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   793  000526  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   794  000530  000532                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   795  000532  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   796  000534  000536                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   797  000536  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   798  000540  000542                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   799  000542  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   800  000544  000546                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   801  000546  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   802  000550  000552                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   803  000552  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   804  000554  000556                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   805  000556  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   806  000560  000562                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   807  000562  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   808  000564  000566                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   809  000566  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   810  000570  000572                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   811  000572  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   812  000574  000576                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   813  000576  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   814  000600  000602                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   815  000602  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   816  000604  000606                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   817  000606  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   818  000610  000612                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   819  000612  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   820  000614  000616                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   821  000616  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   822  000620  000622                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   823  000622  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   824  000624  000626                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   825  000626  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   826  000630  000632                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   827  000632  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   828  000634  000636                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   829  000636  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   830  000640  000642                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   831  000642  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   832  000644  000646                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   833  000646  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   834  000650  000652                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   835  000652  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   836  000654  000656                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   837  000656  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   838  000660  000662                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   839  000662  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   840  000664  000666                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   841  000666  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
   842  000670  000672                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   843  000672  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
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   944  000674  000676                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   945  000676  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   946  000700  000702                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   947  000702  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   948  000704  000706                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   949  000706  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   950  000710  000712                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   951  000712  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   952  000714  000716                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   953  000716  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   954  000720  000722                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   955  000722  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   956  000724  000726                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   957  000726  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   958  000730  000732                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   959  000732  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   960  000734  000736                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   961  000736  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   962  000740  000742                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   963  000742  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   964  000744  000746                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   965  000746  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   966  000750  000752                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   967  000752  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   968  000754  000756                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   969  000756  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   970  000760  000762                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   971  000762  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   972  000764  000766                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   973  000766  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   974  000770  000772                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   975  000772  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   976  000774  000776                                .+2             ;UNEXPECTED TRAP TO THIS LOCATION
   977  000776  000000                                HALT            ;EXAMINE STACK TO FIND CAUSE
   978                                  036400    ;VECTOR INITIALIZATION
   979          000024                  036900    .=24
   980  000024  013744                  037000            .PFAIL          ;POWER FAIL VECTOR
   981  000026  000340                  037100            340             ;PRIORITY 7
   982  000030  016132                  037200            .HLT
   983  000032  000340                  037300            340
   984  000034  000056                  037400            .TRPSRV
   985  000036  000340                  037500            340
   986                                  037600
   987          000046                  037650    .=46
   988  000046  012436                  037655    LOGICAL
   989          000052                  037660    .=52
   990  000052  000000                  037665    0
   991          000056                  037700    .=56
   992                                            ;TRAP DISPATCH SERVICE
   993                                            ;ARGUMENT OF TRAP IS EXTRACTED
   994                                            ;AND USED AS OFFSET TO OBTAIN POINTER
   995                                            ;TO SELECTED SUBROUTINE
   996
   997  000056  011646                  .TRPSR: MOV     (SP),-(SP)              ;GET PC OF RETURN
   998  000060  162716  000002                  SUB     #2,(SP)                 ;=PC OF TRAP
   999  000064  017616  000000                  MOV     @(SP),(SP)              ;GET TRP
```

```
 900  000070  006316                          TRPOK:  ASL     (SP)                    ;MULTIPLY TRAP ARG BY 2
 901  000072  042716  177001                          BIC     #177001,(SP)            ;CLEAR UNWANTED BITS
 902  000076  062716  001202                          ADD     #.TRPTAB,(SP)           ;POINTER TO SUBROUTINE ADDRESS
 903  000102  017616  000000                          MOV     @(SP),(SP)              ;SUBROLTINE ADDRESS
 904  000106  000136                                   JMP     @(SP)+                  ;GO TO SUBROUTINE
 905                                   07900
 906          000200                  08000   .=200
 907  000200  005037  001146          08100   START1: CLR     XLINEX
 908  000204  000137  001262          08200           JMP     BEGIN1                  ;SET UP CONSOL SWITCH REGISTER
 909                                   08300
 910          000210                  08400   .=210
 911  000210  005037  001146          08500           CLR     XLINEX
 912  000214  000137  007202          08600           JMP     BEGIN2                  ;D825S CONNECTOR TEST
 913                                   08700
 914          001050                  08800   .=1050
 915
 916
 917                                           ;INDIRECT POINTERS TO TELETYPE VECTORS AND REGISTERS
 918
 919  001050  177560                  TKCSR:  177560                  ;TELETYPE KEYBOARD CONTROL REGISTER
 920  001052  177562                  TKDBR:  177562                  ;TELETYPE KEYBOARD DATA BUFFER
 921  001054  177564                  TPCSR:  177564                  ;TELEPRINTER CONTROL REGISTER
 922  001056  177566                  TPDBR:  177566                  ;TELEPRINTER DATA BUFFER
 923
 924                                           ;PROGRAM CONTROL PARAMETERS
 925
 926  001060  000000                  RETURN: 0                       ;SCOPE ADDRESS FOR LOOP ON TEST
 927  001062  000000                  NEXT:   0                       ;ADDRESS OF NEXT TEST TO BE EXECUTED
 928  001064  000000                  LOCK:   0                       ;ADDRESS FOR LOCK ON CURRENT DATA
 929  001066  000000                  ICOUNT: 0                       ;NUMBER OF ITERATIONS THAT CURRENT TEST WILL BE
 930  001070  000000                  LPCNT:  0                       ;NUMBER OF ITEREATIONS COMPLETED
 931  001072  000000                  TSTNO:  0                       ;NUMBER OF TEST IN PROGRESS
 932  001074  000000                  PASCNT: 0                       ;NUMBER OF PASSES COMPLETED
 933  001076  000000                  ERRCNT: 0                       ;TOTAL NUMBER OF ERRORS
 934  001100  000000                  LSTERR: 0                       ;PC OF LAST ERROR CALL
 935
 936                                           ;PROGRAM VARIABLES
 937
 938  001102  000000                  TEMP1:  0                       ;TEMPORARY STORAGE
 939  001104  000000                  TEMP2:  0                       ;TEMPORARY STORAGE
 940  001106  000000                  TEMP3:  0                       ;TEMPORARY STORAGE
 941  001110  000000                  TEMP4:  0                       ;TEMPORARY STORAGE
 942  001112  000000                  TEMP5:  0                       ;TEMPORARY STORAGE
 943  001114  000000                  SAVR0:  0                       ;R0 STORAGE
 944  001116  000000                  SAVR1:  0                       ;R1 STORAGE
 945  001120  000000                  SAVR2:  0                       ;R2 STORAGE
 946  001122  000000                  SAVR3:  0                       ;R3 STORAGE
 947  001124  000000                  SAVR4:  0                       ;R4 STORAGE
 948  001126  000000                  SAVR5:  0                       ;R5 STORAGE
 949  001130  000000                  SAVSP:  0                       ;STACK POINTER STORAGE
 950  001132  000000                  SAVPC:  0                       ;PROGRAM COUNTER STORAGE
 951  001134  000000                  SAVSR1: 0
 952  001136  000000                  TMPDAT: 0
 953  001140  000000                  SLIM:   0
 954  001142  000000                  BPC:    0
 955  001144  000000                  TSYNC:  0
```

```
   956  001146  000000                          XLINEX: 0
   957  001150  000000                          CABLE:  0
   958  001152  000000                          TDATA:  0
   959  001154  000000                          RDATA:  0
   960  001156  000000                          CHLEN:  0
   961  001160  000000                          LIMIT:  0
   962  001152  000000                          SCNT:   0
   963  001164  000000                          SAVSR2: 0
   964  001166  000000                          TIME:   0
   965  001170  000000                          TP:     0
   966  001172  000000                          RP:     0
   967  001174  000000                          BACK:   0
   968
```

```
                                        ;PROGRAM CONTROL FLAGS

001176      000                 INIFLG: .BYTE   0               ;PROGRAM INITIALIZATION FLAG
001177      000                 STFLG:  .BYTE   0               ;TEST START FLAG
001200      000                 ERRFLG: .BYTE   0               ;ERROR OCCURED FLAG
001201      000                 LOKFLG: .BYTE   0               ;LOCK ON CURRENT TEST FLAG
          000000                $Y=0

                                        ;DEFINITIONS FOR TRAP SUBROUTINE CALLS
                                        ;POINTERS TO SUBROUTINES CAN BE FOUND
                                        ;IN THE TABLE IMMEDIATLY FOLLOWING THE DEFINITIONS

                                ;*******************************************************************
                                ;*******************************************************************
001202                          .TRPTAB:
          104400                SCOPE=TRAP+0              ;CALL TO SCOPE LOOP AND ITERATION HANDLER
001202    015640                      .SCOPE
          104401                CLOCK=TRAP+1              ;CALL TO CLOCK DEVICE
001204    013342                      .CLOCK
          104402                RXCLK=TRAP+2              ;CALL TO CLOCK THE RX
001206    013402                      .RXCLK
          104403                DELAY=TRAP+3              ;CALL TO DELAY FOR SPEC. TIME.
001210    014300                      .DELAY
          104404                CLEAR=TRAP+4              ;CALL TO BIT CLEAR SPEC BIT
001212    012752                      .CLEAR
          104405                VALID=TRAP+5              ;CALL TO MAKE SURE ONLY SPEC BIT CLR
001214    012670                      .VALID
          104406                SCOP1=TRAP+6              ;CALL TO LOOP ON CURRENT DATA HANDLER
001216    016052                      .SCOP1
          104407                TYPE=TRAP+7               ;CALL TO TELETYPE OUTPUT ROUTINE
001220    016070                      .TYPE
          104410                SAV05=TRAP+10             ;CALL TO REGISTER SAVE ROUTINE
001222    016676                      .SAV05
          104411                RES05=TRAP+11             ;CALL TO REGISTER RESTORE ROUTINE
001224    016736                      .RES05
          104412                CONVRT=TRAP+12            ;CALL TO DATA OUTPUT ROUTINE
001226    016476                      .CONVRT
          104413                CNVRT=TRAP+13             ;CALL TO DATA OUTPUT ROUNTINE WITHOUT CR/LF.
001230    016502                      .CNVRT

                                ;*******************************************************************
                                ;*******************************************************************
                        09100
                        09200
                        09300   ;*******************************************************************
                        09400
001232    000001        09500   DPRS:   .BLKW 1                 ;DP11 RECEIVER STATUS
001234    000001        09600   DPRB:   .BLKW 1                 ;DP11 RECEIVER BUFFER
001236    000001        09700   SYNC:   .BLKW 1                 ;SYNC BUFFER
001240    000001        09800   DPTS:   .BLKW 1                 ;DP11 TRANSMITTER STATUS
001242    000001        09900   DPTB:   .BLKW 1                 ;DP11 TRANSMITTER BUFFER
001244    000001        10000   SEXT:   .BLKW 1                 ;DP11 SYNC EXTENSION
                        10100
                        10200
                        10300   ;*******************************************************************
```

```
  1025  001246  000001                    10400   DPRIV:  .BLKW 1                 ;DP11 RECEIVER INTERRUPT VECTOR
  1026  001250  000001                    10500   DPRP:   .BLKW 1                 ;DP11 RECEIVER PRIORITY
  1027  001252  000001                    10600   DPTIV:  .BLKW 1                 ;DP11 TRANSMITTER INTERRUPT VECTOR
  1028  001254  000001                    10700   DPTP:   .BLKW 1                 ;DP11 TRANSMITTER PRIORITY
  1029  001256  000300                    10800   BASVEC: 300                     ;THIS IS THE FIRST VECTOR. PATCH FOR YOUR FIRST
  1030  001260  174770                    10900   BASCSR: 174770                  ;FIRST CSR ADDRESS.MAKE IT YOURS.
  1031                                    11000
  1032                                    11100   ;***************************************************************
  1033                                    11200
  1034  001262  000005                    11300   BEGIN1: RESET                   ;CLEAR THE WORLD.
  1035  001264  005037  001150            11400           CLR     CABLE           ;SET FLAG FOR NO CABLE TEST.
  1036  001270  012706  001050            11500           MOV     #STACK,SP       ;SET UP STACK POINTER
  1037  001274  012737  000340  177776    11600           MOV     #340,PS         ;SET PROCESSOR PRIORITY = 7
  1038  001302  105737  177570            11700   STAR:   TSTB    SWR             ;IS SWITCH SEVEN SET??
  1039  001306  100005                    11800           BPL     BGND            ;BR IF SW 07 NOT UP.
  1040  001310  004737  012462            11900           JSR     PC,CLRVEC       ;SET UP COMM VECTOR AREA.
  1041  001314  004737  012202            12000           JSR     PC,LINE.N       ;GO GET THE DESIERD LINE NO. AND VECTOR.
  1042  001320  000404                    12100           BR      PART1           ;GO TO START THE TEST.
  1043  001322  004737  012462            12200   BGND:   JSR     PC,CLRVEC       ;SET UP COMM VECTORS
  1044  001326  004737  012246            12300           JSR     PC,LINE.X       ;GO AND AUTO CYCLE THROUGH DP11S
  1045  001332  005737  001150            12400   PART1:  TST     CABLE           ;SHOULD I DO THE CABLE TEST OR MAINT. TEST??
  1046  001336  001402                    12500           BEQ     .+6             ;BR IF MAINT. TEST
  1047  001340  000137  007254            12600           JMP     PART2           ;GO DO THE CABLE TEST
  1048  001344  012737  001352  001060    12700           MOV     #TST1,RETURN    ;SET RETURN ADDRESS
  1049                                    12800
  1050                                    12900
  1051                                    13000   ;
  1052                                    13100   ;******TEST 1:  READ/WRITE ALL BITS OF STATUS*********
  1053                                            ;*************
  1054                                            ;            *
  1055                                            ; TEST 1
  1056                                            ;            *
  1057                                            ;*************
  1058                                            ;***************************************************************
  1059  001352  012737  000001  001072            TST1:   MOV     #1,TSTNO
  1060  001360  012737  001464  001062                    MOV     #TST2,NEXT
  1061  001366  012737  000340  177776    13300           MOV     #340,PS         ;SET PROCESSOR STATUS TO 7
  1062  001374  005077  177640            13400           CLR     @DPTS           ;CLEAR TRANSMITTER STATUS
  1063  001400  005077  177626            13500           CLR     @DPRS           ;CLEAR RECEIVER STATUS
  1064  001404  012777  014500  177640    13600           MOV     #TINT,@DPTIV    ;SET UP TRANSMITTER TEST VECTOR 1
  1065  001412  012777  014504  177626    13700           MOV     #RINT,@DPRIV    ;SET UP RECEIVER TEST VECTOR 1
  1066  001420  012777  000240  177622    13800           MOV     #240,@DPRP      ;SET UP RECEIVER PRIORITY=5
  1067  001426  012777  000240  177620    13900           MOV     #240,@DPTP      ;SET UP TRANSMITTER PRIORITY=5
  1068  001434  112777  000026  177574    14000           MOVB    #26,@SYNC       ;CLEAR NOISE FROM SYNC
  1069  001442  052777  000004  177562    14100           BIS     #BIT2,@DPRS     ;SET MAINTENANCE MODE
  1070                                    14200                                   ;TO ENABLE INTERNAL CLOCK (3kHZ)
  1071  001450  032777  000004  177554    14300           BIT     #BIT2,@DPRS     ;MAINT. SET
  1072  001456  001001                    14400           BNE     .+4             ;YES
  1073  001460  104000                    14500           HLT                     ;REPORT ERROR
  1074  001462  104400                    14600           SCOPE
```

```
 1075                                    14800   ;AN ILLEGAL INTERRUPT WILL TRAP TO
 1076                                    14900   ;AN ERROR MESSAGE ROUTINE
 1077                                    15000   ;TEST ALL READ/WRITE BITS OF PECEIVER STATUS
 1078                                    15100
 1079                                    15200
 1080                                            ;*************
 1091                                            ;            *
 1082                                            ; TEST 2
 1083                                            ;            *
 1084                                            ;*************
 1085                                            ;*********************************************************************
 1086  001464  012737  000002  001072            TST2:   MOV     #2,TSTNO
 1087  001472  012737  001572  001062                    MOV     #TST3,NEXT
 1088  001500  005000                    15400           CLR     R0
 1089  001502  013737  001232  013056    15500           MOV     DPRS,REG                ;TEST RECEIVER STATUS BITS
 1090  001510  004537  012510            15600           JSR     R5,BITST                ;SYNC STRIP
 1091  001514  000001                    15700           BIT0
 1092  001516  004537  012510            15800           JSR     R5,BITST                ;HALF DUPLEX
 1093  001522  000002                    15900           BIT1
 1094  001524  004537  012510            16000           JSR     R5,BITST                ;MAINTENANCE MODE
 1095  001530  000004                    16100           BIT2
 1096  001532  004537  012510            16200           JSR     R5,BITST                ;RECEIVER INTERRUPT ENABLE
 1097  001536  000100                    16300           BIT6
 1098  001540  004537  012510            16400           JSR     R5,BITST                ;DONE
 1099  001544  000200                    16500           BIT7
 1100  001546  004537  012510            16600           JSR     R5,BITST                ;BITS/CHAR
 1101  001552  000400                    16700           BIT8
 1102  001554  004537  012510            16800           JSR     R5,BITST                ;" "
 1103  001560  001000                    16900           BIT9
 1104  001562  004537  012510            17000           JSR     R5,BITST                ; "     "
 1105  001566  002000                    17100           BIT10
 1106  001570  104400                    17200           SCOPE
 1107                                    17300
 1108                                    17400
 1109                                    17500   ;BIT3=MISCELLANEOUS RECEIVE=READ ONLY
 1110                                    17600   ;BIT11=RECEIVE ACTIVE=READ/WRITE ZERO
 1111                                    17700   ;BIT12=PARITY(VRC)=READ ONLY
 1112                                    17800   ;ALL OTHER BITS ARE NOT USED
 1113                                    17900
 1114                                    18000   ;TEST ALL READ/WRITE BITS OF TRANSMITTER STATUS
 1115                                    18100
 1116                                    18200
 1117                                            ;*************
 1118                                            ;            *
 1119                                            ; TEST 3
 1120                                            ;            *
 1121                                            ;*************
 1122                                            ;*********************************************************************
 1123  001572  012737  000003  001072            TST3:   MOV     #3,TSTNO
 1124  001600  012737  001722  001062                    MOV     #TST4,NEXT
 1125  001606  005000                    18400           CLR     R0
 1126  001610  013737  001240  013056    18500           MOV     DPTS,REG                ;TEST TRANS STATUS BITS
 1127  001616  004537  012510            18600           JSR     R5,BITST                ;TERMINAL READY R/W
 1128  001622  000001                    18700           BIT0
 1129  001624  042777  000004  177400    18800           BIC     #BIT2,@DPRS             ;SHUT OFF CLOCK FOR IDLE SYNC
 1130  001632  004537  012510            18900           JSR     R5,BITST                ;IDLE SYNC R/W
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 1131  001636  000002                        19000          BIT1
 1132  001640  052777  000004  177364        19100          BIS     #BIT2,@DPRS             ;START CLOCK
 1133  001646  004537  012510                19200          JSR     R5,BITST                ;SECONDARY TRANSMIT R/W
 1134  001652  000010                        19300          BIT3
 1135  001654  004537  012510                19400          JSR     R5,BITST                ;STATUS INTERRUPT ENABLE R/W
 1136  001660  000040                        19500          BIT5
 1137  001662  004537  012510                19600          JSR     R5,BITST                ;TRANSMITTER INTERRUPT R/W
 1138  001666  000100                        19700          BIT6
 1139  001670  004537  012510                19800          JSR     R5,BITST                ;DONE
 1140  001674  000200                        19900          BIT7
 1141  001676  004537  012510                20000          JSR     R5,BITST                ;RING FLAG R/W
 1142  001702  020000                        20100          BIT13
 1143  001704  004537  012510                20200          JSR     R5,BITST                ;CARRIER DOWN
 1144  001710  100000                        20300          BIT15
 1145  001712  004537  012510                20400          JSR     R5,BITST                ;RECEIVER OVERUN FLAG R/W
 1146  001716  040000                        20500          BIT14
 1147  001720  104400                        20600          SCOPE
 1148                                        20700
 1149                                        20800
 1150                                        20900
 1151                                        21000
 1152                                        21100      ;RESET TEST
 1153                                        21200      ;SET PROCESSOR PRIORITY TO 7
 1154                                        21300      ;SET ALL WRITE BITS IN T & R STATUS
 1155                                        21400      ;ISSUE RESET AND VERIFY ALL BITS THAT ARE
 1156                                        21500      ;TO BE CLEARED BY RESET--WERE
 1157                                        21600
 1158                                        21700      ;NOTE: IF BITS/CHAR BITS ARE SET TO ALL 1'S RCV WILL
 1159                                        21800      ;NOT GO ACTIVE
 1160                                        21900
 1161                                        22000      ;TEST READ/WRITE BITS OF RECEIVER STATUS
 1162                                        22100      ;SECTION 1
 1163                                        22200
 1164                                                   ;*************
 1165                                                   ;             *
 1166                                                   ; TEST 4      
 1167                                                   ;             *
 1168                                                   ;*************
 1169                                                   ;*********************************************************************
 1170  001722  012737  000004  001072                   TST4:   MOV     #4,TSTNO
 1171  001730  012737  002002  001062                           MOV     #TST5,NEXT
 1172  001736  005077  177276                22400              CLR     @DPTS                   ;CLEAR TRANSMITTER STATUS
 1173  001742  012777  000004  177262        22500              MOV     #BIT2,@DPRS             ;MAINTENANCE MODE
 1174  001750  012777  143707  177254        22600              MOV     #143707,@DPRS           ;SET ALL RECEIVER STATUS BITS
 1175  001756  017701  177250                22700              MOV     @DPRS,R1                ;SAVE THE RX STATUS
 1176  001762  042701  010000                22800              BIC     #BIT12,R1               ;CLEAR THE PARITY BIT
 1177  001766  012700  003707                22900              MOV     #3707,R0                ;SET R0 FOR ERROR MESSAGE
 1178  001772  020001                        23000              CMP     R0,R1                   ;IS THE STATUS WHAT I EXPECTED??
 1179  001774  001401                        23100              BEQ     .+4                     ;BR IF STATLS IS OK.
 1180  001776  104001                        23200              HLT     1                       ;ERROR RX STATUS NOT WHAT EXPECTED.
 1181  002000  104400                        23300              SCOPE                           ;SCOPE THIS TEST.
 1182                                        23400
 1183                                        23500
 1184                                        23600
 1185                                        23700      ;TEST ALL READ/WRITE BITS OF THE TRANSMITTER STATLS
 1186                                        23900      ;SECTION 2
```

```
                                                33300
                                                        ;*************
                                                        ;             *
                                                        ; TEST 5      *
                                                        ;             *
                                                        ;*************
                                                        ;*************************************************************************
002002  012737  000005  001072                  TST5:   MOV     #5,TSTNO
002010  012737  002062  001062                          MOV     #TST6,NEXT
002016  012777  000004  177126          24100           MOV     #BIT2,@DPRS             ;SET MAINT MODE
002024  012777  160353  177126          24200           MOV     #160353,@DPTS           ;SET R/W BITS ON TX
002032  005000                          24300           CLR     R0                      ;SET FOR A DELAY
002034  062700  000001                  24400   1$:     ADD     #1,R0                   ;WAIT FOR CLEAR TO SEND AND REQUEST TO S
002040  001375                          24500           BNE     1$                      ;TO COME UP.
002042  017701  177172                  24600           MOV     @DPTS,R1                ;SAVE THE TX STATUS.
002046  012700  163353                  24700           MOV     #163353,R0              ;SET R0 FOR ERROR MESSAGE.
002052  020001                          24800           CMP     R0,R1                   ;IS THE TX STATUS CORRECT??
002054  001401                          24900           BEQ     .+4                     ;BR IF GOOD
002056  104001                          25000           HLT     1                       ;TX STATUS ERROR
002060  104400                          25100           SCOPE                           ;SCOPE THIS TEST
                                        25200
                                        25300
                                        25400
                                        25500   ;ISSUE "RESET" AND VERIFY ALL BITS ARE CLEARED
                                        25600   ;SECTION 3
                                        25700
                                                        ;*************
                                                        ;             *
                                                        ; TEST 6      *
                                                        ;             *
                                                        ;*************
                                                        ;*************************************************************************
002062  012737  000006  001072                  TST6:   MOV     #6,TSTNO
002070  012737  002134  001062                          MOV     #TST7,NEXT
002076  012777  000004  177126          25900           MOV     #BIT2,@DPRS             ;SET MAINT MODE
002104  052777  143707  177120          26000           BIS     #143707,@DPRS           ;WRITE THE STATUS REG
002112  000006                          26100           RESET                           ;ISSUE RESET INSTR.
002114  005100                          26200           COM     R0                      ;FLASH THE LIGHTS
002116  017701  177110                  26300           MOV     @DPRS,R1                ;SAVE THE STATUS
002122  005701                          26400           TST     R1                      ;IS IT ZERO??
002124  001402                          26500           BEQ     .+6                     ;BR IF GOOD
002126  005000                          26600           CLR     R0                      ;SET R0 FOR ERROR MESSAGE
002130  104001                          26700           HLT     1                       ;RX CSR NOT CLEARED BY INIT.
002132  104400                          26800           SCOPE                           ;SCOPE THIS TEST
                                        26900
                                        27000
                                        27100
                                        27200
                                        27300
                                        27400   ;VERIFY ALL READ-WRITE BITS OF TRANSMITTER STATUS ARE CLEAR
                                        27500   ;SECTION 4
                                        27600
                                                        ;*************
                                                        ;             *
                                                        ; TEST 7      *
                                                        ;             *
```

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1243                                                    ;*************
1244                                                    ;*************************************************************************
1245  002134  012737  000007  001072                    TST7:   MOV     #7,TSTNO
1246  002142  012737  002206  001062                            MOV     #TST10,NEXT
1247  002150  012777  000004  177054  27800             MOV     #BIT2,@DPRS             ;SET MAINT MODE
1248  002156  012777  160353  177054  27900             MOV     #160353,@DPTS           ;WRITE TX STATUS
1249  002164  000005                  28000             RESET                           ;ISSUE A RESET INSTRUCTION
1250  002166  005100                  28100             COM     R0                      ;FLASH THE LIGHTS.
1251  002170  017701  177044          28200             MOV     @DPTS,R1                ;SAVE TX STATUS
1252  002174  005701:                 28300             TST     R1                      ;IS IT ZERO??
1253  002176  001402                  28400             BEQ     .+6                     ;BR IF GOOD
1254  002200  005000                  28500             CLR     R0                      ;SET R0 FOR ERROR MSG
1255  002202  104400:                 28600             HLT     1                       ;TX STATUS REG NOT ZEROED BY INIT
1256  002204  104400                  28700             SCOPE                           ;SCOPE THIS TEST
1257                                  28800
1258                                  28900
1259                                  29000
1260                                  29100     ;TEST READY BIT CLEAR BEFORE READY CAN COME UP
1261                                  29200
1262                                            ;*************
1263                                            ;            *
1264                                            ; TEST 10
1265                                            ;            *
1266                                            ;*************
1267                                            ;*************************************************************************
1268  002206  012737  000010  001072            TST10:  MOV     #10,TSTNO
1269  002214  012737  002266  001062                    MOV     #TST11,NEXT
1270  002222  012777  160377  177010  29400             MOV     #160377,@DPTS           ;LOAD STATUS
1271  002230  000005                  29500             RESET                           ;ISSUE RESET INSTR.
1272  002232  005100                  29600             COM     R0                      ;FLASH THE LIGHTS
1273  002234  017701  177000          29700             MOV     @DPTS,R1                ;SAVE THE STATUS.
1274  002240  105777  176774          29800             TSTB    @DPTS                   ;READY CLEARED
1275  002244  100002                  29900             BPL     .+6                     ;YES
1276  002246  005000                  30000             CLR     R0
1277  002250  104001                  30100             HLT     1                       ;REPORT ERROR
1278  002252  005777  176762          30200             TST     @DPTS                   ;STATUS CLEAR
1279  002256  001402                  30300             BEQ     .+6                     ;YES
1280  002260  005000                  30400             CLR     R0
1281  002262  104001                  30500             HLT     1                       ;REPORT ERROR
1282  002264  104400                  30600             SCOPE
1283                                  30700
1284                                  30800
1285                                  30900
1286                                  31000     ;BIT INTERACTION TEST
1287                                  31100     ;SET EACH BIT AND VERIFY THAT ONLY THAT BIT IS AFFECTED
1288                                  31200
1289                                  31300
1290                                  31400     ;RECEIVER STATUS BIT VALIDITY TEST
1291                                  31500
1292                                            ;*************
1293                                            ;            *
1294                                            ; TEST 11
1295                                            ;            *
1296                                            ;*************
1297                                            ;*************************************************************************
1298  002266  012737  000011  001072            TST11:  MOV     #11,TSTNO
```

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 1299  002274  012737  002354  001062                MOV     #TST12,NEXT
 1300  002302  005000                      31700     CLR     R0
 1301  002304  013737  001232  013056      31800     MOV     DPRS,REG                ;TEST RCV
 1302  002312  104405                      31900     VALID                           ;STRIP SYNC
 1303  002314  000001                      32000     BIT0
 1304  002316  104405                      32100     VALID                           ;HALF DUPLEX
 1305  002320  000002                      32200     BIT1
 1306  002322  104405                      32300     VALID                           ;MAINTENANCE MODE
 1307  002324  000004                      32400     BIT2
 1308  002326  104405                      32500     VALID                           ;INTERRUPT ENABLE
 1309  002330  0001C0                      32600     BIT6
 1310  002332  104405                      32700     VALID                           ;DONE
 1311  002334  000200                      32800     BIT7
 1312  002336  104405                      32900     VALID                           ;BITS/CHAR
 1313  002340  000400                      33000     BIT8
 1314  002342  104405                      33100     VALID                           ;"   "
 1315  002344  001000                      33200     BIT9
 1316  002346  104405                      33300     VALID                           ; "   "
 1317  002350  002000                      33400     BIT10
 1318  002352  104400                      33500     SCOPE
 1319                                      33600
 1320                                      33700 ;TRANSMITTER STATUS BIT VALIDITY TEST
 1321                                      33800
 1322                                            ;*************
 1323                                            ;             *
 1324                                            ; TEST 12     *
 1325                                            ;             *
 1326                                            ;*************
 1327                                            ;*****************************************************************
 1328  002354  012737  000012  001072      TST12:  MOV     #12,TSTNO
 1329  002362  012737  002452  001062              MOV     #TST13,NEXT
 1330  002370  005000                      34000     CLR     R0
 1331  002372  013737  001240  013056      34100     MOV     DPTS,REG                ;TEST XMIT STATUS
 1332  002400  005077  176634              34200     CLR     @DPTS                   ;CLEAR TRANSMITTER STATUS
 1333  002404  104405                      34300     VALID                           ;TERMINAL READY
 1334  002406  000001                      34400     BIT0
 1335  002410  104405                      34500     VALID                           ;IDLE SYNC
 1336  002412  000002                      34600     BIT1
 1337  002414  104405                      34700     VALID                           ;MISC TRANSMIT
 1338  002416  000010                      34800     BIT3
 1339  002420  104405                      34900     VALID                           ;STATUS ENABLE
 1340  002422  000040                      35000     BIT5
 1341  002424  104405                      35100     VALID                           ;TRANSMITTER ENABLE
 1342  002426  000100                      35200     BIT6
 1343  002430  104405                      35300     VALID                           ;TRANSMITTER DONE
 1344  002432  000200                      35400     BIT7
 1345  002434  104405                      35500     VALID                           ;RING FLAG
 1346  002436  020000                      35600     BIT13
 1347  002440  104405                      35700     VALID                           ;RECEIVER OVERRUN
 1348  002442  040000                      35800     BIT14
 1349  002444  104405                      35900     VALID                           ;CARRIER DOWN
 1350  002446  100000                      36000     BIT15
 1351  002450  104400                      36100     SCOPE
 1352                                      36200
 1353                                      36300
 1354                                      36400
```

```
1355                                    36500   ;VERIFY BIT CLEAR ONLY CLEARS SPECIFIED BIT
1356                                    36600
1357                                    36700
1358                                    36800   ;RECEIVER TEST SECTION
1359                                    36900
1360                                            ;*************
1361                                            ;            *
1362                                            ; TEST 13    *
1363                                            ;            *
1364                                            ;*************
1365                                            ;*********************************************************************
1366  002452  012737  000013  001072            TST13:  MOV     #13,TSTNO
1367  002460  012737  002560  001062                    MOV     #TST14,NEXT
1368  002466  112777  000026  176542  37100             MOVB    #26,@SYNC       ;LOAD SYNC WITH ANYTHING
1369  002474  013737  001232  013056  37200             MOV     DPRS,REG        ;TEST RCV STATUS
1370  002502  012737  003707  001136  37300             MOV     #3707,TMPDAT    ;STORE STATUS IMAGE
1371  002510  012777  003707  176514  37400             MOV     #3707,@DPRS     ;SET UP STATUS
1372  002516  104404                  37500             CLEAR                   ;STRIP SYNC
1373  002520  000001                  37600             BIT0
1374  002522  104404                  37700             CLEAR                   ;HALF DUPLEX
1375  002524  000002                  37800             BIT1
1376  002526  104404                  37900             CLEAR                   ;MAINTENANCE MODE
1377  002530  000004                  38000             BIT2
1378  002532  104404                  38100             CLEAR                   ;RECEIVER INT ENB
1379  002534  000100                  38200             BIT6
1380  002536  104404                  38300             CLEAR                   ;RECEIVER DONE
1381  002540  000200                  38400             BIT7
1382  002542  104404                  38500             CLEAR                   ;BITS CHAR
1383  002544  000400                  38600             BIT8
1384  002546  104404                  38700             CLEAR                   ; "   "
1385  002550  001000                  38800             BIT9
1386  002552  104404                  38900             CLEAR                   ; "   "
1387  002554  002000                  39000             BIT10
1388  002556  104400                  39100             SCOPE
1389                                    39200
1390                                    39300   ;TRANSMITTER TEST SECTION
1391                                    39400
1392                                    39500   ;NOTE: "SEND REQUEST" IS SET BY "IDLE SYNC"
1393                                    39600   ;       "CLEAR-TO-SEND" IS SET BY MAINTENANCE MODE
```

```
1394                                    39800
1395                                    ;*************
1396                                    ;             *
1397                                    ; TEST 14
1398                                    ;             *
1399                                    ;*************
1400                                    ;*****************************************************************************
1401  002560  012737  000014  001072    TST14:  MOV     #14,TSTNO
1402  002566  012737  003044  001062            MOV     #TST15,NEXT
1403  002574  012737  000340  177776  40000     MOV     #340,PS         ;SET STATUS TO LEVEL SEVEN
1404  002602  012777  000004  176422  40100     MOV     #BIT2,@DPRS     ;SET MAINTENANCE MODE
1405  002610  012777  160353  176422  40200     MOV     #160353,@DPTS   ;SET UP STATUS
1406  002616  012737  163353  001136  40300     MOV     #163353,TMPDAT  ;STORE STATUS IMAGE
1407  002624  012700  005050          40400     MOV     #2600.,R0       ;DELAY 6MS FOR SEND REQUEST
1408  002630  005300                  40500     DEC     R0
1409  002632  001376                  40600     BNE     .-2
1410  002634  032777  001000  176378  40700     BIT     #BIT9,@DPTS     ;SEND REQUEST UP
1411  002642  001001                  40800     BNE     .+4             ;YES
1412  002644  104000                  40900     HLT                     ;REPORT ERROR
1413  002646  013737  001240  013056  41000     MOV     DPTS,REG        ;TEST TRANS
1414  002654  104404                  41100     CLEAR                   ;TERMINAL READY
1415  002656  000001                  41200     BIT0
1416                                  41300 ;IDLE SYNC
1417                                  41400
1418  002660  042737  003002  001136  41500     BIC     #3002,TMPDAT    ;CLEARING IDLE SYNC SHOULD CLEAR SEND REQUEST
1419  002666  042777  000002  176344  41600     BIC     #2,@DPTS        ;CLEAR IDLE SYNC
1420  002674  012700  007020          41700     MOV     #3600.,R0       ;WAIT FOR "CLEAR-TO-SEND" TO DROP
1421  002700  005300                  41800     DEC     R0
1422  002702  001376                  41900     BNE     .-2
1423  002704  013700  001136          42000     MOV     TMPDAT,R0
1424  002710  017701  176324          42100     MOV     @DPTS,R1
1425  002714  023777  001136  176316  42200     CMP     TMPDAT,@DPTS    ;IDLE SYNC AND SEND REQUEST CLEAR
1426  002722  001401                  42300     BEQ     .+4             ;YES
1427  002724  104001                  42400     HLT     1               ;REPORT ERROR
1428  002726  052737  003002  001136  42500     BIS     #3002,TMPDAT    ;REINSTATE IMAGE
1429  002734  052777  000002  176276  42600     BIS     #2,@DPTS        ;REINSTATE STATUS
1430  002742  104404                  42700     CLEAR                   ;MISC TRANSMIT
1431  002744  000010                  42800     BIT3
1432  002746  104404                  42900     CLEAR                   ;STATUS INTERRUPT ENABLE
1433  002750  000040                  43000     BIT5
1434  002752  104404                  43100     CLEAR                   ;TRANSMITTER INTERRUPT ENABLE
1435  002754  000100                  43200     BIT6
1436  002756  042777  000004  176246  43300     BIC     #BIT2,@DPRS     ;MAINT MODE OFF(STOP CLOCK)
1437  002764  042737  002000  001136  43400     BIC     #BIT10,TMPDAT   ;CLEAR "CLEAR-TO-SEND"
1438  002772  104404                  43500     CLEAR                   ;READY
1439  002774  000200                  43600     BIT7
1440  002776  052777  000004  176226  43700     BIS     #BIT2,@DPRS     ;MAINT MODE ON
1441  003004  052737  002000  001136  43800     BIS     #BIT10,TMPDAT   ;SET "CLEAR-TO-SEND" TEST BIT
1442  003012  042777  004004  176212  43900     BIC     #4004,@DPRS     ;SHUT OFF CLOCK
1443  003020  042737  002000  001136  44000     BIC     #BIT10,TMPDAT   ;CLEAR -TO -SEND
1444  003026  104404                  44100     CLEAR                   ;RING FLAG
1445  003030  020000                  44200     BIT13
1446  003032  104404                  44300     CLEAR                   ;RECEIVER OVERRUN
1447  003034  040000                  44400     BIT14
1448  003036  104404                  44500     CLEAR                   ;CARRIER DOWN
1449  003040  100000                  44600     BIT15
```

```
 1450  003042  104400                  44700          SCOPE
 1451                                  44800
 1452                                  44900    ;*****************************************************************
 1453                                  45000
 1454                                  45100    ;PRIORITY TESTS
 1455                                  45200    ;VERIFY THAT THERE ARE NO STATUS INTERRUPTS
 1456                                  45300    ;WHEN PS=5
 1457                                  45400    ;INTERRUPT WILL TRAP TO ERROR MESSAGE
 1458                                  45500
 1459                                           ;*************
 1460                                           ;             *
 1461                                           ; TEST 15     
 1462                                           ;             *
 1463                                           ;*************
 1464                                           ;*****************************************************************
 1465  003044  012737  000015  001072           TST15:  MOV     #15,TSTNO
 1466  003052  012737  003260  001062                   MOV     #TST16,NEXT
 1467  003060  012737  000240  177776  45700            MOV     #240,PS                 ;PRIORITY=5
 1468  003066  012777  014500  176156  45800            MOV     #FTINT,@DPTIV           ;SET FOR UNEXPECTED INTERUPT.
 1469  003074  012777  014504  176144  45900            MOV     #FRINT,@DPRIV           ;SET FOR UNEXPECTED INTERUPT.
 1470  003102  052777  000004  176122  46000            BIS     #BIT2,@DPRS             ;SET MAINTENANCE MODE
 1471  003110  052777  000040  176122  46100            BIS     #BIT5,@DPTS             ;STATUS INTERRUPT ENABLE (SIE)
 1472  003116  052777  010000  176114  46200            BIS     #BIT12,@DPTS            ;RING FLAG
 1473  003124  042777  020040  176106  46300            BIC     #20040,@DPTS            ;CLEAR CSR
 1474  003132  052777  000040  176100  46400            BIS     #BIT5,@DPTS             ;INT ENB (STATUS)
 1475  003140  052777  040000  176072  46500            BIS     #BIT14,@DPTS            ;RECEIVER OVERRUN FLAG
 1476  003146  042777  040040  176064  46600            BIC     #40040,@DPTS            ;CLEAR CSR
 1477  003154  052777  000040  176056  46700            BIS     #BIT5,@DPTS             ;INT ENB (STATUS)
 1478  003162  052777  100000  176050  46800            BIS     #BIT15,@DPTS            ;CARRIER DOWN FLAG
 1479  003170  042777  100040  176042  46900            BIC     #100040,@DPTS           ;CLEAR CSR
 1480                                  47000
 1481                                  47100    ;VERIFY NO TRANSMITTER READY INTERRUPTS
 1482                                  47200
 1483  003176  052777  000100  176034  47300            BIS     #BIT6,@DPTS             ;XMIT INT ENB
 1484  003204  052777  000001  176026  47400            BIS     #BIT0,@DPTS             ;NOISE
 1485  003212  052777  000002  176020  47500            BIS     #BIT1,@DPTS             ;MORE NOISE
 1486  003220  052777  000004  176012  47600            BIS     #BIT2,@DPTS             ;MORE NOISE
 1487  003226  052777  000010  176004  47700            BIS     #BIT3,@DPTS             ;MORE NOISE
 1488  003234  052777  000020  175776  47800            BIS     #BIT4,@DPTS             ;MORE NOISE
 1489  003242  042777  000037  175770  47900            BIC     #37,@DPTS               ;QUIET!
 1490  003250  042777  000100  175762  48000            BIC     #BIT6,@DPTS
 1491  003256  104400                  48100            SCOPE
 1492                                  48200
 1493                                  48300
 1494                                  48400    ;TEST FOR CONTROL OF STATUS INTERRUPT ENABLE BIT
 1495                                  48500    ;NO INTERRUPT SHOULD OCCUR IF INT ENB IS NOT SET
 1496                                  48600    ;INTERRUPT VECTOR POINTS TO ERROR MESSAGE ROUTINE
 1497                                  48700
 1498                                           ;*************
 1499                                           ;             *
 1500                                           ; TEST 16     
 1501                                           ;             *
 1502                                           ;*************
 1503                                           ;*****************************************************************
 1504  003260  012737  000016  001072           TST16:  MOV     #16,TSTNO
 1505  003266  012737  003416  001062                   MOV     #TST17,NEXT
```

```
 1506  003274  012737  000200  177776  48900          MOV     #200,PS                 ;PRIORITY=4
 1507  003302  012777  014500  175742  49000          MOV     #FTINT,@DPTIV           ;SET FOR UNEXPECTED TX INTER.
 1508  003310  012777  014504  175730  49100          MOV     #FRINT,@DPRIV           ;SET FOR UNEXPECTED RX INTER.
 1509  003316  052777  020000  175714  49200  1$:     BIS     #BIT13,@DPTS            ;RING FLAG
 1510  003324  042777  020000  175706  49300          BIC     #BIT13,@DPTS            ;CLEAR
 1511  003332  052777  040000  175700  49400          BIS     #BIT14,@DPTS            ;RECEIVER OVERRUN FLAG
 1512  003340  042777  040000  175672  49500          BIC     #BIT14,@DPTS            ;CLEAR
 1513  003346  052777  100000  175664  49600          BIS     #BIT15,@DPTS            ;CARRIER DOWN FLAG
 1514  003354  042777  100000  175656  49700          BIC     #BIT15,@DPTS
 1515  003362  052777  160000  175650  49800          BIS     #160000,@DPTS           ;SET ALL STATUS ERROR BITS
 1516  003370  042777  160000  175642  49900          BIC     #160000,@DPTS           ;CLEAR
 1517  003376  162737  000040  177776  50000          SUB     #40,PS                  ;DECREASE PRIORITY LEVEL
 1518  003404  032737  000340  177776  50100          BIT     #340,PS
 1519  003412  001341                  50200          BNE     1$
 1520  003414  104400                  50300          SCOPE                           ;YES
 1521                                  50400
 1522                                  50500  ;VERIFY THAT ALL STATUS BITS INTERRUPT AT ALL LEVELS
 1523                                  50600  ;EQUAL TO OR LESS THAN 4
 1524                                  50700  ;IF THE DEVICE INTERRUPTS SUCCESSFULLY, THE
 1525                                  50800  ;INTERRUPT SERVICE ROUTINE WILL RETURN
 1526                                  50900  ;THE PROGRAM COUNTER TO THE INSTRUCTION AFTER
 1527                                  51000  ;THE HLT CALL
 1528                                  51100
 1529                                         ;*************
 1530                                         ;            *
 1531                                         ; TEST 17    *
 1532                                         ;            *
 1533                                         ;*************
 1534                                         ;*************************************************************************
 1535  003416  012737  000017  001072         TST17:  MOV     #17,TSTNO
 1536  003424  012737  003602  001062                 MOV     #TST20,NEXT
 1537  003432  012777  003466  175612  51300          MOV     #1$,@DPTIV              ;SET UP INTERRUPT VECTOR=RTI
 1538  003440  012737  000200  177776  51400          MOV     #200,PS                 ;PRIORITY=4
 1539  003446  052777  000040  175564  51500          BIS     #BIT5,@DPTS             ;INT ENB STATUS
 1540  003454  052777  020000  175556  51600          BIS     #BIT13,@DPTS            ;RING FLAG
 1541  003462  000240                  51700          NOP                             ;SHOULD INTERRUPT AFTER NOP
 1542  003464  104003                  51800          HLT     3                       ;REPORT ERROR
 1543  003466  042777  020000  175544  51900  1$:     BIC     #BIT13,@DPTS            ;CLEAR RING
 1544  003474  022626                  52000          POP.SP                          ;ADJUST STACK
 1545  003476  012777  003524  175546  52100          MOV     #2$,@DPTIV              ;SET UP NEXT INTERRUPT VECTOR
 1546  003504  042737  000040  177776  52200          BIC     #BIT5,PS                ;SET PRIORITY TO 4
 1547  003512  052777  040000  175520  52300          BIS     #BIT14,@DPTS            ;RECEIVER OVERRUN FLAG
 1548  003520  000240                  52400          NOP
 1549  003522  104003                  52500          HLT     3                       ;REPORT ERROR
 1550  003524  042777  040000  175506  52600  2$:     BIC     #BIT14,@DPTS            ;CLEAR RCV O RUN
 1551  003532  022626                  52700          POP.SP                          ;ADJUST STACK
 1552  003534  012777  003562  175510  52800          MOV     #3$,@DPTIV              ;SET UP NEXT INTERRUPT VECTOR
 1553  003542  042737  000040  177776  52900          BIC     #BIT5,PS                ;SET PRIORITY TO 4
 1554  003550  052777  100000  175462  53000          BIS     #BIT15,@DPTS            ;CARRIER DOWN FLAG
 1555  003556  000240                  53100          NOP
 1556  003560  104003                  53200          HLT     3                       ;REPORT ERROR
 1557  003562  042777  100000  175450  53300  3$:     BIC     #BIT15,@DPTS            ;CLEAR CARRIER DOWN FLAG
 1558  003570  022626                  53400          POP.SP                          ;ADJUST STACK
 1559  003572  012777  014500          53500          MOV     #FTINT,@DPTIV           ;FALSE INT TRAP
 1560  003600  104400                  53600          SCOPE                           ;YES
 1561                                  53700
```

```
1562                                        53800
1563                                        53900   ;DOES LOADING XMIT BUFFER CLEAR XMT DONE
1564                                        54000
1565                                                ;*************
1566                                                ;            *
1567                                                ; TEST 20
1568                                                ;            *
1569                                                ;*************
1570                                                ;*************************************************************
1571  003602  012737  000020  001072                TST20:  MOV     #20,TSTNO
1572  003610  012737  003656  001062                        MOV     #TST21,NEXT
1573  003616  005077  175410              54200             CLR     @DPRS                   ;CLEAR RCV STATUS
1574  003622  012777  000200  175410      54300             MOV     #BIT7,@DPTS             ;DONE
1575  003630  105777  175404              54400             TSTB    @DPTS                   ;DONE SET
1576  003634  100401                      54500             BMI     .+4                     ;YES
1577  003636  104000                      54600             HLT                             ;REPORT ERROR
1578  003640  010077  175376              54700             MOV     R0,@DPTB                ;LOAD BUFFER
1579  003644  105777  175370              54800             TSTB    @DPTS                   ;DONE CLEARED
1580  003650  100001                      54900             BPL     .+4                     ;YES
1581  003652  104000                      55000             HLT                             ;REPORT ERROR
1582  003654  104400                      55100             SCOPE
1583                                      55200
1584                                      55300   ;VERIFY TRANSMITTER READY INTERRUPTS AT LEVEL 4
1585                                      55400   ;AT 8 BITS PER CHARACTER
1586                                      55500
1587                                                ;*************
1588                                                ;            *
1589                                                ; TEST 21
1590                                                ;            *
1591                                                ;************-*
1592                                                ;*************************************************************
1593  003656  012737  000021  001072                TST21:  MOV     #21,TSTNO
1594  003664  012737  003760  001062                        MOV     #TST22,NEXT
1595  003672  012777  000004  175332      55700             MOV     #BIT2,@DPRS
1596  003700  005077  175334              55800             CLR     @DPTS                   ;CLR STATUS
1597  003704  012777  003750  175340      55900             MOV     #1$,@DPTIV              ;TEST PASS VECTOR = RT1 TO IT3A
1598  003712  012737  000200  177776      56000             MOV     #200,PS                 ;PRIORITY=4
1599  003720  110077  175316              56100             MOVB    R0,@DPTB                ;LOAD XMIT BUFFER
1600  003724  052777  000100  175306      56200             BIS     #BIT6,@DPTS             ;XMIT INT ENB
1601  003732  105777  175302              56300             TSTB    @DPTS                   ;READY CLEARED BY BUFF LOAD
1602  003736  100001                      56400             BPL     .+4                     ;YES
1603  003740  104000                      56500             HLT                             ;REPORT ERROR
1604  003742  104403  004704              56600             DELAY   2500.                   ;25 MS
1605  003746  104003                      56700             HLT     3                       ;TRANSMITTER FAILED TO INTERRUPT
1606  003750  005077  175264              56800   1$:       CLR     @DPTS                   ;CLEAR INT ENB
1607  003754  022626                      56900             POP.SP                          ;ADJUST STACK
1608  003756  104400                      57000             SCOPE
1609                                      57100
1610                                      57200
1611                                      57300
1612                                      57400   ;VERIFY READY INTERRUPTS AT LEVEL 4
1613                                      57500   ;AT 7 BITS PER CHARACTER
1614                                      57600
1615                                                ;*************
1616                                                ;            *
1617                                                ; TEST 22
```

```
1618                                                    ;             *
1619                                                    ;*************
1620                                                    ;*****************************************************************************
1621  003760  012737  000022  001072                    TST22:  MOV     #22,TSTNO
1622  003766  012737  004074  001062                            MOV     #TST23,NEXT
1623  003774  012777  000004  175230  57800                     MOV     #BIT2,@DPRS
1624  004002  005077  175232          57900                     CLR     @DPTS                   ;CLR STATUS
1625  004006  012777  004060  175236  58000                     MOV     #1$,@DPTIV              ;TEST PASS VECTOR = IT4A
1626  004014  012737  000200  177776  58100                     MOV     #200,PS                 ;PRIORITY=4
1627  004022  052777  000400  175202  58200                     BIS     #BIT8,@DPRS             ;7 BITS/CHARACTER
1628  004030  110077  175206          58300                     MOVB    R0,@DPTB                ;LOAD XMIT BUFFER
1629  004034  052777  000100  175176  58400                     BIS     #BIT6,@DPTS             ;XMIT INT ENB
1630  004042  105777  175172          58500                     TSTB    @DPTS                   ;LOAD BUFFER CLEARED READY
1631  004046  100001                  58600                     BPL     .+4                     ;YES
1632  004050  104000                  58700                     HLT                             ;REPORT ERROR
1633  004052  104403  004704          58800                     DELAY   ,2500.                  ;25 MS
1634  004056  104003                  58900                     HLT     3                       ;TRANSMITTER FAILED TO INTERRUPT
1635  004060  005077  175146          59000  1$:      CLR     @DPRS                   ;CLR 7 BITS/CHAR
1636  004064  005077  175150          59100                     CLR     @DPTS                   ;CLEAR INT ENB
1637  004070  022626                  59200                     POP.SP                          ;ADJUST STACK
1638  004072  104400                  59300                     SCOPE                           ;YES
1639                                  59400
1640                                  59500  ;VERIFY READY INTERRUPTS AT LEVEL 4
1641                                  59600  ;AT 6 BITS PER CHARACTER
1642                                  59700
1643                                          ;*************
1644                                          ;             *
1645                                          ; TEST 23
1646                                          ;             *
1647                                          ;*************
1648                                          ;*****************************************************************************
1649  004074  012737  000023  001072          TST23:  MOV     #23,TSTNO
1650  004102  012737  004204  001062                  MOV     #TST24,NEXT
1651  004110  012777  000004  175114  59900           MOV     #BIT2,@DPRS
1652  004116  012737  000200  177776  60000           MOV     #200,PS                 ;PRIORITY=4
1653  004124  005077  175110          60100           CLR     @DPTS                   ;CLR STATUS
1654  004130  012777  004174  175114  60200           MOV     #1$,@DPTIV              ;TEST PASS VECTOR = IT5A
1655  004136  052777  001000  175066  60300           BIS     #BIT9,@DPRS             ;6 BITS/CHARACTER
1656  004144  110077  175072          60400           MOVB    R0,@DPTB                ;LOAD XMIT BUFFER
1657  004150  052777  000100  175062  60500           BIS     #BIT6,@DPTS             ;XMIT INT ENB
1658  004156  105777  175056          60600           TSTB    @DPTS                   ;LOAD BUFFER CLEARED READY
1659  004162  100001                  60700           BPL     .+4                     ;YES
1660  004164  104000                  60800           HLT                             ;REPORT ERROR
1661  004166  104403  004704          60900           DELAY   ,2500.                  ;25 MS
1662  004172  104003                  61000           HLT     3                       ;TRANSMITTER FAILED TO INTERRUPT
1663  004174  005077  175032          61100  1$:      CLR     @DPRS                   ;CLR 6 BITS/CHAR
1664  004200  022626                  61200           POP.SP                          ;ADJUST STACK
1665  004202  104400                  61300           SCOPE
1666                                  61400
1667                                  61500
1668                                  61600
1669                                  61700
1670                                  61800
1671                                  61900  ;TEST SYNC BUFFER IS READ/WRITE
1672                                  62000  ;NOTE:  SW09=1 WILL FREEZE ON CURRENT SYNC
1673                                  62100
```

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1674                                                ;*************
1675                                                ;            *
1676                                                ; TEST 24
1677                                                ;            *
1678                                                ;*************
1679                                                ;*************************************************************************
1680  004204  012737  000024  001072                TST24:  MOV     #24,TSTNO
1681  004212  012737  004326  001062                        MOV     #TST25,NEXT
1682  004220  012737  004256  001064                        MOV     #1$,LOCK
1683  004226  005037  001136          62300                CLR     TMPDAT                  ;CLEAR TEST DATA
1684  004232  005077  174774          62400                CLR     @DPRS                   ;CLEAR RECEIVER STATUS
1685  004236  005077  174776          62500                CLR     @DPTS
1686  004242  105077  174770          62600                CLRB    @SYNC                   ;CLEAR SYNC
1687  004246  105777  174764          62700                TSTB    @SYNC                   ;
1688  004252  001401                  62800                BEQ     .+4                     ;BRANCH IF SYNC CLEARED
1689  004254  104000                  62900                HLT                             ;REPORT ERROR
1690  004256  113777  001136  174752  63000  1$:           MOVB    TMPDAT,@SYNC            ;LOAD SYNC
1691  004264  113700  001136          63100                MOVB    TMPDAT,R0
1692  004270  117701  174742          63200                MOVB    @SYNC,R1
1693  004274  123777  001136  174734  63300                CMPB    TMPDAT,@SYNC            ;TEST IF LOAD OK
1694  004302  001401                  63400                BEQ     .+4                     ;BRANCH OK
1695  004304  104001                  63500                HLT     1                       ;REPORT ERROR
1696  004306  104406                  63600                SCOP1
1697  004310  105237  001136          63700                INCB    TMPDAT                  ;NEXT SYNC
1698  004314  001360                  63800                BNE     1$                      ;NO,TEST NEXT SYNC
1699  004316  112777  000026  174712  63900                MOVB    #26,@SYNC               ;ANY SYNC BUT ALL 1'S
1700  004324  104400                  64000                SCOPE
1701                                    64100
1702                                    64200  ;READ/WRITE ALL CHARACTERS IN SYNC EXTENSION
1703                                    64300  ;NOTE:  SW09=1 WILL FREEZE ON CURRENT SYNC
1704                                    64400
1705                                                ;*************
1706                                                ;            *
1707                                                ; TEST 25
1708                                                ;            *
1709                                                ;*************
1710                                                ;*************************************************************************
1711  004326  012737  000025  001072                TST25:  MOV     #25,TSTNO
1712  004334  012737  004462  001062                        MOV     #TST26,NEXT
1713  004342  032737  000400  001134  64600                BIT     #BIT8,SAVSR1            ;12 BITS/CHAR
1714  004350  001005                  64700                BNE     1$                      ;NO, BRANCH AROUND TEST
1715  004352  013737  001062  001060  64800                MOV     NEXT,RETURN
1716  004360  000177  174474          64900                JMP     @RETURN
1717  004364  005037  001136          65000  1$:           CLR     TMPDAT                  ;LOAD TMPDAT WITH ZEROS
1718  004370  112777  000017  174646  65100                MOVB    #17,@SEXT               ;LOAD SYNC EXT WITH 1'S
1719  004376  113777  001136  174640  65200  2$:           MOVB    TMPDAT,@SEXT            ;LOAD SYNC EXTENSION
1720  004404  117701  174634          65300                MOVB    @SEXT,R1
1721  004410  113700  001136          65400                MOVB    TMPDAT,R0
1722  004414  127737  174624  001136  65500                CMPB    @SEXT,TMPDAT            ;DID SYNC LOAD CORRECTLY
1723  004422  001401                  65600                BEQ     .+4                     ;YES
1724  004424  104001                  65700                HLT     1                       ;REPORT ERROR
1725  004426  104406                  65800                SCOP1
1726  004430  005237  001136          65900                INC     TMPDAT                  ;NEXT SYNC
1727  004434  022737  000020  001136  66000                CMP     #20,TMPDAT              ;HAVE ALL SYNC'S BEEN TESTED
1728  004442  001355                  66100                BNE     2$                      ;NO, CONTINUE TEST
1729  004444  105077  174574          66200                CLRB    @SEXT                   ;CLEAR SYNC EXT
```

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1730  004450  105777  174570          66300          TSTB    @SEXT                   ;TEST SYNC EXT
1731  004454  001401                  66400          BEQ     .+4                     ;BRANCH IF SYNC CLEARED
1732  004456  104000                  66500          HLT                             ;REPORT ERROR
1733  004460  104430                  66600          SCOPE
1734                                  66700
1735                                  66800
1736                                  66900  ;**************** SYNC TESTS ************************
1737                                  67000
1738                                  67100
1739                                  67200
1740                                  67300  ;SYNCHRONIZATION CHARACTER TEST
1741                                  67400  ;ISSUE ALL SYNC CHARACTERS AND VERIFY THAT IT WAS THE
1742                                  67500  ;CORRECT SYNC
1743                                  67600
1744                                  67700
1745                                  67800
1746                                  67900
1747                                  68000
1748                                         ;*************
1749                                         ;            *
1750                                         ; TEST 26
1751                                         ;            *
1752                                         ;*************
1753                                         ;*********************************************************************
1754  004462  012737  000026  001072         TST26:  MOV     #26,TSTNO
1755  004470  012737  005076  001062                 MOV     #TST27,NEXT
1756  004476  105077  174542          68200          CLRB    @SEXT                   ;CLEAR SYNC EXTENSION
1757  004502  005077  174532          68300          CLR     @DPTS                   ;CLEAR TRANSMITTER STATUS
1758  004506  005077  174520          68400          CLR     @DPRS                   ;CLEAR RECEIVER STATUS
1759  004512  012737  000200  177776  68500          MOV     #200,PS                 ;PRIORITY=4
1760  004520  012737  000377  001140  68600          MOV     #377,SLIM               ;SYNC LIMIT FOR 8BITS/CHAR
1761  004526  012737  000400  001142  68700          MOV     #400,BPC                ;INDEX TO  CHANGE BITS/CHAR
1762  004534  052777  000004  174470  68800          BIS     #BIT2,@DPRS             ;MAINT MODE
1763  004542  012737  000001  001144  68900          MOV     #1,TSYNC                ;FIRST SYNC = 1
1764  004550  012777  014504  174470  69000  1$:     MOV     #FRINT,@DPRIV           ;SET UP RECEIVER INT VECTOR TO ERROR
1765  004556  104403  013560          69100  2$:     DELAY   ,6000.                  ;10 CHAR TIMES FOR ALL 1'S IN BUFF
1766  004562  113777  001144  174446  69200          MOVB    TSYNC,@SYNC             ;LOAD SYNC BUFFER
1767  004570  117737  174442  001152  69300          MOVB    @SYNC,TDATA             ;STORE SYNC
1768  004576  113777  001144  174436  69400          MOVB    TSYNC,@DPTB             ;LOAD FIRST SYNC CHAR
1769  004604  105777  174430          69500          TSTB    @DPTS                   ;READY FOR NEXT SYNC
1770  004610  100375                  69600          BPL     .-4                     ;NO TEST AGAIN
1771  004612  032777  004000  174412  69700          BIT     #BIT11,@DPRS            ;TEST FOR PREMATURE ACTIVE
1772  004620  001401                  69800          BEQ     .+4                     ;BRANCH IF NOT SET
1773  004622  104000                  69900          HLT                             ;PREMATURE ACTIVE
1774  004624  113777  001144  174410  70000          MOVB    TSYNC,@DPTB             ;LOAD SECOND SYNC BYTE
1775  004632  012777  004670  174406  70100          MOV     #3$,@DPRIV              ;SET UP TEST VECTOR
1776  004640  105777  174374          70200          TSTB    @DPTS                   ;TRANSMITTER READY
1777  004644  100375                  70300          BPL     .-4                     ;NO
1778  004646  013777  001144  174366  70400          MOV     TSYNC,@DPTB             ;XMIT 3ED SYNC AS DATA
1779  004654  052777  000100  174350  70500          BIS     #BIT6,@DPRS             ;RCV INT ENB
1780  004662  104403  005670          70600          DELAY   ,3000.                  ;STALL 10 CHARACTER TIMES
1781  004666  104004                  70700          HLT     4                       ;REPORT ERROR
1782  004670  017737  174340  001136  70800  3$:     MOV     @DPRB,TMPDAT            ;SAVE DATA
1783  004676  013701  001136          70900          MOV     TMPDAT,R1
1784  004702  013700  001144          71000          MOV     TSYNC,R0
1785  004706  023737  001136  001144  71100          CMP     TMPDAT,TSYNC            ;CORRECT SYNC CHARACTER
```

```
1786  004714  001404                    71200          BEQ     4$                      ;YES
1787  004716  042777  000004  174306    71300          BIC     #BIT2,@DPRS             ;NO,SHUT OFF CLOCK
1788  004724  104001                    71400          HLT     1                       ;REPORT ERROR
1789  004726  105777  174300            71500    4$:   TSTB    @DPRS                   ;DONE CLEARED
1790  004732  100001                    71600          BPL     .+4                     ;YES
1791  004734  104000                    71700          HLT                             ;REPORT ERROR
1792  004736  042777  000100  174266    71800          BIC     #BIT6,@DPRS             ;CLEAR REV INT ENB
1793  004744  032777  004000  174260    71900          BIT     #BIT11,@DPRS            ;RECEIVER ACTIVE
1794  004752  001001                    72000          BNE     .+4                     ;YES
1795  004754  104000                    72100          HLT                             ;REPORT ERROR
1796  004756  112777  000026  174252    72200          MOVB    #26,@SYNC               ;CHANGE SYNC
1797  004764  042777  004000  174240    72300          BIC     #BIT11,@DPRS            ;CLEAR RECEIVER ACTIVE
1798  004772  032777  004000  174232    72400          BIT     #BIT11,@DPRS            ;RCV ACTIVE CLEARED
1799  005000  001401                    72500          BEQ     .+4                     ;YES
1800  005002  104000                    72600          HLT                             ;REPORT ERROR
1801  005004  022626                    72700          POP.SP                          ;ADJUST STACK
1802  005006  042737  000040  177776    72800          BIC     #BIT5,PS                ;SET PRIORITY TO 4
1803  005014  032737  040000  177570    72900          BIT     #BIT14,SWR              ;TEST FOR SCOPE LOOP
1804  005022  001002                    73000          BNE     5$                      ;BRANCH AROUND INC IF SCOPE
1805  005024  105237  001144            73100          INCB    TSYNC                   ;NEXT SYNC
1806  005030  123737  001140  001144    73200    5$:   CMPB    SLIM,TSYNC              ;HAVE ALL SYNC'S BEEN TESTED
1807  005036  001247                    73300          BNE     2$                      ;NO
1808  005040  005037  001144            73400          CLR     TSYNC                   ;YES
1809  005044  053777  001142  174160    73500          BIS     BPC,@DPRS               ;DEC BITS/CHAR BY 1 BIT
1810  005052  006237  001140            73600          ASR     SLIM                    ;DECREASE #BITS/CHAR
1811  005056  062737  000400  001142    73700          ADD     #400,BPC                ;DEC BITS/CHAR BY 1 BIT
1812  005064  022737  001400  001142    73800          CMP     #1400,BPC               ;HAVE ALL CHAR SEIZES BEEN TESTED
1813  005072  001226                    73900          BNE     1$                      ;NO
1814  005074  104400                    74000          SCOPE
1815                                    74100
1816                                    74200    ;********SYNC EXTENSION TEST***********
1817                                    74300
1818                                             ;*************
1819                                             ;             *
1820                                             ; TEST 27
1821                                             ;             *
1822                                             ;*************
1823                                             ;*********************************************************************
1824  005076  012737  000027  001072            TST27: MOV     #27,TSTNO
1825  005104  012737  005510  001062                   MOV     #TST30,NEXT
1826  005112  032737  000400  001134    74500          BIT     #BIT8,SAVSR1            ;DOES TWELVE BIT OPTION EXIST
1827  005120  001005                    74600          BNE     1$                      ;BRANCH IF NOT
1828  005122  013737  001062  001060    74700          MOV     NEXT,RETURN
1829  005130  000177  173726            74800          JMP     @NEXT
1830  005134  012777  002104  174070    74900    1$:   MOV     #2104,@DPRS             ;SET STATUS TO 12 BITS/CHARACTER
1831  005142  012737  000400  001144    75000          MOV     #400,TSYNC              ;FIRST SYNC CHARACTER
1832  005150  105077  174062            75100          CLRB    @SYNC                   ;LOAD SYNC BUFFERS WITH 400
1833  005154  112777  000001  174062    75200          MOVB    #1,@SEXT                ;LOAD SYNC BUFFERS WITH 400
1834  005162  012737  007400  001140    75300          MOV     #7400,SLIM              ;SET UP SYNC LIMIT
1835  005170  012737  002000  001142    75400          MOV     #2000,BPC               ;SET # BITS/CHAR TO 12
1836  005176  012777  014504  174042    75500    2$:   MOV     #FRINT,@DPRIV           ;RCV INTERRUPT VECTOR = ERROR
1837  005204  104403  006000            75600          DELAY   .6000                   ;WAIT FOR ALL 1'S
1838                                    75700                                          ;TO SHIFT INTO XMIT,RCV BUFS
1839  005210  105077  174022            75800          CLRB    @SYNC                   ;CLEAR SYNC EXTENTION
1840  005214  113777  001145  174022    75900          MOVB    TSYNC+1,@SEXT           ;LOAD NEXT SYNC
1841  005222  013777  001144  174012    76000          MOV     TSYNC,@DPTB             ;TRANSMIT FIRST SYNC
```

```
 1842  005230  105777  174004          76100          TSTB    @DPTS           ;WAIT FOR "DONE"
 1843  005234  100375                  76200          BPL     .-4             ;
 1844  005236  032777  004000  173774  76300          BIT     #BIT11,@DPTS    ;TEST FOR PREMATURE "ACTIVE"
 1845  005244  001401                  76400          BEQ     .+4             ;NO
 1846  005246  104000                  76500          HLT                     ;REPORT ERROR
 1847  005250  013777  001144  173764  76600          MOV     TSYNC,@DPTB     ;TRANSMIT SECOND SYNC
 1848  005256  105777  173756          76700          TSTB    @DPTS           ;WAIT FOR "DONE"
 1849  005262  100375                  76800          BPL     .-4             ;
 1850  005264  012777  005334  173754  76900          MOV     #3$,@DPRIV      ;SET UP RECEIVER INT VECTOR
 1851  005272  052777  000100  173732  77000          BIS     #BIT6,@DPRS     ;RCV INTERRUPT ENABLE
 1852  005300  013777  001144  173734  77100          MOV     TSYNC,@DPTB     ;TRANSMIT 3ED SYNC AS DATA
 1853  005306  105777  173726          77200          TSTB    @DPTS           ;WAIT FOR "DONE"
 1854  005312  100375                  77300          BPL     .-4             ;
 1855  005314  032777  004000  173710  77400          BIT     #BIT11,@DPRS    ;TEST FOR ACTIVE
 1856  005322  001001                  77500          BNE     .+4             ;OK
 1857  005324  104000                  77600          HLT                     ;REPORT ERROR
 1858  005326  104403  013560          77700          DELAY   .6000.          ;WAIT FOR INTERRUPT
 1859  005332  104004                  77800          HLT     4               ;DEVICE FAILED TO INTERRUPT
 1860  005334  017737  177674  001136  77900  3$:     MOV     @DPRB,TMPDAT    ;SAVE RECEIVED DATA
 1861  005342  013700  001144          78000          MOV     TSYNC,R0
 1862  005346  013701  001136          78100          MOV     TMPDAT,R1
 1863  005352  023737  001144  001136  78200          CMP     TSYNC,TMPDAT    ;COMPARE SYNC
 1864  005360  001401                  78300          BEQ     .+4             ;BRANCH IF SYNC OK
 1865  005362  104001                  78400          HLT     1               ;REPORT ERROR
 1866  005364  022626                  78500          POP.SP                  ;ADJUST STACK
 1867  005366  042737  000040  177776  78600          BIC     #BIT5,PS        ;LOWER PRIORITY
 1868  005374  042777  004000  173630  78700          BIC     #BIT11,@DPRS    ;CLEAR ACTIVE
 1869  005402  042777  000100  173622  78800          BIC     #BIT6,@DPRS     ;CLEAR INT ENB
 1870  005410  032737  040000  177570  78900          BIT     #BIT14,SWR      ;TEST FOR SCOPE LOOP
 1871  005416  001002                  79000          BNE     4$              ;BRANCH AROUND INC IF SCOPE
 1872  005420  105237  001145          79100          INCB    TSYNC+1         ;INC TO NEXT TEST SYNC
 1873  005424  123737  001145  001141  79200  4$:     CMPB    TSYNC+1,SLIM+1  ;HAVE ALL SYNC'S BEEN TESTED
 1874  005432  001404                  79300          BEQ     5$              ;YES
 1875  005434  112777  000026  173574  79400          MOVB    #26,@SYNC
 1876  005442  000655                  79500          BR      2$
 1877  005444  005037  001144          79600  5$:     CLR     TSYNC           ;CLEAR TSYNC
 1878  005450  006237  001140          79700          ASR     SLIM            ;DECREASE SYNC LIMIT
 1879  005454  043777  001142  173550  79800          BIC     BPC,@DPRS       ;CLEAR OLD CHAR SIZE
 1880  005462  062737  000400  001142  79900          ADD     #400,BPC        ;INC BITS/CHAR TO NEXT SIZE
 1881  005470  053777  001142  173534  80000          BIS     BPC,@DPRS       ;CHANGE BIT MODE
 1882  005476  022737  003400  001142  80100          CMP     #3400,BPC       ;CHECK CHARACTER SIZE
 1883  005504  001234                  80200          BNE     2$              ;BRANCH UNTIL ALL SIZES HAVE BEEN TESTED
 1884  005506  104400                  80300          SCOPE
 1885
```

```
                                    00100
                                    00200
                                    00300
                                    00400   ;*****************************************************************
                                    00500
                                    00600   ;IDLE SYNC TEST
                                    00700   ;
                                    00800   ;RAISE "ACTIVE" BY IDLEING IN EACH AVAILABLE CHARACTER LENGTH
                                    00900
                                            ;*************
                                            ;             *
                                            ; TEST 30
                                            ;             *
                                            ;*************
                                            ;*****************************************************************
1901  005510  012737  000030  001072        TST30:  MOV     #30,TSTNO
1902  005516  012737  006104  001362                MOV     #TST31,NEXT
1903  005524  012737  000026  001144  01100         MOV     #26,TSYNC               ;LOAD TEST SYNC CHARACTER
1904  005532  005077  173502          01200         CLR     @DPTS                   ;CLEAR STATUS REGISTERS
1905  005536  005077  173470          01300         CLR     @DPRS                   ;
1906  005542  013703  001232          01400         MOV     DPRS,R3                 ;FETCH DEVICE ADRS
1907  005546  005203                  01500         INC     R3                      ;CHANGE ADRS TO HIGH BYTE OF STATUS
1908  005550  052777  000004  173454  01600         BIS     #BIT2,@DPRS             ;START MAINTENANCE
1909  005556  012702  006062          01700         MOV     #6$,R2                  ;SET UP CHARACTER LENGTH SELECTOR
1910                                  01800
1911  005562  104403  013560          01900   1$:   DELAY   ,6000.                 ;WAIT FOR ALL 1'S TO SHIFT IN
1912  005566  012777  005640  173452  02000         MOV     #2$,@DPRIV              ;LOAD DP RCV INTERRUPT VECTOR
1913  005574  113777  001144  173434  02100         MOVB    TSYNC,@SYNC             ;LOAD LOW BYTE OF SYNC
1914  005602  113777  001145  173434  02200         MOVB    TSYNC+1,@SEXT           ;LOAD SYNC EXTENSION BITS
1915  005610  013777  001144  173424  02300         MOV     TSYNC,@DPTB             ;LOAD XMIT BUFFER
1916  005616  052777  000002  173414  02400         BIS     #BIT1,@DPTS             ;SET IDLE SYNC
1917  005624  052777  000100  173400  02500         BIS     #BIT6,@DPRS             ;SET RCV INTERRUPT ENABLE
1918                                  02600
1919  005632  104403  027340          02700         DELAY   ,12000.                 ;WAIT FOR RCV INTERRUPT
1920  005636  104004                  02800         HLT     4                       ;REPORT ERROR
1921  005640  017737  173370  001136  02900   2$:   MOV     @DPRB,TMPDAT            ;SAVE RCV DATA
1922  005646  000412                  03000   3$:   BR      4$                      ;CONTROL WORD 12 BITS=BR .+2
1923  005650  013700  001144          03100         MOV     TSYNC,R0
1924  005654  013701  001136          03200         MOV     TMPDAT,R1
1925  005660  023737  001136  001144  03300         CMP     TMPDAT,TSYNC            ;DOES SYNC CHECK
1926  005666  001401                  03400         BEQ     .+4                     ;YES
1927  005670  104001                  03500         HLT     1                       ;REPORT ERROR
1928  005672  000415                  03600         BR      5$
1929  005674  105737  001137          03700   4$:   TSTB    TMPDAT+1                ;VERIFY ONLY 8 BITS WERE TRANSMITTED
1930  005700  001401                  03800         BEQ     .+4                     ;BRANCH IF OK
1931  005702  104000                  03900         HLT                             ;REPORT ERROR
1932  005704  013700  001144          04000         MOV     TSYNC,R0
1933  005710  013701  001136          04100         MOV     TMPDAT,R1
1934  005714  123737  001136  001144  04200         CMPB    TMPDAT,TSYNC            ;CHECK SYNC IN LOW BYTE
1935  005722  001401                  04300         BEQ     .+4                     ;BRANCH IF SYNC OK
1936  005724  104001                  04400         HLT     1                       ;REPORT ERROR
1937  005726  105777  173300          04500   5$:   TSTB    @DPRS                   ;DID READING RCV BUFF CLR DONE
1938  005732  100001                  04600         BPL     .+4                     ;YES
1939  005734  104000                  04700         HLT                             ;REPORT ERROR
1940  005736  042777  004000  173266  04800         BIC     #BIT11,@DPRS            ;CLEAR ACTIVE
1941  005744  032777  004000  173260  04900         BIT     #BIT11,@DPRS            ;ACTIVE CLEARED
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 1942  005752  001401                    05000          BEQ     .+4                     ;YES
 1943  005754  104000                    05100          HLT                             ;REPORT ERROR
 1944  005756  042777  000302  173354    05200          BIC     #BIT1,@DPTS             ;CLEAR IDLE
 1945  005764  042737  000340  177776    05300          BIC     #BITS,PS                ;LOWER PRICRITY TO 4
 1946  005772  022626                    05400          POP.SP                          ;ADJUST STACK
 1947  005774  142213                    05500          BICB    (R2)+,@R3               ;CLEAR CHAR LENGTH
 1948  005776  152213                    05600          BISB    (R2)+,@R3               ;SELECT NEXT CHAR LENGTH
 1949  006000  020227  006066            05700          CMP     R2,#6$+4                ;END OF MODE?
 1950  006004  001366                    05800          BNE     1$                      ;NO
 1951  006006  032737  000400  001134    05900          BIT     #BIT8,SAVSR1            ;TEST 12 BITS/CHARACTER
 1952  006014  001424                    06000          BEQ     7$                      ;NO
 1953  006016  032777  002000  173206    06100          BIT     #BIT10,@DPRS            ;END OF 12 BIT TEST
 1954  006024  001020                    06200          BNE     7$                      ;YES
 1955  006026  052777  002000  173176    06300          BIS     #BIT10,@DPRS            ;NO
 1956  006034  024242                    06400          CMP     -(R2),-(R2)             ;ADJUST CHAR SELECTION
 1957  006036  042777  001400  173156    06500          BIC     #1400,@DPRS             ;CLEAR CHAR LENGTH LSB'S
 1958  006044  012737  000400  005646    06600          MOV     #400,3$                 ;CHANGE CONTROL WORD
 1959  006052  012737  001426  001144    06700          MOV     #1426,TSYNC             ;CHANGE SYNC
 1960  006060  000640                    06800          BR      1$
 1961  006062  000403                    06900     6$:  403                             ;CHARACTER LENGTH SELECTION
 1962  006064  001003                    07000          1003                            ;CHARACTER LENGTH SELECTION
 1963  006066  012737  000026  001144    07100     7$:  MOV     #26,TSYNC               ;RESTORE TSYNC
 1964  006074  012737  000412  005646    07200          MOV     #412,3$                 ;RESTORE CONTROL WORD
 1965  006102  104400                    07300          SCOPE
 1966                                    07400
 1967                                    07500
 1968                                    07600     ;******INTERRUPT DRIVEN SEQUENTIAL DATA TEST********
 1969                                    07700
 1970                                              ;*************
 1971                                              ;             *
 1972                                              ; TEST 31     
 1973                                              ;             *
 1974                                              ;*************
 1975                                              ;*************************************************************************
 1976  006104  012737  000031  001372              TST31:  MOV     #31,TSTNO
 1977  006112  012737  006316  001062                      MOV     #TST32,NEXT
 1978  006120  012737  006314  001174    07900             MOV     #3$,BACK
 1979  006126  105077  173112            08000             CLRB    @SEXT                   ;CLEAR SYNC EXTENTION
 1980  006132  005037  001154            08100             CLR     RDATA                   ;INIT RCV DATA
 1981  006136  005037  001152            08200             CLR     TDATA                   ;INIT XMIT DATA
 1982  006142  005077  173072            08300             CLR     @DPTS                   ;TRANSMITTER STATUS
 1983  006146  012777  000035  173056    08400             MOV     #5,@DPRS                ;CLOCK ON + STRIP SYNC
 1984  006154  012737  000400  001156    08500             MOV     #400,CHLEN              ;CHAR LENGTH INDEX
 1985  006162  032737  000400  001134    08600             BIT     #BIT8,SAVSR1            ;TEST 12 BIT CHAR MODE
 1986  006170  001414                    08700             BEQ     1$                      ;NO
 1987  006172  012737  010000  001160    08800             MOV     #10000,LIMIT            ;SELECT END OF DATA
 1988  006200  052777  002000  173024    08900             BIS     #BIT10,@DPRS            ;SELECT 12 BITS/CHARACTER
 1989  006206  012737  000426  001144    09000             MOV     #426,TSYNC              ;SYNC FOR 12 BIT CHAR
 1990  006214  105277  173024            09100             INCB    @SEXT                   ;PLACE MSB OF SYNC IN SYNC EXT
 1991  006220  000406                    09200             BR      2$
 1992  006222  012737  000400  001160    09300     1$:     MOV     #400,LIMIT              ;TEMPORARY CHARACTER LIMIT
 1993  006230  012737  000026  001144    09400             MOV     #26,TSYNC               ;INIT SYNC STORAGE
 1994  006236  012777  014510  173006    09500     2$:     MOV     #TV18,@DPTIV            ;TRANSMITTER VECTOR
 1995  006244  012777  014616  172774    09600             MOV     #RV18,@DPRIV            ;RECEIVER VECTOR
 1996  006252  012737  000200  177776    09700             MOV     #200,PS                 ;PRIORITY=4
 1997  006260  012737  000003  001162    09800             MOV     #3,SCNT                 ;SYNC COUNT=3
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 1998  006266  113777  001144  172742  09900          MOVB    TSYNC,@SYNC             ;LOAD SYNC
 1999  006274  052777  000100  172730  10000          BIS     #BIT6,@DPRS             ;RCV INT ENB
 2000  006302  052777  000340  172730  10100          BIS     #340,@DPTS              ;STATUS INT ENB
 2001                                  10200                                         ;TRANS INT ENB
 2002                                  10300                                         ;TRANS DONE
 2003  006310  000001                  10400          WAIT                            ;WAIT FOR INTERRUPTS
 2004  006312  000776                  10500          BR      .-2
 2005  006314  104400                  10600  3$:     SCOPE
 2006                                  10700
 2007                                  10800  ;******RANDOM DATA, RANDOM STALL********
 2008                                  10900
 2009                                  11000
 2010                                         ;*************
 2011                                         ;             *
 2012                                         ; TEST 32     
 2013                                         ;             *
 2014                                         ;*************
 2015                                         ;*********************************************************************
 2016  006316  012737  000032  001072         TST32:  MOV     #32,TSTNO
 2017  006324  012737  006442  001062                 MOV     #TST33,NEXT
 2018  006332  005037  001156          11200          CLR     CHLEN                   ;SET CHAR LENGTH TO 8 BITS
 2019  006336  012737  000026  001144  11300          MOV     #26,TSYNC               ;SYNC = 26
 2020  006344  113777  001144  172664  11400          MOVB    TSYNC,@SYNC             ;LOAD SYNC BUFFER
 2021  006352  004737  013060          11500          JSR     PC,AND                  ;EXECUTE DATA + STALL MODES
 2022                                  11600
 2023                                  11700  ;REPEAT PREVIOUS TEST AT 7 BITS/CHAR
 2024                                  11800
 2025  006356  012737  000200  001156  11900          MOV     #200,CHLEN              ;SET CHAR LENGTH TO 7 BITS
 2026  006364  052777  000400  172640  12000          BIS     #BIT8,@DPRS             ;7 BITS/CHAR
 2027  006372  042777  004000  172632  12100          BIC     #BIT11,@DPRS            ;CLEAR ACTIVE
 2028  006400  004737  013060          12200          JSR     PC,AND                  ;EXECUTE DATA + STALL MODES
 2029                                  12300
 2030                                  12400  ;REPEAT PREVIOUS TEST AT 6 BITS/CHAR
 2031                                  12500
 2032  006404  012737  000300  001156  12600          MOV     #300,CHLEN              ;SET CHAR LENGTH TO 6 BITS
 2033  006412  042777  000400  172612  12700          BIC     #BIT8,@DPRS
 2034  006420  052777  001000  172604  12800          BIS     #BIT9,@DPRS             ;SET MODE TO 6 BITS/CHAR
 2035  006426  042777  004000  172576  12900          BIC     #BIT11,@DPRS            ;CLEAR ACTIVE
 2036                                  13000
 2037  006434  004737  013060          13100          JSR     PC,AND                  ;EXECUTE DATA & STALL MODES
 2038  006440  104400                  13200          SCOPE
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2039                                    13400   ;******PARITY TEST******
2040                                    13500
2041                                    13600   ;VERIFY "PARITY" BIT=1 FOR ODD PARITY AND=0 FOR EVEN
2042                                    13700
2043                                            ;*************
2044                                            ;            *
2045                                            ; TEST 33
2046                                            ;            *
2047                                            ;*************
2048                                            ;*************************************************************************
2049  006442  012737  000033  001072            TST33:  MOV     #33,TSTNO
2050  006450  012737  006646  001062                    MOV     #TST34,NEXT
2051  006456  012737  006644  001174  13900             MOV     #2$,BACK
2052  006464  005077  172542          14000             CLR     @DPRS
2053  006470  005077  172544          14100             CLR     @DPTS
2054  006474  012737  001401  015422  14200             MOV     #1401,RPRT1     ;LOAD RPRT2WITH BEQ .+4
2055  006502  012737  000400  001160  14300             MOV     #400,LIMIT      ;SET UP CHARACTER LIMIT
2056  006510  005037  001154          14400             CLR     RDATA           ;CLR RCV DATA
2057  006514  005037  001152          14500             CLR     TDATA           ;CLR XMIT DATA
2058  006520  105077  172520          14600             CLRB    @SEXT           ;CLEAR SYNC EXTENTION
2059  006524  012737  000026  001144  14700             MOV     #26,TSYNC       ;SET UP SYNC
2060  006532  113777  001144  172476  14800             MOVB    TSYNC,@SYNC     ;INIT SYNC
2061  006540  012737  000003  001162  14900             MOV     #3,SCNT         ;3 SYNC'S
2062  006546  005077  172460          15000             CLR     @DPRS           ;CLR RECEIVER STATUS
2063  006552  005077  172462          15100             CLR     @DPTS           ;CLR TRANSMITTER STATUS
2064  006556  032737  000400  001134  15200             BIT     #BIT8,SAVSR1    ;8/12 BITS/CHAR
2065  006564  001406                  15300             BEQ     1$              ;BRANCH IF 8 BITS/CHAR
2066  006566  012737  010000  001160  15400             MOV     #10000,LIMIT    ;SET LIMIT TO 12 BITS/CHAR
2067  006574  052777  002000  172430  15500             BIS     #BIT10,@DPRS    ;SELECT 12 BIT MODE
2068  006602  012737  000200  177776  15600   1$:       MOV     #200,PS         ;PRIORITY = 4
2069  006610  012777  015266  172434  15700             MOV     #TPRTY,@DPTIV   ;TRANSMITTER PARITY TEST VECTOR
2070  006616  012777  015356  172422  15800             MOV     #RPRTY,@DPRIV   ;RECEIVER PARITY TEST VECTOR
2071  006624  052777  000105  172400  15900             BIS     #105,@DPRS      ;RCV INT ENB, STRIP SYNC, CLOCK
2072  006632  052777  000300  172400  16000             BIS     #300,@DPTS      ;XMIT INT ENB,DONE
2073  006640  000001                  16100             WAIT
2074  006642  000776                  16200             BR      .-2
2075  006644  104400                  16300   2$:       SCOPE
2076                                    16400
2077                                    16500   ;RECEIVER OVERRUN TST
2078                                    16600
2079                                            ;*************
2080                                            ;            *
2081                                            ; TEST 34
2082                                            ;            *
2083                                            ;*************
2084                                            ;*************************************************************************
2085  006646  012737  000034  001072            TST34:  MOV     #34,TSTNO
2086  006654  012737  007104  001062                    MOV     #TST35,NEXT
2087  006662  005037  001136          16800             CLR     TMPDAT          ;STOR TEST CHAR IN TMPDAT
2088  006666  105077  172352          16900             CLRB    @SEXT           ;CLEAR SYNC EXTENTION
2089  006672  112777  000026  172336  17000             MOVB    #26,@SYNC       ;LOAD SYNC BUFFER
2090  006700  032737  000400  001134  17100             BIT     #BIT8,SAVSR1    ;8/12 BITS/CHAR
2091  006706  001403                  17200             BEQ     1$              ;BRANCH IF 8 BITS/CHAR
2092  006710  012777  002000  172314  17300             MOV     #BIT10,@DPRS    ;SELECT 12 BITS/CHAR
2093  006716  012777  007040  172326  17400   1$:       MOV     #3$,@DPTIV      ;XMIT STATUS INT VECTOR=0'RUN
2094  006724  052777  000004  172300  17500             BIS     #BIT2,@DPRS     ;TURN ON CLOCK
```

```
2095  006732  104403  013560          17600   2$:     DELAY   ,6000.          ;WAIT FOR BCV TO CLEAR
2096  006736  052777  000200  172274  17700           BIS     #BIT7,@DPTS     ;DONE
2097  006744  105777  172270          17800           TSTB    @DPTS           ;TRANSMIT FIRST SYNC
2098  006750  100375                  17900           BPL     .-4
2099  006752  012777  000026  172262  18000           MOV     #26,@DPTB
2100  006760  105777  172254          18100           TSTB    @DPTS
2101  006764  100375                  18200           BPL     .-4
2102  006766  012777  000026  172246  18300           MOV     #26,@DPTB       ;TRANSMIT SECOND SYNC
2103  006774  105777  172240          18400           TSTB    @DPTS
2104  007000  100375                  18500           BPL     .-4
2105  007002  013777  001136  172232  18600           MOV     TMPDAT,@DPTB    ;TRANSMIT DATA CHAR #1
2106  007010  105777  172224          18700           TSTB    @DPTS
2107  007014  100375                  18800           BPL     .-4
2108  007016  013777  001136  172216  18900           MOV     TMPDAT,@DPTB    ;TRANSMIT DATA CHAR #2
2109  007024  052777  000040  172206  19000           BIS     #BIT5,@DPTS     ;SET STATUS INT ENB
2110  007032  104403  005670          19100           DELAY   .3000.          ;WAIT FOR O'RUN INTERRUPT
2111  007036  104000                  19200           HLT                     ;REPORT ERROR, NO O'RUN INT
2112  007040  032777  040000  172172  19300   3$:     BIT     #BIT14,@DPTS    ;TEST FOR O'RUN
2113  007046  001001                  19400           BNE     .+4             ;BRANCH IF O'RUN CAUSED INT
2114  007050  104000                  19500           HLT                     ;REPORT ERROR
2115  007052  005077  172162          19600           CLR     @DPTS           ;CLEAR XMIT STATUS
2116  007056  042777  004000  172146  19700           BIC     #BIT11,@DPRS    ;CLEAR ACTIVE
2117  007064  022626                  19800           POP.SP                  ;ADJUST STACK
2118  007066  042737  000040  177776  19900           BIC     #BIT5,PS        ;LOWER PRIORITY TO 4
2119  007074  105237  001136          20000           INCB    TMPDAT          ;INC TO NEXT DATA
2120  007100  001314                  20100           BNE     2$              ;BRANCH IF NOT END
2121  007102  104400                  20200           SCOPE
2122                                  20300
2123                                  20400
2124                                  20500   ;HALF DUPLEX TEST
2125                                  20600
2126                                          ;*************
2127                                          ;           *
2128                                          ; TEST 35
2129                                          ;           *
2130                                          ;*************
2131                                          ;*************************************************************************
2132  007104  012737  000035  001072          ST35:   MOV     #35,TSTNO
2133  007112  012737  007306  001062                  MOV     #TST36,NEXT
2134  007120  005077  172114          20800           CLR     @DPTS           ;CLEAR TRANSMITTER STATUS
2135  007124  012777  000103  172100  20900           MOV     #103,@DPRS      ;HALF DUPLEX,INT EN,TURN CLK ON
2136  007132  012777  014504  172106  21000           MOV     #FRINT,@DPRIV   ;SETUP TEST VECTOR
2137  007140  005037  001144          21100           CLR     TSYNC           ;CLR TEST SYNC
2138  007144  012737  000200  177776  21200           MOV     #200,PS         ;PRIORITY=4
2139  007152  113777  001144  172056  21300   1$:     MOVB    TSYNC,@SYNC     ;LOAD SYNC BUFFER
2140  007160  052777  000002  172052  21400           BIS     #BIT1,@DPTS     ;IDLE SYNC
2141  007166  104403  005670          21500           DELAY   .3000.          ;DELAY 20.1 MS
2142  007172  105237  001144          21600           INCB    TSYNC           ;HAVE ALL SYNC BEEN TESTED
2143  007176  001365                  21700           BNE     1$              ;NO
2144  007200  104400                  21800           SCOPE
2145                                  21900   ;NOTE END OF THIS TEST.
```

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2146                                                    22100
2147                                                    22200   ;******PART2 DB25S CONNECTOR TEST SECTION******
2148  007202  000005                                    22300   BEGIN2: RESET
2149  007204  012737  177777  001150                    22400           MOV     #-1,CABLE
2150  007212  012706  001050                            22500           MOV     #STACK,SP       ;SET UP STACK POINTER
2151  007216  012737  000340  177776                    22600           MOV     #340,PS         ;SET PROCESSOR PRICRITY = 7
2152  007224  105737  177570                            22700           TSTB    SWR             ;TEST FOR CHANGE IN DP ADRS
2153  007230  100005                                    22800           BPL     BGNOA           ;BRANCH IF NO CHANGE
2154  007232  004737  012462                            22900           JSR     PC,CLRVEC       ;LOAD ENTIRE VECTOR AREA WITH
2155                                                    23000                                   ; .+2
2156                                                    23100                                   ; HALT
2157  007236  004737  012202                            23200           JSR     PC,LINE.N       ;FETCH LINE NUMBER FROM SWR
2158  007242  000404                                    23300           BR      PART2
2159  007244  004737  012462                            23400   BGNOA:  JSR     PC,CLRVEC
2160  007250  004737  012246                            23500           JSR     PC,LINE.X
2161  007254  032737  000001  001134                    23600   PART2:  BIT     #BIT0,SAVSR1
2162  007262  001405                                    23700           BEQ     1$
2163  007264  012737  011770  001060                    23800           MOV     #PART3,RETURN
2164  007272  000177  171562                            23900           JMP     @RETURN
2165  007276  012737  007254  001060                    24000   1$:     MOV     #PART2,RETURN
2166  007304  000240                                    24100           NOP
2167                                                    24200
2168                                                    24300
2169                                                    24400
2170                                                    24500   ;******TEST 1: CABLE TESTS
2171                                                    24600
2172                                                            ;*************
2173                                                            ;             *
2174                                                            ; TEST 36
2175                                                            ;             *
2176                                                            ;*************
2177                                                            ;*************************************************************************
2178  007306  012737  000036  001072                            TST36:  MOV     #36,TSTNO
2179  007314  012737  007436  001062                            MOV     #TST37,NEXT
2180  007322  005737  001150                    24800           TST     CABLE
2181  007326  001013                            24900           BNE     1$
2182  007330  032737  000001  001134            25000           BIT     #BIT0,SAVSR1
2183  007336  001405                            25100           BEQ     .+14
2184  007340  012737  011770  001060            25200           MOV     #PART3,RETURN
2185  007346  000177  171506                    25300           JMP     @RETURN
2186  007352  000137  015750                    25400           JMP     .EOP
2187  007356  112777  000026  171652            25500   1$:     MOVB    #26,@SYNC               ;CLEAR NOISE FROM SYNC
2188  007364  005077  171650                    25600           CLR     @DPTS                   ;CLEAR TRANSMITTER STATUS
2189  007370  105077  171650                    25700           CLRB    @SEXT                   ;CLEAR SYNC EXT
2190  007374  005077  171632                    25800           CLR     @DPRS                   ;CLEAR RECEIVER STATUS
2191  007400  012777  014500  171644            25900           MOV     #FTINT,@DPTIV           ;SET UP TRANSMITTER TEST VECTOR 1
2192  007406  012777  014504  171632            26000           MOV     #FRINT,@DPRIV           ;SET UP RECEIVER TEST VECTOR 1
2193  007414  012777  000240  171626            26100           MOV     #240,@DPRP              ;SET UP RECEIVER PRIORITY=6
2194  007422  012777  000240  171624            26200           MOV     #240,@DPTP              ;SET UP TRANSMITTER PRIORITY=6
2195  007430  104401                            26300           CLOCK                           ;RUN CLOCK
2196  007432  000030                            26400           30
2197  007434  104400                            26500           SCOPE
2198                                            26600
2199                                            26700   ;SYNCHRONIZATION CHARACTER TEST 8/12 BITS CHARACTER
2200                                            26800   ;INTERRUPT ENABLE, COMPARE SYNC, TEST PARITY
2201                                            26900
```

```
2202                                    27000
2203                                    ;*************
2204                                    ;             *
2205                                    ; TEST 37     
2206                                    ;             *
2207                                    ;*************
2208                                    ;*********************************************************************
2209  007436  012737  000037  001072    TST37:  MOV     #37,TSTNO
2210  007444  012737  007726  001062            MOV     #TST40,NEXT
2211  007452  004537  013472    27200           JSR     R5,REE                  ;REINIT FOR TEST
2212  007456  012737  000376  001160  27300     MOV     #376,LIMIT              ;8 BIT SYNC LIMIT
2213  007464  000403            27400           BR      .+10                    ;BRANCH AROUND 12 BIT LIMIT
2214                            27500   ;REE WILL ENER HERE IF 12 BITS/CHAR
2215  007466  012737  007776  001160  27600     MOV     #7776,LIMIT             ;SET UP 12 BITS/CHAR LIMIT
2216  007474  012737  007656  001174  27700     MOV     #2$,BACK                ;SET UP RCV SERVICE RETURN
2217  007502  012777  014510  171542  27800  1$:MOV     #TV18,@DPTIV            ;SET XMIT INT VECTOR TO SYNC
2218  007510  012737  000003  001162  27900     MOV     #3,SCNT                 ;SYNC COUNT = 3
2219                            28000
2220  007516  104401            28100           CLOCK                           ;RUN CLOCK
2221  007520  000030            29200           30
2222  007522  113777  001144  171506  28300     MOVB    TSYNC,@SYNC             ;LOAD SYNC BUFFER
2223  007530  113777  001145  171506  28400     MOVB    TSYNC+1,@SEXT           ;LOAD SYNC EXT
2224  007536  052777  000100  171466  28500     BIS     #BIT6,@DPRS             ;RCV INT ENB
2225  007544  052777  000300  171466  28600     BIS     #300,@DPTS              ;XMIT INT ENB
2226  007552  104402            28700           RXCLK
2227  007554  000003            28800           3
2228  007556  032777  001000  171454  28900     BIT     #BIT9,@DPTS             ;SEND REQUEST UP?
2229  007564  001001            29000           BNE     .+4                     ;YES
2230  007566  104000            29100           HLT                             ;REPORT ERROR
2231  007570  104401            29200           CLOCK                           ;RUN CLOCK
2232  007572  000010            29300           10
2233  007574  032777  004000  171430  29400     BIT     #BIT11,@DPRS            ;RECEIVER ACTIVE
2234  007602  001401            29500           BEQ     .+4                     ;NO
2235  007604  104000            29600           HLT                             ;REPORT ERROR
2236  007606  104401            29700           CLOCK                           ;RUN CLOCK
2237  007610  000007            29800           7
2238  007612  032777  004000  171420  29900     BIT     #BIT11,@DPTS            ;RCV    ACTIVE?
2239  007620  001401            30000           BEQ     .+4                     ;NO
2240  007622  104000            30100           HLT                             ;REPORT ERROR
2241  007624  104402            30200           RXCLK
2242  007626  000001            30300           1
2243  007630  032777  004000  171374  30400     BIT     #BIT11,@DPRS            ;RCV ACTIVE?
2244  007636  001001            30500           BNE     .+4                     ;YES
2245  007640  104000            30600           HLT                             ;REPORT ERROR
2246  007642  012777  015570  171376  30700     MOV     #SRV5,@DPRIV            ;TEST PASS VECTOR
2247  007650  104401            30800           CLOCK                           ;RUN CLOCK
2248  007652  000010            30900           10
2249  007654  104000            31000           HLT                             ;REPORT ERROR
2250  007656  042777  004000  171346  31100  2$:BIC     #BIT11,@DPRS            ;CLEAR ACTIVE
2251  007664  042777  000100  171346  31200     BIC     #BIT6,@DPTS             ;CLEAR INT ENB
2252  007672  032737  040000  177570  31300     BIT     #BIT14,SWR              ;TEST FOR SCOPE LOOP
2253  007700  001300            31400           BNE     1$                      ;BRANCH IF SCOPE LOOP
2254  007702  112777  000026  171326  31500     MOVB    #26,@SYNC               ;CHANGE SYNC
2255  007710  005237  001144            31600     INC     TSYNC                   ;NEXT SYNC, ENTRY FROM INTERRUPT
2256  007714  023737  001160  001144  31700     CMP     LIMIT,TSYNC             ;HAVE ALL SYNC'S BEEN TESTED
2257  007722  001267            31800           BNE     1$
```

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2258  007724  104400                    31900          SCOPE
2259                                    32000
2260                                    32100    ;SYNCHRONIZATION CHARACTER TEST 7/11 BITS/CHARACTER
2261                                    32200    ;INTERRUPT ENABLE AND SYNC CHARACTER CHECK
2262                                    32300
2263                                    32400
2264                                             ;*************
2265                                             ;            *
2266                                             ; TEST 40
2267                                             ;            *
2268                                             ;*************
2269                                             ;*****************************************************************************
2270  007726  012737  000040  001072             TST40:  MOV     #40,TSTNO
2271  007734  012737  010224  001062                     MOV     #TST41,NEXT
2272  007742  004537  013472            32600            JSR     R5,REE                  ;REINIT  DP11
2273                                    32700    ;RETURN HERE IF 8 BITS/CHAR
2274  007746  012737  000176  001160    32800            MOV     #176,LIMIT              ;7 BIT LIMIT
2275  007754  000403                    32900            BR      .+10                    ;BRANCH AROUND 12 BITS/CHAR LIMIT
2276                                    33000    ;RTETURN HERE IF 12 BITS/CHAR
2277  007756  012737  003776  001160    33100            MOV     #3776,LIMIT             ;11 BITS/CHAR LIMIT
2278  007764  052777  000400  171240    33200            BIS     #BIT8,@DPRS             ;7/11 BITS PER CHAR
2279  007772  012737  010154  001174    33300            MOV     #2$,BACK                ;SET UP RCV SERVICE RETURN
2280  010000  012777  014504  171240    33400            MOV     #FRINT,@DPRIV           ;FALSE INT TEST VECTOR
2281  010006  012777  014510  171236    33500    1$:     MOV     #TV18,@DPTIV            ;SET XMIT INT VECTOR TO SYNC
2282  010014  012737  000003  001162    33600            MOV     #3,SCNT                 ;XMIT 3 SYNCS
2283  010022  104401                    33700            CLOCK                           ;RUN CLOCK
2284  010024  000024                    33800            24
2285  010026  113777  001144  171202    33900            MOVB    TSYNC,@SYNC             ;LOAD SYNC BUFFER
2286  010034  052777  000300  171176    34000            BIS     #300,@DPTS              ;XMIT INT ENB
2287  010042  052777  000100  171162    34100            BIS     #BIT6,@DPRS             ;RCINT ENB
2288  010050  104402                    34200            RXCLK
2289  010052  000003                    34300            3
2290  010054  032777  001000  171156    34400            BIT     #BIT9,@DPTS             ;SEND REQUEST UP?
2291  010062  001001                    34500            BNE     .+4
2292  010064  104000                    34600            HLT                             ;REPORT ERROR
2293  010066  104401                    34700            CLOCK                           ;RUN CLOCK
2294  010070  000007                    34800            7
2295  010072  032777  004000  171132    34900            BIT     #BIT11,@DPRS            ;RECEIVER ACTIVE
2296  010100  001401                    35000            BEQ     .+4                     ;NO
2297  010102  104000                    35100            HLT                             ;REPORT ERROR
2298  010104  104401                    35200            CLOCK                           ;RUN CLOCK
2299  010106  000006                    35300            6
2300  010110  032777  004000  171122    35400            BIT     #BIT11,@DPTS            ;RCV ACTIVE?
2301  010116  001401                    35500            BEQ     .+4                     ;NO
2302  010120  104000                    35600            HLT                             ;REPORT ERROR
2303  010122  104402                    35700            RXCLK
2304  010124  000001                    35800            1
2305  010126  032777  004000  171076    35900            BIT     #BIT11,@DPRS            ;RCV ACTIVE?
2306  010134  001001                    36000            BNE     .+4                     ;YES
2307  010136  104000                    36100            HLT                             ;REPORT ERROR
2308  010140  012777  015570  171100    36200            MOV     #SRV5,@DPRIV            ;TEST PASS VECTOR
2309  010146  104401                    36300            CLOCK                           ;RUN CLOCK
2310  010150  000007                    36400            7
2311  010152  104000                    36500            HLT                             ;REPORT ERROR
2312  010154  042777  004000  171050    36600    2$:     BIC     #BIT11,@DPRS            ;CLEAR RCV ACTIVE
2313  010162  042777  000100  171050    36700            BIC     #BIT6,@DPTS             ;CLEAR XMIT INT ENB
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 2314  010170  112777  000026  171040  36800          MOVB    #26,@SYNC               ;DUMMY SYNC
 2315  010176  032737  040000  177570  36900          BIT     #BIT14,SWR              ;TEST FOR SCOPE LOOP
 2316  010204  001300                  37000          BNE     1$                      ;BRANCH IF SCOPE
 2317  010206  005237  001144          37100          INC     TSYNC                   ;NEXT SYNC
 2318  010212  023737  001160  001144  37200          CMP     LIMIT,TSYNC             ;HAVE ALL SYNC'S BEEN TESTED
 2319  010220  001272                  37300          BNE     1$
 2320  010222  104400                  37400          SCOPE
 2321                                  37500
 2322                                  37600  ;SYNCHRONIZATION CHARACTER TEST 6/10 BITS/CHARACTER
 2323                                  37700  ;INTERRUPT ENABLE AND SYNC CHARACTER CHECK
 2324                                  37800
 2325                                  37900
 2326                                         ;*************
 2327                                         ;            *
 2328                                         ; TEST 41
 2329                                         ;            *
 2330                                         ;*************
 2331                                         ;*****************************************************************
 2332  010224  012737  000041  001072         TST41:  MOV     #41,TSTNO
 2333  010232  012737  010530  001062                 MOV     #TST42,NEXT
 2334  010240  004537  013472          38100          JSR     R5,REE                  ;REINIT DP11
 2335  010244  012737  000075  001160  38200          MOV     #75,LIMIT               ;6 BIT LIMIT
 2336  010252  000403                  38300          BR      .+10                    ;BRANCH AROUND 10 BIT LIMIT
 2337                                  38400  ;RETURN HERE IF 10 BITS/CHAR
 2338  010254  012737  001775  001160  38500          MOV     #1775,LIMIT             ;SET UP 10 BITS/CHAR
 2339  010262  052777  001000  170742  38600          BIS     #BIT9,@DPRS             ;6/10 BITS/CHAR
 2340  010270  012737  010466  001174  38700          MOV     #2$,BACK                ;SET UP RCV SERVICE RETURN
 2341  010276  012777  014510  170746  38800  1$:     MOV     #TV18,@DPTIV            ;SET XMIT INT VECTOR TO SYNC
 2342  010304  012737  000003  001162  38900          MOV     #3,SCNT                 ;XMIT 3 SYNCS
 2343  010312  042777  000100  170720  39000          BIC     #BIT6,@DPTS             ;CLEAR XMIT INT ENB
 2344  010320  042777  004000  170704  39100          BIC     #BIT11,@DPRS            ;CLEAR ACTIVE
 2345  010326  112777  000026  170702  39200          MOVB    #26,@SYNC               ;CHALGE SYNC
 2346  010334  104401                  39300          CLOCK                           ;RUN CLOCK
 2347  010336  000021                  39400          21
 2348  010340  113777  001144  170670  39500          MOVB    TSYNC,@SYNC             ;LOAD SYNC BUFFER
 2349  010346  052777  000100  170656  39600          BIS     #BIT6,@DPRS             ;RCVINT ENB
 2350  010354  052777  000300  170656  39700          BIS     #300,@DPTS              ;XMIT INT ENB
 2351  010362  104402                  39800          RXCLK
 2352  010364  000003                  39900          3
 2353  010366  032777  001000  170644  40000          BIT     #BIT9,@DPTS             ;SEND REQUEST UP?
 2354  010374  001001                  40100          BNE     .+4
 2355  010376  104000                  40200          HLT                             ;REPORT ERROR
 2356  010400  104401                  40300          CLOCK                           ;RUN CLOCK
 2357  010402  000006                  40400          6
 2358  010404  032777  004000  170620  40500          BIT     #BIT11,@DPRS            ;RECEIVER ACTIVE
 2359  010412  001401                  40600          BEQ     .+4                     ;NO
 2360  010414  104000                  40700          HLT                             ;REPORT ERROR
 2361  010416  104401                  40800          CLOCK                           ;RUN CLOCK
 2362  010420  000005                  40900          5
 2363  010422  032777  004000  170610  41000          BIT     #BIT11,@DPTS            ;RCV ACTIVE?
 2364  010430  001401                  41100          BEQ     .+4                     ;NO
 2365  010432  104000                  41200          HLT                             ;REPORT ERROR
 2366  010434  104402                  41300          RXCLK
 2367  010436  000001                  41400          1
 2368  010440  032777  004000  170564  41500          BIT     #BIT11,@DPRS            ;RCV ACTIVE?
 2369  010446  001001                  41600          BNE     .+4                     ;YES
```

```
2370  010450  104000                    41700          HLT                             ;REPORT ERROR
2371  010452  012777  015570  170566    41800          MOV     #SRV5,@DPRIV            ;TEST VECTOR
2372  010460  104401                    41900          CLOCK                           ;RUN CLOCK
2373  010462  000006                    42000          6
2374  010464  104000                    42100          HLT                             ;REPORT ERROR
2375                                     42200
2376  010466  042777  004000  170536    42300  2$:     BIC     #BIT11,@DPRS
2377  010474  112777  000026  170534    42400          MOVB    #26,@SYNC
2378  010502  032737  040000  177570    42500          BIT     #BIT14,SWR              ;TEST FOR SCOPE LOOP
2379  010510  001272                    42600          BNE     1$                      ;BRANCH IF SCOPE
2380  010512  005237  001144            42700          INC     TSYNC                   ;NEXT SYNC
2381  010516  023737  001160  001144    42800          CMP     LIMIT,TSYNC             ;HAVE ALL SYNC'S BEEN TESTED
2382  010524  001264                    42900          BNE     1$
2383  010526  104400                    43000          SCOPE
2384                                     43100
2385                                     43200  ;INTERRUPT DRIVEN SEQUENTIAL DATA TEST
2386                                     43300
2387                                            ;*************
2388                                            ;            *
2389                                            ; TEST 42
2390                                            ;            *
2391                                            ;*************
2392                                            ;*************************************************************************
2393  010530  012737  000042  001072            TST42:  MOV     #42,TSTNO
2394  010536  012737  010552  001062                    MOV     #TST43.NEXT
2395  010544  004737  014000            43500          JSR     PC,SEQ.DATA     ;DO THE TEST.
2396  010550  104400                    43600          SCOPE
2397                                     43700
2398                                     43800  ;*************************************************************
2399                                     43900
2400                                     44000  ;RANDOM DATA RANDOM IDLE
2401                                     44100
2402                                     44200
2403                                            ;*************
2404                                            ;            *
2405                                            ; TEST 43
2406                                            ;            *
2407                                            ;*************
2408                                            ;*************************************************************************
2409  010552  012737  000043  001072            TST43:  MOV     #43,TSTNO
2410  010560  012737  010730  001062                    MOV     #TST44,NEXT
2411  010566  005077  170446            44400          CLR     @DPTS
2412  010572  005077  170434            44500          CLR     @DPRS
2413  010576  105077  170442            44600          CLRB    @SEXT                   ;CLEAR SYNC EXTENTION
2414  010602  012737  177400  001156    44700          MOV     #177400,CHLEN           ;SET CHAR LENGTH TO 8 BITS
2415  010610  012737  000026  001144    44800          MOV     #26,TSYNC               ;SYNC = 26
2416  010616  113777  001144  170412    44900          MOVB    TSYNC,@SYNC             ;LOAD SYNC BUFFER
2417  010624  012701  015371            45000          MOV     #15371,R1               ;PRIME RANDOM # GEN
2418  010630  012702  072414            45100          MOV     #72 14,R2
2419  010634  012703  004036            45200          MOV     #4036,R3
2420  010640  004737  013562            45300          JSR     PC,A2ND
2421                                     45400
2422                                     45500  ;REPEAT PREVIOUS TEST AT 7 BITS/CHAR
2423                                     45600
2424                                     45700
2425  010644  012737  177600  001156    45800          MOV     #177600,CHLEN           ;SET CHAR LENGHT TO 7 BITS
```

```
2426  010652  052777  000400  170352  45900          BIS     #BIT8,@DPRS             ;7 BITS/CHAR
2427  010660  042777  004000  170344  46000          BIC     #BIT11,@DPRS            ;CLEAR ACTIVE
2428  010666  004737  013562          46100          JSR     PC,A2ND
2429                                  46200
2430                                  46300  ;REPEAT PREVIOUS TEST AT 6 BITS/CHAR
2431                                  46400
2432  010672  012737  177700  001156  46500          MOV     #177700,CHLEN           ;SET CHAR LENGTH TO 6 BITS
2433  010700  042777  000400  170324  46600          BIC     #BIT8,@DPRS
2434  010706  052777  001000  170316  46700          BIS     #BIT9,@DPRS             ;SET MODE TO 6 BITS/CHAR
2435  010714  042777  004000  170310  46800          BIC     #BIT11,@DPRS            ;CLEAR ACTIVE
2436  010722  004737  013562          46900          JSR     PC,A2ND
2437  010726  104400                  47000          SCOPE
2438
```

```
2439                                    00100
2440                                    00200
2441                                    00300
2442                                    00400
2443                                    00500   ;DB255 TEST CONNECTOR DISCRETE EVENTS TEST
2444                                    00600
2445                                    00700   ;VERIFY "SEND REQUEST" RAISES "CLEAR-TO-SEND" AND "MODEM READY"
2446                                    00800   ;WHEN TRANSMITTER BUFFER IS LOADED
2447                                    00900
2448                                            ;*************
2449                                            ;            *
2450                                            ; TEST 44
2451                                            ;            *
2452                                            ;*************
2453                                            ;*****************************************************************
2454  010730  012737  000044  001072            TST44:  MOV     #44,TSTNO
2455  010736  012737  011124  001062                    MOV     #TST45,NEXT
2456  010744  012737  000240  177776  01100             MOV     #240,PS         ;PRIORITY=5
2457  010752  005077  170262          01200             CLR     @DPTS           ;CLR XMIT STATUS
2458  010756  005077  170250          01300             CLR     @DPRS           ;CLR RCV STATUS
2459  010762  104401                  01400             CLOCK                   ;RUN CLOCK
2460  010764  000010                  01500             10
2461  010766  012777  014500  170256  01600             MOV     #FTINT,@DPTIV   ;XMIT ERROR TRAP VECTOR
2462  010774  012777  014504  170244  01700             MOV     #FRINT,@DPRIV   ;RCV ERROR TRAP VECTOR
2463  011002  052777  000040  170230  01800             BIS     #BIT5,@DPTS     ;STATUS+RDY INT ENB
2464  011010  013777  001152  170224  01900             MOV     TDATA,@DPTB     ;LOAD BUFFER
2465  011016  104401                  02000             CLOCK                   ;RUN CLOCK
2466  011020  000003                  02100             3
2467  011022  032777  001000  170210  02200             BIT     #BIT9,@DPTS     ;"SEND REQUEST" ON
2468  011030  001001                  02300             BNE     .+4             ;YES
2469  011032  104000                  02400             HLT                     ;REPORT ERROR
2470  011034  032777  002000  170176  02500             BIT     #BIT10,@DPTS    ;"CLEAR-TO-SEND" UP?
2471  011042  001001                  02600             BNE     .+4             ;YES
2472  011044  104000                  02700             HLT                     ;REPORT ERROR
2473  011046  032777  010000  170164  02800             BIT     #BIT12,@DPTS    ;"MODEM READY" UP
2474  011054  001001                  02900             BNE     .+4             ;YES
2475  011056  104000                  03000             HLT                     ;REPORT ERROR
2476  011060  104401                  03100             CLOCK                   ;RUN CLOCK
2477  011062  000012                  03200             12
2478  011064  032777  001000  170146  03300             BIT     #BIT9,@DPTS     ;"SEND REQUEST" DOWN
2479  011072  001401                  03400             BEQ     .+4             ;YES
2480  011074  104000                  03500             HLT                     ;REPORT ERROR
2481  011076  032777  002000  170134  03600             BIT     #BIT10,@DPTS    ;"CLEAR-TO-SEND" DOWN
2482  011104  001401                  03700             BEQ     .+4             ;YES
2483  011106  104000                  03800             HLT                     ;REPORT ERROR
2484  011110  032777  010000  170122  03900             BIT     #BIT12,@DPTS    ;"MODEM READY" DOWN
2485  011116  001401                  04000             BEQ     .+4             ;YES
2486  011120  104000                  04100             HLT                     ;REPORT ERROR
2487  011122  104400                  04200             SCOPE
```

```
 2488                                          04400   ;PERFORM PREVIOUS TEST AT 7/11 BITS/CHARACTER
 2489                                          04500
 2490                                                  ;*************
 2491                                                  ;             *
 2492                                                  ; TEST 45     *
 2493                                                  ;             *
 2494                                                  ;*************
 2495                                                  ;*********************************************************************
 2496  011124  012737  000045  001072                 TST45:  MOV     #45,TSTNO
 2497  011132  012737  011472  001062                         MOV     #TST46,NEXT
 2498  011140  012737  000240  177776  04700                 MOV     #240,PS         ;PRIORITY = 5
 2499  011146  005077  170066          04800                 CLR     @DPTS           ;CLR XMIT STATUS
 2500  011152  005077  170054          04900                 CLR     @DPRS           ;CLR RCV STATUS
 2501  011156  012777  014500  170066  05000                 MOV     #FTINT,@DPTIV   ;XMIT ERROR TRAP VECTOR
 2502  011164  012777  014504  170054  05100                 MOV     #FRINT,@DPRIV   ;RCV ERROR TRAP VECTOR
 2503  011172  052777  000400  170032  05200                 BIS     #BIT8,@DPRS     ;7/11 BITS/CHARACTER
 2504  011200  052777  000040  170032  05300                 BIS     #BIT5,@DPTS     ;STATUS+RDY INT ENB
 2505  011206  013777  001152  170026  05400                 MOV     TDATA,@DPTB     ;LOAD BUFFER
 2506  011214  104401                  05500                 CLOCK                   ;RUN CLOCK
 2507  011216  000003                  05600                 3
 2508  011220  032777  001000  170012  05700                 BIT     #BIT9,@DPTS     ;"SEND REQUEST" ON
 2509  011226  001001                  05800                 BNE     .+4             ;YES
 2510  011230  104000                  05900                 HLT                     ;REPORT ERROR
 2511  011232  032777  002000  170000  06000                 BIT     #BIT10,@DPTS    ;CLEAR-TO-SEND" UP?
 2512  011240  001001                  06100                 BNE     .+4             ;YES
 2513  011242  104000                  06200                 HLT                     ;REPORT ERROR
 2514  011244  032777  010000  167766  06300                 BIT     #BIT12,@DPTS    ;"MODEM READY" UP
 2515  011252  001001                  06400                 BNE     .+4             ;YES
 2516  011254  104000                  06500                 HLT                     ;REPORT ERROR
 2517                                    06600
 2518  011256  104401                  06700                 CLOCK                   ;RUN CLOCK
 2519  011260  000011                  06800                 11
 2520  011262  032777  001000  167750  06900                 BIT     #BIT9,@DPTS     ;"SEND REQUEST" DOWN
 2521  011270  001401                  07000                 BEQ     .+4             ;YES
 2522  011272  104000                  07100                 HLT                     ;REPORT ERROR
 2523  011274  032777  002000  167736  07200                 BIT     #BIT10,@DPTS    ;"CLEAR-TO-SEND"DOWN
 2524  011302  001401                  07300                 BEQ     .+4             ;YES
 2525  011304  104000                  07400                 HLT                     ;REPORT ERROR
 2526  011306  032777  010000  167724  07500                 BIT     #BIT12,@DPTS    ;"MODEM READY" DOWN
 2527  011314  001401                  07600                 BEQ     .+4             ;YES
 2528  011316  104000                  07700                 HLT                     ;REPORT ERROR
 2529  011320  104400                  07800                 SCOPE
 2530                                    07900
 2531                                    08000   ;PERFORM PREVIOUS TEST AT 6/10 BITS/CHARACTER
 2532                                    08100
 2533  011322  012737  000240  177776  08200                 MOV     #240,PS         ;PRIORITY = 5
 2534  011330  005077  167704          08300                 CLR     @DPTS           ;CLR XMIT STATUS
 2535  011334  005077  167672          08400                 CLR     @DPRS           ;CLR RCV STATUS
 2536  011340  012777  014500  167704  08500                 MOV     #FTINT,@DPTIV   ;XMIT ERROR TRAP VECTOR
 2537  011346  012777  014504  167672  08600                 MOV     #FRINT,@DPRIV   ;RCV ERROR TRAP VECTOR
 2538  011354  052777  001000  167650  08700                 BIS     #BIT9,@DPRS     ;6 BITS/CHARACTER
 2539  011362  052777  000040  167650  08800                 BIS     #BIT5,@DPTS     ;STATUS+RDY INT ENB
 2540  011370  013777  001152  167644  08900                 MOV     TDATA,@DPTB     ;LOAD BUFFER
 2541  011376  104401                  09000                 CLOCK                   ;RUN CLOCK
 2542  011400  000003                  09100                 3
 2543  011402  032777  001000  167630  09200                 BIT     #BIT9,@DPTS     ;"SEND REQUEST" ON
```

```
011412  001201                  09300          BNE     .+4                     ;YES
011412  104000                  09400          HLT                             ;REPORT ERROR
011414  032777  010000  167616  09500          BIT     #BIT12,@DPTS            ;"MODEM READY" UP
011422  001001                  09600          BNE     .+4                     ;YES
011424  104000                  09700          HLT                             ;REPORT ERROR
011426  104401                  09800          CLOCK                           ;RUN CLOCK
011430  000010                  09900          10
011432  032777  001000  167600  10000          BIT     #BIT9,@DPTS             ;"SEND REQUEST" DOWN
011440  001401                  10100          BEQ     .+4                     ;YES
011442  104000                  10200          HLT                             ;REPORT ERROR
011444  032777  002000  167566  10300          BIT     #BIT10,@DPTS            ;"CLEAR-TO-SEND" DOWN
011452  001401                  10400          BEQ     .+4                     ;YES
011454  104000                  10500          HLT                             ;REPORT ERROR
011456  032777  010000  167554  10600          BIT     #BIT12,@DPTS            ;"MODEM READY" DOWN
011464  001401                  10700          BEQ     .+4                     ;YES
011466  104000                  10800          HLT                             ;REPORT ERROR
011470  104400                  10900          SCOPE
                                11000
                                11100  ;DB25S TEST CONNECT CONNECTOR TEST
                                11200
                                11300
                                11400  ;TERMINAL READY
                                11500
                                11600
                                11700  ;TERM RDY-RAISE "CARRIER" AND "RING FLAG", NO INT ENB
                                       ;*************
                                       ;            *
                                       ; TEST 46    *
                                       ;            *
                                       ;*************
                                       ;*****************************************************************************
011472  012737  000046  001072          TST46:  MOV     #46,TSTNO
011500  012737  011770  001062                  MOV     #TST47,NEXT
011506  012737  000240  177776  11800          MOV     #240,PS                 ;PRIORITY = 5
011514  005077  167520          12000          CLR     @DPTS                   ;CLR XMIT STATUS
011520  012777  014500  167512  12100          MOV     #FTINT,@DPTS            ;ERROR TRAP VECTOR
011526  012777  000001  167504  12200          MOV     #BIT0,@DPTS             ;TERMINAL READY
011534  104403  001500          12300          DELAY   .1500                   ;15MS PROPOGATION DELAY
011540  032777  000001  167472  12400          BIT     #BIT0,@DPTS             ;TERMINAL READY
011546  001001                  12500          BNE     .+4                     ;YES
011550  104000                  12600          HLT                             ;REPORT ERROR
011552  032777  004000  167460  12700          BIT     #BIT11,@DPTS            ;CARRIER
011560  001001                  12800          BNE     .+4                     ;YES
011562  104000                  12900          HLT                             ;REPORT ERROR
011564  032777  020000  167446  13000          BIT     #BIT13,@DPTS            ;RING FLAG UP
011572  001001                  13100          BNE     .+4                     ;YES
011574  104000                  13200          HLT                             ;REPORT ERROR
                                13300
                                13400  ;CLEAR TERMINAL READY
                                13500
011576  042777  000001  167434  13600          BIC     #BIT0,@DPTS             ;CLEAR TERMINAL READY
011604  104403  001500          13700          DELAY   .1500
011610  032777  000001  167422  13800          BIT     #BIT0,@DPTS             ;TERM RDY DOWN
011616  001401                  13900          BEQ     .+4                     ;YES
011620  104000                  14000          HLT                             ;REPORT ERROR
011622  032777  004000  167410  14100          BIT     #BIT11,@DPTS            ;CARRIER DOWN
```

```
 2600  011630  001401                        14200          BEQ     .+4                 ;YES
 2601  011632  104000                        14300          HLT                         ;REPORT ERROR
 2602  011634  032777  100000  167376        14400          BIT     #BIT15,@DPTS        ;"CARRIER DOWN" FLAG UP
 2603  011642  001001                        14500          BNE     .+4                 ;YES
 2604  011644  104000                        14600          HLT                         ;REPORT EPROR
 2605  011646  042777  100000  167364        14700          BIC     #BIT15,@DPTS        ;CLEAR DOWN FLAG
 2606                                        14800
 2607                                        14900  ;VERIFY THAT "RING" AND "CARRIER DOWN" INTERRUPT
 2608  011654  012777  000240  167372        15000          MOV     #240,@DPTP          ;INTERRUPT PRIORITY 5.
 2609  011662  005077  167352                15100  RCD:    CLR     @DPTS               ;CLEAR XMT STATUS
 2610  011666  005077  167340                15200          CLR     @DPRS               ;CLEAR RCV STATUS
 2611  011672  012777  014354  167352        15300          MOV     #TV24,@DPTIV        ;TEST PASS VECTOR
 2612  011700  012737  000200  177776        15400          MOV     #200,PS             ;PRIORITY = 4
 2613  011706  012777  000041  167324        15500          MOV     #BIT5+BIT0,@DPTS        ;STATUS INTERRUPT ENABLE
 2614  011714  104403  001500                15600          DELAY   .1500               ;15.75 MS DELAY
 2615  011720  104000                        15700          HLT                         ;REPORT ERROR
 2616                                        15800
 2617                                        15900  ;VERIFY "CARRIER DOWN" RAISES INTERRUPT
 2618  011722  012777  014426  167322        16000  RCD1:   MOV     #TV25,@DPTIV        ;NEXT TEST VECTOR
 2619  011730  012737  011766  001174        16100          MOV     #1$,BACK
 2620  011736  012737  000200  177776        16200          MOV     #200,PS
 2621  011744  042777  000001  167266        16300          BIC     #BIT0,@DPTS         ;CLEAR TERM. RDY. SHOULD SET 'CARRIER DOWN'.
 2622  011752  104403  001500                16400          DELAY   .1500               ;15.75MS DELA'
 2623  011756  104000                        16500          HLT                         ;REPORT ERROR
 2624  011760  042777  100000  167252        16600          BIC     #BIT15,@DPTS        ;CLEAR "CARRIER DOWN"
 2625  011766  104400                        16700  1$:     SCOPE
 2626                                        16800
 2627                                        16900
```

```
 2628                                   17100   ;CABLE TEST WITH OUT EXERCISING THE SOFTWARE CLOCK.
 2629                                   17200   ;IN THIS TEST FUNCTIONS OF THE CABLE WILL BE
 2630                                   17300   ;TESTED WITHOUT THE SOFTWARE CLOCK. THE CLOCK MUST BE
 2631                                   17400   ;SUPPLIED BY THE DP11.
 2632                                   17500
 2633  011770                           17600   PART3:
 2634                                   17700   ;       DF11-L TEST!!!
 2635                                   17800   ;VERIFY THAT LOADING THE TRANSMITTER BUFFER
 2636                                   17900   ;BRINGS UP "REQUEST TO SEND" WHICH IN TURN WILL
 2637                                   18000   ;BRING UP "CLEAR TO SEND" AND "MODEM READY".
 2638                                   18100   ;VERIFY ALSO THAT THEY GO AWAY.
 2639                                   18200
 2640                                           ;*************
 2641                                           ;            *
 2642                                           ; TEST 47
 2643                                           ;            *
 2644                                           ;*************
 2645                                           ;*************************************************************************
 2646  011770  012737  000047  001072           TST47:  MOV     #47,TSTNO
 2647  011776  012737  015750  001062                   MOV     #.EOP,NEXT
 2648  012004  032737  000001  001134  18400            BIT     #BIT0,SAVSR1
 2649  012012  001002                   18500            BNE     .+6
 2650  012014  000137  015750           18600            JMP     .EOP
 2651  012020  005077  167214           18700            CLR     @DPTS           ;CLEAR THE TX STATUS
 2652  012024  005077  167202           18800            CLR     @DPRS           ;CLEAR THE RX STATUS.
 2653  012030  005002                   18900            CLR     R2              ;SET TIME OUT
 2654  012032  012700  001300           19000            MOV     #1300,R0
 2655  012036  010277  167200           19100            MOV     R2,@DPTB        ;LOAD THE TX BUFFER
 2656  012042  017701  167172           19200    1$:     MOV     @DPTS,R1
 2657  012046  042701  164777           19300            BIC     #164777,R1
 2658  012052  022701  013000           19400            CMP     #13000,R1
 2659  012056  001403                   19500            BEQ     2$
 2660  012060  005202                   19600            INC     R2              ;UPDATE DELAY
 2661  012062  001367                   19700            BNE     1$              ;IS IT DONE?
 2662  012064  104001                   19800            HLT     1               ;ERROR REQUEST TO SEND,CLEAR TO
 2663                                   19900                                    ;SEND AND MODEM READY NOT UP.
 2664  012066  005002                   20000    2$:     CLR     R2              ;SET FOR TIME OUT
 2665  012070  005202                   20100            INC     R2              ;DELAY
 2666  012072  001376                   20200            BNE     .-2             ;
 2667  012074  032777  013000  167136   20300            BIT     #13000,@DPTS    ;ARE THEY GONE?
 2668  012102  001401                   20400            BEQ     .+4
 2669  012104  104000                   20500            HLT
 2670                                   20600
 2671                                   20700   ;VERIFY THAT THE SETTING OF "TERMINAL READY" BRINGS
 2672                                   20800   ;UP "RING" AND "CARRIER DOWN" ALSO VERIFY THAT
 2673                                   20900   ;CLEARING "TERMINAL READY" BRINGS DOWN "RING"
 2674                                   21000   ;AND "CARRIER DOWN".
 2675                                   21100
 2676  012106  012777  000001  167124   21200            MOV     #BIT0,@DPTS
 2677  012114  104403  001500           21300            DELAY   .1500
 2678  012120  017701  167114           21400            MOV     @DPTS,R1
 2679  012124  042701  153776           21500            BIC     #153776,R1
 2680  012130  022701  024001           21600            CMP     #24001,R1
 2681  012134  001401                   21700            BEQ     .+4
 2682  012136  104001                   21800            HLT     1
 2683  012140  042777  000001  167072   21900            BIC     #BIT0,@DPTS
```

E05


```
2694  012146  104403  001500          22000          DELAY   ,1500
2695  012152  022777  120000  167060  22100          CMP     #120000,@DPTS
2696  012160  001401                  22200          BEQ     .+4
2697  012162  104000                  22300          HLT
2698                                  22400
2699                                  22500  ;NOW TEST THAT DATA CAN BE TRANSFERED.
2690                                  22600  ;A BINARY COUNT PATTERN WILL BE TRANSMITTED AND RECEIVED
2691                                  22700  ;WITH OUT THE USE OF THE SOFTWARE CLOCK.
2692                                  22800
2693  012164  005037  001102          22900          CLR     TEMP1
2694  012170  005037  001104          23000          CLR     TEMP2
2695  012174  004737  014000          23100          JSR     PC,SEQ.DATA
2696  012200  104400                  23200          SCOPE
2697
```

```
                                                00100
                                                00200   ;LINE.N  SUBROUTINE TO FETCH THE LINE
                                                00300   ;NUMBER AND FIRST DP11 VECTOR ADDRESS FROM
                                                00400   ;THE CONSOL SWITCHES
                                                00500   ;SW0-SW8=VECTOR ADDRESS OF FIRST DP11
                                                00600   ;SW9-SW15=LINE NUMBER OF DP11 SELECTED FOR TEST
                                                00700
2705  012202  005037  001076                   00800   LINE.N: CLR     ERRCNT                  ;CLEAR ERROR COUNT
2706  012206  013737  177570  001134            00900           MOV     SWR,SAVSR1              ;SAVE CONSOL SWITCH SETTINGS
2707  012214  013700  177570                   01000           MOV     SWR,R0
2708  012220  000000                           01100           HALT                            ;SET SWR TO LINE NUMBER
2709                                           01200                                           ;LOW BYTE = FIRST DP VECTOR
2710                                           01300                                           ;HIGH BYTE = LINE NUMBER(8)
2711  012222  013737  177570  001164            01400           MOV     SWR,SAVSR2              ;SAVE CONSOL SWITCHES
2712  012230  013700  177570                   01500           MOV     SWR,R0
2713  012234  000000                           01600           HALT
2714  012236  005001                           01700           CLR     R1
2715  012240  113701  001165                   01800           MOVB    SAVSR2+1,R1             ;SAVE LINE NUMBER
2716  012244  000405                           01900           BR      XTAG
2717  012246  013701  001146                   02000   LINE.X: MOV     XLINEX,R1
2718  012252  005037  001134                   02100           CLR     SAVSR1
2719  012256  006301                           02200           ASL     R1
2720  012260  006201                           02300   XTAG:   ASR     R1                      ;CLEAR LSB
2721  012262  010137  001146                   02400           MOV     R1,XLINEX
2722  012266  006301                           02500           ASL     R1                      ;SCALE LINE NUMBER TO ADDRESS
2723  012270  006301                           02600           ASL     R1                      ;MODULO 10(8)
2724  012272  006301                           02700           ASL     R1
2725  012274  005777  166760                   02800           TST     @BASCSR                 ;DOES LINE 0 REALLY EXIST??
2726  012300  000240                           02900           NOP                             ..
2727  012302  105737  001134                   03000           TSTB    SAVSR1                  .
2728  012306  100403                           03100           BMI     .+10
2729  012310  012737  012422  000004           03200           MOV     #3$,@#4
2730  012316  013702  001260                   03300           MOV     BASCSR,R2               ;SET R2 = LINE 0 ADDRESS
2731  012322  160102                           03400           SUB     R1,R2                   ;MANUFACTURE DEVICE ADDRESS
2732  012324  012703  001232                   03500           MOV     #DPRS,R3                ;R3 = ADDRESS OF RCV STATUS ADRS
2733  012330  010223                           03600           MOV     R2,(R3)+                ;LOAD RCV STATUS ADRS
2734  012332  005722                           03700           TST     (R2)+                   ;INC TO RCV BUFFER ADRS
2735  012334  010223                           03800           MOV     R2,(R3)+                ;LOAD RCV BUFFER ADRS
2736  012336  005202                           03900           INC     R2                      ;INC TO SYNC BUFFER ADRS
2737  012340  010223                           04000           MOV     R2,(R3)+                ;LOAD SYNC ADRS
2738  012342  005202                           04100           INC     R2                      ;INC TO XMIT STATUS ADRS
2739  012344  010223                           04200           MOV     R2,(R3)+                ;LOAD TRANSMITTER STATUS ADRS
2740  012346  005722                           04300           TST     (R2)+                   ;INC TO XMIT BUFFER
2741  012350  010223                           04400           MOV     R2,(R3)+                ;LOAD XMIT BUFFER ADRS
2742  012352  005202                           04500           INC     R2                      ;INC TO SYNC EXTENTION
2743  012354  010223                           04600           MOV     R2,(R3)+                ;LOAD SYNC EXTENSION ADRS
2744  012356  013702  001164                   04700           MOV     SAVSR2,R2               ;SET UP VECTOR ADDRESS
2745  012362  042702  177000                   04800           BIC     #177000,R2              ;CLEAR LINE NUMBER FROM VEC ADRS
2746  012366  105737  001134                   04900           TSTB    SAVSR1
2747  012372  100402                           05000           BMI     2$
2748  012374  013702  001256                   05100           MOV     BASVEC,R2
2749  012400  060102                           05200   2$:     ADD     R1,R2                   ;SET VECTOR ADDRESS TO LINE NUMBER
2750  012402  010223                           05300           MOV     R2,(R3)+                ;LOAD RCV VECTOR ADRS
2751  012404  005722                           05400           TST     (R2)+                   ;INC TO NEXT VECTOR
2752  012406  010223                           05500           MOV     R2,(R3)+                ;LOAD RCV PRIORITY ADRS
2753  012410  005722                           05600           TST     (R2)+                   ;INC TO NEXT VECTOR
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2754  012412  010223                05700           MOV     R2,(R3)+                ;LOAD XMIT VECTOR ADRS
2755  012414  005722                05800           TST     (R2)+                   ;INC TO NEXT VECTOR
2756  012416  010213                05900           MOV     R2,(R3)                 ;LOAD XMIT PRIORITY ADRS
2757  012420  000414                06000           BR      5$
2758  012422  005037  001146        06100   3$:     CLR     XLINEX
2759  012426  013701  000042        06200           MOV     @#42,R1
2760  012432  001405                06300           BEQ     4$
2761  012434  000005                06400           RESET
2762          012436                06550   LOGICAL=.
2763  012436  004711                06500           JSR     PC,(R1)
2764  012440  000240                06600           NOP
2765  012442  000240                06700           NOP
2766  012444  000240                06800           NOP
2767  012446  022626                06900   4$:     POP.SP
2768  012450  000676                07000           BR      LINE.X
2769  012452  012737  000006  000034 07100   5$:     MOV     #6,@#4
2770  012460  000207                07200           RTS     PC
2771                                07300   ;**********************CLRVEC**********************************
2772                                07400
2773                                07500   ;CLRVEC,ROUTINE TO FILL COMMUNICATION VECTOR AREA WITH .+2,HALT
2774                                07600
2775  012462  012702  000300        07700   CLRVEC: MOV     #300,R2                 ;R2 COMM VECTOR AREA ADRS
2776  012466  012701  000302        07800           MOV     #302,R1                 ;INIT R1 WITH ADRS OF HALT
2777  012472  010122                07900   1$:     MOV     R1,(R2)+                ;MOV .+2 TO PC
2778  012474  005022                08000           CLR     (R2)+                   ;MOV HALT TO PC
2779  012476  022121                08100           CMP     (R1)+,(R1)+             ;INC TO NEXT VECTOR AREA
2780  012500  022701  000776        08200           CMP     #776,R1                 ;END OF VECTOR AREA
2781  012504  001372                08300           BNE     1$                      ;NO
2782  012506  000207                08400           RTS     PC                      ;RETURN
2783                                08500
2784                                08600
2785                                08700
2786                                08800   ;BITSR,ROUTINE TO TEST READ WRITE BITS OF STATUS
2787                                08900   ;THIS ROUTINE VERIFIES THAT EACH READ/WRITE BIT
2788                                09000   ;CAN BE SET AND CLEARED
2789                                09100   ;EXAMINE LOCATIONS
2790                                09200   ;BITS: FOR BIT UNDER TEST
2791                                09300   ;REG:  FOR REGISTER UNDER TEST
2792                                09400
2793  012510  010537  001110        09500   BITST:  MOV     R5,TEMP4
2794  012514  012537  013054        09600           MOV     (R5)+,BITS              ;SAVE BIT NUMBER
2795  012520  053777  013054  000330 09700          BIS     BITS,@REG               ;SET BIT
2796  012526  053700  013054        09800           BIS     BITS,R0
2797  012532  017701  000320        09900           MOV     @REG,R1
2798  012536  033777  013054  000312 10000          BIT     BITS,@REG               ;IS BIT SET?
2799  012544  001001                10100           BNE     .+4                     ;YES
2800  012546  104002                10200           HLT     2                               ;REPORT ERROR
2801  012550  043777  013054  000300 10300          BIC     BITS,@REG               ;CLEAR BIT
2802  012556  043700  013054        10400           BIC     BITS,R0
2803  012562  017701  000270        10500           MOV     @REG,R1
2804  012566  033777  013054  000262 10600          BIT     BITS,@REG               ;IS BIT CLEARED
2805  012574  001401                10700           BEQ     .+4                     ;YES
2806  012576  104002                10800           HLT     2                               ;REPORT ERROR
2807  012600  053777  013054  000250 10900          BIS     BITS,@REG               ;SET BIT
2808  012606  053700  013054        11000           BIS     BITS,R0
2809  012612  017701  000240        11100           MOV     @REG,R1
```

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 2810  012616  033777  013054  000232  11200          BIT     BITS,@REG               ;IS BIT SET
 2811  012624  001001                  11300          BNE     .+4                     ;YES
 2812  012626  104002                  11400          HLT     2                       ;REPORT ERROR
 2813  012630  005077  000222          11500          CLR     @REG                    ;CLEAR REG
 2814  012634  005000                  11600          CLR     R0
 2815  012636  017701  000214          11700          MOV     @REG,R1
 2816  012642  033777  013054  000206  11800          BIT     BITS,@REG               ;IS BIT CLEARED
 2817  012650  001401                  11900          BEQ     .+4                     ;YES
 2818  012652  104002                  12000          HLT     2                       ;REPORT ERROR
 2819  012654  052777  000004  166350  12100          BIS     #BIT2,@DPRS             ;KEEP CLOCK HUMMING
 2820  012662  052700  000004          12200          BIS     #BIT2,R0
 2821  012666  000205                  12300          RTS     R5
 2822                                  12400
 2823                                  12500
 2824                                  12600
 2825                                  12700  ;VALID,ROUTINE TO TEST FOR ANY INTERACTION BETWEEN BITS
 2826                                  12800  ;THIS ROUTINE CHECKS THAT WHEN EXECUTING A BIT SET INSTRUCTION
 2827                                  12900  ;ONLY THE SPECIFIED BIT IS SET
 2828                                  13000
 2829  012670  011637  001110          13100  .VALID: MOV     (SP),TEMP4
 2830  012674  017637  000000  013054  13200          MOV     @(SP),BITS              ;FETCH BIT NUMBER
 2831  012702  062716  000002          13300          ADD     #2,(SP)
 2832  012706  053777  013054  000142  13400          BIS     BITS,@REG               ;SET BIT
 2833  012714  053700  013054          13500          BIS     BITS,R0
 2834  012720  017701  000132          13600          MOV     @REG,R1
 2835  012724  023777  013054  000124  13700          CMP     BITS,@REG               ;WAS ONLY THAT BIT SET?
 2836  012732  001401                  13800          BEQ     .+4                     ;YES
 2837  012734  104002                  13900          HLT     2                       ;REPORT ERROR
 2838  012736  043777  013054  000112  14000          BIC     BITS,@REG               ;RESTORE REG
 2839  012744  053700  013054          14100          BIS     BITS,R0
 2840  012750  000002                  14200          RTI                             ;RETURN
 2941                                  14300  ;
 2842                                  14400  ;CLEAR,ROUTINE TO TEST THAT BIC ONLY CLEARS SPECIFIED BIT
 2843                                  14500
 2844  012752  011637  001110          14600  .CLEAR: MOV     (SP),TEMP4
 2845  012756  017637  000000  013054  14700          MOV     @(SP),BITS              ;FETCH BIT NUMBER
 2846  012764  062716  000002          14800          ADD     #2,(SP)
 2847  012770  043777  013054  000060  14900          BIC     BITS,@REG               ;CLEAR BIT
 2848  012776  043737  013054  001136  15000          BIC     BITS,TMPDAT             ;CLEAR MASK
 2849  013004  012700  013000          15100          MOV     #13000,R0
 2850  013010  005300                  15200          DEC     R0
 2851  013012  001376                  15300          BNE     .-2
 2852  013014  013700  001136          15400          MOV     TMPDAT,R0
 2853  013020  017701  000032          15500          MOV     @REG,R1
 2854  013024  023777  001136  000024  15600          CMP     TMPDAT,@REG             ;WERE ANY OTHER BITS CLEARED
 2855  013032  001401                  15700          BEQ     .+4                     ;NO
 2856  013034  104002                  15800          HLT     2                       ;REPORT ERROR
 2857  013036  053777  013054  000012  15900          BIS     BITS,@REG               ;RESTORE REG
 2858  013044  053737  013054  001136  16000          BIS     BITS,TMPDAT             ;RESTORE MASK
 2859  013052  000002                  16100          RTI                             ;RETURN
 2860                                  16200
 2861  013054  000000                  16300  BITS:   0
 2862  013056  000000                  16400  REG:    0
 2863                                  16500
 2864                                  16600  ;COMMON DATA AND IDLE SUBROUTINE
 2865                                  16700
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 2866  013060  012701  015371          16800  AND:    MOV     #15371,R1               ;PRIME RANDOM # GEN
 2867  013064  012702  072414          16900          MOV     #72414,R2               ;"      "       "
 2868  013070  012703  004036          17000          MOV     #4036,R3                ;"      "       "
 2869  013074  042777  004300  166130  17100          BIC     #4300,@DPRS             ;RCV INT ENB, RCV ACTIVE
 2870  013102  042777  160342  166130  17200          BIC     #160342,@DPTS           ;INT ENBS IDLE SYNC, ERRORS
 2871  013110  012737  015556  001172  17300          MOV     #BOTTOM,RP              ;SET UP RCV POINTER
 2872  013116  013737  001172  001170  17400          MOV     RP,TP                   ;SET UP XMIT POINTER
 2873  013124  012777  015172  166114  17500          MOV     #RRRR,@DPRIV            ;RCV INT VECTOR
 2874  013132  012777  015044  166112  17600          MOV     #RRRT,@DPTIV            ;XMIT INT VECTOR
 2875  013140  012737  000002  001162  17700          MOV     #2,SCNT                 ;SYNC COUNT = 2
 2876  013146  110237  001152          17800          MOVB    R2,TDATA                ;RANDOM DATA
 2877  013152  052777  000100  166052  17900          BIS     #100,@DPRS              ;RCV INT ENB
 2878  013160  013777  001144  166054  18000  1$:     MOV     TSYNC,@DPTB             ;LOAD BUFFER
 2879  013166  052777  000340  166044  18100          BIS     #340,@DPTS              ;XMIT DONE, INT ENB, STATUS ENB
 2880  013174  010137  001166          18200          MOV     R1,TIME                 ;"ON" STALL
 2881  013200  005337  001166          18300  2$:     DEC     TIME                    ;0.6 SEC MAX
 2882  013204  001375                  18400          BNE     2$
 2883  013206  042777  000140  166024  18500          BIC     #140,@DPTS              ;TURN OFF INT ENB
 2884  013214  052777  000002  166016  18600          BIS     #BIT1,@DPTS             ;IDLE SYNC
 2885  013222  004537  013310          19700          JSR     R5,RNUM                 ;GENERATE "STALL" TIME
 2886  013226  010137  001166          18800          MOV     R1,TIME                 ;FETCH RANDOM STALL TIME
 2887  013232  005337  001166          18900  3$:     DEC     TIME                    ;COUNT IDLE TIME
 2888  013236  001375                  19000          BNE     3$                      ;TIME OUT?
 2889  013240  004537  013310          19100          JSR     R5,RNUM                 ;GENERATE "ON" TIME + SYNC
 2890  013244  042777  000002  165766  19200          BIC     #BIT1,@DPTS             ;CLEAR IDLE
 2891  013252  000240                  19300          NOP
 2892  013254  042777  000100  165750  19400          BIC     #100,@DPRS              ;CLEAR RCV INT ENB
 2893  013262  000207                  19500          RTS     PC
 2894                                  19600
 2895                                  19700
 2896                                  19800  ;SGEN,ROUTINE TO GENERATE A UNIQUE SYNC CHARACTER
 2897                                  19900
 2898  013264  112777  000026  165744  20000  SGEN:   MOVB    #26,@SYNC               ;SET UP FILLER SYNC
 2899  013272  104403  005670          20100          DELAY   ,3000.                  ;DELAY 10 CHAR
 2900  013276  004537  013310          20200          JSR     R5,RNUM                 ;RANDOM #
 2901  013302  110137  001144          20300          MOVE    R1,TSYNC                ;LOAD SYNC
 2902  013306  000207                  20400          RTS     PC
 2903                                  20500
 2904                                  20600
 2905                                  20700
 2906                                  20800  ;RNUM, PSEUDO RANDOM NUMBER GENERATOR
 2907                                  20900
 2908  013310  032737  040000  177570  21000  RNUM:   BIT     #BIT14,SWR              ;TEST FOR SCOPE LOOP
 2909  013316  001010                  21100          BNE     1$                      ;EXIT IF SCOPE
 2910  013320  060201                  21200          ADD     R2,R1
 2911  013322  005501                  21300          ADC     R1
 2912  013324  060102                  21400          ADD     R1,R2
 2913  013326  005502                  21500          ADC     R2
 2914  013330  060302                  21600          ADD     R3,R2
 2915  013332  005502                  21700          ADC     R2
 2916  013334  060203                  21800          ADD     R2,R3
 2917  013336  005503                  21900          ADC     R3
 2918  013340  000205                  22000  1$:     RTS     R5
 2919                                  22100
 2920                                  22200
 2921                                  22300
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 2922                                          22400  ;CLOCK,SUBROUTINE TO RUN SOFTWARE CLOCK
 2923                                          22500  ;NUMBER OF CYCLES IS FETCHED  CALL
 2924                                          22600
 2925  013342  005037  001102                 22700  .CLOCK: CLR     TEMP1
 2926  013346  032737  000400  001134         22800          BIT     #BIT8,SAVSR1            ;12/8 BITS/CHAR
 2927  013354  001412                         22900          BEQ     .RXCLK                  ;BRANCH IF 9 BITS/CHAR
 2928  013356  052777  002000  165646         23000          BIS     #BIT10,@DPRS            ;SELECT 12 BIT MODE
 2929  013364  052737  000400  001160         23100          BIS     #BIT8,LIMIT             ;9 BIT SYNC
 2930  013372  062737  000004  001102         23200          ADD     #4,TEMP1                ;INCREASE CLOCK COUNT
 2931  013400  000402                         23300          BR      .+6
 2932  013402  005037  001102                 23400  .RXCLK: CLR     TEMP1
 2933  013406  005037  177776                 23500          CLR     PS
 2934  013412  067637  000000  001102         23600          ADD     @(SP),TEMP1
 2935  013420  062716  000002                 23700          ADD     #2,(SP)
 2936  013424  052777  000010  165606         23800  1$:     BIS     #BIT3,@DPTS             ;SET CLOCK HIGH
 2937  013432  013705  013470                 23900          MOV     FREQ,R5                 ;SET UP DELAY COUNT
 2938          013436                         24000  DEL=.
 2939  013436  005305                         24100          DEC     R5                      ;DECREMENT COUNT
 2940  013440  001376                         24200          BNE     DEL                     ;BRANCH IF NO TIMEOUT
 2941  013442  042777  000010  165570         24300          BIC     #BIT3,@DPTS             ;SET CLOCK LOW
 2942  013450  013705  013470                 24400          MOV     FREQ,R5                 ;SET UP DELAY COUNT
 2943          013454                         24500  DEL=.
 2944  013454  005305                         24600          DEC     R5                      ;DEC COUNT
 2945  013456  001376                         24700          BNE     DEL                     ;BRANCH IF NO TIMEOUT
 2946  013460  005337  001102                 24800          DEC     TEMP1
 2947  013464  001357                         24900          BNE     1$
 2948  013466  000002                         25000          RTI
 2949  013470  000030                         25100  FREQ:   30                              ;NORMAL 12.8 US DELAY
 2950                                          25200                                          ;PATCH FOR 50 FT CABEL
 2951                                          25300
 2952                                          25400
 2953                                          25500  ;REE, SUBROUTINE TO REINITIALIZE DP11 FOR NEXT TEST
 2954                                          25600
 2955  013472  012737  000200  177776         25700  REE:    MOV     #200,PS                 ;SET PRIORITY TO 4
 2956  013500  005077  165534                 25800          CLR     @DPTS                   ;CLEAR XMIT STATUS
 2957  013504  005077  165522                 25900          CLR     @DPRS                   ;CLEAR RCV STATUS
 2958  013510  105077  165530                 26000          CLRB    @SEXT                   ;CLEAR SYNC EXTENTION
 2959  013514  012737  000001  001144         26100          MOV     #1,TSYNC                ;INIT TEST SYNC
 2960  013522  012777  014504  165516         26200          MOV     #FRINT,@DPRIV           ;SET UP RVI INT VECTOR
 2961  013530  012777  014510  165514         26300          MOV     #TV18,@DPTIV            ;SET XMIT INT VECTOR TO SYNC
 2962  013536  032737  000400  001134         26400          BIT     #BIT8,SAVSR1            ;TEST FOR 8/12 BITS/CHAR
 2963  013544  001405                         26500          BEQ     1$                      ;EXIT IF 8 BITS
 2964  013546  062705  000010                 26600          ADD     #10,R5                  ;SET RETURN ADRS FOR 12 BIT LIMIT
 2965  013552  052777  002000  165452         26700          BIS     #BIT10,@DPRS            ;SET 12 BIT/CHAR MODE
 2966  013560  000205                         26800  1$:     RTS     R5                      ;RETURN
 2967                                          26900
 2968                                          27000  ;COMMON DATA AND IDLE SUBROUTINE
 2969                                          27100
 2970  013562  042777  004300  165442         27200  A2ND:   BIC     #4300,@DPRS             ;RCV INT ENB, RCV ACTIVE
 2971  013570  042777  160342  165442         27300          BIC     #160342,@DPTS           ;INT ENBS IDLE SYNC, ERRORS
 2972  013576  012737  015556  001172         27400          MOV     #BOTTOM,RP              ;RP = BOTTOM OF TUMBLE TABLE
 2973  013604  013737  001172  001170         27500          MOV     RP,TP                   ;SET UP TRANSMIT POINTER
 2974  013612  012777  015172  165426         27600          MOV     #RRRR,@DPRIV            ;RCV INT VECTOR
 2975  013620  012777  015044  165424         27700          MOV     #RRRT,@DPTIV            ;XMIT INT VECTOR
 2976  013626  012737  000002  001162         27800          MOV     #2,SCNT                 ;SYNC COUNT = 2
 2977  013634  110237  001152                 27900          MOVB    R2,TDATA                ;RANDOM DATA
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 2978  013640  013777  001144  165374  28000          MOV     TSYNC,@DPTB             ;LOAD BUFFER
 2979  013646  052777  000100  165356  28100          BIS     #100,@DPRS              ;RCV INT ENB
 2980  013654  052777  000140  165356  28200          BIS     #140,@DPTS              ;XMIT INT ENB
 2981  013662  010137  001166          28300          MOV     R1,TIME                 ;"ON" STALL
 2982  013666  104402                  28400  1$:     RXCLK
 2983  013670  000001                  28500          1
 2984  013672  005337  001166          28600          DEC     TIME                    ;0.6 SEC AVERAGE
 2985  013676  001373                  28700          BNE     1$
 2986  013700  042777  000140  165332  28800          BIC     #140,@DPTS              ;TURN OFF INT ENB
 2987  013706  052777  000002  165324  28900          BIS     #BIT1,@DPTS             ;IDLE SYNC
 2988  013714  004537  013310          29000          JSR     R5,RNUM                 ;GENERATE "STALL" TIME
 2989  013720  010137  001166          29100          MOV     R1,TIME                 ;
 2990  013724  104402                  29200  2$:     RXCLK
 2991  013726  000001                  29300          1
 2992  013730  005337  001166          29400          DEC     TIME                    ;COUNT IDLE TIME
 2993  013734  001373                  29500          BNE     2$                      ;TIME OUT?
 2994  013736  004537  013310          29600          JSR     R5,RNUM                 ;GENERATE "ON" TIME + SYNC
 2995  013742  000207                  29700          RTS     PC
 2996                                  29800
 2997                                  29900
 2998                                  30000  ;POWER FAIL ROUTINE
 2999                                  30100
 3000  013744  012737  013754  000024  30200  .PFAIL: MOV     #PWRUP,24               ;LOAD PFAIL VECTOR FOR POWER UP
 3001  013752  000000                  30300          HALT                            ;
 3002  013754  000005                  30400  PWRUP:  RESET                           ;WAIT TTY TO COME UP
 3003  013756  012706  001050          30500          MOV     #STACK,SP               ;REINIT STACK POINTER
 3004  013762  012737  013744  000024  30600          MOV     #.PFAIL,24              ;LOAD PFAIL VECTOR FOR POWER DOWN
 3005  013770  104407                  30700          TYPE
 3006  013772  016770                  30800          MPOWER
 3007  013774  000177  165060          30900          JMP     @RETURN
 3008                                  31000
 3009                                  31100
 3010  014000                          31200  SEQ.DATA:
 3011  014000  011637  001174          31300          MOV     (SP),BACK
 3012  014004  105077  165234          31400          CLRB    @SEXT                   ;CLEAR SYNC EXTENTION
 3013  014010  005037  001154          31500          CLR     RDATA                   ;RECEIVER DATA
 3014  014014  005037  001152          31600          CLR     TDATA                   ;TRANSMITTER DATA
 3015  014020  005077  165206          31700          CLR     @DPRS                   ;RECEIVER STATUS
 3016  014024  005077  165210          31800          CLR     @DPTS                   ;TRANSMITTER STATUS
 3017  014030  052777  000001  165174  31900          BIS     #BIT0,@DPRS             ; STRIP SYNC
 3018  014036  012737  000400  001156  32000          MOV     #400,CHLEN              ;CHAR LENGTH INDEX
 3019  014044  032737  000400  001134  32100          BIT     #BIT8,SAVSR1            ;TEST 12 BIT CHAR MODE
 3020  014052  001414                  32200          BEQ     1$                      ;NO
 3021  014054  012737  010000  001160  32300          MOV     #10000,LIMIT            ;SELECT END OF DATA
 3022  014062  052777  002000  165142  32400          BIS     #BIT10,@DPRS            ;SELECT 12 BITS/CHARACTER
 3023  014070  012737  000426  001144  32500          MOV     #426,TSYNC              ;SYNC FOR 12 BIT CHAR
 3024  014076  105277  165142          32600          INCB    @SEXT                   ;PLACE MSB OF SYNC IN SYNC EXT
 3025  014102  000406                  32700          BR      2$
 3026  014104  012737  000400  001160  32800  1$:     MOV     #400,LIMIT              ;TEMPORARY CHARACTER LIMIT
 3027  014112  012737  000026  001144  32900          MOV     #26,TSYNC               ;INIT SYNC STORAGE
 3028  014120  012777  014510  165124  33000  2$:     MOV     #TV18,@DPTIV            ;TRANSMITTER VECTOR
 3029  014126  012777  014616  165112  33100          MOV     #RV18,@DPRIV            ;RECEIVER VECTOR
 3030  014134  012737  000200  177776  33200          MOV     #200,PS                 ;PRIORITY=4
 3031  014142  012737  000004  001162  33300          MOV     #4,SCNT                 ;SYNC COUNT=4
 3032  014150  113777  001144  165360  33400          MOVB    TSYNC,@SYNC             ;LOAD SYNC
 3033  014156  052777  000100  165046  33500          BIS     #BIT6,@DPRS             ;RCV INT ENB
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 3034  014164  032737  000001  001134  33600           BIT     #BIT0,SAVSR1
 3035  014172  001004                  33700           BNE     .+12
 3036  014174  052777  000340  165036  33800           BIS     #340,@DPTS              ;STATUS INT ENB
 3037  014202  000403                  33900           BR      .+10
 3038  014204  052777  000301  165026  34000           BIS     #301,@DPTS
 3039                                  34100                                           ;TRANS INT ENB
 3040                                  34200                                           ;TRANS DONE
 3041  014212  032737  000001  001134  34300           BIT     #BIT0,SAVSR1
 3042  014220  001017                  34400           BNE     5$
 3043  014222  022737  000001  013470  34500           CMP     #1,FREQ                 ;TEST FOR HIGH SPEED
 3044  014230  001010                  34600           BNE     4$                      ;BRANCH IF NOT HIGH SPEED
 3045  014232  052777  000010  165000  34700   3$:     BIS     #BIT3,@DPTS             ;SET CLOCK HIGH
 3046  014240  042777  000010  164772  34800           BIC     #BIT3,@DPTS             ;SET CLOCK LOW
 3047  014246  000771                  34900           BR      3$
 3048  014250  000000                  35000           HALT
 3049                                  35100
 3050  014252  104402                  35200   4$:     RXCLK                           ;RUN SLOW CLOCK
 3051  014254  000001                  35300           1
 3052  014256  000775                  35400           BR      4$
 3053  014260  005237  001102          35500   5$:     INC     TEMP1
 3054  014264  001375                  35600           BNE     5$
 3055  014266  005337  001104          35700           DEC     TEMP2
 3056  014272  001372                  35800           BNE     5$
 3057  014274  104000                  35900           HLT
 3058  014276  000207                  36000   6$:     RTS     PC
 3059                                  36100
 3060  014300  017637  000000  001106          .DELAY: MOV     @(SP),TEMP3             ;SET UP COUNT
 3061  014306  062716  000002                          ADD     #2,(SP)
 3062  014312  011637  001110                          MOV     (SP),TEMP4
 3063  014316  022626                                  POP.SP
 3064  014320  005037  177776                          CLR     PS
 3065  014324  162737  001106                          SUB     (PC)+,TEMP3             ;FOR A SMALLER DELAY TIME
 3066  014330                          LESS.TIME:                                      ;PUT A NUMBER IN HERE TO BE
 3067  014330  000000                                  000                             ;SUBTRACTED FROM TOTAL.
 3068  014332  062737  001106                          ADD     (PC)+,TEMP3             ;FOR A LONGER DELAY TIME
 3069  014336                          MORE.TIME:                                      ;PUT A NUMBER IN HERE TO BE ADDED
 3070  014336  000000                                  000                             ;TO THE TOTAL TIME.
 3071          014340                  DEL=.
 3072  014340  162737  000001  001106                  SUB     #1,TEMP3                ;TIME OUT
 3073  014346  001374                                  BNE     DEL                     ;NO
 3074  014350  000177  164534                          JMP     @TEMP4
 3075
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3076                                        00100
3077                                        00200
3078                                        00300    ;
3079                                        00400    ;INTERRUPT SERVICE ROUTINES
3080                                        00500    ;
3081                                        00600    ;THESE ROUTINES MAY FUNCTION AS:
3082                                        00700    ; 1.  ERROR TRAPS FOR FALSE INTERRUPTS
3083                                        00800    ; 2.  POINTERS BACK TO THE MAIN LINE FOR VALID INTERRUPTS
3084                                        00900    ; 3.  FUNCTIONAL TEST WHICH ARE INTERRUPT DRIVEN
3095                                        01000
3086                                        01100    ;VERIFY THAT INTERRUPT RESULTED FROM RING.
3087  014354  032777  020000  164656        01200    TV24:   BIT     #BIT13,@DPTS    ;TEST FOR RING
3088  014362  001001                        01300            BNE     1$              ;BRANCH IF SET.
3089  014364  104000                        01400            HLT                     ;REPORT ERROR
3090                                        01500
3091  014366  042777  020000  164644        01600    1$:     BIC     #BIT13,@DPTS    ;CLEAR RING FLAG.
3092  014374  032777  020000  164636        01700            BIT     #BIT13,@DPTS    ;TEST IT
3093  014402  001401                        01800            BEQ     2$              ;BRANCH IF CLEAR.
3094  014404  104000                        01900            HLT                     ;REPORT ERROR
3095                                        02000
3096  014406  032777  140200  164624        02100    2$:     BIT     #140200,@DPTS   ;NO OTHER STATUS FLAG ON?
3097  014414  001401                        02200            BEQ     3$
3098  014416  104000                        02300            HLT                     ;REPORT ERROR
3099  014420  022626                        02400    3$:     POP.SP
3100  014422  000137  011722                02500            JMP     RCD1
31C1                                        02600
3102                                        02700    ;VERIFY THAT INTERRUPT RESULTED FROM 'CARRIER DOWN' FLAG
3103  014426  032777  100000  164604        02800    TV25:   BIT     #BIT15,@DPTS    ;TEST FOR 'CARRIER DOWN' FLAG
3104  014434  001001                        02900            BNE     1$              ;BRANCH IF SET
3105  014436  104000                        03000            HLT                     ;REPORT ERROR
3106                                        03100
3107  014440  042777  100000  164572        03200    1$:     BIC     #BIT15,@DPTS    ;CLEAR 'CARRIER DOWN' FLAG.
3108  014446  032777  100000  164564        03300            BIT     #BIT15,@DPTS    ;TEST IT
3109  014454  001401                        03400            BEQ     2$              ;BRANCH IF CLEAR.
3110  014456  104000                        03500            HLT                     ;REPORT ERROR
3111                                        03600
3112  014460  032777  060200  164552        03700    2$:     BIT     #060200,@DPTS   ;NO OTHER FLAGS ON?
3113  014466  001401                        03800            BEQ     3$
3114  014470  104000                        03900            HLT                     ;REPORT ERROR
3115                                        04000
3116  014472  013716  001174                04100    3$:     MOV     BACK,(SP)
3117  014476  000002                        04200            RTI
3118                                        04300
3119                                        04400
3120                                        04500
3121                                        04600
3122  014500  104005                        04700    FTINT:  HLT     5                       ;ERROR ROUTINE SHOULD RETURN TO MAINLINE
3123  014502  000002                        04800            RTI
3124                                        04900
3125  014504  104006                        05000    FRINT:  HLT     6                       ;ERROR ROUTINE SHOULD RETURN TO MAINLINE
3126  014506  000002                        05100            RTI
3127                                        05200
3128                                        05300
3129                                        05400
3130  014510  013777  001144  164524        05500    TV18:   MOV     TSYNC,@DPTB     ;XMIT SYNC
3131  014516  113777  001145  164520        05600            MOVB    TSYNC+1,@SEXT   ;LOAD SYNC EXT
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 3132  014524  005337  001162          05700          DEC     SCNT            ;HAVE 2 SYNC'S BEEN XMITED
 3133  014530  001003                  05800          BNE     1$              ;NO
 3134  014532  012777  014542  164512  05900          MOV     #TV19,@DPTIV    ;YES CHANGE VECTOR
 3135  014540  000002                  06000  1$:     RTI
 3136                                  06100
 3137                                  06200  ;SEQUENTIAL DATA TRANSMITTION ROUTINE
 3138                                  06300
 3139                                  06400
 3140  014542  032777  140000  164470  06500  TV19:   BIT     #140000,@DPTS   ;ANY STATUS ERRORS
 3141  014550  001401                  06600          BEQ     .+4             ;NO
 3142  014552  104000                  06700          HLT                     ;REPORT ERROR
 3143  014554  105777  164460          06800          TSTB    @DPTS           ;TRANSMITTER READY
 3144  014560  100401                  06900          BMI     .+4             ;YES
 3145  014562  104000                  07000          HLT                     ;REPORT ERROR
 3146  014564  013777  001152  164450  07100          MOV     TDATA,@DPTB     ;LOAD BUFFER
 3147  014572  005237  001152          07200          INC     TDATA           ;NEXT CHARACTER
 3148  014576  023737  001160  001152  07300          CMP     LIMIT,TDATA     ;HAVE ALL CHARACTERS
 3149  014604  001003                  07400          BNE     1$              ;NO
 3150  014606  042777  000140  164424  07500          BIC     #140,@DPTS      ;YES, CLEAR INTERRUPTS
 3151  014614  000002                  07600  1$:     RTI
 3152                                  07700
 3153                                  07800  ;RECEIVE SEQUENTIAL DATA
 3154                                  07900
 3155  014616  105777  164410          08000  RV18:   TSTB    @DPRS           ;RECEVIER DONE??
 3156  014622  100401                  08100          BMI     .+4             ;YES
 3157  014624  104000                  08200          HLT                     ;REPORT ERROR
 3158  014626  013700  001154          08300          MOV     RDATA,R0
 3159  014632  017701  164376          08400          MOV     @DPRB,R1
 3160  014636  023777  001154  164370  08500          CMP     RDATA,@DPRB     ;CORRECT DATA
 3161  014644  001404                  08600          BEQ     1$
 3162  014646  017737  164362  001136  08700          MOV     @DPRB,TMPDAT    ;STORE DATA
 3163  014654  104001                  08800          HLT     1                       ;REPORT ERROF
 3164  014656  042777  000001  164346  08900  1$:     BIC     #BIT0,@DPRS     ;CLEAR STRIP SYNC
 3165  014664  005237  001154          09000          INC     RDATA           ;NEXT CHARACTER
 3166  014670  023737  001160  001154  09100          CMP     LIMIT,RDATA
 3167  014676  001047                  09200          BNE     3$
 3169  014700  005037  001154          09300          CLR     RDATA
 3169  014704  005037  001152          09400          CLR     TDATA
 3170  014710  006237  001160          09500          ASR     LIMIT           ;DECREASE LIMIT TO 7 BITS
 3171  014714  012777  014510  164330  09600          MOV     #TV18,@DPTIV    ;SET UP SYNC TRANSMITTION
 3172  014722  012737  000004  001162  09700          MOV     #4,SCNT         ;SYNC COUNT =4
 3173  014730  052777  000001  164274  09800          BIS     #BIT0,@DPRS     ;STRIP SYNC
 3174  014736  042777  004000  164266  09900          BIC     #BIT11,@DPRS    ;CLEAR RCV ACTIVE
 3175  014744  032737  000001  001134  10000          BIT     #BIT0,SAVSR1
 3176  014752  001004                  10100          BNE     .+12
 3177  014754  052777  000340  164256  10200          BIS     #340,@DPTS      ;INT ENB + DONE
 3178  014762  000403                  10300          BR      .+10
 3179  014764  052777  000301  164246  10400          BIS     #301,@DPTS
 3180  014772  053777  001156  164232  10500          BIS     CHLEN,@DPRS     ;CHANGE CHAR LENGTH
 3181  015000  062737  000400  001156  10600          ADD     #400,CHLEN      ;DECREASE CHAR LENGTH
 3182  015006  022737  001400  001156  10700  2$:     CMP     #1400,CHLEN     ;HAVE ALL LENGTHS BEEN TESTED
 3183  015014  001401                  10800          BEQ     4$              ;YES
 3184  015016  000002                  10900  3$:     RTI                     ;NO
 3185  015020  005077  164214          11000  4$:     CLR     @DPTS           ;CLR TRANSMITTER STATUS
 3186  015024  005077  164202          11100          CLR     @DPRS           ;CLR TECEIVER STATUS
 3187  015030  005037  177776          11200          CLR     PS
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 3188  015034  013705  001350          11300          MOV     #STACK,SP
 3189  015040  000177  164130          11400          JMP     @BACK
 3190                                  11500  ;SYNC ROUTINE FOR RANDOM DATA TEST
 3191                                  11600
 3192                                  11700
 3193                                  11800  ;SYNC ROUTINE FOR RANDOM DATA TEST
 3194                                  11900
 3195  015044                          12000  RRRT:
 3196  015044  105777  164170          12100          TSTB    @DPTS           ;READY
 3197  015050  100401                  12200          BMI     .+4             ;YES
 3198  015052  104000                  12300          HLT                     ;REPORT ERROR
 3199  015054  013777  001144  164160  12400          MOV     TSYNC,@DPTB     ;TRANSMIT SYNC
 3200  015062  005337  001162          12500          DEC     SCNT            ;2 SYNC'S
 3201  015066  001006                  12600          BNE     1$              ;NO
 3202  015070  012777  015106  164154  12700          MOV     #RRT1,@DPTIV    ;YES,SET UP DATA TRANSMIT VECTOR
 3203  015076  042777  160000  164134  12800          BIC     #160000,@DPTS   ;CLEAR ERROR BITS
 3204  015104                          12900  1$:
 3205  015104  000002                  13000          RTI
 3206                                  13100
 3207                                  13200  ;RRRT, RANDOM DATA,  SYNC, RANDOM STALL
 3208                                  13300  ;TRANSMITTER SERVICE ROUTINE
 3209                                  13400
 3210  015106                          13500  RRT1:
 3211  015106  105777  164126          13600          TSTB    @DPTS           ;TRANSMITTER READY
 3212  015112  100401                  13700          BMI     .+4             ;YES
 3213  015114  104000                  13800          HLT                     ;REPORT ERROR
 3214  015116  004537  013310          13900          JSR     R5,RNUM         ;GENERATE NEXT CHARACTER
 3215  015122  010137  001152          14000          MOV     R1,TDATA
 3216  015126  043737  001156  001152  14100          BIC     CHLEN,TDATA     ;REDUCE DATA TO # BITS/CHAR
 3217  015134  013777  001152  164100  14200          MOV     TDATA,@DPTB     ;TRANSMIT CHARACTER
 3218  015142  013704  001170          14300          MOV     TP,R4           ;SET UP TRANSMITTER POINTER
 3219  015146  013724  001152          14400          MOV     TDATA,(R4)+     ;MOV CHARACTER TO TUMBLE TABLE
 3220  015152  020427  015566          14500          CMP     R4,#TOP         ;END OF TUMBLE TABLE
 3221  015156  001002                  14600          BNE     1$
 3222  015160  012704  015556          14700          MOV     #BOTTOM,R4
 3223  015164  010437  001170          14800  1$:     MOV     R4,TP           ;SAVE TRANSMITTER POINTER
 3224  015170  000002                  14900          RTI
 3225                                  15000  ;RRRR, RANDOM DATA, RANDOM SYNC, RANDOM STALL, RECEIVER SERVICE
 3226                                  15100
 3227  015172  011637  001110          15200  RRRR:   MOV     (SP),TEMP4
 3228  015176  017737  164032  001154  15300          MOV     @DPRB,RDATA     ;SAVE RECEIVED DATA
 3229  015204  013702  001172          15400          MOV     RP,R2           ;SET UP RECEIVER POINTER
 3230  015210  013701  001154          15500          MOV     RDATA,R1
 3231  015214  011200                  15600          MOV     (R2),R0
 3232  015216  023722  001154          15700          CMP     RDATA,(R2)+     ;IS DATA CORRECT
 3233  015222  001406                  15800          BEQ     1$              ;YES
 3234  015224  023737  001154  001144  15900          CMP     RDATA,TSYNC     ;IF NOT DATA IS IT SYNC
 3235  015232  001401                  16000          BEQ     .+4             ;YES
 3236  015234  104002                  16100          HLT     2               ;REPORT ERROR
 3237  015236  005742                  16200          TST     -(R2)           ;ADJUST TUMBLE TABLE
 3238  015240  022702  015566          16300  1$:     CMP     #TOP,R2         ;TOP OF TUMBLE TABLE
 3239  015244  001002                  16400          BNE     2$              ;NO
 3240  015246  012702  015556          16500          MOV     #BOTTOM,R2      ;YES,RAP AROUND
 3241  015252  010237  001172          16600  2$:     MOV     R2,RP           ;SAVE RECEIVER POINTER
 3242  015256  042777  000001  163746  16700          BIC     #BIT0,@DPRS     ;CLEAR STRIP SYNC
 3243  015264  000002                  16800          RTI
```

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                                                16900
                                                17000
                                                17100
                                                17200
                                                17300   ;TRANSMITTER SERVICE ROUTINES FOR PARITY TEST
                                                17400
015266                                          17500   TPRTY:
015266  013777  001144  163746                17600           MOV     TSYNC,@DPTB     ;XMIT SYNC CHARACTER
015274  005337  001162                        17700           DEC     SCNT            ;DEC SYNC COUNT
015300  001003                                17800           BNE     1$              ;BRANCH IF LESS THAN 2 SYNCS
015302  012777  015312  163742                17900           MOV     #2$,@DPTIV      ;SET VECTOR TO TRANSMIT DATA
015310  000002                                18000   1$:     RTI                     ;RETURN TO MAINLINE
                                                18100
015312  032777  160000  163720                18200   2$:     BIT     #160000,@DPTS   ;ANY ERRORS
015320  001401                                18300           BEQ     .+4             ;NO
015322  104000                                18400           HLT                     ;REPORT ERROR
015324  013777  001152  163710                18500           MOV     TDATA,@DPTB     ;TRANSMIT DATA
015332  005237  001152                        18600           INC     TDATA           ;INC TRANSMIT DATA
015336  023737  001152  001160                18700           CMP     TDATA,LIMIT     ;IS UPPER LIMIT REACHED
015344  00140:                                18800           BEQ     3$              ;YES, EXIT
015346  000002                                18900           RTI                     ;NO, RETURN TO MAINLINE
015350  005077  163664                        19000   3$:     CLR     @DPTS           ;CLEAR STATUS REGISTER
015354  000002                                19100           RTI
                                                19200
                                                19300   ;RECEIVER SERVICE ROUTINE FOR PARITY TEST
                                                19400
        000000                                  19500   HERE=0
                                                19600
015356  017727  163650  000000                19700   RPRTY:  MOV     @DPRS,#HERE     ;SAVE RCV STATUS HERE
015364  017737  163644  001136                19800           MOV     @DPRB,TMPDAT    ;SAVE RCV DATA
015372  013700  001154                        19900           MOV     RDATA,R0
015376  013701  001136                        20000           MOV     TMPDAT,R1
015402  023737  001136  001154                20100           CMP     TMPDAT,RDATA    ;CHECK FOR CORRECT DATA
015410  001401                                20200           BEQ     .+4             ;BRANCH IF DATA Ok
015412  104001                                20300           HLT     1               ;REPORT ERROR
015414  032737  010000  015362                20400           BIT     #BIT12,RPRTY+4  ;TEST PARITY
015422  001401                                20500   RPRT1:  BEQ     .+4             ;(RPRT1)=BEQ .+4 FOR EVEN PARITY
                                                20600                                   ;(RPRT1)=BNE .+4 FOR ODD PARITY
015424  104000                                20700           HLT                     ;REPORT ERROR
                                                20800                                   ;EXAMIN #HERE FOR STATUS
                                                20900                                   ;       TMPDAT FOR DATA
                                                21000                                   ;       RPRT1 FOR ODD EVEN
015426  005237  001154                        21100           INC     RDATA           ;INC TO NEXT EXPECTED DATA
015432  005037  001104                        21200           CLR     TEMP2           ;PARITY FLAG
015436  012737  000020  001106                21300           MOV     #16.,TEMP3      ;SET ROTATE COUNT TO 16.
015444  000241                                21400           CLC                     ;CLEAR CARRY
015446  006137  001154                        21500   RPRT2:  ROL     RDATA           ;ROTATE  DATA
015452  103002                                21600           BCC     RPRT3           ;BRANCH IF BIT IS A "0"
015454  005137  001104                        21700           COM     TEMP2           ;SET FLAG TO A "1" FOR ODD PARITY
015460  005337  001106                        21800   RPRT3:  DEC     TEMP3           ;DEC ROTATE COUNT
015464  001370                                21900           BNE     RPRT2           ;BRANCH IF 16 BIT WORD NOT CHECKED
                                                22000
                                                22100   ;IF FLAG=1 EXPECTED DATA SHOULD CAUSE ODD PARITY
                                                22200   ;BIT 12="1"
                                                22300
015466  006137  001154                        22400           ROL     RDATA           ;RESTORE EXPECTED DATA
```

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  3300  015472  005737  001104          22500            TST     TEMP2           ;TEST FOR NEXT PARITY
  3301  015476  100404                  22600            BMI     RPRT4           ;BRANCH FOR ODD PARITY
  3302  015500  052737  000400  015422  22700            BIS     #BIT8,RPRT1     ;EVEN PARITY=BEQ .+4
  3303  015506  000403                  22800            BR      RPRT5           ;
  3304  015510  042737  000400  015422  22900  RPRT4:    BIC     #BIT8,RPRT1     ;ODD PARITY=BNE .+4
  3305  015516  042777  000001  163506  23000  RPRT5:    BIC     #BIT0,@DPRS     ;CLEAR SYNC STRIP
  3306  015524  023737  001160  001154  23100            CMP     LIMIT,RDATA     ;END OF DATA
  3307  015532  001401                  23200            BEQ     RPRT6           ;YES
  3308  015534  000002                  23300            RTI                     ;NO
  3309  015536  005077  163470          23400  RPRT6:    CLR     @DPRS           ;CLEAR STATUS
  3310  015542  042737  000040  177776  23500            BIC     #BIT5,PS        ;LOWER PRIORITY
  3311  015550  062715  000002          23600            ADD     #2,(SP)         ;
  3312  015554  000002                  23700            RTI
  3313  015556  000000                  23800  BOTTOM:   0                       ;BOTTOM OF TUMBLE TABLE
  3314  015560  000000                  23900            0
  3315  015562  000000                  24000            0
  3316  015564  000000                  24100            0
  3317  015566  000000                  24200  TOP:      0
  3318                                  24300
  3319                                  24400
  3320                                  24500  ;
  3321                                  24600  ;INTERRUPT SERVICE ROUTINES FOR DB25S TESTS
  3322                                  24700  ;
  3323                                  24800  ;THESE ROUTINES MAY FUNCTION AS:
  3324                                  24900  ; 1.  ERROR TRAPS FOR FALSE INTERRUPTS
  3325                                  25000  ; 2.  POINTERS BACK TO THE MAIN LINE FOR VALID INTERRUPTS
  3326                                  25100  ; 3.  FUNCTIONAL TEST WHICH ARE INTERRUPT DRIVEN
  3327                                  25200
  3328                                  25300
  3329                                  25400
  3330  015570  105777  163436          25500  SRV5:     TSTB    @DPRS           ;RCV DONE
  3331  015574  100401                  25600            BMI     .+4
  3332  015576  104000                  25700            HLT                     ;REPORT ERRCR
  3333  015600  013700  001144          25800            MOV     TSYNC,R0
  3334  015604  017701  163424          25900            MOV     @DPRB,R1
  3335  015610  123777  001144  163416  26000            CMPB    TSYNC,@DPRB     ;CORRECT SYNC CHARACTER
  3336  015616  001401                  26100            BEQ     .+4             ;YES
  3337  015620  104001                  26200            HLT     1               ;REPORT ERROR
  3338  015622  022626                  26300            POP.SP                  ;ADJUST STACK
  3339  015624  022626                  26400            POP.SP                  ;ADJUST STACK FOR CLOCK SUB
  3340  015626  042737  000040  177776  26500            BIC     #BIT5,PS        ;LOWER PRIORITY
  3341  015634  000177  163334          26600            JMP     @BACK           ;JMP
  3342                                  26700                                    ;BACK TO MAINLINE
```

```
                                                        ;SCOPE LOOP AND INTERATION HANDLER
                                                        
015640  032737  040000  177570          .SCOPE: BIT     #BIT14,SWR
015646  001407                          TTST:   BEQ     1$
015650  000432                                  BR      3$
015652  105777  163172                          TSTB    @TKCSR
015656  100027                                  BPL     3$
015660  017700  163166                          MOV     @TKDBR,R0
015664  000412                                  BR      2$
015666  032737  004000  177570          1$:     BIT     #SW11,SWR
015674  001006                                  BNE     2$
015676  005237  001070                          INC     LPCNT
015702  023737  001070  001066                  CMP     LPCNT,ICOUNT
015710  001012                                  BNE     3$
015712  105037  001200                  2$:     CLRB    ERRFLG
015716  005037  001070                          CLR     LPCNT
015722  012737  000012  001066                  MOV     #10.,ICOUNT
015730  013737  001062  001060                  MOV     NEXT,RETURN
015736  013716  001060                  3$:     MOV     RETURN,(SP)
015742  000002                                  RTI
015744  001407                          BRW:    1407
015746  000432                          BRX:    432
                                                        
                                                        ;END OF PASS
                                                        ;TYPE "END OF PASS CSR: XXXXXX"
                                                        ;UPDATE PASS COUNT
                                                        ;UPDATE LINE NUMBER
                                                        ;IF IN CYCLE MODE
                                                        ;RESTART TEST
                                                        
015750  005037  001100                  .EOP:   CLR     LSTERR                  ;CLEAR LAST ERROR PC
015754  005037  001200                          CLR     ERRFLG                  ;CLEAR ERROR FLAG
015760  005237  001074                          INC     PASCNT                  ;UPDATE PASS COUNT
015764  104407                                  TYPE
015766  017005                                  MEPASS
015770  104413                                  CNVRT
015772  016044                                  XCSR
015774  105737  001134                          TSTB    SAVSR1
016000  100402                                  BMI     .+6
016002  005237  001146                          INC     XLINEX
016006  013737  001074  177570                  MOV     PASCNT,LIGHTS           ;DISPLAY PASS COUNT
016014  012737  001332  001060          RESTRT: MOV     #PART1,RETURN
016022  012706  001050                          MOV     #STACK,SP
016026  105737  001134                          TSTB    SAVSR1
016032  100002                                  BPL     .+6
016034  000137  001332                          JMP     PART1
016040  000137  001322                          JMP     BGNO
016044  000001                          XCSR:   1
016046     006     002                          .BYTE   6,2
016050  001232                                  DPRS
                                                        
                                                        ;CHECK FOR FREEZE ON CURRENT DATA
                                                        
016052  032737  001000  177570          .SCOP1: BIT     #SW09,SWR
016060  001402                                  BEQ     1$
```

```
 3399  016062  013716  001064                        MOV     LOCK,(SP)
 3400  016066  000002                        1$:     RTI
 3401
 3402                                                ;TELETYPE OUTPUT ROUTINE
 3403
 3404  016070  017605  000000                .TYPE:  MOV     @(SP),R5
 3405  016074  062716  000002                        ADD     #2,(SP)
 3406  016100  032737  010000  177570        1$:     BIT     #SW12,SWR
 3407  016106  001010                                BNE     3$
 3408  016110  105715                                TSTB    (R5)
 3409  016112  001406                                BEQ     3$
 3410  016114  105777  162734                2$:     TSTB    @TPCSR
 3411  016120  100375                                BPL     2$
 3412  016122  112577  162730                        MOVB    (R5)+,@TPDBR
 3413  016126  000764                                BR      1$
 3414  016130  000002                        3$:     RTI
 3415
 3416                                                ;ERROR HANDLER
 3417
 3418  016132  032737  010000  177570        .HLT:   BIT     #SW12,SWR
 3419  016140  001406                                BEQ     XBX
 3420  016142  105777  162706                        TSTB    @TPCSR
 3421  016146  100003                                BPL     XBX
 3422  016150  112777  000207  162700                MOVB    #207,@TPDBR
 3423  016156  032737  020000  177570        XBX:    BIT     #SW13,SWR
 3424  016164  001075                                BNE     HALTS
 3425  016166  021637  001100                        CMP     (SP),LSTERR
 3426  016172  001404                                BEQ     1$
 3427  016174  011637  001100                        MOV     (SP),LSTERR
 3428  016200  105037  001200                        CLRB    ERRFLG
 3429  016204  104410                        1$:     SAVOS
 3430  016206  011605                                MOV     (SP),R5
 3431  016210  162705  000002                        SUB     #2,R5
 3432  016214  011504                                MOV     (R5),R4
 3433  016216  006304                                ASL     R4
 3434  016220  061504                                ADD     (R5),R4
 3435  016222  006304                                ASL     R4
 3436  016224  042704  177001                        BIC     #177001,R4
 3437  016230  062704  017246                        ADD     #.ERRTAB,R4
 3438  016234  012437  016330                        MOV     (R4)+,ERRMSG
 3439  016240  012437  016342                        MOV     (R4)+,DATAHD
 3440  016244  011437  016354                        MOV     (R4),DATABP
 3441  016250  105737  001200                        TSTB    ERRFLG
 3442  016254  001403                                BEQ     TYPMSG
 3443  016256  005737  016354                        TST     DATABP
 3444  016262  001030                                BNE     TYPDAT
 3445  016264  104407                TYPMSG: TYPE
 3446  016266  017030                        MTSTN
 3447  016270  104413                        CNVRT
 3448  016272  016462                        XTSTN
 3449  016274  104407                        TYPE
 3450  016276  017044                        MLINE
 3451  016300  104413                        CNVRT
 3452  016302  016470                        ZLINE
 3453  016304  104407                        TYPE
 3454  016306  017053                        MERRPC
```

```
3455  016310  104413                                CNVRT
3456  016312  016454                                ERTABO
3457  016314  104407                                TYPE
3458  016316  017062                                MCRLF
3459  016320  112737  177777  001200                MOVB    #-1,ERRFLG
3460  016326  104407                                TYPE
3461  016330  000000                        ERRMSG: 0
3462  016332  005737  016342                        TST     DATAHD
3463  016336  001402                                BEQ     TYPDAT
3464  016340  104407                                TYPE
3465  016342  000000                        DATAHD: 0
3466  016344  005737  016354                TYPDAT: TST     DATABP
3467  016350  001402                                BEQ     RESREG
3468  016352  104412                                CONVRT
3469  016354  000000                        DATABP: 0
3470  016356  104411                        RESREG: RESCS
3471  016360  005737  177570                HALTS:  TST     SWR
3472  016364  100005                                BPL     EXITER
3473  016366  010046                                PUSHRO
3474  016370  016600  000002                        MOV     2(SP),RO
3475  016374  000000                                HALT
3476  016376  012600                                POPRO
3477  016400  005237  001076                EXITER: INC     ERRCNT
3478  016404  032737  000001  001134                BIT     #BIT0,SAVSR1
3479  016412  001013                                BNE     1$
3480  016414  032737  000400  177570                BIT     #SW08,SWR
3481  016422  001007                                BNE     1$
3482  016424  032737  002000  177570                BIT     #SW10,SWR
3483  016432  001407                                BEQ     2$
3484  016434  013737  001062  001060                MOV     NEXT,RETURN
3485  016442  012706  001050                1$:     MOV     #STACK,SP
3486  016446  000177  162406                        JMP     @RETURN
3487  016452  000002                        2$:     RTI
3488  016454  000001                        ERTABO: 1
3489  016456     006     002                        .BYTE   6,2
3490  016460  001122                                SAVPC
3491  016462  000001                        XTSTN:  1
3492  016464     003     002                        .BYTE   3,2
3493  016466  001072                                TSTNO
3494  016470  000001                        ZLINE:  1
3495  016472     002     002                        .BYTE   2,2
3496  016474  001146                                XLINEX
3497
3498                                                ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
3499
3500  016476  104407                        .CONVR: TYPE
3501  016500  017062                                MCRLF
3502  016502  017601  000000                .CNVRT: MOV     @(SP),R1
3503  016506  013737  017350  001106                MOV     TEMP,TEMP3
3504  016514  062716  000002                        ADD     #2,(SP)
3505  016520  012137  016670                        MOV     (R1)+,WRDCNT
3506  016524  112137  016672                1$:     MOVB    (R1)+,CHRCNT
3507  016530  112137  016673                        MOVB    (R1)+,SPACNT
3508  016534  013137  016674                        MOV     @(R1)+,BINWRD
3509  016540  013704  016674                2$:     MOV     BINWRD,R4
3510  016544  113705  016672                        MOVB    CHRCNT,R5
```

```
3511  016550  012700  017350                    MOV     #TEMP,R0
3512  016554  010403                    3$:     MOV     R4,R3
3513  016556  042703  177770                    BIC     #177770,R3
3514  016562  062703  000260                    ADD     #260,R3
3515  016566  110320                            MOVB    R3,(R0)+
3516  016570  000241                            CLC
3517  016572  006004                            ROR     R4
3518  016574  000241                            CLC
3519  016576  006004                            ROR     R4
3520  016600  000241                            CLC
3521  016602  006004                            ROR     R4
3522  016604  005305                            DEC     R5
3523  016606  001362                            BNE     3$
3524  016610  012703  017412                    MOV     #MDATA,R3
3525  016614  114023                    4$:     MOVB    -(R0),(R3)+
3526  016616  105337  016672                    DECB    CHRCNT
3527  016622  001374                            BNE     4$
3528  016624  105737  016673                    TSTB    SPACNT
3529  016630  001405                            BEQ     6$
3530  016632  112723  000240            5$:     MOVB    #240,(R3)+
3531  016636  105337  016673                    DECB    SPACNT
3532  016642  001373                            BNE     5$
3533  016644  105013                    6$:     CLRB    (R3)
3534  016646  104407                            TYPE
3535  016650  017412                            MDATA
3536  016652  005337  016670                    DEC     WRDCNT
3537  016656  001322                            BNE     1$
3538  016660  013737  001106  017350            MOV     TEMP3,TEMP
3539  016666  000002                            RTI
3540  016670  000000                    WRDCNT: 0
3541  016672  000000                    CHRCNT: 0
3542          016673                    SPACNT=CHRCNT+1
3543  016674  000000                    BINWRD: 0
3544
3545                                            ;SAVE PC OF TEST THAT FAILED AND R0-R5
3546
3547  016676  016637  000004  001132    .SAV05: MOV     4(SP),SAVPC
3548
3549                                            ;SAVE R0-R5
3550
3551  016704  010537  001126            SV05:   MOV     R5,SAVR5
3552  016710  010437  001124                    MOV     R4,SAVR4
3553  016714  010337  001122                    MOV     R3,SAVR3
3554  016720  010237  001120                    MOV     R2,SAVR2
3555  016724  010137  001116                    MOV     R1,SAVR1
3556  016730  010037  001114                    MOV     R0,SAVR0
3557  016734  000002                            RTI
3558
3559                                            ;RESTORE R0-R5
3560
3561  016736  013700  001114            .RES05: MOV     SAVR0,R0
3562  016742  013701  001116                    MOV     SAVR1,R1
3563  016746  013702  001120                    MOV     SAVR2,R2
3564  016752  013703  001122                    MOV     SAVR3,R3
3565  016756  013704  001124                    MOV     SAVR4,R4
3566  016762  013705  001126                    MOV     SAVR5,R5
```

```
  3567  016756  000002                                        RTI
  3568  016770  005015  053520  020122  27600   MPOWER: .ASCIZ <15><12>/PWR FAILED/
  3569  016776  040506  046111  042105
  3570  017004     000
  3571  017005     007  005407  042412  27700   MEPASS: .ASCIZ <7><7><15><12>/END PASS CSR: /
  3572  017012  042116  050040  051501
  3573  017020  020123  051503  035122
  3574  017026  000040
  3575  017030  005015  042524  052123  27800   MTSTN:  .ASCIZ <15><12>/TEST NO. /
  3576  017036  047040  027117  000040
  3577  017044  044514  042516  020072  27900   MLINE:  .ASCIZ /LINE: /
  3578  017052     000
  3579  017053     015  050012  035103  28000   MERRPC: .ASCIZ <15><12>/PC: /
  3580  017060  000040
  3581  017062  005015     000          28100   MCRLF:  .ASCIZ <15><12>
  3582  017065     015  042412  052116  28200   EM1:    .ASCIZ <15><12>/ENTERED FROM  /
  3583  017072  051105  042105  043040
  3584  017100  047522  020115  000040
  3585  017106  005015  051124  047101  28300   EM2:    .ASCIZ <15><12>/TRANSMITTER  /
  3586  017114  046523  052111  042524
  3587  017122  020122  000040
  3588  017126  005015  042522  042503  28400   EM3:    .ASCIZ <15><12>/RECEIVER  /
  3589  017134  053111  051105  020040
  3590  017142     000
  3591  017143     105  050130  041505  28500   DH0:    .ASCIZ /EXPECTED  RECEIVED /
  3592  017150  042524  020104  051040
  3593  017156  041505  044505  042526
  3594  017164  020104     000
  3595  017167     106  044501  042514  28600   DH1:    .ASCIZ /FAILED TO INTERUPT. /
  3596  017174  020104  047524  044440
  3597  017202  052116  051105  050125
  3598  017210  027124  000040
  3599  017214  047111  042524  052522  28700   DH2:    .ASCIZ /INTERUPTED UNEXPECTEDLY./
  3600  017222  052120  042105  052440
  3601  017230  042516  050130  041505
  3602  017236  042524  046104  027131
  3603  017244     000
  3604                                  28800
  3605          017246                  28900   .EVEN
  3606  017246                          29000   .ERRTAB:
  3607  017246  000000                  29100           0
  3608  017250  000000                  23200           0
  3609  017252  000000                  29300           0
  3610  017254  017062                  29400           MCRLF
  3611  017256  017143                  29500           DH0     ;HALT 1
  3612  017260  017320                  29600           DT0
  3613                                  29700
  3614  017262  017065                  29800           EM1
  3615  017264  017143                  29900           DH0     ;HALT 2
  3616  017266  017332                  30000           DT1
  3617                                  30100
  3618  017270  017106                  30200           EM2
  3619  017272  017167                  30300           DH1     ;HALT 3
  3620  017274  000000                  30400           0
  3621                                  30500
  3622  017276  017126                  30600           EM3
```

```
 3623  017300  017167                30700           DH1     ;HALT 4
 3624  017302  000000                30800           0
 3625                                30900
 3626  017304  017106                31000           EM2
 3627  017306  017214                31100           DH2     ;HALT 5
 3628  017310  000000                31200           0
 3629                                31300
 3630  017312  017126                31400           EM3
 3631  017314  017214                31500           DH2     ;HALT 6
 3632  017316  000000                31600           0
 3633                                31700
 3634  017320  000002                31800   DT0:    2
 3635  017322     006      004       31900           .BYTE   6,4
 3636  017324  001114                32000           SAVR0
 3637  017326     006      002       32100           .BYTE   6,2
 3638  017330  001116                32200           SAVR1
 3639                                32300
 3640  017332  000003                32400   DT1:    3
 3641  017334     006      010       32500           .BYTE   6,8.
 3642  017336  001110                32600           TEMP4
 3643  017340     006      004       32700           .BYTE   6,4
 3644  017342  001114                32800           SAVR0
 3645  017344     006      002       32900           .BYTE   6,2
 3646  017346  001116                33000           SAVR1
 3647                                33100
 3648  017350  000000                33200   TEMP:   0
 3649          017412                33300   .=.+4C
 3650  017412  000000                33400   MDATA:  0
 3651          017454                33500   .=.+40
 3652          000001                33600   .END
```

```
AND     013060            2021    2028    2037    2866#
A2ND    013562            2420    2428    2436    2970#
BACK    001174             967#   1978*   2051*   2216*   2279*   2340*   2619*   3011*   3116    3189    3341
BASCSR  001260            1030#   2725    2730
BASVEC  001256            1029#   2748
BEGIN1  001262             908    1034#
BEGIN2  007202             912    2148#
BGNO    001322            1039    1043#   3390
BGNOA   007244            2153    2159#
BINWRD  016674            3508*   3509    3543#
BITS    013054            2794*   2795    2796    2798    2801    2802    2804    2807    2808    2810    2816    2830*   2832
                          2833    2835    2838    2839    2845*   2847    2848    2857    2858    2861#
BITST   012510            1090    1092    1094    1096    1098    1100    1102    1104    1127    1130    1133    1135    1137
                          1139    1141    1143    1145    2793#
BIT0  = 000001             617#   1091    1128    1303    1334    1373    1415    1484    2161    2182    2580    2582    2594
                          2596    2613    2621    2648    2676    2683    3017    3034    3041    3164    3173    3175    3242
                          3305    3478
BIT1  = 000002             516#   1093    1131    1305    1336    1375    1485    1916    1944    2140    2884    2890    2987
BIT10 = 002000             607#   1105    1317    1387    1437    1441    1443    1953    1955    1998    2067    2092    2470
                          2481    2511    2523    2554    2926    2965    3022
BIT11 = 004000             606#   1771    1793    1797    1798    1844    1855    1868    1940    1941    2027    2035    2116
                          2233    2238    2243    2250    2295    2300    2305    2312    2344    2358    2363    2368    2376
                          2427    2435    2585    2599    3174
BIT12 = 010000             605#   1176    1472    2473    2484    2514    2526    2546    2557    3279
BIT13 = 020000             604#   1142    1346    1445    1509    1510    1540    1543    2588    3087    3091    3092
BIT14 = 040000             603#   1146    1348    1447    1475    1511    1512    1547    1550    1803    1870    2112    2252
                          2315    2378    2908    3346
BIT15 = 100000             602#   1144    1350    1449    1478    1513    1514    1554    1557    2602    2605    2624    3103
                          3107    3108
BIT2  = 000004             615#   1069    1071    1095    1129    1132    1173    1196    1221    1247    1307    1377    1404
                          1436    1440    1470    1486    1595    1623    1651    1762    1787    1908    2094    2819    2920
BIT3  = 000010             614#   1134    1338    1431    1487    2936    2941    3045    3046
BIT4  = 000020             613#   1488
BIT5  = 000040             612#   1136    1340    1433    1471    1474    1477    1539    1546    1553    1802    1867    1945
                          2109    2118    2463    2504    2539    2613    3310    3340
BIT6  = 000100             611#   1097    1138    1309    1342    1379    1435    1483    1490    1600    1629    1657    1779
                          1792    1851    1869    1917    1999    2224    2251    2287    2313    2343    2349    3033
BIT7  = 000200             610#   1099    1140    1311    1344    1381    1439    1574    2096
BIT8  = 000400             609#   1101    1313    1383    1627    1713    1826    1951    1985    2026    2033    2064    2090
                          2278    2426    2433    2503    2926    2929    2962    3019    3302    3304
BIT9  = 001000             608#   1103    1315    1385    1410    1655    2034    2228    2290    2339    2353    2434    2467
                          2478    2508    2520    2538    2543    2551
BOTTOM  015556            2871    2972    3222    3240    3313#
BPC     001142             954#   1761*   1809    1811*   1812    1835*   1879    1880*   1881    1882
BRW     015744            3364#
BRX     015746            3365#
CABLE   001150             957#   1035*   1045    2149*   2180
CHLEN   001156             960#   1984*   2018*   2025*   2032*   2414*   2425*   2432*   3018*   3180    3181*   3182    3216
CHRCNT  016672            3506*   3510    3526*   3541#   3542
CLEAR = 104404             993#   1372    1374    1376    1378    1380    1382    1384    1386    1414    1430    1432    1434
                          1438    1444    1446    1448
CLOCK = 104401             987#   2195    2220    2231    2236    2247    2283    2293    2298    2309    2346    2356    2361
                          2372    2459    2465    2476    2506    2518    2541    2549
CLRVEC  01_462            1040    1043    2154    2159    2775#
CNVRT = 104413            1007#   3379    3447    3451    3455
CONVRT= 104412            1005#   3468
```

```
DATABP  016354          3440* 3443  3466  3469#
DATAHD  016342          3439* 3462  3465#
DEL   = 014340          2938# 2940  2943# 2945  3071# 3073
DELAY = 104403           991# 1604  1633  1661  1765  1780  1837  1858  1911  1919  2095  2110  2141
                        2591  2595  2614  2622  2677  2684  2899
DH0     017143          3591# 3611  3615
DH1     017167          3595# 3619  3623
DH2     017214          3599# 3627  3631
DPRB    001234          1017# 1782  1860  1921  3159  3160  3162  3228  3273  3334  3335
DPRIV   001246          1025# 1065* 1469* 1508* 1764* 1775* 1836* 1850* 1912* 1995* 2070* 2136* 2192*
                        2246* 2280* 2308* 2371* 2462* 2502* 2537* 2873* 2960* 2974* 3029*
DPRP    001250          1026# 1066* 2193*
DPRS    001232          1016# 1063* 1069* 1071  1089  1129* 1132* 1173* 1174* 1175  1196* 1221* 1222*
                        1225  1247* 1301  1369  1371* 1404* 1436* 1440* 1442* 1470* 1573* 1595* 1623*
                        1627* 1635* 1651* 1655* 1663* 1684* 1758* 1762* 1771  1779* 1787* 1789  1792*
                        1793  1797* 1798  1809* 1830* 1851* 1855  1868* 1869* 1879* 1881* 1905* 1906
                        1908* 1917* 1937  1940* 1941  1953  1955* 1957* 1983* 1988* 1999* 2026* 2027*
                        2033* 2034* 2035* 2052* 2062* 2067* 2071* 2092* 2094* 2116* 2135* 2190* 2224*
                        2233  2243  2250* 2278* 2287* 2295  2305  2312* 2339* 2344* 2349* 2358  2368
                        2376* 2412* 2426* 2427* 2433* 2434* 2435* 2458* 2500* 2503* 2535* 2538* 2610*
                        2652* 2732  2815* 2869* 2877* 2892* 2928* 2957* 2965* 2970* 2979* 3015* 3017*
                        3022* 3033* 3155  3164* 3173* 3174* 3180* 3186* 3242* 3272  3305* 3309* 3330
                        3393
DPTB    001242          1020# 1578* 1599* 1628* 1656* 1768* 1774* 1778* 1841* 1847* 1852* 1915* 2099*
                        2102* 2105* 2108* 2464* 2505* 2540* 2655* 2878* 2978* 3130* 3146* 3199* 3217*
                        3251* 3260*
DPTIV   001252          1027# 1064* 1468* 1507* 1537* 1545* 1552* 1559* 1597* 1625* 1654* 1994* 2069*
                        2093* 2191* 2217* 2281* 2341* 2461* 2501* 2536* 2611* 2618* 2874* 2961* 2975*
                        3028* 3134* 3171* 3202* 3254*
DPTP    001254          1028# 1067* 2194* 2608*
DPTS    001240          1019# 1062* 1126  1172* 1197* 1201  1248* 1251  1270* 1273  1274  1278  1331
                        1332* 1405* 1410  1413  1419* 1424  1425  1429* 1471* 1472* 1473* 1474* 1475*
                        1476* 1477* 1478* 1479* 1483* 1484* 1485* 1486* 1487* 1488* 1489* 1490* 1509*
                        1510* 1511* 1512* 1513* 1514* 1515* 1516* 1539* 1540* 1543* 1547* 1550* 1554*
                        1557* 1574* 1575  1579  1596* 1600* 1601  1606* 1624* 1629* 1630  1636* 1653*
                        1657* 1658  1685* 1757* 1769  1776  1842  1844  1848  1853  1904* 1916* 1944*
                        1982* 2000* 2053* 2063* 2072* 2096* 2097  2100  2103  2106  2109* 2112  2115*
                        2134* 2140* 2188* 2225* 2228  2238  2251* 2286* 2290  2300  2313* 2343* 2350*
                        2353  2363  2411* 2457* 2463* 2467  2470  2473  2478  2481  2484  2499* 2504*
                        2508  2511  2514  2520  2523  2526  2534* 2539* 2543  2546  2551  2554  2557
                        2578* 2579* 2580* 2582  2585  2588  2594* 2596  2599  2602  2605* 2609* 2613*
                        2621* 2624* 2651* 2656  2667  2676* 2678  2683* 2685  2870* 2879* 2883* 2884*
                        2890* 2936* 2941* 2956* 2971* 2980* 2986* 2987* 3016* 3036* 3038* 3045* 3046*
                        3087  3091* 3092  3096  3103  3107* 3108  3112  3140  3143  3150* 3177* 3179*
                        3185* 3196  3203* 3211  3257  3265*
DTO     017320          3612  3634#
DTI     017332          3616  3640#
EM1     017065          3582# 3614
EM2     017106          3585# 3618  3626
EM3     017126          3588# 3622  3630
ERRCNT  001076           933# 2705* 3477*
ERRFLG  001200           974# 3358* 3375* 3428* 3441  3459*
ERRMSG  016330          3438* 3461#
ERTABO  016454          3456  3488#
EXITER  016400          3472  3477#
FREQ    013470          2937  2942  2949# 3043
```

```
FRINT   014504          1065    1469    1508    1764    1836    2136    2192    2280    2462    2502    2537    2960    3125#
FTINT   014500          1064    1468    1507    1559    2191    2461    2501    2536    2579    3122#
HALTS   016360          3424    3471#
HERE  = 000000          3270#   3272*
ICOUNT  001066           929#   3356    3360*
INIFLG  001176           972#
LESS.T  014330          3066#
LIGHTS= 177570           587#   3384*
LIMIT   001160           961#   1987*   1992*   2055*   2066*   2212*   2215*   2256    2274*   2277*   2318    2335*   2338*
                        2381    2929*   3021*   3026*   3148    3166    3170*   3262    3306
LINE.N  012202          1041    2157    2705#
LINE.X  012246          1044    2160    2717#   2768
LOCK    001064           928#   1682*   3399
LOGICA= 012436           888    2762#
LOKFLG  001201           975#
LPCNT   001070           930#   3355*   3356    3359*
LSTERR  001100           934#   3374*   3425    3427*
MCRLF   017062          3458    3501    3581#   3610
MDATA   017412          3524    3535    3650#
MEPASS  017005          3378    3571#
MERRPC  017053          3454    3579#
MLINE   017044          3450    3577#
MORE.T  014336          3069#
MPOWER  016770          3006    3568#
MTSTN   017030          3446    3575#
NEXT    001062           927#   1060*   1087*   1124*   1171*   1195*   1220*   1246*   1269*   1299*   1329*   1367*   1402*
                        1466*   1505*   1536*   1572*   1594*   1622*   1650*   1681*   1712*   1715    1755*   1825*   1828
                        1829    1902*   1977*   2017*   2050*   2086*   2133*   2179*   2210*   2271*   2333*   2394*   2410*
                        2455*   2497*   2576*   2647*   3361    3484
PART1   001332          1042    1045#   3385    3389
PART2   007254          1047    2158    2161#   2165
PART3   011770          2163    2184    2633#
PASCNT  001074           932#   3376*   3384
PC    =%000007           582#   1040*   1041*   1043*   1044*   2021*   2028*   2037*   2154*   2157*   2159*   2160*   2395*
                        2420*   2428*   2436*   2695*   2763*   2770*   2782*   2893*   2902*   2995*   3058*   3065    3068
POPRO = 012600           596#   3476
POP.SP= 022626           598#   1544    1551    1558    1607    1637    1664    1801    1866    1946    2117    2767    3063
                        3099    3338    3339
PCP1SP= 005726           594#
PS    = 177776           588#   1037*   1061*   1403*   1467*   1506*   1517*   1518    1538*   1546*   1553*   1598*   1626*
                        1652*   1759*   1802*   1867*   1945*   1996*   2068*   2118*   2138*   2151*   2456*   2498*   2533*
                        2577*   2612*   2620*   2933*   2955*   3030*   3064*   3187*   3310*   3340*
PUSHRO= 010046           595#   3473
PUSH.S= 024646           597#
PUSH1S= 005746           593#
PWRUP   013754          3000    3002#
RCD     011662          2609#
RCD1    011722          2618#   3100
RDATA   001154           959#   1980*   2056*   3013*   3158    3160    3165*   3166    3168*   3228*   3230    3232    3234
                        3274    3276    3286*   3290*   3299*   3306
REE     013472          2211    2272    2334    2955#
REG     013056          1089*   1126*   1301*   1331*   1369*   1413*   2795*   2797    2798    2801*   2803    2804    2807*
                        2809    2810    2813*   2815    2816    2832*   2834    2835    2838*   2847*   2853    2854    2957*
                        2862#
RESREG  016356          3467    3470#
RESTRT  016014          3385#
```

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RESOS = 104411          1003#   3470
RETURN  001060           926#   1048*   1715*   1716    1928*   2163*   2164    2165*   2184*   2185    3007    3361*   3362
                        3385*   3484*   3486
RNUM    013310          2885    2889    2900    2908#   2988    2994    3214
RP      001172           966#   2871*   2872    2972*   2973    3229    3241*
RPRTY   015356          2070    3272#   3279
RPRT1   015422          2054*   3280#   3302*   3304*
RPRT2   015446          3290#   3294
RPRT3   015460          3291    3293#
RPRT4   015510          3301    3304#
RPRT5   015516          3303    3305#
RPRT6   015536          3307    3309#
RRRR    015172          2873    2974    3227#
RRRT    015044          2874    2975    3195#
RRT1    015106          3202    3210#
RV18    014616          1995    3029    3155#
RXCLK = 104402           989#   2226    2241    2288    2303    2351    2366    2982    2990    3050
R0    =%000000           575#   1088*   1125*   1177*   1178    1198*   1199*   1202*   1203    1224*   1228*   1250*   1254*
                        1272*   1276*   1280*   1300*   1330*   1407*   1408*   1420*   1421*   1423*   1578    1599    1628
                        1656    1691*   1721*   1784*   1861*   1923*   1932*   2654*   2707*   2712*   2796*   2802*   2808*
                        2814*   2820*   2833*   2839*   2849*   2850*   2852*   3158*   3231*   3274*   3333*   3351*   3474*
                        3511*   3515*   3525    3556    3561*
R1    =%000001           576#   1175*   1176*   1178    1201*   1203    1225*   1226    1251*   1252    1273*   1424*   1692*
                        1720*   1783*   1862*   1924*   1933*   2417*   2656*   2657*   2658    2678*   2679*   2680    2714*
                        2715*   2717*   2719*   2720*   2721    2722*   2723*   2724*   2731    2749    2759*   2763    2776*
                        2777    2779    2780    2797*   2803*   2809*   2815*   2834*   2853*   2866*   2880    2886    2901
                        2910*   2911*   2912    2981    2989    3159*   3215    3230*   3275*   3334*   3502*   3505    3506
                        3507    3508    3555    3562*
R2    =%000002           577#   1909*   1947    1948    1949    1956    2418*   2653*   2655    2660*   2664*   2665*   2730*
                        2731*   2733    2734    2735    2736*   2737    2738*   2739    2740    2741    2742*   2743    2744*
                        2745*   2748*   2749*   2750    2751    2752    2753    2754    2755    2756    2775*   2777*   2778*
                        2867*   2876    2910    2912*   2913*   2914*   2915*   2916    2977    3229*   3231    3232    3237
                        3238    3240*   3241    3554    3563*
R3    =%000003           578#   1906*   1907*   1947*   1948*   2419*   2732*   2733*   2735*   2737*   2739*   2741*   2743*
                        2750*   2752*   2754*   2756*   2868*   2914    2916*   2917*   3512*   3513*   3514*   3515    3524*
                        3525*   3530*   3533*   3553    3564*
R4    =%000004           579#   3218*   3219*   3220    3222*   3223    3432*   3433*   3434*   3435*   3436*   3437*   3438
                        3439    3440    3509*   3512    3517*   3519*   3521*   3552    3565*
R5    =%000005           580#   1090*   1092*   1094*   1096*   1098*   1100*   1102*   1104*   1127*   1130*   1133*   1135*
                        1137*   1139*   1141*   1143*   1145*   2211*   2272*   2334*   2793    2794    2821*   2895*   2899*
                        2900*   2918*   2937*   2939*   2942*   2944*   2964*   2966*   2988*   2994*   3214*   3404*   3409
                        3412    3430*   3431*   3432    3434    3510*   3522*   3551    3566*
SAVPC   001132           950#   3490    3547*
SAVR0   001114           942#   3556*   3561    3636    3644
SAVR1   001116           944#   3555*   3562    3638    3646
SAVR2   001120           945#   3554*   3563
SAVR3   001122           946#   3553*   3564
SAVR4   001124           947#   3552*   3565
SAVR5   001126           948#   3551*   3566
SAVSP   001130           949#
SAVSR1  001134           951#   1713    1826    1951    1985    2064    2090    2161    2182    2648    2706*   2718*   2727
                        2746    2926    2962    3019    3034    3041    3175    3381    3397    3478
SAVSR2  001164           963#   2711*   2715    2744
SAVOS = 104410          1001#   3429
SCNT    001162           962#   1997*   2061*   2218*   2282*   2342*   2875*   2976*   3031*   3132*   3172*   3200*   3252*
SCOPE = 104400           985#   1074    1106    1147    1181    1206    1230    1256    1282    1318    1351    1388    1453
```

B07


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                       1491   1520   1560   1592   1608   1638   1665   1700   1733   1814   1884   1965   2005
                       2038   2075   2121   2144   2197   2258   2320   2383   2336   2437   2487   2523   2560
                       2625   2696
SCOP1 = 104406          997#  1596   1725
SEQ.DA  014000         2395   2695   3010#
SENT    001244         1021#  1718*  1719*  1720   1722   1729*  1730   1756*  1833*  1840*  1914*  1979*  1990*
                       2058*  2088*  2189*  2223*  2413*  2958*  3012*  3024*  3131*
SGEN    013264         2898#
SLIM    001140          953#  1760*  1806   1810*  1834*  1873   1978*
SP     =%000006         581#   897*   898*   899*   900*   901*   902*   903*   904   1036*  2150*  2929   2930
                       2831*  2844   2845   2846*  2934   2935*  3003*  3011   3060   3061*  3062   3116*  3139*
                       3227   3311*  3362*  3386*  3399*  3404   3405*  3425   3427   3430   3474   3485*  3502
                       3504*  3547
SPACNT= 016673         3507*  3529   3531*  3542#
SRVS    015570         2246   2308   2371   3330#
STACK = 001350          589#  1035   2150   3003   3188   3396   3495
STAR    001302         1038#
START1  000200          907#
STFLG   001177          973#
SVCS    016704         3551#
SWR   = 177570          586#  1048   1803   1870   2152   2252   2315   2379   2706   2707   2711   2712   2909
                       3346   3353   3397   3406   3418   3423   3471   3480   3492
SW00  = 000001          570#
SW01  = 000002          569#
SW02  = 000004          568#
SW03  = 000010          567#
SW04  = 000020          566#
SW05  = 000040          565#
SW06  = 000100          564#
SW07  = 000200          563#
SW08  = 000400          562#  3480
SW09  = 001000          561#  3397
SW10  = 002000          560#  3492
SW11  = 004000          559#  3353
SW12  = 010000          558#  3406   3418
SW13  = 020000          557#  3423
SW14  = 040000          556#
SW15  = 100000          555#
SYNC    001236         1018#  1068*  1369*  1686*  1687   1690*  1692   1693   1699*  1766*  1767   1768*  1932*
                       1839*  1875*  1913*  1998*  2020*  2060*  2069*  2139*  2157*  2222*  2254*  2255*  2314*
                       2345*  2348*  2377*  2416*  2898*  3032*
TDATA   001152          958#  1767*  1981*  2057*  2464   2505   2540   2876*  2977*  3014*  3146   3147*  3148
                       3169*  3215*  3216*  3217   3219   3260   3261*  3262
TEMP    017350         3503   3511   3538*  3648#
TEMP1   001102          938#  2693*  2925*  2930*  2932*  2934*  2946*  3053*
TEMP2   001104          939#  2694*  3055*  3287*  3292*  3300
TEMP3   001106          940#  3060*  3065*  3069*  3072*  3288*  3293*  3503*  3538
TEMP4   001110          941#  2793*  2829*  2944*  3062*  3074   3227*  3642
TEMP5   001112          942#
TIME    001166          964#  2980*  2881*  2886*  2887*  2981*  2984*  2989*  2992*
TKCSR   001050          919#  3349
TKDBR   001052          920#  3351
T.LAST = 011770        3367#
TMPDAT  001136          952#  1370*  1406*  1418*  1423   1425   1428*  1437*  1441*  1443*  1683*  1690   1691
                       1693   1697*  1717*  1719   1721   1722   1726*  1727   1782*  1783   1785   1960*  1962
                       1863   1921*  1924   1925   1929   1933   1934   2087*  2105   2109   2119*  2949*  2952
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                        3333    3335
TTST    015646          3347#
TV18    014510          1994    2217    2281    2341    2961    3028    3130#   3171
TV19    014542          3134    3140#
TV24    014354          2611    3087#
TV25    014426          2618    3103#
TYPDAT  016344          3444    3463    3466#
TYPE  = 104407           999#   3005    3377    3445    3449    3453    3457    3460    3464    3500    3534
TYPMSG  016264          3442    3445#
VALID = 104405           995#   1302    1304    1306    1308    1310    1312    1314    1316    1333    1335    1337    1339
                        1341    1343    1345    1347    1349
ARDCNT  016670          3505*   3536*   3540#
XBX     016156          3419    3421    3423#
XCSR    016044          3380    3391#
XLINEX  001146           907*    911*    956#   2717    2721*   2758*   3383*   3496
XTAG    012260          2716    2720#
XTSTN   016462          3448    3491#
ZLINE   016470          3452    3494#
$E    = 000051           522#   1060    1061#   1087    1088#   1124    1125#   1171    1172#   1195    1196#   1220    1221#
                        1246    1247#   1269    1270#   1299    1300#   1329    1330#   1367    1368#   1402    1403#   1466
                        1467#   1505    1506#   1536    1537#   1572    1573#   1594    1595#   1622    1623#   1650    1651#
                        1681    1683#   1712    1713#   1755    1756#   1825    1826#   1902    1903#   1977    1978#   2017
                        2018#   2050    2051#   2086    2087#   2133    2134#   2179    2180#   2210    2211#   2271    2272#
                        2333    2334#   2394    2395#   2410    2411#   2455    2456#   2497    2498#   2576    2577#   2647
                        2648#
$N    = 000047           522#   1053    1061#   1080    1088#   1117    1125#   1164    1172#   1188    1196#   1213    1221#
                        1239    1247#   1262    1270#   1292    1300#   1322    1330#   1360    1368#   1395    1403#   1459
                        1467#   1498    1506#   1529    1537#   1565    1573#   1597    1595#   1615    1623#   1643    1651#
                        1674    1683#   1705    1713#   1748    1756#   1818    1826#   1895    1903#   1970    1978#   2010
                        2018#   2043    2054#   2079    2087#   2126    2134#   2172    2180#   2203    2211#   2264    2272#
                        2326    2334#   2387    2395#   2403    2411#   2448    2456#   2490    2498#   2569    2577#   2640
                        2648#   3367#
$Y    = 000014           522#    976#    985     987#    989#    991#    993#    995#    997#    999#   1001#   1003#   1005#
                        1007#   1009#
.     = 017454           621#    622     624     626     628     630     632     634     636     638     640     642     644
                         646     648     650     652     654     656     658     660     662     664     666     668     670
                         672     674     676     678     680     682     684     686     688     690     692     694     696
                         698     700     702     704     706     708     710     712     714     716     718     720     722
                         724     726     728     730     732     734     736     738     740     742     744     746     748
                         750     752     754     756     758     760     762     764     766     768     770     772     774
                         776     778     780     782     784     796     788     790     792     794     796     798     900
                         802     804     806     808     810     812     814     816     818     820     922     824     926
                         828     830     832     834     836     838     840     842     944     846     948     950     952
                         854     856     858     860     862     864     866     869     870     872     874     876     879#
                         887#    889#    891#    906#    910#    914#   1016#   1017#   1018#   1019#   1020#   1021#   1025#
                        1026#   1027#   1028#   1046    1072    1179    1204    1227    1253    1275    1279    1409    1411
                        1422    1426    1576    1580    1602    1631    1659    1688    1694    1723    1731    1770    1772
                        1777    1790    1794    1799    1843    1845    1849    1854    1856    1864    1926    1930    1935
                        1938    1942    2004    2074    2098    2101    2104    2107    2113    2193    2213    2223    2237
                        2239    2244    2275    2291    2296    2301    2306    2336    2354    2359    2364    2369    2469
                        2471    2474    2479    2482    2485    2509    2512    2515    2521    2524    2527    2544    2547
                        2552    2555    2558    2583    2586    2589    2597    2600    2603    2649    2666    2668    2681
                        2686    2728    2762    2799    2805    2811    2817    2336    2851    2855    2931    2939    2943
                        3035    3037    3071    3141    3144    3156    3176    3178    3197    3212    3235    3259    3277
                        3280    3331    3336    3382    3388    3605#   3649#   3651#
.CLEAR  012752           994    2844#
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.CLOCK	013342	998	2925#		
.CNVRT	016502	1008	3502#		
.CONVR	016476	1006	3500#		
.DELAY	014300	992	3060#		
.EOP	015750	2186	2647	2650	33?4#
.ERRTA	017246	3437	3606#		
.HLT	016?32	892	3418#		
.PFAIL	013744	880	3000#	3004	
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.RXCLK	013402	990	2927	2932#	
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ASL      900  2719  2722  2723  2724  3433  3435
ASR     1910  1878  2720  3170
BCC     3291
BEG     1046  1179  1204  1227  1253  1279  1426  1688  1694  1723  1731  1772  1786  1799  1845
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DZDPAB.SRC CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

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DECB    3526  3531
EMT      599
HALT     623   625   627   629   631   633   635   637   639   641   643   645   647   649   651
         653   655   657   659   661   663   665   667   669   671   673   675   677   679   681
         683   685   687   689   691   693   695   697   699   701   703   705   707   709   711
         713   715   717   719   721   723   725   727   729   731   733   735   737   739   741
         743   745   747   749   751   753   755   757   759   761   763   765   767   769   771
         773   775   777   779   781   783   785   787   789   791   793   795   797   799   801
         803   805   807   809   811   813   815   817   819   821   823   825   827   829   831
         833   835   837   839   841   843   845   847   849   851   853   855   857   859   861
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INCB    1697  1805  1872  1990  2119  2142  3024
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SUB       898  1517  2731  3065  3072  3431
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.BLKW    1016  1017  1018  1019  1020  1021  1025  1026  1027  1028
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J07

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.REPT      522
.TITLE     552


 ERRORS DETECTED:  0
 DEFAULT GLOBALS GENERATED:  0

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 RUN-TIME RATIO: 223/50=4.4
 CORE USED:  15K  (29 PAGES)
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K07

Spooler runtime 14 Seconds, 419 KCS, 374 disk reads, 3 disk writes, 87 pages