

# CB11

TEST PROGRAM  
MD-11-DZCBH-B

EP-DZCBH-B-DL-A  
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FICHE 1 OF 1

NOV 1976  
**digital**  
MADE IN USA

This microfiche card contains a grid of 100 frames of test program data, arranged in 10 rows and 10 columns. Each frame displays a different screen of the test program, showing various data points, status indicators, and control options. The frames are densely packed and cover most of the left side of the card. The data within the frames is too small to read clearly but appears to consist of alphanumeric characters and symbols.



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INIT ERROR  
(TER) WORD#6

PROBABLE FAULT LOGIC: M7291 (D6-B2) E24

002524 004737 013374

JSR PC,HTSTS ;OUTPUT TEST # !

(TER) WORD#6  
DISPLAY SIGNIFICANCE

(PC) (PS) (SP) TEST DEV# DEVADD WAS SHOULD BE  
(R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)

002530 104004

ERY1: HLT+4 ;DEVICE ADDRESS (R2) FAILED TO INITIALIZE BY RESET

002532 032737 000400 177570  
002540 001257

SYNC ON SELECT 6 ;TEST LOCK ON ERROR SELECTED  
BIT #BITB,SWR ;(YES)BRANCHES  
BNE TST1

002542 005012  
002544 005512

LPC1: CLR (R2) ;VERIFY (WRITE)  
ADC (R2) ;VERIFY (READ/WRITE)

002546 006201  
002550 005201

ASR R1 ;ADVANCE TO NEXT DEVICE  
INC R1 ;INDEX

002552 000137 002334

JMP TS1

002556 123700 177570  
002562 001002

END1: CMPB SWR,RD ;TEST LOCK ON SUBTEST SELECTED  
BNE OUT1 ;(NO)BRANCHES

002564 000137 002300

JMP TST1 ;(YES)JUMPS

002570 104400

OUT1: SCOPE ;TEST SCOPE SELECTION

.SBTTL TST2: TEST DEVICE REGISTER DATOB RESPONSE TEST

\*\*\* BASIC LOGIC TEST \*\*\*

DATOB RESPONSE TEST

THE PURPOSE OF THIS TEST IS TO VERIFY THAT  
THE DEVICE(S) WILL NOT RESPOND TO "DATOB".  
SSYN WILL OCCURE BUT NO DATA "D LINES" TO  
DEVICE REGISTER(S) WILL TAKE PLACE.

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002572 004737 013072  
002576 012700 000002  
002602 006301  
002604 016102 016262  
002610 001515  
002612 012703 177777  
002616 005004  
002620 110312  
002622 110362 000001  
002626 110462 000002  
002632 110462 000003  
002636 110362 000004  
002642 110362 000005  
002646 110362 000006  
002652 110362 000007  
002656 011203  
002660 016104 016612  
002664 020304  
002666 001405

TST2: JSR PC,INIT0 ;CLEAR ALL REGISTERS  
MOV #2,R0 ;MOVE TEST # TO DISPLAY REGISTER>0  
TS2: ASL R1 ;FORM WORD OFFSET  
LOP2: MOV CADCSR(R1),R2 ;CURRENT DEVICE ADDRESS>R2  
BEQ END2 ;BRANCH IF ALL DEVICES TESTED  
MOV #ONES,R3  
CLR R4  
MOV R3,(R2) ;DATOB CSR  
MOV R3,1(R2) ;EVEN BYTE  
MOV R4,2(R2) ;ODD BYTE  
MOV R4,3(R2) ;DATOB DDR  
MOV R3,4(R2) ;EVEN BYTE  
MOV R3,5(R2) ;ODD BYTE  
MOV R3,6(R2) ;DATOB TSR  
MOV R3,7(R2) ;EVEN BYTE  
 ;ODD BYTE  
MOV (R2),R3 ;FETCH CURRENT CONTENTS OF CSR>R3  
MOV CVT.CB(R1),R4 ; CSR SET ADDRESS (VECTOR) BITS 08-02  
CMP R3,R4 ;VERIFY RESULTS  
BEQ TS2 ;TEST IF CSR INITIALIZED RESET

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INIT ERROR  
CSR WORD#0

PROBABLE FAULT LOGIC: M7291 (D6-B2) E24

(CSR) WORD#0  
DISPLAY SIGNIFICANCE

(PC) (PS) (SP) TEST DEV# DEVADD WAS SHOULD BE  
(R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)

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002670 104004

ERA2: HLT+4 ;DEVICE ADDRESS (R2) RESPONDING TO DATOB

PROBABLE FAULT LOGIC: M7291 (D2 C2) E35  
(D2 C4,C3) E21, E23

SYNC ON SELECT 0

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002672 032737 000400 177570  
002700 001334

BIT #BITB,SWR ;TEST FOR LOCK ON ERROR SELECTED  
BNE TST2 ;(YES) BRANCHES

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002702 005712  
002704 005012  
002706 005512

ts2: (CSR) WORD#0  
TST (R2) ;VERIFY (READ)  
CLR (R2) ;VERIFY (WRITE)  
ADC (R2) ;VERIFY (READ/WRITE)

002710 005722

TST (R2)+ ;ADVANCE TO  
(DDR) WORD#2

002712 005712  
002714 004737 011614

TST (R2) ;VERIFY (READ)  
JSR PC,OLYGMS ;DELAY 7 MILLISECOND

002720 011203  
002722 012704 177777

MOV (R2),R3 ;FETCH CONTENTS DDR>R3  
MOV #177777,R4 ;SHOULD INITIALIZE TO ALL ONES>R4

002726 020304

CMP R3,R4 ;TEST RESULTS

002730 001405

BEG LPA2 ;(OK) BRANCHES

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INIT ERROR  
(DDR) WORD#2

PROBABLE FAULT LOGIC: M7291 (D6-B2) E24

(DDR) WORD#2  
DISPLAY SIGNIFICANCE

(PC) (PS) (SP) TEST DEV# DEVADD WAS SHOULD BE  
(R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)

002732 104004

ERB2: HLT+4 ;DEVICE ADDRESS (R2) RESPONDING TO DATOB

PROBABLE FAULT LOGIC: M7291 (D2 C2) E35  
(D2 C4,C3) E21, E23

SYNC ON SELECT 2

E03

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1544 002734 032737 000400 177570 BIT #BIT8,SWR ;TEST LOCK ON ERROR SELECTED
1545 002742 001313 BNE TST2 ;(YES)BRANCHES
1546
1547
1548 002744 005012 LPA2: CLR (R2) ;VERIFY (WRITE)
1549
1550 002746 005512 ADC (R2) ;VERIFY (READ/WRITE)
1551
1552 002750 005722 TST (R2)+ ;ADVANCE TO
1553
1554
1555 002752 011203 (TSR) WORD#4
1556 MOV (R2),R3 ;FETCH CONTENTS TSR>R3
1557
1558 002754 005004 CLR R4 ;SHOULD INITIALIZE TO ALL ZEROS>R4
1559
1560 002756 005703 TST R3 ;TEST RESULTS
1561
1562 002760 001405 BEQ LPB2 ;(OK) BRANCHES

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INIT ERROR  
(TSR) WORD#4

PROBABLE FAULT LOGIC: M7291 (D6-B2) E24

(TSR) WORD#4  
DISPLAY SIGNIFICANCE

(PC) (R7)	(PS) (PSW)	(SP) (R6)	TEST (R0)	DEV# (R1)	DEVADD (R2)	WAS (R3)	SHOULD BE (R4)
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1578 002762 104004 ERC24: HLT+4 ;DEVICE ADDRESS (R2) RESPONDING TO DATOB
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PROBABLE FAULT LOGIC: M7291 (D2 C2) E35  
(D2 C4,C3) E21, E23

SYNC ON SELECT 4

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1587 002764 032737 000400 177570 BIT #BIT8,SWR ;TEST LOCK ON ERROR SELECTED
1588 002772 001277 BNE TST2 ;(YES)BRANCHES
1589
1590 002774 005012 LPB2: CLR (R2) ;VERIFY (WRITE)
1591
1592 002776 005512 ADC (R2) ;VERIFY (READ/WRITE)
1593
1594 003000 005722 TST (R2)+ ;ADVANCE TO
1595 (TSR) WORD#6
1596
1597 003002 011203 MOV (R2),R3 ;FETCH CONTENTS TSR>R3
1598
1599 003004 005004 CLR R4 ;SHOULD INITIALIZE TO ALL ZEROES>R4

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1600
1601 003006 005703          TST   R3          ;TEST RESULTS
1602
1603 003013 001407          BEQ   LPC2
1604 *****
1605
1606          INIT ERROR
1607          (TER) WORD#6
1608
1609          PROBABLE FAULT LOGIC: M7291 (D6-B2) E24
1610
1611 003012 004737 013374    JSR   PC,HTST$      ;OUTPUT TEST # 2
1612
1613          (TER) WORD#6
1614          DISPLAY SIGNIFICANCE
1615
1616          (PC) (PS) (SP) TEST DEV# DEVADD WAS SHOULD BE
1617          (R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)
1618
1619 003016 104004    ERD2:  HLT+4      ;DEVICE ADDRESS (R2) RESPONDING TO DATOB
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1621          PROBABLE FAULT LOGIC: M7291 (D2 C2) E35
1622          (D2 C4,C3) E21, E23
1623
1624
1625          SYNC ON SELECT 6
1626 003020 032737 000400 177570  BIT   #BIT8,SWR    ;TEST LOCK ON ERROR SELECTED
1627 003026 001261          BNE   TST2        ;(YES)BRANCHES
1628
1629
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1631 003030 005012    LPC2:  CLR   (R2)    ;VERIFY (WRITE)
1632 003032 005512          ADC   (R2)    ;VERIFY (READ/WRITE)
1633
1634
1635
1636 003034 006201          ASR   R1        ;ADVANCE TO NEXT DEVICE
1637 003036 0052C1          INC   R1        ;INDEX
1638
1639 003040 000137 002602    JMP   TS2
1640
1641 003044 123700 177570    END2:  CMPB  SWR,R0  ;TEST LOCK ON SUBTEST SELECTED
1642 003050 001002          BNE   OUT2      ;(NO)BRANCHES
1643
1644 003052 000137 002572    JMP   TST2      ;(YES)JUMPS
1645
1646 003056 104400    OUT2:  SCOPE      ;TEST SCOPE SELECTION
1647

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1648 .SBTTL TST3: TEST DEVICE CNTL+STATUS CSR RESPONSE SET TO ONE
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1650 000004 N=N+1
1651
1652 : *** STATIC LOGIC TESTS ***
1653 ;
1654 ; CSR SET TO ONE #BIT13
1655 ;
1656 ; THE PURPOSE OF THIS TEST IS TO VERIFY THE
1657 ; BASIC LOGIC RESPONSE (SET TO ONES/CLR TO
1658 ; ZEROES) FOR EACH CB11-HA REGISTER ADDRESS.
1659 ;
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1662
1663 003060 004737 013072 TST3: JSR PC,INIT9 ;CLEAR WORK REGISTERS R0-R4
1664 003064 012700 000003 MOV #3,R0 ;MOVE TEST# 3 TO DISPLAY R0
1665
1666 003070 006301 LOP3: ASL R1 ;FORM WORD OFFSET
1667
1668 003072 016102 016262 RA3: MOV CADCSR(R1),R2 ;CURRENT DEVICE CSR ADDRESS > R2
1669 003076 001421 BEQ END3 ;BRANCH IF ALL DEVICES TESTED
1670
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1673 003100 012704 020000 MOV #BIT13,R4 ;#BIT13 > SHOULD BE > R4
1674
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1676
1677 003104 012712 020000 MOV #BIT13,(R2) ;OUTPUT TO #BIT13 > I.E. (WRITE #BIT13 TO CSR)
1678
1679
1680 003110 056104 016612 BIS CVT.CB(R1),R4 ;CSR MASK IN VECTOR ADDRESS RESPONSE
1681 003114 011203 MOV (R2),R3 ;INPUT RESULTS (CSR ) >R3
1682
1683
1684 003116 020304 CMP R3,R4 ;VERIFY RESULTS
1685 003120 001405 BEQ RB3 ;(OK) BRANCHES
1686
1687 *****
1688
1689 :
1690 :ERR3 DEVICE CSR (R2) FAILED TO RESPOND CORRECTLY
1691 :
1692 :PROBABLE FAULT LOGIC: M7291 (D6-2B) E24
1693 :
1694 : CSR
1695 :
1696 : #BIT13 = ONE FAILURE
1697 : (D6 D2) E16
1698 :
1699 :
1700 : OR
1701 :
1702 : VECTOR PRESENTATION
1703 :

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H03

(05 D2,06) E1, E2  
(04 A6) E34

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DISPLAY SIGNIFICANCE

(PC) (PS) (SP) TEST DEV# DEVADD WAS SHOULD BE  
(R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)

003122 104004

ERR3: HLT+4 ;DEVICE CSR (R2) #BIT13 FAILED TO RESPOND CORRECTLY  
ON  
SET TO ONE

CHECK:

CSR BITS 15 THRU 13  
CSR BITS 08 THRU 02

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TEST 3 = SWITCH SETTINGS D2A6 E32 CHECK D3-D4-D5 E25-E23 SET TO ONE

003124 032737 000400 177570

BIT #BIT8,SWR ;TEST FOR LOCK ON ERROR SELECTED  
BNE RA3 ;(YES) LOOP ON CURRENT DATA ERROR

003134 006201

R83: ASR R1 ;ADVANCE  
INC R1 ;DEVICE CSR ADDRESS  
BR LOP3 ;CONTINUE

003136 005201

003140 000753

003142 123700 177570

END3: CMPB SWR,R0 ;TEST LOCK ON SUBTEST SELECTED

003146 001002

BNE OUT3 ;(NO) BRANCHES

003153 000137 003060

JMP TST3 ;YES JUMPS

003154 104400

OUT3: SCOPE ;SCOPE LOOP



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1742 .SBTTL TST4: TEST DEVICE CNTL+STATUS CSR RESPONSE SET TO ONE
1743
1744 000005 N=N+1
1745
1746 ; *** STATIC LOGIC TESTS ***
1747 ;
1748 ; CSR SET TO ONE #BIT14
1749 ;
1750 ; THE PURPOSE OF THIS TEST IS TO VERIFY THE
1751 ; BASIC LOGIC RESPONSE (SET TO ONES/CLR TO
1752 ; ZEROES) FOR EACH CB11-HA REGISTER ADDRESS.
1753 ;
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1756
1757 003156 004737 013072 TST4: JSR PC,INITG ;CLEAR WORK REGISTERS R0-R4
1758 003162 012700 000004 MOV #4,R0 ;MOVE TEST# 4 TO DISPLAY R0
1759
1760 003166 006301 LOP4: ASL R1 ;FORM WORD OFFSET
1761
1762 003170 016102 016262 RA4: MOV CADCSR(R1),R2 ;CURRENT DEVICE CSR ADDRESS > R2
1763 003174 001421 BEQ END4 ;BRANCH IF ALL DEVICES TESTED
1764
1765
1766
1767 003176 012704 040000 MOV #BIT14,R4 ;#BIT14 > SHOULD BE > R4
1768
1769
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1771 003202 012712 040000 MOV #BIT14,(R2) ;OUTPUT TO #BIT14 > I.E. (WRITE #BIT14 TO CSR)
1772
1773
1774 003206 056104 016612 BIS CVT.CB(R1),R4 ;CSR MAS IN VECTOR ADDRESS RESPONSE
1775 003212 011203 MOV (R2),R3 ;INPUT RESULT.S (CSR ) >R3
1776
1777
1778 003214 020304 CMP R3,R4 ;VERIFY RESULTS
1779 003216 001405 BEQ RB4 ;(OK) BRANCHES
1780
1781 ;*****
1782 ;
1783 ;ERR4 DEVICE CSR (R2) FAILED TO RESPOND CORRECTLY
1784 ;
1785 ;PROBABLE FAULT LOGIC: M7291 (D6-B2) E24
1786 ;
1787 ;
1788 ; CSR
1789 ;
1790 ; #BIT14 = ONE FAILURE
1791 ; (D6 D2) E16
1792 ;
1793 ;
1794 ; OR
1795 ;
1796 ; VECTOR PRESENTATION
1797 ;

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(D5 D2, D6) E1, E2  
(D4 A6) E34

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DISPLAY SIGNIFICANCE

(PC) (PS) (SP) TEST DEV# DEVADD WAS SHOULD BE  
(R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)

003220 104004

ERR4: HLT+4 ;DEVICE CSR (R2) #BIT14 FAILED TO RESPOND CORRECTLY  
ON  
SET TO ONE

CHECK:

CSR BITS 15 THRU 13  
CSR BITS 08 THRU 02

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TEST 4 = SWITCH SETTINGS D2A6 E32 CHECK D3-D4-D5 E25-E23 SET TO ONE

003222 032737 000400 177570

BIT #BIT8, SWR ;TEST FOR LOCK ON ERROR SELECTED  
BNE RA4 ;(YES) LOOP ON CURRENT DATA ERROR

003232 006201

RB4: ASR R1 ;ADVANCE  
INC R1 ;DEVICE CSR ADDRESS  
BR LOP4 ;CONTINUE

003234 005201

003236 000753

003240 123700 177570

END4: CMPB SWR, R0 ;TEST LOCK ON SUBTEST SELECTED

003244 001002

BNE OUT4 ;(NO) BRANCHES

003246 000137 003156

JMP TST4 ;YES JUMPS

003252 104400

OUT4: SCOPE ;SCOPE LOOP

1836 .SBTTL TST5: TEST DEVICE CNTL+STATUS CSR RESPONSE READ ONLY

1837  
1838 000006 N=N+1

1839  
1840 : \*\*\* STATIC LOGIC TESTS \*\*\*

1841  
1842 : CSR READ ONLY #BIT15

1843  
1844 : THE PURPOSE OF THIS TEST IS TO VERIFY THE  
1845 : BASIC LOGIC RESPONSE (SET TO ONES/CLR TO  
1846 : ZEROES) FOR EACH CB11-HA REGISTER ADDRESS.

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1850  
1851 003254 004737 013072 TST5: JSR PC,INITG ;CLEAR WORK REGISTERS R0-R4

1852 003260 012700 000005 MOV #5,R0 ;MOVE TEST# 5 TO DISPLAY R0

1853  
1854 003264 006301 LOPS: ASL R1 ;FORM WORD OFFSET

1855  
1856 003266 016102 016262 RAS: MOV CADCSR(R1),R2 ;CURRENT DEVICE CSR ADDRESS > R2

1857 003272 001421 BEQ ENDS ;BRANCH IF ALL DEVICES TESTED

1858  
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1860

1861 003274 013704 013220 MOV ZERO,R4 ;ZERO > SHOULD BE > R4

1862  
1863  
1864  
1865 003300 012712 100000 MOV #BIT15,(R2) ;OUTPUT TO #BIT15 > I.E. (WRITE #BIT15 TO CSR)

1866  
1867  
1868 003304 056104 016612 BIS CVT.CB(R1),R4 ;CSR MASK IN VECTOR ADDRESS RESPONSE

1869 003310 011203 MOV (R2),R3 ;INPUT RESULTS (CSR ) >R3

1870  
1871  
1872 003312 020304 CMP R3,R4 ;VERIFY RESULTS

1873 003314 001405 BEQ RBS ;(OK) BRANCHES

1874  
1875 ;\*\*\*\*\*

1876 ;

1877 ;

1878 ;ERRS DEVICE CSR (R2) FAILED TO RESPOND CORRECTLY

1879 ;PROBABLE FAULT LOGIC: M7291 (D6-B2) E24

1880 ;

1881 ;

1882 ; CSR

1883 ;

1884 ; #BIT15 = READ ONLY FAILURE

1885 ; (D4 C5) E7

1886 ;

1887 ; OR

1888 ; VECTOR PRESENTATION

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(D5 D2, D6) E1, E2  
(D4 A6) E34

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DISPLAY SIGNIFICANCE

(PC) (PS) (SP) TEST DEV# DEVADD WAS SHOULD BE  
(R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)

003316 104004

ERR5: HLT+4 ;DEVICE CSR (R2) #BIT15 FAILED TO RESPOND CORRECTLY  
ON  
READ ONLY

CHECK:  
CSR BITS 15 THRU 13  
CSR BITS 08 THRU 02

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TEST 5 = READ ONLY

003320 032737 000400 177570

BIT #BIT8, SWR ;TEST FOR LOCK ON ERROR SELECTED  
BNE RAS ;(YES) LOOP ON CURRENT DATA ERROR

003330 006201

RBS: ASR R1 ;ADVANCE  
INC R1 ;DEVICE CSR ADDRESS  
BR LOPS ;CONTINUE

003336 123700 177570

END5: CMPB SWR, R0 ;TEST LOCK ON SUBTEST SELECTED

003342 001002

BNE OUT5 ;(NO) BRANCHES

003344 000137 003254

JMP TST5 ;YES JUMPS  
OUT5: SCOPE ;SCOPE LOOP

003350 104400

M03

1930 .SBTTL TST6: TEST DEVICE TRN ENB REG TER RESPONSE ENABLE TO ONE

1931  
1932 000007 N=N+1

1933  
1934 ; \*\*\* STATIC LOGIC TESTS \*\*\*

1935  
1936 ; TER ENABLE TO ONE #ONES

1937  
1938 ; THE PURPOSE OF THIS TEST IS TO VERIFY THE  
1939 ; BASIC LOGIC RESPONSE (SET TO ONES/CLR TO  
1940 ; ZEROES) FOR EACH CB11-HA REGISTER ADDRESS.  
1941 ;  
1942 ;  
1943 ;  
1944 ;

1945 003352 004737 013072 TST6: JSR PC,INITQ ;CLEAR WORK REGISTERS R0-R4  
1946 003356 012700 000006 MOV #6,R0 ;MOVE TEST# 6 TO DISPLAY R0  
1947  
1948 003362 006301 LOP6: ASL R1 ;FORM WORD OFFSET  
1949  
1950 003364 016102 016524 RAB: MOV CADTER(R1),R2 ;CURRENT DEVICE TER ADDRESS > R2  
1951 003370 001417 BEQ ENDB ;BRANCH IF ALL DEVICES TESTED  
1952  
1953  
1954

1955 003372 012704 177777 MOV #ONES,R4 ;#ONES > SHOULD BE > R4  
1956  
1957

1958  
1959 003376 012712 177777 MOV #ONES,(R2) ;OUTPUT TO #ONES > I.E. (WRITE #ONES TO TER)  
1960  
1961

1962 003402 011203 MOV (R2),R3 ;INPUT RESULTS (TER ) >R3  
1963  
1964

1965 003404 020304 CMP R3,R4 ;VERIFY RESULTS  
1966 003406 001405 BEQ RAB ;(OK) BRANCHES  
1967

1968 ;\*\*\*\*\*  
1969 ;

1970 DATA ERROR

1971 ;ERR6 DEVICE TER (R2) FAILED TO RESPOND CORRECTLY  
1972 ;

1973 ;PROBABLE FAULT LOGIC: M7291 (D6-B2) E24  
1974 ;

1975 ; (D7) ALL  
1976 ; (D2 C2) E35,E36  
1977 ;

1978 ;\*\*\*\*\*  
1979 ;

1980 ;  
1981 ; DISPLAY SIGNIFICANCE  
1982 ;

1983 ; (PC) (PS) (SP) TEST DEV# DEVADD WAS SHOULD BE  
1984 ; (R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)  
1985 ;

# N03

```
1986  
1987  
1988 003410 104004 ERR6: HLT+4 ;DEVICE TER (R2) #ONES FAILED TO RESPOND CORRECTLY  
1989 ; ON  
1990 ; ENABLE TO ONE  
1991  
1992 ;*****  
1993 ;TEST 6 = ENABLE TO ONE  
1994 ;  
1995 003412 032737 000400 177570 BIT #BITS,SWR ;TEST FOR LOCK ON ERROR SELECTED  
1996 003420 001361 BNE RA6 ;(YES) LOOP ON CURRENT DATA ERROR  
1997  
1998 003422 006201 RB6: ASR R1 ;ADVANCE  
1999 003424 005201 INC R1 ;DEVICE TER ADDRESS  
2000 003426 000755 BR LOP6 ;CONTINUE  
2001  
2002 003430 123700 177570 END6: CMPB SWR,RO ;TEST LOCK ON SUBTEST SELECTED  
2003 003434 001002 BNE OUT6 ;(NO) BRANCHES  
2004 003436 000137 003352 JMP TST6 ;YES JUMPS  
2005 003442 104400 OUT6: SCOPE ;SCOPE LOOP  
2006  
2007  
2008
```

.SBTTL TST7: TEST DEVICE TRN ENB REG TER RESPONSE CLEAR TO ZERO

000010

N=N+1

\*\*\* STATIC LOGIC TESTS \*\*\*

TER CLEAR TO ZERO ZERO

THE PURPOSE OF THIS TEST IS TO VERIFY THE BASIC LOGIC RESPONSE (SET TO ONES/CLR TO ZEROES) FOR EACH CB11-HA REGISTER ADDRESS.

003444	004737	013072	TST7:	JSR	PC,INITG	;CLEAR WORK REGISTERS R0-R4
003450	012700	000007		MOV	#7,R0	;MOVE TEST# 7 TO DISPLAY R0
003454	006301		LOP7:	ASL	R1	;FORM WORD OFFSET
003456	016102	016524	RA7:	MOV	CADTER(R1),R2	;CURRENT DEVICE TER ADDRESS > R2
003462	001417			BEQ	END7	;BRANCH IF ALL DEVICES TESTED
003464	013704	013220		MOV	ZERO,R4	;ZERO > SHOULD BE > R4
003470	013712	013220		MOV	ZERO,(R2)	;OUTPUT TO ZERO > I.E. (WRITE ZERO TO TER)
003474	011203			MOV	(R2),R3	;INPUT RESULTS (TER) > R3
003476	020304			CMP	R3,R4	;VERIFY RESULTS
003500	001405			BEQ	RB7	; (OK) BRANCHES

\*\*\*\*\*

DATA ERROR

ERR7 DEVICE TER (R2) FAILED TO RESPOND CORRECTLY

PROBABLE FAULT LOGIC: M7291 (D6-B2) E24

(D7) ALL  
(D2 C2) E35,E36

\*\*\*\*\*

DISPLAY SIGNIFICANCE

(PC)	(PS)	(SP)	TEST	DEV#	DEVADD	WAS	SHOULD BE
(R7)	(PSW)	(R6)	(R0)	(R1)	(R2)	(R3)	(R4)

000010  
000020  
000030  
000040  
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000060  
000070  
000080  
000090  
000100  
000110  
000120  
000130  
000140  
000150  
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000170  
000180  
000190  
000200  
000210  
000220  
000230  
000240  
000250  
000260  
000270  
000280  
000290  
000300  
000310  
000320  
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000350  
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000370  
000380  
000390  
000400  
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000690  
000700  
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000950  
000960  
000970  
000980  
000990  
001000

C04

```

2065      :
2066      :
2067 003502 104004 ERR7: HLT+4 :DEVICE TER (R2) ZERO FAILED TO RESPOND CORRECTLY
2068      : ON
2069      : CLEAR TO ZERO
2070      :
2071      :*****
2072      : TEST 7 = SWITCH SETTINGS D2A6 E32 CHECK D3-04-05 E25-E23 CLEAR TO ZERO
2073      :
2074 003504 032737 000400 177570 BIT #BIT8,SWR :TEST FOR LOCK ON ERROR SELECTED
2075 003512 001361 BNE RA7 : (YES) LOOP ON CURRENT DATA ERROR
2076      :
2077 003514 006201 RB7: ASR R1 :ADVANCE
2078 003516 005201 INC R1 :DEVICE TER ADDRESS
2079 003520 000755 BR LOP7 :CONTINUE
2080      :
2081 003522 123700 177570 END7: CMPB SWR,R0 :TEST LOCK ON SUBTEST SELECTED
2082 003526 001002 BNE OUT7 : (NO) BRANCHES
2083 003530 000137 003444 JMP TST7 :YES JUMPS
2084 003534 104400 OUT7: SCOPE :SCOPE LOOP
2085
2086
2087

```



2088 .SBTTL TST10: TEST DEVICE TRANSITION TSR RESPONSE SET TO ONE

2089  
2090 000011 N=N+1

2091  
2092 : \*\*\* STATIC LOGIC TESTS \*\*\*  
2093  
2094 :  
2095 : TSR SET TO ONE #ONES

2096 :  
2097 : THE PURPOSE OF THIS TEST IS TO VERIFY THE  
2098 : BASIC LOGIC RESPONSE (SET TO ONES/CLR TO  
2099 : ZEROES) FOR EACH CB11-MA REGISTER ADDRESS.  
2100 :  
2101  
2102

2103 003536 004737 013072 TST10: JSR PC,INITG ;CLEAR WORK REGISTERS R0-R4  
2104 003542 012700 000010 MOV #10,R0 ;MOVE TEST# 10 TO DISPLAY R0

2105  
2106 003546 006301 LOP10: ASL R1 ;FORM WORD OFFSET

2107  
2108 003550 016102 016436 RA10: MOV CADTSR(R1),R2 ;CURRENT DEVICE TSR ADDRESS , R2  
2109 003554 001442 BEQ END10 ;BRANCH IF ALL DEVICES TESTED

2110  
2111  
2112  
2113 003556 016102 016524 MOV CADTER(R1),R2 ;TRANSITION ENABLE TER ADDRESS > R2  
2114 003562 012704 177777 MOV #ONES,R4 ;#ONES TO SHOULD BE  
2115 003566 010412 MOV R4,(R2) ;#ONES TO TER  
2116 003570 011203 MOV (R2),R3 ;FETCH RESULTS  
2117 003572 020304 CMP R3,R4 ;VERIFY RESULTS  
2118 003574 001401 BEQ RAA10 ;(OK) BRANCHES

2119  
2120 003576 104004 ETR10: HLT+4 ;TER (R2) RESPONSE FAILURE  
2121 : FAILURE TO ENABLE TO #ONES

2122  
2123 003600 016102 016262 RAA10: MOV CADCSR(R1),R2 ;TOGGIE CONTROL AND STATUS REGISTER  
2124 003604 052712 020000 BIS #20000,(R2) ;MAINTENANCE BIT 13 SET  
2125 003610 004737 011614 JSR PC,DLYGMS ;DELAY  
2126 003614 042712 020000 BIC #20000,(R2) ;MAINTENANCE BIT 13 CLEAR  
2127 003620 004737 011614 JSR PC,DLYGMS ;DELAY

2128  
2129 003624 016102 016436 MOV CADTSR(R1),R2

2130  
2131  
2132  
2133 003630 012704 177777 MOV #ONES,R4 ;#ONES > SHOULD BE > R4  
2134  
2135

2136  
2137 003634 011203 MOV (R2),R3 ;INPUT RESULTS (TSR ) >R3

2138  
2139  
2140 003636 020304 CMP R3,R4 ;VERIFY RESULTS  
2141 003640 001405 BEQ RB10 ;(OK) BRANCHES

2142  
2143 :\*\*\*\*\*

E04

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2166

DATA ERROR

ERR10 DEVICE TSR (R2) FAILED TO RESPOND CORRECTLY

PROBABLE FAULT LOGIC: M7291 (D6-B2) E24

(D8 B4)E25, (D2 C2)E35, (D6 C2)E38  
(D4 OR D5 OR D6 OR D8 OR D9) ALL

\*\*\*\*\*

DISPLAY SIGNIFICANCE

(PC) (R7)	(PS) (PSW)	(SP) (R6)	TEST (R0)	DEV# (R1)	DEVADD (R2)	WAS (R3)	SHOULD BE (R4)
--------------	---------------	--------------	--------------	--------------	----------------	-------------	-------------------

003642 104004

ERR10: HLT+4 ;DEVICE TSR (R2) #ONES FAILED TO RESPOND CORRECTLY  
ON  
SET TO ONE

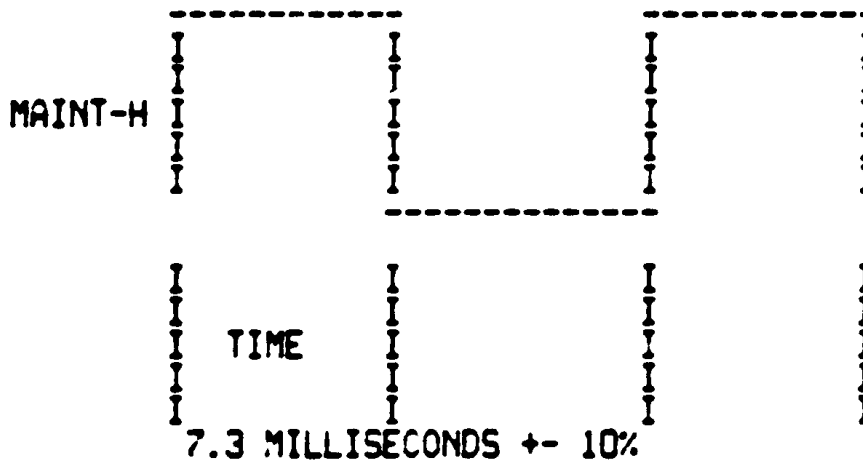
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NOTE:

AN ALL ZERO ERROR RESPONSE MAY SIGNIFY THAT THE DELAY INTERVAL CALCULATED USING THE REALTIME CLOCK IS INCORRECT, I.E. THAT THE INTERVAL IS MUCH TO FAST. THIS MAY BE VERIFIED BY CONFIGURING A SINGLE CB11-HA MODULE FOR TEST, SELECTING TEST 10 IN THE LOWER 8 BITS OF THE SWITCH REGISTER, AND INHIBITING ERROR PRINTOUTS BY SETTING SWITCH 13 OF THE SWITCH REGISTER.

VERIFY SOFTWARE TIMING BY DISPLAYING BIT 13 OF THE DEVICE "CSR" REGISTER (MAINTAINENCE). THIS WILL REQUIRE THE USE OF AN OSCILLOSCOPE. SYNC POSITIVE AND DISPLAY (MAINT H) AT D6-B2-E24 PIN 7.

THE FOLLOWING TIMING RELATIONSHIP DISPLAYED BELOW SHOULD EXIST:



\*\*\*\*\*  
TEST 10 = 10 SET TO ONE

```

003644 032737 000400 177570      BIT      #BIT8,SWR      ;TEST FOR LOCK ON ERROR SELECTED
003652 001336                      BNE      RA10        ;(YES) LOOP ON CURRENT DATA ERROR

003654 006201      RB10:  ASR      R1          ;ADVANCE
003656 005201      INC      R1          ;DEVICE TSR ADDRESS
003660 000732      BR      LOP10       ;CONTINUE

003662 123700 177570      END10:  CMPB     SWR,R0  ;TEST LOCK ON SUBTEST SELECTED
003666 001002      BNE     OUT10       ;(NO) BRANCHES
003670 000137 003536      JMP     TST10       ;YES JUMPS
003674 104400      OUT10:  SCOPE      ;SCOPE LOOP

```

```

2218 .SBTTL TST11: TEST DEVICE TRANSITION TSR RESPONSE READ ONCE
2219
2220 00001E N=N+1
2221
2222 *** STATIC LOGIC TESTS ***
2223
2224 TSR READ ONCE #ONES
2225
2226 THE PURPOSE OF THIS TEST IS TO VERIFY THE
2227 BASIC LOGIC RESPONSE (SET TO ONES/CLR TO
2228 ZEROES) FOR EACH CB11-HA REGISTER ADDRESS.
2229
2230
2231
2232
2233 003676 004737 013072 TST11: JSR PC,INITG ;CLEAR WORK REGISTERS R0-R4
2234 003702 012700 000011 MOV #11,R0 ;MOVE TEST# 11 TO DISPLAY R0
2235
2236 003706 006301 LOP11: ASL R1 ;FORM WORD OFFSET
2237
2238 003710 016102 016436 RA11: MOV CADTSR(R1),R2 ;CURRENT DEVICE TSR ADDRESS > R2
2239 003714 001443 BEQ END11 ;BRANCH IF ALL DEVICES TESTED
2240
2241
2242
2243 003716 015102 016524 MOV CADTER(R1),R2 ;TRANSITION ENABLE TER ADDRESS > R2
2244 003722 012704 177777 MOV #ONES,R4 ;#ONES TO SHOULD BE
2245 003726 010412 MOV R4,(R2) ;#ONES TO TER
2246 003730 011203 MOV (R2),R3 ;FETCH RESULTS
2247 003732 020304 CMP R3,R4 ;VERIFY RESULTS
2248 003734 001401 BEQ RAA11 ;(OK) BRANCHES
2249
2250 003736 104004 ETR11: HLT+4 ;TER (R2) RESPONSE FAILURE
2251 ; FAILURE TO ENABLE TO #ONES
2252
2253 003740 016102 016262 RAA11: MOV CADCSR(R1),R2 ;TOGGIE CONTROL AND STATUS REGISTER
2254 003744 052712 020000 BIS #20000,(R2) ;MAINTENANCE BIT 13 SET
2255 003750 004737 011614 JSR PC,DLYGMS ;DELAY
2256 003754 042712 020000 BIC #20000,(R2) ;MAINTENANCE BIT 13 CLEAR
2257 003760 004737 011614 JSR PC,DLYGMS ;DELAY
2258
2259 003764 016102 016436 MOV CADTSR(R1),R2
2260
2261
2262
2263 003770 013704 013220 MOV ZERO,R4 ;ZERO > SHOULD BE > R4
2264
2265
2266
2267 003774 011203 MOV (R2),R3 ;INPUT RESULTS (TSR ) >R3
2268
2269 003776 011203 CLR11: MOV (R2),R3 ;INPUT RESULTS (TSR) >R3(DUAL READ)
2270
2271 004000 020304 CMP R3,R4 ;VERIFY RESULTS
2272 004002 001405 BEQ RB11 ;(OK) BRANCHES
2273
    
```

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\*\*\*\*\*

DATA ERROR

ERR11 DEVICE TSR (R2) FAILED TO RESPOND CORRECTLY

PROBABLE FAULT LOGIC: M7291 (D5-2A) E24

(D8 B4)E25, (D2 C2)E35, (D6 C2)E39  
(D4 OR D5 OR D6 OR D8 OR D9) ALL

\*\*\*\*\*

DISPLAY SIGNIFICANCE

(PC) (PS) (SP) TEST DEV# DEVADD WAS SHOULD BE  
(R7) (PSW) (R6) (RC) (R1) (R2) (R3) (R4)

004004 104004

ERR11: HLT+4 ;DEVICE TSR (R2) #ONES FAILED TO RESPOND CORRECTLY  
ON  
CLR11: (ABOVE) FAILURE  
(ZERO) SECOND READ

\*\*\*\*\*

TEST 11 = SWITCH SETTINGS D2A6 E32 CHECK D3-D4-D5 E25-E23 READ ONCE

004006 032737 000400 177570

BIT #BITS,SWR ;TEST FOR LOCK ON ERROR SELECTED  
BNE R11 ;(YES) LOOP ON CURRENT DATA ERROR

004014 001335

RB11: ASR R1 ;ADVANCE  
INC R1 ;DEVICE TSR ADDRESS  
BR LOP11 ;CONTINUE

004016 006201

004020 005201

004022 000731

004024 123700 177570

END11: CMPB SWR,RD ;TEST LOCK ON SUBTEST SELECTED  
BNE OUT11 ;(NO) BRANCHES  
JMP TST11 ;YES JUMPS

004030 001002

004032 007137 003676

OU11: SCOPE ;SCOPE LOOP

004036 104400

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000013

.SBTTL TST12: TEST DEVICE CONTROL AND DATA  
N=N+1

\*\*\* STATIC LOGIC TESTS \*\*\*  
CONTROL AND DATA VARIATIONS

THE PURPOSE OF THIS TEST IS TO VERIFY THE  
CB11-HA(S) ABILITY TO PROCESS DATA PATTERNS.  
ALL PROCESSING IS STATIC (FLAGMODE) THAT IS  
NON-INTERRUPT DRIVEN.  
ACTIVITY IS UNDER CONTROL OF THE CB11-HA(S)  
CSR BIT 13 MAINT/TRANS, NO DISTRIBUTE MODULE  
PROCESSING IS DONE IN THIS TEST.

TST12: JSR PC, INITQ ; CLEAR WORK REGISTERS  
RX12: MOV #12, R0 ; MOVE TEST #12 TO DISPLAY R0  
LOP12: MOV #CNTL, R5 ; FETCH DATA TABLE ADDRESS BASE > R5  
ASL R1 ; FORM WORD OFFSET  
RA12: MOV CADCSR(R1), R2 ; CURRENT CSR ADDRESS > R2  
BNE LNKO ; BRANCH IF ALL DEVICES NOT TESTED  
JMP END12 ; JUMP IF ALL DEVICES TESTED  
LNKO: CLR 6(R2) ; CLEAR TER  
TST 4(R2) ; CLEAR TSR  
CLR (R2) ; CLEAR CSR  
ADD #6, R2 ; SET R2=TER ADDRESS  
MOV (R5), R4 ; CURRENT DATA CONFIGURATION > R4  
RB12: MOV R4, (R2) ; SET TER (TRANSITION ENABLE REGISTER)  
MOV (R2), R3 ; FETCH RESULTS  
CMP R3, R4 ; VERIFY  
BEQ LNK1 ; OK BRANCHES  
; SYNC ON SELECT 6  
SETER1: HLT+4 ; TER REGISTER RESPONSE ERROR  
; SET SWR BIT 8 TO LOOP  
; PROBABLE FAULT LOGIC: (D2 C2) E36, (D7) ALL  
; (D5 A4) E62  
; (D5 C2, D2) E1  
; (D5 C6, D6) E2  
LNK1: BIT #BIT8, SWR ; TEST LOCK ON ERROR SELECTED  
BNE RB12 ; (YES) LOOP ON CURRENT ERROR  
MOV CADCSR(R1), R2 ; SET DEVICE BASE CSR ADDRESS > R2  
MOV #20000, R4 ; SET BIT 13 > R4  
MOV R4, (R2) ; ENABLE MAINTENANCE BIT 13 > CSR  
; TOGGLE DATA REGISTER NEGATIVE [ZERO]  
JSR PC, DLYGMS ; DELAY  
BIS CVT.CB(R1), R4 ; SET VECTOR RESPONSE  
MOV (R2), R3 ; FETCH RESULTS  
BIC #BIT15, R3 ; INT/RDY (DON'T CARE)  
CMP R3, R4 ; VERIFY  
BEQ RC12 ; OK BRANCHES  
; SYNC ON SELECT 0  
SECSR1: HLT+4 ; CSR REGISTER RESPONSE ERROR

177570

100000

104004

```

2371          :                               SET SWR BIT 8 TO LOOP
2372
2373
2374          ;PROBABLE FAULT LOGIC: (D6 B2) E24
2375          ;                               (D5 D3,D6) E1, E2
2376          ;                               (D5 B4) E62
2377
2378 004170 032737 000400 177570          BIT      #BIT8,SWR          ;TEST LOCK ON ERROR SELECTED
2379 004176 001355          BNE      LNK1              ;(YES) LOOP ON CURRENT ERROR
2380
2381 004200 005004          RC12:   CLR      R4              ;RESET BIT 13>R4
2382 004202 005012          CLR      (R2)             ;DISABLE MAINTENANCE BIT13>CSR
2383          ;                               ;TOGGLE DATA RESPONSE POSITIVE [ONES]
2384 004204 004737 011614          JSR      PC,DLYGMS        ;DELAY
2385 004210 056104 016612          BIS      CVT.CB(R1),R4   ;SET VECTOR RESPONSE
2386 004214 005715          TST      (R5)            ;TEST TER DEVICE ACTIVITY
2387 004216 001402          BEQ      1$              ;(NONE) BRANCHES
2388 004220 052704 100000          BIS      #BIT15,R4       ;(ACTIVE) INT/RDY SHOULD BE = 1
2389 004224 011203          1$:    MOV      (R2),R3     ;FETCH RESULTS
2390 004226 020304          CMP      R3,R4           ;VERIFY
2391 004230 001405          BEQ      LNK3           ;OK BRANCHES
2392          ;                               SYNC ON SELECT 0
2393 004232 104004          SECSR2: HLT+4          ;CSR REGISTER RESPONSE ERROR
2394          ;                               ;SET SWR BIT 8 TO LOOP
2395
2396          ;PROBABLE FAULT LOGIC: (D6 B2) E24
2397          ;                               (D5 D3,D6) E1, E2
2398          ;                               (D5 B4) E62
2399
2400 004234 032737 000400 177570          BIT      #BIT8,SWR          ;TEST LOCK ON ERROR SELECTED
2401 004242 001356          BNE      RC12            ;(YES) LOOP ON CURRENT ERROR
2402
2403 004244 012704 140000          LNK3:   MOV      #140000,R4 ;SET BITS 15,14>R4
2404 004250 012712 040000          MOV      #40000,(R2)     ;ENABLE INTERRUPT ENABLE BIT14>CSR
2405 004254 056104 016612          BIS      CVT.CB(R1),R4   ;SET VECTOR RESPONSE
2406
2407 004260 005715          TST      (R5)            ;TEST DATA CONFIGURATION ZERO
2408 004262 001002          BNE      1$              ;(NO) BRANCHES
2409 004264 042704 100000          BIC      #100000,R4      ;ZERO CLEAR INTERRUPT READY BIT15>R4
2410
2411 004270 011203          1$:    MOV      (R2),R3     ;FETCH RESULTS
2412 004272 020304          CMP      R3,R4           ;VERIFY
2413 004274 001411          BEQ      LNK4           ;OK BRANCHES
2414          ;                               SYNC ON (4TH) SELECT 0
2415 004276 104004          ERERDY: HLT+4          ;CSR REGISTER RESPONSE ERROR
2416
2417          ;PROBABLE FAULT LOGIC: (D6 B2) E24
2418          ;                               (D5 D3,D6) E1, E2
2419          ;                               (D5 B4) E62
2420
2421          ;                               (D4 D6) E7
2422          ;                               (D6 D2) E38
2423
2424
2425 004300 005703          TST      R3              ;
2426 004302 100004          BPL      1$              ;

```





# L04

2483									
2484	004424	005703			TST	R3			; TEST IF BIT 15 FAILURE TO CLEAR
2485	004426	100002			BPL	L1\$			; (NO) BRANCHES
2486									
2487									
2488									
2489									
2490									
2491	004430	000137	004056		JMP	RA12			; NO GO LOOP
2492									
2493									
2494									
2495									
2496									
2497									
2498									
2499	004434	032737	000400	177570	L1\$:	BIT	#BIT8, SWR		; TEST LOCK ON ERROR SELECTED
2500	004442	001402				BEQ	LNK7		; (NO) BRANCHES
2501	004444	000137	004056			JMP	RA12		; (YES) JUMPS
2502	004450	005725			LNK7:	TST	(R5)+		; ADVANCE TO NEXT DATA CONFIGURATION
2503	004452	005765	177776			TST	-2(R5)		; TEST FOR END OF DATA SCAN
2504	004456	001402				BEQ	LNK8		; (YES) BRANCHES
2505	004460	000137	004056			JMP	RA12		; (NO) JUMPS
2506									
2507	004464	006201			LNK8:	ASR	R1		; ADVANCE
2508	004466	005201				INC	R1		; TO NEXT DEVICE INDEX
2509	004470	000137	004050			JMP	RX12		; CONTINUE
2510									
2511	004474	123700	177570		END12:	CMPB	SWR, R0		; TEST LOCK ON SUBTEST SELECTED
2512									
2513									
2514									
2515									
2516									
2517	004500	001002				BNE	OUT12		; (NO) BRANCHES
2518	004502	000137	004040			JMP	TST12		; (YES) JUMPS
2519									
2520									
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2533									
2534	004506	104400			OUT12:	SCOPE			; TEST SCOPE SELECTION
2535									
2536		000014				N=N+1			

:  
 :  
 : A FAILURE OF BIT 15 OF THE CURRENT CSR TO CLEAR IS UNRECOVERABLE  
 : CONTINUATION WOULD RESULT IN MISLEADING RESULTS IN DYNAMIC TESTING  
 : THIS FAILURE MUST BE CORRECTED BEFORE THE PROGRAM WILL CONTINUE  
 :  
 :  
 : NOTE:  
 : INTERMITTENT TYPE FAILURE WILL NOT HANG THE PROGRAM  
 : ONLY HARD FAILURE. THIS TEST SEQUENCE CAN BE LOCKED  
 : ON VIA THE USE OF SWR BIT'S 07 THRU 00 SET TO THE  
 : CURRENT TEST #12 FOR TROUBLE SHOOTING INTERMITTENT  
 : FAILURES.

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.SBTTL TST13: TEST DEVICE INTERRUPT CONTROL ENB

\*\*\* STATIC LOGIC TESTS \*\*\*

DEVICE INTERRUPT CONTROL

THE PURPOSE OF THIS TEST IS TO VERIFY (STATICALLY) THE INTERRUPT CONTROL LOGIC OF THE CB11-HA(S) IN NON-INTERRUPT MODE. DEVICE ACTIVITY IS UNDER THE CONTROL OF THE MAINT/TRANS BIT 13 OF THE DEVICE CSR REGISTER FOR NORMAL OPERATION AND CAN BE UNDER THE JOINT CONTROL OF A DISTRIBUTE MODULE INPUT WHEN DISTRIBUTE TIED TO THE INTERRUPT MODULE MODE OF TESTING IS SELECTED BY THE USER.

NOTE: NO DISTRIBUTE MODE OF TESTING IS ALLOWED IN MCNITOR MODE OF EXECUTION.

TEST ABILITY TO SET BIT 15 INT/RDY OF CURRENT CSR REGCTER WORD 0

THE FOLLOWING SEQUENCE OF COMMANDS ARE ISSUED

SET CSR BIT 14 VERIFY RESULTS

MOV #ONES INTO TER REGISTER VERIFY RESULTS

SET BIT13 OF CSR VERIFY RESULTS MAINT/TRANS

DELAY APPROMIMATELY 7 MILLISECONDS  
CLR BIT13 OF CSR VERIFY RESULTS MAINT/TRANS

DELAY APPROXIMATELY 7 MILLISECONDS

TEST BIT 15 OF CSR INT/RDY VERIFY SET TO ONE

TEST TSR WORD 4 NON-ZERO

N04

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2580 004510 000240          TST13: NUP
2581 004512 004737 013072    JSR      PC,INITQ      ;CLEAR WORK REGISTERS R0-R4
2582 004516 012700 000013    MOV      #13,R0        ;MOVE TEST#13 TO DISPLAY R0
2583
2584 004522 006301          LOP13: ASL      R1        ;FORM WORD OFFSET
2585 004524 013737 012430 005216 RA13:  MOV      ERRORS,RERR13 ;RECORD ERROR COUNT ON ENTRY
2586 004532 016102 016262    MOV      CADCSR(R1),R2 ;CURRENT DEVICE CSR ADDRESS>R2
2587 004536 001002          BNE      1$            ;BRANCH IF ACTIVE
2588 004540 000137 005204    JMP      END13         ;JUMP ON END OF SCAN
2589 004544 005012          1$:  CLR      (R2)        ;INIT CONTROL AND STATUS
2590 004546 005062 000006    CLR      6(R2)        ;TER
2591 004552 012704 040000    MOV      #BIT14,R4    ;#BIT14 TO SHOULD BE R4
2592 004556 052704 020000    BIS      #BIT13,R4    ;SET MAINT/TRANS BIT13 OF CSR = 1
2593
2594
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2596
2597 004562 010412          ;
2598 004564 011203          ;      SET MAINT/TRANS BIT 13 OF CSR = 1
2599 004566 056104 016612    MOV      R4,(R2)      ;#BIT14, #BIT13 TO CSR
2600 004572 020304          MOV      (R2),R3      ;FETCH RESULTS
2601 004574 001401          BIS      CVT.CB(R1),R4 ;MASK IN VECTOR ADDRESS RESPONSE
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2604 004576 104004          CMP      R3,R4        ;VERIFY RESULTS
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2611 004600 013702 002176    BEQ      RB13         ;(OK) BRANCHES
2612 004604 001002          ;*****
2613 004606 000137 004730    (CSR) SHOULD BE #BIT14
2614 004612 004737 011614    ECSR13: HLT+4        ;DEVICE CSR (R2) FAILED TO RESPOND CORRECTLY
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2630 004636 104004          ;PROBABLE FAULT LOGIC: (D2 C2) E36
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B05

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004640  
004640 012702 002176  
004644 012704 177777  
004650 010412  
004652 011203  
004654 020304  
004656 001401  
004660 104004  
004662 004737 011606  
004666 016102 016350  
004672 011203  
004674 020304  
004676 001401  
004700 104004  
004702 005004  
004704 013702 002176  
004710 005012  
004712 011203  
004714 001401  
004716 104004  
004720 004737 011606  
004724 000137 005042  
004730 016102 016524  
004734 012704 177777  
004740 010412

```
*****  
RBC13:  
*****  
:  
: DISTRIBUTE TIED TO INTERRUPT TESTING  
: DELAY FOR PREVIOUS BIT 13 OF CSR = 1  
: TOGGLE DISTRIBUTE MODULE TO #ONES VERIFY RESULTS  
:  
: MOV DSTADR,R2 ;DISTRIBUTE MODULE DEVICE ADDRESS  
: MOV #ONES,R4 ;DATA (TEST) BITS TO R4  
: MOV R4,(R2) ;SET DISTRIBUTE MODULE BITS  
: MOV (R2),R3 ;FETCH  
: CMP R3,R4 ;VERIFY  
: BEQ RDA13 ;(OK) BRANCHES  
: DISTRIBUTE MODULE RESPONSE FAILURE  
EDST13: HLT+4 ;ERROR DISTRIBUTE MODULE RESPONSE  
:  
: SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS  
: OR REMOVE CB11-HA MODULE FROM CRUTCH CARD  
:  
RDA13: JSR PC,EDLYMS ;DELAY 7.3 (X2) MILLISECONDS  
: MOV CADDR(R1),R2 ;*** NOTE IF NOT DISTRIBUTE/MODE CSR BIT 13 = 0  
: MOV (R2),R3 ;FETCH CONTENTS OF INTR/HA DATA REGISTER  
: CMP R3,R4 ;COMPARE RESULTS  
: BEQ RDB13 ;(OK) BRANCHES  
: INTERRUPT MODULE DATA REGISTER RESPONSE FAILURE  
EDDR13: HLT+4 ;DATA REGISTER (R2) RESPONSE FAILURE  
: BITS "IN" R3 SHOULD HAVE SET ACCORDING TO BITS "OUT" R4  
:  
: PROBABLE FAULT LOGIC: (DB B4) E25  
: (DB OR D9) ALL  
: IF EDST13: ERROR ABOVE  
: SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS  
RDB13: CLR R4 ;CLEAR SHOULD BE  
: MOV DSTADR,R2 ;SET DISTRIBUTE ADDRESS  
: CLR (R2) ;CLEAR DISTRIBUTE MODULE REGISTER  
: MOV (R2),R3 ;FETCH RESULTS  
: BEQ RX13 ;VERIFY (OK) BRANCHES  
: DISTRIBUTE REGISTER (R2) RESPONSE FAILURE  
EDCZ13: HLT+4 ;DEVICE DISTRIBUTE REGISTER (R2) FAILED TO CLEAR  
: DISTRIBUTE TIED TO INTERRUPT MODE OF TESTING  
:  
: SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS  
:  
RX13: JSR PC,DDLYMS ;DELAY 7.3 (X2) MILLISECONDS  
: JMP EXD13 ;VERIFY RESULTS  
:  
: NON DISTRIBUTE MODE PROCESSING  
:  
RE13: MOV CADTER(R1),R2 ;FETCH TER ADDRESS  
: MOV #ONES,R4 ;#ONES TEST DATA TO SHOULD BE  
: MOV R4,(R2) ;TO TER REGISTER
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C05

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2692 004742 011203          MOV      (R2),R3      ;FETCH RESULTS IN CSR
2693 004744 020304          CMP      R3,R4       ;VERIFY
2694 004746 001401          BEQ     R#13        ;(OK) BRANCHES
2695
2696 ;*****
2697
2698 004750 104004          EBXX13: HLT+4      ;DEVICE TER (R2) FAILED TO RESPOND CORRECTLY
2699
2700 ;PROBABLE FAULT LOGIC: (D4 D6,C2) E7, E8
2701 ;                      (D2 C2) E36
2702 ;                      (D7) ALL
2703
2704 ;*****
2705
2706
2707
2708 004752 004737 011614          RF13: JSR      PC,DLYGMS ;DELAY 7 MILLISECONDS
2709 004756 016102 016262          MOV      CADCSR(R1),R2 ;FETCH CSR ADDRESS
2710 004762 012704 040000          MOV      #BIT14,R4     ;#BIT14 TO SHOULD BE
2711 004766 052704 020000          BIS      #BIT13,R4     ;FIRST TOGGLE MAINT/TRANS =1
2712 004772 056104 016612          BIS      CVT.C9(R1),R4 ;MASK IN VECTOR RESPONSE
2713 004776 011203          MOV      (R2),R3      ;FETCH RESPONSE
2714 005000 042703 100000          BIC      #BIT15,R3     ;FIRST TOGGLE BIT 15 DON'T CARE
2715 005004 020304          CMP      R3,R4       ;VERIFY RESULTS
2716 005006 001401          BEQ     R#13        ;(OK) BRANCHES
2717
2718 005010 104004          ERF13: HLT+4      ;DEVICE CSR (R2) RESPONSE FAILURE
2719
2720 005012 042712 020000          RG13: BIC      #BIT13,(R2) ;RESET BIT 13 MAINT/TRANS CSR = 0
2721 ;                      ;SECOND TOGGLE
2722 005016 011203          MOV      (R2),R3      ;FETCH RESULTS
2723 005020 042703 100000          BIC      #BIT15,R3     ;DON'T CARE
2724 005024 042704 020000          BIC      #BIT13,R4
2725 005030 020304          CMP      R3,R4       ;VERIFY RESULTS
2726 005032 001401          BEQ     R#13        ;(OK) BRANCHES
2727
2728 005034 104004          ERH13: HLT+4      ;DEVICE CSR (R2) RESPONSE ERROR
2729
2730 ;PROBABLE FAULT LOGIC: (D2 C2) E36
2731 ;                      (D6 C2) E24
2732 ;                      (D4 D6,D7) E7, E42
2733
2734
2735 005036 004737 011614          RH13: JSR      PC,DLYGMS ;DELAY 7 MILLISECONDS
2736
2737 ;                      ;ACTIVITY VERIFICATION
2738
2739 005042 016102 016262          EXD13: MOV      CADCSR(R1),R2 ;FETCH CURRENT CSR ADDRESS
2740
2741 005046 012704 040000          MOV      #BIT14,R4     ;#BIT14 TO SHOULD BE
2742 005052 005737 002176          TST     DSTADR        ;TEST DISTB/MODE
2743 005056 001402          BEQ     1$           ;(NO) BRANCHES
2744 005060 052704 020000          BIS      #BIT13,R4     ;(YES) MAINT/TRANS BIT 13 = 1
2745 005064 005727 177777          1$: TST     #ONES        ;TEST TRANS/ENB ARGUMENT #ONES
2746 005070 001402          BEQ     2$           ;(NOT ACTIVE) BRANCHES
2747 005072 052704 100000          BIS      #BIT15,R4     ;ACTIVE SET INT/ROY BIT 15 SHOULD BE

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2748 005076 056104 016612 28:  B15  CVT.CB(R1),R4 ;MASK IN VECTOR RESPONSE
2749 005102 011203      MOV  (R2),R3 ;FETCH RESULTS
2750 005104 020304      CMP  R3,R4 ;VERIFY
2751 005106 001401      BEQ  R13 ;(OK) BRANCHES
2752 005110 104004      ERJ13: HLT+4 ;DEVICE CSR (R2) RESPONSE FAILURE
2753
2754 ;PROBABLE FAULT LOGIC: (D2 C2) E36
2755 ; (D6 C2) E24
2756 ; (D4 D6,D7) E7, E42
2757
2758
2759
2760 005112 016102 016436  RI13:  MOV  CADTSR(R1),R2 ;SET DEVICE TSR REGISTER > R2
2761 005116 011203      MOV  (R2),R3 ;:(FIRST READ) CHANGE OF STATE REGISTER TSR
2762 005120 012704 177777      MOV  #ONES,R4 ;APPROPRIATE BITS TO SHOULD BE
2763 005124 020304      CMP  R3,R4 ;VERIFY RESULTS
2764 005126 001401      BEQ  R13 ;(OK) BRANCHES
2765 ; TRANSITION STATE REGISTER RESPONSE FAILURE
2766 005130 104004      ETSR13: HLT+4 ;DEVICE TSR (R2) RESPONSE FAILURE
2767 ; BITS "IN" R3 SHOULD HAVE SET ACCORDING TO BITS "OUT" R4
2768
2769 ;PROBABLE FAULT LOGIC: (D4 OR D5) ALL
2770 ; (D6) ALL
2771 ; (D7) ALL
2772 ; (D8 OR D9) ALL
2773
2774
2775 005132 016102 016436  RJ13:  MOV  CADTSR(R1),R2 ;SET DEVICE TSR ADDRESS>R2
2776 005136 005004      CLR  R4 ;CLR SHOULD BE
2777 005140 011203      MOV  (R2),R3 ;FETCH CONTENTS OF TSR
2778 005142 020304      CMP  R3,R4 ;VERIFY RESULTS
2779 005144 001401      BEQ  R13 ;(OK) BRANCHES
2780
2781 ;*****
2782 ; TSR (R2) RESPONSE FAILURE
2783
2784 005146 104004      ERK13: HLT+4 ;DEVICE TSR (R2) FAILED TO RESPOND CORRECTLY
2785 ; SHOULD HAVE CLEARED BY FIRST READ ABOVE (RI13)
2786 ;PROBABLE FAULT LOGIC: (D4 OR D5) ALL
2787 ; (D6) ALL
2788 ; (D7) ALL
2789 ; (D8 OR D9) ALL
2790
2791 ;*****
2792
2793 005150 023737 012430 005216 RK13:  CMP  ERRORS,RERR13 ;TEST ANY ERRORS RECORED
2794 ; (NO) BRANCHES
2795 005156 001004      BNE  R13 ;(YES) BRANCHES
2796
2797 005160 006201      LOPX13: ASR  R1 ;ADVANCE TO
2798 005162 005201      INC  R1 ;NEXT DEVICE
2799 005164 000137 004522      JMP  LOP13 ;CONTINUE
2800
2801 005170 032737 000400 177570 RL13:  BIT  #BIT8,SWR ;TEST LOCK ON ERROR SELECTED
2802 005176 001770      BEQ  LOPX13 ;(NO) BRANCHES
2803 005200 000137 004524      JMP  RA13 ;(YES) JUMPS

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MAINDEC-11-DZCBH-8  
DZCBHB.P11

CS11-HP LOGIC TEST  
TST13: TEST DEVICE INTERRUPT CONTROL ENB

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005204 123700 177570  
005210 001003  
005212 000137 004510  
005216 000000  
005220 104400  
000015

END13: CMPB SWR,RO  
BNE OUT13  
JMP TST13  
RERR13:0  
OUT13: SCOPE  
N=N+1

;TEST LOCK ON SUBTEST SELECTED  
;(NO) BRANCHES  
;(YES)JUMPS  
:RECORD ERROR COUNT ENTRY

.SBTTL TST14: TEST DEVICE INTERRUPT CONTROL DSB

\*\*\* STATIC LOGIC TESTS \*\*\*

DEVICE INTERRUPT CONTROL

THE PURPOSE OF THIS TEST IS TO VERIFY (STATICALLY) THE INTERRUPT CONTROL LOGIC OF THE CB11-HA(S) IN NON-INTERRUPT MODE. DEVICE ACTIVITY IS UNDER THE CONTROL OF THE MAINT/TRANS BIT 13 OF THE DEVICE CSR REGISTER FOR NORMAL OPERATION AND CAN BE UNDER THE JOINT CONTROL OF A DISTRIBUTE MODULE INPUT WHEN DISTRIBUTE TIED TO THE INTERRUPT MODULE MODE OF TESTING IS SELECTED BY THE USER.

NOTE:

NO DISTRIBUTE MODE OF TESTING IS ALLOWED IN MONITOR MODE OF EXECUTION.

TEST ABILITY TO INHIBIT SETTING BIT 15 INT/RDY OF CURRENT CSR REGISTER WORD 0

THE FOLLOWING SEQUENCE OF COMMANDS ARE ISSUED

SET CSR BIT 14 VERIFY RESULTS

MOV ZERO INTO TER REGISTER      VERIFY RESULTS

SET BIT13 OF CSR      VERIFY RESULTS    MAINT/TRANS

DELAY APPROXIMATELY 7 MILLISECONDS

CLR BIT13 OF CSR      VERIFY RESULTS    MAINT/TRANS

DELAY APPROXIMATELY 7 MILLISECONDS

TEST BIT 15 OF CSR INT/RDY VERIFY SET TO ZERO

TEST TSR WORD 4 ZERO

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G05

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2857 005222 000240          TST14: NUP
2858 005224 004737 013072          JSR    PC,INITQ      ;CLEAR WORK REGISTERS R0-R4
2859 005230 012700 000014          MOV    #14,R0        ;MOVE TEST#14 TO DISPLAY R0
2860
2861 005234 006301          LOP14: ASL    R1      ;FORM WORD OFFSET
2862 005236 013737 012430 005730 RA14: MOV    ERRORS,RERR14 ;RECORD ERROR COUNT ON ENTRY
2863 005244 016102 016262          MOV    CADCSR(R1),R2 ;CURRENT DEVICE CSR ADDRESS>R2
2864 005250 001002          BNE    1$           ;BRANCH IF ACTIVE
2865 005252 000137 005716          JMP    END14        ;JUMP ON END OF SCAN
2866 005256 005012          1$:  CLR    (R2)      ;INIT CONTROL AND STATUS
2867 005260 005062 000000          CLR    6(R2)        ;TER
2868 005264 012704 040000          MOV    #BIT14,R4    ;#BIT14 TO SHOULD BE R4
2869 005270 052704 020000          BIS    #BIT13,R4    ;SET MAINT/TRANS BIT13 OF CSR = 1
2870
2871
2872          ; SET MAINT/TRANS BIT 13 OF CSR = 1
2873
2874          MOV    R4,(R2)    ;#BIT14, #BIT13 TO CSR
2875          MOV    (R2),R3    ;FETCH RESULTS
2876          BIS    CVT.CB(R1),R4 ;MASK IN VECTOR ADDRESS RESPONSE
2877          CMP    R3,R4      ;VERIFY RESULTS
2878          BEQ    RB14      ;(OK) BRANCHES
2879          ;*****
2880          ;(CSR) SHOULD BE #BIT14
2881 005310 104004          ECSR14: HLT+4 ;DEVICE CSR (R2) FAILED TO RESPOND CORRECTLY
2882
2883          ;PROBABLE FAULT LOGIC: (D2 C2) E36
2884          ; (D6 B2) E24
2885          ; (D4 D7,D6) E42, E7
2886
2887          ;*****
2888 005312 013702 002176          RB14: MOV    DSTADR,R2    ;FETCH DISTRIBUTE ADDRESS
2889 005316 001002          BNE    1$           ;ACTIVE BRANCHES
2890 005320 000137 005442          JMP    RE14        ;(NOT DISTR/MODE) JUMPS
2891 005324 004737 011614          1$:  JSR    PC,DLYGMS    ;DELAY 7 MILLISECONDS
2892
2893          ; DISTRIBUTE TIED TO INTERRUPT MODE PROCESSING
2894
2895 005330 016102 016524          MOV    CADTER(R1),R2 ;CURRENT DEVICE TER ADDRESS>R2
2896 005334 012704 177777          MOV    #ONES,R4
2897 005340 010412          MOV    R4,(R2)      ;ONES TO TER REGISTER
2898
2899          ; ALL ONES ENABLE TER REGISTER
2900
2901          MOV    (R2),R3    ;FETCH RESULTS
2902          CMP    R3,R4      ;VERIFY RESULTS
2903          BEQ    RBC14    ;(OK) BRANCHES
2904
2905          ;*****
2906
2907 005350 104004          ETER14: HLT+4 ;DEVICE TER (R2) FAILED TO RESPOND CORRECTLY
2908
2909          ;PROBABLE FAULT LOGIC: (D4 C2,D6) E8, E7
2910          ; (D2 C2) E36
2911          ; (D7) ALL
2912

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# H05

MAINDEC-11-DZCBH-5      CB11-4A LOGIC TEST      MACY11 27(732)      11-OCT-76      10:43      PAGE 60  
DZCBHB.P11      TST14: TEST DEVICE INTERRUPT CONTROL DSB

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2915 005352
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2922 005352 013702 002176
2923 005356 013704 013220
2924 005362 010412
2925 005364 011203
2926 005366 020304
2927 005370 001401
2928
2929 005372 104004
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2935 005374 004737 011606
2936 005400 016102 016350
2937 005404 011203
2938 005406 020304
2939 005410 001401
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2941 005412 104004
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2949 005414 005004
2950 005416 013702 002176
2951 005422 005012
2952 005424 011203
2953 005426 001401
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2955 005430 104004
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2960
2961 005432 004737 011606
2962 005436 000137 005554
2963
2964
2965
2966 005442 016102 016524
2967 005446 013704 013220
2968 005452 010412
```

\*\*\*\*\*  
RBC14:  
\*\*\*\*\*

;  
DISTRIBUTE TIED TO INTERRUPT TESTING  
;  
DELAY FOR PREVIOUS BIT 13 OF CSR = 1  
;  
TOGGLE DISTRIBUTE MODULE TO ZERO VERIFY RESULTS  
;  
MOV DSTADR,R2 ;DISTRIBUTE MODULE DEVICE ADDRESS  
MOV ZERO,R4 ;DATA (TEST) BITS TO R4  
MOV R4,(R2) ;SET DISTB MODULE BITS  
MOV (R2),R3 ;FETCH  
CMP R3,R4 ;VERIFY  
BEQ RDA14 ;(OK) BRANCHES  
;  
DISTRIBUTE MODULE RESPONSE FAILURE  
EDST14: HLT+4 ;ERRCP DISTRIBUTE MODULE RESPONSE  
;  
SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS  
;  
OR REMOVE CB11-HA MODULE FROM CRUTCH CARD  
;  
RDA14: JSR PC,DDLIMS ;DELAY 7.3 (X2) MILLISECONDS  
MOV CADDR(R1),R2 ;\*\*\* NOTE IF NOT DISTB/MODE CSR BIT 13 = 0  
MOV (R2),R3 ;FETCH CONTENTS OF INTR/HA DATA REGISTER  
CMP R3,R4 ;COMPARE RESULTS  
BEQ RDB14 ;(OK) BRANCHES  
;  
INTERUPT MODULE DATA REGISTER RESPONSE FAILURE  
EDDR14: HLT+4 ;DATA REGISTER (R2) RESPONSE FAILURE  
;  
BITS "IN" R3 SHOULD HAVE SET ACCORDING TO BITS "OUT" R4  
;  
;  
PROBABLE FAULT LOGIC: (DB B4) E25  
;(DB OR D9) ALL  
;  
IF EDST14: ERROR ABOVE  
;  
SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS  
RDB14: CLR R4 ;CLEAR SHOULD BE  
MOV DSTADR,R2 ;SET DISTRIBUTE ADDRESS  
CLR (R2) ;CLEAR DISTB MODULE REGISTER  
MOV (R2),R3 ;FETCH RESULTS  
BEQ RX14 ;VERIFY (OK) BRANCHES  
;  
DISTRIBUTE REGISTER (R2) RESPONSE FAILURE  
EDDZ14: HLT+4 ;DEVICE DISTRIBUTE REGISTER (R2) FAILED TO CLEAR  
;  
DISTRIBUTE TIED TO INTERRUPT MODE OF TESTING  
;  
SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS  
;  
RX14: JSR PC,DDLIMS ;DELAY 7.3 (X2) MILLISECONDS  
JMP EXD14 ;VERIFY RESULTS  
;  
NON DISTRIBUTE MODE PROCESSING  
;  
RE14: MOV CADTER(R1),R2 ;FETCH TER ADDRESS  
MOV ZERO,R4 ;ZERO TEST DATA TO SHOULD BE  
MOV R4,(R2) ;TO TER REGISTER

```

2969 005454 011203          MOV      (R2),R3          ;FETCH RESULTS IN CSR
2970 005456 020304          CMP      R3,R4           ;VERIFY
2971 005460 001401          BEQ     RF14            ;(OK) BRANCHES
2972
2973
2974
2975 005462 104004          EBXX14: HLT+4           ;DEVICE TER (R2) FAILED TO RESPOND CORRECTLY
2976
2977
2978          ;PROBABLE FAULT LOGIC: (D4 D6,C2) E7, E8
2979          ;                   (D2 C2) E36
2980          ;                   (D7) ALL
2981
2982
2983          ;*****
2984
2985 005464 004737 011614          RF14:   JSR      PC,DLYGMS          ;DELAY 7 MILLISECONDS
2986 005470 016102 016262          MOV     CADCSR(R1),R2      ;FETCH CSR ADDRESS
2987 005474 012704 040000          MOV     #BIT14,R4         ;#BIT14 TO SHOULD BE
2988 005500 052704 020000          BIS     #BIT13,R4         ;FIRST TOGGLE MAINT/TRANS =1
2989 005504 056104 016612          BIS     CVT.CB(R1),R4     ;MASK IN VECTOR RESPONSE
2990 005510 011203          MOV     (R2),R3           ;FETCH RESPONSE
2991 005512 042703 100000          BIC     #BIT15,R3         ;FIRST TOGGLE BIT 15 DON'T CARE
2992 005516 020304          CMP     R3,R4             ;VERIFY RESULTS
2993 005520 001401          BEQ     RG14            ;(OK) BRANCHES
2994
2995 005522 104004          ERF14: HLT+4           ;DEVICE CSR (R2) RESPONSE FAILURE
2996
2997 005524 042712 020000          RG14:   BIC     #BIT13,(R2)      ;RESET BIT 13 MAINT/TRANS CSR = 0
2998          ;SECOND TOGGLE
2999 005530 011203          MOV     (R2),R3           ;FETCH RESULTS
3000 005532 042703 100000          BIC     #BIT15,R3         ;DON'T CARE
3001 005536 042704 020000          BIC     #BIT13,R4
3002 005542 020304          CMP     R3,R4             ;VERIFY RESULTS
3003 005544 001401          BEQ     RH14            ;(OK) BRANCHES
3004
3005 005546 104004          ERH14: HLT+4           ;DEVICE CSR (R2) RESPONSE ERROR
3006
3007
3008          ;PROBABLE FAULT LOGIC: (D2 C2) E36
3009          ;                   (D6 C2) E24
3010          ;                   (D4 D6,D7) E7, E42
3011
3012 005550 004737 011614          RH14:   JSR      PC,DLYGMS          ;DELAY 7 MILLISECONDS
3013
3014          ;ACTIVITY VERIFICATION
3015
3016 005554 016102 016262          EXD14:  MOV     CADCSR(R1),R2      ;FETCH CURRENT CSR ADDRESS
3017
3018 005560 012704 040000          MOV     #BIT14,R4         ;#BIT14 TO SHOULD BE
3019 005564 005737 002176          TST     DSTADR           ;TEST DISTB/MODE
3020 005570 001402          BEQ     1$              ;(NO) BRANCHES
3021 005572 052704 020000          BIS     #BIT13,R4         ;(YES) MAINT/TRANS BIT 13 = 1
3022 005576 005737 013220          1$:    TST     ZERO           ;TEST TRANS/ENB ARGUMENT ZERO
3023 005602 001402          BEQ     2$              ;(NOT ACTIVE) BRANCHES
3024 005604 052704 100000          BIS     #BIT15,R4         ;ACTIVE SET INT/RDY BIT 15 SHOULD BE

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3025 005610 056104 016612 2S:  B1S  CVT.CB(R1),R4 ;MASK IN VECTOR RESPONSE
3026 005614 011203          MOV  (R2),R3 ;FETCH RESULTS
3027 005616 020304          CMP  R3,R4 ;VERIFY
3028 005620 001401          BEQ  R114 ;(OK) BRANCHES
3029
3030 005622 104004          ERJ14: HLT+4 ;DEVICE CSR (R2) RESPONSE FAILURE
3031
3032          ;PROBABLE FAULT LOGIC: (D2 C2) E36
3033          ;(D6 C2) E24
3034          ;(D4 D6,D7) E7, E42
3035
3036
3037 005624 016102 016436  R114: MOV  CADTSR(R1),R2 ;SET DEVICE TSR REGISTER > R2
3038 005630 011203          MOV  (R2),R3 ;:(FIRST READ) CHANGE OF STATE REGISTER TSR
3039 005632 013704 013220  MOV  ZERO,R4 ;APPROPRIATE BITS TO SHOULD BE
3040 005636 020304          CMP  R3,R4 ;VERIFY RESULTS
3041 005640 001401          BEQ  R114 ;(OK) BRANCHES
3042          ;
3043 005642 104004          ETSR14: HLT+4 ;DEVICE TSR (R2) RESPONSE FAILURE
3044          ;
3045          ;BITS "IN" R3 SHOULD HAVE SET ACCORDING TO BITS "OUT" R4
3046          ;PROBABLE FAULT LOGIC: (D4 OR D5) ALL
3047          ;(D6) ALL
3048          ;(D7) ALL
3049          ;(D8 OR D9) ALL
3050
3051
3052 005644 016102 016436  RJ14: MOV  CADTSR(R1),R2 ;SET DEVICE TSR ADDRESS>R2
3053 005650 005004          CLR  R4 ;CLR SHOULD BE
3054 005652 011203          MOV  (R2),R3 ;FETCH CONTENTS OF TSR
3055 005654 020304          CMP  R3,R4 ;VERIFY RESULTS
3056 005656 001401          BEQ  RK14 ;(OK) BRANCHES
3057
3058          ;*****
3059          ; TSR (R2) RESPONSE FAILURE
3060
3061 005660 104004          ERK14: HLT+4 ;DEVICE TSR (R2) FAILED TO RESPOND CORRECTLY
3062          ;SHOULD HAVE CLEARED BY FIRST READ ABOVE (R114)
3063          ;PROBABLE FAULT LOGIC: (D4 OR D5) ALL
3064          ;(D6) ALL
3065          ;(D7) ALL
3066          ;(D8 OR D9) ALL
3067
3068          ;*****
3069
3070 005662 023737 012430 005730 RK14:  CMP  ERRORS,RERR14 ;TEST ANY ERRORS RECORDED
3071          ;(NO) BRANCHES
3072 005670 001004          BNE  RL14 ;(YES) BRANCHES
3073
3074 005672 006201          LOPX14: ASR  R1 ;ADVANCE TO
3075 005674 005201          INC  R1 ;NEXT DEVICE
3076 005676 000137 005234          JMP  LOP14 ;CONTINUE
3077
3078 005702 032737 000400 177570 RL14:  BIT  #BIT8,SWR ;TEST LOCK ON ERROR SELECTED
3079 005710 001770          BEQ  LOPX14 ;(NO) BRANCHES
3080 005712 000137 005236          JMP  RA14 ;(YES) JUMPS

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# K05

MAINDEC-11-DZCBH-8  
DZCBHB.P11

CS11-HA LOGIC TEST  
TST14: TEST DEVICE INTERRUPT CONTROL DSB

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3081								
3082	005716	123700	177570	END14:	CMPB	SWR,RO		;TEST LOCK ON SUBTEST SELECTED
3083	005722	001003			BNE	OUT14		; (NO) BRANCHES
3084	005724	000137	005222		JMP	TST14		; (YES) JUMPS
3085								
3086	005730	000000		RERR14:0				;RECORD ERROR COUNT ENTRY
3087								
3088	005732	104400		OUT14:	SCOPE			
3089								
3090		000016			N=N+1			

.SBTTL TST15: TEST DEVICE INTERRUPT CONTROL ENB

\*\*\* STATIC LOGIC TESTS \*\*\*

DEVICE INTERRUPT CONTROL

THE PURPOSE OF THIS TEST IS TO VERIFY (STATICALLY) THE INTERRUPT CONTROL LOGIC OF THE CB11-HA(S) IN NON-INTERRUPT MODE. DEVICE ACTIVITY IS UNDER THE CONTROL OF THE MAINT/TRANS BIT 13 OF THE DEVICE CSR REGISTER FOR NORMAL OPERATION AND CAN BE UNDER THE JOINT CONTROL OF A DISTRIBUTE MODULE INPUT WHEN DISTRIBUTE TIED TO THE INTERRUPT MODULE MODE OF TESTING IS SELECTED BY THE USER.

NOTE:

NO DISTRIBUTE MODE OF TESTING IS ALLOWED IN MONITOR MODE OF EXECUTION.

TEST ABILITY TO SET BIT 15 INT/RDY OF CURRENT CSR REGISTER WORD 0

THE FOLLOWING SEQUENCE OF COMMANDS ARE ISSUED

SET CSR BIT 14 VERIFY RESULTS

MOV #ONES INTO TER REGISTER VERIFY RESULTS

MOV #ONES INTO DIST/MODULE VERIFY RESULTS

SET BIT13 OF CSR VERIFY RESULTS MAINT/TRANS

DELAY APPROXIMATELY 7 MILLISECONDS

DELAY AN ADDITIONAL 7 MILLISECONDS

CLR DSTADR DIST/MODULE VERIFY RESULTS

DELAY APPROXIMATELY 7 MILLISECONDS

DELAY AN ADDITIONAL 7 MILLISECONDS

TEST BIT 15 OF CSR INT/RDY VERIFY SET TO ONE

TEST TSR WORD 4 NON-ZERO

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M05

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3140 005734 000240          TST15: NUP
3141 005736 004737 013072      JSR      PC,INITQ      ;CLEAR WORK REGISTERS R0-R4
3142 005742 012700 000015      MOV      #15,R0        ;MOVE TEST#15 TO DISPLAY R0
3143
3144 005746 006301          LCP15: ASL      R1        ;FORM WORD OFFSET
3145 005750 013737 012430 006442 RA15: MOV      ERRORS,RERR15 ;RECORD ERROR COUNT ON ENTRY
3146 005756 016102 016262      MOV      CADCSR(R1),R2 ;CURRENT DEVICE CSR ADDRESS>R2
3147 005762 001002          BNE      1$           ;BRANCH IF ACTIVE
3148 005764 000137 006430      JMP      END15        ;JUMP ON END OF SCAN
3149 005770 005012          1$:  CLR      (R2)      ;INIT CONTROL AND STATUS
3150 005772 005062 000006      CLR      6(R2)       ;TER
3151 005776 012704 040000      MOV      #BIT14,R4   ;#BIT14 TO SHOULD BE R4
3152 006002 052704 020000      BIS      #BIT13,R4   ;SET MAINT/TRANS BIT13 OF CSR = 1
3153
3154          ;
3155          ; SET MAINT/TRANS BIT 13 OF CSR = 1
3156          ;
3157 006006 ( 0412          MOV      R4,(R2)     ;#BIT14, #BIT13 TO CSR
3158 006010 ( 1203          MOV      (R2),R3    ;FETCH RESULTS
3159 006012 055104 016612      BIS      CVT.CB(R1),R4 ;MASK IN VECTOR ADDRESS RESPONSE
3160 006016 020304          CMP      R3,R4      ;VERIFY RESULTS
3161 006020 001401          BEQ      RB15       ;(OK) BRANCHES
3162          ;*****
3163          ;(CSR) SHOULD BE #BIT14
3164 006022 104004      ECSR15: HLT+4      ;DEVICE CSR (R2) FAILED TO RESPOND CORRECTLY
3165
3166          ;PROBABLE FAULT LOGIC: (D2 C2) E36
3167          ; (D6 B2) E24
3168          ; (D4 D7,D6) E42, E7
3169
3170          ;*****
3171 006024 013702 002176      RB15: MOV      DSTADR,R2 ;FETCH DISTRIBUTE ADDRESS
3172 006030 001002          BNE      1$         ;ACTIVE BRANCHES
3173 006032 000137 006154      JMP      RE15       ;(NOT DISTR/MODE) JUMPS
3174 006036 004737 011614      1$:  JSR      PC,DLYGMS ;DELAY 7 MILLISECOND
3175
3176          ; DISTRIBUTE TIED TO INTERRUPT MODE PROCESSING
3177          ;
3178 006042 016102 016524      MOV      CADTER(R1),R2 ;CURRENT DEVICE TER ADDRESS>R2
3179 006046 012704 177777      MOV      #ONES,R4   ;ONES TO TER REGISTER
3180 006052 010412          MOV      R4,(R2)
3181
3182          ; ALL ONES ENABLE TER REGISTER
3183          ;
3184 006054 011203          MOV      (R2),R3    ;FETCH RESULTS
3185 006056 020304          CMP      R3,R4      ;VERIFY RESULTS
3186 006060 001401          BEQ      RBC15     ;(OK) BRANCHES
3187
3188          ;*****
3189
3190 006062 104004      ETER15:HLT+4      ;DEVICE TER (R2) FAILED TO RESPOND CORRECTLY
3191
3192          ;PROBABLE FAULT LOGIC: (D4 C2,D6) E8, E7
3193          ; (D2 C2) E36
3194          ; (D7) ALL
3195

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NOS

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3198 006064
3199
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3201
3202
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3204
3205 006064 013702 002176
3206 006070 012704 177777
3207 006074 010412
3208 006076 011203
3209 006100 020304
3210 006102 001401
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3212 006104 104004
3213
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3218 006106 004737 011606
3219 006112 016102 016353
3220 006116 011203
3221 006120 020304
3222 006122 001401
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3224 006124 104004
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3232 006126 005004
3233 006130 013702 002176
3234 006134 005012
3235 006136 011203
3236 006140 001401
3237
3238 006142 104004
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3244 006144 004737 011606
3245 006150 000137 006266
3246
3247
3248
3249 006154 016102 016524
3250 006160 012704 177777
3251 006164 010412

```

```

;*****
RBC15:
;*****
;
; DISTRIBUTE TIED TO INTERRUPT TESTING
; DELAY FOR PREVIOUS BIT 13 OF CSR = 1
; TOGGLE DISTRIBUTE MODULE TO #ONES VERIFY RESULTS
;
;
; MOV DSTADR,R2 ;DISTRIBUTE MODULE DEVICE ADDRESS
; MOV #ONES,R4 ;DATA (TEST) BITS TO R4
; MOV R4,(R2) ;SET DISTB MODULE BITS
; MOV (R2),R3 ;FETCH
; CMP R3,R4 ;VERIFY
; BEQ RDA15 ;(OK) BRANCHES
;
; DISTRIBUTE MODULE RESPONSE FAILURE
EDST15: HLT+4 ;ERROR DISTRIBUTE MODULE RESPONSE
;
; SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS
; OR REMOVE CB11-HA MODULE FROM CRUTCH CARD
;
;
; RDA15: JSR PC,DDLYMS ;DELAY 7.3 (X2) MILLISECONDS
; MOV CADDR(R1),R2 ;*** NOTE IF NOT DISTB/MODE CSR BIT 13 = 0
; MOV (R2),R3 ;FETCH CONTENTS OF INTR/HA DATA REGISTER
; CMP R3,R4 ;COMPARE RESULTS
; BEQ RDB15 ;(OK) BRANCHES
;
; INTERRUPT MODULE DATA REGISTER RESPONSE FAILURE
EDDR15: HLT+4 ;DATA REGISTER (R2) RESPONSE FAILURE
;
; BITS "IN" R3 SHOULD HAVE SET ACCORDING TO BITS "OUT" R4
;
;
; PROBABLE FAULT LOGIC: (D8 B4) E25
; (D8 OR D9) ALL
;
; IF EDST15: ERROR ABOVE
; SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS
;
; RDB15: CLR R4 ;CLEAR SHOULD BE
; MOV DSTADR,R2 ;SET DISTRIBUTE ADDRESS
; CLR (R2) ;CLEAR DISTB MODULE REGISTER
; MOV (R2),R3 ;FETCH RESULTS
; BEQ RX15 ;VERIFY (OK) BRANCHES
;
; DISTRIBUTE REGISTER (R2) RESPONSE FAILURE
EDDZ15: HLT+4 ;DEVICE DISTRIBUTE REGISTER (R2) FAILED TO CLEAR
;
; DISTRIBUTE TIED TO INTERRUPT MODE OF TESTING
;
; SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS
;
;
;
; RX15: JSR PC,DDLYMS ;DELAY 7.3 (X2) MILLISECONDS
; JMP EXD15 ;VERIFY RESULTS
;
;
; NON DISTRIBUTE MODE PROCESSING
;
;
; RE15: MOV CADDR(R1),R2 ;FETCH TER ADDRESS
; MOV #ONES,R4 ;#ONES TEST DATA TO SHOULD BE
; MOV R4,(R2) ;TO TER REGISTER

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B06

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3252 006166 011203      MOV      (R2),R3      ;FETCH RESULTS IN CSR
3253 006170 020304      CMP      R3,R4       ;VERIFY
3254 006172 001401      BEQ      RF15        ;(OK) BRANCHES
;*****
3258 006174 104004      EBXX15: HLT+4      ;DEVICE TER (R2) FAILED TO RESPOND CORRECTLY
;
;PROBABLE FAULT LOGIC: (D4 D6,C2) E7, E8
;                      (D2 C2) E36
;                      (D7) ALL
;*****
3268 006176 004737 011614      RF15: JSR      PC,DLYGMS ;DELAY 7 MILLISECOND
3269 006202 016102 016262      MOV      CADCSR(R1),R2 ;FETCH CSR ADDRESS
3270 006206 012704 040000      MOV      #BIT14,R4     ;#BIT14 TO SHOULD BE
3271 006212 052704 020000      BIS      #BIT13,R4     ;FIRST TOGGLE MAINT/TRANS =1
3272 006216 056104 016612      BIS      CVT.CB(R1),R4 ;MASK IN VECTOR RESPONSE
3273 006222 011203      MOV      (R2),R3      ;FETCH RESPONSE
3274 006224 042703 100000      BIC      #BIT15,R3     ;FIRST TOGGLE BIT 15 DON'T CARE
3275 006230 020304      CMP      R3,R4       ;VERIFY RESULTS
3276 006232 001401      BEQ      RG15        ;(OK) BRANCHES
;
3278 006234 104004      ERF15: HLT+4      ;DEVICE CSR (R2) RESPONSE FAILURE
;
3280 006236 042712 020000      RG15: BIC      #BIT13,(R2) ;RESET BIT 13 MAINT/TRANS CSR = 0
3281 ;                      ;SECOND TOGGLE
3282 006242 011203      MOV      (R2),R3      ;FETCH RESULTS
3283 006244 042703 100000      BIC      #BIT15,R3     ;DON'T CARE
3284 006250 042704 020000      BIC      #BIT13,R4
3285 006254 020304      CMP      R3,R4       ;VERIFY RESULTS
3286 006256 001401      BEQ      RH15        ;(OK) BRANCHES
;
3288 006260 104004      ERH15: HLT+4      ;DEVICE CSR (R2) RESPONSE ERROR
;
;PROBABLE FAULT LOGIC: (D2 C2) E36
;                      (D6 C2) E24
;                      (D4 D6,D7) E7, E42
;
3295 006262 004737 011614      RH15: JSR      PC,DLYGMS ;DELAY 7 MILLISECOND
3296 ;
3297 ;                      ACTIVITY VERIFICATION
;
3299 006266 016102 016262      EXD15: MOV      CADCSR(R1),R2 ;FETCH CURRENT CSR ADDRESS
3300 ;
3301 006272 012704 040000      MOV      #BIT14,R4     ;#BIT14 TO SHOULD BE
3302 006276 005737 002176      TST      DSTADR       ;TEST DISTB/MODE
3303 006302 001402      BEQ      1$          ;(NO) BRANCHES
3304 006304 052704 020000      BIS      #BIT13,R4     ;(YES) MAINT/TRANS BIT 13 = 1
3305 006310 005727 177777      1$: TST      #ONES      ;TEST TRANS/ENB ARGUMENT #ONES
3306 006314 001402      BEQ      2$          ;(NOT ACTIVE) BRANCHES
3307 006316 052704 100000      BIS      #BIT15,R4     ;ACTIVE SET INT/ROY BIT 15 SHOULD BE

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C06

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3308 006322 056104 015612 2S:  BIS  CVT.CB(R1),R4 ;MASK IN VECTOR RESPONSE
3309 006326 011203          MOV  (R2),R3 ;FETCH RESULTS
3310 006330 020304          CMP  R3,R4 ;VERIFY
3311 006332 001401          BEQ  R15 ;(OK) BRANCHES
3312
3313 006334 104004          ERJ15: HLT+4 ;DEVICE CSR (R2) RESPONSE FAILURE
3314
3315          ;PROBABLE FAULT LOGIC: (D2 C2) E36
3316          ;(D6 C2) E24
3317          ;(D4 D6,D7) E7, E42
3318
3319
3320 006336 016102 016436  RI15:  MOV  CADTSR(R1),R2 ;SET DEVICE TSR REGISTER , R2
3321 006342 011203          MOV  (R2),R3 ;:(FIRST READ) CHANGE OF STATE REGISTER TSR
3322 006344 012704 177777          MOV  #ONES,R4 ;APPROPERIATE BITS TO SHOULD BE
3323 006350 020304          CMP  R3,R4 ;VERIFY RESULTS
3324 006352 001401          BEQ  R15 ;(OK) BRANCHES
3325          ;TRANSITION STATE REGISTER RESPONSE FAILURE
3326 006354 104004          ETSR15: HLT+4 ;DEVICE TSR (R2) RESPONSE FAILURE
3327          ;BITS "IN" R3 SHOULD HAVE SET ACCORDING TO BITS "OUT" R4
3328
3329          ;PROBABLE FAULT LOGIC: (D4 OR D5) ALL
3330          ;(D6) ALL
3331          ;(D7) ALL
3332          ;(D8 OR D9) ALL
3333
3334
3335 006356 016102 016436  RJ15:  MOV  CADTSR(R1),R2 ;SET DEVICE TSR ADDRESS R2
3336 006362 005004          CLR  R4 ;CLR SHOULD BE
3337 006364 011203          MOV  (R2),R3 ;FETCH CONTENTS OF TSR
3338 006366 020304          CMP  R3,R4 ;VERIFY RESULTS
3339 006370 001401          BEQ  R15 ;(OK) BRANCHES
3340
3341          ;*****
3342          ;TSR (R2) RESPONSE FAILURE
3343
3344 006372 104004          ERK15: HLT+4 ;DEVICE TSR (R2) FAILED TO RESPOND CORRECTLY
3345          ;SHOULD HAVE CLEARED BY FIRST READ ABOVE (RI15)
3346          ;PROBABLE FAULT LOGIC: (D4 OR D5) ALL
3347          ;(D6) ALL
3348          ;(D7) ALL
3349          ;(D8 OR D9) ALL
3350
3351          ;*****
3352
3353 006374 023737 012430 006442  RK15:  CMP  ERRORS,RERR15 ;TEST ANY ERRORS RECORDED
3354          ;(NO) BRANCHES
3355 006402 001004          BNE  R15 ;(YES) BRANCHES
3356
3357 006404 006201          LOPX15: ASR  R1 ;ADVANCE TO
3358 006406 005201          INC  R1 ;NEXT DEVICE
3359 006410 000137 005746          JMP  LOP15 ;CONTINUE
3360
3361 006414 032737 000400 177570  RL15:  BIT  #BITB,SWR ;TEST LOCK ON ERROR SELECTED
3362 006422 001770          BEQ  LOPX15 ;(NO) BRANCHES
3363 006424 000137 005750          JMP  RA15 ;(YES) JUMPS

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3364							
3365	006430	123700	177570	END15:	CMPB	SWR,RO	:TEST LOCK ON SUBTEST SELECTED
3366	006434	001003			BNE	OUT15	:(NO) BRANCHES
3367	006436	000137	005734		JMP	TST15	:(YES) JUMPS
3368							
3369	006442	000000		RERR15:	0		:RECORD ERROR COUNT ENTRY
3370							
3371	006444	104400		OUT15:	SCOPE		
3372							
3373		000017			N=N+1		

.S3TTL TST16: TEST DEVICE INTERRUPT CONTROL DSB

\*\*\* STATIC LOGIC TESTS \*\*\*

DEVICE INTERRUPT CONTROL

THE PURPOSE OF THIS TEST IS TO VERIFY (STATICALLY) THE INTERRUPT CONTROL LOGIC OF THE CB11-MA(S) IN NON-INTERRUPT MODE. DEVICE ACTIVITY IS UNDER THE CONTROL OF THE MAINT/TRANS BIT 13 OF THE DEVICE CSR REGISTER FOR NORMAL OPERATION AND CAN BE UNDER THE JOINT CONTROL OF A DISTRIBUTE MODULE INPUT WHEN DISTRIBUTE TIED TO THE INTERRUPT MODULE MODE OF TESTING IS SELECTED BY THE USER.  
NOTE:

NO DISTRIBUTE MODE OF TESTING IS ALLOWED IN MONITOR MODE OF EXECUTION.

TEST ABILITY TO INHIBIT SETTING BIT 15 INT/RDY OF CURRENT CSR REGISTER WORD 0

THE FOLLOWING SEQUENCE OF COMMANDS ARE ISSUED

SET CSR BIT 14 VERIFY RESULTS

MOV #ONES INTO TER REGISTER VERIFY RESULTS

MOV ZERO INTO DIST/MODULE VERIFY RESULTS

SET BIT13 OF CSR VERIFY RESULTS MAINT/TRANS

DELAY APPROXIMATELY 7 MILLISECONDS

DELAY AN ADDITIONAL 7 MILLISECONDS

CLR DSTADR DIST/MODULE VERIFY RESULTS

DELAY APPROXIMATELY 7 MILLISECONDS

DELAY AN ADDITIONAL 7 MILLISECONDS

TEST BIT 15 OF CSR INT/RDY VERIFY SET TO ZERO

TEST TSR WORD 4 ZERO

Vertical column of characters on the left margin, possibly a page number or identifier, including characters like '33', '32', '31', '30', '29', '28', '27', '26', '25', '24', '23', '22', '21', '20', '19', '18', '17', '16', '15', '14', '13', '12', '11', '10', '9', '8', '7', '6', '5', '4', '3', '2', '1'.

# F06

```

3423 006446 000240          TST16: NUP
3424 006450 004737 013072      JSR      PC,INITQ      ;CLEAR WORK REGISTERS RC-R4
3425 006454 012700 000016      MOV      #16,R0        ;MOVE TEST#16 TO DISPLAY R0
3426
3427 006460 006301          LOP16: ASL      P1      ;FORM WORD OFFSET
3428 006462 013737 012430 007154 RA16:  MOV      ERRORS,RERR16 ;RECORD ERROR COUNT ON ENTRY
3429 006470 016102 016262      MOV      CADCSR(R1),R2 ;CURRENT DEVICE CSR ADDRESS>R2
3430 006474 001002          BNE      IS           ;BRANCH IF ACTIVE
3431 006476 000137 007142      JMP      END16        ;JUMP ON END OF SCAN
3432 006502 005012          IS:   CLR      (R2)     ;INIT CONTROL AND STATUS
3433 006504 005062 000006      CLR      6(R2)       ;TER
3434 006510 012704 040000      MOV      #BIT14,R4   ;#BIT14 TO SHOULD BE R4
3435 006514 052704 020000      BIS      #BIT13,R4   ;SET MAINT/TRANS BIT13 OF CSR = 1
3436
3437
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3440
3441 006520 010412          MOV      R4,(R2)     ;#BIT14,#BIT13 TO CSR
3442 006522 011203          MOV      (R2),R3     ;FETCH RESULTS
3443 006524 056104 016612      BIS      CVT.CB(R1),R4 ;MASK IN VECTOR ADDRESS RESPONSE
3444 006530 020304          CMP      R3,R4       ;VERIFY RESULTS
3445 006532 001401          BEQ      RB16        ;(OK) BRANCHES
3446
3447 006534 104004          ECSR16: HLT+4      ;(CSR) SHOULD BE #BIT14
3448
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3454 006536 013702 002176          RB16:  MOV      DSTADR,R2 ;FETCH DISTRIBUTE ADDRESS
3455 006542 001002          BNE      IS           ;ACTIVE BRANCHES
3456 006544 000137 006666      JMP      RE16        ;(NOT DISTR/MODE) JUMPS
3457 006550 004737 011614          IS:   JSR      PC,DLYGMS ;DELAY 7 MILLISECONDS
3458
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3466
3467 006554 016102 016524          MOV      CADTER(R1),R2 ;CURRENT DEVICE TER ADDRESS>R2
3468 006560 012704 !77777      MOV      #ONES,R4    ;ONES TO TER REGISTER
3469 006564 010412          MOV      R4,(R2)
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3471
3472
3473 006574 104004          ETER16: HLT+4      ;ALL ONES ENABLE TER REGISTER
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3489 006602 013704 013220
3490 006606 010412
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3492 006612 020304
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3501 006620 004737 011606
3502 006624 016102 016350
3503 006630 011203
3504 006632 020304
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3515 006640 005004
3516 006642 013702 002176
3517 006646 005012
3518 006650 011203
3519 006652 001401
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3521 006654 104004
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3527 006656 004737 011606
3528 006662 000137 007000
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3532 006666 016102 016524
3533 006672 013704 013220
3534 006676 010412

```

```

*****
RBC16:
*****
;
; DISTRIBUTE TIED TO INTERRUPT TESTING
; DELAY FOR PREVIOUS BIT 13 OF CSR = 1
; TOGGLE DISTRIBUTE MODULE TO ZERO VERIFY RESULTS
;
; MOV DSTADR,R2 ;DISTRIBUTE MODULE DEVICE ADDRESS
; MOV ZERO,R4 ;DATA (TEST) BITS TO R4
; MOV R4,(R2) ;SET DISTB MODULE BITS
; MOV (R2),R3 ;FETCH
; CMP R3,R4 ;VERIFY
; BEQ RDA16 ;(OK) BRANCHES
; DISTRIBUTE MODULE RESPONSE FAILURE
EDST16: HLT+4 ;ERROR DISTRIBUTE MODULE RESPONSE
;
; SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS
; OR REMOVE CB11-HA MODULE FROM CRUTCH CARD
;
RDA16: JSR PC,DDLIMS ;DELAY 7.3 (X2) MILLISECONDS
; MOV CADDDR(R1),R2 ;** NOTE IF NOT DISTB/MODE CSR BIT 13 = 0
; MOV (R2),R3 ;FETCH CONTENTS OF INTR/HA DATA REGISTER
; CMP R3,R4 ;COMPARE RESULTS
; BEQ RDB16 ;(OK) BRANCHES
; INTERRUPT MODULE DATA REGISTER RESPONSE FAILURE
EDDR16: HLT+4 ;DATA REGISTER (R2) RESPONSE FAILURE
; BITS "IN" R3 SHOULD HAVE SET ACCORDING TO BITS "OUT" R4
;
;PROBABLE FAULT LOGIC: (D8 B4) E25
; (D8 OR D9) ALL
; IF EDST16: ERROR ABOVE
; SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS
RDB16: CLR R4 ;CLEAR SHOULD BE
; MOV DSTADR,R2 ;SET DISTRIBUTE ADDRESS
; CLR (R2) ;CLEAR DISTB MODULE REGISTER
; MOV (R2),R3 ;FETCH RESULTS
; BEQ RX16 ;VERIFY (OK) BRANCHES
; DISTRIBUTE REGISTER (R2) RESPONSE FAILURE
EDDZ16: HLT+4 ;DEVICE DISTRIBUTE REGISTER (R2) FAILED TO CLEAR
; DISTRIBUTE TIED TO INTERRUPT MODE OF TESTING
;
; SUGGEST YOU RUN DISTRIBUTE MODULE DIAGNOSTICS
;
RX16: JSR PC,DDLIMS ;DELAY 7.3 (X2) MILLISECONDS
; JMP EXD16 ;VERIFY RESULTS
;
; NON DISTRIBUTE MODE PROCESSING
;
RE16: MOV CADTER(R1),R2 ;FETCH TER ADDRESS
; MOV ZERO,R4 ;ZERO TEST DATA TO SHOULD BE
; MOV R4,(R2) ;TO TER REGISTER

```

# H06

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3535 006700 011203          MOV      (R2),R3      ;FETCH RESULTS IN CSR
3536 006702 020304          CMP      R3,R4       ;VERIFY
3537 006704 001401          BEQ     RF16        ;(OK) BRANCHES
3538
3539 ;*****
3540
3541 006706 104004          EBXX16: HLT+4      ;DEVICE TER (R2) FAILED TO RESPOND CORRECTLY
3542
3543
3544 ;PROBABLE FAULT LOGIC: (D4 D6,C2) E7, E8
3545 ;                       (D2 C2) E36
3546 ;                       (D7) ALL
3547
3548
3549 ;*****
3550
3551 006710 004737 011614          RF16:  JSR      PC,DLYGMS ;DELAY 7 MILLISECONDS
3552 006714 016102 016262          MOV      CADCSR(R1),R2 ;FETCH CSR ADDRESS
3553 006720 012704 040000          MOV      #BIT14,R4    ;#BIT14 TO SHOULD BE
3554 006724 052704 020000          BIS      #BIT13,R4    ;FIRST TOGGLE MAINT/TRANS =1
3555 006730 056104 016612          BIS      CVT.CB(R1),R4 ;MASK IN VECTOR RESPONSE
3556 006734 011203          MOV      (R2),R3     ;FETCH RESPONSE
3557 006736 042703 100000          BIC      #BIT15,R3    ;FIRST TOGGLE BIT 15 DON'T CARE
3558 006742 020304          CMP      R3,R4       ;VERIFY RESULTS
3559 006744 001401          BEQ     RG16        ;(OK) BRANCHES
3560
3561 006746 104004          ERF16: HLT+4      ;DEVICE CSR (R2) RESPONSE FAILURE
3562
3563 006750 042712 020000          RG16:  BIC      #BIT13,(R2) ;RESET BIT 13 MAINT/TRANS CSR = 0
3564 ;
3565 ;
3565 006754 011203          MOV      (R2),R3     ;SECOND TOGGLE
3566 006756 042703 100000          BIC      #BIT15,R3    ;FETCH RESULTS
3567 006762 042704 020000          BIC      #BIT13,R4    ;DON'T CARE
3568 006766 020304          CMP      R3,R4       ;VERIFY RESULTS
3569 006770 001401          BEQ     RH16        ;(OK) BRANCHES
3570
3571 006772 104004          ERH16: HLT+4      ;DEVICE CSR (R2) RESPONSE ERROR
3572 ;
3573 ;
3574 ;PROBABLE FAULT LOGIC: (D2 C2) E36
3575 ;                       (D6 C2) E24
3576 ;                       (D4 D6,D7) E7, E42
3577
3578 006774 004737 011614          RH16:  JSR      PC,DLYGMS ;DELAY 7 MILLISECONDS
3579 ;
3580 ;
3581 ;
3582 ;
3582 007000 016102 016262          EXD16: MOV      CADCSR(R1),R2 ;FETCH CURRENT CSR ADDRESS
3583 ;
3584 ;
3584 007004 012704 040000          MOV      #BIT14,R4    ;#BIT14 TO SHOULD BE
3585 007010 005737 002176          TST     DSTADR       ;TEST DISTB/MODE
3586 007014 001402          BEQ     1$          ;(NO) BRANCHES
3587 007016 052704 020000          BIS      #BIT13,R4    ;(YES) MAINT/TRANS BIT 13 = 1
3588 007022 005737 013220          1$:   TST     ZERO       ;TEST TRANS/ENB ARGUMENT ZERO
3589 007026 001402          BEQ     2$          ;(NOT ACTIVE) BRANCHES
3590 007030 052704 100000          BIS      #BIT15,R4    ;ACTIVE SET INT/RDY BIT 15 SHOULD BE
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3591 007034 056104 016612 2S: B1S CVT.CB(R1),R4 ;MASK IN VECTOR RESPONSE
3592 007040 011203 MOV (R2),R3 ;FETCH RESULTS
3593 007042 020304 CMP R3,R4 ;VERIFY
3594 007044 001401 BEQ R16 ;(OK) BRANCHES
3595
3596 007046 104004 ERJ16: HLT+4 ;DEVICE CSR (R2) RESPONSE FAILURE
3597
3598 ;PROBABLE FAULT LOGIC: (D2 C2) E36
3599 ; (D6 C2) E24
3600 ; (D4 D6,D7) E7. E42
3601
3602
3603 007050 016102 016436 RI16: MOV CADTSR(R1),R2 ;SET DEVICE TSR REGISTER > R2
3604 007054 011203 MOV (R2),R3 ;(FIRST READ) CHANGE OF STATE REGISTER TSR
3605 007056 013704 013220 MOV ZERO,R4 ;APPROPRIATE BITS TO SHOULD BE
3606 007062 020304 CMP R3,R4 ;VERIFY RESULTS
3607 007064 001401 BEQ R16 ;(OK) BRANCHES
3608 ; TRANSITION STATE REGISTER RESPONSE FAILURE
3609 007066 104004 ETSR16: HLT+4 ;DEVICE TSR (R2) RESPONSE FAILURE
3610 ; BITS "IN" R3 SHOULD HAVE SET ACCORDING TO BITS "OUT" R4
3611
3612 ;PROBABLE FAULT LOGIC: (D4 OR D5) ALL
3613 ; (D6) ALL
3614 ; (D7) ALL
3615 ; (D8 OR D9) ALL
3616
3617
3618 007070 016102 016436 RJ16: MOV CADTSR(R1),R2 ;SET DEVICE TSR ADDRESS>R2
3619 007074 005004 CLR R4 ;CLR SHOULD BE
3620 007076 011203 MOV (R2),R3 ;FETCH CONTENTS OF TSR
3621 007100 020304 CMP R3,R4 ;VERIFY RESULTS
3622 007102 001401 BEQ R16 ;(OK) BRANCHES
3623
3624 ;*****
3625 ; TSR (R2) RESPONSE FAILURE
3626
3627 007104 104004 ERK16: HLT+4 ;DEVICE TSR (R2) FAILED TO RESPOND CORRECTLY
3628 ; SHOULD HAVE CLEARED BY FIRST READ ABOVE (RI16)
3629 ;PROBABLE FAULT LOGIC: (D4 OR D5) ALL
3630 ; (D6) ALL
3631 ; (D7) ALL
3632 ; (D8 OR D9) ALL
3633
3634 ;*****
3635
3636 007106 023737 012430 007154 RK16: CMP ERRORS,RERR16 ;TEST ANY ERRORS RECORDED
3637 ; (NO) BRANCHES
3638 007114 001004 BNE RL16 ;(YES) BRANCHES
3639
3640 LOPX16: ASR R1 ;ADVANCE TO
3641 007120 005201 INC R1 ;NEXT DEVICE
3642 007122 000137 006460 JMP LOP16 ;CONTINUE
3643
3644 007126 032737 000400 177570 RL16: BIT #BIT8,SWR ;TEST LOCK ON ERROR SELECTED
3645 007134 001770 BEQ LOPX16 ;(NO) BRANCHES
3646 007136 000137 006462 JMP RA16 ;(YES) JUMPS

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# K06

MAINT:DEC-11-DZCBH-B      CS11-HP LOGIC TEST      MACY11 27(732)    11-OCT-76    10:43    PAGE 76  
 JZCBHB.P11      TST16: TEST DEVICE INTERRUPT CONTROL DSB

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3656          000020          N=N+1
3657          .SBTTL  TST17:  DEVICE DYNAMIC INTERRUPT TEST
3658
3659          ;  ***  DYNAMIC INTERRUPT TESTS  ***
3660
3661          ;  THIS TEST VERIFIES THE ABILITY OF THE CB11-HA(S)
3662          ;  TO INTERRUPT AT THE PROPER LEVEL AND THE PROPER
3663          ;  VECTOR ADDRESS. ALL CONTROL IS UNDER THE MAINT/TRANS
3664          ;  BIT 13 OF THE CSR REGISTER.
3665
3666          ;NOTE:
3667          ;  IF THE PROCESSOR "HANGS" (CONTINUES TO RUN WITH THE
3668          ;  HALT ENABLE SWITCH SET), THIS INDICATES THAT THE INTERRUPT
3669          ;  REQUEST HAS BEEN GRANTED BUT THE DEVICE FAILED TO CLEAR BBSY
3670          ;  TO RELEASE THE BUS TO THE PROCESSOR.
3671          ;PROBABLE FAULT LOGIC:  M7291 (D3 B2) E12, E15
3672          ;                               (D3 C7) E05, E09, E11
3673          ;                               (D3 D5,D6) E09, E11, E19
3674
3675
3676          ;  ALSO CHECK:  M9000 GRANT CONTINUITY MODULE(S)
3677
3678  007160  004737  013114          TST17:  JSR      PC,INTR          ;INITIALIZE ALSO AUTO ASSIGN PRIORITY ENTRY
3679  007164  012700  000017          MOV      #17,R0          ;TEST # TO DISPLAY R0
3680  007170  013737  012430  007764  LOP17:  MOV      ERRORS,RERR17 ;RECORD ERROR COUNT ON ENTRY
3681  007176  012703  000340          MOV      #340,R3        ;INITIALIZE FOR INHIBIT(LEVEL#7)TEST
3682  007202  006301          ASL      R!              ;FORM WORD OFFSET
3683
3684  007204  016102  016262          RA17:   MOV      CADCSTR(R1),R2 ;FETCH CURRENT CSR ADDRESS> R2
3685  007210  001002          BNE     TEST17          ;SCAN ACTIVITY BRANCHES
3686  007212  000137  007752          JMP      END17          ;ALL DEVICES TESTED END OF SCAN JUMP
3687
3688          ;NOTE:
3689          ;  WITH THE EXCEPTION OF UNIBUS TIME OUT ERROR TRAPS
3690          ;  NO ATTEMPT IS MADE TO VERIFY DEVICE REGISTER RESPONSE
3691          ;  (FAILURES) IN ORDER TO MINIMIZE COMPLEXITY OF CODE.
3692          ;  THEREFORE THE INABILITY OR ABILITY OF A DEVICE TO
3693          ;  INTERRUPT AT A GIVEN LEVEL COULD BE DUE TO A
3694          ;  FAILURE MODE WHICH EXISTED AND WAS REPORTED
3695          ;  EARLIER IN THE STATIC TEST PORTION OF THE PROGRAM.
3696
3697  007216  005012          TEST17: CLR      (R2)          ;(PREVIOUS PROCESS) BIT 14 CLR
3698  007220  016105  016612          MOV      CVT.CB(R1),R5 ;FETCH DEVICE ASSOCIATED VECTOR ADDRESS
3699  007224  010537  013216          MOV      R5,$VEC        ;RECORD
3700  007230  012725  007322          MOV      #ERINH,(R5)+  ;SET INTERRUPT INHIBIT FAILURE ERROR LINK
3701  007234  012715  000340          MOV      #340,(R5)     ;SET DEVICE PRIORITY (VECTOR ENTRY) TO LEVEL#7
3702  007240  012703  000340          MOV      #340,R3        ;SET PSW PRIORITY DISPLAY >R3
3703  007244  010337  177776          MOV      R3,PSW        ;SET PSW PRIORITY=7
3704  007250  010304          MOV      R3,R4          ;SET DEVICE PRIORITY(VECTOR ENTRY)DISPLAY>R4
3705
3706          ;NOTE:  DEVICE INTERRUPT GENERATION CODE
3707          ;  THIS CODE IS EXECUTED ONCE FOR EACH ACTIVE DEVICE
3708          ;  IN ORDER TO CONDITION THAT DEVICE FOR INTERRUPTING.
3709
3710
3711  007252  012762  177777  000006          MOV      #177777,6(R2) ;ARM TRANSITION ENABLE REGISTER (ALL BITS)
  
```

L06

```
3712 007260 012712 060000      MOV      #60000(R2)      ;ENABLE CONTROL AND STATUS REGISTER (BITS 14,13)
3713 007264 004737 011614      JSR      PC,DLYGMS      ;DELAY 7 MILLISECONDS FOR MAINT (BIT13)=1
3714 007270 012712 040000      MOV      #40000(R2)      ;DISABLE CONTROL AND STATUS REGISTER (BIT 13)
3715 007274 004737 011614      JSR      PC,DLYGMS      ;DELAY 7 MILLISECONDS FOR MAINT (BIT13)=0
```

THE TOGGLEING OF BIT 13 OF THE CSR (I.E. MAINT)ASSURES THAT BOTH NEGATIVE AND POSITIVE STRAPPED CHANGE OF STATE TRANSITIONS WILL HAVE BEEN PRODUCED. THE DEVICE IS NOW ARMED AND SHOULD INTERRUPT WHEN THE PRIORITY IN THE PSW (PROCESSOR STATUS WORD)IS LOWERED BELOW THE DEVICE LEVEL.

NOTE:

- 1) AN ERROR REPORT AT LOCATION "ERRINH" SIGNIFIES THAT THE DEVICE INTERRUPTED WHEN IT SHOULD HAVE BEEN INHIBITED.
- 2) AN ERROR REPORT AT LOCATION "ERREN8" SIGNIFIES THAT THE DEVICE DID NOT INTERRUPT WHEN IT SHOULD HAVE.
- 3) AN ERROR REPORT AT LOCATION "ERBEN8" SIGNIFIES THAT THE DEVICE DID NOT INTERRUPT AT PRIORITY LEVEL ZERO.
- 4) AN ERROR REPORT AT LOCATION "ERMINT" SIGNIFIES THAT THE DEVICE CONTINUOUSLY INTERRUPTED. I.E. DURING DEVICE SERVICE THE PROCESSOR STATUS WORD (DEVICE INTERRUPT VECTOR ADDRESS+2) PROCESSOR PRIORITY FIELD BITS 07 THROUGH 05 FAILED TO INHIBIT INTERRUPTS AT IT'S CURRENT LEVEL.

INTERRUPT PRIORITY INHIBIT TESTING

CONTINUE TO LOWER PRIORITY OF THE CPU (PSW) UNTIL EQUAL TO THAT OF THE DEVICE. NO INTERRUPTS ARE EXPECTED.

```
3746 007300 120361 016701      1$: CMPB    R3,CLV.CB+1(R1) ;SCAN LEVEL UNDER TEST
3747 007304 101432                BLOS    RB17             ;LOWER OR SAME BRANCHES
3748 007306 162703 000040      SUB     #40,R3           ;LOWER PROCESSOR PRIORITY DISPLAY>R3
3749 007312 010337 177776      MOV     R3,PSW          ;LOWER PROCESSOR PRIORITY>PSW
3750 007316 001443                BEQ     ERREN8-8.
3751 007320 000767                BR      1$              ;(OK)CONTINUE TO ENABLE TEST
```

\*\*\*\*\*  
DEVICE INTERRUPTED WHEN INHIBITED

SIGNIFICANCE

- (R2) DEVICE ADDRESS (CSR) UNDER TEST
- (R3) PROCESSOR PRIORITY DISPLAY (PSW)
- (R4) DEVICE PRIORITY DISPLAY (VECTOR ADDRESS +2)

NOTE:

THE FOLLOWING CODE IS FOR AUTO PRIORITY ASSIGNMENT MONITOR MODE EXECUTION ONLY.

```
3764 007322 005737 000230      ERINH: TST     FLGPTY      ;TEST AUTO PRIORITY MODE EXECUTION
3765 007326 001415                BEQ     ERRINH          ;(NO) BRANCHES
3766
3767 007330 105761 016701      TSTB   CLV.CB+1(R1)    ;HAS CODE BEEN EXECUTED BEFORE
```

M06

MAINDEC-11-DZCBH-B CS11-HP LOGIC TEST MACY11 27(732) 11-OCT-76 10:43 PAGE 78  
DZCBHB.P11 TST17: DEVICE DYNAMIC INTERRUPT TEST

3768 007334 001012 BNE ERRINH ;(YES) BRANCHES  
3769  
3770 007336 062703 000040 ADD #40,R3 ;AUTO ASSIGN (RESTORE LEVEL)  
3771 007342 010361 013306 MOV R3,LVL.HO(R1) ;RECORD NEW DEFAULT  
3772 007346 110361 016701 MCVB R3,CLV.CB+1(R1) ;RECORD ACTIVE ENTRY  
3773 007352 162703 000040 SUB #40,R3 ;RESTORE  
3774 007356 000137 007450 JMP ENBRTN ;CONTINUE

3775  
3776 007362 104004 ERRINH: HLT+4 ;(PSW) INTERRUPT PRIORITY INHIBIT FAILURE  
3777  
3778 ;PROBABLE FAULT LOGIC: (D3 A7) E13  
3779 ; (D3 D2) E18

3780  
3781 ; CHECK DEVICE PRIORITY PLUG  
3782 ;

3783  
3784 007364 000000 HALT ;UNRECOVERABLE ERROR HALT  
3785 ;  
3786 ; CONTINUATION WILL RESULT IN UNMEANINGFUL ERRORS  
3787 ; BEING REPORTED IN DYNAMIC TESTING.  
3788 ; NOTE:

3789 ; IF DEFAULT PRIORITY OF SOFTWARE (PROGRAM)  
3790 ; IS HIGHER THAN ACTUAL DEVICE PRIORITY (PLUG)  
3791 ; DEPRESS THE START SWITCH AND RECONFIGURE THE  
3792 ; DEVICE PRIORITY LEVEL.

3793  
3794 007366 000137 001320 JMP START2 ;CONFIGURATION PROCESS RESTART  
3795

3796 ;PROBABLE FAULT:  
3797 ;  
3798 ; CHECK DEVICE PRIORITY PLUG  
3799 ; \*\*\*\*\*  
3800

```

3801          :      INTERRUPT PRIORITY ENABLE TESTING
3802
3803          ;      TEST INTERRUPT OCCURS AT ONE LEVEL BELOW DEVICE LEVEL
3804
3805 007372 012765 007450 177776 RB17:  MOV      #ENBRTN,-2(R5) ;SET INTERRUPT ENABLE RETURN
3806
3807          :NOTE:
3808          :      IF THE PROCESSOR "HANGS" (CONTINUES TO RUN WITH THE
3809          :      HALT ENABLE SWITCH SET), THIS INDICATES THAT THE INTERRUPT
3810          :      REQUEST HAS BEEN GRANTED BUT THE DEVICE FAILED TO CLEAR BBSY
3811          :      TO RELEASE THE BUS TO THE PROCESSOR.
3812          :PROBABLE FAULT LOGIC:  M7291 (D3 B2) E12, E15
3813          :                        (D3 C7) E05, E09, E11
3814          :                        (D3 D5,D6) E09, E11, E19
3815
3816          :      ALSO CHECK:  M9000 GRANT CONTINUITY MODULE(S)
3817
3818
3819
3820
3821 007400 162703 000040          RTN17:  SUB      #40,R3          ;LOWER PROCESSOR PRIORITY DISPLAY>R3
3822 007404 042703 177400          BIC      #177400,R3
3823 007410 010337 177776          MOV      R3,PSW          ;LOWER PROCESS PRIORITY (PSW)
3824 007414 032703 000340          BIT      #340,R3        ;TEST FOR FULL RANGE
3825 007420 001002          BNE      1$             ;ADDITIONAL FETCH CYCLE 11/15 OR 11/20
3826          :                        ;AND UNRECOVERABLE ERROR LINK
3827 007422 000000          HALT     ;DEVICE FAILED TO INTERRUPT AT LEVEL ZERO
3828          :                        ;DEPRESS CONTINUE SWITCH FOR DYNAMIC DEBUG
3829
3830 007424 000001          WAIT    ;STALL ON HARD FAILURE
3831
3832          ;*****
3833
3834 007426 010537 013216          1$:     MOV      R5,$VEC
3835 007432 011237 007446          MOV      (R2),RX5
3836
3837          :      DEVICE DID NOT INTERRUPT WHEN ENABLED
3838          :SIGNIFICANCE:
3839          :      (R2)DEVICE ADDRESS(CSR) UNDER TEST
3840          :      (R3) PROCESSOR PRIORITY DISPLAY (PSW)
3841          :      (R4) DEVICE PRIORITY DISPLAY (VECTOR ADDRESS+2)
3842          :      (RX5) CSR CONTENTS AT TIME OF FAILURE
3843
3844 007436 104004          ERRENB: HLT+4          ;DEVICE INTERRUPT PRIORITY ENABLE FAILURE TO INTERRUPT
3845
3846 007440 013705 013216          MOV      $VEC,R5
3847 007444 000755          BR      RTN17          ;CONTINUE
3848
3849
3850          :PROBABLE FAULT LOGIC:  (D3 A7) E13
3851          :                        (D3 D2) E18
3852          :                        (D6 C1,C2) E33, "DL1"
3853
3854          :      CHECK DEVICE PRIORITY PLUG
3855
3856          :                        (D3 D2,C2) E15, E34

```

:(D3 C5) E09, E11  
:(D3 D6, D7) E06, E17, E19  
DELAY NETWORK(S)  
:(D6 C2) "DL1"  
:(D3 B2) "DL2"

\*\*\*\*\*

3865 007446 000000 RX5: C

3868 007450 012765 007542 177776 ENBRTN: MOV #EXTRN, -2(R5) ;SET INTERRUPT ENABLE RETURN LINKAGE  
3869 007456 022626 CMP (SP)+, (SP)+ ;ADJUST THE STACK  
3870 007460 012737 000340 177776 MOV #340, PSW  
3871 007466 042712 040000 BIC #40000, (R2) ;TOGGLE INT/ENB ZERO  
3872 007472 052712 040000 BIS #40000, (R2) ;TOGGLE INT/ENB ONE  
3873 007476 116104 016701 MOVB CLV.CB+, (R1), R4 ;SET DEVICE PRIORITY DISPLAY>R4  
3874 007502 042704 177400 BIC #177400, R4  
3875 007506 010415 MOV R4, (R5) ;SET DEVICE SERVICE PRIORITY=ACTUAL

3876 ;NOTE:  
3877 THE EXISTING INTERRUPT CONDITION HAS NOT BEEN DISMISSED, THE  
3878 DEVICE SHOULD INTERRUPT A MINIMUM OF ONE FETCH CYCLE (11/15-11/20)  
3879 FOLLOWING THE LOWERING OF THE PROCESSOR PRIORITY  
3880  
3881

3882 007510 005003 RTNZ: CLR R3 ;SET PROCESSOR PRIORITY DISPLAY>R3  
3883 007512 010337 177776 MOV R3, PSW ;SET PROCESSOR PRIORITY>PSW=ZERO  
3884 007516 000240 NOP ;ADDITIONAL FETCH CYCLE 11/15 OR 11/20  
3885 007520 001236 BNE TEST17 ;AND UNRECOVERABLE ERROR LINK

\*\*\*\*\*

3887 007522 011237 007446 MOV (R2), RX5

3888 ;DEVICE DID NOT INTERRUPT WHEN ENABLED

3889 ;SIGNIFICANCE:  
3890 (R2) DEVICE ADDRESS (CSR) UNDER TEST  
3891 (R3) PROCESSOR PRIORITY DISPLAY (PSW)  
3892 (R4) DEVICE PRIORITY DISPLAY (VECTOR ADDRESS+2)  
3893 (RX5) CSR CONTENTS AT TIME OF FAILURE

3897 007526 104004 ERBENB: HLT+4 ;DEVICE INTERRUPT PRIORITY ENABLE FAILURE TO INTERRUPT  
3898 AT LEVEL ZERO

3899 ;PROBABLE FAULT LOGIC: (D3 A5) E13  
3900 (D3 D2) E18

3901 ;CHECK DEVICE PRIORITY PLUG

3902  
3903  
3904 (D3 C2) E15, E34  
3905 (D3 C5) E09, E11  
3906 (D3 D6, D7) E06, E17, E19

3907  
3908 007530 013705 013216 MOV SVEC, R5  
3909 007534 062703 000040 ADD #40, R3 ;SET UNRECOVERABLE SWITCH+TRY AGAIN  
3910 007540 000717 BR RTN17 ;CONTINUE

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: TEST DEVICE VECTOR ADDRESS + 2 PRIORITY PRESENTATION
: ABILITY TO INHIBIT INTERRUPTS
007542 062737 000040 177776 EXTRTN: ADD #40,PSW ;ANTI HANG CONTROL ADVANCE
007550 012765 007616 177776 MOV #ENTERM,-2(R5) ;LINK ERROR REPORT ENTRY VECTADD +2
007556 032737 000340 177776 BIT #340,PSW ;CHECK LEVEL #7 OR BELOW
007564 001404 BEQ 1$ ;(NO) BRANCHES
007566 162737 000040 177776 SUB #40,PSW ;(YES) LEVEL BELOW #7
: RESTORE ORIGINAL DEVICE LEVEL
007574 000403 BR 2$ ;CONTINUE
007576 012737 000340 177776 1$: MOV #340,PSW ;RESTORE ORIGINAL LEVEL #7
: ENABLE DEVICE INTERRUPT AGAIN
007604 042712 040000 2$: BIC #40000,(R2) ;TOGGLE INT/ENB ZERO
007610 052712 040000 BIS #40000,(R2) ;TOGGLE INT/ENB ONE
; NO INTERRUPT IS EXPECTED AT NORMAL DEVICE LEVEL
007614 000415 BR RT017 ;CONTINUE TO TEST
;*****
007616 012737 000340 177776 ENTERM: MOV #340,PSW ;DISABLE FURTHER INTERRUPTS
007624 116104 016701 MOVB CLV,CB+1(R1),R4 ;DEVICE PRIORITY SHOULD BE TO DISPLAY>R4
007630 042704 177400 BIC #177400,R4
007634 016603 000002 MOV 2(SP),R3 ;CENTRAL PROCESS PRIORITY WAS TO DISPLAY>R3
007640 042703 177437 BIC #177437,R3 ;MASK OUT PRIORITY DISPLAY LEVEL
007644 104004 ERMINT: HLT+4 ;SELECTED DEVICE PRIORITY LEVEL FAILURE TO INHIBIT INTERRUPTS
;PROBABLE FAULT LOGIC: (D3 A5) E13
; CHECK DEVICE PRIORITY PLUG
;SIGNIFICANCE:
: (R2) DEVICE ADDRESS (CSR) UNDER TEST
: (R3) PROCESSOR PRIORITY DISPLAY (PSW) LEVEL REQUIRED TO INHIBIT
: (R4) DEVICE PRIORITY DISPLAY (VECTOR ADDRESS+2)SHOULD HAVE INHIBITED
;*****
; CLEANUP
007646 022626 CMP (SP)+,(SP)+
RT017: 007650 022626 CMP (SP)+,(SP)+ ;ADJUST THE STACK
007652 012737 000340 177776 MOV #340,PSW
007660 005762 000004 TST 4(R2) ;INT/RCY TSR CLR
007664 023737 012430 007764 CMP ERRORS,RERR17 ;TEST FOR RECORDED ERRORS
007672 001406 BEQ 1$ ;(NO)BRANCHES
007674 032737 000400 177570 BIT #BIT8,SWR ;TEST LOCK ON ERROR SELECTED
007702 001402 BEQ 1$ ;(NO)BRANCHES
007704 000137 007204 JMP RA17 ;(YES)LOCK ON CLURRENT DEVICE

```

D07

MAINDEC-11-DZCBH-B  
DZCBHB.P11

TST17:

CS11-HP LOGIC TEST  
DEVICE DYNAMIC INTERRUPT TEST

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3969	007710	005012		:S:	CLR	(R2)		:CLEAR CONTROL +STATUS REGISTER
3970	007712	005762	000004		TST	4(R2)		:CLEAR TRANSITION(CHANGE OF STATE)
3971	007716	005062	000006		CLR	6(R2)		:CLEAR TRANSITION ENABLE REGISTER
3972	007722	013705	013216		MOV	SVEC,RS		
3973	007726	012765	000004	000002	MOV	#IOT,2(R5)		:RESTORE
3974	007734	005725			TST	(R5)+		
3975	007736	010565	177776		MOV	R5,-2(R5)		:TRAP CATCHER
3976								
3977	007742	006201			ASR	R1		:ADVANCE
3978	007744	005201			INC	R1		:DEVICE INDEX
3979	007746	000137	007176		JMP	LOP17		:CONTINUE
3980								
3981	007752	123700	177570	END17:	CMPE	SWR,RO		:TEST LOCK ON SUBTEST SELECTED
3982	007756	001003			BNE	OUT17		: (NO) BRANCHES
3983								
3984	007760	000137	007160		JMP	TST17		: (YES) JUMPS
3985								
3986	007764	000000		RERR17:	0			:RECORDED ERROR COUNT
3987								
3988	007766	005737	000230	OUT17:	TST	FLGPTY		:TEST AUTO ENTRY (MONITOR MODE)
3989	007772	001401			BEG	RZ17		: (NO) BRANCHES
3990	007774	000207			RTS	PC		: (YES) CONTINUE
3991	007776	104400		RZ17:	SCOPE			:TEST SCOPE SELECTION
3992								
3993								
3994								



# E07

MAINDEC-11-DZCBH-B      C911-HA LOGIC TEST      MACY11 27(732)    11-OCT-76    10:43    PAGE 83  
 DZCBH8.P11      TS:17:      DEVICE DYNAMIC INTERRUPT TEST

```

3995          000021          N=N+1
3996
3997          .SBTTL  TST20:  DYNAMIC TEST ROUTINE
3998
3999          :      THIS TEST VERIFIES THE DYNAMIC INTERRUPT CAPABILITY
4000          :      OF THE (C911-HA(S))
4001
4002
4003 010000  012700  000020          DYN1:  MOV      #20,RO          ;DYNAMIC TEST DISPLAY #20 , RO
4004 010004  004737  011206          JSR      PC,SCANNER          ;LINK APPROPRIATE INTERRUPT SERVICE ROUTINE
4005 010010  012737  000340  177776  DYN1:  MOV      #340,PSW
4006
4007 010016  012737  017152  012712          MOV      #CNTL,WORK          ;SET BASE TEST DATA TABLE ADDRESS
4008
4009 010024  012706  001200          MOV      #1200,SP           ;SET PROCESSOR STACK POINTER
4010
4011
4012 010030  004737  010216          DYN2:  JSR      PC,PRIME          ;PRIME DEVICES
4013
4014 010034  005737  002176          TST     DSTADR              ;TEST DISTRIBUTE TIED TO INTERRUPT MODULE
4015 010040  001003          BNE     1$                  ;(YES) BRANCHES
4016 010042  004737  010452          JSR     PC,SERV              ;SERVICE DEVICE REGISTERS
4017 010046  000402          BR      2$
4018
4019 010050  004737  010664          1$:   JSR     PC,SERVD          ;SERVICE DISTB/INTR MODE
4020 010054  005037  177776          2$:   CLR     PSW              ;LOWER PRIORITY TO ZERO
4021 010060  004737  011044          JSR     PC,VERFY             ;VERIFY RESULTS OF ACTIVITY
4022 010064  062737  000002  012712          ADD     #2,WORK              ;ADVANCE TO NEXT DATA CONFIGURATION
4023
4024 010072  013704  012712          MOV     WORK,R4
4025 010076  011404          MOV     (R4),R4              ;TEST DATA BASE SCAN COMPLETED
4026
4027 010100  001053          BNE     DYN2                 ;(NO) CONTINUES
4028 010102  122737  000020  177570  ENDDYN:  CMPB     #20,SWR          ;TEST FOR LOCK ON SUBTEST SELECTION
4029
4030 010110  001737          BEQ     DYN1                 ;(YES) BRANCHES
4031
4032 010112  104400          SCOPE                          ;TEST SCOPE LOOP
4033
4034
4035 010114  005237  001262          PASEND:  INC     PASSES          ;ADVANCE PASS COUNT
4036 010120  032737  020000  177570          BIT     #BIT13,SWR          ;TEST TYPEOUT INHIBIT SELECTION SWITCH
4037 010126  001016          BNE     PS1$                 ;(YES) BRANCHES
4038 010130  000004  015650          TYPE,   MSGPAS              ;TYPE PASS(ES)
4039 010134  013705  001262          MOV     PASSES,TTY          ;OCTAL
4040 010140  004737  013452          JSR     PC,PRINTR           ;
4041 010144  000004  015666          TYPE,   MSGERR              ;TYPE ERROR(S)
4042 010150  013705  012430          MOV     ERRORS,TTY          ;OCTAL
4043 010154  004737  013452          JSR     PC,PRINTR           ;
4044 010160  000004  015412          TYPE,   MCRLF                ;TYPE RETURN
4045
4046 010164  013700  000042          PS1$:  MOV     #42,RO           ;FETCH SOFT VECTOR (MONITOR CONTROL)
4047 010170  001410          BEQ     OUTT                 ;BRANCH IF NO MONITOR
4048 010172  022700  017146          CMP     #ENDPRO,RO          ;TEST ACT11 OR PSEUDO
4049 010176  001401          BEQ     PROEND              ;PSEUDO BYPASS RESET
4050 010200  000005          RESET                          ;CLEAR ALL I/O
  
```

# F07

MAINDEC-11-DZCBH-8  
DZCBHB.P11

CS11-HA LOGIC TEST  
TST20: DYNAMIC TEST ROUTINE

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4051	010202	004710		PROEND: JSR	PC, (RO)	;RETURN TO MONITOR
4052	010204	000240			NOP	
4053	010206	000240			NOP	
4054	010210	000240			NOP	
4055						
4056	010212	000137	002300	OUTT: JMP	TST1	; CONTINUE
4057						
4058						
4059						
4060				.SBTTL	PRIME DEVICE REGISTER(S) ROUTINE LINK APPROPRIATE INTERRUPT SERVICE ROUTINE	
4061						
4062						
4063	010216	004737	013114	PRIME: JSR	PC, INTR	;INITIALIZE REGISTERS

# G07

MAINDEC-11-DZCBH-8 CS11-HP LOGIC TEST MACY11 27(732) 11-OCT-76 10:43 PAGE 85  
 DZCBHB.P11 PRIME DEVICE REGISTER(S) ROUTINE LINK APPROPRIATE INTERRUPT SERVICE ROUTINE

```

4064 010222 006301          PRIMA: ASL      R1          ;FORM WORD OFFSET
4065
4066 010224 016102 016262          MOV      CADCSR(R1),R2
4067 010230 001507          BEQ      OUTPRI          ;TEST CYCLE COMPLETED BRANCHES
4068
4069 010232 012704 040000          MOV      #40000,R4      ;SET SHOULD BE
4070 010236 010412          MOV      R4,(R2)        ;SET BITS 14
4071 010240 056104 016612          BIS      CVT.CB(R1),R4  ;MASK IN VECTOR RESPONSE ENTRY
4072
4073 010244 011203          MOV      (R2),R3 ;VERIFY RESULTS
4074 010246 020304          CMP      R3,R4
4075 010250 001401          SEQ      PRIMB          ;(OK) BRANCHES
4076
4077 010252 104004          ECSR:   HLT+4          ;CSR BIT 14 OR 08 THRU 02 FAILURE
4078
4079 010254 016102 016612          PRIMB:  MOV      CVT.CB(R1),R2 ;SETUP VECTOR LINKAGE
4080
4081 010260 032761 000400 016700          BIT      #400,CLV.CB(R1) ;CHECK GROUP ID
4082 010266 001403          BEQ      1$            ;1ST BRANCHES
4083 010270 012722 011270          2$:     MOV      #ISR1,(R2)+ ;LINK GROUP 2
4084 010274 000402          BR       3$
4085
4086 010276 012722 011304          1$:     MOV      #ISR,(R2)+ ;TO INTERRUPT SERVICE ROUTINE
4087 010302 005737 011266          3$:     TST      LINKER      ;TEST MULTIPLE DEVICE/VECTOR
4088 010306 001403          BEQ      4$            ;(NO) BRANCHES
4089 010310 013762 011266 177776          MOV      LINKER,-2(R2) ;(YES)LINK MULTIPLE SCAN ISR
4090 010316 116112 016700          4$:     MOV      CLV.CB(R1),(R2) ;SETUP PRIORITY LEVEL =7 AND DEVICE OFFSET
4091
4092
4093 010322 013704 012712          MOV      WORK,R4      ;DATA (TEST) BASE
4094 010326 011404          MOV      (R4),R4      ;TO R4
4095
4096 010330 005737 000042          TST      #42          ;TEST AUTO ACCEPT (MONITOR)
4097 010334 001017          BNE      PRIMC        ;(YES) BRANCHES
4098
4099 010336 032737 001000 177570          BIT      #BIT9,SWR    ;TEST FOR WORD SWITCH REG PATTERN
4100 010344 001413          BEQ      PRIMC        ;EXCLUSIVELY FIRST PASS
4101
4102          ; SET DATA PATTERN TO BE TESTED INTO SWITCH REGISTER SWITCHES
4103
4104          HALT          ;HALT FOR SWITCH REGISTER PATTERN HERE
4105 010346 000000          HALT
4106 010350 013704 012712          MOV      WORK,R4
4107 010354 013714 177570          MOV      SWR,(R4)    ;RETAIN NEW ENTRY
4108 010360 005064 000002          CLR      2(R4)       ;DELIMIT (ONLY ONE PATTERN)
4109
4110 010364 012700 177777          MOV      #177777,R0  ;ALL ONES HALT INDICATION
4111
4112          ; RESET SWITCH REGISTER TO PROGRAM CONTROL SETTINGS
4113 010370 000000          HALT          ;SET SWITCH REGISTER FOR PROGRAM CONTROL
4114
4115 010372 011404          MOV      (R4),R4
4116 010374 005061 017054          PRIMC:  CLR      CNGBUF(R1) ;FETCH CURRENT PATTERN
4117
4118 010400 016102 016524          MOV      CADTER(R1),R2
4119 010404 005737 002176          TST      DSTADR      ;TEST DISTRIBUTE TIED TO INTERRUPT
  
```

# H07

MAINDEC-11-DZCBH-B      CB11-HP LOGIC TEST      MACY11 27(732)    11-OCT-76    10:43    PAGE 86  
 DZCBHB.P11      PRIME DEVICE REGISTER(S) ROUTINE LINK APPROPRIATE INTERRUPT SERVICE ROUTINE

4120	010410	001407		BEQ	1\$	;(NO) BRANCHES
4121	010412	012762	020000 177772	MOV	#20000,-6(R2)	;FIRST
4122	010420	004737	011614	JSR	PC,DLYGMS	;NEG/TRANS E'LOCK
4123	010424	012704	177777	MOV	#177777,R4	; (YES) SET TER ENABLE SHOULD BE TO ONES
4124	010430	010412	1\$:	MOV	R4,(R2)	;MAKE TRANS DETECTION ENABLE REG ENTRY (TER)
4125						
4126	010432	011203		MOV	(R2),R3	
4127	010434	020304		CMP	R3,R4	;VERIFY RESULTS
4128	010436	001401		BEQ	PRIMD	; (OK) BRANCHES
4129						
4130	010440	104004	ETER:	HLT+4		;TER BIT(S) FAILED TO RESPOND CORRECTLY
4131	010442	006201	PRIMD:	ASR	R1	
4132	010444	005201		INC	R1	
4133	010446	000E65		BR	PRIMA	;CONTINUE
4134						
4135	010450	000207	OUTPRI:	RTS	PC	;CONTINUE
4136						
4137						

```

4138
4139          .SBTTL  SERVICE DEVICE REGISTERS ROUTINE NORMAL (NO DISTRIBUTE MODE TESTING)
4140
4141
4142 010452 004737 013114  SERV:  JSR PC,INITR          ;INITIALIZE REGISTERS
4143
4144 010456 006301          SERV1:  ASL      R1
4145
4146 010460 016102 016262          MOV     CADCSR(R1),R2
4147 010464 001416          BEQ     SERV3
4148
4149 010466 012704 060000          MOV     #60000,R4          ;SET MAINT/TRANS INT/ENB CSR
4150 010472 056104 016612          BIS     CVT.CB(R1),R4    ;MASK IN VECTOR RESPONSE ENTRY
4151
4152 010476 050412          BIS     R4,(R2)          ;SET DEVICE TRANS/MAINT INT/ENB
4153
4154 010500 011203          MOV     (R2),R3          ;FETCH RESULTS
4155 010502 042703 100000          BIC     #100000,R3      ;DON'T CARE BIT 15
4156 010506 020304          CMP     R3,R4          ;VERIFY RESULTS
4157
4158 010510 001401          BEQ     SERV2          ;OK BRANCHES
4159
4160 010512 104004          ESER:  HLT+4          ;CSR BIT(S) 14 OR 13 FAILURE
4161
4162 010514 006201          SERV2:  ASR      R1
4163 010516 005201          INC     R1
4164 010520 000756          BR     SERV1          ;CONTINUE
4165
4166 010522 004737 011614          SERV3:  JSR     PC,DLYGMS ;DELAY
4167 010526 004737 013114          JSR     PC,INITR      ;INITIALIZE REGISTERS
4168
4169
4170 010532 006301          SERV4:  ASL      R1
4171
4172 010534 016102 016262          MOV     CADCSR(R1),R2
4173 010540 001417          BEQ     SEROUT
4174
4175 010542 042712 020000          SERV5:  BIC     #20000,(R2) ;RESET MAINT/TRANS BIT 13 OF CSR
4176 010546 012704 040000          MOV     #40000,R4      ;SET INT/ENB SHOULD BE > R4
4177
4178 010552 056104 016612          BIS     CVT.CB(R1),R4  ;MASK IN VECTOR RESPONSE ENTRY
4179
4180 010556 011203          MOV     (R2),R3          ;VERIFY RESULTS
4181 010560 042703 100000          BIC     #100000,R3     ;BIT 15 DON'T CARE
4182 010564 020304          CMP     R3,R4
4183 010566 001401          BEQ     SERV6          ;(OK) BRANCHES
4184

```

# J07

MAINDEC-11-DZCBH-8      CS11-HP LOGIC TEST      MACY11 27(732)    11-OCT-76    10:43    PAGE 88  
 DZCBHB.P11      SERVICE DEVICE REGISTERS ROUTINE NORMAL (NO DISTRIBUTE MODE TESTING)

```

4185 010570 104004            ESERO: HLT+4    ;CSR BIT(S) 14 OR 13 FAILURE OR BIT(S) 08 THRU 02
4186
4187 010572 006201            SERV6: ASR      R1
4188 010574 005201                        INC      R1
4189 010576 000755                        BR      SER4                        ;CONTINUE
4190
4191 010600 004737 011614        SEROUT: JSR     PC,DLYGMS                        ;DELAY
4192
4193 010604 004737 013114                        JSR     PC,INTR                        ;INITIALIZE REGISTERS
4194
4195 010610 006301            SER7: ASL      R1
4196 010612 013704 012712                        MOV     WORK,R4
4197 010616 011427                        MOV     (R4),(PC)+
4198 010620 000000            TEMP: 0
4199 010622 012704 040000                        MOV     #40000,R4
4200 010626 056104 016612                        BIS     CVT.CB(R1),R4                        ;MASK IN VECTOR RESPONSE ENTRY
4201 010632 016102 016262                        MOV     CADCSR(R1),R2                        ;SET CURRENT CSR ADDRESS > R2
4202 010636 001411                        BEQ     SER9                        ;SCAN COMPLETED BRANCHES
4203 010640 011203                        MOV     (R2),R3                        ;FETCH CURRENT CSR CONTENTS
4204
4205 010642 042703 100000                        BIC     #100000,R3                        ; CLR INT/RDY BIT 15 SHOULD BE DON'T CARE
4206 010646 020304                        CMP     R3,R4                        ;VERIFY RESULTS
4207 010650 001401                        BEQ     SER8                        ;(OK) BRANCHES
4208
4209 010652 104004            ESTAT: HLT+4    ;CSR STATUS FAILURE BITS 15 THRU 13 OR 08 THRU 02
4210
4211 010654 006201            SER8: ASR      R1
4212 010656 005201                        INC      R1
4213 010660 000753                        BR      SER7                        ;CONTINUE
4214
4215 010662 000207            SER9: RTS      PC                        ;CONTINUE
4216
4217
4218                        .SBTTL SERVICE DEVICE REGISTER(S) ROUTINE (DISTRIBUTE TIED TO INTERRUPT)
  
```

# K07

MAINDEC-11-DZCBH-8      C811-HP LOGIC TEST      MACY11 27(732)    11-OCT-76 10:43    PAGE 89  
 DZCBHB.P11      SERVICE DEVICE REGISTER(S) ROUTINE (DISTRIBUTE TIED TO INTERRUPT)

```

4219 010664 004737 013114      SERVD: JSR      PC, INTR            ; INITIALIZE REGISTERS
4220 010670 006301      SERVD1: ASL      R1
4221 010672 016102 016262      MOV      CADCSR(R1), R2      ; SET DEVICE CSR ADDRESS > R2
4222 010676 001461      BEQ      SDOUT            ; (NO ACTIVITY) BRANCHES
4223 010700 012704 060000      MOV      #60000, R4        ; SET INT/ENB MAINT/TRANS CSR SHOULD BE
4224 010704 010412      MOV      R4, (R2)         ; ACTIVATE DEVICE
4225 010706 056104 016612      BIS      CVT.CB(R1), R4    ; MASK IN VECTOR RESPONSE
4226 010712 011203      MOV      (R2), R3        ; FETCH RESULTS
4227 010714 042703 100000      BIC      #100000, R3      ; BIT# 15 DON'T CARE
4228 010720 020304      CMP      R3, R4         ; VERIFY
4229 010722 001401      BEQ      SERVD2           ; (OK) BRANCHES
4230                            ; DEVICE CSR (R2) RESPONSE FAILURE
4231 010724 104004      ESDCSR: HLT+4        ; CSR REGISTER (R2) BITS 15 THRU 00 FAILURE
4232                            ;
4233 010726 013704 012712      SERVD2: MOV      WORK, R4
4234 010732 011404      MOV      (R4), R4        ; CURRENT DATA CONFIGURATION TO R4
4235 010734 010437 010620      MOV      R4, TEMP        ; RECORD
4236 010740 013702 002176      MOV      DSTADR, R2      ; DISTRIBUTE MODULE ADDRESS > R2
4237 010744 010412      MOV      R4, (R2)        ; SET DISTB ASSOCIATED DATA BITS
4238 010746 011203      MOV      (R2), R3        ; FETCH RESULTS
4239 010750 020304      CMP      R3, R4         ; VERIFY
4240 010752 001401      BEQ      SERVD3           ; (OK) BRANCHES
4241                            ; DISTRIBUTE MODULE (R2) DATA RESPONSE ERROR
4242 010754 104004      SERDST: HLT+4        ; DISTRIBUTE MODULE (R2) RESPONSE FAILURE
4243                            ; BITS "IN" R3 FAILURE TO RESPOND TO "OUT" R4 DATA
4244 010756 004737 011606      SERVD3: JSR      PC, DDLYMS    ; DELAY 7.3 (X2) MILLISECONDS
4245 010762 016102 016350      MOV      CADDDR(R1), R2   ; DEVICE DDR ADDRESS > R2
4246 010766 013704 010620      MOV      TEMP, R4        ; RECORD DATA "OUT" TO DISTRIBJTE
4247 010772 011203      MOV      (R2), R3        ; INPUT RESULTS "IN" DDR
4248 010774 020304      CMP      R3, R4         ; VERIFY RESULTS
4249 010776 001401      BEQ      SERVD4           ; (OK) BRANCHES
4250                            ; DDR (R2) DATA RESPONSE ERROR
4251 011000 104004      SERDDR: HLT+4        ; DEVICE DDR (R2) DATA RESPONSE ERROR
4252                            ; BITS "IN" R3 FAILED TO RESPOND TO DIST "OUT" R4
4253 011002 013702 002176      SERVD4: MOV      DSTADR, R2    ; DIST ADDRESS > R2
4254 011006 005004      CLR      R4             ; CLEAR SHOULD BE
4255 011010 010412      MOV      R4, (R2)        ; CLEAR DISTRIBUTE MODULE
4256 011012 011203      MOV      (R2), R3        ; FETCH RESULTS
4257 011014 001401      BEQ      SERVD5           ; (OK) BRANCHES
4258                            ; DATA DISTRIBUTE MODULE (R2) CLEAR RESPONSE FAILURE
4259 011016 104004      SECOST: HLT+4        ; DISTRIBUTE MODULE (R2) CLEAR RESPONSE FAILURE
4260 011020 004737 011606      SERVD5: JSR      PC, DDLYMS    ; DELAY 7.3 (X2) MILLISECONDS
4261 011024 011203      MOV      (R2), R3        ; FETCH RESULTS (POST)
4262 011026 020304      CMP      R3, R4         ; VERIFY
4263 011030 001401      BEQ      SERVD6           ; (OK) BRANCHES
4264                            ; DISTRIBUTE DATA BITS "IN" R3 FAILURE
4265 011032 104004      SEZOST: HLT+4        ; DISTRIBUTE MODULE (R2) DATA RESPONSE FAILURE
4266                            ;
4267 011034 006201      SERVD6: ASR      R1
4268 011036 005201      INC      R1
4269 011040 000713      BR      SERVD1           ; CONTINUE
4270 011042 000207      SDOUT: RTS        PC                    ; EXIT
4271

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4272
4273          .SBTTL  DEVICE VERIFICATION ROUTINE
4274
4275 011044 004737 013114  VERFY: JSR    PC, INTR
4276 011050 012700 000020      MOV    #20, R0
4277 011054 006301          VRFY0: ASL    R1          ;NOTE LAST TOGGLE WAS MAINT BIT #13 = 1
4278                                     ;IF DISTRIBUTE TIED TO SCAN
4279 011056 013704 012712          MOV    WORK, R4      ;DATA ADDRESS
4280 011062 011404          MOV    (R4), R4      ;CURRENT CONFIGURATION
4281 011064 005737 002176          TST   DSTADR       ;TEST DISTRB/MODE TESTING
4282 011070 001003          BNE   1$          ;(YES) BRANCHES
4283 011072 012704 177777          MOV    #-1, R4 ;
4284 011076 000401          BR    2$
4285 011100 005004          1$: CLR    R4
4286 011102 016102 016262          2$: MOV    CADCSR(R1), R2 ;TEST FOR COMPLETION OF SCAN
4287 011106 001436          BEQ   VEROUT      ;(YES) BRANCHES
4288 011110 062702 000002          ADD   #2, R2      ;FORM DDR ADDRESS
4289 011114 011203          MOV   (R2), R3    ;FETCH CURRENT CONTENTS
4290 011116 020304          CMP   R3, R4      ;DDR REG SHOULD EQUAL ALL ONES NORMALLY
4291                                     ;CLEAR TO ZERO IF DISTRB/MODE TESTING
4292 011120 001401          BEQ   VERFY1      ;(OK) BRANCHES
4293
4294 011122 104004          VEDDR: HLT+4      ;VERIFICATION ERROR OF DDR CONTENTS
4295
4296 011124 012702 017054          VRFY1: MOV   #CNGBUF, R2 ;FETCH RECORDED ACTIVITY ADDRESS
4297 011130 060102          ADD   R1, R2      ;SET ADDRESS OF BUFFER >R2
4298
4299 011132 011203          MOV   (R2), R3    ;FETCH ACTIVITY ENTRY > R3
4300 011134 013704 012712          MOV   WORK, R4    ;FETCH CURRENT DATA WORD ADDRESS
4301 011140 011404          MOV   (R4), R4    ;FETCH CURRENT DATA CONFIGURATION
4302 011142 020304          CMP   R3, R4      ;VERIFY RESULTS
4303 011144 001410          BEQ   VRFY2      ;(OK) BRANCHES
4304          ;SIGNIFICANCE:
4305          ;
4306          ;
4307          ;
4308          ;
4309          ;
4310 011146 010137 011426          MOV   R1, R51
4311 011152 016101 016436          MOV   CADTSR(R1), R1
4312
4313 011156 006301          VETER: ASL    R1
4314 011160 104004          HLT+4 ;VERIFICATION ERROR OF TSR CONTENTS
4315
4316 011162 013701 011426          VRFY2: MOV   R51, R1
4317 011166 005061 017054          CLR   CNGBUF(R1) ;CLEAR PREVIOUS SCAN ENTRY
4318 011172 005061 016766          CLR   DATABF(R1)
4319 011176 006201          ASR   R1
4320 011200 005201          INC   R1
4321 011202 000724          BR    VRFY0      ;CONTINUE
4322 011204 000207          VEROUT: RTS    PC ;CONTINUE

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4323      .SBTTL  MULTIPLE DEVICE TO SINGULAR VECTOR ADDRESS DETECTOR
4324
4325      ;NOTE:
4326      ; THIS SUBROUTINE SCANS ACTIVE VECTOR TABLE ENTRIES
4327      ; AND UPON DETECTION OF DUPLICATE ASSIGNMENTS IT
4328      ; LINKS ALL DEVICES TO THE MULTIPLE INTERRUPT SERVICE
4329      ; ROUTINE BY ENTRY IN "LINKER".
4330
4331      011206 005001      SCANNER: CLR      R1      ;CLEAR
4332      011210 005002      CLR      R2      ;REGISTERS
4333      011212 005003      CLR      R3      ;AND
4334      011214 005037 011266 CLR      LINKER ;CONTROL FLAG
4335
4336      011220 005723      LXA:   TST      (R3)+ ;SET BASE OFFSET SUBSCAN
4337      011222 010302      MOV      R3,R2 ;RECORD>R2
4338      011224 005761 016262 TST      CADCSR(R1) ;TEST SCAN COMPLETED
4339      011230 001415      BEQ      LXOUT   ;(YES) BRANCHES
4340
4341      011232 026162 016612 016612 LXB:  CMP      CVT.CB(R1),CVT.CB(R2) ;TEST FOR DUPLICATE ENTRY
4342      011240 001406      BEQ      PXOUT   ;(YES) BRANCHES
4343      011242 005722      TST      (R2)+ ;ADVANCE SUBSCAN INDEX
4344      011244 005762 016260 TST      CADCSR-2(R2) ;TEST SUBSCAN COMPLETED
4345      011250 001370      BNE      LXB    ;(NO) BRANCHES
4346
4347      011252 005721      TST      (R1)+ ;ADVANCE SUBSCAN BASE INDEX
4348      011254 000761      BR       LXP    ;CONTINUE
4349
4350      011256 012737 011432 011266 PXOUT: MOV      #MISR,LINKER ;SET MULTIPLE DEVICE/VECTOR LINKER
4351
4352      011264 000207      LXOUT: RTS      PC ;EXIT
4353      011266 000000      LINKER: 0 ;MULTIPLE DEVICE/VECTOR LINKER
4354      ; ;CONTAINS #MISR WHEN ACTIVE
4355      ;*****
4356

```

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4357
4358
4359          .SBTTL  INTERRUPT SERVICE ROUTINE (SINGLE DEVICE PER VECTOR)
4360
4361
4362 011270 013737 177776 011310 5.2  ISR1:  MOV    PSW,IPSW      ;GROUP 2 ENTRY
4363 011276 006337 011310          3.7          ASL    IPSW        ;FORM INDEX OFFSET
4364 011302 000403          2.6          BR     ISRPSH     ;TO SECOND GROUP
4365
4366
4367 011304 013727 177776          5.2  ISR:   MOV    PSW,(PC)+
4368
4369 011310 000000          IPSW:  0
4370
4371 011312 010146          4.9  ISRPSH: MOV    R1,-(SP)
4372 011314 010246          4.9          MOV    R2,-(SP)
4373 011316 010346          4.9          MOV    R3,-(SP)
4374 011320 010446          4.9          MOV    R4,-(SP)
4375
4376 011322 013701 011310          3.8  IXRX:  MOV    IPSW,R1      ;FETCH CURRENT PROCESSOR STATUS WORD
4377
4378 011326 042701 177740          4.4          BIC    #177740,R1    ;CLEAR TO DEVICE LEVEL ENTRY
4379 011332 006301          2.3          ASL    R1            ;FORM WORD OFFSET
4380
4381 011334 016102 016262          5.0          MOV    CADCSR(R1),R2
4382
4383 011340 012704 140000          3.8          MOV    #140000,R4    ;SHOULD BE TO R4
4384 011344 056104 016612          5.0          BIS    CVT.CB(R1),R4 ;MASK IN VECTOR RESPONSE
4385 011350 011203          3.8          MOV    (R2),R3      ;FETCH CONTENTS OF CSR
4386 011352 042703 020000          4.4          BIC    #20000,R3    ;MASK OUT MAINTENANCE TOGGLE
4387 011356 020304          2.3          CMP    R3,R4        ;VERIFY CSR CONTENTS
4388 011360 001403          2.6          BEQ    OK$          ;(OK) BRANCHES
4389 011362 012700 000020          3.8          MOV    #20,R0       ;SET MODULE NUMBER IN R0
4390
4391 011366 104004          XCER:  HLT+4      ;CSR BITS 15,14 OR 08 THRU 00 FAILURE
4392
4393 011370 062702 000002          3.8  OK$:   ADD    #2,R2        ;FORM DDR (DATA) ADDRESS
4394
4395 011374 051261 016766          6.4          BIS    (R2),DATABF(R1) ;COLLECT DATA REGISTER (N) ENTRIES
4396          ;FOR DISTRIBUTE MODULE VERIFICATION
4397 011400 062702 000002          3.8          ADD    #2,R2        ;FORM TSR (CHANGE OF STATE) ADDRESS
4398
4399 011404 051261 0.7054          6.4          BIS    (R2),CNGBUF(R1) ;COLLECT CHANGE REGISTER (N) ENTRIES
4400 011410 051261 017054          6.4          BIS    (R2),CNG2UF(R1) ;COLLECT CHANGE REGISTER TWICE
4401 011414 012604          3.8  ISRPOP: MOV    (SP)+,R4      ;RESTORE REGISTERS
4402 011416 012603          3.8          MOV    (SP)+,R3
4403 011420 012602          3.8          MOV    (SP)+,R2
4404 011422 012601          3.8          MOV    (SP)+,R1
4405 011424 000002          4.8  RTB:   RTI          ;EXIT INTERRUPT SCAN
4406 011426 000000          RSI:   0
4407 011430 000000          RS2:   0
4408
4409

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011606 012737 000004 011674 5.2
011614 010527 3.7
011616 000000
011620 013737 011742 011746 5.2
011626 013705 177570 3.8
011632 042705 127777 4.4
011636 001415 2.6
011640 022705 050000 3.8
011644 001412 2.6
011646 032705 010000 4.4
011652 001404 2.6
011654 013737 011740 011746 5.2
011662 000403 2.6
011664 013737 011744 011746 5.2
011672 012727 000002 5.2
011676 000000 1.5
011700 013737 011746 011710 5.2
011706 005327 3.7
011710 000000 3.5
011712 001375 2.6
011714 005337 011676 3.7
011720 001367 2.6
011722 012737 000002 011674 5.2
011730 013705 011616 3.8
011734 000207 3.5
011736 000000
011740 017700
011742 017777
011744 020777
011746 017777
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```
.SBTTL
DOLYMS: MOV
DLYGMS: MOV
TSS:
1S:
2S:
3S:
4S:
DTIME:
TIMEW:
TIMEX:
TIMEY:
TIME:
NOTE:
.SBTTL
CLKSCN:
```

```
6.4 MILLISECOND DELAY
#4,MS6D+2 ;DISTRIBUTE MODE CALL
NOTE:
THE NORMAL 7.3 MILLISECOND INTERVAL MAY BE REDUCED
BY 10% VIA SETTING SWITCH REGISTER BIT #12 = 1.
THE NORMAL 7.3 MILLISECOND DELAY INTERVAL MAY BE INCREASED
BY 10% VIA SETTING SWITCH REGISTER BIT #14 = 1.
DISTRIBUTE MODE CALL USE TWICE THE SELECTED INTERVAL
R5,(PC)+
0
MOV TIMEX,TIME ;PRESET NOMINAL TIME INTERVAL
MOV SWR,R5
BIC #127777,R5
BEQ MS6D
CMP #50000,R5
BEQ MS6D
BIT #BIT12,R5
BEQ 1$
MOV TIMEW,TIME ;-10% DELAY > TIME
BR MS6D
MOV TIMEY,TIME ;+10% DELAY > TIME
MOV #2,(PC)+ ; NO DELAY = 7.308 MILLISECOND INTERVAL
0
MOV TIME,4$
DEC (PC)+ ;DELAY
;INTERVAL
;EXECUTION
;HERE
MOV #2,MS6D+2 ;RESTORE NON DISTRIBUTE MODE INTERVAL CONTROL
MOV TSS,R5
RTS PC ;RETURN
0 ;REPLACED BY 10% INTERVAL
;LONG
;-10%
;DELAY INTERVAL
;+10%
;DYNAMIC DELAY INTERVAL
ENTRY "TIME:" ABOVE IS MODIFIED BY SOFTWARE
CLKSCN TO 7.3 /2 MILLISECOND DELAY INTERVAL.
SOFTWARE CLOCK 7.3 MILLISECOND TIME INTERVAL GENERATOR
TST DTIME ;TEST CODE EXECUTION FLAG
BNE CLKOUT ;BYPASS (ALREADY EXECUTED)
```

```

4519 011756 000137 016264 3.7 JMP CLKRTN ;EXECUTE TIME INTERVAL GENERATOR
4520 011762 012700 016262 3.8 CLKOUT: MOV #TABLEB,R0 ;SET BASE
4521 011766 012701 017142 3.8 MOV #TABLEN,R1 ;SET LIMIT
4522 011772 005020 3.7 IS: CLR (R0)+ ;CLEAR
4523 011774 020001 2.3 CMP R0,R1 ;TABLE
4524 011776 001375 3.6 BNE IS ;AREA
4525 012000 000207 3.5 RTS PC ;EXIT

:
: DEVICE TRAP TO ZERO
: AND
: BUS ERROR TIME-OUT
: ERROR REPORT ROUTINE
:
012002 000004 015332 TRAPD: TYPE, MSGTPO ;OUTPUT "DEVICE TRAPPED TO ZERO"
012006 000402 BR BUSL1 ;CONTINUE

:
: ON DEVICE TRAPPED TO ZERO IT IS SUGGESTED
: THAT EACH DEVICE BE CONFIGURED SEPERATELY
: FOR TESTING UNTIL THE FAILING DEVICE IS
: ISOLATED.
:
012010 000004 015300 BUSERR: TYPE, MSGBUS
012014 011603 BUSL1: MOV (SP),R3
012016 162703 000002 SUB #2,R3

012022 104003 ERRSYN: HLT+3 ;BUS ERROR TIME-OUT TRAP
:SIGNIFICANCE:
:DEVICE ADDRESS (R2)
:FAILED TO RESPOND AT
:PROGRAM LOCATION (R3)

:PROBABLE FAULT LOGIC: (D3 D4) E23, E25
: (D2 A6,A7,B6,B7) E32 (SWITCH SETTINGS)
:
012024 000002 ERRRTT: RTI ;RETURN
.SBTTL SWAP OUT BUS ERROR CONTROL FOR RTI ROUTINE

012026 005004 SWAPO: CLR R4 ;UNIQUE SIZER ENTRY
012030 012702 160000 MOV #160000,R2
012034 010237 001566 MOV R2,LOWADD
012040 000004 015141 TYPE, MSG2X
012044 000004 015157 TYPE, MSG3X

012050 013727 000004 SWAPO: MOV @#4,(PC)+
012054 012010 SWAP4: BUSERR
012056 013727 000006 MOV @#6,(PC)+
012062 000340 SWAP6: 340
012064 012737 000006 000004 MOV #6,@#4
012072 012737 013372 000006 MOV RTX,@#6
012100 000207 RTS PC

```

```

4575          .SBTTL          SWAP IN BUS ERROR CONTROL REPLACE RTI
4576
4577 012102 013737 012054 000004 SWAPI: MOV      2#SWAP4,2#4
4578 012110 013737 012062 000006        MOV      2#SWAP6,2#6
4579 012116 000207          RTS      PC
4580
4581 012120 001260 $END:  RESTAR
4582 012122 000002        YESRT: RTI          ;RETURN FROM TRACE TRAP
4583          ;
4584          $SCOPE          SCOPE LOOP HANDLER
4585
4586          ;THIS ROUTINE HANDLES THE ITERATIONS, LOOPING, ERROR
4587          ;LOOPING, AND THE DISPLAYING OF THE TEST NUMBER.
4588
4589          ;"SCOPE" IS PLACED BETWEEN EACH SUBTEST IN THE TEST AND
4590          ;RECORDS THE STARTING ADDRESS OF THE SUBTEST IN "LAD:"
4591
4592 012124 032737 000400 177570 TRAPS: BIT      #SW8,2#SWR          ;LOOP ON SPEC. TEST?
4593 012132 001404          BEQ      1$                    ;NO LOOP ON SPEC. TEST
4594 012134 123737 177570 00120C CMPB    2#SWR,ICNT          ;ON RIGHT TEST? *SW7-0*
4595 012142 001433          BEQ      OVER$                ;NOT RIGHT TEST
4596
4597 012144 005737 001262          1$:   TST      PASSES                ;TEST PASS COUNT
4598 012150 001416          BEQ      SVLAD$                ;FIRST PASS BYPASS ITERATIONS
4599 012152 032737 004000 177570 BIT      #SW11,2#SWR          ;KILL ITERATIONS
4600 012160 001012          BNE     SVLAD$                ;YES - KILL ITERATIONS
4601 012162 105737 001201          TSTB   ICNT+1              ;FIRST ONE?
4602 012166 001404          BEQ      2$                    ;BRANCH IF FIRST
4603 012170 123737 012256 001201 CMPB    TIMES,ICNT+1        ;DONE?
4604 012176 001013          BNE     KITS$                ;BRANCH IF NOT
4605 012200 112737 000001 001201 2$:   MOVB   #1,ICNT+1          ;FIRST ITERATION
4606 012206 105237 001200          SVLAD$: INCB   ICNT          ;COUNT TEST NUMBERS
4607 012212 011637 012254          MOV    (6),LAD             ;SAVE LOOP ADDRESS
4608 012216 013737 001200 177570 MOV    ICNT,2#DISPLAY        ;DISPLAY TEST NO. AND ITERATION COUNT
4609 012224 000002          RTE:   RTI             ;RETURN
4610
4611 012226 105237 001201          KITS$: INCB   ICNT+1          ;INC THE ITERATION COUNT
4612 012232 013737 001200 177570 OVER$: MOV    ICNT,2#DISPLAY        ;SET UP DISPLAY
4613 012240 005737 012254          TST    LAD                 ;FIRST ONE?
4614 012244 001760          BEQ    SVLAD$              ;YES
4615 012246 013716 012254          MOV    LAD,(6)            ;FUDGE RETURN ADDRESS
4616 012252 000002          RTF:   RTI             ;FIXES PS
4617
4618 012254 000000          LAD:   0                   ;LOOP ADDRESS
4619 012256 000020          TIMES: 20                ;RUN 20 TIMES

```

# F08

MAINDEC-11-DZC84-B  
DZC84B.P11

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HLT ROUTINE (ERROR TYPEOUT)

```

4619          :          $HLT          ERROR TYPEOUT HANDLER
4620
4621          : THIS ROUTINE PRINTS OUT ERROR MESSAGES STARTING WITH THE
4622          : ADDRESS OF THE "HLT". IT ALSO COUNTS THE NUMBER OF ERRORS
4623          : AND HAS THE CAPABILITY OF LOOPING ON ERROR, BELL ON ERROR,
4624          : "HALT" ON ERROR, AND INHIBIT TYPEOUTS. AN OPTIONAL ARGUMENT
4625          : (HLT+(N)) WILL BE PLACED IN "HLTCTS:" FOR ADITIONAL TYPEOUTS.
4626
4627 012260 004737 013132          EMTS: JSR      PC,PUSHX          ;SAVE REGISTERS
4628 012264 005237 012430          INC      ERRORS          ;COUNT THE NUMBER OF ERRORS
4629 012270 032737 020000 177570 BIT      #SW13,2#SWR      ;SKIP TYPEOUT IF SET
4630 012276 001041          BNE     Y$              ;SKIP TYPEOUTS
4631 012300 023737 013410 013440 CMP      RSO,FLAGH      ;TEST FOR HEADER REQUIREMENT
4632 012306 001413          BEQ     X$              ;(NO) BRANCHES
4633 012310 004737 013374          JSR      PC,HTSTS       ;OUTPUT TEST #
4634 012314 013737 013410 013440 MOV      RSO,FLAGH      ;SET HEADER INHIBIT FLAG
4635 012322 000004 015446          TYPE,   MSGHED         ;OUTPUT (PC),(PS),(SP) ETC.
4636
4637 012326 000004 015550          TYPE,   MSGSUB
4638
4639 012332 000004 015412          TYPE,   MCRLF
4640
4641 012336 000004 015412          X$:    TYPE,   MCRLF
4642 012342 011637 012434          MOV      (6),HLTADR     ;PUT ADDRESS OF INSTRUCTION ON STACK
4643 012346 162737 000002 012434 SUB      #2,HLTADR       ;FUDGE ADDRESS
4644 012354 117737 000054 012432 MOV      #HLTADR,HLTCTS ;GET HLT ARGUMENT
4645 012362 013705 012434          MOV      HLTADR,TTY     ;TYPE HLTADR IN OCTAL
4646 012366 004737 013452          JSR      PC,PRINTR     ;TYPE LEADING ZERO'S
4647 012372 000004 015704          TYPE,   SPACE          ;" "
4648 012376 004737 012436          JSR      PC,ERRORS     ;GO TO USER ERROR ROUTINE
4649 012402 004737 013164          Y$:    JSR      PC,POPX ;RESTORE REGISTERS
4650 012406 005737 177570          TST     2#SWR          ;HALT ON ERROR
4651 012412 100001          BPL     .+4            ;SKIP IF CONTINUE
4652 012414 000000          HALT                    ;HALT ON ERROR!
4653 012416 000002          RTH:   RTI             ;RETURN
4654 012420 105037 001201          CLRB   ICNT+1         ;CLEAR ITERATION COUNT
4655 012424 000137 012226          JMP     KITS           ;LOOP ON TEST UNTIL NO ERRORS
4656
4657 012430 000000          ERRORS: 0             ;ERROR COUNT
4658 012432 000000          HLTCTS: 0             ;HLT ARGUMENT
4659 012434 000000          HLTADR: 0             ;LAST HLT INSTRUCTION EXECUTED
4660
4661 012436          ERRORS:
4662 012436 016605 000004          MOV     4(SP),TTY      ;
4663 012442 004737 013452          JSR     PC,PRINTR     ;OUTPUT (PS)
4664 012446 000004 015704          TYPE,   SPACE
4665 012452 010605          MOV     SP,TTY
4666 012454 062705 000002          ADD     #2,TTY
4667 012460 004737 013452          JSR     PC,PRINTR     ;OUTPUT (SP)
4668 012464 004737 013164          JSR     PC,POPX
4669 012470 005237 012432          INC     HLTCTS
4670 012474 006201          ASR     R1
4671 012476 042737 007700 012516 BIC     #7700,2$
4672 012504 105337 012432          1$:    DECB   HLTCTS
4673 012510 100411          BMI     3$
4674 012512 000004 015704          TYPE,   SPACE

```

```

4675 012516 010005      2$:   MOV      %0,TTY           ;OUTPUT (REG"N")IN OCTAL
4676 012520 004737      013452   JSR      %7,PRINTR
4677 012524 062737      000100 012516   ADD     #100,2$
4678 012532 000764           BR      1$
4679 012534 006301      3$:   ASL     R1
4680 012536 000207           RTS     PC

4681
4682
4683           ;SUBROUTINE TO SAVE INPUT AS OCTAL NUMBER
4684
4685 012540 004737      013634  READIN: JSR     PC,READ$      ;GO READ TTY UNTIL CR
4686 012544 010146           MOV     R1,-(6)           ;PUSH R1 ON STACK
4687 012546 010246           MOV     R2,-(6)           ;PUSH R2 ON STACK
4688 012550 010346           MOV     R3,-(6)           ;PUSH R3 ON STACK
4689 012552 012501           MOV     (R5)+,R1
4690 012554 012702      013734   MOV     #INPUT,R2
4691 012560 042712      000200   BIC     #200,(R2)         ;REDUCE TO 7 LEVEL CODE
4692 012564 122712      000120   CMPB   #120,(R2)         ;CHECK"P"
4693 012570 001412           BEQ     POK
4694 012572 122712      000131   CMPB   #131,(R2)         ;CHECK "Y"
4695 012576 001407           BEQ     POK
4696 012600 122712      000116   CMPB   #116,(R2)         ;CHECK "N"
4697 012604 001404           BEQ     POK
4698 012606 005011           CLR     (R1)
4699 012610 122712      000052   CMPB   #52,(R2)         ;CHECK FOR ASTERICK "*"
4700 012614 001002           BNE     TOK              ;(NO) BRANCHES
4701 012616 111211           POK:   MOVB   (R2),(R1)     ;(YES) RECORD
4702 012620 000417           BR      MOK              ;REPORT
4703 012622 112203           TJK:   MOVB   (R2)+,R3
4704 012624 001416           BEQ     ZOK              ;BRANCH DONE
4705 012626 162703      000060   SUB     #60,R3
4706 012632 032703      177770   BIT     #177770,R3
4707 012636 001011           BNE     ZOK              ;BRANCH BAD DATREG
4708 012640 006311           ASL     (R1)
4709 012642 103406           BCS     MOK
4710 012644 006311           ASL     (R1)
4711 012646 103404           BCS     MOK
4712 012650 006311           ASL     (R1)
4713 012652 103402           BCS     MOK
4714 012654 050311           BIS     R3,(R1)
4715 012656 000761           BR      TOK
4716 012660 000244           MOK:   CLZ
4717 012662 013737      177776 012706  ZOK:   MOV     @#PS,PSTEMP      ;CLR"Z"BIT
4718 012670 012603           MOV     (6)+,R3         ;SAVE CONDITION CODES
4719 012672 012602           MOV     (6)+,R2         ;POP STACK INTO R3
4720 012674 012601           MOV     (6)+,R1         ;POP STACK INTO R2
4721 012676 013737      012706 177776   MOV     PSTEMP,@#PS     ;POP STACK INTO R1
4722 012704 000205           RTS     R5              ;RESTORE CONDITION CODES
4723 012706 000000           PSTEMP: 0
4724 012710 000000           WORK:   0
4725 012712 000000           0
4726 012714 000000           0
4727 012716 000000           0
4728           .SBTTL           TABLE AND REGISTER INITIALIZATION SUBROUTINES
4729           ;
4730           INITIALIZE STACK LIMIT REGISTER ON 11/40 OR 11/45

```



# H08

MAINDEC-11-DZCBH-B  
DZCBHB.P11

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TABLE AND REGISTER INITIALIZATION SUBROUTINES

```

4731      :      CHANGE RTI TO RTT  11/40 OR 11/45
4732      :      CLEAR REGISTERS
4733      :      CLEAR TABLES
4734      :
4735 012720 005037 014410  INITA: CLR      NSCAN
4736 012724 005037 002176      CLR      DSTADR
4737 012730 012737 012764 000010      MOV      #INITB, a#10      ;SET RESERVE INSTRUCTION TRAP VECTOR
4738 012736 012737 000340 000012      MOV      #340, a#12
4739 012744 005046      CLR      -(SP)
4740 012746 012746 012754      MOV      #INITZ, -(SP)
4741 012752 000006      RTT
4742 012754 012737 000006 013372  INITZ: MOV      #6, RTX      ;TEST RTT EXECUTION
                                        ;SET RTT CONTROL ENTRY
4743
4744
4745 012762 000402      BR      INITC      ;(OK) BRANCHES
4746
4747 012764 022626      INITB: CMP      (SP)+, (SP)+      ;RESTORE STACK
4748 012766 022626      CMP      (SP)+, (SP)+      ;TWICE ON TIMEOUT
4749 012770 013737 013372 012122  INITC: MOV      RTX, YESRT      ;REPLACE RTI WITH RTT
4750 012776 012737 000012 000010      MOV      #12, a#10
4751 013004 005037 000012      CLR      a#12
4752 013010 012737 000006 000004      MOV      #5, a#4
4753 013016 013737 013372 000006      MOV      RTX, a#6      ;SET TIME OUT TRAP VECTOR
4754 013024 012737 000400 177774      MOV      #400, SLR      ;SET STACK LIMIT REGISTER
4755 013032 005037 000006      CLR      a#6      ;TRAP CATCHER
4756 013036 012700 000630      INITX: MOV      #630, R0      ;DEVICE VECTOR BASE
4757 013042 012701 000632      MOV      #632, R1      ;SET "IOT"
4758 013046 010120      4$:  MOV      R1, (R0)+      ;UNEXPECTED
4759 013050 012720 000004      MOV      #IOT, (R0)+      ;INTERRUPT
4760 013054 062701 000004      ADD      #4, R1      ;VECTOR(S)
4761 013060 022701 001000      CMP      #1000, R1      ;TRAP
4762 013064 101370      BHI     4$      ;CATCHER
4763
4764 013066 005037 001262      CLR      PASSES
4765
4766 013072 012737 000340 177776  INITQ: MOV      #340, PSW      ;SET PROCESSOR PRIORITY = 7
4767 013100 012737 012010 000004      MOV      #BUSERR, a#4      ;LINK BUS TIME-OUT ERROR TRAP CATCHER
4768 013106 012737 000340 000006      MOV      #340, a#6      ;LEVEL = 7
4769
4770      :
4771 013114 005000      INITR: CLEAR REGISTERS
4772 013116 005001      CLR      R0      ;CLEAR
4773 013120 005002      CLR      R1
4774 013122 005003      CLR      R2      ;ALL
4775 013124 005004      CLR      R3      ;WORKING
4776 013126 005005      CLR      R4      ;REGISTERS
4777      CLR      R5
4778 013130 000207      ;      RTS      PC      ;CONTINUE
4779
4780 013132 010027      PUSHX: MOV      R0, (PC)+
4781 013134 000000      S0:  0      ;SAVE REGISTERS
4782 013136 010127      MOV      R1, (PC)+
4783 013140 000000      S1:  0
4784 013142 010227      MOV      R2, (PC)+
4785 013144 000000      S2:  0
4786 013146 010327      MOV      R3, (PC)+

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4787	013150	000000		S3:	0		
4788	013152	010427			MOV	R4, (PC)+	
4789	013154	000000		S4:	0		
4790	013156	010527			MOV	R5, (PC)+	
4791	013160	000000		S5:	0		
4792	013162	000207			RTS	PC	; RETURN
4793							
4794	013164	013705	013160	POPX:	MOV	S5, R5	
4795	013170	013704	013154		MOV	S4, R4	; RESTORE REGISTERS
4796	013174	013703	013150		MOV	S3, R3	
4797	013200	013702	013144		MOV	S2, R2	
4798	013204	013701	013140		MOV	S1, R1	
4799	013210	013700	013134		MOV	S0, R0	
4800	013214	000207			RTS	PC	; RETURN
4801							
4802	013216	000774		\$VEC:	774		; CB11-HA INTERRUPT VECTOR ADDRESS UNDER TEST
4803	013220	000000		ZERO:	0		
4804							
4805							
4806	013222	000774		VT.H0:	774		; DEFAULT VECTOR ADDRESS BUFFER
4807	013224	000770		VT.H1:	770		
4808	013226	000764		VT.H2:	764		
4809	013230	000760		VT.H3:	760		
4810	013232	000754		VT.H4:	754		
4811	013234	000750		VT.H5:	750		
4812	013236	000744		VT.H6:	744		
4813	013240	000740		VT.H7:	740		
4814	013242	000734		VT.H10:	734		
4815	013244	000730		VT.H11:	730		
4816	013246	000724		VT.H12:	724		
4817	013250	000720		VT.H13:	720		
4818	013252	000714		VT.H14:	714		
4819	013254	000710		VT.H15:	710		
4820	013256	000704		VT.H16:	704		
4821	013260	000700		VT.H17:	700		
4822	013262	000674		VT.H20:	674		
4823	013264	000670		VT.H21:	670		
4824	013266	000664		VT.H22:	664		
4825	013270	000660		VT.H23:	660		
4826	013272	000654		VT.H24:	654		
4827	013274	000650		VT.H25:	650		
4828	013276	000644		VT.H26:	644		
4829	013300	000640		VT.H27:	640		
4830	013302	000634		VT.H30:	634		
4831	013304	000630		VT.H31:	630		
4832	013306	000040		LVL.H0:	40		
4833	013310	000040		LVL.H1:	40		
4834	013312	000040		LVL.H2:	40		
4835	013314	000040		LVL.H3:	40		
4836	013316	000040		LVL.H4:	40		
4837	013320	000040		LVL.H5:	40		
4838	013322	000040		LVL.H6:	40		
4839	013324	000040		LVL.H7:	40		
4840	013326	000040		LVL.H10:	40		
4841	013330	000040		LVL.H11:	40		
4842	013332	000040		LVL.H12:	40		

4843	013334	000040			LVLH13:	40		
4844	013336	000040			LVLH14:	40		
4845	013340	000040			LVLH15:	40		
4846	013342	000040			LVLH16:	40		
4847	013344	000040			LVLH17:	40		
4848	013346	000040			LVLH20:	40		
4849	013350	000040			LVLH21:	40		
4850	013352	000040			LVLH22:	40		
4851	013354	000040			LVLH23:	40		
4852	013356	000040			LVLH24:	40		
4853	013360	000040			LVLH25:	40		
4854	013362	000040			LVLH26:	40		
4855	013364	000040			LVLH27:	40		
4856	013366	000040			LVLH30:	40		
4857	013370	000040			LVLH31:	40		
4858	013372	000002			RTX:	RTI		:
4859								
4860	013374	032737	020000	177570	HTST\$:	BIT	#BIT13,SWR	;TEST SUPPRESS TYPEOUT SELECTED
4861	013402	001401				BEQ	IS	; (NO) BRANCHES
4862	013404	000207				RTS	PC	; (YES) EXIT
4863								
4864	013406	020027			IS:	CMP	RD,(PC)+	
4865	013410	000000			RSO:	0		;TEST HEADER REQUIRED
4866	013412	001407				BEQ	HOUT	; (NO) BRANCHES
4867	013414	010037	013410			MOV	RD,RSO	;SET SINGLE OUTPUT CONTROL FLAG
4868	013420	000004	015375			TYPE,	MTST	
4869	013424	010005				MOV	RD,TTY	
4870	013426	004737	013462			JSR	PC,PRINTS	
4871								
4872	013432	000004	015412		HOUT:	TYPE,	MCRLF	
4873	013436	000207				RTS	PC	
4874								
4875	013440	177777			FLAGH:	177777		

# K08

MAINDEC-11-DZCBH-B  
DZCBHB.P11

CS11-MA LOGIC TEST  
OCTAL DUMP OF A WORD

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4876 ; SUCTAL OCTAL TYPEOUT ROUTINE
4877
4878 ; THIS ROUTINE IS USED TO TYPE AN OCTAL NUMBER ON THE TTY. IT WILL TYPE
4879 ; ALL 6 CHARACTERS, SUPPRESS LEADING ZEROES, TYPE AN 18 BIT ADDRESS, OR TYPE
4880 ; THE 16 BITS. IT IS CALLED VIA THE DUMP, SDUMP, DUMP18, OR BITYPE MACRO'S.
4881
4882 013442 012737 170101 013610 BITYPS: MOV #170101,.PR ;SET BIT FLAG ANS 16. CHARACTER COUNT
4883 013450 000411 BR .PTIT ;NOW TYPE IT IN BIT FORM
4884 013452 112737 000001 013610 PRINTR: MOVB #1,.PR ;SET ZERO FILL SWITCH
4885 013460 000402 BR .+6 ;SKIP
4886 013462 005037 013610 PRINTS: CLR .PR ;SUPPRESS LEADING ZERO'S
4887 013466 112737 177772 013611 MOVB #-6,.PR+1 ;SET COUNT
4888 013474 010446 .PTIT: MOV R4,-(6) ;SAVE R4
4889 013476 012704 013612 MOV #.PR+2,R4 ;SET POINTER TO FIRST ASCII CHAR.
4890 013502 105014 CLRB (4) ;CLEAR FIRST BYTE
4891 013504 000411 BR .PRF ;ROTATE FIRST BIT
4892 013506 105014 .PRL: CLRB (4) ;CLEAR BYTE OF CHARACTER
4893 013510 032737 000100 013610 BIT #100,.PR ;BIT TYPING MODE?
4894 013516 001004 BNE .PRF ;YES - SKIP 2 ROTATES
4895 013520 006105 ROL TTY ;ROTATE BIT INTO C
4896 013522 106114 ROLB (4) ;PACK IT
4897 013524 006105 ROL TTY ;ROTATE BIT INTO C
4898 013526 106114 ROLB (4) ;PACK IT
4899 013530 006105 .PRF: ROL TTY ;ROTATE BIT INTO C
4900 013532 106114 ROLB (4) ;PACK IT
4901 013534 105714 TSTB (4) ;IS IT ZERO?
4902 013536 001402 BEQ .+6 ;SKIP INC
4903 013540 105237 013610 INCB .PR ;SET FILL SWITCH
4904 013544 105737 013610 TSTB .PR ;CHECK FILL SWITCH
4905 013550 001402 BEQ .+6 ;SKIP BITSET
4906 013552 152724 000060 BISB #'0,(4)+ ;MAKE INTO ASCII CHAR
4907 013556 105237 013611 INCB .PR+1 ;INC COUNT
4908 013562 001351 BNE .PRL ;REPEAT
4909 013564 022704 013612 CMP #.PR+2,R4 ;EMPTY BUFFER?
4910 013570 001002 BNE .+6 ;SKIP IF NOT
4911 013572 112724 000060 MOVB #'0,(4)+ ;LOAD 1 ZERO
4912 013576 105014 CLRB (4) ;NULL TERMINATOR
4913 013500 000004 013612 TYPE .PR+2 ;TYPE IT
4914 013604 012604 MOV (6)+,R4 ;RESTORE R4
4915 013606 000207 RTS PC ;RETURN
4916 013610 000012 .PR: .BLKW 12 ;COUNT, SWITCH, AND OUTPUT BUFFER

```

# L08

MAINDEC-11-DZCBH-B  
DZCBHB.P11

CS11-MA LOGIC TEST  
TTY INPUT ROUTINE

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4917	013634	010346		READS:	MOV	R3, -(6)	:SAVE R3
4918	013636	012703	013734	1\$:	MOV	#INPUT, R3	:GET ADDRESS
4919	013642	022703	013754	2\$:	CMP	#INPUT+20, R3	:BUFFER FULL?
4920	013646	001412			BEQ	4\$	:YES - TYPE "?"
4921	013650	105737	177560		TSTB	@#177560	:WAIT FOR
4922	013654	100375			BPL	.-4	:A CHARACTER
4923	013656	113713	177562		MOVB	@#177562, (3)	:GET CHARACTER
4924	013662	142713	000200		BICB	#200, (3)	:GET RID OF JUNK
4925	013666	122713	000177		CMPB	#177, (3)	:IS IT A RUBOUT
4926	013672	001003			BNE	3\$	:SKIP IF NOT
4927	013674	000004	016011	4\$:	TYPE,	MSGQQ	:ASCII "?"<15><12>
4928	013700	000756			BR	1\$	:ZAP THE BUFFER AND LOOP
4929	013702	111337	014370	3\$:	MOVB	(3), .TYPE	:SET UP FOR TYPING
4930	013706	000004	014370		TYPE	.TYPE	:ECHO IT
4931	013712	122723	000015		CMPB	#15, (3)+	:CHECK FOR RETURN
4932	013716	001351			BNE	2\$	:LOOP IF NOT RETURN
4933	013720	105063	177777		CLRB	-1(3)	:ZAP RETURN (THE 15)
4934	013724	000004	000012		TYPE	.12	:TYPE A LINE FEED
4935	013730	012603			MOV	(6)+, R3	:RESTORE R3
4936	013732	000207			RTS	PC	:RETURN
4937	013734	000020		INPUT:	.BLKW	20	:TTY INPUT AREA

# M08

MAINDEC-11-DZCBH-B  
DZCBHB.P11

CS11-MA LOGIC TEST      MACY11 27(732)    11-OCT-76    10:43    PAGE 104  
POWER DOWN AND UP ROUTINES

```

4938 013774 012777 014120 000124 PDOWN$: MOV #ILLUP, @PUVECS ;SET FOR FAST UP
4939 014002 012777 000340 000120 MOV #340, @PUVECS+2 ;PRIO:7
4940 014010 010046 MOV R0, -(6) ;PUSH R0 ON STACK
4941 014012 010146 MOV R1, -(6) ;PUSH R1 ON STACK
4942 014014 010246 MOV R2, -(6) ;PUSH R2 ON STACK
4943 014016 010346 MOV R3, -(6) ;PUSH R3 ON STACK
4944 014020 010446 MOV R4, -(6) ;PUSH R4 ON STACK
4945 014022 010546 MOV R5, -(6) ;PUSH R5 ON STACK
4946 014024 010637 014124 MOV SP, SAVR6 ;SAVE SP
4947 014030 012777 014040 000070 MOV #PUP$, @PUVECS ;SET UP VECTOR
4948 014036 000000 HALT ;WAIT FOR PF
4949
4950 014040 013706 014124 PUP$: MOV .SAVR6, SP ;GET SP
4951 014044 005001 CLR R1 ;WAIT LOOP FOR THE TTY
4952 014046 005201 1$: INC R1 ;WAIT FOR THE INC
4953 014050 001376 BNE 1$ ;OF WORD
4954 014052 012605 MOV (6)+, R5 ;POP STACK INTO R5
4955 014054 012604 MOV (6)+, R4 ;POP STACK INTO R4
4956 014056 012603 MOV (6)+, R3 ;POP STACK INTO R3
4957 014060 012602 MOV (6)+, R2 ;POP STACK INTO R2
4958 014062 012601 MOV (6)+, R1 ;POP STACK INTO R1
4959 014064 012600 MOV (6)+, R0 ;POP STACK INTO R0
4960 014066 012737 013774 000024 MOV #PDOWN$, @#24 ;SET UP THE POWER DOWN VECTOR
4961 014074 012737 000340 000026 MOV #340, @#26 ;PRIO:7
4962 014102 052737 000017 000022 BIS #17, @#22 ;SET UNCONDITIONAL TEXT CONTROL ACTIVE
4963 014110 000004 016015 TYPE, MSGPWR ;<15><12> POWER
4964 014114 000137 001260 JMP RESTAR ;JMP TO USER ADDRESS
4965
4966 014120 000000 ILLUP: HALT ;THE POWER UP SEQUENCE WAS STARTED
4967 014122 000776 BR .-2 ; BEFORE THE POWER DOWN WAS COMPLETE
4968
4969 014124 000000 .SAVR6: 0 ;PUT THE SP HERE
4970 014126 000024 000026 PUVECS: 24, 26 ;POWER UP VECTOR

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4971 ;*****
4972 ;
4973 ; IOT PROCESSOR: DETERMINE IF CALL IS A "FALSE INTERRUPT/TRAP"
4974 ; OR "TYPE MESSAGE CALL".
4975 ;*****
4976
4977 014132 013737 177776 014226 IOTRAP: MOV PSW,PSWS ;RECORD CONDITION CODES
4978 014140 022716 000100 CMP #100,(SP) ;TEST FOR FALSE INTERRUPT/TRAP
4979 014144 002431 BLT IOTS ;(NC) "TYPE" COMMAND BRANCHES
4980 ; UNEXPECTED INTERRUPT
4981 014146 012737 000340 177776 ;
4982 014154 010127 MOV #340,PSW ;RAISE PRIORITY LEVEL TO 7
4983 014156 000000 MOV R1,(PC)+
4984 014160 010227 SAV1: 0 ;SAVE R1
4985 014162 000000 MOV R2,(PC)+ ;SAVE R2
4986 014164 010527 SAV2: 0
4987 014166 000000 SAV5: 0 ;SAVE R5
4988 014170 162716 000004 SUB #4,(SP) ;FETCH VECTOR ADDRESS
4989 014174 012601 MOV (SP)+,R1 ;VECTOR ADDRESS>R1
4990 014176 005726 TST (SP)+ ;POP STACK
4991 014200 011602 MOV (SP),R2 ;RETURN PC> R2
4992 ;*****
4993 ;
4994 ; UNEXPECTED INTERRUPT
4995 ;
4996 ; DISPLAY SIGNIFICANCE
4997 ;
4998 014202 006301 ASL R1
4999 ; (PC) (PS) (SP) TEST VECTOR INSTADD
5000 ; (R7) (PSW) (R6) (R0) (R1) (R2)
5001 ;
5002 014204 104002 ERTRAP: HLT+2 ;UNEXPECTED INTERRUPT TO VECTOR ADDRESS (R1)
5003 ; WHILE EXECUTING CODE PRIOR TO ADDRESS (R2)
5004 ; IN TEST NUMBER (R0)
5005 ;
5006 014206 000000 ; HALT ;NOT EXPECTED TO RECOVER
5007 ;
5008 014210 013705 014166 MOV SAV5,R5 ;RESTORE R5
5009 014214 013702 014162 MOV SAV2,R2 ;RESTORE R2
5010 014220 013701 014156 MOV SAV1,R1 ;RESTORE R1
5011 014224 000002 RTA ;CONTINUE
5012 014226 000000 PSWS: 0
5013 ;
5014 ; MCALL $TYPE
5015 ; $TYPE MESSAGE TYPEOUT ROUTINE
5016 ;
5017 ; THIS ROUTINE IS USE TO TYPE ASCII MESSAGES ON THE TTY. THE
5018 ; CALL CAN BE IN ONE OF 3 FORMS: 1) "TYPE ADR" - TYPES THE
5019 ; MESSAGE STARTING IN LOCATION "ADR:", 2) "TYPE CHAR" - TYPES
5020 ; THE ASCII "CHAR", AND 3) "PRINT <<15><12>"MESSAGE">" - TYPES
5021 ; THE MESSAGE WHICH IS INLINE ASCII.
5022 ;
5023 014230 032737 020000 177570 IOTS: BIT #BIT13,SWR ;INHIBIT OUTPUT SELECTED
5024 014236 001412 BEQ FS ;(NO) BRANCHES
5025 ;
5026 014240 042737 177760 014226 BIC #177760,PSWS

```

MACY11-11-0208H-S  
TYPE ROUTINE

0311-HP LOGIC TEST  
TYPE ROUTINE

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```

000001 014246 022737 000017 014226
000002 014251 001403
000003 014256 062716 000002
000004 014261 000441
000005 014266 010546 FS:
000006 014271 017605 000002
000007 014276 032705 177400
000008 014281 001004
000009 014286 010537 014370
000010 014291 012705 014370
000011 014300 105715 IS:
000012 014305 001406
000013 014310 112537 177566
000014 014315 105737 177564
000015 014320 109375
000016 014325 000770
000017 014330 017646 000002 28:
000018 014335 062766 000002 000004
000019 014340 022666 000002
000020 014345 001006
000021 014350 062705 000002
000022 014355 042705 000001
000023 014360 010566 000002
000024 014365 012605 38:
000025 014370 000002 RTK:
000026 014375 000000 .TYPE:
000027 .EVEN

```

```

CMP #17,PSWS
BEQ FS
ADD #2,(6) ;BYPASS ADDRESS
BR RTK ;EXIT
MOV TTY,-(6) ;SAVE TTY
MOV #2(6),TTY ;GET ADDRESS TO BE TYPED
BIT #177400,TTY ;IS IT A TYPEM?
BNE IS ;NO
MOV TTY,TYPE ;GET THE CHARACTER
MOV #.TYPE,TTY ;FUDGE THE ADDRESS
TSTB (TTY) ;TERMINATOR?
SEQ #25 ;GET OUT IF SO
MOV# (TTY)+,#177566 ;LOAD AND TYPE THE CHARACTER
TSTB #177564 ;IS THE PRINTER READY
BPL -4 ;WAIT UNTIL IT IS
BR IS ;GET THE NEXT CHARACTER
MOV #2(6),-(6) ;GET ADDRESS TO BE TYPED
ADD #2,4(6) ;ADD 2 TO THE ADDRESS
CMP (6)+,#2(6) ;IS IT .+2?
BNE #25 ;NO
ADD #2,TTY ;ADD 2 TO THE ADDRESS
BIC #1,TTY ;BACK UP TO AN EVEN BYTE
MOV TTY,2(6) ;RESTORE ADDRESS
MOV (6)+,TTY ;RESTORE TTY
RTN ;RETURN
;CHARACTER TYPE LOCATION

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1000

014372 004737 013114  
014376 012700 164000  
014402 010037 000316  
014406 005027  
014410 000000  
014412 005037 014456  
014416 112760 000377 000001  
014424 000261  
014426 005710  
014430 103002  
014432 000137 014506  
014436 122760 000017 000001  
014444 001011  
014446 005737 014456  
014450 001002  
014454 010027  
014456 000000  
014460 010027  
014462 000000  
014464 005237 014410  
014470 005010  
014472 020027  
014474 167770  
014476 101014  
014500 062700 000010  
014504 000744  
014506 005737 014410  
014512 001766  
014514 062700 000010  
014520 010037 000316  
014524 010037 001566  
014530 005737 014410  
014534 001420  
014536 013705 014456  
014542 000004 015707  
014546 004737 013462  
014550 023737 014456 014462  
014560 001406  
014562 000004 015740  
014566 013705 014462  
014572 004737 013462  
014576 000207

.SBTTL SYSTEMS SIZER (SCAN) MODULE

SCNMAP: JSR PC, INTR  
MOV #164000, RO ;SET BASE SCAN ADDRESS  
MOV RO, FSTADR  
CLR (PC)+  
NSCAN: 0  
CLR FSCAN  
MAP.S0: MOV #377, 1(RO) ;INITIALIZE MAINTENANCE SCAN RESPONSE  
SEC ;SET CARRY  
TST (RO) ;TEST DEVICE RESPONSE  
BCC MAP.S1 ;ACTIVE BRANCHES  
JMP MAP.S2 ;NONE JUMPS  
MAP.S1: CMP #17, 1(RO) ;TEST SCAN MAINTAINANCE RESPONSE  
BNE XAS ;NOT A SCAN BRANCHES  
TST FSCAN  
BNE MIS  
MOV RO, (PC)+  
FSCAN: 0  
MIS: MOV RO, (PC)+  
LSCAN: 0  
INC NSCAN  
XAS: CLR (RO)  
CMP RO, (PC)+ ;TEST SCAN LIMIT  
LIMITS: 167770  
BHI XXAS  
ADD #10, RO ;NEXT ADDRESS  
BR MAP.S0  
MAP.S2: TST NSCAN ;TEST ACTIVITY  
BEQ XAS ;(NO) BRANCHES  
ADD #10, RO ;OFFSET MODULO 10  
MAP.S3: MOV RO, FSTADR ;SET INTERRUPT MODULE BASE  
MOV RO, LOWADD ;SET LOW ADDRESS  
XXAS: TST NSCAN ;CHECK ACTIVITY  
BEQ SCNOUT ;(NO) BRANCHES  
MOV FSCAN, TTY  
TYPE, MSCN ;OUTPUT SCAN ADDRESSES  
JSR PC, PRINTS ;IN OCTAL  
CMP FSCAN, LSCAN ;TEST ADDITIONAL  
BEQ SCNOUT ;(NO) BRANCHES  
TYPE, MTHRU ;OUTPUT "THRU"  
MOV LSCAN, TTY  
JSR PC, PRINTS  
SCNOUT: RTS PC ;RETURN

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.SBTTL          SYSTEMS SIZER (DISTRIBUTE) MODULE
S101
S102
S103 014600 004737 013114 DSTMAP: JSR PC, INTR
S104 014604 013700 000352          MOV LSTADR, RO          ;SET BASE DISTRIBUTE ADDRESS
S105 014610 010037 000316          MOV RO, FSTADR
S106 014614 005027          CLR (PC)+
S107 014616 000000          NDSTB: 0
S108 014620 005037 014652          CLR FDSTB
S109 014624 012710 177777 MAP.DO: MOV #177777, (RO) ;INITIALIZE MAINTENANCE DISTB RESPONSE
S110 014630 000261          SEC ;SET CARRY
S111 014632 005710          TST (RO) ;TEST DEVICE RESPONSE
S112 014634 103002          BCC MAP.D1 ;ACTIVE BRANCHES
S113 014636 000137 014722          JMP MAP.D2 ;NONE JUMPS
S114 014642 022710 177777 MAP.D1: CMP #177777, (RO) ;TEST DISTB MAINTAINENANCE RESPONSE
S115 014646 001016          BNE XBS ;NOT A DISTRIBUTE BRANCHES
S116 014650 005727          TST (PC)+
S117 014652 000000          FDSTB: 0
S118 014654 001002          BNE IS
S119 014656 010037 014652          MOV RO, FDSTB
S120 014662 010027          IS: MOV RO, (PC)+
S121 014664 000000          LDSTB: 0
S122 014666 005010          CLR (RO) ;INITIALIZE DISTRIBUTE
S123 014670 005710          TST (RO) ;TEST RESULTS
S124 014672 00:402          BEQ ZS ;(OK) BRANCHES
S125
S126 014674 000000          HALT ;DISTRIBUTE MODULE (RO) FAILED TO CLEAR
S127 ;SUGGEST YOU RUN THE DISTRIBUTE DIAGNOSTICS
S128 014676 000740          BR DSTMAP ;NO GO BRANCH
S129
S130 014700 005237 014616          ZS: INC NDSTB
S131 014704 005010          XBS: CLR (RO)
S132 014706 062700 000004          ADD #4, RO ;NEXT ADDRESS
S133 014712 020027          CMP RO, (PC)+ ;TEST SCAN LIMIT
S134 014714 170000          LIMITD: 170000
S135 014716 101033          BHI DSTOUT ;EXCEEDED EXIT
S136 014720 000741          BR MAP.DO
S137 014722 005737 014616          MAP.D2: TST NDSTB ;TEST ACTIVITY
S138 014726 001766          BEQ XBS ;(NO) BRANCHES
S139 014730 062700 000004          ADD #4, RO ;OFFSET MODULO 4
S140 014734 010037 000316          MAP.D3: MOV RO, FSTADR ;SET DISTRIBUTE MODULE BASE
S141 014740 005737 014616          MAP.D4: TST NDSTB ;CHECK ACTIVITY
S142 014744 001420          BEQ DSTOUT ;(NO) BRANCHES
S143 014746 000004 015755          TYPE, MOST ;OUTPUT DISTRIBUTE ADDRESSES
S144 014752 013705 014652          MOV FDSTB, TTY
S145 014756 004737 013462          JSR PC, PRINTS ;IN OCTAL
S146 014762 023737 014652 014664          CMP FDSTB, LDSTB ;TEST ADDITIONAL
S147 014770 001406          BEQ DSTOUT ;(NO) BRANCHES
S148 014772 000004 015740          TYPE, MTHRU ;OUTPUT "THRU"
S149 014776 013705 014664          MOV LDSTB, TTY
S150 015002 004737 013462          JSR PC, PRINTS
S151 015006 000207          DSTOUT: RTS ;RETURN
S152
S153 015010 000032          MX.CBH: 32

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E09

MAINDEC-11-DZC84-8  
DZC84B.P11

CB11-HA LOGIC TEST MACY11 27(732) 11-OCT-76 10:43 PAGE 109  
SYSTEMS SIZER (DISTRIBUTE) MODULE

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015012 005015 041103 030461 MSG1: .ASCIZ <15><12>"CB11-HA"<15><12>"CONFIGURATION"<15><12>  
015020 044055 006501 041412  
015026 047117 044506 052507  
015034 040522 044524 047117  
015042 005015 000

015045 101 042104 042522 MSG2: .ASCIZ "ADDRESS(ES) VECTOR(S) PRIORITY (-)TRANS (+)TRANS"<15><12><15><12>  
015052 051523 042450 024523  
015060 053040 041505 047524  
015066 024122 024523 050040  
015074 044522 051117 052111  
015102 020131 020040 026450  
015110 052051 040522 051516  
015116 020040 020040 020040  
015124 025450 052051 040522  
015132 051516 005015 005015

015140 000  
015141 015 044412 052116 MSG2X: .ASCIZ <15><12>"INTERRUPT"<15><12>  
015146 051105 052522 052120  
015154 005015 000

015157 015 040412 042104 MSG3X: .ASCIZ <15><12>"ADDRESS(ES)"<15><12>  
015164 042522 051523 042450  
015172 024523 005015 000

015177 015 000012  
015202 005015 042524 052123 CRLF: .ASCIZ <15><12>  
MSG3: .ASCIZ <15><12>"TEST:"<15><12>

015210 006472 000012  
015214 005015 047516 042040 MSG6: .ASCIZ <15><12>"NO DEVICE RESPONSE TO ADDRESS ?"<15><12>  
015222 053105 041511 020105  
015230 042522 050123 047117  
015236 042523 052040 020117  
015244 042101 051104 051505

015252 020123 006477 000012  
015260 005015 047516 020127 MSG7: .ASCIZ <15><12>"NOW TESTING" <15><12>  
015266 042524 052123 047111  
015274 006507 000012

015300 005015 052502 020123 MSGBUS: .ASCIZ <15><12>"BUS TIME-OUT ERROR TRAP"  
015306 044524 042515 047455  
015314 052125 042440 051122  
015322 051117 052040 040522  
015330 000120

015332 005015 042504 044526 MSGTPO: .ASCIZ <15><12>"DEVICE TRAPPING TO LOCATION ZERO"  
015340 042503 052040 040522

015346 050120 047111 020107  
015354 047524 046040 041517  
015362 052101 047511 020116  
015370 042532 047522 000  
015375 015 006412 052012 MTST: .ASCIZ <15><12><15><12>"TEST# : "  
015402 051505 021524 035040

015410 000040  
015412 005015 000 MCRLF: .ASCIZ <15><12>  
015415 040 020040 020040 MSGSP: .ASCIZ " " " "  
015422 020040 000040

015426 036440 044440 046114 MSGE: .ASCIZ " = ILLEGAL ? "<15><12>

# F09

MAINDEC-11-0208n-8  
0208MB.P11

0311-HP LOGIC TEST  
ASCIZ TEXT BUFFERS

MAC11 27(732) 11-OCT-76 10:43 PAGE 110

5211	015434	043505	046101	037440																
5212	015442	006440	000012																	
5213	015446	005015	024040	041520	MSGMED: .ASCIZ	<15><12>"	(PC)	(PS)	(SP)	TEST	DEV#	ADDRESS	WAS	SHD	BE					
5214	015454	020051	020040	024040																
5215	015462	051520	020051	020040																
5216	015470	024040	050123	020051																
5217	015476	020040	052040	051505																
5218	015504	020124	020040	042040																
5219	015512	053105	020043	040440																
5220	015520	042104	042522	051523																
5221	015526	020040	053440	051501																
5222	015534	020040	020040	051440																
5223	015542	042110	041040	000105																
5224	015550	005015	024040	033522	MSGSUB: .ASCIZ	<15><12>"	(R7)	(PSW)	(R6)	(R0)	(R1)	(R2)	(R3)	(R4)"						
5225	015556	020051	020040	024040																
5226	015564	051520	024527	020040																
5227	015572	024040	033122	020051																
5228	015600	020040	024040	030122																
5229	015606	020051	020040	024040																
5230	015614	030522	020051	020040																
5231	015622	051050	024462	020040																
5232	015630	020040	024040	031522																
5233	015636	020051	020040	024040																
5234	015644	032122	000051																	
5235	015650	005015	040520	051523	MSGPAS: .ASCIZ	<15><12>"	PASS(ES) = "													
5236	015656	042450	024523	036440																
5237	015664	000040																		
5238	015666	005015	051105	047522	MSGERR: .ASCIZ	<15><12>"	ERROR(S) = "													
5239	015674	024122	024523	036440																
5240	015702	000040																		
5241	015704	020040	000		SPACE: .ASCIZ	" "														
5242																				
5243																				
5244	015707	015	020012	020040	MSCN: .ASCIZ	<15><12>"	SCAN"	<15><12>"	ADDRESS(ES)"	<15><12>										
5245	015714	041523	047101	005015																
5246	015722	042101	051104	051505																
5247	015730	024123	051505	006451																
5248	015736	000012																		
5249	015740	005015	020040	020040	MTHRU: .ASCIZ	<15><12>"	THRU"	<15><12>												
5250	015746	044124	052522	005015																
5251	015754	000																		
5252	015755	015	042012	051511	MDST: .ASCIZ	<15><12>"	DISTRIBUTE"	<15><12>"	ADDRESS(ES)"	<15><12>										
5253	015762	051124	041111	052125																
5254	015770	006505	040412	042104																
5255	015776	042522	051523	042450																
5256	016004	024523	005015	000																
5257	016011	077	005015	000	MSGQQ: .ASCIZ	"?"	<15><12>													
5258	016015	015	020012	047520	MSGPWR: .ASCIZ	<15><12>"	POWER "													
5259	016022	042527	020122	000																
5260																				
5261																				
5262																				
5263																				
5264																				
5265																				
5266	016027	015	042012	051511	MSGO: .ASCIZ	<15><12>"	DISCONNECT USER INTERFACE"													

;  
;  
;  
; THE FOLLOWING ASCII TEXT IS UNCONDITIONAL  
I.E. IT CAN NOT BE INHIBITED BY SWR BIT 13  
(INHIBIT/TYPOUT) IT IS RESPONSE REQUEST RELPY TEXT.

5267	016034	047503	047116	041505	
5268	016042	020124	051525	051105	
5269	016050	044440	052116	051105	
5270	016056	040506	042503	000	
5271	016063	015	052012	050131	MSG0: .ASCIZ <15><12>"TYPE 'P' TO PROCEED ?"<15><12>
5272	016070	020105	050047	020047	
5273	016076	047524	050040	047522	
5274	016104	042503	042105	037440	
5275	016112	005015	000		
5276	016115	015	040412	042104	MSG4: .ASCIZ <15><12>"ADDRESS: ?"<15><12>
5277	016122	042522	051523	020072	
5278	016130	006477	000012		
5279	016134	005015	042526	052103	MSG5: .ASCIZ <15><12>"VECTOR: ?"<15><12>
5280	016142	051117	020072	006477	
5281	016150	000012			
5282	016152	005015	051120	047511	MSG8: .ASCIZ <15><12>"PRIORITY: ?"<15><12>
5283	016160	044522	054524	020072	
5284	016166	006477	000012		
5285					
5286	016172	005015	044504	052123	MDSTB: .ASCIZ <15><12>"DISTB TIED TO INTERRUPT ?"<15><12>
5287	016200	020102	044524	042105	
5288	016206	052040	020117	047111	
5289	016214	042524	051122	050125	
5290	016222	020124	006477	000012	
5291	016230	005015	044504	052123	MDADR: .ASCIZ <15><12>"DISTRIBUTE"<15><12>"ADDRESS ?"<15><12>
5292	016236	044522	052502	042524	
5293	016244	005015	042101	051104	
5294	016252	051505	020123	006477	
5295	016260	000012			
5296					
5297					.EVEN
5298					
5299	016262	000000			TABLEB: 0
5300					
5301		016262			CADCSR=TABLEB
5302		016350			CADDR=CADCSR+54.
5303		016436			CADTSR=CADDR+54.
5304		016524			CADTER=CADTSR+54.
5305		016612			CVT.CB=CADTER+54.
5306		016700			CLV.CB=CVT.CB+54.
5307		016766			DATABF=CLV.CB+54.
5308		017054			CNGBUF=DATABF+54.
5309		017142			TABLEN=CNGBUF+54.
5310					
5311					
5312					

```

5313 .SBTTL          CLOCK TIMING ONCE ONLY EXECUTION CODE
5314
5315 :             THE FOLLOWING CODE IS "ONCE ONLY EXECUTION CODE"
5316 :             I.E. ONCE THE CODE IS EXECUTED IN THIS AREA OF
5317 :             THE PROGRAM, THE AREA IS CLEARED OUT AND UTILIZED
5318 :             FOR CONTROL TABLE STORAGE.
5319
5320
5321 016264 012737 016402 000100 5.2 CLKRTN: MOV    #TICK, @#100
5322 016272 012737 016402 000104 5.2      MOV    #TICK, @#104
5323 016300 012737 016346 000004 5.2      MOV    #XLINK, @#4
5324 016306 012737 000240 000006 5.2      MOV    #240, @#6
5325 016314 004737 013114          5.8      JSR    PC, INTR          ;CLEAR ALL REGISTERS
5326
5327 016320 005037 016442          3.7 CLKRTX: CLR    TIMEXX      ;INITIALIZE
5328 016324 005037 177776          3.7      CLR    PSW
5329
5330 :             CLOCK ENABLE
5331 :
5332 016330 012737 000001 172542 5.2      MOV    #1, @#172542      ;KW11P COUNT SET BUFFER = 1
5333 016336 012737 000115 172540 5.2      MOV    #115, @#172540  ;KW11P CONTROL + STATUS REGISTER ENB
5334 016344 000411          2.6      BR     Q2$
5335 016346 022626          4.7 XLINK:  CMP    (SP)+, (SP)+
5336 016350 012737 016366 000004 5.2      MOV    #Q1$, @#4
5337 015356 012737 000115 177546 5.2      MOV    #115, @#177546  ;KW11L CONTROL + STATUS REGISTER ENB
5338 016364 000401          2.6      BR     Q2$
5339 016366 022626          4.7 Q1$:   CMP    (SP)+, (SP)+
5340 016370 005205          2.3 Q2$:   INC    R5
5341 016372 001376          2.6      BNE   Q2$          ;STALL FOR FIRST CLOCK TICK
5342
5343 016374 104000          ERNCLK: HLT          ;NO REAL TIME CLOCK PRESENT
5344
5345 :             PLUG IN A KW11L OR KW11P PLEASE
5346
5347 016376 000000          1.8 HALT          ;NO GO HALT
5348 016400 000731          2.6 BR     CLKRTN      ;TRY AGAIN
5349
5350 :             ENTRY FOLLOWING FIRST CLOCK TICK
5351
5352 016402 022626          4.7 TICK:  CMP    (SP)+, (SP)+      ;RESTORE STACK
5353 016404 012737 000006 000004 5.2      MOV    #6, @#4
5354 016412 013737 013372 000006 5.2      MOV    RTX, @#6
5355 016420 012737 016454 000100 5.2      MOV    #TOCK, @#100
5356 016426 012737 016454 000104 5.2      MOV    #TOCK, @#104
5357 016434 005037 177776          3.7      CLR    PSW
5358
5359 016440 005227          3.7 TIMIT: INC    (PC)+      ;CALCULATE 16.7 MILLISECOND
5360 016442 017777          2.6 TIMEXX: 17777      ;HERE
5361 016444 001375          2.6      BNE   TIMIT
5362
5363 016446 104000          1.8 ERTCLK: HLT          ;TIME INTERVAL MUCH TO LONG ERROR
5364 016450 000000          1.8 HALT          ;NO GO HALT
5365
5366 :             WIND YOUR CLOCK AND TRY AGAIN
5367
5368 016452 000704          2.6 BR     CLKRTN      ;TRY AGAIN

```

Address	OpCode	OpCode	OpCode	OpCode	Time	Instruction	Comment
5369							
5370							
5371							
5372	016454	022626			4.7	TICK: CMP (SP)+,(SP)+	;RESTORE THE STACK
5373	016456	005037	172540		3.7	CLR @172540	;TURN OFF KW11P
5374	016462	005037	177546		3.7	CLR @177546	;TURN OFF KW11L
5375							
5376							
5377							
5378							
5379	016466	013705	016442		3.8	MOV TIMEXX,R5	;RECORD 16.7 MILLISECOND INTERVAL
5380	016472	010504			2.3	MOV R5,R4	
5381							
5382							
5383							
5384							
5385							
5386							
5387							
5388							
5389	016474	022737	050000	177570	4.7	CMP #50000,SWR	;TEST LINE FREQUENCY SELECTION
5390	016502	001002			2.6	BNE CPS60	;60 CPS BRANCHES
5391	016504	000137	016614		3.7	JMP CPS50	;50 CPS JUMPS
5392							
5393							
5394	016510	006204			2.3	CPS60: ASR R4	
5395	016512	005200			2.3	INC R0	
5396	016514	020027	000005		3.2	CMP R0,#5	
5397	016520	001373			2.6	BNE CPS60	
5398							
5399							
5400							
5401	016522	010403			2.3	MOV R4,R3	
5402	016524	006203			2.3	ASR R3	
5403	016526	006203			2.3	ASR R3	
5404							
5405							
5406							
5407	016530	005002			2.3	CLR R2	
5408	016532	060402			2.3	ADD R4,R2	
5409	016534	005200			2.3	INC R0	
5410	016536	020027	000023		2.2	CMP R0,#23	
5411	016542	001373			2.6	BNE 3\$	
5412							
5413							
5414							
5415	016544	000240			1.5	NOP	
5416							
5417	016546	006202			2.3	ASR R2	/2
5418	016550	010237	011742		3.7	MOV R2,TIMEX	;RECORD 7.308 MILLISECOND INTERVAL /2
5419	016554	006303			2.3	ASL R3	;R3 = .260 MILLISECOND INTERVAL
5420	016556	060304			2.3	ADD R3,R4	;R4 = .782 MILLISECOND INTERVAL
5421	016560	006204			2.3	ASR R4	/2
5422	016562	010437	011736		3.7	MOV R4,DTIME	;DTIME.782 MILLISECOND INTERVAL /2
5423							;I.E. 10% OF 7.308
5424	016566	010204			2.3	MOV R2,R4	

```

5425 016570 163702 011736 3.8 SUB DTIME,R2
5426 016574 010237 011740 3.7 MOV R2,TIMEW ;RECORD -10% INTERVAL
5427 016600 063704 011736 3.7 ADD DTIME,R4
5428 016604 010437 011744 3.7 MOV R4,TIMEY ;RECORD +10% INTERVAL
5429 016E10 000137 011762 3.7 JMP CLKOUT ;EXIT
5430
5431 ; CALCULATE 50 CPS INTERVALS
5432
5433 CPS50: ASR R4
5434 016614 006204 3.3 ASR R4 ;RECORD
5435 016616 006204 3.3 MOV R4,R0 ;1/4 > R0 .250000
5436 016620 010400 3.3 ASR R4,R0
5437 016622 006204 3.3 MOV R4,R1 ;1/8 > R1 .125000
5438 016624 010401 3.3 ASR R4,R1
5439 016626 006204 3.3 MOV R4,R2 ;1/16 > R2 .062500
5440 016630 010402 3.3 ASR R4,R2
5441 016632 006204 3.3 ASR R4,R2
5442 016634 006204 3.3 ASR R4,R2
5443 016636 010403 3.3 MOV R4,R3 ;1/64 > R3 .015625
5444 016640 006204 3.3 ASR R4,R3 ;1/128 > R4 .0078125
5445 016642 010037 011742 3.3 MOV R0,TIMEX ;.250000
5446 016646 060137 011742 3.3 ADD R1,TIMEX ;.062500
5447 016652 160437 011742 3.3 SUB R4,TIMEX ;.3671875 OF 20 MS, IE 7.343 MS.
5448 016656 013700 011742 3.3 MOV TIMEX,R0
5449 016662 006200 3.3 ASR R0
5450 016664 006200 3.3 ASR R0
5451 016666 006200 3.3 ASR R0 ;1/8 OF 7.3M >R0
5452 016670 010001 3.3 MOV R0,R1
5453 016672 006201 3.3 ASR R1
5454 016674 006201 3.3 ASR R1
5455 016676 006201 3.3 ASR R1 ;1/64 OF 7.3M >R1
5456 016700 160100 3.3 SUB R1,R0 ;7/64'S OF 7.3 > R0
5457 016702 006201 3.3 ASR R1 ;1/128 OF 7.3M > R1
5458 016704 160100 3.3 SUB R1,R0 ;13/128'S OF 7.3M >R0
5459 ;13 X .078125 = .1015625 OF 7.3M
5460 ;I.E. .73 MILLISECONDS
5461 016706 010037 011736 3.7 MOV R0,DTIME ;RECORD
5462 016712 013737 011742 3.7 MOV TIMEX,TIMEW
5463 016720 013737 011744 3.7 MOV TIMEX,TIMEY
5464 016726 160037 011740 3.7 SUB R0,TIMEW ;-10% > TIMEW
5465 016732 060037 011744 3.7 ADD R0,TIMEY ;+10% > TIMEY
5466 016736 006237 011736 3.7 ASR DTIME ;/2
5467 016742 006237 011740 3.7 ASR TIMEW ;/2
5468 016746 006237 011744 3.7 ASR TIMEY ;/2
5469 016752 006237 011742 3.7 ASR TIMEX ;/2
5470 016756 000137 011762 3.7 JMP CLKOUT
5471
5472 ;=TABLEN
5473
5474 017142 000000 0
5475 017144 177777 177777
5476
5477 017146 000207 3.5 ENDPRO: RTS PC
5478
5479
5480

```



K09

MAINDEC-11-DZCBH-B  
DZCBHB.P11

CS11-HP LOGIC TEST  
CLOCK TIMING ONCE ONLY EXECUTION CODE

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5481 017150 177777

177777

TEST DATA CONFIGURATION TABLE

.SBTTL  
NOTE:

WHEN A SELECTED DATA PATTERN FOR TEST IS MADE (I.E. SWITCH REGISTER BIT 9 = 1), THE CONTENTS OF LOCATION "CNTL" IS MODIFIED TO THE DATA PATTERN SELECTED FOR TEST AND THE CONTENTS OF "CNTL+2" IS CLEARED. HOWEVER WHEN THE PROGRAM IS RESTARTED AT LOCATION 200 (OCTAL) THE CONTENTS OF THESE TWO LOCATIONS ("CNTL" AND "CNTL+2") ARE RESTORED TO THEIR ORIGINAL VALUES.

CNTL:	0
	177776
	177775
	177773
	177767
	177757
	177737
	177677
	177577
	177377
	176777
	175777
	173777
	167777
	157777
	137777
	077777
	1
	2
	4
	10
	20
	40
	100
	200
	400
	1000
	2000
	4000
	10000
	20000
	40000
	100000
	052525
	125252
	177777
	155555
	022222
	123456
	011111
	176543

5482		
5483		
5484		
5485		
5486		
5487		
5488		
5489		
5490		
5491		
5492		
5493	017152	000000
5494	017154	177776
5495	017156	177775
5496	017160	177773
5497	017162	177767
5498	017164	177757
5499	017166	177737
5500	017170	177677
5501	017172	177577
5502	017174	177377
5503	017176	176777
5504	017200	175777
5505	017202	173777
5506	017204	167777
5507	017206	157777
5508	017210	137777
5509	017212	077777
5510	017214	000001
5511	017216	000002
5512	017220	000004
5513	017222	000010
5514	017224	000020
5515	017226	000040
5516	017230	000100
5517	017232	000200
5518	017234	000400
5519	017236	001000
5520	017240	002000
5521	017242	004000
5522	017244	010000
5523	017246	020000
5524	017250	040000
5525	017252	100000
5526	017254	052525
5527	017256	125252
5528	017260	177777
5529	017262	155555
5530	017264	022222
5531	017266	123456
5532	017270	011111
5533	017272	176543
5534		
5535		
5536		
5537		

NOTE:

THE DATA CONFIGURATION TABLE IS POSITIONED AT THE PHYSICAL END OF THE PROGRAM TO ALLOW THE USER THE ABILITY TO EXPAND TEST DATA

# M09

MAINDEC-11-DZCBH-8  
DZCBHB.P11

CS11-HP LOGIC TEST  
TEST DATA CONFIGURATION TABLE

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```
5538  
5539  
5540  
5541  
5542  
5543  
5544  
5545  
5546  
5547  
5548  
5549  
5550  
5551  
5552 017274 000000  
5553 017276 000000  
5554 017300 177777  
5555  
5556  
000001  
END
```

TABLE ENTRIES AS REQUIRED. THE FOLLOWING LOCATIONS MAY BE ALTERED TO ANY NON ZERO ENTRY MANUALLY BY THE USER. THE NEXT ZERO ENTRY INSERTED BY THE USER WILL TERMINATE (DELIMIT) THE DATA TABLE SCAN DURING PROGRAM EXECUTION.

THE USER MUST BE AWARE HOWEVER THAT ANY INCREASE IN THE NUMBER OF DATA PERMUTATIONS (ENTRIES ADDED), WILL ALSO RESULT IN AN INCREASE IN TEST PASS EXECUTION TIMING.

ALSO BE AWARE THAT ON MINIMAL (4K) MEMORY SYSTEMS THAT ADDITIONAL PERMUTATIONS (ENTRIES ADDED) MAY OVERWRITE (DESTROY) THE "ABS" LOADER AND THE BOOTSTRAP LOADER CODE RESIDENT. THIS WILL REQUIRE RESTORATION OF THAT CODE PRIOR TO ATTEMPTING REUSE.

```
000000  
000000  
177777
```

ADDXS	001272	1019	1065*	1176										
AJTO	000042	857*												
BADB15	011534	4431	4440*											
BSS	000166	878	893*											
BEGINX	002102	1185	1187*											
BELL =	000007	801*												
BITYPS	013442	4882*												
BIT0 =	000001	811*												
BIT1 =	000002	812*												
BIT10 =	002000	821*	1241	1257										
BIT11 =	004000	822*												
BIT12 =	010000	823*	4484											
BIT13 =	020000	824*	943	1097	1673	1677	2592	2711	2720	2724	2744	2869	2988	2997
		3001	3021	3152	3271	3280	3284	3304	3435	3554	3563	3567	3587	4036
		4860	5023											
BIT14 =	040000	825*	1767	1771	2591	2710	2741	2868	2987	3018	3151	3270	3301	3434
		3553	3584											
BIT15 =	100000	826*	1865	2366	2388	2714	2723	2747	2991	3000	3024	3274	3283	3307
		3557	3566	3590	4442									
BIT2 =	000004	813*												
BIT3 =	000010	814*												
BIT4 =	000020	815*												
BIT5 =	000040	816*												
BIT6 =	000100	817*												
BIT7 =	000200	818*												
BIT8 =	000400	819*	1294	1336	1375	1410	1498	1544	1587	1626	1728	1822	1916	1995
		2074	2204	2302	2357	2378	2400	2432	2450	2467	2499	2801	3078	3361
		3644	3966											
BIT9 =	001000	820*	4099											
BUSERR	012010	848	4542*	4568	4767									
EJSL1	012014	4534	4543*											
CADCSR=	016262	929*	945*	948*	1132*	1187*	1209*	1254	1448	1668	1762	1856	2123	2253
		2335	2359	2473	2586	2709	2739	2863	2986	3016	3146	3269	3299	3429
		3552	3582	3684	4066	4146	4172	4201	4221	4286	4338	4344	4381	4426
		4448	5301*	5302										
CADDR=	016350	1066*	2659	2936	3219	3502	4245	5302*	5303					
CADTER=	016524	950*	1070*	1189*	1211*	1950	2029	2113	2243	2612	2689	2895	2966	3178
		3249	3461	3532	4118	5304*	5305							
CADTSR=	016436	949*	1068*	1188*	1210*	2108	2129	2238	2259	2760	2775	3037	3052	3320
		3335	3603	3618	4311	5303*	5304							
CBM1	000454	969	974*											
CBM2	000332	938	942*											
CBM3	001202	940	1025	1036*										
CBM4	001236	1037	1049*											
CBNV	001542	1117	1119*											
CBNY	002072	1118	1182	1184*										
CBN2	001612	1129	1132*											
CB.MMP	000320	935*	1021	1042										
CB.XXX	001474	1104	1106*	1183										
CLKOUT	011762	4518	4520*	5429	5469									
CLKRTN	016264	4519	5321*	5348	5368									
CLKRTY	016320	5327*												
CLKSCN	011750	915	1084	4517*										
CLRTSR	004362	2459*												
C_R11	003776	2269*												
CLV.CB=	016700	979*	1001*	1012*	1014*	1016*	1017*	1166*	1170*	1172*	1174*	1175*	3746	3767











LPA2	002744	1519	1548#					
LPB1	002506	1353	1378#					
LPB2	002774	1561	1590#					
LPC1	002542	1391	1415#					
LPC2	003030	1603	1631#					
_SCAN	014462	5076#	5094	5097				
LSTADR	000352	947#	1049*	1133*	5104			
LVLH10	013326	4840#						
LVLH11	013330	4841#						
LVLH12	013332	4842#						
LVLH13	013334	4843#						
LVLH14	013336	4844#						
LVLH15	013340	4845#						
LVLH16	013342	4846#						
LVLH17	013344	4847#						
LVLH20	013346	4848#						
LVLH21	013350	4849#						
LVLH22	013352	4850#						
LVLH23	013354	4851#						
LVLH24	013356	4852#						
LVLH25	013360	4853#						
LVLH26	013362	4854#						
LVLH27	013364	4855#						
LVLH30	013366	4856#						
LVLH31	013370	4857#						
LVL.H0	013306	985	1017	1165*	3771*	4832#		
LVL.H1	013310	4833#						
LVL.H2	013312	4834#						
LVL.H3	013314	4835#						
LVL.H4	013316	4836#						
LVL.H5	013320	4837#						
LVL.H6	013322	4838#						
LVL.H7	013324	4839#						
LVL7 =	000340	844#						
LXA	011220	4336#	4348					
LXB	011232	4341#	4345					
LXOUT	011264	4339	4352#					
LIS	004434	2485	2499#					
MAP.D0	014624	5109#	5136					
MAP.D1	014642	5112	5114#					
MAP.D2	014722	5113	5137#					
MAP.D3	014734	5140#						
MAP.D4	014740	5141#						
MAP.S0	014416	5064#	5083					
MAP.S1	014436	5067	5069#					
MAP.S2	014506	5068	5084#					
MAP.S3	014520	5087#						
MCRLF	015412	890	1000	4044	4639	4741	4872	5207#
MOCOR	016230	1201	5291#					
MOST	015755	5143	5252#					
MOSTB	016172	1192	5286#					
MISR	011432	4350	4416#					
MOK	012660	4702	4709	4711	4713	4716#		
MOUT	011574	4427	4456#					
MRLO	011452	4423#	4454					
MR.L	011460	4425#	4429	4438				





RA7	003456	2029#	2075					
RBC13	004640	2626	2638#					
RBC14	005352	2903	2915#					
RBC15	006064	3186	3198#					
RBC16	006576	3469	3481#					
RB10	003654	2141	2207#					
RB11	004016	2272	2305#					
RB12	004110	2344#	2358					
RB13	004600	2601	2611#					
RB14	005312	2878	2888#					
RB15	006024	3161	3171#					
RB16	006536	3444	3454#					
RB17	007372	3747	3805#					
RB3	003134	1685	1731#					
RB4	003232	1779	1825#					
RB5	003330	1873	1919#					
RB6	003422	1966	1998#					
RB7	003514	2045	2077#					
RC12	004200	2368	2381#	2401				
RDA13	004662	2650	2658#					
RDA14	005374	2927	2935#					
RDA15	006106	3210	3218#					
RDA16	006620	3493	3501#					
ROB13	004702	2662	2672#					
ROB14	005414	2939	2949#					
ROB15	006126	3222	3232#					
ROB16	006640	3505	3515#					
READIN	012540	1086	1112	1137	1153	1193	1202	4685#
READS	013634	4685	4917#					
RERR13	005216	2585#	2793	2809#				
RERR14	005730	2862#	3070	3086#				
RERR15	006442	3145#	3353	3369#				
RERR16	007154	3428#	3636	3652#				
RERR17	007764	3680#	3964	3986#				
RESET	002310	1244#						
RESTAR	001260	1060#	4581	4964				
RE13	004730	2613	2689#					
RE14	005442	2890	2966#					
RE15	006154	3173	3249#					
RE16	006666	3456	3532#					
RF13	004752	2694	2708#					
RF14	005464	2971	2985#					
RF15	006176	3254	3268#					
RF16	006710	3537	3551#					
RG13	005012	2716	2720#					
RG14	005524	2993	2997#					
RG15	006236	3276	3280#					
RG16	006750	3559	3563#					
RH13	005036	2726	2735#					
RH14	005550	3003	3012#					
RH15	006262	3286	3295#					
RH16	006774	3569	3578#					
RI13	005112	2751	2760#					
RI14	005624	3028	3037#					
RI15	006336	3311	3320#					
RI16	007050	3594	3603#					

RJ13	005132	2764	2775*											
RJ14	005544	3041	3052*											
RJ15	006356	3324	3335*											
RJ16	007070	3507	3618*											
RK13	005150	2779	2793*											
RK14	005662	3056	3070*											
RK15	006374	3339	3353*											
RK16	007106	3622	3636*											
RL13	005170	2795	2801*											
RL14	005702	3072	3078*											
RL15	006414	3355	3361*											
RL16	007126	3638	3644*											
RS0	013410	4631	4634	4865*	4867*									
RS1	011426	4310*	4316	4406*										
RS2	011430	4407*	4447*	4452										
RTA	014224	5011*												
RTB	011424	4405*												
RTF	012224	4608*												
RTF	012252	4615*												
RTH	012416	4653*												
RTI	= 000002	772*												
RTK	014366	5030	5051*											
RTNZ	007512	3883*												
RTN17	007400	3821*	3847	3910										
RT017	007650	3933	3961*											
RTT	= 000006	770*												
RTX	013372	4572	4742*	4749	4753	4858*	5354							
RT2	011604	4460*												
RX12	004050	2332*	2509											
RX13	004720	2676	2684*											
RX14	005432	2953	2961*											
RX15	006144	3236	3244*											
RX16	006656	3519	3527*											
RX5	007446	3835*	3865*	3888*										
RZ17	007776	3989	3991*											
RO	=%000000	780*	802*	930*	937	942*	943*	945	946	952	957	960	961*	968
		974	977	978*	1026	1039*	1040	1065	1066	1067	1068	1069	1070	1071
		1126*	1128	1132	1133	1251*	1425	1445*	1641	1664*	1735	1758*	1829	1852*
		1923	1946*	2002	2025*	2081	2104*	2211	2234*	2309	2331*	2511	2582*	2805
		2859*	3082	3142*	3365	3425*	3648	3679*	3981	4003*	4046*	4048	4051	4109*
		4276*	4389*	4421*	4449*	4520*	4522*	4523	4756*	4758*	4759*	4771*	4780	4799*
		4864	4867	4869	4940	4959*	5059*	5060	5064*	5066	5069	5073	5075	5078*
		5079	5082*	5086*	5087	5088	5104*	5105	5109*	5111	5114	5119	5120	5122*
		5123	5131*	5132*	5133	5139*	5140	5395*	5396	5409*	5410	5435*	5444	5447*
		5448*	5449*	5450*	5451	5455*	5457*	5460	5463	5464				
R1	=%000001	781*	803*	1002	1011*	1012	1013*	1016	1018*	1023	1036	1167	1169*	1170
		1171*	1174	1179*	1181	1184	1190	1252*	1254	1268	1420*	1421*	1446*	1448
		1468	1636*	1637*	1666*	1668	1680	1731*	1732*	1760*	1762	1774	1825*	1826*
		1854*	1856	1868	1919*	1920*	1948*	1950	1998*	1999*	2027*	2029	2077*	2078*
		2106*	2108	2113	2123	2129	2207*	2208*	2236*	2238	2243	2253	2259	2305*
		2306*	2333*	2335	2359	2364	2385	2405	2472	2473	2507*	2508*	2584*	2586
		2599	2618	2659	2689	2709	2712	2739	2748	2760	2775	2797*	2798*	2861*
		2863	2876	2895	2936	2966	2986	2989	3016	3025	3037	3052	3074*	3075*
		3144*	3146	3159	3178	3219	3249	3269	3272	3299	3308	3320	3335	3357*
		3358*	3427*	3429	3442	3461	3502	3532	3552	3555	3582	3591	3603	3618
		3640*	3641*	3682*	3684	3698	3745	3767	3771*	3772*	3873	3938	3977*	3978*

# K10

MAINDEC-11-DZCBH-B  
DZCPMB.P11

C911-49  
CROSS REFERENCE

LOGIC TEST  
TABLE

MACY11 27(732)  
-- USER SYMBOLS

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4064*	4066	4071	4079	4081	4090	4116*	4118	4131*	4132*	4144*	4146	4150
4162*	4163*	4170*	4172	4178	4187*	4188*	4195*	4200	4201	4211*	4212*	4220*
4221	4225	4245	4267*	4268*	4277*	4286	4297	4310	4311*	4313*	4316*	4317*
4318*	4319*	4320*	4331*	4338	4341	4347	4371	4376*	4378*	4379*	4381	4384
4395*	4399*	4400*	4404*	4416	4420*	4425	4426	4432	4434*	4435*	4436*	4441
4448	4459*	4521*	4523	4670*	4679*	4686	4689*	4698*	4701*	4708*	4710*	4712*
4714*	4720*	4757*	4758	4760*	4761	4772*	4782	4798*	4941	4951*	4952*	4958*
4982	4989*	4998*	5010*	5437*	5445	5451*	5452*	5453*	5454*	5455	5456*	5457
875*	892											
782*	804*	875	876	885	886	891*	1254*	1260*	1261*	1262*	1265	1300
1301*	1302*	1304	1307	1310	1340*	1342*	1344	1347	1378*	1380*	1382	1385
1415*	1416*	1448*	1453*	1454*	1456*	1457*	1459*	1460*	1462*	1463*	1466	1504
1505*	1506*	1508	1511	1514	1548*	1550*	1552	1555	1590*	1592*	1594	1597
1631*	1632*	1668*	1677*	1681	1762*	1771*	1775	1856*	1865*	1869	1950*	1959*
1962	2029*	2038*	2041	2108*	2113*	2115*	2116	2123*	2124*	2126*	2129*	2137
2238*	2243*	2245*	2246	2253*	2254*	2256*	2259*	2267	2269	2335*	2338*	2339
2340*	2341*	2344*	2345	2359*	2361*	2365	2382*	2389	2404*	2411	2438*	2440
2455	2473*	2474	2586*	2589*	2590*	2597*	2598	2611*	2618*	2620*	2624	2645*
2647*	2648	2659*	2660	2673*	2674*	2675	2689*	2691*	2692	2709*	2713	2720*
2722	2739*	2749	2760*	2761	2775*	2777	2863*	2866*	2867*	2874*	2875	2888*
2895*	2897*	2901	2922*	2924*	2925	2936*	2937	2950*	2951*	2952	2966*	2968*
2969	2986*	2990	2997*	2999	3016*	3026	3037*	3038	3052*	3054	3146*	3149*
3150*	3157*	3158	3171*	3178*	3180*	3184	3205*	3207*	3208	3219*	3220	3233*
3234*	3235	3249*	3251*	3252	3269*	3273	3280*	3282	3299*	3309	3320*	3321
3335*	3337	3429*	3432*	3433*	3440*	3441	3454*	3461*	3463*	3467	3488*	3490*
3491	3502*	3503	3516*	3517*	3518	3532*	3534*	3535	3552*	3556	3563*	3565
3582*	3592	3603*	3604	3618*	3620	3684*	3697*	3711*	3712*	3714*	3835	3871*
3872*	3888	3928*	3929*	3963	3969*	3970	3971*	4066*	4070*	4073	4079*	4083*
4086*	4089*	4090*	4118*	4121*	4124*	4126	4146*	4152*	4154	4172*	4175*	4180
4201*	4203	4221*	4224*	4226	4236*	4237*	4238	4245*	4247	4253*	4255*	4256
4261	4286*	4288*	4289	4296*	4297*	4299	4332*	4337*	4341	4343	4344	4372
4381*	4385	4393*	4395	4397*	4399	4400	4403*	4417	4426*	4428	4433*	4434
4435	4436	4447	4448*	4452*	4458*	4562*	4563	4687	4690*	4691*	4692	4694
4696	4699	4701	4703	4719*	4773*	4784	4797*	4942	4957*	4984	4991*	5009*
5407*	5408*	5417*	5418	5424	5425*	5426	5439*					
880	882	891*										
783*	805*	945*	948*	949*	950*	952*	954*	965	979*	985	995*	999*
1001*	1012*	1014*	1016*	1017*	1020*	1021*	1022*	1066*	1068*	1070*	1105*	1132*
1148*	1165*	1166*	1170*	1172*	1174*	1175*	1177*	1178*	1180*	1187*	1188*	1189*
1266*	1270	1310*	1313	1347*	1351	1385*	1389	1450*	1453	1454	1459	1460
1462	1463	1466*	1470	1514*	1517	1555*	1559	1597*	1601	1621*	1684	1775*
1778	1869*	1872	1962*	1965	2041*	2044	2116*	2117	2137*	2140	2246*	2247
2267*	2269*	2271	2345*	2346	2365*	2366*	2367	2389*	2390	2411*	2412	2425
2440*	2441	2455*	2456	2474*	2475	2484	2598*	2600	2624*	2625	2648*	2649
2660*	2661	2675*	2692*	2693	2713*	2714*	2715	2722*	2723*	2725	2749*	2750
2761*	2763	2777*	2778	2875*	2877	2901*	2902	2925*	2926	2937*	2938	2952*
2969*	2970	2990*	2991*	2992	2999*	3000*	3002	3026*	3027	3038*	3040	3054*
3055	3158*	3160	3184*	3185	3208*	3209	3220*	3221	3235*	3252*	3253	3273*
3274*	3275	3282*	3283*	3285	3309*	3310	3321*	3323	3337*	3338	3441*	3443
3467*	3468	3491*	3492	3503*	3504	3518*	3535*	3536	3556*	3557*	3559	3565*
3566*	3568	3592*	3593	3604*	3606	3620*	3621	3681*	3702*	3703	3704	3746
3748*	3749	3770*	3771	3772	3773*	3821*	3822*	3823	3824	3882*	3883	3909*
3940*	3941*	4073*	4074	4126*	4127	4154*	4155*	4156	4180*	4181*	4182	4203*
4205*	4206	4226*	4227*	4228	4238*	4239	4247*	4248	4256*	4261*	4262	4289*
4290	4299*	4302	4333*	4336	4337	4373	4385*	4386*	4387	4402*	4418	4428*
4440	4457*	4543*	4544*	4688	4703*	4705*	4706	4714	4718*	4774*	4786	4796*

R1S 000114  
R2 =:000002

R2S 000160  
R3 =:000003











SITYPE	10	8270						
BLKBLK	10							
BUFHOR	10							
DUMP	10	8270	4645					
DUMP18	10							
FILBLK	10							
LNKBLK	10							
OOT11	10							
OOT11X	10							
POP	10	7250	8270	4718	4954			
PRINT	10	8270						
PUSH	10	7250	8270	4686	4940			
SCOPE.	10							
SCOP.	10							
SOUND	10	8270						
TRACE	10							
TRMBLK	10							
TYPEN	10							
WRITE	10							
SCATCH	10							
SCHTAG	10							
SDATAI	12220	2315						
SEID	10	7250						
SEQUAT	10	7250	795					
SHIT	10	7250	4619					
SINIT	12220	1223	1431					
SINTR	12220	2536	2813	3090	3373			
SIOCAT	7250							
SLOT	7250	4971						
SKPAT	10							
SLQADR	10							
SOCAL	10	7250	4875					
SOCUER	10	46820	4938					
SPRIOT	12220	3656						
SRAND	10							
SRAND4	10							
SREAD	10	7250	4917					
SSCOPE	10	7250	4583					
SSETUP	10							
SSPAT	10							
SSYREG	12220	1647	1741	1835	1929	2008	2087	2217
SSWOC	10	7250						
STRAP	10							
STYPE	10	7250	50140	5015				
SURAT	10							
.SCOP	10							
.SCOPE	10							

RDC	1302	1342	1380	1416	1506	1550	1592	1632									
RDD	891	1039	1049	2341	2438	2770	3909	3918	4022	4288	4297	4393	4397	4422	4666		
RSL	4677	4760	5029	5044	5047	5082	5096	5132	5139	5408	5420	5427	5445	5454			
RSR	987	988	989	1022	1105	1180	1252	1446	1666	1760	1854	1948	2027	2106	2236		
	2233	2584	2861	3144	3427	3622	4064	4144	4170	4195	4220	4277	4313	4363	4379		
	4679	4708	4710	4712	4998	5419											
	1020	1162	1163	1164	1177	1420	1636	1731	1825	1919	1998	2077	2207	2305	2507		
	797	3074	3357	3640	3977	4131	4162	4187	4211	4267	4319	4670	5394	5402	5403		
	417	421	5433	5434	5436	5438	5440	5441	5443	5448	5449	5450	5452	5453	5454		
	5456	5455	5466	5467	5468												
	938	1129	5067	5112	5468												
	4709	4711	4713	5112													
	969	969	975	981	1003	1062	1076	1078	1168	1182	1195	1197	1206	1242	1255		
	1315	1315	1353	1391	1449	1472	1519	1561	1603	1669	1585	1763	1779	1857	1873		
	1966	1966	2030	2045	2109	2118	2141	2239	2248	2272	2347	2368	2387	2391	2413		
	2442	2442	2451	2457	2468	2476	2500	2504	2601	2626	2650	2662	2676	2694	2716		
	2743	2743	2746	2751	2764	2779	2802	2878	2903	2927	2939	2953	2971	2993	3003		
	3020	3023	3028	3041	3056	3079	3161	3186	3210	3222	3236	3254	3276	3286	3303		
	3306	3311	3324	3339	3362	3444	3469	3493	3505	3519	3537	3559	3569	3586	3589		
	3594	3607	3622	3645	3750	3765	3922	3965	3967	3989	4030	4047	4049	4067	4075		
	4082	4086	4100	4120	4126	4147	4158	4173	4183	4202	4207	4222	4229	4240	4249		
	4257	4253	4287	4292	4303	4339	4342	4388	4427	4481	4483	4485	4592	4594	4597		
	4601	4613	4632	4693	4695	4697	4704	4861	4866	4902	4905	4920	5024	5028	5038		
	5085	5090	5095	5124	5138	5142	5147										
	882	1028	1041	1122	1144	1146	1157	4762	5081	5135							
	914	954	986	1011	1169	1217	2126	2256	2366	2409	2714	2720	2723	2724	2991		
	2997	3000	3071	3274	3280	3283	3284	3557	3563	3566	3567	3822	3871	3874	3928		
	3939	3941	4155	4175	4181	4205	4227	4378	4386	4442	4480	4671	4691	5026	5048		
	4924																
	543	1012	1013	1014	1016	1081	1107	1170	1171	1172	1174	1680	1774	1868	2124		
	2254	2364	2385	2388	2405	2472	2592	2599	2711	2712	2744	2747	2748	2859	2876		
	2988	2989	3021	3024	3025	3152	3159	3271	3272	3304	3307	3308	3435	3442	3554		
	3555	3587	3590	3591	3872	3929	4071	4150	4152	4178	4200	4225	4384	4395	4399		
	4400	4434	4435	4436	4441	4714	4962										
	1017	1175	4906														
	958	1002	1097	1119	1140	1167	1204	1241	1257	1294	1336	1375	1410	1498	1544		
	1587	1626	1728	1822	1916	1995	2074	2204	2302	2357	2378	2400	2432	2450	2467		
	2499	2801	3078	3361	3644	3824	3921	3966	4036	4081	4099	4484	4591	4598	4629		
	4706	4860	4893	5023	5033												
	1125	1159															
	880	3747															
	4979																
	4431	4673															
	894	906	1024	1037	1090	1098	1117	1120	1139	1142	1155	1185	1191	1199	1258		
	1295	1337	1376	1411	1426	1499	1545	1588	1627	1642	1729	1736	1823	1830	1917		
	1924	1996	2003	2075	2082	2205	2212	2303	2310	2336	2358	2379	2401	2408	2517		
	2587	2612	2795	2806	2364	2889	3072	3083	3147	3172	3355	3366	3430	3455	3638		
	3649	3685	3768	3825	3885	3982	4015	4027	4037	4097	4282	4345	4494	4496	4518		
	4524	4559	4603	4630	4700	4707	4894	4908	4910	4926	4932	4953	5034	5046	5070		
	5072	5115	5118	5341	5361	5390	5397	5411									
	2426	2485	4429	4651	4922	5041											
	892	957	1004	1015	1104	1109	1131	1134	1149	1173	1208	1212	1733	1827	1921		
	2000	2079	2209	2307	3751	3847	3910	3925	3933	4017	4084	4133	4164	4189	4213		
	4269	4284	4321	4348	4364	4422	4438	4454	4487	4534	4678	4702	4715	4745	4833		
	4885	4891	4928	4967	5030	5042	5083	5128	5136	5334	5338	5348	5368				
	909	929	948	949	950	961	978	979	995	999	1052	1080	1091	1092	1093		

# E11

	1106	1187	1188	1189	1209	1210	1211	1213	1215	1216	1218	1260	1261	1262	1301
	1340	1349	1378	1387	1415	1451	1505	1548	1557	1590	1599	1621	2238	2340	2381
	2382	2454	2589	2590	2672	2674	2776	2866	2867	2949	2951	3053	3149	3150	3232
	3236	3432	3433	3515	3517	3619	3697	3882	3882	3969	3971	4020	4107	4116	4254
	4234	4217	4216	4331	4332	4334	4420	4522	4522	4561	4698	4735	4736	4739	4751
	4755	4764	4771	4772	4773	4774	4775	4776	4886	4951	5061	5053	5078	5106	5108
	5122	5131	5327	5328	5357	5373	5374	5407							
	4654	4890	4892	4912	4923										
	4716														
	876	974	1023	1026	1040	1077	1115	1121	1123	1143	1145	1181	1190	1196	1198
	1270	1313	1470	1517	1684	1778	1872	1965	2044	2117	2140	2247	2271	2346	2367
	2390	2412	2441	2456	2475	2600	2625	2649	2661	2693	2715	2725	2750	2763	2778
	2877	2902	2926	2928	2938	2970	2992	3002	3027	3040	3055	3070	3160	3185	3209
	3223	3275	3285	3310	3323	3338	3353	3443	3443	3468	3492	3504	3535	3558	3568
	3593	3606	3621	3636	3869	3958	3961	3964	4048	4074	4127	4156	4182	4206	4228
	4239	4248	4262	4290	4302	4341	4387	4482	4523	4631	4747	4748	4761	4864	4909
	4919	4978	5027	5045	5079	5094	5114	5133	5146	5335	5339	5352	5372	5389	5396
	5410														
	879	881	1088	1156	1158	1425	1641	1735	1829	1923	2002	2081	2211	2309	2511
	2805	3082	3365	3648	3746	3981	4028	4593	4602	4692	4694	4696	4699	4925	4931
	5069														
	927														
	4430	4492	4495												
	4672														
	796														
	895	972	1045	3784	3827	4104	4113	4453	4652	4948	4966	5006	5126	5347	5364
	1018	1021	1178	1179	1421	1637	1732	1826	1920	1999	2078	2208	2306	2508	2798
	3075	3358	3641	3978	4035	4132	4163	4188	4212	4268	4320	4628	4669	4952	5077
	5130	5340	5359	5395	5409										
	4605	4610	4903	4907											
	900	940	1008	1025	1031	1042	1047	1054	1063	1079	1118	1183	1186	1423	1428
	1639	1644	1737	1831	1925	2004	2083	2213	2311	2337	2435	2452	2469	2491	2501
	2505	2509	2518	2588	2613	2685	2799	2803	2807	2865	2890	2962	3076	3080	3084
	3148	3173	3245	3359	3363	3367	3431	3456	3528	3642	3646	3650	3686	3774	3794
	3958	3979	3984	4056	4519	4655	4964	5068	5113	5391	5429	5469			
	874	889	915	916	923	924	958	966	982	983	984	991	994	998	1019
	1050	1084	1086	1095	1099	1100	1112	1137	1153	1176	1193	1202	1220	1249	1308
	1399	1444	1512	1611	1663	1757	1851	1945	2024	2103	2125	2127	2233	2255	2257
	2329	2363	2384	2581	2614	2658	2684	2708	2735	2858	2891	2935	2961	2985	3012
	3141	3174	3218	3244	3268	3295	3424	3457	3501	3527	3551	3578	3678	3713	3715
	4004	4012	4016	4019	4021	4040	4043	4051	4063	4122	4142	4166	4167	4191	4193
	4219	4244	4260	4275	4627	4633	4646	4648	4649	4663	4667	4668	4676	4685	4870
	5058	5093	5098	5103	5145	5150	5325								
	875	885	886	888	903	907	912	930	942	945	946	952	957	960	965
	977	985	993	997	1001	1066	1068	1070	1073	1074	1126	1132	1133	1148	1166
	1214	1219	1246	1247	1251	1254	1266	1268	1310	1311	1347	1385	1445	1448	1450
	1466	1468	1514	1515	1555	1597	1664	1668	1673	1677	1681	1758	1762	1767	1771
	1775	1852	1856	1861	1865	1869	1946	1950	1955	1959	1962	2025	2029	2034	2038
	2041	2104	2108	2113	2114	2115	2116	2123	2129	2133	2137	2234	2238	2243	2244
	2245	2246	2253	2259	2263	2267	2269	2331	2332	2335	2342	2344	2345	2359	2360
	2361	2365	2389	2403	2404	2411	2437	2440	2455	2471	2473	2474	2582	2585	2586
	2591	2597	2598	2611	2618	2619	2620	2624	2645	2646	2647	2648	2659	2660	2673
	2675	2689	2690	2691	2692	2709	2710	2713	2722	2739	2741	2749	2760	2761	2762
	2775	2777	2859	2862	2863	2868	2874	2875	2888	2895	2896	2897	2901	2922	2923
	2924	2925	2936	2937	2950	2952	2966	2967	2968	2969	2986	2987	2990	2999	3016
	3018	3026	3037	3038	3039	3052	3054	3142	3145	3146	3151	3157	3158	3171	3178

	3179	3180	3184	3205	3206	3207	3208	3219	3220	3233	3235	3249	3250	3251	3252
	3269	3270	3273	3282	3299	3301	3309	3320	3321	3322	3335	3337	3425	3428	3429
	3434	3440	3441	3454	3461	3462	3463	3467	3488	3489	3490	3491	3502	3502	3516
	3518	3532	3533	3534	3535	3552	3553	3556	3555	3582	3584	3592	3603	3604	3605
	3618	3620	3679	3680	3681	3684	3698	3699	3700	3701	3702	3703	3704	3711	3712
	3714	3749	3771	3805	3823	3834	3835	3846	3868	3870	3875	3892	3888	3908	3920
	3926	3937	3940	3962	3972	3973	3975	4003	4005	4007	4009	4024	4025	4039	4042
	4046	4066	4069	4070	4073	4079	4083	4086	4089	4093	4094	4105	4106	4109	4115
	4118	4121	4123	4124	4126	4146	4149	4154	4172	4176	4180	4196	4197	4199	4200
	4203	4221	4223	4224	4226	4233	4234	4235	4236	4237	4238	4245	4246	4247	4253
	4255	4256	4261	4276	4279	4280	4283	4286	4289	4296	4299	4300	4301	4310	4311
	4316	4327	4350	4362	4367	4371	4372	4373	4374	4376	4381	4383	4385	4389	4401
	4402	4403	4404	4416	4417	4418	4419	4421	4423	4426	4428	4440	4447	4448	4449
	4452	4453	4457	4458	4459	4463	4476	4478	4479	4486	4488	4489	4491	4498	4499
	4520	4521	4543	4562	4563	4567	4569	4571	4572	4577	4578	4606	4607	4611	4614
	4624	4642	4645	4662	4665	4675	4686	4687	4688	4689	4690	4717	4718	4719	4720
	4721	4737	4738	4740	4742	4749	4750	4752	4753	4754	4756	4757	4758	4759	4766
	4767	4768	4780	4782	4784	4786	4788	4790	4794	4795	4796	4797	4798	4799	4867
	4869	4882	4888	4889	4914	4917	4918	4935	4938	4939	4940	4941	4942	4943	4944
	4945	4946	4947	4950	4954	4955	4956	4957	4958	4959	4960	4961	4977	4981	4982
	4984	4986	4989	4991	5008	5009	5010	5031	5032	5035	5036	5043	5049	5050	5059
	5060	5073	5075	5087	5088	5091	5097	5104	5105	5109	5119	5120	5140	5144	5149
	5221	5322	5323	5324	5332	5333	5336	5337	5353	5354	5355	5356	5379	5380	5401
	5418	5422	5424	5426	5428	5435	5437	5439	5442	5444	5447	5451	5460	5461	5462
MOV8	1455	1453	1454	1455	1457	1459	1460	1462	1463	3772	3873	3938	4090	4432	4604
	4644	4701	4703	4884	4887	4911	4923	4929	5039	5064					
NOP	1263	2580	2857	3140	3423	3884	4052	4053	4054	5415					
RESET	1244	4050													
ROL	4895	4897	4899												
ROLB	4896	4898	4900												
RTI	4405	4460	4557	4582	4608	4615	4653	4858	5011	5051					
RTS	898	1072	3990	4135	4215	4270	4322	4352	4500	4525	4573	4579	4680	4722	4778
	4792	4800	4862	4873	4915	4936	5099	5151	5477						
RTT	4741														
SEC	935	1127	5065	5110											
SUB	3748	3773	3921	3923	4544	4643	4705	4988	5425	5446	5455	5457	5463		
SWAB	990	1160													
TRAP	795														
TST	893	905	937	980	1036	1060	1065	1067	1069	1071	1075	1128	1184	1300	1304
	1307	1344	1351	1382	1389	1504	1508	1511	1552	1559	1594	1601	2339	2386	2407
	2425	2484	2502	2503	2742	2745	3019	3022	3302	3305	3585	3588	3764	3963	3970
	3974	3988	4014	4087	4096	4119	4281	4336	4338	4343	4344	4347	4425	4517	4596
	4612	4650	4990	5066	5071	5084	5089	5111	5116	5123	5137	5141			
TSTB	3767	4600	4901	4904	4921	5037	5040								
WAIT	3830														
.RES	725														
.ASCIZ	5159	5164	5175	5178	5181	5182	5184	5190	5193	5198	5204	5207	5208	5210	5213
	5224	5235	5238	5241	5244	5249	5252	5257	5258	5266	5271	5276	5279	5282	5286
	5291														
.BLKW	4916	4937													
.DSABL	4527	5479													
.ENABL	1	725	4358	5320											
.END	5556														
.ENDC	827	1431	1647	1672	1678	1725	1766	1772	1819	1860	1866	1913	1954	1960	1992
	2033	2039	2071	2132	2135	2167	2201	2262	2265	2299	2561	2573	2838	2850	3115
	3133	3398	3416	4595	4616	4629	4631	4649	4656	4876	4892	4917	4920	4938	4946

# G11

	4954	4964	4965	5037	5052													
.EVEN	5053	5297																
.IF	811	1231	1439	1672	1675	1680	1725	1766	1769	1774	1819	1860	1863	1868	1913			
	1954	1957	1962	1992	2033	2036	2041	2071	2112	2135	2137	2167	2242	2265	2267			
	2299	2556	2564	2833	2841	3110	3118	3393	3401	4591	4616	4627	4629	4648	4653			
	4876	4892	4917	4919	4937	4946	4954	4963	4964	5033	5043							
.IFF	1231	1237	1256	1289	1332	1371	1407	1439	1444	1450	1489	1536	1579	1619	1675			
	1689	1698	1769	1783	1792	1863	1877	1886	1957	1970	1976	2036	2049	2055	2135			
	2145	2151	2265	2276	2282	2560	2566	2570	2572	2573	2833	2843	2847	2849	2850			
	3114	3118	3126	3128	3131	3393	3401	3409	3411	3414	4595	4627	4653	4876	4920			
	4938	4964	5052															
.IFT	1237	1251	1265	1290	1333	1372	1408	1439	1444	1450	1489	1536	1579	1619	1672			
	1680	1694	1698	1721	1725	1766	1774	1788	1792	1815	1819	1860	1868	1882	1986			
	1909	1913	1954	1962	1976	1979	1992	2033	2041	2055	2058	2071	2112	2137	2151			
	2154	2167	2242	2267	2282	2285	2299	2556	2564	2570	2641	2833	2841	2847	2918			
	3110	3118	3128	3201	3393	3401	3411	3484										
.IFTF	1251	1265	1290	1333	1372	1408	1445	1465	1494	1541	1584	1624	1681	1689	1708			
	1725	1775	1783	1802	1819	1869	1877	1896	1913	1962	1971	1979	1992	2041	2050			
	2058	2071	2137	2146	2154	2167	2201	2267	2277	2285	2299	2560	2566	2572	2581			
	2837	2843	2849	2858	3114	3122	3130	3141	3397	3405	3413	3424						
.IIF	1677	1683	1696	1697	1696	1719	1720	1771	1777	1790	1791	1792	1813	1814	1865			
	1871	1884	1885	1907	1908	1959	1964	1976	1977	1978	1990	1991	2038	2043	2055			
	2056	2057	2069	2070	2139	2151	2152	2165	2166	2269	2282	2283	2296	2297	2562			
	2563	2574	2575	2576	2578	2839	2840	2851	2853	2854	3116	3117	3134	3135	3136			
	3138	3399	3400	3417	3419	3420	4608	4612	4617	4618	4657	4659	4937					
.IRP	4686	4718	4940	4954														
.LIST	1	725	827	902	1008	1033	1057	1222	1223	1431	4358	4527	4583	4619	4682			
	4860	4876	4917	4938	5015	5157	5320	5479										
.MACRO	1	725	1222															
.MCALL	725	827	4682	5014														
.NLIST	1	725	827	902	1008	1033	1057	1222	1223	1431	4358	4527	4583	4619	4682			
	4860	4876	4917	4938	5015	5157	5320	5479										
.PAGE	768	862	902	1008	1057	1224	1432	1648	1742	1836	1930	2009	2088	2167	2218			
	2315	2537	2580	2814	2857	3091	3140	3374	3423	3656	3801	3995	4138	4219	4272			
	4323	4357	4410	4463	4619	4682	4860	4876	4917	4938	4971	5055	5101	5155	5157			
	5313	5482																
.REM	1	727																
.REPT	725																	
.SBTTL	726	768	863	902	1008	1057	1224	1432	1648	1742	1836	1930	2009	2088	2218			
	2315	2537	2814	3091	3374	3657	3997	4060	4139	4218	4273	4323	4359	4410	4463			
	4514	4527	4559	4575	4583	4619	4682	4728	4860	4876	4917	4938	5015	5056	5101			
	5157	5313	5482															
.TITLE	724																	
.WORD	1087	1113	1138	1154	1194	1203												

ERRORS DETECTED: 0  
 DEFAULT GLOBALS GENERATED: 0

\* DZCBHB.SEG/SOL/CRF/PAGNUM/NL: TOC=SYSMAC.CBH, DZCBHB.P11  
 RUN-TIME: 31 49 7 SECONDS  
 RUN-TIME RATIO: 171/89=1.9  
 CORE USED: 31K (61 PAGES)

