

# PDP11

1080 MEMORY TIMING TEST  
MD-11-DBKMA-A

EP-DBKMA-A-DL-A  
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- Technical diagrams and flowcharts.
- Tables of data, possibly test results or timing parameters.
- Textual descriptions and labels.
- Small graphs or plots.

The text and diagrams are very small and difficult to read due to the resolution of the scan. Some legible text includes "1080 MEMORY TIMING TEST" and "MD-11-DBKMA-A".

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IDENTIFICATION

PRODUCT CODE: MAINDEC-1080-BNTT  
 PRODUCT NAME: DECSYSTEM-1080 BASIC MEMORY TIMING  
 TEST  
 DATE RELEASED: JUNE 20, 1975  
 MAINTAINED BY: DIAGNOSTIC ENGINEERING  
 AUTHOR: JAMES KELLY

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2015-10-16 16:22:22.111 BNTT MACY11 27(732) 14-OCT-76 16:22 PAGE 2 DIBOR.P11

XX

TABLE OF CONTENTS

1.0	ABSTRACTS
2.0	REQUIREMENTS
2.1	EQUIPMENT
2.2	STORAGE
2.3	PRELIMINARY PROGRAMS
3.0	PROGRAM PROCEDURES
3.1	LOADING PROCEDURES
3.2	STARTING PROCEDURES
4.0	ERRORS
4.1	ERROR PC RANGE
5.0	CYCLE TIME
6.0	PROGRAM DESCRIPTION
7.0	LISTING



3.0 PROGRAM PROCEDURES

3.1 LOADING PROCEDURES

1. MOUNT THE DECTAPE CONTAINING THE BMTT DIAGNOSTIC TEST ONTO A WORKING DECTAPE DRIVE.
2. SET THE WRITE LOCK SWITCH TO WRITE LOCK.
3. SET THE DRIVES SELECT TO UNIT #0.
4. SET THE MODE SWITCH TO ONLINE.
5. SET 177072 INTO THE PDP-11/40 SWITCH REGISTER.
6. DEPRESS THE HALT SWITCH ON THE PDP-11/40.
7. DEPRESS THE START KEY ON THE PDP-11/40 SEVERAL TIMES. THIS INITIALIZES THE CPU.
8. SET THE HALT KEY TO THE RUN POSITION (UP).
9. DEPRESS THE START KEY AND RELEASE ONE TIME.
10. THE SELECTED DECTAPE DRIVE WILL BEGIN TO TURN.
11. THE CONSOLE WILL TYPE THE MONITOR'S NAME FOLLOWED BY A "#".
12. TYPE DEKMA.BIN <CR>.

3.2 STARTING PROCEDURES

TO START THE BMTT PROGRAM PROCEED AS FOLLOWS:

1. SET THE PDP-11/40 ADDRESS TO 1000.
2. DEPRESS AND RELEASE THE START KEY.
3. THE PROCESSOR WILL RUN FOR LESS THAN A SECOND AND HALT WITH ADDRESS 1514 DISPLAYED IN THE ADDRESS REGISTER.
4. IF THE PROCESSOR HALTS AT ANY ADDRESS OTHER THAN THE ABOVE, IT IS AN ERROR. REFER TO THE LISTING FOR A DETAILED DESCRIPTION OF THE SYNTON.

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**4.0 ERRORS**

ANY HALT OTHER THAN WITH 1514 DISPLAYED IS AN ERROR AND WILL HAVE TO BE REPAIRED BEFORE ATTEMPTING ANY FURTHER TESTING. TO TROUBLE SHOOT AN ERROR USING BMTT THE ERROR HALT SHOULD BE REPLACED WITH A "NOP" 240. THE PROGRAM CAN THEN BE RESTARTED AT THE BEGINNING OF THE FAILING SUBTEST.

**4.1 ERROR PC RANGE**

ADDRESS(ES) 1000 THRU 1516 INCLUSIVE ARE LEGAL ERROR HALTS WITH THE SINGLE EXCEPTION OF ADDRESS 1512 DISPLAYED AS 1514.

**5.0 CYCLE TIME**

THE SPEED OF EXECUTION IS PRACTICALLY INSTANTLY.

**6.0 PROGRAM DESCRIPTION**

BMTT CONSISTS OF FIVE BASIC TESTS. THE FIRST FOUR ARE A CURSORY CHECK OF THE KILL-L REAL TIME CLOCK, THE FIFTH BEING THE ACTUAL TIMING TEST. THE FIRST FOUR TESTS DETERMINE THAT THE CLOCK EXISTS, THAT IT WILL SET ITS MONITOR BIT, CAUSE INTERRUPTS AND THAT IT CAN BE LOCKED OUT BY CLEARING THE INTERRUPT ENABLE BIT. THE FINAL TEST WAITS FOR THE CLOCK TO SET ITS MONITOR BIT THUS GIVING US A COMPLETE CYCLE FOR ONE TEST, THEN STARTING A SIMPLE TIME OUT LOOP. WHEN THE KILL-L CAUSES AN INTERRUPT THE NUMBER OF ITERATIONS IN THE TIMEOUT LOOP ARE COMPARED TO A PREVIOUSLY CALCULATED NORMAL RANGE TO DETERMINE THAT THE MACHINE SPEED IS NORMAL.

BASIC MEMORY TIMING TESTS FLOWS

DECALO VER 00.0

DBM000.P11

FLOW CHART  
\*\*\*\*\*  
BASIC MEMORY TIMING TESTS FLOWS  
\*\*\*\*\*

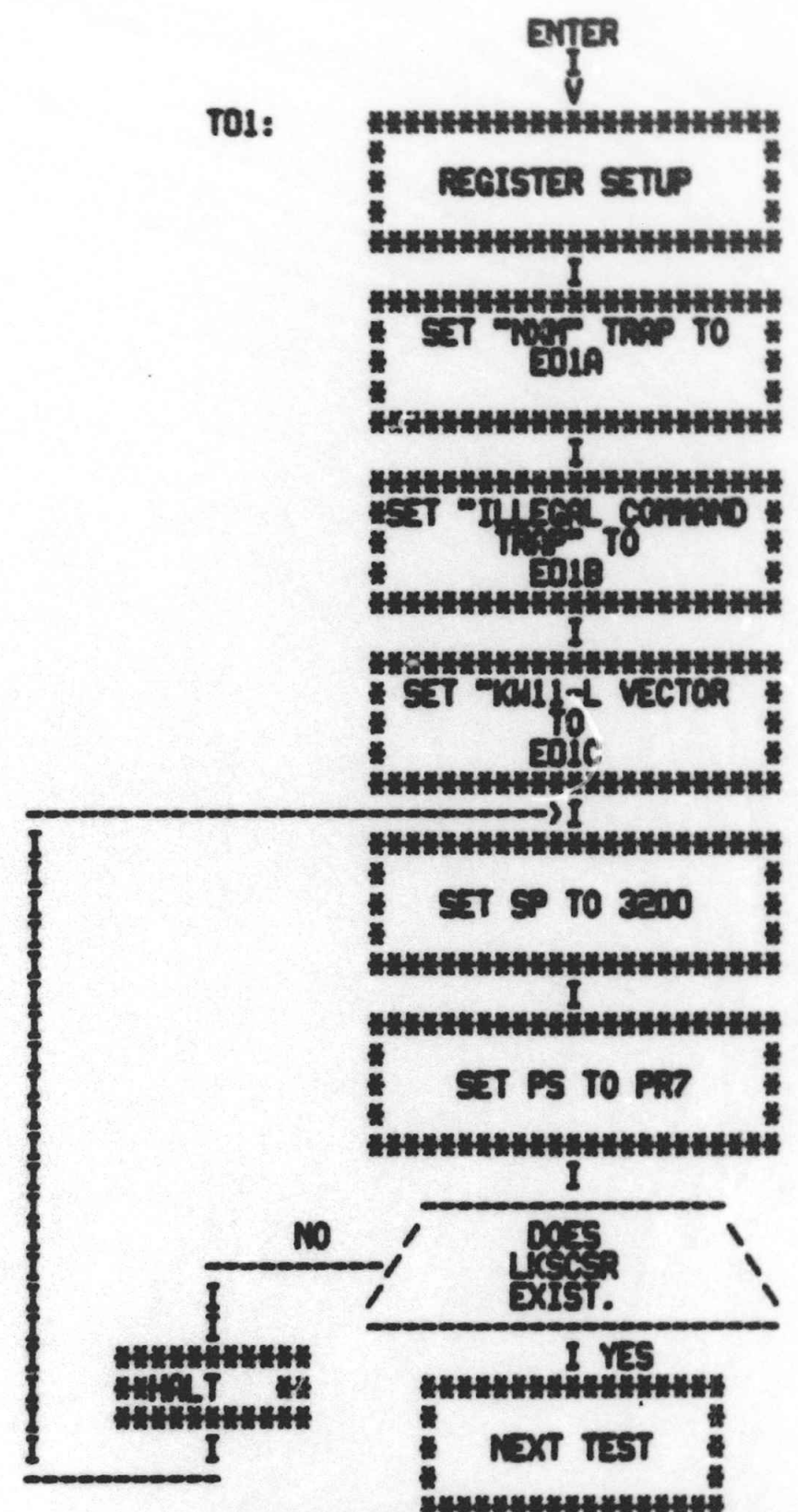
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BASIC MEMORY TIMING TESTS FLOWS

DECFL0 VER 00.0

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T01:



T01 DETERMINES IF THE K11-L REAL TIME CSR REGIST CAUSING A TIME OUT.  
NOTE

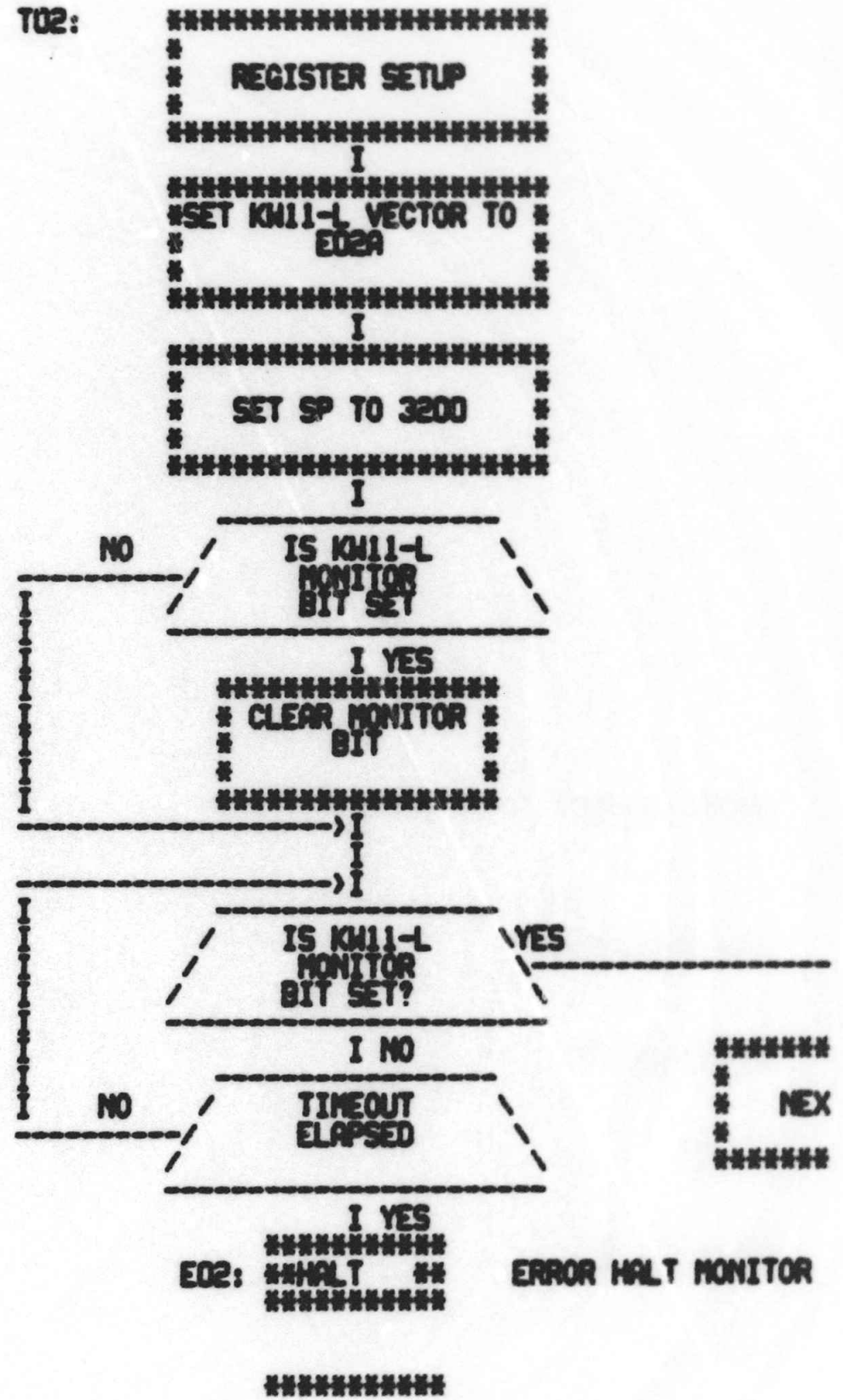


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THE RESERVED INSTRUCTION AND NON-EXISTANT MEMORY  
SHOWN IN THIS TEST, SHOULD ANY TEST IN THIS DIAGN  
HALT WILL BE ON THIS PAGE IT WILL BE NECESSARY TO  
STACK TO DETERMINE WHERE THE TRAPPED WAS CAUSED.

BASIC MEMORY TIMING TESTS FLOWS

DEC FLO VER 00.0



K01

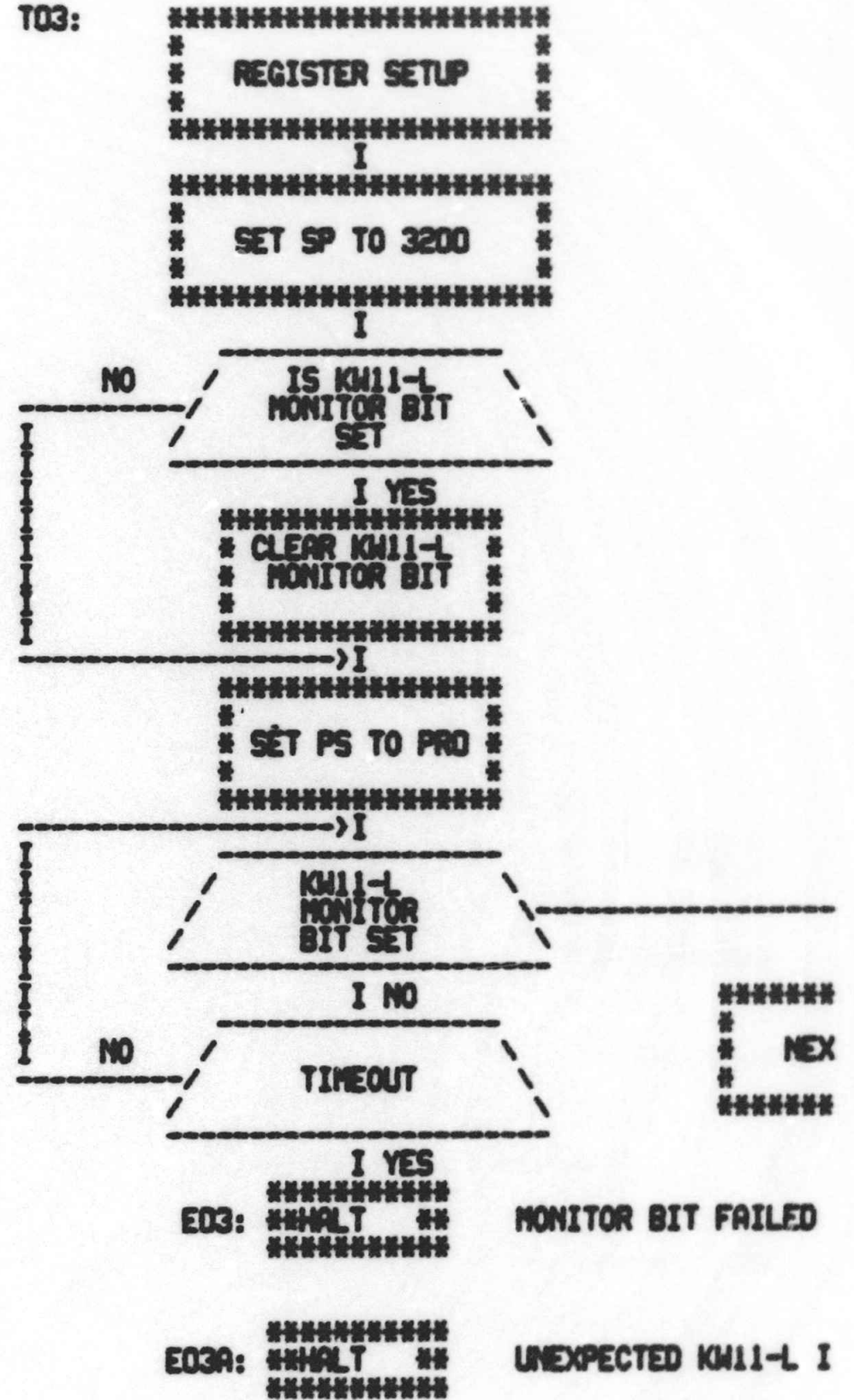
BMTT MACY11 27(732) 14-OCT-76 16:22 PAGE 11  
DBKMAR.P11

ED2A: ##HALT ## UNEXPECTED KW11-L I  
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BASIC MEMORY TIMING TESTS FLOWS

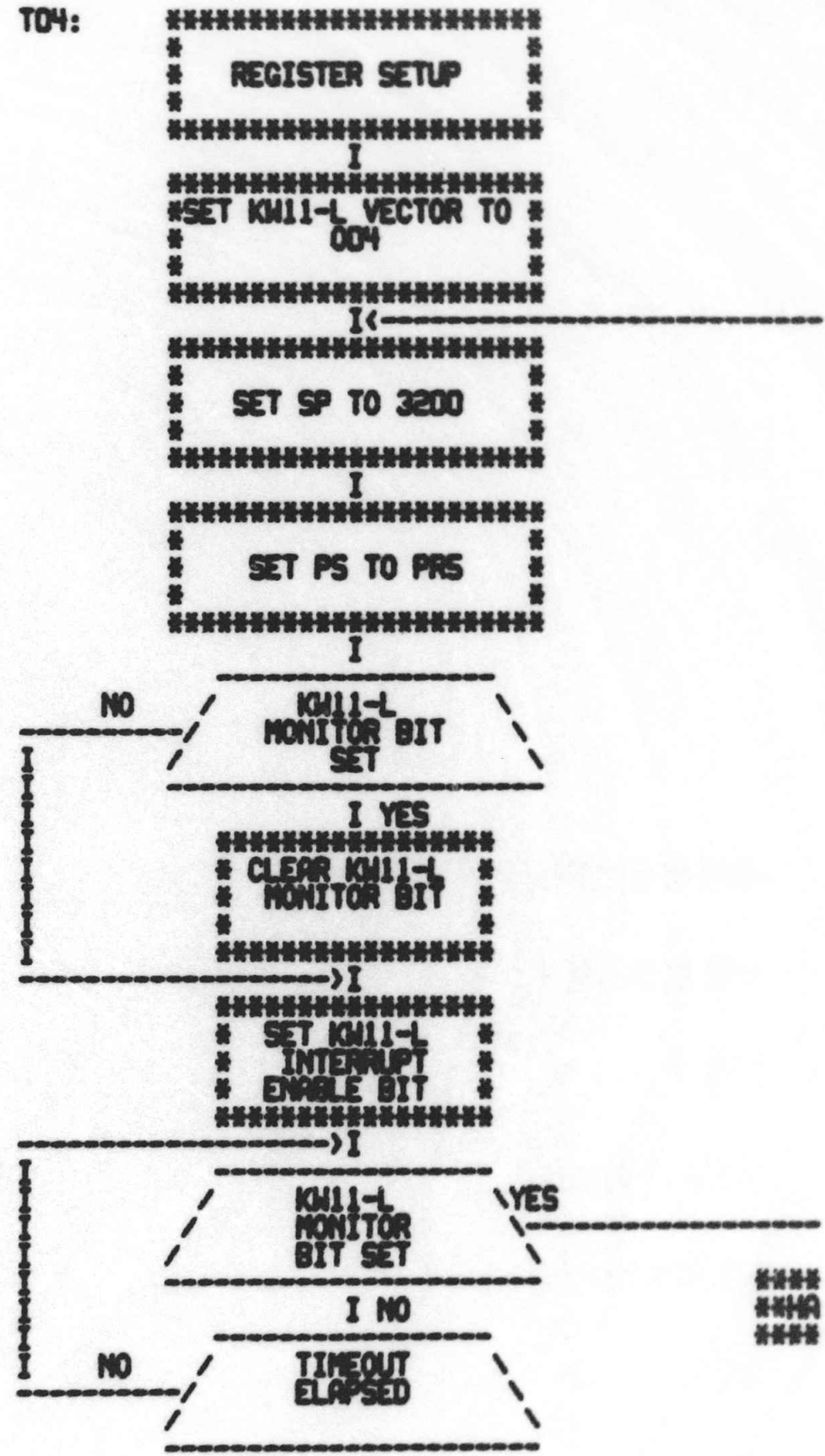
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BASIC MEMORY TIMING TESTS FLOWS

DECFL0 VER 00.0

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004: INTERRUPTS TO NEG

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*****
* SET PS TO PR7 *
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      I
*****
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```

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###  
###

NO1.

BMTT MACY11 27(732) 14 OCT-76 16:22 PAGE 14  
DBK1AA.P11

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# NEXT TEST #  
#  
#####

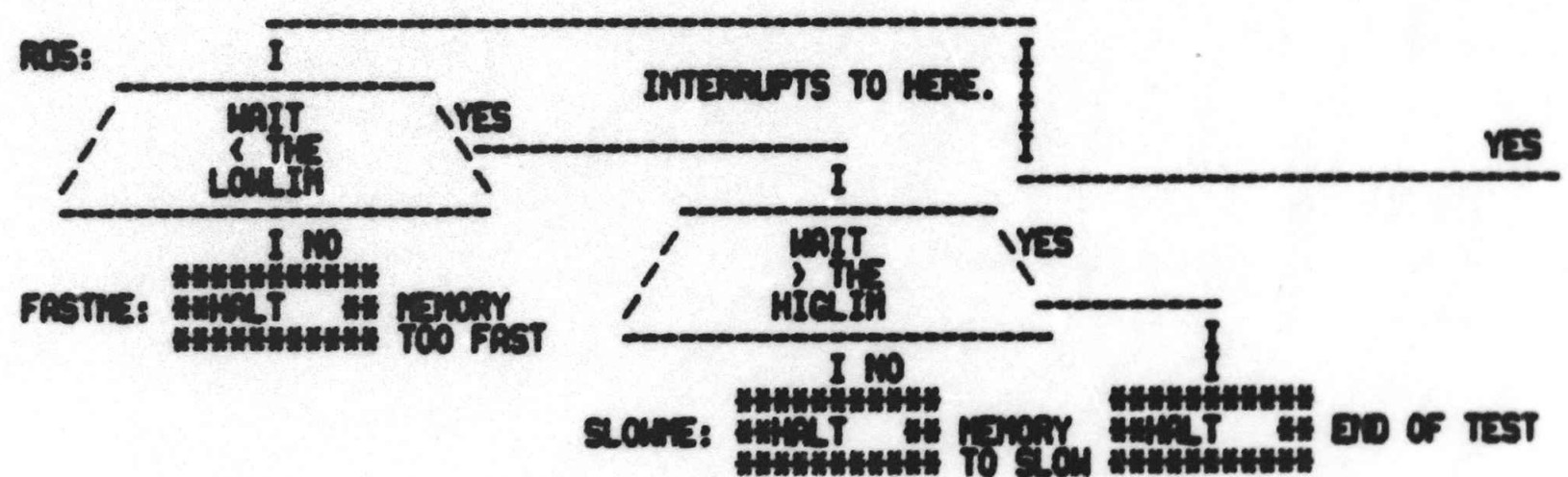
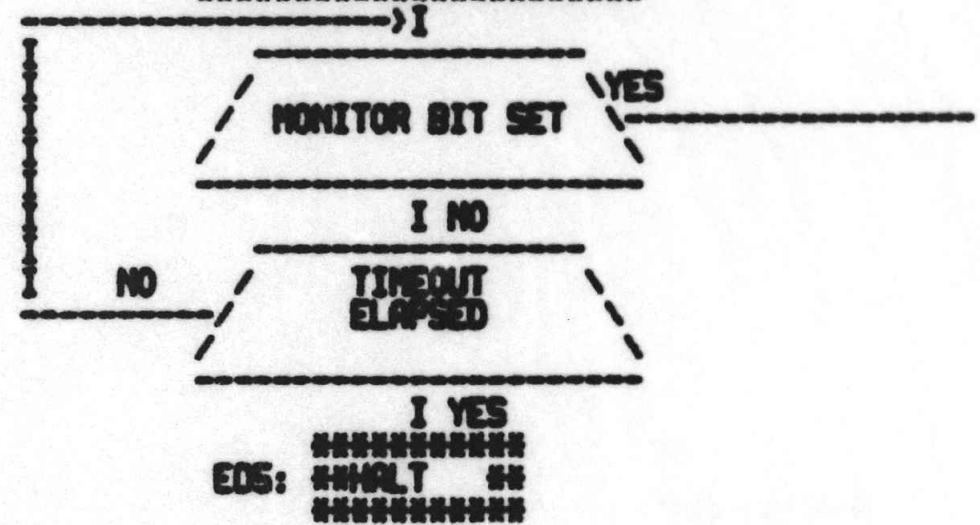
BASIC MEMORY TIMING TESTS FLOWS

FETCH CYCLE TIME:  
TOS:

```

*****
* REGISTER SETUP *
*****
      I
*****
* SET SP TO 3200 *
*****
      I
*****
* SET KILL-L VECTOR *
* TO "R05" *
*****

```



REVERSE SIDE OF PAGE - NOT REPRODUCED

C02

BHTT MACY11 27(732) 14-OCT-76 16:22 PAGE 16  
DEKVAR.P11

END

EO



00000007  
00000006  
00000005  
00000004  
00000003  
00000002  
00000001  
00000000

BASIC MEMORY TIMING TESTS FLOWS  
FLOW CHART CROSS REFERENCE LIST

DECFL0 VER 00.0

HALT      01# 02 02 03 03 04# 05 05 05 05 05

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      .TITLE      X
      .ENABL     BMTT
      .=1000     ABS

001000      ;KM11-L REAL TIME CLOCK BIT DEFINITIONS

000200      KMLMON=200      ;SET BY THE LINE FREQUENCY CLOCK
000100      KMLENA=100      ;LINE CLOCK INTERRUPT ENABLE

      ;REGISTER ADDRESSES

177546      LKSCSR=177546      ;COMMAND STATUS REGISTER ADDRESS

      ;DEVICE VECTOR ASSIGNMENTS

000100      LKSVEC=100      ;INTERRUPT VECTOR ADDRESS
000300      LKSPRT=PR6      ;PRIORITY 6

177776      PS=177776      ;PROCESSOR STATUS.
003200      STACK=3200      ;STACK PRESET.

      ;PRIORITY LEVELS EQUATES

000340      PR7=340
000300      PR6=300
000240      PR5=240
000200      PR4=200
000140      PR3=140
000100      PR2=100
000040      PR1=040
000000      PRO=000

      ;
000004      ETRVEC=4      ;BUS TIMEOUT TRAP (ILLEGAL OR NONEXISTANT MEMORY).
000010      RESVEC=10     ;RESERVED INTRUCTION TRAP.

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SBTTL KM11-L DEVICE RESPONSE  
\*\*\*\*\*  
THIS ROUTINE MAKES A BASIC CHECK OF THE KM11-L REAL TIME CLOCK  
THE TESTS TEST AS FOLLOWS:

- (T01) THAT WE CAN ACCESS THE "LKSCSR" WITHOUT A NCM TIMEOUT.
- (T02) THAT THE MONITOR BIT IS SET BY THE LINE CURRENT AFTER A REASONABLE PERIOD OF TIME
- (T03) THAT THE MONITOR BIT SET WITHOUT INTERRUPT ENABLE DOES NOT CAUSE AN INTERRUPT
- (T04) THAT THE INTERRUPT ENABLE BIT WHEN SET WILL ALLOW INTERRUPTS
- (T05) THIS TEST DETERMINES THAT THE CPU CYCLE TIME IS WITHIN LIMITS.

\*\*\*\*\*

```

001000 012700 000001
001004 012701 000001
001010 012702 177546
001014 005003
001016 005004

001020 012737 001102 000004
001026 012737 000340 000006

001034 012737 001106 000010
001042 012737 000340 000012

001050 012737 001112 000100
001056 012737 000300 000102

001064 012706 003200
001070 012737 000340 177776

001076 005712
001100 000406

```

```

T01:  MOV    #1,R0          ;R0=TEST NUMBER.
      MOV    #1,R1          ;R1=DEVICE (CLOCK #1).
      MOV    @LKSCSR,R2     ;R2=TEST ADDRESS.
      CLR    R3             ;CLEAR WAS ADDRESS.
      CLR    R4             ;CLEAR SHOULD BE ADDRESS.

      MOV    @ED1A,@ERRVEC  ;SET NCM TRAP.
      MOV    @PR7,@ERRVEC+2 ;SET PRIORITY TO #7.

      MOV    @ED1B,@RESVEC  ;SET ILLEGAL COMMAND TRAP.
      MOV    @PR7,@RESVEC+2 ;SET PRIORITY TO #7.

      MOV    @ED1C,@LKSVEC  ;SET CLOCK INTERRUPT VECTOR.
      MOV    @LKSPRT,@LKSVEC+2 ;SET CLOCK PRIORITY.

L01:  MOV    @STACK,SP      ;SET STACK TO 3200.
      MOV    @PR7,@MPS     ;SET CPU PRIORITY TO #7.

I01:  TST    (R2)           ;TEST FOR THE CLOCK.
      BR     T02           ;GOTO NEXT TEST.

```

\*\*\*\*\*

```

TEST #1.
(PC) (PS) (SP) TEST DEV# ADDRESS WAS S/B
(R7) (PSM) (R6) (R0) (R1) (R2) (R3) (R4)
1104 340 3174 1 1 177546 0 0

```

\*\*\*\*\*

```

001102 000000
001104 000767

```

```

ED1A: HALT
      BR    L01
      ;NON EXISTANT MEMORY TRAP (NO CLOCK).
      ;LOCK ON FATAL ERROR.
      ;THIS ERROR MCOULD BE CAUSED
      ;BY A TEST OTHER THAN "TEST #1"

```

;CHECK THE CONTENTS OF THE STACK  
;TO DETERMINE IT'S ORIGIN.

\*\*\*\*\*

TEST #1	(PC)	(PS)	(SP)	TEST	DEV#	ADDRESS	WAS	S/B
	(R7)	(PSW)	(R6)	(R0)	(R1)	(R2)	(R3)	(R4)
	1110	340	3174	1	1	177546	0	0

\*\*\*\*\*

ED1B: HALT  
BR LO1

;;;ILLEGAL COMMAND.  
;LOCK ON FATAL ERROR.  
;SEE COMMENT FOR PREVIOUS ERROR.

\*\*\*\*\*

TEST #1	(PC)	(PS)	(SP)	TEST	DEV#	ADDRESS	WAS	S/B
	(R7)	(PSW)	(R6)	(R0)	(R1)	(R2)	(R3)	(R4)
	1114	340	3174	1	1	177546	0	0

ED1C: HALT  
BR LO1

;;; UNEXPECTED KM11-L INTERRUPT.  
;LOCK ON FATAL ERROR.

001106 000000  
001110 000765

001112 000000  
001114 000763

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SBTTL KM11-L MONITOR BIT.

\*\*\*\*\*  
T02 ATTEMPTS TO SEE IF THE LINE CURRENT EVER SETS THE MONITOR BIT. THIS IS ACCOMPLISHED AS FOLLOWS:

- 1). TEST TO SEE IF THE MONITOR BIT IS ALREADY SET, IT PROBABLY WILL BE.
- 2). IF THE MONITOR BIT WAS SET CLEAR IT.
- 3). CLEAR A TIMER REGISTER FOR MAXIMUM WAITING TIME.
- 4). WAIT AROUND IN A TIME LOOP FOR THE FLAG TO SET.
- 5). IF IT FAILS TO SET PRIOR TO TIMEOUT THEN HALT.

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001116 012700 000002
001120 012701 000001
001124 012702 177546
001132 012704 000200
710
001136 012737 001204 000100
001144 012737 000340 000102
714
001152 012706 003200
001156 005005
715
001160 030412
001162 001401
717
001164 040412
001166 011203
001170 030412
001172 001006
001174 005205
001176 001373

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T02:  MOV    #2,R0           ;R0=TEST NUMBER.
      MOV    #1,R1         ;R1=DEVICE (CLOCK #1).
      MOV    @LKSCSR,R2    ;ADDRESS TO R2.
      MOV    @KALMON,R4    ;SHOULD BE.
      MOV    @ED2A,@LKSVEC ;SET KM11-L INTERRUPT VECTOR.
      MOV    @PR7,@LKSVEC+2 ;SET PRIORITY TO #7.
L02:  MOV    @STACK,SP     ;SET STACK TO 3200.
      CLR    R5            ;CLEAR TIMER.
      BIT    R4,(R2)       ;MONITOR BIT SET?
      BEQ   R02            ;NO!
      BIC   R4,(R2)       ;YES!
                        ;CLEAR MONITOR BIT.
R02:  MOV    (R2),R3       ;CONTENTS OF LKSCSR TO R3.
      BIT    R4,(R2)       ;MONITOR BIT SET?
      BNE   T03           ;YES! GOTO "T03"
      INC   R5            ;NO!
                        ;TIMEOUT OVER?
      BNE   R02           ;NO! CHECK MONITOR BIT AGAIN.

```

\*\*\*\*\*

TEST	#2						
(PC)	(PS)	(SP)	TEST	DEV#	ADDRESS	WAS	SHD BE
(R7)	(PSW)	(R6)	(R0)	(R1)	(R2)	(R3)	(R4)
1202	340	3200	2	1	177546	??????	200

\*\*\*\*\*

```

001200 000000
001202 000763

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E02:  HALT
      BR    L02           ;### MONITOR BIT FAILED TO SET.
                        ;LOCK ON FATAL ERROR.

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```

*****
TEST #2
(PC) (PS) (SP) TEST DEV# ADDRESS WAS S/B
(R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)
1206 340 3174 2 1 177546 ?????? 200
*****

```

001204 000000  
001206 000761

ED2A: HALT  
BR L02

;###UNEXPECTED KILL - L INTERRUPT.  
;LOCK ON FATAL ERROR.

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SBTTL KM11-L INTERRUPT ENABLE BIT.

\*\*\*\*\*

T03 VERIFYS THAT THE MONITOR ENABLE BIT BECOMING SET WITH MACHINE PRIORITY AT 0, WILL NOT CAUSE AN INTERRUPT UNLESS INTERRUPT ENABLE IS ALSO SET, AS FOLLOWS:

- 1).TEST TO SEE IF MONITOR BIT IS SET.
- 2). IF THE MONITOR BIT WAS SET THEN CLEAR IT.
- 3).SET CPU PRIORITY TO #0.
- 4).CLEAR THE TIMER FOR MAXIMUM WAITING TIME.
- 5).WAIT FOR THE MONITOR BIT TO SET IF IT DOESNT SET PRIOR TO THE TIMEOUT THAN HALT.

\*\*\*\*\*

```

001210 012700 000003
001214 012701 000001
001220 012702 177546
001224 012704 000200
001230 012737 001274 000100
001236 012706 003200
001242 030412
001244 001401
001246 040412
001250 005037 177776
001254 005005
001256 011203
001260 030412
001262 001006
001264 005205
001266 001373

```

```

T03:  NOV  #3,R0      ;R0=TEST NUMBER.
      NOV  #1,R1      ;DEVICE (CLOCK #1).
      NOV  #LKSCSR,R2 ;ADDRESS TO R2.
      NOV  #M0LNON,R4 ;SHOULD BE.
      NOV  #ED3A,#LKSV ;SET KM11 - L INTERRUPT VECTOR.

L03:  NOV  #STACK,SP ;SET THE STACK POINTER TO 3200.

      BIT  R4,(R2)    ;MONITOR BIT SET?
      BEQ  #03        ;NO!
      BIC  R4,(R2)    ;YES!
                        ;CLEAR MONITOR BIT.

N03:  CLR  #0PS       ;SET CPU PRIORITY TO PRO.
      CLR  #R5        ;CLEAR TIMER.

R03:  NOV  (R2),R3     ;CONTENTS OF LKSCSR TO R3.
      BIT  R4,(R2)    ;MONITOR BIT SET?
      BNE  #T04       ;YES! GOTO "T04"
                        ;NO!
      INC  #R5        ;TIMEOUT OVER?
      BNE  #R03       ;NO! CHECK MONITOR BIT AGAIN.

```

\*\*\*\*\*

```

TEST #3
(PC) (PS) (SP) TEST DEVS ADDRESS WAS SHD BE
(R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)
1272 0 3200 3 1 177546 ?????? 200

```

\*\*\*\*\*

001270 000000

E03: HALT ;\*\*\* MONITOR BIT FAILED TO SET.

016 001272 000761

BR L03

;LOCK ON FATAL ERROR.

017  
018  
019  
020  
021  
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029  
030  
031

\*\*\*\*\*

TEST	83						
(PC)	(PS)	(SP)	TEST	DEV8	ADDRESS	WAS	S/B
(R7)	(PSW)	(R6)	(R0)	(R1)	(R2)	(R3)	(R4)
1276	340	3174	1	1	177564	??????	200

\*\*\*\*\*

001274 000000  
001276 000757

ED3A: HALT  
BR L03

\*\*\*UNEXPECTED KM11 - L INTERRUPT.  
;LOCK ON FATAL ERROR.



001300  
001304  
001310  
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001962  
001966  
001970  
001974  
001978  
001982  
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001990  
001994  
001998

```

.SBTTL KM11-L INTERRUPT.
*****
T04 VERIFYS THAT THE KM11-L WILL CAUSE
AN INTERRUPT WHEN THE ENABLE BIT IS SET AND THE LINE
CURRENT CAUSES THE MONITOR BIT TO BE SET, AND THE CPU PRIORITY
IS SET AT #5 AS FOLLOWS.

1). SET UP KM11-L CLOCK TO TRAP TO NEXT TEST.
2). IF MONITOR BIT IS SET. CLEAR IT.
3). SET INTERRUPT ENABLE BIT.
4). CLEAR THE TIMER REGISTER FOR MAXIMUM WAITING TIME.
5). TEST TO SEE IF THE MONITOR BIT IS SET.
6). IF WE GET INTERRUPTED WE WILL GO TO NEXT TEST.
   OTHERWISE ERROR HALT.
*****

T04:  MOV      #4,R0          ;R0=TEST NUMBER.
      MOV      #1,R1          ;R1=DEVICE (CLOCK #1).
      MOV      @LKSCSR,R2      ;ADDRESS TO R2.
      MOV      @K1LMON,R4      ;SHOULD BE.
      MOV      #004,@LKSVCEC   ;SET KM11 - L VECTOR.

L04:  MOV      @STACK,SP      ;SET STACK TO 3200.
      MOV      @PRS,@PS       ;SET CPU STATUS TO #5.

      BIT      R4,(R2)        ;MONITOR BIT SET?
      BEQ      NO4            ;NO!
      BIC      R4,(R2)        ;YES!
      BIC      R4,(R2)        ;CLEAR MONITOR BIT.

NO4:  BIS      @K1LENA,(R2)    ;SET ENABLE BIT.

R04:  MOV      (R2),R3        ;CONTENT R04 OF LKSCSR TO R3.
      BIT      R4,(R2)        ;MONITOR BIT SET?
      BNE      ED4            ;YES! GOTO "ED4" NO INTERRUPTS.
      INC      R5              ;NO!
      BNE      R04            ;TIMEOUT OVER?
      INC      R5              ;NO!

```

```

*****
TEST #4
(PC) (PS) (SP) TEST DEV# ADDRESS WAS SHD BE
(R7) (PSW) (R6) (R0) (R1) (R2) (R3) (R4)
;1366 240 3200 4 1 177546 ?????? 200

```

888  
889  
890  
891  
892  
893  
894

001364 000000  
001366 000757  
001370 012737 000340 177776

.....

ED4: HALT  
BR L04  
MOV #PR7, @PS

; FATAL ERROR  
; HANG ON FATAL ERROR.  
; SET PRIORITY TO #7.



17072  
17073  
17074  
17075  
17076  
17077  
17078  
17079  
17080  
17081  
17082  
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17099  
17100

```

001450 040412      NOS:   BIC   R4,(R2)      ;CLEAR MONITOR BIT
001452 052712 000100      BIS   BKLENA,(R2)   ;SET INTERRUPT ENABLE BIT.

001456 005005      CLR   R5           ;CLEAR TIMER.
001460 012737 000240 177776  MOV   @R5,@R5     ;SET CPU TO PRIORITY #5.

001466 005205      IS:    INC   R5           ;AWAIT AN INTERRUPT.
001470 001376      BNE   IS

```

\*\*\*\*\*

```

TEST  #5
(PC)  (PS)  (SP)  TEST  DEV#  ADDRESS WAS  SHD BE
(R7)  (PSM) (R6)  (R0)  (R1)  (R2)  (R3)  (R4)
1470  240   3200  5     1     177546  ??????  200

```

\*\*\*\*\*

```

001472 000000      ED5A:  HALT
001474 000750      BR    LOS           ;### NO KM11-L INTERRUPT.
                                ;LOCK ON FATAL ERROR.

001476 020537 001520      NOS:  CMP    R5,@LOWLIN ;IS MEMORY TO FAST?
001502 103404      BLO   FASTME       ;YES!

001504 020537 001522      CMP    R5,@HIGLIN  ;IS MEMORY TO SLOW?
001510 103402      BHS   SLOWME       ;YES!
001512 000000      HALT ;TEST OKAY. NORMAL HALT

```

```

001514 000000      FASTME: HALT
001516 000000      SLOWME: HALT
001520 012000      LOWLIN: 012000
001522 012300      HIGLIN: 012300
000001      .END

```



T08	001116	637	7068
T03	001210	724	7808
T04	001300	798	8558
T05	001376	9208	
.	001524	9668	



REQ	718	789	856															
MEMS	980																	
INSTR	720	791	858	952														
INSTR	870	723	788	797	865	873	931											
INSTR	717																	
INSTR	977																	
INSTR	724	727	798	801	874	877	932	935	959									
INSTR	637	655	671	687	743	757	816	831	892	950	974							
INSTR	931	935	915	933	794	926	955											
INSTR	976	979																
INSTR	551	670	686	741	750	815	830	891	949	973	981	984	985					
INSTR	725	800	876	934	956													
INSTR	618	619	620	624	625	627	628	630	631	633	634	706	707	708	709			
INSTR	711	712	714	722	785	781	782	783	784	786	796	855	856	857	858			
INSTR	853	861	863	872	894	920	921	922	923	925	928	930	956					
INSTR	526																	
INSTR	988	565																
INSTR																		
INSTR																		
INSTR																		
INSTR																		
INSTR																		
INSTR																		
INSTR	599	688	760	832	895													
INSTR	564																	

ERRORS DETECTED: 0  
 DEFAULT GLOBALS GENERATED: 0  
 # DBKMAA.SEG/SOL/CRF/PAGN/NL:TOC/DS:ERFZ-DBKMAA.SML,DBKMAA.P11  
 RUN-TIME: 14 17 5 SECONDS  
 RUN-TIME RATIO: 109/32=3.4  
 CORE USED: 20K (39 PAGES)