

TR79-F

DRS TR79F UTIL TIM
CZTRBDO

AH-9433D-MC
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MADE IN USA



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IDENTIFICATION

PRODUCT CODE: AC-9431D-MC
PRODUCT NAME: CZTRBD0 TR79 UTILITY PROGRAMS
PRODUCT DATE: FEBURARY 1982
MAINTAINER: MERRIMACK DIAGNOSTIC ENGINEERING

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TR79 UTILITY PROGRAM

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1. ABSTRACT

THIS PROGRAM IS IN TWO PARTS, AND IS INTENDED TO PROVIDE THE USER WITH A TOOL FOR TROUBLE-SHOOTING THE TR79 MAGTAPE SUBSYSTEM ON A PDP-11 COMPUTER SYSTEM. THE FIRST PART OF THE PROGRAM ALLOWS THE USER TO GIVE THE MAGTAPE, COMMANDS, TO SIMULATE USER ROUTINES BY MERELY INSERTING THESE COMMANDS IN THE CORE LOCATIONS PROVIDED. THE USER MAY EXECUTE ONE OR SEVERAL INSTRUCTIONS IN ANY LEGAL SEQUENCE. WHILE THE CODE FOR THE DRIVER IS SIMPLE AND USES NO INTERRUPTS, DUE TO THE DESIGN OF THE HARDWARE CERTAIN ERROR CONDITIONS MUST BE IDENTIFIED IN ORDER TO PREVENT MISINTERPRITATION OF THE DESIRED RESULTS.

PART TWO OF THE PROGRAM CONSIST OF SELF CONTAINED ROUTINES TO PERMIT THE USER TO SET UP AND CHECK THE DELAYS CONTAINED WITHIN THE TR79 CONTROLLER, BY USING THE SWITCH REGISTER TO SELECT THE APPROPRIATE ROUTINE.

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2. REQUIREMENTS

2.1 HARDWARE

- A. PDP-11 PROCESSOR
- B. TR79 MAGTAPE TRANSPORT (HP-7970E DRIVE)
- C. TR79F MAGTAPE CONTROLLER

2.2 STORAGE

THIS PROGRAM REQUIRES A MINIMUM OF 4K OF CORE

3. LOADING

USE STANDARD BINARY LOADING PROCEDURE

4.0 STARTING PROCEDURE

THERE ARE TWO STARTING ADDRESSES THAT MAY BE USED

- 4.1 200 (8): LA 200 SR=0 A START AT THIS ADDRESS WILL RESULT IN A PROGRAMMED DEFAULT OPERATION OF A WRITE FORWARD WITH A WORD COUNT OF -20 AND A DATA PATTERN OF ALL 1'S. TO MODIFY THESE PARAMETERS SEE SECTION 7.1 PROGRAM OPERATION
NOTE: ALSO SEE SECTION 5.0 PROGRAM RESTRICTIONS, THE DEFAULT OF WRITE WILL NOT WORK IF TAPE IS AT B.O.T..

- 4.2 204 (8) LA 204 SR=0 A START AT THIS ADDRESS WILL EXECUTE THE SPECIALLY DESIGNED SETUP ROUTINES TO ALLOW THE USER TO SETUP OR VERIFY THE DELAYS WITHIN THE TR79 CONTROLLER.
NOTE: ALWAYS USE SCRATCH TAPES WHEN TAPE MOTION IS INDICATED.

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5.0 RESTRICTIONS

- 5.1 A. A PSEUDO-OP OF A 20(8) HAS BEEN PROVIDED TO ALLOW THE USER TO POWER CLEAR BETWEEN OPERATIONS IF DESIRED, HOWEVER THE PROGRAM CAN RECOVER FROM ERRORS. THIS IS A POWER CLEAR AND TAKES 900 MILI-SECONDS TO COMPLETE.
ANY ATTEMPTS TO ISSUE INSTRUCTIONS TO THE CONTROLLER WHILE A POWER CLEAR IS IN PROGRESS WILL RESULT IN ILLEGAL COMMAND BIT SETTING WHICH WILL INHIBIT ANY FURTHER INSTRUCTIONS FROM BEING EXECUTED. A POWER CLEAR IS ALSO GENERATED FROM A BUS INIT WHICH OCCURS FROM A RESET INSTRUCTION. THE DRIVER USES NO RESETS. (USE CAUTION IF YOU MODIFY THE DRIVER PACKAGE.)
- B. THE TR79 CONTROLLER CHECKS FOR CERTAIN ILLEGAL FUNCTIONS DUE TO TAPE POSITION OR STATUS, THE DRIVER PACKAGE WILL CHECK THESE CONDITIONS AND HALT AT APPROPRIATE LOCATIONS WITH MEANINGFULL DATA DISPLAYED (SEE SECTION 7.2 ERROR CHECKS).
THE LISTED CONDITIONS WILL PRODUCE ILLEGAL COMMAND ERRORS:
1. ATTEMPT TO WRITE DATA FROM LOAD POINT WITHOUT AN I.D.B.
 2. ATTEMPT TO WRITE A TAPE MARK FROM LOAD POINT
 3. ATTEMPT TO MOVE TAPE IN REVERSE FROM LOAD POINT
 4. ATTEMPT TO WRITE AN I.D.B. AT OTHER THAN LOAD POINT
 5. ATTEMPT TO WRITE DATA WITH THE WRITE RING REMOVED
 6. ISSUE A COMMAND WHILE THE MAGTAPE IS NOT READY
 7. ISSUE A COMMAND WHILE THE CONTROLLER IS NOT READY
 8. ISSUE A COMMAND WITH INHIBIT BIT SET
 9. ILLEGAL FUNCTION CODES 00,03,05,06,11,12,14
- C. THE PROGRAM DOES NO DATA CHECKS ON READ OR WRITE DATA TRANSFERRED. IT IS THE RESPONSIBILITY OF THE OPERATOR TO MANUALLY EXAMINE THE BUFFER LOCATIONS TO DETERMINE IF THERE HAVE BEEN ANY PICKED OR DROPPED BITS IF DESIRED.
- D. NOTE: HARDWARE OPERATION OF THE TR-79 SPECIFIES THAT EACH CORE WORD LOCATION CONTAIN ONE BYTE (BITS 0-7) OF DATA AND PARITY (BIT 8). THEREFORE WHEN CALCULATING THE WORD COUNT FOR A TRANSFER THE ACTUAL NUMBER OF CORE BYTE LOCATIONS ACCESSED IS EQUAL TO 2X THE NUMBER LOADED IN THE WORD COUNT REGISTER. ALSO NOTE THAT THE CONTROLLER DOES NOT APPEND PARITY TO THE BYTE BEFORE DOING A WRITE OPERATION. PARITY MUST BE CORRECT IN CORE OTHERWISE ERRORS WILL OCCUR ON THE TRANSFER (ODD PARITY) IS ALWAYS USED.

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6.0 CONSOLE SWITCH SETTINGS

SW 15 = 1 STOP AFTER EACH OPERATION (ONLY WITH START 200)
0 PROCEED

SW 14 = 1 STOP AT THE END OF EACH PROGRAM PASS (ONLY WITH START 200)
0 PROCEED

SW 7 = 1 ENABLE FOR DELAY ROUTINES (EXECUTE ROUTINE ONLY WITH START 204)
0 ALLOW SELECTION OF DELAY ROUTINES WITH SW 0-3

SW 0 THU 3 = DELAY ROUTINE TO BE EXECUTED (ONLY WITH START 204)

6.1 DELAY SETUP TABLE

SWITCH SETING	DELAY NAME	MODULE TYPE	LOCATION	PRINT PAGE	INPUT PIN	OUTPUT PIN	TIME
00	NO-OP						
01	P CLR	M-302	C-06	T02-2	H2	F2	20 MILI SEC.
02	P CLR OFF	M-306	D-09	T04-1	H2	T2	900 MILI SEC.
03	ERROR CLK	M-302	C-10	T04-2	H2	F2	200 NANO SEC.
04	WRITE ENAB	M-302	C-10	T09-3	M2	T2	40 MICRO SEC.
05	BUFF CONT	M-304	B-18	T11-1	E1	J1	1 MICRO SEC.
06	END WR DAT	M-302	A-16	T11-1	M2	T2	18 MICRO SEC.
07	1ST WD REQ	M-302	A-22	T11-2	H2	F2	100 MICRO SEC.
10	ERASE	M-304	B-18	T09-3	S1	M1	1 MICRO SEC.
11	WRITE IDB	M-302	A-16	T09-1	H2	F2	17 MILI SEC.
12	IDB TIMING	M-302	D-13	T09-1	H2	F2	75 MILI SEC.
13	ABORT	M-306	A-25	T09-3	H2	T2	1.5 SEC.
14	BUSY DELAY	M-304	B-18	T05-1	R1	P1	100 NANO SEC.
15	GO BIT DEL	M-304	B-18	T06-1	D1	H1	1 MICRO SEC.
16	M.S.D.	M-302	A-22	T09-2	M2	T2	900 MILI SEC.
17	NO-OP						

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 * DELAY CONDITION NOTES *

6.2 DELAY

\$\$=FIXED DELAYS

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257			
258		00	NO OPERATION PERFORMED WAITING SWITCH SELECTION AND ENABLE
259		01	POWER CLEAR PERFORMED NO TAPE MOTION DELAY PULSE IS POSITIVE GOING
260		02	POWER CLEAR PERFORMED NO TAPE MOTION DELAY PULSE IS POSITIVE GOING
261		03	NO TAPE MOTION, PROGRAM FORCES AN ERROR WITH THE BGL BIT
262			IN THE TR STATUS REGISTER (BIT 11) DELAY PULSE IS POSITIVE GOING
263		04	TAPE MOTION, PROGRAM DOES A SHORT ERASE WHILE MOVING TAPE
264			TAPE MOTION IS NOT READILY NOTICIBLE WHILE EXECUTING THIS ROUTINE
265			DELAY PULSE IS POSITIVE GOING
266			
267			
268			
269			
270			
271	\$\$	05	TAPE MOTION, PROGRAM DOES A 10 BYTE WRITE, PROGRAM CHECKS
272			FOR LOAD POINT AND WILL WRITE AN I.D.B. BEFORE ENTERING THE
273			DELAY LOOP. DELAY PULSE IS POSITIVE GOING
274			
275		06	SAME CONDITIONS AS 05 DELAY PULSE IS POSITIVE GOING
276			
277		07	SAME CONDITIONS AS 05 DELAY PULSE IS POSITIVE GOING
278			
279	\$\$	10	TAPE MOTION, PROGRAM WILL CHECK FOR LOAD POINT THEN DO A
280			MAXIMUM ERASE TO MAKE THE OPERATION CONTINUOUS THE PROGRAM
281			WILL CLEAR THE ERASE COUNT BEFORE THE OPERATION IS DONE.
282			DELAY PULSE IS NEGATIVE GOING
283			
284		11	TAPE MOTION, PROGRAM WILL CONTINUOUSLY WRITE THE I.D.B.
285			DELAY PULSE IS POSITIVE GOING
286			
287		12	SAME CONDITIONS AS DELAY 11. DELAY PULSE IS POSITIVE GOING
288			
289		13	PROGRAM WILL REWIND TAPE TO L.P. AND FORCE AN ERROR BY DOING
290			A WRITE DATA. DELAY PULSE IS POSITIVE GOING.
291			
292	\$\$	14	TAPE WILL MOVE TO L.P. , AND DO A MAXIMUM ERASE.
293			WHILE THIS IS HAPPENING PROGRAM WILL LOAD THE COMMAND
294			REGISTER TO PRODUCE A LD CTRL PULSE. DELAY PULSE IS POSITIVE GOING
295			
296	\$\$	15	SAME CONDITIONS AS DELAY 04. DELAY PULSE IS NEGATIVE GOING
297			
298		16	PROGRAM WILL MOVE TAPE TO E.O.T. AND ATTEMPT TO DO A FAST
299			FORWARD TO PRODUCE THE MOTION STOP DELAY. DELAY IS POSITIVE.
300			NOTE: AFTER COMPLETION OF THIS ROUTINE A MANUAL REWIND
301			SHOULD BE PERFORMED.
302			
303		17	THIS IS A NO OPERATION SAME AS 00
304			

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7.0 OPERATION

THE PROGRAM IS QUITE SIMPLE HOWEVER IT DOES REQUIRE KNOWLEGE OF THE OF THE TR-79 MAGTAPE SYSTEM AND AN UNDERSTANDING OF THE PROGRAM FUNCTIONS AND RESTRICTIONS. THE CODE HAS BEEN ASSEMBLED IN IMMEDIATE AND ABSOLUTE MODES USING PC ADRESSING. IT IS RECOMMENDED THAT THE USER READ AND UNDERSTAND THE RESTRICTIONS AND OPERATIONS SECTIONS.

THE DRIVER PROGRAM (LOAD ADRESS 200, START SWITCHES =0) CAN BE MADEB TO EXECUTE ANY LEGAL SEQUENCE OF OPERATIONS (SEE SECTION 7.3) BY INSERTING THE COMMANDS IN THE OPERATIONS TABLE, (CORE LOCATIONS 722 THRU 766). EACH COMMAND SHOULD OCCUPY ONE CORE LOCATION BITS 0-4 ONLY. THE TOTAL NUMBER OF COMMANDS TO BE EXECUTED SHOULD THEN BE ENTERED IN LOCATION 720. THE PROGRAM PARAMETERS MAY BE ALTERED BY CHANGING THE APPROPRIATE CORE LOCATIONS (SEE SECTION 7.1). PROGRAM DEFAULT IS A SINGLE WRITE COMMAND OF 20 WORDS OF ALL 1'S FROM LOCATION 2700 WITH MINIMUM DELAY BETWEEN OPERATIONS. THIS DEFAULT WILL NOT WORK IF THE TAPE IS POSITIONED AT LOAD POINT.

THE DELAY PROGRAM (LOAD 204, START SWITCHES=0) WILL EXECUTE THE DELAY SET-UP ROUTINES TO ALLOW SET-UP OF ALL THE DELAYS IN THE TR-79 CONTROLLER THE PROGRAM HAS AN ACTIVE SWITCH REGISTER AFTER STARTING. BY SELECTING THE DESIRED DELAY ROUTINE IN SWITCH REGISTER 0 THRU 3, AND THEN SETTING BIT 7 =1 THE ROUTINE WILL BEGIN EXECUTION. TO CHANGE THE DELAY ROUTINE SET BIT 7=0, WAIT A FEW SECONDS FOR COMPLETION OF THE ROUTINE, THEN ENTER THE NEW ROUTINE NUMBER IN BITS 0-3 AND SET BIT 7=1. THE DELAY PROGRAM CONTAINS NO ERROR HALTS, HOWEVER IF ERRORS ARE DETECTED THE PROGRAM WILL INFORM THE USER BY OUTPUTTING A BELL CODE TO THE CONSOLE TERMINAL. THE PROGRAM WILL THEN DO A CONTROL RESET AND CONTINUE.

NOTE: THE PROGRAM BUILDS THE CORE DATA BUFFERS EACH TIME THE PROGRAM IS STARTED. THE PROGRAM DEFAULT IS LOCATION 2700 HOWEVER THIS MAY BE CHANGED BY MODIFYING LOCATION 242 IN THE CORE BUILD ROUTINE TO PUT THE BUFFERS ANYPLACE IN THE LOWER 28K. THIS PROGRAM DOES NOT PROGRAM THE KT AND DOES NOT RELOCATE ABOVE THE LOWER 28K OF MEMORY.

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7.1 PROGRAM PARAMETER LIST AND CORE ADDRESSES

PARAMETER	LOCATION	DESCRIPTION
EXTENDED CORE ADDRESS	700	BITS 12 AND 13 OF THIS LOCATION REPRESENT XBA 16 AND XBA 17 OF THE TR CONTROL REGISTER. THESE BITS ALLOW RELOCATION OF THE DATA BUFFER.
UNIT SELECT	702	BITS 8+9 IN THIS LOCATION REPRESENT THE UNIT NUMBERS OF THE TAPE DRIVES. A MAXIMUM OF 4 DRIVES PER CONTROLLER DEFAULT IS UNIT 0.
WORD COUNT	704	THIS IS THE 2'S COMPLIMENT OF THE NUMBER OF WORDS TRANSFERRED. SINCE EACH BYTE OCCUPIES A WORD LOCATION THE NUMBER OF CORE LOCATIONS USED IS 2X THE WORD COUNT. PROGRAM DEFAULT IS -20 WORDS.
READ ADDRESS	706	CONTAINS ADDRESS OF THE READ BUFFER. PROGRAM DEFAULT IS LOCATION 6700.
WRITE ADDRESS	710	CONTAINS ADDRESS OF THE WRITE BUFFER. THE PROGRAM CONTAINS 4 WRITE PATTERNS CONTIGIOUS IN CORE. LOCATION 2700 = ALL 1'S PATTERN LOCATION 3700 = ALTERNATE 1 AND 0 BYTES LOCATION 4700 = ALTERNATE 1 AND 0 BITS LOCATION 5700 = SLIDING 1 BIT PATTERN PROGRAM DEFAULT IS LOCATION 2700
ERASE COUNT	712	CONTAINS A 2'S COMPLIMENT NUMBER PROPORTIONAL TO THE AMOUNT OF TAPE TO BE ERASED. THIS NUMBER IS LOADED INTO THE WORD COUNT REGISTER PRIOR TO AN ERASE COMMAND BEING PERFORMED. PROGRAM DEFAULT IS 77777. EACH INCREMENT CAUSES .02 INCHES OF TAPE TO BE ERASED.
OPERATION DELAY	714	CONTAINS A NUMBER USED IN A TIMER BETWEEN OPERATIONS DEFAULT =000001 MINIMUM DELAY
OPERATION DELAY MULT.	716	THIS IS USED IN CONJUNCTION WITH LOC. 714 AS A MULTIPLIER IN THE DELAY TIMER. DEFAULT IS 000004 MINIMUM DELAY. INCREASING THIS NUMBER WILL ALLOW MORE TIME BETWEEN OPERATIONS.
OPERATIONS NUMBER	720	THIS LOCATION CONTAINS THE NUMBER OF OPERATIONS TO BE PERFORMED IN THE OP TABLE. DEFAULT = 1.
OPERATIONS TABLE	722 THRU 766	THIS IS THE BEGINNING OF THE OPERATIONS TABLE. ALL OPERATIONS TO BE PERFORMED SHOULD BE ENTERED IN THE DESIRED SEQUENCE IN THIS TABLE. DEFAULT IS A WRITE OPERATION.

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7.2 ERROR CHECKS AND HALTS

LOCATION	DESCRIPTION
1320	HALT HERE IF THERE WAS AN ATTEMPT TO EXECUTE AN ILLEGAL FUNCTION, DUE TO TAPE POSITION OR SEQUENCE OF INSTRUCTIONS. THE ILLEGAL COMMAND IS DISPLAYED IN RO WHEN THE PROGRAM HALTS. SEE SECTION 5.1B FOR ILLEGAL FUNCTIONS
1332	HALT HERE IF THERE WAS A HARDWARE ERROR ON THE PREVIOUS OPERATION IF IT IS DESIRED TO BYPASS THE ERROR FLAG NOP THIS LOCATION. THE COMMAND AND STATUS REGISTER SHOULD BE EXAMINED AT THIS TIME TO DETERMINE THE PROBABLE CAUSE OF THE ERROR. PRESSING CONTINUE WILL CLEAR THE ERROR BY EXECUTING A CONTROL RESET.
1350	HALT HERE IF YOUR OPERATION TABLE LOC.722-766 HAS AN OPERATION THAT IS NOT DEFINED IN THE LEGAL FUNCTION CODES. RO HAS THE BAD CODE IN IT,CHECK YOUR TABLE IN LOCATIONS 722 THRU 766.
1406	HALT HERE IF BIT 15 OF THE SWR IS SET. THIS IS THE HALT BETWEEN INSTRUCTIONS.
1432	HALT HERE IF BIT 14 OF THE SWR IS SET. THIS IS THE HALT BETWEEN PASSES OF INSTRUCTIONS IN THE OP TABLE.

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7.3 TABLE OF LEGAL FUNCTIONS AND CODES FOR USE IN OPERATIONS TABLE (LOC 722-766)

<u>CODE</u>	<u>FUNCTION</u>
00	**** ILLEGAL ****
01	WRITE DATA (ILLEGAL IF EXECUTED FROM LOAD POINT)
02	READ (DATA, TAPE MARK OR I.D.B.)
03	**** ILLEGAL ****
04	SPACE REVERSE (ILLEGAL IF ISSUED FROM LOAD POINT)
05	**** ILLEGAL ****
06	**** ILLEGAL ****
07	ERASE
10	REWIND (TAPE MOVES AT 160 I.P.S.) ILLEGAL IF ISSUED FROM LOAD POINT.
11	**** ILLEGAL ****
12	**** ILLEGAL ****
13	FAST FORWARD (TAPE MOVES FORWARD AT 160 I.P.S.)
14	**** ILLEGAL ****
15	WRITE I.D.B. (ILLEGAL IF ISSUED AT OTHER THAN LOAD POINT)
16	WRITE TAPE MARK (ILLEGAL IF ISSUED FROM LOAD POINT)
17	OFFLINE (REQUIRES MANUAL INTERVENTION)
20	CONTROL RESET (PROGRAM PSEUDO OP)

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8. PROGRAM LISTING

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481 000000
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489 000001
490 000002
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495 000007
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503 164000
504 164002
505 164004
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.TITLE TR79 UTILITY DRIVER
.ASECT

* GENERAL REGISTER DEFINITIONS *

R0=%0
R1=%1
R2=%2
R3=%3
R4=%4
R5=%5
SP=%6
PC=%7

* TR79 REGISTER DEFINITIONS *

TRCOM=164000
TRSTAT=164002
TRWC=164004
TRBA=164006

* PROCESSOR REGISTER DEFINITIONS *

PSW=177776
SWR=177570

* TTY REGISTERS *

TTSTAT=177564
TTBUF=177566

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536      000000
537      000200
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546
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548      000200
549 000200 000137 000230
550 000204 005237 000356
551 000210 000137 000230
552 000214 000777
553 000216 000777
554 000220 000400
555 000222 000777
556 000224 000525
557 000226 000652
558 000230 012701 000214
559 000234 012703 000216
560 000240 012702 002700
561 000244 012700 177400
562 000250 011122
563 000252 005200
564 000254 001403
565 000256 011322
566 000260 005200
567 000262 001372
568 000264 062701 000004
569 000270 062703 000004
570 000274 022701 000230

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*****
* TRAP CATCHERS *
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.=0
.REPT 200
.+2
HALT
.ENDR

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*****
* STARTS AND CORE BUFFER BUILD *
*****

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BEGIN:
BEGIN2:

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.=200
JMP @#CORBIL      ;NORMAL START
INC @#NORST        ;SETS FLAG TO DETERMINE WHO STARTED
JMP @#CORBIL      ;START HERE FOR DELAY ROUTINES

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CORBIL:

X1:
X2:
X3:

X4:

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000777
000777
000400
000777
000525
000652
MOV #214,R1      ;SET UP PATTERN GENERATOR
MOV #216,R3      ;SET UP PATTERN GENERATOR
MOV #2700,R2     ;SET UP ADDRESS POINTER
MOV #177400,R0   ;SET UP COUNTER
MOV (R1),(R2)+  ;DO IT
INC R0           ;KEEP TRACK OF HOW MANY
BEQ X4          ;CHECK FOR DONE
MOV (R3),(R2)+  ;DO IT
INC R0           ;KEEP COUNTING
BNE X3          ;LOOP HERE
ADD #4,R1       ;NEXT PATTERN
ADD #4,R3       ;GO TO NEXT PATTERN
CMP #230,R1     ;DONE YET

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571      ;
572      ;
573 000300 001361      BNE X2      ;NOT DONE YET
574 000302 005000      SLB: CLR R0      ;CLEAR THE PATTERN GENERATOR
575 000304 005001      CLR R1      ;CLEAR THE PATTERN COUNTER
576 000306 005200      INC R0      ;SET BIT IN PATTERN
577 000310 005201      SLB1: INC R1      ;KEEP COUNT
578 000312 010022      MOV R0,(R2)+ ;PUT IT IN CORE
579 000314 022702 006700 CMP #6700,R2 ;SEE IF WERE FINISHED
580 000320 001405      BEQ SLBDON ;YES JUMP OUT
581 000322 022701 000011 CMP #11,R1 ;CHECK ON THE BIT POSITION
582 000326 001765      BEQ SLB      ;RESET THE SLIDING BIT
583 000330 006300      ASL R0      ;SHIFT THE BIT
584 000332 000765      BR SLB1     ;LOOP AGAIN
585 000334 005737 000356 SLBDON: TST @#NORST ;SEE WHERE THE START CAME FROM
586 000340 001404      BEQ ALD      ;IF = 0 MUST HAVE BEEN START 200
587 000342 005037 000356 CLR @#NORST ;CLEAR IT OUTFOR NEXT TIME
588 000346 000137 001462 JMP @#DRTN  ;NOT = GO TO 204 START
589 000352 000137 001000 JMP @#START ;GO TO A 200 START
590 000356 000000      NORST: 000000 ;TEMPORARY LOCATION
591      ;
592      ;
593      ;
594      ;
595      ;
596      ;
597 000500 000500      SUBSTK: 000000      .=500      ;SUBROUTINE STACK
598      ;
599      ;
600      ;
601      ;
602 000600 000600      ;STACK: 000000      .=600      ;SET STACK HERE
603      ;
604      ;
605      ;

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*****
*   STACKS   *
*****

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788
789 001352 013737 000716 000666 OPDEL: MOV @#OPDLX,@#TIMMUL ;SET UP OPERATIONS DELAY MULTIPLIER
790 001360 013700 000714 MOV @#OPDLY,R0 ;SET UP OPERATIONS DELAY TIMER
791 001364 005300 8$: DEC R0 ;TIMER IS TICKING
792 001366 001376 BNE 8$ ;GET MORE TIME
793 001370 005337 000666 DEC @#TIMMUL ;COUNT DOWN THE MULTIPLIER
794 001374 001373 BNE 8$ ;GET MORE TIME
795 001376 032737 100000 177570 BIT #100000,@#SWR ;TIMES UP CHECK SWITCHES TO SEE IF WE HALT OR CONTINUF
796 001404 001401 BEQ .+4 ;DONT STOP NOW SKIP THE HALT
797 001406 000000 INSHLT: HALT ;STOP BETWEEN INSTRUCTIONS
798 001410 005301 DEC R1 ;-1 FROM THE NUMBER OF OPERATIONS IN R1
799 001412 001001 BNE 9$ ;GO AND DO THE NEXT INSTRUCTION
800 001414 000401 BR .+4 ;SKIP THE JUMP
801 001416 000137 001040 9$: JMP @#LOOP ;DO THE LOOP AGAIN
802 001422 032737 040000 177570 BIT #40000,@#SWR ;CHECK SWITCHES TO SEE IF WE WANT TO STOP AT END OF PAS
803 001430 001401 BEQ REST ;DO THE NEXT PASS SKIP THE HALT
804 001432 000000 PASHLT: HALT ;STOP BETWEEN PASSES
805 001434 000137 001000 REST: JMP @#START ;GO DO IT AGAIN (NEXT PASS)
806
807
808
809
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811
812 001440 000001 LEGOPS: 00001 ;WRITE
813 001442 000002 00002 ;READ
814 001444 000004 00004 ;SPACE REVERSE
815 001446 000007 00007 ;ERASE
816 001450 000010 00010 ;REWIND
817 001452 000013 00013 ;FAST FORWARD
818 001454 000015 00015 ;WRITE IDB
819 001456 000016 00016 ;WRITE TAPE MARK
820 001460 000017 00017 ;OFFLINE
821

```

* OPERATION DELAY BETWEEN INSTRUCTIONS *

* LEGAL OPERATIONS COMPARITOR TABLE *

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```

*****
* INDEX TABLE OF DELAY PROGRAM DIRECTIVES *
*****

```

```

844
845
846
847
848
849
850
851 001546 000137 001510
852 001552 000137 001646
853 001556 000137 001646
854 001562 000137 001702
855 001566 000137 001752
856 001572 000137 002J14
857 001576 000137 002014
858 001602 000137 002014
859 001606 000137 002150
860 001612 000137 002234
861 001616 000137 002234
862 001622 000137 002354
863 001626 000137 002070
864 001632 000137 001752
865 001636 000137 002274
866 001642 000137 001510
867
868
869
870

```

TABLE:

```

JMP @#BR1
JMP @#BR2
JMP @#BR2
JMP @#BR3
JMP @#BR4
JMP @#BR5
JMP @#BR5
JMP @#BR5
JMP @#BR10
JMP @#BR11
JMP @#BR11
JMP @#BR16
JMP @#BR6
JMP @#BR4
JMP @#BR14
JMP @#BR1

```

```

:DELAY 0 IS A NO-OP
:DELAY 1 IS FOR POWER CLEAR
:DELAY 2 IS FOR POWER CLEAR
:DELAY 3 IS FOR ERROR CLK
:DELAY 4 IS FOR WRITE ENABLE
:DELAY 5 IS FOR OUT BUFF FLAG
:DELAY 6 IS FOR END WRITE DATA
:DELAY 7 IS FOR FIRST WORD WRITE REQUEST
:DELAY 10 IS FOR ERASE
:DELAY 11 IS FOR WRITE I.D.B.
:DELAY 12 IS FOR I.D.B. TIMING
:DELAY 13 IS FOR ABORT WINDOW
:DELAY 14 IS FOR LD CTRL + BUSY
:DELAY 15 IS FOR GO PULSE DELAY
:DELAY 16 IS FOR M.S.D. DELAY
:DELAY 17 IS A NO-OP

```


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```

871
872
873
874
875 001646 004537 002502
876 001652 005000
877 001654 012701 000004
878 001660 005300
879 001662 001376
880 001664 005301
881 001666 001374
882 001670 105737 177570
883 001674 100764
884 001676 000137 001510
885
886
887
888
889
890 001702 012700 000070
891 001706 012701 000004
892 001712 052737 004000 164002
893 001720 005300
894 001722 001376
895 001724 005037 164002
896 001730 005301
897 001732 001372
898 001734 105737 177570
899 001740 100760
900 001742 004537 002502
901 001746 000137 001510
902
903
904
905
906
907 001752 004537 002522
908 001756 012737 177777 164004
909 001764 012737 000017 164000
910 001772 004537 002522
911 001776 004537 002540
912 002002 105737 177570
913 002006 100763
914 002010 000137 001510

```

```

*****
* ROUTINE FOR DELAYS 1 AND 2 *
*****
BR2: JSR R5,@#PCL ;DO A POWER CLEAR
      CLR R0 ;CLEAR THE TIMER
      MOV #4,R1 ;SET TIMING DELAY MULTIPLIER
BR2A: DEC R0 ;TIMER IS TICKING
      BNE BR2A ;WAIT TILL ITS DONE
      DEC R1 ;ONCE THROUGH THE TIMING LOOP
      BNE BR2A ;REPEAT LOOP IF MULTIPLIER IS NON ZERO
      TSTB @#SWR ;CHECK FOR A LOOP
      BMI BR2 ;DO IT AGAIN
      JMP @#BR1 ;GET NEXT TEST

```

```

*****
* ROUTINE FOR DELAY 3 *
*****
BR3: MOV #70,R0 ;SET UP DELAY MULTIPLIER
      MOV #4,R1 ;SET TIMING DELAY MULTIPLIER
      BIS #4000,@#TRSTAT ;FORCE AN ERROR WITH B.G.L. BIT
13$: DEC R0 ;TIMER IS TICKING
      BNE 13$ ;CHECK TIMER
      CLR @#TRSTAT ;OK NOW CLEAR THE BIT
      DEC R1 ;ONCE THROUGH TIMING LOOP
      BNE 13$ ;REPEAT LOOP IF MULTIPLIER IS NON ZERO
      TSTB @#SWR ;SEE IF WE WANT TO DO IT AGAIN
      BMI BR3 ;OK LOOP BACK
      JSR R5,@#PCL ;DONE HERE DO A POWER CLEAR AND GET THE NEXT ONE
      JMP @#BR1 ;GET THE NEXT DELAY DIRECTIVE

```

```

*****
* ROUTINE FOR DELAY 4 AND 15 *
*****
BR4: JSR R5,@#RDY ;CHECK FOR READY
BR4A: MOV #-1,@#TRWC ;THIS NUMBER IS USED FOR AN ERASE COUNT
      MOV #17,@#TRCOM ;DO THE ERASE
      JSR R5,@#RDY ;WAIT TILL DONE
      JSR R5,@#ERCK ;SEE IF WE ERRORED OUT
      TSTB @#SWR ;SEE IF WE LOOPON TEST
      BMI BR4A ;LOOP HERE AND DO IT AGAIN
      JMP @#BR1 ;GET OUT AND GET NEXT DELAY DIRECTIVE

```

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 * ROUTINE FOR DELAY 5 , 6 AND 7 *

915						
916						
917						
918						
919						
920	002014	004537	002570		BR5:	JSR R5,@#OFLP ;SEE IF WE ARE AT LOAD POINT
921	002020	005037	164002			CLR @#TRSTAT ;CLEAR INHIBIT BIT
922	002024	012737	177774	164004	BR5A:	MOV #-4,@#TRWC ;SET UP FOR A 10 BYTE WRITE
923	002032	013737	000710	164006		MOV @#WADDR,@#TRBA ;SET UP THE WRITE ADRESS BUFFER
924	002040	012737	000003	164000		MOV #3,@#TRCOM ;DO THE WRITE
925	002046	004537	002522			JSR R5,@#RDY ;WAIT FOR READY
926	002052	004537	002540			JSR R5,@#ERCK ;CHECK FOR ERRORS
927	002056	105737	177570			TSTB @#SWR ;SEE IF WE WANT TO LOOP
928	002062	100760				BMI BR5A ;LOOP HERE AND DO IT AGAIN
929	002064	000137	001510			JMP @#BR1 ;GET OUT AND GET NEXT DELAY DIRECTIVE

 * ROUTINE FOR DELAY 14 *

930						
931						
932						
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935						
936	002070	004537	002624		BR6:	JSR R5,@#REW ;DO A REWIND GET TO B.O.T.
937	002074	004537	002654		BR6C:	JSR R5,@#ETS ;CHECK FOR END OF TAPE ANYWAY
938	002100	005037	164002			CLR @#TRSTAT ;CLEAR THE INHIBIT BIT
939	002104	005037	164004			CLR @#TRWC ;CLEAR THE WORD COUNT
940	002110	012737	000017	164000		MOV #17,@#TRCOM ;DO AN ERASE
941	002116	005037	164000		BR6A:	CLR @#TRCOM ;FORCE A LOAD PULSE
942	002122	105737	177570			TSTB @#SWR ;SEE IF WE WANT TO LOOP
943	002126	100004				BPL BR6B ;ALL DONE
944	002130	105737	164000			TSTB @#TRCOM ;SEE IF ERASE IS DONE YET
945	002134	100370				BPL BR6A ;NOT DONE DO ANOTHER LOAD PULSE
946	002136	000756				BR BR6C ;DO IT AGAIN
947	002140	004537	002502		BR6B:	JSR R5,@#PCL ;DO A CLEAR AND EXIT
948	002144	000137	001510			JMP @#BR1 ;GO BACK TO MAIN

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002150 004537 002654
002154 004537 002570
002160 005037 164002
002164 012737 000017
002172 012700 005000
002176 012701 000004
002202 005300
002204 001376
002206 005301
002210 001374
002212 005037 164004
002216 105737 177570
002222 100763
002224 004537 002502
002230 000137 001510

164000

BR10:
BR10A:
BR10B:

JSR R5,@#ETS
JSR R5,@#OFLP
CLR @#TRSTAT
MOV #17,@#TRCOM
MOV #5000,R0
MOV #4,R1
DEC R0
BNE BR10B
DEC R1
BNE BR10B
CLR @#TRWC
TSTB @#SWR
BMI BR10A
JSR R5,@#PCL
JMP @#BR1

:CHECK FOR E.O.T.
:GET US OFF LOAD POINT
:CLEAR INHIBIT
:DO A MAXIMUM ERASE
:SET UP COUNTER
:SET TIMING LOOP MULTIPLIER
:START COUNTDOWN
:TIMER IS TICKING
:ONCE THROUGH TIMING LOOP
:REPEAT LOOP IF MULTIPLIER IS NON ZERO
:RE ESTABLISH THE ERASE COUNT TO 0
:SEE IF WE LOOP HERE
:DO IT AGAIN
:DO A POWER CLEAR
:GET OUT AND GET THE NEXT DELAY DIRECTIVE

* ROUTINE FOR DELAY 10 *

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* ROUTINE FOR DELAY 11 AND 12 *

```

975
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980 002234 004537 002624 BR11: JSR R5,@REW ;DO A REWIND
981 002240 012737 000033 164000 MOV #33,@TRCOM ;WRITE AN I.D.B.
982 002246 004537 002522 JSR R5,@RDY ;CHECK FOR DONE
983 002252 004537 002540 JSR R5,@ERCK ;SEE IF ANY ERRORS UP
984 002256 105737 177570 TSTB @SWR ;SEE IF WE WANT TO LOOP
985 002262 100764 BMI BR11 ;LOOP BACK DO IT AGAIN
986 002264 004537 002502 JSR R5,@PCL ;DO A POWER CLEAR
987 002270 000137 001510 JMP @BR1 ;GET OUT AND GET NEXT DELAY DIRECTIVE

```

* ROUTINE FOR DELAY 16 *

```

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996
997 002274 105737 164002 BR14: TSTB @TRSTAT ;CHECK FOR EOT UP
998 002300 100407 BMI BR14A ;SKIP THE FAST FORWARD
999 002302 005037 164002 CLR @TRSTAT ;CLEAR INHIBIT
1000 002306 012737 000027 164000 MOV #27,@TRCOM ;DO A FAST FORWARD
1001 002314 004537 002522 JSR R5,@RDY ;WAIT TILL DONE
1002 002320 005037 164002 BR14A: CLR @TRSTAT ;CLEAR INHIBIT
1003 002324 012737 000027 164000 MOV #27,@TRCOM ;TRY A FAST FORWARD ,SHOULD PPODUCE ERROR
1004 002332 004537 002522 JSR R5,@RDY ;WAIT TILL DONE
1005 002336 105737 177570 TSTB @SWR ;SEE IF WE LOOP HERE
1006 002342 100766 BMI BR14A ;YES LOOP HERE
1007 002344 004537 002502 JSR R5,@PCL ;DO A POWER CLEAR
1008 002350 000137 001510 JMP @BR1 ;GET OUT DO NEXT DELAY
1009

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002502 052737 004000 164000
002510 032737 004000 164000
002516 001374
002520 000205

002522 105737 164000
002526 100375
002530 042737 000001 164002
002536 000205

002540 005737 164000
002544 100010
002546 012737 000007 177566
002554 105737 177564
002560 100375
002562 004537 002502
002566 000205

.....
PCL:
PCL1:
.....
RDY:
IHB:
.....
ERCK:
ERCK1:
ERCK2:
:

```
*****
* SUBROUTINE FOR POWER CLEAR *
*****
BIS #4000,@#TRCOM ;SET POWER CLEAR
BIT #4000,@#TRCOM ;WAIT FOR 900 MILI SECONDS
BNE PCL1 ;STILL WAITING
RTS R5 ;RETURN TO MAIN ROUTINE
```

* SUBROUTINE FOR READY AND CLEAR INHIBIT *

```
TSTB @#TRCOM ;CHECK ON DONE BIT
BPL RDY ;WAIT TILL DONE
BIC #1,@#TRSTAT ;CLEAR THE INHIBIT BIT
RTS R5 ;RETUN TO MAIN ROUTINE
```

* SUBROUTINE TO CHECK FOR ERRORS *

```
TST @#TRCOM ;SEE IF ERROR IS UP
BPL ERCK2 ;NO ERRORS JUMP OUT
MOV #7,@#TTBUF ;GOT AN ERROR RING A BELL
TSTB @#TTSTAT ;WAIT HERE
BPL ERCK1 ;WAIT HERE
JSR R5,@#PCL ;CLEAR THE ERROR WITH A POWER CLEAR
RTS R5 ;GO BACK TO MAIN
```

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1085 002570 032737 000040 164002 OFLP: BIT #40,@#TRSTAT ;SEE IF LOAD POINT IS UP
1086 002576 001411 BEQ OFLP1 ;NO LP JUMP OUT
1087 002600 005037 164002 CLR @#TRSTAT ;CLEAR THE INHIBIT
1088 002604 012737 000033 164000 MOV #33,@#TRCOM ;WRITE AN I.D.B.
1089 002612 004537 002522 JSR R5,@#RDY ;WAIT FOR READY
1090 002616 004537 002540 JSR R5,ERCK ;CHECK FOR ERRORS
1091 002522 000205 OFLP1: RTS R5 ;GO BACK TO MAIN
1092
1093
1094
1095
1096
1097
1098
1099 002624 032737 000040 164002 REW: BIT #40,@#TRSTAT ;AT LOAD POINT??
1100 002632 001007 BNE REW2 ;YES DON'T NEED REWIND
1101 002634 005037 164002 REW1: CLR @#TRSTAT ;CLR THE INHIBIT
1102 002640 012737 000021 164000 MOV #21,@#TRCOM ;DO A REWIND
1103 002646 004537 002522 JSR R5,@#RDY ;WAIT TILL DONE
1104 002652 000205 REW2: RTS R5 ;GO BACK
1105
1106
1107
1108
1109
1110 002654 105737 164002 ETS: TSTB @#TRSTAT ;IS END OF TAPE UP ?
1111 002660 100002 BPL ETS1 ;NOT AT E.O.T.
1112 002662 004537 002624 JSR R5,@#REW ;DO A REWIND
1113 002666 000205 ETS1: RTS R5 ;GET BACK
1114
1115
1116

```

```

*****
* SUBROUTINE TO GET OFF LOAD POINT LEGALLY *
*****

```

```

*****
* SUBROUTINE FOR REWIND AND L.P. *
*****

```

```

*****
* SUBROUTINE FOR E.O.T. *
*****

```


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000001

* WRITE BUFFER PATTERNS *

.=2700
.REPT 1000 ;ALL 1'S
.WORD 000777 ;PATTERN = 0 000 000 111 111 111
.ENDR

.=3700
.REPT 1000 ;1'S AND 0'S ALTERNATE WORDS
.WORD 000400 ;PATTERN = 0 000 000 100 000 000
.WORD 000777 ;PATTERN = 0 000 000 111 111 111
.ENDR

.=4700
.REPT 1000 ;ALTERNATE BITS
.WORD 000525 ;PATTERN = 0 000 000 101 010 101
.WORD 000652 ;PATTERN = 0 000 000 110 101 010
.ENDR

.=5700
.REPT 1000 ;SLIDING 1 BIT
.WORD 000001 ;PATTERN = 0 000 000 000 000 001
.WORD 000002 ;PATTERN = 0 000 000 000 000 010
.WORD 000004 ;PATTERN = 0 000 000 000 000 100
.WORD 000010 ;PATTERN = 0 000 000 000 001 000
.WORD 000020 ;PATTERN = 0 000 000 000 010 000
.WORD 000040 ;PATTERN = 0 000 000 000 100 000
.WORD 000100 ;PATTERN = 0 000 000 001 000 000
.WORD 000200 ;PATTERN = 0 000 000 010 000 000
.WORD 000400 ;PATTERN = 0 000 000 100 000 000
.ENDR

* READ BUFFER AREA *

.=6700 ;1000 WORD LOCATIONS RESERVED FOR READ BUFFER
.END

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CROSS REFERENCE TABLE -- USER SYMBOLS

NORST	000356	550*	585	587*	590#													
OFLP	002570	920	956	1021	1085#													
OFLP1	002622	1086	1091#															
OPDEL	001352	775	789#															
OPDLX	000716	626#	789															
OPDLY	000714	625#	790															
OPNUM	000720	627#	665															
OPTBL	000722	633#	673															
PASHLT	001432	804#																
PCL	002502	875	900	947	968	986	1007	1032	1035	1046#	1075							
PCL1	002510	1047#	1048															
PSW =	177776	513#	662*	832*														
R	001144	713#																
RADDR	000706	622#	743															
RDY	002522	907	910	925	982	1001	1004	1019	1058#	1059	1089	1103						
READ	001220	713	743#															
REST	001434	803	805#															
REW	002624	936	980	1015	1020	1099#	1112											
REWD	001152	716#																
REW1	002634	1101#																
REW2	002652	1100	1104#															
SGOB	001162	727#	745	747														
SLB	000302	574#	582															
SLBDON	000334	580	585#															
SLB1	000310	577#	584															
SR	001146	714#																
START	001000	589	661#	805														
STEM	000672	616#	767*															
SUBSTK	000500	597#																
SWR =	177570	514#	795	802	835	882	898	912	927	942	966	984	1005	1033				
SWRTEM	000664	613#	835*	836	838*	839*	840*	841										
TABLE	001546	851#																
TEMP1	000674	617#	674*	679*														
TEMP2	000676	618#	676*	677	688	727*	728*	729*	730*	756	771*	772	778*	779				
TIMPUL	000666	614#	789*	793*														
TRBA =	164006	506#	741*	743*	923*	1023*												
TRCOM =	164000	503#	663	691*	692	756*	757	768	833	909*	924*	940*	941*	944				
		958*	981*	1000*	1003*	1018*	1025*	1046*	1047	1058	1070	1088*	1102*					
TRSTAT =	164002	504#	702*	767	892*	895*	921*	938*	957*	997	999*	1002*	1016*	1024*				
		1060*	1085	1087*	1099	1101*	1110											
TRWC =	164004	505#	744*	746*	908*	922*	939*	965*	1017*	1022*								
TTBUF =	177566	522#	1072*															
TTSTAT =	177564	521#	1073															
UNIT	000702	620#	666*	728														
UNUM	001026	666#																
W	001142	712#																
WADDR	000710	623#	741	923														
WCNT	000704	621#	744															
WRITE	001210	712	741#															
WR1WC	001226	742	744#															
WTM	001160	719#																
X1	000240	560#																
X2	000244	561#	573															
X3	000250	562#	567															
X4	000264	564	568#															
.	= 002670	536#	541	548#	596#	601#	612#	660#	714	796	800	829#						

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CROSS REFERENCE TABLE -- USER SYMBOLS

. ABS. 002670 000

ERRORS DETECTED: 0

CZTRBD/1,CZTRBD,SEQ/CRF/SOL/NL:TOC=CZTRBD.P11
RUN-TIME: 1 2 .2 SECONDS
RUN-TIME RATIO: 6/4=1.4
CORE USED: 16K (31 PAGES)