

LPA11

LPA/KW11-K TEST
CRLPGCO

AH-B038C-MC
FICHE 1 OF 1

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Identification

SEQ 0001

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1.0 ABSTRACT

SEQ 0003

"C" VERSION OF THE PROGRAM IS DUE TO A CHANGE IN THE MICRO-CODE IN THE LPA-11 (DMC-11).

"B" VERSION OF THE PROGRAM FIXES LS210 THRU LS230 PROGRAM BUGS AND SEVERAL DOCUMENTATION ERRORS.

This program allows the user to check out or debug the KW11K, DUAL REAL TIME CLOCK. The logic test is self contained and needs no external maintenance hardware or operator intervention.

Five special tests are included within this program to allow the user to check out and debug the external I/O signals. To run these tests a jumper wires is needed in order to loop output to an input.

THIS PROGRAM IS A MODIFIED VERSION OF "MD-11-DZWK-A". IT WAS MODIFIED TO ENABLE THE OPERATOR TO CHECK OUT THE KW11K OPTION WHEN IT IS ON THE LPA11-KX I/O BUS. NO RECABLING IS NEEDED. SOME TEST DONE IN THE ORIGINAL DIAGNOSTIC SUCH AS ARBITRATION TEST, WERE DELETED AS THEY COULD NOT BE CHECKED. IF THIS DIAGNOSTIC DOESN'T FIND A SUSPECTED PROBLEM, YOU MAY HAVE TO RUN "MD-11-DZWK-A". YOU SHOULD RUN "MD-11-CRLPA" BEFORE RUNNING THIS DIAGNOSTIC. PLEASE READ SECTION 10.

2.0 REQUIREMENTS

2.1 Equipment

1. PDP11 FAMILY COMPUTER with 16K of memory or more and I/O facilities (a switch register or TTY).
2. KW11K under test installed in the LPA-11KX.
3. For external I/O signal tests a loopback wire (Jumper) is needed. Jumpers are 30 AWG jumper type 915.
4. LPA11-KX

2.2 Storage

This program occupies and uses only the lower 16K of memory.

3.0 LOADING PROCEDURE

SEQ 0004

3.1 Method

Standards procedure for normal binary tapes should be followed.

1. Absolute loader must be in memory.
2. Place binary tape in reader.
3. Load address *7500 (* determined by location of loader).
4. Press "Start" (program will be loaded into memory).

The program can also be loaded by XXDP, ACT, or APT.

3.2 Non-Standard Address, Vector, or Priority; or Use of Software Switch Register

This program is set to test a KW11K with a standard address, vector, and priority. If any of these are different on the KW11K you are testing, change the corresponding location in memory before starting this test.

LOCATION	TAG	CURRENT CONTENTS	COMMENTS
1254	\$BASE:	170404	;:Base address of equipment ;: under test
1250	\$VECT1:	000344	;:INTERRUPT Vector #1
1252	\$PRIOR:	000006	;:Bus priority - 1,#2
176	\$SWREG:	000000	;:Manual SWR.
	\$TPFLG:	.BYTE 0	;:"Terminal Available" ;: Flag (Bit<0:7>=0=Yes)

NOTE

If no hardware Switch Register exists,
you may set any bit in "SWREG" as you
would have set it in the SWR.

4.0 STARTING PROCEDURE

4.1 Control Switch Settings

Starting at memory locations 200, 204, 210, 214, 220, 224, 230 or 234, set all switches as desired. See Section 5.1.

4.2 Starting Addresses

- 200 Start address for logic test.
- 204 Restart address for logic test.
- 210 Start address for "STP2 OUT", "SCHMITT TRIG 1" tests.
- 214 Start address for "STP1 OUT", "SCHMITT TRIG 2" tests.
- 220 Start address for "SCHMITT TRIG 3 IN", "ST3 OUT" tests.
- 224 Starting address for 'A EVENT OUT' test.
- 230 Starting address for 'B EVENT OUT' test.
- 234 Starting address for 'USER LINK' loop.

4.3 Program AND/OR Operator Action

1. Load program into core.
2. Set switch register to starting address.
3. Load address.
4. Set switches to deisred settings - see section 5.1.
5. IF starting a special I/O signal test:
MAKE WIRE LOOP CONNECTION.
6. Press Start.

5.0 OPERATING PROCEDURE

5.1 Switch Register Function

Switch use

```
15 Halt on error
14 Loop on test
13 Inhibit error typeout (all tests)
13 Inhibit "*" typeout (special I/O signal tests)
10 Bell on error
 9 Loop on error
 8 Loop on test in SWR <7:0>
```

5.2 Scope Loops

If an error occurs and the user wishes to scope the error, he (or she) should set SW15=1 to halt on error, then when the program halts on error, SW15=0, set SW14=1. To loop on current test, set SW13=1 to inhibit error printout, and press continue on the CPU's console.

NOTE

For each test in the listing, you will find a test description. In each description a probable SYNC Point is listed. These Points are listed AS A GUIDE in order for you to SYNC your scope to the Signals being generated.

5.3 Program AND/OR Operator Action

5.3.1 Logic Test

For each pass through the program "END PASS" will be printed out at the end of a pass.

If not inhibited by APT, the program will look for more KW11Ks to exercise, one pass will exercise all KW11Ks.

5.3.2 Special I/O Signal Tests

There are no "Short Passes". Each pass will iterate 65,324 times. A "*" is typed at the end of a pass unless SWR13=1.

6.0 ERRORS

SEQ 0007

6.1 Error Printout

Printout varies with the error detected. The error PC typed out is the actual location of the error call.

A halt at location "\$TYPE"+10 when running with no terminal indicates an error has occurred. To find out the number of the error, examine location "\$STSTNM". This is the item number of the error. To find out what the error typout would have been GOTO to the error pointer table beginning at location "\$ERRTB".

6.1.1 Example

If we examined location "\$STSTNM" and found a 5 (101) we go to location "\$ERRTB" and look through the error pointer table until we found item 5. The information would look like:

;ITEM 5

EM5	:CLOCK B SR DATA ERROR
DHS	:ERRPC BSR WAS S/B
DT5	:\$ERRPC,BSR,\$BDDAT,\$GDDAT
DFO	:ALL NUMBERS ARE IN OCTAL FORM

To find out the information specified by DT5 (\$ERRPC,BSR,\$GDADR,\$BDADR) follow these steps:

1. Look up the address of the label (i.e., \$ERRPC) in the symbol table which follows the listing.
2. Put this address in the watch register and depress the load address switch on the processor's console.
3. Now depress the Examine switch.
4. The data displayed in the data lights is the information that would have been printed for his label if you had a input/output terminal.

6.2 Non-Standard Error HALTS

A HALT MAY OCCUR IF THE PROGRAM DETECTS AN LPA11-KX ERROR.
CHECK THE COMMENTS IN THE LISTING OPPOSITE THE PC HALT.

7.0 RESTRICTIONS

Jumper W2 must be installed if not jumpered on module.
JUMPER W3, W4, AND W5 MUST BE INSTALLED TO RUN SIGNAL TESTS.

Logic Test must be run before any special I/O Signal Test.

The program is chainable under XXDP. However only one pass may
be made (R RLPGC0/1).

8.0 MISCELLANEOUS

After a power failure occurs, program execution will NOT continue at
the point where the power failure occurred.
The program will be restarted.

This program is chainable under XXDP, ACT, or APT.

Logic Test

90 SECONDS if no errors.

8.3.2 Special I/O Signal Tests

1.0 Minutes No errors, SW13=0.

Execution times are approximate, as the various PDP-11 CPU's have
varied instruction execution times.
Times quoted were taken from a run on a PDP-11/34.

8.4 USER LINK TO I/O DEVICE

A SPECIAL USER LINK HAS BEEN PROVIDED IN ORDER FOR THE OPERATOR TO EXAMINE OR MODIFY LOCATIONS ON THE LPA11-KX I/O BUS. (NOTE: THIS CANNOT BE DONE DIRECTLY.)

PROCEDURE:

- 1) START THE PROCESSOR AT LOCATION 234
- 2) THE DIALOG TO EXAMINE A LOCATION IS AS FOLLOWS:

E OR D "E"
DEVICE ADDRS= "OCTAL ADDRS"
XXXXXX

WHERE XXXXXX IS THE CONTENTS OF THE SPECIFIED LOC.

- 3) THE DIALOG TO MODIFY A LOCATION IS AS FOLLOWS:

E OR D "D"
DATA= "DATA TO BE DEPOSITED"

- 4) THE PROGRAM WILL STAY IN THIS LOOP UNTIL THE OPERATOR IS FINISHED. AT THIS TIME THE PROCESSOR SHOULD BE HALTED.

NOTE: THE OPERATORS RESPONSE IS ENCLOSED IN QUOTES.

9.0 PROGRAM DESCRIPTION

9.1 Logic Tests

A complete description of each test is included withing the listing before each test.

9.2 Special External I/O Signal Tests

9.2.1 LS210 "STP2 OUT" to "SCHMITT RIG 1 IN" Tests

This is a special section devoted for testing and providing scope loop capabilities for "STP2 OUT" L and "SCHMITT TRIG 1" IN.

When you load and start at location 210, program control is transferred here. "STP2 OUT" L pulses are generated by "LO STAT A HI" H + "BD10" H (Main. STP2).

Pin V ("STP2 OUT") is wired to pin LL (SCHMITT TRIG1) for this test. "STP2 OUT" pulses are received as "SCHMITT TRIG 1" pulses which set clock A's status register bit 15. If an error is detected, normal error reporting technique. and error switch register options are used. An "*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins V and LL of J1 together.
Jumper W3 must be INSTALLED.

Logic test (L + S 200) should be run first.

9.2.2 LS214 "STP1 OUT" to "SCHMITT RIG 2" H Tests

This is a special test section devoted for testing and providing scope loop capabilities for "STP2 OUT" and "SCHMITT TRIG2" IN.

When you load and start at location 214, program control is transferred here. "STP1 OUT" L pulses are generated by "LD STAT A HI" + "BD12" H (mIn S). Pin DD ("STP1 OUT") is wired to pin BB ("SCHMITT TRIG 2") for this test. "STP1 OUT" pulses are received as "SCHMITT TRIG 2" pulses which will clear clock A's count register if mode 3 is selected. If an error is detected, normal error reporting technique. and error switch register options are used. An "*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins DD and BB of J1 together.
Jumper W4 must be installed.

Logic tests (L + S at 200) should be run first.

9.2.3 LS220 "SCHMITT TRIG 3" in, "ST3 OUT" Tests

This is a special section devoted for testing and providing scope loops capabilities for "SCHMITT TRIG 3" AND "ST3 OUT".

When you load and start at location 220, program control is transferred here. "STP1" pulses are generated by "LD STAT A H," + "BD12" H (main STP1). Pin dd ("STP1 OUT") is wired to pin T ("SCHMITT TRIG 3"). "SCHMITT TRIG 3" pulses give us "ST3 OUT" pulses. Pin L ("ST3 OUT") is wired to pin BB ("SCHMITT TRIG2"), and "SCHMITT TRIG 2" will set clock A's status register bit 7.

If an error is detected, normal error reporting technique. and error switch register options are used. An "*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins DD to T of J1 together, as well as pins L to BB of J1 together. Jumpers W4 and W5 must also be installed.

Tests LS210 and LS214 should be run first.

9.2.4 LS224 "A EVENT OUT" Test

This is a special section devoted for testing and providing scope loop capabilities for "A EVENT OUT".

When you load and start at location 224, program control is transferred here. "A EVENT OUT" pulses are generated by clock A overflows. Pin VV ("A EVENT OUT") is wired to pin BB ("SCHMITT TRIG 2"). "SCHMITT TRIG 2" pulses will set clock A's CSR bit 7. If an error is detected, normal error reporting technique. and error switch register options are used. An "*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins VV and BB of J1 together. Jumper W4 must also be installed.

Test LS210 should be run first.

9.2.5 LS230 "B EVENT OUT" Test

This is a special section devoted for testing and providing scope loop capabilities for "B EVENT OUT".

When you load and start at location 230, program control is transferred here. "B EVENT OUT" pulses are generated by clock B overflows. Pin TT ("B EVENT OUT") is wired to pin BB ("SCHMITT TRIG 2"). "SCHMITT TRIG 2" pulses will set clock A's CSR bit 7. And error switch register options are used. An "+" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins TT and BB of J1 together. Jumper W4 must be installed also.

Test LS210 should be run first.

10.0 LPA11 (SYSTEM) DIAGNOSTIC SUMMARY

DIAGNOSTICS FOR THE LPA11 ARE WRITTEN AT THREE LEVELS: (1) TOTAL PDP-11 SYSTEM, (2) LPA11 SYSTEM; AND, (3) LPA11 OPTIONS.

LEVEL 1, IS DESIGNED TO ISOLATE A FAILURE TO THE LPA11 SYSTEM. ALL OPTIONS ON THE PDP-11 ARE EXERCISED.

LEVEL 2 DIAGNOSTICS ISOLATE A FAILURE TO THE INDIVIDUAL OPTION WITHIN THE LPA11. THE LEVEL 2 DIAGNOSTIC IS MD-11-DRLPA. WHEN THE USER RUNS DRLPA HE CAN GENERALLY TELL WHICH OPTION DIAGNOSTIC (LEVEL 3) TO RUN NEXT. M8254 AND M8200-YC ERRORS MAY "LOOK" ALIKE AND DRLPA MAY NOT BE ABLE TO DISTINGUISH BETWEEN THEM. ARBITRATION ERRORS WILL NOT BE DETECTED BY THIS DIAGNOSTIC.

LEVEL THREE DIAGNOSTICS AID IN DETERMINING IF THE ERROR WAS IN FACT ON THE OPTION THE DRLPA SPECIFIED. THE USER MAY "LOOP" ON THE ERROR. WITHIN LEVEL THREE, THERE ARE TWO GROUPS OF DIAGNOSTICS. THE FIRST GROUP REQUIRES NO "EXTRA" WORK BY THE USER IN ORDER TO RUN. GROUP "A" DIAGNOSTICS DO NOT CHECK ARBITRATION, AND REQUIRE EXTRA TIME FOR EXECUTION. THE SECOND GROUP (GROUP 'B') REQUIRES THAT THE USER RECONFIGURE THE PDP-11 SYSTEM. THIS RECONFIGURATION INVOLVES CABLING THE UNIBUS TO THE LPA'S I/O BUS.

THE DIAGNOSTIC FOR THE M8254 FALLS INTO THE GROUP 'B' CATALOGY.

THE LPA11-KX DIAGNOSTIC KIT WILL INCLUDE:

SEQ 0013

OPTION -----	GROUP -----	DIAG. # -----	DIAG. TITLE
LPA11-KX	LEVEL 2	MD-11-CRLPA	LPA11-K SYSTEM EXER.
M8254	"B"	MD-11-CRLPM	M8254 (IPBM) FIELD DIAG.
AA11-K	A	MD-11-CRLPB	LPA/AA11-K DIAG.
	B	MD-11-DZAAC	AA11-K DIAG.
AR11	A	MD-11-CRLPC	LPA/AR11 DIAG. #1
	A	MD-11-CRLPD	LPA/AR11 DIAG. #2
	A	MD-11-CRLPE	LPA/AR11 DIAG. #3
	B	MD-11-DZARA	AR11 DIAG. #1
	B	MD-11-DZARB	AR11 DIAG. #2
	B	MD-11-DZARC	AR11 DIAG. #3
DR11-K	A	MD-11-CRLPF	LPA/DR11-K DIAG.
	B	MD-11-DZDRG	DR11-K DIAG.
KW11-K	A	MD-11-CRLPG	LPA/KW11-K DIAG.
	B	MD-11-DZKWK	KW11-K DIAG.
LPS-11	A	MD-11-CRLPH	LPA/LPS11 DIAG. #1
	A	MD-11-CRLPI	LPA/LPS11 DIAG. #2
	A	MD-11-CRLPJ	LPA/LPS11 DIAG. #3
	B	MD-11-DZLPC	LPS11 DIAG. #1
	B	MD-11-DZLPD	LPS11 DIAG. #2
	B	MD-11-DZLPI	LPS11 DIAG. #3
AD11-K	A	MD-11-CRLPK	LPA/AD11-K DIAG.
	B	MD-11-DZADL	AD11-K DIAG.
M8200-YC	B	MD-11-CRLPL	LPA/DMC-11 DIAG. TST I
	B	MD-11-CRLPM	LPA/DMC-11 DIAG. TST II

THIS IS A HISTORY FILE OF CRLPG-C

THE "C" VERSION SOURCE ONLY HAS THE B TO C VERSION CHANGES
THE BIG CHANGE IS IN THE "CRLPA.MAC" FILE THAT HANDLES THE
NEW VERSION OF THE MICRO-CODE IN THE LPA-11

THE "A" VERSION HAD SEVERAL PROBLEMS WHEN DEALING WITH LS204
AND LS210 THRU LS230. THE FIRST WAS THAT LS204 FAILED TO CLEAR
A LOCATION ".DVLS", WHICH INDICATED THE MICRO-CODE WAS LOADED
AND RUNNING <AFTER A RESTART IS IS NOT RUNNING DUE TO "INIT">.
THIS PROBLEM IS ALSO COMMON TO LS210 THRU LS230.
THE SECOND PROBLEM IS THAT LS210 HAD A DESIGN FLAW <REALLY ONLY A
ONE LINE TYPING REVERSAL>

JAN 1979 R. SHOOP

HISTORY FILE OF DRLPG-A

PRODUCT CODE: MAINDEC-11-DZWK-A
PRODUCT NAME: KW11-K DIAGNOSTIC TEST
DATE: FEBRUARY 1976
MAINTAINER: DIAGNOSTIC GROUP

PRODUCT CODE: MAINDEC-11-DRLPG-A
PRODUCT NAME: LPA/KW11-K DIAGNOSTIC TEST
DATE: JANUARY 1978
MAINTAINER: DIAGNOSTIC GROUP

REASON FOR DEVELOPMENT:

- 1) TO ENABLE THE OPERATOR TO CHECK OUT THE KW11-K OPTION
WHEN IT IS ON THE LPA11-KX I/O BUS.

CHANGES MADE:

- 1) TOOK OUT CERTAIN TESTS FROM ORIGINAL DIAGNOSTIC (I.E.
INTERRUPTS, TIME DEPENDENT CODE).
- 2) REPLACED DIRECT LINKS TO DEVICE WITH MACRO CALLS TO THE
KMC-11 MICRO CODE. KMC-11 MICRO CODE (FILE:DRLPX2) HANDLES
DIRECT COMMUNICATIONS WITH THE DEVICE.

FILE: DRLPA.MAC
CONTAINS MACRO LINKS BETWEEN PDP-11 CODE AND KMC-11
MICRO CODE. FILE: DRLPX2 NEEDS TO BE ASSEMBLED WITH
DRLPG (SEE .CTL FILE).

FILE: DRLPX2
MICRO CODE FILE THAT GETS LOADED INTO THE KMC-11
VIA ROUTINES IN DRLPA.MAC.
DRLPX2.P11 IS ASSEMBLED WITH MACY11 (ONLY) AS ANY OTHER
.P11 FILE. THE RESULTS OF ITS ASSEMBLY IS A .OBJ
MODULE AS WAS THE RESULT OF THE ASSEMBLY OF THE
DIAGNOSTIC .P11 FILE. BOTH .OBJ FILES GET LINKED
WITH LNKX11 (ONLY).

FILE: DRLPG.CTL
THIS FILE EXPLAINS SEQUENCE OF ASSEMBLES AND LINKS.
IT IS IN TOPS-20 FORMAT.

LNKX11 V023 24-OCT-80 9:45

#CRLPGC.BIN/B:42000,CRLPGC.MAP=CRLPGC,CRLPX2/E

LOAD MAP

IDENT: V1015B

TRANSFER ADDRESS: 000001

LOW LIMIT: 042000

HIGH LIMIT: 046000

MODULE LPA

SECTION ENTRY	ADDRESS	SIZE
<. ABS.>	000000	000000
DRLPX2	042000	
< >	042000	000000

MODULE DRLPX2

SECTION ENTRY	ADDRESS	SIZE
< >	042000	000000
<ABCODE>	042000	004000

RUN-TIME: 1 SECONDS

2K CORE USED

1208 OPERATIONAL SWITCH SETTINGS
1209 TRAP CATCHER
1220 BASIC DEFINITIONS
1275 ACT11 HOOKS
1277 APT PARAMETER BLOCK
1279 COMMON TAGS
(2) APT MAILBOX-ETABLE
(1) ERROR POINTER TABLE
1440 PROGRAM START
1444 INITIALIZE THE COMMON TAGS
1489 *
1490 * PHASE 1CLOCKS A+B BASIC LOGIC TESTS.
1491 *
1518 T1 *TEST THAT ADDRESSABILITY OF CLOCK ADDRESS
1542 T2 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN INTO
1571 T3 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN TO A ZERO
1604 T4 *TEST THAT CLOCK A'S STATUS CAN BE WRITTEN AND READ
1630 T5 *TEST THAT CLOCK B'S STATUS REGISTER CAN BE WROTE/READ
1655 T6 *TEST THAT CLOCK B'S BUFFER REGISTER CAN BE WROTE/READ
1778 T7 *TEST THAT CLOCK A STATUS REGISTER BIT 15 CAN BE SET AND CLEARED
(5) T10 *TEST THAT CLOCK A STATUS REGISTER BIT 14 CAN BE SET AND CLEARED
(5) T11 *TEST THAT CLOCK A STATUS REGISTER BIT 13 CAN BE SET AND CLEARED
(5) T12 *TEST THAT CLOCK A STATUS REGISTER BIT 9 CAN BE SET AND CLEARED
(5) T13 *TEST THAT CLOCK A STATUS REGISTER BIT 8 CAN BE SET AND CLEARED
(5) T14 *TEST THAT CLOCK A STATUS REGISTER BIT 7 CAN BE SET AND CLEARED
(5) T15 *TEST THAT CLOCK A STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(5) T16 *TEST THAT CLOCK A STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
(5) T17 *TEST THAT CLOCK A STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(5) T20 *TEST THAT CLOCK A STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
(5) T21 *TEST THAT CLOCK A STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
(5) T22 *TEST THAT CLOCK A STATUS REGISTER BIT 0 CAN BE SET AND CLEARED
(6) T23 *TEST THAT CLOCK A BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(6) T24 *TEST THAT CLOCK A BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(6) T25 *TEST THAT CLOCK A BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(6) T26 *TEST THAT CLOCK A BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
(6) T27 *TEST THAT CLOCK A BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(6) T30 *TEST THAT CLOCK A BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(6) T31 *TEST THAT CLOCK A BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
(6) T32 *TEST THAT CLOCK A BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED
(6) T33 *TEST THAT CLOCK A BUFFER REGISTER BIT 8 CAN BE SET AND CLEARED
(6) T34 *TEST THAT CLOCK A BUFFER REGISTER BIT 9 CAN BE SET AND CLEARED
(6) T35 *TEST THAT CLOCK A BUFFER REGISTER BIT 10 CAN BE SET AND CLEARED
(6) T36 *TEST THAT CLOCK A BUFFER REGISTER BIT 11 CAN BE SET AND CLEARED
(6) T37 *TEST THAT CLOCK A BUFFER REGISTER BIT 12 CAN BE SET AND CLEARED
(6) T40 *TEST THAT CLOCK A BUFFER REGISTER BIT 13 CAN BE SET AND CLEARED
(6) T41 *TEST THAT CLOCK A BUFFER REGISTER BIT 14 CAN BE SET AND CLEARED
(6) T42 *TEST THAT CLOCK A BUFFER REGISTER BIT 15 CAN BE SET AND CLEARED
(6) T43 *TEST THAT CLOCK B STATUS REGISTER BIT 11 CAN BE SET AND CLEARED
(6) T44 *TEST THAT CLOCK B STATUS REGISTER BIT 7 CAN BE SET AND CLEARED
(6) T45 *TEST THAT CLOCK B STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(6) T46 *TEST THAT CLOCK B STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
(6) T47 *TEST THAT CLOCK B STATUS REGISTER BIT 4 CAN BE SET AND CLEARED
(6) T50 *TEST THAT CLOCK B STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(6) T51 *TEST THAT CLOCK B STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
(6) T52 *TEST THAT CLOCK B STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
(6) T53 *TEST THAT CLOCK B STATUS REGISTER BIT 0 CAN BE SET AND CLEARED

(6) T54 *TEST THAT CLOCK B BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(6) T55 *TEST THAT CLOCK B BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(6) T56 *TEST THAT CLOCK B BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(6) T57 *TEST THAT CLOCK B BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
(6) T60 *TEST THAT CLOCK B BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(6) T61 *TEST THAT CLOCK B BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(6) T62 *TEST THAT CLOCK B BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
(6) T63 *TEST THAT CLOCK B BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED

1779 *

1780 * PHASE 2 ADVANCED BASIC LOGIC TESTS

1781 *

1789 T64 *TEST THAT CLOCK A'S COUNT REGISTER IS CLEAR
1812 T65 *TEST CLOCK A'S COUNT REGISTER WITH 125252 PATTERN
1840 T66 *TEST CLOCK A'S COUNT REGISTER WITH 052525 PATTERN
1874 T67 *TEST THAT CLOCK B'S COUNT REGISTER IS CLEAR
1898 T70 *TEST CLOCK B'S COUNT REGISTER WITH 125 PATTERN
1926 T71 *TEST CLOCK B'S COUNT REGISTER WITH 252 PATTERN
1968 T72 *TEST THE SETTING OF MAINTENANCE STP1 IN CLOCK A BIT 15 TO SET
1998 T73 *TEST THAT BIT00 IN CLOCK A STATUS REG. WILL SET WHEN BIT13 AND MAIN. STP1
2034 T74 *TEST THAT CLOCK A WILL INCREMENT - MODE 0 - RATE STP1 FIRST COUNT TEST
2083 T75 *TEST THE ABILITY OF CLOCK A TO COUNT FROM ZERO TO OVERFLOW USING M STP1'S

2130 *

2131 * PHASE 3 CLOCK A COUNT FUNCTION TESTS

2132 *

2144 T76 *TEST THAT CLOCK A OVERFLOW WILL OCCUR
2190 T77 *TEST IN CLOCK A THAT OVERFLOW IN MODE 0 CAUSE CLEARING OF "ENB CNTR" F/F
2281 T100 *TEST THE ABILITY OF CLOCK A TO COUNT AT 1MHZ RATE PART 1
2282 T101 *TEST THE ABILITY OF CLOCK A TO COUNT AT 100KHZ RATE PART 1
2283 T102 *TEST THE ABILITY OF CLOCK A TO COUNT AT 10KHZ RATE PART 1
2284 T103 *TEST THE ABILITY OF CLOCK A TO COUNT AT 1KHZ RATE PART 1
2285 T104 *TEST THE ABILITY OF CLOCK A TO COUNT AT 100HZ RATE PART 1
2286 T105 *TEST THE ABILITY OF CLOCK A TO COUNT AT LINE-FREQ RATE PART 1
2297 T106 *TEST THAT CLOCK A DOESN'T COUNT WHEN NO RATE IS SELECTED
2339 T107 *TEST THAT CLOCK A'S COUNT REG ISN'T LOADED WHEN CLOCK A IS ENABLED
2379 T110 *TEST THAT CLOCK A IN MODE 1 DOES NOT CLEAR ENABLE ON OVERFLOW
2418 T111 *TEST THAT A CLOCK A 'BUFFER TO COUNT REG' DOESN'T TAKE PLACE ON A MODE 2 OVERFLOW
2467 T112 *TEST THAT CLOCK A MODE 2 + MAINTENANCE ST2 SET MODE FLG
2548 T113 *TEST THAT PATTERN 052525 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
2549 T114 *TEST THAT PATTERN 125252 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
2593 T115 *TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 1 WHEN STP2 IS GENERATED
2594 T116 *TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 2 WHEN STP2 IS GENERATED
2607 T117 *TEST THAT MODE 3 + 'STP2' CLEARS A'S COUNT REGISTER.
2651 T120 *TEST THE AUTODECREMENT FEATURE OF CLOCK A'S BUFFER
2724 T121 *TEST THAT CLOCK A'S 1 MHZ CLK CAN BE DISABLED

2756 *

2757 * PHASE 4 CLOCK B COUNT FUNCTION TESTS

2758 *

2776 T122 *TEST THAT CLOCK B WILL COUNT ONCE FIRST CLOCK B COUNT
2827 T123 *TEST THE ABILITY IF CLOCK B TO COUNT FROM ZERO TO OVERFLOW
2893 T124 *TEST THAT CLOCK B CAN GENERATE AN OVERFLOW
2943 T125 *TEST THE INIT. ABILITY OF CLOCK B'S COUNT REG.
2968 T126 *TEST THAT CLOCK B DOESN'T COUNT WHEN NO RATE IS SELECTED
3048 T127 *TEST THE ABILITY OF CLOCK B TO COUNT AT 1MHZ PART 1
3049 T130 *TEST THE ABILITY OF CLOCK B TO COUNT AT 100KHZ PART 1
3050 T131 *TEST THE ABILITY OF CLOCK B TO COUNT AT 10KHZ PART 1
3051 T132 *TEST THE ABILITY OF CLOCK B TO COUNT AT 1KHZ PART 1

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3052 T133 *TEST THE ABILITY OF CLOCK B TO COUNT AT 100HZ PART 1
3053 T134 *TEST THE ABILITY OF CLOCK B TO COUNT AT LINE-FREQ PART 1
3064 T135 *TEST THE "FEED B TO A" 24 BIT COUNTER FEATURE OF CLOCKS A + B
3113 *
3114 * PHASE 6 CLOCK A+B ADVANCE TESTING
3115 *
3136 T136 *TEST THAT THE TRAILING EDGE OF STP1 WILL INCR. COUNTER
3258 T137 *TEST CLOCK A'S 100KHZ DIVIDER
3259 T140 *TEST CLOCK A'S 10KHZ DIVIDER
3260 T141 *TEST CLOCK A'S 1KHZ DIVIDER
3261 T142 *TEST CLOCK A'S 100HZ DIVIDER
3362 T143 *TEST CLOCK B'S 100KHZ DIVIDER
3363 T144 *TEST CLOCK B'S 10KHZ DIVIDER
3364 T145 *TEST CLOCK B'S 1KHZ DIVIDER
3365 T146 *TEST CLOCK B'S 100HZ DIVIDER
3393
3395 END OF PASS ROUTINE
3396 *
3397 * SPECIAL I/O SIGNAL TESTS
3398 *
3434 * "STP2 OUT" TO "SCHMITT TRIG 1 IN" TESTS
3484 :* "STP1 OUT" TO "SCHMITT TRIG 2" H TESTS
3538 * "SCHMITT TRIG 3" IN, "ST3 OUT" TESTS
3590 * "A EVENT OUT" TEST
3643 * "B EVENT OUT" TEST
3733
3734 *SYSMAC ROUTINES
3735
3737 BINARY TO OCTAL (ASCII) AND TYPE
3738 ERROR HANDLER ROUTINE
3739 ERROR MESSAGE TYPEOUT ROUTINE
3740 CONVERT BINARY TO DECIMAL AND TYPE ROUTINE
3741 SCOPE HANDLER ROUTINE
3742 READ AN OCTAL NUMBER FROM THE TTY
3743 TTY INPUT ROUTINE
3744 TYPE ROUTINE
3745 APT COMMUNICATIONS ROUTINE
3746 POWER DOWN AND UP ROUTINES
3751 TRAP DECODER
TRAP TABLE
(3)

1
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169
182
183
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417
458
510
609
651
698
747

.REM [

CRLPAB.MAC

WELCOME, THIS DIAGNOSTIC IS ONE IN A SERIES OF DIAGNOSTIC
DESIGNED IN ORDER TO AID YOU IN TESTING THE LPA-11XX OPTION.
I HOPE THAT YOU HAVE READ THE DOCUMENTATION SECTION OF THIS
DIAGNOSTIC. IF YOU HAVE, YOU KNOW ABOUT ALL OF THE DIAGNOSTICS
THAT ARE AVAILABLE FOR TESTING THE LPA SYSTEM.

GOOD LUCK !

[
.GLOBL DRLPX2

MMAST.MAC
CRLPAB.MAC 26-SEP-80 13:48

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SEQ 0020

763 .TITLE MMAST.MAC
764 .IDENT /4.01/
765
766 : LPA11-K MICRO CODE
767 :
768 : CHARLES A. SAMUELSON
769 : NOVEMBER, 1977
770 :
771
905 .TITLE DMASTER.MAC
906 .IDENT /4.01/
907
908 : LPA11-K MICRO CODE
909 :
910 : CHARLES A. SAMUELSON
911 : NOVEMBER, 1977
912 :
913 :
1047

1169
1170
1171 THIS IS A LIST OF TESTS DELETED FROM THIS DIAGNOSTIC.
1172 THESE TEST COULD NOT BE DONE THROUGH THE LPA-11.
1173
1174 TEST THE LOW BYTE OPERATION OF CLOCK A'S STATUS REGISTER
1175 TEST THE HIGH BYTE OPERATION OF A'S STATUS REGISTER
1176 TEST THE LOW BYTE OPERATION OF B'S STATUS REGISTER
1177 TEST THE HIGH BYTE OPERATION OF B'S STATUS REGISTER
1178 TEST THAT INIT CLEARS STATUS REGISTER A
1179 TEST THAT INIT CLEARS BUFFER REGISTER A
1180 TEST THAT INIT CLEARS STATUS REGISTER B
1181 TEST THAT INIT CLEARS BUFFER REGISTER B
1182 TEST THAT A'S COUNT REGISTER IS CLEARED BY INIT
1183 TEST THAT CLOCK A WILL INTR. AND TO THE RIGHT VECTOR
1184 TEST THAT CLOCK A WILL INTR. WHEN CPU PSW = CLK INTR LEV -1
1185 TEST THAT CLOCK A WILL NOT INTR. WHEN CPU PSW = CLK INTR LEVEL
1186 TEST THAT ST1 WILL CAUSE CLOCK A TO INTER.
1187 TEST THAT CLOCK A OVERFLOW WILL CAUSE AN INTR.
1188 TEST THAT A CLOCK A COUNTER BUFFER WILL CAUSES AN INTR.
1189 TEST THAT CLOCK B WILL INTR. AND TO THE RIGHT VECTOR
1190 TEST THAT CLOCK B WILL INTR. WHEN CPU PSW=CLK INTR LEV -1
1191 TEST THAT CLOCK B WILL NOT INTR. WHEN CPU PSW=CLK INTR LEVEL
1192 TEST THAT A CLOCKB OVERFLOW WILL CAUSE AN INTR.
1193 TEST CLOCK A'S REPEATABILITY AT 1MHZ RATE
1194 TEST CLOCK A'S REPEATABILITY AT 100KHZ RATE
1195 TEST CLOCK A'S REPEATABILITY AT 10KHZ RATE
1196 TEST CLOCK A'S REPEATABILITY AT 1KHZ RATE
1197 TEST CLOCK A'S REPEATABILITY AT 100HZ RATE
1198 TEST CLOCK B'S REPEATABILITY AT 1MHZ RATE
1199 TEST CLOCK B'S REPEATABILITY AT 100KHZ RATE
1200 TEST CLOCK B'S REPEATABILITY AT 10KHZ RATE
1201 TEST CLOCK B'S REPEATABILITY AT 1KHZ RATE
1202 TEST CLOCK B'S REPEATABILITY AT 100HZ RATE
1203 TEST THAT "INIT" CLEARS B'S 100KHZ DIVIDE BY 10 CHIPS
1204
1205
1206
1207 .TITLE LPA-KW11K DIAGNOSTIC MD-11-CRLPG-C
(1) :*COPYRIGHT (C) 1980
(1) :*DIGITAL EQUIPMENT CORP.
(1) :*MAYNARD, MASS. 01754
(1)
(1) :*PROGRAM BY EDWARD C. BADGER REV B BY R. SHOOP
(1)
(1) :*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
(1) :*PACKAGE (MAINDEC-11-DZQAC-C3), JAN 19, 1977.
(1)
(1) \$TN=1
1208 .SBTTL OPERATIONAL SWITCH SETTINGS
(1) :*
(1) :* SWITCH USE
(1) :* -----
(1) :* 15 HALT ON ERROR
(1) :* 14 LOOP ON TEST
(1) :* 13 INHIBIT ERROR TYPEOUTS

000001

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(1)          :*      10      BELL ON ERROR
(1)          :*      9       LOOP ON ERROR
(1)          :*      8       LOOP ON TEST IN SWR<7:0>
1209        .SBTTL TRAP CATCHER

(1)          0000000
(1)          .=0
(1)          ;*ALL UNUSED LOCATIONS FROM 4 - 776 CONTAIN A ".+2,HALT"
(1)          ;*SEQUENCE TO CATCH ILLEGAL TRAPS AND INTERRUPTS
(1)          ;*LOCATION 0 CONTAINS 0 TO CATCH IMPROPERLY LOADED VECTORS
(1)          .=174
(1) 000174 0000000
(1) 000176 0000000
1210        .WORD 0           ;;SOFTWARE DISPLAY REGISTER
(1)          SWREG: .WORD 0           ;;SOFTWARE SWITCH REGISTER
(1)          .=200
1211        000200 000137 001726
(1)          JMP    @#START        ;GO TO STARTING ADDRESS OF PROGRAM
1212
1213 000204 000137 002462
(1)          JMP    @#RSTART        ;GO TO RESTART ADDRESS.
1214 000210 000137 022450
(1)          JMP    @#LS210         ;GO TO SPECIAL TEST #1.
1215 000214 000137 022646
(1)          JMP    @#LS214         ;GO TO SPECIAL TEST #2.
1216 000220 000137 023062
(1)          JMP    @#LS220         ;GO TO SPECIAL TEST #3.
1217 000224 000137 023246
(1)          JMP    @#LS224         ;GO TO SPECIAL TEST #4.
1218 000230 000137 023454
(1)          JMP    @#LS230         ;GO TO SPECIAL TEST #5.

1219
1220        .SBTTL BASIC DEFINITIONS
(1)
(1)          001100
(1)          ;*INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***
(1)          STACK= 1100
(1)          .EQUIV EMT,ERROR      ;;BASIC DEFINITION OF ERROR CALL
(1)          .EQUIV IOT,SCOPE      ;;BASIC DEFINITION OF SCOPE CALL

(1)          ;*MISCELLANEOUS DEFINITIONS
(1)          000011   HT= 11          ;;CODE FOR HORIZONTAL TAB
(1)          000012   LF= 12          ;;CODE FOR LINE FEED
(1)          000015   CR= 15          ;;CODE FOR CARRIAGE RETURN
(1)          000200   CRLF= 200       ;;CODE FOR CARRIAGE RETURN-LINE FEED
(1)          177776   PS= 177776      ;;PROCESSOR STATUS WORD
(1)          .EQUIV PS,PSW
(1)          177774   STKLMIT= 177774   ;;STACK LIMIT REGISTER
(1)          177772   PIRQ= 177772      ;;PROGRAM INTERRUPT REQUEST REGISTER
(1)          177570   DSWR= 177570      ;;HARDWARE SWITCH REGISTER
(1)          177570   DDISP= 177570      ;;HARDWARE DISPLAY REGISTER

(1)          ;*GENERAL PURPOSE REGISTER DEFINITIONS
(1)          000000   R0= %0          ;;GENERAL REGISTER
(1)          000001   R1= %1          ;;GENERAL REGISTER
(1)          000002   R2= %2          ;;GENERAL REGISTER
(1)          000003   R3= %3          ;;GENERAL REGISTER
(1)          000004   R4= %4          ;;GENERAL REGISTER
(1)          000005   R5= %5          ;;GENERAL REGISTER
(1)          000006   R6= %6          ;;GENERAL REGISTER
(1)          000007   R7= %7          ;;GENERAL REGISTER
(1)          000006   SP= %6          ;;STACK POINTER
(1)          000007   PC= %7          ;;PROGRAM COUNTER

(1)          ;*PRIORITY LEVEL DEFINITIONS
(1)          000000   PR0= 0           ;;PRIORITY LEVEL 0
(1)          000040   PR1= 40          ;;PRIORITY LEVEL 1

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(1) 000100 PR2= 100 ;:PRIORITY LEVEL 2
(1) 000140 PR3= 140 ;:PRIORITY LEVEL 3
(1) 000200 PR4= 200 ;:PRIORITY LEVEL 4
(1) 000240 PR5= 240 ;:PRIORITY LEVEL 5
(1) 000300 PR6= 300 ;:PRIORITY LEVEL 6
(1) 000340 PR7= 340 ;:PRIORITY LEVEL 7
(1)

:*'"SWITCH REGISTER" SWITCH DEFINITIONS

(1) 100000 SW15= 100000
(1) 040000 SW14= 40000
(1) 020000 SW13= 20000
(1) 010000 SW12= 10000
(1) 004000 SW11= 4000
(1) 002000 SW10= 2000
(1) 001000 SW09= 1000
(1) 000400 SW08= 400
(1) 000200 SW07= 200
(1) 000100 SW06= 100
(1) 000040 SW05= 40
(1) 000020 SW04= 20
(1) 000010 SW03= 10
(1) 000004 SW02= 4
(1) 000002 SW01= 2
(1) 000001 SW00= 1
(1) .EQUIV SW09,SW9
(1) .EQUIV SW08,SW8
(1) .EQUIV SW07,SW7
(1) .EQUIV SW06,SW6
(1) .EQUIV SW05,SW5
(1) .EQUIV SW04,SW4
(1) .EQUIV SW03,SW3
(1) .EQUIV SW02,SW2
(1) .EQUIV SW01,SW1
(1) .EQUIV SW00,SW0
(1)

:*DATA BIT DEFINITIONS (BIT00 TO BIT15)

(1) 100000 BIT15= 100000
(1) 040000 BIT14= 40000
(1) 020000 BIT13= 20000
(1) 010000 BIT12= 10000
(1) 004000 BIT11= 4000
(1) 002000 BIT10= 2000
(1) 001000 BIT09= 1000
(1) 000400 BIT08= 400
(1) 000200 BIT07= 200
(1) 000100 BIT06= 100
(1) 000040 BIT05= 40
(1) 000020 BIT04= 20
(1) 000010 BIT03= 10
(1) 000004 BIT02= 4
(1) 000002 BIT01= 2
(1) 000001 BIT00= 1
(1) .EQUIV BIT09,BIT9
(1) .EQUIV BIT08,BIT8
(1) .EQUIV BIT07,BIT7
(1) .EQUIV BIT06,BIT6

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(1) .EQUIV BIT05,BITS
(1) .EQUIV BIT04,BIT4
(1) .EQUIV BIT03,BIT3
(1) .EQUIV BIT02,BIT2
(1) .EQUIV BIT01,BIT1
(1) .EQUIV BIT00,BITO

(1)      ;*BASIC "CPU" TRAP VECTOR ADDRESSES
(1) 000004  ERRVEC= 4          ;TIME OUT AND OTHER ERRORS
(1) 000010  RESVEC= 10         ;RESERVED AND ILLEGAL INSTRUCTIONS
(1) 000014  TBITVEC=14        ;"T" BIT
(1) 000014  TRTVEC= 14         ;TRACE TRAP
(1) 000014  BPTVEC= 14         ;BREAKPOINT TRAP (BPT)
(1) 000020  IOTVEC= 20         ;INPUT/OUTPUT TRAP (IOT) **SCOPE**
(1) 000024  PWRVEC= 24         ;POWER FAIL
(1) 000030  EMTVEC= 30         ;EMULATOR TRAP (EMT) **ERROR**
(1) 000034  TRAPVEC=34        ;"TRAP" TRAP
(1) 000060  TKVEC= 60          ;TTY KEYBOARD VECTOR
(1) 000064  TPVEC= 64          ;TTY PRINTER VECTOR
(1) 000240  PIROVEC=240       ;PROGRAM INTERRUPT REQUEST VECTOR
1221    170404   ABASE= 170404
1222    000344   AVECT1= 344
1223    000006   APRIOR= 6

1265
1275      .SBTTL ACT11 HOOKS
(1)
(2)      ;*****
(1)      ;HOOKS REQUIRED BY ACT11
(1) 000234  $SVPC=.           ;SAVE PC
(1) 000046  022414           ;=46
(1) 000046  000046           ;SENDAD             ;;1)SET LOC.46 TO ADDRESS OF SENDAD IN .SEOP
(1) 000052  000052           ;=52
(1) 000052  000000           ;.WORD 0            ;;2)SET LOC.52 TO ZERO
(1) 000234  000234           ;=$SVPC
(1) 001000  001000           ;=1000             ;; RESTORE PC
1276
1277      .SBTTL APT PARAMETER BLOCK
(1)
(2)      ;*****
(1)      ;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
(2)
(1) 001000  001000           ;$X=.               ;SAVE CURRENT LOCATION
(1) 000024  000024           ;=24                ;SET POWER FAIL TO POINT TO START OF PROGRAM
(1) 000024  000200           ;200                ;FOR APT START UP
(1) 000044  000044           ;=44                ;POINT TO APT INDIRECT ADDRESS PNTR.
(1) 000044  001000           ;$APTHDR           ;POINT TO APT HEADER BLOCK
(1) 001000  001000           ;.=.$X              ;RESET LOCATION COUNTER
(2)
(1)      ;SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC
(1)      ;INTERFACE SPEC.
(1)
(1) 001000  000000           ;SAPTHD:
(1) 001000  000000           ;SHIBTS: .WORD 0    ;TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
(1) 001002  001200           ;SMBADR: .WORD $MAIL ;ADDRESS OF APT MAILBOX (BITS 0-15)
(1) 001004  000002           ;STSTM: .WORD 2     ;RUN TIM OF LONGEST TEST
(1) 001006  000120           ;SPASTM: .WORD 120   ;RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
(1) 001010  000120           ;SUNITM: .WORD 120   ;ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT

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APT PARAMETER BLOCK

SEQ 0025

(1) 001012 000052
1278

.WORD \$ETEND-\$MAIL/2 ::LENGTH MAILBOX-ETABLE(WORDS)

1279

.SBTTL COMMON TAGS

;*****
;*THIS TABLE CONTAINS VARIOUS COMMON STORAGE LOCATIONS
;*USED IN THE PROGRAM.

(1)	001100	001100	.=1100			
(1)	001100	000000	SCMTAG:		;;START OF COMMON TAGS	
(1)	001102	000	STSTNM:	.WORD 0	;;CONTAINS THE TEST NUMBER	
(1)	001103	000	SERFLG:	.BYTE 0	;;CONTAINS ERROR FLAG	
(1)	001104	000000	SICNT:	.WORD 0	;;CONTAINS SUBTEST ITERATION COUNT	
(1)	001106	000000	SLPADR:	.WORD 0	;;CONTAINS SCOPE LOOP ADDRESS	
(1)	001110	000000	SLPERR:	.WORD 0	;;CONTAINS SCOPE RETURN FOR ERRORS	
(1)	001112	000000	SERTTL:	.WORD 0	;;CONTAINS TOTAL ERRORS DETECTED	
(1)	001114	000	SITEMB:	.BYTE 0	;;CONTAINS ITEM CONTROL BYTE	
(1)	001115	001	SERMAX:	.BYTE 1	;;CONTAINS MAX. ERRORS PER TEST	
(1)	001116	000000	SERRPC:	.WORD 0	;;CONTAINS PC OF LAST ERROR INSTRUCTION	
(1)	001120	000000	SGDADR:	.WORD 0	;;CONTAINS ADDRESS OF 'GOOD' DATA	
(1)	001122	000000	SBDADR:	.WORD 0	;;CONTAINS ADDRESS OF 'BAD' DATA	
(1)	001124	000000	SGDDAT:	.WORD 0	;;CONTAINS 'GOOD' DATA	
(1)	001126	000000	SBDDAT:	.WORD 0	;;CONTAINS 'BAD' DATA	
(1)	001130	000000		.WORD 0	;;RESERVED--NOT TO BE USED	
(1)	001132	000000		.WORD 0		
(1)	001134	000	SAUTOB:	.BYTE 0	;;AUTOMATIC MODE INDICATOR	
(1)	001135	000	\$INTAG:	.BYTE 0	;;INTERRUPT MODE INDICATOR	
(1)	001136	000000		.WORD 0		
(1)	001140	177570	SWR:	.WORD DSWR	;;ADDRESS OF SWITCH REGISTER	
(1)	001142	177570	DISPLAY:	.WORD DDISP	;;ADDRESS OF DISPLAY REGISTER	
(1)	001144	177560	STKS:	177560	TTY KBD STATUS	
(1)	001146	177562	STKB:	177562	TTY KBD BUFFER	
(1)	001150	177564	STPS:	177564	TTY PRINTER STATUS REG. ADDRESS	
(1)	001152	177566	STPB:	177566	TTY PRINTER BUFFER REG. ADDRESS	
(1)	001154	000	\$NULL:	.BYTE 0	CONTAINS NULL CHARACTER FOR FILLS	
(1)	001155	002	\$FILLS:	.BYTE 2	CONTAINS # OF FILLER CHARACTERS REQUIRED	
(1)	001156	012	\$FILLC:	.BYTE 12	INSERT FILL CHARS. AFTER A 'LINE FEED'	
(1)	001157	000	STPFLG:	.BYTE 0	'TERMINAL AVAILABLE' FLAG (BIT<07>=0=YES)	
(1)	001160	000000	\$REGAD:	.WORD 0	CONTAINS THE ADDRESS FROM WHICH (\$REGO) WAS OBTAINED	
(3)	001162	000000	\$REGO:	.WORD 0	CONTAINS ((SREGAD)+0)	
(3)	001164	000000	STMPO:	.WORD 0	USER DEFINED	
(1)	001166	000000	\$ESCAPE:	0	ESCAPE ON ERROR ADDRESS	
(1)	001170	177607	000377	\$BELL:	.ASCIZ <207><377><377>	CODE FOR BELL
(1)	001174	077	\$QUES:	.ASCII /?	QUESTION MARK	
(1)	001175	015	SCRLF:	.ASCII <15>	CARRIAGE RETURN	
(1)	001176	000012	SLF:	.ASCIZ <12>	LINE FEED	
(2)			*****			
(2)			.SBTTL APT MAILBOX-ETABLE			
(2)			*****			
(2)			.EVEN			
(2)	001200	000000	\$MAIL:		APT MAILBOX	
(2)	001200	000000	SMSGTY:	.WORD AMSGTY	MESSAGE TYPE CODE	
(2)	001202	000000	SFATAL:	.WORD AFATAL	FATAL ERROR NUMBER	
(2)	001204	000000	STESTN:	.WORD ATESDN	TEST NUMBER	
(2)	001206	000000	SPASS:	.WORD APASS	PASS COUNT	

(2) 001210 000000	SDEVCT: .WORD	ADEVCT	::DEVICE COUNT
(2) 001212 000000	SUNIT: .WORD	AUNIT	::I/O UNIT NUMBER
(2) 001214 000000	SMSGAD: .WORD	AMSGAD	::MESSAGE ADDRESS
(2) 001216 000000	SMSGLG: .WORD	AMSLG	::MESSAGE LENGTH
(2) 001220 000	SETABLE:		::APT ENVIRONMENT TABLE
(2) 001220 000	SENV: .BYTE	AENV	::ENVIRONMENT BYTE
(2) 001221 000	SENVM: .BYTE	AENVM	::ENVIRONMENT MODE BITS
(2) 001222 000000	SSWREG: .WORD	ASWREG	::APT SWITCH REGISTER
(2) 001224 000000	SUSR: .WORD	AUSR	::USER SWITCHES
(2) 001226 000000	SCPUOP: .WORD	ACPUOP	::CPU TYPE,OPTIONS
(2)	:		BITS 15-11=CPU TYPE
(2)	:		11/04=01,11/05=02,11/20=03,11/40=04,11/45=05
(2)	:		11/70=06,PDQ=07,Q=10
(2)	:		BIT 10=REAL TIME CLOCK
(2)	:		BIT 9=FLOATING POINT PROCESSOR
(2)	:		BIT 8=MEMORY MANAGEMENT
(2) 001230 000	\$MAMS1: .BYTE	AMAMS1	::HIGH ADDRESS,M.S. BYTE
(2) 001231 000	SMTYP1: .BYTE	AMTYP1	::MEM. TYPE,BLK#1
(2)	:		MEM.TYPE BYTE -- (HIGH BYTE)
(2)	:		900 NSEC CORE=001
(2)	:		300 NSEC BIPOLAR=002
(2)	:		500 NSEC MOS=003
(2) 001232 000000	\$MADR1: .WORD	AMADR1	::HIGH ADDRESS,BLK#1
(2)	:		MEM.LAST ADDR.=3 BYTES,THIS WORD AND LOW OF "TYPE" ABOVE
(2) 001234 000	\$MAMS2: .BYTE	AMAMS2	::HIGH ADDRESS,M.S. BYTE
(2) 001235 000	SMTYP2: .BYTE	AMTYP2	::MEM. TYPE,BLK#2
(2) 001236 000000	\$MADR2: .WORD	AMADR2	::MEM.LAST ADDRESS,BLK#2
(2) 001240 000	\$MAMS3: .BYTE	AMAMS3	::HIGH ADDRESS,M.S.BYTE
(2) 001241 000	SMTYP3: .BYTE	AMTYP3	::MEM. TYPE,BLK#3
(2) 001242 000000	\$MADR3: .WORD	AMADR3	::MEM.LAST ADDRESS,BLK#3
(2) 001244 000	\$MAMS4: .BYTE	AMAMS4	::HIGH ADDRESS,M.S.BYTE
(2) 001245 000	SMTYP4: .BYTE	AMTYP4	::MEM. TYPE,BLK#4
(2) 001246 000000	\$MADR4: .WORD	AMADR4	::MEM.LAST ADDRESS,BLK#4
(2) 001250 000344	SVECT1: .WORD	AVECT1	::INTERRUPT VECTOR#1,BUS PRIORITY#1
(2) 001252 000000	SVECT2: .WORD	AVECT2	::INTERRUPT VECTOR#2BUS PRIORITY#2
(2) 001254 170404	SBASE: .WORD	ABASE	::BASE ADDRESS OF EQUIPMENT UNDER TEST
(2) 001256 000000	SDEVM: .WORD	ADEV	::DEVICE MAP
(2) 001260 000000	SCDW1: .WORD	ACDW1	::CONTROLLER DESCRIPTION WORD#1
(2) 001262 000000	SCDW2: .WORD	ACDW2	::CONTROLLER DESCRIPTION WORD#2
(2) 001264 000000	SDDW0: .WORD	ADDW0	::DEVICE DESCRIPTOR WORD#0
(2) 001266 000000	SDDW1: .WORD	ADDW1	::DEVICE DESCRIPTOR WORD#1
(2) 001270 000000	SDDW2: .WORD	ADDW2	::DEVICE DESCRIPTOR WORD#2
(2) 001272 000000	SDDW3: .WORD	ADDW3	::DEVICE DESCRIPTOR WORD#3
(2) 001274 000000	SDDW4: .WORD	ADDW4	::DEVICE DESCRIPTOR WORD#4
(2) 001276 000000	SDDW5: .WORD	ADDW5	::DEVICE DESCRIPTOR WORD#5
(2) 001300 000000	SDDW6: .WORD	ADDW6	::DEVICE DESCRIPTOR WORD#6
(2) 001302 000000	SDDW7: .WORD	ADDW7	::DEVICE DESCRIPTOR WORD#7
(2) 001304 000000	SDDW8: .WORD	ADDW8	::DEVICE DESCRIPTOR WORD#8
(2) 001306 000000	SDDW9: .WORD	ADDW9	::DEVICE DESCRIPTOR WORD#9
(2) 001310 000000	SDDW10: .WORD	ADDW10	::DEVICE DESCRIPTOR WORD#10
(2) 001312 000000	SDDW11: .WORD	ADDW11	::DEVICE DESCRIPTOR WORD#11
(2) 001314 000000	SDDW12: .WORD	ADDW12	::DEVICE DESCRIPTOR WORD#12
(2) 001316 000000	SDDW13: .WORD	ADDW13	::DEVICE DESCRIPTOR WORD#13
(2) 001320 000000	SDDW14: .WORD	ADDW14	::DEVICE DESCRIPTOR WORD#14
(2) 001322 000000	SDDW15: .WORD	ADDW15	::DEVICE DESCRIPTOR WORD#15

(2) 001324 SETEND:
(2)
(3)
(3) 001324 170404 ASR: 170404 :/CLOCK A STATUS REGISTER.
(3) 001326 170406 ABR: 170406 :/CLOCK A BUFFER REGISTER.
(3) 001330 170430 ACR: 170430 :/CLOCK A COUNT REGISTER.
(3)
(3) 001332 170432 BSR: 170432 :/CLOCK B STATUS REGISTER.
(3) 001334 170434 BBR: 170434 :/CLOCK B BUFFER REGISTER.
(3) 001336 170436 BCR: 170436 :/CLOCK B COUNT REGISTER.
(3)
(3) 001340 000344 AVECT: 344 :/CLOCK A INTR. VECTOR ADDR.
(3) 001342 000346 AVECP2: 346 :/CLOCK A INTR. STATUS WORD.
(3)
(3) 001344 000364 BVECT: 364 :/CLOCK B INTR. VECTOR ADDR.
(3) 001346 000366 BVECT2: 366 :/CLOCK B INTR. STATUS WORD.
(3)
(3) 001350 000006 APRITY: 6 :/PRIORITY LEVEL OF CLOCK A.
(3) 001352 000006 BPRITY: 6 :/PRIORITY LEVEL OF CLOCK B.
(3) 001354 000000 \$TMDAT: 0
(3)

(1)

.SBTTL ERROR POINTER TABLE

(1)
(1) /*THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.
(1) /*THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN
(1) /*LOCATION \$ITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.
(1) /*NOTE1: IF \$ITEMB IS 0 THE ONLY PERTINENT DATA IS (\$ERRPC).
(1) /*NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:
(1)

(1) :* EM ::POINTS TO THE ERROR MESSAGE
(1) :* DH ::POINTS TO THE DATA HEADER
(1) :* DT ::POINTS TO THE DATA
(1) :* DF ::POINTS TO THE DATA FORMAT
(1)

1284 001356

SERRTB:

1285 :ITEM 1
1286
1287 001356 027166 EM1 :CLOCK A SR FUNCTION ERROR
1288 001360 030053 DH1 :ERRPC ASR WAS S/B
1289 001362 030666 DT1 :\$ERRPC,ASR,\$BDDAT,\$GDDAT
1290 001364 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)

1291
1292 :ITEM 2
1293
1294 001366 027221 EM2 :CLOCKA SR DATA ERROR
1295 001370 030053 DH1 :ERRPC ASR WAS S/B
1296 001372 030666 DT1 :\$ERRPC,ASR,\$BDDAT,\$GDDAT
1297 001374 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)

1298
1299 :ITEM 3
1300
1301 001376 027250 EM3 :CLOCKA BR DATA ERROR
1302 001400 030111 DH3 :ERRPC ABR WAS S/B
1303 001402 030700 DT3 :\$ERRPC,ABR,\$BDDAT,\$GDDAT
1304 001404 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)

1305
1306 :ITEM 4
1307
1308 001406 027277 EM4 :CLOCKA CR DATA ERROR
1309 001410 030147 DH4 :ERRPC ACR WAS S/B
1310 001412 030712 DT4 :\$ERRPC,ACR,\$BDDAT,\$GDDAT
1311 001414 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)

1312
1313 :ITEM 5
1314
1315 001416 027326 EM5 :CLOCK B SR DATA ERROR
1316 001420 030205 DH5 :ERRPC BSR WAS S/B
1317 001422 030724 DT5 :\$ERRPC,BSR,\$BDDAT,\$GDDAT
1318 001424 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)

1319

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ERROR POINTER TABLE

SEQ 0030

1320 :ITEM 6
1321
1322 001426 027355 EM6 ;CLOCK B BR DATA ERROR
1323 001430 030243 DH6 ;ERRPC BBR WAS S/B
1324 001432 030736 DT6 ;\$ERRPC,BBR,\$BDDAT,\$GDDAT
1325 001434 031070 DFO ;ALL NUMBERS ARE IN OCTAL FORM
(1)
1326
1327 :ITEM 7
1328
1329 001436 027404 EM7 ;CLOCK B CR DATA ERROR
1330 001440 030301 DH7 ;ERRPC BCR WAS S/B
1331 001442 030750 DT7 ;\$ERRPC,BCR,\$BDDAT,\$GDDAT
1332 001444 031070 DFO ;ALL NUMBERS ARE IN OCTAL FORM
(1)
1333
1334 :ITEM 10
1335
1336 001446 027433 EM10 ;DUAL ADDRESS ERROR
1337 001450 030337 DH10 ;ERROR GOOD BAD GOOD DATA READ FROM
1338
1339 001452 030762 DT10 ;PC ADDR ADDR DATA DUAL ADDRESS
1340 001454 031070 DFO ;\$ERRPC,\$GDADR,\$BDADR,\$GDDAT,\$BDDAT
;ALL NUMBERS ARE IN OCTAL FORM
(1)
1341
1342 :ITEM 11
1343
1344 001456 027460 EM11 ;CLOCK A COUNT ERROR
1345 001460 030147 DH4 ;ERRPC ACR WAS S/B
1346 001462 030712 DT4 ;\$ERRPC,ACR,\$BDDAT,\$GDDAT
1347 001464 031070 DFO ;ALL NUMBERS ARE IN OCTAL FORM
(1)
1348
1349 :ITEM 12
1350
1351 001466 027507 EM12 ;CLOCK A COUNT FUNCTION ERROR
1352 001470 030476 DH12 ;ERRPC ASR
1353 001472 030776 DT12 ;\$ERRPC,ASR
1354 001474 031070 DFO ;ALL NUMBERS ARE IN OCTAL FORM
(1)
1355
1356 :ITEM 13
1357
1358 001476 031070 DFO ;ERROR 13 DOES NOT EXSIST.
1359 001500 031070 DFO ;IT WOULD BE BAD LUCK.
1360 001502 031070 DFO
1361 001504 031070 DFO
1362
1363 :ITEM 14
1364
1365 001506 027547 EM14 ;CLOCK B COUNT FUNCTION ERROR
1366 001510 030515 DH14 ;ERRPC BSR
1367 001512 031004 DT14 ;\$ERRPC,BSR
1368 001514 031070 DFO ;ALL NUMBERS ARE IN OCTAL FORM
(1)
1369

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ERROR POINTER TABLE

SEQ 0031

1370 :ITEM 15
1371
1372 001516 027607 EM15 :CLOCK B COUNT ERROR
1373 001520 030301 DH7 :ERRPC CSR WAS S/B
1374 001522 030750 DT7 :\$ERRPC, BCR, \$BDDAT, \$GDDAT
1375 001524 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)
1376
1377 :ITEM 16
1378
1379 001526 027636 EM16 :CLOCK A INTERRUPT ERROR
1380 001530 030476 DH12 :ERRPC ASR
1381 001532 030776 DT12 :\$ERRPC, ASR
1382 001534 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)
1383
1384 :ITEM 17
1385
1386 001536 027671 EM17 :CLOCK B INTERRUPT ERROR
1387 001540 030515 DH14 :ERRPC BSR
1388 001542 031004 DT14 :\$ERRPC, BSR
1389 001544 031070 DFO
1390
1391 :ITEM 20
1392
1393 001546 027724 EM20 :CLOCK A REPEATABILITY ERROR
1394 001550 030533 DH20 :ERROR ASR 2ND CNT 1ST CNT
1395 001552 030666 DT1 :\$ERRPC, ASR, \$BDDAT, \$GDDAT
1396 001554 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)
1397
1398 :ITEM 21
1399
1400 001556 027460 EM11 :CLOCK A COUNT ERROR
1401 001560 030147 DH4 :ERROR ASR 2ND CNT 1ST CNT
1402 001562 031012 DT21 :\$ERRPC, ASR, \$BDDAT, \$GDDAT
1403 001564 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)
1404
1405 :ITEM 22
1406
1407 001566 027460 EM11 :CLOCK A COUNT ERROR
1408 001570 030147 DH4 :ERRPC ASR WAS S/B
1409 001572 031024 DT22 :\$ERRPC, ACR, \$BDDAT, \$TMPO
1410 001574 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)
1411
1412 :ITEM 23
1413
1414 001576 027763 EM23 :CLOCK B REPEATABILITY ERROR
1415 001600 030575 DH23 :ERROR ASR 2ND CNT 1ST CNT
1416 001602 030666 DT1 :\$ERRPC, ASR, \$BDDAT, \$GDDAT
1417 001604 031070 DFO :ALL NUMBERS ARE IN OCTAL FORM
(1)
1418
1419 :ITEM 24

1420				
1421	001606	027607	EM15	:CLOCK B COUNT ERROR
1422	001610	030301	DH7	:ERRPC BCR WAS S/B
1423	001612	031036	DT24	:\$ERRPC, BCR, \$GDDAT, \$TMO
1424	001614	031070	DFO	;ALL NUMBERS ARE IN OCTAL FORM
(1)				
1425				
1426			:ITEM 25	
1427				
1428	001616	027607	EM15	:CLOCK B COUNT ERROR
1429	001620	030301	DH7	:ERRPC BCR WAS S/B
1430	001622	031050	DT25	:\$ERRPC, BCR, \$BDDAT, \$TMO
1431	001624	031070	DFO	;ALL NUMBERS ARE IN OCTAL FORM
(1)				
1432				
1433			:ITEM 26	
1434				
1435	001626	030022	EM26	:CLOCK ADDRESSING ERROR
1436	001630	030637	DH26	:ERRPC CLOCK ADDR.
1437	001632	031062	DT26	:\$ERRPC, \$TMO
1438	001634	031070	DFO	;ALL NUMBERS ARE IN OCTAL FORM
(1)				
1439				
(1)			:ADDRESS OF KMC-11 OF LPA-11	THE ADDR FOR KMAD0 MAY BE
(1)			:	CHANGED BY THE USER TO REFLECT
(1)			:	A DIFFERENT KMC-11 ADDR. THE
(1)			:	REST OF THE ADDRESSES WILL
(1)			:	BE CHANGED BY THE PROGRAM.
(1)				
(1)	001636	170460	LPCI: KMAD0: .WORD 170460	:BASE KMC ADDR. MAY BE PATCHED BY USER.
(1)	001636	170460		
(1)	001640	170461	LPMR: KMAD1: .WORD 170460+1	;>DO NOT <;KMC-CSR ADDR
(1)	001640	170461		
(1)	001642	170462	LPC0: KMAD2: .WORD 170460+2	;>PATCH <
(1)	001642	170462		
(1)	001644	170463	LPS0: KMAD3: .WORD 170460+3	;>THIS AREA <
(1)	001644	170463		
(1)	001646	170464	LPADL: KMAD4: .WORD 170460+4	:
(1)	001646	170464		
(1)	001650	170465	LPADH: KMAD5: .WORD 170460+5	;>DO NOT <
(1)	001650	170465		
(1)	001652	170466	LPMS1: KMAD6: .WORD 170460+6	;>PATCH <
(1)	001652	170466		
(1)	001654	170467	LPMS2: KMAD7: .WORD 170460+7	;>THIS AREA <
(1)	001654	170467		
(1)	001656	000344	VECTOR: .WORD AVECT1&777	:BASE VECTOR OF KMC
(1)	001660	000350	VECTPS: .WORD 4+AVECT1&777	:VECOTR ADDR.+2
(1)	001662	000005	VERSN: .WORD 5	:CURRENT VERSION NUMBER OF MICROCODE.
(1)	001664	000000	.DVLS: .WORD 0	:/DEVICE LIST OF I/O ADDR. DEFINED
(1)	001666	000020	.BLKW 16.	:/BY INIT.
(1)				

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PROGRAM START

SEQ 0033

1440

.SBTTL PROGRAM START

1443
 1444 001726

```

START:
(1) .SBTTL INITIALIZE THE COMMON TAGS
(1)      ;:CLEAR THE COMMON TAGS ($CMTAG) AREA
(1) 001726 012706 001100      MOV #$CMTAG,R6      ;:FIRST LOCATION TO BE CLEARED
(1) 001732 005026            CLR (R6)+           ;:CLEAR MEMORY LOCATION
(1) 001734 022706 001140      CMP #$WR,R6       ;:DONE?
(1) 001740 001374            BNE -6             ;:LOOP BACK IF NO
(1) 001742 012706 001100      MOV #$STACK,SP    ;:SETUP THE STACK POINTER
(1)      ;:INITIALIZE A FEW VECTORS
(1) 001746 012737 025062 000020      MOV #$SCOPE,@#IOTVEC ;:IOT VECTOR FOR SCOPE ROUTINE
(1) 001754 012737 000340 000022      MOV #340,@#IOTVEC+2 ;:LEVEL 7
(1) 001762 012737 024302 000030      MOV #$ERROR,@#EMTVEC ;:EMT VECTOR FOR ERROR ROUTINE
(1) 001770 012737 000340 000032      MOV #340,@#EMTVEC+2 ;:LEVEL 7
(1) 001776 012737 027102 000034      MOV #$STRAP,@#TRAPVEC ;:TRAP VECTOR FOR TRAP CALLS
(1) 002004 012737 000340 000036      MOV #340,@#TRAPVEC+2;LEVEL 7
(1) 002012 012737 026662 000024      MOV #$PWRDN,@#PWRVEC ;:POWER FAILURE VECTOR
(1) 002020 012737 000340 000026      MOV #340,@#PWRVEC+2 ;:LEVEL 7
(1) 002026 013737 022362 022354      MOV SENDCT,$EOPCT ;:SETUP END-OF-PROGRAM COUNTER
(1) 002034 005037 001166            CLR $ESCAPE        ;:CLEAR THE ESCAPE ON ERROR ADDRESS
(1) 002040 112737 000001 001115      MOVB #1,$ERMAX     ;:ALLOW ONE ERROR PER TEST
(1) 002046 012737 002046 001106      MOV #.,$LPADR     ;:INITIALIZE THE LOOP ADDRESS FOR SCOPE
(1) 002054 012737 002054 001110      MOV #.,$LPERR      ;:SETUP THE ERROR LOOP ADDRESS
(2)      ;:SIZE FOR A HARDWARE SWITCH REGISTER. IF NOT FOUND OR IT IS
(2)      ;:EQUAL TO A "-1", SETUP FOR A SOFTWARE SWITCH REGISTER.
(2) 002062 013746 000004            MOV @#ERRVEC,-(SP) ;:SAVE ERROR VECTOR
(2) 002066 012737 002122 000004      MOV #64$,@#ERRVEC ;:SET UP ERROR VECTOR
(2) 002074 012737 177570 001140      MOV #DSWR,$WR      ;:SETUP FOR A HARDWARE SWICH REGISTER
(2) 002102 012737 177570 001142      MOV #DDISP,DISPLAY ;:AND A HARDWARE DISPLAY REGISTER
(2) 002110 022777 177777 177022      CMP #-1,@SWR       ;:TRY TO REFERENCE HARDWARE SWR
(2) 002116 001012                  BNE 66$          ;:BRANCH IF NO TIMEOUT TRAP OCCURRED
(2)                      ;:AND THE HARDWARE SWR IS NOT = -1
(2) 002120 000403                  BR 65$          ;:BRANCH IF NO TIMEOUT
(2) 002122 012716 002130            64$: MOV #65$, (SP) ;:SET UP FOR TRAP RETURN
(2) 002126 000002                  RTI
(2) 002130 012737 000176 001140      65$: MOV #SWREG,$WR    ;:POINT TO SOFTWARE SWR
(2) 002136 012737 000174 001142      MOV #DISPREG,DISPLAY
(2) 002144 012637 000004            66$: MOV (SP)+,@#ERRVEC ;:RESTORE ERROR VECTOR
(1)
(2) 002150 005037 001206            CLR SPASS        ;:CLEAR PASS COUNT
(2) 002154 132737 000200 001221      BITB #APT SIZE,$ENV  ;:TEST USER SIZE UNDER APT
(2) 002162 001403                  BEQ 67$          ;:YES,USE NON-APT SWITCH
(2) 002164 012737 001222 001140      MOV #SSWREG,$WR    ;:NO,USE APT SWITCH REGISTER
(2) 002172 122737 000001 001134      67$: CMPB #1,$AUTOB   ;:IF RUNNING XXDP ETC.
1445 002172
1446 002200 001426
1447
1448 002202 104401 002210
(1) 002206 000423
(1) 002256
1449
1450 002256 013737 001254 001324 10$: MOV $BASE,ASR
1451 002264 012737 000001 001210      MOV #1,$DEVCT
1452 002272 005037 001206            CLR SPASS
1453

```

TYPE ,69\$;:TYPE ASCIZ STRING
 BR ,68\$;:GET OVER THE ASCIZ
 .ASCIZ <15><12><12>#CRLPGC LPA/KW11-K DIAGNOSTIC<15><12>

1454 ;THIS SECTION OF CODE HANDLES INITIALIZING LPA-11 FUNCTIONS
 (1)
 (1)
 (1)
 (1) 002276 010046
 (1) 002300 010146
 (1) 002302 013700 001636
 (1) 002306 012701 001640
 (1)
 (1) 002312 005200
 (1) 002314 010021
 (1) 002316 020127 001656
 (1) 002322 001373
 (1) 002324 005037 001664
 (1) 002330 012601
 (1) 002332 012600

70\$: MOV R0,-(SP)
 MOV R1,-(SP)
 MOV KMAD0,R0 ;GET KMC-11 ADDRESS.
 MOV #KMAD1,R1 ;GET ADDR. OF ADDR. LIST.

70\$: INC R0 ;UPDATE ADDR.
 MOV R0,(1)+ ;WRITE ADDR.
 CMP R1,#KMAD7+2 ;DONE ALL ADDRESSES?
 BNE 70\$;NO - DO NEXT ADDR.
 CLR DVLS ;CLR ADDR. LIST.
 MOV (SP)+,R1
 MOV (SP)+,R0

1455
 1456 002334
 1457 002334 005000
 1458 002336 005200
 1459 002340 001376
 1460 002342 013700 001324
 1461 002346 062700 000002
 1462 002352 010037 001326
 1463 002356 062700 000022
 1464 002362 010037 001330
 1465 002366 062700 000002
 1466 002372 010037 001332
 1467 002376 062700 000002
 1468 002402 010037 001334
 1469 002406 062700 000002
 1470 002412 010037 001336

LOOP:
 1\$: CLR R0 ;DELAY SOME TIME SO THAT FIRST RESET
 INC R0 ;INSTR. WON'T CLOBBER TYPEOUT.
 BNE 1\$;NOW WE'RE GONNA FIX
 MOV ASR,R0 ;ALL CLOCK ADDRESSES BASED ON ASR.

1471
 1472 002416 013700 001340
 1473 002422 062700 000002
 1474 002426 010037 001342
 1475 002432 062700 000016
 1476 002436 010037 001344
 1477 002442 062700 000002
 1478 002446 010037 001346

MOV AVECT,R0 ;NOW FIX VECTOR ADDRESSES
 ADD #2,R0 ;BASED ON AVECT.

1479
 1480 002452 013737 001350 001352
 1481 002460 000402
 1482 002462 005037 001664
 1483 002466 012706 001100
 1484 002472 012746 000340
 1485 002476 012746 002504
 1486 002502 000002
 1487 002504

MOV APRITY,BPRITY ;FIX CLK B'S PRIORITY BASED ON A'S.
 BR SSTART
 RSTART: CLR DVLS
 SSTART: MOV #STACK,SP
 MOV #340,-(SP)
 MOV #1\$,-(SP) ;SET PROCESSOR PRIORITY TO 7.

RTI
 1\$: ;
 .SBTTL *
 .SBTTL * PHASE 1CLOCKS A+B BASIC LOGIC TESTS.
 .SBTTL *

1518

```
(1)
(5) **** TEST 1      *TEST THE ADDRESSABILITY OF CLOCK ADDRESS
(4)
(5) *'BUS A17':'A04'='DEVICE' H; 'DEVICE' H +'TP0' H='DEV ENABLE' H
(5) *'DEV ENABLE'- H+'TP1' H='DEV ENB Z' H
(5)
(6)
(6) * PROBABLE SYNC POINT FOR THIS TEST:: 'BUS A17'
(6)
(5) * CLOCK ADDRESS TEST. SCOPE FOR 'DEV ENB Z' H AND WORK BACK
(5)
(4) ****
(3) 002504 000240
(1) 002506 112737 000001 001102 TST1: NOP
(1) 002514 112737 000001 001204 1$: MOVB #1,$TSTMN
(1)                                MOVB #1,$TESTN

(1)
(1)
(2)          ;*     MOV    @ASR,$BDDAT    ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2)          ;*     MOV    @ABR,$BDDAT    ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(2)          ;*     MOV    @ACR,$BDDAT    ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(2)          ;*     MOV    @BSR,$BDDAT    ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(2)          ;*     MOV    @BBR,$BDDAT    ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(2)          ;*     MOV    @BCR,$BDDAT    ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
```

1541

```
1542 ****
(3) *TEST 2      *TEST THAT CLOCK A BUFFER CAN BE WRITTEN INTO
(4)
(4) *FOR LOADING DATA:
(4)
(4) * (WE KNOW WE CAN ADDR. KW11), 'BUS A01' L + 'A02' H + 'A03' H
(4) *+'BUS C1' L='LD BUFF A' L
(4) *'LD BUF A' L + BUFFERED DATA LOADS INTO MUX LATCH (NOTE WE KNOW
(4) *BY NOW 'TP1' L SHOULD BE GOOD).
(4)
(4) * FOR READING DATA:
(4)
(4) *BUS A01 L + (DATA 1N H + EV ENABLE(1) H)=RD BUFF AL
(4) * [BA01H*(DEPENDING ON WHICH DATA BITS READ) RD BUF AL]+BUFF A00:15
(4) *+[DEV ENABLE*DATA IN L]=BUS DATA
(4)
(4) * SINCE WE WONT LOOK FOR ANY SPECIFIC DATA BIT FAILURE,
(4) * JUST THAT WE CAN WRITE INTO BUFFER + READ BACK,
(4) * IF FAILED, KEY ON 'LD BUFF A L' AND 'RD BUFF A L'
(5)
(5) * PROBABLE SYNC POINT FOR THIS TEST:: 'BUS A17' (2 OCCURANCES PER LOOP)
(5)
(4)
```

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T2 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN INTO

SEQ 0037

(4)
(3)
(2) 002602 000004 TST2: SCOPE
1543
1544
1545
1546
1547 002604 012737 001416 001124 MOV #1416,\$GDDAT ;WRITE INTO PRESET BUFFER.
1548 (1) . ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
1549 (1) . ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
1550 002632 005737 001126 TST SBDDAT
1551 002636 001001 BNE 1\$;IF ANY DATA WAS READ BACK, WE WILL
1552 ;BR PAST THE ERROR CALL.
1553
1554 ;:;\$>> ERROR <<\$
1555 002640 104003 ERROR 3 ;UNABLE TO LOAD AND READ BACK
1556 ;FROM THE BUFFER REGISTER CLOCK A.
1557 ;:;\$>> ERROR <<\$
1558 002642 1\$: .

1570
1571 :*****
(3) *TEST 3 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN TO A ZERO
(4)
(4) *THE LAST TEST WROTE 1'S INTO CLOCK A'S BUFFER. IN THIS
(4) TEST WE TRY TO WRITE ALL ZEROS.
(4)
(4) *SIGNALS - SAME AS LAST TEST. SUSPECT F/F OR DATA GATE STUCK OPEN
(5)
(5) * PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
(5)
(4)
(4)
(3)
(2) 002642 000004 TST3: SCOPE
1572
1573 002644 005037 001124 CLR SGDDAT ;INDICATE WE EXPECT 0'S.
1574 ;CLEAR BUFFER REGISTER.
1575 ;READ CLOCK A'S BUFFER REGISTER
1576 (1) ;* MOV SGDDAT,ABR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
1577 (1) ;* MOV ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN SBDDAT.
1578 002670 005737 001126 TST \$GDDAT
1579 002674 001401 1\$ BEQ ;SHOULD BE CLEAR - IF CLEAR - NEXT TEST.
1580
1581 ;:;SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
1582 002676 104003 ERROR 3 ;CLEAR INTR. FAILED TO CLEAR CLOCK A'S
1583 ;BUFFER REGISTER.
1584 ;:;SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
1585 002700 1\$:
1586
1603
1604 :*****
(3) *TEST 4 *TEST THAT CLOCK A'S STATUS CAN BE WRITTEN AND READ
(4)
(4) *NOW THAT WE CAN WRITE INTO THE BUFFER REGISTER, WE'RE GOING TO TRY
(4) WRITING INTO THE STATUS REGISTER AND READ IT BACK.
(4)
(4) *NEW SIGNALS: ['BA03' L + 'BA02' L + 'BA01' L] = 'LD STAT A' L
(4) * 'DATA OUT LO' L + 'DATA OUT HI' L + 'LD STATA' L = 'LD STAT A HI' H
(4) * + 'LD STATA LO' H
(4) *FOR READ BACK: 'RD STATA' L
(4)
(4) *NO ATTEMPT MADE TO VERIFY THAT CORRECT DATA CAME BACK, BUT
(4) *JUST THAT SOME DATA CAME BACK.
(5)
(5) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEV ENABLE (1)' 2 OCCURANCES PER PASS
(5)
(4)
(3) ;*****

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T4 *TEST THAT CLOCK A'S STATUS CAN BE WRITTEN AND READ

SEQ 0039

(2) 002700 000004 TST4: SCOPE
1605 002702 012737 001416 001124 MOV #1416,\$GDDAT ;LOAD SGDDAT WITH S/B.
1606 ;* MOV \$GDDAT,@ASR ;LOAD STATUS REGISTER.
1607 ;* TST SBDDAT ;READ BACK STATUS REGISTER
1608 (1) ;* MOV @ASR,\$BDDAT ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
1609 (1) ;* BNE 1S ;/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
1610 002730 005737 001126 ;IF ANY BITS RETURNED - NO ERROR.
1611 002734 001001
1612 ;;;\$>> ERROR <<\$
1613 002736 104002 ERROR 2 ;ERROR-UNABLE TO LOAD AND READ BACK
1614 ;STATUS REGISTER OF CLOCK A.
1615 ;;;\$>> ERROR <<\$
1616 002740 005037 001124 1\$: CLR \$GDDAT ;CLEAR CLOCKA'S STATUS REG.
1617 ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
1618 ;*****
1619 ;* TEST 5 *TEST THAT CLOCK B'S STATUS REGISTER CAN BE WROTE/READ
1620 ;* NEW SIGNALS: ['BA03' H + 'BA02' L + 'BA01' L] = 'LD STATB' L * 'RD STAT B' L
1621 ;* PROBABLE SYNC POINT FOR THIS TEST:: "DEV ENABLE (1)" 2 OCCURANCES PER PASS
1622 ;*
1623 ;*****
1624 (3) 002754 000004 TST5: SCOPE
1625 002756 012737 001016 001124 MOV #1016,\$GDDAT ;USE 1016 AS PATTERN, PUT IN SGDDAT.
1626 ;* MOV \$GDDAT,@BSR ;LOAD B'S STAT REG.
1627 ;* TST SBDDAT ;READ BACK THE STATUS REG.
1628 ;* BNE 1S ;/ PUT DATA FROM SGDDAT TO DEVICE REG BSR
1629 ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN SBDDAT.
1630 003004 005737 001126 ;IF ANY BITS CAME BACK, SUBTEST OK.
1631 003010 001001
1632 ;;;\$>> ERROR <<\$
1633 003012 104005 ERROR 5 ;ERROR-COULD NOT WRITE/READ BACK
1634 ;CLOCK B'S STATUS REGISTER.
1635 ;;;\$>> ERROR <<\$

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TS *TEST THAT CLOCK B'S STATUS REGISTER CAN BE WROTE/READ

B 4
SEQ 0040

1645 003014

1\$:

1646
1647
1654
1655
(3) *TEST 6 *TEST THAT CLOCK B'S BUFFER REGISTER CAN BE WROTE/READ
(4)
(4) *NEW SIGNALS: [''BA03'' H + ''BA02'' L + ''BA01'' H] = ''LD BUFF B'' L * ''RD BUFF B'' L
(5)
(5) * PROBABLE SYNC POINT FOR THIS TEST:: ''DEV ENABLE (1)'' 2 OCCURANCES PER PASS
(5)
(4)
(3)
(2) 003014 000004 TST6: SCOPE

1656
1657 003016 012737 000370 001124 MOV #370,\$GDDAT ;USE PATTERN ''370'', PUT IN \$GDDAT.
1658 ;WRITE INTO CLOCK B'S BUFFER REGISTER.
1659 ;READ IT BACK.
1660 (1) ;* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
1661 (1) ;* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
1662 003044 005737 001126 TST \$BDDAT
1663 003050 001001 BNE 1\$;IF ANY BITS COME BACK-SUBTEST OK.

1664
1665 ;:;SSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSS

1666 003052 104006 ERROR 6 ;ERROR-FAILED TO WRITE/READ CLOCKB'S
1667 ;BUFFER REGISTER.

1668
1669 ;:;SSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSS

1670 003054 1\$:

1671
1679

1778 :/#
(6) :*****
(5) *TEST 7 *TEST THAT CLOCK A STATUS REGISTER BIT 15 CAN BE SET AND CLEARED
(6)
(6) *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) *F/FS OR GATES
(7)
(7) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(7)
(6)
(5)
(4) 003054 000004 TST7: SCOPE
(2) :CLEAR THE STATUS REGISTER.
(2) :SET BIT 15.
(2) :SET FOR ERROR TYPEOUT S/B.
(2) :READ THE STATUS REGISTER.
(2) 003056 012737 100000 001124 MOV #BIT15,\$GDDAT
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 003104 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 15 AND ONLY BIT 15 SET?
(2) 003112 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(3) ::::::::::::::> ERROR <:::::::::::
(2) 003114 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;/BIT 15 FAILED TO BIT SET.
(3) ::::::::::::::> ERROR <:::::::::::
(2) 003116 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(2) 003120 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 15.
(2) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 003144 005737 001126 TST \$BDDAT
(2) 003150 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(3) ::::::::::::::> ERROR <:::::::::::
(2) 003152 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;/BIT 15 FAILED TO CLEAR.
(3) ::::::::::::::> ERROR <:::::::::::
(2) 003154 2\$:

(2) ;#
(6) :*****
(5) *TEST 10 *TEST THAT CLOCK A STATUS REGISTER BIT 14 CAN BE SET AND CLEARED
(6) :*
(6) :CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) :F/FS OR GATES
(7) :*
(7) : PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(7) :*
(6) :*
(5) :*****
(4) 003154 000004 TST10: SCOPE
(2) :/CLEAR THE STATUS REGISTER.
(2) :/SET BIT 14.
(2) :/SET FOR ERROR TYPEOUT S/B.
(2) :/READ THE STATUS REGISTER.
(2) 003156 012737 040000 001124 MOV #BIT14,\$GDDAT
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 003204 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 14 AND ONLY BIT 14 SET?
(2) 003212 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(3) ::\$> ERROR <<\$
(2) 003214 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;/BIT 14 FAILED TO BIT SET.
(3) ::\$> ERROR <<\$
(2) 003216 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(2) 003220 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 14.
(2) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 003244 005737 001126 TST \$BDDAT
(2) 003250 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(3) ::\$> ERROR <<\$
(2) 003252 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;/BIT 14 FAILED TO CLEAR.
(3) ::\$> ERROR <<\$
(2) 003254 2\$:

(2) ;/*
(6) :*****
(5) *TEST 11 *TEST THAT CLOCK A STATUS REGISTER BIT 13 CAN BE SET AND CLEARED
(6) *
(6) *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) *F/FS OR GATES
(7) *
(7) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(7) *
(6) *
(5) *
(4) 003254 000004 TST11: SCOPE
(2) :/CLEAR THE STATUS REGISTER.
(2) :/SET BIT 13.
(2) :/SET FOR ERROR TYPEOUT S/B.
(2) :/READ THE STATUS REGISTER.
(2) 003256 012737 020000 001124 MOV #BIT13,\$GDDAT
(3) :* MOV \$GDDAT,@ASR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) :* MOV @ASR,\$BDDAT :/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 003304 023737 001124 001126 CMP \$GDDAT,\$BDDAT :/DID BIT 13 AND ONLY BIT 13 SET?
(2) 003312 001402 BEQ 1\$:/IF SO-LETS TRY CLEARING IT.
(3) ::\$>> ERROR <<\$
(2) 003314 104002 ERROR 2 :/ERROR CLOCK AS STATUS REGISTER.
(2) :/BIT 13 FAILED TO BIT SET.
(3) ::\$>> ERROR <<\$
(2) 003316 000416 BR 2\$:/BR TO END SUBTEST.
(2) 003320 005037 001124 1\$: CLR \$GDDAT :/TRY CLEARING BIT 13.
(2) :/CLEAR S/B FOR TYPEOUT IF ANY.
(2) :/NOW READ IT BACK.
(3) :* MOV \$GDDAT,@ASR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) :* MOV @ASR,\$BDDAT :/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 003344 005737 001126 TST \$BDDAT
(2) 003350 001401 BEQ 2\$:/IF ZERO-NO ERROR!
(3) ::\$>> ERROR <<\$
(2) 003352 104002 ERROR 2 :/ERROR-CLOCK A STATUS REGISTER.
(2) :/BIT 13 FAILED TO CLEAR.
(3) ::\$>> ERROR <<\$
(2) 003354 2\$:

(2) :/#
(6) ;*****
(5) ;*TEST 12 *TEST THAT CLOCK A STATUS REGISTER BIT 9 CAN BE SET AND CLEARED
(6) ;*
(6) ;*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) ;*F/FS OR GATES
(7) ;*
(7) ;* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(7) ;*
(6) ;*
(5) ;*****
(4) 003354 000004 TST12: SCOPE ;/CLEAR THE STATUS REGISTER.
(2) ;/SET BIT 9.
(2) ;/SET FOR ERROR TYPEOUT S/B.
(2) ;/READ THE STATUS REGISTER.
(2) 003356 012737 001000 001124 MOV #BIT9,\$GDDAT
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 003404 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 9 AND ONLY BIT 9 SET?
(2) 003412 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(3) ;:\$> ERROR <<\$
(2) 003414 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;/BIT 9 FAILED TO BIT SET.
(3) ;:\$> ERROR <<\$
(2) 003416 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(2) 003420 CLR \$GDDAT ;/TRY CLEARING BIT 9.
(2) 003420 005037 001124 ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 003444 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(2) 003450 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(3) ;:\$> ERROR <<\$
(2) 003452 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;/BIT 9 FAILED TO CLEAR.
(3) ;:\$> ERROR <<\$
(2) 003454 2\$:

(2) :#
(6) :*****
(5) :*TEST 13 *TEST THAT CLOCK A STATUS REGISTER BIT 8 CAN BE SET AND CLEARED
(6) :*
(6) :*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) :*F/FS OR GATES
(7) :*
(7) :* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(7) :*
(6) :*
(5) :*****
(4) 003454 000004 TST13: SCOPE
(2) :/CLEAR THE STATUS REGISTER.
(2) :/SET BIT 8.
(2) :/SET FOR ERROR TYPEOUT S/B.
(2) :/READ THE STATUS REGISTER.
(2) 003456 012737 000400 001124 MOV #BIT8,\$GDDAT
(3) ;* MOV \$GDDAT,@ASR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT :/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
(2) 003504 023737 001124 001126 CMP \$GDDAT,\$BDDAT :/DID BIT 8 AND ONLY BIT 8 SET?
(2) 003512 001402 BEQ 1\$:/IF SO-LETS TRY CLEARING IT.
(3) ;:\$> ERROR <<\$
(2) 003514 104002 ERROR 2 :/ERROR CLOCK AS STATUS REGISTER.
(2) :/BIT 8 FAILED TO BIT SET.
(3) ;:\$> ERROR <<\$
(2) 003516 000416 1\$: BR 2\$:/BR TO END SUBTEST.
(2) 003520 005037 001124 CLR \$GDDAT :/TRY CLEARING BIT 8.
(2) :/CLEAR S/B FOR TYPEOUT IF ANY.
(2) :/NOW READ IT BACK.
(3) ;* MOV \$GDDAT,@ASR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT :/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
(2) 003544 005737 001126 TST \$BDDAT
(2) 003550 001401 BEQ 2\$:/IF ZERO-NO ERROR!
(3) ;:\$> ERROR <<\$
(2) 003552 104002 ERROR 2 :/ERROR-CLOCK A STATUS REGISTER.
(2) :/BIT 8 FAILED TO CLEAR.
(3) ;:\$> ERROR <<\$
(2) 003554 2\$:

(2) ;#
(6) :*****
(5) *TEST 14 *TEST THAT CLOCK A STATUS REGISTER BIT 7 CAN BE SET AND CLEARED
(6) :*
(6) *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) *F/FS OR GATES
(7) :*
(7) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(7) :*
(6) :*
(5) :*****
(4) 003554 000004 TST14: SCOPE ;/CLEAR THE STATUS REGISTER.
(2) ;/SET BIT 7.
(2) ;/SET FOR ERROR TYPEOUT S/B.
(2) ;/READ THE STATUS REGISTER.
(2) 003556 012737 000200 001124 MOV #BIT7,\$GDDAT ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV \$GDDAT,@ASR ;/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
(3) ;* MOV @ASR,\$BDDAT ;/DID BIT 7 AND ONLY BIT 7 SET?
(2) 003604 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/IF SO-LETS TRY CLEARING IT.
(2) 003612 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(3) ;:\$> ERROR <<\$
(2) 003614 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;/BIT 7 FAILED TO BIT SET.
(3) ;:\$> ERROR <<\$
(2) 003616 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(2) 003620 CLR \$GDDAT ;/TRY CLEARING BIT 7.
(2) 003620 005037 001124 ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
(2) 003644 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(2) 003650 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(3) ;:\$> ERROR <<\$
(2) 003652 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;/BIT 7 FAILED TO CLEAR.
(3) ;:\$> ERROR <<\$
(2) 003654 2\$:

(2) ;#
(6) :*****
(5) *TEST 15 *TEST THAT CLOCK A STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(6) :*
(6) *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) *F/FS OR GATES
(7) :*
(7) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(7) :*
(6) :*
(5) :*****
(4) 003654 000004 TST15: SCOPE
(2) :/CLEAR THE STATUS REGISTER.
(2) :/SET BIT 6.
(2) :/SET FOR ERROR TYPEOUT S/B.
(2) :/READ THE STATUS REGISTER.
(2) 003656 012737 000100 001124 MOV #BIT6,\$GDDAT
(3) :* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) :* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 003704 023737 001124 001126 CMP SGDDAT,\$BDDAT ;/DID BIT 6 AND ONLY BIT 6 SET?
(2) 003712 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(3) ::::::::::::::> ERROR <<:::::::::::::
(2) 003714 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;/BIT 6 FAILED TO BIT SET.
(3) ::::::::::::::> ERROR <<:::::::::::::
(2) 003716 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(2) 003720 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 6.
(2) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) :* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) :* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 003744 005737 001126 TST SBDDAT
(2) 003750 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(3) ::::::::::::::> ERROR <<:::::::::::::
(2) 003752 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;/BIT 6 FAILED TO CLEAR.
(3) ::::::::::::::> ERROR <<:::::::::::::
(2) 003754 2\$:

(2) ;#
(6) ;*****
(5) *TEST 16 *TEST THAT CLOCK A STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
(6) ;*
(6) ;*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) ;*F/FS OR GATES
(7) ;*
(7) ;* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(7) ;*
(6) ;*
(5) ;*****
(4) 003754 000004 TST16: SCOPE
(2) ;/CLEAR THE STATUS REGISTER.
(2) ;/SET BIT 5.
(2) ;/SET FOR ERROR TYPEOUT S/B.
(2) ;/READ THE STATUS REGISTER.
(2) 003756 012737 000040 001124 MOV #BIT5,\$GDDAT
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 004004 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 5 AND ONLY BIT 5 SET?
(2) 004012 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(3) ;:\$> ERROR <<\$
(2) 004014 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;/BIT 5 FAILED TO BIT SET.
(3) ;:\$> ERROR <<\$
(2) 004016 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(2) 004020 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 5.
(2) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 004044 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(2) 004050 001401 BEQ 2\$
(3) ;:\$> ERROR <<\$
(2) 004052 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;/BIT 5 FAILED TO CLEAR.
(3) ;:\$> ERROR <<\$
(2) 004054 2\$:

(2) ;#
(6) :*****
(5) *TEST 17 *TEST THAT CLOCK A STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(6) :*
(6) *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) :*F/FS OR GATES
(7) :*
(7) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(7) :*
(6) :*
(5) :*****
(4) 004054 000004 TST17: SCOPE
(2) ;/CLEAR THE STATUS REGISTER.
(2) ;/SET BIT 3.
(2) ;/SET FOR ERROR TYPEOUT S/B.
(2) ;/READ THE STATUS REGISTER.
(2) 004056 012737 000010 001124 MOV #BIT3,\$GDDAT
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 004104 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 3 AND ONLY BIT 3 SET?
(2) 004112 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(3) ;:\$> ERROR <<\$
(2) 004114 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;/BIT 3 FAILED TO BIT SET.
(3) ;:\$> ERROR <<\$
(2) 004116 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(2) 004120 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 3.
(2) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(2) 004144 005737 001126 TST \$BDDAT
(2) 004150 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(3) ;:\$> ERROR <<\$
(2) 004152 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;/BIT 3 FAILED TO CLEAR.
(3) ;:\$> ERROR <<\$
(2) 004154 2\$:

```

(2)          :/*
(6)          ;*****
(5)          ;*TEST 20      *TEST THAT CLOCK A STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
(6)
(6)          ;*
(6)          ;*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6)          ;*F/FS OR GATES
(7)
(7)          ;* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(7)
(6)
(5)
(4) 004154 000004          TST20: SCOPE
(2)          ;/CLEAR THE STATUS REGISTER.
(2)          ;/SET BIT 2.
(2)          ;/SET FOR ERROR TYPEOUT S/B.
(2)          ;/READ THE STATUS REGISTER.
(2) 004156 012737 000004 001124      MOV    #BIT2,$GDDAT
(3)          ;*      MOV    $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)
(3)          ;*      MOV    @ASR,$BDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004204 023737 001124 001126      CMP    $GDDAT,$BDDAT      ;/DID BIT 2 AND ONLY BIT 2 SET?
(2) 004212 001402      BEQ    1$          ;/IF SO-LETS TRY CLEARING IT.
(3)
(3)          ;:$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(2) 004214 104002          ERROR  2          ;/ERROR CLOCK AS STATUS REGISTER.
(2)          ;/BIT 2 FAILED TO BIT SET.
(3)
(3)          ;:$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(2) 004216 000416          1$:      BR     2$          ;/BR TO END SUBTEST.
(2) 004220 005037 001124      CLR    $GDDAT      ;/TRY CLEARING BIT 2.
(2)          ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2)          ;/NOW READ IT BACK.
(3)
(3)          ;*      MOV    $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)
(3)          ;*      MOV    @ASR,$BDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004244 005737 001126      TST    $BDDAT      ;/IF ZERO-NO ERROR!
(2) 004250 001401      BEQ    2$          ;/IF ZERO-NO ERROR!
(3)
(3)          ;:$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(2) 004252 104002          ERROR  2          ;/ERROR-CLOCK A STATUS REGISTER.
(2)          ;/BIT 2 FAILED TO CLEAR.
(3)
(3)          ;:$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(2) 004254 2$:

```

```

(2)          ;/*
(6)          ;*****
(5)          *TEST 21      *TEST THAT CLOCK A STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
(6)          *
(6)          *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6)          *F/FS OR GATES
(7)          *
(7)          * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(7)          *
(6)          *
(5)          ****
(4) 004254 000004          TST21: SCOPE
(2)          :/CLEAR THE STATUS REGISTER.
(2)          :/SET BIT 1.
(2)          :/SET FOR ERROR TYPEOUT S/B.
(2)          :/READ THE STATUS REGISTER.
(2) 004256 012737 000002 001124          MOV    #BIT1,$GDDAT
(3)          ;*   MOV    $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)          ;*   MOV    @ASR,$BDDAT    ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(3)          ;*   CMP    $GDDAT,$BDDAT  ;/DID BIT 1 AND ONLY BIT 1 SET?
(2) 004304 023737 001124 001126          BEQ    1$           ;/IF SO-LETS TRY CLEARING IT.
(2) 004312 001402
(3)          ::::::::::::::::::::> ERROR <<::::::::::::::::::
(2) 004314 104002          ERROR  2          ;/ERROR CLOCK AS STATUS REGISTER.
(2)          ;/BIT 1 FAILED TO BIT SET.
(3)          ::::::::::::::::::::> ERROR <<::::::::::::::::::
(2) 004316 000416          1$:   BR    2$           ;/BR TO END SUBTEST.
(2) 004320 005037 001124          CLR    $GDDAT      ;/TRY CLEARING BIT 1.
(2)          ;*   MOV    $GDDAT,@ASR      ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2)          ;*   MOV    @ASR,$BDDAT    ;/NOW READ IT BACK.
(3)          ;*   TST    $BDDAT
(2) 004344 005737 001126          BEQ    2$           ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)          ;*   MOV    $GDDAT,@ASR      ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004350 001401
(3)          ::::::::::::::::::::> ERROR <<::::::::::::::::::
(2) 004352 104002          ERROR  2          ;/ERROR-CLOCK A STATUS REGISTER.
(2)          ;/BIT 1 FAILED TO CLEAR.
(3)          ::::::::::::::::::::> ERROR <<::::::::::::::::::
(2) 004354 2$:

```

(2) :/#
(6) :*****
(5) *TEST 22 *TEST THAT CLOCK A STATUS REGISTER BIT 0 CAN BE SET AND CLEARED
(6) *
(6) *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) *F/FS OR GATES
(7) *
(7) * PROBABLE SYNC POINT FOR THIS TEST::: "DEVICE OUT" 2 OCCURANCES PER PASS
(7)
(6)
(5)
(4) 004354 000004 TST22: SCOPE
(2) :/CLEAR THE STATUS REGISTER.
(2) :/SET BIT 0.
(2) :/SET FOR ERROR TYPEOUT S/B.
(2) :/READ THE STATUS REGISTER.
(2) 004356 012737 000001 001124 MOV #BIT0,\$GDDAT
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
(2) 004404 023737 001124 001126 ;* CMP \$GDDAT,\$BDDAT ;/DID BIT 0 AND ONLY BIT 0 SET?
(2) 004412 001402 BEQ 1S ;/IF SO-LETS TRY CLEARING IT.
(3) :::\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(2) 004414 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;/BIT 0 FAILED TO BIT SET.
(3) :::\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(2) 004416 000416 1S: BR 2\$;/BR TO END SUBTEST.
(2) 004420 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 0.
(2) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
(2) 004444 005737 001126 TST \$BDDAT
(2) 004450 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(3) :::\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(2) 004452 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;/BIT 0 FAILED TO CLEAR.
(3) :::\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(2) 004454 2\$:

(3) ://
(7) :*****
(6) *TEST 23 *TEST THAT CLOCK A BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****
(5) 004454 000004 TST23: SCOPE :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 0.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 004456 012737 000001 001124 MOV #BIT0,\$GDDAT :/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
(4) ;* MOV \$GDDAT,@ABR :/ READ DEVICE REG ABR,PUT DATA IN SBDDAT.
(4) ;* MOV @ABR,\$BDDAT :/DID BIT 0 AND ONLY BIT 0 SET?
(3) 004504 023737 001124 001126 CMP \$GDDAT,\$BDDAT :/IF SO-LETS TRY CLEARING IT.
(3) 004512 001402 BEQ * 1S
(4) ::\$>> ERROR <<\$
(3) 004514 104003 ERROR 3 :/ERROR CLOCK AS BUFFER REGISTER.
(3) :/BIT 0 FAILED TO BIT SET.
(4) ::\$>> ERROR <<\$
(3) 004516 000416 BR 2\$:/BR TO END SUBTEST.
(5) 004520 005037 001124 1\$: CLR \$GDDAT :/TRY CLEARING BIT 0.
(3) :/CLEAR S/B FOR TYPEOUT IF ANY.
(3) :/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@ABR :/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT :/READ DEVICE REG ABR,PUT DATA IN SBDDAT.
(3) 004544 005737 001126 TST \$BDDAT
(3) 004550 001401 BEQ 2\$:/IF ZERO-NO ERROR!
(4) ::\$>> ERROR <<\$
(3) 004552 104003 ERROR 3 :/ERROR-CLOCK A BUFFER REGISTER.
(3) :/BIT 0 FAILED TO CLEAR.
(4) ::\$>> ERROR <<\$
(3) 004554 2\$:

(3) //#
(7) *****
(6) *TEST 24 *TEST THAT CLOCK A BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(7)
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8)
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8)
(7)
(6) *****
(5) 004554 000004 TST24: SCOPE //CLEAR THE BUFFER REGISTER.
(3)
(3)
(3)
(3) ://SET BIT 1.
(3) ://SET FOR ERROR TYPEOUT S/B.
(3) ://READ THE BUFFER REGISTER.
(3) 004556 012737 000002 001124 MOV #BIT1,\$GDDAT // PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4)
(4) :* MOV \$GDDAT,@ABR
(4) :* MOV @ABR,\$BDDAT //READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 004604 023737 001124 001126 CMP \$GDDAT,\$BDDAT //DID BIT 1 AND ONLY BIT 1 SET?
(3) 004612 001402 BEQ 1\$ //IF SO-LETS TRY CLEARING IT.
(4) ;;;\$>> ERROR <<\$
(3) 004614 104003 ERROR 3 //ERROR CLOCK AS BUFFER REGISTER.
(3) //BIT 1 FAILED TO BIT SET.
(4) ;;;\$>> ERROR <<\$
(3) 004616 000416 1\$: BR 2\$ //BR TO END SUBTEST.
(3) 004620 005037 001124 CLR \$GDDAT //TRY CLEARING BIT 1.
(3) ;//CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;//NOW READ IT BACK.
(4)
(4) :* MOV \$GDDAT,@ABR // PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) :* MOV @ABR,\$BDDAT //READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 004644 005737 001126 TST \$BDDAT
(3) 004650 001401 BEQ 2\$ //IF ZERO-NO ERROR!
(4) ;;;\$>> ERROR <<\$
(3) 004652 104003 ERROR 3 //ERROR-CLOCK A BUFFER REGISTER.
(3) //BIT 1 FAILED TO CLEAR.
(4) ;;;\$>> ERROR <<\$
(3) 004654 2\$: ;;

(3) ://
(7) :*****
(6) *TEST 25 *TEST THAT CLOCK A BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(7) :*
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) :*
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 004654 000004 TST25: SCOPE :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 2.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 004656 012737 000004 001124 MOV #BIT2,\$GDDAT :/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) :* MOV \$GDDAT,@ABR :/ READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(4) :* MOV @ABR,\$BDDAT :/DID BIT 2 AND ONLY BIT 2 SET?
(3) 004704 023737 001124 001126 CMP \$GDDAT,\$BDDAT :/IF SO-LETS TRY CLEARING IT.
(3) 004712 001402 BEQ 1\$
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 004714 104003 ERROR 3 :/ERROR CLOCK AS BUFFER REGISTER.
(3) :/BIT 2 FAILED TO BIT SET.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 004716 000416 BR 2\$:/BR TO END SUBTEST.
(5) 004720 005037 001124 1\$: CLR \$GDDAT :/TRY CLEARING BIT 2.
(3) :/CLEAR S/B FOR TYPEOUT IF ANY.
(3) :/NOW READ IT BACK.
(4) :* MOV \$GDDAT,@ABR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) :* MOV @ABR,\$BDDAT :/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 004744 005737 001126 TST \$BDDAT
(3) 004750 001401 BEQ 2\$:/IF ZERO-NO ERROR!
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 004752 104003 ERROR 3 :/ERROR-CLOCK A BUFFER REGISTER.
(3) :/BIT 2 FAILED TO CLEAR.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 004754 2\$:

(3) :/#
(7) :*****
(6) *TEST 26 *TEST THAT CLOCK A BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) *
(7) *
(6) *
(5) 004754 000004 TST26: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 3.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 004756 012737 000010 001124 MOV #BIT3,\$GDDAT
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005004 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 3 AND ONLY BIT 3 SET?
(3) 005012 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005014 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 3 FAILED TO BIT SET.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005016 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 005020 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 3.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005044 005737 001126 TST \$BDDAT
(3) 005050 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005052 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 3 FAILED TO CLEAR.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005054 2\$:

(3) ://
(7) ****
(6) *TEST 27 *TEST THAT CLOCK A BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) ****
(5) 005054 000004 TST27: SCOPE
(3) :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 4.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 005056 012737 000020 001124 MOV #BIT4,\$GDDAT
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005104 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 4 AND ONLY BIT 4 SET?
(3) 005112 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;:\$> ERROR <<\$
(3) 005114 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 4 FAILED TO BIT SET.
(4) ;:\$> ERROR <<\$
(3) 005116 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 005120 ;* CLR \$GDDAT ;/TRY CLEARING BIT 4.
(3) 005120 005037 001124 ;* ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005144 005737 001126 TST \$BDDAT
(3) 005150 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ;:\$> ERROR <<\$
(3) 005152 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 4 FAILED TO CLEAR.
(4) ;:\$> ERROR <<\$
(3) 005154 2\$:

(3) ://
(7) :*****
(6) *TEST 30 *TEST THAT CLOCK A BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(7) :*
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) :*
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 005154 000004 TST30: SCOPE
(3) :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 5.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 005156 012737 000040 001124 MOV #BITS,\$GDDAT
(4) :* MOV \$GDDAT,@ABR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) :* MOV @ABR,\$BDDAT :/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005204 023737 001124 001126 CMP \$GDDAT,\$BDDAT :/DID BIT 5 AND ONLY BIT 5 SET?
(3) 005212 001402 BEQ 1\$:/IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005214 104003 ERROR 3 :/ERROR CLOCK AS BUFFER REGISTER.
(3) :/BIT 5 FAILED TO BIT SET.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005216 000416 1\$: BR 2\$:/BR TO END SUBTEST.
(5) 005220 005037 001124 CLR \$GDDAT :/TRY CLEARING BIT 5.
(3) :/CLEAR S/B FOR TYPEOUT IF ANY.
(3) :/NOW READ IT BACK.
(4) :* MOV \$GDDAT,@ABR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) :* MOV @ABR,\$BDDAT :/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005244 005737 001126 TST \$BDDAT
(3) 005250 001401 BEQ 2\$:/IF ZERO-NO ERROR!
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005252 104003 ERROR 3 :/ERROR-CLOCK A BUFFER REGISTER.
(3) :/BIT 5 FAILED TO CLEAR.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005254 2\$:

(3) ;/*
(7) ****
(6) *TEST 31 *TEST THAT CLOCK A BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
(7)
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8)
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8)
(7)
(6)
(5) 005254 000004 TST31: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 6.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 005256 012737 000100 001124 MOV #BIT6,\$GDDAT
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005304 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 6 AND ONLY BIT 6 SET?
(3) 005312 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::::::::> ERROR <:::::::::::::::::::
(3) 005314 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 6 FAILED TO BIT SET.
(4) ::::::::::::::::::::> ERROR <:::::::::::::::::::
(3) 005316 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 005320 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 6.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005344 005737 001126 TST \$BDDAT
(3) 005350 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ::::::::::::::::::::> ERROR <:::::::::::::::::::
(3) 005352 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 6 FAILED TO CLEAR.
(4) ::::::::::::::::::::> ERROR <:::::::::::::::::::
(3) 005354 2\$:

(3) :#
(7) ****
(6) *TEST 32 *TEST THAT CLOCK A BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) *
(7) *
(6) ****
(5) 005354 000004 TST32: SCOPE
(3) :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 7.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 005356 012737 000200 001124 MOV #BIT7,\$GDDAT
(4) ;* MOV \$GDDAT,@ABR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT :/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005404 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 7 AND ONLY BIT 7 SET?
(3) 005412 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005414 104003 ERROR 3 :/ERROR CLOCK AS BUFFER REGISTER.
(3) :/BIT 7 FAILED TO BIT SET.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005416 000416 1\$: BR 2\$:/BR TO END SUBTEST.
(5) 005420 ;* CLR \$GDDAT :/TRY CLEARING BIT 7.
(3) 005420 005037 001124 ;* CLR \$GDDAT :/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;* NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@ABR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT :/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005444 005737 001126 TST \$BDDAT
(3) 005450 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005452 104003 ERROR 3 :/ERROR-CLOCK A BUFFER REGISTER.
(3) :/BIT 7 FAILED TO CLEAR.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 005454 2\$:

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(3) ;#
(7) :*****
(6) *TEST 33 *TEST THAT CLOCK A BUFFER REGISTER BIT 8 CAN BE SET AND CLEARED
(7) :*
(7) :CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :F/FS OR GATES
(8) :*
(8) : PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 005454 000004 TST33: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 8.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 005456 012737 000400 001124 MOV #BIT8,\$GDDAT
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005504 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 8 AND ONLY BIT 8 SET?
(3) 005512 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;;;\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(3) 005514 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 8 FAILED TO BIT SET.
(4) ;;;\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(3) 005516 000416 BR 2\$;/BR TO END SUBTEST.
(5) 005520 005037 001124 1\$: CLR \$GDDAT ;/TRY CLEARING BIT 8.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005544 005737 001126 TST \$BDDAT
(3) 005550 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ;;;\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(3) 005552 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 8 FAILED TO CLEAR.
(4) ;;;\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(3) 005554 2\$:

(3) ;#
(7) :*****
(6) *TEST 34 *TEST THAT CLOCK A BUFFER REGISTER BIT 9 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) *
(5) 005554 000004 TST34: SCOPE
(3) :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 9.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 005556 012737 001000 001124 MOV #BIT9,\$GDDAT
(4) :* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) :* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005604 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 9 AND ONLY BIT 9 SET?
(3) 005612 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) :::\$> ERROR <<\$
(3) 005614 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 9 FAILED TO BIT SET.
(4) :::\$> ERROR <<\$
(3) 005616 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 005620 CLR \$GDDAT ;/TRY CLEARING BIT 9.
(3) 005620 005037 001124 ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) :* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) :* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005644 005737 001126 TST \$BDDAT,
(3) 005650 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) :::\$> ERROR <<\$
(3) 005652 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 9 FAILED TO CLEAR.
(4) :::\$> ERROR <<\$
(3) 005654 2\$:

(3) ;/*
(7) :*****
(6) *TEST 35 *TEST THAT CLOCK A BUFFER REGISTER BIT 10 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****
(5) 005654 000004 TST35: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 10.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 005656 012737 002000 001124 MOV #BIT10,\$GDDAT
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005704 023737 001124 001126 CMP SGDDAT,\$BDDAT ;/DID BIT 10 AND ONLY BIT 10 SET?
(3) 005712 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;:;\$>> ERROR <<\$
(3) 005714 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 10 FAILED TO BIT SET.
(4) ;:;\$>> ERROR <<\$
(3) 005716 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(3) 005720 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 10.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 005744 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(3) 005750 001401 BEQ 2\$
(4) ;:;\$>> ERROR <<\$
(3) 005752 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 10 FAILED TO CLEAR.
(4) ;:;\$>> ERROR <<\$
(3) 005754 2\$:

```

(3)          :/#*****
(7)          :*TEST 36      *TEST THAT CLOCK A BUFFER REGISTER BIT 11 CAN BE SET AND CLEARED
(7)          :*
(7)          :*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7)          :*F/FS OR GATES
(8)          :*
(8)          :* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8)          :*
(7)          :*
(6)          :*****005754 000004***** TST36: SCOPE
(3)          :/CLEAR THE BUFFER REGISTER.
(3)          :/SET BIT 11.
(3)          :/SET FOR ERROR TYPEOUT S/B.
(3)          :/READ THE BUFFER REGISTER.
(3) 005756 012737 004000 001124      MOV    #BIT11,$GDDAT
(4)          ;*      MOV    $GDDAT,@ABR      ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
(4)          ;*      MOV    @ABR,$BDDAT      ;/READ DEVICE REG ABR,PUT DATA IN SBDDAT.
(4) 006004 023737 001124 001126      CMP    $GDDAT,$BDDAT      ;/DID BIT 11 AND ONLY BIT 11 SET?
(3) 006012 001402      BEQ    1$          ;/IF SO-LETS TRY CLEARING IT.
(4)          ;:;$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(3) 006014 104003      ERROR  3          ;/ERROR CLOCK AS BUFFER REGISTER.
(3)          ;/BIT 11 FAILED TO BIT SET.
(4)          ;:;$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(3) 006016 000416      1$:      BR    2$          ;/BR TO END SUBTEST.
(5) 006020 005037 001124      CLR    $GDDAT      ;/TRY CLEARING BIT 11.
(3)          ;*      MOV    $GDDAT,@ABR      ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)          ;*      MOV    @ABR,$BDDAT      ;/NOW READ IT BACK.
(4)          ;*      TST    $BDDAT
(4)          ;*      BEQ    2$          ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
(4)          ;*      MOV    $GDDAT,@ABR      ;/READ DEVICE REG ABR,PUT DATA IN SBDDAT.
(3) 006044 005737 001126      TST    $BDDAT      ;/IF ZERO-NO ERROR!
(3) 006050 001401      BEQ    2$          ;:;$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(3) 006052 104003      ERROR  3          ;/ERROR-CLOCK A BUFFER REGISTER.
(3)          ;/BIT 11 FAILED TO CLEAR.
(4)          ;:;$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(3) 006054      2$:

```

(3) ;#
(7) ;*****
(6) ;*TEST 37 *TEST THAT CLOCK A BUFFER REGISTER BIT 12 CAN BE SET AND CLEARED
(7) ;*
(7) ;*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) ;*F/FS OR GATES
(8) ;*
(8) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) ;*
(7) ;*
(6) ;*****
(5) 006054 000004 TST37: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 12.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 006056 012737 010000 001124 MOV #BIT12,\$GDDAT
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 006104 023737 001124 001126 CMP SGDDAT,\$BDDAT ;/DID BIT 12 AND ONLY BIT 12 SET?
(3) 006112 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;:;\$> ERROR <<\$
(3) 006114 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 12 FAILED TO BIT SET.
(4) ;:;\$> ERROR <<\$
(3) 006116 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 006120 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 12.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 006144 005737 001126 TST SBDDAT
(3) 006150 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ;:;\$> ERROR <<\$
(3) 006152 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 12 FAILED TO CLEAR.
(4) ;:;\$> ERROR <<\$
(3) 006154 2\$: ;

(3) ;#
(7) ****
(6) *TEST 40 *TEST THAT CLOCK A BUFFER REGISTER BIT 13 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) ****
(5) 006154 000004 TST40: SCOPE
(3) :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 13.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 006156 012737 020000 001124 MOV #BIT13,\$GDDAT
(4) ;* MOV \$GDDAT,@ABR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT :/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(4) 006204 023737 001124 001126 CMP \$GDDAT,\$BDDAT :/DID BIT 13 AND ONLY BIT 13 SET?
(3) 006212 001402 BEQ 1S :/IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::>> ERROR <<::::::::::::
(3) 006214 104003 ERROR 3 :/ERROR CLOCK AS BUFFER REGISTER.
(3) :/BIT 13 FAILED TO BIT SET.
(4) ::::::::::::::>> ERROR <<::::::::::::
(3) 006216 000416 BR 2\$:/BR TO END SUBTEST.
(5) 006220 005037 001124 1\$: CLR \$GDDAT :/TRY CLEARING BIT 13.
(3) :/CLEAR S/B FOR TYPEOUT IF ANY.
(3) :/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@ABR :/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT :/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 006244 005737 001126 TST \$BDDAT
(3) 006250 001401 BEQ 2\$:/IF ZERO-NO ERROR!
(4) ::::::::::::::>> ERROR <<::::::::::::
(3) 006252 104003 ERROR 3 :/ERROR-CLOCK A BUFFER REGISTER.
(3) :/BIT 13 FAILED TO CLEAR.
(4) ::::::::::::::>> ERROR <<::::::::::::
(3) 006254 2\$:

(3) ://
(7) :*****
(6) :*TEST 41 *TEST THAT CLOCK A BUFFER REGISTER BIT 14 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 006254 000004 TST41: SCOPE
(3) :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 14.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 006256 012737 040000 001124 MOV #BIT14,\$GDDAT
(4) :* MOV \$GDDAT,@ABR :/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
(4) :* MOV @ABR,\$BDDAT :/READ DEVICE REG ABR,PUT DATA IN SBDDAT.
(3) 006304 023737 001124 001126 CMP \$GDDAT,\$BDDAT :/DID BIT 14 AND ONLY BIT 14 SET?
(3) 006312 001402 BEQ 1\$:/IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 006314 104003 ERROR 3 :/ERROR CLOCK AS BUFFER REGISTER.
(3) :/BIT 14 FAILED TO BIT SET.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 006316 000416 BR 2\$:/BR TO END SUBTEST.
(5) 006320 005037 001124 1\$: CLR \$GDDAT :/TRY CLEARING BIT 14.
(3) :/CLEAR S/B FOR TYPEOUT IF ANY.
(3) :/NOW READ IT BACK.
(4) :* MOV \$GDDAT,@ABR :/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
(4) :* MOV @ABR,\$BDDAT :/READ DEVICE REG ABR,PUT DATA IN SBDDAT.
(3) 006344 005737 001126 TST \$BDDAT :/IF ZERO-NO ERROR!
(3) 006350 001401 BEQ 2\$:/IF ZERO-NO ERROR!
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 006352 104003 ERROR 3 :/ERROR-CLOCK A BUFFER REGISTER.
(3) :/BIT 14 FAILED TO CLEAR.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 006354 2\$:

(3) ;/*
(7) *TEST 42 *TEST THAT CLOCK A BUFFER REGISTER BIT 15 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) *
(7)
(6)
(5) 006354 000004 TST42: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 15.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 006356 012737 100000 001124 MOV #BIT15,\$GDDAT
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 006404 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 15 AND ONLY BIT 15 SET?
(3) 006412 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ::;\$> ERROR <<\$
(3) 006414 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 15 FAILED TO BIT SET.
(4) ::;\$> ERROR <<\$
(3) 006416 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(3) 006420 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 15.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.
(3) 006444 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(3) 006450 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ::;\$> ERROR <<\$
(3) 006452 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 15 FAILED TO CLEAR.
(4) ::;\$> ERROR <<\$
(3) 006454 2\$: ;

(3) :/#
(7) ****
(6) *TEST 43 *TEST THAT CLOCK B STATUS REGISTER BIT 11 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) *
(7) *
(6) *
(5) 006454 000004 TST43: SCOPE
(3) ;/CLEAR THE STATUS REGISTER.
(3) ;/SET BIT 11.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE STATUS REGISTER.
(3) 006456 012737 004000 001124 MOV #BIT11,\$GDDAT
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(3) 006504 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 11 AND ONLY BIT 11 SET?
(3) 006512 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ::;\$>> ERROR <<\$
(3) 006514 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.
(3) ;/BIT 11 FAILED TO BIT SET.
(4) ::;\$>> ERROR <<\$
(3) 006516 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(3) 006520 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 11.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(3) 006544 005737 001126 TST \$BDDAT
(3) 006550 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ::;\$>> ERROR <<\$
(3) 006552 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.
(3) ;/BIT 11 FAILED TO CLEAR.
(4) ::;\$>> ERROR <<\$
(3) 006554 2\$:

(3) ;#
(7) ;*****
(6) *TEST 44 *TEST THAT CLOCK B STATUS REGISTER BIT 7 CAN BE SET AND CLEARED
(7) ;*
(7) ;CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) ;F/FS OR GATES
(8) ;*
(8) ; PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) ;*
(7) ;*
(6) ;*****
(5) 006554 000004 TST44: SCOPE
(3) ;/CLEAR THE STATUS REGISTER.
(3) ;/SET BIT 7.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE STATUS REGISTER.
(3) 006556 012737 000200 001124 MOV #BIT7,\$GDDAT
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(3) 006604 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 7 AND ONLY BIT 7 SET?
(3) 006612 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;:\$> ERROR <<\$
(3) 006614 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.
(3) ;/BIT 7 FAILED TO BIT SET.
(4) ;:\$> ERROR <<\$
(3) 006616 000416 BR 2\$;/BR TO END SUBTEST.
(5) 006620 005037 001124 1\$: CLR \$GDDAT ;/TRY CLEARING BIT 7.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(3) 006644 005737 001126 TST \$BDDAT
(3) 006650 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ;:\$> ERROR <<\$
(3) 006652 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.
(3) ;/BIT 7 FAILED TO CLEAR.
(4) ;:\$> ERROR <<\$
(3) 006654 2\$:

(3) ://
(7) :*****
(6) *TEST 45 *TEST THAT CLOCK B STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(7) :*
(7) *CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) :*
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" ? OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 006654 000004 TST45: SCOPE
(3) :/CLEAR THE STATUS REGISTER.
(3) :/SET BIT 6.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE STATUS REGISTER.
(3) 006656 012737 000100 001124 MOV #BIT6,\$GDDAT
(4) :* MOV \$GDDAT,@BSR :/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) :* MOV @BSR,\$BDDAT :/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(3) 006704 023737 001124 001126 CMP \$GDDAT,\$BDDAT :/DID BIT 6 AND ONLY BIT 6 SET?
(3) 006712 001402 BEQ 1\$:/IF SO-LETS TRY CLEARING IT.
(4) ;:\$> ERROR <<\$
(3) 006714 104005 ERROR 5 :/ERROR CLOCK BS STATUS REGISTER.
(3) :/BIT 6 FAILED TO BIT SET.
(4) ;:\$> ERROR <<\$
(3) 006716 000416 BR 2\$:/BR TO END SUBTEST.
(5) 006720 005037 001124 1\$: CLR \$GDDAT :/TRY CLEARING BIT 6.
(3) :/CLEAR S/B FOR TYPEOUT IF ANY.
(3) :/NOW READ IT BACK.
(4) :* MOV \$GDDAT,@BSR :/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) :* MOV @BSR,\$BDDAT :/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(3) 006744 005737 001126 TST \$BDDAT
(3) 006750 001401 BEQ 2\$:/IF ZERO-NO ERROR!
(4) ;:\$> ERROR <<\$
(3) 006752 104005 ERROR 5 :/ERROR-CLOCK B STATUS REGISTER.
(3) :/BIT 6 FAILED TO CLEAR.
(4) ;:\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(3) 006754 2\$:

(3) :#
(7) ****
(6) *TEST 46 *TEST THAT CLOCK B STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) *
(7) *
(6) ****
(5) 006754 000004 TST46: SCOPE
(3) ;/CLEAR THE STATUS REGISTER.
(3) ;/SET BIT 5.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE STATUS REGISTER.
(3) 006756 012737 000040 001124 MOV #BITS,\$GDDAT
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(4) 007004 023737 001124 001126 ;* CMP \$GDDAT,\$BDDAT ;/DID BIT 5 AND ONLY BIT 5 SET?
(3) 007012 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;:\$> ERROR <<\$
(3) 007014 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.
(3) ;/BIT 5 FAILED TO BIT SET.
(4) ;:\$> ERROR <<\$
(3) 007016 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 007020 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 5.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(4) 007044 005737 001126 TST \$BDDAT
(3) 007050 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ;:\$> ERROR <<\$
(3) 007052 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.
(3) ;/BIT 5 FAILED TO CLEAR.
(4) ;:\$> ERROR <<\$
(3) 007054 2\$: ;

(3) :/*
(7) :*****
(6) :*TEST 47 *TEST THAT CLOCK B STATUS REGISTER BIT 4 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 007054 000004 TST47: SCOPE :/CLEAR THE STATUS REGISTER.
(3) :/SET BIT 4.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE STATUS REGISTER.
(3) 007056 012737 000020 001124 MOV #BIT4,\$GDDAT :/PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) :* MOV \$GDDAT,@BSR :/ READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(4) :* MOV @BSR,\$BDDAT :/DID BIT 4 AND ONLY BIT 4 SET?
(3) 007104 023737 001124 001126 CMP \$GDDAT,\$BDDAT :/IF SO-LETS TRY CLEARING IT.
(3) 007112 001402 BEQ 1\$
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 007114 104005 ERROR 5 :/ERROR CLOCK BS STATUS REGISTER.
(3) :/BIT 4 FAILED TO BIT SET.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 007116 000416 1\$: BR 2\$:/BR TO END SUBTEST.
(5) 007120 005037 001124 CLR \$GDDAT :/TRY CLEARING BIT 4.
(3) :/CLEAR S/B FOR TYPEOUT IF ANY.
(3) :/NOW READ IT BACK.
(4) :* MOV \$GDDAT,@BSR :/PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) :* MOV @BSR,\$BDDAT :/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(3) 007144 005737 001126 TST \$BDDAT :/IF ZERO-NO ERROR!
(3) 007150 001401 BEQ 2\$
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 007152 104005 ERROR 5 :/ERROR-CLOCK B STATUS REGISTER.
(3) :/BIT 4 FAILED TO CLEAR.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 007154 2\$:

(3) ;#
(7) :*****
(6) *TEST 50 *TEST THAT CLOCK B STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 007154 000004 TST50: SCOPE
(3) :/CLEAR THE STATUS REGISTER.
(3) :/SET BIT 3.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE STATUS REGISTER.
(3) 007156 012737 000010 001124 MOV #BIT3,\$GDDAT
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(3) 007204 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 3 AND ONLY BIT 3 SET?
(3) 007212 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;:;\$> ERROR <<\$
(3) 007214 104005 ERROR 5 ;/ERROR CLOCK B STATUS REGISTER.
(3) ;/BIT 3 FAILED TO BIT SET.
(4) ;:;\$> ERROR <<\$
(3) 007216 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 007220 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 3.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(3) 007244 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(3) 007250 001401 BEQ 2\$
(4) ;:;\$> ERROR <<\$
(3) 007252 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.
(3) ;/BIT 3 FAILED TO CLEAR.
(4) ;:;\$> ERROR <<\$
(3) 007254 2\$: ;

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T50 *TEST THAT CLOCK B STATUS REGISTER BIT 3 CAN BE SET AND CLEARED

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(3)          ;/*
(7)          :*TEST 51      *TEST THAT CLOCK B STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
(6)
(7)          :*CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7)          :*F/FS OR GATES
(8)          :*
(8)          :* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8)
(7)
(6)
(5) 007254 000004          TST51: SCOPE
(3)          :/*CLEAR THE STATUS REGISTER.
(3)          :/SET BIT 2.
(3)          :/SET FOR ERROR TYPEOUT S/B.
(3)          :/READ THE STATUS REGISTER.
(3) 007256 012737 000004 001124      MOV      #BIT2,$GDDAT
(4)          ;*      MOV      $GDDAT,@BSR      :/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4)
(4)          ;*      MOV      @BSR,$BDDAT      :/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 007304 023737 001124 001126      CMP      $GDDAT,$BDDAT      :/DID BIT 2 AND ONLY BIT 2 SET?
(3) 007312 001402              BEQ      1$      :/IF SO-LETS TRY CLEARING IT.
(4)
(4)          ;;;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(3) 007314 104005          ERROR    5      :/ERROR CLOCK BS STATUS REGISTER.
(3)          :/BIT 2 FAILED TO BIT SET.
(4)
(4)          ;;;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(3) 007316 000416          1$:      BR      2$      :/BR TO END SUBTEST.
(5) 007320              CLR      $GDDAT      :/TRY CLEARING BIT 2.
(3) 007320 005037 001124      ;*      MOV      $GDDAT,@BSR      :/CLEAR S/B FOR TYPEOUT IF ANY.
(3)          :/NOW READ IT BACK.
(4)
(4)          ;*      MOV      $GDDAT,@BSR      :/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4)
(4)          ;*      MOV      @BSR,$BDDAT      :/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 007344 005737 001126      TST      $BDDAT      :/IF ZERO-NO ERROR!
(3) 007350 001401              BEQ      2$      :/IF ZERO-NO ERROR!
(4)
(4)          ;;;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(3) 007352 104005          ERROR    5      :/ERROR-CLOCK B STATUS REGISTER.
(3)          :/BIT 2 FAILED TO CLEAR.
(4)
(4)          ;;;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
(3) 007354          2$:

```

(3) ;#
(7) ;*****
(6) ;*TEST 52 *TEST THAT CLOCK B STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
(7) ;*
(7) ;*CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) ;*F/FS OR GATES
(8) ;*
(8) ;* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) ;*
(7) ;*
(6) ;*****
(5) 007354 000004 TST52: SCOPE ;/CLEAR THE STATUS REGISTER.
(3) ;/SET BIT 1.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE STATUS REGISTER.
(3) 007356 012737 000002 001124 MOV #BIT1,\$GDDAT ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) ;* MOV \$GDDAT,@BSR ;/READ DEVICE REG BSR,PUT DATA IN SBDDAT.
(4) ;* MOV @BSR,\$BDDAT ;/DID BIT 1 AND ONLY BIT 1 SET?
(3) 007404 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/IF SO-LETS TRY CLEARING IT.
(3) 007412 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;:;\$> ERROR <<\$
(3) 007414 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.
(3) ;/BIT 1 FAILED TO BIT SET.
(4) ;:;\$> ERROR <<\$
(3) 007416 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 007420 CLR \$GDDAT ;/TRY CLEARING BIT 1.
(3) 007420 005037 001124 ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN SBDDAT.
(3) 007444 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(3) 007450 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ;:;\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(3) 007452 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.
(3) ;/BIT 1 FAILED TO CLEAR.
(4) ;:;\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
(3) 007454 2\$: ;

(3) ;/*
(7) :*****
(6) *TEST 53 *TEST THAT CLOCK B STATUS REGISTER BIT 0 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****
(5) 007454 000004 TST53: SCOPE
(3) :/CLEAR THE STATUS REGISTER.
(3) :/SET BIT 0.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE STATUS REGISTER.
(3) 007456 012737 000001 001124 MOV #BIT0,\$GDDAT
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM SGDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN SBDDAT.
(3) 007504 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 0 AND ONLY BIT 0 SET?
(3) 007512 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;:;\$> ERROR <<\$
(3) 007514 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.
(3) ;/BIT 0 FAILED TO BIT SET.
(4) ;:;\$> ERROR <<\$
(3) 007516 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 007520 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 0.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM SGDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN SBDDAT.
(3) 007544 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(3) 007550 001401 BEQ 2\$
(4) ;:;\$> ERROR <<\$
(3) 007552 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.
(3) ;/BIT 0 FAILED TO CLEAR.
(4) ;:;\$> ERROR <<\$
(3) 007554 2\$:

(3) ;#
(7) :*****
(6) *TEST 54 *TEST THAT CLOCK B BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(7) :*
(7) *CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) :*
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 007554 000004 TST54: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 0.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 007556 012737 000001 001124 MOV #BIT0,\$GDDAT
(4) ;* MOV \$GDDAT,\$BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) ;* MOV \$BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 007604 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 0 AND ONLY BIT 0 SET?
(3) 007612 001402 BEQ 1S ;/IF SO-LETS TRY CLEARING IT.
(4) ;:SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS> ERROR <>SSSSSSSSSSSSSSSSSSSSSSSSSS
(3) 007614 104006 ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.
(3) ;/BIT 0 FAILED TO BIT SET.
(4) ;:SSSSSSSSSSSSSSSSSSSSSSSSSS> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
(3) 007616 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 007620 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 0.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,\$BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) ;* MOV \$BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 007644 005737 001126 TST \$BDDAT
(3) 007650 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ;:SSSSSSSSSSSSSSSSSSSSSSSSSS> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
(3) 007652 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
(3) ;/BIT 0 FAILED TO CLEAR.
(4) ;:SSSSSSSSSSSSSSSSSSSSSSSSSS> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
(3) 007654 2\$:

(3) //#
(7) :*****
(6) *TEST 55 *TEST THAT CLOCK B BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(7) /*
(7) *CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) /*
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) /*
(7) /*
(6) :*****
(5) 007654 000004 TST55: SCOPE
(3) /*CLEAR THE BUFFER REGISTER.
(3) /*SET BIT 1.
(3) /*SET FOR ERROR TYPEOUT S/B.
(3) /*READ THE BUFFER REGISTER.
(3) 007656 012737 000002 001124 MOV #BIT1,\$GDDAT
(4) /* MOV \$GDDAT,@BBR /* PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) /* MOV @BBR,\$BDDAT /*READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 007704 023737 001124 001126 CMP \$GDDAT,\$BDDAT /*DID BIT 1 AND ONLY BIT 1 SET?
(3) 007712 001402 BEQ 1\$ /*IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 007714 104006 ERROR 6 /*ERROR CLOCK B BUFFER REGISTER.
(3) /*BIT 1 FAILED TO BIT SET.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 007716 000416 BR 2\$ /*BR TO END SUBTEST.
(5) 007720 005037 001124 1\$: CLR \$GDDAT /*TRY CLEARING BIT 1.
(3) /*CLEAR S/B FOR TYPEOUT IF ANY.
(3) /*NOW READ IT BACK.
(4) /* MOV \$GDDAT,@BBR /* PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) /* MOV @BBR,\$BDDAT /*READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 007744 005737 001126 TST \$BDDAT /*IF ZERO-NO ERROR!
(3) 007750 001401 BEQ 2\$ /*
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 007752 104006 ERROR 6 /*ERROR-CLOCK B BUFFER REGISTER.
(3) /*BIT 1 FAILED TO CLEAR.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 007754 2\$:

(3) :#
(7) :*****
(6) *TEST 56 *TEST THAT CLOCK B BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(7) *
(7) :CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :F/FS OR GATES
(8) *
(8) : PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) *
(7) :
(6) :*****
(5) 007754 000004 TST56: SCOPE
(3) :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 2.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 007756 012737 000004 001124 MOV #BIT2,\$GDDAT
(4) ;* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010004 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 2 AND ONLY BIT 2 SET?
(3) 010012 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 010014 104006 ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.
(3) ;/BIT 2 FAILED TO BIT SET.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 010016 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 010020 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 2.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010044 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(3) 010050 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 010052 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
(3) ;/BIT 2 FAILED TO CLEAR.
(4) ::::::::::::::> ERROR <<:::::::::::::
(3) 010054 2\$:

(3) ;#
(7) ****
(6) *TEST 57 *TEST THAT CLOCK B BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
(7)
(7) *CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8)
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8)
(7)
(6) ****
(5) 010054 000004 TST57: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 3.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 010056 012737 000010 001124 MOV #BIT3,\$GDDAT
(4) ;* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010104 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 3 AND ONLY BIT 3 SET?
(3) 010112 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::::::::> ERROR <:::::::::::::::::::
(3) 010114 104006 ERROR 6 ;/ERROR CLOCK B BUFFER REGISTER.
(3) ;/BIT 3 FAILED TO BIT SET.
(4) ::::::::::::::::::::> ERROR <:::::::::::::::::::
(3) 010116 000416 BR 2\$;/BR TO END SUBTEST.
(5) 010120 005037 001124 1\$: CLR \$GDDAT ;/TRY CLEARING BIT 3.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010144 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(3) 010150 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ::::::::::::::::::::> ERROR <:::::::::::::::::::
(3) 010152 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
(3) ;/BIT 3 FAILED TO CLEAR.
(4) ::::::::::::::::::::> ERROR <:::::::::::::::::::
(3) 010154 2\$:

(3) ;#
(7) ****
(6) *TEST 60 *TEST THAT CLOCK B BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) *
(5) 010154 000004 TST60: SCOPE
(3) :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 4.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 010156 012737 000020 001124 MOV #BIT4,\$GDDAT
(4) :* MOV \$GDDAT,ABBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) :* MOV ABBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010204 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 4 AND ONLY BIT 4 SET?
(3) 010212 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::::::::> ERROR <<:::::::::::::::::::
(3) 010214 104006 ERROR 6 ;/ERROR CLOCK B BUFFER REGISTER.
(3) ;/BIT 4 FAILED TO BIT SET.
(4) ::::::::::::::::::::> ERROR <<:::::::::::::::::::
(3) 010216 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 010220 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 4.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) :* MOV \$GDDAT,ABBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) :* MOV ABBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010244 005737 001126 TST \$BDDAT
(3) 010250 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ::::::::::::::::::::> ERROR <<:::::::::::::::::::
(3) 010252 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
(3) ;/BIT 4 FAILED TO CLEAR.
(4) ::::::::::::::::::::> ERROR <<:::::::::::::::::::
(3) 010254 2\$:

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T60 *TEST THAT CLOCK B BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED

SEQ 0083

(3) ;/*
(7) :*****
(6) *TEST 61 *TEST THAT CLOCK B BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(7) :*
(7) :CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 010254 000004 TST61: SCOPE
(3) :CLEAR THE BUFFER REGISTER.
(3) :SET BIT 5.
(3) :SET FOR ERROR TYPEOUT S/B.
(3) :READ THE BUFFER REGISTER.
(3) 010256 012737 000040 001124 MOV #BITS,\$GDDAT
(4) :* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) :* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010304 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 5 AND ONLY BIT 5 SET?
(3) 010312 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;:\$>> ERROR <<\$
(3) 010314 104006 ERROR 6 ;/ERROR CLOCK B BUFFER REGISTER.
(3) ;/BIT 5 FAILED TO BIT SET.
(4) ;:\$>> ERROR <<\$
(3) 010316 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 010320 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 5.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) :* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) :* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010344 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(3) 010350 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ;:\$>> ERROR <<\$
(3) 010352 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
(3) ;/BIT 5 FAILED TO CLEAR.
(4) ;:\$>> ERROR <<\$
(3) 010354 2\$:

(3) ;/*
(7) ****
(6) *TEST 62 *TEST THAT CLOCK B BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) *
(7) *
(6) ****
(5) 010354 000004 TST62: SCOPE
(3) :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 6.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 010356 012737 000100 001124 MOV #BIT6,\$GDDAT
(4) :* MOV \$GDDAT,@BBR :/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) :* MOV @BBR,\$BDDAT :/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010404 023737 001124 001126 CMP \$GDDAT,\$BDDAT :/DID BIT 6 AND ONLY BIT 6 SET?
(3) 010412 001402 BEQ 1\$:/IF SO-LETS TRY CLEARING IT.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 010414 104006 ERROR 6 :/ERROR CLOCK B BUFFER REGISTER.
(3) :/BIT 6 FAILED TO BIT SET.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 010416 000416 1\$: BR 2\$:/BR TO END SUBTEST.
(5) 010420 005037 001124 CLR \$GDDAT :/TRY CLEARING BIT 6.
(3) :/CLEAR S/B FOR TYPEOUT IF ANY.
(3) :/NOW READ IT BACK.
(4) :* MOV \$GDDAT,@BBR :/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) :* MOV @BBR,\$BDDAT :/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010444 005737 001126 TST \$BDDAT
(3) 010450 001401 BEQ 2\$:/IF ZERO-NO ERROR!
(4) ::::::::::::::> ERROR <:::::::::::
(3) 010452 104006 ERROR 6 :/ERROR-CLOCK B BUFFER REGISTER.
(3) :/BIT 6 FAILED TO CLEAR.
(4) ::::::::::::::> ERROR <:::::::::::
(3) 010454 2\$:

(3) ;/*
(7) :*****
(6) *TEST 63 *TEST THAT CLOCK B BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****
(5) 010454 000004 TST63: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 7.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 010456 012737 000200 001124 MOV #BIT7,\$GDDAT
(4) ;* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010504 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 7 AND ONLY BIT 7 SET?
(3) 010512 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(4) ;;;\$>> ERROR <<\$
(3) 010514 104006 ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.
(3) ;/BIT 7 FAILED TO BIT SET.
(4) ;;;\$>> ERROR <<\$
(3) 010516 000416 1\$: BR 2\$;/BR TO END SUBTEST.
(5) 010520 005037 001124 CLR \$GDDAT ;/TRY CLEARING BIT 7.
(3) ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.
(3) 010544 005737 001126 TST \$BDDAT ;/IF ZERO-NO ERROR!
(3) 010550 001401 BEQ 2\$;/IF ZERO-NO ERROR!
(4) ;;;\$>> ERROR <<\$
(3) 010552 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
(3) ;/BIT 7 FAILED TO CLEAR.
(4) ;;;\$>> ERROR <<\$
(3) 010554 2\$: .SBTTL *
(3) .SBTTL * PHASE 2 ADVANCED BASIC LOGIC TESTS
(3) .SBTTL *
(3) ;*****
1779
1780
1781
1782
1788
1789

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T64 *TEST THAT CLOCK A'S COUNT REGISTER IS CLEAR

SEQ 0086

(3) :*TEST 64 *TEST THAT CLOCK A'S COUNT REGISTER IS CLEAR
(4)
(5)
(5) :*CLOCK A COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5) :*F/FS OR GATES
(6)
(6) :* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(6)
(5)
(4)
(3)
(2) 010554 000004 TST64: SCOPE
1790
1791 :SELECT MODE 0.
1792 :CLEAR THE BUFFER REGISTER. BUFFER
1793 :REGISTER WILL BE TRANSFERRED TO
1794 :COUNT REGISTER SINCE THIS IS MODE 0.
1795 010556 005037 001124 CLR SGDDAT
1796 (1) :* MOV SGDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
1797 (1) :* MOV SGDDAT,@ABR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
1798 010602 005037 001124 CLR SGDDAT ;EXPECT TO READ BACK ALL 0'S.
1800 ;READ THE COUNT REGISTER - IT SHOULD BE CLEAR.
1801 (1) 010616 005737 001126 :* MOV @ACR,\$BDDAT ;READ DEVICE REG ACR,PUT DATA IN SBDDAT.
1802 010622 001401 TST \$BDDAT 1\$;BR IF YES TO NEXT TEST
1803
1804
1805 :;;\$> ERROR <<\$
1806 010624 104004 ERROR 4 ;ERROR - CLOCK A'S COUNTER REGISTER
1807 ;NOT CLEAR.
1808
1809 :;;\$> ERROR <<\$
1810 010626 1\$:
1811
1812 (3) :*TEST 65 *TEST CLOCK A'S COUNT REGISTER WITH 125252 PATTERN
(4)
(5)
(5) :*CLOCK A COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5) :*F/FS OR GATES
(6)
(6) :* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
(6)
(5)
(4)
(3)
(2) 010626 000004 TST65: SCOPE
1813 ;SELECT MODE 0.
1814

1815
1816
1817
1818
1819 010630 005037 001124 CLR \$GDDAT :LOAD THE BUFFER REGISTER WITH
1820 (1) ;* MOV \$GDDAT,@ASR ;PATTERN 125252. IT WILL BE
1821 010644 012737 125252 001124 MOV #125252,\$GDDAT ;TRANSFERRED TO THE COUNT REGISTER
1822 (1) ;* MOV \$GDDAT,@ABR ;SINCE THIS IS MODE 0.
1823 (1) ;* MOV @ACR,\$BDDAT ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
1824 (1) ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
1825 010672 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;SET EXPECTED TO PATTERN IN CASE OF
1826 (1) ;NEED OF ERROR TYPEOUT.
1827 010700 001401 BEQ 1\$;READ THE COUNT REGISTER
1828 (1) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
1829 (1) ;* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
1830 (1) ;CMP \$GDDAT,\$BDDAT ;DID ALL THE BITS AND NO OTHER BITS
1831 (1) ;BEQ 1\$;COME THROUGH?
1832 (1) ;* MOV \$GDDAT,@ABR ;BR IF YES TO NEXT TEST.
1833 010702 104004 ERROR 4 ;:DATA ERROR CLOCK A PATTERN '125252'
1834 (1) ;FAILED TO TRANSFER PROPERLY BETWEEN
1835 (1) ;BUFFER AND COUNT REGISTERS.
1836 (1) ;
1837 (1) ;
1838 010704 1\$: ;
1839 (1) ;*****
1840 (3) ;*TEST 66 *TEST CLOCK A'S COUNT REGISTER WITH 052525 PATTERN
1841 (4)
1842 (5)
1843 (5) ;*CLOCK A COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
1844 (5) ;*F/FS OR GATES
1845 (6)
1846 (6) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
1847 (6)
1848 (5)
1849 (4)
1850 (3) ;
1851 (2) 010704 000004 TST66: SCOPE ;
1852 (1) ;SELECT MODE 0.
1853 010706 005037 001124 CLR \$GDDAT ;
1854 (1) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
1855 (1) ;LOAD THE BUFFER REGISTER WITH
1856 (1) ;PATTERN 052525. IT WILL BE
1857 (1) ;TRANSFERRED TO THE COUNT REGISTER
1858 (1) ;SINCE THIS IS MODE 0.
1859 010722 012737 052525 001124 MOV #052525,\$GDDAT ;SET EXPECTED TO PATTERN IN CASE OF

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T66 *TEST CLOCK A'S COUNT REGISTER WITH 052525 PATTERN

SEQ 0088

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1851 ;NEED OF ERROR TYPEOUT.
1852 ;READ THE COUNT REGISTER
1853
1854 (1) ;*
1855 (1) ;*
1856 010750 023737 001124 001126 MCV $GDDAT,0ABR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
1857 ;*
1858 010756 001401 MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN SBDDAT.
1859
1860
1861 010760 104004 CMP $GDDAT,$BDDAT ;DID ALL THE BITS AND NO OTHER BITS
1862 ;COME THROUGH?
1863 BEQ 1$ ;BR IF YES TO NEXT TEST.
1864
1865 ;;;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$>>
1866 010762 1$: ;DATA ERROR CLOCK A PATTERN '052525'
1867 ;FAILED TO TRANSFER PROPERLY BETWEEN
1868 ;BUFFER AND COUNT REGISTERS.
1869
1870 ;;;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$>>
1871
1872 010762 ;*****
1873 ;*TEST 67 *TEST THAT CLOCK B'S COUNT REGISTER IS CLEAR
1874 (3)
1875 (4)
1876 (5)
1877 (5)
1878 (5)
1879 (6)
1880 (6)
1881 (6)
1882 (6)
1883 (6)
1884 (6)
1885 (6)
1886 (6)
1887 (6)
1888 (6)
1889 (6)
1890 (6)

1874 ;*TEST 67 *TEST THAT CLOCK B'S COUNT REGISTER IS CLEAR
1875 ;*****
1876 ;*CLOCK B COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
1877 ;*F/FS OR GATES
1878 ;*
1879 ;* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
1880 ;*
1881 ;*
1882 ;*
1883 ;*****
1884 010762 000004 TST67: SCOPE ;SELECT MODE 0.
1885 ;CLEAR THE BUFFER REGISTER. BUFFER
1886 ;REGISTER WILL BE TRANSFERRED TO
1887 ;COUNT REGISTER SINCE THIS IS MODE 0.
1888
1889 010764 005037 001124 CLR $GDDAT ;/
1890 (1) ;*
1891 (1) ;*
1892 (1) ;*
1893 011010 005037 001124 CLR $GDDAT ;EXPECT TO READ BACK ALL 0'S.
1894 ;READ THE COUNT REGISTER - IT SHOULD BE CLEAR.
1895
1896 (1) ;*
1897 011024 005737 001126 MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN SBDDAT.
1898 TST SBDDAT ;*
1899 BEQ 1$ ;BR IF YES TO NEXT TEST
1900

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T67 *TEST THAT CLOCK B'S COUNT REGISTER IS CLEAR

SEA 0089

1924 011112 1\$:
1925
1926 ;*****
1927 (3) *TEST 71 *TEST CLOCK B'S COUNT REGISTER WITH 252 PATTERN
1928 (4)
1929 (5)
1930 (5) *CLOCK B COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
1931 (5) *F/FS OR GATES
1932 (6) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
1933 (6)
1934 (6)
1935 (6)
1936 (6)
1937 (6)
1938 (6)
1939 (6)
1940 (6)
1941 (6)
1942 011156 023737 001124 001126 CMP \$GDDAT,\$BDDAT :DID ALL THE BITS AND NO OTHER BITS
1943 011164 001401 BEQ 1\$:COME THROUGH?
1944 :BR IF YES TO NEXT TEST.
1945
1946 ;;;\$>> ERROR <<\$
1947 011166 104007 ERROR 7 :DATA ERROR CLOCK B - PATTERN "252"
1948 :FAILED TO TRANSFER PROPERLY BETWEEN
1949 :BUFFER AND COUNT REGISTERS.
1950
1951 ;;;\$>> ERROR <<\$
1952 011170 1\$:
1953
1954
1955
1956 ;*****
1957 (3) *TEST 72 *TEST THE SETTING OF MAINTENANCE STP1 IN CLOCK A BIT 15 TO SET
1958 (4)
1959 (4) *NEW SIGNALS GENERATION OF "STP1" BY 'LD STAT A' H + 'BD 12' H
1960 (5)
1961 (5) * PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 PER PASS

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T72 *TEST THE SETTING OF MAINTENANCE STP1 IN CLOCK A BIT 15 TO SET

N 7
SEQ 0091

(5)
(4)
(3)
(2) 011170 000004
1969
1970 011172 005037 001124 TST72: SCOPE
1971 CLR SGDDAT
1972 ;* MOV SGDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
1973 ;* MOV @ASR,SGDDAT ;/READ DEVICE REG ASR,PUT DATA IN SGDDAT.
1974 ;MAKE SURE THE STATUS REGISTER IS CLEAR.
1975 011216 012737 010000 001124 ;SET MAINTENANCE STP1.
1976 MOV #BIT12,SGDDAT
1977 ;* MOV SGDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
1978 ;DID BIT15 (STP1 FLAG) SET?
1979
1980 011244 005737 001126 ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
1981 011250 100401 TST \$BDDAT
1982 BMI 1\$;BR IF YES - NEXT TEST
1983
1984 011252 104001 ;;;\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$
1985 ERROR 1 ;ERROR - MAINTENANCE STP1 (BIT12)
1986 ;DID NOT SET BIT15 (STP1 FLAG) CLOCK A.
1987 ;;;\$> ERROR <<\$
1988 011254 1\$:
1989
1990
1991
1992
1993 ;*TEST 73 *TEST THAT BIT00 IN CLOCK A STATUS REG. WILL SET WHEN BIT13 AND MAIN. ST
1994 ;*NEW SIGNALS "STP1" H + "ST1 ENB CNTR (1)" H DIRECT SETTING
1995 ;* "ST1 FLAG"
1996 ;* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 PER PASS
1997
1998 ;*
1999
2000 011254 000004 TST73: SCOPE
2001 ;SET "ST1 ENB COUNTER" IN CLK A'S STATUS REG.
2002 ;GENERATE A MAINTENANCE ST1.
2003 011256 012737 020000 001124 MOV #BIT13,SGDDAT ;DID BIT00 (ENABL CNTR A) SET?
2004 ;* MOV SGDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
2005 ;* MOV @ASR,SGDDAT ;/READ DEVICE REG ASR,PUT DATA IN SGDDAT.
2006 011304 052737 010000 001124 BIS #BIT12,SGDDAT
2007

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T73 *TEST THAT BIT00 IN CLOCK A STATUS REG. WILL SET WHEN BIT13 AND MAIN. STP SEQ 0092

(1) 2008 :* MOV SGDDAT, @ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(1) 2009 011332 032737 000001 001126 :* MOV @ASR, \$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
2010 011340 001001 BIT #BIT00,\$BDDAT
2011 BNE 1S ;BR IF YES - NEXT TEST.
2012
2013 011342 104001 ::::::::::::::::::::> ERROR <<::::::::::::::::::
2014 2015 2016 2017 :ERROR - BIT00 OF CLOCK A'S STATUS REGISTER
:FAILED TO SET WHEN BIT13 WAS SET
:AND A MAINTENANCE ST1 GENERATED.
2018 011344 1S: CLR SGDDAT ;LEAVE SUBTEST WITH CLOCK CLEAR.
2019 011344 005037 001124 :* MOV SGDDAT, @ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
2020
(1) 2021
2022 2023
2024 011344 :*****
011344 :*TEST 74 *TEST THAT CLOCK A WILL INCREMENT - MODE 0 - RATE STP1 FIRST COUNT TEST
011344 :*
011344 :*COUNT TEST - THIS IS THE VERY FIRST TIME THAT THE COUNTER
011344 :*HAS BEEN ASKED TO INCREMENT! WHAT WE ARE GOING TO DO IS
011344 :*CLEAR THE BUFFER, SELECT MODE 0, RATE OF STP1.
011344 :*NEXT WILL GENERATE THE STP1 THROUGH MAINTENANCE MODE (WE'VE
011344 :*DONE THIS BEFORE IN A PREVIOUS TEST TO SEE IF THE FLAG WOULD SET)
011344 :*AND SEE IF THE COUNTER HAS INCREMENTED.
011344 :*
011344 :* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
011344 :*
011344 :*
011344 :*****
011360 000004 TST74: SCOPE .
011360 :CLEAR CLOCK A.
011360 :CLEAR BUFFER REGISTER.
011362 005037 001124 CLR SGDDAT
011362 :* MOV SGDDAT, @ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
011362 :* MOV SGDDAT, @ABR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
011362 :SELECT: MODE0! RATE "STP1" AND ENABLE
011362 :CLOCK A TO COUNT.
011362 :NOW GENERATE A MAINTENANCE STP1 - AT
011362 :THIS TIME THE CLOCK SHOULD COUNT ONCE.
011406 012737 000015 001124 MOV #15, SGDDAT
011406 :* MOV SGDDAT, @ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
011434 052737 010000 001124 :* MOV @ASR, SGDDAT ;/READ DEVICE REG ASR,PUT DATA IN SGDDAT.
011434 BIS #BIT12, SGDDAT
011434

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T74 *TEST THAT CLOCK A WILL INCREMENT - MODE 0 - RATE STP1 FIRST COUNT TEST SEQ 0093

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T75 *TEST THE ABILITY OF CLOCK A TO COUNT FROM ZERO TO OVERFLOW USING M STP1' SEQ 0094

2095
2096
2097
2098 011534 012737 000015 001354 MOV #15,\$TMDAT
2099 (1) :* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
2100 ;ENABLE COUNTER TO COUNT. SELECTED:
2101 ;MODE 0, RATE "STP1"
2102 011552 2\$:
2103 (1) 011562 052737 010000 001354 :* MOV @ASR,\$TMDAT #BIT12,\$TMDAT ;/ READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
2104 (1) :* MOV \$TMDAT,@ASR ;GENERATE A MAINTENANCE "STP1". THIS
2105 ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
2106 011600 005237 001124 INC \$GDDAT ;ONE VALUE.
2107 ;\$GDDAT IS USED TO KEEP TRACK OF THE
2108 ;VALUE THE CLOCK SHOULD COUNT TO.
2109 (1) :* MOV @ACR,\$BDDAT ;/ READ DEVICE REG ACR,PUT DATA IN SBDDAT.
2110 2111 011614 023737 001126 001124 CMP \$BDDAT,\$GDDAT ;DID COUNT OCCUR CORRECTLY?
2112 011622 001402 BEQ 3\$;IF YES - BR TO '3\$'.
2113
2114 ;:;\$>> ERROR <<\$
2115 011624 104011 ERROR 11 ;ERROR - CLOCK A FAILED TO UPCOUNT
2116 ;CORRECTLY USING MODE 0 - RATE "STP1".
2117
2118 ;:;\$>> ERROR <<\$
2119 011626 000403 3\$: BR 4\$
2120 011630 005737 001124 TST \$GDDAT ;DID WE ACHIEVE OVERFLOW TO ZERO YET?
2121 011634 001410 BEQ 5\$;IF YES - BR NEXT TEST
2122
2123 011636 032777 040000 167274 4\$: BIT #BIT14,@ASWR ;LOOP CURRENT COUNT?
2124 011644 001742 BEQ 2\$;BR IF NO TO NEXT COUNT UPDATE.
2125 011646 162737 000001 001124 SUB #1,\$GDDAT ;IF YES - DECREMENT EXPECTED AND RELOAD.
2126 011654 000715 BR 1\$;GOTO RELOAD POINT.
2127
2128 011656 5\$: ;END SUBTEST
2129
2130 .SBTTL *
2131 .SBTTL * PHASE 3 CLOCK A COUNT FUNCTION TESTS
2132 .SBTTL *
2133
2143
2144 ;*****
(3) *TEST 76 *TEST THAT CLOCK A OVERFLOW WILL OCCUR
(4)
(4) ;*NOW WE'LL TRY AND GENERATE "A OVERFLOW L"
(4) ;*WHICH SETS BD05. WE'LL DO IT BY PRESETTING THE BUFFER
(4) ;*AT 177777 AND GENERATE A MAINTENANCE STP1. WE ALREADY
(4) ;*KNOW MAINTENANCE STP1'S WILL ADVANCE THE COUNTER.

(4)
(5)
(5)
(5)
(3)
(2) 011656 000004 TST76: SCOPE
2145
2146 ;*ALSO SEE IF "MODE" FLG GETS SET.
2147 ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
2148 ;*
2149 ;*****
2150 (2) 011660 005037 001124 CLR SGDDAT ;MAKE SURE CLOCK A CLEAR.
2151 (1) 011674 012737 177777 001124 ;* MOV SGDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
2152 ;* MOV #177777,SGDDAT ;PRESET BUFFER TO ALL ONES.
2153 (1) 011712 012737 000015 001124 ;* MOV SGDDAT,@ABR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
2154 ;* SELECT MODE 0; RATE STP4; GO.
2155 ;* GENERATE A MAINTENANCE STP1.
2156 (1) 011740 052737 010000 001124 ;* MOV #15,SGDDAT ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
2157 ;* MOV SGDDAT,@ASR ;/READ DEVICE REG ASR,PUT DATA IN SGDDAT.
2158 (1) 011756 1\$: ;* MOV @ASR,\$BDDAT ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
2159 ;* DID OVERFLOW BIT SET?
2160 (1) 011766 032737 000040 001126 ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
2161 ;* BIT #BIT05,\$BDDAT ;BR IF YES TO '2\$'.
2162 011774 001002 BNE 2\$
2163 ;;;\$>> ERROR <<\$
2164 011776 104012 ERROR 12 ;ERROR BIT05 OF CSR CLOCK A FAILED
2165 ;TO SET ON OVERFLOW.
2166 ;;;\$>> ERROR <<\$
2167 012000 000411 BR 3\$
2168 012002 2\$: ;DID BIT07 - "MODE" FLG SET?
2169 ;*
2170 (1) 012012 032737 000200 001126 ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
2171 ;* BIT #BIT07,\$BDDAT ;IT SHOULD SET WHEN BIT05 SETS.
2172 ;* BNE 3\$;BR IF YES TO 3\$.
2173 ;;;\$>> ERROR <<\$
2174 012022 104012 ERROR 12 ;OVERFLOW FAILED TO SET CLOCK A'S
2175 ;CSR BIT07 "MODE" FLG. IT
2176 ;HAD; HOWEVER SET BIT05 "OVERFLOW"
2177 ;FLAG.
2178 ;;;\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$>> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$

```

2180 012024
2190      3$:
2191      :***** TEST 77 *TEST IN CLOCK A THAT OVERFLOW IN MODE 0 CAUSE CLEARING OF 'ENB CNTR' F/
2192      (*
2193      (*WE'RE GOING TO SEE IF "A RELOAD" H AND "MODE 0" H CLEAR
2194      (*'ENB CNTR A' F/F. "A RELOAD" GENERATED ON OVERFLOW AND
2195      (*"MODE 0" GENERATED BY "MODE AO (0)" AND "MODE AO (1)"
2196      (*ALSO SEE IF COUNTER REGISTER GETS RELOADED
2197      (*
2198      (* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
2199      (*
2200      (*
2201      (*
2202      (*
2203      (*
2204      (*
2205      (*
2206      (*
2207      (*
2208      (*
2209      (*
2210      (*
2211      (*
2212      (*
2213      ;:;$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$
2214      012144 104012          ERROR 12          ;'ENB CNTR A' F/F NOT CLEARED
2215      ;ON OVERFLOW.
2216      ;:;$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$
2217      012146 000411          BR   2$:
2218      (*
2219      012150          1$:
2220      (*
2221      (*
2222      012160 022737 177777 001126  ;*: MOV @ACR,$BDDAT ;READ DEVICE REG ACR,PUT DATA IN $BDDAT.
2223      (*      CMP    #177777,$BDDAT ;DID COUNTER GET RELOADED AFTER

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T77 *TEST IN CLOCK A THAT OVERFLOW IN MODE 0 CAUSE CLEARING OF "ENB CNTR" F/F SEQ 0097

2221 012166 001401 BEQ 2\$;THE OVERFLOW OCCURRED?
2222 ;BR IF YES - NEXT TEST.
2223 :;;\$> ERROR <<\$
2224 012170 104012 ERROR 12 ;ERROR CLOCK A - COUNTER DID NOT GET RELOAD FROM
2225 ;BUFFER AFTER OVERFLOW. "A RELOAD" H
2226 ;DID GET GENERATED ON WE WOULD
2227 ;HAVE GOT PREVIOUS ERROR; THEREFORE PROBLEM
2228 ;MUST EXIST WITH COMBINING "A RELOAD" H
2229 ;WITH "MODE A1 (0)" H TO GENERATE A
2230 ;COUNTER LOAD.
2231 :;;\$> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
2232 012172 2\$:
2280

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T77 *TEST IN CLOCK A THAT OVERFLOW IN MODE 0 CAUSE CLEARING OF "ENB CNTR" F/F SEQ 0098

2281 ://
(1)
(5)
(4) :***** *TEST 100 *TEST THE ABILITY OF CLOCK A TO COUNT AT 1MHZ RATE PART 1
(5)
(5) :* THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT
(5) :* IN RATE: 1MHZ PART 1
(6)
(6) :* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(6)
(5)
(4)
(3) 012172 000004 :*****
(1)
(1) TST100: SCOPE
(1)
(1) :/MAKE SURE CLOCK IS CLEAR.
(1) :/CLEAR THE BUFFER.
(1) :/SELECT: MODE 0, RATE 1MHZ ; GO.
(1) 012174 005037 001124 CLR \$GDDAT
(2) :* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(2) :* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(1) 012220 012737 000003 001124 :* MOV #1!2,\$GDDAT
(2) :* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(1) 012236 005000 CLR RO ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY
(1) 012240 005200 INC RO ;/WILL AMOUNT TO 369MS ON A PDP-11/20
(1) 012242 001376 BNE 1\$;/DID COUNTER INCREMENT AT ALL?
(2)
(2) :* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN SBDDAT.
(1) 012254 005737 001126 TST \$BDDAT
(1) 012260 001011 BNE 2\$;/IF YES - BR NEXT TEST.
(1)
(1) ;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.
(2)
(2) :* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
(1) 012272 032737 000040 001126 BIT #BIT05,\$BDDAT ;/AT HIGH RATE - SO WE'LL SEE IF "OVERFLOW"
(1)
(1) 012300 001001 BNE 2\$;/F/F HAD SET.
(2) ;:SSSSSSSSSSSSSSSSSSSSSSSSSS> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
(1) 012302 104012 ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO
(1) ;/COUNT RATE: 1MHZ.
(2) ;:SSSSSSSSSSSSSSSSSSSSSSSS> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSS
(1) 012304 2\$:

2282

;#

(1)
(5) :*****
(4) ;*TEST 101 *TEST THE ABILITY OF CLOCK A TO COUNT AT 100KHZ RATE PART 1
(5) ;*
(5) ;*THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT
(5) ;*IN RATE: 100KHZ PART 1
(6) ;*
(6) ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(6) ;*
(5) :*****
(4) :*****
(3) 012304 000004 TST101: SCOPE
(1)
(1) ;/MAKE SURE CLOCK IS CLEAR.
(1) ;/CLEAR THE BUFFER.
(1) ;/SELECT: MODE 0, RATE 100KHZ ; GO.
(1) 012306 005037 001124 CLR SGDDAT
(2) ;* MOV SGDDAT, @ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(2) ;* MOV SGDDAT, @ABR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
(1) 012332 012737 000005 001124 ;* MOV #1!4, SGDDAT
(2) ;* MOV SGDDAT, @ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(1) 012350 005000 CLR R0 ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY
(1) 012352 005200 INC R0 ;/WILL AMOUNT TO 369MS ON A PDP-11/20
(1) 012354 001376 BNE 1\$;/DID COUNTER INCREMENT AT ALL?
(2) ;* MOV @ACR, \$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN SBDDAT.
(1) 012366 005737 001126 TST \$BDDAT
(1) 012372 001011 BNE 2\$;/IF YES - BR NEXT TEST.
(1) ;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.
(2) ;* MOV @ASR, \$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
(1) 012404 032737 000040 001126 BIT #BIT05, \$BDDAT ;/AT HIGH RATE - SO WE'LL SEE IF "OVERFLOW"
(1) ;/F/F HAD SET.
(1) 012412 001001 BNE 2\$;/BR IF YES NEXT TEST.
(2) ;:\$>> ERROR <<\$
(1) 012414 104012 ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO
(1) ;/COUNT RATE: 100KHZ.
(2) ;:\$>> ERROR <<\$
(1) 012416 2\$:

2283

:/#

```
*****  
*: TEST 102      *TEST THE ABILITY OF CLOCK A TO COUNT AT 10KHZ RATE PART 1  
*: THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT  
*: IN RATE: 10KHZ          PART 1  
*: PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"  
*:*****
```

(3) 012416 000004

TST102: SCOPE

;/MAKE SURE CLOCK IS CLEAR.
;/CLEAR THE BUFFER.
;/SELECT: MODE 0, RATE 10KHZ ; GO.

(1) 012420 005037 001124	CLR	\$GDDAT	
(2)	;	MOV	\$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(2)	;	MOV	\$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(1) 012444 012737 000007 001124	;	MOV	#1:6,\$GDDAT
(2)	;	MOV	\$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(1) 012462 005000	CLR	R0	;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY
(1) 012464 005200	INC	R0	;/WILL AMOUNT TO 369MS ON A PDP-11/20
(1) 012466 001376	BNE	1\$;/DID COUNTER INCREMENT AT ALL?
(2)	;	MOV	@ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
(1) 012500 005737 001126	TST	\$BDDAT	
(1) 012504 001011	BNE	2\$;/IF YES - BR NEXT TEST.
(1)			;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.
(2)	;	MOV	@ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(1) 012516 032737 000040 001126	BIT	#BIT05,\$BDDAT	;/AT HIGH RATE - SO WE'LL SEE IF "OVERFLOW" ;/F/F HAD SET.
(1) 012524 001001	BNE	2\$;/BR IF YES NEXT TEST.
(2)	;	;	; ;:\$>> ERROR <<\$
(1) 012526 104012	ERROR	12	;/ERROR CLOCK A COUNTER FAILED TO ;/COUNT RATE: 10KHZ.
(2)	;	;	; ;:\$>> ERROR <<\$
(1) 012530		2\$:	

2284 :/#
(1)
(5)
(4) :***** *TEST 103 *TEST THE ABILITY OF CLOCK A TO COUNT AT 1KHZ RATE PART 1
(5)*
(5) *THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT
(5) IN RATE: 1KHZ PART 1
(6)*
(6) * PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(6)*
(5)*
(4)*
(3) 012530 000004 TST103: SCOPE
(1)
(1) :/MAKE SURE CLOCK IS CLEAR.
(1) :/CLEAR THE BUFFER.
(1) :/SELECT: MODE 0, RATE 1KHZ ; GO.
(1) 012532 005037 001124 CLR \$GDDAT
(2) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(2) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(1) 012556 012737 000011 001124 ;* MOV #1!10,\$GDDAT
(2) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(1) 012574 005000 CLR R0 ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY
(1) 012576 005200 INC R0 ;/WILL AMOUNT TO 369MS ON A PDP-11/20
(1) 012600 001376 BNE 1\$;/DID COUNTER INCREMENT AT ALL?
(2)
(2) ;* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
(1) 012612 005737 001126 TST \$BDDAT
(1) 012616 001011 BNE 2\$;/IF YES - BR NEXT TEST.
(1) ;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.
(2)
(2) ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(1) 012630 032737 000040 001126 BIT #BIT05,\$BDDAT ;/AT HIGH RATE - SO WE'LL SEE IF "OVERFLOW"
(1) ;/F/F HAD SET.
(1) 012636 001001 BNE 2\$;/BR IF YES NEXT TEST.
(2) ;:\$> ERROR <<\$
(1) 012640 104012 ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO
(1) ;/COUNT RATE: 1KHZ.
(2) ;:\$> ERROR <<\$
(1) 012642 2\$:

2285 ://
(1)
(5)
(4) :*TEST 104 *TEST THE ABILITY OF CLOCK A TO COUNT AT 100HZ RATE PART 1
(5)*
(5) *THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT
(5) IN RATE: 100HZ PART 1
(6)*
(6) * PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(5)*
(4)*
(3) 012642 000004 TST104: SCOPE
(1)
(1) :/MAKE SURE CLOCK IS CLEAR.
(1) :/CLEAR THE BUFFER.
(1) :/SELECT: MODE 0, RATE 100HZ ; GO.
(1) 012644 005037 001124 CLR SGDDAT
(2) :* MOV SGDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(2) :* MOV SGDDAT,@ABR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
(1) 012670 012737 000013 001124 :* MOV #1!12,\$GDDAT
(2) :* MOV SGDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(1) 012706 005000 CLR RO ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY
(1) 012710 005200 INC RO ;/WILL AMOUNT TO 369MS ON A PDP-11/20
(1) 012712 001376 BNE 1\$;/DID COUNTER INCREMENT AT ALL?
(2)
(2) :* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN SBDDAT.
(1) 012724 005737 001126 TST \$BDDAT
(1) 012730 001011 BNE 2\$;/IF YES - BR NEXT TEST.
(1)
(1) ;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.
(2)
(2) :* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN SBDDAT.
(1) 012742 032737 000040 001126 BIT #BIT05,\$BDDAT ;/AT HIGH RATE - SO WE'LL SEE IF "OVERFLOW"
(1)
(1) 012750 001001 BNE 2\$;/F/F HAD SET.
(2) ;/BR IF YES NEXT TEST.
:::\$> ERROR <<\$
(1) 012752 104012 ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO
(1) ;/COUNT RATE: 100HZ.
(2) ;:\$> ERROR <<\$
(1) 012754 2\$:


```

(4)          :*ITS RATES, SO LETS BE SURE IT DOESNT
(4)          :COUNT WHEN NO RATE IS SELECTED. ON
(4)          :ERROR SUSPECT DUAL RATE SELECTION.
(5)
(5)          :* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(5)
(3)
(2) 013066 000004          *****

2298          TST106: SCOPE

2299          :CLEAR CLOCK A.
2300          :ZERO ITS BUFFER.
2301          :TELL THE CLOCK TO GO!
2302 013070 005037 001124      CLR    SGDDAT
2303          ;*      MOV    SGDDAT,@ASR   ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
2304          ;*      MOV    SGDDAT,@ABR   ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
2305 013114 005237 001124      INC    SGDDAT
2306          ;*      MOV    SGDDAT,@ASR   ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
2307          ;*      CLR    RO
2308 013130 005000          INC    RO
2309 013132 005200          BNE    1$           ;ANY COUNT OCCUR?
2310 013134 001376          1$:   INC    RO
2311          ;*      MOV    @ACR,$BDDAT  ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
2312          ;*      TST    $BDDAT
2313 013146 005737 001126      BNE    2$           ;IF COUNTER HAS SOMETHING IN IT REPORT ERROR
2314 013152 001010          ;*      MOV    @ASR,$BDDAI  ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
2315          ;*      BIT    #BIT05,$BDDAT ;IF THE OVERFLOW BIT SET THEN IT MUST
2316          ;*      BEQ    3$           ;HAVE COUNTED.
2317 013164 032737 000040 001126 ;*
2318          ;*      MOV    BIT
2319 013172 001401          BEQ    3$           ;;
2320          ;;
2321          ;:;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
2322 013174 104012          2$:   ERROR  12          ;AH HA! ERROR CLOCK A COUNTED WHEN
2323          ;ENABLED-BUT-NO-RATE SELECTED
2324          ;BETTER FIND OUT HOW CAUSED SIGNAL:
2325          ;;"CLOCK A" L.
2326          ;:;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
2327 013176          3$:
2328          ;;
2329          ;;
2330          ;;
2331          ;;
2332          ;;
2333          ;;
2334          ;;
2335          ;;
2336          ;;
2337          ;;
2338          ;;
2339          ;;
(3)          ;*TEST 107      *TEST THAT CLOCK A'S COUNT REG ISN'T LOADED WHEN CLOCK A IS ENABLED
(4)
(4)          ;*IN THIS TEST WE'LL FIND OUT IF F/F "ENB CNTR A" WHEN SET,
(4)          ;*INHIBITS LOADING OF CLOCK A'S COUNT REGISTER
(4)          ;*THE LOADING OF THE COUNT REGISTER IS A FUNCTION OF:
(4)          ;*'"ENB CNTR (0)" H + "BUFFER LOAD" H

```

```

(4)
(5)
(5)      ;*
(5)      ;* PROBABLE SYNC POINT FOR THIS TEST:: "RD STAT B"
(5)
(3)      ;***** ****
(2) 013176 000004      TST107: SCOPE

2340
2341      ;GENERATE A SYNC PULSE
2342      ;CLEAR CLOCK A'S STATUS REG.
2343      ;CLEAR CLOCK A'S BUFFER REG. NOTE
2344      ;THIS WILL ALSO CAUSE ZEROS TO BE
2345      ;LOADED INTO THE COUNT REG.
2346
2347 (1) 013210 005737 001126      ;*    MOV    @BSR,$BDDAT    ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
2348 013214 005037 001124      TST    $BDDAT
2349      CLR    $GDDAT
2350
2351 (1) 013240 005237 001124      ;*    MOV    $GDDAT,@ASR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2352      ;*    INC    $GDDAT    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
2353      ;SET THE ENABLE F/F. THIS
2354      ;*    MOV    $GDDAT,@ASR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2355 013254 012737 177777 001124      MOV    #177777,$GDDAT    ;FROM BEING LOADED WHEN THE
2356      ;BUFFER IS LOADED.
2357      ;NOW LOAD THE BUFFER REG.
2358
2359 (1)      ;*    MOV    $GDDAT,@ABR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
2360      ;TO THE COUNT REGISTER.
2361 013302 005737 001126      ;DID ANY BITS GET TRANSFERRED TO
2362 013306 001401      TST    $BDDAT    ;THE COUNT REGISTER?
2363      BEQ    1$      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
2364      ;BR IF NO - NEXT TEST.

2363      ;;;$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$

2364 013310 104012      ERROR 12      ;ERROR CLOCK A BUFFER TO COUNT REG TRANSFER
2365      ;OCCURRED EVEN THOUGH THE 'ENB CNTR A' F/F
2366      ;WAS SET.
2367
2368      ;;;$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$

2368 013312      1$:

2369
2370
2371
2372
2373
2374
2375
2376
2377
2378
2379      ;***** ****
(3)      ;*TEST 110      *TEST THAT CLOCK A IN MODE 1 DOES NOT CLEAR ENABLE ON OVERFLOW
(4)
(4)      ;*NOW WE'RE GOING TO SEE IF "A OVERFLOW" H WHEN GENERATED
(4)      ;*BY CAUSING AN OVERFLOW DOESN'T CLEAR THE "ENB CNTR A" F/F
(4)      ;*WHEN IN MODE 1. IF F/F GETS CLEARED SUSPECT SIGNAL "MODE 0" H.
(4)
(5)
(5)      ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"

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T110 *TEST THAT CLOCK A IN MODE 1 DOES NOT CLEAR ENABLE ON OVERFLOW

SEQ 0106

(5)
(3)
(2) 013312 000004 :*
2380 :*****
2381 :ST110: SCOPE
2382 :MAKE SURE CLOCK A IS CLEAR.
2383 :SET BUFFER + COUNT REG. TO -1 FROM OVERFLOW
2384 :SET: MODE 1; RATE STP1; GO.
2385 :CAUSE A MAINTENANCE STP4. CLOCK 1
2386 :SHOULD OVERFLOW - BUT THIS OVERFLOW SHOULD
2387 :NOT CLEAR 'ENB CNTR A' F/F.
2388 :DID BIT00, 'ENB CNTR A' F/F GET CLEARED?
2389 013314 005037 001124 CLR \$GDDAT
2390 013330 012737 177777 001124 :* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
2391 (1) 013346 012737 000415 001124 :* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
2392 (1) 013374 052737 010000 001354 :* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
2393 (1) 013422 032737 000001 001126 :* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
2394 013430 001001 BIS #BIT12,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
2395 (1) 013432 104012 ERROR 12 :/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
2396 (1) 013434 000004 :* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
2397 (1) 013430 BNE #BIT00,\$BDDAT 1\$;BR IF NO TO NEXT TEST.
2398 2400 :;;:\$>> ERROR <<\$
2401 013432 104012 ERROR 12 :ERROR MODE 1 OPERATION 'ENB CNTR A' F/F
2402 :WAS CLEARED ON OVERFLOW.
2403 :;;:\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$>> ERROR <<\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$
2404 013434 1\$:
2405 :*****
2417 :*TEST 111 *TEST THAT A CLOCK A 'BUFFER TO COUNT REG' DOESN'T TAKE PLACE ON A MODE
2418 (3) :*THIS WILL BE THE FIRST TIME WE'VE DONE A MODE 2 OPERATION
2419 (4) :*ON CLOCK A. THE FUNCTION OF THIS TEST WILL BE TO MAKE
(4) :*SURE A BUFFER TO COUNT REGISTER DOESN'T TAKE PLACE ON OVERFLOW
(4) :*THE COMBO THAT GAVE US BUFFER TO COUNT REG ON OVERFLOW BEFORE
(4) :*IS ['MODE A1 (0)' H + "A RELOAD" H]. WE'LL STILL BE GENERATING
(5) :* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(5) :*
(4) :* "A RELOAD" H BUT SHOULD NOT GET."MODE A1 (0)" H AS THIS IS MODE 2.
(4) :*
(3) :*****
(2) 013434 000004 :ST111: SCOPE
2419

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T111 *TEST THAT A CLOCK A "BUFFER TO COUNT REG" DOESN'T TAKE PLACE ON A MODE 2 SEQ 0107

;MAKE SURE CLOCK A IS CLEAR.
;SET BUFFER + COUNT REG TO -1 FROM OVERFLOW.
;SET: MODE 2; RATE STP1; GO.
;CAUSE A MAINTENANCE STP1 - CLOCK ONCE.
;THIS SHOULD CAUSE AN OVERFLOW AND LEAVE
;THE COUNT REGISTER CLEAR AS A
;BUFFER TO COUNT REG. SHOULDN'T OCCUR.
;IS THE COUNT REG. CLEAR?

```

2427      ;15 THE COUNT REG. CLEAR.
2428 013436 005037 001124           CLR    $GDDAT
2429
2429 (1)          ;*
2430 013452 012737 177777 001124   MOV    $GDDAT,@ASR
2431                                         MOV    #177777,$GDDAT  ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2431 (1)
2432 013470 012737 001015 001124   MOV    $GDDAT,@ABR
2433                                         MOV    #1015,$GDDAT  ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
2433 (1)
2434 (1)          ;*
2435 013516 052737 010000 001124   MOV    $GDDAT,@ASR
2436                                         BIS    @ASR,$GDDAT  ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
2436 (1)
2437 (1)          ;*
2438 013544 005737 001126           MOV    $GDDAT,@ASR
2439 013550 001401                 TST    @ACR,$BDDAT  ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
2440                                         BEQ    $BDDAT
2440                                         1$               ;BR IF YES TO NEXT TEST.

```

2441 013552 104012 ERROR 12 ;ERROR THE CONTENTS OF THE BUFFER REG.
2442 ;GOT TRANSFERRED TO THE COUNT REG.
2443 ;(CLOCK A) ON OVERFLOW DOING A
2444 ;MODE 2 OPERATION.

THERE'S AN OUTSIDE CHANCE THAT THE COUNT REG. NEVER GOES TO ZERO ON AN OVERFLOW - THIS IS THE FIRST TIME THAT WE WERE ABLE TO LOOK AT IT ON OVERFLOW BECAUSE MODES 0 + 1 CAUSED THAT AUTOMATIC BUFFER TO COUNT REG.

:::SSSSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSSSS

2453 013554

```
;*****  
;*TEST 112      *TEST THAT CLOCK A MODE 2 + MAINTENANCE ST2 SET MODE FLG  
;  
;*NOW WE'LL SEE IF CAN GENERATE A "CNTR TO BUFF" H SIGNAL.  
;*TO DETECT IT, WE'RE GOING TO DEPEND ON IT SETTING THE MODE FLAG,  
;*CLOCK A CSR BIT07. [ "MODE A1 (0)" H + "ST2 (1)" H ] + "TPO" L = "CNTR TO BUFF" H.  
;*BEING IN MODE 2, SHOULD GIVE US "MODE A1 (1)" H. WELL GET ST2 (1) H  
;*BY GENERATING A MAINTENANCE "ST2". TPO COMES FROM THE INTERNAL  
;*CLOCK PAGE.  
;
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T112 *TEST THAT CLOCK A MODE 2 + MAINTENANCE ST2 SET MODE FLG

SEQ 0108

```

(5)          ;* PROBABLE SYNC POINT FOR THIS TEST:: 'RD STAT B'
(5)
(4)
(3)
(2)        013554 000004
2468        TST112: SCOPE
2469
2470
2471        013566 005737 001126      ;*    MOV    @BSR,$BDDAT    ;GENERATE A SYNC PULSE
2472          TST    $BDDAT
2473        013572 005037 001124      CLR    $GDDAT    ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
2474          ;*    MOV    $GDDAT,@ASR    ;MAKE SURE CLOCK A'S STAT REG IS CLEAR.
2475
2476
2477
2478
2479        013606 012737 001000 001124      MOV    #1000,$GDDAT    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2480          ;*    MOV    $GDDAT,@ASR    ;SET MODE 2.
2481          ;*    MOV    @ASR,$GDDAT    ;GENERATE MAINTENANCE ST2.
2482          ;*    BIS    #BIT10,$GDDAT    ;THE COMBO OF MODE 2 + ST2 SHOULD
2483        013634 052737 002000 001124      ;*    MOV    $GDDAT,@ASR    ;GET "CNTR TO BUFF" H WHICH SHOULD
2484          ;*    BIS    #BIT10,$GDDAT    ;SET 'MODE FLG' F/F.
2485          ;*    MOV    $GDDAT,@ASR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2486          ;*    BIS    #BIT10,$GDDAT    ;DID IT SET?
2487        013662 032737 000200 001126      ;*    MOV    @ASR,$BDDAT    ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
2488          ;*    BIT    #BIT07,$BDDAT    ;IF YES-BR TO NEXT TEST.
2489          ;*    BNE    1$                  ;IF YES-BR TO NEXT TEST.
2490        013672 104012          ERROR 12      ;ERROR - MODE 2 + ST2 DID NOT SET MODE FL.
2491          ;:;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
2492        013674          1$:                  ;:;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
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2548        ;:;*****TEST 113      *TEST THAT PATTERN 052525 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
2549          ;*
2550          ;*NOW WE'LL SHOT THE WORKS - WE KNOW FROM THE PREVIOUS TEST WE
2551          ;*CAN GENERATE "CNTR TO BUFF" H FROM MODE 2 + MAINTENANCE ST2, NOW
2552          ;*WE WELL TRY AND GENERATE A TRANSFER BETWEEN THE COUNTER AND BUFFER
2553          ;*USING A CB PAT PATTERN.
2554          ;*IF NO DATA PATTERN GETS TRANSFERRED, SUSPECT SIG 'LD BUFFER'
2555          ;*TO BE STUCK LOW AT THE MUX INPUT FOR THE BUFFER OR
2556          ;*"CNTR TO BUFF" H NOT GETTING THROUGH TO THE LOAD INPUTS OF THE
2557          ;*BUFFER REGISTER.
2558          ;*IF JUST ONE OR A FEW BITS GETS MESSED UP ON THE XFERR-
2559          ;*SUSPECT THE RESPECTIVE MUX OR ETCH BETWEEN THE COUNT REG
2560          ;*AND MUX. GOOD LUCK.

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T113 *TEST THAT PATTERN 052525 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS

SEQ 0109

(6) :*
(6) ** PROBABLE SYNC POINT FOR THIS TEST:: 'RD STAT B'
(6)
(5)
(4)
(3) 013674 000004 TST113: SCOPE
(1)
(1) :*****
(2)
(2) 013706 005737 001126 :* MOV ABSR,\$BDDAT ;READ DEVICE REG BSR,PUT DATA IN SBDDAT.
(1)
(1) :* TST \$BDDAT ;MAKE SURE CLOCK A IS CLEAR.
(1)
(1) :* #052525 INTO BUFFER REG.
(1)
(1) :* IT SHOULD GET XFERRED TO COUNT REG.
(1)
(1) :* SELECT: MODE 2, ENABLE.
(1)
(1) :* NOW GENERATE A MAINTENANCE ST2.
(1) 013712 005037 001124 CLR SGDDAT
(2)
(2) 013726 012737 052525 001124 :* MOV \$GDDAT,ABSAR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(1) :* MOV #052525,\$GDDAT
(2)
(2) 013744 012737 001001 001124 :* MOV \$GDDAT,AABR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
(1) :* MOV #1001,\$GDDAT
(2)
(2) 013762 005037 001124 :* MOV \$GDDAT,ABSAR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(1) :* CLR SGDDAT
(2)
(2) :* MOV \$GDDAT,AABR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
(2)
(2) 014006 052737 002000 001124 :* MOV @ASR,\$GDDAT ;READ DEVICE REG ASR,PUT DATA IN SGDDAT.
(1) :* BIS #BIT10,\$GDDAT
(2)
(2) 014024 012737 052525 001124 :* MOV \$GDDAT,ABSAR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(1) :* MOV #052525,\$GDDAT ;RECORD SGDDAT (PATTERN) IN CASE WE
(1) :* NEED TO TYPE OUT AN ERROR.
(1) :* NOW READ BACK THE BUFFER REG.
(2)
(2) 014042 023737 001126 001124 :* MOV AABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN SBDDAT.
(1) :* CMP \$BDDAT,\$GDDAT ;WAS THE TRANSFER SUCCESSFUL?
(1) :* BEQ 1\$;IF YES THEN BR TO NEXT TEST.
(2)
;:;SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
(1) 014052 104012 ERROR 12 ;ERROR FAILED TO XFERR 052525 PATTERN
(1) ;CORRECTLY FROM COUNT TO BUFFER REG.
(1) ;SEE INIT. COMMENT AS TO WHY
(1) ;IT MIGHT HAVE GONE SOUR.
(2)
;:;SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
(1) 014054 000011 1\$: P=P+1
(1)
2549
(5)
(4)
(5) :*****
;*TEST 114 *TEST THAT PATTERN 125252 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
;*

```
(5)      ;*NOW WE'LL SHOT THE WORKS - WE KNOW FROM THE PREVIOUS TEST WE
(5)      ;*CAN GENERATE "CNTR TO BUFF" H FROM MODE 2 + MAINTENANCE ST2, NOW
(5)      ;*WE WELL TRY AND GENERATE A TRANSFER BETWEEN THE COUNTER AND BUFFER
(5)      ;*USING A CB PAT PATTERN.
(5)      ;*IF NO DATA PATTERN GETS TRANSFERRED, SUSPECT SIG "LD BUFFER"
(5)      ;*TO BE STUCK LOW AT THE MUX INPUT FOR THE BUFFER OR
(5)      ;*'"CNTR TO BUFF" H NOT GETTING THROUGH TO THE LOAD INPUTS OF THE
(5)      ;*BUFFER REGISTER.
(5)      ;*IF JUST ONE OR A FEW BITS GETS MESSED UP ON THE XFERR-
(5)      ;*SUSPECT THE RESPECTIVE MUX OR ETCH BETWEEN THE COUNT REG
(5)      ;*AND MUX. GOOD LUCK.
```

```
(6)      ;* PROBABLE SYNC POINT FOR THIS TEST:: "RD STAT B"
```

```
(6)
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```
(5)
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```
(4)      ;*****
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014054 000004

TST114: SCOPE

;GENERATE A SYNC PULSE

014066 005737 001126	;	MOV TST	@BSR,\$BDDAT \$BDDAT	;READ DEVICE REG BSR,PUT DATA IN \$BDDAT. ;MAKE SURE CLOCK A IS CLEAR. ;PUT PATTERN 125252 INTO BUFFER REG. ;IT SHOULD GET XFERRRED TO COUNT REG. ;SELECT: MODE 2, ENABLE. ;NOW GENERATE A MAINTENANCE ST2.
----------------------	---	---------	----------------------	--

014072 005037 001124

	;	CLR	\$GDDAT	;PUT DATA FROM \$GDDAT TO DEVICE REG ASR
--	---	-----	---------	--

014106 012737 125252 001124

	;	MOV	\$GDDAT,@ASR #125252,\$GDDAT	;PUT DATA FROM \$GDDAT TO DEVICE REG ABR
--	---	-----	------------------------------	--

014124 012737 001001 001124

	;	MOV	\$GDDAT,@ABR #1001,\$GDDAT	;PUT DATA FROM \$GDDAT TO DEVICE REG ASR
--	---	-----	----------------------------	--

014142 005037 001124

	;	CLR	\$GDDAT	;PUT DATA FROM \$GDDAT TO DEVICE REG ABR
--	---	-----	---------	--

014166 052737 002000 001124

	;	MOV	@ASR,\$GDDAT #BIT10,\$GDDAT	;READ DEVICE REG ASR,PUT DATA IN \$GDDAT.
--	---	-----	-----------------------------	---

014204 012737 125252 001124

	;	MOV	\$GDDAT,@ASR #125252,\$GDDAT	;PUT DATA FROM \$GDDAT TO DEVICE REG ASR ;RECORD \$GDDAT (PATTERN) IN CASE WE ;NEED TO TYPE OUT AN ERROR. ;NOW READ BACK THE BUFFER REG.
--	---	-----	------------------------------	---

014222 023737 001126 001124

	;	MOV CMP BEQ	@ABR,\$BDDAT \$BDDAT,\$GDDAT 1\$;READ DEVICE REG ABR,PUT DATA IN \$BDDAT. ;WAS THE TRANSFER SUCCESSFUL? ;IF YES THEN BR TO NEXT TEST.
--	---	-------------	----------------------------------	---

;;;;SSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS

014232 104012

ERROR 12	;	ERROR FAILED TO XFERR 125252 PATTERN ;CORRECTLY FROM COUNT TO BUFFER REG.
----------	---	--

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T114 *TEST THAT PATTERN 125252 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS SEQ 0111

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T116 *TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 2 WHEN STP2 IS GENERA SEQ 0112

(5) :*****
(4) :*TEST 116 *TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 2 WHEN STP2 IS GENER
(5) :*
(5) :*THIS TEST IS DESIGNED TO MAKE SURE THAT WE DON'T CLEAR THE COUNT
(5) :*REGISTER IN MODE 2 WHEN AN STP2 IS GENERATED.
(6) :*
(6) :* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(6) :*
(5) :*
(4) :*****
(3) 014354 000004 TST116: SCOPE
(1)
(1) :MAKE SURE CLOCK A IS CLEAR.
(1) :LOAD ALL ONES INTO BUFFER COUNT REGS.
(1) :SET MODE 2.
(1) :GENERATE A MAINTENANCE STP2.
(1) :SEE IF IT CLEARED COUNT REG.
(1) 014356 005037 001124 CLR \$GDDAT
(2)
(2) 014372 012737 177777 001124 ;* MOV \$GDDAT,@ASR / PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(1) #177777,\$GDDAT
(2)
(2) 014410 012737 001000 001124 ;* MOV \$GDDAT,@ABR / PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(1) #1000,\$GDDAT
(2)
(2) ;* MOV \$GDDAT,@ASR / PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(2) #ASR,\$GDDAT
(2) ;* BIS #BIT10,\$GDDAT /READ DEVICE REG ASR,PUT DATA IN \$GDDAT.
(1) 014436 052737 002000 001124
(2)
(2) ;* MOV \$GDDAT,@ASR / PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(2) #ACR,\$BDDAT /READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
(1) 014464 005737 001126
(1) 014470 001001 TST SBDDAT
(2) BNE 1\$;BR IF NO - NEXT TEST.

;:\$>> ERROR <<\$
(1) 014472 104012 ERROR 12 :ERROR CLOCK A MODE 2 + STP2 CLEARED COUNT REG.
(1) :TO SCOPE FIND OUT WHAT IS GENERATING
(1) :SIGNAL ON CLR INPUT OF COUNT REG.
(2)

;:\$>> ERROR <<\$
(1) 014474 1\$:

2595
2606
2607 :*****
(3) :*TEST 117 *TEST THAT MODE 3 + "STP2" CLEARS A'S COUNT REGISTER.
(4) :*
(4) :*IN THIS TEST WE'LL DO A MODE 3 FOR THE FIRST TIME.
(4) :*MODE 3 + "STP2" SHOULD CLEAR THE COUNT REGISTER.
(4) :*WE KNOW FROM A PREVIOUS TEST THAT "INIT" L WAS ABLE TO
(4) :*CLEAR THE REG. AND ALSO THAT WE CAN GENERATE AN "STP2" H.
(4) :*'MODE A0 (1)" H + 'MODE A1 (1)" H + "STP2" H = CLEARING SIGNAL.
(5) :*

```

(5)          :* PROBABLE SYNC POINT FOR THIS TEST::: "LD BUFF A"
(5)
(4)
(3)
(2) 014474 000004          TST117: SCOPE
2608
2609
2610
2611
2612
2613
2614          ;CLEAR CLOCK A + SELECT MODE 3.
2615 014476 012737 001400 001124      MOV    #1400,$GDDAT   ;LOAD ALL ONE'S TO BUFFER + COUNTER REGS.
2616          ;GENERATE A MAINTENANCE "STP2".
2617 014514 012737 177777 001124      ;*    MOV    $GDDAT,@ASR    ;THIS SHOULD CLEAR THE COUNT REG.
2618          ;*    MOV    #177777,$GDDAT
2619          ;*    MOV    $GDDAT,@ABR
2620 014542 052737 002000 001124      ;*    MOV    @ASR,$GDDAT  ;/READ DEVICE REG ASR,PUT DATA IN SGDDAT.
2621          ;*    BIS    #BIT10,$GDDAT
2622          ;*    MOV    $GDDAT,@ASR  ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
2623 014570 005737 001126          ;*    MOV    @ACR,$BDDAT  ;/READ DEVICE REG ACR,PUT DATA IN SBDDAT.
2624 014574 001401          TST    $BDDAT
2625          BEQ    1$          ;BR IF YES - NEXT TEST.

          ;;;$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$
2626 014576 104012          ERROR 12          ;ERROR-CLOCK A-COUNT REGISTER FAILED TO
2627          ;CLEAR IN MODE 3 ON 'STP2' PULSE.
2628          ;;;$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$

2629 014600          1$:
2630
2650
2651          ;*TEST 120 *TEST THE AUTODECREMENT FEATURE OF CLOCK A'S BUFFER
(3)
(4)
(4)          ;*THIS IS GOING TO BE A BIGGIE-WITH TWO PARTS.
(4)          ;*PART1: WE'RE LOADING THE BUFFER WITH ALL ONES; MODE 0; RATE STP1,
(4)          ;*           WITH "AUTO INC (1)" SET (FOR FIRST TIME!). NOW WE'LL GENERATE
(4)          ;*           THE THING TO WATCH FOR IS THE EXPLOSIVE COMBO OF
(4)          ;*           "MODE A0 (0)" H + "MODE A1 (0)" H (MODE 0) + "AUTO INC (1)" H +
(4)          ;*           "A OVERFLOW" ALL FEEDING THE DOWN COUNT SIDE OF THE 74193 CHIP.
(4)          ;*           THE RESULTS SHOULD BE 177776.
(4)          ;*PART2: IF PART 1 WAS SUCCESSFUL WE'LL LOOK TO SEE IF
(4)          ;*           THE COUNTER GOT LOADED WITH THE NEW VALUE 177776.
(4)          ;*           THE HANG-UP HERE IS THAT "A OVERFLOW" FEEDS A ONE SHOT
(4)          ;*           THAT GENERATES "A RELOAD" H. WE KNOW THAT WE CAN
(4)          ;*           GET "A RELOAD" H BUT THE BIG TEST HERE IS SEEING IF THAT
(4)          ;*           ONE SHOT SPITS OUT "A RELOAD" H TOO SOON TO CATCH THE BUFFER
(4)          ;*           WITH ITS PANTS DOWN AS ITS DECREMENTING ITSELF.
(4)

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T120 *TEST THE AUTODECREMENT FEATURE OF CLOCK A'S BUFFER

SEQ 0114

```

(5)          :* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(5)
(3)
(2)          014600 000004          TST120: SCOPE

2652          :MAKE SURE CLOCK B IS CLEAR.
2653          :MAKE SURE CLOCK A IS CLEAR.
2654          :LOAD BUFFER + COUNT REGS.
2655          :SET AUTO INCREMENT MODE
2656          :ENABLE COUNTER, MODE 0, RATE STP1
2657          :ZAP! A MAINTENANCE STP1 HAS BEEN MADE.
2658          :STOP HERE AND LOOK WHAT JUST HAPPENED.
2659          :1. STP1 CLOCKED THE COUNTER (SET 177777).
2660          :2. COUNTER OVERFLOWED - "A OVERFLOW" L
2661          :3. MODE 0 + "A OVERFLOW" L + "A AUTO INC (1)" H
2662          :DOWN COUNTED THE BUFFER.
2663          :4. "A OVERFLOW" L GOES THROUGH ONE SHOT DELAY
2664          :TO GIVE "A RELOAD" H
2665          :5. "A RELOAD" H CAUSES A BUFFER TO COUNTER
2666          :RELOAD.

2667          014602 005037 001124          CLR      $GDDAT
2668          :*      MOV      $GDDAT,@BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
2669          (1)     MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2670          (1)     MOV      #177777,$GDDAT
2671          014626 012737 177777 001124          :*      MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
2672          (1)     MOV      #20,$GDDAT
2673          014644 012737 000020 001124          :*      MOV      $GDDAT,@BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
2674          (1)     MOV      #15,$GDDAT
2675          014662 012737 000015 001124          :*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2676          (1)     MOV      #15,$GDDAT
2677          (1)     MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2678          014710 052737 010000 001124          :*      MOV      @ASR,$GDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
2679          (1)     BIS      #BIT12,$GDDAT
2680          (1)     MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2681          :PART 1 DID BUFFER GET DECREMENTED?
2682          014726 012737 177776 001124          MOV      #177776,$GDDAT      ;SET FOR ERROR TYPEOUT IF ANY.
2683          :READ THE RESULTS OF THE BUFFER.
2684
2685          (1)     MOV      @ABR,$BDDAT      ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
2686          014744 023727 001126 177776          :*      CMP      $BDDAT,#177776      ;DID BUFFER DECREMENT TO 177776?
2687          014752 001402                      BEQ      1$      ;BR IF YES TO PART 2
2688
2689          ::::::::::::::::::::> ERROR <<::::::::::::::::::
2690          014754 104012          ERROR    12          ;ERROR-CLOCK A. AFTER AN OVERFLOW
2691          :WITH AUTO INC ENABLED MODE 0, THE
2692          :BUFFER REGISTER FAILED TO DOWN COUNT
          :SEE ABOVE COMMENTS FOR SEQUENCE

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T120 *TEST THE AUTODECREMENT FEATURE OF CLOCK A'S BUFFER

SEQ 0115

2693 014756 000411 BR 2\$:OF EVENTS.
2694 ;IF ERROR ONLY LOOP ON PART 1.
2695 ;;;\$>> ERROR <<\$
2696 014760 1\$: " ;PART 2 DID NEW COUNT GET TRANSFERRED TO COUNT REGISTER?
2697 ;READ THE COUNT REGISTER
2698
2699 (1)
2700 014770 023727 001126 177776 ;*. MOV AACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
2701 CMP \$BDDAT,#177776 ;DID NEW VALUE OF THE BUFFER
2702 ;REGISTER GET PROPERLY LOADED INTO
2703 014776 001401 BEQ 2\$;THE COUNT REGISTER?
2704 ;BR IF YES - NEXT TEST.
2705 ;;;\$>> ERROR <<\$
2706 015000 104012 ERROR 12 ;ERROR CLOCK A. NEW CONTENTS OF
2707 ;BUFFER REGISTER FAILED TO BE PROPERLY
2708 ;LOADED INTO COUNT REGISTER AFTER
2709 ;AUTO DECREMENT.
2710 ;SEE ABOVE COMMENTS FOR SEQUENCE OF EVENTS.
2711 ;;;\$>> ERROR <<\$
2712 015002 005037 001124 2\$: CLR SGDDAT ;CLEAR AUTO INC OPTION.
2713 (1) ;*: MOV SGDDAT,@BSR ;/ PUT DATA FROM SGDDAT TO DEVICE REG BSR
2714 ;*****
2715 (3) ;*TEST 121 *TEST THAT CLOCK A'S 1 MHZ CLK CAN BE DISABLED
2716 (4) ;*FOR THIS TEST, WE'LL TRY DISABLING THE 1 MHZ CLOCK. TO DO THIS.
2717 (4) ;*WE'LL SET THE "DISABLE OSC 1 MHZ", BIT 11 IN CLOCK B SR. THEN
2718 (4) ;*COUNTED OR OVERFLOWED, IF SO ERROR.
2719 (4) ;*THE UNKNOWN THING HERE IS BIT 11 SETTING THE DISABLE F/F THAT
2720 (4) ;*GATES WITH THE 1 MHZ FREG TO PRODUCE "A 1 MHZ CLK" L
2721 (5) ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT B"
2722 (5) ;*
2723 (3) ;*****
2724 (2) 015016 000004 TST121: SCOPE ;CLEAR CLOCK A.
2725 ;SET THE "DISABLE OSC 1 MHZ" F/F.
2726 ;CLEAR THE BUFFER + COUNT REGS.
2727 ;START CLOCK: RATE 1 MHZ, MODE 0, GO.
2728 2729 015020 005037 001124 CLR SGDDAT
2730 ;CLEAR CLOCK A.
2731 ;SET THE "DISABLE OSC 1 MHZ" F/F.
2732 ;CLEAR THE BUFFER + COUNT REGS.
2733 ;START CLOCK: RATE 1 MHZ, MODE 0, GO.
2734 015034 012737 004000 001124 ;*: MOV SGDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
2735 015052 005037 001124 MOV #BIT11,SGDDAT
2736 ;*: MOV SGDDAT,@BSR ;/ PUT DATA FROM SGDDAT TO DEVICE REG BSR
2737 CLR SGDDAT

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T121 *TEST THAT CLOCK A'S 1 MHZ CLK CAN BE DISABLED

SEQ 0116

(1) 2736 015066 012737 000003 001124 ;* MOV \$GDDAT,ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
2737 (1) 2738 015104 005000 ;* MOV \$GDDAT,ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
2739 015106 105200 CLR RO ;SHORT DELAY. WE ALLOW THIS DELAY TO
2740 015110 100376 1\$: INC B RO OCCUR. IF THE 1 MHZ CLOCK IS DISABLED
2741 ; SEE SOMETHING IN THE COUNT REGISTERS
2742 (1) 2743 015122 005737 001126 ;* MOV AACR,\$BDDAT ;READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
2744 015126 001007 TST SBDDAT ;DOES COUNT REG HAVE ANYTHING IN IT?
BNE 2\$;YES - REPORT ERROR!
2745 (1) 2746 015140 105737 001126 ;* MOV AASR,\$BDDAT ;READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
2747 015144 100001 TSTB SBDDAT ;NO - BR NEXT TEST - NO ERROR.
2748 ;;;\$>> ERROR <<\$
2749 015146 104012 2\$: ERROR 12 ;ERROR - UNABLE TO DISABLE 1 MHZ CLK
2750 ;USING 'DISABLE OSC 1 MHZ' F/F
2751 ;;;\$>> ERROR <<\$
2752 2753 015150 005037 001124 3\$: CLR \$GDDAT ;CLEAR CLOCK A.
2754 (1) ;* MOV \$GDDAT,ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR

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T122 *TEST THAT CLOCK B WILL COUNT ONCE FIRST CLOCK B COUNT

SEQ 0118

2800 :TO SCOPE: CHECK LOAD + CLEAR INPUTS TO
2801 :COUNT REG TO SEE IF NOT BEING HELD LOW.
2802 :IF OK SEE IF WE'RE GETTING ANY "CLOCK B" L
2803 :PULSES - WE SHOULD GET ONE EACH LOOP OF
2804 :THIS SUBTEST. "CLOCK B" L COMES FROM
2805 :THE B CLOCK TIMING SECTION. THE RATE IS
2806 :1 MHZ. "B 1 MHZ" L IS GENERATED BY
2807 :"A 1 MHZ" H + "FEED B TO A (1)" H.
2808 :THE "A 1 MHZ" IS GENERATED BY "MAINT
2809 :SIMUL 1 MHZ" IN CLOCK A.
2810

2811 015314 1\$:
 2812
 2826
 2827
 (3) ;*****
 (4) *TEST 123 *TEST THE ABILITY IF CLOCK B TO COUNT FROM ZERO TO OVERFLOW
 (4)
 (4) ;*
 (4) *LAST TEST WE FOUND OUT WE COULD ADVANCE CLOCK A'S COUNTER,
 (4) *SO IN THIS TEST WE'RE GOING TO GO FROM 0-377 COUNTING.
 (4) *WE'LL USE THE SAME PROCEDURE AS LAST TEST TO GENERATE "CLOCK B" L.
 (4) *UNKNOWN IS THE ABILITY OF THE F/F'S TO PROPAGATE THEIR OVERFLOWS.
 (4)
 (4) ;*
 (4) *IF IT IS DESIRED TO START THIS TEST AT A VALUE OTHER THAN 0, CHANGE
 (4) *THE SECOND INSTR. OF THIS TEST TO A VALUE TO BE LOADED INTO THE BUFFER
 (4) *TO THAT VALUE DESIRED.
 (4)
 (5)
 (5) ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF B"
 (5)
 (3)
 (2) 015314 000004 TST123: SCOPE
 2828
 2829 015316 005037 001124 CLR \$GDDAT ;START THE COUNTER FROM ZERO.
 2830 ;NOTE: A VALUE OTHER THAN ZERO MAY BE
 2831 ;PATCHED IN HERE IN ORDER THAT A COUNT
 2832 ;MAY BE STARTED HIGHER.
 2833 015322 005037 001354 1\$: CLR \$TMDAT
 2834 ;* MOV \$TMDAT,@ASR ; PUT DATA FROM \$TMDAT TO DEVICE REG ASR
 2835 ;CLEAR CLOCK B, DISABLE 1 MHZ CLOCK A.
 2836 015336 012737 004000 001354 MOV #BIT11,\$TMDAT
 2837 ;* MOV \$TMDAT,@BSR ; PUT DATA FROM \$TMDAT TO DEVICE REG BSR
 2838 ;LOAD VALUE INTO COUNT + BUFFER REGS.
 2839 ;"1\$" IS THE LOOP BACK POINT ON
 2840 ;"LOOP ON TEST" (SW14=1) FEATURE. NORMAL
 2841 ;LOOP BACK POINT WILL BE '2\$'.
 2842
 2843 ;* MOV \$GDDAT,@BBR ; PUT DATA FROM \$GDDAT TO DEVICE REG BBR
 2844 ;SELECT: "DISABLE OSC 1 MHZ"; "FEED B TO A";
 2845 ;RATE 1 MHZ.
 2846 ;GO. ENABL MUST BE SET AFTER "FEED B TO A"
 2847 015364 012737 004042 001354 MOV #4042,\$TMDAT

```

2848
2849 015402 005237 001354      ;*    MOV    $TMDAT,@BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
2850
2851 015416      ;*    MOV    $TMDAT,@BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
2852
2853      2$:          ;GENERATE A CLOCK PULSE.  
;SHOULD CAUSE THE CLOCK TO  
;INCREMENT ONCE.
2854
2855 015426 052737 004000 001354 ;*    MOV    @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
2856
2857 015444 005237 001124      ;*    MOV    $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
2858      INC    $GDDAT      ;$GDDAT IS USED TO KEEP TRACK OF THE  
;VALUE THE CLOCK SHOULD COUNT TO.
2859
2860
2861 015460 123737 001126 001124      ;*    MOV    @BCR,$BDDAT      ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
2862
2863 015466 001402      CMPB   $BDDAT,$GDDAT      ;DID THE COUNT OCCUR CORRECTLY?  
BEQ    3$      ;IF YES - BR '3$'.
2864
2865      ;;;$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$
2866 015470 104015      ERROR   15      ;ERROR CLOCK B FAILED TO UPCOUNT  
;CORRECTLY - SEE COMMENTS AT SUB-TEST  
;HEADING FOR MORE DETAILS.
2867
2868
2869      ;;;$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$
2870 015472 000403      BR     4$      ;  

2871
2872 015474 105737 001124      3$:    TSTB   $GDDAT      ;DID WE ACHIEVE OVERFLOW YET?  
015500 001410      BEQ    5$      ;
2873
2874
2875 015502 032777 040000 163430 4$:    BIT    #BIT14,@SWR      ;LOOP ON CURRENT COUNT?
2876 015510 001742      BEQ    2$      ;BR IF NO TO NEXT COUNT UPDATE.
2877 015512 162737 000001 001124      SUB    #1,$GDDAT      ;IF YES DECREMENT EXPECTED AND RELOAD.
2878 015520 000700      BR     1$      ;GO TO RELOAD POINT
2879
2880 015522      5$:          ;END SUBTEST.
2881
2882
2883
2884      ;*****  
2885  (3) *TEST 124      *TEST THAT CLOCK B CAN GENERATE AN OVERFLOW  
2886  (4)      ;*  
2887  (4)      ;*NOW WE'LL TRY AND GENERATE 'B OVERFLOW' L WHICH SETS BIT 07.  
2888  (4)      ;*WE'LL DO IT BY PRESETTING THE BUFFER TO 377 AND GENERATING A "CLOCK B" L  
2889  (4)      ;*WE ALREADY KNOW WE CAN ADVANCE THE COUNTER, WHAT WE  
2890  (4)      ;*WANT TO SEE IS 'B OVERFLOW' L COME OVER AND DIRECT SET  
2891  (4)      ;*'OVERFLOW FL B' F/F (BIT 07 IN CSR).  
2892  (5)      ;*  
2893  (5)      ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF B"  
2894  (5)      ;*  
2895  (4)

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T124 *TEST THAT CLOCK B CAN GENERATE AN OVERFLOW

SEQ 0120

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(3) 015522 000004 :***** TST124: SCOPE *****
2894
2895
2896
2897
2898
2899
2900
2901
2902
2903
2904 015524 005037 001124 CLR $GDDAT ;DID OVERFLOW FLAG SET?
2905
2906 (1)
2907 (1)
2908 015550 012737 000377 001124 ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2909 (1)
2910 015566 012737 004042 001124 ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
2911 (1)
2912 015604 005237 001124 ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
2913 (1)
2914 015630 052737 004000 001124 ;* INC $GDDAT ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
2915 (1)
2916 (1)
2917 015656 105737 001126 ;* MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
2918 015662 100402 TSTB $BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
2919 BMI 1$ ;BR IF YES TO "1$".
2920
2921 015664 104014 ERROR 14 ;ERROR CLOCK B 'B OVERFL FLAG' (CSR BIT7)
2922
2923 015666 000411 ;* BR 2$ ;FAILED TO SET ON OVERFLOW.
2924 015670 1$ ;WAS COUNTER RELOAD AFTER OVERFLOW
2925 (1)
2926 015700 022737 000377 001126 ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
2927
2928 015706 001401 BEQ 2$ ;BR IF YES TO NEXT TEST.
2929
2930 015710 104014 ERROR 14 ;ERROR CLOCK B COUNT REG. FAILED
2931
2932

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T126 *TEST THAT CLOCK B DOESN'T COUNT WHEN NO RATE IS SELECTED

SEQ 0122

2968
(3)
(3)
(2) 016006 000004
2969
2970
2971
2972
2973
2974
2975 016010 005037 001124
2976 (1) CLR \$GDDAT
2977 (1) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
2978 (1) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
2979 016044 005237 001124
2980 (1) ;* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
2981 016060 005000
2982 016062 105200
2983 016064 001376
2984
2985
2986
2987 (1) ;* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
2988 016076 005737 001126
2989 016102 001401
2990 ;:;\$> ERROR <<\$
2991 016104 104014
2992
2993
2994 ;:;\$> ERROR <<\$
2995 016106
2996
3047 2\$:;

;CLEAR CLOCK A.
;CLEAR CLOCK B.
;ZEROS TO BUFFER + COUNT REGS.
;ENABLE COUNTER TO COUNT - RATE - 0
;(NO RATE).

;* CLR RO
;* INC RO
;* BNE 1\$
;/ DELAY FOR ANY COUNT THAT
; COULD FALSELY OCCUR.
; THIS DELAY APPROX. 369 MS ON A
; PDP 11/20.

;DID ANY COUNT OCCUR?

;* MOV TST 2\$
;* BEQ 2\$
;/IF NO BR TO NEXT TEST.

;ERROR - CLOCK B COUNTED WHEN ENABLED BUT
;NO RATE SELECTED. BETTER FIND OUT
;WHATS GENERATING 'CLOCK B' L PULSES.

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T126 *TEST THAT CLOCK B DOESN'T COUNT WHEN NO RATE IS SELECTED

SEQ 0123

3048 :/#
(1)
(5)
(4) :***** *TEST 127 *TEST THE ABILITY OF CLOCK B TO COUNT AT 1MHZ PART 1
(5)*
(5) :THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
(5) :IN RATE: 1MHZ PART1
(6)*
(6) : PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT A"
(6)*
(5)*
(4)*
(3) 016106 000004 TST127: SCOPE
(1)
(1) 016110 005037 001124 CLR \$GDDAT ;/CLEAR CLOCK A.
(1)
(1) ;* MOV \$GDDAT,@ASR ;/ CLEAR CLOCK B.
(1) ;* MOV \$GDDAT,@BSR ;/ CLEAR THE BUFFER + COUNT REGS.
(1) ;/SELECT: RATE: 1MHZ ; GO.
(2)
(2) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(2) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(2) ;* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
(1) 016144 012737 000003 001124 ;* MOV #1!2,\$GDDAT
(2) ;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
(1)
(1) 016162 005000 ;\$: CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.
(1) 016164 005200 ;INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.
(1) 016166 001376 ;BNE 1\$;/ON A PDP-11/20.
(1)
(1) ;/DID COUNTER COUNT AT ALL?
(2)
(2) ;* MOV @BCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN \$BDDAT.
(1) 016200 005737 001126 ;TST \$BDDAT ;/BR IF YES - NEXT TEST.
(1)
(2) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(1) 016216 105737 001126 ;TSTB \$BDDAT ;/COUNT TO OVERFLOW - SO WE'LL SEE IF
(1) ;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
(1) 016222 100401 BMI 2\$;/BR IF SET - NEXT TEST.
(2) ;:\$> ERROR <<\$
(1) 016224 104014 ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT
(1) ;/AT 1MHZ RATE.
(2) ;:\$> ERROR <<\$
(1) 016226 2\$:

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T127 *TEST THE ABILITY OF CLOCK B TO COUNT AT 1MHZ PART 1

SEQ 0124

3049

;#

;*****
;*TEST 130 *TEST THE ABILITY OF CLOCK B TO COUNT AT 100KHZ PART 1
;*
;*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
;*IN RATE: 100KHZ PART1
;*
;* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT A"
;*

(3) 016226 000004

TST130: SCOPE

;CLEAR CLOCK A.

(1) 016230 005037 001124

CLR \$GDDAT

;CLEAR CLOCK B.
;CLEAR THE BUFFER + COUNT REGS.
;SELECT: RATE: 100KHZ ; GO.

(1) 016264 012737 000005 001124

;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
;* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR

(1) 016302 005000

;* MOV #1!4,\$GDDAT ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
1\$: CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.
INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.
BNE 1\$;/ON A PDP-11/20.

(1) 016304 005200

(1) 016306 001376

;/DID COUNTER COUNT AT ALL?

(1) 016320 005737 001126

;* MOV ABCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN \$BDDAT.
TST SBDDAT ;/BR IF YES - NEXT TEST.

(1) 016324 001010

;* TSTB SBDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
BNE 2\$;/COUNT TO OVERFLOW - SO WE'LL SEE IF
;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.

(1) 016336 105737 001126

;* BMI 2\$;/BR IF SET - NEXT TEST.

(1) 016342 100401

;:\$>> ERROR <<\$

(1) 016344 104014

ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT
;/AT 100KHZ RATE.

(1) 016346

2\$:

3050 ;#
(1)
(5)
(4) :*****
(4) *TEST 131 *TEST THE ABILITY OF CLOCK B TO COUNT AT 10KHZ PART 1
(5)*
(5) *THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
(5) IN RATE: 10KHZ PART1
(6)*
(6) * PROBABLE SYNC POINT FOR THIS TEST: 'LD STAT A'
(6)*
(5)*
(4) :*****
(3) 016346 000004 TST131: SCOPE
(1)
(1) 016350 005037 001124 CLR SGDDAT ;/CLEAR CLOCK A.
(1) ;/CLEAR CLOCK B.
(1) ;/CLEAR THE BUFFER + COUNT REGS.
(1) ;/SELECT: RATE: 10KHZ ; GO.
(2)
(2) ;* MOV SGDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(2) ;* MOV SGDDAT,@BSR ;/ PUT DATA FROM SGDDAT TO DEVICE REG BSR
(2) ;* MOV SGDDAT,@BBR ;/ PUT DATA FROM SGDDAT TO DEVICE REG BBR
(1) 016404 012737 000007 001124 ;* MOV #1!6,\$GDDAT
(2) ;* MOV SGDDAT,@BSR ;/ PUT DATA FROM SGDDAT TO DEVICE REG BSR
(1)
(1) 016422 005000 1\$: CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.
(1) 016424 005200 INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.
(1) 016426 001376 BNE 1\$;/ON A PDP-11/20.
(1)
(1) ;/DID COUNTER COUNT AT ALL?
(2)
(2) ;* MOV ABCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN SBDDAT.
(1) 016440 005737 001126 TST \$BDDAT
(1) 016444 001010 BNE 2\$;/BR IF YES - NEXT TEST.
(1)
(2)
(2) ;* MOV ABSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN SBDDAT.
(1) 016456 105737 001126 TSTB \$BDDAT ;/COUNT TO OVERFLOW - SO WE'LL SEE IF
(1) ;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
(1) 016462 100401 BMI 2\$;/BR IF SET - NEXT TEST.
(2)
;:\$>> ERROR <<\$
(1) 016464 104014 ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT
(1) ;/AT 10KHZ RATE.
(2)
;:\$>> ERROR <<\$
(1) 016466 2\$:

3051

;/#

*:TEST 132 *TEST THE ABILITY OF CLOCK B TO COUNT AT 1KHZ PART 1
*:THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
*:IN RATE: 1KHZ PART1
*: PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT A"

(3) 016466 000004

TST132: SCOPE

(1)
(1) 016470 005037 001124 CLR SGDDAT ;/CLEAR CLOCK A.
(1)
(1) ;* MOV SGDDAT,@ASR ;/CLEAR CLOCK B.
(1) ;* MOV SGDDAT,@BSR ;/CLEAR THE BUFFER + COUNT REGS.
(1) ;* MOV SGDDAT,@BBR ;/SELECT: RATE: 1KHZ ; GO.
(2)
(2) ;* MOV SGDDAT,@ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
(2)
(2) ;* MOV SGDDAT,@BSR ;/ PUT DATA FROM SGDDAT TO DEVICE REG BSR
(2)
(2) ;* MOV SGDDAT,@BBR ;/ PUT DATA FROM SGDDAT TO DEVICE REG BBR
(1) 016524 012737 000011 001124 ;* MOV #1!10,\$GDDAT
(2)
(2) ;* MOV SGDDAT,@BSR ;/ PUT DATA FROM SGDDAT TO DEVICE REG BSR
(1)
(1) 016542 005000 ;* CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.
(1) 016544 005200 1\$: INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.
(1) 016546 001376 BNE 1\$;/ON A PDP-11/20.
(1)
(1) ;/DID COUNTER COUNT AT ALL?
(2)
(2) ;* MOV ABCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN \$BDDAT.
(1) 016560 005737 001126 TST \$BDDAT
(1) 016564 001010 BNE 2\$;/BR IF YES - NEXT TEST.
(1)
(2) ;* MOV ABCR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
(1) 016576 105737 001126 TSTB \$BDDAT
(1) ;/COUNT TO OVERFLOW - SO WE'LL SEE IF
(1) ;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
(1) 016602 100401 BMI 2\$;/BR IF SET - NEXT TEST.
(2) ;:SSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSS
(1) 016604 104014 ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT
(1) ;/AT 1KHZ RATE.
(2) ;:SSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSS
(1) 016606 2\$:

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T133 *TEST THE ABILITY OF CLOCK B TO COUNT AT 100HZ PART 1

SEQ 0128

3053

```

(1)      :/#  

(5)      ;*****  

(4)      *TEST 134      *TEST THE ABILITY OF CLOCK B TO COUNT AT LINE-FREQ PART 1  

(5)  

(5)      ;*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT  

(5)      ;IN RATE: LINE-FREQ      PART1  

(6)      ;*  

(6)      ; PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT A"  

(6)  

(5)  

(4)  

(3) 016726 000004  

(1)      TST134: SCOPE  

(1)  

(1) 016730 005037 001124          CLR      $GDDAT      ;/CLEAR CLOCK A.  

(1)  

(1)          ;/CLEAR CLOCK B.  

(1)          ;/CLEAR THE BUFFER + COUNT REGS.  

(1)          ;/SELECT: RATE: LINE-FREQ ; GO.  

(2)  

(2)          ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  

(2)  

(2)          ;*      MOV      $GDDAT,@BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  

(2)  

(2)          ;*      MOV      $GDDAT,@BBR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  

(1) 016764 012737 000017 001124  ;*      MOV      #1!16,$GDDAT  

(2)          ;*      MOV      -$GDDAT,@BSR      ;/-PUT DATA EROM $GDDAT TO DEVICE REG BSR  

(1)  

(1) 017002 005000          CLR      R0      ;/NOW WE'LL DO A LITTLE DELAY.  

(1) 017004 005200          INC      R0      ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.  

(1) 017006 001376          BNE      1$      ;/ON A PDP-11/20.  

(1)  

(1)          ;/DID COUNTER COUNT AT ALL?  

(2)  

(2) 017020 005737 001126      ;*      MOV      @BCR,$BDDAT      ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  

(1) 017024 001010          TST      $BDDAT      ;/BR IF YES - NEXT TEST.  

(1)  

(2)  

(2) 017036 105737 001126      ;*      MOV      @BSR,$BDDAT      ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.  

(1)  

(1)          ;/COUNT TO OVERFLOW - SO WE'LL SEE IF  

(1)          ;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.  

(1) 017042 100401          BMI      2$      ;/BR IF SET - NEXT TEST.  

(2)  

(2)      ::::::::::::::> ERROR <<:::::::::::::::::::  

(1) 017044 104014          ERROR    14      ;/ERROR CLOCK B - COUNTER FAILED TO COUNT  

(1)          ;/AT LINE-FREQ RATE.  

(2)  

(2)      ::::::::::::::> ERROR <<:::::::::::::::::::  

(1) 017046          2$:

```

3054
3063

3064

(3) :*****
(4) *TEST 135 *TEST THE "FEED B TO A" 24 BIT COUNTER FEATURE OF CLOCKS A + B
(4)
(4) *WE'RE GOING TO TEST CLOCKS A+B AS A 24 BIT COUNTER; THAT IS;
(4) *WE'RE GOINT TO TAKE THE OVERFLOW FROM CLOCK B AND FEED IT INTO
(4) *CLOCK A.
(5)
(5) * PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF B"
(5)
(4)
(3) :*****
(2) 017046 000004 TST135: SCOPE

3065

3066 :CLEAR CLOCK A.
3067 :CLEAR CLOCK B.
3068 :CLEAR A'S BUFFER + COUNT REGISTERS.
3069 :PRESET B'S BUFFER + COUNT TO -1 FROM
3070 :OVERFLOW.
3071 :SELECT: "DISABLE OSC 1 MHZ"; RATE 1 MHZ;
3072 :"FEED B TO A"
3073 :SET ENABL. MUST BE SET AFTER "FEED B TO A".
3074 :ENABLE CLOCK A; MODE 0; RATE 0.
3075 :SIMULATE A 1 MHZ PULSE - THIS PULSE
3076 :WILL CLOCK CLOCK B'S COUNTER
3077 :REGISTER. AN OVERFLOW WILL
3078 :OCCUR - THAT OVERFLOW SHOULD
3079 :CLOCK CLOCK A'S COUNT REGISTER.
3080 :DID CLOCK A'S COUNT REG GET CLOCKED?

3081 017050 005037 001124

CLR \$GDDAT

3082 (1)		;	MOV \$GDDAT,@ASR	;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
3083 (1)		;	MOV \$GDDAT,@BSR	;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
3084 (1)		;	MOV \$GDDAT,@ABR	;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
3085 017104 012737 000377 001124		;	MOV #377,\$GDDAT	
3086 (1)		;	MOV \$GDDAT,@BBR	;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
3087 017122 012737 004042 001124		;	MOV #4042,\$GDDAT	
3088 (1)		;	MOV \$GDDAT,@BSR	;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
3089 017140 005237 001124		;	INC \$GDDAT	
3090 (1)		;	MOV \$GDDAT,@BSR	;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
3091 017154 012737 000001 001124		;	MOV #1,\$GDDAT	
3092 (1)		;	MOV \$GDDAT,@ASR	;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
3093 (1)		;	BIS #BIT11,\$GDDAT	;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.
3094 017202 052737 004000 001124		;	MOV \$GDDAT,@ASR	;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
3095 (1)		;	MOV @ACR,\$BDDAT	
3096 (1)		;	TST \$BDDAT	;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
3097 017230 005737 001126				
3098				

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T135 *TEST THE "FEED B TO A" 24 BIT COUNTER FEATURE OF CLOCKS A + B

SEQ 0130

3099 017234 001001 BNE 1\$;IF YES THEN BR NEXT TEST.
3100 :::\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$

3101 017236 104014 ERROR 14 ;ERROR - UNABLE TO CLOCK CLOCK A'S
3102 ;COUNT REGISTER WITH THE OVERFLOW
3103 ;FROM CLOCK B.
3104 ;THE MOST LOGICAL PLACE TO START
3105 ;WOULD BE !A CLOCK TIMING'.
3106 ;"FEED B TO A (1)" H + 'B OVERFLOW' H
3107 ;SHOULD BE COMING TOGETHER GOING
3108 ;INTO THE MUX - BEGING SELECTED AND
3109 ;COMING OUT OF THE MUX TO BECOME
3110 ;"CLOCK A" L.
3111 :::\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$> ERROR <<\$

3112 017240 1\$:
3113 .SBTTL *
3114 .SBTTL * PHASE 6 CLOCK A+B ADVANCE TESTING
3115 .SBTTL *
3116

3134 ;//
 3135
 3136 ;*****
 (3) *TEST 136 *TEST THAT THE TRAILING EDGE OF STP1 WILL INCR. COUNTER
 (4)
 (4) *IN THIS TEST WE'LL SEE IF WE CATCH THE FIRST COUNT
 (4) *AFTER STP1 COMES IN AND SETS THE ENABLE F/F ('ST1 ENB COUNTER'
 (4) *SET).
 (4) *WHAT WE SHOULD SEE IS THE LEADING EDGE OF ST1 COME
 (4) *IN AND SET THE ENB F/F AND THE TRAILING EDGE TRIGGER
 (4) *A 'CLOCK A' PULSE TO INCREMENT THE COUNTER.
 (4) *WE KNOW FROM A PREVIOUS TEST THAT AN STP1 WILL
 (4) *COME IN AND SET 'ENABL CNTR A' F/F AND THAT THE
 (4) *COUNTER WILL INCREMENT, SO WHATS HAPPENING IS WE'RE ACCUALLY
 (4) *LOOKING AT THE TRAILING EDGE OF STP1 TO SEE IF ITS DOING
 (4) *THE INCREMENTING
 (4)
 (5)
 (5) * PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
 (5)
 (3) ;*****
 (2) 017240 000004 TST136: SCOPE
 3137
 3138 ;CLR CLK A, SET 'ST1 ENB COUNTER'.;RATE:STP1.
 3139 ;CLR COUNT + BUFFER REGS.
 3140 ;GENERATE A MAINTENANCE ST1.
 3141 ;THE LEADING EDGE SHOULD CAUSE
 3142 ;'ENABL CNTR A' F/F TO SET (CSR BIT 00).
 3143 ;THE TRAILING EDGE SHOULD CLOCK
 3144 ;THE COUNTER ONCE.
 3145 017242 012737 000001 001354 MOV #BIT0,\$TMDAT
 3146 (1) ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
 3147 017260 005037 001124 CLR \$GDDAT
 3148 (1) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
 3149 (1) ;* MOV @ASR,\$GDDAT ;READ DEVICE REG ASR,PUT DATA IN \$GDDAT.
 3150 017304 052737 010000 001124 BIS #BIT12,\$GDDAT
 3151 (1) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
 3152 017322 012737 000001 001124 MOV #1,\$GDDAT ;SET S/B FOR ERROR TYPEOUT IF NEEDED.
 3153 ;READ THE COUNT REGISTER.
 3154
 3155 (1) ;* MOV @ACR,\$BDDAT ;READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
 3156 017340 023737 001126 001124 CMP SBDDAT,\$GDDAT ;DID THE COUNT REG COUNT ONCE?
 3157 017346 001401 BEQ 1\$;BR IF YES TO NEXT TEST.
 3158
 3159 ;:;SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
 3160
 3161 017350 104012 ERROR 12 :ST1 FAILED TO COUNT
 3162 ;CLOCK A'S COUNT REG. AFTER SETTING
 3163 ;'ENABL CNTR A' - SEE TEST HEADING

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T136 *TEST THAT THE TRAILING EDGE OF STP1 WILL INCR. COUNTER

C 11
SEQ 0132

3164
3165

:COMMENTS

::;SSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS

3166
3167 017352
3168
3257

1\$:

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T136 *TEST THAT THE TRAILING EDGE OF STP1 WILL INCR. COUNTER

SEQ 0133

3258 ;#
(1)
(5)
(4) :*****
(5) *TEST 137 *TEST CLOCK A'S 100KHZ DIVIDER
(5) *
(5) *IN THIS TEST WE'LL SEE IF THE 100KHZ DIVIDER WILL DIVIDE 1MHZ
(5) *BY 10 TO GIVE US A 100KHZ CLK L PULSE.
(5) *TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
(5) *PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100KHZ
(5) *PULSES.
(5) *THEN WE'LL GENERATE 9 MORE 1MHZ PULSES AND MAKE
(5) *SURE THAT WE DON'T GET ANOTHER 100KHZ PULSE.
(5)
(6)
(6) * PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
(6)
(4) :*****
(3) 017352 000004 TST137: SCOPE
(1)
(1) :/CLEAR CLOCK B.
(1) :/CLEAR CLOCK A.
(1) :/CLEAR A'S BUFFER + COUNT REGS.
(1) :/DISABLE THE 1MHZ OSC.
(1) :/ENABLE CNTR, RATE: 100KHZ ;MODE.
(1) 017354 005037 001354 CLR STMDAT
(2) ;* MOV STMDAT,@BSR ;/ PUT DATA FROM STMDAT TO DEVICE REG BSR
(2) ;* MOV STMDAT,@ASR ;/ PUT DATA FROM STMDAT TO DEVICE REG ASR
(2) ;* MOV STMDAT,@ABR ;/ PUT DATA FROM STMDAT TO DEVICE REG ABR
(1) 017410 012737 004000 001354 ;* MOV #BIT11,\$STMDAT
(2) ;* MOV STMDAT,@BSR ;/ PUT DATA FROM STMDAT TO DEVICE REG BSR
(2) ;* MOV @ASR,\$STMDAT ;/READ DEVICE REG ASR,PUT DATA IN STMDAT.
(1) 017436 052737 000405 001354 ;* BIS #401!4,\$STMDAT
(2) ;* MOV STMDAT,@ASR ;/ PUT DATA FROM STMDAT TO DEVICE REG ASR
(1) ;/SET TO GENERATE ON 1MHZ PULSES
(1) 017454 012700 177766 MOV #-10.,R0
(1) 017460 1\$: ;/GENERATE 1 1MHZ PULSE
(1) ;/HAS COUNTER ADVANCED ANY?
(2) ;* MOV @ASR,\$STMDAT ;/READ DEVICE REG ASR,PUT DATA IN STMDAT.
(1) 017470 052737 004000 001354 ;* BIS #BIT11,\$STMDAT
(2) ;* MOV STMDAT,@ASR ;/ PUT DATA FROM STMDAT TO DEVICE REG ASR
(2) ;* MOV @ACR,\$SBDDAT ;/READ DEVICE REG ACR,PUT DATA IN SBDDAT.
(1) 017516 005737 001126 TST
(1) 017522 001002 BNE 10\$;/IF SO EXIT THIS LOOP.
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.

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T137 *TEST CLOCK A'S 100KHZ DIVIDER

E 11

SEQ 0134

3259

(1)
(5)
(4) ;/* TEST 140 *TEST CLOCK A'S 10KHZ DIVIDER
(5)
(5) *IN THIS TEST WE'LL SEE IF THE 10KHZ DIVIDER WILL DIVIDE 100KHZ
(5) *BY 10 TO GIVE US A 10KHZ CLK L PULSE.
(5) *TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
(5) *PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 10KHZ
(5) *PULSES.
(5) *THEN WE'LL GENERATE 9 MORE 100KHZ PULSES AND MAKE
(5) *SURE THAT WE DON'T GET ANOTHER 10KHZ PULSE.
(5)
(6)
(6) * PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(6)
(4)
(3) 017642 000004 TST140: SCOPE
(1)
(1) ;/CLEAR CLOCK B.
(1) ;/CLEAR CLOCK A.
(1) ;/CLEAR A'S BUFFER + COUNT REGS.
(1) ;/DISABLE THE 1MHZ OSC.
(1) ;/ENABLE CNTR, RATE: 10KHZ ;MODE.
(1) 017644 005037 001354 CLR \$TMDAT
(2) ;* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
(2) ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(2) ;* MOV \$TMDAT,@ABR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ABR
(1) 017700 012737 004000 001354 ;* MOV #BIT11,\$TMDAT
(2) ;* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
(2) ;* MOV @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
(1) 017726 052737 000407 001354 ;* BIS #401!6,\$TMDAT
(2) ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(1) ;/SET TO GENERATE ON 1MHZ PULSES
(1) 017744 012700 177634 MOV #-100.,R0
(1) 017750 1\$:
(1) ;/GENERATE 1 1MHZ PULSE
(1) ;/HAS COUNTER ADVANCED ANY?
(2) ;* MOV @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
(1) 017760 052737 004000 001354 ;* BIS #BIT11,\$TMDAT
(2) ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(2) ;* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
(1) 020006 005737 001126 TST
(1) 020012 001002 BNE SBDDAT
(1) 10\$;/IF SO EXIT THIS LOOP.
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.

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T140 *TEST CLOCK A'S 10KHZ DIVIDER

SEQ 0136

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(1)          020014 005200           INC      R0      //OSC., THE DIVIDER COULD HAVE
(1)          020016 001354           BNE     1$      //AND COUNT LEFT IN IT.
(1)          020020 012737 000001 001124 10$: MOV      #1,$GDDAT  //AFTER THIS LOOP ,WE SHOULD BE SUNK.
(1)                                     ;/DONE 100. 1MHZ PULSES?
(1)                                     ;/IF NOT - DO ANOTHER.
(1)                                     //SET FOR ERROR TYPEOUT IF NEEDED.
(1)                                     //READ THE COUNTER.
(2)                                     ;*    MOV      @ACR,$BDDAT  //READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(1)          020036 023737 001126 001124  CMP      SBDDAT,$GDDAT  //DID THE COUNTER ADVANCE ONCE?
(1)          020044 001402           BEQ     2$      ;/IF YES - NEXT CHECK.
(2)          ::::::::::::::::::::> ERROR <::::::::::::::::::::::::::::::::::>
(1)          020046 104012           ERROR   12      //ERROR - CLOCK A - 10KHZ - PULSE
(1)                                     ;/NOT GENERATED WHEN 10 100KHZ PULSES
(2)          ::::::::::::::::::::> ERROR <::::::::::::::::::::::::::::>
(1)          020050 000430           BR      4$      //OSC., THE DIVIDER COULD HAVE
(1)          020052 012700 000143           MOV      #99.,R0 ;/GET THE NUMBER OF '1 MHZ' H PULSES
(1)          020056           3$:           ;/GENERATE 9 100KHZ PULSES
(2)          020066 052737 004000 001354  ;*    MOV      @ASR,$TMDAT  //READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(2)                                     BIS      #BIT11,$TMDAT
(1)          020104 005300           ;*    MOV      STMDAT,@ASR  // PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1)          020106 001363           DEC      R0      ;/INORDER TO CHECK TO SEE THAT
(1)                                     BNE     3$      ;/WE DON'T GENERATE ANOTHER 10KHZ PULSE.
(1)                                     //READ THE COUNTER
(2)          020120 023737 001126 001124  ;*    MOV      @ACR,$BDDAT  //READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(1)                                     CMP      SBDDAT,$GDDAT  //WAS ANOTHER 10KHZ PULSE GENERATED?
(1)                                     BEQ     4$      ;/NO-GO TO NEXT TEST!
(2)          ::::::::::::::::::::> ERROR <::::::::::::::::::::::::::::>
(1)          020130 104012           ERROR   12      //ERROR CLOCK A WE SEEM TO HAVE
(1)                                     ;/GENERATED A SECOND 10KHZ PULSE
(1)                                     ;/ON ONLY 9 100KHZ PULSES.
(2)          ::::::::::::::::::::> ERROR <::::::::::::::::::::::::::::>

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T140 *TEST CLOCK A'S 10KHZ DIVIDER

SEQ 0137

3260 ;#
(1)
(5)
(4) :*TEST 141 *TEST CLOCK A'S 1KHZ DIVIDER
(5);*
(5);+IN THIS TEST WE'LL SEE IF THE 1KHZ DIVIDER WILL DIVIDE 10KHZ
(5);+BY 10 TO GIVE US A 1KHZ CLK L PULSE.
(5);+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
(5);+PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 1KHZ
(5);+PULSES.
(5);+THEN WE'LL GENERATE 9 MORE 10KHZ PULSES AND MAKE
(5);+SURE THAT WE DON'T GET ANOTHER 1KHZ PULSE.
(5);*
(6);*
(6);+ PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(6);*
(4);*****
(3) 020132 000004 TST141: SCOPE
(1);/CLEAR CLOCK B.
(1);/CLEAR CLOCK A.
(1);/CLEAR A'S BUFFER + COUNT REGS.
(1);/DISABLE THE 1MHZ OSC.
(1);/ENABLE CNTR, RATE: 1KHZ ;MODE.
(1) 020134 005037 001354 CLR \$TMDAT
(2);* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
(2);* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(2);* MOV \$TMDAT,@ABR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ABR
(1) 020170 012737 004000 001354 ;* MOV #BIT11,\$TMDAT
(2);* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
(2);* BIS @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
(1) 020216 052737 000411 001354 ;* BIS #401!10,\$TMDAT
(2);* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(1);/SET TO GENERATE ON 1MHZ PULSES
(1) 020234 012700 176030 MOV #-1000.,R0
(1) 020240 1\$: ;/GENERATE 1 1MHZ PULSE
(1);/HAS COUNTER ADVANCED ANY?
(2);* MOV @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
(1) 020250 052737 004000 001354 ;* BIS #BIT11,\$TMDAT
(2);* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(2);* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
(1) 020276 005737 001126 TST BNE \$BDDAT
(1) 020302 001002 10\$;/IF SO EXIT THIS LOOP.
(1);/NOTE: WHEN WE DISABLED THE 1 MHZ.

(1) ;/OSC., THE DIVIDER COULD HAVE
(1) ;/AND COUNT LEFT IN IT.
(1) ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
(1) ;/DONE 1000. 1MHZ PULSES?
(1) ;/IF NOT - DO ANOTHER.
(1) 020304 005200 INC R0
(1) 020306 001354 BNE 1\$
(1) 020310 012737 000001 001124 10\$: MOV #1,\$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.
(1) ;/READ THE COUNTER.
(2) ;*: MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
(1) 020326 023737 001126 001124 CMP \$BDDAT,\$GDDAT ;/DID THE COUNTER ADVANCE ONCE?
(1) 020334 001402 BEQ 2\$;/IF YES - NEXT CHECK.
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 020336 104012 ERROR 12 ;/ERROR - CLOCK A - 1KHZ - PULSE
(1) ;/NOT GENERATED WHEN 10 10KHZ PULSES
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 020340 000430 BR 4\$
(1) 020342 012700 001747 2\$: MOV #999.,R0 ;/GET THE NUMBER OF '1 MHZ' H PULSES
(1) 020346 3\$:
(2) ;/GENERATE 9 10KHZ PULSES
(2) 020356 052737 004000 001354 ;*: MOV @ASR,\$TMDAT
(1) BIS #BIT11,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
(2) ;*: MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(1) 020374 005300 DEC R0 ;/INORDER TO CHECK TO SEE THAT
(1) 020376 001363 BNE 3\$;/WE DON'T GENERATE ANOTHER 1KHZ PULSE.
(1) ;/READ THE COUNTER
(2) ;*: MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
(1) 020410 023737 001126 001124 CMP \$BDDAT,\$GDDAT ;/WAS ANOTHER 1KHZ PULSE GENERATED?
(1) 020416 001401 BEQ 4\$;/NO-GO TO NEXT TEST!
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 020420 104012 ERROR 12 ;/ERROR CLOCK A WE SEEM TO HAVE
(1) ;/GENERATED A SECOND 1KHZ PULSE
(1) ;/ON ONLY 9 10KHZ PULSES.
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 020422 4\$:

3261 ;/#
(1)
(5)
(4) :*****
(5) *TEST 142 *TEST CLOCK A'S 100HZ DIVIDER
(5) *
(5) :+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
(5) :+BY 10 TO GIVE US A 100HZ CLK L PULSE.
(5) :+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
(5) :PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
(5) :PULSES.
(5) :+THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
(5) :SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
(5)
(6)
(6) :* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(6)
(4) :*****
(3) 020422 000004 TST142: SCOPE
(1)
(1) :/CLEAR CLOCK B.
(1) :/CLEAR CLOCK A.
(1) :/CLEAR A'S BUFFER + COUNT REGS.
(1) :/DISABLE THE 1MHZ OSC.
(1) :/ENABLE CNTR, RATE: 100HZ ;MODE.
(1) 020424 005037 001354 CLR \$TMDAT
(2) :* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
(2) :* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(2) :* MOV \$TMDAT,@ABR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ABR
(1) 020460 012737 004000 001354 :* MOV #BIT11,\$TMDAT
(2) :* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
(2) :* MOV @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
(1) 020506 052737 000413 001354 :* BIS #401!12,\$TMDAT
(2) :* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(1) :/SET TO GENERATE ON 1MHZ PULSES
(1) 020524 012700 154360 MOV #-10000.,R0
(1) 020530 1\$: ;/GENERATE 1 1MHZ PULSE
(1) ;/HAS COUNTER ADVANCED ANY?
(2) :* MOV @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
(1) 020540 052737 004000 001354 :* BIS #BIT11,\$TMDAT
(2) :* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(2) :* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
(1) 020566 005737 001126 TST \$BDDAT
(1) 020572 001002 BNE 10\$;/IF SO EXIT THIS LOOP.
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.

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(1)                                ;/OSC., THE DIVIDER COULD HAVE
(1)                                ;/AND COUNT LEFT IN IT.
(1)                                ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
(1)                                ;/DONE 10000. 1MHZ PULSES?
(1)                                ;/IF NOT - DO ANOTHER.

(1) 020574 005200      INC    R0
(1) 020576 001354      BNE    1$                ;/SET FOR ERROR TYPEOUT IF NEEDED.

(1) 020600 012737 000001 001124 10$: MOV    #1,$GDDAT      ;/READ THE COUNTER.

(2)                                ;*: MOV    @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.

(1) 020616 023737 001126 001124  CMP    $BDDAT,$GDDAT      ;/DID THE COUNTER ADVANCE ONCE?
(1) 020624 001402      BEQ    2$                ;/IF YES - NEXT CHECK.

(2)                                ;;;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$

(1) 020626 104012          ERROR   12      ;/ERROR - CLOCK A - 100HZ - PULSE
(1)                                ;/NOT GENERATED WHEN 10 1KHZ PULSES

(2)                                ;;;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$

(1) 020630 000430          BR     4$                ;/GET THE NUMBER OF '1 MHZ' H PULSES
(1) 020632 012700 023417      2$: MOV    #9999.,R0
(1) 020636                      3$:                  ;/GENERATE 9 1KHZ PULSES

(2)                                ;*: MOV    @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(1) 020646 052737 004000 001354  BIS    #BIT11,$TMDAT
(2)                                ;*: MOV    $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1) 020664 005300          DEC    R0                ;/INORDER TO CHECK TO SEE THAT
(1) 020666 001363          BNE    3$                ;/WE DON'T GENERATE ANOTHER 100HZ PULSE.

(1)                                ;/READ THE COUNTER

(2)                                ;*: MOV    @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(1) 020700 023737 001126 001124  CMP    $BDDAT,$GDDAT      ;/WAS ANOTHER 100HZ PULSE GENERATED?
(1) 020706 001401          BEQ    4$                ;/NO-GO TO NEXT TEST.

(2)                                ;;;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$

(1) 020710 104012          ERROR   12      ;/ERROR CLOCK A WE SEEM TO HAVE
(1)                                ;/GENERATED A SECOND 100HZ PULSE
(1)                                ;/ON ONLY 9 1KHZ PULSES.

(2)                                ;;;$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$

(1) 020712          4$:

3262
3361
3362
(5)
(4)
(5)

*****  

;*TEST 143      *TEST CLOCK B'S 100KHZ DIVIDER
;*

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T143 *TEST CLOCK B'S 100KHZ DIVIDER

SEQ 0141

(5) :+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
(5) :+BY 10 TO GIVE US A 100HZ CLK L PULSE.
(5) :+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
(5) :+PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
(5) :+PULSES.
(5) :+THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
(5) :+SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
(5)
(6)
(6) :+ PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(6)

(4) 020712 000004

TST143: SCOPE

:/CLEAR CLOCK B.
:/CLEAR CLOCK A.

;/CLEAR B'S BUFFER + COUNT REGS.
;/DISABLE THE 1MHZ OSC.
;/RATE: 100KHZ
;/ENABLE CLOCK B.

(1) 020714 005037 001354

CLR STMDAT

;/ PUT DATA FROM STMDAT TO DEVICE REG BSR

(2) :* MOV STMDAT,@BSR

;/ PUT DATA FROM STMDAT TO DEVICE REG ASR

(2) :* MOV STMDAT,@ASR

;/ PUT DATA FROM STMDAT TO DEVICE REG BBR

(1) 020750 012737 004040 001354 :* MOV #BIT11!BITS5,STMDAT

;

(2) :* MOV STMDAT,@BSR

;/ PUT DATA FROM STMDAT TO DEVICE REG BSR

(2) :* MOV ABRS,\$STMDAT

;/READ DEVICE REG BSR.PUT DATA IN STMDAT.

(1) 020776 052737 000004 001354 :* BIS #4,\$STMDAT

;

(2) :* MOV STMDAT,@BSR

;/ PUT DATA FROM STMDAT TO DEVICE REG BSR

(1) 021014 005237 001354 :* INC STMDAT

;

(2) :* MOV STMDAT,@BSR

;/ PUT DATA FROM STMDAT TO DEVICE REG BSR

(1) 021030 012700 177766 :* MOV #10.,R0

;/SET TO GENERATE 10. 1MHZ PULSES

(1) 021034 :\$:

;/GENERATE 1 1MHZ PULSE

(1) :HAS THE COUNTER ADVANCED?

(2) ;/

(2) :* MOV BIS #BIT11,\$STMDAT

;/READ DEVICE REG ASR.PUT DATA IN STMDAT.

(1) 021044 052737 004000 001354 :* MOV STMDAT,@ASR

;/ PUT DATA FROM STMDAT TO DEVICE REG ASR

(2) :* MOV ABCR,\$SBDDAT

;/READ DEVICE REG BCR.PUT DATA IN SBDDAT.

(1) 021072 005737 001126 :* TST \$BDDAT

;/EXIT LOOP IF SO.

(1) :* BNE 10\$

;/NOTE: WHEN WE DISABLED THE 1 MHZ.

(1) :/ OSC., THE DIVIDER COULD HAVE

;/ HAD ANY COUNT IN IT.

(1) :/AFTER THIS LOOP, WE SHOULD BE SUNK.

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T143 *TEST CLOCK B'S 100KHZ DIVIDER M 11

SEQ 0142

(1) 021100 005200
(1) 021102 001354
(1)
(1) 021104 012737 000001 001124 10\$: MOV #1,\$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.
(1)
(1)
(2)
(2) ;* MOV @BCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN \$BDDAT.
(1)
(1) 021122 023737 001126 001124 CMP \$BDDAT,\$GDDAT ;/DID THE COUNTER ADVANCE ONCE?
(1) 021130 001402 BEQ 2\$;/IF YES - NEXT CHECK
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 021132 104015
(1)
(1)
(1)
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 021134 000430 BR 4\$
(1)
(1) 021136 012700 177767, 2\$: MOV #-9.,R0 ;/GET THE NUMBER OF "1 MHZ" H PULSES
(1)
(1) 021142 3\$:
(2)
(2) 021152 052737 004000 001354 ;* MOV @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
(1)
(2) BIS #BIT11,\$TMDAT
(2) ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(1) 021170 005200 INC R0 ;/IN ORDER TO CHECK TO SEE THAT
(1) 021172 001363 BNE 3\$;/WE DON'T GENERATE ANOTHER 100KHZ PULSE
(1)
(2)
(2) 021204 023737 001126 001124 ;* MOV @BCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN \$BDDAT.
(1) 021212 001401 CMP \$BDDAT,\$GDDAT ;/WAS ANOTHER 100KHZ PULSE GENERATED?
(1)
(2) BEQ 4\$;/NO - GO TO NEXT CHECK.
(1)
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 021214 104015
(1)
(1)
(1)
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 021216 4\$:
3363
(5)
(4) ;*****
(4) ;*TEST 144 *TEST CLOCK B'S 10KHZ DIVIDER
(5)
(5) ;*
(5) ;+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
(5) ;+BY 10 TO GIVE US A 100HZ CLK L PULSE.
(5) ;+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND

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T144 *TEST CLOCK B'S 10KHZ DIVIDER N 11

SEQ 0143

(5) :*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
(5) :*PULSES.
(5) :*THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
(5) :*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
(5)
(6)
(6) :* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(6)
(4) :*****
(3) 021216 000004 TST144: SCOPE
(1)
(1) :/CLEAR CLOCK B.
(1) :/CLEAR CLOCK A.
(1)
(1) :/CLEAR B'S BUFFER + COUNT REGS.
(1) :/DISABLE THE 1MHZ OSC.
(1) :/RATE: 10KHZ
(1) :/ENABLE CLOCK B.
(1) 021220 005037 001354 CLR STMDAT
(2) :* MOV STMDAT,ABSR ;/ PUT DATA FROM STMDAT TO DEVICE REG BSR
(2) :* MOV STMDAT,AASR ;/ PUT DATA FROM STMDAT TO DEVICE REG ASR
(2) :* MOV STMDAT,ABBR ;/ PUT DATA FROM STMDAT TO DEVICE REG BBR
(1) 021254 012737 004040 001354 :* MOV #BIT11!BITS5,STMDAT
(2) :* MOV STMDAT,ABSR ;/ PUT DATA FROM STMDAT TO DEVICE REG BSR
(2) :* MOV ABRS,STMDAT #6,STMDAT ;/READ DEVICE REG BSR,PUT DATA IN STMDAT.
(1) 021302 052737 000006 001354 :* BIS STMDAT
(2) :* MOV INC STMDAT ;/ PUT DATA FROM STMDAT TO DEVICE REG BSR
(1) 021320 005237 001354 :* MOV STMDAT,ABSR ;/ PUT DATA FROM STMDAT TO DEVICE REG BSR
(2) :* MOV MOV #100.,R0 ;/SET TO GENERATE 100. 1MHZ PULSES
(1) 021334 012700 177634 :*
(1) 021340 1\$: ;/GENERATE 1 1MHZ PULSE
(1) :/HAS THE COUNTER ADVANCED?
(2) :/READ DEVICE REG ASR,PUT DATA IN STMDAT.
(1) 021350 052737 004000 001354 :* MOV BIS #BIT11,STMDAT
(2) :* MOV STMDAT,AASR ;/ PUT DATA FROM STMDAT TO DEVICE REG ASR
(2) :* MOV ABCR,SBDDAT ;/READ DEVICE REG BCR,PUT DATA IN SBDDAT.
(1) 021376 005737 001126 TST
(1) 021402 001002 BNE SBDDAT
(1) 10\$;/EXIT LOOP IF SO.
(1) :/NOTE: WHEN WE DISABLED THE 1 MHZ.
(1) :/ OSC., THE DIVIDER COULD HAVE
(1) :/ HAD ANY COUNT IN IT.
(1) :/AFTER THIS LOOP, WE SHOULD BE SUNK.
(1) 021404 005200 INC R0 ;/DONE 100. 1MHZ PULSES?
(1) 021406 001354 BNE 1\$;/IF NOT - DO ANOTHER.

(1) 021410 012737 000001 001124 10\$: MOV #1,\$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.
(1) ;/READ THE COUNTER
(2) (2) ;* MOV ABCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN \$BDDAT.
(1) 021426 023737 001126 001124 CMP SBDDAT,\$GDDAT ;/DID THE COUNTER ADVANCE ONCE?
(1) 021434 001402 BEQ 2\$;/IF YES - NEXT CHECK
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 021436 104015 ERROR 15 ;/ERROR - CLOCK B - 10KHZ - PULSE
(1) ;/NOT GENERATED WHEN 10 100KHZ PULSE
(1) ;/WERE GENERATED.
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 021440 000430 BR 4\$
(1) 021442 012700 177635 2\$: MOV #-99.,R0 ;/GET THE NUMBER OF "1 MHZ" H PULSES
(1) ;/NEED TO GIVE 9 100KHZ PULSES
(1) 021446 3\$:
(2) (2) ;* MOV @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
(1) 021456 052737 004000 001354 BIS #BIT11,\$TMDAT
(2) (2) ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(1) 021474 005200 INC R0 ;/IN ORDER TO CHECK TO SEE THAT
(1) 021476 001363 BNE 3\$;/WE DON'T GENERATE ANOTHER 10KHZ PULSE
(1) (2) ;* MOV ABCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN \$BDDAT.
(1) 021510 023737 001126 001124 CMP SBDDAT,\$GDDAT ;/WAS ANOTHER 10KHZ PULSE GENERATED?
(1) 021516 001401 BEQ 4\$;/NO - GO TO NEXT CHECK.
(1) (2) ::::::::::::::> ERROR <<:::::::::::::
(1) 021520 104015 ERROR 15 ;/ERROR CLOCK B WE SEEM TO HAVE
(1) ;/GENERATED A SECOND 10KHZ PULSE
(1) ;/ON ONLY 9 100KHZ PULSES.
(2) ::::::::::::::> ERROR <<:::::::::::::
(1) 021522 4\$:
3364
(5) ;*****
(4) ;*TEST 145 *TEST CLOCK B'S 1KHZ DIVIDER
(5) ;*
(5) ;+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
(5) ;+BY 10 TO GIVE US A 100HZ CLK L PULSE.
(5) ;+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
(5) ;+PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
(5) ;+PULSES.
(5) ;+THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE

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T145 *TEST CLOCK B'S 1KHZ DIVIDER

SEQ 0145

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(5)          ;* SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
(5)
(6)          ;*
(6)          ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
(6)
(4)          ;*****
(3)          021522 000004          TST145: SCOPE
(1)
(1)          ;*****                                ;/CLEAR CLOCK B.
(1)          ;*****                                ;/CLEAR CLOCK A.
(1)
(1)          ;*****                                ;/CLEAR B'S BUFFER + COUNT REGS.
(1)          ;*****                                ;/DISABLE THE 1MHZ OSC.
(1)          ;*****                                ;/RATE: 1KHZ
(1)          ;*****                                ;/ENABLE CLOCK B.

(1)          021524 005037 001354          CLR      STMDAT
(2)          ;*      MOV      STMDAT,ABSR      ;/ PUT DATA FROM STMDAT TO DEVICE REG BSR
(2)          ;*      MOV      STMDAT,BASR      ;/ PUT DATA FROM STMDAT TO DEVICE REG ASR
(2)
(2)          021560 012737 004040 001354  ;*      MOV      STMDAT,ABBR      ;/ PUT DATA FROM STMDAT TO DEVICE REG BBR
(1)          ;*      MOV      #BIT11!BITS,STMDAT
(2)
(2)          ;*      MOV      STMDAT,ABSR      ;/ PUT DATA FROM STMDAT TO DEVICE REG BSR
(2)
(2)          021606 052737 000010 001354  ;*      MOV      ABRS,STMDAT      ;/READ DEVICE REG BSR,PUT DATA IN STMDAT.
(1)          ;*      BIS      #10,STMDAT
(2)
(2)          021624 005237 001354          ;*      MOV      STMDAT,ABSR      ;/ PUT DATA FROM STMDAT TO DEVICE REG BSR
(1)          ;*      INC      STMDAT
(2)
(2)          021640 012700 176030          ;*      MOV      STMDAT,ABSR      ;/ PUT DATA FROM STMDAT TO DEVICE REG BSR
(1)          ;*      MOV      #-1000.,R0      ;/SET TO GENERATE 1000. 1MHZ PULSES
(1)
(1)          021644          1$:          ;/GENERATE 1 1MHZ PULSE
(1)          ;/HAS THE COUNTER ADVANCED?
(2)
(2)          021654 052737 004000 001354  ;*      MOV      ABASR,STMDAT      ;/READ DEVICE REG ASR,PUT DATA IN STMDAT.
(1)          ;*      BIS      #BIT11,STMDAT
(2)
(2)          -          ;*      MOV      STMDAT,BASR      ;/ PUT DATA FROM STMDAT TO DEVICE REG ASR
(2)
(2)          021702 005737 001126          ;*      MOV      ABCR,SBDDAT      ;/READ DEVICE REG BCR,PUT DATA IN SBDDAT.
(1)          ;*      TST      SBDDAT
(1)          021706 001002          BNE      10$          ;/EXIT LOOP IF SO.
(1)
(1)          ;/NOTE: WHEN WE DISABLED THE 1 MHZ.
(1)          ;/          OSC., THE DIVIDER COULD HAVE
(1)          ;/          HAD ANY COUNT IN IT.
(1)          ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
(1)
(1)          021710 005200          INC      R0          ;/DONE 1000. 1MHZ PULSES?
(1)          021712 001354          BNE      1$          ;/IF NOT - DO ANOTHER.
(1)
(1)          021714 012737 000001 001124  10$:    MOV      #1,SGDDAT      ;/SET FOR ERROR TYPEOUT IF NEEDED.
(1)

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T145 *TEST CLOCK B'S 1KHZ DIVIDER

SEQ 0146

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(1) ;/READ THE COUNTER
(2)
(1) ;*      MOV      @BCR,$BDDAT    ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1) 021732 023737 001126 001124      CMP      $BDDAT,$GDDAT    ;/DID THE COUNTER ADVANCE ONCE?
(1) 021740 001402                   BEQ      2$          ;/IF YES - NEXT CHECK
(2)
(2) ::::::::::::::::::::> ERROR <::::::::::::::::::
(1) 021742 104015                  ERROR    15          ;/ERROR - CLOCK B - 1KHZ - PULSE
(1)                                         ;/NOT GENERATED WHEN 10 10KHZ PULSE
(1)                                         ;/WERE GENERATED.
(2)
(2) ::::::::::::::::::::> ERROR <::::::::::::::::::
(1) 021744 000430                  BR       4$          ;/REACH HERE
(1) 021746 012700 176031      2$:    MOV      #-999.,R0    ;/GET THE NUMBER OF "1 MHZ" H PULSES
(1)                                         ;/NEED TO GIVE 9 10KHZ PULSES
(1) 021752                      3$:    .          .
(2)
(2) 021762 052737 004000 001354  ;*:    MOV      @ASR,$STMDAT    ;/READ DEVICE REG ASR,PUT DATA IN $STMDAT.
(1)                                         BIS      #BIT11,$STMDAT
(2)
(2) 022000 005200                  ;*:    MOV      $STMDAT,@ASR    ;/ PUT DATA FROM $STMDAT TO DEVICE REG ASR
(1)                                         INC      R0          ;/IN ORDER TO CHECK TO SEE THAT
(1) 022002 001363                  BNE      3$          ;/WE DON'T GENERATE ANOTHER 1KHZ PULSE
(1)
(2)
(2) 022014 023737 001126 001124  ;*:    MOV      @BCR,$BDDAT    ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1)                                         CMP      $BDDAT,$GDDAT    ;/WAS ANOTHER 1KHZ PULSE GENERATED?
(1) 022022 001401                  BEQ      4$          ;/NO - GO TO NEXT CHECK.
(1)
(2)
(2) ::::::::::::::::::::> ERROR <::::::::::::::::::
(1) 022024 104015                  ERROR    15          ;/ERROR CLOCK B WE SEEM TO HAVE
(1)                                         ;/GENERATED A SECOND 1KHZ PULSE
(1)                                         ;/ON ONLY 9 10KHZ PULSES.
(2)
(2) ::::::::::::::::::::> ERROR <::::::::::::::::::
(1) 022026                      4$:
3365
(5) :*****:TEST 146      *TEST CLOCK B'S 100HZ DIVIDER
(4) :*
(5) :+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
(5) :+BY 10 TO GIVE US A 100HZ CLK L PULSE.
(5) :+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
(5) :+PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
(5) :+PULSES.
(5) :+THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
(5) :+SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
(5)
(6)

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T146 *TEST CLOCK B'S 100HZ DIVIDER

SEQ 0147

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T146 *TEST CLOCK B'S 100HZ DIVIDER

SEQ 0148

(1) 022344 042737	100000 001206	BIC #100000,\$PASS	;:DON'T ALLOW A NEG. NUMBER
(1) 022352 005327		DEC (PC)+	;:LOOP?
(1) 022354 000001		WORD 1	
(1) 022356 003022		BTG \$DOAGN	;:YES
(1) 022360 012737		MOV (PC)+,@(PC)+	;:RESTORE COUNTER
(1) 022362 000001		WORD 1	
(1) 022364 022354		\$EOOPCT	
(1) 022366 104401	022433	TYPE \$ENDMG	;:TYPE "END PASS #"
(2) 022372 013746	001206	MOV \$PASS,-(SP)	;:SAVE SPASS FOR TYPEOUT
(2) 022376 104405		TYPDS	;:GO TYPE--DECIMAL ASCII WITH SIGN
(1) 022400 104401	022430	TYPE ,SENULL	;:TYPE A NULL CHARACTER
(1) 022404 013700	000042	SGET42: MOV @#42,R0	;:GET MONITOR ADDRESS
(1) 022410 001405		BEQ \$DOAGN	;:BRANCH IF NO MONITOR
(1) 022412 000005		RESET	;:CLEAR THE WORLD
(1) 022414 004710		SENDAD: JSR PC,(R0)	;:GO TO MONITOR
(1) 022416 000240		NOP	;:SAVE ROOM
(1) 022420 000240		NOP	;:FOR
(1) 022422 000240		NOP	;:ACT11
(1) 022424		\$DOAGN:	
(1) 022424 000137		JMP @(PC)+	;:RETURN
(1) 022426 002334		SRTNAD: WORD LOOP	
(1) 022430 377	377 000	SENULL: .BYTE -1,-1,0	;:NULL CHARACTER STRING
(1) 022433 015	042412 042116	SENDMG: .ASCIZ <15><12>/END PASS #/	
(1) 022440 050040	051501 020123		
(1) 022446 000043			

3396 .SBTTL *

3397 .SBTTL * SPECIAL I/O SIGNAL TESTS

3398 .SBTTL *

3415 .SBTTL * "STP2 OUT" TO "SCHMITT TRIG 1 IN" TESTS

3433 * THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND
 3434 * PROVIDING SCOPE LOOP CAPABILITIES FOR "STP2 OUT" L
 3435 * AND "SCHMITT TRIG 1" IN.
 3436 *
 3437 * WHEN YOU LOAD AND START AT LOCATION 210, PROGRAM
 3438 * CONTROL IS TRANSFERRED HERE. "STP2 OUT" L PULSES ARE
 3439 * GENERATED BY "LO STAT A HI" H + "BD10" H (MAIN. STP2).
 3440 * PIN V ("STP2 OUT") IS WIRED TO PIN LL (SCHMITT TRIG1) FOR
 3441 * THIS TEST. "STP2 OUT" PULSES ARE RECEIVED AS "SCHMITT TRIG 1"
 3442 * PULSES WHICH SET CLOCK A'S STATUS REGISTER BIT 15.
 3443 * IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
 3444 * AND ERROR SWITCH REGISTER OPTIONS ARE USED.
 3445 * AN "*" IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE
 3446 * TEST. SW13=1 WILL INHIBIT THIS FEATURE.

3447 .*: PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT B"

3448 .*: YOU MUST WIRE PINS V AND LL OF J1 TOGETHER AND INSTALL JUMPER W3
 3449 .*: LOGIC TEST (L + S 200) SHOULD BE RUN FIRST.
 3450 .*

3451 (1)
 3452 (1)
 3453

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* "STP2 OUT" TO "SCHMITT TRIG 1 IN" TESTS

SEQ 0150

3457 022450 005037 001664 LS210: CLR .DVLS
3458 (1) 022454 005037 001104 001206 1\$: CLR \$ICNT
 (1) 022460 012737 177704 MOV #-60.,\$PASS ;/CLEAR ITERATION COUNT
 (1) ;/SET PASS COUNT.
 (1) ;/NOTE: PASS COUNT USED ONLY
 (1) ;/ TO DETECT 60 PASSES SO
 (1) ;/ IT CAN GENERATE A CRLF.
 (1) ;/ AFTER CRLF IT WILL BE ZEROED.
 (1) ;/CLEAR CLOCK A.
 (1) 022466 005037 001354 2\$: CLR \$TMDAT
 (1) 022466 005037 001354 ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
 (2) ;* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
 (2)
 (1)
3459
3460
3461
3462
3463
3464
3465
3466
3467
3468 022532 052737 002000 001354 ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
 (1) ;* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
 (1) ;/GENERATE STP2
3469
3470 022550 000240 ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
3471 022552 000240 NOP
 (1) ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
3472
3473 022564 032737 100000 001354 ;* MOV @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
 (1) BIT #BIT15,\$TMDAT ;/IS ST1 FLAG SET <BIT 15>
3474 022572 001001 BNE 3\$;/BR IF YES TO 3\$:
3475
3476 ;:\$> ERROR <<\$
3477
3478 022574 104000 ERROR ;ERROR "SCHMITT TRIG 1" IN NOT
 (1) ;RECEIVED. HAVE YOU WIRED IT RIGHT?
3479
3480 ;:\$> ERROR <<\$
3481 022576 3\$:
3482 (1) 022576 032777 020000 156334 BIT #BIT13,@ASWR ;/INHIBIT "*" TYPEOUT?
 (1) BNE 2\$;/YES - IGNORE ANY UPDATES.
 (1)
 (1) 022606 005237 001104 INC \$ICNT ;/UPDATE COUNT.
 (1) 022612 001325 BNE 2\$;/IF NOT DONE 65,324 TIMES,
 (1) ;/DO IT AGAIN.
 (2) 022614 104401 022622 TYPE ,65\$;/TYPE ASCIZ STRING

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* "STP2 OUT" TO "SCHMITT TRIG 1 IN" TESTS

SEQ 0151

(2) 022620 000401 :;65\$: BR 64\$::GET OVER THE ASCIZ
(2) 022624 64\$: .ASCIZ #*#
(1)
(1) 022624 005237 001206 INC SPASS :/DONE 60 PASSES?
(1) 022630 100716 BMI 2\$:/NO - NO NEED FOR CR,LF.
(2) 022632 104401 022640 TYPE ,67\$:/TYPE ASCIZ STRING
(2) 022636 000402 BR 66\$::GET OVER THE ASCIZ
(2) 66\$: .ASCIZ <15><12>##
(2) 022644 000703 BR 1\$
(1)
3483
3484 .SBTTL :: "STP1 OUT" TO "SCHMITT TRIG 2" H TESTS
3485 *
3486 * THIS IS A SPECIAL TEST SECTION DEVOTED FOR TESTING AND
3487 * PROVIDING SCOPE LOOP CAPABILITIES FOR "STP1 OUT" AND
3488 * "SCHMITT TRIG2" IN.
3489 *
3490 * WHEN YOU LOAD AND START AT LOCATION 214, PROGRAM
3491 * CONTROL IS TRANSFERRED HERE. "STP1 OUT" L PULSES ARE
3492 * GENERATED BY "LD STAT A HI" + "BD12" H (MAIN ST1).
3493 * PIN DD ("STP1 OUT") IS WIRED TO PIN BB ("SCHMITT
3494 * TRIG 2") FOR THIS TEST. "STP1 OUT" PULSES ARE RECEIVED AS
3495 * "SCHMITT TRIG 2" PULSES WHICH WILL CLEAR CLOCK A'S
3496 * COUNT REGISTER IF MODE 3 IS SELECTED.
3497 * IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
3498 * AND ERROR SWITCH REGISTER OPTIONS ARE USED.
3499 * AN "*" IS TYPED AFTER EACH 65,324 LOOPS THROUGH
3500 * THE TEST. SW13=1 WILL INHIBIT THIS FEATURE.
3501 *
3502 *
3503 (1) :: PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT B"
3504 (1) *
3505 * YOU MUST WIRE PINS DD AND BB OF J1 TOGETHER AND INSTALL JUMPER W4.
3506 *
3507 *
3508 022646 005037 001664 LS214: CLR .DVLS
3509 (1) 022652 005037 001104 1\$: CLR \$ICNT :/CLEAR ITERATION COUNT
3510 (1) 022656 012737 177704 001206 MOV #-60.,\$PASS :/SET PASS COUNT.
* /NOTE: PASS COUNT USED ONLY
* / TO DETECT 60 PASSES SO
* / IT CAN GENERATE A CRLF.
* / AFTER CRLF IT WILL BE ZEROED.
* /CLEAR CLOCK A.
* /CLEAR CLOCK B.
(1) 022664 005037 001354 2\$: CLR \$TMDAT
(2) * MOV \$TMDAT,@ASR :/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(2) * MOV \$TMDAT,@BSR :/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
(1) 3510 * LOAD ALL ONES TO CLK A'S BUFFER + COUNT REG.

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;* "STP1 OUT" TO "SCHMITT TRIG 2" H TESTS

SEQ 0152

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3511
3512
3513
3514
3515
3516
3517
3518
3519 022710 012737 177777 001354      MOV    #-1,$TMDAT
3520
3521 (1) 022726 012737 001400 001354      ;*    MOV    $TMDAT,@ABR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
3522      MOV    #BIT8!BIT9,$TMDAT
3523 (1)
3524 (1) 022754 052737 010000 001354      ;*    MOV    $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
3525      BIS    @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
3526 (1)
3527 (1) 023002 005737 001126      ;*    MOV    $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
3528      TST    @ACR,$BDDAT      ;/WAS THE COUNT REGISTER CLEARED?
3529
3530 023006 001401      BEQ    3$      ;IF YES BR 3$.
3531
3532 023010 104000      ERROR      ;ERROR "SCHMITT TRIG 2" IN NOT
3533
3534
3535 023012      3$:          ;INHIBIT "*" TYPEOUT?
3536 (1) 023012 032777 020000 156120      BIT    #BIT13,@SWR      ;/YES - IGNORE ANY UPDATES.
(1) 023020 001321      BNE    2$          ;/UPDATE COUNT.
(1) 023022 005237 001104      INC    $ICNT      ;/IF NOT DCNE 65,324 TIMES,
(1) 023026 001316      BNE    2$          ;/DO IT AGAIN.
(1)
(2) 023030 104401 023036      TYPE   ,65$      ;TYPE ASCIZ STRING
(2) 023034 000401      BR    64$      ;GET OVER THE ASCIZ
(2) 023040      64$:      .ASCIZ  #*#      ;
(1)
(1) 023040 005237 001206      INC    $PASS      ;DONE 60 PASSES?
(1) 023044 100707      BMI    2$      ;/NO - NO NEED FOR CR,LF.
(2) 023046 104401 023054      TYPE   ,67$      ;TYPE ASCIZ STRING
(2) 023052 000402      BR    66$      ;GET OVER THE ASCIZ
(2)
(2) 023060      66$:      .ASCIZ <15><12>##      ;
(1) 023060 000674      BR    1$          ;

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* "SCHMITT TRIG 3" IN, "ST3 OUT" TESTS

SEQ 0153

3538 .SBTTL * "SCHMITT TRIG 3" IN, "ST3 OUT" TESTS
3539
3540 :* THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND
3541 :* PROVIDING SCOPE LOOP CAPABILITIES FOR 'SCHMITT TRIG 3'
3542 :* AND "ST3 OUT".
3543 :*
3544 :* WHEN YOU LOAD AND START AT LOCATION 220, PROGRAM
3545 :* CONTROL IS TRANSFERRED HERE. "STP1" PULSES ARE GENERATED
3546 :* BY "LD STAT A H," + "BD12" H (MAIN STP1). PIN DD ('STP1 OUT')
3547 :* IS WIRED TO PIN T ('SCHMITT TRIG 3'), 'SCHMITT TRIG 3' PULSES
3548 :* GIVE US "ST3 OUT" PULSES. PIN L ('ST3 OUT') IS WIRED
3549 :* TO PIN BB ('SCHMITT TRIG2'), AND "SCHMITT TRIG 2" WILL SET
3550 :* CLOCK A'S STATUS REGISTER BIT 7.
3551 :* IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
3552 :* AND ERROR SWITCH REGISTER OPTIONS ARE USED.
3553 :* AN "*" IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE
3554 :* TEST. SW13=1 WILL INHIBIT THIS FEATURE.
3555 :*
3556 :* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT B"
(1)
(1)
3557 :* YOU MUST WIRE PINS DD TO T OF J1 TOGETHER, AS WELL AS
3558 :* PINS L TO BB OF J1 TOGETHER AND INSTALL JUMPERS W4 AND W5.
3559 :*
3560 :* TESTS LS210 AND LS214 SHOULD BE RUN FIRST.
3561 :*
3562
3563 023062 005037 001664 LS220: CLR DVLS
3564
(1) 023066 005037 001104 1\$: CLR \$ICNT /CLEAR ITERATION COUNT
(1) 023072 012737 177704 001206 MOV #60.,\$PASS /SET PASS COUNT.
:NOTE: PASS COUNT USED ONLY
:/ TO DETECT 60 PASSES SO
:/ IT CAN GENERATE A CRLF.
:/ AFTER CRLF IT WILL BE ZEROED.
:/ CLEAR CLOCK A.
:/ CLEAR CLOCK B.
(1) 023100 005037 001354 2\$: CLR \$TMDAT
(1) 023100 005037 001354 ;* MOV \$TMDAT,\$ASR / PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(2) ;* MOV \$TMDAT,\$BSR / PUT DATA FROM \$TMDAT TO DEVICE REG BSR
(2)
(1)
3565 023124 005037 001354 CLR \$TMDAT :GENERATE A "STP2 OUT" PULSE.
3566
3567
(1) 023140 052737 011000 001354 ;* MOV \$ASR,\$TMDAT /READ DEVICE REG ASR,PUT DATA IN \$TMDAT.
3568 BIS #BIT12!BIT9,\$TMDAT
3569 ;* MOV \$TMDAT,\$ASR / PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(1) :AT THIS POINT YOU SHOULD SEE AN
3570 :OUTPUT AT PIN DD. PIN DD SHOULD BE
3571 :WIRED TO PIN T TO GIVE "SCHMITT TRIG3"
3572 :INPUT WHICH IN TURN SHOULD GIVE
3573 :AN OUTPUT AT PIN L ("ST3"). PIN
3574 :L BEING WIRED TO PIN BB ("SCHMITT
3575

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3576                                ;TRIG2 IN") SHOULD GIVE "ST2" WHICH
3577                                ;SETS CLOCK A'S CSR BIT 7.
3578
3579                                ;DID BIT 7 SET?
3580
3581 023166 105737 001126      :*    MOV    @ASR,$BDDAT   ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
3582 023172 100401      TSTB   $BDDAT
3583                                BMI    3$          ;IF YES, BR TO 3$.

:::$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$

3584 023174 104000      ERROR      ;ERROR "SCHMITT TRIG 2" NOT RECEIVED
3585                                ;
3586                                ;HAVE YOU WIRED IT RIGHT?

:::$$$$$$$$$$$$$$$$$$$$$$> ERROR <<$$$$$$$$$$$$$$$$$$$$$$

3587 023176      3$:          3$:
3588
3589
3590
3591
3592
3593
3594
3595
3596
3597
3598
3599
3600
3601
3602
3603
3604
3605
(1) 023176 032777 020000 155734      BIT    #BIT13,ASWR   ;/INHIBIT "*" TYPEOUT?
(1) 023204 001335      BNE    2$          ;/YES - IGNORE ANY UPDATES.
(1)
(1) 023206 005237 001104      INC    $ICNT     ;/UPDATE COUNT.
(1) 023212 001332      BNE    2$          ;/IF NOT DONE 65,324 TIMES,
(1)
(1)
(2) 023214 104401 023222      TYPE   ,65$        ;:TYPE ASCIZ STRING
(2) 023220 000401      BR    64$        ;:GET OVER THE ASCIZ
(2) 023224      .ASCIZ  #*#
(1)
(1) 023224 005237 001206      INC    $PASS     ;/DONE 60 PASSES?
(1) 023230 100723      BMI    2$          ;/NO - NO NEED FOR CR,LF.
(2) 023232 104401 023240      TYPE   ,67$        ;:TYPE ASCIZ STRING
(2) 023236 000402      BR    66$        ;:GET OVER THE ASCIZ
(2) 023244      .ASCIZ  <15><12>##
(1) 023244 000710      BR    1$          ;*
(1)

.SBTTL *      "A EVENT OUT" TEST
*: THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND
*: PROVIDING SCOPE LOOP CAPABILITIES FOR "A EVENT OUT".
*:
*: WHEN YOU LOAD AND START AT LOCATION 224, PROGRAM
*: CONTROL IS TRANSFERRED HERE. "A EVENT OUT" PULSES ARE
*: GENERATED BY CLOCK A OVERFLOWS. PIN VV
*: ("A EVENT OUT") IS WIRED TO PIN BB ("SCHMITT TRIG 2")
*: "SCHMITT TRIG 2" PULSES WILL SET CLOCK A'S CSR BIT 7.
*: IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING
*: AND ERROR SWITCH REGISTER OPTIONS ARE USED.
*: AN "*" IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE TEST.
*: SW13=1 WILL INHIBIT THIS FEATURE.
*:
*: PROBABLE SYNC POINT FOR THIS TEST::: "LD STAT B"

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* "A EVENT OUT" TEST

SEQ 0155

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(1) 3606      ;*YOU MUST WIRE PINS VV AND BB OF J1 TOGETHER AND INSTALL JUMPER W4
3607
3608
3609
3610
3611 023246 005037 001664      LS224: CLR    .DVLS
3612      (1) 023252 005037 001104      1$: CLR    $ICNT
3613      (1) 023256 012737 177704 001206      MOV    #-60.,$PASS      ;/CLEAR ITERATION COUNT
3614      ;*          ;/SET PASS COUNT.
3615      ;*          ;/NOTE: PASS COUNT USED ONLY
3616      ;*          ;/TO DETECT 60 PASSES SO
3617      ;*          ;/IT CAN GENERATE A CRLF.
3618      ;*          ;/AFTER CRLF IT WILL BE ZEROED.
3619      ;*          ;/CLEAR CLOCK A.
3620      ;*          ;/CLEAR CLOCK B.
3621      (1) 023264 005037 001354      2$: CLR    $TMDAT
3622      ;*          ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
3623      ;*          ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
3624      ;*          ;/PRELOAD CLOCK A'S BUFFER + COUNT REGS.
3625      (1) 023310 012737 177777 001354      MOV    #-1,$TMDAT
3626      ;*          ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
3627      ;*          ;/RATE: 1MHZ, ENABLE COUNTER
3628      (1) 023326 012737 001003 001354      MOV    #1003,$TMDAT
3629      ;*          ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
3630      ;*          ;HAS AN OVERFLOW OCCURRED?
3631      ;*          ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
3632      (1) 023354 032737 000040 001354      MOV    $ASR,$TMDAT
3633      023362 001770      ;*: BIT    #BIT05,$TMDAT      ;NO - THEN WAIT FOR IT.
3634      ;*          ;OVERFLOW SHOULD GO OUT AS
3635      ;*          ;"A EVENT OUT". YOU SHOULD SEE
3636      ;*          ;AN OUTPUT AT PIN VV.
3637      ;*          ;THIS IN TURN IS BROUGHT
3638      ;*          ;IN AS "SCHMITT TRIG 2" IN TO
3639      ;*          ;SET CLOCK A'S CSR BIT 7.
3640      ;*          ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
3641      (1) 023374 105737 001126      ;*: MOV    $ASR,$BDDAT
3642      023400 100401      TSTB   $BDDAT
3643      ;*          ;DID BIT 7 SET
3644      ;*          ;BMI    4$      ;BR IF YES TO 4$
3645      ;*          ;:::SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
3646      023402 104000      ERROR
3647      ;*          ;ERROR "A EVENT OUT" PULSE
3648      ;*          ;NOT DETECTED. HAVE YOU
3649      ;*          ;WIRED IT RIGHT?
3650      ;*          ;:::SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS

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* 'B EVENT OUT' TEST B 13

SEQ 0157

(1) 023472 005037 001354 2\$: CLR \$TMDAT ;/CLEAR CLOCK B.
(1) 023472 005037 001354 ;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(2) ;* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
(2) ;* MOV #1,\$TMDAT ;PRELOAD CLOCK B'S BUFFER + COUNT REGS.
(1) 3666 023516 012737 177777 001354
(1) 3667 023534 012737 001000 001354 ;* MOV \$TMDAT,@BBR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BBR
(1) 3669 023534 012737 001000 001354 ;* MOV #1000,\$TMDAT
(1) 3670 023552 012737 000003 001354 ;* MOV #3,\$TMDAT ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
(1) 3671 023570 3\$: MOV \$TMDAT,@BSR ;/ RATE: 1MHZ, ENABLE COUNTER
(1) 3672 ;HAS AN OVERFLOW OCCURRED?
(1) 3673 023552 012737 000003 001354 ;* MOV #3,\$TMDAT ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
(1) 3676 023570 ;* MOV \$TMDAT,@BSR ;/ READ DEVICE REG BSR,PUT DATA IN \$TMDAT.
(1) 3677 023600 032737 000200 001354 ;* MOV @ASR,\$TMDAT ;NO -THEN WAIT FOR IT.
(1) 3678 023606 001770 ;* BIT #BIT07,\$TMDAT ;OVERFLOW SHOULD GO OUT AS
(1) 3679 ;BEQ 3\$;'B EVENT OUT'. YOU SHOULD SEE
(1) 3680 ;AN OUTPUT AT PIN TT.
(1) 3681 ;THIS IN TURN IS BROUGHT
(1) 3682 ;IN AS "SCHMITT TRIG 2" IN TO
(1) 3683 ;SET CLOCK A'S CSR BIT 7.
(1) 3684
(1) 3685
(1) 3686
(1) 3687 ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
(1) 3688 023620 105737 001126 ;* TSTB \$BDDAT ;DID BIT 7 SET
(1) 3689 023624 100401 ;* BMI 4\$;BR IF YES TO 4\$
(1) 3690 ;:::SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
(1) 3691 023626 104000 ;* ERROR ;ERROR 'B EVENT OUT' PULSE
(1) 3692 ;NOT DETECTED. HAVE YOU
(1) 3693 ;WIRED IT RIGHT?
(1) 3694 ;:::SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
(1) 3695 023630 4\$:
(1) 3696 023630 032777 020000 155302 ;* BIT #BIT13,@SWR ;/INHIBIT "*" TYPEOUT?
(1) 023636 001315 ;* BNE 2\$;/YES - IGNORE ANY UPDATES.
(1) 023640 005237 001104 ;* INC \$ICNT ;/UPDATE COUNT.
(1) 023644 001312 ;* BNE 2\$;/IF NOT DONE 65,324 TIMES.
(1) 023646 104401 023654 ;* TYPE ,65\$;/DO IT AGAIN.
(2) ;TYPE ASCIZ STRING

LP
CR

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* 'B EVENT OUT' TEST 09:38 PAGE 3-137

SEQ 0158

LP
CR

(2) 023652 000401
(2) 023656
(1) 023656 005237 001206
(1) 023662 100703
(2) 023664 104401 023672
(2) 023670 000402
(2) 023676
(1) 023676 000670

64\$: BR 64\$;;GET OVER THE ASCIZ
64\$: .ASCIZ #*#
INC SPASS ;/DONE 60 PASSES?
BMI 2\$;/NO - NO NEED FOR CR,LF.
TYPE ,67\$;;TYPE ASCIZ STRING
BR 66\$;;GET OVER THE ASCIZ
67\$: .ASCIZ <15><12>##
66\$: BR 1\$

3697
3698 :*ROUTINE TO HANDLE TRAPS TO LOC 4, 10 AND .
3699 :*INTERRUPTS TO WRONG VECTORS.
3700 :*.+2, IOTT(TRAPS) WERE PUT IN LOCATIONS 4-1000
3701
3702
3703 023700
3704 023700 011637 024050 IOTRD:
3705 023704 162737 000004 024050 MOV (R6),2\$;GET WHERE WE TRAPPED TO.
3706 023712 104401 023720 SUB #4,2\$;=WHERE R6 RETURN 10-4
3707 (1) 023716 000412 TYPE ,65\$;;TYPE ASCIZ STRING
3708 (1) 023744 013746 024050 BR 64\$;;GET OVER THE ASCIZ
3709 (1) 023750 104402 .ASCIZ <15><12>#ILLEGAL TRAP TO: #
3710 (1) 023752 104401 023760
3711 (1) 023756 000407
3712 (1) 023776 062706 000004
3713 023776 000004 ADD #4,R6 ;POINT TO WHERE WE TRAPPED FROM.
3714 024002 011637 024052
3715 024006 162737 000002 024052 MOV (R6),3\$;PICK UP LOC
3716 024014 013746 024052 SUB #2,3\$;FROM REAL ADDR.
3717 (1) 024020 104402 MOV 3\$,-(SP) ;;SAVE 3\$ FOR TYPEOUT
3718 024022 023727 024050 000004 CMP 2\$,#4 ;DID WE TRAP TO LOC 4?
3719 024030 001405 BEQ 1\$;IF SO - DON'T RETURN!
3720 024032 023727 024050 000010 CMP 2\$,#10 ;DID WE TRAP TO LOC. 10?
3721 024040 001401 BEQ 1\$;ID SO - DON'T RETURN!
3722 024042 000002 RTI ;TRY RETURNING.
3723
3724 ;:\$> ERROR <<\$

3725 024044 000000 1\$: HALT ;WE STOPPED HERE BECAUSE WE TRAPPED
3726 024046 000776 BR 1\$;TO LOC 4 OR LOC 10. THIS IS A
3727 ;FATAL CONDITION THAT WE CAN NOT
3728 ;RECOVER FROM.
3729
3730

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* 'B EVENT OUT' TEST

SEQ 0159

.....>> ERROR <<.....

```

(1) 024172 010503
(1) 024174 006103
(1) 024176 105337 024300
(1) 024202 100016
(1) 024204 042703 177770
(1) 024210 001002
(1) 024212 005704
(1) 024214 001403
(1) 024216 005204
(1) 024220 052703 000060
(1) 024224 052703 000040
(1) 024230 110337 024274
(1) 024234 104401 024274
(1) 024240 105337 024276
(1) 024244 003347
(1) 024246 002402
(1) 024250 005204
(1) 024252 000744
(1) 024254 012605
(1) 024256 012604
(1) 024260 012603
(1) 024262 016666 000002 000004
(1) 024270 012616
(1) 024272 000002
(1) 024274 000
(1) 024275 000
(1) 024276 000
(1) 024277 000
(1) 024300 000000

3$:      MOV    R5,R3          ;:GET LSB OF THIS DIGIT
         ROL    R3
         DECB   $0MODE
         BPL    7$          ;:TYPE THIS DIGIT?
         BIC    #177770,R3
         BNE    4$          ;:BR IF NO
         TST    R4
         BEQ    5$          ;:GET RID OF JUNK
         BNE    4$          ;:TEST FOR 0
         TST    R4
         BEQ    5$          ;:SUPPRESS THIS 0?
         BNE    4$          ;:BR IF YES
         INC    R4
         INC    R4          ;:DON'T SUPPRESS ANYMORE 0'S
         BIS    #'0,R3
         BIS    #'R3          ;:MAKE THIS DIGIT ASCII
         MOVB   R3,8$          ;:MAKE ASCII IF NOT ALREADY
         TYPE   ,8$          ;:SAVE FOR TYPING
         DEC B   $0CNT
         BGT    2$          ;:GO TYPE THIS DIGIT
         INC    R4          ;:COUNT BY 1
         BLT    6$          ;:BR IF MORE TO DO
         INC    R4
         BR     2$          ;:BR IF DONE
         INC    R4          ;:INSURE LAST DIGIT ISN'T A BLANK
         BR     2$          ;:GO DO THE LAST DIGIT
         MOV    (SP)+,R5
         MOV    (SP)+,R4
         MOV    (SP)+,R3
         MOV    2(SP),4(SP)    ;:RESTORE R5
         MOV    (SP)+,(SP)    ;:RESTORE R4
         MOV    (SP)+,(SP)    ;:RESTORE R3
         RTI
         .BYTE  0          ;:SET THE STACK FOR RETURNING
         .BYTE  0
         .BYTE  0
         SOCNT: .BYTE  0
         SOFILL: .BYTE  0
         SOMODE: .WORD 0
         .SBttl  ERROR HANDLER ROUTINE
         .*****  

         ;:THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT,  

         ;:SAVE THE ERROR ITEM NUMBER AND THE ADDRESS OF THE ERROR CALL  

         ;:AND GO TO SERRTYP ON ERROR  

         ;:THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:  

         ;:SW15=1 HALT ON ERROR  

         ;:SW13=1 INHIBIT ERROR TIMEOUTS  

         ;:SW10=1 BELL ON ERROR  

         ;:SW09=1 LOOP ON ERROR  

         ;:CALL  

         ;:    ERROR N      ;:ERROR=EMT AND N=ERROR ITEM NUMBER
         .SBttl  SERROR:
         CKSWR
         7$:      INC B   SERFLG
         BEQ    7$          ;:TEST FOR CHANGE IN SOFT-SWR
         SERFLG
         BEQ    7$          ;:SET THE ERROR FLAG
         DON'T LET THE FLAG GO TO ZERO
         STSTNM,DISPLAY
         BIT    #BIT10,ASWR
         BEQ    1$          ;:DISPLAY TEST NUMBER AND ERROR FLAG
         BIT    #BIT10,ASWR
         BEQ    1$          ;:BELL ON ERROR?
         TYPE   ,$BELL
         INC    $ERTTL
         MOV    (SP),SERRPC
         SUB    #2,SERRPC
         MOV    ASERRPC,$ITEMB
         BIT    #BIT13,ASWR
         .SBttl  ;:RING BELL
         .SBttl  ;:COUNT THE NUMBER OF ERRORS
         .SBttl  ;:GET ADDRESS OF ERROR INSTRUCTION
         .SBttl  ;:STRIP AND SAVE THE ERROR ITEM CODE
         .SBttl  ;:SKIP TIMEOUT IF SET

```

3738

```

(1) 024302 104407
(1) 024302 105237 001103
(1) 024310 001775
(1) 024312 013777 001102 154622
(1) 024320 032777 002000 154612
(1) 024326 001402
(1) 024330 104401 001170
(1) 024334 005237 001112
(1) 024340 011637 001116
(1) 024344 162737 000002 001116
(1) 024352 117737 154540 001114
(1) 024360 032777 020000 154552

7$:      CKSWR
         INC B   SERFLG
         BEQ    7$          ;:TEST FOR CHANGE IN SOFT-SWR
         SERFLG
         BEQ    7$          ;:SET THE ERROR FLAG
         DON'T LET THE FLAG GO TO ZERO
         STSTNM,DISPLAY
         BIT    #BIT10,ASWR
         BEQ    1$          ;:DISPLAY TEST NUMBER AND ERROR FLAG
         BIT    #BIT10,ASWR
         BEQ    1$          ;:BELL ON ERROR?
         TYPE   ,$BELL
         INC    $ERTTL
         MOV    (SP),SERRPC
         SUB    #2,SERRPC
         MOV    ASERRPC,$ITEMB
         BIT    #BIT13,ASWR
         .SBttl  ;:RING BELL
         .SBttl  ;:COUNT THE NUMBER OF ERRORS
         .SBttl  ;:GET ADDRESS OF ERROR INSTRUCTION
         .SBttl  ;:STRIP AND SAVE THE ERROR ITEM CODE
         .SBttl  ;:SKIP TIMEOUT IF SET

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15
ERROR HANDLER ROUTINE

SEQ 0161


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(1) 024736 103003
(1) 024740 116663 000001 177777
(1) 024746 052702 000060
(1) 024752 052702 000040
(1) 024756 110223
(1) 024760 005720
(1) 024762 020027 000010
(1) 024766 002746
(1) 024770 003002
(1) 024772 010502
(1) 024774 000764
(1) 024776 105726
(1) 025000 100003
(1) 025002 116663 177777 177776
(1) 025010 105013
(3) 025012 012605
(3) 025014 012603
(3) 025016 012602
(3) 025020 012601
(3) 025022 012600
(1) 025024 104401 025052
(1) 025030 016666 000002 000004
(1) 025036 012616
(1) 025040 000002
(1) 025042 023420
(1) 025044 001750
(1) 025046 000144
(1) 025050 000012
(1) 025052 000004
3741
      BCC   6$          ;:BR IF NO
      MOVB  1(SP),-1(R3)  ;:YES--SET THE SIGN
      BIS   #'0,R2          ;:MAKE THE BCD DIGIT ASCII
      BIS   #' ,R2          ;:MAKE IT A SPACE IF NOT ALREADY A DIGIT
      MOVB  R2,(R3)+        ;:PUT THIS CHARACTER IN THE OUTPUT BUFFER
      TST   (R0)+          ;:JUST INCREMENTING
      CMP   R0,#10          ;:CHECK THE TABLE INDEX
      BLT   2$              ;:GO DO THE NEXT DIGIT
      BGT   8$              ;:GO TO EXIT
      MOV   R5,R2          ;:GET THE LSD
      BR    6$              ;:GO CHANGE TO ASCII
      TSTB  (SP)+          ;:WAS THE LSD THE FIRST NON-ZERO?
      BPL   9$              ;:BR IF NO
      MOVB  -1(SP),-2(R3)  ;:YES--SET THE SIGN FOR TYPING
      CLR B (R3)            ;:SET THE TERMINATOR
      MOV   (SP)+,R5          ;:POP STACK INTO R5
      MOV   (SP)+,R3          ;:POP STACK INTO R3
      MOV   (SP)+,R2          ;:POP STACK INTO R2
      MOV   (SP)+,R1          ;:POP STACK INTO R1
      MOV   (SP)+,R0          ;:POP STACK INTO R0
      TYPE  $DBLK            ;:NOW TYPE THE NUMBER
      MOV   2(SP),4(SP)       ;:ADJUST THE STACK
      MOV   (SP)+,(SP)
      RTI
      SDTBL: 10000.
      1000.
      100.
      10.
      SDBLK: .BLKW 4
      .SBttl  SCOPE HANDLER ROUTINE
      ****
      /*THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
      AND LOAD THE TEST NUMBER($TSTNM) INTO THE DISPLAY REG.(DISPLAY<7:0>)
      AND LOAD THE ERROR FLAG ($ERFLG) INTO DISPLAY<15:08>
      THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
      SW14=1    LOOP ON TEST
      SW09=1    LOOP ON ERROR
      SW08=1    LOOP ON TEST IN SWR<7:0>
      CALL
      */
      SCOPE           ;:SCOPE=IOT
      $SCOPE:
      CKSWR          ;:TEST FOR CHANGE IN SOFT-SWR
      1$:  BIT #BIT14,@SWR  ;:LOOP ON PRESENT TEST?
      BNE  $OVER        ;:YES IF SW14=1
      /*START OF CODE FOR THE XOR TESTER*/
      $XTSTR: BR 6$      ;:IF RUNNING ON THE "XOR" TESTER CHANGE
      MOV   @#ERRVEC,-(SP) ;:THIS INSTRUCTION TO A "NOP" (NOP=240)
      MOV   #5$,@#ERRVEC  ;:SAVE THE CONTENTS OF THE ERROR VECTOR
      TST   @#177060        ;:SET FOR TIMEOUT
      MOV   (SP)+,@#ERRVEC  ;:TIME OUT ON XOR?
      BR    $SVLAD         ;:RESTORE THE ERROR VECTOR
      CMP   (SP)+,(SP)+     ;:GO TO THE NEXT TEST
      MOV   (SP)+,@#ERRVEC  ;:CLEAR THE STACK AFTER A TIME OUT
      MOV   (SP)+,@#ERRVEC  ;:RESTORE THE ERROR VECTOR

```

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(1) 025130 000417          BR    7$      ::LOOP ON THE PRESENT TEST
(1) 025132 000400 154000   6$:;#####END OF CODE FOR THE XOR TESTER#####
(1) 025132 032777          BIT   #BIT08,@ASWR   ::LOOP ON SPEC. TEST?
(1) 025140 001404          BEQ   2$      ::BR IF NO
(1) 025142 127737 153772  001102          CMPB  @ASWR,$TSTNM  ::ON THE RIGHT TEST? SWR<7:0>
(1) 025150 001433          BEQ   $OVER   ::BR IF YES
(1) 025152 105737 001103          2$:   TSTB   SERFLG   ::HAS AN ERROR OCCURRED?
(1) 025156 001412          BEQ   $SVLAD   ::BR IF NO
(1) 025160 032777 001000 153752          BIT   #BIT09,@ASWR   ::LOOP ON ERROR?
(1) 025166 001404          BEQ   4$      ::BR IF NO
(1) 025170 013737 001110 001106          7$:   MOV    SLPERR,$LPADR  ::SET LOOP ADDRESS TO LAST SCOPE
(1) 025176 000420          BR    $OVER   ::ZERO THE ERROR FLAG
(1) 025200 105037 001103          4$:   CLR   SERFLG   ::COUNT TEST NUMBERS
(1) 025204 105237 001102          $SVLAD: INCB  STSTNM  ::SET TEST NUMBER IN APT MAILBOX
(1) 025210 113737 001102 001204          MOVB  STSTNM,$TESTN  ::SAVE SCOPE LOOP ADDRESS
(1) 025216 011637 001106          MOV    (SP),$LPADR  ::SAVE ERROR LOOP ADDRESS
(1) 025222 011637 001110          MOV    (SP),$LPERR  ::CLEAR THE ESCAPE FROM ERROR ADDRESS
(1) 025226 005037 001166          CLR    $ESCAPE   ::ONLY ALLOW ONE(1) ERROR ON NEXT TEST
(1) 025232 112737 000001 001115          MOVB  #1,SERMAX  ::DISPLAY TEST NUMBER
(1) 025240 013777 001102 153674          $OVER: MOV    STSTNM,@DISPLAY  ::FUDGE RETURN ADDRESS
(1) 025246 013716 001106          MOV    SLPADR,(SP)  ::FIXES PS
(1) 025252 000002          RTI    .SBTTL READ AN OCTAL NUMBER FROM THE TTY
3742

```

```

(1)
(2) :*****THIS ROUTINE WILL READ AN OCTAL (ASCII) NUMBER FROM THE TTY AND
(1) :*CHANGE IT TO BINARY.
(1) :*CALL:
(1) :*    RDOCT
(1) :*    RETURN HERE          ::READ AN OCTAL NUMBER
(1) :*                          ::LOW ORDER BITS ARE ON TOP OF THE STACK
(1) :*                          ::HIGH ORDER BITS ARE IN $HIOCT
(1)
(1) 025254 011646          $RDOCT: MOV    (SP),-(SP)  ::PROVIDE SPACE FOR THE
(1) 025256 016666 000004 000002          MOV    4(SP),2(SP)  ::INPUT NUMBER
(3) 025264 010046          MOV    R0,-(SP)   ::PUSH R0 ON STACK
(3) 025266 010146          MOV    R1,-(SP)   ::PUSH R1 ON STACK
(3) 025270 010246          MOV    R2,-(SP)   ::PUSH R2 ON STACK
(1) 025272 104411          1$:   RDLIN   ::READ AN ASCIZ LINE
(1) 025274 012600          MOV    (SP)+,R0  ::GET ADDRESS OF 1ST CHARACTER
(1) 025276 005001          CLR    R1      ::CLEAR DATA WORD
(1) 025300 005002          CLR    R2      ::PICKUP THIS CHARACTER
(1) 025302 112046          2$:   MOVB   (R0)+,-(SP)  ::IF ZERO GET OUT
(1) 025304 001412          BEQ   3$      ::*2
(1) 025306 006301          ASL    R1      ::*4
(1) 025310 006102          ROL    R2      ::*8
(1) 025312 006301          ASL    R1      ::STRIP THE ASCII JUNK
(1) 025314 006102          ROL    R2      ::ADD IN THIS DIGIT
(1) 025316 006301          ASL    R1      ::LOOP
(1) 025320 006102          ROL    R2      ::CLEAN TERMINATOR FROM STACK
(1) 025322 042716 177770          BIC    #^C7,(SP)  ::SAVE THE RESULT
(1) 025326 062601          ADD    (SP)+,R1
(1) 025330 000764          BR    2$      ::POP STACK INTO R2
(1) 025332 005726          3$:   TST    (SP)+
(1) 025334 010166 000012          MOV    R1,12(SP)
(1) 025340 010237 025354          MOV    R2,$HIOCT
(3) 025344 012602          MOV    (SP)+,R2

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READ AN OCTAL NUMBER FROM THE TTY

SEQ 0165

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(1) 025550 012777 000100 153366      MOV    #100,ASTKS   ;RE-ENABLE TTY KBD INTERRUPTS
(1) 025556 000002                   15$: RTI     ;RETURN
(1) 025560 004737 026344           16$: JSR    PC,$TYPEC ;ECHO CHAR
(1) 025564 021627 000060           CMP    (SP),#60  ;CHAR < 0?
(1) 025570 002420                   BLT    18$    ;BRANCH IF YES
(1) 025572 021627 000067           CMP    (SP),#67  ;CHAR > ??
(1) 025576 003015                   BGT    18$    ;BRANCH IF YES
(1) 025600 042726 000060           BIC    #60,(SP)+ ;STRIP-OFF ASCII
(1) 025604 005766 000002           TST    2(SP)  ;IS THIS THE FIRST CHAR
(1) 025610 001403                   BEQ    17$    ;BRANCH IF YES
(1) 025612 006316                   ASL    (SP)   ;NO, SHIFT PRESENT
(1) 025614 006316                   ASL    (SP)   ;CHAR OVER TO MAKE
(1) 025616 006316                   ASL    (SP)   ;ROOM FOR NEW ONE.
(1) 025620 005266 000002           INC    2(SP)  ;KEEP COUNT OF CHAR
(1) 025624 056616 177776           BIS    -2(SP),(SP) ;SET IN NEW CHAR
(1) 025630 000707                   BR     7$    ;GET THE NEXT ONE
(1) 025632 104401 001174           TYPE   ,SQUES ;TYPE ?<CR><LF>
(1) 025636 000720                   BR     20$    ;SIMULATE CONTROL-U
(1) .DSABL LSB

(1)
(1)
(2) ****
(1) /*THIS ROUTINE WILL INPUT A SINGLE CHARACTER FROM THE TTY
(1) :*CALL:
(1) :* RDCHR
(1) :* RETURN HERE
(1) :*: RDCHR: MOV    (SP),-(SP)   ;INPUT A SINGLE CHARACTER FROM THE TTY
(1) :*:          MOV    4(SP),2(SP) ;CHARACTER IS ON THE STACK
(1) :*:          TSTB  ASTKS        ;WITH PARITY BIT STRIPPED OFF
(1) :*:          BPL   1$          ;
(1) :*:          MOVB  ASTKB,4(SP) ;
(1) :*:          BIC   #^C<177>,4(SP) ;GET RID OF JUNK IF ANY
(1) :*:          CMP   4(SP),#23  ;IS IT A CONTROL-S?
(1) :*:          BNE   3$          ;BRANCH IF NO
(1) :*:          TSTB  ASTKS        ;WAIT FOR A CHARACTER
(1) :*:          BPL   2$          ;LOOP UNTIL ITS THERE
(1) :*:          MOVB  ASTKB,-(SP) ;
(1) :*:          BIC   #^C177,(SP) ;GET CHARACTER
(1) :*:          CMP   (SP)+,#21  ;MAKE IT 7-BIT ASCII
(1) :*:          BNE   2$          ;IS IT A CONTROL-Q?
(1) :*:          BR    1$          ;IF NOT DISCARD IT
(1) :*:          BR    1$          ;YES, RESUME
(1) :*:          CMP   4(SP),#140 ;IS IT UPPER CASE?
(1) :*:          BLT   4$          ;BRANCH IF YES
(1) :*:          CMP   4(SP),#175 ;IS IT A SPECIAL CHAR?
(1) :*:          BGT   4$          ;BRANCH IF YES
(1) :*:          BIC   #40,4(SP) ;MAKE IT UPPER CASE
(1) :*:          RTI
(2) ****
(1) /*THIS ROUTINE WILL INPUT A STRING FROM THE TTY
(1) :*CALL:
(1) :* RDLIN
(1) :* RETURN HERE
(1) :*: RDLIN: INPUT A STRING FROM THE TTY
(1) :*: ADDRESS OF FIRST CHARACTER WILL BE ON THE STACK
(1) :*: TERMINATOR WILL BE A BYTE OF ALL 0'S

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TTY INPUT ROUTINE

SEQ 0167

(1) 026162	132737	000100	001221	BITB	#APTPPOOL,SENVM	;SPOOL MESSAGE TO APT
(1) 026170	001405			BEQ	62\$;NO, GO CHECK FOR CONSOLE
(1) 026172	010037	026202		MOV	R0,61\$;SETUP MESSAGE ADDRESS FOR APT
(1) 026176	004737	026422		JSR	PC,\$ATY3	;SPOOL MESSAGE TO APT
(1) 026202	000000			.WORD	0	;MESSAGE ADDRESS
(1) 026204	132737	000040	001221	61\$: BITB	#APTCSUP,SENVM	;APT CONSOLE SUPPRESSED
(1) 026212	001003			BNE	60\$;YES, SKIP TYPE OUT
(1) 026214	112046			2\$: MOVB	(R0)+,-(SP)	;PUSH CHARACTER TO BE TYPED ONTO STACK
(1) 026216	001005			BNE	4\$;BR IF IT ISN'T THE TERMINATOR
(1) 026220	005726			TST	(SP)+	;IF TERMINATOR POP IT OFF THE STACK
(1) 026222	012600			MOV	(SP)+,R0	;RESTORE R0
(1) 026224	062716	000002		ADD	#2,(SP)	;ADJUST RETURN PC
(1) 026230	000002			RTI		;RETURN
(1) 026232	122716	000011		CMPB	#HT,(SP)	;BRANCH IF <HT>
(1) 026236	001430			BEQ	8\$	
(1) 026240	122716	000200		CMPB	#CRLF,(SP)	;BRANCH IF NOT <CRLF>
(1) 026244	001006			BNE	5\$	
(1) 026246	005726			TST	(SP)+	;POP <CR><LF> EQUIV
(1) 026250	104401			TYPE		;TYPE A CR AND LF
(1) 026252	001175			\$CRLF		
(1) 026254	105037	026410		CLRB	\$CHARCNT	;CLEAR CHARACTER COUNT
(1) 026260	000755			BR	2\$;GET NEXT CHARACTER
(1) 026262	004737	026344		5\$: JSR	PC,\$TYPEC	;GO TYPE THIS CHARACTER
(1) 026266	123726	001156		6\$: CMPB	\$FILLC,(SP)+	;IS IT TIME FOR FILLER CHARS.?
(1) 026272	001350			BNE	2\$;IF NO GO GET NEXT CHAR.
(1) 026274	013746	001154		MOV	\$NULL,-(SP)	;GET # OF FILLER CHARS. NEEDED
(1)						;AND THE NULL CHAR.
(1)						;DOES A NULL NEED TO BE TYPED?
(1) 026300	105366	000001		7\$: DECB	1(SP)	
(1) 026304	002770			BLT	6\$;BR IF NO--GO POP THE NULL OFF OF STACK
(1) 026306	004737	026344		JSR	PC,\$TYPEC	;GO TYPE A NULL
(1) 026312	105337	026410		DEC B	\$CHARCNT	;DO NOT COUNT AS A COUNT
(1) 026316	000770			BR	7\$;LOOP
(1)						
;HORIZONTAL TAB PROCESSOR						
(1) 026320	112716	000040		8\$: MOVB	#" ,(SP)	;REPLACE TAB WITH SPACE
(1) 026324	004737	026344		9\$: JSR	PC,\$TYPEC	;TYPE A SPACE
(1) 026330	132737	000007	026410	BITB	#7,\$CHARCNT	;BRANCH IF NOT AT
(1) 026336	001372			BNE	9\$;TAB STOP
(1) 026340	005726			TST	(SP)+	;POP SPACE OFF STACK
(1) 026342	000724			BR	2\$;GET NEXT CHARACTER
(1) 026344	105777	152600		STYPEC: TSTB	@\$TPS	;WAIT UNTIL PRINTER IS READY
(1) 026350	100375			BPL	STYPEC	
(1) 026352	116677	000002	152572	MOVB	2(SP),@\$TPB	;LOAD CHAR TO BE TYPED INTO DATA REG.
(1) 026360	122766	000015	000002	CMPB	#CR,2(SP)	;IS CHARACTER A CARRIAGE RETURN?
(1) 026366	001003			BNE	1\$;BRANCH IF NO
(1) 026370	105037	026410		CLRB	\$CHARCNT	;YES--CLEAR CHARACTER COUNT
(1) 026374	000406			BR	STYPEX	;EXIT
(1) 026376	122766	000012	000002	1\$: CMPB	#LF,2(SP)	;IS CHARACTER A LINE FEED?
(1) 026404	001402			BEQ	STYPEX	;BRANCH IF YES
(1) 026406	105227			INC B	(PC)+	;COUNT THE CHARACTER
(1) 026410	000000			0		;CHARACTER COUNT STORAGE
(1) 026412	000207			RTS	PC	

.SBTTL APT COMMUNICATIONS ROUTINE

```

(2)
(1) 026414 112737 000001 026660 $ATY1: MOVB #1,$FFLG      ;:TO REPORT FATAL ERROR
(1) 026422 112737 000001 026656 $ATY3: MOVB #1,$MFLG      ;:TO TYPE A MESSAGE
(1) 026430 000403          BR $ATYC
(1) 026432 112737 000001 026660 SATY4: MOVB #1,$FFLG      ;:TO ONLY REPORT FATAL ERROR
(1) 026440          SATYC:
(3) 026440 010046          MOV R0,-(SP)      ;:PUSH R0 ON STACK
(3) 026442 010146          MOV R1,-(SP)      ;:PUSH R1 ON STACK
(1) 026444 105737 026656          TSTB $MFLG      ;:SHOULD TYPE A MESSAGE?
(1) 026450 001450          BEQ SS
(1) 026452 122737 000001 001220 CMPB #APTEENV,SENV   ;:OPERATING UNDER APT?
(1) 026460 001031          BNE 3S
(1) 026462 132737 000100 001221 BITB #APTSPOOL,SENVM ;:SHOULD SPOOL MESSAGES?
(1) 026470 001425          BEQ 3S
(1) 026472 017600 000004          MOV @4(SP),R0      ;:GET MESSAGE ADDR.
(1) 026476 062766 000002 000004 ADD #2,4(SP)      ;:BUMP RETURN ADDR.
(1) 026504 005737 001200          1$: TST $MSGTYPE    ;:SEE IF DONE W/ LAST XMISSION?
(1) 026510 001375          BNE 1S
(1) 026512 010037 001214          MOV R0,$MSGAD      ;:PUT ADDR IN MAILBOX
(1) 026516 105720          TSTB (R0)+      ;:FIND END OF MESSAGE
(1) 026520 001376          BNE 2S
(1) 026522 163700 001214          SUB $MSGAD,R0      ;:SUB START OF MESSAGE
(1) 026526 006200          ASR R0
(1) 026530 010037 001216          MOV R0,$MSGLGT      ;:GET MESSAGE LENGTH IN WORDS
(1) 026534 012737 000004 001200 MOV #4,$MSGTYPE    ;:PUT LENGTH IN MAILBOX
(1) 026542 000413          BR SS
(1) 026544 017637 000004 026570 3$: MOV @4(SP),4S      ;:TELL APT TO TAKE MSG.
(1) 026552 062766 000002 000004 ADD #2,4(SP)      ;:PUT MSG ADDR IN JSR LINKAGE
(3) 026560 013746 177776          MOV 177776,-(SP)  ;:BUMP RETURN ADDRESS
(1) 026564 004737 026132          JSR PC,$TYPE      ;:PUSH 177776 ON STACK
(1) 026570 000000          .WORD 0
(1) 026572 105737 026660          4$: .WORD 0
(1) 026576 001416          5$: .WORD 0
(1) 026600 005737 001220          10$: TSTB $FFLG      ;:SHOULD REPORT FATAL ERROR?
(1) 026604 001413          BEQ 12S
(1) 026606 005737 001200          TST $ENV
(1) 026612 001375          BEQ 12S
(1) 026614 017637 000004 001202 11$: TST $MSGTYPE    ;:FINISHED LAST MESSAGE?
(1) 026622 062766 000002 000004 MOV @4(SP),$FATAL    ;:IF NOT: WAIT
(1) 026630 005237 001200          ADD #2,4(SP)      ;:GET ERROR #
(1) 026634 105037 026660          INC $MSGTYPE      ;:BUMP RETURN ADDR.
(1) 026640 105037 026657          CLR B $FFLG
(1) 026644 105037 026656          CLR B $LFLG
(3) 026650 012601          CLR B $MFLG
(3) 026652 012600          MOV (SP)+,R1
(1) 026654 000207          MOV (SP)+,R0
(1) 026656 000          RTS PC
(1) 026657 000          .BYTE 0
(1) 026660 000          .BYTE 0
(1) 026662 000          .BYTE 0
(1) 000200          .EVEN
(1) 000001          APTSIZE=200
(1) 000100          APTENV=001
(1) 000040          APTSPPOOL=100
(1) 000040          APTCSUP=040
(1) 000000          .SBTTL POWER DOWN AND UP ROUTINES

```

```

(1)
(2)
(1) :*****POWER DOWN ROUTINE*****
(1) 026662 012737 027026 000024 $PWRDN: MOV #SILLUP,a#PWRVEC ;:SET FOR FAST UP
(1) 026670 012737 000340 000026 MOV #340,a#PWRVEC+2 ;:PRIO:7
(3) 026676 010046 MOV R0,-(SP) ;:PUSH R0 ON STACK
(3) 026700 010146 MOV R1,-(SP) ;:PUSH R1 ON STACK
(3) 026702 010246 MOV R2,-(SP) ;:PUSH R2 ON STACK
(3) 026704 010346 MOV R3,-(SP) ;:PUSH R3 ON STACK
(3) 026706 010446 MOV R4,-(SP) ;:PUSH R4 ON STACK
(3) 026710 010546 MOV R5,-(SP) ;:PUSH R5 ON STACK
(3) 026712 017746 152222 MOV @SWR,-(SP) ;:PUSH @SWR ON STACK
(1) 026716 010637 027032 MOV SP,$SAVR6 ;:SAVE SP
(1) 026722 012737 026734 000024 MOV #$PWRUP,a#PWRVEC ;:SET UP VECTOR
(1) 026730 000000 HALT
(1) 026732 000776 BR .-2 ;:HANG UP
(1)

(2) :*****POWER UP ROUTINE*****
(1) 026734 012737 027026 000024 $PWRUP: MOV #SILLUP,a#PWRVEC ;:SET FOR FAST DOWN
(1) 026742 013706 027032 MOV $SAVR6,SP ;:GET SP
(1) 026746 005037 027032 CLR $SAVR6 ;:WAIT LOOP FOR THE TTY
(1) 026752 005237 027032 1$: INC $SAVR6 ;:WAIT FOR THE INC
(1) 026756 001375 BNE 1$ ;:OF WORD
(3) 026760 012677 152154 MOV (SP)+,@SWR ;:POP STACK INTO @SWR
(3) 026764 012605 MOV (SP)+,R5 ;:POP STACK INTO R5
(3) 026766 012604 MOV (SP)+,R4 ;:POP STACK INTO R4
(3) 026770 012603 MOV (SP)+,R3 ;:POP STACK INTO R3
(3) 026772 012602 MOV (SP)+,R2 ;:POP STACK INTO R2
(3) 026774 012601 MOV (SP)+,R1 ;:POP STACK INTO R1
(3) 026776 012600 MOV (SP)+,R0 ;:POP STACK INTO R0
(1) 027000 012737 026662 000024 MOV #$PWRDN,a#PWRVEC ;:SET UP THE POWER DOWN VECTOR
(1) 027006 012737 000340 000026 MOV #340,a#PWRVEC+2 ;:PRIO:7
(1) 027014 104401 TYPE
(1) 027016 027034 SPWRMG: .WORD PWRMSG ;:REPORT THE POWER FAILURE
(1) 027020 012716 MOV (PC)+,(SP) ;:POWER FAIL MESSAGE POINTER
(1) 027022 001726 SPWRAD: .WORD START ;:RESTART AT START
(1) 027024 000002 RTI ;:RESTART ADDRESS
(1) 027026 000000 SILLUP: HALT ;:THE POWER UP SEQUENCE WAS STARTED
(1) 027030 000776 BR .-2 ;:BEFORE THE POWER DOWN WAS COMPLETE
(1) 027032 000000 $SAVR6: 0 ;:PUT THE SP HERE
3747 027034 015 012 PWRMSG: .BYTE 15,12
3748 027036 042522 052123 051101 .ASCII /RESTARTING AFTER A POWER FAILURE/
027044 044524 043516 040440
027052 052106 051105 040440
027060 050040 053517 051105
027066 043040 044501 052514
027074 042522 012 .BYTE 15,12,12,0
3749 027076 015 000 .EVEN
3750 027101 000 .SBTTL TRAP DECODER
(1)
(2)
(1) :*****THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION
(1) :*AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS

```

(1) ;*OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
(1) ;*GO TO THAT ROUTINE.

```
(1) 027102 010046      STRAP: MOV    R0,-(SP)      ;;SAVE R0
(1) 027104 016600      MOV    2(SP),R0      ;;GET TRAP ADDRESS
(1) 027110 005740      TST    -(R0)       ;;BACKUP BY 2
(1) 027112 111000      MOVB   (R0),R0      ;;GET RIGHT BYTE OF TRAP
(1) 027114 006300      ASL    RC          ;;POSITION FOR INDEXING
(1) 027116 016000      MOV    $TRPAD(R0),R0  ;;INDEX TO TABLE
(1) 027122 000200      RTS    R0          ;;GO TO ROUTINE
```

(1) ;;THIS IS USE TO HANDLE THE "GETPRI" MACRO

```
(1) 027124 011646      STRAP2: MOV   (SP),-(SP)    ;;MOVE THE PC DOWN
(1) 027126 016666      MOV   4(SP),2(SP)  ;;MOVE THE PSW DOWN
(1) 027134 000002      RTI    .           ;;RESTORE THE PSW
```

(3) .SBttl TRAP TABLE

(3) ;*THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED
(3) ;*BY THE "TRAP" INSTRUCTION.

(3) : ROUTINE

		STRPAD:	.WORD	STRAP2	
(3)	027136	027124	\$TYPE	;CALL=TYPE	TRAP+1(104401) TTY TYPEOUT ROUTINE
(3)	027140	026132	\$TYPLOC	;CALL=TYPLOC	TRAP+2(104402) TYPE OCTAL NUMBER (WITH LEADING ZEROS)
(3)	027142	024100	\$TYPPOS	;CALL=TYPOS	TRAP+3(104403) TYPE OCTAL NUMBER (NO LEADING ZEROS)
(3)	027144	024054	\$TYPON	;CALL=TYPON	TRAP+4(104404) TYPE OCTAL NUMBER (AS PER LAST CALL)
(3)	027146	024114	\$TYPDS	;CALL=TYPDS	TRAP+5(104405) TYPE DECIMAL NUMBER (WITH SIGN)

(1) 027152 025426 \$GTSWR :;CALL=GTSWR TRAP+6(104406) GET SOFT-SWR SETTING

(3)	027154	025356	\$CKSWR	;CALL=CKSWR	TRAP+7(104407) TEST FOR CHANGE IN SOFT-SWR
(3)	027156	025640	SRDCHR	;CALL=RDCHR	TRAP+10(104410) TTY TYPEIN CHARACTER ROUTINE
(3)	027160	025760	SRDLIN	;CALL=RDLIN	TRAP+11(104411) TTY TYPEIN STRING ROUTINE
(3)	027162	025254	SRDOCT	;CALL=RDOCT	TRAP+12(104412) READ AN OCTAL NUMBER FROM TTY

3752 027164 023700 IOTRD :;CALL=IOTT TRAP+13(104413)

3753 027166 005015 046103 041517 EM1: .ASCIZ <15><12>/CLOCKA SR FUNCTION ERROR/

027174 040513 051440 020122
 027202 052506 041516 044524
 027210 047117 042440 051122

027216 051117 000

3754 027221 015 041412 047514 EM2: .ASCIZ <15><12>/CLOCKA SR DATA ERROR/

027226 045503 020101 051123
 027234 042040 052101 020101

027242 051105 047522 000122

3755 027250 005015 046103 041517 EM3: .ASCIZ <15><12>/CLOCKA BR DATA ERROR/

027256 040513 041040 020122

027264 040504 040524 042440

027272 051122 051117 000

3756 027277 015 041412 047514 EM4: .ASCIZ <15><12>/CLOCKA CR DATA ERROR/

027304 045503 020101 051103

027312 042040 052101 020101

027320 051105 047522 000122

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TRAP TABLE

SEQ 0172

3757	027326	005015	046103	041517	EM5: .ASCIZ <15><12>/CLOCKB SR DATA ERROR/
	027334	041113	051440	020122	
	027342	040504	040524	042440	
	027350	051122	051117	000	
3758	027355	015	041412	047514	EM6: .ASCIZ <15><12>/CLOCKB BR DATA ERROR/
	027362	045503	020102	051102	
	027370	042040	052101	020101	
	027376	051105	047522	000122	
3759	027404	005015	046103	041517	EM7: .ASCIZ <15><12>/CLOCKB CR DATA ERROR/
	027412	041113	041440	020122	
	027420	040504	040524	042440	
	027426	051122	051117	000	
3760	027433	015	042012	040525	EM10: .ASCIZ <15><12>/DUAL ADDRESS ERROR/
	027440	020114	042101	051104	
	027446	051505	020123	051105	
	027454	047522	000122		
3761	027460	005015	046103	041517	EM11: .ASCIZ <15><12>#CLOCK A COUNT ERROR #
	027466	020113	020101	047503	
	027474	047125	020124	051105	
	027502	047522	020122	000	
3762	027507	015	041412	047514	EM12: .ASCIZ <15><12>#CLOCK A COUNT FUNCTION ERROR #
	027514	045503	040440	041440	
	027522	052517	052116	043040	
	027530	047125	052103	047511	
	027536	020116	051105	047522	
	027544	020122	000		
3763	027547	015	041412	047514	EM14: .ASCIZ <15><12>#CLOCK B COUNT FUNCTION ERROR #
	027554	045503	041040	041440	
	027562	052517	052116	043040	
	027570	047125	052103	047511	
	027576	020116	051105	047522	
	027604	020122	000		
3764	027607	015	041412	047514	EM15: .ASCIZ <15><12>#CLOCK B COUNT ERROR #
	027614	045503	041040	041440	
	027622	052517	052116	042440	
	027630	051122	051117	000040	
3765	027636	005015	046103	041517	EM16: .ASCIZ <15><12>#CLOCK A INTERRUPT ERROR #
	027644	020113	020101	047111	
	027652	042524	051122	050125	
	027660	020124	051105	047522	
	027666	020122	000		
3766	027671	015	041412	047514	EM17: .ASCIZ <15><12>#CLOCK B INTERRUPT ERROR #
	027676	045503	041040	044440	
	027704	052116	051105	052522	
	027712	052120	042440	051122	
	027720	051117	000040		
3767	027724	005015	046103	041517	EM20: .ASCIZ <15><12>#CLOCK A REPEATABILITY ERROR #
	027732	020113	020101	042522	
	027740	042520	052101	041101	
	027746	046111	052111	020131	
	027754	051105	047522	020122	
	027762	000			
3768	027763	015	041412	047514	EM23: .ASCIZ <15><12>#CLOCK B REPEATABILITY ERROR #
	027770	045503	041040	051040	
	027776	050105	040505	040524	
	030004	044502	044514	054524	

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TRAP TABLE

SEQ 0173

	030012	042440	051122	051117					
	030020	000040							
3769	030022	005015	046103	041517	EM26:	.ASCIIZ <15><12>#CLOCK ADDRESSING ERROR#			
	030030	020113	042101	051104					
	030036	051505	044523	043516					
	030044	042440	051122	051117					
	030052	000							
3770									
3771	030053	015	042412	051122	DH1:	.ASCIIZ <15><12>#ERRPC	ASR	WAS	S/B#
	030060	041520	020040	040440					
	030066	051123	020040	020040					
	030074	053440	051501	020040					
	030102	020040	051440	041057					
	030110	000							
3772	030111	015	042412	051122	DH3:	.ASCIIZ <15><12>#ERRPC	ABR	WAS	S/B#
	030116	041520	020040	040440					
	030124	051102	020040	020040					
	030132	053440	051501	020040					
	030140	020040	051440	041057					
	030146	000							
3773	030147	015	042412	051122	DH4:	.ASCIIZ <15><12>#ERRPC	ACR	WAS	S/B#
	030154	041520	020040	040440					
	030162	051103	020040	020040					
	030170	053440	051501	020040					
	030176	020040	051440	041057					
	030204	000							
3774	030205	015	042412	051122	DH5:	.ASCIIZ <15><12>#ERRPC	BSR	WAS	S/B#
	030212	041520	020040	041040					
	030220	051123	020040	020040					
	030226	053440	051501	020040					
	030234	020040	051440	041057					
	030242	000							
3775	030243	015	042412	051122	DH6:	.ASCIIZ <15><12>#ERRPC	BBR	WAS	S/B#
	030250	041520	020040	041040					
	030256	051102	020040	020040					
	030264	053440	051501	020040					
	030272	020040	051440	041057					
	030300	000							
3776	030301	015	042412	051122	DH7:	.ASCIIZ <15><12>#ERRPC	BCR	WAS	S/B#
	030306	041520	020040	041040					
	030314	051103	020040	020040					
	030322	053440	051501	020040					
	030330	020040	051440	041057					
	030336	000							
3777	030337	015	042412	051122	DH10:	.ASCII <15><12>/ERROR	GOOD	BAD	GOOD DATA READ FROM/
	030344	051117	020040	043440					
	030352	047517	020104	020040					
	030360	041040	042101	020040					
	030366	020040	043440	047517					
	030374	020104	020040	042040					
	030402	052101	020101	042522					
	030410	042101	043040	047522					
	030416	115							
3778	030417	015	020012	050040		.ASCIIZ <15><12>/ PC	ADDR	ADDR	DATA DUAL ADDRESS/
	030424	020103	020040	040440					
	030432	042104	020122	020040					

030440	040440	042104	020122				
030446	020040	042040	052101				
030454	020101	020040	042040				
030462	040525	020114	042101				
030470	051104	051505	000123				
3779	030476	005015	051105	050122	DH12:	.ASCIZ <15><12>#ERRPC	ASR #
	030504	020103	020040	051501			
	030512	020122	000				
3780	030515	015	042412	051122	DH14:	.ASCIZ <15><12>#ERRPC	BSR#
	030522	041520	020040	041040			
	030530	051123	000				
3781	030533	015	042412	051122	DH20:	.ASCIZ <15><12>#ERRPC	ASR 2NDCNT 1STCNT #
	030540	041520	020040	040440			
	030546	051123	020040	020040			
	030554	031040	042116	047103			
	030562	020124	030440	052123			
	030570	047103	020124	000			
3782	030575	015	042412	051122	DH23:	.ASCIZ <15><12>#ERRPC	BSR 2NDCNT 1STCNT #
	030602	041520	020040	041040			
	030610	051123	020040	020040			
	030616	031040	042116	047103			
	030624	020124	030440	052123			
3783	030632	047103	020124	000	DH26:	.ASCIZ <15><12>#ERRPC	CLOCK ADDR.#
	030637	015	042412	051122			
	030644	041520	020040	041440			
	030652	047514	045503	040440			
	030660	042104	027122	000			
3784							
3785		030666				.EVEN	
3786							
3787	030666	001116	001324	001126	DT1:	.WORD	SERRPC,ASR,\$BDDAT,\$GDDAT,0
	030674	001124	000000				
3788	030700	001116	001326	001126	DT3:	.WORD	SERRPC,ABR,\$BDDAT,\$GDDAT,0
	030706	001124	000000				
3789	030712	001116	001330	001126	DT4:	.WORD	SERRPC,ACR,\$BDDAT,\$GDDAT,0
	030720	001124	000000				
3790	030724	001116	001332	001126	DT5:	.WORD	SERRPC,BSR,\$BDDAT,\$GDDAT,0
	030732	001124	000000				
3791	030736	001116	001334	001126	DT6:	.WORD	SERRPC,BBR,\$BDDAT,\$GDDAT,0
	030744	001124	000000				
3792	030750	001116	001336	001126	DT7:	.WORD	SERRPC,BCR,\$BDDAT,\$GDDAT,0
	030756	001124	000000				
3793	030762	001116	001120	001122	DT10:	.WORD	SERRPC,\$GDADR,\$BDADR,\$GDDAT,\$BDDAT,0
	030770	001124	001126	000000			
3794	030776	001116	001324	000000	DT12:	.WORD	SERRPC,ASR,0
	031004	001116	001332	000000	DT14:	.WORD	SERRPC,BSR,0
3795	031012	001116	001330	001124	DT21:	.WORD	SERRPC,ACR,\$GDDAT,\$TMPO,0
	031020	001164	000000				
3797	031024	001116	001330	001126	DT22:	.WORD	SERRPC,ACR,\$BDDAT,\$TMPO,0
	031032	001164	000000				
3798	031036	001116	001336	001124	DT24:	.WORD	SERRPC,BCR,\$GDDAT,\$TMPO,0
	031044	001164	000000				
3799	031050	001116	001336	001126	DT25:	.WORD	SERRPC,BCR,\$BDDAT,\$TMPO,0
	031056	001164	000000				
3800	031062	001116	001164	000000	DT26:	.WORD	SERRPC,\$TMPO,0
3801							

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TRAP TABLE

SEQ 0176

(2) 031162 001376
(2) 031164 012777 104000 150444 25\$: BNE 2\$
MOV #BIT15!BIT11,@KMADO ;SET RUN, AND ENABLE ARBITRATION.
(2) 031172 105201 INCB R1
(2) 031174 001376 BNE 25\$
(2)
(2) 031176 032777 000040 150432 BIT #BITS,@KMADO ;SLAVE READY? (READING IPBM SR)
(2) 031204 001401 BEQ 3\$;FATAL LPA-11 ERROR SLAVE NOT READY.
(2) 031206 104000 ERROR
(2)
(2) 031210 012777 000004 150424 3\$: MOV #4,@KMAD2 ;READ FAST PATH
(2) 031216 4\$: JSR R5, \$STOUT ;-TOUT-CHECK FOR TIMEOUT
(3) 031216 004537 032474
(3) 031222 104000 ERROR ;/TIME-OUT ERROR
;/WE FAILED TO COMPLETE
;/CURRENT OPERATION.
;/CONTINUES IN THIS LOOP
;/WOULD MAKE US "HANG" HERE
(3)
(3) 031224 000774 BR 4\$
(3)
(3) 031226 122777 000377 150406 CMPB #377,@KMAD2 ;/RETURNS HERE-FROM-TIMED OUT.
BNE 4\$;WAIT TILL KMC DONE COMMAND.
(2) 031234 001370 000377 150402 CMPB #377,@KMAD4 ;IF FAST PATH=377 THEN ERROR.
BNE 35\$
(2) 031244 001001 104000 ERROR ;IPBM ERROR (SLAVE SIDE)
;/YOU MUST RUN IPBM DIAGNOSTIC.
(2)
(2) 031250 117737 150372 031530 35\$: MOVB @KMAD4,11\$;GET THE VERSION NUMBER FROM DMC-11
INC #-1
(2) 031262 001045 BNE 5\$
(2) 031264 005227 177777 INC #-1
(2) 031270 001042 BNE 5\$
(3) 031272 104401 031300 TYPE ,67\$;;TYPE ASCIZ STRING
(3) 031276 000426 031300 BR ,66\$;;GET OVER THE ASCIZ
;:67\$: .ASCIZ <200>'M8200-YC (DMC) MICROCODE VERSION NUMBER = ''
;:66\$:
(3) 031354 013746 031530 MOVB 11\$,-(SP)
(2) 031360 104403 TYPOS
(2) 031362 002 000 BYTE 2,0
(3) 031364 104401 031372 TYPE ,69\$;;TYPE ASCIZ STRING
(3) 031370 000402 BR ,68\$;;GET OVER THE ASCIZ
;:69\$: .ASCIZ <200>'' ''
;:68\$:
(2)
(2) 031376 112737 177777 031530 5\$: MOVB #0-1,11\$;DAC CODE FOR SLAVE.
MOV (5)+,R1 ;GET NEXT DEVICE ADDR.
(2) 031404 012501 CMP (R1),#0 ;TERM REACHED?
(2) 031406 021127 000000 6\$: BEQ 10\$
(2) 031412 001444 INCB 11\$
(2) 031414 105237 031530 MOV B 11\$,@KMAD4 ;FIFO DATA
(2) 031420 113777 031530 150220 JSR PC,20\$;ISSUE SEND
(2) 031426 004737 031532 MOV B (R1)+,@KMAD4 ;SEND LOW BYTE OF DEVICE ADDR TO SLAVE.
(2) 031432 112177 150210 JSR PC,20\$;ISSUE SEND
(2) 031436 004737 031532

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SEQ 0177

(2) 031442 112177 150200
(2) 031446 004737 031532
(2)
(2) 031452 032777 000002 150156 7\$: MOVB (R1)+, @KMAD4 ;SEND HIGH BYTE OF DEVICE ADDR. TO SLAVE.
(2) 031460 001374 7\$:
(2) 031462 112777 000002 150152 BIT #BIT1, @KMAD0 ;WAIT FOR FIFO DATA
BNE 7\$;=1 NO DATA. =0 DATA.
MOVBL #2, @KMAD2 ;READ FIFO.
(2)
(2) 031470 004537 032474 8\$: JSR R5, \$OUT ;-TOUT-CHECK FOR TIMEOUT
(3) 031474 104000 ERROR ;/TIME-OUT ERROR
;/WE FAILED TO COMPLETE
;/CURRENT OPERATION.
;/CONTINUES IN THIS LOOP
;/WOULD MAKE US "HANG" HERE
(3) 031476 000774 BR 8\$
;/RETURNS HERE-FROM-TIMED OUT.
;/WAIT FOR READ.
(2) 031500 122777 000377 150134 CMPB #377, @KMAD2 ;WAS A ZERO RETURNED?
(2) 031506 001370 BNE 8\$;YES GET NEXT ADDR.
(2) 031510 105777 150132 TSTB @KMAD4 ;SLAVE WILL RETURN CODE 0 IF
(2) 031514 001734 BEQ 6\$;DEV PRESENT. ELSE
INC SAERR ;EXIT SAERR=1 IF SLAVE GIVES ERROR.
;(2) 031516 005237 031562 CLR -(1) ;GET RID OF REFERENCE TO BAD ADDR.
;(2) 031522 005041 MOV (SP)+, R1 ;RETURN ALL ADDR. CHECKED.
;(2) 031524 012601 RTS R5
;(2) 031526 000205
;(2) 031530 000000 11\$: .WORD 0 ;HOLDS DAC CODE PLUS OFFSET
;(2) ;TO SLAVES ADDR. TABLE.
;(2) 031532 112777 000003 150102 20\$: MOVBL #3, @KMAD2 ;ISSUE FIFO WRITE
;(2) 031540 004537 032474 21\$: JSR R5, \$OUT ;-TOUT-CHECK FOR TIMEOUT
(3) 031540 004537 032474 ERROR ;/TIME-OUT ERROR
;/WE FAILED TO COMPLETE
;/CURRENT OPERATION.
;/CONTINUES IN THIS LOOP
;/WOULD MAKE US "HANG" HERE
(3) 031546 000774 BR 21\$
;/RETURNS HERE-FROM-TIMED OUT.
;(2) 031550 122777 000377 150064 CMPB #377, @KMAD2 ;KMC CODE WILL RETURN A "377"
(2) 031556 001370 BNE 21\$;WHEN DONE COMMAND.
(2) 031560 000207 RTS PC
;(2) 031562 000000 SAERR: .WORD 0 ;=0 IF ADDR. LIST OK, =1 IF BAD.
;(2)
;(2) ;* THIS SUB CODE USED TO LOAD MICRO-CODE INTO LPA-11.
;(2) ;* CALL = JSR R5, \$LOAD
;(2) ;* .WORD XX ;ADDR. OF MICRO CODE.

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TRAP TABLE

SEQ 0179

(2) 031740 010037 032032 MOV R0,W1
(2) 031744 010077 147676 MOV R0,@KMA4
(2) 031750 112777 000005 147664 MOV #5,@KMA2 ;ISSUE FAST PATH WRITE
(2) 031756 004737 032206 JSR PC,SLPW ;WAIT FOR RDY
(2) 031762 011537 032034 MOV (5),W2
(2) 031766 112577 147654 MOV #5+,@KMA4 ;WRITE LOW BYTE DATA.
(2)
(2) 031772 112777 000005 147642 MOV #5,@KMA2 ;FP WRITE
(2) 032000 004737 032206 JSR PC,SLPW
(2) 032004 111537 032036 MOV (5),W3
(2) 032010 112577 147632 MOV #5+,@KMA4 ;WRITE HIGH BYTE
(2) 032014 112777 000005 147620 MOV #5,@KMA2
(2) 032022 004737 032206 JSR PC,SLPW
(2) 032026 012600 MOV (SP)+,R0
(2) 032030 000205 RTS R5 ;EXIT DONE.
(2)
(2) W1: 0
(2) W2: 0
(2) W3: 0

;*
;* THIS ROUTINE ISSUES A READ COMMAND TO THE LPA-11
;*
;* CALL = JSR R5,STLKR ;OFFSET OF DEVICE
;* .WORD 0
;* :RETURNS HERE
;* DATA IN WORD \$DATR
;*

(2) 032040 010046 STLKR: MOV R0,-(SP) ;SAVE R0
(2) 032042 012500 MOV (5)+,R0 ;GET OFFSET
(2) 032044 052700 000300 BIS #300,R0 ;ADD READ CODE
(2) 032050 004737 032206 JSR PC,SLPW ;WAIT TILL READY
(2) 032054 110077 147566 MOV R0,@KMA4
(2) 032060 112777 000005 147554 MOV #5,@KMA2 ;ISSUE WRITE FP
(2) 032066 004737 032206 JSR PC,SLPW
(2) 032072 010037 032202 MOV R0,RD1
(2) 032076 004537 032474 1\$: JSR R5, STOUT ;-TOUT-CHECK FOR TIMEOUT
(3) 032076 004537 032474 ERROR ;/TIME-OUT ERROR
(3) 032102 104000 ;/WE FAILED TO COMPLETE
(3) ;/CURRENT OPERATION.
(3) ;/CONTINUES IN THIS LOOP
(3) ;/WOULD MAKE US 'HANG' HERE
(3) 032104 000774 BR 1\$
(3) ;/RETURNS HERE-FROM-TIMED OUT.
(2) 032106 032777 000040 147522 BIT #BITS,@KMA0 ;FAST PATH GOT DATA?
(2) 032114 001370 BNE 1\$
(2) 032116 112777 000004 147516 MOV #4,@KMA2 ;ISSUE FAST PATH READ
(2) 032124 004737 032206 JSR PC,SLPW
(2) 032130 117737 147512 032204 MOV @KMA4,\$DATR ;GET LOW BYTE
(2) 032136 004537 032474 2\$: JSR R5, STOUT ;-TOUT-CHECK FOR TIMEOUT
(3)

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(3) 032142 104000           ERROR
(3)
(3)
(3)
(3)
(3) 032144 000774           BR      2$ 
(3)
(3)
(3) 032146 032777 000040 147462   BIT    #BIT5,@KMADO ;/TIME-OUT ERROR
(2) 032154 001370           BNE    2$ ;/WE FAILED TO COMPLETE
(2) 032156 112777 000004 147456   MOVB   #4,@KMAD2 ;/CURRENT OPERATION.
(2) 032164 004737 032206           JSR    PC,$LPW ;/CONTINUES IN THIS LOOP
(2) 032170 117737 147452 032205   MOVB   @KMAD4,$DATR+1 ;/WOULD MAKE US 'HANG' HERE
(2) 032176 012600           MOV    (SP)+,R0
(2) 032200 000205           RTS    R5
(2) 032202 000000           RD1:  0
(2) 032204 000000           SDATR: .WORD 0 ;/RETURNS HERE-FROM-TIMED OUT.
(2)
(2)
(2) :FAST PATH READY?
(2) :ISSUE FAST PATH READ
(2) :SAVE HIGH BYTE
(2)
(2)
(2) RD1: 0
(2) SDATR: .WORD 0
(2)
(2) :THIS ROUTINE WAITS FOR KMC-CODE TO BECOME READY AS WELL
(2) :AS FAST PATH TO BE READ.
(2)
(2) CALL = JSR PC,$LPW
(2)
(2) :IT WILL TIME OUT IF TOO MUCH TIME IS TAKEN BY
(2) :THE MICRO-PROCESSORS AND REPORT AN ERROR, THEN HALT.
(2)
(2) 032206 010146           SLPW:  MOV    R1,-(SP) ;SAVE R1
(2) 032210 005001           CLR    R1
(2) 032212 122777 000377 147422 1$:  CMPB   #377,@KMAD2 ;FINISHED INSTRUCTION?
(2) 032220 001403           BEQ    2$ ;TIME OUT?
(2) 032222 005201           INC    R1
(2) 032224 001372           BNE    1$ ;TIME OUT?
(2) 032226 000411           BR     10$ ;YES - REPORT AN ERROR
(2)
(2) 032230 032777 000020 147400 2$:  BIT    #BIT4,@KMADO ;FAST PATH READ?
(2) 032236 001403           BEQ    3$ ;NO - TIME OUT?
(2) 032240 005201           INC    R1
(2) 032242 001372           BNE    2$ ;YES - REPORT AN ERROR
(2) 032244 000402           BR     10$ ;RESTORE R1
(2)
(2) 032246 012601           3$:  MOV    (SP)+,R1 ;RESTORE R1
(2) 032250 000207           RTS    PC ;EXIT
(2)
(2) 032252 104401 032260       10$: TYPE   ,65$ ;:TYPE ASCIZ STRING
(3) 032252 000407           BR     ,64$ ;:GET OVER THE ASCIZ
(3) :;65$: .ASCIZ <200>#LPA-11 FAULT#
(3) 032276                 64$: 
(2)
(2) 032276 000000           11$: HALT  11$ ;LPA-11 FAULT RUN LPA-11
(2) 032300 000776           BR     11$ ;DIAGNOSTICS.
(2)
(2)

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(2)                                ;*
(2)                                ;*THIS ROUTINE PROVIDES THE LINKAGE FROM USER CODE TO
(2)                                ;*A DEVICE ADDRESS ON THE I/O BUSS FOR WRITE ONLY.
(2)
(2)                                ;*
(2)                                ;* FIRST WE WILL DETERMINE IF THE ADDRESS HAS BEEN USED
(2)                                ;* BEFORE. IF NOT WE HAVE TO INITIALIZE THE LPA WITH
(2)                                ;* THAT ADDRESS.
(2)                                ;* WHEN THE ADDR. IS KNOWN BY THE LPA, DO THE OUTPUT BY
(2)                                ;* $TLKW
(2)
(2)                                ;*
(2) 032302 010046                 $OUTLP: MOV    R0,-(SP)      ;SAVE R0
(2) 032304 010146                 MOV    R1,-(SP)      ;SAVE R1
(2)
(2) 032306 012700 001664          1$:   MOV    #.DVLS,R0      ;PROGRAM DEFINED LIST.
(2) 032312 005001                 CLR    R1
(2) 032314 005710                 TST    (0)          ;TERMINATOR REACHED?
(2) 032316 001421                 BEQ    10$         ;YES NEXT STEP.
(2) 032320 027520 000000          CMP    @($),($)+    ;MATCH WITH ADDR IN LIST?
(2) 032324 001402
(2) 032326 005201
(2) 032330 000771
(2)
(2) 032332 010137 032350          2$:   MOV    R1,3$        ;SAVE OFFSET, DEVICE KNOWN.
(2) 032336 005725
(2) 032340 013537 032352          3$:   TST    ($)+        ;GET DATA TO BE WRITTEN
(2) 032344 004537 031724          JSR    R5,$TLKW     ;DO WRITE
(2) 032350 000000                 .WORD  0           ;DEVICE OFFSET
(2) 032352 000000                 4$:   .WORD  0           ;DATA TO BE WRITTEN.
(2) 032354 012601
(2) 032356 012600
(2) 032360 000205
(2) 032362 017520 000000          10$:  RTS   R5
(2) 032366 005010
(2) 032370 004537 031074          MOV    @($),($)+    ;SAVE ADDR.
(2) 032374 001664
(2) 032376 000755
(2)

(2)                                ;*
(2)                                ;*THIS ROUTINE PROVIDES THE LINKAGE FROM USER CODE
(2)                                ;*TO A DEVICE ADDR. ON THE I/O BUSS FOR READ ONLY.
(2)
(2)                                ;*
(2)                                ;* FIRST WE WILL DETERMINE IF THE ADDRESS HAS BEEN
(2)                                ;* USED BEFORE. IF NOT, WE HAVE TO INITIALIZE THE LPA
(2)                                ;* WITH THE NEW ADDR.
(2)                                ;* WHEN THE ADDR IS KNOWN WE CAN DO OUTPUT THROUGH
(2)                                ;* $TLKR
(2)                                ;* CALL THROUGH MOVEI  DATA,ADDR.
(2)                                ;* WHICH EQUALS:
(2)                                ;* JSR    R5,$INLP
(2)                                ;* .WORD XX      ADDR OF DEVICE
(2)                                ;* .WORD YY      ADDR TO STORE READ DATA.
(2)
(2) 032400 010046                 $INLP: MOV    R0,-(SP)      ;SAVE R0
(2) 032402 010146                 MOV    R1,-(SP)      ;SAVE R1
(2)

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(2) 032404 012700 001664          MOV    #.DVLS,R0      ;PROG DEFINED ADDR. LIST.
(2) 032410 005001
(2) 032412 005710
(2) 032414 001420
(2) 032416 027520 000000          1$:   CLR    R1
(2) 032422 001402
(2) 032424 005201
(2) 032426 000771
(2) 032430 010137 032442          CMP    a(5),(0)+   ;ADDR. MATCH?
(2) 032434 005725
(2) 032436 004537 032040          TST    (0)
(2) 032442 032442
(2) 032442 000000          JSR    R5,$STLKR   ;GO READ DEVICE
(2) 032442 000000          $OFS=. .WORD  0           ;OFFSET OF DEVICE
(2) 032444 013735 032204          MOV    SDATR,a(5)+ ;STORE DATA.
(2) 032450 012601
(2) 032452 012600
(2) 032454 000205
(2) 032456 017520 000000          2$:   MOV    (5)+,R1   ;RESTORE R1
(2) 032462 005010
(2) 032464 004537 031074          CLR    (SP)+,R1   ;RESTORE R2
(2) 032470 001664
(2) 032472 000756
(2) 032474 020537 032530          3$:   JSR    R5,$LPAL   ;EXIT
(2) 032500 001405
(2) 032502 010537 032530          .WORD  DVLS
(2) 032506 005037 032532          BR    2$           ;*
(2) 032512 000403
(2) 032514 005237 032532          $STOUT: CMP    R5,$$AD   ;SAME ADDR?
(2) 032520 100402
(2) 032522 062705 000004          BEQ    1$           ;NO-SAVE THIS ADDR.
(2) 032526 000205
(2) 032530 000000          1$:   MOV    R5,$$AD   ;CLR CNT AT ADDR.
(2) 032532 000000          CLR    SCNT
(2) 032530 000000          BR    2$           ;OVERFLOW?
(2) 032532 000000          2$:   INC    SCNT
(2) 032530 000000          BMI    3$           ;YES-ERROR RETURN
(2) 032532 000000          3$:   ADD    #4,R5   ;NO-NON ERROR RETURN
(2) 032530 000000
(2) 032532 000000          RTS    R5           ;RETURN.
(2) 032530 000000          $SAD: .WORD  0           ;CONTAINS LOOP ADDR.
(2) 032532 000000          $CNT: .WORD  0           ;# OF TIMES AT ADDR.
(2) 032530 000000
(2) 032532 000000          :* THIS ROUTINE REPLACES WHAT THE USER WOULD ORDINARILY
(2) 032530 000000          :* USE FOR A RESET. FIRST, WE DO A RESET INSTRUCTION.
(2) 032532 000000          :* THEN WE CLR ".DVLST" WHICH FORCES US TO RESET BOTH THE
(2) 032530 000000          :* KMC AND DMC AS SOON AS A DEVICE IS REFERENCED.
(2) 032532 000000          :* CALL=JSR      PC,$RESET   ;REPLACES 'RESET INSTRUCTION
(2) 032530 000000          :* ;RETURNS HERE.

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SEA 0183

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(2) 032534 000005      $RESET: RESET          ;RESET THE WORLD.
(2) 032546 005737 031562      :*    MOV    #2$,1$  ;/READ DEVICE REG 2$,PUT DATA IN 1$.
(2) 032552 001004      TST    $AERR           ;IF NO ERROR,LOOP
(2) 032554 062737 000002 032570      BNE    10$            ;THERE WAS AN ERROR.
(2)                                ADD    #2,2$          ;UPDATE DEVICE ADDR.
(2)                                :YOU SEE ,WE HAVE TO PROTECT OUR SELF!
(2)                                :IF 2$ CONTAINED A VALID ADDR,WE
(2)                                :MUST KEEP TRYING UNTIL WE GENERATE
(2)                                :AN INVALID ADDR.

(2) 032562 000764      BR     $RESET
(2) 032564 000207      10$:   RTS    PC
(2) 032564 000000      1$:    .WORD   0             ;JUNK LOC.
(2) 032570 160000      2$:    .WORD   160000        ;DUMB ADDR. FORCES INIT OF DMC/KMC.

(2)
(2)
(2)                                :SDELAY- ROUTINE TO GIVE A MINOR DELAY.
(2)                                :IS NOT TIME DEPENDENT CODE SENCE
(2)                                :NOT USED TO GET SPECIFIC TIME BUT
(2)                                :JUST A LITTLE DELAY.

(2)
(2)                                :THAT IS UNLESS A REAL TIME CLOCK IS PRESENT!
(2)                                :THEN WE'LL GENERATE A TIME BETWEEN 16MS TO 32 MS

(2)
(2)                                :CALL= JSR PC, SDELAY

(2) 032572      SDELAY:
(2) 032572 005737 032654      TST    RTCCSR          ;CLOCK PRESENT?
(2) 032576 100016      BPL    10$            ;TIME
(2) 032600 012737 000002 032644      MOV    #2,TIME
(2) 032606 052777 000115 000040      BIS    #115,@RTCCSR ;START CLOCK
(2) 032614 005037 177776      CLR    PS
(2) 032620 005737 032644      1$:    TST    TIME
(2) 032624 001375      BNE    1$            ;STOP CLOCK
(2) 032626 005077 000022      CLR    @RTCCSR         ;STOP CLOCK

(2) 032632 000207      RTS    PC
(2) 032634 105237 032644      10$:   INCB   TIME
(2) 032640 001375      BNE    10$            ;TIME
(2) 032642 000207      RTS    PC

(2) 032644 000000      TIME:  .WORD   0

(2) 032646 005337 032644      CLKINT: DEC    TIME
(2) 032652 000002      RTI
(2) 032654 000000      RTCCSR: .WORD   0             ;CLOCK CSR IF USED.

(2)
(2)
(2)                                :*THIS MACRO ALLOWS THE OPERATOR TO TALK TO
(2)                                :*ANY DEVICE ON THE I/O BUS
(2)                                :*USER MUST START AT THIS ADDR.
(2)                                :*HE MUST SAY EITHER 'E' FOR EXAMINE, OR 'D' FOR DEPOSIT.

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(2) ;*'E' IS DEFAULT.
 (2) ;*NEXT, HE MUST SUPPLY AN ADDR.
 (2) ;*NOTE IF ADDR. IS NOT FOUND ON I/O BUS, A HALT
 (2) ;*WILL OCCUR.

(2) 032656	005037	001664	SUTK:	CLR	.DVLS	
(2) 032662	104401	032670	21\$:	TYPE	,65\$;TYPE ASCIZ STRING
(3) 032666	000405			BR	,64\$;GET OVER THE ASCIZ
(3) 032702	105777	146236	:65\$:	.ASCIZ	<200>#E OR D?#	
(2) 032702	100375		64\$:	TSTB	a\$TKS	
(2) 032710	117737	146232	1\$:	BPL	1\$	
(2) 032716	104401	033032		MOVB	a\$TKB,20\$:GET INPUT
(2) 032722	142737	000240		TYPE,	20\$:ECHO, NEXT MESSAGE.
(2) 032730	104412			BICB	#240,20\$:STRIP PARITY, LC
(2) 032732	012637	033030		RDOCT		:GET ADDR.
(2) 032736	123727	033032	000104	MOV	(SP)+,14\$	
(2) 032744	001411			CMPB	20\$,#D	:DEPOSIT?
(2) 032746	004537	032400		BEQ	10\$	
(2) 032752	033030		2\$:	JSR	R5,\$INLP	:GET DATA
(2) 032754	032766			.WORD	14\$	
(3) 032756	013746	032766		.WORD	5\$	
(3) 032762	104402			MOV	5\$,-(SP)	;SAVE 5\$ FOR TYPEOUT
(2) 032764	000736			TYPOC		;GO TYPE--OCTAL ASCII(ALL DIGITS)
(2) 032766	000000		5\$:	BR	21\$;LOOP.
(2) 032770			10\$:	.WORD	0	
(5) 032770	104401	032776		TYPE	,67\$;TYPE ASCIZ STRING
(3) 032774	000404			BR	,66\$;GET OVER THE ASCIZ
(3) 033006			:67\$:	.ASCIZ	<200>#DATA= #	
(3) 033006	104412		66\$:	RDOCT		
(2) 033010	012637	033026		MOV	(SP)+,13\$	
(2) 033014	004537	032302	11\$:	JSR	R5,\$OUTLP	:OUTPUT ROUTINE.
(2) 033020	033030		12\$:	.WORD	14\$:DEVICE ADDR.
(2) 033022	033026			.WORD	13\$:DATA
(2) 033024	000716			BR	21\$	
(2) 033026	000000		13\$:	.WORD	0	
(2) 033030	000000		14\$:	.WORD	0	
(2) 033032	100001	042504	044526	.ASCIZ	<1><200>#DEVICE ADDR= #	
(2) 033040	042503	040440	042104			
(2) 033046	036522	000040		EVEN		

(2)
 (1)
 (2)
 (2)
 (2)
 :THIS ROUTINE LOOKS THROUGH CURRENT .DVLS FOR A/D ADDR.
 :IF UNFOUND, GENERATES IT. THIS ROUTINE'S WHOLE PURPOSE IS

(2) :TO SET UP THE USER PROGRAM TO LINK TO FILE 'DRLPX2' FOR
(2) SAMPLE TAKEING PURPOSES.
(2) TO TAKE SAMPLES, THE USER PROGRAM MUST SET UP
(2) A/D CSR IN BSEL 4, AND 5.
(2) (2) HE MUST CALL THIS ROUTINE:
(2) JSR R5,\$PUTS ;CALL SET UP ROUTINE.
(2) .WORD ADCSR ;ADDR. OF A/D CSR.
(2) ;RETURNS HERE ;KMC BSEL 3,6,7 PERMINENTLY SET UP
(2) ;(UNTILL ONE DOES A RESET)
(2)
(2) (3) THE USER MUST PUT CODE 006 INTO KMC REG 2 TO
(2) START CONVERSION CAUTION*DO WITH MOVB INSTR.!
(2) (4) MONITOR KMC REG 2 FOR CODE 377 (DRLPX2 IS DONE)
(2) (5) READ KMC REG 4,5 FOR A/D RESULT.
(2) (6) TO TAKE MORE SAMPLES, SIMPLY PUT A/D CSR INTO
(2) BSEL 4,5 AND CODE 6 INTO BSEL 2.
(2)
(2) 033052 012537 033062 \$PUTS: MOV (5)+,1\$;GET ADDR. OF A/D
(2) 033056 004537 032400 JSR R5,\$INLP
(2) 033062 000000 1\$: .WORD 0
(2) 033064 033160 .WCRD 10\$
(2) 033066 113777 032442 146556 MOVB \$OFS,@KMAD6
(2) 033074 113777 032442 146552 MOVB \$OFS,@KMAD7
(2) 033102 013737 033062 033122 MOV 1\$,2\$
(2) 033110 062737 000002 033122 ADD #2,2\$
(2) 033116 004537 032400 JSR R5,\$INLP
(2) 033122 000000 2\$: .WORD 0
(2) 033124 033160 .WORD 10\$
(2) 033126 113777 032442 146510 MOVB \$OFS,@KMAD3
(2) 033134 152777 000340 146510 BISB #340,@KMAD6
(2) 033142 152777 000300 146504 BISB #300,@KMAD7
(2) 033150 152777 000300 146466 BISB #300,@KMAD5
(2) 033156 000205 RTS R5
(2) 033160 000000 10\$: .WORD 0
(2)
3806
3807 042000 .=42000
3808
3809 043000 .=43000 ;HERE RESIDES THE MICRO-CODE USED BY THE PROGRAM
3810
3811
3812 000001 .END ;FREE LOCATION AFTER THE MICRO-CODE

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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0186

ABASE = 170404	1221#	1279													
ABR 001326	1279#	1462*	1518	1548	1549	1576	1577	1778	1797	1825	1853	2040	2092		
	2150	2202	2281	2282	2283	2284	2285	2286	2304	2350	2356	2391	2431		
	2548	2549	2593	2594	2618	2672	2685	2735	3084	3148	3258	3259	3260		
	3261	3520	3615	3788											
ACDW1 = 000000	1279														
ACDW2 = 000000C	1279														
ACPUOP= 000000	1279														
ACR 001330	1279#	1464*	1518	1801	1826	1854	2052	2109	2219	2281	2282	2283	2284		
	2285	2286	2312	2360	2437	2593	2594	2622	2699	2742	2987	3096	3155		
	3258	3259	3260	3261	3527	3789	3796	3797							
ADDW0 = 000000	1279														
ADDW1 = 000000	1279														
ADDW10= 000000	1279														
ADDW11= 000000	1279														
ADDW12= 000000	1279														
ADDW13= 000000	1279														
ADDW14= 000000	1279														
ADDW15= 000000	1279														
ADDW2 = 000000	1279														
ADDW3 = 000000	1279														
ADDW4 = 000000	1279														
ADDW5 = 000000	1279														
ADDW6 = 000000	1279														
ADDW7 = 000000	1279														
ADDW8 = 000000	1279														
ADDW9 = 000000	1279														
ADEVCT= 000000	1279														
ADEVM = 000000	1279														
AENV = 000000	1279														
AENVM = 000000	1279														
AFATAL= 000000	1279														
AMADR1= 000000	1279														
AMADR2= 000000	1279														
AMADR3= 000000	1279														
AMADR4= 000000	1279														
AMAMS1= 000000	1279														
AMAMS2= 000000	1279														
AMAMS3= 000000	1279														
AMAMS4= 000000	1279														
AMSGAD= 000000	1279														
AMSGLG= 000000	1279														
AMSGTY= 000000	1279														
AMTYP1= 000000	1279														
AMTYP2= 000000	1279														
AMTYP3= 000000	1279														
AMTYP4= 000000	1279														
APASS = 000000	1279														
APRIOR= 000006	1223#	1279													
APRITY 001350	1279#	1480													
APTCSU= 000040	3744	3745#													
APTENV= 000001	3738	3744	3745#												
APTSIZ= 000200	1444	3745#													
APTSPO= 000100	3744	3745#													
ASR 001324	1279#	1450*	1460	1518	1609	1610	1620	1778	1796	1820	1844	1971	1972		
	1976	1979	2004	2005	2007	2008	2020	2039	2046	2047	2049	2091	2099		

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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0187

2102	2104	2148	2154	2155	2157	2160	2170	2194	2204	2205	2207	2210
2281	2282	2283	2284	2285	2286	2303	2306	2316	2349	2352	2389	2393
2394	2396	2397	2429	2433	2434	2436	2474	2481	2482	2484	2486	2548
2549	2593	2594	2616	2619	2621	2670	2676	2677	2679	2731	2737	2745
2754	2791	2793	2834	2855	2857	2905	2913	2915	2949	2976	2980	3048
3049	3050	3051	3052	3053	3082	3092	3093	3095	3146	3149	3151	3258
3259	3260	3261	3362	3363	3364	3365	3458	3466	3469	3472	3509	3522
3523	3525	3564	3567	3569	3580	3612	3619	3622	3632	3665	3670	3687
3787	3794											
ASWREG= 000000		1279										
ATESTN= 000000		1279										
AUNIT = 000000		1279										
AUSWR = 000000		1279										
AVECP2 001342		1279#	1474*									
AVECT 001340		1279#	1472									
AVECT1= 000344		1222#	1279	1439								
AVECT2= 000000		1279										
BBR 001334		1279#	1468*	1518	1660	1661	1778	1882	1909	1937	2784	2843
		2978	3048	3049	3050	3051	3052	3053	3086	3362	3363	3364
		3791										
BCR 001336		1279#	1470*	1518	1886	1912	1940	2794	2861	2925	2958	3048
		3051	3052	3053	3362	3363	3364	3365	3792	3798	3799	3049
BIT0 = 000001		1220#	1778	2789	3145							
BIT00 = 000001		1220#	2009	2211	2398							
BIT01 = 000002		1220#										
BIT02 = 000004		1220#										
BIT03 = 000010		1220#										
BIT04 = 000020		1220#										
BIT05 = 000040		1220#	2161	2281	2282	2283	2284	2285	2286	2317	3623	
BIT06 = 000100		1220#										
BIT07 = 000200		1220#	2171	2487	3678							
BIT08 = 000400		1220#	3741									
BIT09 = 001000		1220#	3738	3741								
BIT1 = 000002		1220#	1778	2789	3805							
BIT10 = 002000		1220#	1778	2483	2548	2549	2593	2594	2620	3468	3738	
BIT11 = 004000		1220#	1778	2732	2779	2792	2836	2856	2914	3094	3258	3259
		3362	3363	3364	3365	3805						
BIT12 = 010000		1220#	1778	1975	2006	2048	2103	2156	2206	2395	2435	2678
		3568										
BIT13 = 020000		1220#	1778	2003	3482	3536	3588	3641	3696	3738		
BIT14 = 040000		1220#	1778	2123	2875	3741	3805					
BIT15 = 100000		1220#	1778	3473	3805							
BIT2 = 000004		1220#	1778									
BIT3 = 000010		1220#	1778									
BIT4 = 000020		1220#	1778	3805								
BIT5 = 000040		1220#	1778	2789	3362	3363	3364	3365	3805			
BIT6 = 000100		1220#	1778									
BIT7 = 000200		1220#	1778									
BIT8 = 000400		1220#	1778	3521								
BIT9 = 001000		1220#	1778	3521	3568							
BPRITY 001352		1279#	1480*									
BPTVEC= 000014		1220#										
BSR 001332		1279#	1466*	1518	1635	1636	1778	1881	1902	1930	2346	2470
		2669	2674	2713	2733	2780	2788	2790	2837	2848	2850	2906
		2916	2950	2977	3048	3049	3050	3051	3052	3053	3083	3088
		3259	3260	3261	3362	3363	3364	3365	3458	3467	3509	3564

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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0188

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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0189

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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0190

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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0191

TST12	003354	1778#
TST120	014600	2651#
TST121	015016	2724#
TST122	015164	2776#
TST123	015314	2827#
TST124	015522	2893#
TST125	015712	2943#
TST126	016006	2968#
TST127	016106	3048#
TST13	003454	1778#
TST130	016226	3049#
TST131	016346	3050#
TST132	016466	3051#
TST133	016606	3052#
TST134	016726	3053#
TST135	017046	3064#
TST136	017240	3136#
TST137	017352	3258#
TST14	003554	1778#
TST140	017642	3259#
TST141	020132	3260#
TST142	020422	3261#
TST143	020712	3362#
TST144	021216	3363#
TST145	021522	3364#
TST146	022026	3365#
TST15	003654	1778#
TST16	003754	1778#
TST17	004054	1778#
TST2	002602	1542#
TST20	004154	1778#
TST21	004254	1778#
TST22	004354	1778#
TST23	004454	1778#
TST24	004554	1778#
TST25	004654	1778#
TST26	004754	1778#
TST27	005054	1778#
TST3	002642	1571#
TST30	005154	1778#
TST31	005254	1778#
TST32	005354	1778#
TST33	005454	1778#
TST34	005554	1778#
TST35	005654	1778#
TST36	005754	1778#
TST37	006054	1778#
TST4	002700	1604#
TST40	006154	1778#
TST41	006254	1778#
TST42	006354	1778#
TST43	006454	1778#
TST44	006554	1778#
TST45	006654	1778#
TST46	006754	1778#
TST47	007054	1778#

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CROSS REFERENCE TABLE -- USER SYMBOLS

SEA 0192

LPA-KW11K DIAGNOSTIC MD-11-CRLPG-C
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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0193

LPA-KW11K DIAGNOSTIC MD-11-CRLPG-C
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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0194

LPA-KW11K DIAGNOSTIC MD-11-CRLPG-C
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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0195

LPA-KW11K DIAGNOSTIC MD-11-CRLPG-C
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CROSS REFERENCE TABLE -- USER SYMBOLS

SEA 0196

LPA-KW11K DIAGNOSTIC MD-11-CRLPG-C
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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0197

\$UTK	032656	3805#
\$VECT1	001250	1279#
\$VECT2	001252	1279#
\$XTSTR	025074	3741#
\$\$GET4=	000000	3395#
\$OFILL	024277	3737#*
\$40CAT=	***** U	3738 3741
	= 043000	1209# 1210# 1275# 1276# 1277# 1279# 1439# 1444 1448# 3395 3482# 3536# 3588#
		3641# 3696# 3710# 3738 3739# 3740# 3741 3743# 3744 3745# 3746 3785# 3805#
		3807# 3809#
.DVLS	001664	1439# 1454* 1482* 3457* 3508* 3563* 3611* 3664* 3805*
.SASTA=	***** U	3745
.SX	= 001000	1277#

LPA-KW11K DIAGNOSTIC MD-11-CRLPG-C
CRLPG.C.P11 18-AUG-80 09:15

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CROSS REFERENCE TABLE -- MACRO NAMES

SEQ 0198

ADTST	1493#	1518												
AREPT	3263#													
BREPT	3367#													
BRTM	2997#	3048	3049	3050	3051	3052	3053							
CADT	3169#	3258	3259	3260	3261									
CADTB	3288#	3362	3363	3364	3365									
CBC	1778#													
CBTC	2558#	2593	2594											
CBT25	2494#	2548	2549											
COMMEN	1220#	1554	1557	1581	1584	1613	1617	1640	1644	1665	1669	1778	1805	1809
	1837	1860	1865	1890	1894	1918	1923	1946	1951	1983	1987	2012	2017	2056
	2114	2118	2163	2166	2174	2179	2213	2216	2223	2231	2281	2282	2283	2284
	2286	2321	2326	2363	2367	2400	2403	2440	2452	2489	2491	2548	2549	2593
	2625	2628	2688	2695	2704	2710	2748	2751	2797	2810	2865	2869	2919	2922
	2932	2962	2965	2990	2994	3048	3049	3050	3051	3052	3053	3100	3111	3159
	3258	3259	3260	3261	3362	3363	3364	3365	3476	3480	3531	3534	3583	3586
	3639	3690	3694	3724	3730									3635
CSRDAT	1680#	1778												
DFC	1280#	1290	1297	1304	1311	1318	1325	1332	1340	1347	1354	1368	1375	1382
	1403	1410	1417	1424	1431	1438								1396
E CALL	1717#	1778												
ECB	1254#	1554	1557	1581	1584	1613	1617	1640	1644	1665	1669	1778	1805	1809
	1837	1860	1865	1890	1894	1918	1923	1946	1951	1983	1987	2012	2017	2056
	2114	2118	2163	2166	2174	2179	2213	2216	2223	2231	2281	2282	2283	2284
	2286	2321	2326	2363	2367	2400	2403	2440	2452	2489	2491	2548	2549	2593
	2625	2628	2688	2695	2704	2710	2748	2751	2797	2810	2865	2869	2919	2922
	2932	2962	2965	2990	2994	3048	3049	3050	3051	3052	3053	3100	3111	3159
	3258	3259	3260	3261	3362	3363	3364	3365	3476	3480	3531	3534	3583	3586
	3639	3690	3694	3724	3730									3635
ENDCOM	1220#	1554	1557	1581	1584	1613	1617	1640	1644	1665	1669	1778	1805	1809
	1837	1860	1865	1890	1894	1918	1923	1946	1951	1983	1987	2012	2017	2056
	2114	2118	2163	2166	2174	2179	2213	2216	2223	2231	2281	2282	2283	2284
	2286	2321	2326	2363	2367	2400	2403	2440	2452	2489	2491	2548	2549	2593
	2625	2628	2688	2695	2704	2710	2748	2751	2797	2810	2865	2869	2919	2922
	2932	2962	2965	2990	2994	3048	3049	3050	3051	3052	3053	3100	3111	3159
	3258	3259	3260	3261	3362	3363	3364	3365	3476	3480	3531	3534	3583	3586
	3639	3690	3694	3724	3730									3635
ERROR	1220#	1555	1582	1614	1641	1666	1778	1806	1833	1861	1891	1919	1947	1984
	2057	2115	2164	2175	2214	2224	2281	2282	2283	2284	2285	2286	2322	2364
	2441	2490	2548	2549	2593	2594	2626	2689	2705	2749	2798	2866	2920	2930
	2991	3048	3049	3050	3051	3052	3053	3101	3161	3258	3259	3260	3261	3362
	3364	3365	3478	3532	3584	3636	3691	3805						3363
ESCAPE	1220#													
GETPRI	1220#													
GETSWR	1220#													
MOVE I	170#	1518	1549	1577	1610	1636	1661	1778	1801	1826	1854	1886	1912	1940
	1979	2005	2008	2047	2052	2102	2109	2155	2160	2170	2205	2210	2219	2281
	2283	2284	2285	2286	2312	2316	2346	2360	2394	2397	2434	2437	2470	2482
	2548	2549	2593	2594	2619	2622	2677	2685	2699	2742	2745	2788	2791	2794
	2861	2913	2916	2925	2958	2987	3048	3049	3050	3051	3052	3053	3093	3096
	3155	3258	3259	3260	3261	3362	3363	3364	3365	3472	3523	3527	3567	3580
	3632	3677	3687	3805										3622
MOVEM	157#	1548	1576	1609	1620	1635	1660	1778	1796	1797	1820	1825	1844	1853
	1882	1902	1909	1930	1937	1971	1976	2004	2007	2020	2039	2040	2046	2049
	2092	2099	2104	2148	2150	2154	2157	2194	2202	2204	2207	2281	2282	2283
	2285	2286	2303	2304	2306	2349	2350	2352	2356	2389	2391	2393	2429	2431

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CROSS REFERENCE TABLE -- MACRO NAMES

SEQ C199

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CROSS REFERENCE TABLE -- MACRO NAMES

SEQ 0200

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CROSS REFERENCE TABLE -- MACRO NAMES

SEQ 0201

.TRMTR 1156#
.UTK 699# 3805
.SACT1 1159# 1275
.SAPTB 1159# 1279#
.SAPTH 1159# 1277
.SAPTY 1159# 3745
.SCATC 1157# 1209
.SCMTA 1157# 1279
.SEOP 1158# 3395
.SERRO 1158# 3738
.SERRT 1158# 3739
.SINLP 652# 3805
.SMMAC 141#
.SOUTL 610# 3805
.SPOWE 1157# 3746
.SRDOC 1156# 1159# 3742
.SREAD 1158# 3743
.SSCOP 1158# 3741
.STLKW 511# 3805
.STOUT 1439# 3805
.STRAP 1156# 3751
.STYPD 1156# 1158# 3740
.STYPE 1158# 3744
.STYPO 1157# 3737

. ABS. 043000 000 CON RW ABS LCL I
000000 001 CON RW REL LCL I

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

CRLPGC,CRLPGC/CRF=CRLPAB.MAC,CRLPGC.P11
RUN-TIME: 42 36 1 SECONDS
RUN-TIME RATIO: 390/80=4.8
CORE USED: 42K (83 PAGES)

DRLPX2(IMAGE) MICRO CODE
CRLPX2.P11 02-NOV-79 11:22

H 16
;DEFAULT TITLE MACY11 30G(1063) 24-OCT-80 09:45 PAGE 1

SEQ 0202

1 ;THIS FILE IS THE SAME AS "CRLPX0.P11" EXCEPT IT IS LOADED INTO 65000
2 ;IT IS ALSO THE SAME AS "DRLPX2.P11" EXCEPT NAME CHANGE "CRLPX2.P11"
3
4
5 .LIST MC,BIN,BEX,MEB
6 .NLIST MD,CND,ME
7
8 177777
9 :
10 : ADDRESS=-1
11 : MACRO DEFINITIONS FOR M8200 AND M8204 MICRO-PROCESSOR
12 : INSTRUCTION SET.
13 : TO BE USED WITH RSX MACRO-11 ASSEMBLER
14 :
15 : 26-MAY-1976
16 \$BEGIN
17 \$LOC 42000
18 .GLOBL DRLPX2
19 .ENABL GBL
20 :
21 :*
22 :*MICRO CODE FOR KMC-11
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52 000000'
53 000000
54
55
56
57
58

```

460                                ;*THIS CODE WILL BE DOWN LOADED INTO BOTH
461                                ;*KMC-11'S. THE CODE RUNS ASYNCHRONOUS TO THE PDP-11 CODE
462                                ;*WE SYNC THROUGH COMMANDS PASSED VIA THE OUT*/IBUS* REGS.
463                                ;*
464
465
466 042000 DRLPX2: JUMP TABLE USED FOR COMMANDS
467 042000   BR STARTU      ;GOTO START
468 042000   .WORD $SS.
469 042002   BR CMNOP       ;NOP=1
470 042002   .WORD $SS.
471 042004   BR RDSILO      ;=2 READ SILO PUT IN BSEL4
472 042004   .WORD $SS.
473 042006   BR WRSILO      ;=3 READ BSEL4 PUT IN SILO.
474 042006   .WORD $SS.
475 042010   BR RDCMND      ;=4 READ FAST PATH PUT IN BSEL4
476 042010   .WORD $SS.
477 042012   BR WRCMND      ;=5 READ BSEL4, PUT IN FAST PATH.
478 042012   .WORD $SS.
479 042014   BR SAMP        ;=6 TAKE AN A/D SAMPLE
480 042014   .WORD $SS.
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495

:START OF U CODED

STARTU:
MOVE # 0,BREG
.WORD $SS.
MOVE BREG,OUT1 <0> ;CLEAR UNIBUS CSRS
.WORD $SS.
MOVE BREG,OUT1 <2>
.WORD $SS.
MOVE BREG,OUT1 <3>
.WORD $SS.
MOVE BREG,OUT1 <4>
.WORD $SS.
MOVE BREG,OUT1 <5>
.WORD $SS.
MOVE BREG,OUT1 <6>
.WORD $SS.
MOVE BREG,OUT1 <7>
.WORD $SS.
MOVE BREG,SPAD <6>
.WORD $SS.

CMNOP: MOVE INPO <12>,OUT1 <0> ;READ STATUS
.WORD $SS.
MOVE # 377,BREG
.WORD $SS.
MOVE BREG,OUT1 <2> ;INDICATE READY FOR COMMAND.
.WORD $SS.

LOOP:  MOVE INPO <12>,OUT1 <0> ;READ STATUS
.WORD $SS.
MOVE INP1 <2>,SPAD <0> ;READ COMMAND REG.

```

DRLPX2(IMAGE) MICRO CODE
CRLPX2.P11 02-NOV-79 11:22

:DEFAULT TITLE MACY11 30G(1063) J 16
24-OCT-80 09:45 PAGE 2-1

SEQ 0204

(3) 042050 123040 .WORD \$\$\$.
496 042052 BZ LOOP ;NO COMMAND THEN LOOP
(2) 042052 101423 .WORD \$\$\$.
497
498 042054 MOVE INP1 <2>,SPAD <0> ;RE-READ COMMAND.
(3) 042054 123040 .WORD \$\$\$.
499
500 042056 BR SPAD <0> ;BR BASED ON CMND.
(2) 042056 160600 .WORD \$\$\$.
501 ;NO-USER PROTECTION OFFERED.
502 ;IF YOU ENTER WRONG CODE -
503 ;YOU LOSE.
504
505
506 ;ROUTINE TO READ THE SILO, PUT IN
507 ;*BUS REG 4
508 ;CMD=2
509
510 042060 RDSILO: MOVE INP0 <10>,OUT1 <4> ;READ SILO.
(3) 042060 021204 .WORD \$\$\$.
511 042062 BR CMNOP ;WRITE *BUS
(2) 042062 100420 .WORD \$\$\$.;RETURN.
513
514
515 ;ROUTINE TO WRITE SILO, READ DATA FROM
516 ;*BUS REG 4
517 ;CMD=3
518
519
520 042064 WRSILO: MOVE INP1 <4>,OUT0 <10> ;READ DATA IN *BUS
(3) 042064 122110 .WORD \$\$\$.;WRITE SILO.
521 042066 BR CMNOP
(2) 042066 100420 .WORD \$\$\$.
523
524
525 ;ROUTINE TO READ FAST PATH (CMND) REG.
526 ;PUT IN *BUS REG 4
527 ;CMD=4
528
529
530 042070 RDCMND: MOVE INP0 <11>,OUT1 <4> ;READ FAST PATH
(3) 042070 021224 .WORD \$\$\$.
531 042072 BR CMNOP ;WRITE *BUS.
(2) 042072 100420 .WORD \$\$\$.;RETURN
533
534
535 ;ROUTINE TO WRITE FAST PATH (CMND) REG.
536 ;TAKE DATA FROM *BUS REG 4.
537 ;CMD=5
538
539
540 042074 WRCMND: MOVE INP1 <4>,OUT0 <11> ;READ DATA IN *BUS
(3) 042074 122111 .WORD \$\$\$.

```

541          BR      CMNOP      :WRITE INTO FAST PATH.
542 042076   .WORD  .SSS.      :RETURN.
(2) 042076  100420

543
544
545
546          ;THIS ROUTINE TAKES AN A/D SAMPLE.
547          ;CALL= CMND 6 IN BSEL2
548          ;THESE REGS. MUST BE SET UP IN ADVANCE.
549          ;BSEL 3 MUST CONTAIN READ CODE FOR A/D BUFFER.
550          ;BSEL 4,5 MUST CONTAIN A/D CSR SETTING.
551          ;BSEL 6 MUST CONTAIN WRITE CODE FOR A/D CSR
552          ;BSEL 7 MUST CONTAIN READ CODE FOR A/D CSR
553          ; BSEL 3,6,7 WILL REMAIN UNEFFECTED.
554          ; BSEL 4,5 WILL CONTAIN A/D SAMPLE.
555          ;BSEL2 WILL CONTAIN CODE 377 WHEN DONE.
556
557 042100   WTMC  SAMP
(4) 042100  020640   .WORD  .SSS.
(3) 042102  103040   .WORD  .SSS.
568 042104   MOVE   INP1 <6>,OUT0 <11>    ;SEND A/D WRITE CODE.
(3) 042104  122151   .WORD  .SSS.
569 042106   WTMC  SAMP1
(4) 042106  020640   .WORD  .SSS.
(3) 042110  103043   .WORD  .SSS.
570 042112   MOVE   INP1 <4>,OUT0 <11>    ;SEND LOW BYTE CSR INFO.
(3) 042112  122111   .WORD  .SSS.
571 042114   WTMC  SAMP2
(4) 042114  020640   .WORD  .SSS.
(3) 042116  103046   .WORD  .SSS.
572 042120   MOVE   INP1 <5>,OUT0 <11>    ;SEND HIGH BYTE CSR INFO.
(5) 042120  122131   .WORD  .SSS.
573 042122   WTMC  SLOOP
(4) 042122  020640   .WORD  .SSS.
(3) 042124  103051   .WORD  .SSS.
574 042126   MOVE   INP1 <7>,OUT0 <11>    ;SEND READ CODE TO GET A/D CSR.
(3) 042126  122171   .WORD  .SSS.
575 042130   WTMC  SAMP3
(4) 042130  020640   .WORD  .SSS.
(3) 042132  103054   .WORD  .SSS.
576 042134   WTMM  SLOOP1
(4) 042134  020640   .WORD  .SSS.
(4) 042136  061620   .WORD  .SSS.
(3) 042140  103056   .WORD  .SSS.
577 042142   MOVE   INPO <11>,BREG
(3) 042142  020620   .WORD  .SSS.
578 042144   MOVE   BREG,SPAD <0>
(3) 042144  063220   .WORD  .SSS.
579 042146   WTMM  SLOOP2
(4) 042146  020640   .WORD  .SSS.
(4) 042150  061620   .WORD  .SSS.
(3) 042152  103063   .WORD  .SSS.
580 042154   MOVE   INPO <11>,BREG
(3) 042154  020620   .WORD  .SSS.
581 042156   BB7   CMNOP      ;ABORT IF A/D BIT 15=1

```

DRLPX2(IMAGE) MICRO CODE
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SEQ 0206

(2)	042156	103420	.WORD	\$\$\$.	
582	042160		MOVE	SPAD <0>,BREG	
(3)	042160	060600	.WORD	\$\$\$.	
583	042162		BB7	LOPE	
(2)	042162	103473	.WORD	\$\$\$.	
584	042164		BR	SLOOP	:IF A/D NOT DONE, EXIT.
(2)	042164	100451	.WORD	\$\$\$.	
585	042166		LOPE:	MOVE INP1 <3>,OUT0 <11>	;ISSUE READ A/B BUFFER.
(3)	042166	122071	.WORD	\$\$\$.	
586	042170		WTMM	SLOOP3	
(4)	042170	020640	.WORD	\$\$\$.	
(4)	042172	061620	.WORD	\$\$\$.	
(3)	042174	103074	.WORD	\$\$\$.	
587	042176		MOVE	INPO <11>,OUT1 <4>	
(3)	042176	021224	.WORD	\$\$\$.	
588	042200		WTMM	SLOOP4	
(4)	042200	020640	.WORD	\$\$\$.	
(4)	042202	061620	.WORD	\$\$\$.	
(3)	042204	103100	.WORD	\$\$\$.	
589	042206		MOVE	INPO <11>,OUT1 <5>	
(3)	042206	021225	.WORD	\$\$\$.	
590	042210		BR	CMNOP	
(2)	042210	100420	.WORD	\$\$\$.	
591	042212	177777	.WORD	-1	
592		000001	.END		

DRLPX2(IMAGE) MICRO CODE
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SYMBOL TABLE

SEQ 0207

ADDRES= 177777	SAMP 042100	.ADDWC= 000020	.DMEM = 002400	.SELB = 000220
CLK = 000020	SAMP1 042106	.AND = 000260	.DNOP = 000000	.SIMM = 000000
CMNOP 042040	SAMP2 042114	.BB0 = 002000	.DOUT0= 002000	.SINO = 020000
DRLPX2 042000 G	SAMP3 042130	.BB1 = 002400	.DOUT1= 001000	.SIN1 = 120000
LOOP 042046	SLOOP 042122	.BB4 = 003000	.DSPAD= 003000	.SMEM = 040000
LOPE 042166	SLOOP1 042134	.BB7 = 003400	.DSPBR= 003400	.SUB = 000340
MARHLD= 000000	SLOOP2 042146	.BC = 001000	.DO = 000400	.SUBWC= 000040
MARINC= 014000	SLOOP3 042170	.BR = 000400	.FO = 000020	.SUB2C= 000360
MARLD = 010000	SLOOP4 042200	.BSBRG= 160000	.INC = 000060	.SO = 020000
MARLDX= 004000	STARTU 042016	.BSIMM= 100000	.LORN = 000240	.XOR = 000320
PAGE0 = 000000	WRCMND 042074	.BSMEM= 140000	.MINUS= 000360	\$.SS\$. = 100420
PAGE1 = 001000	WRSILO 042064	.BZ = 001400	.MO = 004000	.LOC = 042040
PAGE2 = 002000	\$\$\$\$ER= 000001	.CO = 000400	.OR = 000300	.2A = 000120
PAGE3 = 003000	.	.DBR = 000400	.PLUS = 000000	.2AWC = 000140
RDCMND 042070	.ADC = 000100	.DBRSH= 001400	.SBREG= 060000	
RDSILO 042060	.ADD = 000000	.DEC = 000160	.SELA = 000200	
. ABS. 042214	000 OVR RW ABS LCL D			
000000 001 CON RW ABS LCL I				
ABCODE 004000 002 CON RW REL LCL I				

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

CRLPX2,CRLPX2=CRLPX2
RUN-TIME: 3 3 0 SECONDS
RUN-TIME RATIO: 49/7=6.5
CORE USED: 42K (83 PAGES)