

# LPA11,KW11K

LPA/KW11K DIAG TEST  
CRLPGB0

AH-B038B-MC

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The main body of the document is a microfiche card containing a grid of 10 columns and 20 rows of data. Each cell in the grid contains a small, high-contrast image or text fragment, likely representing a specific test result or component status. The data is organized into a structured table format, with some cells containing graphical representations of waveforms or data plots. The overall appearance is that of a technical diagnostic report or test log.

Identification  
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'FD 000'

Product Code:	AC-90373-AC
Product Name:	CRLEPGB0 LPA/RW11-R DIAGNOSTIC
Date Revised:	JULY 1979
Maintainer:	DIAGNOSTIC ENGINEERING

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1.0 ABSTRACT

\*\*\*\*\*

'B' VERSION OF THE PROGRAM FIXES LS210 THRU LS230 PROGRAM BUGS AND SEVERAL DOCUMENTATION ERRORS.

This program allows the user to check out or debug the KW11K, DUAL REAL TIME CLOCK. The logic test is self contained and needs no external maintenance hardware or operator intervention.

Five special tests are included within this program to allow the user to check out and debug the external I/O signals. To run these tests a jumper wires is needed in order to loop output to an input.

THIS PROGRAM IS A MODIFIED VERSION OF 'MD-11-DZKWK-A'. IT WAS MODIFIED TO ENABLE THE OPERATOR TO CHECK OUT THE KW11K OPTION WHEN IT IS ON THE LPA11-KX I/O BUS. NO RECABLING IS NEEDED. SOME TEST DONE IN THE ORIGINAL DIAGNOSTIC SUCH AS ARBITRATION TEST, WERE DELETED AS THEY COULD NOT BE CHECKED. IF THIS DIAGNOSTIC DOESN'T FIND A SUSPECTED PROBLEM, YOU MAY HAVE TO RUN 'MD-11-DZKWK-A'. YOU SHOULD RUN 'MD-11-DRLPA' BEFORE RUNNING THIS DIAGNOSTIC. PLEASE READ SECTION 10.

## 2.0 REQUIREMENTS \*\*\*\*\*

### 2.1 Equipment

1. PDP11<sup>00</sup>FAMILY COMPUTER with 16K of memory or more and I/O facilities (switch register or TTY).
2. KW11K under test installed in the LPA-11KX.
3. For external I/O signal tests a loopback wire (Jumper) is needed. Jumpers are 30 AWG jumper type 915.
4. LPA11-KX

### 2.2 Storage

This program occupies and uses only the lower 16K of memory.

3.1 Method

Standards procedure for normal binary tapes should be followed.

1. Absolute loader must be in memory.
2. Place binary tape in reader.
3. Load address \*7500 (\* determined by location of loader).
4. Press 'Start' (program will be loaded into memory).

The program can also be loaded by XXDP, ACT, or APT.

3.2 Non-Standard Address, Vector, or Priority; or Use of Software Switch Register

This program is set to test a KW1K with a standard address, vector, and priority. If any of these are different on the KW1K you are testing, change the corresponding location in memory before starting this test.

LOCATION	TAG	CURRENT CONTENTS	COMMENTS
1254	\$BASE:	170404	::Base address of equipment :: under test
1250	\$VECT1:	000344	:: INTERRUPT Vector #1
1252	\$PRIOR:	000006	:: Bus priority - 1,#2
176	\$SWREG:	000000	:: Manual SWR.
	\$TPFLG:	.BYTE 0	:: 'Terminal Available' : Flag (Bit<0:7>-0=Yes)

NOTE

If no hardware Switch Register exists, you may set any bit in 'SWREG' as you would have set it in the SWR.

#### 4.0 STARTING PROCEDURE \*\*\*\*\*

##### 4.1 Control Switch Settings

Starting at memory locations 200, 204, 210, 214, 220, 224, 230 or 234, set all switches as desired. See Section 5.1.

##### 4.2 Starting Addresses

200	Start address for logic test.
204	Restart address for logic test.
210	Start address for 'STP2 OUT', 'SCHMITT TRIG 1' tests.
214	Start address for 'STP1 OUT', 'SCHMITT TRIG 2' tests.
220	Start address for 'SCHMITT TRIG 3 IN', 'ST3 OUT' tests.
224	Starting address for 'A EVENT OUT' test.
230	Starting address for 'B EVENT OUT' test.
234	Starting address for 'USER LINK' loop.

##### 4.3 Program AND/OR Operator Action

1. Load program into core.
2. Set switch register to starting address.
3. Load address.
4. Set switches to desired settings - see section 5.1.
5. IF starting a special I/O signal test:  
MAKE WIRE LOOP CONNECTION.
6. Press Start.

## 5.0 OPERATING PROCEDURE \*\*\*\*\*

### 5.1 Switch Register Function

#### Switch use -----

15 Halt on error  
 14 Loop on test  
 13 Inhibit error typeout (all tests)  
 13 Inhibit '\*' typeout (special I/O signal tests)  
 11 Inhibit iterations (short pass)  
 10 Bell on error  
 9 Loop on error  
 8 Loop on test in SWR <7:0>

### 5.2 Scope Loops

If an error occurs and the user wishes to scope the error, he (or she) should set SW15-1 to halt on error, then when the program halts on error, SW15=0, set SW14=1. To loop on current test, set SW13=1 to inhibit error printout, and press continue on the CPU's console.

#### NOTE

For each test in the listing, you will find a test description. In each description a probable SYNC Point is listed. These Points are listed AS A GUIDE in order for you to SYNC your scope to the Signals being generated.

### 5.3 Program AND/OR Operator Action

#### 5.3.1 Logic Test

The first pass through the program will be made with iterations inhibited. Successive passes will enable iterations if SWR1=0. 'END PASS' is printed out at the end of a pass.

If not inhibited by APT, the program will look for more KW11ks to exercise, one pass will exercise all KW11ks.

#### 5.3.2 Special I/O Signal Tests

There are no 'Short Passes'. Each pass will iterate 65,324 times. A '\*' is typed at the end of a pass unless SWR13 1.

## 6.0 ERRORS



\*\*\*\*\*

## 6.1 Error Printout

Printout varies with the error detected. The error PC typed out is the actual location of the error call.

A halt at location '\$TYPE'+10 when running with no terminal indicates an error has occurred. To find out the number of the error, examine location '\$STNM'. This is the item number of the error. To find out what the error typout would have been GOTO to the error pointer table beginning at location '\$ERRTB'.

### 6.1.1 Example

If we examined location '\$STNM' and found a 5 (101) we go to location '\$ERRTB' and look through the error pointer table until we found item 5. The information would look like:

```
;ITEM 5
    EMS           ;CLOCK B SR DATA ERROR
    DHS           ;ERRPC BSR WAS S/B
    DT5           ;$ERRPC,BSR,$BDADR,$GDDR
    DFO           ;ALL NUMBERS ARE IN OCTAL FORM
```

To find out the information specified by DT5 (\$ERRPC,BSR,\$GDDR,\$BDADR) follow these steps:

1. Look up the address of the label (i.e., \$ERRPC) in the symbol table which follows the listing.
2. Put this address in the witch register and depress the load address switch on the processor's console.
3. Now depress the Examine switch.
4. The data displayed in the data lights is the information that would have been printed for this label if you had a input/output terminal.

## 6.2 Non-Standard Error HALTS

A HALT MAY OCCUR IF THE PROGRAM DETECTS AN LPA11-KX ERROR. CHECK THE COMMENTS IN THE LISTING OPPOSITE THE PC HALT.

## 7.0 RESTRICTIONS \*\*\*\*\*

### 7.1

Jumper W2 must be installed if not jumpered on module.  
JUMPER W3, W4, AND W5 MUST BE INSTALLED TO RUN SIGNAL TESTS.

### 7.2

Logic Test must be run before any special I/O Signal Test.

## 8.0 MISCELLANEOUS \*\*\*\*\*

### 8.1

After a power failure occurs, program execution will continue at the point where the power failure occurred after the program types 'POWER'.

### 8.2

This program is chainable under XXDP, ACT, or APT.

### 8.3 Execution Time

#### 8.3.1 Logic Test

90 SECONDS iterations inhibited - no errors.

375 SECONDS with iterations - no errors.

#### 8.3.2 Special I/O Signal Tests

1.0 Minutes No errors, SW13 0.

Execution times are approximate, as the various PDP-11 CPU's have varied instruction execution times.  
Times quoted were taken from a run on a PDP-11/34.

## 8.4 USER LINK TO I/O DEVICE

A SPECIAL USER LINK HAS BEEN PROVIDED IN ORDER FOR THE OPERATOR TO EXAMINE OR MODIFY LOCATIONS ON THE LPA11-KX I/O BUS. (NOTE: THIS CANNOT BE DONE DIRECTLY.)

## PROCEDURE:

- 1) START THE PROCESSOR AT LOCATION 234
- 2) THE DIALOG TO EXAMINE A LOCATION IS AS FOLLOWS:

```
E OR D      'E'  
DEVICE ADDR= 'OCTAL ADDRS'  
XXXXXX
```

WHERE XXXXXX IS THE CONTENTS OF THE SPECIFIED LOC.

- 3) THE DIALOG TO MODIFY A LOCATION IS AS FOLLOWS:

```
E OR D      'D'  
DATA=       'DATA TO BE DEPOSITED''
```

- 4) THE PROGRAM WILL STAY IN THIS LOOP UNTIL THE OPERATOR IS FINISHED. AT THIS TIME THE PROCESSOR SHOULD BE HALTED.

NOTE: THE OPERATORS RESPONSE IS ENCLOSED IN QUOTES.

## 9.0 PROGRAM DESCRIPTION \*\*\*\*\*

### 9.1 Logic Tests

A complete description of each test is included withing the listing before each test.

### 9.2 Special External I/O Signal Tests

#### 9.2.1 LS210 'STP2 OUT' to 'SCHMITT RIG 1 IN' Tests

This is a special section devoted for testing and providing scope loop capabilities for 'STP2 OUT' L and 'SCHMITT TRIG 1' IN.

When you load and start at location 210, program control is transferred here. 'STP2 OUT' L pulses are generated by 'LD STAT A HI' H + 'BD10' H (Main. STP2).

Pin V ('STP2 OUT') is wired to pin LL (SCHMITT TRIG1) for this test. 'STP2 OUT' pulses are received as 'SCHMITT TRIG 1' pulses which set clock A's status register bit 15. If an error is detected, normal error reporting technique, and error switch register options are used. An '\*' is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins V and LL of J1 together.  
Jumper W3 must be INSTALLED.

Logic test (L + S 200) should be run first.

#### 9.2.2 LS214 'STP1 OUT' to 'SCHMITT RIG 2' H Tests

This is a special test section devoted for testing and providing scope loop capabilities for 'STP2 OUT' and 'SCHMITT TRIG2' IN.

When you load and start at location 214, program control is transferred here. 'STP1 OUT' L pulses are generated by 'LD STAT A HI' + 'BD12' H (mIn S ). Pin DD ('STP1 OUT') is wired to pin BB ('SCHMITT TRIG 2') for this test. 'STP1 OUT' pulses are received as 'SCHMITT RIG 2' pulses which will clear clock A's count register if mode 3 is selected. If an error is detected, normal error reporting technique, and error switch register options are used. An '\*' is typed after each 65,324 loops through the test. SW13-1 will inhibit this feature.

You must wire pins DD and BB of J1 together.  
Jumper W4 must be installed.

Logic tests (L + S at 200) should be run first.

## 9.2.3 LS220 'SCHMITT TRIG 3' in, 'ST3 OUT' Tests

This is a special section devoted for testing and providing scope LOOPS CAPABILITIES FOR 'SCHMITT TRIG 3' AND 'ST3 OUT'.

When you load and start at location 220, program control is transferred here. 'STP1' pulses are generated by 'LD STAT A H,' + 'BD12' H (main STP1). Pin dd ('STP1 OUT') is wired to pin T ('SCHMITT RIG 3'). 'SCHMITT TRIG 3' pulses give us 'ST3 OUT' pulses. Pin L ('ST3 OUT') is wired to pin BB ('SCHMITT TRIG2'), and 'SCHMITT TRIG 2' will set clock A's status register bit 7.

If an error is detected, normal error reporting technique, and error switch register options are used. An '\*' is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins DD to T of J1 together, as well as pins L to BB of J1 together. Jumpers W4 and W5 must also be installed.

Tests LS210 and LS214 should be run first.

## 9.2.4 LS224 'A EVENT OUT' Test

This is a special section devoted for testing and providing scope loop capabilities for 'A EVENT OUT'.

When you load and start at location 224, program control is transferred here. 'A EVENT OUT' pulses are generated by clock A overflows. Pin VV ('A EVENT OUT') is wired to pin BB ('SCHMITT TRIG 2'). 'SCHMITT TRIG 2' pulses will set clock A's CSR bit 7. If an error is detected, normal erroporting technique, and error switch register options are used. An '\*' is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins VV and BB of J1 together. Jumper W4 must also be installed.

Test LS210 should be run first.

## 9.2.5 LS230 'B EVENT OUT' Test

This is a special section devoted for testing and providing scope loop capabilities for 'B EVENT OUT'.

When you load and start at location 230, program control is transferred here. 'B EVENT OUT' pulses are generated by clock B overflows. Pin IT ('B EVENT OUT') is wired to pin BB ('SCHMITT TRIG 2'). 'SCHMITT TRIG 2' pulses will set clock A's CSR bit 7. And error switch register options are used. An '\*' is typed after each 65,324 loops through the test. SW13-1 will inhibit this feature.

You must wire pins IT and BB of J1 together. Jumper W4 must be installed also.

Test LS210 should be run first.

## 10.0 LPA11 (SYSTEM) DIAGNOSTIC SUMMARY

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DIAGNOSTICS FOR THE LPA11 ARE WRITTEN AT THREE LEVELS: (1) TOTAL PDP-11 SYSTEM, (2) LPA11 SYSTEM; AND, (3) LPA11 OPTIONS.

LEVEL 1, IS DESIGNED TO ISOLATE A FAILURE TO THE LPA11 SYSTEM. ALL OPTIONS ON THE PDP-11 ARE EXERCISED.

LEVEL 2 DIAGNOSTICS ISOLATE A FAILURE TO THE INDIVIDUAL OPTION WITHIN THE LPA11. THE LEVEL 2 DIAGNOSTIC IS MD-11-DRLPA. WHEN THE USER RUNS DRLPA HE CAN GENERALLY TELL WHICH OPTION DIAGNOSTIC (LEVEL 3) TO RUN NEXT. M8254 AND M8200-YC ERRORS MAY 'LOOK' ALIKE AND DRLPA MAY NOT BE ABLE TO DISTINGUISH BETWEEN THEM. ARBITRATION ERRORS WILL NOT BE DETECTED BY THIS DIAGNOSTIC.

LEVEL THREE DIAGNOSTICS AID IN DETERMINING IF THE ERROR WAS IN FACT ON THE OPTION THE DRLPA SPECIFIED. THE USER MAY 'LOOP' ON THE ERROR. WITHIN LEVEL THREE, THERE ARE TWO GROUPS OF DIAGNOSTICS. THE FIRST GROUP REQUIRES NO 'EXTRA' WORK BY THE USER IN ORDER TO RUN. GROUP 'A' DIAGNOSTICS DO NOT CHECK ARBITRATION, AND REQUIRE EXTRA TIME FOR EXECUTION. THE SECOND GROUP (GROUP 'B') REQUIRES THAT THE USER RECONFIGURE THE PDP-11 SYSTEM. THIS RECONFIGURATION INVOLVES CABLING THE UNIBUS TO THE LPA'S I/O BUS.

THE DIAGNOSTIC FOR THE M8254 FALLS INTO THE GROUP 'B' CATEGORY.

<u>FUNCTION</u>	<u>GROUP</u>	<u>DIAG. #</u>	<u>DIAG. TITLE</u>
LPA11-K	LEVEL 2	MD-11-DRLPA	LPA11-K SYSTEM DIAG.
M8254	'B'	MD-11-DRMBA	M8254 (JPSM) DIAG.
AA11-K	A	MD-11-DRLPB	AA11-K DIAG.
	B	MD-11-DZAAC	AA11-K DIAG.
AR11	A	MD-11-DRLPC	LPA/AR11 DIAG. #1
	A	MD-11-DRLPD	LPA/AR11 DIAG. #2
	A	MD-11-DRLPE	LPA/AR11 DIAG. #3
	B	MD-11-DZARA	AR11 DIAG. #1
	B	MD-11-DZARB	AR11 DIAG. #2
	B	MD-11-DZARC	AR11 DIAG. #3
DR11-K	A	MD-11-CRLPF	LPA/DR11-K DIAG.
	B	MD-11-DZDRG	DR11-K DIAG.
KW11-K	A	MD-11-CRLPG	LPA/KW11-K DIAG.
	B	MD-11-DZKWK	KW11-K DIAG.
LPS11	A	MD-11-DRLPH	LPA/LPS11 DIAG. #1
	A	MD-11-DRLPI	LPA/LPS11 DIAG. #2
	A	MD-11-DRLPJ	LPA/LPS11 DIAG. #3
	B	MD-11-DZLPC	LPS11 DIAG. #1
	B	MD-11-DZLPD	LPS11 DIAG. #2
	B	MD-11-DZLPI	LPS11 DIAG. #3
AD11-K	A	MD-11-CRLPK	LPA/AD11-K DIAG.
	B	MD-11-DZADL	AD11-K DIAG.
M8200-YC	B	MD-11-DZLPL	LPA/M8200-YC BASIC MICRO-CPU R/W TEST
	B	MD-11-DZLPM	LPA/M8200-YC JMP+ROM READ TEST

## THIS IS A HISTORY FILE OF CRLPG-B

-----  
 THE 'A' VERSION HAD SEVERAL PROBLEMS WHEN DEALING WITH LS204 AND LS210 THRU LS230. THE FIRST WAS THAT LS204 FAILED TO CLEAR A LOCATION ".DVLS", WHICH INDICATED THE MICRO-CODE WAS LOADED AND RUNNING <AFTER A RESTART IS IS NOT RUNNING DUE TO 'INIT'>. THIS PROBLEM IS ALSO COMMON TO LS210 THRU LS230. THE SECOND PROBLEM IS THAT LS210 HAD A DESIGN FLAW <REALLY ONLY A ONE LINE TYPING REVERSAL>  
 JAN 1979 R. SHOOP

## HISTORY FILE OF DRLPG-A

-----  
 PRODUCT CODE: MAINDEC-11-DZKWK-A  
 PRODUCT NAME: KW11-K DIAGNOSTIC TEST  
 DATE: FEBRUARY 1976  
 MAINTAINER: DIANOSTIC GROUP

PRODUCT CODE: MAINDEC-11-DRLPG-A  
 PRODUCT NAME: LPA/KW11-K DIAGNOSTIC TEST  
 DATE: JANUARY 1978  
 MAINTAINER: DIAGNOSTIC GROUP

## REASON FOR DEVELOPMENT:

- 1) TO ENABLE THE OPERATOR TO CHECK OUT THE KW11-K OPTION WHEN IT IS ON THE LPA11-KX I/O BUS.

## CHANGES MADE:

- 1) TOOK OUT CERTAIN TESTS FROM ORIGINAL DIAGNOSTIC (I.E. INTERRUPTS, TIME DEPENDENT CODE).
- 2) REPLACED DIRECT LINKS TO DEVICE WITH MACRO CALLS TO THE KMC-11 MICRO CODE. KMC-11 MICRO CODE (FILE:DRLPX2) HANDLES DIRECT COMMUNICATIONS WITH THE DEVICE.

FILE: DRLPA.MAC  
 CONTAINS MACRO LINKS BETWEEN PDP-11 CODE AND KMC-11 MICRO CODE. FILE: DRLPX2 NEEDS TO BE ASSEMBLED WITH DRLPG (SEE .CTL FILE).

FILE: DRLPX2  
 MICRO CODE FILE THAT GETS LOADED INTO THE KMC-11 VIA ROUTINES IN DRLPA.MAC.  
 DRLPX2.P11 IS ASSEMBLED WITH MACY11 (ONLY) AS ANY OTHER .P11 FILE. THE RESULTS OF ITS ASSEMBLY IS A .OBJ MODULE AS WAS THE RESULT OF THE ASSEMBLY OF THE DIAGNOSTIC .P11 FILE. BOTH .OBJ FILES GET LINKED WITH LNKX11 (ONLY).

FILE: DRLPG.CTL  
 THIS FILE EXPLAINS SEQUENCE OF ASSEMBLES AND LINKS. IT IS IN TOPS-20 FORMAT.



2981	OPERATIONAL SWITCH SETTINGS
2982	TRAP CATCHER
2993	BASIC DEFINITIONS
3057	ACT11 HOOKS
3059	APT PARAMETER BLOCK
3061	COMMON TAGS
(2)	APT MAILBOX-ETABLE
(1)	ERROR POINTER TABLE
3224	PROGRAM START
3228	INITIALIZE THE COMMON TAGS
3273	*
3274	* PHASE 1 CLOCKS A+B BASIC LOGIC TESTS.
3275	*
3302	T1 *TEST THE ADDRESSABILITY OF CLOCK ADDRESS
3326	T2 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN INTO
3355	T3 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN TO A ZERO
3388	T4 *TEST THAT CLOCK A'S STATUS CAN BE WRITTEN AND READ
3414	T5 *TEST THAT CLOCK B'S STATUS REGISTER CAN BE WROTE/READ
3439	T6 *TEST THAT CLOCK B'S BUFFER REGISTER CAN BE WROTE/READ
3562	T7 *TEST THAT CLOCK A STATUS REGISTER BIT 15 CAN BE SET AND CLEARED
(5)	T10 *TEST THAT CLOCK A STATUS REGISTER BIT 14 CAN BE SET AND CLEARED
(5)	T11 *TEST THAT CLOCK A STATUS REGISTER BIT 13 CAN BE SET AND CLEARED
(5)	T12 *TEST THAT CLOCK A STATUS REGISTER BIT 9 CAN BE SET AND CLEARED
(5)	T13 *TEST THAT CLOCK A STATUS REGISTER BIT 8 CAN BE SET AND CLEARED
(5)	T14 *TEST THAT CLOCK A STATUS REGISTER BIT 7 CAN BE SET AND CLEARED
(5)	T15 *TEST THAT CLOCK A STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(5)	T16 *TEST THAT CLOCK A STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
(5)	T17 *TEST THAT CLOCK A STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(5)	T20 *TEST THAT CLOCK A STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
(5)	T21 *TEST THAT CLOCK A STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
(5)	T22 *TEST THAT CLOCK A STATUS REGISTER BIT 0 CAN BE SET AND CLEARED
(6)	T23 *TEST THAT CLOCK A BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(6)	T24 *TEST THAT CLOCK A BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(6)	T25 *TEST THAT CLOCK A BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(6)	T26 *TEST THAT CLOCK A BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
(6)	T27 *TEST THAT CLOCK A BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(6)	T30 *TEST THAT CLOCK A BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(6)	T31 *TEST THAT CLOCK A BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
(6)	T32 *TEST THAT CLOCK A BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED
(6)	T33 *TEST THAT CLOCK A BUFFER REGISTER BIT 8 CAN BE SET AND CLEARED
(6)	T34 *TEST THAT CLOCK A BUFFER REGISTER BIT 9 CAN BE SET AND CLEARED
(6)	T35 *TEST THAT CLOCK A BUFFER REGISTER BIT 10 CAN BE SET AND CLEARED
(6)	T36 *TEST THAT CLOCK A BUFFER REGISTER BIT 11 CAN BE SET AND CLEARED
(6)	T37 *TEST THAT CLOCK A BUFFER REGISTER BIT 12 CAN BE SET AND CLEARED
(6)	T40 *TEST THAT CLOCK A BUFFER REGISTER BIT 13 CAN BE SET AND CLEARED
(6)	T41 *TEST THAT CLOCK A BUFFER REGISTER BIT 14 CAN BE SET AND CLEARED
(6)	T42 *TEST THAT CLOCK A BUFFER REGISTER BIT 15 CAN BE SET AND CLEARED
(6)	T43 *TEST THAT CLOCK B STATUS REGISTER BIT 11 CAN BE SET AND CLEARED
(6)	T44 *TEST THAT CLOCK B STATUS REGISTER BIT 7 CAN BE SET AND CLEARED
(6)	T45 *TEST THAT CLOCK B STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(6)	T46 *TEST THAT CLOCK B STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
(6)	T47 *TEST THAT CLOCK B STATUS REGISTER BIT 4 CAN BE SET AND CLEARED
(6)	T50 *TEST THAT CLOCK B STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(6)	T51 *TEST THAT CLOCK B STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
(6)	T52 *TEST THAT CLOCK B STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
(6)	T53 *TEST THAT CLOCK B STATUS REGISTER BIT 0 CAN BE SET AND CLEARED

(6)	T54	*TEST THAT CLOCK B BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(6)	T55	*TEST THAT CLOCK B BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(6)	T56	*TEST THAT CLOCK B BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(6)	T57	*TEST THAT CLOCK B BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
(6)	T60	*TEST THAT CLOCK B BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(6)	T61	*TEST THAT CLOCK B BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(6)	T62	*TEST THAT CLOCK B BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
(6)	T63	*TEST THAT CLOCK B BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED
3563	*	
3564	*	PHASE 2 ADVANCED BASIC LOGIC TESTS
3565	*	
3573	T64	*TEST THAT CLOCK A'S COUNT REGISTER IS CLEAR
3596	T65	*TEST CLOCK A'S COUNT REGISTER WITH 125252 PATTERN
3624	T66	*TEST CLOCK A'S COUNT REGISTER WITH 052525 PATTERN
3658	T67	*TEST THAT CLOCK B'S COUNT REGISTER IS CLEAR
3682	T70	*TEST CLOCK B'S COUNT REGISTER WITH 125 PATTERN
3710	T71	*TEST CLOCK B'S COUNT REGISTER WITH 252 PATTERN
3752	T72	*TEST THE SETTING OF MAINTENANCE STP1 IN CLOCK A BIT 15 TO SET
3782	T73	*TEST THAT BIT00 IN CLOCK A STATUS REG. WILL SET WHEN BIT13 AND MAIN. STP1
3818	T74	*TEST THAT CLOCK A WILL INCREMENT - MODE 0 - RATE STP1 FIRST COUNT TEST
3867	T75	*TEST THE ABILITY OF CLOCK A TO COUNT FROM ZERO TO OVERFLOW USING M STP1'S
3914	*	
3915	*	PHASE 3 CLOCK A COUNT FUNCTION TESTS
3916	*	
3928	T76	*TEST THAT CLOCK A OVERFLOW WILL OCCUR
3974	T77	*TEST IN CLOCK A THAT OVERFLOW IN MODE 0 CAUSE CLEARING OF 'ENB CNTR' F/F
4065	T100	*TEST THE ABILITY OF CLOCK A TO COUNT AT 1MHZ RATE PART 1
4066	T101	*TEST THE ABILITY OF CLOCK A TO COUNT AT 100KHZ RATE PART 1
4067	T102	*TEST THE ABILITY OF CLOCK A TO COUNT AT 10KHZ RATE PART 1
4068	T103	*TEST THE ABILITY OF CLOCK A TO COUNT AT 1KHZ RATE PART 1
4069	T104	*TEST THE ABILITY OF CLOCK A TO COUNT AT 100HZ RATE PART 1
4070	T105	*TEST THE ABILITY OF CLOCK A TO COUNT AT LINE-FREQ RATE PART 1
4081	T106	*TEST THAT CLOCK A DOESN'T COUNT WHEN NO RATE IS SELECTED
4123	T107	*TEST THAT CLOCK A'S COUNT REG ISN'T LOADED WHEN CLOCK A IS ENABLED
4163	T110	*TEST THAT CLOCK A IN MODE 1 DOES NOT CLEAR ENABLE ON OVERFLOW
4202	T111	*TEST THAT A CLOCK A 'BUFFER TO COUNT REG' DOESN'T TAKE PLACE ON A MODE 2 OVERFLOW
4251	T112	*TEST THAT CLOCK A MODE 2 + MAINTENANCE ST2 SET MODE FLG
4332	T113	*TEST THAT PATTERN 052525 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
4333	T114	*TEST THAT PATTERN 125252 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
4377	T115	*TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 1 WHEN STP2 IS GENERATED
4378	T116	*TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 2 WHEN STP2 IS GENERATED
4391	T117	*TEST THAT MODE 3 + 'STP2' CLEARS A'S COUNT REGISTER.
4435	T120	*TEST THE AUTODECREMENT FEATURE OF CLOCK A'S BUFFER
4508	T121	*TEST THAT CLOCK A'S 1 MHZ CLK CAN BE DISABLED
4540	*	
4541	*	PHASE 4 CLOCK B COUNT FUNCTION TESTS
4542	*	
4560	T122	*TEST THAT CLOCK B WILL COUNT ONCE FIRST CLOCK B COUNT
4611	T123	*TEST THE ABILITY IF CLOCK B TO COUNT FROM ZERO TO OVERFLOW
4677	T124	*TEST THAT CLOCK B CAN GENERATE AN OVERFLOW
4727	T125	*TEST THE INIT. ABILITY OF CLOCK B'S COUNT REG.
4752	T126	*TEST THAT CLOCK B DOESN'T COUNT WHEN NO RATE IS SELECTED
4832	T127	*TEST THE ABILITY OF CLOCK B TO COUNT AT 1MHZ PART 1
4833	T130	*TEST THE ABILITY OF CLOCK B TO COUNT AT 100KHZ PART 1
4834	T131	*TEST THE ABILITY OF CLOCK B TO COUNT AT 10KHZ PART 1
4835	T132	*TEST THE ABILITY OF CLOCK B TO COUNT AT 1KHZ PART 1

4836	T133	*TEST THE ABILITY OF CLOCK B TO COUNT AT 100HZ PART 1
4837	T134	*TEST THE ABILITY OF CLOCK B TO COUNT AT LINE-FREQ PART 1
4848	T135	*TEST THE 'FEED B TO A' 24 BIT COUNTER FEATURE OF CLOCKS A + B
4897	*	
4898	*	PHASE 6 CLOCK A+B ADVANCE TESTING
4899	*	
4920	T136	*TEST THAT THE TRAILING EDGE OF STP <sup>1</sup> WILL INCR. COUNTER
5042	T137	*TEST CLOCK A'S 100KHZ DIVIDER
5043	T140	*TEST CLOCK A'S 10KHZ DIVIDER
5044	T141	*TEST CLOCK A'S 1KHZ DIVIDER
5045	T142	*TEST CLOCK A'S 100HZ DIVIDER
5146	T143	*TEST CLOCK B'S 100KHZ DIVIDER
5147	T144	*TEST CLOCK B'S 10KHZ DIVIDER
5148	T145	*TEST CLOCK B'S 1KH7 DIVIDER
5149	T146	*TEST CLOCK B'S 100HZ DIVIDER
5177		
5179		END OF PASS ROUTINE
5180	*	
5181	*	SPECIAL I/O SIGNAL TESTS
5182	*	
5218	*	'STP2 OUT' TO 'SCHMITT TRIG 1 IN' TESTS
5268	;	'STP1 OUT' TO 'SCHMITT TRIG 2' H TESTS
5322	*	'SCHMITT TRIG 3' IN, 'ST3 OUT' TESTS
5374	*	'A EVENT OUT' TEST
5427	*	'B EVENT OUT' TEST
5517		
5518	*	SYSMAC ROUTINES
5519		
5521		BINARY TO OCTAL (ASCII) AND TYPE
5522		ERROR HANDLER ROUTINE
5523		ERROR MESSAGE TIMEOUT ROUTINE
5524		CONVERT BINARY TO DECIMAL AND TYPE ROUTINE
5525		SCOPE HANDLER ROUTINE
5526		READ AN OCTAL NUMBER FROM THE TTY
5527		TTY INPUT ROUTINE
5528		TYPE ROUTINE
5529		APT COMMUNICATIONS ROUTINE
5530		POWER DOWN AND UP ROUTINES
5531		TRAP DECODER
(3)		TRAP TABLE

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.REM [

LPA.MAC

WELCOME, THIS DIAGNOSTIC IS ONE IN A SERIES OF DIAGNOSTIC  
DESIGNED IN ORDER TO AID YOU IN TESTING THE LPA-11XX OPTION.  
I HOPE THAT YOU HAVE READ THE DOCUMENTATION SECTION OF THIS  
DIAGNOSTIC. IF YOU HAVE, YOU KNOW ABOUT ALL OF THE DIAGNOSTICS  
THAT ARE AVAILABLE FOR TESTING THE LPA SYSTEM.

GOOD LUCK .

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.GLOBL DRLPX2

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.REM  
THIS IS A LIST OF TESTS DELETED FROM THIS DIAGNOSTIC.  
THESE TEST COULD NOT BE DONE THROUGH THE LPA-11.  
TEST THE LOW BYTE OPERATION OF CLOCK A'S STATUS REGISTER  
TEST THE HIGH BYTE OPERATION OF A'S STATUS REGISTER  
TEST THE LOW BYTE OPERATION OF B'S STATUS REGISTER  
TEST THE HIGH BYTE OPERATION OF B'S STATUS REGISTER  
TEST THAT INIT CLEARS STATUS REGISTER A  
TEST THAT INIT CLEARS BUFFER REGISTER A  
TEST THAT INIT CLEARS STATUS REGISTER B  
TEST THAT INIT CLEARS BUFFER REGISTER B  
TEST THAT A'S COUNT REGISTER IS CLEARED BY INIT  
TEST THAT CLOCK A WILL INTR. AND TO THE RIGHT VECTOR  
TEST THAT CLOCK A WILL INTR. WHEN CPU PSW = CLK INTR LEV -1  
TEST THAT CLOCK A WILL NOT INTR. WHEN CPU PSW = CLK INTR LEVEL  
TEST THAT ST1 WILL CAUSE CLOCK A TO INTER.  
TEST THAT CLOCK A OVERFLOW WILL CAUSE AN INTR.  
TEST THAT A CLOCK A COUNTER BUFFER WILL CAUSES AN INTR.  
TEST THAT CLOCK B WILL INTR. AND TO THE RIGHT VECTOR  
TEST THAT CLOCK B WILL INTR. WHEN CPU PSW=CLK INTR LEV -1  
TEST THAT CLOCK B WILL NOT INTR. WHEN CPU PSW=CLK INTR LEVEL  
TEST THAT A CLOCKB OVERFLOW WILL CAUSE AN INTR.  
TEST CLOCK A'S REPEATIBILITY AT 1MHZ RATE  
TEST CLOCK A'S REPEATIBILITY AT 100KHZ RATE  
TEST CLOCK A'S REPEATIBILITY AT 10KHZ RATE  
TEST CLOCK A'S REPEATIBILITY AT 1KHZ RATE  
TEST CLOCK A'S REPEATIBILITY AT 100HZ RATE  
TEST CLOCK B'S REPEATIBILITY AT 1MHZ RATE  
TEST CLOCK B'S REPEATIBILITY AT 100KHZ RATE  
TEST CLOCK B'S REPEATIBILITY AT 10KHZ RATE  
TEST CLOCK B'S REPEATIBILITY AT 1KHZ RATE  
TEST CLOCK B'S REPEATIBILITY AT 100HZ RATE  
TEST THAT "INIT" CLEARS B'S 100KHZ DIVIDE BY 10 CHIPS

.TITLE LPA-KW11K DIAGNOSTIC MD-11-CRLPG-B  
:\*COPYRIGHT (C) 1978  
:\*DIGITAL EQUIPMENT CORP.  
:\*MAYNARD, MASS. 01754  
:\*  
:\*PROGRAM BY EDWARD C. BADGER REV B BY R. SHOOP  
:\*  
:\*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC  
:\*PACKAGE (MAINDEC-11-DZQAC-C3), JAN 19, 1977.  
:\*

\$TN 1  
.SBTTL OPERATIONAL SWITCH SETTINGS  
:\*  
:\* SWITCH USE  
:\*-----  
:\* 15 HALT ON ERROR  
:\* 14 LOOP ON TEST  
:\* 13 INHIBIT ERROR TYPEOUTS

```

(1)          :*          11          INHIBIT ITERATIONS
(1)          :*          10          BELL ON ERROR
(1)          :*          9           LOOP ON ERROR
(1)          :*          8           LOOP ON TEST IN SWR<7:0>
2982         .SBTTL TRAP CATCHER
(1)          :
(1)          :          .=0
(1)          :          ;*ALL UNUSED LOCATIONS FROM 4 - 776 CONTAIN A '+2,HALT'
(1)          :          ;*SEQUENCE TO CATCH ILLEGAL TRAPS AND INTERRUPTS
(1)          :          ;*LOCATION 0 CONTAINS 0 TO CATCH IMPROPERLY LOADED VECTORS
(1)          :          :          .=174
(1)          000174 000174          DISPREG: .WORD 0          ;;SOFTWARE DISPLAY REGISTER
(1)          000176 000000          SWREG:   .WORD 0          ;;SOFTWARE SWITCH REGISTER
2983         000200 000200          :          .-200
2984         000200 000137 001730          JMP      @#START          ;GO TO STARTING ADDRESS OF PROGRAM
2985         :
2986         000204 000137 002436          JMP      @#RSTART          ;GO TO RESTART ADDRESS.
2987         000210 000137 023410          JMP      @#LS210          ;GO TO SPECIAL TEST #1.
2988         000214 000137 023606          JMP      @#LS214          ;GO TO SPECIAL TEST #2.
2989         000220 000137 024022          JMP      @#LS220          ;GO TO SPECIAL TEST #3.
2990         000224 000137 024206          JMP      @#LS224          ;GO TO SPECIAL TEST #4.
2991         000230 000137 024414          JMP      @#LS230          ;GO TO SPECIAL TEST #5.
2992         :
2993         .SBTTL BASIC DEFINITIONS
(1)          :
(1)          :          ;*INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***
(1)          001100          STACK= 1100
(1)          :          .EQUIV EMT,ERROR          ;;BASIC DEFINITION OF ERROR CALL
(1)          :          .EQUIV IOT,SCOPE          ;;BASIC DEFINITION OF SCOPE CALL
(1)          :
(1)          :          ;*MISCELLANEOUS DEFINITIONS
(1)          000011          HT= 11          ;;CODE FOR HORIZONTAL TAB
(1)          000012          LF= 12          ;;CODE FOR LINE FEED
(1)          000015          CR= 15          ;;CODE FOR CARRIAGE RETURN
(1)          000200          CRLF= 200          ;;CODE FOR CARRIAGE RETURN-LINE FEED
(1)          177776          PS= 177776          ;;PROCESSOR STATUS WORD
(1)          :          .EQUIV PS,PSW
(1)          177774          STKLMT= 177774          ;;STACK LIMIT REGISTER
(1)          177772          PIRQ= 177772          ;;PROGRAM INTERRUPT REQUEST REGISTER
(1)          177570          DSWR= 177570          ;;HARDWARE SWITCH REGISTER
(1)          177570          DDISP= 177570          ;;HARDWARE DISPLAY REGISTER
(1)          :
(1)          :          ;*GENERAL PURPOSE REGISTER DEFINITIONS
(1)          000000          R0= %0          ;;GENERAL REGISTER
(1)          000001          R1= %1          ;;GENERAL REGISTER
(1)          000002          R2= %2          ;;GENERAL REGISTER
(1)          000003          R3= %3          ;;GENERAL REGISTER
(1)          000004          R4= %4          ;;GENERAL REGISTER
(1)          000005          R5= %5          ;;GENERAL REGISTER
(1)          000006          R6= %6          ;;GENERAL REGISTER
(1)          000007          R7= %7          ;;GENERAL REGISTER
(1)          000006          SP= %6          ;;STACK POINTER
(1)          000007          PC= %7          ;;PROGRAM COUNTER
(1)          :
(1)          :          ;*PRIORITY LEVEL DEFINITIONS
(1)          000000          PRO= 0          ;;PRIORITY LEVEL 0

```

(1)	000040	PR1=	40	:::PRIORITY LEVEL 1
(1)	000100	PR2=	100	:::PRIORITY LEVEL 2
(1)	000140	PR3=	140	:::PRIORITY LEVEL 3
(1)	000200	PR4=	200	:::PRIORITY LEVEL 4
(1)	000240	PR5=	240	:::PRIORITY LEVEL 5
(1)	000300	PR6=	300	:::PRIORITY LEVEL 6
(1)	000340	PR7=	340	:::PRIORITY LEVEL 7

(1) :\*'SWITCH REGISTER' SWITCH DEFINITIONS

(1)	100000	SW15=	100000
(1)	040000	SW14=	40000
(1)	020000	SW13=	20000
(1)	010000	SW12=	10000
(1)	004000	SW11=	4000
(1)	002000	SW10=	2000
(1)	001000	SW09=	1000
(1)	000400	SW08=	400
(1)	000200	SW07=	200
(1)	000100	SW06=	100
(1)	000040	SW05=	40
(1)	000020	SW04=	20
(1)	000010	SW03=	10
(1)	000004	SW02=	4
(1)	000002	SW01=	2
(1)	000001	SW00=	1

(1) .EQUIV SW09,SW9  
(1) .EQUIV SW08,SW8  
(1) .EQUIV SW07,SW7  
(1) .EQUIV SW06,SW6  
(1) .EQUIV SW05,SW5  
(1) .EQUIV SW04,SW4  
(1) .EQUIV SW03,SW3  
(1) .EQUIV SW02,SW2  
(1) .EQUIV SW01,SW1  
(1) .EQUIV SW00,SW0

(1) :\*DATA BIT DEFINITIONS (BIT00 TO BIT15)

(1)	100000	BIT15=	100000
(1)	040000	BIT14=	40000
(1)	020000	BIT13=	20000
(1)	010000	BIT12=	10000
(1)	004000	BIT11=	4000
(1)	002000	BIT10=	2000
(1)	001000	BIT09=	1000
(1)	000400	BIT08=	400
(1)	000200	BIT07=	200
(1)	000100	BIT06=	100
(1)	000040	BIT05=	40
(1)	000020	BIT04=	20
(1)	000010	BIT03=	10
(1)	000004	BIT02=	4
(1)	000002	BIT01=	2
(1)	000001	BIT00=	1

(1) .EQUIV BIT09,BIT9  
(1) .EQUIV BIT08,BIT8  
(1) .EQUIV BIT07,BIT7

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(1) .EQUIV BIT06,BIT6
(1) .EQUIV BIT05,BIT5
(1) .EQUIV BIT04,BIT4
(1) .EQUIV BIT03,BIT3
(1) .EQUIV BIT02,BIT2
(1) .EQUIV BIT01,BIT1
(1) .EQUIV BIT00,BIT0

(1) ;*BASIC 'CPU' TRAP VECTOR ADDRESSES
(1) 000004 ERRVEC= 4 ;:TIME OUT AND OTHER ERRORS
(1) 000010 RESVEC= 10 ;:RESERVED AND ILLEGAL INSTRUCTIONS
(1) 000014 TBITVEC=14 ;:'T' BIT
(1) 000014 TRTVEC= 14 ;:TRACE TRAP
(1) 000014 BPTVEC= 14 ;:BREAKPOINT TRAP (BPT)
(1) 000020 IOTVEC= 20 ;:INPUT/OUTPUT TRAP (IOT) **SCOPE**
(1) 000024 PWRVEC= 24 ;:POWER FAIL
(1) 000030 EMTVEC= 30 ;:EMULATOR TRAP (EMT) **ERROR**
(1) 000034 TRAPVEC=34 ;:'TRAP' TRAP
(1) 000060 TKVEC= 60 ;:TTY KEYBOARD VECTOR
(1) 000064 TPVEC= 64 ;:TTY PRINTER VECTOR
(1) 000240 PIRQVEC=240 ;:PROGRAM INTERRUPT REQUEST VECTOR
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2994
2995 170404 ABASE= 170404
2996 000344 AVECT1= 344
2997 000006 APRIOR= 6
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.SBTTL ACT11 HOOKS

```
(1) ;:*****
(2) ;:HOOKS REQUIRED BY ACT11
(1) $SVPC= ;:SAVE PC
(1) . =46
(1) 000046 $ENDAD ;:1)SET LOC.46 TO ADDRESS OF $ENDAD IN .$EOP
(1) . =52
(1) 000052 .WORD 0 ;:2)SET LOC.52 TO ZERO
(1) . =$SVPC ;: RESTORE PC
(1) . =1000
```

.SBTTL APT PARAMETER BLOCK

```
(1) ;:*****
(2) ;:SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
(2) ;:*****
(1) . $X= ;:SAVE CURRENT LOCATION
(1) . -24 ;:SET POWER FAIL TO POINT TO START OF PROGRAM
(1) 000024 200 ;:FOR APT START UP
(1) . -44 ;:POINT TO APT INDIRECT ADDRESS PNTR.
(1) 000044 $APTHDR ;:POINT TO APT HEADER BLOCK
(1) . $X ;:RESET LOCATION COUNTER
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(1) 001000  
(1) 001000 000000  
(1) 001002 001202  
(1) 001004 000002  
(1) 001006 000120  
(1) 001010 000120  
(1) 001012 000052  
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::\*\*\*\*\*  
: SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC  
: INTERFACE SPEC.  
\$APTHD:  
\$HIBTS: .WORD 0 ;;TWO HIGH BITS OF 18 BIT MAILBOX ADDR.  
\$MBADR: .WORD \$MAIL ;;ADDRESS OF APT MAILBOX (BITS 0-15)  
\$STSM: .WORD 2 ;;RUN TIM OF LONGEST TEST  
\$PASTM: .WORD 120 ;;RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)  
\$UNITM: .WORD 120 ;;ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT  
.WORD \$ETEND-\$MAIL/2 ;;LENGTH MAILBOX-ETABLE(WORDS)



(2)	001210	000000	\$PASS:	.WORD	APASS	::PASS COUNT
(2)	001212	000000	\$DEVCT:	.WORD	ADEVCT	::DEVICE COUNT
(2)	001214	000000	\$UNIT:	.WORD	AUNIT	::I/O UNIT NUMBER
(2)	001216	000000	\$MSGAD:	.WORD	AMSGAD	::MESSAGE ADDRESS
(2)	001220	000000	\$MSGLG:	.WORD	AMSGLG	::MESSAGE LENGTH
(2)	001222		\$ETABLE:			::APT ENVIRONMENT TABLE
(2)	001222	000	\$ENV:	.BYTE	AENV	::ENVIRONMENT BYTE
(2)	001223	000	\$ENVM:	.BYTE	AENVM	::ENVIRONMENT MODE BITS
(2)	001224	000000	\$SWREG:	.WORD	ASWREG	::APT SWITCH REGISTER
(2)	001226	000000	\$USWR:	.WORD	AUSWR	::USER SWITCHES
(2)	001230	000000	\$CPUOP:	.WORD	ACPUOP	::CPU TYPE,OPTIONS
(2)			*			BITS 15-11=CPU TYPE
(2)			*			11/04=01,11/05=02,11/20 03,11/40-04,11/45=05
(2)			*			11/70=06,PDQ=07,Q=10
(2)			*			BIT 10=REAL TIME CLOCK
(2)			*			BIT 9=FLOATING POINT PROCESSOR
(2)			*			BIT 8=MEMORY MANAGEMENT
(2)	001232	000	\$MAMS1:	.BYTE	AMAMS1	::HIGH ADDRESS,M.S. BYTE
(2)	001233	000	\$MTYP1:	.BYTE	AMTYP1	::MEM. TYPE,BLK#1
(2)			*			MEM. TYPE BYTE -- (HIGH BYTE)
(2)			*			900 NSEC CORE=001
(2)			*			300 NSEC BIPOLAR=002
(2)			*			500 NSEC MOS=003
(2)	001234	000000	\$MADR1:	.WORD	AMADR1	::HIGH ADDRESS,BLK#1
(2)			*			MEM.LAST ADDR.=3 BYTES,THIS WORD AND LOW OF 'TYPE' ABOVE
(2)	001236	000	\$MAMS2:	.BYTE	AMAMS2	::HIGH ADDRESS,M.S. BYTE
(2)	001237	000	\$MTYP2:	.BYTE	AMTYP2	::MEM. TYPE,BLK#2
(2)	001240	000000	\$MADR2:	.WORD	AMADR2	::MEM.LAST ADDRESS,BLK#2
(2)	001242	000	\$MAMS3:	.BYTE	AMAMS3	::HIGH ADDRESS,M.S.BYTE
(2)	001243	000	\$MTYP3:	.BYTE	AMTYP3	::MEM. TYPE,BLK#3
(2)	001244	000000	\$MADR3:	.WORD	AMADR3	::MEM.LAST ADDRESS,BLK#3
(2)	001246	000	\$MAMS4:	.BYTE	AMAMS4	::HIGH ADDRESS,M.S.BYTE
(2)	001247	000	\$MTYP4:	.BYTE	AMTYP4	::MEM. TYPE,BLK#4
(2)	001250	000000	\$MADR4:	.WORD	AMADR4	::MEM.LAST ADDRESS,BLK#4
(2)	001252	000344	\$VECT1:	.WORD	AVECT1	::INTERRUPT VECTOR#1,BUS PRIORITY#1
(2)	001254	000000	\$VECT2:	.WORD	AVECT2	::INTERRUPT VECTOR#2BUS PRIORITY#2
(2)	001256	170404	\$BASE:	.WORD	ABASE	::BASE ADDRESS OF EQUIPMENT UNDER TEST
(2)	001260	000000	\$DEVN:	.WORD	ADEVN	::DEVICE MAP
(2)	001262	000000	\$CDW1:	.WORD	ACDW1	::CONTROLLER DESCRIPTION WORD#1
(2)	001264	000000	\$CDW2:	.WORD	ACDW2	::CONTROLLER DESCRIPTION WORD#2
(2)	001266	000000	\$DDW0:	.WORD	ADDW0	::DEVICE DESCRIPTOR WORD#0
(2)	001270	000000	\$DDW1:	.WORD	ADDW1	::DEVICE DESCRIPTOR WORD#1
(2)	001272	000000	\$DDW2:	.WORD	ADDW2	::DEVICE DESCRIPTOR WORD#2
(2)	001274	000000	\$DDW3:	.WORD	ADDW3	::DEVICE DESCRIPTOR WORD#3
(2)	001276	000000	\$DDW4:	.WORD	ADDW4	::DEVICE DESCRIPTOR WORD#4
(2)	001300	000000	\$DDW5:	.WORD	ADDW5	::DEVICE DESCRIPTOR WORD#5
(2)	001302	000000	\$DDW6:	.WORD	ADDW6	::DEVICE DESCRIPTOR WORD#6
(2)	001304	000000	\$DDW7:	.WORD	ADDW7	::DEVICE DESCRIPTOR WORD#7
(2)	001306	000000	\$DDW8:	.WORD	ADDW8	::DEVICE DESCRIPTOR WORD#8
(2)	001310	000000	\$DDW9:	.WORD	ADDW9	::DEVICE DESCRIPTOR WORD#9
(2)	001312	000000	\$DDW10:	.WORD	ADDW10	::DEVICE DESCRIPTOR WORD#10
(2)	001314	000000	\$DDW11:	.WORD	ADDW11	::DEVICE DESCRIPTOR WORD#11
(2)	001316	000000	\$DDW12:	.WORD	ADDW12	::DEVICE DESCRIPTOR WORD#12
(2)	001320	000000	\$DDW13:	.WORD	ADDW13	::DEVICE DESCRIPTOR WORD#13
(2)	001322	000000	\$DDW14:	.WORD	ADDW14	::DEVICE DESCRIPTOR WORD#14
(2)	001324	000000	\$DDW15:	.WORD	ADDW15	::DEVICE DESCRIPTOR WORD#15

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001336 170434  
001340 170436  
001342 000344  
001344 000346  
001346 000364  
001350 000366  
001352 000006  
001354 000006  
001356 000000

SETEND:  
ASR: 170404 ;/CLOCK A STATUS REGISTER.  
ABR: 170406 ;/CLOCK A BUFFER REGISTER.  
ACR: 170430 ;/CLOCK A COUNT REGISTER.  
BSR: 170432 ;/CLOCK B STATUS REGISTER.  
BBR: 170434 ;/CLOCK B BUFFER REGISTER.  
BCR: 170436 ;/CLOCK B COUNT REGISTER.  
AVECT: 344 ;/CLOCK A INTR. VECTOR ADDR.  
AVECP2: 346 ;/CLOCK A INTR. STATUS WORD.  
BVECT: 364 ;/CLOCK B INTR. VECTOR ADDR.  
BVECT2: 366 ;/CLOCK B INTR. STATUS WORD.  
APRITY: 6 ;/PRIORITY LEVEL OF CLOCK A.  
BPRITY: 6 ;/PRIORITY LEVEL OF CLOCK B.  
\$TMDA: 0



3102			:ITEM 6	
3103				
3104	001430	030327	EM6	:CLOCK B BR DATA ERROR
3105	001432	031215	DH6	:ERRPC BBR WAS S/B
3106	001434	031710	DT6	:\$ERRPC, BBR, \$BDDAT, \$GDDAT
3107	001436	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3108				
3109			:ITEM 7	
3110				
3111	001440	030356	EM7	:CLOCK B CR DATA ERROR
3112	001442	031253	DH7	:ERRPC BCR WAS S/B
3113	001444	031722	DT7	:\$ERRPC, BCR, \$BDDAT, \$GDDAT
3114	001446	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3115				
3116			:ITEM 10	
3117				
3118	001450	030405	EM10	:DUAL ADDRESS ERROR
3119	001452	031311	DH10	:ERROR GOOD BAD GOOD DATA READ FROM
3120				: PC ADDR ADDR DATA DUAL ADDRESS
3121	001454	031734	DT10	:\$ERRPC, \$GDADR, \$BDADR, \$GDDAT, \$BDDAT
3122	001456	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3123				
3124			:ITEM 11	
3125				
3126	001460	030432	EM11	:CLOCK A COUNT ERROR
3127	001462	031121	DH4	:ERRPL ACR WAS S/B
3128	001464	031664	DT4	:\$ERRPC, ACR, \$BDDAT, \$GDDAT
3129	001466	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3130				
3131			:ITEM 12	
3132				
3133	001470	030461	EM12	:CLOCK A COUNT FUNCTION ERROR
3134	001472	031450	DH12	:ERRPC ASR
3135	001474	031750	DT12	:ERRPC, ASR
3136	001476	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3137				
3138			:ITEM 13	
3139				
3140	001500	032042	DF0	:ERROR 13 DOES NOT EXIST.
3141	001502	032042	DF0	:IT WOULD BE BAD LUCK.
3142	001504	032042	DF0	
3143	001506	032042	DF0	
3144				
3145			:ITEM 14	
3146				
3147	001510	030521	EM14	:CLOCK B COUNT FUNCTION ERROR
3148	001512	031467	DH14	:ERRPC BSR
3149	001514	031756	DT14	:\$ERRPC, BSR
3150	001516	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3151				

3152			:ITEM 15	
3153				
3154	001520	030561	EM15	:CLOCK B COUNT ERROR
3155	001522	031253	DH7	:ERRPC CSR WAS S/B
3156	001524	031722	DT7	:SERRPC, BCR, \$BDDAT, \$GDDAT
3157	001526	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3158				
3159			:ITEM 16	
3160				
3161	001530	030610	EM16	:CLOCK A INTERRUPT ERROR
3162	001532	031450	DH12	:ERRPC ASR
3163	001534	031750	DT12	:SERRPC, ASR
3164	001536	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3165				
3166			:ITEM 17	
3167				
3168	001540	030643	EM17	:CLOCK B INTERRUPT ERROR
3169	001542	031467	DH14	:ERRPC BSR
3170	001544	031756	DT14	:SERRPC, BSR
3171	001546	032042	DF0	
3172				
3173			:ITEM 20	
3174				
3175	001550	030676	EM20	:CLOCK A REPEATABILITY ERROR
3176	001552	031505	DH20	:ERROR ASR 2ND CNT 1ST CNT
3177	001554	031640	DT1	:SERRPC, ASR, \$BDDAT, \$GDDAT
3178	001556	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3179				
3180			:ITEM 21	
3181				
3182	001560	030432	EM11	:CLOCK A COUNT ERROR
3183	001562	031121	DH4	:ERROR ASR 2ND CNT 1ST CNT
3184	001564	031764	DT21	:SERRPC, ASR, \$BDDAT, \$GDDAT
3185	001566	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3186				
3187			:ITEM 22	
3188				
3189	001570	030432	EM11	:CLOCK A COUNT ERROR
3190	001572	031121	DH4	:ERRPC ASR WAS S/B
3191	001574	031776	DT22	:SERRPC, ACR, \$BDDAT, \$TMP0
3192	001576	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3193				
3194			:ITEM 23	
3195				
3196	001600	030735	EM23	:CLOCK B REPEATABILITY ERROR
3197	001602	031547	DH23	:ERROR ASR 2NDCNT 1STCNT
3198	001604	031640	DT1	:SERRPC, ASR, \$BDDAT, \$GDDAT
3199	001606	032042	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
3200				
3201			:ITEM 24	

```

3202
3203 001610 030561          EM15          :CLOCK B COUNT ERROR
3204 001612 031253          DH7           :ERRPC BCR WAC S/B
3205 001614 032010          DT24          :$ERRPC,BCR,$GDDA1,$TMPO
3206 001616 032042          DF0           :ALL NUMBERS ARE IN OCTAL FORM
(1)
3207
3208          :ITEM 25
3209
3210 001620 030561          EM15          :CLOCK B COUNT ERROR
3211 001622 031253          DH7           :ERRPC BCR WAS S/B
3212 001624 032022          DT25          :$ERRPC,BCR,$BDDAT,$TMPO
3213 001626 032042          DF0           :ALL NUMBERS ARE IN OCTAL FORM
(1)
3214
3215          :ITEM 26
3216
3217 001630 030774          EM26          :CLOCK ADDRESSING ERROR
3218 001632 031611          DH26          :ERRPC CLOCK ADDR.
3219 001634 032034          DT26          :$ERRPC,$TMPO
3220 001636 032042          DF0           :ALL NUMBERS ARE IN OCTAL FORM
(1)
3221
3222
3223          :
          : ADDRESS OF KMC-11 OF LPA-11 THE ADDR FOR KMADO MAY BE
          : CHANGED BY THE USER TO REFLECT
          : A DIFFERENT KMC-11 ADDR. THE
          : REST OF THE ADDRESSES WILL
          : BE CHANGED BY THE PROGRAM.
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1) 001640          LPCI:
(1) 001640 170460          KMADO: .WORD 170460          :BASE KMC ADDR. MAY BE PATCHED BY USER.
(1)
(1) 001642          LPMR:
(1) 001642 170461          KMAD1: .WORD 170460+1          ;>DO NOT <;KMC-CSR ADDR
(1) 001644          LPCO:
(1) 001644 170462          KMAD2: .WORD 170460+2          ;>PATCH <;
(1) 001646          LPSO:
(1) 001646 170463          KMAD3: .WORD 170460+3          ;>THIS AREA <
(1) 001650          LPADL:
(1) 001650 170464          KMAD4: .WORD 170460+4          :
(1) 001652          LPADH:
(1) 001652 170465          KMAD5: .WORD 170460+5          ;>DO NOT <
(1) 001654          LPMS1:
(1) 001654 170466          KMAD6: .WORD 170460+6          ;>PATCH <
(1) 001656          LPMS2:
(1) 001656 170467          KMAD7: .WORD 170460+7          ;>THIS AREA <
(1)
(1) 001660 000344          VECTOR: .WORD AVECT18777          :BASE VECTOR OF KMC
(1) 001662 000350          VECTPS: .WORD 4+AVECT18777          :VECTOR ADDR.+2
(1)
(1) 001664 000004          VERSN: .WORD 4          :CURRENT VERSION NUMBER OF MICROCODE.
(1)
(1) 001666 000000          .DVLS: .WORD 0          ;/DEVICE LIST OF I/C ADDR. DEFINED

```



LPA-KW11K DIAGNOSTIC MD-11-CRLPG-8  
(RLPGB.P11 08-AUG-79 10:30

MACY11 30G(1063) 08-AUG-79<sup>G 3</sup> 10:30 PAGE 6-12  
ERROR POINTER TABLE

SEQ 0032

(1) 001670 000020  
(1)  
3224

.BLKW 16. ;/BY INIT.  
.SBTTL PROGRAM START

```

3227
3228 001730
(1)
(1)
(1) 001730 012706 001100
(1) 001734 005026
(1) 001736 022706 001140
(1) 001742 001374
(1) 001744 012706 001100
(1)
(1) 001750 012737 026010 000020
(1) 001756 012737 000340 000022
(1) 001764 012737 025242 000030
(1) 001772 012737 000340 000032
(1) 002000 012737 030054 000034
(1) 002006 012737 000340 000036
(1) 002014 012737 027676 000024
(1) 002022 012737 000340 000026
(1) 002030 005037 001166
(1) 002034 005037 001170
(1) 002040 112737 000001 001115
(1) 002046 012737 002046 001106
(1) 002054 012737 002054 001110
(2)
(2)
(2) 002062 013746 000004
(2) 002066 012737 002122 000004
(2) 002074 012737 177570 001140
(2) 002102 012737 177570 001142
(2) 002110 022777 177777 177022
(2) 002116 001012
(2)
(2) 002120 000403
(2) 002122 012716 002130 64$:
(2) 002126 000002
(2) 002130 012737 000176 001140 65$:
(2) 002136 012737 000174 001142
(2) 002144 012637 000004 66$:
(1)
(2) 002150 005037 001210
(2) 002154 132737 000200 001223
(2) 002162 001403
(2) 002164 012737 001224 001140
(2) 002172
3229 002172 005737 000042
3230 002176 001015
3231
3232 002200 104401 002206
(1) 002204 000412
(1)
(1) 002232
3233
3234 002232 013737 001256 001326 10$:
3235 002240 012737 000001 001212
3236 002246 005037 001210
3237

```

```

START:
.SBTTL INITIALIZE THE COMMON TAGS
::CLEAR THE COMMON TAGS ($CMTAG) AREA
MOV #CMTAG,R6 ;;FIRST LOCATION TO BE CLEARED
CLR (R6)+ ;;CLEAR MEMORY LOCATION
CMP #SWR,R6 ;;DONE?
BNE -6 ;;LOOP BACK IF NO
MOV #STACK,SP ;;SETUP THE STACK POINTER
::INITIALIZE A FEW VECTORS
MOV #SCOPE,@IOTVEC ;;IOT VECTOR FOR SCOPE ROUTINE
MOV #340,@IOTVEC+2 ;;LEVEL 7
MOV #ERROR,@EMTVEC ;;EMT VECTOR FOR ERROR ROUTINE
MOV #340,@EMTVEC+2 ;;LEVEL 7
MOV #STRAP,@TRAPVEC ;;TRAP VECTOR FOR TRAP CALLS
MOV #340,@TRAPVEC+2;LEVEL 7
MOV #SPWRDN,@PWRVEC ;;POWER FAILURE VECTOR
MOV #340,@PWRVEC+2 ;;LEVEL 7
CLR $TIMES ;;INITIALIZE NUMBER OF ITERATIONS
CLR $ESCAPE ;;CLEAR THE ESCAPE ON ERROR ADDRESS
MOVB #1,$ERMAX ;;ALLOW ONE ERROR PER TEST
MOV #,$SLPADR ;;INITIALIZE THE LOOP ADDRESS FOR SCOPE
MOV #,$SLPERR ;;SETUP THE ERROR LOOP ADDRESS
::SIZE FOR A HARDWARE SWITCH REGISTER. IF NOT FOUND OR IT IS
::EQUAL TO A "-1", SETUP FOR A SOFTWARE SWITCH REGISTER.
MOV @ERRVEC,-(SP) ;;SAVE ERROR VECTOR
MOV #64$,@ERRVEC ;;SET UP ERROR VECTOR
MOV #DSWR,SWR ;;SETUP FOR A HARDWARE SWICH REGISTER
MOV #DDISP,DISPLAY ;;AND A HARDWARE DISPLAY REGISTER
CMP #-1,@SWR ;;TRY TO REFERENCE HARDWARE SWR
BNE 66$ ;;BRANCH IF NO TIMEOUT TRAP OCCURRED
;;AND THE HARDWARE SWR IS NOT -1
BR 65$ ;;BRANCH IF NO TIMEOUT
MOV #65$, (SP) ;;SET UP FOR TRAP RETURN
RTI
MOV #SWREG,SWR ;;POINT TO SOFTWARE SWR
MOV #DISPREG,DISPLAY
MOV (SP)+,@ERRVEC ;;RESTORE ERROR VECTOR
CLR $PASS ;;CLEAR PASS COUNT
BITB #APTSIZE,$ENVM ;;TEST USER SIZE UNDER APT
BEQ 67$ ;;YES,USE NON-APT SWITCH
MOV #SSWREG,SWR ;;NO,USE APT SWITCH REGISTER
TST @42 ;;IF RUNNING UNDER ACT-
BNE 10$ ;;NO TYPEOUT.
TYPE ,69$ ;;TYPE ASCIZ STRING
BR 68$ ;;GET OVER THE ASCIZ
::69$: .ASCIZ <15><12><12>#MD-11-CRLPG-B#<15><12>
68$:

```

```
3238      ; THIS SECTION OF CODE HANDLES INITIALIZING LPA-11 FUNCTIONS
(1)      ;
(1)      ;
(1)      ;
(1) 002252 010046      MOV      R0,-(SP)
(1) 002254 010146      MOV      R1,-(SP)
(1) 002256 013700 001640      MOV      KMADO,R0      ;GET KMC-11 ADDRESS.
(1) 002262 012701 001642      MOV      #KMAD1,R1     ;GET ADDR. OF ADDR. LIST.
(1)      ;
(1) 002266 005200      70$: INC      R0      ;UPDATE ADDR.
(1) 002270 010021      MOV      R0,(1)+      ;WRITE ADDR.
(1) 002272 020127 001660      CMP      R1,#KMAD7+2  ;DONE ALL ADDRESSES?
(1) 002276 001373      BNE      70$          ;NO - DO NEXT ADDR.
(1) 002300 005037 001666      CLR      .DVLS        ;CLR ADDR. LIST.
(1) 002304 012601      MOV      (SP)+,R1
(1) 002306 012600      MOV      (SP)+,R0
3239
3240 002310      LOOP:
3241 002310 005000      CLR      R0
3242 002312 005200      1$: INC      R0      ;DELAY SOME TIME SO THAT FIRST RESET
3243 002314 001376      BNE      1$          ;INSTR. WON'T CLOBBER TYPEOUT.
3244 002316 013700 001326      MOV      ASR,R0      ;NOW WE'RE GONNA FIX
3245 002322 062700 000002      ADD      #2,R0      ;ALL CLOCK ADDRESSES BASED ON ASR.
3246 002326 010037 001330      MOV      R0,ABR
3247 002332 062700 000022      ADD      #22,R0
3248 002336 010037 001332      MOV      R0,ACR
3249 002342 062700 000002      ADD      #2,R0
3250 002346 010037 001334      MOV      R0,BSR
3251 002352 062700 000002      ADD      #2,R0
3252 002356 010037 001336      MOV      R0,BBR
3253 002362 062700 000002      ADD      #2,R0
3254 002366 010037 001340      MOV      R0,BCR
3255
3256 002372 013700 001342      MOV      AVECT,R0     ;NOW FIX VECTOR ADDRESSES
3257 002376 062700 000002      ADD      #2,R0      ;BASED ON AVECT.
3258 002402 010037 001344      MOV      R0,AVECP2
3259 002406 062700 000016      ADD      #16,R0
3260 002412 010037 001346      MOV      R0,BVECT
3261 002416 062700 000002      ADD      #2,R0
3262 002422 010037 001350      MOV      R0,BVECT2
3263
3264 002426 013737 001352 001354      MOV      APRITY,BPRITY ;FIX CLK B'S PRIORITY BASED ON A'S.
3265 002434 000402      BR      SSTART
3266 002436 005037 001666      RSTART: CLR      .DVLS
3267 002442 012706 001100      SSTART: MOV      #STACK,SP
3268 002446 012746 000340      MOV      #340,-(SP)   ;SET PROCESSOR PRIORITY TO 7.
3269 002452 012746 002460      MOV      #1$,-(SP)
3270 002456 000002      RTI
3271 002460      1$:
3272
3273      .SBTTL *
3274      .SBTTL * PHASE 1 CLOCKS A+B BASIC LOGIC TESTS.
3275      .SBTTL *
```

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002460	000240		
002462	012737	000050	001166
002470	012737	002476	001106
002476	112737	000001	001102
002504	112737	000001	001206

```

*****
*TEST 1      *TEST THE ADDRESSABILITY OF CLOCK ADDRESS
*****
*BUS A17': 'A04'='DEVICE' H; 'DEVICE' H + 'TPO' H='DEV ENABLE' H
*DEV ENABLE' H+'TP1' H='DEV ENB 2' H
*****
* PROBABLE SYNC POINT FOR THIS TEST:: 'BUS A17'
* CLOCK ADDRESS TEST. SCOPE FOR 'DEV ENB 2' H AND WORK BACK
*****
TST1:  NOP
      MOV   #50,$TIMES          ;;DO 50 ITERATIONS
      MOV   #1$, $LPADR        ;;SET SCOPE LOOP ADDRESS
1$:    MOVB  #1,$STNM
      MOVB  #1,$TESTN
*****
;*    MOV   @ASR,$BDDAT        ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
;*    MOV   @ABR,$BDDAT        ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
;*    MOV   @ACR,$BDDAT        ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
;*    MOV   @BSR,$BDDAT        ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
;*    MOV   @BBR,$BDDAT        ;/READ DEVICE REG SBR,PUT DATA IN $BDDAT.
;*    MOV   @BCR,$BDDAT        ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
*****
*TEST 2      *TEST THAT CLOCK A BUFFER CAN BE WRITTEN INTO
*****
*FOR LOADING DATA:
*(WE KNOW WE CAN ADDR. KW11), 'BUS A01' L + 'A02' H + 'A03' H
*+'BUS C1' L='LD BUFF A' L
*LD BUF A' L + BUFFERED DATA LOADS INTO MUX LATCH (NOTE WE KNOW
*BY NOW 'TP1' L SHOULD BE GOOD).
*****
* FOR READING DATA:
*BUS A01 L + (DATA 1N H + EV ENABLE(1) H)-RD BUFF AL
*[BA01H*(DEPENDING ON WHICH DATA BITS READ) RD BUF AL]+BUFF A00:15
*+[DEV ENABLE*DATA IN L]=BUS DATA
*****
*SINCE WE WONT LOOK FOR ANY SPECIFIC DATA BIT FAILURE,
*JUST THAT WE CAN WRITE INTO BUFFER + READ BACK,
*IF FAILED, KEY ON 'LD BUFF A L' AND 'RD BUFF A L'
*****
* PROBABLE SYNC POINT FOR THIS TEST:: 'BUS A17'' (2 OCCURANCES PER LOOP)

```





```

(3)
(2) 002704 000004
(1) 002706 012737 000050 001166
3389
3390 002714 012737 001416 001124
3391
3392
3393
(1)
3394
(1)
3395 002742 005737 001126
3396 002746 001001
3397
  
```

```

*****
TST4: SCOPE
MOV #50,$TIMES ;;DO 50 ITERATIONS
MOV #1416,$GDDAT ;LOAD $GDDAT WITH S/B.
;LOAD STATUS REGISTER.
;READ BACK STATUS REGISTER
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 1$ ;IF ANY BITS RETURNED - NO ERROR.
  
```

::: \$>> ERROR << \$

```

3398 002750 104002 ERROR 2 ;ERROR-UNABLE TO LOAD AND READ BACK
3399 ;STATUS REGISTER OF CLOCK A.
3400
3401
  
```

::: \$>> ERROR << \$

```

3402 002752
3403 002752 005037 001124
3404
(1)
3405
3413
3414
(3)
(4)
(4)
(5)
(5)
(5)
(4)
(4)
(3)
  
```

```

1$: CLR $GDDAT ;CLEAR CLOCK A'S STATUS REG.
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
  
```

```

(3)
(4)
(4)
(5)
(5)
(5)
(4)
(4)
(3)
  
```

```

*****
*TEST 5 *TEST THAT CLOCK B'S STATUS REGISTER CAN BE WROTE/READ
;*
;*NEW SIGNALS: ['BA03'' H + 'BA02'' L + 'BA01'' L]='LD STATB'' L*'RD STAT B'' L
;*
;* PROBABLE SYNC POINT FOR THIS TEST:: 'DEV ENABLE (1)'' 2 OCCURANCES PER PASS
;*
*****
  
```

```

(2) 002766 000004
(1) 002770 012737 000050 001166
3415
3416 002776 012737 001016 001124
3417
3418
3419
(1)
3420
(1)
3421 003024 005737 001126
3422 003030 001001
3423
3424
  
```

```

*****
TST5: SCOPE
MOV #50,$TIMES ;;DO 50 ITERATIONS
MOV #1016,$GDDAT ;USE 1016 AS PATTERN, PUT IN $GDDAT.
;LOAD B'S STAT REG.
;READ BACK THE STATUS REG.
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 1$ ;IF ANY BITS CAME BACK, SUBTEST OK.
  
```

::: \$>> ERROR << \$

```

3425 003032 104005 ERROR 5 ;ERROR-COULD NOT WRITE/READ BACK
3426 ;CLOCK B'S STATUS REGISTER.
  
```





3562

(6)  
 (5)  
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 (3)

```

003102 000004
003104 012737 000100 001166
003112 012737 100000 001124
003140 023737 001124 001126
003146 001402
    
```

```

: /#
*****
*TEST 7 *TEST THAT CLOCK A STATUS REGISTER BIT 15 CAN BE SET AND CLEARED
*
*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
*F/FS OR GATES
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
*
*****
TST7:  SCOPE
      MOV     #100,$TIMES      ;;DO 100 ITERATIONS
                               ;/CLEAR THE STATUS REGISTER.
                               ;/SET BIT 15.
                               ;/SET FOR ERROR TYPEOUT S/B.
                               ;/READ THE STATUS REGISTER.
      MOV     #BIT15,$GDDAT
      ;*     MOV     $GDDAT,@ASR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
      ;*     MOV     @ASR,$BDDAT    ; READ DEVICE REG ASR,PUT DATA IN $BDDAT.
      CMP     $GDDAT,$BDDAT      ;/DID BIT 15 AND ONLY BIT 15 SET?
      BEQ     1$                ;/IF SO-LETS TRY CLEARING IT.
    
```

::: \$ \$\$\$\$>> ERROR << \$ \$\$\$\$\$\$

```

(2) 003150 104002          ERROR 2                ;/ERROR CLOCK AS STATUS REGISTER.
(2)                                     ;/BIT 15 FAILED TO BIT SET.
(3)
    
```

::: \$ \$\$\$\$>> ERROR << \$ \$\$\$\$\$\$

```

(2) 003152 000416          BR     2$                ;/BR TO END SUBTEST.
(2) 003154                                     ;/TRY CLEARING BIT 15.
(2) 003154 005037 001124  1$:    CLR     $GDDAT          ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2)                                     ;/NOW READ IT BACK.
(3)
(3) ;*     MOV     $GDDAT,@ASR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;*     MOV     @ASR,$BDDAT    ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 003200 005737 001126  TST     $BDDAT
(2) 003204 001401          BEQ     2$                ;/IF ZERO-NO ERROR.
(3)
    
```

::: \$ \$\$\$\$>> ERROR << \$ \$\$\$\$\$\$

```

(2) 003206 104002          ERROR 2                ;/ERROR-CLOCK A STATUS REGISTER.
(2)                                     ;/BIT 15 FAILED TO CLEAR.
(3)
    
```

::: \$ \$\$\$\$>> ERROR << \$ \$\$\$\$\$\$

```

(2) 003210          2$:
    
```



```

(2)      :/*
(5)      :*****
(5)      *TEST 11      *TEST THAT CLOCK A STATUS REGISTER BIT 13 CAN BE SET AND CLEARED
(6)      *
(6)      *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6)      *F/FS OR GATES
(7)      *
(7)      * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(7)      *
(6)      *
(5)      :*****

```

```

(4) 003316 000004 TST11: SCOPE
(3) 003320 012737 000100 001166      MOV      #100,$TIMES      ;;DO 100 ITERATIONS
(2)                                      ;/CLEAR THE STATUS REGISTER.
(2)                                      ;/SET BIT 13.
(2)                                      ;/SET FOR ERROR TYPEOUT S/B.
(2)                                      ;/READ THE STATUS REGISTER.
(2) 003326 012737 020000 001124      MOV      #BIT13,$GDDAT
(3)                                      ;*
(3)                                      ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)                                      ;*
(3)                                      ;*      MOV      @ASR,$RDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $RDDAT.
(2) 003354 023737 001124 001126      CMP      $GDDAT,$RDDAT      ;/DID BIT 13 AND ONLY BIT 13 SET?
(2) 003362 001402      BEQ      1$                ;/IF SO-LETS TRY CLEARING IT.
(3)

```

;;;\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```

(2) 003364 104002      ERROR      2                ;/ERROR CLOCK AS STATUS REGISTER.
(2)                                      ;/BIT 13 FAILED TO BIT SET.
(3)

```

;;;\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```

(2) 003366 000416      BR      2$                ;/BR TO END SUBTEST.
(2) 003370      1$:      ;/TRY CLEARING BIT 13.
(2) 003370 005037 001124      CLR      $GDDAT          ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2)                                      ;/NOW READ IT BACK.
(3)
(3)      ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)      ;*
(3)      ;*      MOV      @ASR,$RDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $RDDAT.
(2) 003414 005737 001126      TST      $RDDAT
(2) 003420 001401      BEQ      2$                ;/IF ZERO-NO ERROR.
(3)

```

;;;\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```

(2) 003422 104002      ERROR      2                ;/ERROR-CLOCK A STATUS REGISTER.
(2)                                      ;/BIT 13 FAILED TO CLEAR.
(3)

```

;;;\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(2) 003424 2\$:

```
(2)                                     :/*
(6)                                     :*****
(5) :*TEST 12          *TEST THAT CLOCK A STATUS REGISTER BIT 9 CAN BE SET AND CLEARED
(6) :*
(6) :*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) :*F/FS OR GATES
(7) :*
(7) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(7) :*
(6) :*
(5) :******
(4) 003424 000004 TST12: SCOPE
(3) 003426 012737 000100 001166 MOV #100,$TIMES ;;DO 100 ITERATIONS
(2)                                     ;/CLEAR THE STATUS REGISTER.
(2)                                     ;/SET BIT 9.
(2)                                     ;/SET FOR ERROR TYPEOUT S/B.
(2)                                     ;/READ THE STATUS REGISTER.
(2) 003434 012737 001000 001124 MOV #BIT9,$GDDAT
(3)                                     ;*
(3)                                     ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)                                     ;*
(3)                                     ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 003462 023737 001124 001126 CMF $GDDAT,$BDDAT ;/DID BIT 9 AND ONLY BIT 9 SET?
(2) 003470 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(3)
(2)                                     :*:*****>> ERROR <<*****
(2) 003472 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2)                                     ;/BIT 9 FAILED TO BIT SET.
(3)
(2)                                     :*:*****>> ERROR <<*****
(2) 003474 000416 BR 2$ ;/BR TO END SUBTEST.
(2) 003476 1$: ;/TRY CLEARING BIT 9.
(2) 003476 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2)                                     ;/NOW READ IT BACK.
(3)
(3)                                     ;*
(3)                                     ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)                                     ;*
(3)                                     ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 003522 005737 001126 TST $BDDAT
(2) 003526 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
(3)
(2)                                     :*:*****>> ERROR <<*****
(2) 003530 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2)                                     ;/BIT 9 FAILED TO CLEAR.
(3)
(2)                                     :*:*****>> ERROR <<*****
(2) 003532 2$:
```

(2) :/\*  
(6) :\*\*\*\*\*  
(5) :\*TEST 13 \*TEST THAT CLOCK A STATUS REGISTER BIT 8 CAN BE SET AND CLEARED  
(6) :\*  
(6) :\*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(6) :\*F/FS OR GATES  
(7) :\*  
(7) :\* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(7) :\*  
(6) :\*  
(5) :\*\*\*\*\*

```
(4) 003532 000004  
(3) 003534 012737 000100 001166 TST13: SCOPE  
(2) MOV #100,$TIMES ;:DO 100 ITERATIONS  
(2) ;/CLEAR THE STATUS REGISTER.  
(2) ;/SET BIT 8.  
(2) ;/SET FOR ERROR TIMEOUT S/B.  
(2) ;/READ THE STATUS REGISTER.  
(2) 003542 012737 000400 001124 MOV #BIT8,$GDDAT  
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
(2) 003570 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 8 AND ONLY BIT 8 SET?  
(2) 003576 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.  
(3)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(2) 003600 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.  
(2) ;/BIT 8 FAILED TO BIT SET.  
(3)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(2) 003602 000416 BR 2$ ;/BR TO END SUBTEST.  
(2) 003604 1$: ;/TRY CLEARING BIT 8.  
(2) 003604 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TIMEOUT IF ANY.  
(2) ;/NOW READ IT BACK.  
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
(2) 003630 005737 001126 TST $BDDAT  
(2) 003634 001401 BEQ 2$ ;/IF ZERO-NO ERROR.  
(3)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(2) 003636 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.  
(2) ;/BIT 8 FAILED TO CLEAR.  
(3)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(2) 003640 2\$:

(2) :/#  
(6) :\*\*\*\*\*  
(5) \*TEST 14 \*TEST THAT CLOCK A STATUS REGISTER BIT 7 CAN BE SET AND CLEARED  
(6) \*  
(6) \*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(6) \*F/FS OR GATES  
(7) \*  
(7) \* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(7) \*  
(6) \*  
(5) :\*\*\*\*\*

```
TST14: SCOPE
(4) 003640 000004
(3) 003642 012737 000100 001166 MOV #100,$TIMES ;;DO 100 ITERATIONS
(2) ;;CLEAR THE STATUS REGISTER.
(2) ;;SET BIT 7.
(2) ;;SET FOR ERROR TYPEOUT S/B.
(2) ;;READ THE STATUS REGISTER.
(2) 003650 012757 000200 001124 MOV #BIT7,$GDDAT
(3)
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 003676 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 7 AND ONLY BIT 7 SET?
(2) 003704 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(3)
```

(2) :::\*\*\*\*\*>> ERROR <<\*\*\*\*\*  
(2) 003706 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.  
(2) ;/BIT 7 FAILED TO BIT SET.  
(3)

```
(2) 003710 000416 BR 2$ ;/BR TO END SUBTEST.
(2) 003712 1$: ;/TRY CLEARING BIT 7.
(2) 003712 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3)
(3) ;* MOV $GDDAT,@ASH ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 003736 005737 001126 TST $BDDAT
(2) 003742 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
(3)
```

(2) :::\*\*\*\*\*>> ERROR <<\*\*\*\*\*  
(2) 003744 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.  
(2) ;/BIT 7 FAILED TO CLEAR.  
(3)

(2) :::\*\*\*\*\*>> ERROR <<\*\*\*\*\*  
(2) 003746 2\$:

(2) ;/ #  
(6) :\*\*\*\*\*  
(5) :\*TEST 15 \*TEST THAT CLOCK A STATUS REGISTER BIT 6 CAN BE SET AND CLEARED  
(6) :\*  
(6) :\*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(6) :\*F/FS OR GATES  
(7) :\*  
(7) :\* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(7) :\*  
(6) :\*  
(5) :\*\*\*\*\*

```
(4) 003746 000004 TST15: SCOPE
(3) 003750 012737 000100 001166 MOV #100,$TIMES ;:DO 100 ITERATIONS
(2) ;:/CLEAR THE STATUS REGISTER.
(2) ;:/SET BIT 6.
(2) ;:/SET FOR ERROR TIMEOUT S/B.
(2) ;:/READ THE STATUS REGISTER.
(2) 003756 012737 000100 001124 MOV #BIT6,$GDDAT
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004004 023737 001124 001126 CMP $GDDAT,$BDDAT ;:/DID BIT 6 AND ONLY BIT 6 SET?
(2) 004012 001402 BEQ 1$ ;:/IF SO-LETS TRY CLEARING IT.
(3)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(2) 004014 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;:/BIT 6 FAILED TO BIT SET.
(3)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(2) 004016 000416 BR 2$ ;/BR TO END SUBTEST.
(2) 004020 1$: CLR $GDDAT ;/TRY CLEARING BIT 6.
(2) 004020 005037 001124 ;:/CLEAR S/B FOR TIMEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004044 005737 001126 TST $BDDAT
(2) 004050 001401 BEQ 2$ ;/IF ZERO-NO ERROR
(3)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(2) 004052 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;:/BIT 6 FAILED TO CLEAR.
(3)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(2) 004054 2$
```

```
(2)                                     :/*  
(6) :*****  
(5) :*TEST 16 *TEST THAT CLOCK A STATUS REGISTER BIT 5 CAN BE SET AND CLEARED  
(6) :*  
(6) :*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(6) :*F/FS OR GATES  
(7) :*  
(7) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(7) :*  
(6) :*  
(5) :*****  
(4) 004054 000004 TST16: SCOPE  
(3) 004056 012737 000100 001'66 MOV #100,$TIMES ;;DO 100 ITERATIONS  
(2)                                     ;/CLEAR THE STATUS REGISTER.  
(2)                                     ;/SET BIT 5.  
(2)                                     ;/SET FOR ERROR TYPEOUT S/B.  
(2)                                     ;/READ THE STATUS REGISTER.  
(2) 004064 012737 000040 001124 MOV #BIT5,$GDDAT  
(3)                                     ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
(3)                                     ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
(2) 004112 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 5 AND ONLY BIT 5 SET?  
(2) 004120 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.  
(3)                                     :::*****>> ERROR <<*****  
(2) 004122 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.  
(2)                                     ;/BIT 5 FAILED TO BIT SET.  
(3)                                     :::*****>> ERROR <<*****  
(2) 004124 000416 BR 2$ ;/BR TO END SUBTEST.  
(2) 004126 1$: ;/TRY CLEARING BIT 5.  
(2) 004126 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.  
(2)                                     ;/NOW READ IT BACK.  
(3)                                     ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
(3)                                     ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
(2) 004152 005737 001126 TST $BDDAT  
(2) 004156 001401 BEQ 2$ ;/IF ZERO-NO ERROR!  
(3)                                     :::*****>> ERROR <<*****  
(2) 004160 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.  
(2)                                     ;/BIT 5 FAILED TO CLEAR.  
(3)                                     :::*****>> ERROR <<*****  
(2) 004162 2$:
```



```
(2)                                     ;/
(6) :*****
(5) :*TEST 17      *TEST THAT CLOCK A STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(6) :*
(6) :*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAI (RE-SUSPECT INDIVIDUAL
(6) :*F/FS OR GATES
(7) :*
(7) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(7) :*
(6) :*
(5) :*****
(4) 004162 000004 TST17: SCOPE
(3) 004164 012737 000100 001166 MOV #100,$TIMES ;:DO 100 ITERATIONS
(2) ;:/CLEAR THE STATUS REGISTER.
(2) ;:/SET BIT 3.
(2) ;:/SET FOR ERROR TYPEOUT S/B.
(2) ;:/READ THE STATUS REGISTER.
(2) 004172 012737 000010 001124 MOV #BIT3,$GDDAT
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004220 023737 001124 001126 CMP $GDDAT,$BDDAT ;:/DID BIT 3 AND ONLY BIT 3 SET?
(2) 004226 001402 BEQ 1$ ;:/IF SO-LETS TRY CLEARING IT.
(3)
:::*****>> ERROR <<*****
(2) 004230 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;:/BIT 3 FAILED TO BIT SET.
(3)
:::*****>> ERROR <<*****
(2) 004232 000416 BR 2$ ;/BR TO END SUBTEST.
(2) 004234 1$: ;/TRY CLEARING BIT 3.
(2) 004234 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3)
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004260 005737 001126 TST $BDDAT
(2) 004264 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
(3)
:::*****>> ERROR <<*****
(2) 004266 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;:/BIT 3 FAILED TO CLEAR.
(3)
:::*****>> ERROR <<*****
(2) 004270 2$:
```



```
(2)                                     :/##
(6) :*****
(5) :*TEST 21      *TEST THAT CLOCK A STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
(6) :*
(6) :*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) :*F/FS OR GATES
(7) :*
(7) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(7) :*
(6) :*
(5) :*****
(4) 004376 000004 TST21: SCOPE
(3) 004400 012737 000100 001166   MOV      #100,$TIMES      ;;DO 100 ITERATIONS
(2)                                     ;/CLEAR THE STATUS REGISTER.
(2)                                     ;/SET BIT 1.
(2)                                     ;/SET FOR ERROR TYPEOUT S/B.
(2)                                     ;/READ THE STATUS REGISTER.
(2) 004406 012737 000002 001124   MOV      #BIT1,$GDDAT
(3)                                     ;*
(3)                                     ;* MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)                                     ;*
(3)                                     ;* MOV      @ASR,$BDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004434 023737 001124 001126   CMP      $GDDAT,$BDDAT    ;/DID BIT 1 AND ONLY BIT 1 SET?
(2) 004442 001402   BEQ      1$              ;/IF SO-LETS TRY CLEARING IT.
(3)
      ;;:*****>> ERROR <<*****
(2) 004444 104002   ERROR  2              ;/ERROR CLOCK AS STATUS REGISTER.
(2)                                     ;/BIT 1 FAILED TO BIT SET.
(3)
      ;;:*****>> ERROR <<*****
(2) 004446 000416   BR      2$              ;/BR TO END SUBTEST.
(2) 004450   1$:          ;/TRY CLEARING BIT 1.
(2) 004450 005037 001124   CLR      $GDDAT          ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2)                                     ;/NOW READ IT BACK.
(3)
(3)                                     ;*
(3)                                     ;* MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)                                     ;*
(3)                                     ;* MOV      @ASR,$BDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004474 005737 001126   TST      $BDDAT
(2) 004500 001401   BEQ      2$              ;/IF ZERO-NO ERROR!
(3)
      ;;:*****>> ERROR <<*****
(2) 004502 104002   ERROR  2              ;/ERROR-CLOCK A STATUS REGISTER.
(2)                                     ;/BIT 1 FAILED TO CLEAR.
(3)
      ;;:*****>> ERROR <<*****
(2) 004504   2$:
```



```
(3)                                     :/N
(7)                                     :*****
(6) *TEST 23 *TEST THAT CLOCK A BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) ******
(5) 004612 000004 TST23: SCOPE
(4) 004614 012737 000100 001166 MOV #100,$TIMES ;;DO 100 ITERATIONS
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 0.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 004622 012737 000001 001124 MOV #BIT0,$GDDAT
(4)                                     ;*
(4) * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) * MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 004650 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 0 AND ONLY BIT 0 SET?
(3) 004656 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
    ;;:*****>> ERROR <<*****
(3) 004660 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     ;/BIT 0 FAILED TO BIT SET.
(4)
    ;;:*****>> ERROR <<*****
(3) 004662 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 004664 1$: ;/TRY CLEARING BIT 0.
(3) 004664 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)
(4) * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) * MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 004710 005737 001126 TST $BDDAT
(3) 004714 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
(4)
    ;;:*****>> ERROR <<*****
(3) 004716 104003 ERRUR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     ;/BIT 0 FAILED TO CLEAR.
(4)
    ;;:*****>> ERROR <<*****
(3) 004720 2$:
```

(3) :/#  
(7) :\*\*\*\*\*  
(6) :\*TEST 24 \*TEST THAT CLOCK A BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED  
(7) :\*  
(7) :\*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(7) :\*F/FS OR GATES  
(8) :\*  
(8) :\* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(8) :\*  
(7) :\*  
(6) :\*\*\*\*\*

```
TST24: SCOPE
(5) 004720 000004
(4) 004722 012737 000100 001166   MOV     #100,$TIMES      ;;DO 100 ITERATIONS
(3)                                     ;;CLEAR THE BUFFER REGISTER.
(3)                                     ;;SET BIT 1.
(3)                                     ;;SET FOR ERROR TYPEOUT S/B.
(3)                                     ;;READ THE BUFFER REGISTER.
(3) 00473C 012737 000002 001124   MOV     #BIT1,$GDDAT
(4)                                     ;*
(4)                                     MOV     $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     MOV     @ABR,$BDDAT     ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 004756 023737 001124 001126   CMP     $GDDAT,$BDDAT  ;/DID BIT 1 AND ONLY BIT 1 SET?
(3) 004764 001402                   BEQ     1$             ;/IF SO-LETS TRY CLEARING IT.
(4)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 004766 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.  
(3) ;/BIT 1 FAILED TO BIT SET.  
(4)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```

(3) 004770 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 004772 1$: ;/TRY CLEARING BIT 1.
(3) 004772 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;*
(4) MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) ;*
(4) MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005016 005737 001126 TST $BDDAT
(3) 005022 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
(4)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 005024 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.  
(3) ;/BIT 1 FAILED TO CLEAR.  
(4)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 005026 2\$:

```
(3)                                     :/#
(7)                                     :*****
(6) *TEST 25 *TEST THAT CLOCK A BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****
(5) 005026 000004 TST25: SCOPE
(4) 005030 012737 000100 001166 MOV #100,$TIMES ;;DO 100 ITERATIONS
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 2.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 005036 012737 000004 001124 MOV #BIT2,$GDDAT
(4)                                     ;*
(4)                                     ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005064 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 2 AND ONLY BIT 2 SET?
(3) 005072 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
    :::*****>> ERROR <<*****
(3) 005074 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     ;/BIT 2 FAILED TO BIT SET.
(4)
    :::*****>> ERROR <<*****
(3) 005076 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 005100 1$: CLR $GDDAT ;/TRY CLEARING BIT 2.
(3) 005100 005037 001124 ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)
(4)                                     ;*
(4)                                     ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDA*.
(3) 005124 005737 001126 TST $BDDAT
(3) 005130 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
(4)
    :::*****>> ERROR <<*****
(3) 005132 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     ;/BIT 2 FAILED TO CLEAR.
(4)
    :::*****>> ERROR <<*****
(3) 005134 2$:
```





(3) :/\*  
(7) :\*\*\*\*\*  
(6) :\*TEST 27 \*TEST THAT CLOCK A BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED  
(7) :\*  
(7) :\*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(7) :\*F/FS OR GATES  
(8) :\*  
(8) :\* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(8) :\*  
(7) :\*  
(6) :\*\*\*\*\*

```
(5) 005242 000004 TST27: SCOPE  
(4) 005244 012737 000100 001166 MOV #100,$TIMES ;:DO 100 ITERATIONS  
(3) ;:/CLEAR THE BUFFER REGISTER.  
(3) ;:/SET BIT 4.  
(3) ;:/SET FOR ERROR TIMEOUT S/B.  
(3) ;:/READ THE BUFFER REGISTER.  
(3) 005252 012737 000020 001124 MOV #BIT4,$GDDAT  
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.  
(3) 005300 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 4 AND ONLY BIT 4 SET?  
(3) 005306 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.  
(4)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 005310 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.  
(3) ;/BIT 4 FAILED TO BIT SET.  
(4)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(3) 005312 000416 BR 2$ ;/BR TO END SUBTEST.  
(3) 005314 1$: ;/TRY CLEARING BIT 4.  
(3) 005314 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TIMEOUT IF ANY.  
(3) ;/NOW READ IT BACK.  
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.  
(3) 005340 005737 001126 TST $BDDAT  
(3) 005344 001401 BEQ 2$ ;/IF ZERO-NO ERROR.  
(4)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 005346 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.  
(3) ;/BIT 4 FAILED TO CLEAR.  
(4)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 005350 2\$:

```

(3)                                     :/
(7)                                     :*****
(6) *TEST 30 *TEST THAT CLOCK A BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****

```

```

(5) 005350 000004 TST30: SCOPE
(4) 005352 012737 000100 001166 MOV #100,$TIMES ;;DO 100 ITERATIONS
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 5.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 005360 012737 000040 001124 MOV #BIT5,$GDDAT
(4)                                     ;*
(4)                                     MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005406 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 5 AND ONLY BIT 5 SET?
(3) 005414 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)

```

::: \$ ERROR << \$

```

(3) 005416 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     ;/BIT 5 FAILED TO BIT SET.
(4)

```

::: \$ ERROR << \$

```

(3) 005420 000416 BR 2$ ;/BR TO FND SUBTEST.
(3) 005422 1$: ;/TRY CLEARING BIT 5.
(3) 005422 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)                                     ;*
(4)                                     MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005446 005737 001126 TST $BDDAT
(3) 005452 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
(4)

```

::: \$ ERROR << \$

```

(3) 005454 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     ;/BIT 5 FAILED TO CLEAR.
(4)

```

::: \$ ERROR << \$

```

(3) 005456 2$:

```









```
(3)                                     :/#
(7)                                     :*****
(6) :*TEST 35          *TEST THAT CLOCK A BUFFER REGISTER BIT 10 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 006106 000004 TST35: SCOPE
(4) 006110 012737 000100 001166      MOV      #100,$TIMES      ;,DO 100 ITERATIONS
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 10.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 006116 012737 002000 001124      MOV      #BIT10,$GDDAT
(4)                                     ;*
(4)                                     ;* MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     ;* MOV      @ABR,$BDDAT      ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006144 023737 001124 001126      CMP      $GDDAT,$BDDAT  ;/DID BIT 10 AND ONLY BIT 10 SET?
(3) 006152 001402      BEQ      1$             ;/IF SO-LETS TRY CLEARING IT.
(4)
      ;:;*****>> ERROR <<*****
(3) 006154 104003      ERROR      3             ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     ;/BIT 10 FAILED TO BIT SET.
(4)
      ;:;*****>> ERROR <<*****
(3) 006156 000416      BR        2$             ;/BR TO END SUBTEST.
(3) 006160      1$:      ;/TRY CLEARING BIT 10.
(3) 006160 005037 001124      CLR      $GDDAT        ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)
(4)                                     ;*
(4)                                     ;* MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     ;* MOV      @ABR,$BDDAT      ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006204 005737 001126      TST      $BDDAT
(3) 006210 001401      BEQ      2$             ;/IF ZERO-NO ERROR!
(4)
      ;:;*****>> ERROR <<*****
(3) 006212 104003      ERROR      3             ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     ;/BIT 10 FAILED TO CLEAR.
(4)
      ;:;*****>> ERROR <<*****
(3) 006214      2$:
```

```
(3)                                     :/ #
(7)                                     :*****
(6) *TEST 36 *TEST THAT CLOCK A BUFFER REGISTER BIT 11 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****
(5) 006214 000004 TST36: SCOPE
(4) 006216 012737 000100 001166 MOV #100,$TIMES ;;DO 100 ITERATIONS
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 11.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 006224 012737 004000 001124 MOV #BIT11,$GDDAT
(4)                                     ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006252 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 11 AND ONLY BIT 11 SET?
(3) 006260 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
    ;;:*****>> ERROR <<*****
(3) 006262 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     ;/BIT 11 FAILED TO BIT SET.
(4)
    ;;:*****>> ERROR <<*****
(3) 006264 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 006266 1$: ;/TRY CLEARING BIT 11.
(3) 006266 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006312 005737 001126 TST $BDDAT
(3) 006316 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
(4)
    ;;:*****>> ERROR <<*****
(3) 006320 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     ;/BIT 11 FAILED TO CLEAR.
(4)
    ;;:*****>> ERROR <<*****
(3) 006322 2$:
```



```

(3)                               :/*
(7)                               :*****
(6) *TEST 37 *TEST THAT CLOCK A BUFFER REGISTER BIT 12 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****

```

```

(5) 006322 000004 TST37: SCOPE
(4) 006324 012737 000100 001166 MOV #100,$TIMES ;;DO 100 ITERATIONS
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 12.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 006332 012737 010000 001124 MOV #BIT12,$GDDAT
(4)
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006360 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 12 AND ONLY BIT 12 SET?
(3) 006366 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)

```

::: \$>> ERROR <<\$

```

(3) 006370 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     ;/BIT 12 FAILED TO BIT SET.
(4)

```

::: \$>> ERROR <<\$

```

(3) 006372 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 006374 1$: ;/TRY CLEARING BIT 12.
(3) 006374 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006420 005737 001126 TST $BDDAT
(3) 006424 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4)

```

::: \$>> ERROR <<\$

```

(3) 006426 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     ;/BIT 12 FAILED TO CLEAR.
(4)

```

::: \$>> ERROR <<\$

(3) 006430 2\$:

```
(3)                                     :/N
(7) :*****
(6) :*TEST 40      *TEST THAT CLOCK A BUFFER REGISTER BIT 13 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 006430 000004 TST40: SCOPE
(4) 006432 012737 000100 001166 MOV #100,$TIMES ;;DO 100 ITERATIONS
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 13.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 006440 012737 020000 001124 MOV #BIT13,$GDDAT
(4)                                     ;*
(4)                                     ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006466 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 13 AND ONLY BIT 13 SET?
(3) 006474 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
    ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006476 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     ;/BIT 13 FAILED TO BIT SET.
(4)
    ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006500 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 006502 1$: ;/TRY CLEARING BIT 13.
(3) 006502 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)
(4)                                     ;*
(4)                                     ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006526 005737 001126 TST $BDDAT
(3) 006532 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
(4)
    ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006534 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     ;/BIT 13 FAILED TO CLEAR.
(4)
    ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006536 2$:
```

```
(3) ;/#
(7) .....
(6) *TEST 41 *TEST THAT CLOCK A BUFFER REGISTER BIT 14 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) .....
(5) 006536 000004
```

```
(4) 006540 012737 000100 001166 TST41: SCOPE
(3) MOV #100,$TIMES ;;DO 100 ITERATIONS
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 14.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 006546 012737 040000 001124 MOV #BIT14,$GDDAT
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006574 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 14 AND ONLY BIT 14 SET?
(3) 006602 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
```

```
::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```

```
(3) 006604 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 14 FAILED TO BIT SET.
(4)
```

```
::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```

```
(3) 006606 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 006610 1$: ;/TRY CLEARING BIT 14.
(3) 006610 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4)
```

```
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006634 005737 001126 TST $BDDAT
(3) 006640 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4)
```

```
::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```

```
(3) 006642 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 14 FAILED TO CLEAR.
(4)
```

```
::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```

```
(3) 006644 2$:
```

C 6

```

(3)                               :/*
(7)                               :*****
(6) *TEST 42                       *TEST THAT CLOCK A BUFFER REGISTER BIT 15 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****
(5) 006644 000004
(4) 006646 012737 000100 001166
(3)
(3)
(3)
(3)
(3)
(3) 006654 012737 100000 001124
(4)
(4) *
(4) *
(4) *
(3) 006702 023737 001124 001126
(3) 006710 001402
(4)

```

```

          ST42:  SCOPE
                   MOV      #100,$TIMES          ;;DO 100 ITERATIONS
                   ;/CLEAR THE BUFFER REGISTER.
                   ;/SET BIT 15.
                   ;/SET FOR ERROR TYPEOUT S/B.
                   ;/READ THE BUFFER REGISTER.
(4)                   MOV      #BIT15,$GDDAT
(4)                   *
(4)                   MOV      $GDDAT,@ABR        ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                   *
(4)                   MOV      @ABR,$BDDAT        ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3)                   CMP      $GDDAT,$BDDAT      ;/DID BIT 15 AND ONLY BIT 15 SET?
(3)                   BEQ      1$                   ;/IF SO-LETS TRY CLEARING IT.
(4)

```

```

::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006712 104003           ERROR 3             ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     ;/BIT 15 FAILED TO BIT SET.
(4)

```

```

::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006714 000416           BR      2$         ;/BR TO END SUBTEST.
(3) 006716                 1$:           ;/TRY CLEARING BIT 15.
(3) 006716 005037 001124   CLR      $GDDAT    ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)
(4) *
(4) *
(4) *
(3) 006742 005737 001126   *
(3) 006746 001401           MOV      $GDDAT,@ABR        ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     *
(4)                                     *
(4) *
(4) *
(3) 006742 005737 001126   *
(3) 006746 001401           MOV      @ABR,$BDDAT        ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(4)                                     TST      $BDDAT
(4)                                     BEQ      2$                   ;/IF ZERO-NO ERROR.

```

```

::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006750 104003           ERROR 3             ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     ;/BIT 15 FAILED TO CLEAR.
(4)

```

```

::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006752                 2$:
(1)
(2)

```



(3) :/#  
(7) :\*\*\*\*\*  
(6) :\*TEST 44 \*TEST THAT CLOCK B STATUS REGISTER BIT 7 CAN BE SET AND CLEARED  
(7) :\*  
(7) :\*CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(7) :\*F/FS OR GATES  
(8) :\*  
(8) :\* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(8) :\*  
(7) :\*  
(6) :\*\*\*\*\*

```
(5) 007060 000004 TST44: SCOPE
(4) 007062 012737 000100 001166 MOV #100,$TIMES ;:DO 100 ITERATIONS
(3) ;:/CLEAR THE STATUS REGISTER.
(3) ;:/SET BIT 7.
(3) ;:/SET FOR ERROR TYPEOUT S/B.
(3) ;:/READ THE STATUS REGISTER.
(3) 007070 012737 000200 001124 MOV #BIT7,$GDDAT
(4) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 007116 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 7 AND ONLY BIT 7 SET?
(3) 007124 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 007126 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.  
(3) ;/BIT 7 FAILED TO BIT SET.

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(3) 007130 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 007132 1$: ;/TRY CLEARING BIT 7.
(3) 007132 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 007156 005737 001126 TST $BDDAT
(3) 007162 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 007164 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.  
(3) ;/BIT 7 FAILED TO CLEAR.

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 007166 2\$:  
(2)

```

(3)          ;/#
(7)          :*****
(6)          *TEST 45      *TEST THAT CLOCK B STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(7)          *
(7)          *CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7)          *F/FS OR GATES
(8)          *
(8)          * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8)          *
(7)          *
(6)          :*****
(5) 007166 000004          TST45: SCOPE
(4) 007170 012737 000100 001166      MOV      #100,$TIMES          ;;DO 100 ITERATIONS
(3)                                          ;/CLEAR THE STATUS REGISTER.
(3)                                          ;/SET BIT 6.
(3)                                          ;/SET FOR ERROR TIMEOUT S/B.
(3)                                          ;/READ THE STATUS REGISTER.
(3) 007176 012737 000100 001124      MOV      #BIT6,$GDDAT
(4)                                          ;*
(4)                                          ;* MOV      $GDDAT,@BSR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4)                                          ;*
(4)                                          ;* MOV      @BSR,$BDDAT        ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 007224 023737 001124 001126      CMP      $GDDAT,$BDDAT      ;/DID BIT 6 AND ONLY BIT 6 SET?
(3) 007232 001402          BEQ      1$                    ;/IF SO-LETS TRY CLEARING IT.
(4)
      ;;:*****>> ERROR <<*****
(3) 007234 104005          ERROR      5                          ;/ERROR CLOCK BS STATUS REGISTER.
(3)                                          ;/BIT 6 FAILED TO BIT SET.
(4)
      ;;:*****>> ERROR <<*****
(3) 007236 000416          BR      2$                          ;/BR TO END SUBTEST.
(3) 007240          1$:          ;/TRY CLEARING BIT 6.
(3) 007240 005037 001124      CLR      $GDDAT                  ;/CLEAR S/B FOR TIMEOUT IF ANY.
(3)                                          ;/NOW READ IT BACK.
(4)
(4)          ;* MOV      $GDDAT,@BSR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4)          ;*
(4)          ;* MOV      @BSR,$BDDAT        ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 007264 005737 001126      TST      $BDDAT
(3) 007270 001401          BEQ      2$                          ;/IF ZERO-NO ERROR!
(4)
      ;;:*****>> ERROR <<*****
(3) 007272 104005          ERROR      5                          ;/ERROR-CLOCK B STATUS REGISTER.
(3)                                          ;/BIT 6 FAILED TO CLEAR.
(4)
      ;;:*****>> ERROR <<*****
(3) 007274          2$:
(2)
  
```

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```

;/#
*****
*TEST 46      *TEST THAT CLOCK B STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
*
*CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
*F/FS OR GATES
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
*****

```

```

TST46:  SCOPE
MOV     #100,$TIMES           ;;DO 100 ITERATIONS
                        ;/CLEAR THE STATUS REGISTER.
                        ;/SET BIT 5.
                        ;/SET FOR EPROR TIMEOUT S/B.
                        ;/READ THE STATUS REGISTER.
MOV     #BIT5,$GDDAT
;*     MOV     $GDDAT,@BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
;*     MOV     @BSR,$BDDAT      ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
CMP     $GDDAT,$BDDAT        ;/DID BIT 5 AND ONLY BIT 5 SET?
BEQ     1$                   ;/IF SO-LETS TRY CLEARING IT.

```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```

ERROR 5                   ;/ERROR CLOCK BS STATUS REGISTER.
                          ;/BIT 5 FAILED TO BIT SET.

```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```

BR     2$                   ;/BR TO END SUBTEST.
1$:   CLR     $GDDAT         ;/TRY CLEARING BIT 5.
                          ;/CLEAR S/B FOR TIMEOUT IF ANY.
                          ;/NOW READ IT BACK.
;*     MOV     $GDDAT,@BSR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
;*     MOV     @BSR,$BDDAT    ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
TST     $BDDAT
BEQ     2$                   ;/IF ZERO-NO ERROR.

```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```

ERROR 5                   ;/ERROR-CLOCK B STATUS REGISTER.
                          ;/BIT 5 FAILED TO CLEAR.

```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```

2$:

```



(3) ;/R  
(7) \*\*\*\*\*  
(6) \*TEST 47 \*TEST THAT CLOCK B STATUS REGISTER BIT 4 CAN BE SET AND CLEARED  
(7) \*  
(7) \*CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(7) \*F/FS OR GATES  
(8) \*  
(8) \* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(8) \*  
(7) \*  
(6) \*\*\*\*\*

(5) 007402 000004 TST47: SCOPE  
(4) 007404 012737 000100 001166 MOV #100,\$TIMES ;:DO 100 ITERATIONS  
(3) ;/CLEAR THE STATUS REGISTER.  
(3) ;/SET BIT 4.  
(3) ;/SET FOR ERROR TIMEOUT S/B.  
(3) ;/READ THE STATUS REGISTER.  
(3) 007412 012737 000020 001124 MOV #BIT4,\$GDDAT  
(4) ;\* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR  
(4) ;\* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.  
(3) 007440 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 4 AND ONLY BIT 4 SET?  
(3) 007446 001402 BEQ 1\$ ;/IF SO-LETS TRY CLEARING IT.  
(4)

::: \$>> ERROR <<\$

(3) 007450 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.  
(3) ;/BIT 4 FAILED TO BIT SET.  
(4)

::: \$>> ERROR <<\$

(3) 007452 000416 BR 2\$ ;/BR TO END SUBTEST.  
(3) 007454 1\$: CLR \$GDDAT ;/TRY CLEARING BIT 4.  
(3) 007454 005037 001124 ;/CLEAR S/B FOR TYPEOUT IF ANY.  
(3) ;/NOW READ IT BACK.  
(4) ;\* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR  
(4) ;\* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.  
(3) 007500 005737 001126 TST \$BDDAT  
(3) 007504 001401 BEQ 2\$ ;/IF ZERO-NO ERROR.  
(4)

::: \$>> ERROR <<\$

(3) 007506 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.  
(3) ;/BIT 4 FAILED TO CLEAR.  
(4)

::: \$>> ERROR <<\$

(3) 007510 2\$:  
(2)



(3) ;/ #  
(7) :\*\*\*\*\*  
(6) :\*TEST 51 \*TEST THAT CLOCK B STATUS REGISTER BIT 2 CAN BE SET AND CLEARED  
(7) :\*  
(7) :\*CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(7) :\*F/FS OR GATES  
(8) :\*  
(8) :\* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(8) :\*  
(7) :\*  
(6) :\*\*\*\*\*

(5) 007616 000004  
(4) 007620 012737 000100 001166 TST51: SCOPE  
(3) MOV #100,\$TIMES ;;DO 100 ITERATIONS  
(3) ;/CLEAR THE STATUS REGISTER.  
(3) ;/SET BIT 2.  
(3) ;/SET FOR ERROR TYPEOUT S/B.  
(3) ;/READ THE STATUS REGISTER.  
(3) 007626 012737 000004 001124 MOV #BIT2,\$GDDAT  
(4) ;\* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR  
(4) ;\* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.  
(3) 007654 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 2 AND ONLY BIT 2 SET?  
(3) 007662 001402 BEQ 1\$ ;/IF SO-LETS TRY CLEARING IT.  
(4)

;;:\*\*\*\*\*>> ERROR <<\*\*\*\*\*  
(3) 007664 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.  
(3) ;/BIT 2 FAILED TO BIT SET.  
(4)

;;:\*\*\*\*\*>> ERROR <<\*\*\*\*\*  
(3) 007666 000416 BR 2\$ ;/BR TO END SUBTEST.  
(3) 007670 1\$: ;/TRY CLEARING BIT 2.  
(3) 007670 005037 001124 CLR \$GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.  
(3) ;/NOW READ IT BACK.  
(4) ;\* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR  
(4) ;\* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.  
(3) 007714 005737 001126 TST \$BDDAT  
(3) 007720 001401 BEQ 2\$ ;/IF ZERO-NO ERROR.  
(4)

;;:\*\*\*\*\*>> ERROR <<\*\*\*\*\*  
(3) 007722 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.  
(3) ;/BIT 2 FAILED TO CLEAR.  
(4)

;;:\*\*\*\*\*>> ERROR <<\*\*\*\*\*  
(3) 007724 2\$:  
(2)

(3) ;/ #  
(7) :\*\*\*\*\*  
(6) :\*TEST 52 \*TEST THAT CLOCK B STATUS REGISTER BIT 1 CAN BE SET AND CLEARED  
(7) :\*  
(7) :\*CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(7) :\*F/FS OR GATES  
(8) :\*  
(8) :\* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(8) :\*  
(7) :\*

```
(6) :*****  
(5) 007724 000004 TST52: SCOPE  
(4) 007726 012737 000100 001166 MOV #100,$TIMES ;:DO 100 ITERATIONS  
(3) ;/CLEAR THE STATUS REGISTER.  
(3) ;/SET BIT 1.  
(3) ;/SET FOR ERROR TYPEOUT S/B.  
(3) ;/READ THE STATUS REGISTER.  
(3) 007734 012737 000002 001124 MOV #BIT1,$GDDAT  
(4) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
(4) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.  
(3) 007762 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 1 AND ONLY BIT 1 SET?  
(3) 007770 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.  
(4)
```

(3) ;:\*\*\*\*\*>> ERROR <<\*\*\*\*\*  
(3) 007772 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.  
(4) ;/BIT 1 FAILED TO BIT SET.

```
(3) ;:*****>> ERROR <<*****  
(3) 007774 000416 BR 2$ ;/BR TO END SUBTEST.  
(3) 007776 1$: CLR $GDDAT ;/TRY CLEARING BIT 1.  
(3) 007776 005037 001124 ;/CLEAR S/B FOR TYPEOUT IF ANY.  
(4) ;/NOW READ IT BACK.  
(4) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
(4) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.  
(3) 010022 005737 001126 TST $BDDAT  
(3) 010026 001401 BEQ 2$ ;/IF ZERO-NO ERROR!  
(4)
```

(3) ;:\*\*\*\*\*>> ERROR <<\*\*\*\*\*  
(3) 010030 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.  
(4) ;/BIT 1 FAILED TO CLEAR.

```
(3) ;:*****>> ERROR <<*****  
(3) 010032 2$:  
(2)
```



```
(3)                                     :/*  
(7) :*****  
(6) :*TFST 54      *TEST THAT CLOCK B BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED  
(7) :*  
(7) :*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(7) :*F/FS OR GATES  
(8) :*  
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(8) :*  
(7) :*  
(6) :*****  
(5) 010140 000004 TST54: SCOPE  
(4) 010142 012737 000100 001166      MOV      #100,$TIMES      ;;DO 100 ITERATIONS  
(3)                                     ;/CLEAR THE BUFFER REGISTER.  
(3)                                     ;/SET BIT 0.  
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.  
(3)                                     ;/READ THE BUFFER REGISTER.  
(3) 010150 012737 000001 001124      MOV      #BIT0,$GDDAT  
(4)                                     ;*      MOV      $GDDAT,@BBR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
(4)                                     ;*      MOV      @BBR,$BDDAT      ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.  
(3) 010176 023737 001124 001126      CMP      $GDDAT,$BDDAT      ;/DID BIT 0 AND ONLY BIT 0 SET?  
(3) 010204 001402      BEQ      1$      ;/IF SO-LETS TRY CLEARING IT.  
(4)                                     ;;:*****>> ERROR <<*****  
(3) 010206 104006      ERROR      6      ;/ERROR CLOCK BS BUFFER REGISTER.  
(3)                                     ;/BIT 0 FAILED TO BIT SET.  
(4)                                     ;;:*****>> ERROR <<*****  
(3) 010210 000416      BR      2$      ;/BR TO END SUBTEST.  
(3) 010212      1$:      ;/TRY CLEARING BIT 0.  
(3) 010212 005037 001124      CLR      $GDDAT      ;/CLEAR S/B FOR TYPEOUT IF ANY.  
(3)                                     ;/NOW READ IT BACK.  
(4)                                     ;*      MOV      $GDDAT,@BBR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
(4)                                     ;*      MOV      @BBR,$BDDAT      ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.  
(3) 010236 005737 001126      TST      $BDDAT  
(3) 010242 001401      BEQ      2$      ;/IF ZERO-NO ERROR.  
(4)                                     ;;:*****>> ERROR <<*****  
(3) 010244 104006      ERROR      6      ;/ERROR-CLOCK B BUFFER REGISTER.  
(3)                                     ;/BIT 0 FAILED TO CLEAR.  
(4)                                     ;;:*****>> ERROR <<*****  
(3) 010246      2$:
```

```

(3)                                     :/#
(7)                                     :*****
(6) :*TEST 55 *TEST THAT CLOCK B BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 010246 000004 TST55: SCOPE
(4) 010250 012737 000100 001166 MOV #100,$TIMES ;;DO 100 ITERATIONS
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 1.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 010256 012737 000002 001124 MOV #BIT1,$GDDAT
(4)                                     ;*
(4)                                     ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4)                                     ;*
(4)                                     ;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010304 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 1 AND ONLY BIT 1 SET?
(3) 010312 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 010314 104006 ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.
(3) ;/BIT 1 FAILED TO BIT SET.
(4)
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 010316 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 010320 1$: ;/TRY CLEARING BIT 1.
(3) 010320 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4)
(4) ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) ;*
(4) ;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010344 005737 001126 TST $BDDAT
(3) 010350 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4)
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 010352 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
(3) ;/BIT 1 FAILED TO CLEAR.
(4)
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 010354 2$:

```

```
(3) ;/N
(7) :*****
(6) :*TEST 56 *TEST THAT CLOCK B BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 010354 000004 TST56: SCOPE
(4) 010356 012737 000100 001166 MOV #100,$TIMES ;:DO 100 ITERATIONS
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 2.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 010364 012737 000004 001124 MOV #BIT2,$GDDAT
(4) ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010412 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 2 AND ONLY BIT 2 SET?
(3) 010420 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
(4) :::*****>> ERROR <<*****
(3) 010422 104006 ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.
(3) ;/BIT 2 FAILED TO BIT SET.
(4)
(4) :::*****>> ERROR <<*****
(3) 010424 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 010426 1$: ;/TRY CLEARING BIT 2.
(3) 010426 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(4) ;/NOW READ IT BACK.
(4) ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010452 005737 001126 TST $BDDAT
(3) 010456 001401 BEQ 2$ ;/IF ZERO-NO ERROR.
(4)
(4) :::*****>> ERROR <<*****
(3) 010460 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
(3) ;/BIT 2 FAILED TO CLEAR.
(4)
(4) :::*****>> ERROR <<*****
(3) 010462 2$:
```



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(5) 010462 000004  
(4) 010464 012737 000100 001166  
(3)  
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(3) 010472 012737 000010 001124  
(4)  
(4)  
(4)  
(3) 010520 023737 001124 001126  
(3) 010526 001402  
(4)

:/#  
:\*\*\*\*\*  
: \*TEST 57 \*TEST THAT CLOCK B BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED  
:  
: \*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
: \*F/FS OR GATES  
:  
: \* PROBABLE SYNC POINT FOR THIS TEST.: 'DEVICE OUT' 2 OCCURANCES PER PASS  
:  
:\*\*\*\*\*  
TST57: SCOPE  
MOV #100,\$TIMES ;:DO 100 ITERATIONS  
;/CLEAR THE BUFFER REGISTER.  
;/SET BIT 3.  
;/SET FOR ERROR TYPEOUT S/B.  
;/READ THE BUFFER REGISTER.  
MOV #BIT3,\$GDDAT  
;\* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR  
;\* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.  
CMP \$GDDAT,\$BDDAT ;/DID BIT 3 AND ONLY BIT 3 SET?  
BEQ 1\$ ;/IF SO-LETS TRY CLEARING IT.

::: \$ ERROR << \$

(3) 010530 104006  
(3)  
(4)

ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.  
;/BIT 3 FAILED TO BIT SET.

::: \$ ERROR << \$

(3) 010532 000416  
(3) 010534  
(3) 010534 005037 001124  
(3)  
(4)  
(4)  
(4)  
(3) 010560 005737 001126  
(3) 010564 001401  
(4)

BR 2\$ ;/BR TO END SUBTEST.  
1\$: ;/TRY CLEARING BIT 3.  
CLR \$GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.  
;/NOW READ IT BACK.  
;\* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR  
;\* MOV @BBR,\$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN \$BDDAT.  
TST \$BDDAT  
BEQ 2\$ ;/IF ZERO-NO ERROR!

::: \$ ERROR << \$

(3) 010566 104006  
(3)  
(4)

ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.  
;/BIT 3 FAILED TO CLEAR.

::: \$ ERROR << \$

(3) 010570 2\$:

```
(3)                                ;/#
(7)                                ::*****
(6)                                *TEST 60      *TEST THAT CLOCK B BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(7)                                :*
(7)                                *CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7)                                *F/FS OR GATES
(8)                                :*
(8)                                * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8)                                :*
(7)                                :*
(6)                                ::*****
(5) 010570 000004                   TST60:  SCOPE
(4) 010572 012737 000100 001166     MOV      #100,$TIMES      ;;DO 100 ITERATIONS
(3)                                     ;;CLEAR THE BUFFER REGISTER.
(3)                                     ;;SET BIT 4.
(3)                                     ;;SET FOR ERROR TYPEOUT S/B.
(3)                                     ;;READ THE BUFFER REGISTER.
(3) 010600 012737 000020 001124     MOV      #BIT4,$GDDAT
(4)                                     ;*
(4)                                     MOV      $GDDAT,@BBR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4)                                     ;*
(4)                                     MOV      @BBR,$BDDAT      ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010626 023737 001124 001126     CMP      $GDDAT,$BDDAT  ;/DID BIT 4 AND ONLY BIT 4 SET?
(3) 010634 001402                   BEQ      1$              ;/IF SO-LETS TRY CLEARING IT.
(4)                                     ;;:;*****>> ERROR <<*****
(3) 010636 104006                   ERROR    6              ;/ERROR CLOCK BS BUFFER REGISTER.
(3)                                     ;/BIT 4 FAILED TO BIT SET.
(4)                                     ;;:;*****>> ERROR <<*****
(3) 010640 000416                   1$:   BR      2$        ;/BR TO END SUBTEST.
(3) 010642 000416                   CLR      $GDDAT       ;/TRY CLEARING BIT 4.
(3) 010642 005037 001124           CLR      $GDDAT       ;/CLEAR S/B FOR TYPEOUT IF ANY.
(4)                                     ;/NOW READ IT BACK.
(4)                                     ;*
(4)                                     MOV      $GDDAT,@BBR   ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4)                                     ;*
(4)                                     MOV      @BBR,$BDDAT   ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010666 005737 001126           TST      $BDDAT
(3) 010672 001401                   BEQ      2$          ;/IF ZERO-NO ERROR.
(4)                                     ;;:;*****>> ERROR <<*****
(3) 010674 104006                   ERROR    6              ;/ERROR-CLOCK B BUFFER REGISTER.
(3)                                     ;/BIT 4 FAILED TO CLEAR.
(4)                                     ;;:;*****>> ERROR <<*****
(3) 010676 000416                   2$:
```



(3) :/ #  
(7) \*\*\*\*\*  
(6) \*TEST 62 \*TEST THAT CLOCK B BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED  
(7) \*  
(7) \*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(7) \*F/FS OR GATES  
(8) \*  
(8) \* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(8) \*  
(7) \*  
(6) \*\*\*\*\*

```
(5) 011004 000004 TST62: SCOPE  
(4) 011006 012737 000100 001166 MOV #100,$TIMES ;:DO 100 ITERATIONS  
(3) ;:/CLEAR THE BUFFER REGISTER.  
(3) ;:/SET BIT 6.  
(3) ;:/SET FOR ERROR TYPEOUT S/B.  
(3) ;:/READ THE BUFFER REGISTER.  
(3) 011014 012737 000100 001124 MOV #BIT6,$GDDAT  
(4) ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
(4) ;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.  
(3) 011042 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 6 AND ONLY BIT 6 SET?  
(3) 011050 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.  
(4)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 011052 104006 ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.  
(3) ;/BIT 6 FAILED TO BIT SET.  
(4)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(3) 011054 000416 BR 2$ ;/BR TO END SUBTEST.  
(3) 011056 1$: ;/TRY CLEARING BIT 6.  
(3) 011056 005037 001124 CLR $GDDAT ;/C FAR S/B FOR TYPEOUT IF ANY.  
(3) ;/NOW READ IT BACK.  
(4)
```

```
(4) ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
(4) ;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR PUT DATA IN $BDDAT.  
(3) 011102 005737 001126 TST $BDDAT  
(3) 011106 001401 BEQ 2$ ;/IF ZERO-NO ERROR.  
(4)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 011110 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.  
(3) ;/BIT 6 FAILED TO CLEAR.  
(4)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(3) 011112 2\$.

(3)  
(7)  
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3563  
3564  
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3566  
3572

:/#  
\*\*\*\*\*  
\*TEST 63 \*TEST THAT CLOCK B BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED  
\*  
\*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
\*F/FS OR GATES  
\*  
\* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
\*  
\*\*\*\*\*

```
TST63: SCOPE
MOV #100,$TIMES ;:DO 100 ITERATIONS
;:/CLEAR THE BUFFER REGISTER.
;:/SET BIT 7.
;:/SET FOR ERROR TYPEOUT S/B.
;:/READ THE BUFFER REGISTER.
MOV #BIT7,$GDDAT
;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
CMP $GDDAT,$BDDAT ;/DID BIT 7 AND ONLY BIT 7 SET?
BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.
;:/BIT 7 FAILED TO BIT SET.
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
BR 2$ ;/BR TO END SUBTEST.
1$: ;/TRY CLEARING BIT 7.
CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
;:/NOW READ IT BACK.
;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
TST $BDDAT
BEQ 2$ ;/IF ZERO-NO ERROR.
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
;:/BIT 7 FAILED TO CLEAR.
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
2$:
.SBTTL *
.SBTTL * PHASE 2 ADVANCED BASIC LOGIC TESTS
.SBTTL *
```

```

3573          :*****
(3)          :*TEST 64          *TEST THAT CLOCK A'S COUNT REGISTER IS CLEAR
(4)          :
(5)          :*
(5)          :*CLOCK A COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5)          :*F/FS OR GATES
(6)          :
(6)          :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(6)          :
(5)          :*
(4)          :*****
(3)          :*****
(2) 011220 000004 TST64: SCOPE
(1) 011222 012737 000002 001166 MOV #2,$TIMES      ;;DO 2 ITERATIONS
3574          :
3575          :
3576          :SELECT MODE 0.
3577          :CLEAR THE BUFFER REGISTER. BUFFER
3578          :REGISTER WILL BE TRANSFERRED TO
3579 011230 005037 001124 CLR $GDDAT      ;COUNT REGISTER SINCE THIS IS MODE 0.
3580          :
(1)          :* MOV $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
3581          :* MOV $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(1)          :
3582          :
3583 011254 005037 001124 CLR $GDDAT      ;EXPECT TO READ BACK ALL 0'S.
3584          :READ THE COUNT REGISTER - IT SHOULD BE CLEAR.
3585          :
(1)          :* MOV @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
3586 011270 005737 001126 TST $BDDAT
3587 011274 001401 BEQ 1$      ;BR IF YES TO NEXT TEST
3588          :
3589          :

```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```

3590 011276 104004 ERROR 4      ;ERROR - CLOCK A'S COUNTER REGISTER
3591          :NOT CLEAR.
3592          :
3593          :

```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```

3594 011300 1$:
3595          :*****
3596          :*TEST 65          *TEST CLOCK A'S COUNT REGISTER WITH 125252 PATTERN
(3)          :
(4)          :
(5)          :*
(5)          :*CLOCK A COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5)          :*F/FS OR GATES
(6)          :
(6)          :* PROBABLE SYNC POINT FOR THIS TEST:. 'DEVICE OUT' 2 OCCURANCES PER PASS
(6)          :
(5)          :*
(4)          :*****
(3)          :*****
(2) 011300 000004 TST65: SCOPE

```













```

3787 011766 012737 020000 001124      MOV   #BIT13,$GDDAT
3788          ;*   MOV   $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1)
3789          ;*   MOV   @ASR,$GDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
(1)
3790 012014 052737 010000 001124      BIS   #BIT12,$GDDAT
3791          ;*   MOV   $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1)
3792          ;*   MOV   @ASR,$BDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(1)
3793 012042 032737 000001 001126      BIT   #BIT00,$BDDAT
3794 012050 001001                    BNE   1$
3795          ;BR IF YES - NEXT TEST.
3796

```

;;; \$>> ERROR <<\$

```

3797 012052 104001                      ERROR   1                   ;ERROR - BIT00 OF CLOCK A'S STATUS REGISTER
3798                                         ;FAILED TO SET WHEN BIT13 WAS SET
3799                                         ;AND A MAINTENANCE ST1 GENERATED.
3800
3801

```

;;; \$>> ERROR <<\$

```

3802 012054                    1$:          CLR   $GDDAT          ;LEAVE SUBTEST WITH CLOCK CLEAR.
3803 012054 005037 001124          ;*   MOV   $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
3804          ;*
(1)
3805
3817
3818

```

```

(3) ;*****
(4) ;*TEST 74      *TEST THAT CLOCK A WILL INCREMENT - MODE 0 - RATE STP1 FIRST COUNT TEST
(4) ;*
(4) ;*COUNT TEST - THIS IS THE VERY FIRST TIME THAT THE COUNTER
(4) ;*HAS BEEN ASKED TO INCREMENT! WHAT WE ARE GOING TO DO IS
(4) ;*CLEAR THE BUFFER, SELECT MODE 0, RATE OF STP1.
(4) ;*NEXT WILL GENERATE THE STP1 THROUGH MAINTENANCE MODE (WE'VE
(4) ;*DONE THIS BEFORE IN A PREVIOUS TEST TO SEE IF THE FLAG WOULD SET)
(4) ;*AND SEE IF THE COUNTER HAS INCREMENTED.
(5) ;*
(5) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
(5) ;*
(4) ;*
(3) ;*****

```

```

(2) 012070 000004      TST74: SCOPE
3819          ;CLEAR CLOCK A.
3820          ;CLEAR BUFFER REGISTER.
3821
3822 012072 005037 001124      CLR   $GDDAT
3823          ;*   MOV   $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1) ;*
3824          ;*   MOV   $GDDAT,@ABR     ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(1) ;*          ;SELECT: MODE0! RATE 'STP1' AND ENABLE
3825          ;CLOCK A TO COUNT.
3826          ;NOW GENERATE A MAINTENANCE STP1 - AT
3827          ;THIS TIME THE CLOCK SHOULD COUNT ONCE.
3828

```

```
3829 012116 012737 000015 001124      MOV     #15,$GDDAT
3830                                          ;*      MOV     $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1)                                          ;*      MOV     @ASR,$GDDAT     ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
3831                                          ;*      BIS     #BIT12,$GDDAT
(1)
3832 012144 052737 010000 001124      ;*      MOV     $GDDAT,@ASR     ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
3833                                          ;*      MOV     #1,$GDDAT      ;FOR ERROR TYPEOUT (IF NEEDED) SET THE #1.
(1)                                          ;      MOV     @ACR,$BDDAT     ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
3834 012162 012737 000001 001124      ;*      CMP     $BDDAT,$GDDAT   ;DID THE COUNTER COUNT ONCE?
3835                                          ;      BEQ     1$              ;IF YES - BR NEXT TEST.
3836
(1)
3837 012200 023737 001126 001124
3838 012206 001401
3839
3840
```

::: \$>> ERROR <<\$

```
3841 012210 104011                      ERROR 11                      ;ERROR - COUNT A FAILED TO COUNT
3842                                          ;ONCE, WHEN ENABLED, MODE 0
3843                                          ;RATE 'STP1' SEE ABOVE COMMENTS
3844                                          ;FOR COMPLETE DESCRIPTION AND LIST
3845                                          ;OF EVENTS.
3846
3847
```

::: \$>> ERROR <<\$

```
3848 012212                               1$:
3849
3866
3867
(3)
(4)
(4)
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(3)
(2) 012212 000004
(1) 012214 012737 000001 001166
```

:\*\*\*\*\*  
: \*TEST 75 \*TEST THE ABILITY OF CLOCK A TO COUNT FROM ZERO TO OVERFLOW USING M STP1  
: \*  
: \*IN THIS TEST WE'LL COUNT THE COUNTER THROUGH EACH STEP  
: \*FROM ZERO TO OVERFLOW USING MAINTENANCE 'STP1' COUNTS.  
: \*IT IS KNOWN THAT THE COUNTER WILL INCREMENT ONCE USING  
: \*THE MAINTENANCE STP1 AND THAT THE COUNTER F/FS WILL  
: \*PASS ALL DATA BITS.  
: \*UNKNOW IS THE ABILITY OF THE F/F'S TO PROPAGATE THEIR  
: \*OVERFLOWS.  
: \*  
: \*IF IT IS DESIRED TO START THIS TEST AT A VALUE OTHER THAN  
: \*ZERO, CHANGE THE SECOND INSTR. OF THIS TEST TO A VALUE TO BE  
: \*LOADED INTO THE BUFFER TO THAT VALUE DESIRED.  
: \*  
: \* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
: \*  
: \*  
:\*\*\*\*\*

```
TST75: SCOPE
(1) 012214 012737 000001 001166      MOV     #1,$TIMES      ;;DO 1 ITERATION
3868
3869 012222 005037 001124              CLR     $GDDAT        ;START THE COUNTER FROM ZERO.
3870                                          ;NOTE: A VALUE OTHER THAN ZERO MAY BE
3871                                          ;PATCHED IN HERE IN ORDER THAT A COUNT
3872                                          ;MAY BE STARTED HIGHER.
```

```
3873 012226          1$:          ;DISABLE CLOCK A.
3874 012226 005037 001356      CLR      $TMDAT
3875          ;*          ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1)          ;*          ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
3876          ;*          ;LOAD THE COUNTER BUFFER WITH VALUE.
(1)          ;*          ;'1$' IS THE LOOP BACK POINT ON
3877          ;*          ;'LOOP ON TEST' (SW14=1) FEATURE. NOWMAL
3878          ;*          ;LOOP BACK POINT WILL BE '2$'.
3879
3880
3881
3882 012252 012737 000015 001356      MOV      #15,$TMDAT
3883          ;*          ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1)          ;*          ;ENABLE COUNTER TO COUNT. SELECTED:
3884          ;*          ;MODE 0, RATE 'STP1'
3885
3886 012270          2$:
(1)
(1)          ;*          ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
3887 012300 052737 010000 001356      BIS      #BIT12,$TMDAT ;GENERATE A MAINTENANCE 'STP1'. THIS
3888          ;*          ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1)          ;*          ;ONE VALUE.
3889          ;*          ;$GDDAT IS USED TO KEEP TRACK OF THE
3890 012316 005237 001124          INC      $GDDAT ;VALUE THE CLOCK SHOULD COUNT TO.
3891          ;*          ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
3892          ;*          ;DID COUNT OCCUR CORRECTLY?
3893          ;*          ;IF YES - BR TO '3$'.
(1)
3894
3895 012332 023737 001126 001124      CMP      $BDDAT,$GDDAT
3896 012340 001402          BEQ      3$
3897
3898          ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
3899 012342 104011          ERROR 11 ;ERROR - CLOCK A FAILED TO UPCOUNT
3900          ;CORRECTLY USING MODE 0 - RATE 'STP1'.
3901
3902          ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
3903 012344 000403          BR      4$
3904 012346 005737 001124          3$:      TST      $GDDAT ;DID WE ACHIEVE OVERFLOW TO ZERO YET?
3905 012352 001410          BEQ      5$ ;IF YES - BR NEXT TEST
3906
3907 012354 032777 040000 166556      4$:      BIT      #BIT14,@SWR ;LOOP CURRENT COUNT?
3908 012362 001742          BEQ      2$ ;BR IF NO TO NEXT COUNT UPDATE.
3909 012364 162737 000001 001124      SUB      #1,$GDDAT ;IF YES - DECREMENT EXPECTED AND RELOAD.
3910 012372 000715          BR      1$ ;GOTO RELOAD POINT.
3911
3912 012374          5$:          ;END SUBTEST
3913
3914          .SBTTL *
3915          .SBTTL * PHASE 3 CLOCK A COUNT FUNCTION TESTS
3916          .SBTTL *
3917
```

3927  
3928  
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(4)  
(5)  
(5)  
(5)  
(3)

```
*****
*TEST 76      *TEST THAT CLOCK A OVERFLOW WILL OCCUR
*
*NOW WE'LL TRY AND GENERATE 'A OVERFLOW L'
*WHICH SETS BDOS. WE'LL DO IT BY PRESETTING THE BUFFER
*AT 177777 AND GENERATE A MAINTENANCE STP1. WE ALREADY
*KNOW MAINTENANCE STP1'S WILL ADVANCE THE COUNTER.
*ALSO SEE IF 'MODE' FLG GETS SET.
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
*
*****
TST76: SCOPE
```

(2) 012374 000004

3929  
3930  
3931  
3932

```
CLR      $GDDAT      ;MAKE SURE CLOCK A CLEAR.
```

(1) 3933 012412 012737 177777 001124

```
;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
MOV      #177777,$GDDAT      ;PRESET BUFFER TO ALL ONES.
```

3934  
3935

```
;*      MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
;SELECT MODE 0; RATE STP4; GO.
;GENERATE A MAINTENANCE STP1.
```

(1) 3937 012430 012737 000015 001124

```
MOV      #15,$GDDAT
```

3938  
3939

```
;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
```

(1) 3940 012456 052737 010000 001124

```
;*      MOV      @ASR,$GDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
BIS      #BIT12,$GDDAT
```

3941  
3942

```
;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
```

3943  
3944

```
1$:      ;DID OVERFLOW BIT SET?
```

(1) 3945 012504 032737 000040 001126

```
;*      MOV      @ASR,$BDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
```

3946  
3947

```
BIT      #BIT05,$BDDAT
BNE      ?$          ;BR IF YES TO '2$'.
```

::: \$>> ERROR <<\$

3948 012514 104012

```
ERROR 12      ;ERROR BIT05 OF CSR CLOCK A FAILED
;TO SET ON OVERFLOW.
```

3949  
3950

::: \$>> ERROR <<\$

3951 012516 000411

```
BR      3$
```

3952  
3953  
3954

```
2$:      ;DID BIT07 - 'MODE' FLG SET?
```

(1) 3955 012530 032737 000200 001126

```
;*      MOV      @ASR,$BDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
BIT      #BIT07,$BDDAT
```

3956  
3957  
3958

```
;IT SHOULD SET WHEN BIT05 SETS.
BNE      3$          ;BR IF YES TO 3$.
```

::: \$>> ERROR <<\$

3959 012540 104012 ERROR 12 :OVERFLOW FAILED TO SET CLOCK A'S  
3960 :CSR BIT07 'MODE' FLG. IT  
3961 :HAD: HOWEVER SET BIT05 'OVERFLOW'  
3962 :FLAG.  
3963

::: \$>> ERROR <<\$

3964 012542 3\$:  
3974 :\*\*\*\*\*  
(3) :\*TEST 77 \*TEST IN CLOCK A THAT OVERFLOW IN MODE 0 CAUSE CLEARING OF 'ENB CNTR' F/  
(4) :\*  
(4) :\*WE'RE GOING TO SEE IF 'A RELOAD' H AND 'MODE 0' H CLEAR  
(4) :\* 'ENB CNTR A' F/F. 'A RELOAD' GENERATED ON OVERFLOW AND  
(4) :\* 'MODE 0' GENERATED BY 'MODE A0 (0)' AND 'MODE A0 (1)'  
(4) :\*ALSO SEE IF COUNTER REGISTER GETS RELOADED  
(5) :\*  
(5) :\* PROBABLE SYNC POINT FOR THIS TEST: 'LD BUFF A'  
(5) :\*  
(4) :\*  
(3) :\*\*\*\*\*

(2) 012542 000004 TST77: SCOPE  
3975 :\*\*\*\*\*  
3976 :MAKE SURE CLOCK A IS CLEAR.  
3977 012544 005037 001124 CLR \$GDDAT  
3978 :\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
(1) :\* PRESET BUFFER TO ALL ONES.  
3979 :\* SELECT MODE 0, RATE 'STP4': GO.  
3980 :\* GENERATE A MAINTENANCE STP1.  
3981 :\* THIS SHOULD CAUSE AN OVERFLOW  
3982 :\* OVERFLOW WILL GENERATE 'A RELOAD' H  
3983 :\* COMBINE THIS WITH MODE 0 AND WE  
3984 012560 012737 177777 001124 MOV #177777,\$GDDAT  
3985 :\* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR  
(1) :\* MOV #15,\$GDDAT  
3987 012576 012737 000015 001124 :\*  
3988 :\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
(1) :\*  
3989 :\* MOV @ASR,\$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.  
(1) :\*  
3990 012624 052737 010000 001124 :\* MOV #BIT12,\$GDDAT  
3991 :\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
(1) :\* SHOULD CLEAR 'ENB CNTR A' F/F.  
3992 :\*  
3993 :\*  
3994 :\* MOV @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.  
(1) :\*  
3995 012652 032737 000001 001356 :\* BIT #BIT00,\$TMDAT ;DID BIT00 'ENB CNTR A' F/F CLEAR?  
3996 012660 001402 :\* BEQ 1\$ ;BR IF YES - NEXT TEST.  
3997

::: \$>> ERROR <<\$

3998 012662 104012 ERROR 12 : 'ENB CNTR A' F/F NOT CLEARED  
3999 :ON OVERFLOW.  
4000





4065  
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;/#  
:\*\*\*\*\*  
: \*TEST 100 \*TEST THE ABILITY OF CLOCK A TO COUNT AT 1MHZ RATE PART 1  
: \*  
: \*THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT  
: \*IN RATE: 1MHZ PART 1  
: \*  
: \* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
: \*  
:\*\*\*\*\*

(3) 012710 000004  
(2) 012712 012737 000020 001166  
(1)  
(1)  
(1)  
(1)  
(1) 012720 005037 001124  
(2)  
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(2) 012744 012737 000003 001124  
(2)  
(2)  
(1) 012762 005000  
(1) 012764 005200  
(1) 012766 001376  
(1)  
(2)  
(2)  
(1) 013000 005737 001126  
(1) 013004 001011  
(1)  
(1)  
(2)  
(2)  
(1) 013016 032737 000040 001126  
(1)  
(1)  
(1) 013024 001001  
(2)

TST100: SCOPE  
MOV #20,\$TIMES ;;DO 20 ITERATIONS  
;/MAKE SURE CLOCK IS CLEAR.  
;/CLEAR THE BUFFER.  
;/SFLECT: MODE 0, RATE 1MHZ ; GO.  
CLR \$GDDAT  
;\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
;\* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR  
MOV #12,\$GDDAT  
;\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
CLR RO ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY  
INC RO ;/WILL AMOUNT TO 369MS ON A PDP-11/20  
BNE 1\$ ;/DID COUNTER INCREMENT AT ALL?  
;\* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.  
TST \$BDDAT  
BNE 2\$ ;/IF YES - BR NEXT TEST.  
;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.  
;\* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.  
BIT #BIT05,\$BDDAT  
;/AT HIGH RATE - SO WE'LL SEE IF 'OVERFLOW'  
;/F/F HAD SET.  
BNE 2\$ ;/BR IF YES NEXT TEST.

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(1) 013026 104012  
(1)  
(2)

ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO  
;/COUNT RATE: 1MHZ.

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(1) 013030

2\$:

4066  
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```

      ;/#
      *****
      *TEST 101      *TEST THE ABILITY OF CLOCK A TO COUNT AT 100KHZ RATE PART 1
      *
      *THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT
      *IN RATE: 100KHZ      PART 1
      *
      * PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
      *
      *****
      TST101: SCOPE
      MOV      #20,$TIMES      ;;DO 20 ITERATIONS
      ;;MAKE SURE CLOCK IS CLEAR.
      ;;CLEAR THE BUFFER.
      ;;SELECT: MODE 0, RATE 100KHZ ; GO.
      CLR      $GDDAT
      ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
      ;*      MOV      $GDDAT,@ABR      ;/ PUT DA'A FROM $GDDAT TO DEVICE REG ABR
      MOV      #14,$GDDAT
      ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
      CLR      R0      ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY
      INC      R0      ;/WILL AMOUNT TO 369MS ON A PDP-11/20
      BNE      1$      ;/DID COUNTER INCREMENT AT ALL?
      ;*      MOV      @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
      TST      $BDDAT
      BNE      2$      ;/IF YES - BR NEXT TEST.
      ;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.
      ;*      MOV      @ASR,$BDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
      BIT      #BIT05,$BDDAT
      ;/AT HIGH RATE - SO WE'LL SEE IF 'OVERFLOW'
      ;/F/F HAD SET.
      BNE      2$      ;/BR IF YES NEXT TEST.
      ;;:*****>> ERROR <<*****
      ERROR 12      ;/ERROR CLOCK A COUNTER FAILED TO
      ;/COUNT RATE: 100KHZ.
      ;;:*****>> ERROR <<*****
      2$:
  
```

(1) 013150



4068

(1)  
(5)  
(4)  
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(1)

013270 000004  
013272 012737 000020 001166  
  
013300 005037 001124  
  
013324 012737 000011 001124  
  
013342 005000  
013344 005200  
013346 001376  
  
013360 005737 001126  
013364 001011  
  
013376 032737 000040 001126  
  
013404 001001  
  
013406 104012  
  
013410

```
:/#  
:*****  
:*TEST 103 *TEST THE ABILITY OF CLOCK A TO COUNT AT 1KHZ RATE PART 1  
:*  
:*THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT  
:*IN RATE: 1KHZ PART 1  
:*  
:* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
:*  
:*****  
TST103: SCOPE  
MOV #20,$TIMES ;;DO 20 ITERATIONS  
;/  
;/  
;/  
CLR $GDDAT  
; * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
; * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
MOV #1!10,$GDDAT  
; * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
CLR R0 ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY  
1$: INC R0 ;/WILL AMOUNT TO 369MS ON A PDP-11/20  
BNE 1$ ;/DID COUNTER INCREMENT AT ALL?  
; * MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
TST $BDDAT  
BNE 2$ ;/IF YES - BR NEXT TEST.  
;/  
;/  
; * MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
BIT #BIT05,$BDDAT ;/AT HIGH RATE - SO WE'LL SEE IF 'OVERFLOW'  
;/  
;/  
BNE 2$ ;/BR IF YES NEXT TEST.  
;:  
;:  
ERROR <<*****  
ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO  
;/  
;:  
;:  
2$:
```









N 8

(4)  
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(5)  
(5)  
(5)  
(3)  
(2) 013766 000004

THE LOADING OF THE COUNT REGISTER IS A FUNCTION OF:  
\*ENB CNTR (0)' H + 'BUFFER LOAD' H

PROBABLE SYNC POINT FOR THIS TEST: 'RD STAT B'

\*\*\*\*\*  
ST107: SCOPE

4124 :GENERATE A SYNC PULSE  
4125 :CLEAR CLOCK A'S STATUS REG.  
4126 :CLEAR CLOCK A'S BUFFER REG. NOTE  
4127 :THIS WILL ALSO CAUSE ZEROS TO BE  
4128 :LOADED INTO THE COUNT REG.  
4129  
4130

(1) ;\* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.  
4131 014000 005737 001126 TST \$BDDAT  
4132 014004 005037 001124 CLR \$GDDAT

(1) ;\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
4134

(1) ;\* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR  
4135 014030 005237 001124 INC \$GDDAT ;SET THE ENABLE F/F. THIS

(1) ;\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
4137 :FROM BEING LOADED WHEN THE  
4138 :BUFFER IS LOADED.

4139 014044 012737 177777 001124 MOV #177777,\$GDDAT ;NOW LOAD THE BUFFER REG.

(1) ;\* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR  
4141 :TO THE COUNT REGISTER.  
4142 :DID ANY BITS GET TRANSFERRED TO  
4143 :THE COUNT REGISTER?

(1) ;\* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.  
4145 014072 005737 001126 TST \$BDDAT  
4146 014076 001401 BEQ 1\$ ;BR IF NO - NEXT TEST.  
4147

::: \$>> ERROR << \$

4148 014100 104012 ERROR 12 ;ERROR CLOCK A BUFFER TO COUNT REG TRANSFER  
4149 :OCCURRED EVEN THOUGH THE 'ENB CNTR A' F/F  
4150 :WAS SET.  
4151

::: \$>> ERROR << \$

4152 014102 1\$:

4153  
4162  
4163 :\*\*\*\*\*  
(3) ;\*TEST 110 \*TEST THAT CLOCK A IN MODE 1 DOES NOT CLEAR ENABLE ON OVERFLOW  
(4)  
(4) ;\*NOW W'RE GOING TO SEE IF 'A OVERFLOW' H WHEN GENERATED  
(4) ;\*BY CAUSING AN OVERFLOW DOESN'T CLEAR THE 'ENB CNTR A' F/F  
(4) ;\*WHEN IN MODE 1. IF F/F GETS CLEARED SUSPECT SIGNAL 'MODE 0' H.  
(4)  
(4) ;\*

(5)  
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 (3)  
 (2) 014102 000004  
 4164  
 4165  
 4166  
 4167  
 4168  
 4169  
 4170  
 4171  
 4172 014104 005037 001124  
 4173  
 (1)  
 4174 014120 012737 177777 001124  
 4175  
 (1)  
 4176 014136 012737 000415 001124  
 4177  
 (1)  
 4178  
 (1)  
 4179 014164 052737 010000 001356  
 4180  
 (1)  
 4181  
 (1)  
 4182 014212 032737 000001 001126  
 4183 014220 001001  
 4184  
 4185 014222 104012  
 4186  
 4187  
 4188 014224  
 4189  
 4201  
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 (3)

```

; *
; * PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
; *
; *****
TST110: SCOPE
; MAKE SURE CLOCK A IS CLEAR.
; SET BUFFER + COUNT REG. TO -1 FROM OVERFLOW
; SET: MODE 1; RATE STP1; GO.
; CAUSE A MAINTENANCE STP4. CLOCK 1
; SHOULD OVERFLOW - BUT THIS OVERFLOW SHOULD
; NOT CLEAR 'ENB CNTR A' F/F.
; DID BIT00, 'ENB CNTR A' F/F GET CLEARED?

CLR      $GDDAT
; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
MOV      $GDDAT,@ASR
MOV      #177777,$GDDAT
; / PUT DATA FROM $GDDAT TO DEVICE REG ABR
MOV      $GDDAT,@ABR
MOV      #415,$GDDAT
; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
MOV      $GDDAT,@ASR
; /READ DEVICE REG ASR,PUT DATA IN $TMDAT.
MOV      @ASR,$TMDAT
BIS      #BIT12,$TMDAT
; / PUT DATA FROM $TMDAT TO DEVICE REG ASR
MOV      $TMDAT,@ASR
; /READ DEVICE REG ASR,PUT DATA IN $BDDAT.
MOV      @ASR,$BDDAT
BIT      #BIT00,$BDDAT
BNE      1$
; BR IF NO TO NEXT TEST.

;:::*****>> ERROR <<*****
ERROR 12
; ERROR MODE 1 OPERATION 'ENB CNTR A' F/F
; WAS CLEARED ON OVERFLOW.

;:::*****>> ERROR <<*****

1$:
; *****
; *TEST 111 *TEST THAT A CLOCK A 'BUFFER TO COUNT REG' DOESN'T TAKE PLACE ON A MODE
; *
; *THIS WILL BE THE FIRST TIME WE'VE DONE A MODE 2 OPERATION
; *ON CLOCK A. THE FUNCTION OF THIS TEST WILL BE TO MAKE
; *SURE A BUFFER TO COUNT REGISTER DOESN'T TAKE PLACE ON OVERFLOW
; *THE COMBO THAT GAVE US BUFFER TO COUNT REG ON OVERFLOW BEFORE
; *IS ['MODE A1 (0)'' H + 'A RELOAD'' H]. WE'LL STILL BE GENERATING
; *
; * PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
; *
; *'A RELOAD'' H BUT SHOULD NOT GET.'MODE A1 (0)'' H AS THIS IS MODE 2.
; *
; *****

```



```
(4) ;*CLOCK PAGE.  
(5) ;*  
(5) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'RD STAT B'  
(5) ;*  
(4) ;*  
(3) ;*  
(2) 014344 000004 TST112: SCOPE  
4252 ;GENERATE A SYNC PULSE  
4253 ;  
4254 ;  
(1) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.  
4255 014356 005737 001126 TST $BDDAT ;MAKE SURE CLOCK A'S STAT REG IS CLEAR.  
4256 ;*  
4257 014362 005037 001124 CLR $GDDAT ;  
4258 ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
(1) ;* SET MODE 2.  
4259 ;GENERATE MAINTENANCE ST2.  
4260 ;THE COMBO OF MODE 2 + ST2 SHOULD  
4261 ;GET 'CNTR TO BUFF' H WHICH SHOULD  
4262 ;SET 'MODE FLG' F/F.  
4263 ;*  
4264 014376 012737 001000 001124 MOV #1000,$GDDAT ;  
4265 ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
(1) ;*  
(1) ;* MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.  
4267 014424 052737 002000 001124 BIS #BIT10,$GDDAT ;  
4268 ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
(1) ;* DID IT SET?  
4269 ;*  
4270 ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
(1) ;* BIT #BIT07,$BDDAT ;  
4271 014452 032737 000200 001126 BNE 1$ ;IF YES-BR TO NEXT TEST.  
4272 014460 001001 ;*  
4273 ;*  
4274 014462 104012 ERROR 12 ;ERROR - MODE 2 + ST2 DID NOT SET MODE FL.  
4275 ;*  
4276 014464 1$:  
4277 ;*  
4332 ;*  
(5) ;*****  
(4) ;*TEST 113 *TEST THAT PATTERN 052525 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS  
(5) ;*  
(5) ;*NOW WE'LL SHOT THE WORKS - WE KNOW FROM THE PREVIOUS TEST WE  
(5) ;*CAN GENERATE 'CNTR TO BUFF' H FROM MODE 2 + MAINTENANCE ST2, NOW  
(5) ;*WE WELL TRY AND GENERATE A TRANSFER BETWEEN THE COUNTER AND BUFFER  
(5) ;*USING A CB PAT PATTERN.  
(5) ;*IF NO DATA PATTERN GETS TRANSFERRED, SUSPECT SIG 'LD BUFFER'  
(5) ;*TO BE STUCK LOW AT THE MUX INPUT FOR THE BUFFER OR  
(5) ;*'CNTR TO BUFF' H NOT GETTING THROUGH TO THE LOAD INPUTS OF THE  
(5) ;*BUFFER REGISTER.  
(5) ;*IF JUST ONE OR A FEW BITS GETS MESSED UP ON THE XFERR-
```

(5)  
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(6)  
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(3) 014464 000004  
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(2)  
(2) 014476 005737 001126  
(1)  
(1)  
(1)  
(1)  
(1)  
(1) 014502 005037 001124  
(2)  
(2) 014516 012737 052525 001124  
(1)  
(2)  
(2) 014534 012737 001001 001124  
(1)  
(2)  
(2) 014552 005037 001124  
(1)  
(2)  
(2) 014576 052737 002000 001124  
(1)  
(2)  
(1) 014614 012737 052525 001124  
(1)  
(1)  
(2)  
(2) 014632 023737 001126 001124  
(1) 014640 001401  
(2)  
  
(1) 014642 104012  
(1)  
(1)  
(1)  
(1)  
(2)  
  
(1) 014644  
(1) 000011  
4333  
(5)

```
;*SUSPECT THE RESPECTIVE MUX OR ETCH BETWEEN THE COUNT REG
;*AND MUX. GOOD LUCK.
;*
;* PROBABLE SYNC POINT FOR THIS TEST:: 'RD STAT B'
;*
;*****
TST113: SCOPE
;GENERATE A SYNC PULSE
;*      MOV      @BSR,$BDDAT      ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
TST      $BDDAT
;*      CLR      $GDDAT
014476 005737 001126      ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
;*      MOV      #052525,$GDDAT
014502 005037 001124      CLR      $GDDAT
;*      MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
014516 012737 052525 001124 ;*      MOV      #1001,$GDDAT
;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
014534 012737 001001 001124 ;*      CLR      $GDDAT
;*      MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
014552 005037 001124      ;*      MOV      @ASR,$GDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
;*      CLR      $GDDAT
;*      MOV      $GDDAT,@ABR
014576 052737 002000 001124 ;*      MOV      @ASR,$GDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
;*      BIS      #BIT10,$GDDAT
014614 012737 052525 001124 ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
;*      MOV      #052525,$GDDAT ;RECORD $GDDAT (PATTERN) IN CASE WE
;*                                     ;NEED TO TYPE OUT AN ERROR.
;*                                     ;NOW READ BACK THE BUFFER REG.
014632 023737 001126 001124 ;*      MOV      @ABR,$BDDAT      ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
;*      CMP      $BDDAT,$GDDAT ;WAS THE TRANSFER SUCCESSFUL?
014640 001401      ;*      BEQ      1$              ;IF YES THEN BR TO NEXT TEST.
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

ERROR 12 ;ERROR FAILED TO XFERR 052525 PATTERN  
;CORRECTLY FROM COUNT TO BUFFER REG.  
;SEE INIT. COMMENT AS TO WHY  
;IT MIGHT HAVE GONE SOUR.

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

1\$: P P+1

;\*\*\*\*\*

```

(4) : *TEST 114 *TEST THAT PATTERN 125252 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
(5) : *
(5) : *NOW WE'LL SHOT THE WORKS - WE KNOW FROM THE PREVIOUS TEST WE
(5) : *CAN GENERATE 'CNTR TO BUFF' H FROM MODE 2 + MAINTENANCE ST2, NOW
(5) : *WE WELL TRY AND GENERATE A TRANSFER BETWEEN THE COUNTER AND BUFFER
(5) : *USING A CB PAT PATTERN.
(5) : *IF NO DATA PATTERN GETS TRANSFERRED, SUSPECT SIG 'LD BUFFER''
(5) : *TO BE STUCK LOW AT THE MUX INPUT FOR THE BUFFER OR
(5) : *'CNTR TO BUFF' H NOT GETTING THROUGH TO THE LOAD INPUTS OF THE
(5) : *BUFFER REGISTER.
(5) : *IF JUST ONE OR A FEW BITS GETS MESSED UP ON THE XFERR-
(5) : *SUSPECT THE RESPECTIVE MUX OR ETCH BETWEEN THE COUNT REG
(5) : *AND MUX. GOOD LUCK.

```

```

(6) : * PROBABLE SYNC POINT FOR THIS TEST:: 'RD STAT B''
(6) : *
(5) : *
(4) : *****

```

```

(3) 014644 000004

```

```

*ST114: SCOPE

```

```

(1) : GENERATE A SYNC PULSE
(1)
(2)
(2) : * MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(1) 014656 005737 001126 : * TST $BDDAT
(1) : MAKE SURE CLOCK A IS CLEAR.
(1) : PUT PATTERN 125252 INTO BUFFER REG.
(1) : IT SHOULD GET XFERRED TO COUNT REG.
(1) : SELECT: MODE 2, ENABLE.
(1) : NOW GENERATE A MAINTENANCE ST2.
(1) 014662 005037 001124 CLR $GDDAT
(2)
(2) : * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1) 014676 012737 125252 001124 : * MOV #125252,$GDDAT
(2)
(2) : * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(1) 014714 012737 001001 001124 : * MOV #1001,$GDDAT
(2)
(2) : * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1) 014732 005037 001124 : * CLR $GDDAT
(2)
(2) : * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(2)
(2) : * MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
(1) 014756 052737 002000 001124 : * BIS #BIT10,$GDDAT
(2)
(2) : * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1) 014774 012737 125252 001124 : * MOV #125252,$GDDAT
(1) : RECORD $GDDAT (PATTERN) IN CASE WE
(1) : NEED TO TYPE OUT AN ERROR.
(1) : NOW READ BACK THE BUFFER REG.
(2)
(2) : * MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(1) 015012 023737 001126 001124 : * CMP $BDDAT,$GDDAT
(1) 015020 001401 : * BEQ 1$
(2) : IF YES THEN BR TO NEXT TEST.

```

```

::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ >> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

```

(1) 015022 104012 ERROR 12 ;ERROR FAILED TO XFERP 125252 PATTERN  
(1) ;CORRECTLY FROM COUNT TO BUFFER REG.  
(1) ;SEE INIT. COMMENT AS TO WHY  
(1) ;IT MIGHT HAVE GONE SOJR.  
(2)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(1) 015024 000012 'S: P=P+1  
(1)  
4334  
4341  
4377  
(5)

\*\*\*\*\*  
;\*TEST 115 \*TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 1 WHEN STP2 IS GENER  
;\*THIS TEST IS DESIGNED TO MAKE SURE THAT WE DON'T CLEAR THE COUNT  
;\*REGISTER IN MODE 1 WHEN AN STP2 IS GENERATED.  
;\* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
\*\*\*\*\*  
TST115: SCOPE

(3) 015024 000004  
(1) ;MAKE SURE CLOCK A IS CLEAR.  
(1) ;LOAD ALL ONES INTO BUFFER COUNT REGS.  
(1) ;SET MODE 1.  
(1) ;GENERATE A MAINTENANCE STP2.  
(1) ;SEE IF IT CLEARED COUNT REG.

(1) 015026 005037 001124 CLR \$GDDAT  
(2) ;\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
(1) 015042 012737 177777 001124 ;\* MOV #177777,\$GDDAT  
(2) ;\* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR  
(1) 015060 012737 000200 001124 ;\* MOV #200,\$GDDAT  
(2) ;\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
(2) ;\* MOV @ASR,\$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.  
(1) 015106 052737 002000 001124 ;\* BIS #BIT10,\$GDDAT  
(2) ;\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
(2) ;\* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.  
(1) 015134 005737 001126 TST \$BDDAT  
(1) 015140 001001 BNE 1\$ ;BR IF NO - NEXT TEST.  
(2)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(1) 015142 104012 ERROR 12 ;ERROR CLOCK A MODE 1 + STP2 CLEARED COUNT REG.  
(1) ;TO SCOPE FIND OUT WHAT IS GENERATING  
(1) ;SIGNAL ON CLR INPUT OF COUNT REG.  
(2)

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(1) 015144  
4378  
(5)  
(4) :\*\*\*\*\*  
(5) :\*TEST 116 \*TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 2 WHEN STP2 IS GENER  
(5) :\*  
(5) :\*THIS TEST IS DESIGNED TO MAKE SURE THAT WE DON'T CLEAR THE COUNT  
(6) :\*REGISTER IN MODE 2 WHEN AN STP2 IS GENERATED.  
(6) :\*  
(6) :\* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
(5)  
(4) :\*\*\*\*\*  
(3) 015144 000004

```
TST116: SCOPE
;MAKE SURE CLOCK A IS CLEAR.
;LOAD ALL ONES INTO BUFFER COUNT REGS.
;SET MODE 2.
;GENERATE A MAINTENANCE STP2.
;SEE IF IT CLEARED COUNT REG.
(1) 015146 005037 001124 CLR $GDDAT
(2)
(2) * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1) 015162 012737 177777 001124 * MOV #177777,$GDDAT
(2) * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(1) 015200 012737 001000 001124 * MOV #1000,$GDDAT
(2) * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(2) * MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
(1) 015226 052737 002000 001124 * BIS #BIT10,$GDDAT
(2) * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(2) * MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(1) 015254 005737 001126 TST $BDDAT
(1) 015260 001001 BNE 1$ ;BR IF NO - NEXT TEST.
(2)
```

;;;\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(1) 015262 104012 ERROR 12 ;ERROR CLOCK A MODE 2 + STP2 CLEARED COUNT REG.  
(1) ;TO SCOPE FIND OUT WHAT IS GENERATING  
(1) ;SIGNAL ON CLR INPUT OF COUNT REG.  
(2)  
;;;\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(1) 015264  
4379  
4390  
4391  
(3) :\*\*\*\*\*  
(4) :\*TEST 117 \*TEST THAT MODE 3 + 'STP2' CLEARS A'S COUNT REGISTER.  
(4) :\*  
(4) :\*IN THIS TEST WE'LL DO A MODE 3 FOR THE FIRST TIME.  
(4) :\*MODE 3 + 'STP2' SHOULD CLEAR THE COUNT REGISTER.  
(4) :\*WE KNOW FROM A PREVIOUS TEST THAT 'INIT'L WAS ABLE TO  
(4) :\*CLEAR THE REG. AND ALSO THAT WE CAN GENERATE AN 'STP2' H.



(4)  
(5)  
(5)  
(5)  
(4)  
(3)  
(2) 015264 000004  
4392  
4393  
4394  
4395  
4396  
4397  
4398  
4399 015266 012737 001400 001124  
4400  
(1)  
4401 015304 012737 177777 001124  
4402  
(1)  
4403  
(1)  
4404 015332 052737 002000 001124  
4405  
(1)  
4406  
(1)  
4407 015360 005737 001126  
4408 015364 001401  
4409

;\*MODE A0 (1)' H + 'MODE A1 (1)' H + 'STP2' H = CLEARING SIGNAL.  
;\*PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
\*\*\*\*\*  
TST117: SCOPE  
;CLEAR CLOCK A + SELECT MODE 3.  
;LOAD ALL ONE'S TO BUFFER + COUNTER REGS.  
;GENERATE A MAINTENANCE 'STP2'.  
;THIS SHOULD CLEAR THE COUNT REG.  
;IS COUNT REG. CLEAR?  
MOV #1400,\$GDDAT  
;\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
MOV #177777,\$GDDAT  
;\* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR  
;\* MOV @ASR,\$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.  
BIS #BIT10,\$GDDAT  
;\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
;\* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.  
TST \$BDDAT  
BEQ 1\$ ;BR IF YES - NEXT TEST.

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

4410 015366 104012 ERROR 12 ;ERROR-CLOCK A-COUNT REGISTER FAILED TO  
4411 ;CLEAR IN MODE 3 ON 'STP2' PULSE.  
4412

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

4413 015370 1\$:  
4414  
4434  
4435

\*\*\*\*\*  
;\*TEST 120 \*TEST THE AUTODECREMENT FEATURE OF CLOCK A'S BUFFER  
;\*THIS IS GOING TO BE A BIGGIE-WITH TWO PARTS.  
;\*PART1: WE'RE LOADING THE BUFFER WITH ALL ONES; MODE 0; RATE STP1,  
WITH 'AUTO INC (1)' SET (FOR FIRST TIME!). NOW WE'LL GENERATE  
THE THING TO WATCH FOR IS THE EXPLOSIVE COMBO OF  
'MODE A0 (0)' H + 'MODE A1 (0)' H (MODE 0) + 'AUTO INC (1)' H +  
'A OVERFLOW' ALL FEEDING THE DOWN COUNT SIDE OF THE 74193 CHIP.  
THE RESULTS SHOULD BE 177776.  
;\*PART2: IF PART 1 WAS SUCCESSFUL WE'LL LOOK TO SEE IF  
THE COUNTER GOT LOADED WITH THE NEW VALUE 177776.  
THE HANG-UP HERE IS THAT 'A OVERFLOW' FEEDS A ONE SHOT  
THAT GENERATES 'A RELOAD' H. WE KNOW THAT WE CAN  
GET 'A RELOAD' H BUT THE BIG TEST HERE IS SEEING IF THAT  
ONE SHOT SPITS OUT 'A RELOAD' H TOO SOON TO CATCH THE BUFFER



```

4475                                     ;BUFFER REGISTER FAILED TO DOWN COUNT
4476                                     ;SEE ABOVE COMMENTS FOR SEQUENCE
4477                                     ;OF EVENTS.
4478 015546 000411          BR      2$      ;IF ERROR ONLY LOOP ON PART 1.
4479                                     ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

4480 015550          1$:      ;PART 2 DID NEW COUNT GET TRANSFERRED TO COUNT REGISTER?
4481                                     ;:READ THE COUNT REGISTER
4482                                     ;:READ DEVICE REG ACR,PUT DATA IN $BDDAT.
4483                                     ;:DID NEW VALUE OF THE BUFFER
(1)                                     ;:REGISTER GET PROPERLY LOADED INTO
4484 015560 023727 001126 177776  ;*      MOV      @ACR,$BDDAT      ;THE COUNT REGISTER?
4485                                     ;:BR IF YES - NEXT TEST.
4486                                     ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
4487 015566 001401          BEQ      2$
4488                                     ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

4489 015570 104012          ERROR  12      ;ERROR CLOCK A. NEW CONTENTS OF
4490                                     ;:BUFFER REGISTER FAILED TO BE PROPERLY
4491                                     ;:LOADED INTO COUNT REGISTER AFTER
4492                                     ;:AUTO DECREMENT.
4493                                     ;:SEE ABOVE COMMENTS FOR SEQUENCE OF EVENTS.
4494                                     ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

4495 015572          2$:      ;CLEAR AUTO INC OPTION.
4496 015572 005037 001124          CLR      $GDDAT
4497                                     ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1)                                     ;*      MOV      $GDDAT,@BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
4507                                     ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
4508                                     ;*****
(3)                                     ;*TEST 121          *TEST THAT CLOCK A'S 1 MHZ CLK CAN BE DISABLED
(4)                                     ;*
(4)                                     ;*FOR THIS TEST, WE'LL TRY DISABLING THE 1 MHZ CLOCK. TO DO THIS,
(4)                                     ;*WE'LL SET THE 'DISABLE OSC 1 MHZ', BIT 11 IN CLOCK B SR. THEN
(4)                                     ;*COUNTED OR OVERFLOWED, IF SO ERROR.
(4)                                     ;*THE UNKNOWN THING HERE IS BIT 11 SETTING THE DISABLE F/F THAT
(4)                                     ;*GATES WITH THE 1 MHZ FREQ TO PRODUCE 'A 1 MHZ CLK' L
(5)                                     ;*
(5)                                     ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT B'
(5)                                     ;*
(3)                                     ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(2) 015606 000004          TST121: SCOPE
(1) 015610 012737 000100 001166          MOV      #100,$TIMES      ;;DO 100 ITERATIONS
4509                                     ;:CLEAR CLOCK A.
4510                                     ;:SET THE 'DISABLE OSC 1 MHZ' F/F.
4511                                     ;:CLEAR THE BUFFER + COUNT REGS.
4512                                     ;:START CLOCK: RATE 1 MHZ, MODE 0, GO.
4513 015616 005037 001124          CLR      $GDDAT
4514                                     ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1)                                     ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
4515                                     ;*      MOV      #BIT11,$GDDAT
4516 015632 012737 004000 001124          MOV
4517

```

```
(1)
4518 015650 005037 001124      :*      MOV      $GDDAT,@BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
4519                                CLR      $GDDAT
(1)
4520 015664 012737 000003 001124 :*      MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
4521                                MOV      #3,$GDDAT
(1)
4522 015702 005000                :*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
4523 015704 105200                CLR      R0                      ;SHORT DELAY. WE ALLOW THIS DELAY TO
4524 015706 100376                1$:    INCB   R0                      ;OCCUR. IF THE 1 MHZ CLOCK IS DISABLED
4525                                BPL      1$                      ;NO CLOCKING OF CLOCK A WILL OCCUR.
4526                                ;SEE SOMETHING IN THE COUNT REGISTERS
(1)
4527 015720 005737 001126      :*      MOV      @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
4528 015724 001007                TST     $BDDAT                   ;DOES COUNT REG HAVE ANYTHING IN IT?
4529                                BNE     2$                      ;YES - REPORT ERROR!
(1)
4530 015736 105737 001126      :*      MOV      @ASR,$BDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
4531 015742 100001                TSTB   $BDDAT                   ;NO - BR NEXT TEST - NO ERROR.
4532                                BPL     3$
                                ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
4533 015744 104012                2$:    ERROR  12                   ;ERROR - UNABLE TO DISABLE 1 MHZ CLK
4534                                ;USING 'DISABLE OSC 1 MHZ' F/F
4535                                ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
4536                                ;CLEAR CLOCK A.
4537 015746 005037 001124      3$:    CLR      $GDDAT
4538                                :*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1)
```



4584  
4585  
4586  
4587  
4588  
4589  
4590  
4591  
4592  
4593  
4594

:TO SCOPE: CHECK LOAD + CLEAR INPUTS TO  
:COUNT REG TO SEE IF NOT BEING HELD LOW.  
:IF OK SEE IF WE'RE GETTING ANY 'CLOCK B' L  
:PULSES - WE SHOULD GET ONE EACH LOOP OF  
:THIS SUBTEST. 'CLOCK B' L COMES FROM  
:THE B CLOCK TIMING SECTION. THE RATE IS  
:1 MHZ. 'B 1 MHZ' L IS GENERATED BY  
: 'A 1 MHZ' H + 'FEED B TO A (1)' H.  
:THE 'A 1 MHZ' IS GENERATED BY 'MAINT  
:SIMUL 1 MHZ' IN CLOCK A.

::: \$>> ERROR <<\$

4595 016112  
4596  
4610  
4611

1\$:  
:\*\*\*\*\*  
:\*TEST 123 \*TEST THE ABILITY IF CLOCK B TO COUNT FROM ZERO TO OVERFLOW  
:\*  
:\*LAST TEST WE FOUND OUT WE COULD ADVANCE CLOCK A'S COUNTER,  
:\*SO IN THIS TEST WE'RE GOING TO GO FROM 0-377 COUNTING.  
:\*WE'LL USE THE SAME PROCEDURE AS LAST TEST TO GENERATE 'CLOCK B' L.  
:\*UNKNOWN IS THE ABILITY OF THE F/F'S TO PROPAGATE THEIR OVERFLOWS.  
:\*  
:\*IF IT IS DESIRED TO START THIS TEST AT A VALUE OTHER THAN 0, CHANGE  
:\*THE SECOND INSTR. OF THIS TEST TO A VALUE TO BE LOADED INTO THE BUFFER  
:\*TO THAT VALUE DESIRED.  
:\*  
:\*  
:\* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF B'  
:\*\*\*\*\*

(3)  
(4)  
(4)  
(4)  
(4)  
(4)  
(4)  
(4)  
(4)  
(4)  
(4)  
(5)  
(5)  
(5)  
(3)  
(2) 016112 000004  
(1) 016114 012737 000001 001166  
4612  
4613 016122 005037 001124  
4614  
4615  
4616  
4617 016126 005037 001356  
4618  
(1)  
4619  
4620 016142 012737 004000 001356  
4621  
(1)  
4622  
4623  
4624  
4625  
4626  
4627  
(1)  
4628  
4629  
4630

TST123: SCOPE  
MOV #1,\$TIMES ;:DO 1 ITERATION  
CLR \$GDDAT ;START THE COUNTER FROM ZERO.  
;NOTE: A VALUE OTHER THAN ZERO MAY BE  
;PATCHED IN HERE IN ORDER THAT A COUNT  
;MAY BE STARTED HIGHER.  
1\$: CLR \$TMDAT  
:\* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR  
;CLEAR CLOCK B, DISABLE 1 MHZ CLOCK A.  
MOV #BIT11,\$TMDAT  
:\* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR  
;LOAD VALUE INTO COUNT + BUFFER REGS.  
;'1\$' IS THE LOOP BACK POINT ON  
;'LOOP ON TEST' (SW14=1) FEATURE. NORMAL  
;LOOP BACK POINT WILL BE '2\$'.  
:\* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR  
;SELECT: 'DISABLE OSC 1 MHZ'; 'FEED B TO A';  
;RATE 1 MHZ.  
;GO. ENABL MUST BE SET AFTER 'FEED B TO A'

B 10

```

4631 016170 012737 004042 001356 MOV #4042,$TMDAT
4632 (1)
4633 016206 005237 001356 ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
4634 (1) ;* INC $TMDAT
4635 016222 ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
4636 2$: ;GENERATE A CLOCK PULSE.
4637 ;SHOULD CAUSE THE CLOCK TO
4638 ;INCREMENT ONCE.
4639 (1)
4640 016232 052737 004000 001356 ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
4641 (1) BIS #BIT11,$TMDAT
4642 016250 005237 001124 ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
4643 INC $GDDAT ;$GDDAT IS USED TO KEEP TRACK OF THE
4644 ;VALUE THE CLOCK SHOULD COUNT TO.
4645 (1) ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
4646 016264 123737 001126 001124 CMPB $BDDAT,$GDDAT ;DID THE COUNT OCCUR CORRECTLY?
4648 016272 001402 BEQ 3$ ;IF YES - BR '3$'.
4649
;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
4650 016274 104015 ERROR 15 ;ERROR CLOCK B FAILED TO UPCOUNT
4651 ;CORRECTLY - SEE COMMENTS AT SUB-TEST
4652 ;HEADING FOR MORE DETAILS.
4653
;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
4654 016276 000403 BR 4$
4655
4656 016300 105737 001124 3$: TSTB $GDDAT ;DID WE ACHIEVE OVERFLOW YET?
4657 016304 001410 BEQ 5$ ;
4658
4659 016306 032777 040000 162624 4$: BIT #BIT14,@SWR ;LOOP ON CURRENT COUNT?
4660 016314 001742 BEQ 2$ ;BR IF NO TO NEXT COUNT UPDATE.
4661 016316 162737 000001 001124 SUB #1,$GDDAT ;IF YES DECREMENT EXPECTED AND RELOAD.
4662 016324 000700 BR 1$ ;GO TO RELOAD POINT
4663
4664 016326 5$: ;END SUBTEST.
4665
4677 (3) ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(4) ;*TEST 124 *TEST THAT CLOCK B CAN GENERATE AN OVERFLOW
(4) ;*
(4) ;*NOW WE'LL TRY AND GENERATE 'B OVERFLOW' L WHICH SETS BIT 07.
(4) ;*WE'LL DO IT BY PRESETTING THE BUFFER TO 377 AND GENERATING A 'CLOCK B' L
(4) ;*WE ALREADY KNOW WE CAN ADVANCE THE COUNTER, WHAT WE
(4) ;*WANT TO SEE IS 'B OVERFLOW' L COME OVER AND DIRECT SET
(4) ;*'OVERFLOW FL B' F/F (BIT 07 IN CSR).
(5) ;*
(5) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF B'
(5) ;*

```





4716

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

4717 016516

2\$:

4718

4726

4727

(3)

(4)

(4)

(4)

(5)

(5)

(5)

(4)

(3)

(2)

(1)

016516 000004  
016520 012737 000001 001166

\*\*\*\*\*  
\*TEST 125 \*TEST THE INIT. ABILITY OF CLOCK B'S COUNT REG.  
\*ALL WE'RE GOING TO DO HERE IS TEST THE INITIALIZE INPUTS  
\*TO THE 74193 ICS THAT FORM THE COUNT REGISTER.  
\* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT A'  
\*\*\*\*\*

TST125: SCOPE

MOV #1,\$TIMES ;DO 1 ITERATION

;CLEAR CLOCK A.  
;CLEAR CLOCK B.  
;LOAD ALL ONES TO BUFFER + COUNT REGS.

4728

4729

4730

4731

4732

4733

(1)

4734

(1)

4735

4736

(1)

4737

4738

4739

4740

4741

4742

(1)

4743

4744

4745

4746

016526 005037 001124 CLR \$GDDAT  
;\* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
;\* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR  
016552 012737 000377 001124 MOV #377,\$GDDAT  
;\* MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR  
016570 004737 033676 JSR PC,\$RESET ;DO SYSTEM INIT - GENERATES 'INIT' H.  
016574 005037 001124 CLR \$GDDAT ;FIX \$GDDAT FOR ERROR TYPEOUT, IF NEEDED.  
;\* MOV @BCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN \$BDDAT.  
TST \$BDDAT ;SHOULD HAVE MADE IT AL ZEROS.  
016610 005737 001126 BEQ 1\$ ;BR IF YES - NEXT TEST.  
016614 001401

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

4747 016616

104007

ERROR 7

;ERROR CLOCK B - INIT FAILED TO CLEAR  
;COUNT REG.

4748

4749

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

4750 016620

1\$:

```

4752          ;*****
(3)          ;*TEST 126      *TEST THAT CLOCK B DOESN'T COUNT WHEN NO RATE IS SELECTED
(3)          ;*****
(2) 016620 000004          TST126: SCOPE
(1) 016622 012737 000100 001166      MOV      #100,$TIMES      ;;DO 100 ITERATIONS
4753                                     ;CLEAR CLOCK A.
4754                                     ;CLEAR CLOCK B.
4755                                     ;ZEROS TO BUFFER + COUNT REGS.
4756                                     ;ENABLE COUNTER TO COUNT - RATE - 0
4757                                     ;(NO RATE).
4758
4759 016630 005037 001124          CLR      $GDDAT
4760                                     ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1)                                     ;*      MOV      $GDDAT,@BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
4761                                     ;*      MOV      $GDDAT,@BBR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(1)                                     ;*      MOV      $GDDAT,@BBR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
4762                                     ;*      INC      $GDDAT
(1)                                     ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
4763 016664 005237 001124          INC      $GDDAT
4764                                     ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(1)                                     ;*      CLR      R0      ;DELAY FOR ANY COUNT THAT
4765 016700 005000          ;*      CLR      R0      ;COULD FALSELY OCCUR.
4766 016702 105200          1$:      INCB   R0      ;THIS DELAY APPROX. 369 MS ON A
4767 016704 001376          ;*      BNE     1$      ;PDP 11/20.
4768                                     ;DID ANY COUNT OCCUR?
4769
4770                                     ;DID ANY COUNT OCCUR?
4771
4772 (1)          ;*      MOV      @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
4773 016716 005737 001126          ;*      TST     $BDDAT
4774 016722 001401          ;*      BEQ     2$      ;IF NO BR TO NEXT TEST.
          ;*****
          ;*****>> ERROR <<*****
4775 016724 104014          ERROR 14      ;ERROR - CLOCK B COUNTED WHEN ENABLED BUT
4776                                     ;NO RATE SELECTED. BETTER FIND OUT
4777                                     ;WHATS GENERATING 'CLOCK B' L PULSES.
4778
          ;*****
          ;*****>> ERROR <<*****
4779 016726          2$:
4780
4831
  
```

4832  
(1)  
(5)  
(4)  
(5)  
(5)  
(5)  
(6)  
(6)  
(6)  
(6)  
(5)  
(4)  
(3)  
(2)  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)  
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016726 000004  
016730 012737 000020 001166  
016736 005037 001124  
016772 012737 000003 001124  
017010 005000  
017012 005200  
017014 001376  
017026 005737 001126  
017032 001010  
017044 105737 001126  
017050 100401  
017052 104014  
017054

```
:/#  
*****  
*TEST 127 *TEST THE ABILITY OF CLOCK B TO COUNT AT 1MHZ PART 1  
*  
*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT  
*IN RATE: 1MHZ PART1  
*  
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT A'  
*  
*****  
TST127: SCOPE  
MOV #20,$TIMES ;;DO 20 ITERATIONS  
;/CLEAR CLOCK A.  
CLR $GDDAT  
;/CLEAR CLOCK B.  
;/CLEAR THE BUFFER + COUNT REGS.  
;/SELECT: RATE: 1MHZ ; GO.  
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
MOV #1!2,$GDDAT  
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.  
1$: INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.  
BNE 1$ ;/ON A PDP-11/20.  
;/DID COUNTER COUNT AT ALL?  
;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
TST $BDDAT  
BNE 2$ ;/BR IF YES - NEXT TEST.  
;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.  
TSTB $BDDAT  
;/COUNT TO OVERFLOW - SO WE'LL SEE IF  
;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.  
BMI 2$ ;/BR IF SET - NEXT TEST.  
:::#####>> ERROR <<#####  
ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT  
;/AT 1MHZ RATE.  
:::#####>> ERROR <<#####  
2$:
```

4833

;/#

```
(1)
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(4) *****
(5) *TEST 130 *TEST THE ABILITY OF CLOCK B TO COUNT AT 100KHZ PART 1
(5) *
(5) *THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
(5) *IN RATE: 100KHZ PART1
(6) *
(6) * PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT A'
(6) *
(5) *
(4) *****
(3) 017054 000004
(2) 017056 012737 000020 001166 TST130: SCOPE
(1) MOV #20,$TIMES ;;DO 20 ITERATIONS
(1)
(1) 017064 005037 001124 CLR $GDDAT ;/CLEAR CLOCK A.
(1) ;/CLEAR CLOCK B.
(1) ;/CLEAR THE BUFFER + COUNT REGS.
(1) ;/SELECT: RATE: 100KHZ ; GO.
(2)
(2) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(2) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(2) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(1) 017120 012737 000005 001124 MOV #14,$GDDAT
(2) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(1)
(1) 017136 005000 CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.
(1) 017140 005200 1$: INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.
(1) 017142 001376 BNE 1$ ;/ON A PDP-11/20.
(1)
(1) ;/DID COUNTER COUNT AT ALL?
(2)
(2) ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1) 017154 005737 001126 TST $BDDAT
(1) 017160 001010 BNE 2$ ;/BR IF YES - NEXT TEST.
(1)
(2) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(1) 017172 105737 001126 TSTB $BDDAT
(1) ;/COUNT TO OVERFLOW - SO WE'LL SEE IF
(1) ;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
(1) 017176 100401 BMI 2$ ;/BR IF SET - NEXT TEST.
(2)
(2) :::*****>> ERROR <<*****
(1) 017200 104014 ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT
(1) ;/AT 100KHZ RATE.
(2)
(2) :::*****>> ERROR <<*****
(1) 017202 2$:
```

4834

;/#

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```
*****
*TEST 131      *TEST THE ABILITY OF CLOCK B TO COUNT AT 10KHZ PART 1
*
*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
*IN RATE: 10KHZ      PART1
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT A'
*
```

(3) 017202 000004  
(2) 017204 012737 000020 001166

TST131: SCOPE

MOV #20,\$TIMES ;;DO 20 ITERATIONS

(1)  
(1)  
(1)  
(1)  
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017212 005037 001124

CLR \$GDDAT ;/CLEAR CLOCK A.

;/CLEAR CLOCK B.  
;/CLEAR THE BUFFER + COUNT REGS.  
;/SELECT: RATE: 10KHZ ; GO.

(2)  
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```
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
```

(1) 017246 012737 000007 001124  
(2)

MOV #1.6,\$GDDAT

```
;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
1$: CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.
INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.
BNE 1$ ;/ON A PDP-11/20.
```

(1)  
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(1)  
(2)

017264 005000  
017266 005200  
017270 001376

```
;/DID COUNTER COUNT AT ALL?
;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 2$ ;/BR IF YES - NEXT TEST.
```

(1)  
(1)  
(2)

017302 005737 001126  
017306 001010

```
;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
;* MOV @BSR,$BDDAT
TSTB $BDDAT
;/COUNT TO OVERFLOW - SO WE'LL SEE IF
;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
;/BR IF SET - NEXT TEST.
```

(1)  
(1)  
(2)

017324 100401

BMI 2\$

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(1)  
(1)  
(2)

017326 104014

ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT  
;/AT 10KHZ RATE.

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

(1) 017330

2\$:

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```
;/#  
*****  
*TEST 132 *TEST THE ABILITY OF CLOCK B TO COUNT AT 1KHZ PART 1  
*  
*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT  
*IN RATE: 1KHZ PART1  
*  
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT A'  
*  
*****  
TST132: SCOPE  
MOV #20,$TIMES ;;DO 20 ITERATIONS  
;/CLEAR CLOCK A.  
CLR $GDDAT ;/CLEAR CLOCK B.  
;/CLEAR THE BUFFER + COUNT REGS.  
;/SELECT: RATE: 1KHZ ; GO.  
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
MOV #10,$GDDAT  
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.  
1$: INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.  
BNE 1$ ;/ON A PDP-11/20.  
;/DID COUNTER COUNT AT ALL?  
;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
TST $BDDAT  
BNE 2$ ;/BR IF YES - NEXT TEST.  
;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.  
TSTB $BDDAT  
;/COUNT TO OVERFLOW - SO WE'LL SEE IF  
;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.  
BNI 2$ ;/BR IF SET - NEXT TEST.  
::: <<*****>> ERROR <<*****>>  
ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT  
;/AT 1KHZ RATE.  
::: <<*****>> ERROR <<*****>>  
2$:
```

4836

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(2) 017460 012737 000020 001166  
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(1) 017466 005037 001124  
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(1) 017522 012737 000011 001124  
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(1) 017542 005200  
(1) 017544 001376  
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(1) 017556 005737 001126  
(1) 017562 001010  
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(1) 017574 105737 001126  
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(1) 017600 100401  
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(1) 017602 104014  
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(1) 017604

:/#

```
*****
*TEST 133      *TEST THE ABILITY OF CLOCK B TO COUNT AT 100HZ PART 1
*
*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
*IN RATE: 100HZ      PART1
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT A'
*
*****
TST133: SCOPE
        MOV      #20,$TIMES      ;;DO 20 ITERATIONS
        ;;CLEAR CLOCK A.
        CLR      $GDDAT
        ;;CLEAR CLOCK B.
        ;;CLEAR THE BUFFER + COUNT REGS.
        ;;SELECT: RATE: 100HZ ; GO.
        ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
        ;*      MOV      $GDDAT,@BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
        ;*      MOV      $GDDAT,@BBR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
        MOV      #11,$GDDAT
        ;*      MOV      $GDDAT,@BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
        CLR      R0
        1$: INC      R0
        BNE      1$              ;/NOW WE'LL DO A LITTLE DELAY.
                                   ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.
                                   ;/ON A PDP-11/20.
                                   ;/DID COUNTER COUNT AT ALL?
        ;*      MOV      @BCR,$BDDAT      ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
        TST      $BDDAT
        BNE      2$              ;/BR IF YES - NEXT TEST.
        ;*      MOV      @BSR,$BDDAT      ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
        TSTB     $BDDAT
                                   ;/COUNT TO OVERFLOW - SO WE'LL SEE IF
                                   ;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
        BMI      2$              ;/BR IF SET - NEXT TEST.
        ;: *****
        ;: *****
        ERROR 14              ;/ERROR CLOCK B - COUNTER FAILED TO COUNT
        ;: *****
        2$: *****
```

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017604 000004  
017606 012737 000020 001166  
017614 005037 001124  
017650 012737 000017 001124  
017666 005000  
017670 005200  
017672 001376  
017704 005737 001126  
017710 001010  
017722 105737 001126  
017726 100401  
017730 104014  
017732

```
;/#  
:*****  
*TEST 134 *TEST THE ABILITY OF CLOCK B TO COUNT AT LINE-FREQ PART 1  
:*****  
*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT  
*IN RATE: LINE-FREQ PART1  
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT A'  
:*****  
TST134: SCOPE  
MOV #20,$TIMES ;;DO 20 ITERATIONS  
;/CLEAR CLOCK A.  
CLR $GDDAT  
;/CLEAR CLOCK B.  
;/CLEAR THE BUFFER + COUNT REGS.  
;/SELECT: RATE: LINE-FREQ ; GO.  
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
MOV #1.16,$GDDAT  
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.  
INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.  
BNE 1$ ;/ON A PDP-11/20.  
;/DID COUNTER COUNT AT ALL?  
;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
TST $BDDAT  
BNE 2$ ;/BR IF YES - NEXT TEST.  
;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.  
TSTB $BDDAT  
;/COUNT TO OVERFLOW - SO WE'LL SEE IF  
;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.  
BMI 2$ ;/BR IF SET - NEXT TEST.  
: :$>> ERROR <<$>>  
ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT  
;/AT LINE-FREQ RATE.  
: :$>> ERROR <<$>>  
2$:
```

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017732 000004

017734 005037 001124

017770 012737 000377 001124

020006 012737 004042 001124

020024 005237 001124

020040 012737 000001 001124

020066 052737 004000 001124

020114 005737 001126

```
*****  
*TEST 135 *TEST THE 'FEED B TO A' 24 BIT COUNTER FEATURE OF CLOCKS A + B  
*  
*WE'RE GOING TO TEST CLOCKS A+B AS A 24 BIT COUNTER; THAT IS;  
*WE'RE GOINT TO TAKE THE OVERFLOW FROM CLOCK B AND FEED IT INTO  
*CLOCK A.  
*  
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF B'  
*  
*****  
TST135: SCOPE
```

```
;CLEAR CLOCK A.  
;CLEAR CLOCK B.  
;CLEAR A'S BUFFER + COUNT REGISTERS.  
;PRESET B'S BUFFER + COUNT TO -1 FROM  
;OVERFLOW.  
;SELECT: 'DISABLE OSC 1 MHZ'; RATE 1 MHZ;  
;'FEED B TO A'  
;SET ENABL. MUST BE SET AFTER 'FEED B TO A'.  
;ENABLE CLOCK A; MODE 0; RATE 0.  
;SIMULATE A 1 MHZ PULSE - THIS PULSE  
;WILL CLOCK CLOCK B'S COUNTER  
;REGISTER. AN OVERFLOW WILL  
;OCCUR - THAT OVERFLOW SHOULD  
;CLOCK CLOCK A'S COUNT REGISTER.  
;DID CLOCK A'S COUNT REG GET CLOCKED?
```

```
CLR $GDDAT  
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
MOV #377,$GDDAT  
;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
MOV #4042,$GDDAT  
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
INC $GDDAT  
;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
MOV #1,$GDDAT  
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;* MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.  
BIS #BIT11,$GDDAT  
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
TST $BDDAT
```



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(2) 020124 000004

:/#  
:\*\*\*\*\*  
:\*TEST 136 \*TEST THAT THE TRAILING EDGE OF STP1 WILL INCR. COUNTER  
:  
:\*IN THIS TEST WE'LL SEE IF WE CATCH THE FIRST COUNT  
:\*AFTER STP1 COMES IN AND SETS THE ENABLE F/F ('ST1 ENB COUNTER'  
:\*SET).  
:\*WHAT WE SHOULD SEE IS THE LEADING EDGE OF ST1 COME  
:\*IN AND SET THE ENB F/F AND THE TRAILING EDGE TRIGGER  
:\*A 'CLOCK A' PULSE TO INCREMENT THE COUNTER.  
:\*WE KNOW FROM A PREVIOUS TEST THAT AN STP1 WILL  
:\*COME IN AND SET 'ENABL CNTR A' F/F AND THAT THE  
:\*COUNTER WILL INCREMENT, SO WHATS HAPPENING IS WE'RE ACCUALLY  
:\*LOOKING AT THE TRAILING EDGE OF STP1 TO SEE IF ITS DOING  
:\*THE INCREMENTING  
:  
:  
:\* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
:  
:\*\*\*\*\*  
:ST136: SCOPE

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020126 012737 000001 001356  
020144 005037 001124  
020170 052737 010000 001124  
020206 012737 000001 001124  
020224 023737 001126 001124  
020232 001401

MOV #BIT0,\$TMDAT  
:\* MOV \$TMDAT,@ASR  
CLR \$GDDAT  
:\* MOV \$GDDAT,@ABR  
:\* MOV @ASR,\$GDDAT  
BIS #BIT12,\$GDDAT  
:\* MOV \$GDDAT,@ASR  
MOV #1,\$GDDAT  
:\* MOV @ACR,\$BDDAT  
CMP \$BDDAT,\$GDDAT  
BEQ 1\$

;CLR CLK A, SET 'ST1 ENB COUNTER'.;RATE:STP1.  
;CLR COUNT + BUFFER REGS.  
;GENERATE A MAINTENANCE ST1.  
;THE LEADING EDGE SHOULD CAUSE  
;'.ENABL CNTR A' F/F TO SET (CSR BIT 00).  
;THE TRAILING EDGE SHOULD CLOCK  
;THE COUNTER ONCE.  
;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR  
;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR  
;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.  
;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR  
;SET S/B FOR ERROR TYPEOUT IF NEEDED.  
;READ THE COUNT REGISTER.  
;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.  
;DID THE COUNT REG COUNT ONCE?  
;BR IF YES TO NEXT TEST.

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

4944  
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020234 104012

ERROR 12

;ST1 FAILED TO COUNT  
;CLOCK A'S COUNT REG. AFTER SETTING  
;'ENABL CNTR A' - SEE TEST HEADING

LPA-KW11K DIAGNOSTIC MD-11-CRLPG-B  
CRLPGB.P11 08-AUG-79 10:30

MACY11 30G(1063) 08-AUG-79 10:30 PAGE 6-111  
T136 \*TEST THAT THE TRAILING EDGE OF STP1 WILL INCR. COUNTER

SEQ 0131

4948  
4949

:COMMENTS

:::#####>> ERROR <<#####

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4951 020236  
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18:

5042

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020240 012737 000020 001166  
  
020246 005037 001356  
  
020302 012737 004000 001356  
  
020330 052737 000405 001356  
  
020346 012700 177766  
020352  
  
020362 052737 004000 001356  
  
020410 005737 001126  
020414 001002

```
*****  
*TEST 137 *TEST CLOCK A'S 100KHZ DIVIDER  
*  
*IN THIS TEST WE'LL SEE IF THE 100KHZ DIVIDER WILL DIVIDE 1MHZ  
*BY 10 TO GIVE US A 100KHZ CLK L PULSE.  
*TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND  
*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100KHZ  
*PULSES.  
*THEN WE'LL GENERATE 9 MORE 1MHZ PULSES AND MAKE  
*SURE THAT WE DON'T GET ANOTHER 100KHZ PULSE.  
*  
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
*  
*****  
TST137: SCOPE  
MOV #20,$TIMES ;:DO 20 ITERATIONS  
  
;/CLEAR CLOCK B.  
;/CLEAR CLOCK A.  
;/CLEAR A'S BUFFER + COUNT REGS.  
;/DISABLE THE 1MHZ OSC.  
;/ENABLE CNTR, RATE: 100KHZ ;MODE.  
  
CLR $TMDAT  
* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
* MOV $TMDAT,@ABR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR  
MOV #BIT11,$TMDAT  
* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
BIS #401!4,$TMDAT  
* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
;/SET TO GENFRATE ON 1MHZ PULSES  
MOV #-10.,R0  
1$: ;/GENFRATE 1 1MHZ PULSE  
;/HAS COUNTER ADVANCED ANY?  
* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
BIS #BIT11,$TMDAT  
* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DAIA IN $BDDAT.  
TST $BDDAT  
BNE 10$ ;/IF 30 EXIT THIS LOOP.
```

```
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.  
(1) ;/OSC., THE DIVIDER COULD HAVE  
(1) ;/AND COUNT LEFT IN IT.  
(1) ;/AFTER THIS LOOP ,WE SHOULD BE SUNK.  
(1) 020416 005200 INC R0 ;/DONE 10. 1MHZ PULSES?  
(1) 020420 001354 BNE 1$ ;/IF NOT - DO ANOTHER.  
(1) 020422 012737 000001 001124 10$: MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.  
(1) ;/READ THE COUNTER.  
(2) ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
(1) 020440 023737 001126 001124 CMP $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?  
(1) 020446 001402 BEQ 2$ ;/IF YES - NEXT CHECK.  
(2) ;:::#####>> ERROR <<#####  
(1) 020450 104012 ERROR 12 ;/ERROR - CLOCK A - 100KHZ - PULSE  
(1) ;/NOT GENERATED WHEN 10 1MHZ PULSES  
(2) ;:::#####>> ERROR <<#####  
(1) 020452 000430 BR 4$  
(1) 020454 012700 000011 2$: MOV #9.,R0 ;/GET THE NUMBER OF '1 MHZ' H PULSES  
(1) 020460 3$: ;/GENERATE 9 1MHZ PULSES  
(2) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
(1) 020470 052737 004000 001356 BIS #BIT11,$TMDAT  
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
(1) 020506 005300 DEC R0 ;/INORDER TO CHECK TO SEE THAT  
(1) 020510 001363 BNE 3$ ;/WE DON'T GENERATE ANOTHER 100KHZ PULSE.  
(1) ;/READ THE COUNTER  
(2) ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
(1) 020522 023737 001126 001124 CMP $BDDAT,$GDDAT ;/WAS ANOTHER 100KHZ PULSE GENERATED?  
(1) 020530 001401 BEQ 4$ ;/NO-GO TO NEXT TEST!  
(1) ;:::#####>> ERROR <<#####  
(1) 020532 104012 ERROR 12 ;/ERROR CLOCK A WE SEEM TO HAVE  
(1) ;/GENERATED A SECOND 100KHZ PULSE  
(1) ;/ON ONLY 9 1MHZ PULSES.  
(2) ;:::#####>> ERROR <<#####  
(1) 020534 4$:
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:/#
:*****
:TEST 140 *TEST CLOCK A'S 10KHZ DIVIDER
:
:+IN THIS TEST WE'LL SEE IF THE 10KHZ DIVIDER WILL DIVIDE 100KHZ
:+BY 10 TO GIVE US A 10KHZ CLK L PULSE.
:+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
:+PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 10KHZ
:+PULSES.
:+THEN WE'LL GENERATE 9 MORE 100KHZ PULSES AND MAKE
:+SURE THAT WE DON'T GET ANOTHER 10KHZ PULSE.
:
:PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
:*****
TST140: SCOPE
MOV #20,$TIMES ;:DO 20 ITERATIONS
;:/CLEAR CLOCK B.
;:/CLEAR CLOCK A.
;:/CLEAR A'S BUFFER + COUNT REGS.
;:/DISABLE THE 1MHZ OSC.
;:/ENABLE CNTR, RATE: 10KHZ ;MODE.

CLR $TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV $TMDAT,@ABR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
MOV #BIT11,$TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #40!6,$TMDAT
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;:/SET TO GENERATE ON 1MHZ PULSES
MOV #-100.,R0
1$: ;/GENERATE 1 1MHZ PULSE
;:/HAS COUNTER ADVANCED ANY?
;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #BIT11,$TMDAT
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 10$ ;/IF SO EXIT THIS LOOP.

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020534 000004
020536 012737 000020 001166
020544 005037 001356
020600 012737 004000 001356
020626 052737 000407 001356
020644 012700 177634
020650
020660 052737 004000 001356
020706 005737 001126
020712 001002

```

```

(1)                                     :/NOTE: WHEN WE DISABLED THE 1 MHZ.
(1)                                     :/OSC., THE DIVIDER COULD HAVE
(1)                                     :/AND COUNT LEFT IN IT.
(1)                                     :/AFTER THIS LOOP, WE SHOULD BE SUNK.
(1) 020714 005200           INC      R0          :/DONE 100. 1MHZ PULSES?
(1) 020716 001354           BNE      1$        :/IF NOT - DO ANOTHER.
(1) 020720 012737 000001 001124 10$: MOV     #1,$GDDAT    :/SET FOR ERROR TYPEOUT IF NEEDED.
(1)                                     :/READ THE COUNTER.
(2)                                     :
(2)                                     ;*    MOV     @ACR,$BDDAT    :/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(1) 020736 023737 001126 001124     CMP     $BDDAT,$GDDAT :/DID THE COUNTER ADVANCE ONCE?
(1) 020744 001402           BEQ     2$        :/IF YES - NEXT CHECK.
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 020746 104012           ERROR   12        :/ERROR - CLOCK A - 10KHZ - PULSE
(1)                                     :/NOT GENERATED WHEN 10 100KHZ PULSES
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$

(1) 020750 000430           BR      4$
(1) 020752 012700 000143     2$:   MOV     #99.,R0    ;/GET THE NUMBER OF '1 MHZ' H PULSES
(1) 020756                                     3$:   :/GENERATE 9 100KHZ PULSES
(2)
(2)                                     ;*    MOV     @ASR,$TMDAT    :/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(1) 020766 052737 004000 001356     BIS     #BIT11,$TMDAT
(2)
(2)                                     ;*    MOV     $TMDAT,@ASR   :/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1) 021004 005300           DEC     R0          :/INORDER TO CHECK TO SEE THAT
(1) 021006 001363           BNE     3$        :/WE DON'T GENERATE ANOTHER 10KHZ PULSE.
(1)                                     :/READ THE COUNTER
(2)
(2)                                     ;*    MOV     @ACR,$BDDAT    :/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(1) 021020 023737 001126 001124     CMP     $BDDAT,$GDDAT :/WAS ANOTHER 10KHZ PULSE GENERATED?
(1) 021026 001401           BEQ     4$        :/NO-GO TO NEXT TEST.
(1)
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 021030 104012           ERROR   12        :/ERROR CLOCK A WE SEEM TO HAVE
(1)                                     :/GENERATED A SECOND 10KHZ PULSE
(1)                                     :/ON ONLY 9 100KHZ PULSES.
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$

(1) 021032                                     4$:
  
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(1) 021124 052737 000411 001356
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(1) 021142 012700 176030
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(1) 021156 052737 004000 001356
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(1) 021204 005737 001126
(1) 021210 001002

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:/#
*****
*TEST 141 *TEST CLOCK A'S 1KHZ DIVIDER
*
*IN THIS TEST WE'LL SEE IF THE 1KHZ DIVIDER WILL DIVIDE 10KHZ
*BY 10 TO GIVE US A 1KHZ CLK L PULSE.
*TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 1KHZ
*PULSES.
*THEN WE'LL GENERATE 9 MORE 10KHZ PULSES AND MAKE
*SURE THAT WE DON'T GET ANOTHER 1KHZ PULSE.
*
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
*****
TST141: SCOPE
      MOV      #20,$TIMES      ;;DO 20 ITERATIONS
      ;;CLEAR CLOCK B.
      ;;CLEAR CLOCK A.
      ;;CLEAR A'S BUFFER + COUNT REGS.
      ;;DISABLE THE 1MHZ GSC.
      ;;ENABLE CNTR, RATE: 1KHZ ;MODE.
      CLR      $TMDAT
      ;*      MOV      $TMDAT,@BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
      ;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
      ;*      MOV      $TMDAT,@ABR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
      MOV      #BIT11,$TMDAT
      ;*      MOV      $TMDAT,@BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
      ;*      MOV      @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
      BIS      #401!10,$TMDAT
      ;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
      ;;SET TO GENERATE ON 1MHZ PULSES
      MOV      #-1000.,R0
      1$:
      ;;GENERATE 1 1MHZ PULSE
      ;;HAS COUNTER ADVANCED ANY?
      ;*      MOV      @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
      BIS      #BIT11,$TMDAT
      ;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
      ;*      MOV      @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
      TST      $BDDAT
      BNE      10$              ;/IF SO EXIT THIS LOOP.

```

```
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.  
(1) ;/OSC. THE DIVIDER COULD HAVE  
(1) ;/AND COUNT LEFT IN IT.  
(1) ;/AFTER THIS LOOP WE SHOULD BE SUNK.  
(1) 021212 005200 INC R0  
(1) 021214 001354 BNE 1$ ;/DONE 1000. 1MHZ PULSES?  
(1) ;/IF NOT - DO ANOTHER.  
(1) 021216 012737 000001 001124 10$: MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.  
(1) ;/READ THE COUNTER.  
(2) ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
(1) 021234 023737 001126 001124 CMP $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?  
(1) 021242 001402 BEQ 2$ ;/IF YES - NEXT CHECK.  
(2) ;:::*****>> ERROR <<*****  
(1) 021244 104012 ERROR 12 ;/ERROR - CLOCK A - 1KHZ - PULSE  
(1) ;/NOT GENERATED WHEN 10 10KHZ PULSES  
(2) ;:::*****>> ERROR <<*****  
(1) 021246 000430 BR 4$  
(1) 021250 012700 001747 2$: MOV #999.,R0 ;/GET THE NUMBER OF '1 MHZ' H PULSES  
(1) 021254 3$: ;/GENERATE 9 10KHZ PULSES  
(2) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
(1) 021264 052737 004000 001356 BIS #BIT!1,$TMDAT  
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
(1) 021302 005300 DEC R0 ;/INORDER TO CHECK TO SEE THAT  
(1) 021304 001363 BNE 3$ ;/WE DON'T GENERATE ANOTHER 1KHZ PULSE.  
(1) ;/READ THE COUNTER  
(2) ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
(1) 021316 023737 001126 001124 CMP $BDDAT,$GDDAT ;/WAS ANOTHER 1KHZ PULSE GENERATED?  
(1) 021324 001401 BEQ 4$ ;/NO-GO TO NEXT TEST.  
(2) ;:::*****>> ERROR <<*****  
(1) 021326 104012 ERROR 12 ;/ERROR CLOCK A WE SEEM TO HAVE  
(1) ;/GENERATED A SECOND 1KHZ PULSE  
(1) ;/ON ONLY 9 10KHZ PULSES.  
(2) ;:::*****>> ERROR <<*****  
(1) 021330 4$:
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021330 000004  
021332 012737 000020 001166  
  
021340 005037 001356  
  
021374 012737 004000 001356  
  
021422 052737 000413 001356  
  
021440 012700 154360  
021444  
  
021454 052737 004000 001356  
  
021502 005737 001126  
021506 001002

```

;/#
*****
*TEST 142 *TEST CLOCK A'S 100HZ DIVIDER
*
*IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
*BY 10 TO GIVE US A 100HZ CLK L PULSE.
*TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
*PULSES.
*THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
*
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
*****
TST142: SCOPE
MOV #20,$TIMES ;:DO 20 ITERATIONS
;:/CLEAR CLOCK B.
;:/CLEAR CLOCK A.
;:/CLEAR A'S BUFFER + COUNT REGS.
;:/DISABLE THE 1MHZ OSC.
;:/ENABLE CNTR, RATE: 100HZ ;MODE.

CLR $TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV $TMDAT,@ABR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
MOV #BIT11,$TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #401!12,$TMDAT
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;:/SET TO GENERATE ON 1MHZ PULSES

MOV #-10000.,R0
1$: ;/GENERATE 1 1MHZ PULSE
;:/HAS COUNTER ADVANCED ANY?
;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #BIT11,$TMDAT
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 10$ ;/IF SO EXIT THIS LOOP.

```

```
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.  
(1) ;/OSC., THE DIVIDER COULD HAVE  
(1) ;/AND COUNT LEFT IN IT.  
(1) ;/AFTER THIS LOOP, WE SHOULD BE SUNK.  
(1) 021510 005200 INC R0 ;/DONE 10000. 1MHZ PULSES?  
(1) 021512 001354 BNE 1$ ;/IF NOT - DO ANOTHER.  
(1) 021514 012737 000001 001124 10$: MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.  
(1) ;/READ THE COUNTER.  
(2) ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
(1) 021532 023737 001126 001124 CMP $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?  
(1) 021540 001402 BEQ 2$ ;/IF YES - NEXT CHECK.  
(2) ;:;*****>> ERROR <<*****  
(1) 021542 104012 ERROR 12 ;/ERROR - CLOCK A - 100HZ - PULSE  
(1) ;/NOT GENERATED WHEN 10 1KHZ PULSES  
(2) ;:;*****>> ERROR <<*****  
(1) 021544 000430 BR 4$  
(1) 021546 012700 023417 2$: MOV #9999.,R0 ;/GET THE NUMBER OF '1 MHZ' H PULSES  
(1) 021552 3$: ;/GENERATE 9 1KHZ PULSES  
(2) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
(1) 021562 052737 004000 001356 BIS #BIT11,$TMDAT  
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
(1) 021600 005300 DEC R0 ;/INORDER TO CHECK TO SEE THAT  
(1) 021602 001363 BNE 3$ ;/WE DON'T GENERATE ANOTHER 100HZ PULSE.  
(1) ;/READ THE COUNTER  
(2) ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
(1) 021614 023737 001126 001124 CMP $BDDAT,$GDDAT ;/WAS ANOTHER 100HZ PULSE GENERATED?  
(1) 021622 001401 BEQ 4$ ;/NO-GO TO NEXT TEST!  
(1) ;:;*****>> ERROR <<*****  
(1) 021624 104012 ERROR 12 ;/ERROR CLOCK A WE SEEM TO HAVE  
(1) ;/GENERATED A SECOND 100HZ PULSE  
(1) ;/ON ONLY 9 1KHZ PULSES.  
(2) ;:;*****>> ERROR <<*****  
(1) 021626 4$:  
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5146  
(5) ;:;*****  
(4) ;*TEST 143 *TEST CLOCK B'S 100KHZ DIVIDER
```

```
(5) ;*  
(5) ;+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ  
(5) ;+BY 10 TO GIVE US A 100HZ CLK L PULSE.  
(5) ;+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND  
(5) ;*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ  
(5) ;*PULSES.  
(5) ;*THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE  
(5) ;*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.  
(5) ;*  
(6) ;*  
(6) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
(6) ;*  
(4) ;*****  
(3) 021626 000004 TST143: SCOPE  
(2) 021630 012737 000020 001166 MOV #20,$TIMES ;:DO 20 ITERATIONS  
(1) ;/  
(1) ;/CLEAR CLOCK B.  
(1) ;/CLEAR CLOCK A.  
(1) ;/  
(1) ;/CLEAR B'S BUFFER + COUNT REGS.  
(1) ;/DISABLE THE 1MHZ OSC.  
(1) ;/RATE: 100KHZ  
(1) ;/ENABLE CLOCK B.  
(1) 021636 005037 001356 CLR $TMDAT  
(2) ;*  
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
(2) ;*  
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
(2) ;*  
(1) 021672 012737 004040 001356 ;*  
(2) ;* MOV $TMDAT,@BBR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BBR  
(2) ;* MOV #BIT11!BIT5,$TMDAT  
(2) ;*  
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
(1) 021720 052737 000004 001356 ;*  
(2) ;* MOV @BSR,$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.  
(2) ;* BIS #4,$TMDAT  
(2) ;*  
(1) 021736 005237 001356 ;*  
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
(2) ;* INC $TMDAT  
(1) 021752 012700 177766 ;*  
(1) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
(1) ;* MOV #-10.,R0 ;/SET TO GENERATE 10. 1MHZ PULSES  
(1) 021756 1$: ;/GENERATE 1 1MHZ PULSE  
(1) ;/HAS THE COUNTER ADVANCED?  
(2) ;*  
(1) 021766 052737 004000 001356 ;*  
(2) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
(2) ;* BIS #BIT11,$TMDAT  
(2) ;*  
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
(2) ;*  
(1) 022014 005737 001126 ;*  
(1) 022020 001002 ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
(1) ;* TST $BDDAT  
(1) ;* BNE 10$ ;/EXIT LOOP IF SO.  
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.  
(1) ;/ OSC., THE DIVIDER COULD HAVE
```

```

(1)                                     :/ HAD ANY COUNT IN IT.
(1)                                     :/AFTER THIS LOOP, WE SHOULD BE SUNK.
(1)
(1) 022022 005200          INC      R0          :/DONE 10. 1MHZ PULSES?
(1) 022024 001354          BNE      1$          :/IF NOT - DO ANOTHER.
(1)
(1) 022026 012737 000001 001124 10$: MOV     #1,$GDDAT  :/SET FOR ERROR TYPEOUT IF NEEDED.
(1)
(1)                                     :/READ THE COUNTER
(2)
(2)          :*          MOV     @BCR,$BDDAT  :/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1)
(1) 022044 023737 001126 001124      CMP     $BDDAT,$GDDAT :/DID THE COUNTER ADVANCE ONCE?
(1) 022052 001402                      BEQ     2$          :/IF YES - NEXT CHECK
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 022054 104015          ERROR 15          :/ERROR - CLOCK B - 100KHZ - PULSE
(1)                                     :/NOT GENERATED WHEN 10 1MHZ PULSE
(1)                                     :/WERE GENERATED.
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 022056 000430          BR      4$
(1)
(1) 022060 012700 177767      2$: MOV     #-9.,R0 ;/GET THE NUMBER OF '1 MHZ' H PULSES
(1)                                     :/NEED TO GIVE 9 1MHZ PULSES
(1) 022064                      3$:
(2)
(2)          :*          MOV     @ASR,$TMDAT  :/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(1) 022074 052737 004000 001356      BIS     #BIT11,$TMDAT
(2)
(2)          :*          MOV     $TMDAT,@ASR  :/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1) 022112 005200          INC      R0          :/IN ORDER TO CHECK TO SEE THAT
(1) 022114 001363          BNE      3$          :/WE DON'T GENERATE ANOTHER 100KHZ PULSE
(1)
(2)
(2)          :*          MOV     @BCR,$BDDAT  :/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1) 022126 023737 001126 001124      CMP     $BDDAT,$GDDAT :/WAS ANOTHER 100KHZ PULSE GENERATED?
(1) 022134 001401                      BEQ     4$          :/NO - GO TO NEXT CHECK.
(1)
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 022136 104015          ERROR 15          :/ERROR CLOCK B WE SEEM TO HAVE
(1)                                     :/GENERATED A SECOND 100KHZ PULSE
(1)                                     :/ON ONLY 9 1MHZ PULSES.
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 022140          4$:
5147
(5)                                     : *****
(4)                                     : *TEST 144 *TEST CLOCK B'S 10KHZ DIVIDER
(5)                                     : *
(5)                                     : +IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ

```

```

(5) ;+BY 10 TO GIVE US A 100HZ CLK L PULSE.
(5) ;+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
(5) ;*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
(5) ;*PULSES.
(5) ;*THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
(5) ;*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
(5) ;*
(6) ;*
(6) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
(6) ;*
(4) ;*****
(3) 022140 000004 TST144: SCOPE
(2) 022142 012737 000020 001166 MOV #20,$TIMES ;;DO 20 ITERATIONS
(1) ;/CLEAR CLOCK B.
(1) ;/CLEAR CLOCK A.
(1) ;/CLEAR B'S BUFFER + COUNT REGS.
(1) ;/DISABLE THE 1MHZ OSC.
(1) ;/RATE: 10KHZ
(1) ;/ENABLE CLOCK B.
(1) 022150 005037 001356 CLR $TMDAT
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(2) ;* MOV $TMDAT,@BBR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BBR
(1) 022204 012737 004040 001356 MOV #BIT11,BITS,$TMDAT
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(2) ;* MOV @BSR,$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.
(1) 022232 052737 000006 001356 BIS #6,$TMDAT
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(1) 022250 005237 001356 INC $TMDAT
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(1) 022264 012700 177634 MOV #-100.,R0 ;/SET TO GENERATE 100. 1MHZ PULSES
(1) 022270 1$: ;/GENERATE 1 1MHZ PULSE
(1) ;/HAS THE COUNTER ADVANCED?
(2) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(1) 022300 052737 004000 001356 BIS #BIT11,$TMDAT
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(2) ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1) 022326 005737 001126 TST $BDDAT
(1) 022332 001002 BNE 10$ ;/EXIT LOOP IF SO.
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.
(1) ;/ OSC., THE DIVIDER COULD HAVE
(1) ;/ HAD ANY COUNT IN IT.
(1) ;/AFTER THIS LOOP, WE SHOULD BE SUNK.

```





```
(5) ;*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
(5) ;*PULSES.
(5) ;*THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
(5) ;*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
(5) ;*
(6) ;*
(6) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
(6) ;*
(4) ;*
(3) 022452 000004 TST145: SCOPE
(2) 022454 012737 000020 001166 MOV #20,$TIMES ;:DO 20 ITERATIONS
(1) ;/CLEAR CLOCK B.
(1) ;/CLEAR CLOCK A.
(1) ;/CLEAR B'S BUFFER + COUNT REGS.
(1) ;/DISABLE THE 1MHZ OSC.
(1) ;/RATE: 1KHZ
(1) ;/ENABLE CLOCK B.
(1) 022462 005037 001356 CLR $TMDAT
(2) ;*
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BBR
(1) 022510 012737 004040 001356 MOV #BIT11!BIT5,$TMDAT
(2) ;*
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(1) 022544 052737 000010 001356 MOV @BSR,$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.
(2) ;*
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(1) 022562 005237 001356 INC $TMDAT
(2) ;*
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(1) 022576 012700 176030 MOV #-1000.,R0 ;/SET TO GENERATE 1000. 1MHZ PULSES
(1) 022602 1$: ;/GENERATE 1 1MHZ PULSE
(1) ;/HAS THE COUNTER ADVANCED?
(2) ;*
(1) 022612 052737 004000 001356 MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(2) ;*
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(2) ;*
(1) 022640 005737 001126 MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1) 022644 001002 TST $BDDAT
(1) BNE 10$ ;/EXIT LOOP IF SO.
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.
(1) ;/ OSC., THE DIVIDER COULD HAVE
(1) ;/ HAD ANY COUNT IN IT.
(1) ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
(1) 022646 005200 INC R0 ;/DONE 1000. 1MHZ PULSES?
```

```
(1) 022650 001354          BNE      1$          ;/IF NOT - DO ANOTHER.
(1)
(1) 022652 012737 000001 001124 10$:  MOV      #1,$GDDAT  ;/SET FOR ERROR TYPEOUT IF NEEDED.
(1)
(1)                                ;/READ THE COUNTER
(2)
(2)          :*      MOV      @BCR,$BDDAT  ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1)
(1) 022670 023737 001126 001124      CMP      $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?
(1) 022676 001402          BEQ      2$          ;/IF YES - NEXT CHECK
(2)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(1) 022700 104015          ERROR    15          ;/ERROR - CLOCK B - 1KHZ - PULSE
(1)                                ;/NOT GENERATED WHEN 10 10KHZ PULSE
(1)                                ;/WERE GENERATED.
(2)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(1) 022702 000430          BR       4$
(1)
(1) 022704 012700 176031      2$:  MOV      #-999.,R0    ;/GET THE NUMBER OF '1 MHZ' H PULSES
(1)                                ;/NEED TO GIVE 9 10KHZ PULSES
(1) 022710          3$:
(2)
(2)          :*      MOV      @ASR,$TMDAT  ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(1) 022720 052737 004000 001356      BIS      #BIT11,$TMDAT
(2)
(2)          :*      MOV      $TMDAT,@ASR  ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1) 022736 005200          INC      R0          ;/IN ORDER TO CHECK TO SEE THAT
(1) 022740 001363          BNE      3$          ;/WE DON'T GENERATE ANOTHER 1KHZ PULSE
(1)
(2)
```

```
(1) 022752 023737 001126 001124      MOV      @BCR,$BDDAT  ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1) 022760 001401          CMP      $BDDAT,$GDDAT ;/WAS ANOTHER 1KHZ PULSE GENERATED?
(1)                                BEQ      4$          ;/NO - GO TO NEXT CHECK.
(2)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(1) 022762 104015          ERROR    15          ;/ERROR CLOCK B WE SEEM TO HAVE
(1)                                ;/GENERATED A SECOND 1KHZ PULSE
(1)                                ;/ON ONLY 9 10KHZ PULSES.
(2)
```

:::\*\*\*\*\*>> ERROR <<\*\*\*\*\*

```
(1) 022764          4$:
5149
(5)          :*****
(4)          :*TEST 146      *TEST CLOCK B'S 100HZ DIVIDER
(5)          :*
(5)          ;+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
(5)          ;+BY 10 TO GIVE US A 100HZ CLK L PULSE.
(5)          ;+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
(5)          ;*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
(5)          ;*PULSES.
```

```
(5) ;*THEN WE'LI GENERATE 9 MORE 1KHZ PULSES AND MAKE  
(5) ;*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.  
(5) ;*  
(6) ;*  
(6) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
(6) ;*  
(4) ;*****  
(3) 022764 000004 TST146: SCOPE  
(2) 022766 012737 000020 001166 MOV #20,$TIMES ;:DO 20 ITERATIONS  
(1) ;/CLEAR CLOCK B.  
(1) ;/CLEAR CLOCK A.  
(1) ;/CLEAR B'S BUFFER + COUNT REGS.  
(1) ;/DISABLE THE 1MHZ OSC.  
(1) ;/RATE: 100HZ  
(1) ;/ENABLE CLOCK B.  
(1) 022774 005037 001356 CLR $TMDAT  
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
(1) 023030 012737 004040 001356 MOV #BIT11.BIT5,$TMDAT  
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
(2) ;* MOV @BSR,$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.  
(1) 023056 052737 000012 001356 BIS #12,$TMDAT  
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
(1) 023074 005237 001356 INC $TMDAT  
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
(1) 023110 012700 154360 MOV #-10000.,R0 ;/SET TO GENERATE 10000. 1MHZ PULSES  
(1) 023114 1$: ;/GENERATE 1 1MHZ PULSE  
(1) ;/HAS THE COUNTER ADVANCED?  
(2) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
(1) 023124 052737 004000 001356 BIS #BIT11,$TMDAT  
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
(2) ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
(1) 023152 005737 001126 TST $BDDAT  
(1) 023156 001002 BNE 10$ ;/EXIT LOOP IF SO.  
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.  
(1) ;/ OSC., THE DIVIDER COULD HAVE  
(1) ;/ HAD ANY COUNT IN IT.  
(1) ;/AFTER THIS LOOP, WE SHOULD BE SUNK.  
(1) 023160 005200 INC R0 ;/DONE 10000. 1MHZ PULSES?  
(1) 023162 001354 BNE 1$ ;/IF NOT - DO ANOTHER.  
(1)
```

```

(1) 023164 012737 000001 001124 10$: MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.
(1)                                         ;/READ THE COUNTER
(1)
(2)                                         ;*
(2) * MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1)
(1) 023202 023737 001126 001124 CMP $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?
(1) 023210 001402 BEQ 2$ ;/IF YES - NEXT CHECK
(2)
    :.::$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 023212 104015 ERROR 15 ;/ERROR - CLOCK B - 100HZ - PULSE
(1)                                         ;/NOT GENERATED WHEN 10 1KHZ PULSE
(1)                                         ;/WERE GENERATED.
(2)
    :.::$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

(1) 023214 000430 BR 4$
(1)
(1) 023216 012700 154361 2$: MOV #-9999.,R0 ;/GET THE NUMBER OF '1 MHZ' H PULSES
(1)                                         ;/NEED TO GIVE 9 1KHZ PULSES
(1) 023222 3$:
(2)
(2) * MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(1) 023232 052737 004000 001356 BIS #BIT11,$TMDAT
(2)
(2) * MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1) 023250 005200 INC R0 ;/IN ORDER TO CHECK TO SEE THAT
(1) 023252 001363 BNE 3$ ;/WE DON'T GENERATE ANOTHER 100HZ PULSE
(1)
(2)
(2) * MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1) 023264 023737 001126 001124 CMP $BDDAT,$GDDAT ;/WAS ANOTHER 100HZ PULSE GENERATED?
(1) 023272 001401 BEQ 4$ ;/NO - GO TO NEXT CHECK.
(1)
(2)
    :.::$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 023274 104015 ERROR 15 ;/ERROR CLOCK B WE SEEM TO HAVE
(1)                                         ;/GENERATED A SECOND 100HZ PULSE
(1)                                         ;/ON ONLY 9 1KHZ PULSES.
(2)
    :.::$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

(1) 023276 4$:
5150
5176
5177 .SBTTL
5178
5179 .SBTTL END OF PASS ROUTINE
(1)
(2)
(1) :.*****
(1) * INCREMENT THE PASS NUMBER ($PASS)
(1) * TYPE 'END PASS'
(1) * IF THERES A MONITOR GO TO IT
(1) * IF THERE ISN'T JUMP TO LOOP
    
```

(1)  
 (1)  
 (1)  
 (1) 023276  
 (2) 023276 000240  
 (1) 023300 005037 001102  
 (1) 023304 005037 001166  
 (1) 023310 005237 001210  
 (1) 023314 042737 100000 0012'0  
 (1) 023322 005327  
 (1) 023324 000001  
 (1) 023326 003017  
 (1) 023330 012737  
 (1) 023332 000001  
 (1) 023334 023324  
 (1) 023336 104401 023375  
 (1) 023342 104401 023372  
 (1) 023346 013700 000042  
 (1) 023352 001405  
 (1) 023354 000005  
 (1) 023356 004710  
 (1) 023360 000240  
 (1) 023362 000240  
 (1) 023364 000240  
 (1) 023366  
 (1) 023366 000137  
 (1) 023370 002310  
 (1) 023372 377 377 000  
 (1) 023375 015 042412 042116  
 (1) 023402 050040 051501 000123  
 5180  
 5181  
 5182  
 5183  
 5199  
 5217  
 5218  
 5219  
 5220  
 5221  
 5222  
 5223  
 5224  
 5225  
 5226  
 5227  
 5228  
 5229  
 5230  
 5231  
 5232  
 5233  
 5234  
 (1)  
 (1)  
 5235

```

;*IF IT IS DESIRED TO HAVE A BELL INDICATE THE 'END OF PASS' LOCATION
;*SENDMG CAN BE CHANGED TO 7.

$EOP:
NOP
CLR $STNM ;;ZERO THE TEST NUMBER
CLR $TIMES ;;ZERO THE NUMBER OF ITERATIONS
INC $PASS ;;INCREMENT THE PASS NUMBER
BIC #100000,$PASS ;;DON'T ALLOW A NEG. NUMBER
DEC (PC)+ ;;LOOP?

$EOPCT: .WORD 1
BGT $DOAGN ;;YES
MOV (PC)+,@(PC)+ ;;RESTORE COUNTER

$ENDCT: .WORD 1
$EOPCT
TYPE ,SENDMG ;;TYPE 'END PASS'
TYPE ,SENULL ;;TYPE A NULL CHARACTER
$GET42: MOV @#42,R0 ;;GET MONITOR ADDRESS
BEQ $DOAGN ;;BRANCH IF NO MONITOR
RESET ;;CLEAR THE WORLD
$FNDAD: JSR PC,(R0) ;;GO TO MONITOR
NOP ;;SAVE ROOM
NOP ;;FOR
NOP ;;ACT11

$DOAGN: JMP @(PC)+ ;;RETURN
$RTNAD: .WORD LOOP
$ENULL: .BYTE -1,-1,0 ;;NULL CHARACTER STRING
$SENDMG: .ASCIZ <15><12>/END PASS/

.SBTTL *
.SBTTL * SPECIAL I/O SIGNAL TESTS
.SBTTL *

.SBTTL * 'STP2 OUT' TO 'SCHMITT TRIG 1 IN' TESTS
;*
;* THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND
;* PROVIDING SCOPE LOOP CAPABILITIES FOR 'STP2 OUT' L
;* AND 'SCHMITT TRIG 1' IN.
;*
;* WHEN YOU LOAD AND START AT LOCATION 210, PROGRAM
;* CONTROL IS TRANSFERRED HERE. 'STP2 OUT' L PULSES ARE
;* GENERATED BY 'LD STAT A HI' H + 'BD10' H (MAIN. STP2).
;* PIN V ('STP2 OUT') IS WIRED TO PIN LL (SCHMITT TRIG1) FOR
;* THIS TEST. 'STP2 OUT' PULSES ARE RECEIVED AS 'SCHMITT TRIG 1'
;* PULSES WHICH SET CLOCK A'S STATUS REGISTER BIT 15.
;* IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
;* AND ERROR SWITCH REGISTER OPTIONS ARE USED.
;* AN '*' IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE
;* TEST. SW13=1 WILL INHIBIT THIS FEATURE.
;*
;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT B'
;*

```

```

5236          ;* YOU MUST WIRE PINS V AND LL OF J1 TOGETHER AND INSTALL JUMPER W3
5237          ;*
5238          ;* LOGIC TEST (L + S 200) SHOULD BE RUN FIRST.
5239          ;*
5240
5241 023410 005037 001666      LS210: CLR      .DVLS
5242
5243          ;/ CLEAR ITERATION COUNT
5244          ;/ SET PASS COUNT.
5245          ;/ NOTE: PASS COUNT USED ONLY
5246          ;/      TO DETECT 60 PASSES SO
5247          ;/      IT CAN GENERATE A CRLF.
5248          ;/      AFTER CRLF IT WILL BE ZEROED.
5249          ;/ CLEAR CLOCK A.
5250          ;/ CLEAR CLOCK B.
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(1) 023546 005237 001104      INC      $ICNT      ;/UPDATE COUNT.
(1) 023552 001325              BNE      2$        ;/IF NOT DONE 65,324 TIMES,
(1)                               ;/DO IT AGAIN.
(1)
(2) 023554 104401 023562      TYPE     .65$      ;;TYPE ASCIZ STRING
(2) 023560 000401              BR       64$      ;;GET OVER THE ASCIZ
(2)                               ;;65$: .ASCIZ ##
(2) 023564                    64$:
(1)
(1) 023564 005237 001210      INC      $PASS     ;/DONE 60 PASSES?
(1) 023570 100716              BMI      2$        ;/NO - NO NEED FOR CR,LF.
(2) 023572 104401 023600      TYPE     .67$      ;;TYPE ASCIZ STRING
(2) 023576 000402              BR       66$      ;;GET OVER THE ASCIZ
(2)                               ;;67$: .ASCIZ <15><12>##
(2) 023604                    66$:
(1) 023604 000703              BR       1$
```

```
5267
5268      .SBTTL      ;*      'STP1 OUT' TO 'SCHMITT TRIG 2' H TESTS
5269      ;*
5270      ;* THIS IS A SPECIAL TEST SECTION DEVOTED FOR TESTING AND
5271      ;* PROVIDING SCOPE LOOP CAPABILITIES FOR 'STP1 OUT' AND
5272      ;* 'SCHMITT TRIG2' IN.
5273      ;*
5274      ;* WHEN YOU LOAD AND START AT LOCATION 214, PROGRAM
5275      ;* CONTROL IS TRANSFERRED HERE. 'STP1 OUT' L PULSES ARE
5276      ;* GENERATED BY 'LD STAT A HI' + 'BD12' H (MAIN ST1).
5277      ;* PIN DD ('STP1 OUT') IS WIRED TO PIN BB ('SCHMITT
5278      ;* TRIG 2') FOR THIS TEST. 'STP1 OUT' PULSES ARE RECEIVED AS
5279      ;* 'SCHMITT TRIG 2' PULSES WHICH WILL CLEAR CLOCK A'S
5280      ;* COUNT REGISTER IF MODE 3 IS SELECTED.
5281      ;* IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
5282      ;* AND ERROR SWITCH REGISTER OPTIONS ARE USED.
5283      ;* AN '*' IS TYPED AFTER EACH 65,324 LOOPS THROUGH
5284      ;* THE TEST. SW13=1 WILL INHIBIT THIS FEATURE.
5285      ;*
5286      ;*
5287      ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT B'
5288      ;*
5289      ;* YOU MUST WIRE PINS DD AND BB OF J1 TOGETHER AND INSTALL JUMPER W4.
5290      ;*
5291      ;* LOGIC TESTS (L + S AT 200) SHOULD BE RUN FIRST.
5292      ;*
```

```
5292 023606 005037 001666      LS214: CLR      .DVLS
5293 (1) 023612 005037 001104      1$: CLR      $ICNT      ;/CLEAR ITERATION COUNT
(1) 023616 012737 177704 001210 MCV      #-60.,$PASS ;/SET PASS COUNT.
(1)                               ;/NOTE: PASS COUNT USED ONLY
(1)                               ;/      TO DETECT 60 PASSES SO
(1)                               ;/      IT CAN GENERATE A CRLF.
(1)                               ;/      AFTER CRLF IT WILL BE ZEROED.
(1) 023624                    2$: CLR      $TMDAT ;/CLEAR CLOCK A.
(1) 023624 005037 001356      CLR      $TMDAT ;/CLEAR CLOCK B.
(2)
```





(2)  
(2) 024020  
(1) 024020 000674  
(1)

::67\$: .ASCIZ <15><12>##  
66\$: BR 1\$

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.SBTTL \* 'SCHMITT TRIG 3' IN, 'ST3 OUT' TESTS  
:\*  
:\*THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND  
:\*PROVIDING SCOPE LOOP CAPABILITIES FOR 'SCHMITT TRIG 3'  
:\*AND 'ST3 OUT'.  
:\*  
:\*WHEN YOU LOAD AND START AT LOCATION 220, PROGRAM  
:\*CONTROL IS TRANSFERRED HERE. 'STP1' PULSES ARE GENERATED  
:\*BY 'LD STAT A H,' + 'BD12' H (MAIN STP1). PIN DD ('STP1 OUT')  
:\*IS WIRED TO PIN T ('SCHMITT TRIG 3'), 'SCHMITT TRIG 3' PULSES  
:\*GIVE US 'ST3 OUT' PULSES. PIN L ('ST3 OUT') IS WIRED  
:\*TO PIN BB ('SCHMITT TRIG2'), AND 'SCHMITT TRIG 2' WILL SET  
:\*CLOCK A'S STATUS REGISTER BIT 7.  
:\*IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.  
:\*AND ERROR SWITCH REGISTER OPTIONS ARE USED.  
:\*AN '\*' IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE  
:\*TEST. SW13=1 WILL INHIBIT THIS FEATURE.  
:\*

(1)  
(1)  
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:\*  
:\* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT B'  
:\*  
:\*YOU MUST WIRE PINS DD TO T OF J1 TOGETHER, AS WELL AS  
:\*PINS L TO BB OF J1 TOGETHER AND INSTALL JUMPERS W4 AND W5.  
:\*  
:\*TESTS LS210 AND LS214 SHOULD BE RUN FIRST.  
:\*

5347 024022 005037 001666  
5348 (1) 024026 005037 001104  
(1) 024032 012737 177704 00'210  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)

LS220: CLR .DVLS  
1\$: CLR \$ICNT ;/CLEAR ITERATION COUNT  
MOV #-60.,\$PASS ;/SET PASS COUNT.  
;/NOTE: PASS COUNT USED ONLY  
;/ TO DETECT 60 PASSES SO  
;/ IT CAN GENERATE A CRLF.  
;/ AFTER CRLF IT WILL BE ZEROED.  
;/CLEAR CLOCK A.  
;/CLEAR CLOCK B.

(1) 024040  
(1) 024040 005037 001356  
(2)  
(2)  
(2)  
(2)  
(1)

2\$: CLR \$TMDAT  
:\* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR  
:\* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR  
;/GENERATE A 'STP2 OUT' PULSE.

5349  
5350 024064 005037 001356  
5351  
(1)  
5352 024100 052737 011000 001356  
5353  
(1)  
5354

CLR \$TMDAT  
:\* MOV @ASR,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.  
BIS #BIT12!BIT9,\$TMDAT  
:\* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR  
;/AT THIS POINT YOU SHOULD SEE AN





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5420 024342 104000 ERROR ;ERROR 'A EVENT OUT' PULSE
5421 ;NOT DETECTED. HAVE YOU
5422 ;WIRED IT RIGHT?
5423

```

:::#####>> ERROR <<#####

```

5424 024344 ;:
5425
(1) 024344 032777 020000 154566 BIT #BIT13,@SWR ;/INHIBIT '*' TYPEOUT?
(1) 024352 001324 BNE 2$ ;/YES - IGNORE ANY UPDATES.
(1)
(1) 024354 005237 001104 INC $ICNT ;/UPDATE COUNT.
(1) 024360 001321 BNE 2$ ;/IF NOT DONE 65,324 TIMES,
(1) ;/DO IT AGAIN.
(1)
(2) 024362 104401 024370 TYPE ,65$ ;:TYPE ASCIZ STRING
(2) 024366 000401 BR 64$ ;:GET OVER THE ASCIZ
(2) ;:65$: .ASCIZ ##
(2) 024372 64$:
(1)
(1) 024372 005237 001210 INC $PASS ;/DONE 60 PASSES?
(1) 024376 100712 BMI 2$ ;/NO - NO NEED FOR CR,LF.
(2) 024400 104401 024406 TYPE ,67$ ;:TYPE ASCIZ STRING
(2) 024404 000402 BR 66$ ;:GET OVER THE ASCIZ
(2) ;:67$: .ASCIZ <15><12>##
(2) 024412 66$:
(1) 024412 000677 BR 1$
(1)

```

```

.SBTTL * 'B EVENT OUT' TEST
;*
;*THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND
;*PROVIDING SCOPE LOOP CAPABILITIES FOR 'B EVENT OUT'.
;*
;*WHEN YOU LOAD AND START AT LOCATION 230, PROGRAM
;*CONTROL IS TRANSFERRED HERE. 'B EVENT OUT' PULSES ARE
;*GENERATED BY CLOCK B OVERFLOWS. PIN TT
;*('B EVENT OUT') IS WIRED TO PIN BB ('SCHMITT TRIG 2')
;*SCHMITT TRIG 2 PULSES WILL SET CLOCK A'S CSR BIT 7.
;*IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIQ.
;*AND ERROR SWITCH REGISTER OPTIONS ARE USED.
;*AN '*' IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE TEST.
;*SW13-1 WILL INHIBIT THIS FEATURE.
;*

```

```

;*
;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF B'
;*
;*YOU MUST WIRE PINS TT AND BB OF J1 TOGETHER AND INSTALL JUMPER W4.
;*
;*TEST LS210 SHOULD BE RUN FIRST.
;*

```

```

5448 024414 005037 001666 LS230: CLR .DVLS
5449
(1) 024420 005037 001104 1$: CLR $ICNT ;/CLEAR ITERATION COUNT
(1) 024424 012737 177704 001210 MOV #-60.,$PASS ;/SET PASS COUNT.

```

```
(1) ;/NOTE: PASS COUNT USED ONLY
(1) ;/ TO DETECT 60 PASSES SO
(1) ;/ IT CAN GENERATE A CRLF.
(1) ;/ AFTER CRLF IT WILL BE ZEROED.
(1) ;/CLEAR CLOCK A.
(1) 024432 2$: CLR $TMDAT ;/CLEAR CLOCK B.
(1) 024432 005037 001356
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(1) ;PRELOAD CLOCK E'S BUFFER + COUNT REGS.
5450 MOV #1,$TMDAT
5451 024456 012737 177777 001356
5452 ;* MOV $TMDAT,@BBR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BBR
(1) MOV #1000,$TMDAT
5453 024474 012737 001000 001356
5454 ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1)
5455 ;RATE: 1MHZ, ENABLE COUNTER
5456 ;HAS AN OVERFLOW OCCURRED?
5457
5458 MOV #3,$TMDAT
5459 024512 012737 000003 001356
5460 ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(1) 3$:
5461 024530
(1) ;* MOV @BSR,$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.
(1) BIT #BIT07,$TMDAT
5462 024540 032737 000200 001356 ;NO -THEN WAIT FOR IT.
5463 024546 001770 BEQ 3$ ;OVERFLOW SHOULD GO OUT AS
5464 ;'B EVENT OUT'. YOU SHOULD SEE
5465 ;AN OUTPUT AT PIN 11.
5466 ;THIS IN TURN IS BROUGHT
5467 ;IN AS 'SCHMITT TRIG 2' IN TO
5468 ;SET CLOCK A'S CSR BIT 7.
5469
5470
5471 ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(1) TSTB $BDDAT ;DID BIT 7 SET
5472 024560 105737 001126 BMI 4$ ;BR IF YES TO 4$
5473 024564 100401
5474
::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

5475 024566 104000 ERRGR ;ERROR 'B EVENT OUT' PULSE
5476 ;NOT DETECTED. HAVE YOU
5477 ;WIRED IT RIGHT?
5478
::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

5479 024570 4$:
5480
(1) 024570 032777 020000 154342 BIT #BIT13,@SWR ;/INHIBIT '*' TYPEOUT?
(1) 024576 001315 BNE 2$ ;/YES - IGNORE ANY JDATES.
(1)
```

```

(1) 024600 005237 001104      INC      $ICNT      ;/UPDATE COUNT.
(1) 024604 001312      BNE      2$        ;/IF NOT DONE 65,324 TIMES.
(1)                                ;/DO IT AGAIN.
(1)
(2) 024606 104401 024614      TYPE     ,65$      ;;TYPE ASCIZ STRING
(2) 024612 000401      BR       64$      ;;GET OVER THE ASCIZ
(2)                                ;;65$: .ASCIZ ##
(2) 024616      64$:
(1)
(1) 024616 005237 001210      INC      $PASS     ;/DONE 60 PASSES?
(1) 024622 100703      BMI      2$        ;/NO - NO NEED FOR CR,LF.
(2) 024624 104401 024632      TYPE     ,67$      ;;TYPE ASCIZ STRING
(2) 024630 000402      BR       66$      ;;GET OVER THE ASCIZ
(2)                                ;;67$: .ASCIZ <15><12>##
(2) 024636      66$:
(1) 024636 000670      BR       1$
(1)
5481
5482      ;*ROUTINE TO HANDLE TRAPS TO LOC 4, 10 AND .
5483      ;*INTERRUPTS TO WRONG VECTORS.
5484      ;*.+2, IOTT(TRAPS) WERE PUT IN LOCATIONS 4-1000
5485
5486
5487 024640      IOTRD:
5488 024640 011637 025010      MOV      (R6),2$   ;GET WHERE WE TRAPPED TO.
5489 024644 162737 000004 025010  SUB      #4,2$     ;=WHERE R6 RETURN 10-4
5490 024652 104401 024660      TYPE     ,65$      ;;TYPE ASCIZ STRING
(1) 024656 000412      BR       64$      ;;GET OVER THE ASCIZ
(1)                                ;;65$: .ASCIZ <15><12>#ILLEGAL TRAP TO: #
(1) 024704      64$:
5491
5492 024704 013746 025010      MOV      2$,-(SP)  ;;SAVE 2$ FOR TYPEOUT
(1) 024710 104402      TYPOC    ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
5493
5494 024712 104401 024720      TYPE     ,67$      ;;TYPE ASCIZ STRING
(1) 024716 000407      BR       66$      ;;GET OVER THE ASCIZ
(1)                                ;;67$: .ASCIZ # FROM LOC.: #
(1) 024736      66$:
5495
5496 024736 062706 000004      ADD      #4,R6     ;POINT TO WHERE WE TRAPPED FROM.
5497
5498 024742 011637 025012      MOV      (R6),3$   ;PICK UP LOC
5499 024746 162737 000002 025012  SUB      #2,3$     ;FROM REAL ADDR.
5500 024754 013746 025012      MOV      3$,-(SP)  ;;SAVE 3$ FOR TYPEOUT
(1) 024760 104402      TYPOC    ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
5501
5502 024762 023727 025010 000004      CMP      2$,#4     ;DID WE TRAP TO LOC 4?
5503 024770 001405      BEQ      1$        ;IF SO - DON'T RETURN!
5504 024772 023727 025010 000010      CMP      2$,#10    ;DID WE TRAP TO LOC. 10?
5505 025000 001401      BEQ      1$        ;ID SO - DON'T RETURN.
5506 025002 000002      RTI             ;TRY RETURNING.
5507
5508
      ;;: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
5509 025004 000000      1$: HALT      ;WE STOPPED HERE BECAUSE WE TRAPPED

```

C 13

5510 025006 000776 BR 1\$ ;TO LOC 4 OR LOC 10. THIS IS A  
5511 ;FATAL CONDITION THAT WE CAN NOT  
5512 ;RECOVER FROM.  
5513  
5514

:::\$>> ERROR <<\$

5515 025010 000000 2\$: .WORD 0 ;USED BY IOTRP TO STORE WHERE WE TRAPPED TO.  
5516 025012 000C00 3\$: .WORD 0 ;USED BY IOTRP TO STORE WHERE WE TRAPPED FROM.  
5517 .SBTTL  
5518 .SBTTL \*SYSMAC ROUTINES  
5519 .SBTTL  
5520  
5521

.SBTTL BINARY TO OCTAL (ASCII) AND TYPE

```

(1) ;*****
(1) ;THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 6-DIGIT
(1) ;OCTAL (ASCII) NUMBER AND TYPE IT.
(1) ;$TYPOS---ENTER HERE TO SETUP SUPPRESS ZEROS AND NUMBER OF DIGITS TO TYPE
(1) ;CALL:
(1) ;    MOV    NUM,-(SP)      ;:NUMBER TO BE TYPED
(1) ;    TYPOS   ;:CALL FOR TYPEOUT
(1) ;    .BYTE  N              ;:N=1 TO 6 FOR NUMBER OF DIGITS TO TYPE
(1) ;    .BYTE  M              ;:M=1 OR 0
(1) ;                                     ;:1=TYPE LEADING ZEROS
(1) ;                                     ;:0=SUPPRESS LEADING ZEROS
(1) ;
(1) ;$STYPOIN---ENTER HERE TO TYPE OUT WITH THE SAME PARAMETERS AS THE LAST
(1) ;$TYPOS OR $TYPOC
(1) ;CALL:
(1) ;    MOV    NUM,-(SP)      ;:NUMBER TO BE TYPED
(1) ;    TYPOIN ;:CALL FOR TYPEOUT
(1) ;
(1) ;$TYPOC---ENTER HERE FOR TYPEOUT OF A 16 BIT NUMBER
(1) ;CALL:
(1) ;    MOV    NUM,-(SP)      ;:NUMBER TO BE TYPED
(1) ;    TYPOC  ;:CALL FOR TYPEOUT

```

```

(1) 025014 017646 000000 025237 $TYPOS: MOV    @(SP),-(SP)    ;:PICKUP THE MODE
(1) 025020 116637 000001 25237   MOVB   1(SP),SOFILL ;:LOAD ZERO FILL SWITCH
(1) 025026 112637 025241          MOVB   (SP)+,SOMODE+1 ;:NUMBER OF DIGITS TO TYPE
(1) 025032 062716 000002          ADD    #2,(SP)       ;:ADJUST RETURN ADDRESS
(1) 025036 000406          BR      $TYPON
(1) 025040 112737 000001 25237 $TYPOC: MOVB   #1,SOFILL ;:SET THE ZERO FILL SWITCH
(1) 025046 112737 000006 25241   MOVB   #6,SOMODE+1 ;:SET FOR SIX(6) DIGITS
(1) 025054 112737 000005 25236 $TYPON: MOVB   #5,SOCNT  ;:SET THE ITERATION COUNT
(1) 025062 010346          MOV    R3,-(SP)     ;:SAVE R3
(1) 025064 010446          MOV    R4,-(SP)     ;:SAVE R4
(1) 025066 010546          MOV    R5,-(SP)     ;:SAVE R5
(1) 025070 113704 025241          MOVB   SOMODE+1,R4 ;:GET THE NUMBER OF DIGITS TO TYPE
(1) 025074 005404          NEG    R4
(1) 025076 062704 000006          ADD    #6,R4       ;:SUBTRACT IT FOR MAX. ALLOWED
(1) 025102 110437 025240          MOVB   R4,SOMODE   ;:SAVE IT FOR USE
(1) 025106 113704 025237          MOVB   $OFILL,R4   ;:GET THE ZERO FILL SWITCH
(1) 025112 016605 000012          MOV    12(SP),R5  ;:PICKUP THE INPUT NUMBER
(1) 025116 005003          CLR    R3          ;:CLEAR THE OUTPUT WORD

```

```
(1) 025120 006105 1$: ROL R5 ;;ROTATE MSB INTO 'C'  
(1) 025122 000404 BR 3$ ;;GO DO MSB  
(1) 025124 006105 2$: ROL R5 ;;FORM THIS DIGIT  
(1) 025126 006105 ROL R5  
(1) 025130 006105 ROL R5  
(1) 025132 010503 MOV R5,R3  
(1) 025134 006103 3$: ROL R3 ;;GET LSB OF THIS DIGIT  
(1) 025136 105337 025240 DECB $OMODE ;;TYPE THIS DIGIT?  
(1) 025142 100016 BPL 7$ ;;BR IF NO  
(1) 025144 042703 177770 BIC #177770,R3 ;;GET RID OF JUNK  
(1) 025150 001002 BNE 4$ ;;TEST FOR 0  
(1) 025152 005704 TST R4 ;;SUPPRESS THIS 0?  
(1) 025154 001403 BEQ 5$ ;;BR IF YES  
(1) 025156 005204 4$: INC R4 ;;DON'T SUPPRESS ANYMORE 0'S  
(1) 025160 052703 000060 BIS #'0,R3 ;;MAKE THIS DIGIT ASCII  
(1) 025164 052703 000040 5$: BIS #' ,R3 ;;MAKE ASCII IF NOT ALREADY  
(1) 025170 110337 025234 MOV R3,8$ ;;SAVE FOR TYPING  
(1) 025174 104401 025234 TYPE ,8$ ;;GO TYPE THIS DIGIT  
(1) 025200 105337 025236 7$: DECB $OCNT ;;COUNT BY 1  
(1) 025204 003347 BGT 2$ ;;BR IF MORE TO DO  
(1) 025206 002402 BLT 6$ ;;BR IF DONE  
(1) 025210 005204 INC R4 ;;INSURE LAST DIGIT ISN'T A BLANK  
(1) 025212 000744 BR 2$ ;;GO DO THE LAST DIGIT  
(1) 025214 012605 6$: MOV (SP)+,R5 ;;RESTORE R5  
(1) 025216 012604 MOV (SP)+,R4 ;;RESTORE R4  
(1) 025220 012603 MOV (SP)+,R3 ;;RESTORE R3  
(1) 025222 016666 000002 000004 MOV 2(SP),4(SP) ;;SET THE STACK FOR RETURNING  
(1) 025230 012616 MOV (SP)+,(SP)  
(1) 025232 000002 RTI ;;RETURN  
(1) 025234 000 8$: .BYTE 0 ;;STORAGE FOR ASCII DIGIT  
(1) 025235 000 .BYTE 0 ;;TERMINATOR FOR TYPE ROUTINE  
(1) 025236 000 $OCNT: .BYTE 0 ;;OCTAL DIGIT COUNTER  
(1) 025237 000 $OFILL: .BYTE 0 ;;ZERO FILL SWITCH  
(1) 025240 000000 $OMODE: .WORD 0 ;;NUMBER OF DIGITS TO TYPE  
5522 .SBTTL ERROR HANDLER ROUTINE  
(1) ;;*****  
(2) ;;*THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT,  
(1) ;;*SAVE THE ERROR ITEM NUMBER AND THE ADDRESS OF THE ERROR CALL  
(1) ;;*AND GO TO $ERRTYP ON ERROR  
(1) ;;*THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:  
(1) ;;*SW15=1 HALT ON ERROR  
(1) ;;*SW13=1 INHIBIT ERROR TYPEOUTS  
(1) ;;*SW10=1 BELL ON ERROR  
(1) ;;*SW09=1 LOOP ON ERROR  
(1) ;;*CALL  
(1) ;;* ERROR N ;;ERROR-EMT AND N-ERROR ITEM NUMBER  
(1) $ERROR:  
(1) 025242 104407 CKSWR ;;TEST FOR CHANGE IN SOFT-SWR  
(1) 025244 105237 001103 7$: INCB $ERFLG ;;SET THE ERROR FLAG  
(1) 025250 001775 BEQ 7$ ;;DON'T LET THE FLAG GO TO ZERO  
(1) 025252 013777 001102 153662 MOV $STNM,@DISPLAY ;;DISPLAY TEST NUMBER AND ERROR FLAG  
(1) 025260 032777 002000 153652 BIT #BIT10,@SWR ;;BELL ON ERROR?  
(1) 025266 001402 BEQ 1$ ;;NO - SKIP  
(1) 025270 104401 001172 TYPE ,SBELL ;;RING BELL
```



```

(1) 025274 005237 001112      1$:  INC  $ERTTL      ;;COUNT THE NUMBER OF ERRORS
(1) 025300 011637 001116      MOV  (SP), $ERRPC ;;GET ADDRESS OF ERROR INSTRUCTION
(1) 025304 162737 000002 001116  SUB  #2, $ERRPC
(1) 025312 117737 153600 001114  MOV  @ $ERRPC, $ITEMB ;;STRIP AND SAVE THE ERROR ITEM CODE
(1) 025320 032777 020000 153612  BIT  #BIT13, @SWR      ;;SKIP TYPEOUT IF SET
(1) 025326 001004      BNE  20$          ;;SKIP TYPEOUTS
(1) 025330 004737 025430      JSR  PC, $ERRTYP      ;;GO TO USER ERROR ROUTINE
(1) 025334 104401 001177      TYPE , $CRLF
(1) 025340      20$:
(1) 025340 122737 000001 001222  CMPB #APTENV, $ENV    ;;RUNNING IN APT MODE
(1) 025346 001007      BNE  2$          ;;NO, SKIP APT ERROR REPORT
(1) 025350 113737 001114 025362  MOV  $ITEMB, 21$     ;;SET ITEM NUMBER AS ERROR NUMBER
(1) 025356 004737 027446      JSR  PC, $ATY4      ;;REPORT FATAL ERROR TO APT
(1) 025362 000      21$:  .BYTE 0
(1) 025363 000      .BYTE 0
(1) 025364 000777      22$:  BR  22$          ;;APT ERROR LOOP
(1) 025366 005777 153546      2$:   TST  @SWR          ;;HALT ON ERROR
(1) 025372 100002      BPL  3$          ;;SKIP IF CONTINUE
(1) 025374 000000      HALT          ;;HALT ON ERROR!
(1) 025376 104407      CKSWR          ;;TEST FOR CHANGE IN SOFT-SWR
(1) 025400 032777 001000 153532  3$:  BIT  #BIT09, @SWR   ;;LOOP ON ERROR SWITCH SET?
(1) 025406 001402      BEQ  4$          ;;BR IF NO
(1) 025410 013716 001110      MOV  $LPERR, (SP)   ;;FUDGE RETURN FOR LOOPING
(1) 025414 005737 001170      4$:  TST  $ESCAPE      ;;CHECK FOR AN ESCAPE ADDRESS
(1) 025420 001402      BEQ  5$          ;;BR IF NONE
(1) 025422 013716 001170      MOV  $ESCAPE, (SP) ;;FUDGE RETURN ADDRESS FOR ESCAPE
(1) 025426      5$:
(1) 025426 000002      R*1          ;;RETURN
5523  .SBTTL  ERROR MESSAGE TIMEOUT ROUTINE
(1)
(2)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1) 025430      $ERRTYP:
(1) 025430 104401 001177      TYPE , $CRLF      ;;'CARRIAGE RETURN' & 'LINE FEED'
(1) 025434 010046      MOV  RO, -(SP)    ;;SAVE RO
(1) 025436 005000      CLR  RO          ;;PICKUP THE ITEM INDEX
(1) 025440 153700 001114  BISB @ $ITEMB, RO
(1) 025444 001004      BNE  1$          ;;IF ITEM NUMBER IS ZERO, JUST
(1)      MOV  $ERRPC, -(SP) ;;TYPE THE PC OF THE ERROR
(2) 025446 013746 001116      ;;SAVE $ERRPC FOR TYPEOUT
(2)      ERROR ADDRESS
(2) 025452 104402      TYPCC          ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
(1) 025454 000426      BR  6$          ;;GET OUT
(1) 025456 005300      1$:  DEC  RO          ;;ADJUST THE INDEX SO THAT IT WILL
(1) 025460 006300      ASL  RO          ;;
(1) 025462 006300      ASL  RO          ;;
(1) 025464 006300      ASL  RO          ;;
(1) 025466 062700 001360      ADD  # $ERRTB, RO  ;;FORM TABLE POINTER
(1) 025472 012037 025502      MOV  (RO)+, 2$    ;;PICKUP 'ERROR MESSAGE' POINTER
(1) 025476 001404      BEQ  3$          ;;SKIP TYPEOUT IF NO POINTER
(1) 025500 104401      TYPE          ;;TYPE THE 'ERROR MESSAGE'
(1) 025502 000000      2$:  .WORD 0        ;;'ERROR MESSAGE' POINTER GOES HERE
(1) 025504 104401 001177      TYPE , $CRLF      ;;'CARRIAGE RETURN' & 'LINE FEED'

```

```

*****
*THIS ROUTINE USES THE 'ITEM CONTROL BYTF' ($ITEMB) TO DETERMINE WHICH
*ERROR IS TO BE REPORTED. IT THEN OBTAINS, FROM THE 'ERROR TABLE' ($ERRTB),
*AND REPORTS THE APPROPRIATE INFORMATION CONCERNING THE ERROR.

```

```

(1) 025510 012037 025520 3$: MOV (R0)+,4$ ;;PICKUP 'DATA HEADER' POINTER
(1) 025514 001404 BEQ 5$ ;;SKIP TYPEOUT IF 0
(1) 025516 104401 TYPE ;;TYPE THE 'DATA HEADER'
(1) 025520 000000 4$: .WORD 0 ;;'DATA HEADER' POINTER GOES HERE
(1) 025522 104401 001177 TYPE , $CRLF ;;'CARRIAGE RETURN' & 'LINE FEED'
(1) 025526 011000 5$: MOV (R0),R0 ;;PICKUP 'DATA TABLE' POINTER
(1) 025530 001004 BNE 7$ ;;GO TYPE THE DATA
(1) 025532 012600 6$: MOV (SP)+,R0 ;;RESTORE R0
(1) 025534 104401 001177 TYPE , $CRLF ;;'CARRIAGE RETURN' & 'LINE FEED'
(1) 025540 000207 RTS PC ;;RETURN
(1) 025542 7$:
(2) 025542 013046 MOV @ (R0)+,-(SP) ;;SAVE @ (R0)+ FOR TYPEOUT
(2) 025544 104402 TYPOC ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
(1) 025546 005710 TST (R0) ;;IS THERE ANOTHER NUMBER?
(1) 025550 001770 BEQ 6$ ;;BR IF NO
(1) 025552 104401 025560 TYPE , 8$ ;;TYPE TWO(2) SPACES
(1) 025556 000771 BR 7$ ;;LOOP
(1) 025560 020040 000 8$: .ASCIZ / / ;;TWO(2) SPACES
(1) 025564 .EVEN
5524 .SBTTL CONVERT BINARY TO DECIMAL AND TYPE ROUTINE
(1)
(2)
(1) *****
(1) *THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 5-DIGIT
(1) *SIGNED DECIMAL (ASCII) NUMBER AND TYPE IT. DEPENDING ON WHETHER THE
(1) *NUMBER IS POSITIVE OR NEGATIVE A SPACE OR A MINUS SIGN WILL BE TYPED
(1) *BEFORE THE FIRST DIGIT OF THE NUMBER. LEADING ZEROS WILL ALWAYS BE
(1) *REPLACED WITH SPACES.
(1) *CALL:
(1) * MOV NUM,-(SP) ;;PUT THE BINARY NUMBER ON THE STACK
(1) * TYPDS ;;GO TO THE ROUTINE
(1)
(1) $TYPDS:
(3) 025564 010046 MOV R0,-(SP) ;;PUSH R0 ON STACK
(3) 025566 010146 MOV R1,-(SP) ;;PUSH R1 ON STACK
(3) 025570 010246 MOV R2,-(SP) ;;PUSH R2 ON STACK
(3) 025572 010346 MOV R3,-(SP) ;;PUSH R3 ON STACK
(3) 025574 010546 MOV R5,-(SP) ;;PUSH R5 ON STACK
(1) 025576 012746 020200 MOV #20200,-(SP) ;;SET BLANK SWITCH AND SIGN
(1) 025602 016605 00C020 MOV 20(SP),R5 ;;GET THE INPUT NUMBER
(1) 025606 100004 BPL 1$ ;;BR IF INPUT IS POS.
(1) 025610 005405 NEG R5 ;;MAKE THE BINARY NUMBER POS.
(1) 025612 112766 000055 000001 MOVB #'-,1(SP) ;;MAKE THE ASCII NUMBER NEG.
(1) 025620 005000 1$: CLR R0 ;;ZERO THE CONSTANTS INDEX
(1) 025622 012703 026000 MOV #$DBLK,R3 ;;SETUP THE OUTPUT POINTER
(1) 025626 112723 000040 MOVB #'',(R3)+ ;;SET THE FIRST CHARACTER TO A BLANK
(1) 025632 005002 2$: CLR R2 ;;CLEAR THE BCD NUMBER
(1) 025634 016001 025770 MOV $DTBL(R0),R1 ;;GET THE CONSTANT
(1) 025640 160105 3$: SUB R1,R5 ;;FORM THIS BCD DIGIT
(1) 025642 002402 BLT 4$ ;;BR IF DONE
(1) 025644 005202 INC R2 ;;INCREASE THE BCD DIGIT BY 1
(1) 025646 000774 BR 3$
(1) 025650 060105 4$: ADD R1,R5 ;;ADD BACK THE CONSTANT
(1) 025652 005702 TST R2 ;;CHECK IF BCD DIGIT=0
(1) 025654 001002 BNE 5$ ;;FALL THROUGH IF 0
(1) 025656 105716 TSTB (SP) ;;STILL DOING LEADING 0's?
(1) 025660 100407 BMI 7$ ;;BR IF YES

```



```
(1) 026050 022626 5$: CMP (SP)+,(SP)+ ::CLEAR THE STACK AFTER A TIME OUT
(1) 026052 012637 000004 MOV (SP)+,@ERRVEC ::RESTORE THE ERROR VECTOR
(1) 026056 000423 BR 7$ ::LOOP ON THE PRESENT TEST
(1) 026060 6$:;*****END OF CODE FOR THE XOR TESTER*****
(1) 026060 032777 000400 153052 BIT #BIT08,@SWR ::LOOP ON SPEC. TEST?
(1) 026066 001404 BEQ 2$ ::BR IF NO
(1) 026070 127737 153044 001102 CMPB @SWR,$STSTM ::ON THE RIGHT TEST? SWR<7:0>
(1) 026076 001465 BEQ $OVER ::BR IF YES
(1) 026100 105737 001103 2$: TSTB $ERFLG ::HAS AN ERROR OCCURRED?
(1) 026104 001421 BEQ 3$ ::BR IF NO
(1) 026106 123737 001115 001103 CMPB $ERMAX,$ERFLG ::MAX. ERRORS FOR THIS TEST OCCURRED?
(1) 026114 101015 BHI 3$ ::BR IF NO
(1) 026116 032777 001000 153014 BIT #BIT09,@SWR ::LOOP ON ERROR?
(1) 026124 001404 BEQ 4$ ::BR IF NO
(1) 026126 013737 001110 001106 7$: MOV $LPERR,$LPADR ::SET LOOP ADDRESS TO LAST SCOPE
(1) 026134 000446 BR $OVER
(1) 026136 105037 001103 4$: CLRB $ERFLG ::ZERO THE ERROR FLAG
(1) 026142 005037 001166 CLR $TIMES ::CLEAR THE NUMBER OF ITERATIONS TO MAKE
(1) 026146 000415 BR 1$ ::ESCAPE TO THE NEXT TEST
(1) 026150 032777 004000 152762 3$: BIT #BIT11,@SWR ::INHIBIT ITERATIONS?
(1) 026156 001011 BNE 1$ ::BR IF YES
(1) 026160 005737 001210 TST $PASS ::IF FIRST PASS OF PROGRAM
(1) 026164 001406 BEQ 1$ :: INHIBIT ITERATIONS
(1) 026166 005237 001104 INC $ICNT ::INCREMENT ITERATION COUNT
(1) 026172 023737 001166 001104 CMP $TIMES,$ICNT ::CHECK THE NUMBER OF ITERATIONS MADE
(1) 026200 002024 BGE $OVER ::BR IF MORE ITERATION REQUIRED
(1) 026202 012737 000001 001104 1$: MOV #1,$ICNT ::REINITIALIZE THE ITERATION COUNTER
(1) 026210 013737 026266 001166 MOV $MXCNT,$TIMES ::SET NUMBER OF ITERATIONS TO DO
(1) 026216 105237 001102 $SVLAD: INCB $STSTM ::COUNT TEST NUMBERS
(1) 026222 113737 001102 001206 MOV $STSTM,$TESTN ::SET TEST NUMBER IN APT MAILBOX
(1) 026230 011637 001106 MOV (SP),$LPADR ::SAVE SCOPE LOOP ADDRESS
(1) 026234 011637 001110 MOV (SP),$LPERR ::SAVE ERROR LOOP ADDRESS
(1) 026240 005037 001170 CLR $ESCAPE ::CLEAR THE ESCAPE FROM ERROR ADDRESS
(1) 026244 112737 000001 001115 MOV #1,$ERMAX ::ONLY ALLOW ONE(1) ERROR ON NEXT TEST
(1) 026252 013777 001102 152662 $OVER: MOV $STSTM,@DISPLAY ::DISPLAY TEST NUMBER
(1) 026260 013716 001106 MOV $LPADR,(SP) ::FUDGE RETURN ADDRESS
(1) 026264 000002 RTI ::FIXES PS
(1) 026266 000012 $MXCNT: 10. ::MAX. NUMBER OF ITERATIONS
5526 .SBTTL READ AN OCTAL NUMBER FROM THE TTY
(1)
(2)
(1) ::*****
(1) ::*THIS ROUTINE WILL READ AN OCTAL (ASCII) NUMBER FROM THE TTY AND
(1) ::*CHANGE IT TO BINARY.
(1) ::*CALL:
(1) ::* RDOCT ::READ AN OCTAL NUMBER
(1) ::* RETURN HERE ::LOW ORDER BITS ARE ON TOP OF THE STACK
(1) ::* ::HIGH ORDER BITS ARE IN $HIOCT
(1)
(1) $RDOCT: MOV (SP),-(SP) ::PROVIDE SPACE FOR THE
(1) 026270 011646 MOV 4(SP),2(SP) ::INPUT NUMBER
(1) 026272 016666 000004 000002 MOV R0,-(SP) ::PUSH R0 ON STACK
(3) 026300 010046 MOV R1,-(SP) ::PUSH R1 ON STACK
(3) 026302 010146 MOV R2,-(SP) ::PUSH R2 ON STACK
(3) 026304 010246 1$: RDLIN ::READ AN ASCII LINE
(1) 026306 104411 MOV (SP)+,R0 ::GET ADDRESS OF 1ST CHARACTER
(1) 026310 012600 CLR R1 ::CLEAR DATA WORD
(1) 026312 005001
```

```
(1) 026314 005002
(1) 026316 112046
(1) 026320 001412
(1) 026322 006301
(1) 026324 006102
(1) 026326 006301
(1) 026330 006102
(1) 026332 006301
(1) 026334 006102
(1) 026336 042716 177770
(1) 026342 062601
(1) 026344 000764
(1) 026346 005726
(1) 026350 010166 000012
(1) 026354 010237 026370
(3) 026360 012602
(3) 026362 012601
(3) 026364 012600
(1) 026366 000002
(1) 026370 000000
5527
(1)
(2)
(1)
(1)
(2)
(1)
(1)
(1)
(1)
(1)
(1)
(1) 026372 022737 000176 00-1140
(1) 026400 001074
(1) 026402 105777 152536
(1) 026406 100071
(1) 026410 117746 152532
(1) 026414 042716 177600
(1) 026420 022726 000007
(1) 026424 001062
(1) 026426 123727 001134 000001
(1) 026434 001456
(1)
(1) 026436 104401 027117
(1) 026442 104401 027124
(2) 026446 013746 000176
(2) 026452 104402
(1) 026454 104401 027135
(1) 026460 005046
(1) 026462 005046
(1) 026464 105777 152454
(1) 026470 100375
(1)
(1) 026472 117746 152450
(1) 026476 042716 177600
(1)
(1)
(1)
```

```
CLR R2
2$: MOV (R0)+, -(SP) ;; PICKUP THIS CHARACTER
BEQ 3$ ;; IF ZERO GET OUT
ASL R1 ;; *2
ROL R2
ASL R1 ;; *4
ROL R2 ;; *8
ASL R1
ROL R2
BIC #^C7, (SP) ;; STRIP THE ASCII JUNK
ADD (SP)+, R1 ;; ADD IN THIS DIGIT
BR 2$ ;; LOOP
3$: TST (SP)+ ;; CLEAN TERMINATOR FROM STACK
MOV R1, 12(SP) ;; SAVE THE RESULT
MOV R2, $HIOCT
MOV (SP)+, R2 ;; POP STACK INTO R2
MOV (SP)+, R1 ;; POP STACK INTO R1
MOV (SP)+, R0 ;; POP STACK INTO R0
RTI ;; RETURN
$HIOCT: .WORD 0 ;; HIGH ORDER BITS GO HERE
.SBTTL TTY INPUT ROUTINE

*****
.ENABL LSB

*****
*SOFTWARE SWITCH REGISTER CHANGE ROUTINE.
*ROUTINE IS ENTERED FROM THE TRAP HANDLER, AND WILL
*SERVICE THE TEST FOR CHANGE IN SOFTWARE SWITCH REGISTER TRAP CALL
*WHEN OPERATING IN TTY FLAG MODE.
$CKSWR: CMP #SWREG, SWR ;; IS THE SOFT-SWR SELECTED?
BNE 15$ ;; BRANCH IF NO
TSTB @TKS ;; CHAR THERE?
BPL 15$ ;; IF NO, DON'T WAIT AROUND
MOVB @TKB, -(SP) ;; SAVE THE CHAR
BIC #^C177, (SP) ;; STRIP-OFF THE ASCII
CMP #7, (SP)+ ;; IS IT A CONTROL G?
BNE 15$ ;; NO, RETURN TO USER
CMPB $AUTOB, #1 ;; ARE WE RUNNING IN AUTO-MODE?
BEQ 15$ ;; BRANCH IF YES

$GTSWR: TYPE , $CNTLG ;; ECHO THE CONTROL-G (^G)
TYPE , $MSWR ;; TYPE CURRENT CONTENTS
MOV SWREG, -(SP) ;; SAVE SWREG FOR TYPEOUT
TYPOC ;; GO TYPE--OCTAL ASCII(ALL DIGITS)
TYPE , $MNEW ;; PROMPT FOR NEW SWR
19$: CLR -(SP) ;; CLEAR COUNTER
CLR -(SP) ;; THE NEW SWR
7$: TSTB @TKS ;; CHAR THERE?
BPL 7$ ;; IF NOT TRY AGAIN

MOVB @TKB, -(SP) ;; PICK UP CHAR
BIC #^C177, (SP) ;; MAKE IT 7-BIT ASCII
```

```

(1) 026502 021627 000025    9$:   (MP   (SP),#25    ;;IS IT A CONTROL-U?
(1) 026506 001005          BNE   10$       ;;BRANCH IF NOT
(1) 026510 104401 027112      TYPE  $CNTLU    ;;YES, ECHO CONTROL-U (^U)
(1) 026514 062706 000006    20$:  ADD   #6,SP     ;;IGNORE PREVIOUS INPUT
(1) 026520 000757          BR    19$       ;;LET'S TRY IT AGAIN
(1)
(1)
(1) 026522 021627 000015    10$:  (MP   (SP),#15    ;;IS IT A <CR>?
(1) 026526 001022          BNE   16$       ;;BRANCH IF NO
(1) 026530 005766 000004      TST   4(SP)     ;;YES, IS IT THE FIRST CHAR?
(1) 026534 001403          BEQ   11$       ;;BRANCH IF YES
(1) 026536 016677 000002 152374  MOV   2(SP),@SWR ;;SAVE NEW SWR
(1) 026544 062706 000006    11$:  ADD   #6,SP     ;;CLEAR UP STACK
(1) 026550 104401 001177    14$:  TYPE  $CRLF    ;;ECHO <CR> AND <LF>
(1) 026554 123727 001135 000001  (MPB  $INTAG,#1 ;;RE-ENABLE TTY KBD INTERRUPTS?
(1) 026562 001003          BNE   15$       ;;BRANCH IF NOT
(1) 026564 012777 000100 152352  MOV   #100,@STKS ;;RE-ENABLE TTY KBD INTERRUPTS
(1) 026572 000002          RTI                    ;;RETURN
(1) 026574 004737 027360    16$:  JSR   PC,$TYPEC ;;ECHO CHAR
(1) 026600 021627 000060      (MP   (SP),#50    ;;CHAR < 0?
(1) 026604 002420          BLT   18$       ;;BRANCH IF YES
(1) 026606 021627 000067      (MP   (SP),#67    ;;CHAR > 7?
(1) 026612 003015          BGT   18$       ;;BRANCH IF YES
(1) 026614 042726 000060      BIC   #60,(SP)+ ;;STRIP-OFF ASCII
(1) 026620 005766 000002      TST   2(SP)     ;;IS THIS THE FIRST CHAR
(1) 026624 001403          BEQ   17$       ;;BRANCH IF YES
(1) 026626 006316          ASL   (SP)      ;;NO, SHIFT PRESENT
(1) 026630 006316          ASL   (SP)      ;;  CHAR OVER TO MAKE
(1) 026632 006316          ASL   (SP)      ;;  ROOM FOR NEW ONE.
(1) 026634 005266 000002    17$:  INC   2(SP)     ;;KEEP COUNT OF CHAR
(1) 026640 056616 177776      BIS   -2(SP), (SP) ;;SET IN NEW CHAR
(1) 026644 000707          BR    7$        ;;GET THE NEXT ONE
(1) 026646 104401 001176    18$:  TYPE  $QUES    ;;TYPE ?<CR><LF>
(1) 026652 000720          BR    20$      ;;SIMULATE CONTROL-U
(1)
(1) .DSABL LSB
(1)
(1)
(2)
(1) *****
(1) *THIS ROUTINE WILL INPUT A SINGLE CHARACTER FROM THE TTY
(1) *CALL:
(1) *   RDCHR                    ;;INPUT A SINGLE CHARACTER FROM THE TTY
(1) *   RETURN HERE              ;;CHARACTER IS ON THE STACK
(1) *                               ;;WITH PARITY BIT STRIPPED OFF
(1)
(1)
(1) SRDCHR: MOV   (SP),-(SP)     ;;PUSH DOWN THE PC
(1) 026654 011646          MOV   4(SP),2(SP) ;;SAVE THE PS
(1) 026656 016666 000004 000002    1$:  TSTB @STKS      ;;WAIT FOR
(1) 026664 105777 152254          BPL   1$        ;;A CHARACTER
(1) 026670 100375          MOVB @STKB,4(SP) ;;READ THE TTY
(1) 026672 117766 152250 000004      BIC   #^C<177>,4(SP) ;;GET RID OF JUNK IF ANY
(1) 026700 042766 177600 000004      (MP   4(SP),#23   ;;IS IT A CONTROL-S?
(1) 026706 026627 000004 000023      BNE   3$        ;;BRANCH IF NO
(1) 026714 001013          TSTB @STKS      ;;WAIT FOR A CHARACTER
(1) 026716 105777 152222    2$:  BPL   2$        ;;LOOP UNTIL ITS THERE
(1) 026722 100375          MOVB @STKB,-(SP) ;;GET CHARACTER
(1) 026724 117746 152216

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```
(1) 026730 042716 177600 BIC #^C177,(SP) ;;MAKE IT 7-BIT ASCII
(1) 026734 022627 000021 CMP (SP)+,#21 ;;IS IT A CONTROL-Q?
(1) 026740 001366 BNE 2$ ;;IF NOT DISCARD IT
(1) 026742 000750 BR 1$ ;;YES, RESUME
(1) 026744 026627 000004 000140 3$: CMP 4(SP),#140 ;;IS IT UPPER CASE?
(1) 026752 002407 BLT 4$ ;;BRANCH IF YES
(1) 026754 026627 000004 000175 CMP 4(SP),#175 ;;IS IT A SPECIAL CHAR?
(1) 026762 003003 BGT 4$ ;;BRANCH IF YES
(1) 026764 042766 000040 000004 BIC #40,4(SP) ;;MAKE IT UPPER CASE
(1) 026772 000002 4$: RTI ;;GO BACK TO USER
(2) ;*****
(1) ;*THIS ROUTINE WILL INPUT A STRING FROM THE TTY
(1) ;*CALL:
(1) ;* RDLIN ;;INPUT A STRING FROM THE TTY
(1) ;* RETURN HERE ;;ADDRESS OF FIRST CHARACTER WILL BE ON THE STACK
(1) ;* ;;TERMINATOR WILL BE A BYTE OF ALL 0'S
(1) ;
(1) 026774 010346 $RDLIN: MOV R3,-(SP) ;;SAVE R3
(1) 026776 012703 027102 1$: MOV #$TTYIN,R3 ;;GET ADDRESS
(1) 027002 022703 027112 2$: CMP #$TTYIN+8.,R3 ;;BUFFER FULL?
(1) 027006 101405 BLOS 4$ ;;BR IF YES
(1) 027010 104410 RDCHR ;;GO READ ONE CHARACTER FROM THE TTY
(1) 027012 112613 MOVB (SP)+,(R3) ;;GET CHARACTER
(1) 027014 122713 000177 10$: CMPB #177,(R3) ;;IS IT A RUBOUT
(1) 027020 001003 BNE 3$ ;;SKIP IF NOT
(1) 027022 104401 001176 4$: TYPE ,SQUES ;;TYPE A '?'
(1) 027026 000763 BR 1$ ;;CLEAR THE BUFFER AND LOOP
(1) 027030 111337 027100 3$: MOVB (R3),9$ ;;ECHO THE CHARACTER
(1) 027034 104401 027100 TYPE ,9$
(1) 027040 122723 000015 CMPB #15,(R3)+ ;;CHECK FOR RETURN
(1) 027044 001356 BNE 2$ ;;LOOP IF NOT RETURN
(1) 027046 105063 177777 CLRB -1(R3) ;;CLEAR RETURN (THE '5')
(1) 027052 104401 001200 TYPE ,SLF ;;TYPE A LINE FEED
(1) 027056 012603 MOV (SP)+,R3 ;;RESTORE R3
(1) 027060 011646 MOV (SP),-(SP) ;;ADJUST THE STACK AND PUT ADDRESS OF THE
(1) 027062 016666 000004 000002 MOV 4(SP),2(SP) ;; FIRST ASCII CHARACTER ON IT
(1) 027070 012766 027102 000004 MOV #$TTYIN,4(SP)
(1) 027076 000002 RTI ;;RETURN
(1) 027100 000 9$: .BYTE 0 ;;STORAGE FOR ASCII CHAR. TO TYPE
(1) 027101 000 .BYTE 0 ;;TERMINATOR
(1) 027102 000010 .BLKB 8. ;;RESERVE 8 BYTES FOR TTY INPUT
(1) 027112 052536 005015 000 $UNILG: .ASCIZ /^U/<15><12> ;;CONTROL 'U'
(1) 027117 136 006507 000012 $MSWR: .ASCIZ /^G/<15><12> ;;CONTROL 'G'
(1) 027124 005015 053523 020122 $MNEW: .ASCIZ <15><12>/SWR = /
(1) 027132 020075 000
(1) 027135 040 047040 053505 $MNEW: .ASCIZ / NEW = /
(1) 027142 036440 000040
```

5528

.SBTTL TYPE ROUTINE

```
(1) ;*****
(2) ;*ROUTINE TO TYPE ASCII MESSAGE. MESSAGE MUST TERMINATE WITH A 0 BYTE.
(1) ;*THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.
(1) ;*NOTE1: $NULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.
(1) ;*NOTE2: $FILLS CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.
(1) ;*NOTE3: $FILLC CONTAINS THE CHARACTER TO FILL AFTER.
(1) ;*
```

```

(1)          ;*CALL:
(1)          ;*1) USING A TRAP INSTRUCTION
(1)          ;*          TYPE      ,MESADR          ;;MESADR IS FIRST ADDRESS OF AN ASCIZ STRING
(1)          ;*OR
(1)          ;*          TYPE
(1)          ;*          MESADR
(1)          ;*
(1) 027146 105737 001157 $TYPE: TSTB $TPFLG          ;; IS THERE A TERMINAL?
(1) 027152 100002          BPL 1$          ;; BR IF YES
(1) 027154 000000          HALT          ;; HALT HERE IF NO TERMINAL
(1) 027156 000430          BR 3$          ;; LEAVE
(1) 027160 010046          1$: MOV R0,-(SP)          ;; SAVE R0
(1) 027162 017600 000002 MOV @2(SP),R0          ;; GET ADDRESS OF ASCIZ STRING
(1) 027166 122737 000001 001222 CMPB #APTENV,$ENV          ;; RUNNING IN APT MODE
(1) 027174 001011          BNE 62$          ;; NO,GO CHECK FOR APT CONSOLE
(1) 027176 132737 000100 001223 BITB #APTSPOOL,$ENVM          ;; SPOOL MESSAGE TO APT
(1) 027204 001405          BEQ 62$          ;; NO,GO CHECK FOR CONSOLE
(1) 027206 010037 027216 MOV R0,61$          ;; SETUP MESSAGE ADDRESS FOR APT
(1) 027212 004737 027436 JSR PC,$ATY3          ;; SPOOL MESSAGE TO APT
(1) 027216 000000          61$: .WORD 0          ;; MESSAGE ADDRESS
(1) 027220 132737 000040 001223 62$: BITB #APTCSUP,$ENVM          ;; APT CONSOLE SUPPRESSED
(1) 027226 001003          BNE 60$          ;; YES,SKIP TYPE OUT
(1) 027230 112046          2$: MOVB (R0)+,-(SP)          ;; PUSH CHARACTER TO BE TYPED ONTO STACK
(1) 027232 001005          BNE 4$          ;; BR IF IT ISN'T THE TERMINATOR
(1) 027234 005726          TST (SP)+          ;; IF TERMINATOR POP IT OFF THE STACK
(1) 027236 012600          60$: MOV (SP)+,R0          ;; RESTORE R0
(1) 027240 062716 000002 3$: ADD #2,(SP)          ;; ADJUST RETURN PC
(1) 027244 000002          RTI          ;; RETURN
(1) 027246 122716 000011 4$: CMPB #HT,(SP)          ;; BRANCH IF <HT>
(1) 027252 001430          BEQ 8$          ;; BRANCH IF NOT <CRLF>
(1) 027254 122716 000200 CMPB #CRLF,(SP)          ;; BRANCH IF NOT <CRLF>
(1) 027260 001006          BNE 5$          ;; POP <CR><LF> EQUIV
(1) 027262 005726          TST (SP)+          ;; TYPE A CR AND LF
(1) 027264 104401          TYPE          ;; TYPE A CR AND LF
(1) 027266 001177          $CRLF
(1) 027270 105037 027424 CLRB $CHARCNT          ;; CLEAR CHARACTER COUNT
(1) 027274 000755          BR 2$          ;; GET NEXT CHARACTER
(1) 027276 004737 027360 5$: JSR PC,$TYPEC          ;; GO TYPE THIS CHARACTER
(1) 027302 123726 001156 6$: CMPB $FILLC,(SP)+          ;; IS IT TIME FOR FILLER CHARS.?
(1) 027306 001350          BNE 2$          ;; IF NO GO GET NEXT CHAR.
(1) 027310 013746 001154 MOV $NULL,-(SP)          ;; GET # OF FILLER CHARS. NEEDED
(1)          ;; AND THE NULL CHAR.
(1) 027314 105366 000001 7$: DECB 1(SP)          ;; DOES A NULL NEED TO BE TYPED?
(1) 027320 002770          BLT 6$          ;; BR IF NO--GO POP THE NULL OFF OF STACK
(1) 027322 004737 027360 JSR PC,$TYPEC          ;; GO TYPE A NULL
(1) 027326 105337 027424 DECB $CHARCNT          ;; DO NOT COUNT AS A COUNT
(1) 027332 000770          BR 7$          ;; LOOP
(1)
(1)          ;HORIZONTAL TAB PROCESSOR
(1)
(1) 027334 112716 000040 8$: MOVB #' ,(SP)          ;; REPLACE TAB WITH SPACE
(1) 027340 004737 027360 9$: JSR PC,$TYPEC          ;; TYPE A SPACE
(1) 027344 132737 000007 027424 BITB #7,$CHARCNT          ;; BRANCH IF NOT AT
(1) 027352 001372          BNE 9$          ;; TAB STOP
(1) 027354 005726          TST (SP)+          ;; POP SPACE OFF STACK

```



```
(1) 027356 000724 BR 2$ ::GET NEXT CHARACTER
(1) 027360 105777 151564 $TYPEC: TSTB @STPS ::WAIT UNTIL PRINTER IS READY
(1) 027364 100375 BPL $TYPEC
(1) 027366 116677 000002 151556 MOV 2(SP),@STPB ::LOAD CHAR TO BE TYPED INTO DATA REG.
(1) 027374 122766 000015 000002 CMPB #CR,2(SP) ::IS CHARACTER A CARRIAGE RETURN?
(1) 027402 001003 BNE 1$ ::BRANCH IF NO
(1) 027404 105037 027424 CLRB $CHARCNT ::YES--CLEAR CHARACTER COUNT
(1) 027410 000406 BR $TYPEX ::EXIT
(1) 027412 122766 000012 000002 1$: CMPB #LF,2(SP) ::IS CHARACTER A LINE FEED?
(1) 027420 001402 BEQ $TYPEX ::BRANCH IF YES
(1) 027422 105227 INCB (PC)+ ::COUNT THE CHARACTER
(1) 027424 000000 $CHARCNT: .WORD 0 ::CHARACTER COUNT STORAGE
(1) 027426 000207 $TYPEX: RTS PC
```

5529 (1) .SBTTL APT COMMUNICATIONS ROUTINE

```
(2) ::*****
(1) 027430 112737 000001 027674 $ATY1: MOV #1,$FFLG ::TO REPORT FATAL ERROR
(1) 027436 112737 000001 027672 $ATY3: MOV #1,$MFLG ::TO TYPE A MESSAGE
(1) 027444 000403 BR $ATYC
(1) 027446 112737 000001 027674 $ATY4: MOV #1,$FFLG ::TO ONLY REPORT FATAL ERROR
(1) 027454 $ATYC:
(3) 027454 010046 MOV R0,-(SP) ::PUSH R0 ON STACK
(3) 027456 010146 MOV R1,-(SP) ::PUSH R1 ON STACK
(1) 027460 105737 027672 TSTB $MFLG ::SHOULD TYPE A MESSAGE?
(1) 027464 001450 BEQ 5$ ::IF NOT: BR
(1) 027466 122737 000001 001222 CMPB #APTENV,$ENV ::OPERATING UNDER APT?
(1) 027474 001031 BNE 3$ ::IF NOT: BR
(1) 027476 132737 000100 001223 BITB #APTPOOL,$ENVM ::SHOULD SPOOL MESSAGES?
(1) 027504 001425 BEQ 3$ ::IF NOT: BR
(1) 027506 017600 000004 MOV @4(SP),R0 ::GET MESSAGE ADDR.
(1) 027512 062766 000002 000004 ADD #2,4(SP) ::BUMP RETURN ADDR.
(1) 027520 005737 001202 1$: TST $MSGTYPE ::SEE IF DONE W/ LAST XMISSION?
(1) 027524 001375 BNE 1$ ::IF NOT: WAIT
(1) 027526 010037 001216 MOV R0,$MSGAD ::PUT ADDR IN MAILBOX
(1) 027532 105720 2$: TSTB (R0)+ ::FIND END OF MESSAGE
(1) 027534 001376 BNE 2$
(1) 027536 163700 001216 SUB $MSGAD,R0 ::SUB START OF MESSAGE
(1) 027542 006200 ASR R0 ::GET MESSAGE LNGTH IN WORDS
(1) 027544 010037 001220 MOV R0,$MSGGLT ::PUT LENGTH IN MAILBOX
(1) 027550 012737 000004 001202 MOV #4,$MSGTYPE ::TELL APT TO TAKE MSG.
(1) 027556 000413 BR 5$
(1) 027560 017637 000004 027604 3$: MOV @4(SP),4$ ::PUT MSG ADDR IN JSR LINKAGE
(1) 027566 062766 000002 000004 ADD #2,4(SP) ::BUMP RETURN ADDRESS
(3) 027574 013746 177776 MOV 177776,-(SP) ::PUSH 177776 ON STACK
(1) 027600 004737 027146 JSR PC,$TYPE ::CALL TYPE MACRO
(1) 027604 000000 4$: .WORD 0
(1) 027606 5$:
(1) 027606 105737 027674 10$: TSTB $FFLG ::SHOULD REPORT FATAL ERROR?
(1) 027612 001416 BEQ 12$ ::IF NOT: BR
(1) 027614 005737 001222 TST $ENV ::RUNNING UNDER APT?
(1) 027620 001413 BEQ 12$ ::IF NOT: BR
(1) 027622 005737 001202 11$: TST $MSGTYPE ::FINISHED LAST MESSAGE?
(1) 027626 001375 BNE 11$ ::IF NOT: WAIT
(1) 027630 017637 000004 001204 MOV @4(SP),$FATAL ::GET ERROR #
(1) 027636 062766 000002 000004 ADD #2,4(SP) ::BUMP RETURN ADDR.
```

```

(1) 027644 005237 001202      INC      $MSGTYPE      ;; TELL APT TO TAKE ERROR
(1) 027650 105037 027674      12$: CLR B $FFLG      ;; CLEAR FATAL FLAG
(1) 027654 105037 027673      CLR B $LFLG      ;; CLEAR LOG FLAG
(1) 027660 105037 027672      CLR B $MFLG      ;; CLEAR MESSAGE FLAG
(3) 027664 012601      MOV      (SP)+,R1      ;; POP STACK INTO R1
(3) 027666 012600      MOV      (SP)+,R0      ;; POP STACK INTO R0
(1) 027670 000207      RTS      PC          ;; RETURN
(1) 027672      000      $MFLG: .BYTE 0      ;; MESSG. FLAG
(1) 027673      000      $LFLG: .BYTE 0      ;; LOG FLAG
(1) 027674      000      $FFLG: .BYTE 0      ;; FATAL FLAG
(1)      027676      .EVEN
(1)      000200      APTSIZE=200
(1)      000001      APTENV=001
(1)      000100      APTSPool=100
(1)      000040      APTCSUP=040
5530      .SBTTL POWER DOWN AND UP ROUTINES
(1)
(2)      ;; *****
(1)      :POWER DOWN ROUTINE
(1) 027676 012737 030036 000024 $PWDRN: MOV      #$ILLUP,@#PWRVEC ;; SET FOR FAST UP
(1) 027704 012737 000340 000026      MOV      #340,@#PWRVEC+2 ;; PRIO:7
(3) 027712 010046      MOV      R0,-(SP)      ;; PUSH R0 ON STACK
(3) 027714 010146      MOV      R1,-(SP)      ;; PUSH R1 ON STACK
(3) 027716 010246      MOV      R2,-(SP)      ;; PUSH R2 ON STACK
(3) 027720 010346      MOV      R3,-(SP)      ;; PUSH R3 ON STACK
(3) 027722 010446      MOV      R4,-(SP)      ;; PUSH R4 ON STACK
(3) 027724 010546      MOV      R5,-(SP)      ;; PUSH R5 ON STACK
(3) 027726 017746 151206      MOV      @SWR,-(SP)      ;; PUSH @SWR ON STACK
(1) 027732 010637 030042      MOV      SP,$SAVR6      ;; SAVE SP
(1) 027736 012737 027750 000024      MOV      #SPWRUP,@#PWRVEC ;; SET UP VECTOR
(1) 027744 000000      HALT
(1) 027746 000776      BR      .-2          ;; HANG UP
(1)
(2)      ;; *****
(1)      :POWER UP ROUTINE
(1) 027750 012737 030036 000024 $PWRUP: MOV      #$ILLUP,@#PWRVEC ;; SET FOR FAST DOWN
(1) 027756 013706 030042      MOV      $SAVR6,SP      ;; GET SP
(1) 027762 005037 030042      CLR      $SAVR6      ;; WAIT LOOP FOR THE TTY
(1) 027766 005237 030042      1$: INC      $SAVR6      ;; WAIT FOR THE INC
(1) 027772 001375      BNE     1$          ;; OF WORD
(3) 027774 012677 151140      MOV      (SP)+,@SWR      ;; POP STACK INTO @SWR
(3) 030000 012605      MOV      (SP)+,R5      ;; POP STACK INTO R5
(3) 030002 012604      MOV      (SP)+,R4      ;; POP STACK INTO R4
(3) 030004 012603      MOV      (SP)+,R3      ;; POP STACK INTO R3
(3) 030006 012602      MOV      (SP)+,R2      ;; POP STACK INTO R2
(3) 030010 012601      MOV      (SP)+,R1      ;; POP STACK INTO R1
(3) 030012 012600      MOV      (SP)+,R0      ;; POP STACK INTO R0
(1) 030014 012737 027676 000024      MOV      #SPWRDN,@#PWRVEC ;; SET UP THE POWER DOWN VECTOR
(1) 030022 012737 000340 000026      MOV      #340,@#PWRVEC+2 ;; PRIO:7
(1) 030030 104401      TYPE      ;; REPORT THE POWER FAILURE
(1) 030032 030044      $PWRMG: .WORD $POWER      ;; POWER FAIL MESSAGE POINTER
(1) 030034 000002      RTI
(1) 030036 000000      $ILLUP: HALT      ;; THE POWER UP SEQUENCE WAS STARTED
(1) 030040 000776      BR      .-2          ;; BEFORE THE POWER DOWN WAS COMPLETE
(1) 030042 000000      $SAVR6: 0      ;; PUT THE SP HERE
(1) 030044 005015 047520 042527 $POWER: .ASCIZ <15><12>'POWER''

```

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(1) 030052 000122
(1)
5531 (1)
(1)
(2)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1) 030054 010046
(1) 030056 016600 000002
(1) 030062 005740
(1) 030064 111000
(1) 030066 006300
(1) 030070 016000 030110
(1) 030074 000200
(1)
(1)
(1)
(1)
(1)
(1)
(1) 030076 011646
(1) 030100 016666 000004 000002
(1) 030106 000002
(1)
(3)
(3)
(3)
(3)
(3)
(3)
(3)
(3)
(3) 030110 030076
(3) 030112 027146
(3) 030114 025040
(3) 030116 025014
(3) 030120 025054
(3) 030122 025564
(1)
(3) 030124 026442
(1)
(3) 030126 026372
(3) 030130 026654
(3) 030132 026774
(3) 030134 026270
5532 030136 024640
5533 030140 005015 046103 041517 EM1:
030146 040513 051440 020122
030154 052506 041516 044524
030162 047117 042440 051122
030170 051117 000
5534 030173 015 041412 047514 EM2:
030200 045503 020101 051123
030206 042040 052101 020101
030214 051105 047522 000122
5535 030222 005015 046103 041517 EM3:

```

.EVEN  
.SBTTL TRAP DECODER

```

*****
*THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE 'TRAP' INSTRUCTION
*AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS
*OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
*GO TO THAT ROUTINE.
$TRAP: MOV R0,-(SP) ;;SAVE R0
MOV 2(SP),R0 ;;GET TRAP ADDRESS
TST -(R0) ;;BACKUP BY 2
MOVB (R0),R0 ;;GET RIGHT BYTE OF TRAP
ASL R0 ;;POSITION FOR INDEXING
MOV $TRPAD(R0),R0 ;;INDEX TO TABLE
RTS R0 ;;GO TO ROUTINE

;;THIS IS USE TO HANDLE THE 'GETPRI' MACRO
$TRAP2: MOV (SP),-(SP) ;;MOVE THE PC DOWN
MOV 4(SP),2(SP) ;;MOVE THE PSW DOWN
RTI ;;RESTORE THE PSW

.SBTTL TRAP TABLE

*THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED
*BY THE 'TRAP' INSTRUCTION.

: ROUTINE
:-----
$TRPAD: .WORD $TRAP2
$TYPE ;;CALL=TYPE TRAP+1(104401) TTY TYPEOUT ROUTINE
$TYPOC ;;CALL=TYPOC TRAP+2(104402) TYPE OCTAL NUMBER (WITH LEADING ZEROS)
$TYPOS ;;CALL=TYPOS TRAP+3(104403) TYPE OCTAL NUMBER (NO LEADING ZEROS)
$TYPON ;;CALL=TYPON TRAP+4(104404) TYPE OCTAL NUMBER (AS PER LAST CALL)
$TYPDS ;;CALL=TYPDS TRAP+5(104405) TYPE DECIMAL NUMBER (WITH SIGN)

$GTSWR ;;CALL=GTSWR TRAP+6(104406) GET SOFT-SWR SETTING

$CKSWR ;;CALL=CKSWR TRAP+7(104407) TEST FOR CHANGE IN SOFT-SWR
$RDCHR ;;CALL=RDCHR TRAP+10(104410) TTY TYPEIN CHARACTER ROUTINE
$RDLIN ;;CALL=RDLIN TRAP+11(104411) TTY TYPEIN STRING ROUTINE
$RDOCT ;;CALL=RDOCT TRAP+12(104412) READ AN OCTAL NUMBER FROM TTY
IOTRD ;;CALL=IOTT TRAP+13(104413)

.ASCIZ <15><12>/CLOCKA SR FUNCTION ERROR/

.ASCIZ <15><12>/CLOCKA SR DATA ERROR/

.ASCIZ <15><12>/CLOCKA BR DATA ERROR/

```

Address	Code	Address	Code	Description
030230	040513	041040	020122	
030236	040504	040524	042440	
030244	051122	051117	000	
5536	030251	015 041412	047514	EM4: .ASCIZ <15><12>/CLOCKA CR DATA ERROR/
	030256	045503	020101	
	030264	042040	052101	
	030272	051105	047522	
5537	030300	005015	046103	EM5: .ASCIZ <15><12>/CLOCKB SR DATA ERROR/
	030306	041113	051440	
	030314	040504	040524	
	030322	051122	051117	
5538	030327	015 041412	047514	EM6: .ASCIZ <15><12>/CLOCKB BR DATA ERROR/
	030334	045503	020102	
	030342	042040	052101	
	030350	051105	047522	
5539	030356	005015	046103	EM7: .ASCIZ <15><12>/CLOCKB CR DATA ERROR/
	030364	041113	041440	
	030372	040504	040524	
	030400	051122	051117	
5540	030405	015 042012	040525	EM10: .ASCIZ <15><12>/DUAL ADDRESS ERROR/
	030412	020114	042101	
	030420	051505	020123	
	030426	047522	000122	
5541	030432	005015	046103	EM11: .ASCIZ <15><12>#CLOCK A COUNT ERROR #
	030440	020113	020101	
	030446	047125	020124	
	030454	047522	020122	
5542	030461	015 041412	047514	EM12: .ASCIZ <15><12>#CLOCK A COUNT FUNCTION ERROR #
	030466	045503	040440	
	030474	052517	052116	
	030502	047125	052103	
	030510	020116	051105	
	030516	020122	000	
5543	030521	015 041412	047514	EM14: .ASCIZ <15><12>#CLOCK B COUNT FUNCTION ERROR #
	030526	045503	041040	
	030534	052517	052116	
	030542	047125	052103	
	030550	020116	051105	
	030556	020122	000	
5544	030561	015 041412	047514	EM15: .ASCIZ <15><12>#CLOCK B COUNT ERROR #
	030566	045503	041040	
	030574	052517	052116	
	030602	051122	051117	
5545	030610	005015	046103	EM16: .ASCIZ <15><12>#CLOCK A INTERRUPT ERROR #
	030616	020113	020101	
	030624	042524	051122	
	030632	020124	051105	
	030640	020122	000	
5546	030643	015 041412	047514	EM17: .ASCIZ <15><12>#CLOCK B INTERRUPT ERROR #
	030650	045503	041040	
	030656	052116	051105	
	030664	052120	042440	
	030672	051117	000040	
5547	030676	005015	046103	EM20: .ASCIZ <15><12>#CLOCK A REPEATABILITY ERROR #
	030704	020113	020101	
	030712	042520	052101	



	031346	020104	020040	042040								
	031354	052101	020101	042522								
	031362	042101	043040	047522								
	031370	115										
5558	031371	015	020012	050040		.ASCIZ	<15><12>/	PC	ADDR	ADDR	DATA	DUAL ADDRESS/
	031376	020103	020040	040440								
	031404	042104	020122	020040								
	031412	040440	042104	020122								
	031420	020040	042040	052101								
	031426	020101	020040	042040								
	031434	040525	020114	042101								
	031442	051104	051505	000123								
5559	031450	005015	051105	050122	DH12:	.ASCIZ	<15><12>#ERRPC		ASR #			
	031456	020103	020040	051501								
	031464	020122	000									
5560	031467	015	042412	051122	DH14:	.ASCIZ	<15><12>#ERRPC		BSR#			
	031474	041520	020040	041040								
	031502	051123	000									
5561	031505	015	042412	051122	DH20:	.ASCIZ	<15><12>#ERRPC		ASR	2NDCNT	1STCNT #	
	031512	041520	020040	040440								
	031520	051123	020040	020040								
	031526	031040	042116	047103								
	031534	020124	030440	052123								
	031542	047103	020124	000								
5562	031547	015	042412	051122	DH23:	.ASCIZ	<15><12>#ERRPC		BSR	2NDCNT	1STCNT #	
	031554	041520	020040	041040								
	031562	051123	020040	020040								
	031570	031040	042116	047103								
	031576	020124	030440	052123								
	031604	047103	020124	000								
5563	031611	015	042412	051122	DH26:	.ASCIZ	<15><12>#ERRPC		CLOCK ADDR.#			
	031616	041520	020040	041440								
	031624	047514	045503	040440								
	031632	042104	027122	000								
5564												
5565		031640				.EVEN						
5566												
5567	031640	001116	001326	001126	DT1:	.WORD	\$ERRPC,ASR,\$BDDAT,\$GDDAT,0					
	031646	001124	000000									
5568	031652	001116	001330	001126	DT3:	.WORD	\$ERRPC,ABR,\$BDDAT,\$GDDAT,0					
	031660	001124	000000									
5569	031664	001116	001332	001126	DT4:	.WORD	\$ERRPC,ACR,\$BDDAT,\$GDDAT,0					
	031672	001124	000000									
5570	031676	001116	001334	001126	DT5:	.WORD	\$ERRPC,BSR,\$BDDAT,\$GDDAT,0					
	031704	001124	000000									
5571	031710	001116	001336	001126	DT6:	.WORD	\$ERRPC,BBR,\$BDDAT,\$GDDAT,0					
	031716	001124	000000									
5572	031722	001116	001340	001126	DT7:	.WORD	\$ERRPC,BCR,\$BDDAT,\$GDDAT,0					
	031730	001124	000000									
5573	031734	001116	001120	001122	DT10:	.WORD	\$ERRPC,\$GDADR,\$BDADR,\$GDDAT,\$BDDAT,0					
	031742	001124	001126	000000								
5574	031750	001116	001326	000000	DT12:	.WORD	\$ERRPC,ASR,0					
5575	031756	001116	001334	000000	DT14:	.WORD	\$ERRPC,BSR,0					
5576	031764	001116	001332	001124	DT21:	.WORD	\$ERRPC,ACR,\$GDDAT,\$TMP0,0					
	031772	001164	000000									
5577	031776	001116	001332	001126	DT22:	.WORD	\$ERRPC,ACR,\$BDDAT,\$TMP0,0					



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(2) 032120 052777 040000 147512      BIS      #BIT14,@KMADO      ;ISSUE KMC+DMC INIT.
(2)
(2) 032126      1$:
(2)
(2) 032126 010146      MOV      R1,-(SP)
(2) 032130 005001      CLR      R1
(2) 032132 005201      INC      R1              ;STALL FOR DMC-UP
(2) 032134 001376      BNE      2$
(2) 032136 012777 104000 147474      MOV      #BIT15.BIT11,@KMADO      ;SET RUN, AND ENABLE ARBITRATION.
(2) 032144 105201      INCB    R1
(2) 032146 001376      BNE      25$
(2)
(2) 032150 032777 000040 147462      BIT      #BIT5,@KMADO      ;SLAVE READY? (READING IPBM SR)
(2) 032156 001401      BEQ      3$
(2)
(2) 032160 104000      ERROR
(2)
(2) 032162 012777 000004 147454      3$: MOV      #4,@KMAD2      ;READ FAST PATH
(2) 032170      4$:
(3) 032170 004537 033636      JSR      R5,$TOUT      ;-TOUT-CHECK FOR TIMEOUT
(3)
(3) 032174 104000      ERROR      ;/TIME-OUT ERROR
(3)
(3)
(3)
(3)
(3)
(3)
(3) 032176 000774      BR              4$
(3)
(3)
(2) 032200 122777 000377 147436      CMPB    #377,@KMAD2      ;/RETURNS HERE-FROM-TIMED OUT.
(2) 032206 001370      BNE      4$      ;WAIT TILL KMC DONE COMMAND.
(2) 032210 122777 000377 147432      CMPB    #377,@KMAD4      ;IF FAST PATH=377 THEN ERROR.
(2) 032216 001001      BNE      35$
(2) 032220 104000      ERROR      ;IPBM ERROR (SLAVE SIDE)
(2)
(2)
(2) 032222 122777 000004 147420      35$: CMPB    #4,@KMAD4      ;IS THIS THE CORRECT VERSION OF MICRO-CODE?
(2) 032230 001543      BEQ      5$      ;YES-CONTINUE.
(2) 032232 005227 177777      INC      #-1
(2) 032236 001140      BNE      5$
(2) 032240 005227 177777      INC      #-1
(2) 032244 001135      BNE      5$
(3) 032246 104401 032254      TYPE    ,67$      ;;TYPE ASCIZ STRING
(3) 032252 000440      BR      66$      ;;GET OVER THE ASCIZ
(3)
(3) 032354      ;;67$: .ASCIZ <200>'W A R N I N G THIS PROGRAM WAS DESIGNED TO RUN WITH VERSION 4''
(3) 032354 104401 032362      66$: TYPE    ,69$      ;;TYPE ASCIZ STRING
(3) 032360 000430      BR      68$      ;;GET OVER THE ASCIZ
(3)
(3) 032442      ;;69$: .ASCIZ <200>'MICRO-CODE. ANOTHER VERSION CODE WAS DETECTED.'"
(3) 032442 104401 032450      68$: TYPE    ,71$      ;;TYPE ASCIZ STRING
(3) 032446 000434      BR      70$      ;;GET OVER THE ASCIZ
(3)
(3) 032540      ;;71$: .ASCIZ <200>'THIS MAY OR MAYNOT CAUSE FALSE ERROR TO BE REPORTED.'"<200><200>
(3)
(2)

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(2) 032540 112737 177777 032672 5$:   MOVB   #0-1,11$   ;DAC CODE FOR SLAVE.
(2) 032546 012501                MOV     (5)+,R1    ;GET NEXT DEVICE ADDR.
(2) 032550 021127 000000        6$:   CMP     (R1),#0    ;TERM REACHED?
(2) 032554 001444                BEQ     10$
(2) 032556 105237 032672        INCB   11$
(2) 032562 113777 032672 147060    MOVB   11$,@KMAD4 ;FIFO DATA
(2) 032570 004737 032674        JSR    PC,20$     ;ISSUE SEND
(2) 032574 112177 147050        MOVB   (R1)+,@KMAD4 ;SEND LOW BYTE OF DEVICE ADDR TO SLAVE.
(2) 032600 004737 032674        JSR    PC,20$     ;ISSUE SEND
(2) 032604 112177 147040        MOVB   (R1)+,@KMAD4 ;SEND HIGH BYTE OF DEVICE ADDR. TO SLAVE.
(2) 032610 004737 032674        JSR    PC,20$
(2) 032614 032777 000002 147016 7$:   BIT     #BIT1,@KMAD0 ;WAIT FOR FIFO DATA
(2) 032622 001374                BNE    7$         ;-1 NO DATA. =0 DATA.
(2) 032624 112777 000002 147012    MOVB   #2,@KMAD2  ;READ FIFO.
(2) 032632                8$:
(3) 032632 004537 033636        JSR    R5,$TOUT   ;-TOUT-CHECK FOR TIMEOUT
(3) 032636 104000                ERROR            ;/TIME-OUT ERROR
(3)                                ;/WE FAILED TO COMPLETE
(3)                                ;/CURRENT OPERATION.
(3)                                ;/CONTINUES IN THIS LOOP
(3)                                ;/WOULD MAKE US 'HANG' HERE
(3) 032640 000774                BR      8$
(3)                                ;/RETURNS HERE-FROM-TIMED OUT.
(2) 032642 122777 000377 146774    CMPB   #377,@KMAD2 ;WAIT FOR READ.
(2) 032650 001370                BNE    8$
(2) 032652 105777 146772        TSTB   @KMAD4     ;WAS A ZERO RETURNED?
(2) 032656 001734                BEQ     6$         ;YES GET NEXT ADDR.
(2)                                ;SLAVE WILL RETURN CODE 0 IF
(2) 032660 005237 032724        INC     $AERR     ;DEV PRESENT. ELSE
(2)                                ;EXIT $AERR=1 IF SLAVE GIVES ERROR.
(2) 032664 005041                CLR    -(1)       ;GET RID OF REFERENCE TO BAD ADDR.
(2) 032666 012601                10$:  MOV     (SP)+,R1
(2) 032670 000205                RTS     R5        ;RETURN ALL ADDR. CHECKED.
(2) 032672 000000                11$:  .WORD  0        ;HOLDS DAC CODE PLUS OFFSET
(2)                                ;TO SLAVES ADDR. TABLE.
(2) 032674 112777 000003 146742 20$:  MOVB   #3,@KMAD2 ;ISSUE FIFO WRITE
(2) 032702                21$:
(3) 032702 004537 033636        JSR    R5,$TOUT   ;-TOUT-CHECK FOR TIMEOUT
(3) 032706 104000                ERROR            ;/TIME-OUT ERROR
(3)                                ;/WE FAILED TO COMPLETE
(3)                                ;/CURRENT OPERATION.
(3)                                ;/CONTINUES IN THIS LOOP
(3)                                ;/WOULD MAKE US 'HANG' HERE
(3) 032710 000774                BR      21$
(3)                                ;/RETURNS HERE-FROM-TIMED OUT.
(2) 032712 122777 000377 146724    CMPB   #377,@KMAD2 ;KMC CODE WILL RETURN A '377'

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(2) 032720 001370      BNE 21$      ;WHEN DONE COMMAND.
(2) 032722 000207      RTS      PC
(2) 032724 000000      $AERR: .WORD 0      ; 0 IF ADDR. LIST OK,-1 IF BAD.
(2)
(2)
(2)
(2)      :
(2)      : *THIS SUB CODE USED TO LOAD MICRO-CODE INTO LPA-11.
(2)      : * CALL = JSR R5,$LOAD
(2)      : * .WORD XX      ;ADDR. OF MICRO CODE.
(2)      : * .RETURNS HERE
(2)      : * NOTE: MICRO CODE FILE MUST END IN -1 DATA.
(2)
(2)
(2) 032726 010446      $LOAD: MOV R4,-(SP)      ;SAVE R4.
(2) 032730 010046      MOV R0,-(SP)      ;SAVE R0.
(2) 032732 012500      1$:  MOV (5)+,R0      ;GET PROG. ADDR.
(2) 032734 005077 146700      CLR @KMADO      ;CLEAR CSR
(2) 032740 005077 146704      CLR @KMAD4      ;CLEAR CRAM ADDR.
(2) 032744 052777 002000 146666 2$: BIS #2000,@KMADO      ;SELECT CRAM.
(2) 032752 012077 146676      MOV (0)+,@KMAD6      ;WRITE DATA.
(2) 032756 052777 020000 146654  BIS #20000,@KMADO      ;SET CRAM WRITE
(2) 032764 005077 146650      CLR @KMADO      ;DISABLE CRAM.
(2) 032770 005277 146654      INC @KMAD4      ;UPDATE CRAM ADDR.
(2) 032774 021027 177777      CMP (0),#-1      ;ALL DONE?
(2) 033000 001361      BNE 2$      ;NO LOOP.
(2) 033002 005077 146642      CLR @KMAD4      ;CLEAR CRAM ADDR.
(2) 033006 016500 177776      MOV -2(5),R0      ;GET MICRO CODE ADDR.
(2)
(2) 033012 052777 002000 146620 3$: BIS #2000,@KMADO      ;SELECT CRAM
(2) 033020 022077 146630      CMP (R0)+,@KMAD6      ;DATA OK?
(2) 033024 001013      BNE 5$      ;NO - REPORT AN ERROR.
(2) 033026 021027 177777      CMP (0),#-1      ;ALL DONE?
(2) 033032 001405      BEQ 4$      ;YES - EXIT
(2) 033034 005077 146600      CLR @KMADO      ;NO - DESELECT CRAM.
(2) 033040 005277 146604      INC @KMAD4      ;UPDATE CRAM ADDR.
(2) 033044 000762      BR 3$
(2)
(2) 033046 012600      4$: MOV (SP)+,R0      ;RESTORE R0
(2) 033050 012604      MOV (SP)+,R4      ;RESTORE R4
(2) 033052 000205      RTS      R5      ;EXIT
(2)
(2) 033054      5$:      ;COME HERE ON LOAD ERROR
(2) 033054 005745      TST -(5)
(2) 033056 105204      INCB R4      ;UPDATE ERROR COUNTER.
(2) 033060 100324      BPL 1$      ;IF NOT TOO MANY, TRY AGAIN.
(2) 033062 000000      HALT      ;MICRO CODE LOAD ERROR.
(2)
(2) 033064 000722      BR 1$      ;KMC-11 FAULT. YOU COULD TRY
(2)
(2)
(2)
(2)
(2)
(2)
(2)
(2)
(2)
(2)
(2)      :
(2)
(2)
(2)      : *THIS ROUTINE ISSUES A WRITE COMMAND TO THE LPA-11
(2)

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(3)
(2) 033250 032777 000040 146362      BIT      #BIT5,@KMAD0      ;/RETURNS HERE-FROM-TIMED OUT.
(2) 033256 001370                    BNE      1$              ;FAST PATH GOT DATA?
(2) 033260 112777 000004 146356      MOVB     #4,@KMAD2        ;ISSUE FAST PATH READ
(2) 033266 004737 033350              JSR      PC,$LPW
(2) 033272 117737 146352 033346      MOVB     @KMAD4,$DATR    ;GET LOW BYTE
(2) 033300                    2$:
(3) 033300 004537 033636              JSR      R5,$TOUT        ;-TOUT-CHECK FOR TIMEOUT
(3)
(3) 033304 104000                    ERROR                   ;/TIME-OUT ERROR
(3)                                     ;/WE FAILED TO COMPLETE
(3)                                     ;/CURRENT OPERATION.
(3)                                     ;/CONTINUES IN THIS LOOP
(3)                                     ;/WOULD MAKE US 'HANG' HERE
(3)
(3) 033306 000774                    BR          2$
(3)
(2) 033310 032777 000040 146322      BIT      #BIT5,@KMAD0      ;/RETURNS HERE-FROM-TIMED OUT.
(2) 033316 001370                    BNE      2$              ;FAST PATH READY?
(2) 033320 112777 000004 146316      MOVB     #4,@KMAD2        ;ISSUE FAST PATH READ
(2) 033326 004737 033350              JSR      PC,$LPW
(2) 033332 117737 146312 033347      MOVB     @KMAD4,$DATR+1  ;SAVE HIGH BYTE
(2) 033340 012600                    MOV      (SP)+,R0
(2) 033342 000205                    RTS      R5
(2) 033344 000000                    RD1: 0
(2) 033346 000000                    $DATR: .WORD 0
(2)
(2)                                     ;THIS ROUTINE WAITS FOR KMC-CODE TO BECOME READY AS WELL
(2)                                     ;AS FAST PATH TO BE READ.
(2)
(2)                                     ;CALL = JSR PC,$LPW
(2)
(2)                                     ;IT WILL TIME OUT IF TOO MUCH TIME IS TAKEN BY
(2)                                     ;THE MICRO-PROCESSORS AND REPORT AN ERROR, THEN HALT.
(2)
(2)
(2) 033350 010146                    $LPW: MOV      R1,-(SP)    ;SAVE R1
(2) 033352 005001                    CLR      R1
(2) 033354 122777 000377 146262 1$:  (MPB     #377,@KMAD2    ;FINISHED INSTRUCTION?
(2) 033362 001403                    BEQ      2$
(2) 033364 005201                    INC      R1              ;TIME OUT?
(2) 033366 001372                    BNE      1$
(2) 033370 000411                    BR       10$
(2)
(2) 033372 032777 000020 146240 2$:  BIT      #BIT4,@KMAD0    ;FAST PATH READ?
(2) 033400 001403                    BEQ      3$
(2) 033402 005201                    INC      R1              ;NO - TIME OUT?
(2) 033404 001372                    BNE      2$
(2) 033406 000402                    BR       10$            ;YES - REPORT AN ERROR
(2)
(2) 033410 012601                    3$:  MOV      (SP)+,R1    ;RESTORE R1
(2) 033412 000207                    RTS      PC             ;EXIT
(2)
(2) 033414
(3) 033414 104401 033422 10$:      TYPE     ,65$          ;:TYPE ASCIZ STRING

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(3) 033420 000407 BR 64$ ;:GET OVER THE ASCIZ
(3) ;:65$: .ASCIZ <200>#LPA-11 FAULT#
(3) 033440 64$:
(2)
(2) 033440 000000 11$: HALT ;LPA-11 FAULT RUN LPA-11
(2) 033442 000776 BR 11$ ;DIAGNOSTICS.
(2)
(2)
(2)
(2) ;*
(2) ;*THIS ROUTINE PROVIDES THE LINKAGE FROM USER CODE TO
(2) ;*A DEVICE ADDRESS ON THE I/O BUSS FOR WRITE ONLY.
(2) ;*
(2) ;* FIRST WE WILL DETERMINE IF THE ADDRESS HAS BEEN USED
(2) ;* BEFORE. IF NOT WE HAVE TO INITIALIZE THE LPA WITH
(2) ;* THAT ADDRESS.
(2) ;* WHEN THE ADDR. IS KNOWN BY THE LPA, DO THE OUTPUT BY
(2) ;* $TLKW
(2) ;*
(2) 033444 010046 $OUTLP: MOV R0,-(SP) ;SAVE R0
(2) 033446 010146 MOV R1,-(SP) ;SAVE R1
(2)
(2) 033450 012700 001666 MOV #.DVLS,R0 ;PROGRAM DEFINED LIST.
(2) 033454 005001 CLR R1
(2) 033456 005710 1$: TST (0) ;TERMINATOR REACHED?
(2) 033460 001421 BEQ 10$ ;YES NEXT STEP.
(2) 033462 027520 000000 CMP @ (5), (0)+ ;MATCH WITH ADDR IN LIST?
(2) 033466 001402 BEQ 2$
(2) 033470 005201 INC R1
(2) 033472 000771 BR 1$
(2)
(2) 033474 010137 033512 2$: MOV R1,3$ ;SAVE OFFSET, DEVICE KNOWN.
(2) 033500 005725 TST (5)+
(2) 033502 013537 033514 MOV @ (5)+,4$ ;GET DATA TO BE WRITTEN
(2) 033506 004537 033066 JSR R5,$TLKW ;DO WRITE
(2) 033512 000000 3$: .WORD 0 ;DEVICE OFFSET
(2) 033514 000000 4$: .WORD 0 ;DATA TO BE WRITTEN.
(2) 033516 012601 MOV (SP)+,R1
(2) 033520 012600 MOV (SP)+,R0
(2) 033522 000205 RTS R5
(2) 033524 017520 000000 10$: MOV @ (5), (0)+ ;SAVE ADDR.
(2) 033530 005010 CLR (0)
(2) 033532 004537 032046 JSR R5,$LPAI
(2) 033536 001666 .WORD .DVLS
(2) 033540 000755 BR 2$
(2)
(2) ;*
(2) ;*THIS ROUTINE PROVIDES THE LINKAGE FROM USER CODE
(2) ;*TO A DEVICE ADDR. ON THE I/O BUSS FOR READ ONLY.
(2) ;*
(2) ;*FIRST WE WILL DETERMINE IF THE ADDRESS HAS BEEN
(2) ;*USED BEFORE. IF NOT, WE HAVE TO INITIALIZE THE LPA
(2) ;*WITH THE NEW ADDR.
(2) ;*WHEN THE ADDR IS KNOWN WE CAN DO OUTPUT THROUGH
(2) ;*$TLKR
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(2)          : *      CALL THROUGH      MOVEI  DATA,ADDR.
(2)          : *      WHICH EQUALS:
(2)          : *      JSR      R5,$INLP
(2)          : *      .WORD  XX      ADDR OF DEVICE
(2)          : *      .WORD  YY      ADDR TO STORE READ DATA.
(2)
(2) 033542 010046      $INLP: MOV      R0,-(SP)      ;SAVE R0
(2) 033544 010146      MOV      R1,-(SP)      ;SAVE R1
(2)
(2) 033546 012700 001666      MOV      #.DVLS,R0      ;PROG DEFINED ADDR. LIST.
(2) 033552 005001      CLR      R1
(2) 033554 005710      1$:   TST      (0)      ;EOL REACHED?
(2) 033556 001420      BEQ      10$          ;YES - DEFINE NEW ADDR.
(2)
(2) 033560 027520 000000      CMP      @ (5), (0)+   ;ADDR. MATCH?
(2) 033564 001402      BEQ      2$
(2) 033566 005201      INC      R1
(2) 033570 000771      BR       1$
(2)
(2) 033572 010137 033604      2$:   MOV      R1,3$      ;SAVE LIST OFFSET
(2) 033576 005725      TST      (5)+
(2) 033600 004537 033202      JSR      R5,$TLKR      ;GO READ DEVICE
(2)
(2) 033604 000000      $OFS=.
(2) 033604 000000      3$:   .WORD  0          ;OFFSET OF DEVICE
(2)
(2) 033606 013735 033346      MOV      $DATR,@ (5)+  ;STORE DATA.
(2) 033612 012601      MOV      (SP)+,R1      ;RESTORE R1
(2) 033614 012600      MOV      (SP)+,R0      ;RESTORE R2
(2) 033616 000205      RTS      R5            ;EXIT
(2)
(2) 033620 017520 000000      10$:  MOV      @ (5), (0)+
(2) 033624 005010      CLR      (0)
(2) 033626 004537 032046      JSR      R5,$LPAI
(2) 033632 001666      .WORD  .DVLS
(2) 033634 000756      BR       2$
(2)
(2)          : *
(2)          : * $STOUT ROUTINE USED TO WATCH IF
(2)          : * WE'RE IN A LOOP TOO-LONG
(2)          : * CALL= JSR R5, $STOUT
(2)          : * ERROR X ;RETURNS HERE ON TIMEOUT
(2)          : * BR
(2)          : * ;RETURNS HERE NO ERROR
(2)          : *
(2)
(2) 033636 020537 033672      $STOUT: CMP      R5,$SAD      ;SAME ADDR?
(2) 033642 001405      BEQ      1$
(2) 033644 010537 033672      MOV      R5,$SAD      ;NO-SAVE THIS ADDR.
(2) 033650 005037 033674      CLR      $CNT          ;CLR CNT AT ADDR.
(2) 033654 000403      BR       2$
(2) 033656 005237 033674      1$:   INC      $CNT          ;OVERFLOW?
(2) 033662 100402      BMI      3$          ;YES-ERROR RETURN
(2) 033664 062705 000004      2$:   ADD      #4,R5      ;NO-NON ERROR RETURN
(2) 033670 000205      3$:   RTS      R5          ;RETURN.
(2)
(2) 033672 000000      $SAD:  .WORD  0          ;CONTAINS LOOP ADDR.
(2) 033674 000000      $CNT:  .WORD  0          ;# OF TIMES AT ADDR.

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Address	Label	Value	Code	Comments
(2) 034010	005337	034006	CLKINT: DEC TIME	
(2) 034014	000002		RTI	
(2) 034016	000000		RTCCSR: .WORD 0	;CLOCK CSR IF USED.
(2)				
(2)				
(2)				
(2)				
(2)				
(2)				
(2)				
(2)				
(2)				
(2)				
(2)				
(2)				
(2) 034020			\$UTK:	
(2) 034020	005037	001666	CLR .DVLS	
(2) 034024			21\$:	
(3) 034024	104401	034032	TYPE .65\$	::TYPE ASCIZ STRING
(3) 034030	000405		BR .64\$	::GET OVER THE ASCIZ
(3)			::65\$: .ASCIZ <200>#E OR D?#	
(3) 034044			64\$:	
(2) 034044	105777	145074	1\$: TSTB @STKS	
(2) 034050	100375		BFL 1\$	
(2) 034052	117737	145070 034174	MOVB @STKB,20\$	;GET INPUT
(2) 034060	104401	034174	TYPE, 20\$	;ECHO, NEXT MESSAGE.
(2) 034064	142737	000240 034174	BICB #240,20\$	;STRIP PARITY, LC
(2) 034072	104412		RDOCT	;GET ADDR.
(2) 034074	012637	034172	MOV (SP)+,14\$	
(2) 034100	123727	034174 000104	CMPB 20\$,#D	;DEPOSIT?
(2) 034106	001411		BEQ 10\$	
(2)				
(2) 034110	004537	033542	JSR R5,\$INLP	;GET DATA
(2) 034114	034172		2\$: .WORD 14\$	
(2) 034116	034130		.WORD 5\$	
(2)				
(3) 034120	013746	034130	MOV 5\$,-(SP)	::SAVE 5\$ FOR TYPEOUT
(3) 034124	104402		TYPOC	::GO TYPE--OCTAL ASCII(ALL DIGITS)
(2) 034126	000736		BR 21\$	;LOOP.
(2) 034130	000000		5\$: .WORD 0	
(2)				
(2) 034132			10\$:	
(3) 034132	104401	034140	TYPE .67\$	::TYPE ASCIZ STRING
(3) 034136	000404		BR .66\$	::GET OVER THE ASCIZ
(3)			::67\$: .ASCIZ <200>#DATA= #	
(3) 034150			66\$:	
(2) 034150	104412		RDOCT	
(2) 034152	012637	034170	MOV (SP)+,13\$	
(2)				
(2) 034156	004537	033444	11\$: JSR R5,\$OUTLP	;OUTPUT ROUTINE.
(2) 034162	034172		12\$: .WORD 14\$	;DEVICE ADDR.
(2) 034164	034170		.WORD 13\$	;DATA
(2) 034166	000716		BR 21\$	
(2)				
(2) 034170	000000		13\$: .WORD 0	
(2) 034172	000000		14\$: .WORD 0	
(2) 034174	100001	042504 044526	20\$: .ASCIZ <1><200>#DEVICE ADDR= #	





ABASE = 170404	2995#	3061												
ABR 001330	3061#	3246*	3302	3332	3333	3360	3361	3562	3581	3609	3637	3824	3876	
	3934	3986	4065	4066	4067	4068	4069	4070	4088	4134	4140	4175	4215	
	4332	4333	4377	4378	4402	4456	4469	4519	4868	4932	5042	5043	5044	
	5045	5304	5399	5568										
ACDW1 = 000000	3061													
ACDW2 = 000000	3061													
ACPUOP = 000000	3061													
ACR 001332	3061#	3248*	3302	3585	3610	3638	3836	3893	4003	4065	4066	4067	4068	
	4069	4070	4096	4144	4221	4377	4378	4406	4483	4526	4771	4880	4939	
	5042	5043	5044	5045	5311	5569	5576	5577						
ADDW0 = 000000	3061													
ADDW1 = 000000	3061													
ADDW10 = 000000	3061													
ADDW11 = 000000	3061													
ADDW12 = 000000	3061													
ADDW13 = 000000	3061													
ADDW14 = 000000	3061													
ADDW15 = 000000	3061													
ADDW2 = 000000	3061													
ADDW3 = 000000	3061													
ADDW4 = 000000	3061													
ADDW5 = 000000	3061													
ADDW6 = 000000	3061													
ADDW7 = 000000	3061													
ADDW8 = 000000	3061													
ADDW9 = 000000	3061													
ADEVCT = 000000	3061													
ADEVN = 000000	3061													
AENV = 000000	3061													
AENVN = 000000	3061													
AFATAL = 000000	3061													
AMADR1 = 000000	3061													
AMADR2 = 000000	3061													
AMADR3 = 000000	3061													
AMADR4 = 000000	3061													
AMAMS1 = 000000	3061													
AMAMS2 = 000000	3061													
AMAMS3 = 000000	3061													
AMAMS4 = 000000	3061													
AMSGAD = 000000	3061													
AMSGLG = 000000	3061													
AMSGTY = 000000	3061													
AMTYP1 = 000000	3061													
AMTYP2 = 000000	3061													
AMTYP3 = 000000	3061													
AMTYP4 = 000000	3061													
APASS = 000000	3061													
APRIOR = 000006	2997#	3061												
APRITY 001352	3061#	3264												
APTC SU = 000040	5528	5529#												
APTENV = 000001	5522	5528	5529#											
APTSIZ = 000200	3228	5529#												
APTSPO = 000100	5528	5529#												
ASR 001326	3061#	3234*	3244	3302	3393	3394	3404	3562	3580	3604	3628	3755	3756	
	3760	3763	3788	3789	3791	3792	3804	3823	3830	3831	3833	3875	3883	









TST120	015370	4435#
TST121	015606	4508#
TST122	015762	4560#
TST123	016112	4611#
TST124	016326	4677#
TST125	016516	4727#
TST126	016620	4752#
TST127	016726	4832#
TST13	003532	3562#
TST130	017054	4833#
TST131	017202	4834#
TST132	017330	4835#
TST133	017456	4836#
TST134	017604	4837#
TST135	017732	4848#
TST136	020124	4920#
TST137	020236	5042#
TST14	003640	3562#
TST140	020534	5043#
TST141	021032	5044#
TST142	021330	5045#
TST143	021626	5146#
TST144	022140	5147#
TST145	022452	5148#
TST146	022764	5149#
TST15	003746	3562#
TST16	004054	3562#
TST17	004162	3562#
TST2	002572	3326#
TST20	004270	3562#
TST21	004376	3562#
TST22	004504	3562#
TST23	004612	3562#
TST24	004720	3562#
TST25	005026	3562#
TST26	005134	3562#
TST27	005242	3562#
TST3	002640	3355#
TST30	005350	3562#
TST31	005456	3562#
TST32	005564	3562#
TST33	005672	3562#
TST34	006000	3562#
TST35	006106	3562#
TST36	006214	3562#
TST37	006322	3562#
TST4	002704	3388#
TST40	006430	3562#
TST41	006536	3562#
TST42	006644	3562#
TST43	006752	3562#
TST44	007060	3562#
TST45	007166	3562#
TST46	007274	3562#
TST47	007402	3562#
TST5	002766	3414#















ADTST	3277#	3302														
AREPT	5047#															
BREPT	5151#															
BRTM	4781#	4832	4833	4834	4835	4836	4837									
CADT	4953#	5042	5043	5044	5045											
CADTB	5072#	5146	5147	5148	5149											
CBC	3562#															
CBTC	4342#	4377	4378													
CBT25	4278#	4332	4333													
COMMEN	2993#	3338	3341	3365	3368	3397	3401	3424	3428	3449	3453	3562	3589	3593	3616	
	3621	3644	3649	3674	3678	3702	3707	3730	3735	3767	3771	3796	3801	3840	3847	
	3898	3902	3947	3950	3958	3963	3997	4000	4007	4015	4065	4066	4067	4068	4069	
	4070	4105	4110	4147	4151	4184	4187	4224	4236	4273	4275	4332	4333	4377	4378	
	4409	4412	4472	4479	4488	4494	4532	4535	4581	4594	4649	4653	4703	4706	4713	
	4716	4746	4749	4774	4778	4832	4833	4834	4835	4836	4837	4884	4895	4943	4949	
	5042	5043	5044	5045	5146	5147	5148	5149	5260	5264	5315	5318	5367	5370	5419	
	5423	5474	5478	5508	5514											
CSRDTA	3464#	3562														
DFC	3062#	3072	3079	3086	3093	3100	3107	3114	3122	3129	3136	3150	3157	3164	3178	
	3185	3192	3199	3206	3213	3220										
ECALL	3501#	3562														
ECB	3034#	3338	3341	3365	3368	3397	3401	3424	3428	3449	3453	3562	3589	3593	3616	
	3621	3644	3649	3674	3678	3702	3707	3730	3735	3767	3771	3796	3801	3840	3847	
	3898	3902	3947	3950	3958	3963	3997	4000	4007	4015	4065	4066	4067	4068	4069	
	4070	4105	4110	4147	4151	4184	4187	4224	4236	4273	4275	4332	4333	4377	4378	
	4409	4412	4472	4479	4488	4494	4532	4535	4581	4594	4649	4653	4703	4706	4713	
	4716	4746	4749	4774	4778	4832	4833	4834	4835	4836	4837	4884	4895	4943	4949	
	5042	5043	5044	5045	5146	5147	5148	5149	5260	5264	5315	5318	5367	5370	5419	
	5423	5474	5478	5508	5514											
ENDCOM	2993#	3338	3341	3365	3368	3397	3401	3424	3428	3449	3453	3562	3589	3593	3616	
	3621	3644	3649	3674	3678	3702	3707	3730	3735	3767	3771	3796	3801	3840	3847	
	3898	3902	3947	3950	3958	3963	3997	4000	4007	4015	4065	4066	4067	4068	4069	
	4070	4105	4110	4147	4151	4184	4187	4224	4236	4273	4275	4332	4333	4377	4378	
	4409	4412	4472	4479	4488	4494	4532	4535	4581	4594	4649	4653	4703	4706	4713	
	4716	4746	4749	4774	4778	4832	4833	4834	4835	4836	4837	4884	4895	4943	4949	
	5042	5043	5044	5045	5146	5147	5148	5149	5260	5264	5315	5318	5367	5370	5419	
	5423	5474	5478	5485	5508	5514										
ERROR	2993#	3339	3366	3398	3425	3450	3562	3590	3617	3645	3675	3703	3731	3768	3797	
	3841	3899	3948	3959	3998	4008	4065	4066	4067	4068	4069	4070	4106	4148	4185	
	4225	4274	4332	4333	4377	4378	4410	4473	4489	4533	4582	4650	4704	4714	4747	
	4775	4832	4833	4834	4835	4836	4837	4885	4945	5042	5043	5044	5045	5146	5147	
	5148	5149	5262	5316	5368	5420	5475	5585								
ESCAPE	2993#															
GETPRI	2993#															
GETSWR	2993#															
MOVEI	170#	3302	3333	3361	3394	3420	3445	3562	3585	3610	3638	3670	3696	3724	3756	
	3763	3789	3792	3831	3836	3886	3893	3939	3944	3954	3989	3994	4003	4065	4066	
	4067	4068	4069	4070	4096	4100	4130	4144	4178	4181	4218	4221	4254	4266	4270	
	4332	4333	4377	4378	4403	4406	4461	4469	4483	4526	4529	4572	4575	4578	4639	
	4645	4697	4700	4709	4742	4771	4832	4833	4834	4835	4836	4837	4877	4880	4933	
	4939	5042	5043	5044	5045	5146	5147	5148	5149	5256	5307	5311	5351	5364	5406	
	5416	5461	5471	5585												
MOVEM	157#	3332	3360	3393	3404	3419	3444	3562	3580	3581	3604	3609	3628	3637	3665	
	3666	3686	3693	3714	3721	3755	3760	3788	3791	3804	3823	3824	3830	3833	3875	
	3876	3883	3888	3932	3934	3938	3941	3978	3986	3988	3991	4065	4066	4067	4068	
	4069	4070	4087	4088	4090	4133	4134	4136	4140	4173	4175	4177	4180	4213	4215	







.TRMTR	2929#	
.UTK	698#	5585
.SACT1	2932#	3057
.SAPT8	2932#	3061#
.SAPTH	2932#	3059
.SAPTY	2932#	5529
.SCATC	2930#	2982
.SCMTA	2930#	3061
.SEOP	2931#	5179
.SERRO	2931#	5522
.SERRT	2931#	5523
.SINLP	651#	5585
.SMMAC	141#	
.SOUTL	609#	5585
.SPOWE	2930#	5530
.SRDOC	2929#	2932# 5526
.SREAD	2931#	5527
.SSCOP	2931#	5525
.STLKW	510#	5585
.S-OUT	3223#	5585
.STRAP	2929#	5531
.STYPD	2931#	5524
.STYPE	2931#	5528
.STYPC	2930#	5521

. ABS.	034324	000	OVR	RO	ABS	GBL	D
	000000	001	CON	RW	REL	LCL	I

ERRORS DETECTED: 0  
 DEFAULT GLOBALS GENERATED: 0

CRLPGB,CRLPGB/CRF-DRIPA.MAC,CRLPGB  
 RUN-TIME: 53 47 2 SECONDS  
 RUN-TIME RATIO: 404/103=3.9  
 CORE USED: 46K (91 PAGES)