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LP20 LINE PRINTER SYSTEM MANUAL

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual covers the description, installation, operation, programming, theory, and maintenance of the LP20 Line Printer System. Reference is made, where applicable, to detailed information in other supporting technical documentation. A prerequisite is a basic understanding of PDP-11 processors and peripherals, with emphasis on Unibus operation.

The LP20 Line Printer System is a hard-copy printer system designed to interface with the PDP-11 Unibus. Each printer system comprises a self-contained, free-standing line printer and a separate, solid-state controller (LP20 Controller). The controller consists of three logic modules, a wired back-plane assembly, and associated cabling.

Design of the LP20 Line Printer System provides for large amounts of formatted or unformatted text to be printed with minimum software intervention. This is accomplished by transferring characters under direct memory access (DMA) control and by using a random access memory (RAM) in the LP20 Controller to control actions taken on individual characters. Thus, software need only handle errors and situations that cannot be handled by data stored in the RAM.

Several types of line printers are supported by the LP20 Controller; the line printers are plug-for-plug compatible and use identical cabling.

Table 1-1 summarizes the basic characteristics of LP20 Line Printer Systems.

Table 1-1 Basic Characteristics of LP20 Line Printer Systems

Printer System Model	Print Rate	Character Set	Font	Power	Printer
LP20-AA	300 lpm	64	EDP	120 Vac, 60 Hz	LP05-VK
LP20-AB	300 lpm	64	EDP	240 Vac, 50 Hz	LP05-VN
LP20-AC	300 lpm	64	SCI	120 Vac, 60 Hz	LP05-VP
LP20-AD	300 lpm	64	SCI	240 Vac, 50 Hz	LP05-VT
LP20-BA	230 lpm	96	EDP	120 Vac, 60 Hz	LP05-WK
LP20-BB	230 lpm	96	EDP	240 Vac, 50 Hz	LP05-WN
LP20-BC	230 lpm	96	SCI	120 Vac, 60 Hz	LP05-WP
LP20-BD	230 lpm	96	SCI	240 Vac, 50 Hz	LP05-WT
LP20-CA	890 lpm	64	EDP	120 Vac, 60 Hz	LP14-VK
LP20-CB	890 lpm	64	EDP	240 Vac, 50 Hz	LP14-VN
LP20-CC	890 lpm	64	SCI	120 Vac, 60 Hz	LP14-VP
LP20-CD	890 lpm	64	SCI	240 Vac, 50 Hz	LP14-VT
LP20-DA	650 lpm	96	EDP	120 Vac, 60 Hz	LP14-WK
LP20-DB	650 lpm	96	EDP	240 Vac, 50 Hz	LP14-WN
LP20-DC	650 lpm	96	SCI	120 Vac, 60 Hz	LP14-WP
LP20-DD	650 lpm	96	SCI	240 Vac, 50 Hz	LP14-WT
LP20-FA	1250 lpm	64	EDP	120 Vac, 60 Hz	LP10-JA
LP20-FB	1250 lpm	64	EDP	240 Vac, 50 Hz	LP10-JB
LP20-FC	1250 lpm	64	SCI	120 Vac, 60 Hz	LP10-JC
LP20-FD	1250 lpm	64	SCI	240 Vac, 50 Hz	LP10-JD
LP20-HA	925 lpm	96	EDP	120 Vac, 60 Hz	LP10-KA
LP20-HB	925 lpm	96	EDP	240 Vac, 50 Hz	LP10-KB
LP20-HC	925 lpm	96	SCI	120 Vac, 60 Hz	LP10-KC
LP20-HD	925 lpm	96	SCI	240 Vac, 50 Hz	LP10-KD
LP200-BA	1220 lpm	64	*	220 Vac, 60 Hz	LP07-BA
LP200-BB	905 lpm	96	*	220 Vac, 50 Hz	LP07-BB

*See Table 7-7.

1.2 SPECIFICATIONS

The LP20 Controller is common to all LP20 Line Printer Systems. Performance specifications of the controller are listed in Table 1-2.

Table 1-2 LP20 Line Printer Controller Specifications

Registers	Total of eight registers: Control and Status Register A (CSRA) Control and Status Register B (CSRB) Bus Address Byte Counter Page Counter RAM Data Character Buffer/Column Counter Checksum/LPT Data
Character Dependent Operations	Controlled by internal 256-word RAM which is addressed by the incoming character.
Hardware Defined Functions	Horizontal tab every eight spaces. Line feed on line overflow after 132 columns are printed.
Parity	Memory parity RAM parity Line printer parity (may be disabled)
Character Transfer Mode	PDP-11 Unibus, Direct Memory Access (DMA) transfers.
Checksum	Non-rotated sum of bytes addressed by the bus address register. High-order carries are ignored. Checksum is set to zero each time DMA transfers are started.
Printer Interface Format	Parallel; single character via an ASCII interface. The interface permits the transfer of data at a maximum rate of 5×10^5 characters per second. All signals are differentially driven lines carrying complementary TTL logic levels.
Power Requirements	4.5 A nominal @ 5 Vdc ± 5% (derived from power supply in cabinet where controller is installed).
Cables	One BC06R-10 Input/Output Cable Assembly, supplied with system. One BC11A-02 Unibus Cable Assembly, supplied with system. One 7009563 Power Harness, supplied with system.
Software	PDP-11 compatible. One LP20 Controller supports only one printer.
Physical Characteristics	Overall dimensions of wired assembly and modules are approximately 41.59 cm (16-3/8 in) high by 6.35 cm (2-3/4 in) wide by 25.4 cm (10 in) deep.

1.3 FUNCTIONAL DESCRIPTION

A simplified functional block diagram of an LP20 Line Printer System is shown in Figure 1-1. The controller comprises all the functional elements that interface between the Unibus and the line printer. Primary functions of the controller are to:

1. Indicate to the system the operational status of the printer.
2. Control the transfer of data characters and commands between the system and the printer (via DMA).
3. Perform code conversion and other character code dependent operations as required.
4. Provide hardware horizontal tab (every 8 spaces) and hardware line overflow (activated on the 133rd printable character in the current line).
5. Flag errors and special character conditions to the processor (via bus interrupts).

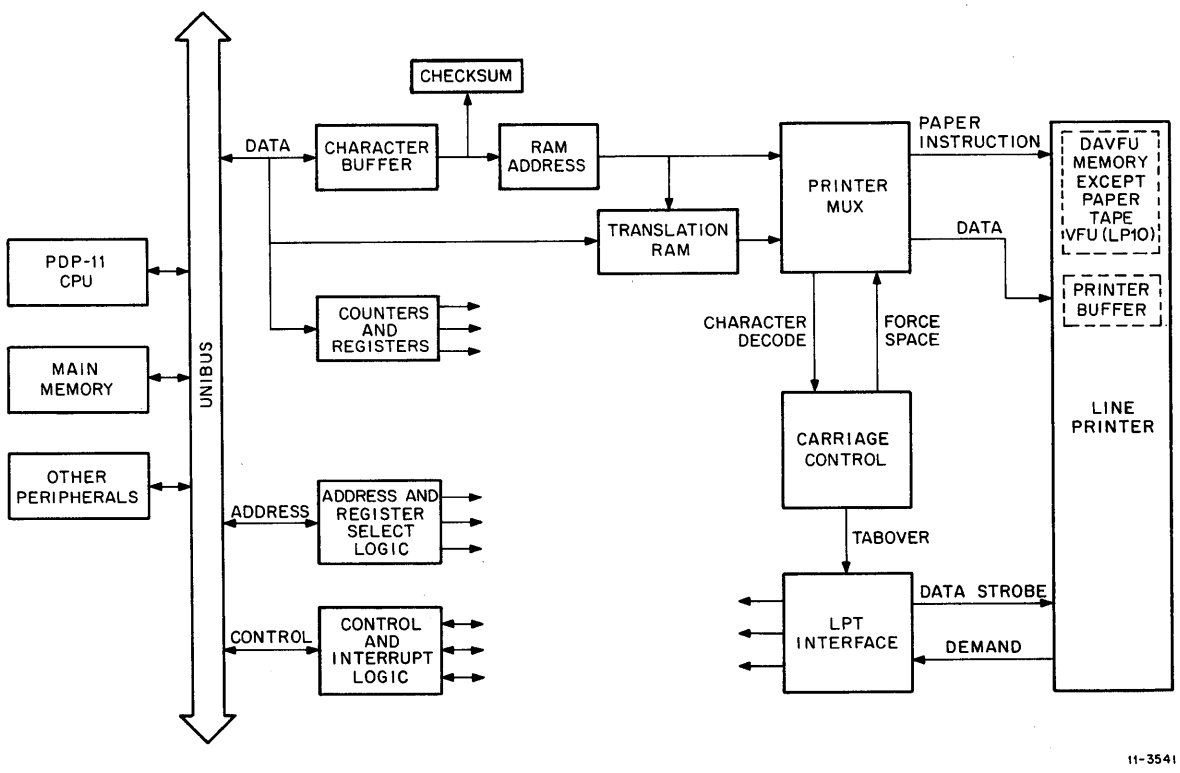


Figure 1-1 LP20 Line Printer System
Simplified Functional Block Diagram

The LP20 Controller has four major operating modes: RAM load, DAVFU load, print, and test. RAM load and DAVFU load modes are used to load the contents of the RAM and DAVFU, respectively, from main memory. The DAVFU load mode is not used when the printer is an LP10-J or LP10-K model. Print mode uses the contents of the RAM to control operation of the controller and is the mode that actually prints data on the line printer. Test mode acts exactly like print mode, except that the operation of the physical output device is simulated by the controller and no data is sent to the physical line printer. This mode is used for diagnostic purposes. The LP10-J, -K VFU is not loaded by the controller as it is a paper tape VFU.

Code conversion and character code dependent operations are controlled by a 256- × 13-bit random access memory (RAM), which is loaded by the user. The 13-bit word stored at each RAM address contains one parity bit, four control bits (paper instruction, translation, delimiter, and interrupt), and eight data bits. Up to 256 such words can be stored in the RAM. Each RAM location is uniquely addressed by an 8-bit code. Hence, each character (in a character set as large as 256 characters) addresses a unique RAM location. This feature enables controller functions to be triggered on a character-specific basis.

The RAM is loaded via DMA by placing the controller in the RAM load mode. It may be loaded location-by-location under program control in RAM load mode, print mode, or test mode by depositing the RAM address into the character buffer (07:00) and then depositing the RAM data into the RAM data register (11:00).

The DAVFU is a programmable, solid-state replacement for the conventional tape reader (except LP10-J, K). It has 12 separate channels for user-definable vertical format control and can also slew paper from 0 to 15 lines on command. The DAVFU is loaded by the user under DMA only by operating the controller in the DAVFU load mode. Two of the DAVFU channels are reserved for specific functions: channel 1 (top-of-form) and channel 12 (bottom-of-form). These channels must always be loaded appropriately.

The print mode is entered after the RAM and DAVFU (or paper tape) have been loaded. In this mode, the controller reads a word from main memory and loads one byte of the word into the character buffer. The byte loaded is controlled by bit 00 of the bus address register. The controller uses this byte as an address for the RAM and decides, on the basis of the data in the addressed RAM location and various control bits, what to do with the character. Depending on the states of the four control bits in the RAM, the character may be converted (translated) to another character, converted to a paper motion command (translated to a paper instruction), flagged to the software as being an "undefined" character, or recognized as a delimiter character.

If the translation bit is set in the currently addressed RAM location, the character stored in the RAM data bits at that location is used as the current character rather than the contents of the character buffer.

If the paper instruction bit is also set, the controller asserts the paper instruction line, which causes the printer to interpret the character stored in the RAM as a carriage control character (vertical formatting instruction to the DAVFU) rather than as data to be printed.

Characters are transferred one at a time from main memory to the printer buffer in the line printer until a print command (carriage control character) is received. Printing is accomplished by first scanning the stored characters in synchronization with the rotating drum characters and then actuating the appropriate hammer as the desired characters move into the printing position.

The interrupt bit being set in the current RAM location causes the controller to interrupt the processor upon receipt of an illegal or undefined character (predetermined before loading of the RAM). The processor may then examine the illegal or undefined character, decide how to handle the situation, and continue printing.

The RAM can also be used to recognize a delimiter character (predetermined before loading the RAM). The controller will convert the delimiter character as well as the next following character to another code (defined by the contents of the RAM) to be sent to the printer. The delimiter feature is normally used to allow a dual definition of a single character, depending on whether or not the character follows an arbitrary but uniquely defined delimiter character. The dual-function character usually will have both a print and a paper motion definition. In this way, FORTRAN carriage control characters (which are also normal print characters that appear as the first rather than the last character in a line) can be handled directly by the controller hardware, rather than by software. Any 1-level escape sequence may be handled in this manner.

The controller has hardware-defined horizontal tab and automatic line-feed-on-line-overflow features. Upon receipt of a tab character, the printer will move to the next column in the sequence 9, 17, 25 . . . 8N + 1. If a line contains more than 132 (decimal) printing characters, the controller will print 132 characters and send a line feed (LF) (ASCII 012_8). The 133rd character will be printed as the first character of the next line. If the printer tries to tab beyond column 128, the line will be printed and the carriage will move to column 9 on the next line (column 1 being the first column).

The LP20 Controller, being a direct memory access (DMA) device, does not allow line printer data to be transferred under program control. Instead, the controller initiates DMA bus cycles to control the flow of data (on a character-by-character basis) to the printer. DMA bus cycles continue until all characters in the current line are stored in the printer buffer. A line is normally terminated by a carriage control character which may be an ASCII carriage return (CR), line feed (LF), form feed (FF), or any of 28 special carriage control commands to the DAVFU. Horizontal tab (HT) is converted into one to eight space characters, depending on the column count stored in the column counter at the time HT is decoded. Lines creating a line overflow condition are always terminated after 132 characters have been sent to the line printer by LF, which is forced onto the printer data lines by the controller hardware.

Communication between the LP20 Controller and the rest of the system is handled by standard PDP-11 control and interrupt logic. Transfer of status information between the LP20 Controller and the processor is accomplished by means of a data multiplexer in the controller through which the processor may examine the contents of any of the eight registers in the controller.

To maintain data integrity, RAM parity checking and generating logic is provided, as well as data transfer checksum computation.

Line printer parity is generated by the controller and is sent to the printer for checking. This feature can be disabled by a hardware jumper if the printer used does not check parity.

1.4 PHYSICAL DESCRIPTION

Figure 1-2 illustrates the basic assemblies that comprise the LP20 Controller. The three printed circuit boards (modules) are equipped with TTL integrated circuits. The modules are:

M8585 LP20 Translation RAM Module (LPR)
M8586 LP20 Line Printer Control Module (LPC)
M8587 LP20 Line Printer Data Paths Module (LPD)
or
M8571 LP20 Line Printer Data Paths Module

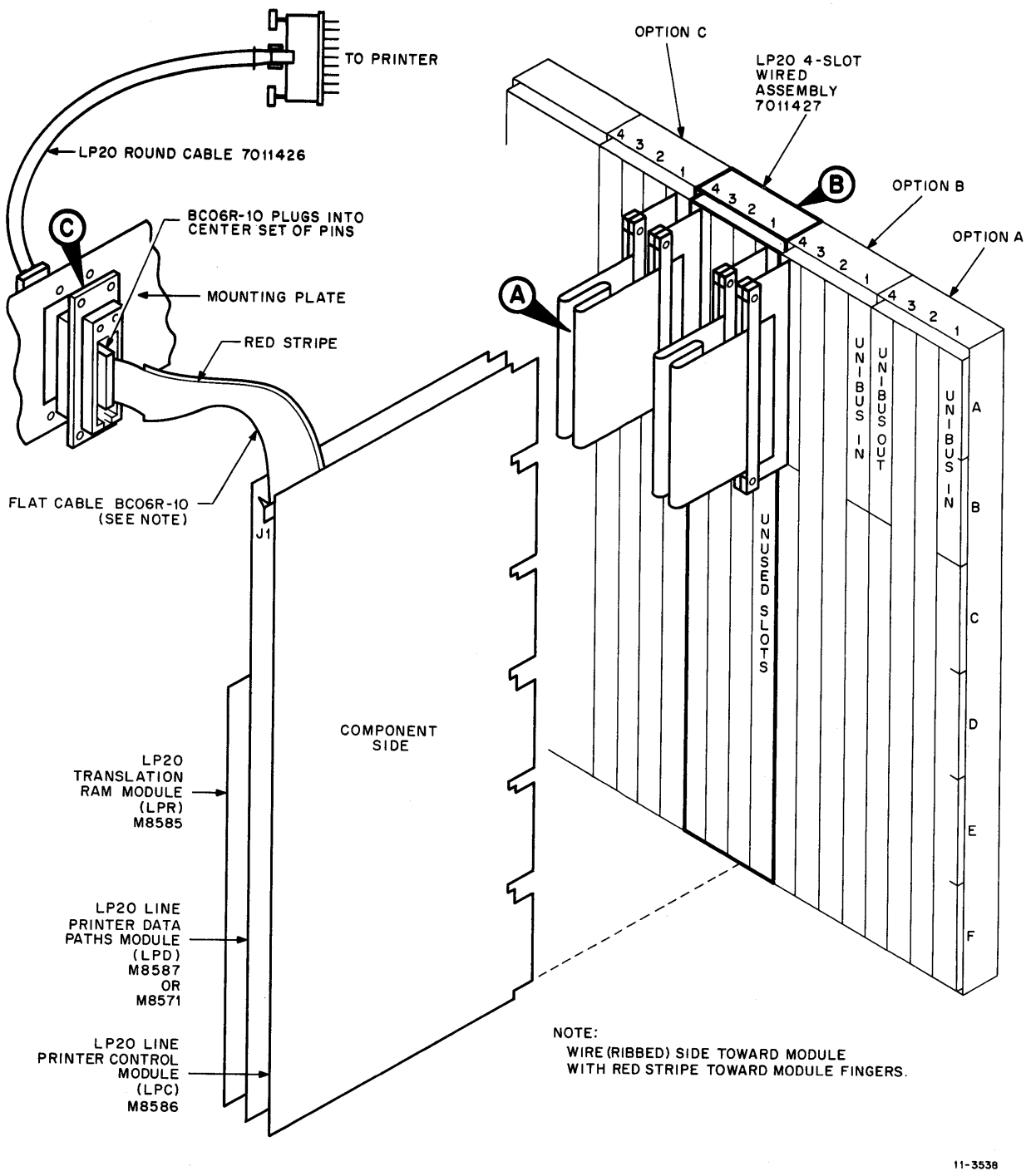


Figure 1-2 Typical LP20 Controller Assembly Mounting (Sheet 1 of 2)

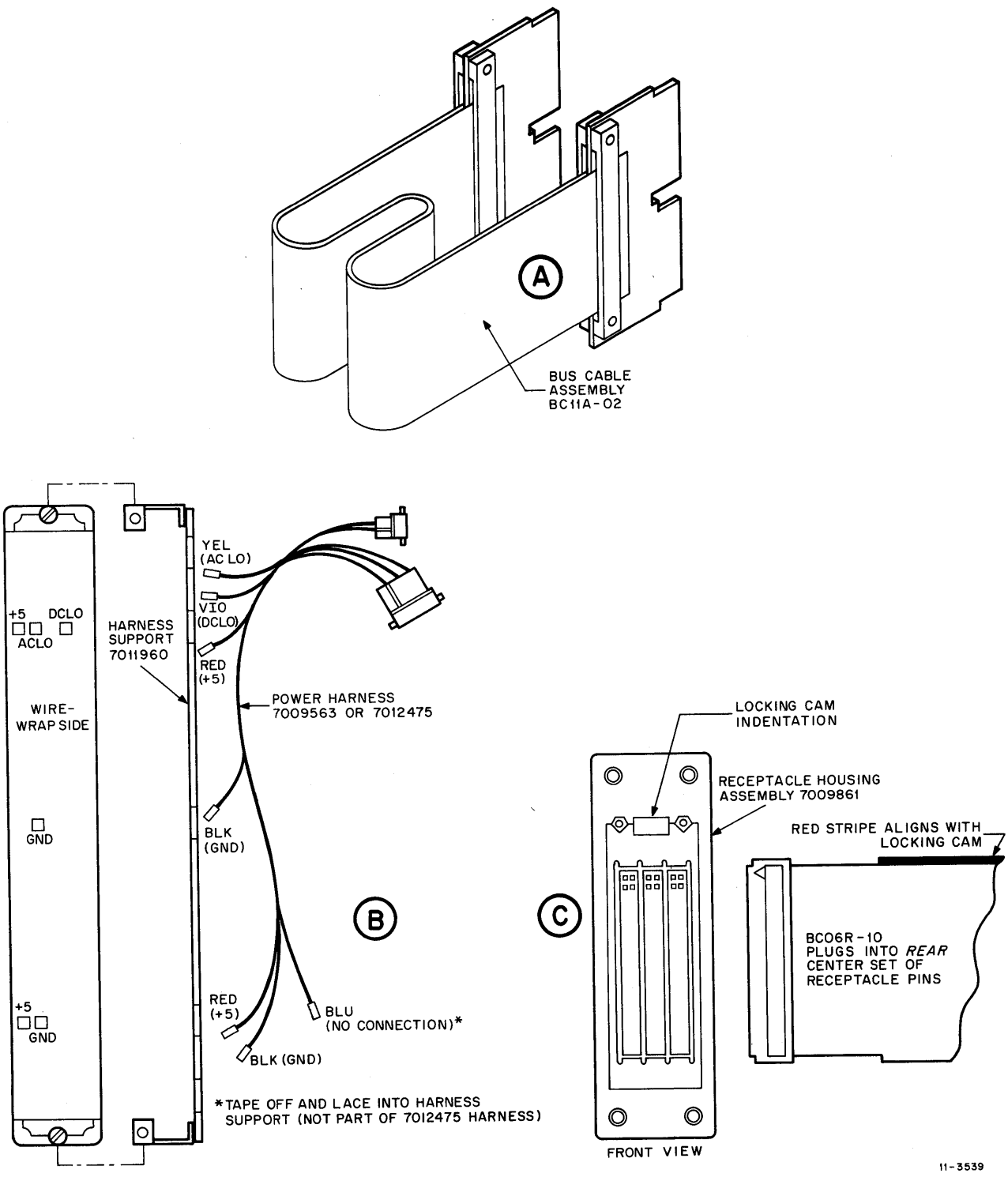


Figure 1-2 Typical LP20 Controller Assembly Mounting (Sheet 2 of 2)

M8586, M8587, and M8571 are hex-height modules and occupy slots A02-F02 and A03-F03 in the 4-slot LP20 wired assembly. The M8585 is a quad-height module and occupies slots C04-F04. BC11A-02 Unibus Cable Assemblies are used for interconnection to other system units. One BC11A-02 is supplied with the LP20 Controller and occupies slots A04 and B04 (Unibus Out). The BC11A from the previous option, option B in Figure 1-2, will occupy slots A01 and B01 (Unibus In).

NOTE
If this LP20 Controller is the last unit on the Unibus, the terminator module occupies slots A04 and B04.

The LP20 cable comes in four standard lengths:

Part No.	Length
7011426-25	7.62 m (25 ft)
7011426-50	15.24 m (50 ft)
7011426-75	22.86 m (75 ft)
7011426-A0	30.48 m (100 ft)

Hardware jumpers on the M8586 module allow the controller to be configured for the correct base address and interrupt vector. A ONE is represented by removal of a base address selection jumper and by insertion of an interrupt vector selection jumper.

A Unibus priority plug sets the priority for bus requests. The plug normally used places bus requests at priority level No. 4 (BR4/BG4).

The LP20 power harness is tied to the harness support bracket on the wire-wrap side of the LP20 wired assembly. Six wires in the power harness connect to associated power terminals on the wired assembly. These wires are ACLO and DCLO (Unibus power supply status signals), two for +5 Vdc, and two for ground.

The 13-bit translation RAM is located on the M8585 module. The RAM storage consists of 13 RAM packages (256 words × 1 bit per package). The translation RAM and the printer DAVFU memory are both volatile memory devices which lose their stored contents when primary power is removed.

1.5 APPLICABLE DOCUMENTS

This manual and the appropriate Dataproducts Corporation line printer manual must be used together for a complete understanding of the LP20 Line Printer System. The prime subject of this manual is the LP20 Controller. The line printers are described in detail in the Dataproducts Corporation manuals.

Table 1-3 lists the documents that are applicable to LP20 Line Printer Systems.

Table 1-3 Applicable Documents

Title	Number	Description
LP20 Line Printer Systems (Field Maintenance Print Set MP00006)	B-TC-LP20-0-1	Detailed LP20 Controller module logic diagrams, backplane, and cable information.
PDP-11 Processor and System Manuals	*	A series of maintenance and theory manuals that provide a detailed description of the basic PDP-11 System.
PDP-11 Processor Handbook	**	A general handbook that discusses system architecture, addressing modes, the instruction set, programming techniques, and software.
PDP-11 Peripherals Handbook	*	A handbook devoted to a discussion of the various peripherals used with PDP-11 Systems. It provides detailed theory, logic flow, and descriptions of the Unibus and external device logic; methods of interface construction; and examples of typical interfaces.

*Applicable manuals are furnished with the system at the time of installation. The document number depends on the specific PDP-11 family processor.

**Use the processor handbook unique to the actual CPU.

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

This chapter is a guide for the installation of LP20 controllers and associated line printers. Detailed information required for installation of the line printer is contained in the appropriate line printer technical manual.

CAUTION

Although specific installation procedures are included in this and the referenced manuals, it is recommended that the equipment be installed by Digital Equipment Corporation field service personnel.

2.2 EQUIPMENT UNPACKING

2.2.1 Unpacking the Line Printer

Before removing the line printer from its shipping container, place it as close as possible to the final installation position. Unpack the equipment according to the detailed procedures in the appropriate line printer technical manual.

2.2.2 Unpacking the LP20 Controller

1. Remove the LP20 Controller from its shipping carton.

2. Check all packing material before discarding to ensure that no components or hardware are accidentally discarded.

2.3 INSPECTION

After removing the equipment, inspect all components according to the following procedure. Report any damage to the local DIGITAL field office.

1. Check the equipment received against the shipping checklist (A-PL-LP20-0-SL) to be certain that all equipment has been received.

2. Inspect the LP20 Controller modules for any signs of damage.

3. Inspect the LP20 wired assembly (7011427) for bent pins and verify that there is no short circuit between +5 V and ground by measuring with an ohmmeter between pins C02A2 and C02C2.

4. Inspect the line printer according to the detailed procedures in the appropriate line printer manual.

2.4 INSTALLATION PROCEDURES

The following paragraphs describe the procedures required for installing an LP20 Line Printer System.

2.4.1 Installing the Line Printer

Install the line printer according to the detailed procedures in the appropriate line printer technical manual.

2.4.2 Installing the LP20 Controller

2.4.2.1 Module Configuration

Device and Vector Addresses – One or two LP20 Controllers may be installed in the peripheral cabinet. When a system has one controller and one line printer, its base address (device address) will be 775400 and its corresponding vector address will be 754. However, when the system has two controllers and two line printers, the base address and vector address are assigned as follows:

Unit No. 1	Base address	775400
	Vector address	754
Unit No. 2	Base address	775420
	Vector address	750

Refer to drawings D-CS-M8586-0-LPC1 and D-CS-M8586-0-LPC4 in the LP20 print set for correct configuration information for the M8586 module.

Priority Level – The bus request/grant priority plug installed at the factory selects priority level BR4/BG4. Details of these jumper connections are provided in Chapter 5.

Direct Access or Optical VFU – All line printers except LP10-J, -K (LP20-F, -A) have a direct access vertical format unit (DAVFU). LP10 line printers have a paper tape (optical) vertical format unit. Refer to drawings D-CS-M8587-0-LPD0 and D-CS-M8571-0-LPD0 for correct jumper or dipswitch configuration for the printer in use.

Line Printer Parity – Refer to drawings D-CS-M8587-0-LPD0 and D-CS-M8571-0-LPD0 for correct jumper or dipswitch configuration based on the model of line printer in use.

2.4.2.2 Installing a Single LP20 Controller – When the appropriate jumper wires on the modules have been removed, the next step is to install the controller. Refer to Figure 1-2 and proceed as follows for a typical installation:

NOTE

Refer to the LP20 Field Maintenance Print Set (MP00006) for cable drawings, circuit schematics, and a drawing of the wired assembly.

1. Determine the proper mounting position for the LP20 wired assembly (7011427).

2. Install the wired assembly and harness support in the mounting drawer. Before tightening the cap screws completely, insert a hex-height module into the wired assembly to check card guide alignment.

3. With a hex-height module in place, tighten the two cap screws securely and remove the hex-height module.

NOTE
Skip steps 4 and 5 if power harness 70-12475 is supplied.

4. Wrap the following unused Faston tabs of the power harness (70-09563) with tape:

   Line clock (brown wire)
   +15 V (grey wire)
   −15 V (blue wire)

5. Tie back the loose wires. Then lace the entire power harness to the harness support.

6. Make the six electrical connections between the power harness and the wired assembly.

7. Make electrical connections between the power harness and the mounting drawer by plugging the two Mate-N-Lok connector plugs into available connector receptacles.

8. Install the Unibus cable assemblies according to Figure 1-2. If this LP20 is the last device on the Unibus, an M930 Unibus Terminator module, instead of the Unibus cable assembly, must be installed in slots A04 and B04.

9. Without modules installed, power up the system and measure ±5.0 V ±5% between either red wire (+5 V) and either black wire (ground) of the power harness at the Mate-N-Lok connector.

10. Power down the system and install the three LP20 modules according to Figure 1-2.

11. Connect the BC06R-10 cable to the Berg connector on the M8587 module with the wire (rib) side toward the module and the red line on the cable away from the handle.

12. Connect the other end of the BC06R-10 cable to the center slot of the receptacle housing assembly (7009861) with the red line on the cable toward the locking cam indentation as shown in Figure 1-2.

13. Connect the LP20 round cable (7011426-XX) to the receptacle housing assembly and connect the other end of the LP20 round cable to the line printer Winchester connector.

CAUTION
Route cables so that they do not bind or interface with other cables or modules. Do not overtighten the printer connector.

14. With modules and cables installed, power up the system and again measure +5.0 V ±5% as described in step 9.

2.4.2.3 Installing Two LP20 Controllers – Installation of the second LP20 Controller is the same as that for the first controller, except for the configuration of address and vector jumpers.

2.5 AC POWER CHECKOUT PROCEDURES FOR LP20 LINE PRINTER SYSTEMS

After an LP20 Line Printer System has been unpacked and installed at the site, perform the following checkout procedure before connecting the printer power cable to the power source. The power source may be either the receptacle in the system cabinet or a separate wall outlet.

1. Measure the ac source voltage to ensure that the proper voltage is present. Check that measured voltage is correct for the line printer power supply, as wired. If rewiring is necessary see appropriate line printer tehnical manual.

2. Plug line printer primary power cable into the power source receptacle.

3. Set the installation source power circuit breaker to the ON position.

4. Measure the potential between earth ground of the power source and the line printer frame. It should be 0 V with the processor on.

5. Power up the line printer according to the procedures in the appropriate line printer technical manual.

2.6 SYSTEM CHECKOUT PROCEDURE

Perform a checkout of the line printer according to the procedures in the appropriate line printer technical manual then perform the following LP20 Line Printer System checkout procedures.

1. Refer to the LP20 Line Printer diagnostic listing for operational assistance and console switches used in debugging the controller.

2. Place the line printer on-line according to the appropriate line printer technical manual. Verify that the ON-LINE indicator lights. Run the following tests as specified. No errors are allowed.

NOTE

Steps a through e below may be performed with the LP20 Controller in the system but no line printer connected.

   a. Place the HALT/ENABLE switch on the processor in the HALT position.

   b. Load the appropriate start address as specified in the LP20 diagnostic listing.

   c. Set all processor data switches down. The controller will simulate the physical output device even if one is not connected. This is the Test mode.

   d. Place the HALT/ENABLE switch in the ENABLE position and press the START switch. Run the diagnostic for five error-free passes.

   e. Halt the processor.

   f. Load the appropriate start address.

   g. Set switch 0 up. The LP20 Controller will send characters to the line printer and printing will occur. This is the Print mode.

   h. Repeat steps c and d above. Verify that the line printer output is correct. This completes the system checkout.

CHAPTER 3
OPERATION

The LP20 Controller does not have controls or indicators and there are no operating procedures applicable to the controller. All LP20 Line Printer System operator controls and indicators are on the associated line printer.

Refer to the appropriate line printer technical manual for detailed descriptions of the line printer controls, indicators, and operating procedures. The line printer technical manuals also contain descriptions of fault indicator and printer form controls, instructions for paper/forms installation and alignment, instructions for ribbon removal and replacement, and instructions for powering up and powering down the line printer.

The line printer technical manuals also contain troubleshooting procedures and corrective action for common problems that could be encountered when operating the line printer. If the corrective action specified does not correct the problem, or if the problem is not listed in the appropriate line printer technical manual, contact service/maintenance personnel.

If problems are attributable to the controller, it is necessary to run the LP20 diagnostic program.

NOTE

If an error in the LP20 Controller is detected during printer operation, the LP20 Controller will interrupt the processor and the print operation will be stopped. If the problem is corrected and the controller is functioning properly, the printer will then continue where it left off.

If an error occurs in the printer, on the other hand, the printer will automatically go off-line and cease printing until the problem is corrected.

Any power supply problem which causes the Unibus fault signal ACLO to be asserted will inhibit the NPR request and bus request logic. This prevents the LP20 Controller from requesting use of the bus during a power-fail or power-down condition.

CHAPTER 4
PROGRAMMING

4.1 INTRODUCTION

This chapter contains detailed information for programming the LP20 Line Printer System. Included is a condensed description of the different operational modes, followed by a tabulation of specific address assignments and bit definitions. A sample device routine program at the end of the chapter illustrates the different functions that can be programmed in a typical printing operation.

Registers and individual flip-flop states are available for examination by the processor. DMA is performed by setting up the correct register contents, setting up status and control bits to select the desired mode of operation in control and status registers A and B (CSRA and CSRB), and then bit-setting the GO bit (bit 00 of CSRA). The bit-set of bit 00 in CSRA is necessary due to timing constraints within the controller.

CAUTION

An attempt to set GO, and any other bits not previously set, in CSRA during the same instruction may produce unpredictable results in operation of the controller. Any attempt to modify bits in CSRA while GO is set may destroy the contents of the checksum register and produce other undesirable results.

4.2 OPERATIONAL MODES

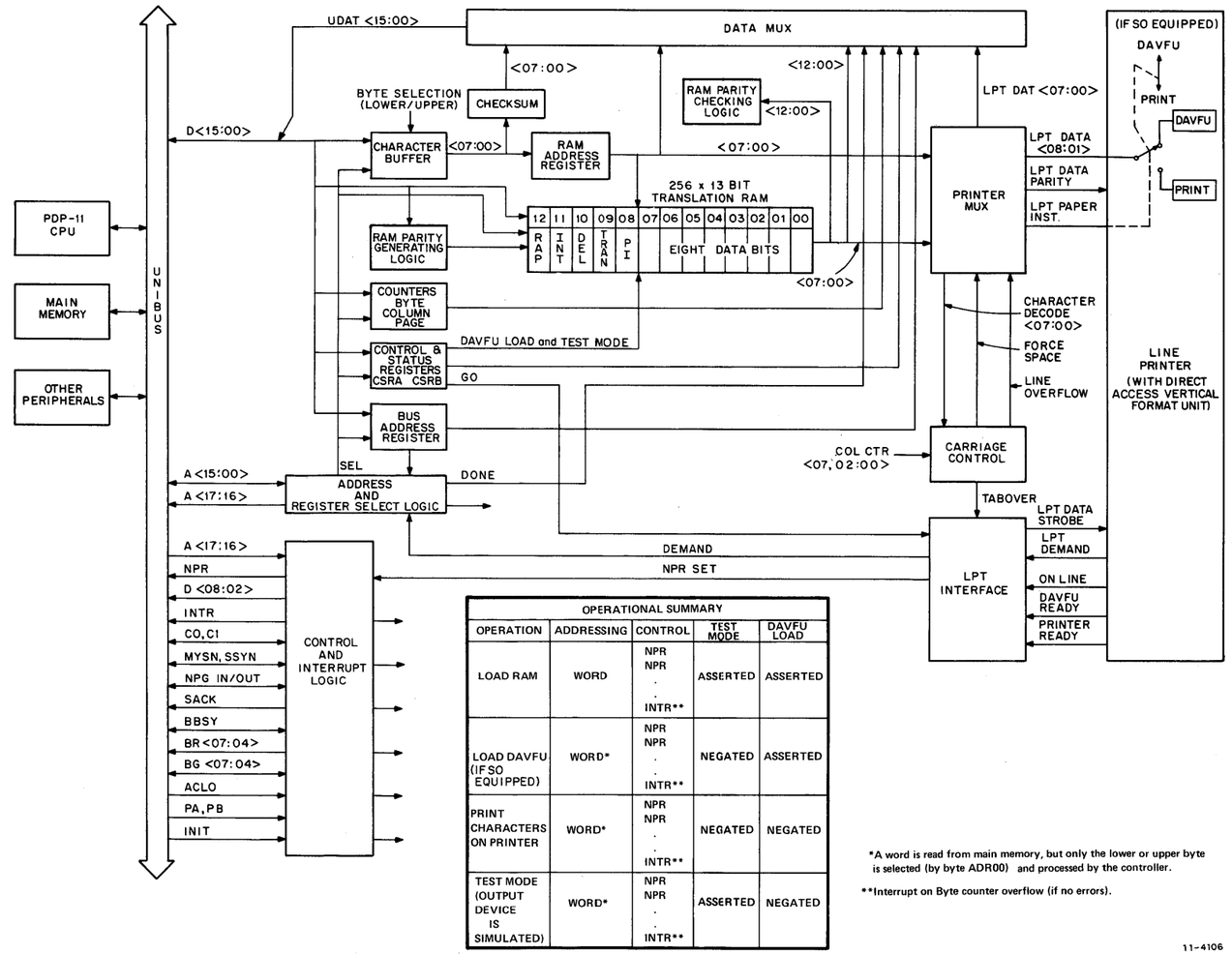
Figure 4-1 shows the block diagram of an LP20 Line Printer System, and also includes a summary of the four modes of operation:

1. Loading the RAM
2. Loading the DAVFU
3. Printing Characters
4. Test Mode

The four modes are microcoded in bit 02 (Test mode) and bit 03 (DAVFU Load) of control and status register A (CSRA). LP20 Line Printer Systems using printers not equipped with a DAVFU do not use the DAVFU Load mode of operation.

Assume initially that the line printer has been placed on-line and that the controller has been initialized by a UBUS INIT signal. (Initialization also occurs whenever the CPU is halted and the CPU START switch is depressed, or a RESET instruction is executed. It is also possible to clear the controller by sending a Local Initialize or Error Reset command* to the LP20 Controller.)

*See Sections 4.6 and 4.7 for details.



OPERATIONAL SUMMARY				
OPERATION	ADDRESSING	CONTROL	TEST MODE	DAVFU LOAD
LOAD RAM	WORD	NPR NPR . . INTR**	ASSERTED	ASSERTED
LOAD DAVFU (IF SO EQUIPPED)	WORD*	NPR NPR . . INTR**	NEGATED	ASSERTED
PRINT CHARACTERS ON PRINTER	WORD*	NPR NPR . . INTR**	NEGATED	NEGATED
TEST MODE (OUTPUT DEVICE IS SIMULATED)	WORD*	NPR NPR . . INTR**	ASSERTED	NEGATED

*A word is read from main memory, but only the lower or upper byte is selected (by byte ADR00) and processed by the controller.

**Interrupt on Byte counter overflow (if no errors).

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Figure 4-1 LP20 Line Printer System Block Diagram

When the printer is placed on-line, the printer DEMAND line is asserted, whereupon the DONE bit in CSRA is asserted. This indicates that the printer is on-line and ready to receive data on the bus.

4.2.1 Loading the RAM

Before characters are actually sent to the line printer, it is normal procedure to first load the translation RAM in the controller. The device routine first checks the status of the ERROR and DONE bits in the CSRA. If the error flag is set (bit 15 of CSRA), the service routine first handles the error condition and then clears the error flag. The bus address register and the byte counter in the controller are then loaded, and the bits necessary for loading the RAM are set.

NOTE

The RAM can be loaded under program control or via DMA. This section discusses loading via DMA. See Section 4.3 for details on RAM load under program control.

The bus address register contains the 18-bit address of the first word to be loaded into the RAM. Bits (15:00) are loaded by depositing them into the bus address register. Bits (17:16) are deposited into bits (05:04) of CSRA.

The byte counter is a 12-bit binary counter and is loaded with the two's complement of the total number of bytes to be loaded into the RAM (2 bytes/word × 256 words = 512 bytes).

When the bus address register and the byte counter have been set up, control flip-flops in CSRA are set to establish the conditions for Interrupt Enable, Parity Enable, DAVFU Load, and Test mode. Asserting DAVFU Load and Test mode set up the condition for loading the translation RAM. In RAM Load or Test mode, the controller will fetch data from main memory, but no data will be sent to the printer.

The device routine then sets the GO flip-flop in CSRA to the one state. At this time, the RAM address register is cleared so that octal address 000 is selected in the RAM. When the GO flip-flop is set, a nonprocessor request (UBUS NPR) is initiated to request use of the bus for a DATI transfer into the LP20.

A DMA bus cycle follows to fetch the data contained in the main location specified by the contents of the bus address register. If the main memory receives and processes the memory request properly, it will return the requested data. Otherwise, the controller will time out, terminate UBUS MSYN, set an error flag in control and status register B (CSRB), and request an interrupt.

Assuming that the DATI transfer is successful, the least significant 12 bits of data, DATA (11:00), from main memory are clocked into octal address 000 of the RAM along with a parity bit for the data word in octal address 000 generated by the controller.

In this case, the parity bit is a 1 if there are an even number of 1s in bits (11:00), and a 0 if there are an odd number of 1s in bits (11:00). This is the condition for odd parity. The high-order bits of the DATI word, (15:12), are ignored by the controller during RAM Load. Even parity may be written or checked by setting the code for RAM Parity Test in the Test Type bits in control and status register B (CSRB).

The RAM is capable of storing 256 13-bit words. Each word contains eight data bits, a paper instruction (PI) bit, a translation (TRANS) bit, a delimiter (DEL) bit, an interrupt (INT) bit, and a RAM parity (RAP) bit. Details of the RAM control bits are provided in Tables 4-4 and 4-5.

The eight data bits (07:00) are a data character. This character can be either a printable character or a non-printing character. Printable characters include letters of the alphabet, numerals, and special symbols, depending on the character set in use.*

Carriage control characters include carriage return (CR), line feed (LF), and form feed (FF). Horizontal tab (HT) is not recognized by the line printer. Instead, horizontal tab is decoded by the controller which then forces one to eight space codes onto the printer data lines depending on the current value of the column counter. The space codes produce 8-column fields, starting at columns 9, 17, 25, . . . 8N + 1, where n = 1, 2, 3, etc. for a maximum of 16 fields per line.

Mnemonic	Code (Octal)	Name	Function
CR	015	Carriage Return	Causes the currently stored characters to be printed; then resets column counter to zero. Does not advance paper.
LF	012	Line Feed	Causes the currently stored characters to be printed; then resets column counter to zero and advances paper one line.
FF	014	Form Feed	Functions the same as LF above except paper is advanced to the next Top-of-Form position.
HT	011	Horizontal Tab	Converted by the controller to 1–8 space codes. The number of spaces sent is determined by the column counter value at the time HT is decoded.

If a line contains more than 132 decimal printing characters, hardware line overflow will occur. The controller will print 132 characters and begin a new line. The 133rd character will be printed as the first character of the next line. Trying the tab beyond column 128 causes the printer to automatically tab to column 9 on the next line.

If the 133rd character is CR, LF, or FF, there will be no hardware line overflow, and the specified function will be executed. If a translated Paper Instruction is programmed, the contents of the printer buffer will be printed and the paper will then slew 0 to 15 lines, or move according to the contents of the preselected DAVFU channel. See Tables 4-6 and 4-7.

The paper instruction (PI) bit is asserted when the character is to be recognized by the DAVFU or VFU as a code for vertical formatting. The PI bit is asserted only if translation is taking place (see Table 4-5). In this case, the signal LPT PAPER INST is asserted. Otherwise, the PI bit is a 0, and the character is routed directly to the printer buffer, either for printing or for print control (that is, CR, LF, or FF).

The translation (TRANS) bit is asserted when the character in that particular RAM location is to be routed to the printer. If translation is not taking place, the character in the character buffer will be routed to the printer (Table 4-5).

Setting the delimiter (DEL) bit to a 1 will cause the current character and the next incoming character to be translated (taken from the RAM instead of the character buffer) regardless of the state of the translation (TRANS) bit. The character with the delimiter bit asserted is normally translated into a no-action character (ASCII 000) (Table 4-5).

*See Appendixes B, C, and D.

Asserting the interrupt (INT) bit will cause the controller to generate a bus request (BR) interrupt to the processor instead of generating a data strobe to the printer, provided Interrupt Enable is set in CSRA. Other RAM control bits being asserted may disable the bus interrupt (Table 4-5).

The least significant eight data bits, DATA (07:00), are also clocked into the character buffer. These bits, which represent the lower order byte of the data word, are then routed to the checksum generator and added to the binary sum currently in the checksum hold register. The data bits from the character buffer are not loaded into the RAM address register during this mode of operation.

Following checksum, both the bus address register and the byte counter are incremented by one. Shortly thereafter, the controller NPG BBSY flip-flop is cleared, which negates UBUS BBSY. At this point, the LP20 relinquishes control of the bus.

When the LP20 relinquishes control of the bus, the Data Strobe flip-flop in the LPT interface is asserted. However, because the controller is in the RAM Load mode (Test mode = 1, DAVFU Load = 1), a data strobe is not sent to the printer. Instead, a simulation of the line printer interface takes place within the controller. Also a Demand Timeout test is activated. If the DEMAND signal is not removed and the Data Strobe flip-flop is not cleared before the Demand Timeout test times out, a Demand Time error occurs. This sets the Error flip-flop and halts the controller.

If the byte count has not reached zero and no error conditions occur, another NPR is requested. Again, UBUS NPR is asserted, indicating that the LP20 is requesting use of the bus for another DATI transfer.

When the second UBUS NPR is asserted, the same data word is written into RAM location 000. All other operation is identical to the preceding, except that: the higher order data byte is clocked into the character buffer and then into the checksum generator; and the RAM address register is incremented by one. This means that, in the RAM Load mode, the bus address register and the byte counter are incremented by one on each NPR so that a total of two NPRs are required to transfer first the lower order byte and then the higher order byte of each RAM word to the character buffer and checksum register. The RAM address register, on the other hand, is only incremented once during the two NPR cycles since the RAM address register contains a RAM word address and each bus cycle is performed to transfer one byte only to the character buffer and checksum generator. Therefore, a total of 512 NPRs are required to fully load the RAM (256 words × 2 bytes/word × 1 NPR/byte = 512 NPRs).

From this point on, words are loaded from main memory into the translation RAM, one at a time, as previously described. The loading of words continues until the byte counter overflows (goes to zero). When this happens, the DONE bit is set to a 1, no further NPRs are requested, the GO flip-flop is cleared, and a bus interrupt is sent to the processor by the assertion of UBUS BR4. The processor responds by asserting UBUS BG4 IN, indicating that use of the bus has been granted for an interrupt. The controller responds by asserting UBUS SACK, thereby acknowledging receipt of the bus grant. The processor, in turn, responds to UBUS SACK by removing UBUS BG4 IN. When the bus becomes idle, the controller sets the BG BBSY flip-flop, which asserts UBUS BBSY. At this time, the interrupt vector address is forced onto the bus data lines.

The vector address is determined by jumpers on the M8586 module (vector address 754 for an installation with one line printer; vector addresses 754 and 750 for an installation with two line printers, No. 1 and No. 2 respectively). The vector address specifies the memory location that contains the starting address of the device routine.

The processor responds to UBUS BBSY by asserting UBUS SSYN. In effect, the controller BG BBSY flip-flop is cleared, so that UBUS INTR and the vector address lines are no longer asserted. The controller then removes UBUS BBSY. The processor responds by removing UBUS SSYN. This completes the RAM Load, and bus control is returned to the LP20 device routine in the processor.

4.2.2 Loading the DAVFU (Not Applicable to LP10 Line Printers)

After the translation RAM has been loaded, it is normal procedure to initialize the LP20 Controller by a Local Initialize or Error Reset command, and then load the direct access vertical format unit (DAVFU) in the line printer. The data path module must be correctly configured for the type of VFU in use. Bit 11 of CSRB asserted indicates an optical VFU (Paragraph 2.4.2.1).

The steps in setting up the controller for DAVFU Load are identical to those for RAM Load except that the DAVFU Load flip-flop is set and the Test Mode flip-flop is cleared. The bus address register and byte counter are loaded and the GO bit is set as before.

The value loaded in the byte counter depends on the maximum number of lines in a complete form (Figure 4-2). For example, an 11-inch form, at 6 lines per inch, is 66 lines long from one Top-Of-Form position to the next. Each line is represented by a bit position in all DAVFU channels. That is, there is one bit position per line in each channel. Bits from each channel that correspond to the same line are referred to as a DAVFU partition. Hence, a 66-line format has 66 partitions of one bit per line per channel each.

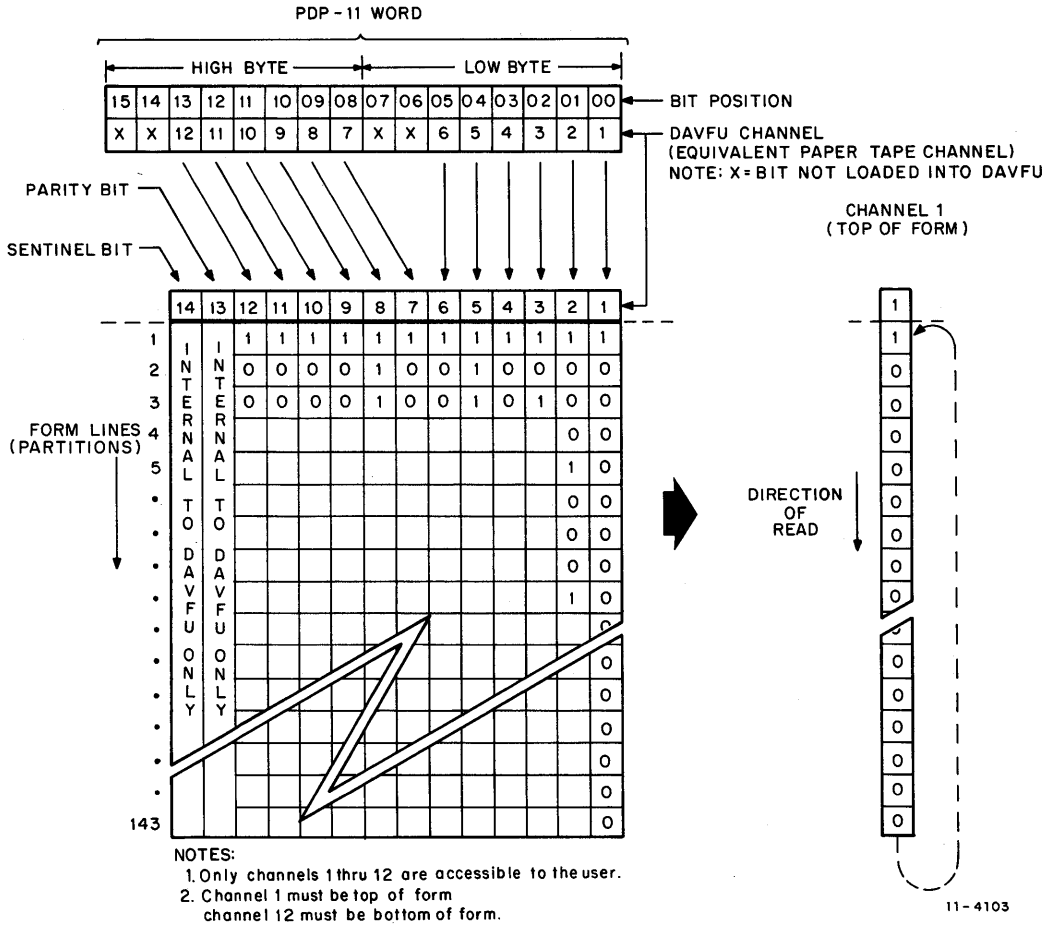


Figure 4-2 Typical Bit Patterns in DAVFU Memory

The bytes to be loaded are always preceded by a start code of 356 and terminated by a stop code of 357.* It is normal procedure to write the program so that the byte counter overflows when a stop code is sent to the printer. Consider the case where the printer is to handle an 11-in. (27.94-cm) form, with a total of 66 lines at a setting of 6 lines per inch by means of the 6LPI switch on the printer. Since two bytes (characters) are loaded per DAVFU partition, the total number of bytes is 2×66, or 132. A DAVFU start code of 356 and a DAVFU stop code of 357 bring the total byte count to 134_{10} or 206_8. (The two's complement of 134_{10} is 7572_8, and this is the octal number loaded into the byte counter.)

When the bus address register and the byte counter have been set up, control flip-flops in control and status register A (CSRA) are set to establish the conditions for Interrupt Enable, Parity Enable, and DAVFU Load. The Test Mode flip-flop is not asserted so that incoming characters will be routed to the printer DAVFU.

The next step is to set the GO flip-flop in CSRA to the one state. The contents of the checksum register are destroyed when GO is set.

With the GO flip-flop set and the printer DEMAND line asserted, the controller will perform a non-processor request (NPR). This NPR indicates that the controller is requesting use of the bus for a DATI transfer.

Assuming that the NPR is completed, the first byte of data from main memory is clocked into the character buffer. The byte loaded is selected by bit 00 of the bus address register. The eight bits constitute one of the bytes of the data word on the bus, which in this case is the DAVFU start code (356_8). The same eight bits are added to the binary sum currently in the checksum hold register.

At the appropriate clock time, the output of the character buffer is loaded into the RAM address register. This 8-bit byte is also applied to the data multiplexer and to the printer multiplexer. Reading of RAM control bits is disabled during DAVFU Load so no translation can occur and the output of the RAM address register (i.e., the DAVFU start code) is applied to the printer multiplexer. The least significant seven bits of the start code are then routed from the printer multiplexer to the line printer as LPT DATA (08:01). The LPT paper instruction is also asserted, causing the start code to be applied to the printer and initiating the DAVFU Load cycle.

The eight bits from the RAM address register are also applied to a parity generator in the printer multiplexer. The DAVFU start code has an even number of 1s, so LPT DATA PARITY is asserted.

Following checksum, both the bus address register and the byte counter are incremented by one. Shortly thereafter, the controller NPG BBSY flip-flop is cleared, negating UBUS BBSY. At this point, the LP20 relinquishes control of the bus.

When the LP20 relinquishes control of the bus, the Data Strobe flip-flop in the LPT interface is asserted. Since the controller is not in the Test mode, a data strobe is sent to the printer, thereby strobing in DAVFU start code 356. At the same time, a Demand Timeout test is activated, during which the printer must remove its DEMAND signal and cause the Data Strobe flip-flop to be cleared. If the printer fails to remove DEMAND before the end of the Demand Timeout test, the error flag is set and the controller halts. When the printer DEMAND signal is again asserted, NPR SET and UBUS NPR are asserted, indicating that the LP20 is requesting use of the bus for another DATI transfer.

*See Section 4.5 for DAVFU details.

When the second UBUS NPR is asserted, operation is the same as before, except that the next data byte is clocked into the character buffer and routed to the checksum generator. The byte is then clocked into the RAM address register and transferred through the printer multiplexer to the printer. The six least significant bits of the data byte are then strobed into the first six bit positions (1–6) of the first DAVFU memory location. On the next UBUS NPR, the six least significant bits of the next data byte will be strobed into the last six bit positions (7–12) of the first DAVFU memory location. From this point on, higher and lower order data bytes are loaded into the DAVFU memory until a DAVFU stop code (357_8) is decoded. Programs are generally written so that the byte counter overflows when the stop code is decoded. When the byte counter overflows, the DONE bit is set to a 1, NPR SET is negated, the GO flip-flop is cleared, and UBUS BR4 is asserted. Operation thereafter is the same as in RAM Load.

It should be noted that a DAVFU READY line runs between the line printer and the controller data multiplexer. When this line is asserted, bit position 12 in data multiplexer status register A (CSRA) becomes a 1, indicating that the DAVFU has been loaded correctly and that no errors have occurred in the DAVFU.

4.2.3 Printing Characters

After the DAVFU has been loaded, it is normal procedure to initialize the LP20 Controller by a Local Initialize or Error Reset command. The next step is to set up the bus address register, the byte counter, and the page counter.

The bus address register is loaded with the starting address in main memory of the data to be sent to the printer for the printing operation.

The byte counter is also loaded under program control. The number loaded, in this case, is the two's complement of the total number of bytes (characters) in the data block to be sent to the printer. The byte counter is capable of counting up to $2^{12} = 4096$ bytes before overflowing.

The page counter is a 12-bit binary counter. It is also loaded under program control, generally to the number of pages to be printed (up to $2^{12} = 4096$). Unlike the bus address register and the byte counter, the page counter is decremented. Decrementing occurs each time the printer reaches the top of a new page (whether by form feed or normal printing) and sends a Top-of-Form signal to the page counter. When the count reaches zero, the controller will stop printing, request an interrupt, and indicate that the page limit has been exceeded by setting a PAGE ZERO bit in control and status register. (The controller will allow printing of one full page more than the count initially loaded into the page counter.) If the page counter is initially cleared and not preset, the counter will contain the two's complement of the number of complete pages printed.

Unlike the other counters, the column counter is not loaded to a preset value under program control. The function of the column counter is to keep track of the number of printable characters (and spaces) stored in the printer buffer. The counter is both readable and writable, but is only written into for diagnostic purposes. In the printer line, the leftmost character position is considered as 0, and the rightmost character position is considered as 131. At any given time, the number in the column counter is the number of the column in which the next printable character will be printed. A character which causes printing (such as line feed) resets the column counter to zero after the printer acknowledges receipt of the character. Sending a non-printing character to the printer causes the column counter to increment, but loads a space code into the printer buffer.

When the bus address register, the byte counter, and the page counter have been set up, control flip-flops in CSRA are set to establish the conditions for Interrupt Enable and Parity Enable. DAVFU Load and Test mode are negated (set to 0) in the Print mode.

The next step is to set the GO flip-flop in CSRA to the one state. Checksum is set to zero when GO is set. With the GO flip-flop set and the printer DEMAND line asserted, an NPR is performed.

This non-processor request indicates that the controller is requesting use of the bus for a DATI transfer. From here on, "handshaking" between the processor and controller is the same as in the other modes up to the point where data and slave sync are sent from main memory to the controller. The desired byte of the current word (selected by bit 00 of the bus address register) from main memory is clocked into the character buffer. These eight bits are routed first to the checksum generator and then to the RAM address register. The byte in the RAM address register is applied to the data multiplexer, the printer multiplexer, and the translation RAM. The byte to the RAM selects the corresponding address in the RAM, which causes the character stored in the RAM data bits at that location to be applied to the printer multiplexer concurrently with the byte from the RAM address register. Depending on the status of the translation bit previously stored in that RAM address (i.e., bit 09) and the status of other control bits in the controller, either the translated or non-translated character is routed to the printer. What happens next depends on the status of the remaining control bits in that RAM address, as shown in Tables 4-4 and 4-5.

Following checksum, both the bus address register and the byte counter are incremented by one. Shortly thereafter, the controller NPG BBSY flip-flop is cleared, negating UBUS BBSY. At this point, the LP20 relinquishes control of the bus.

When the LP20 relinquishes control of the bus, the Data Strobe flip-flop in the LPT interface is asserted. Since the controller is not in the Test mode, a data strobe is sent to the printer, thereby strobing in the character. At the same time, a Demand Timeout test is activated, as discussed in Section 4.2.2 on DAVFU loading. When the printer DEMAND signal is again asserted, another non-processor request is asserted by the controller, indicating that the LP20 is requesting use of the bus for another DATI transfer.

When the second UBUS NPR is asserted, operation is the same as before, except that the next data byte is clocked into the character buffer and routed to the checksum generator. The byte is then clocked into the RAM address register and used to select the corresponding address in the translation RAM. Other operations are the same as the first NPR.

On successive NPRs, characters are routed into the character buffer and then to the printer, either directly or via the RAM. Both the bus address register and byte counter are incremented by one on each NPR cycle, whereas the page counter is decremented by one whenever a Top-of-Form is reached by the printer. When the byte counter overflows, the DONE bit is set to a 1, the GO flip-flop is cleared, UBUS BR4 is asserted, and the printing operation stops. To continue printing, the byte counter must be reloaded.

4.2.4 Test Mode

Programming the controller in Test mode disables any data from reaching the line printer. The controller simulates the DEMAND signal which the printer normally generates to request and acknowledge receipt of data. Hence, the controller operates normally, except that there is no simulation of the Top-of-Form signal, so the page counter will not decrement. The page counter can be tested by setting the test type bits in CSRB to 6_8 and writing a 1 into bit 00 of CSRB. The page counter will decrement by one each time bit 00 is set.

The test type bits cause error states in the controller to allow testing of the error detection logic. Normally, these bits are zeroed. Test type 7 is not used.

See Table 4-3 for an explanation of the various controller tests and error flags in CSRB.

4.3 DEVICE REGISTERS

Software manipulation of the line printer controller is performed by means of eight device registers. These registers have been assigned bus addresses and can be read or loaded under program control. The device registers and associated addresses are listed in Table 4-1. Bit assignments of the two status registers, CSRA and CSRB, are delineated in Tables 4-2 and 4-3.

4.4 TRANSLATION RAM

Interpretation of the bit assignments in the translation RAM is delineated in Table 4-4. A description of the various permutations of LP20 control bits is provided in Table 4-5.

4.5 DIRECT ACCESS VERTICAL FORMAT UNIT (DAVFU) (Not Applicable to LP10 Line Printers)

The DAVFU is a solid-state replacement of the 12-channel optical tape reader. It allows for rapid advancement of paper to a predetermined line position under software control, and permits convenient handling of a variety of form lengths. The DAFVU is loaded by the LP20 Controller under DMA only. The load always starts with start code 356 and ends with stop code 357. Once the DAVFU is loaded and stop code 357 has been received by the printer, it is only necessary to assert the PI bit to select a DAVFU function (coded in the associated RAM data bits). During DAVFU Load, the control bits of the RAM are disabled.

The DAVFU memory has 143 partitions, each 14 bits wide. The DAVFU is capable, therefore, of controlling forms which are up to 143 lines long. This corresponds to a maximum forms length of 24 or 18 in. (61 or 46 cm) for 6- or 8-line-per-inch printing, respectively. The minimum form length which can be accommodated using the DAVFU is 2 in.

Each DAVFU partition is loaded by a 2-character sequence. In each sequence, the low-order six bits of the first character received are used to load DAVFU channels 1 through 6. The low-order six bits of the second character received are used to load channels 7 through 12. A 1 in the character represents a channel stop in the DAVFU memory. For example, to program the first partition with stops in channels 1, 2, 3, 5, 6, and 12, the 2-character sequence 067_8 and 040_8 would be used. Subsequent partitions would be loaded using additional 2-character sequences. This process is repeated until the desired number of partitions have been loaded. At that time, stop code 357 is sent to the printer. The stop code must always follow the second character of a line. The DAVFU will not accept and strobe incomplete data. To do so results in a DAVFU error (DAVFU RDY bit negated). At the completion of a valid memory load, the position of the first line of channel-stops received will be assigned to the line on the form then present at the print station.

It is possible to electrically realign the contents of the memory with respect to the position of the paper by sending only a stop code (357) to the DAVFU. When this is done, the first memory partition of the previous load now corresponds to whatever line of the paper is now in the print position.

The 13th DAVFU memory channel is internally loaded with the parity bit calculated for odd parity. The 14th DAVFU memory channel is internally loaded with a sentinel bit which corresponds to the number of memory positions utilized (i.e., multiple of the forms length). Both of these bits are automatically loaded by the DAVFU.

Table 4-1 LP20 Register Allocation Summary

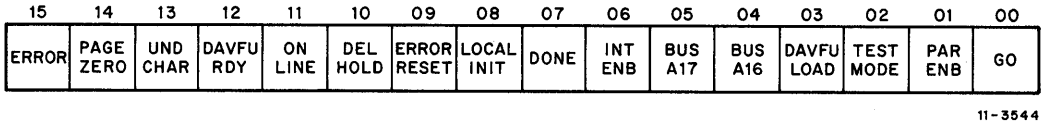
Register	Bus Address	WORD BITS 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
*CSRA Hi Byte	775401 or 775421	ERROR R	PAGE ZERO R	UNDCHAR R	DAVFU RDY R	ON LINE R	DEL HOLD R-W	RSTERR W	LOINIT W								
*CSRA Lo Byte	775400 or 775420									DONE R	INT ENB R-W	BUS ADR17 R-W	BUS ADR16 R-W	DAVFU LOAD R-W	TEST MODE R-W	PAR ENB R-W	GO R-W
*CSRB Hi Byte	775403 or 775423	VALID DATA R	SPARE	PRINTER NOT READY R	LPT DAT PAR R	OPTOVF R	TEST02 R-W	TEST01 R-W	TEST00 R-W								
*CSRB Lo Byte	775402 or 775422									OFF LINE R	DAVFU NOT READY R	LPT PAR ERR R	MEM PAR ERR R	RAM PAR ERR R	MSYN TIME ERR R	DEM TIME ERR R	GO ERR R-W
Bus Address Register	775404 or 775424	BUS ADDRESS R-W															
Byte Counter	775406 or 775426	SPARE				BYTE COUNTER R-W											
Page Counter	775410 or 775430	SPARE				PAGE COUNTER R-W											
RAM Data Register	775412 or 775432	SPARE	SPARE	SPARE	RAMPAR R	RAM DATA R-W											
*Column Counter	775415 or 775435	COLUMN COUNTER R-W															
*Character Buffer	775414 or 775434	CHARACTER BUFFER R-W															
*Checksum	775417 or 775437	CHECKSUM R															
*Printer Data	775416 or 775436	PRINTER DATA R															

*These registers are byte addressable.
Others are word addressable only.

R = read only
R-W = read-write
W = write only

LP20 #1 vector address 754
LP20 #2 " " 750

Table 4-2 CSRA Bit Interpretation



Bit	Name	Mode	Description
15	ERROR	R	Bit 15 = 1 when the following error(s) occur: DAVFU NOT READY* — Printer DAVFU Not Ready OFF LINE* — Printer Off-Line LPT PAR ERR* — Line Printer Parity Error MEM PAR ERR — Memory Parity Error RAM PAR ERR — RAM Parity Error MSYN TIME ERR — Master Sync Time-Out Error DEM TIME ERR — Demand Time-Out Error GO ERR — Go Error
14	PAGE ZERO	R	Page Zero. Bit 14 = 1 when the page count reaches zero.
13	UNDCHAR	R	Undefined Character. Bit 13 = 1 when an illegal or undefined character is detected. **NOTE** **Assertion of bits 14 or 13 will cause an interrupt and reset GO, but will set neither DONE nor ERROR.**
12	DAVFU RDY	R	DAVFU Ready. Bit 12 = 1 if printer DAVFU is loaded and used properly.
11	ON LINE	R	On-Line. Bit 11 = 1 if printer is ready to accept characters. **NOTE** **Bits 12 or 11 changing from 0 to 1 will cause an interrupt (to indicate a corrected error condition). Either bit going from 1 to 0 will set ERROR and cause an interrupt.**
10	DEL HOLD (DELHLD)	R-W	Delimiter Hold. Bit 10 = 1 if the last character received was a delimiter (i.e., RAM bit 10 was set). This bit can also be set or reset under program control.

*Not affected by Error Reset (CSRA bit 09 = 1).

Table 4-2 CSRA Bit Interpretation (Cont)

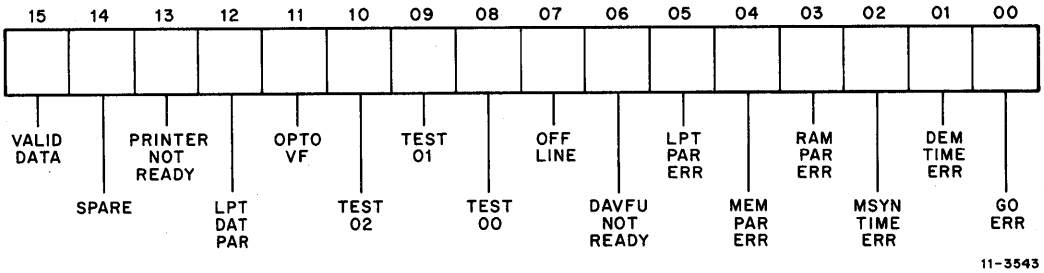
Bit	Name	Mode	Description
09	ERROR RESET (RSTERR)	W	Error Reset. Resets MEM PAR ERR, RAM PAR ERR, MSYN TIME ERR, DEM TIME ERR, and GO ERR. Resets GO bit. Sets Done bit if Test Mode is set or if printer is on-line.
08	LOCAL INIT (LOINIT)	W	Local Initialize. Bit 08 = 1 has same effect as UBUS INIT. Resets all flags, sets DONE bit (if printer is on-line and ready to print), and resets INT ENB, DAVFU LOAD, TEST MODE, PAR ENB, GO, and the three Test bits. Clears column counter, bus address register, and byte counter.
07	DONE	R	Done Bit. Bit 07 = 1 when the byte counter is incremented to zero, or LOCAL INIT or processor initialize is received and printer is ready to print. DONE is cleared when byte counter is loaded.
06	INT ENB	R-W	Interrupt Enable. When bit 06 is set to a 1, the following bits going high will cause an interrupt: ERROR, PAGE ZERO, UNDCHAR, DONE (if DONE was set by byte counter going to zero). DAVFU RDY and ON LINE changing state in either direction will cause an interrupt.
05	BUS ADR17	R-W	Bus address bit 17
04	BUS ADR16	R-W	Bus address bit 16 **NOTE** **Bits 05 and 04 will increment when bus address register overflows.**

Table 4-2 CSRA Bit Interpretation (Cont)

Bit	Name	Mode	Description
03	DAVFU LOAD	R-W	Microcoded mode control bit
02	TEST MODE	R-W	Microcoded mode control bit **NOTE** **Bits 03 and 02 are interpreted as follows:** **03 02 Controller Operation** 0 0 Print Mode. 0 1 Test Mode. Inhibits printing. 1 0 DAVFU Load. Disables RAM during DMA load to DAVFU to prevent unwanted translation, delimiter, and interrupt actions. DMA operation only. 1 1 RAM Load. Loads translation RAM (DMA mode only*).
01	PAR ENB	R-W	Parity Enable. Bit 01 is set to a 1 to enable RAM, memory, and line printer parity checking. Line printer parity may be permanently disabled via a hardware jumper.
00	GO	R-W	GO bit. Bit 00 = 1 starts controller DMA transfers. Bit 00 = 0 stops controller DMA transfers. Controller resets this bit to zero whenever controller stops for any reason (byte counter overflow, ERROR, PAGE ZERO, or UNDCHAR). **NOTE** **This bit must be bit-set after all other bits in CSRA are set up.**

*See Section 4.2.1.

Table 4-3 CSRB Bit Interpretation



Bit	Name	Mode	Description
15	VALID DATA	R	Toggles on each assertion of data strobe.
14	Spare		
13	PRINTER NOT READY	R	Indicates a fault condition is present in the printer.
12	LPT DAT PAR	R	Line Printer Data Parity. Contains the printer data parity bit as sent to the printer.
11	OPTOVF	R	Optical Vertical Format. When asserted, this bit indicates the printer has a paper tape VFU. (Set by hardware jumper. Asserted for LP10 printers only.)
10	TEST 02	R-W	Test bit 02
09	TEST 01	R-W	Test bit 01
08	TEST 00	R-W	Test bit 00

NOTE

Bits 10, 09, and 08 produce error states in the controller to allow testing of the controller error detection logic. Bit interpretation is as follows:

Octal	Test	Error	Result
0			Normal operation.
1	DEM TIME TEST	DEM TIME ERR	Prevents data strobe (DSTRB) from triggering TEST DEMAND and causes controller to time out waiting for an acknowledge. Data is present on printer data lines. Operates in Test mode only.

Table 4-3 CSRB Bit Interpretation (Cont)

Bit	Name	Mode	Description
			Octal / Test / Error / Result
			2 — MSYN TIME TEST / MSYN TIME ERR — Prevents memory SSYN from reaching the controller and causes a controller MSYN time-out.
			3 — RAM PAR TEST / RAM PAR ERR — Causes controller to check for and generate even instead of odd RAM parity on all data transfers which load the RAM. Writing odd and checking even or writing even and checking odd parity will cause a RAM parity error on each transfer.
			4 — MEM PAR TEST / MEM PAR ERR — Causes controller to think that memory has found a parity error on every attempted DMA transfer.
			5 — LPT PAR TEST / LPT DAT PAR — Causes controller to send even (incorrect) parity to the printer.
			6 — PAG CTR TEST — Each time a 1 is written into the GO ERR bit (bit 00), the page counter is decremented by one.
			7 — Not used
07	OFF LINE*	R	Printer Off-Line. Bit 07 = 1 if printer is not ready to print.
06	DAVFU NOT READY*	R	Printer DAVFU Not Ready. Bit 06 = 1 if the printer DAVFU receives a channel code before a start DAVFU Load command, receives a stop DAVFU Load command after an odd number of characters, detects a parity error while processing a control code, receives a code to a channel that has no channel stop in it, or receives a code to a non-existent channel.
05	LPT PAR ERR*	R	Line Printer Parity Error. Bit 05 = 1 if the printer detected an error in the data received from the controller. This bit may be permanently disabled by a hardware jumper.

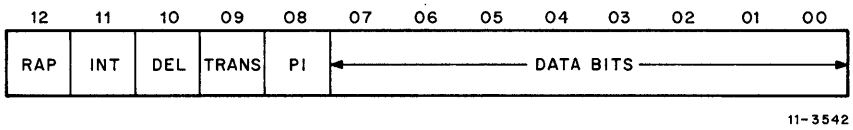
*Error Reset does not affect this bit.

Table 4-3 CSRB Bit Interpretation (Cont)

Bit	Name	Mode	Description
04	MEM PAR ERR	R	Memory Parity Error. Bit 04 = 1 if a memory parity error was detected during a DMA transfer.
03	RAM PAR ERR	R	RAM Parity Error. Bit 03 = 1 if a RAM parity error was detected during a DMA transfer.
02	MSYN TIME ERR	R	Master Sync Time-Out Error. Bit 02 = 1 if the controller MSYN timed out while attempting to reference memory because SSYN was not received.
01	DEM TIME ERR	R	Demand Time-Out Error. Bit 01 = 1 if the controller timed out while waiting for the printer to acknowledge data received.
00	GO ERR	R/W**	Go Error. Bit 00 = 1 if GO was set and an error flag was still up. This bit is written into for diagnostic purposes.

**If Test Type bits are set to 6_8, writing a 1 in this bit will cause the page counter to decrement.

Table 4-4 Translation RAM Bit Interpretation



Bit	Name	Mode	Description
12	RAP	R	RAM Parity Bit. Used to check validity of data stored in the translation RAM. Checked on each character transfer.
11	INT	R-W	Interrupt Bit. Setting bit 11 = 1 causes the controller to generate a bus request (BR) interrupt to the processor instead of generating a data strobe to the line printer if the CSRA Interrupt Enable bit (INT ENB) is set. The current character is not sent to the printer but is held in the character buffer, available for inspection by the processor. If the TRANS bit (bit 09) is also set, an interrupt will only occur if DELHLD has been set. The Undefined Character flag (UNDCHAR) is raised (bit 13 of CSRA) if an interrupt occurs.
10	DEL	R-W	Delimiter Bit. Setting bit 10 = 1 causes the current and next following printer data characters to be taken from the RAM instead of the character buffer, regardless of the state of TRANS bit 09. The delimiter character will normally be translated into a no-action character (ASCII 000). Setting bit 10 = 1 sets the CSRA Delimiter Hold (DELHLD) flag. The flag is raised upon receipt of the delimiter and is cleared upon transfer of the next character.
09	TRANS	R-W	Translation Bit. Setting bit 09 = 1 causes the character in the RAM to be sent to the printer. When bit 09 = 0, the character in the character buffer is sent to the printer, provided that INT (bit 11) is not asserted.

Table 4-4 Translation RAM Bit Interpretation (Cont)

Bit	Name	Mode	Description
08	PI	R-W	Paper Instruction Bit. Setting bit 08 = 1 causes the printer to interpret the character received as a carriage control character (vertical formatting instruction to the DAVFU) rather than as data to be printed. If translation is taking place (TRANS bit 09 is set, or DELHLD bit is set), the content of PI bit 08 is put onto the Paper Instruction line. If no translation is taking place, the PI signal is not asserted (except during DAVFU Load).
07–00	DATA BITS	R-W	Eight data bits comprise a byte. The byte can be either a printable character or a non-printable (control) character. The number of printable characters depends on the character set in use (see Appendices B and C).

Table 4-5 Permutations of LP20 Control Bits

Item	INT RAM 11	DEL RAM 10	TRANS RAM 09	PI RAM 08	INT ENB	DEL HLD[2,3]	
1	0	0	0	0	X[1]	0	Character from Character Buffer to printer[5]
2	0	0	0	0	X	1	RAM character to printer[5]
3	0	0	0	1	X	0	Same as item 1
4	0	0	0	1	X	1	RAM character to printer DAVFU for vertical format control
5	0	0	1	0	X	X	Same as item 2
6	0	0	1	1	X	X	Same as item 4
7	0	1	0	0	X	SET	Sets Delimiter Hold. RAM character to printer.[5]
8	0	1	0	1	X	SET	Sets Delimiter Hold. RAM character to printer DAVFU for vertical format control.
9	0	1	1	0	X	SET	Same as item 7
10	0	1	1	1	X	SET	Same as item 8
11	1	0	0	X	X[6]	X	Resets GO and interrupts.[6] The character causing the interrupt is in the Character Buffer.
12	1	0	1	0	X	0	Same as item 2
13	1	0	1	0	X[6]	1[7]	Same as item 11
14	1	0	1	1	X	0	Same as item 4
15	1	0	1	1	X[6]	1[7]	Same as item 11
16	1	1	X	X	X[6]	SET[7]	Same as item 11, and sets Delimiter Hold.

NOTES:

1. 1 = High, 0 = Low, X = Don't Care

2. DEL HLD being set forces translation regardless of the state of the TRANS bit. Both the delimiter character and following characters are translated (taken from RAM data rather than the Character Buffer).

3. DEL HLD is always cleared on the character following the delimiter character.

4. If this bit is not set, and the controller would do an interrupt if it were, the controller halts and waits until the bit is set. The interrupt then occurs.

5. Unless the character is ASCII 000 which is the "no action" character (nothing is sent to the printer).

6. The controller will halt and then wait for Interrupt Enable to be set. When INT ENB is set, an interrupt will occur. UND CHAR flag is raised.

7. The purpose of micro-coding for INT and TRANS bits is to conform to ASCII escape sequence standard: a character will cause an interrupt only if character was preceded by an escape (delimiter) character.

Once the DAVFU memory load has been completed, DAVFU instructions are transmitted to the printer by asserting the paper instruction (PI) bit at the same time that coded instructions are presented on the data lines (Tables 4-6 and 4-7). By holding data line 5 (data bit D04) high or low, the printer will slew a specified number of lines or will select a particular (tape) channel under program control, respectively. Pressing the TOP OF FORM button on the line printer and receipt of the ASCII character form feed (014_8) have the effect of slewing paper until a partition with a 1 stored in channel 1 is encountered. Channel 1 must be loaded with Top-of-Form to make the page counter and the TOP OF FORM button work properly. Channel 12 is reserved for Bottom-of-Form and must be loaded as such. To do otherwise may not allow the printer to print to the bottom of the last form.

During normal operation, each DAVFU partition is checked for odd parity. If a parity error is detected, or if the channel selected from the DAVFU has no stop bit, or if a tape channel greater than 12 is selected, FORMAT and TAPE fault lights will light, and the printer will complete the current line with a CR and negate the DAVFU RDY and ON-LINE signals.

The controller page counter is decremented by the Top-of-Form signal each time the DAVFU encounters a 1 in channel 1. The counter decrements on the rising edge of the Top-of-Form signal so that, if the DAVFU contains a 1 in channel 1 at the current paper position and the page counter is loaded, the counter will not decrement until the next time a 1 is encountered in channel 1. The PAGE ZERO flag is set on the falling edge (when the paper moves from the Top-of-Form position) of DAVFU channel 1. An example of DAVFU load versatility is presented in Table 4-8.

Once the DAVFU has been loaded, the paper can be manually stepped to a position corresponding to the beginning of the form and a single stop code (357_8) transmitted to the printer. This has the effect of synchronizing the memory with respect to the current line position of the paper so that it becomes the new Top-of-Form. The FORMS LENGTH switch controls the number of lines stepped when the DAVFU is not ready. If the FORMS LENGTH switch is disconnected, a default paper motion will occur. If the DAVFU is ready it will always assume control of paper motion regardless of the position of the FORMS LENGTH switch.

An error exists if:

1. A Channel Select or Lines Stepped (slew) code is received before a DAVFU memory load operation has been initiated.

2. A stop code is received after an odd number of data bytes (i.e., after only the first byte of a pair has been received).

3. A Channel Select code is received and that channel contains no channel stop.

4. A parity discrepancy is detected at any time during a DAVFU memory load or Channel Select operation.

5. A Channel Select for a non-existent channel is received.

When an error is detected:

1. The FORMAT and TAPE fault indicators will light, and the printer will go off-line.

2. DEMAND will be negated and a print cycle will be forced in order to print any data that may be in the printer buffer. No paper motion will occur.

3. The DAVFU RDY signal will be negated and will not be reasserted until a new DAVFU memory load has been completed.

Table 4-6 Vertical Format Instruction – Data Code is Used to Control Duration of Slew (DAVFU or Optical VFU)

	Data Bits								
PI Line	D07	D06	D05	D04	D03	D02	D01	D00	Number of Lines Slewed
1	X	X	X	1	0	0	0	0	0
1	X	X	X	1	0	0	0	1	1
1	X	X	X	1	0	0	1	0	2
1	X	X	X	1	0	0	1	1	3
1	X	X	X	1	0	1	0	0	4
1	X	X	X	1	0	1	0	1	5
1	X	X	X	1	0	1	1	0	6
1	X	X	X	1	0	1	1	1	7
1	X	X	X	1	1	0	0	0	8
1	X	X	X	1	1	0	0	1	9
1	X	X	X	1	1	0	1	0	10
1	X	X	X	1	1	0	1	1	11
1	X	X	X	1	1	1	0	0	12
1	X	X	X	1	1	1	0	1	13
1	X	X	X	1	1	1	1	0	14
1	X	X	X	1	1	1	1	1	15

Note: X means the bit can be either 0 or 1.

Table 4-7 Vertical Format Instruction – DAVFU is Used to Control Duration of Slew (DAVFU or Optical VFU)

	Data Lines								
PI Line	D07	D06	D05	D04	D03	D02	D01	D00	Selected Channel
1	X	X	X	0	0	0	0	0	1
1	X	X	X	0	0	0	0	1	2
1	X	X	X	0	0	0	1	0	3
1	X	X	X	0	0	0	1	1	4
1	X	X	X	0	0	1	0	0	5
1	X	X	X	0	0	1	0	1	6
1	X	X	X	0	0	1	1	0	7
1	X	X	X	0	0	1	1	1	8
1	X	X	X	0	1	0	0	0	9
1	X	X	X	0	1	0	0	1	10
1	X	X	X	0	1	0	1	0	11
1	X	X	X	0	1	0	1	1	12

Note: X means the bit can be either 0 or 1.

Table 4-8 Example of DAVFU Load

Tape Line	Equivalent Paper Tape Channel												DAVFU (Binary)	DAVFU (Octal)
	1	2	3	4	5	6	7	8	9	10	11	12	76543210	
						(Start Code)							11101110	356
1	*												00000001	001
													00000000	000
2													00000000	000
													00000000	000
3		*											00000010	002
													00000000	000
4			*										00000100	004
													00000000	000
5				*									00001000	010
													00000000	000
6					*								00010000	020
													00000000	000
7						*							00100000	040
													00000000	000
8							*						00000000	000
													00000001	001
9								*					00000000	000
													00000010	002
10									*				00000000	000
													00000100	004
11										*			00000000	000
													00001000	010
12											*		00000000	000
													00010000	020
13													00000000	000
													00000000	000
14		*	*	*	*	*	*	*	*	*	*		00111110	076
													00011111	037
15			*										00000100	004
													00000000	000
16		*	*	*				*	*	*			00001110	016
													00001110	016
17					*	*							00110000	060
													00000000	000
18		*											00000010	002
													00000000	000
19			*	*									00001100	014
													00000000	000
20					*					*	*	*	00010000	020
													00111000	070
						(Stop Code)							11101111	357

4.6 LOCAL INITIALIZE

To initialize, or clear, the entire controller, deposit DATA08 = 1 into CSRA, as follows:

Address	775400 or 775420 (CSRA)
Data	DATA08 = 1

This has the same effect as a UBUS INIT signal.

4.7 ERROR RESET

To reset the error circuitry in the controller, deposit DATA09 = 1 in CSRA, as follows:

Address	775400 or 775420 (CSRA)
Data	DATA09 - 1

4.8 DATA MULTIPLEXER

The outputs of the eight controller registers are applied to the data multiplexer. Each output is capable of being selected and routed to the bus via the bus data transceivers. The 16-bit output of the data multiplexer is referred to as UDAT (15:00) in Figure 4-1.

4.8.1 Control and Status Register A (CSRA)

This is the primary status register of the controller and is byte-addressable. The outputs of five control flip-flops in CSRA are applied to the first register (D0) in the data multiplexer as bits 00, 01, 02, 03, and 06 (Table 4-2). Bits 04 and 05 of data multiplexer register D0 come from the bus address register and are labeled as BUS ADR16 and BUS ADR17. Bits 08 and 09 of data multiplexer register D0 are grounded. The other seven bits of data multiplexer register D0 come from various circuits throughout the controller, as indicated in Table 4-2.

4.8.2 Control and Status Register B (CSRB)

This is the secondary status register of the controller and is byte-addressable. It contains logic for initiating tests of the controller and contains the individual error bits. Three test outputs of CSRB are applied to the second register (D1) of the data multiplexer; these are bits 08, 09, and 10. The other inputs to data multiplexer register D1 are delineated in Table 4-3.

4.8.3 Bus Address Register

This register is used in all modes of controller operation to specify the starting address of a particular data block in main memory. It is then incremented during the operational sequence. The 16 outputs of the bus address register are applied to the third register (D2) in the data multiplexer. The bus address register is word-addressable only. Bits 16 and 17 are read and written in CSRA.

4.8.4 Byte Counter

This counter is used in all modes of controller operation to keep track of all the data bytes applied to the controller from the bus. Like the bus address register, it is word-addressable only. The 12 outputs of the byte counter (11:00) are applied to the fourth register (D3) in the data multiplexer.

4.8.5 Page Counter

The page counter is a 12-bit register which is decremented each time a Top-of-Form signal is generated by the printer. All 12 outputs of this counter are applied to the fifth register (D4) in the data multiplexer. The page counter is word-addressable only.

4.8.6 RAM Data

The 13-bit output of the translation RAM is applied to the sixth register (D5) of the data multiplexer. The RAM is word-addressable only.

4.8.7 Character Buffer

All data inputs to the controller are applied to the character buffer, which is byte-addressable. This includes both printable and non-printable (control) characters. The 8-bit output of the character buffer, (07:00), is applied to both the checksum and the RAM address registers. The outputs of the RAM address register and the checksum are then applied to the seventh and eighth data multiplexer registers, D6 and D7, respectively. Note that the output of the RAM address register is the lower byte of data multiplexer register D6 and the checksum register forms the upper byte of D7.

4.8.8 Column Counter

The column counter is byte-addressable. Its function is to keep track of the characters being sent to the printer, up to the maximum line length of 132 characters. The output of this counter is the upper byte of data multiplexer register D6.

4.8.9 Checksum

This register is byte-addressable. Checksum is generated on all DMA data transfer operations including RAM Load and DAVFU Load. The checksum is calculated by adding each byte to a register which is initially set to zero when GO is set. The sum is stored for examination by the program. Any carry signals generated are ignored.

The program reads in the stored checksum calculated by the controller and compares it to the sum previously calculated by the program. On RAM Load transfers (two transfers per RAM word), the checksum is calculated on the low byte of the first, third, fifth, etc., transfers and the high byte of the second, fourth, sixth, etc., transfers of each RAM word.

The output of checksum is the high-order byte of the eighth register (D7) in the data multiplexer. Checksum is byte-addressable and read-only.

4.8.10 Printer Multiplexer

The printer multiplexer is byte-addressable. It contains the character that has just been sent to the printer taken at the point where the character enters the transmitters that drive the printer cable. The printer multiplexer is read-only. An attempt to write into it will not affect the registers in any way. Note that the controller automatically translates a horizontal tab into the appropriate number of spaces. When a tab is being performed (ASCII 011_8), the printer multiplexer will contain 040_8 (i.e., a space code). During the line overflow operation, the printer multiplexer will contain a line feed character (ASCII 012_8) before the 133rd character. The 133rd character becomes character 1 of the next line. The output of the printer multiplexer is the low byte of the eighth register (D7) in the data multiplexer.

4.9 ESCAPE SEQUENCE

By definition, an escape character is a control character for providing code extension (supplementary characters) in general information interchange. The escape character itself is a prefix affecting the interpretation of a limited number of contiguously following characters and, for this reason, is commonly called a "delimiter" character.

In the LP20 Controller, bit 10 of a translation RAM word is the delimiter (DEL) bit. When this bit is asserted, its associated DEL HOLD flip-flop is set, setting up the logic for an escape sequence.

Assume, for example, that RAM location 101_8 has its PI bit set, TRANS bit not set, and a Select Channel 2 code in its data bits. When the controller receives the letter "A" (101_8) and the DEL HOLD flip-flop has not been set, an "A" will be printed. On the other hand, if the DEL HOLD flip-flop has been set, thus forcing translation (whether by the previous character being a delimiter or by the program), then DAVFU vertical format channel 2 will be selected. This illustrates the dual relationship of the escape sequence.

4.10 ILLEGAL OR UNDEFINED CHARACTERS

The user has the option of loading any characters or control codes into the RAM. It is recommended that the 256 locations be loaded, even though every location is not used during the normal printing operation. If the unused locations are loaded with the INT bit set to 1 and the other RAM bits set to all 0s, then any illegal or undefined characters will stop the transfer and, if the CSRA interrupt enable (INT ENB) bit is set, cause the controller to generate a bus request (UBUS BR4) interrupt to the processor instead of generating a data strobe to the line printer. The current character will not be sent to the printer, but rather will be held in the character buffer available for inspection by the processor. Also, the Undefined Character (UNDCHAR) flag will be set (bit 13 of the data multiplexer register associated with CSRA).

The checksum adds each incoming character, even if it is an illegal or undefined character (as defined previous to loading the RAM).

4.11 MEMORY PARITY

Memory parity errors can only occur when the controller is master and main memory is slave (i.e., during NPR data transfers). Main memory signals an error by holding PA low and PB high. When an error is detected, the controller sets the MEM PAR ERR and ERROR bits, halts operation, and requests an interrupt.

4.12 RAM PARITY

RAM parity is generated on all transfers which load the translation RAM (i.e., either discrete loading or DMA loading). Parity is calculated on the low-order 12 bits of the data word, DATA (11:00). RAM parity is checked for all operations that require a character to be read from the RAM (i.e., DMA data transfer). This is done by recalculating parity on the 12 RAM bits, RAM DAT (11:00), and comparing it with the parity bit previously stored in the RAM (RAM DAT12). When an error is detected, the controller sets the RAM PAR ERR and ERROR bits, halts operation, and requests an interrupt if INT ENB is set.

4.13 PROGRAMMING EXAMPLE

Table 4-9 contains a sample program for initializing the LP20 Controller, loading the RAM, loading the DAVFU, printing the numbers 0 through 9 and letters of the alphabet on one line, and performing special functions such as checking delimiter operation, checking RAM translation, checking a paper instruction, and checking a RAM interrupt.

Table 4-9 LP20 Sample Program

```
LPSAMP.TXT      MACY11 27(654)  9-DEC-75  13:51  PAGE 1
LPSAMP.TXT


                                        .TITLE  LPSAMP.TXT
                                                .ENABL AMA,ABS

                                ;CREATED BY ROY FULTON (NOV. 4,1975)
                                ;THIS IS A SAMPLE PROGRAM THAT WILL PRINT A LINE ON THE LP20 PRINTER.
                                ;THIS ROUTINE DOES THE FOLLOWING
                                ;       1)  LOADS THE RAM FROM RAMBUF(A BUFFER IN MEMORY)
                                ;       2)  LOADS THE PRINTER VFU (FROM A BUFFER IN MEMORY)
                                ;       3)  PRINTS DATBUF ON THE PRINTER(DATBUF IS A BUFFER IN MEMORY)
                                ;
                                ;THE LINE THAT WILL BE PRINTED IS AS FOLLOWS
                                ;       0123456789ABCDEFGHIJKLMNOPQRSTUVWXYZ
                                ;
                                ;START PROGRAM AT LOCATION 001000
                                ;


000000                                  R0=%0
000001                                  R1=%1
000002                                  R2=%2
000003                                  R3=%3
000004                                  R4=%4
000005                                  R5=%5
000006                                  R6=SP
000007                                  R7=PC
000006                                  SP=%6
000007                                  PC=%7

000754                                  LPVEC=754
175400                                  LPCSRA=175400
175402                                  LPCSRB=LPCSRA+2
175404                                  LPBSAD=LPCSRA+4
175406                                  LPBCTR=LPCSRA+6
175410                                  LPPCTR=LPCSRA+10
175412                                  LPRAMD=LPCSRA+12
175414                                  LPCBUF=LPCSRA+14
175415                                  LPCCTR=LPCSRA+15
175416                                  LPCKSM=LPCSRA+16
175417                                  LPPDAT=LPCSRA+17
000010                                  PAGES=10

001000                                  RAMSIZ=1000
000206                                  VFUSIZ=206
000046                                  DATSIZ=46
```

Table 4-9 LP20 Sample Program (Cont)

```
LPSAMP.TXT      MACY11 27(654)  9-DEC-75  13:51  PAGE 2
LPSAMP.TXT


                001000                          .=1000

001000  012706  001000          INITI:  MOV #INIT,SP
001004  112737  000003  175401          MOVB #3,LPCSRA+1        ;CLR LP20
001012  012737  001200  000754          MOV #INTR,LPVEC         ;SETUP INTERRUPT CATCHER
001020  005037  000756                  CLR LPVEC+2
001024  032737  004000  175400          BIT #004000,LPCSRA      ;IS PRINTER ONLINE
001032  001003                          BNE RAMSET              ;BRANCH IF ONLINE
001034  000000                          HALT                    ;PRINTER IS OFFLINE, PLACE ONLINE AND
                                                                ;PRESS CONTINUE ON PDP-11 CONSOLE
001036  000137  001000                  JMP INIT                ;TRY AGAIN
001042  012737  002000  175404  RAMSET: MOV #RAMBUF,LPBSAD      ;SETUP BUS ADDRESS TO FIRST WORD OF BUFFER
001050  012737  001000  175406          MOV #RAMSIZ,LPBCTR      ;SET BYTCTR TO NO. OF WORDS
001056  005437  175406                  NEG LPBCTR              ;CHANGE TO TWOS COMPLEMENT
001062  012737  000116  175400          MOV #116,LPCSRA         ;SETUP FOR RAM LOAD (DMA MODE)WITH INT,ENB, SET
001070  105237  175400                  INCB LPCSRA             ;SET GO
001074  000001                          WAIT                    ;WAIT FOR INTERRUPT ON DONE
001076  112737  000003  175401          MOVB #3,LPCSRA+1        ;CLR LP20 SINCE WE ARE LEAVING TEST MODE
001104  012737  003000  175404  VFULOD: MOV #VFUBUF,LPBSAD      ;SETUP BUSADD TO START OF VFU BUFFER
001112  012737  000206  175406          MOV #VFUSIZ,LPBCTR      ;SETUP BYTECTR TO NO. OF BYTES
001120  005437  175406                  NEG LPBCTR              ;CHANGE TO TWOS COMPLEMENT
001124  012737  000113  175400          MOV #113,LPCSRA         ;DO DAVFU LOAD,WITH INT,ENB, SET
001132  000001                          WAIT                    ;WAIT FOR DONE INTERRUPT
001134  012737  004000  175404  PRINT:  MOV #DATBUF,LPBSAD      ;SETUP BUSSADD TO START OF BUFFER
001142  012737  000046  175406          MOV #DATSIZ,LPBCTR      ;SETUP BYTCTR TO NO. OF BYTES
001150  005437  175406                  NEG LPBCTR              ;CHANGE TO TWOS COMPLEMENT
001154  012737  000010  175410          MOV #PAGES,LPPCTR       ;SETUP PAGE COUNTER
001162  012737  000101  175400  CONTIN: MOV #101,LPCSRA         ;PRINT WITH INT, ENAB, SET
001170  000001                          WAIT                    ;WAIT FOR INTERRUPT
001172  000000                          HALT                    ;STOP HERE IF PRINTING COMPLETE
                                                                ;PLACE NOP (240) HERE IF YOU WANT TO LOOP
001174  000137  001000                  JMP INIT                ;PRESS CONTINUE TO PRINT AGAIN
001200  032737  160200  175400  INTR:  BIT #160200,LPCSRA       ;TEST FOR DONE,ERROR,UNDCHR,OR PAGZRO
001206  001001                          BNE 5$                  ;BRANCH IF ONE OF THESE SET
001210  000000                          HALT                    ;UNDEFINED INTERRUPT
001212  032737  020000  175400  5$:     BIT #020000,LPCSRA      ;IS UNDCHR BIT SET?
001220  001404                          BEQ 1$                  ;CONTINUE IF NOT
001222  000000                  3$:     HALT                    ;UNDCHR INTERRUPT
001224  022626                          CMP (SP)+,(SP)+         ;FIX STACK POINTER
001226  000137  001162                  JMP CONTIN              ;CONTINUE PRINTING
001232  032737  140000  175400  1$:     BIT #140000,LPCSRA      ;IS ERROR OR PAGZRO SET
001240  001401                          BEQ 2$                  ;BRANCH IF NOT(DONE WAS SET)
001242  000000                          HALT                    ;ERROR OR PAGZRO SET
001244  000002                  2$:     RTI                     ;RETURN
```

Table 4-9 LP20 Sample Program (Cont)

```
LPSAMP.TXT      MACY11 27(654)  9-DEC-75  13:51  PAGE 3
LPSAMP.TXT


    96
    97
    98          002000                              .=2000
    99
   100
   101  002000  004000  004000  004000  RAMBUF: .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002006  004000  004000  004000
        002014  004000  004000
   102  002020  004000  004000  000000          .WORD   4000,4000,0000,4000,4000,0000,4000,4000
        002026  004000  004000  000000
        002034  004000  004000
   103  002040  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002046  004000  004000  004000
        002054  004000  004000
   104  002060  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002066  004000  004000  004000
        002074  004000  004000
   105  002100  000000  000000  000000          .WORD   0000,0000,0000,0000,0000,0000,0000,0000
        002106  000000  000000  000000
        002114  000000  000000
   106  002120  000000  000000  000000          .WORD   0000,0000,0000,0000,0000,0000,0000,0000
        002126  000000  000000  000000
        002134  000000  000000
   107  002140  000000  000000  000000          .WORD   0000,0000,0000,0000,0000,0000,0000,0000
        002146  000000  000000  000000
        002154  000000  000000
   108  002160  000000  000000  000000          .WORD   0000,0000,0000,0000,0000,0000,0000,0000
        002166  000000  000000  000000
        002174  000000  000000
   109  002200  000000  000000  000000          .WORD   0000,0000,0000,0000,0000,0000,0000,0000
        002206  000000  000000  000000
        002214  000000  000000
   110  002220  000000  000000  000000          .WORD   0000,0000,0000,0000,0000,0000,0000,0000
        002226  000000  000000  000000
        002234  000000  000000
   111  002240  000000  000000  000000          .WORD   0000,0000,0000,0000,0000,0000,0000,0000
        002246  000000  000000  000000
        002254  000000  000000
   112  002260  000000  000000  000000          .WORD   0000,0000,0000,0000,0000,0000,0000,0000
        002266  000000  000000  000000
        002274  000000  000000
   113  002300  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002306  004000  004000  004000
        002314  004000  004000
   114  002320  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002326  004000  004000  004000
        002334  004000  004000
   115  002340  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002346  004000  004000  004000
        002354  004000  004000
   116  002360  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002366  004000  004000  004000
        002374  004000  004000
   117  002400  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
```

Table 4-9 LP20 Sample Program (Cont)

```
LP8AMP.TXT      MACY11 27(654)  9-DEC-75  13:51  PAGE 3-1
LP8AMP.TXT

        002406  004000  004000  004000
        002414  004000  004000
   118  002420  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002426  004000  004000  004000
        002434  004000  004000
   119  002440  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002446  004000  004000  004000
        002454  004000  004000
   120  002460  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002466  004000  004000  004000
        002474  004000  004000
   121  002500  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002506  004000  004000  004000
        002514  004000  004000
   122  002520  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002526  004000  004000  004000
        002534  004000  004000
   123  002540  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002546  004000  004000  004000
        002554  004000  004000
   124  002560  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002566  004000  004000  004000
        002574  004000  004000
   125  002600  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002606  004000  004000  004000
        002614  004000  004000
   126  002620  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002626  004000  004000  004000
        002634  004000  004000
   127  002640  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002646  004000  004000  004000
        002654  004000  004000
   128  002660  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002666  004000  004000  004000
        002674  004000  004000
   129  002700  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002706  004000  004000  004000
        002714  004000  004000
   130  002720  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002726  004000  004000  004000
        002734  004000  004000
   131  002740  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002746  004000  004000  004000
        002754  004000  004000
   132  002760  004000  004000  004000          .WORD   4000,4000,4000,4000,4000,4000,4000,4000
        002766  004000  004000  004000
        002774  004000  004000
   133
```

Table 4-9 LP20 Sample Program (Cont)

```
LPSAMP.TXT      MACY11 27(654)  9-DEC-75  13:51  PAGE 4
LPSAMP.TXT

  135            003000                          .=3000
  136
  137  003000     356                    VFUBUF: .BYTE   356
  138  003001     077      077     020            .BYTE   77,77,20,02,24,02,30,02
       003004     002      024     002
       003007     030      002
  139  003011     024      002     020            .BYTE   24,02,20,06,34,02,20,02
       003014     006      034     002
       003017     020      002
  140  003021     024      002     030            .BYTE   24,02,30,02,64,06,20,02
       003024     002      064     006
       003027     020      002
  141  003031     034      002     020            .BYTE   34,02,20,02,24,02,30,16
       003034     002      024     002
       003037     030      016
  142  003041     024      002     020            .BYTE   24,02,20,02,34,02,20,02
       003044     002      034     002
       003047     020      002
  143  003051     064      017     030            .BYTE   64,17,30,02,24,02,20,02
       003054     002      024     002
       003057     020      002
  144  003061     034      002     020            .BYTE   34,02,20,26,24,02,30,02
       003064     026      024     002
       003067     030      002
  145  003071     024      002     020            .BYTE   24,02,20,02,76,16,20,02
       003074     002      076     016
       003077     020      002
  146  003101     024      002     030            .BYTE   24,02,30,02,24,02,20,06
       003104     002      024     002
       003107     020      006
  147  003111     034      002     020            .BYTE   34,02,20,02,24,02,30,02
       003114     002      024     002
       003117     030      002
  148  003121     064      047     020            .BYTE   64,47,20,02,34,02,20,02
       003124     002      034     002
       003127     020      002
  149  003131     024      002     030            .BYTE   24,02,30,16,24,02,20,02
       003134     016      024     002
       003137     020      002
  150  003141     034      002     020            .BYTE   34,02,20,02,64,26,30,02
       003144     002      064     026
       003147     030      002
  151  003151     024      002     020            .BYTE   24,02,20,02,34,02,20,06
       003154     002      034     002
       003157     020      006
  152  003161     024      002     030            .BYTE   24,02,30,02,24,02,20,02
       003164     002      024     002
       003167     020      002
  153  003171     020      000     020            .BYTE   20,00,20,00,20,00,20,00
       003174     000      020     000
       003177     020      000
  154  003201     020      000     020            .BYTE   20,00,20,00
       003204     000
  155  003205     357                             .BYTE   357

  156
  157
```

Table 4-9 LP20 Sample Program (Cont)

```
LPSAMP.TXT      MACY11 27(654)  9-DEC-75  13:51  PAGE 5
LPSAMP.TXT


  159
  160
  161           004000                          .=4000
  162
  163  004000  030460  031462  032464  DATBUF: .ASCII  /0123456789ABCDEFGHIJKLMNOPQRSTUVWXYZ/
       004006  033466  034470  041101
       004014  042103  043105  044107
       004022  045111  046113  047115
       004030  050117  051121  052123
       004036  053125  054127  055131
  164  004044     015     012                  .BYTE   15,12
```

Table 4-9 LP20 Sample Program (Cont)

```
LPSAMP.TXT      MACY11 27(654)  9-DEC-75  13:51  PAGE 6
LPSAMP.TXT


                                ;TO CHECK DELIMITER OPERATION CHANGE
                                ;       LOC 2202 (A) TO 2057
                                ;       LOC 2204 (B) TO 0012
                                ;THE PROGRAM SHOULD THEN PRINT THE FOLLOWING
                                ;
                                ;       0123456789/
                                ;       CDEFGHIJKLMNOPQRSTUVWXYZ
                                ;
                                ;
                                ;TO CHECK RAM TRANSLATION CHANGE
                                ;       LOC 2202 (A) TO 1102
                                ;       LOC 2204 (B) TO 1012
                                ;THE PROGRAM SHOULD NOW PRINT THE FOLLOWING
                                ;
                                ;       01234567898
                                ;       CDEFGHIJKLMNOPQRSTUVWXYZ
                                ;
                                ;
                                ;TO CHECK A PAPER INSTRUCTION TRANSLATION CHANGE
                                ;       LOC 2202 (A) TO 1400
                                ;       LOC 2204 (B) TO 0000
                                ;THE PROGRAM SHOULD THEN PRINT THE FOLLOWING
                                ;
                                ;       0123456789      (THEN MOVE PAPER TO TOP OF FORM)
                                ;       BCDEFGHI;KLMNOPQRSTUVWXYZ
                                ;
                                ;
                                ;TO CHECK RAM INTERRUPT CHANGE
                                ;       LOC 2202 (A) TO 4000
                                ;       LOC 2204 (B) TO 0000
                                ;THE PROGRAM SHOULD THEN HALT AT LOCATION 38.  IF YOU PRESS CONTINUE
                                ;ON THE CONSOLE THE FOLLOWING SHOULD BE PRINTED.
                                ;
                                ;       0123456789BCDEFGHIJKLMNOPQRSTUVWXYZ
                                ;
                                ;


        000001                          .END

CONTIN  001162          DATBUF  004000          DATSIZ= 000046          INIT    001000
INTR    001200          LPBCTR= 175406          LPBSAD= 175404          LPCBUF= 175414
LPCCTR= 175415          LPCKSM= 175416          LPCSRA= 175400          LPCSRB= 175402
LPPCTR= 175410          LPPDAT= 175417          LPRAMD= 175412          LPVEC = 000754
PAGES = 000010          PC      =%000007        PRINT   001134          RAMBUF  002000
RAMSET  001042          RAMSIZ= 001000          R0      =%000000        R1      =%000001
R2      =%000002        R3      =%000003        R4      =%000004        R5      =%000005
R6      =%000006        R7      =%000007        SP      =%000006        VFUBUF  003000
VFULOD  001104          VFUSIZ= 000206          .       = 004046


 ERRORS DETECTED:  0
```

CHAPTER 5
TECHNICAL DESCRIPTION

5.1 INTRODUCTION

This chapter contains the detailed theory of operation of the LP20 Controller; it also describes controller interfacing to the Unibus and the line printer.

5.2 GENERAL INFORMATION

5.2.1 Logic Diagrams

Figure 5-1 is a detailed block diagram of the LP20 Controller. Individual logic diagrams, contained in the LP20 Field Maintenance Print Set (MP00006), are listed in Table 5-1.

Table 5-1 List of Module Logic Diagrams for LP20 Controller

Module	Diagram Title
M8585	LP20 TRANSLATION RAM LPR1 Translation RAM LPR2 Bus Address Register LPR3 Power Pins
M8586	LP20 CONTROL LPC1 Address Select LPC2 Unibus Control LPC3 NPR Clock LPC4 Interrupt LPC5 RAM Parity LPC6 Status and Test LPC7 Error Status LPC8 UBUS Drivers LPC9 RAM Register Select LP10 Checksum LP11 Power Pins
M8587 or M8571	LP20 DATA PATHS LPD0 Switch Notes (M8571 only) LPD1 Printer Multiplexer LPD2 RAM Address LPD3 Data Multiplexer LPD4 Page Counter LPD5 Carriage Control LPD6 LPT Interface LPD7 UBUS and LPT Cable LPD8 Power Pins

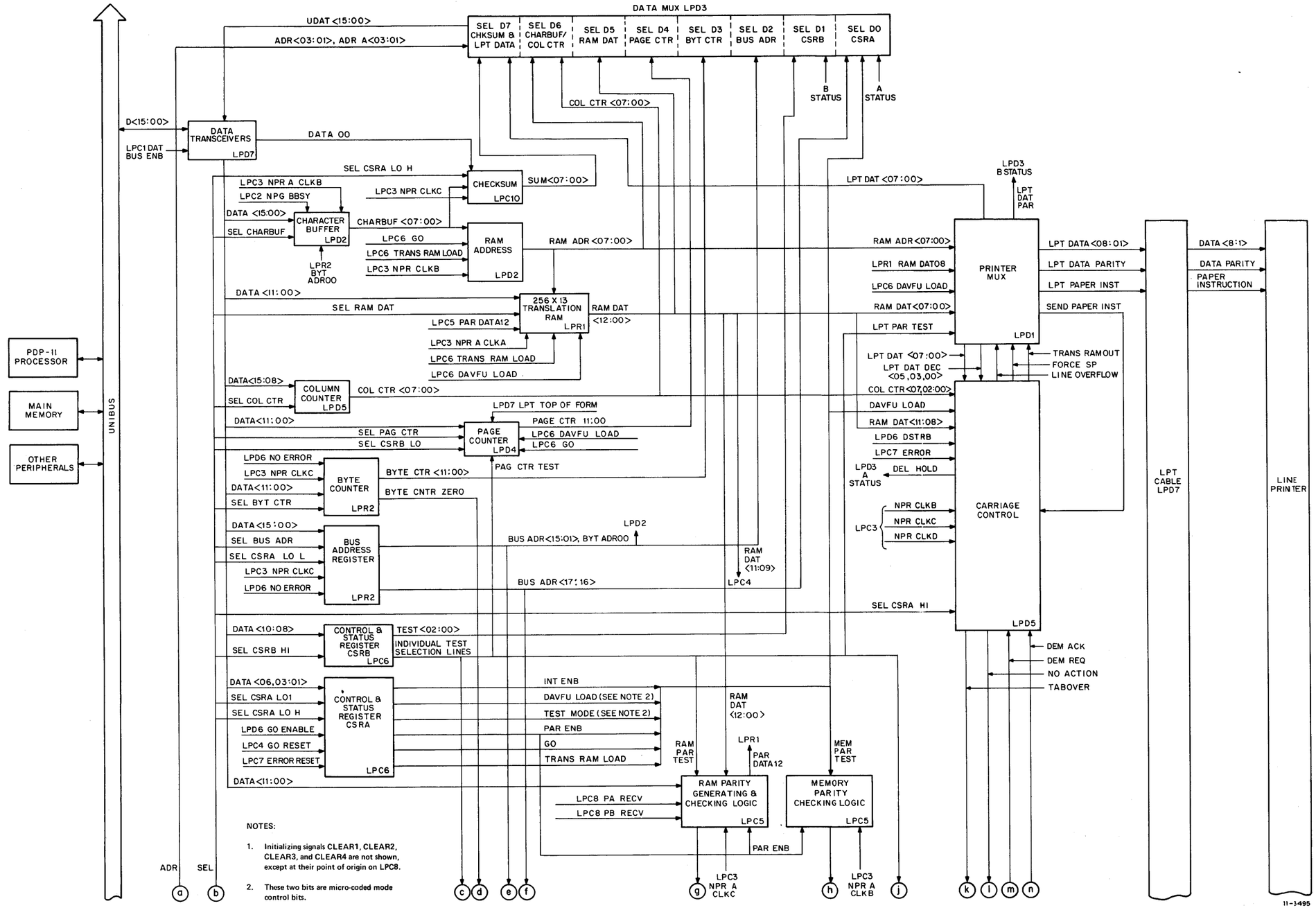
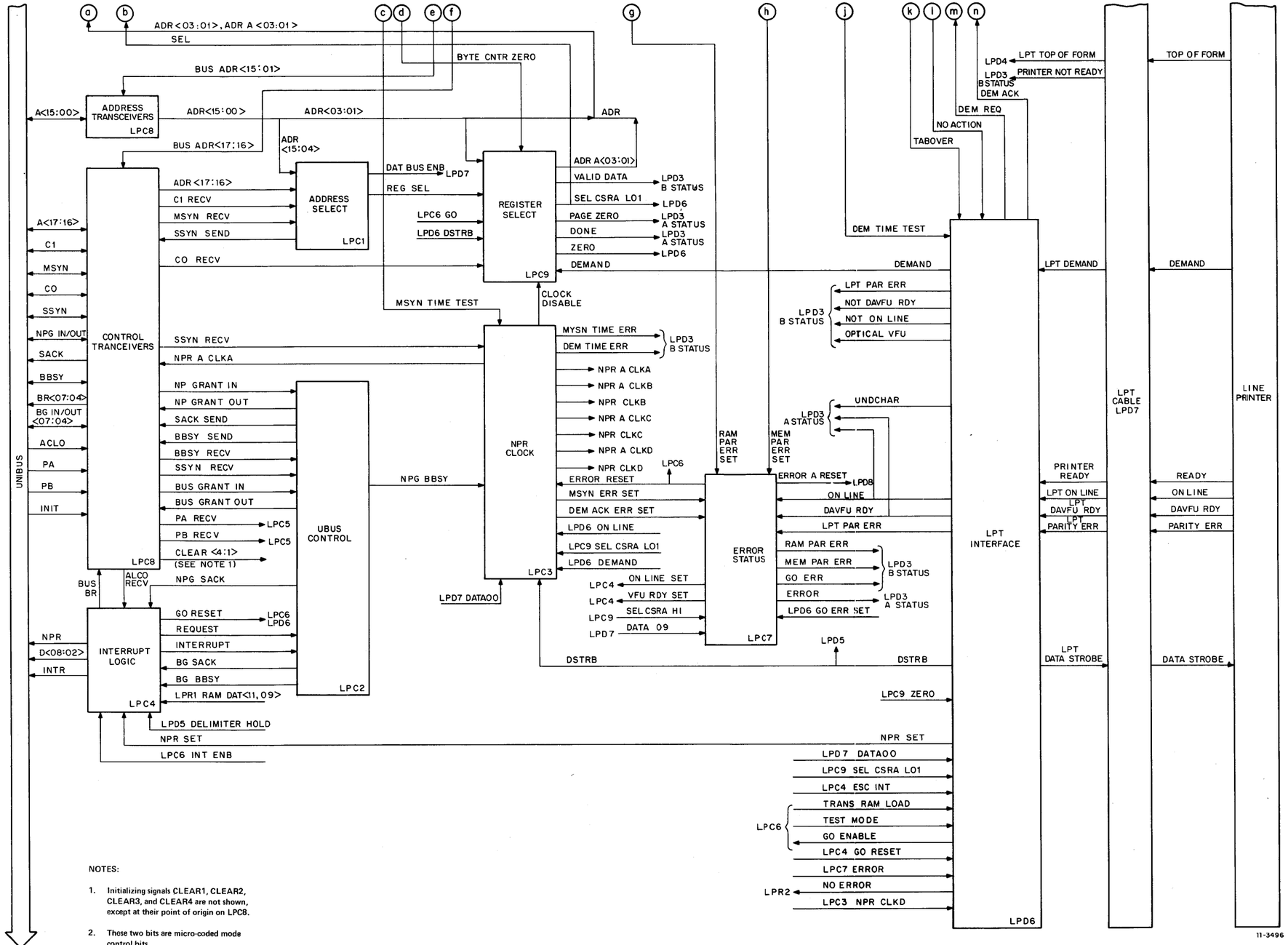


Figure 5-1 LP20 Controller Detailed Block Diagram (Sheet 1 of 2)



NOTES:

1. Initializing signals CLEAR1, CLEAR2, CLEAR3, and CLEAR4 are not shown, except at their point of origin on LPC8.
2. Those two bits are micro-coded mode control bits.

Figure 5-1 LP20 Controller Detailed Block Diagram (Sheet 2 of 2)

5.2.2 IC Complement

The integrated circuits (ICs) used on the three LP20 Controller logic modules are identified and described in Table 5-2.

Table 5-2 IC Complement in LP20 Controller

Type	Name
3106*	256-Bit RAM with 3-State Output
7400	Quadruple 2-Input Positive NAND Gates
7401	Quadruple 2-Input Positive NAND Gates with Open Collector Outputs
7402	Quadruple 2-Input Positive NOR Gates
7404	Hex Inverters
7408	Quadruple 2-Input Positive AND Gates
7410	Triple 2-Input Positive NAND Gates
7420	Dual 4-Input Positive NAND Gates
7427	Triple 3-Input Positive NOR Gates
7430	8-Input Positive NAND Gate
7442	BCD-to-Decimal Decoder
7483A	4-Bit Binary Full Adder
7485	4-Bit Magnitude Comparator
74123	Dual Monostable Multivibrator (One-Shot)
74151	8:1 Multiplexer (8 lines to 1 line)
74153	Dual 4:1 Multiplexer (4 lines to 1 line)
74174	Hex D Flip-Flops
74175	Quad D Flip-Flops
74193	Up/Down Binary Counter
74298	Quadruple 2:1 Multiplexers with Storage Flip-Flops
74H21	Dual 4-Input AND Gate
74H55	Expandable 2-Wide 4-Input AND-OR-INVERT Gate
74H74	Dual D Edge-Triggered Flip-Flop
74S74	Dual D Edge-Triggered Flip-Flop (High-Speed)
74S280	9-Bit Odd/Even Parity Generator/Checker
8641	Quad Unified Bus Transceivers
8815	Dual 4-Input NOR Gate
8820A	Dual Differential Line Receiver
8830	Dual Differential Line Driver
8881	Quadruple 2-Input NAND Gate

*Reference Type 74200

5.2.3 Printer Interface Signals
Descriptions of the printer interface signals are contained in Chapter 7 of this manual.

5.2.4 Unibus Interface Signals
Standard PDP-11 signals interface between the Unibus and the LP20 Controller. Detailed information on the function and timing of these signals is contained in the *PDP-11 Peripherals Handbook.*

5.2.5 PDP-11 Word Structure
The PDP-11 uses 16-bit words. These words start on even addresses. Each word is composed of two bytes of eight bits each. The lower order byte comprises bits 07 through 00 (bit 07 = MSB) and the higher order byte comprises bits 15 through 08 (bit 15 = MSB).

Each byte holds one ASCII character in files accessed by the LP20. Hence, two characters exist in each PDP-11 word. The bus address register contains the address of the next word in main memory to be accessed (bits 17 through 01), while the byte to be processed from that word is selected by bit 00.

5.3 DETAILED THEORY

5.3.1 Modes of Operation
Major signal paths between logic in the LP20 Controller are shown in Figure 5-1 (Sheets 1 and 2). The sequences in which these signals are asserted fall into the following categories:

1. Initialization
2. RAM Load
3. DAVFU Load
4. Print Mode
5. Test Mode

In the following sections, each of these categories is described in detail. A separate section covers error detection and error status reporting.

Throughout the discussion, reference is made to signals that are "high" or "low." By definition, "high" refers to a nominal dc voltage of +3 Vdc, and "low" refers to ground potential. All signals begin with the name of the print containing the signal source.

NOTE

Examples in this chapter pertain to line printer systems designated as LP20 No. 1. The detailed theory is the same for line printer systems designated as LP20 No. 2, except for address assignments.

5.3.2 System Power-Up Sequence
When the system POWER ON switch is activated, ac primary power is applied to the processor, which results in dc power being applied to the LP20 Controller. If the ac line voltage is within specification, then the controller signal LPC8 UBUS ACLO L is high. This permits the controller to issue bus interrupts and non-processor requests (NPRs).

5.3.3 Controller Initialization

When power is applied to the system, UBUS INIT is asserted for approximately 100 ms. In the controller, UBUS INIT causes the four lines labeled LPC8 CLEAR (4:1) L to go low, thereby initializing the various flip-flops, counters, registers, and other logic in the controller. Checksum bits and the Undefined Character (UNDCHAR) flag are not affected by the CLEAR (4:1) L signals, but are cleared each time the GO flip-flop is set.

NOTE

Initialization also occurs whenever the processor is halted and the processor START switch is depressed; a RESET instruction is executed; or there is a power fail sequence. It is also possible to clear the LP20 Controller alone by means of a Local Initialize command. In this case, initialization is accomplished by ANDing LPD7 DATA08 H and LPC9 SEL CSRA HI H to assert LPC8 CLEAR (4:1) L by writing a 1 into bit 08 of CSRA (address 175400).

5.3.4 Printer Power-Up Sequence

The printer is energized by placing the main power circuit breaker in the ON position. After a time delay, the printer POWER indicator illuminates, indicating that all printer dc voltages are within tolerance. If no fault conditions exist, the printer READY indicator illuminates.

Signal flow is as follows: The printer READY signal becomes LPD7 LPT READY H and is high. LPD7 PRINTER NOT READY H goes low (bit 13 of CSRB) and, at the same time, LPD7 PRINTER READY H goes high. Two bits indicate that the printer is off-line at this time: bit 07 in CSRB (-LPD6 ON LINE H is high) and bit 11 in CSRA (LPD6 ON LINE H is low).

5.3.5 Placing the Printer On-Line

When the operator presses the ON/OFF LINE pushbutton on the printer, the printer ON LINE signal becomes LPD7 LPT ON LINE H and is high. This signal is ANDed with LPD7 PRINTER READY H so that LPD6 ON LINE H (bit 11 of CSRA) is asserted and -LPD6 ON LINE H (bit 07 of CSRB) goes low.

The LPD6 ON LINE H signal triggers the ON LINE SET one-shot so that LPC7 ON LINE SET L goes low for 85 ns. This signal, in turn, asserts GO RESET L. GO RESET L sets the Interrupt flip-flop in LPC4 and clears the GO flip-flop in LPC6. Hence, an interrupt is executed if Interrupt Enable is set when the printer is put on-line.

If the printer goes off-line due to operator intervention or goes off-line (and not ready) due to an internal fault condition, the on-line signal LPD7 LPT ON LINE H is negated. This causes LPD6 ON LINE H to go low and trigger the ON LINE ERROR SET one-shot. This one-shot sets the Error flip-flop via LPC7 ERROR SET L. LPC7 ERROR SET L also sets the Interrupt flip-flop and clears GO by asserting LPC7 GO RESET.

5.3.6 Printer Demand

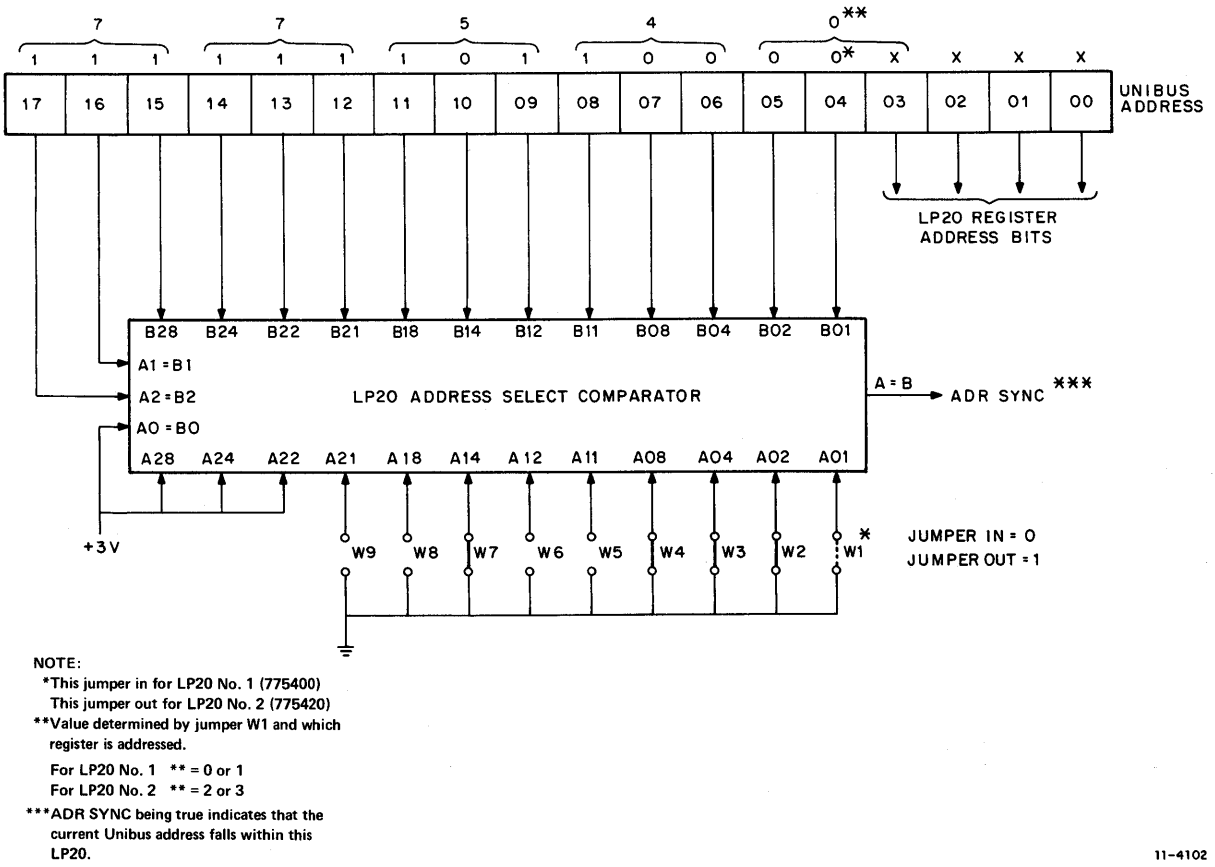
When the printer is ready and on-line, it will assert the printer DEMAND line. The printer DEMAND signal becomes LPD7 LPT DEMAND H and causes LPD6 PRINT DEMAND H to go high. The Test Mode flip-flop being reset allows LPD6 DEMAND H to go high, and LPC9 DONE H (bit 07 of CSRA) is asserted. This signifies that the printer is on-line and ready to receive data.

5.3.7 Reading and Writing Controller Registers

All registers in the controller are readable by the processor. The bus address lines are set up with the address of the desired register, and the C0 and C1 lines are configured for a DATI operation. When the controller receives UBUS MSYN (LPC8 MSYN REC H), the base address of the controller is compared with the current bus address and LPC1 ADR SYNC H becomes true if the base address bits match (Figure 5-2). This signifies that the current bus address resides in this LP20 Controller.

Since the C1 line is low for DATI operations, LPC1 DAT BUS ENB L is asserted. This signal causes the bus data lines to be driven by the transmitters in the UBUS data transceivers shown on LPD8. The data sent to the bus through these transceivers is selected by bus address bits 03, 02, and 01 and multiplexed by sixteen 8-line to 1-line multiplexers in LPD3. The data transceivers are disabled when MSYNC is removed. (This removes LPC1 DAT BUS ENB L.) Figure 5-3 shows which registers are byte-addressable.

All writable register bits are written by DATO or DATOB bus operations with the processor as bus master. When the processor desires to write into a register, the data for that register and the address of that register are placed on the bus data and address lines, respectively. The C0 and C1 lines are configured for a DATO or DATOB operation. When the controller receives MSYN (LPC8 MSYN REC H), the base address bits are compared, as previously described. However, in DATO and DATOB operations, C1 is asserted and LPC1 REG SEL L becomes low. This register select signal going low enables the decoder in LPC9 to select (write into) one of the eight registers. Upper or lower byte selection is controlled by bus address bit 00. If the operation is DATO, then both bytes are written via the C0 line being negated.



NOTE:
*This jumper in for LP20 No. 1 (775400)
This jumper out for LP20 No. 2 (775420)
**Value determined by jumper W1 and which register is addressed.
For LP20 No. 1 ** = 0 or 1
For LP20 No. 2 ** = 2 or 3
***ADR SYNC being true indicates that the current Unibus address falls within this LP20.

11-4102

Figure 5-2 LP20 Address Select Comparator

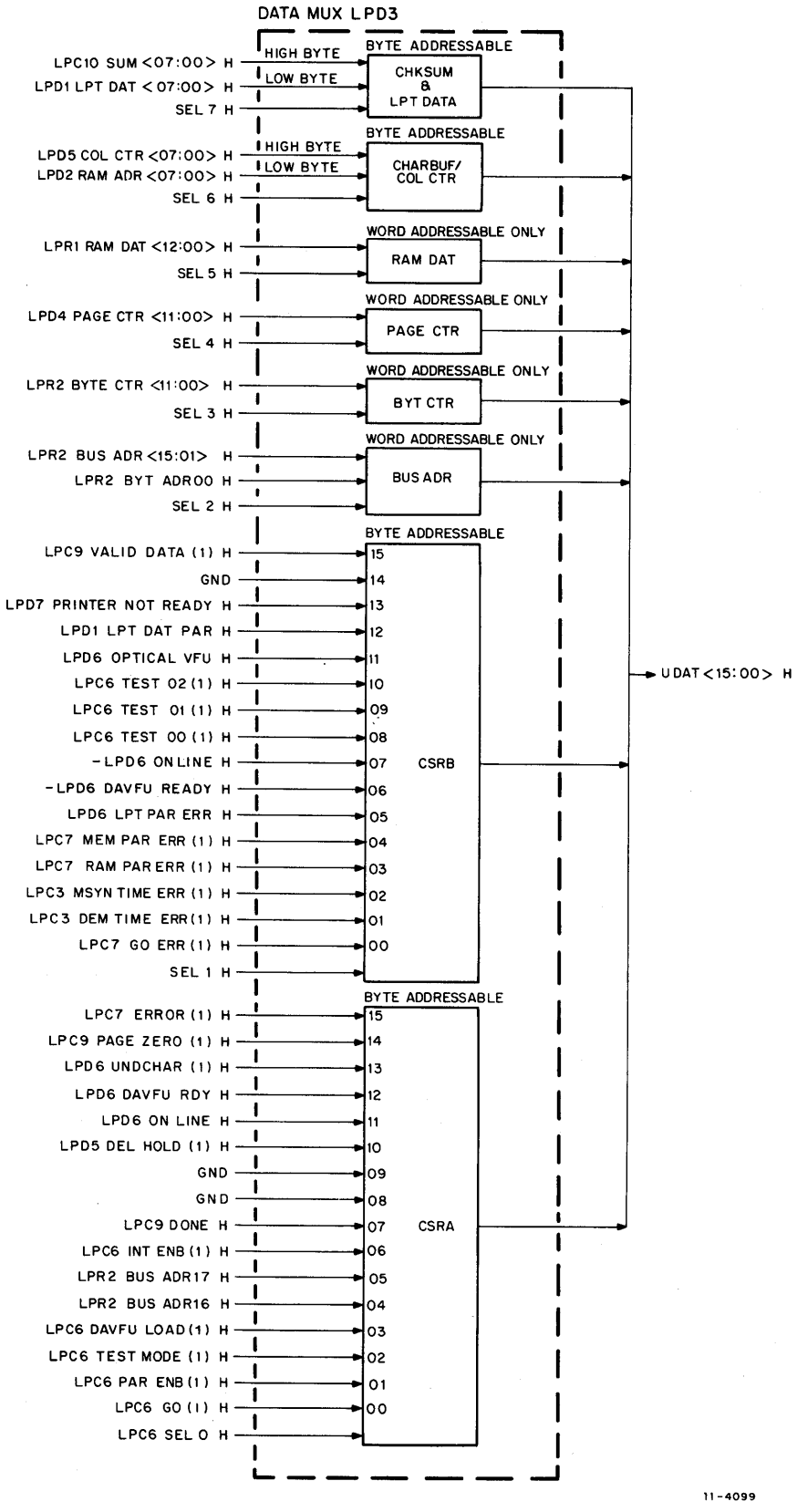


Figure 5-3 Addressable Registers

5.3.8 Non-Processor Request (NPR) Clock

All NPR cycles involve use of the internal clock in the LP20. This clock is turned on when the LP20 gains control of the Unibus and defines time states for processing fetched words in all modes of operation involving DMA.

The clock in the LP20 is built from a 200-ns one-shot and a 100-ns delay line. Each time the one-shot is triggered, a new clock state is entered by a particular state flip-flop being set. The triggering conditions are such that the first clock state is entered (NPR A CLKA) concurrently with UBUS MSYN being placed on the Unibus. The clock then stops and waits until UBUS SSYN is received from main memory. This action restarts the clock and completes the cycle through clock states NPR A CLKB, NPR A CLKC, and NPR A CLKD. The last three clock states direct the necessary internal controller functions for each DMA fetch. The clock halts after leaving the NPR A CLKD state.

Each time state is divided into two substates: NPR A CLK and NPR CLK. The NPR A CLK states come directly from the flip-flop outputs and are 300 ns wide (except NPR A CLKA). The NPR CLK states are true only when the CLOCK one-shot is triggered, and as such, start 200 ns before the end of the corresponding NPR A CLK state.

When LPC2 NPG BBSY (1) H goes high, the LPC3 200-ns CLOCK one-shot is triggered. When this one-shot times out, the NPR A CLKA flip-flop is set and master sync (UBUS MSYN) is asserted on the Unibus. The 25-μs LPC3 MSYN TIMEOUT one-shot is also triggered. If no slave sync is received within this 25-μs interval, an error condition (MSYN TIME ERR, bit 02 of CSRB) occurs and all DMA transfers are halted.

The zero output of the LPC3 NPR A CLKA flip-flop is used to gate off LPC2 NPG BBSY (1) H from the high input of the CLOCK one-shot, disabling it while MSYN is sent. The low input to that CLOCK one-shot goes low, enabling that input 100 ns after the LPC3 CLOCK one-shot times out. The one-shot does not trigger, however, because the true-high input is also low. The controller waits until UBUS SSYN is received before the clock is started again.

Consider the case where the request is received and processed properly, and there is no MSYN time-out error. (See Section 5.3.15.2 for the case where there is an error.) When LPC8 SSYN RECV H goes high, it forces the true-high input of the CLOCK one-shot high and the one-shot triggers. When the CLOCK one-shot times out, the NPR A CLKB flip-flop is set, the NPR A CLKA flip-flop is cleared, and the D input of the MSYN TIMEOUT flip-flop goes low, thereby inhibiting the MSYN time-out error circuitry. In addition, the high input of the LPC3 CLOCK one-shot is held high by LPC2 NPG BBSY (1) H and -NPR A CLKA H being asserted.

The low input of the CLOCK one-shot goes low, triggering the one-shot, 100 ns after the CLOCK one-shot times out. The signals CLOCK H and NPR A CLKB H are ANDed so that LPC3 NPR CLKB H and LPC3 NPR CLKB L are asserted. NPR A CLKB and NPR CLKB control operations involving the character buffer and RAM address register.

When the CLOCK one-shot times out, the NPR A CLKC flip-flop is set and the NPR A CLKB flip-flop is cleared. This causes LPC3 NPR A CLKB H, LPC3 NPR CLKB H, and LPC3 NPR CLKB L to all be negated. After 100 ns, LPC3 NPR CLKC is asserted when the one-shot is retriggered, as discussed previously. NPR CLKC is used to increment the bus address register and the byte counter, to control certain character translation operations, and to update the checksum register. When the CLOCK one-shot times out, the NPR A CLKD flip-flop is set and the NPR A CLKC flip-flop is cleared.

The one-shot is triggered again 100 ns later, and LPC3 NPR CLKD H and LPC3 NPR CLKD L are asserted. When LPC3 NPR CLKD L goes low, the LPC2 NPG BBSY flip-flop is cleared. Any bus interrupts also occur during the NPR CLKD time-state and Data Strobe is asserted on the trailing edge of NPR CLKD.

At the end of NPR CLKD, the one-shot times out and the NPR cycle is completed. The signal LPC3 CLOCK DISABLE L goes high to set up for the next NPR clock cycle.

Exact signals and functions for each clock state are discussed in more detail in sections on specific modes of operation of the LP20.

5.3.9 Interrupts

When conditions are such that the LP20 does a bus interrupt, the following chain of events takes place to transfer the LP20 vector address to the processor (Figure 5-4).

If LPC7 INTERRUPT ENABLE (1) H is true and the Interrupt flip-flop is set, LPC4 BUS BR L is sent out to the Unibus as UBUS BR4 L. When the processor responds to the interrupt request, LPC8 UBUS BG4 IN H and LPC8 BUS BG IN H go high. This causes LPC8 BUS GRANT IN L to be asserted.

NOTE

If the LP20 UBUS BR4 is not asserted, and if the LPC2 Bus Grant Out flip-flop is cleared, then an incoming BUS GRANT IN signal will cause BUS GRANT OUT L to go low. This signal will be routed to LPC8 and onto the bus as UBUS BG4 OUT H.

The LPC2 BG SACK flip-flop is set 100 ns after LPC8 BUS GRANT IN is received from the processor. When LPC2 BG SACK (0) H goes low, the LPC4 Interrupt flip-flop is cleared; this negates LPC4 BUS BR L and LPC8 UBUS BR4 L. LPC2 BG SACK (1) H going high forces LPC2 SACK SEND H high and LPC8 UBUS SACK L low. The latter signal acknowledges receipt of the bus grant.

The processor responds to UBUS SACK L by removing UBUS BG4 IN and hence LPC8 BUS GRANT IN L goes high.

When LPC8 BUS GRANT IN L goes high and the bus is idle, the LPC2 BG BBSY flip-flop is set, LPC2 BBSY SEND H goes high, and the BG SACK flip-flop is cleared. LPC2 BBSY SEND H causes UBUS BBSY to be asserted on the Unibus.

When LPC2 BG BBSY (1) H goes high, the LPC4 UBUS INTR line and the appropriate LPC4 UBUS D (08:02) lines are asserted low, depending on the vector address. For LP20 Printer System No. 1, the vector address is 754_8. The vector address specifies the memory location that contains the starting address of the device routine.

The processor responds to UBUS BBSY by asserting UBUS SSYN and LPC8 SSYN RECV H goes high. The LPC2 BG BBSY flip-flop is then cleared and LPC2 BBSY SEND H is negated. When LPC8 UBUS BBSY L goes high, the processor responds to it by removing UBUS SSYN. This returns control to the service routine.

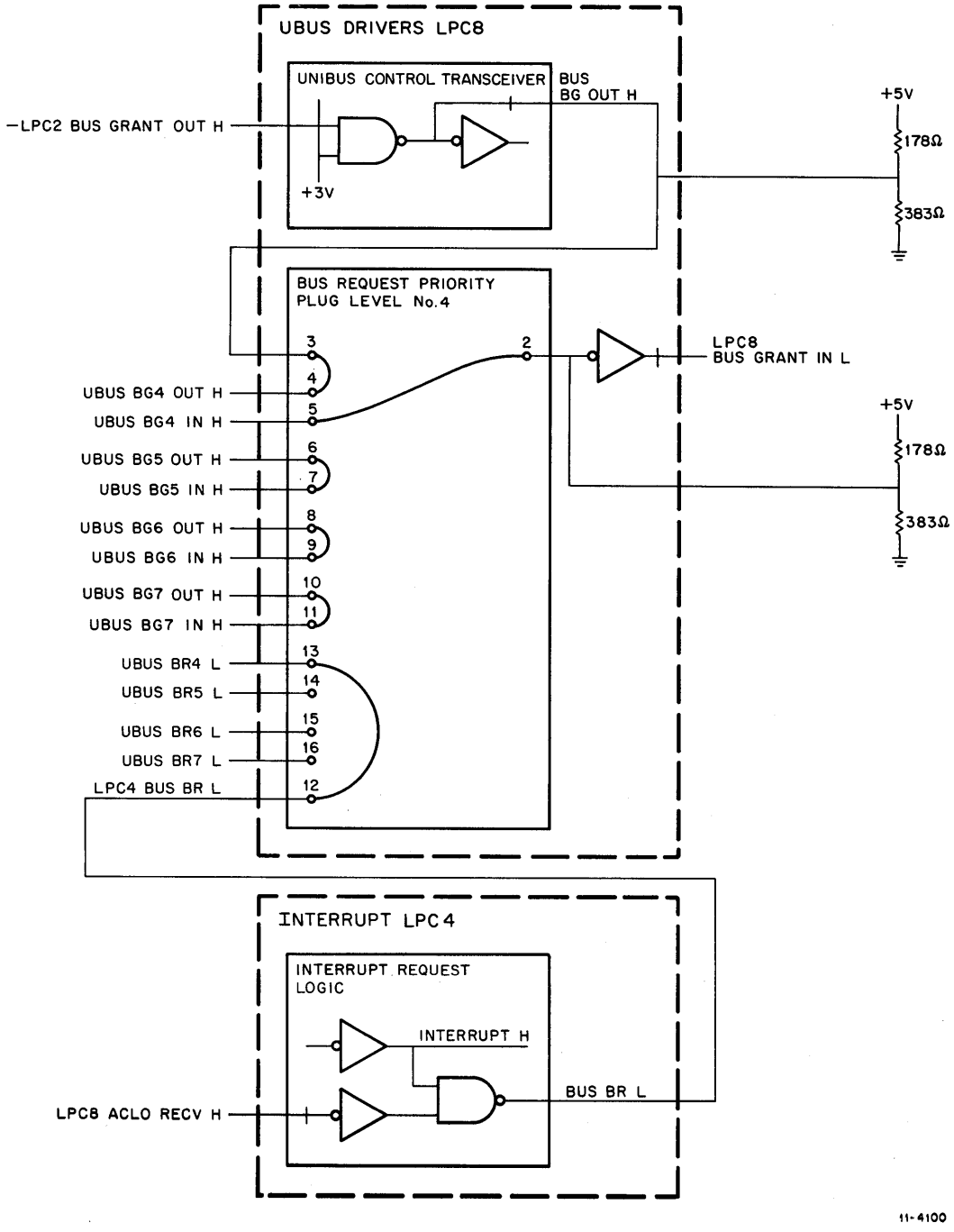


Figure 5-4 Bus Request Priority Plug Jumper Connections

The following is a list of conditions that cause interrupts:

1. Printer going on-line.
2. Printer DAVFU being loaded (DAVFU-equipped printers only).
3. Byte counter going to zero.
4. Detection of an error, specifically:
   Memory Parity Error
   RAM Parity Error
   MSYN Timing Error
   Demand Timing Error
   Printer Going Off-Line
   Printer Parity Error
   Printer DAVFU Error (printers equipped with DAVFU only)
   GO Error

5.3.10 RAM Load (DMA)

The RAM Load mode is entered by setting the Test Mode and DAVFU Load flip-flops in CSRA simultaneously. The starting bus address and the byte count are loaded into their appropriate registers. The GO flip-flop is set to start DMA transfers to the controller.

See Chapter 4 for register addresses and bit assignments.

5.3.10.1 Setting Up Bus Address Register – To set up the bus address register in LPR2 (Figure 5-5), the desired address is written into the register located at 775404.

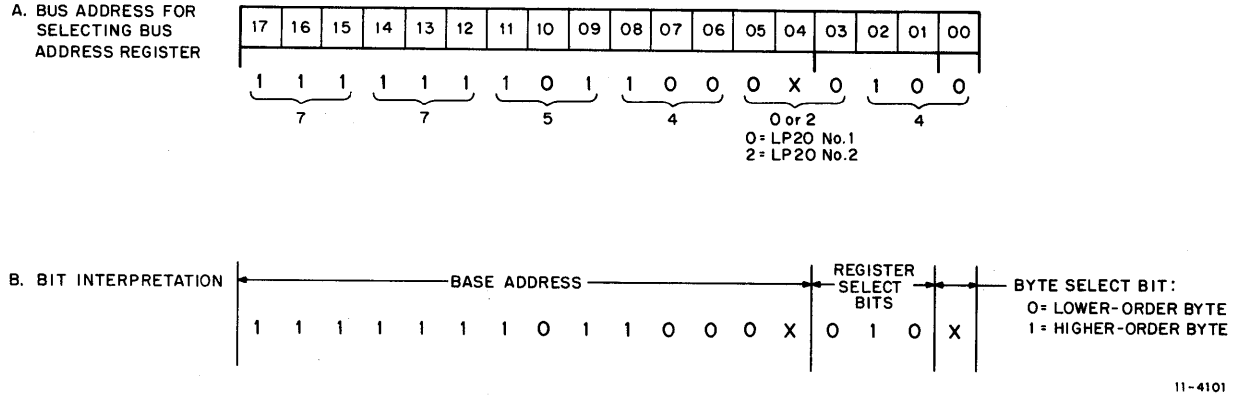


Figure 5-5 Bit Configuration for Bus Address Register

The -LPC1 REG SEL H and LPC8 ADR (03:01) H signals are applied to a decoder in LPC9. Since LPC8 ADR02 H is the only address bit that is high, decimal output No. 2 is selected, so that LPC9 SEL BUS ADR L goes low. When LPC9 SEL BUS ADR L goes low, the 16 data bits DATA (15:00) from LPD7 are loaded into four of the five binary counters that comprise the bus address register. Assume that an octal starting address of 2000 is loaded into the bus address register. Then LPD7 DATA10 H is high, and LPR2 BUS ADR10 H goes high. Bus address bits 16 and 17 are written and read through bits 4 and 5 of CSRA.

5.3.10.2 Setting Up Byte Counter – To set up the byte counter in LPR2, write the desired byte count into the register located at 775406 as discussed in Paragraph 5.3.8.

The -LPC1 REG SEL H and LPC8 ADR (03:01) H signals are applied to a decoder in LPC9. Since ADR02 H and ADR01 H are both high, decimal output No. 3 is selected so that LPC9 SEL BYTE CTR L goes low. The Empty flip-flop in LPC9 is cleared, since a supposed non-zero byte count is loaded. If a zero byte count is loaded, this is equivalent to loading a 4096 byte count.

When LPC9 SEL BYTE CTR L goes low, the 12 data bits DATA (11:00) from LPD7 are loaded into the three binary counters that comprise the byte counter. The number loaded into the byte counter is the two's complement of the total number of bytes (characters) to be transferred. For example, assume the total number of characters to be loaded is 512. In binary this becomes:

001 000 000 000

The two's complement is:

```
110  111  111  111
                +1
-------------------
111  000  000  000
```

which is 7000_8.

5.3.10.3 Setting Up Control Bits for RAM Load – Control bits normally set in the low byte of CSRA (address 775400) are:

06	INT ENB (1)
03	DAVFU LOAD (1)
02	TEST MODE (1)
01	PAR ENB (1)

A data code of 116_8 is used to set these flip-flops. The Test Mode flip-flop is set during a RAM Load so that data will not be routed to the printer.

The -LPC1 REG SEL H and ADR (03:01) H signals are applied to a decoder in LPC9. Since all four signals are low, decimal output No. 0 is selected and applied to an AND gate. With LPC8 CO RECV H in the low condition, LPC9 SEL CSRA LO H goes high, LPC9 SEL CSRA LO L goes low, and LPC9 SEL CSRA LO1 H goes high. SEL CSRA LO1 H is a buffered, but equivalent, signal to SELCSRA LO H.

When LPC6 DAVFU LOAD (1) H goes high, it ensures that the LPD5 Tabover and LPD5 Line Overflow flip-flops remain in the zero state. When the Test Mode flip-flop is set, it selects the TEST DEMAND H signal for LPD6 DEMAND H. TEST MODE (1) H also forces LPD6 LPT PAR ERR H low. LPD6 FORCE VFU L is asserted so LPD6 DAVFU RDY H is asserted.

5.3.10.4 Setting Up GO Flip-Flop – The GO flip-flop must be bit-set. This is accomplished by moving the contents of CSRA into the processor, incrementing by one, and then writing the data back into CSRA.

If LPD6 DEMAND H is high (LPD6 TEST DEMAND H, since Test Mode is set) and no error exists, LPD6 GO ENABLE H is high. LPD6 GO ENABLE H is applied to the D input of the GO flip-flop. When LPC9 SEL CSRA LO H goes high, the GO flip-flop is set.

The signal LPD6 GO ENABLE H is ANDed with LPC9 SEL CSRA LO H in LPC10 and clears the checksum hold register when the GO flip-flop is set. Setting GO also clears the UNDCHAR flag (bit 13 of CSRA) in LPD6.

When LPC6 GO (1) is set in the RAM Load mode, the LPD2 RAM Address Clear one-shot is triggered and produces an 85-ns pulse that clears the RAM address register (up/down counter). Thus, LPD2 RAM ADR (07:00) H go low and octal address 000 is selected in the RAM. The RAM address register load line is disabled in RAM Load mode to prevent loading of this register with the contents of the character buffer since the RAM address register addresses successive RAM memory locations during DMA RAM load operation.

5.3.10.5 Executing an NPR – Refer to the waveforms in Figure 5-6 for the following discussion.

When the GO flip-flop is set, the DEMAND one-shot is triggered, as discussed previously in Section 5.3.9. The LPD6 Demand Request one-shot is triggered 10 μs after LPD6 DEMAND (0) H goes low, producing a 60-ns positive Demand Request pulse, LPD6 DEM REQ H.

Since LPC7 ERROR (0) H and LPD6 NO ERROR H are both true, and there is no line overlow or horizontal tab function in progress (these are held inoperative since the DAVFU Load flip-flop is set), and the byte counter is non-zero, -LPC9 ZERO H and -LPD5 TABOVER H are high. When LPD6 DEM REQ H is ANDed with these signals, the signal LPD6 NPR SET L is asserted. When LPD6 NPR SET L goes low, the LPC4 Request flip-flop is set so that LPC4 REQUEST (1) H goes high and LPC4 UBUS NPR L is asserted. This indicates that the LP20 Controller is requesting use of the bus for a DMA word fetch from main memory.

The processor receives UBUS NPR L and then asserts NPG IN, causing LPC8 UBUS NPG IN H to go high and LPC8 NP GRANT IN L to go low.

When LPC8 NP GRANT IN L goes low, the LPC2 NP Grant flip-flop is set to the one state, since LPC4 REQUEST (1) H is high. The output of the NP Grant flip-flop is low and prevents the grant signal from being sent to the next device on the bus.

The LPC2 NPG SACK flip-flop is set to the one state and LPC2 SACK SEND H is asserted 100 ns after LPC8 NP GRANT IN L goes low. LPC2 SACK SEND H becomes UBUS SACK.

When the NPG SACK flip-flop is set, the LPC4 Request flip-flop is cleared and LPC4 UBUS NPR L is negated since the LP20 has acknowledged receipt of the NPR grant that is initially requested. When the processor receives UBUS SACK L, it removes NPG IN so that LPC8 UBUS NPG IN H and LPC8 NP GRANT IN L are negated. When the bus is no longer busy, LPC8 UBUS BBSY L goes high and LPC8 BBSY RECV H goes low.

When LPC8 BBSY RECV H goes low, LPC2 BBSY RECV L is negated and a high going signal is applied to the clock input of the LPC2 NPG BBSY and BG BBSY flip-flops. In this case, the NPG BBSY flip-flop is set (since the NPG SACK flip-flop was set), and the LPC2 NPG SACK flip-flop is subsequently cleared. LPC8 UBUS BBSY L is asserted and the LP20 is the bus master.

When the NPG BBSY flip-flop is set, it enables the LP20 bus address and control lines. This causes the current contents of the bus address register to be placed on the Unibus address lines and causes the control lines to be configured for a DATI operation. The LP20 internal clock is started, UBUS MSYN is asserted, and the controller awaits completion of a fetch from main memory (see section 5.3.8, NPR Clock).

5.3.10.6 Writing the RAM - When LPC3 NPR A CLKA H (UBUS MSYN) is asserted, LPR1 WRT2 RAM L goes low and LPR1 WRT2 RAM L goes low (Figure 5-7). As a result, the least significant 12 bits of data from the Unibus, i.e., LPD7 DATA (11:00), are written directly into octal address 000 of the translation RAM. Since LPC3 NPR A CLKA is still true for 200 ns after the controller receives UBUS SSYN, the correct data from main memory is written into RAM location 000.

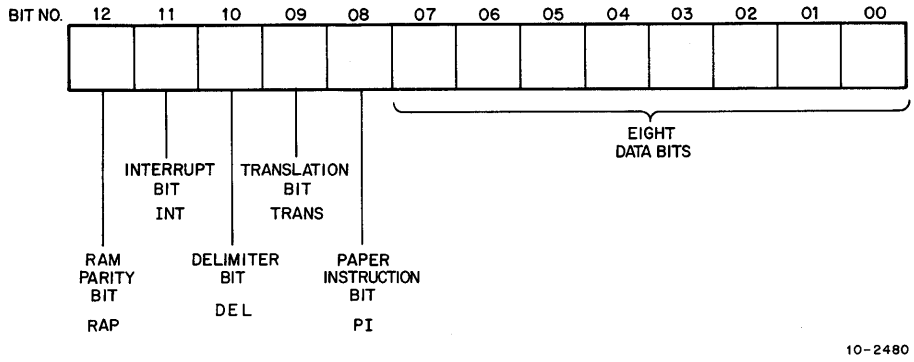
Data bits LPD7 DATA (11:00) are also applied simultaneously to the RAM parity generating logic in LPC5. The rules for RAM parity are summarized as follows:

RAM Parity Generating Logic

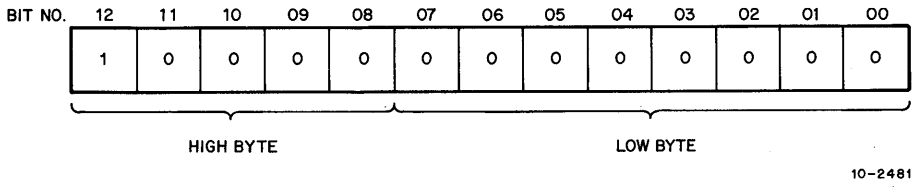
Odd Parity (RAM Parity Test = 0)
Even number of ones gives DATA12 = 1
Odd number of ones gives DATA12 = 0

Even Parity (RAM Parity Test = 1)
Even number of ones gives DATA12 = 0
Odd number of ones gives DATA12 = 1

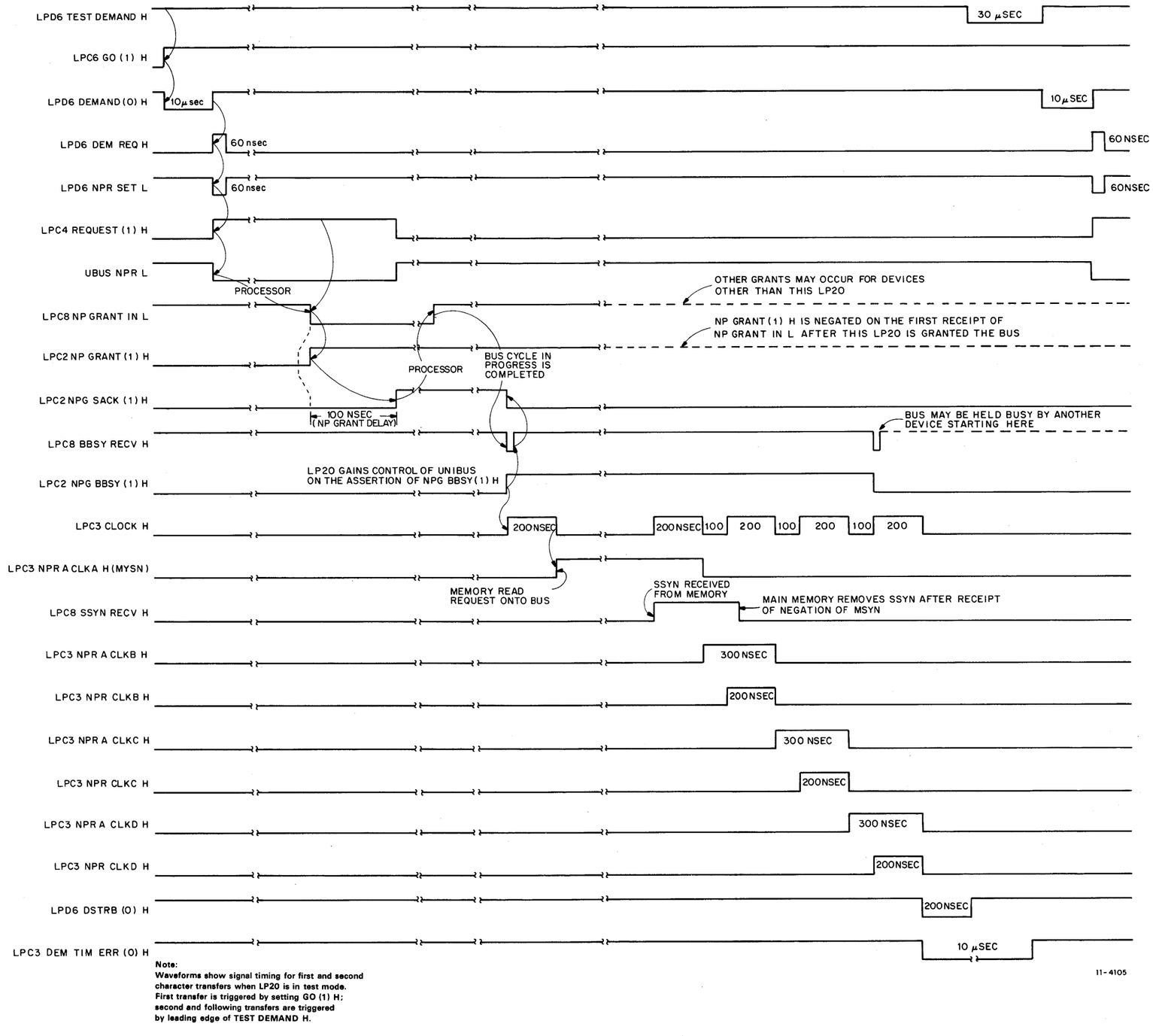
The output of the RAM parity generating logic determines the status of bit 12 in the RAM address, as shown in the following diagram.



Assume that the ASCII character NUL is to be stored in the data bits of address 000 and all control bits are 0. The 13-bit word will then appear as 10000_8 (odd parity):



The signal LPC5 PAR DATA12 H is applied to the 13th RAM in LPR1, thereby completing the 13-bit word in RAM address 000.



Note:
Waveforms show signal timing for first and second character transfers when LP20 is in test mode. First transfer is triggered by setting GO (1) H; second and following transfers are triggered by leading edge of TEST DEMAND H.

Figure 5-6 LP20 Controller Timing Waveforms

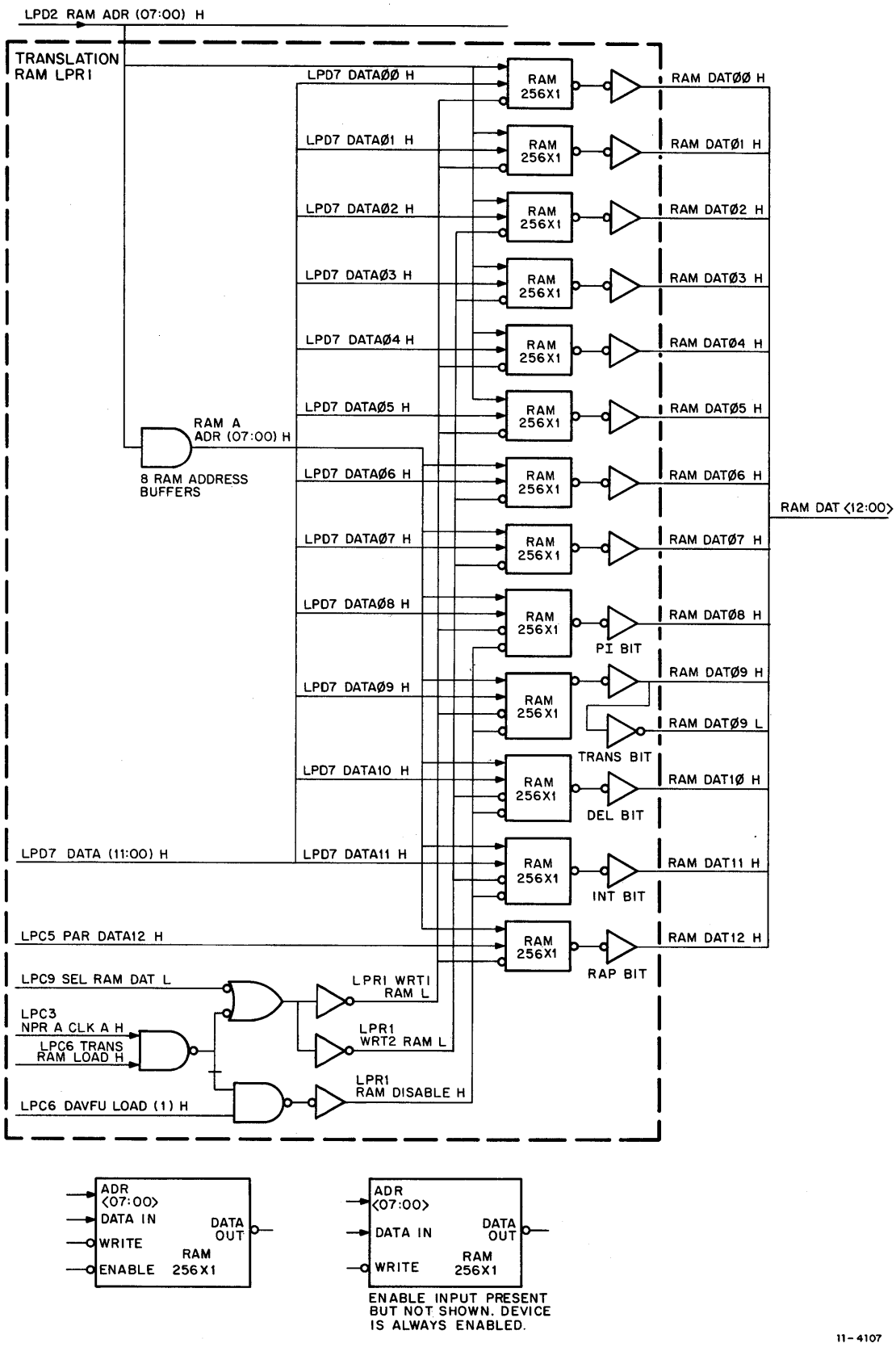


Figure 5-7 Translation RAM Simplified Schematic

5.3.10.7 Other RAM Load Mode Operations – When LPC3 NPR A CLKB H goes high, it enables the memory parity checking logic and clocks the byte selected by bit 00 of the bus address register into the character buffer. The output of the character buffer, CHARBUF (07:00), is the applied to the LPC10 checksum generator.

The signal NPR CLKB H is not used in the RAM Load mode, but is used in all other modes of operation to load the RAM address register with the contents of the character buffer (i.e., the current character). The contents of the character buffer are not loaded into the RAM address register because it is used as a counter to access sequential RAM locations in the RAM Load mode.

The three signals LPC3 NPR CLKC H, -LPC4 ESCAPE INT H, and LPD6 NO ERROR H are all ANDed together in LPR2. Therefore, when LPC3 NPR CLKC H goes high, both the bus address register and the byte counter are incremented by one. In this case, the number in the bus address register becomes 2001_8 and the number in the byte counter becomes 7001_8.

When LPR2 BYT ADR00 H goes high, a high is applied to the word select input of the character buffer. This sets up the character buffer to read the higher order byte on the leading edge of NPR A CLKB H during the next DMA cycle.

The trailing edge of NPR CLKD sets the Data Strobe flip-flop (LPD6 DSTRB (1) H). Since the Test Mode flip-flop is set in RAM Load mode, no data is sent to the printer. Instead, the 200-ns Time Test one-shot is triggered. When the LPD6 200-ns Time Test one-shot times out, the 30-μs Test Demand one-shot is triggered and LPD6 TEST DEMAND H is thereby negated. This, in turn, negates LPD6 DEMAND H.

When LPD6 DEMAND H goes low, the 125-ns Demand Acknowledge one-shot is triggered so that LPD6 DEM ACK H and LPD6 DEM ACK L are asserted. When LPD6 DEM ACK L goes low, the LPD6 DSTRB flip-flop is cleared.

When the 30-μs LPD6 Test Demand one-shot times out, LPD6 TEST DEMAND H goes high and LPD6 DEMAND H is reasserted. When DEMAND H is asserted, the LPD6 10-μs Demand one-shot is triggered, and 10 μs later, the LPD6 60-ns Demand Request one-shot is triggered so that LPD6 DEM REQ H is asserted. As a result, LPD6 NPR SET L is asserted, provided that the appropriate signals are present, as discussed previously.

When LPD6 NPR SET L goes low, the LPC4 Request flip-flop is preset so that LPC4 REQUEST (1) H goes high and LPC4 UBUS NPR L goes low. This indicates that the LP20 Controller is requesting use of the bus for another DATI transfer.

When the second UBUS NPR is asserted, operation is the same as before, with the following exceptions:

1. Since LPR2 BYT ADR00 H is high, the higher order data byte is read into the character buffer and then into checksum.

2. The LPD2 RAM Address Up flip-flop is in the one state. When NPR CLKB L goes high (on the second NPR), the flip-flop goes to the zero state so that LPD2 RAM ADDRESS UP L goes low, thereby incrementing the RAM address register (up/down counter) by one.

It is important to note that the bus address register and the byte counter are incremented by one on each NPR so that a total of two NPRs are required to transfer first the lower order byte and then the higher order byte to the character buffer and checksum register. The RAM address register, on the other hand, is only incremented once during the two NPR cycles. This has the effect of writing the same data word twice into the same RAM address.

In this discussion, the octal number 7000 was loaded in the byte counter prior to RAM load. At the end of the 511th NPR, a total of 255 addresses of the translation RAM are loaded and the byte counter contains a full count of 7777. On the 512th NPR, when LPC3 NPR CLKC H goes high, the byte counter is incremented by one so that the byte counter overflows, and therefore LPR2 BYTE CNTR ZERO L goes low. When LPR2 BYTE CNTR ZERO L goes high on the negation of LPC3 NPR CLKC H, the LPC9 Empty flip-flop is set and LPC9 ZERO L and LPC9 ZERO H are asserted. When LPC9 ZERO L is asserted, LPD6 NPR SET L is held negated (high). Thus no further NPRs are performed.

When the current clock cycle completes and the Data Strobe flip-flop (DSTRB) has been cleared (by the 30-μs Test Demand one-shot being triggered and producing LPD6 DEM ACK), the Done flag is raised (bit 07 of CSRA). This flag indicates that the total number of bytes, as specified by the initial byte count, have been transferred without error.

ANDing of three signals in LPC4 – LPC9 ZERO H, –LPD5 TABOVER H, and LPD6 DEM REQ H – causes LPC4 GO RESET L to be asserted. This clears the LPC4 GO flip-flop and sets the LPC4 Interrupt flip-flop on the leading edge of the 513th occurrence of LPD6 DEM REQ.

5.3.10.8 Summary of DMA in RAM Load Mode of Operation – Direct memory access can be summarized as follows:

1. The controller asserts LPD6 NPR SET L.
2. The Request flip-flop is set.
3. UBUS NPR L is asserted.
4. The processor receives the UBUS NPR L and then asserts NPG IN, thereby granting use of the bus for data transfer under control of the LP20.
5. The NP Grant flip-flop is set.
6. The NPG SACK flip-flop is asserted so that UBUS SACK L goes low, acknowledging the bus grant.
7. When the bus is no longer busy, the NPG BBSY flip-flop is set, with the result that UBUS BBSY is now asserted by the controller. At this point, the LP20 is bus master.
8. With NPG BBSY asserted, the LP20 bus address lines and control lines are enabled. This constitutes the condition for a DATI at the current address in the bus address register.
9. The LP20 clock is started when NPG BBSY is asserted.
10. At the start of clock period NPR A CLKA, UBUS MSYN is asserted, requesting the memory to return a slave sync and the contents of the location specified by the LP20 bus address register. If the memory receives and processes the request properly, it will return the data followed by slave sync before the LP20 MSYN time-out occurs.
11. During clock period NPR A CLKA, the least significant 12 bits of data from the bus, i.e., DATA (11:00) are written into the translation RAM, at the address specified by the RAM address register.

12. The same 12 data bits are applied to the RAM parity generating logic, which produces a high or low output depending on whether there are an even or odd number of 1s, respectively. This parity bit constitutes the 13th bit of the word in each RAM address.

13. At least 75 ns after the memory puts data on the bus, the memory asserts UBUS SSYN, which inhibits the MSYN time-out error circuitry.

14. UBUS SSYN triggers the 200-ns Clock one-shot. When the Clock one-shot times out, clock period NPR A CLKB is initiated and clock period NPR A CLKA is ended.

15. The leading edge of clock NPR A CLKB loads the lower or higher order byte, DATA (07:00) or DATA (15:08), respectively, into the character buffer, depending on whether the least significant bit of the word in the bus address register (i.e., BYT ADR00) is a 0 (lower byte) or a 1 (upper byte).

16. The LPD2 RAM Address Up flip-flop is alternately set to the zero and one states when LPC3 NPR CLKB L goes high. As a result, the RAM address register is incremented by one on every other NPR clock cycle. This means that the same 12 data bits will be written twice into the same RAM address.

17. The output of the character buffer, CHARBUF (07:00), is applied to the checksum generator.

18. The eight bits to the checksum generator are added to the sum currently in the checksum hold register on the leading edge of NPR CLKC. At the same time, both the bus address register and the byte counter are incremented by one.

19. On the leading edge of NPR CLKD, the NPG BBSY flip-flop is cleared, and the LP20 Controller relinquishes control of the bus.

20. On the trailing edge of NPR CLKD, the DSTRB flip-flop is set. Because the LP20 is in the Test mode, a data strobe is not sent to the printer at this time. Instead, a 200-ns Time Test one-shot and a 10-μs DEM TIME ERR one-shot are both triggered, initiating the Demand Time Error circuit.

21. When the 200-ns Time Test one-shot times out, a 30-μs Test Demand one-shot is triggered so that the DEMAND signal is removed. Removal of the DEMAND signal triggers a 125-ns Demand Acknowledge one-shot which, in turn, resets the DSTRB flip-flop. Resetting the DSTRB flip-flop disables the Demand Time Error circuit.

22. When the Test Demand one-shot times out, the DEMAND line is asserted, and a 10-μs Demand one-shot is triggered. When the Demand one-shot times out, the 60-ns Demand Request one-shot is triggered, asserting the signal NPR SET. This causes UBUS NPR to be asserted, which indicates the LP20 Controller is requesting use of the bus for a DATI transfer.

23. The loading of data words into the translation RAM continues until the LPR2 byte counter overflows.

5.3.11 Loading the Direct Access Vertical Format Unit (DAVFU)

After the translation RAM is loaded and the LP20 has been initialized (Local Initialize or Error Reset), it is normal procedure to then load the printer DAVFU. If the printer is equipped with an optical VFU, the DAVFU ready bits in the controller are forced true at all times.

5.3.11.1 Setting Up Bus Address Register and Byte Counter – The initial step is to set up the bus address register (address 775404) in the LPR2 to the first location of DAVFU data in memory. Assume an even address is loaded so BYT ADR00 is low. The next step is to set up the byte counter (address 775406) in LPR2 to the number of bytes required for loading the DAVFU. These registers are loaded as discussed previously in the section on reading and writing registers in the controller. The necessary control bits in CSRA are set up and then the GO bit is bit-set.

5.3.11.2 Determining Correct Byte Count for DAVFU Load – Assume that the printer is to handle an 11-inch form, with a total of 66 lines at a setting of 6 lines per inch, by means of the 6LPI switch on the printer. Since two bytes are loaded per DAVFU partition (see Chapter 4), the total number of bytes in this case is 2 × 66 or 132. A DAVFU start code of 356 and a DAVFU stop code of 357 bring the total byte count to 134_{10} or 206_8. The two's complement of 134_{10} is 7572_8.

5.3.11.3 DAVFU Load Control Bits – When the bus address register and the byte counter in LPR2 have been set up, the next step is to set up the control bits necessary for loading the DAVFU. The bits normally set are:

Bit	Function
06	INT ENB (1)
03	DAVFU LOAD (1)
01	PAR ENB (1)

The Test mode is not set during a DAVFU load so that data for the DAVFU will be routed to the printer.

The LPC6 DAVFU Load flip-flop being set disables line overflow and horizontal tab functions, and the signal LPR1 RAM DISABLE H disables the RAMs associated with the four control bits:

PI Bit	RAM DAT08
TRANS Bit	RAM DAT09
DEL Bit	RAM DAT10
INT Bit	RAM DAT11

This assures that the data destined for the DAVFU is not modified by the contents of the RAM or standard hardwired controller functions. After the control bits are set, the GO bit (bit 00 of CSRA) is bit-set and the controller begins DMA transfers as discussed in Section 5.3.10.5.

When GO is set, the LPC10 checksum hold register is cleared, but the RAM address register is not cleared.

The signals LPC2 NPG BBSY (1) H and LPR2 BYT ADR00 are applied to an AND gate. Since the latter signal is low, the word select input to the character buffer is low so that the lower byte of an incoming data word will be stored first.

When LPC2 NPG BBSY (1) goes high, an NPR clock cycle is initiated. The clock cycle goes through the same states as discussed under RAM Load although some states produce slightly different operations because the Test Mode flip-flop is not set in the DAVFU Load mode.

When LPC3 NPR A CLKA H goes high, a word fetch from main memory is initiated as in RAM Load mode (MSYN is sent).

When LPC3 NPR A CLKB H goes high, it applies a low to the clock input of the character buffer so that data line inputs LPD7 DATA (07:00) (lower order byte) are stored in the character buffer. The output of the character buffer, CHARBUF (07:00), is then applied to the LPD2 RAM address register and to the LPC10 checksum generator. The first word to be stored in the character buffer is DAVFU start code 356_8.

When LPC3 NPR CLKB H goes high, the output of the character buffer is loaded into the RAM address register. This 8-bit byte is applied to the LPD3 CHARBUF/COL CTR multiplexer port and to the LPD1 printer multiplexer.

Since the two signals LPD5 TRANS RAM OUT H and LPD4 LINE OVERFLOW (1) H are both low at this time, the output of the 2 × 4 MUX represents the RAM address. Signal lines for DAVFU start code 356 are asserted as shown below. In addition, LPD1 LPT PAPER INST H goes high.

	Bit							
	07	**06**	**05**	**04**	**03**	**02**	**01**	**00**
RAM ADR (07:00)	1	1	1	0	1	1	1	0
LPT DAT DEC (07,05,03,00)	1		1		1			0
LPT DAT (07:00)	0	1	1	0	1	1	1	0
LPT DATA (8:1)	0	1	1	0	1	1	1	0

The signals labeled LPD1 LPT DAT (07:00) are applied to the D7 Checksum/LPT DAT port in data multiplexer LPS3.

The signals labeled LPD1 LPT DAT (07:00) are also applied to a parity generator in the LPD1 printer multiplexer. The rules for line printer parity can be summarized as follows:

Line Printer Parity Generating Logic

Odd Parity (LPT PAR TEST = 0)
  Even number of ones gives LPT data parity = 1
  Odd number of ones gives LPT data parity = 0

Even Parity (LPT PAR TEST = 1)
  Even number of ones gives LPT data parity = 0
  Odd number of ones gives LPT data parity = 1

The lines in LPD1 labeled LPT DATA (8:1) are applied to the line printer, along with the LPD1 LPT PAPER INST command.

When NPR CLKC H goes high, the contents of the checksum generator are read into the checksum hold register.

When NPR CLKC H goes high, both the bus address register and the byte counter are incremented by one. Now LPR2 BYT ADR00 H goes high and a high is applied to the word select input of the character buffer. This sets up the character buffer to read the higher order byte on the leading edge of the next NPR A CLKB H.

When LPC3 NPR CLKD L goes low, the LPC NPG BBSY flip-flop is cleared and the LP20 releases the bus; when NPR CLKD H goes low, the LPD6 DSTRB flip-flop is set and LPD6 DSTRB (1) H is asserted. Because LPC6 TEST MODE (0) H is high, a data strobe is sent to the printer, thereby strobing in LPD1 LPT DATA (8:1) (DAVFU start code 356).

When LPD6 DSTRB (0) H goes low, the LPC3 10-μs DEM TIME ERR one-shot is triggered so that its zero output goes low. At the same time, LPD6 DSTRB (0) H is applied through an RC integrator to the D input of the DEM TIME ERR flip-flop. The integrator ensures that the DEM TIME ERR one-shot is triggered before the flip-flop D input goes high. If the printer fails to remove the LPD6 DEMAND signal within 10 μs, an error condition results (DEM TIME ERR, bit 01 of CSRB), and the controller halts.

When the printer receives the input data and the data strobe, then LPD7 LPT DEMAND H goes low so that LPD6 PRINT DEMAND H goes low. As a result, LPD6 DEMAND H goes low, thereby triggering the LPD6 125-ns Demand Acknowledge one-shot so that LPD6 DEM ACK H and LPD6 DEM ACK L are asserted. When DEM ACK L goes low, the DSTRB flip-flop is cleared and a low is applied to the D input circuit of the LPC3 DEM TIME ERR flip-flop. Consequently, when the LPC3 10-μs DEM TIME ERR one-shot times out, no error results, since the DEM TIME ERR flip-flop is not set.

When the printer DEMAND line goes high, another NPR is executed to transfer the next byte of data to the DAVFU.

When the second UBUS NPR is asserted, operation is the same as before, with the following exceptions:

1. Since LPR2 BYT ADR00 H and LPC2 NPG BBSY (1) are both high, the higher order DATA byte is read into the character buffer, then into checksum, on the leading edge of LPC3 NPR A CLKB H.

2. The higher order byte is loaded into the RAM address register when NPR CLKB H is asserted. This higher order byte is strobed into the printer when LPC3 NPR CLKD H goes low.

From this point on, characters are loaded into the DAVFU until the byte counter overflows. The manner in which the characters are stored in the DAVFU is described in the following section.

5.3.11.4 DAVFU Character Storage – The DAVFU memory has 143 partitions, each 14 bits wide. The DAVFU is capable, therefore, of controlling forms up to 143 lines long.

Each memory partition is loaded by the recognition of a 2-data-character sequence. In each sequence, the low-order six bits of the first character received are used to load DAVFU bits 01 through 06. The low-order six bits of the second character received are used to load bits 07 through 12. A 1 in the character represents a channel stop in the DAVFU memory (see Chapter 4).

When the byte counter overflows, operation is the same as that at the end of RAM Load, wherein a vector interrupt is performed, returning control to the processor. This completes the DAVFU Load.

NOTE

The signal LPD7 LPT DAVFU READY H goes high when the DAVFU is loaded properly. This causes LPD6 DAVFU RDY L to go low and LPD6 DAVFU RDY H to go high. These conditions are reflected in data multiplexer CSRA and CSRB bits 12 and 06, respectively.

5.3.12 Print Mode

With the RAM and DAVFU loaded, and with the controller initialized, the printer is ready to print up to 143 lines per page, with a maximum of 132 characters (including spaces) per line.

5.3.12.1 Printable Characters – The printer responds to three types of characters. These are printable characters within the character set in use, paper instructions, and the ASCII carriage control characters: carriage return (CR), line feed (LF), and form feed (FF). All other ASCII control characters are printed as spaces, with the exception of ASCII 000 which is the "no-action" character. This character is never sent to the printer, but is deleted by the controller.

5.3.12.2 Print Mode Control Bits and Register Setup – Neither the DAVFU Load flip-flop nor the Test Mode flip-flop is set during normal printing of data. This causes characters to be sent to the printer and enables all character-oriented hardware operations (horizontal tab, line overflow, RAM control bits, "no action" decoding, etc.).

The starting bus address is loaded into the bus address register as discussed in Section 5.3.7 on reading and writing controller registers. Since one character is stored in each byte of the PDP-11 word, the byte count loaded is the total number of characters to be transferred to the printer. After the bus address register, the byte counter, and the correct control bits have been loaded, the GO bit (bit 00 of CSRA) is set to start DMA transfers.

5.3.12.3 Character Processing – Upon receipt of SSYN from memory, the clock in the LP20 is restarted. This indicates that the desired word is present on the data lines.

On the leading edge of LPC3 NPR A CLKB, the byte selected by bit 00 of the bus address register is loaded into the character buffer. From the character buffer, the selected byte is routed to the checksum register and the RAM address register. The RAM address register is loaded on the leading edge of LPC3 NPR CLKB and its output is applied to the printer multiplexer in port 00 and to the RAM. During NPC CLKC, the bus address register and byte counter are incremented if no errors exist.

RAM parity is also checked during LPC3 NPR CLKC. The rules for checking RAM parity can be summarized as follows:

RAM Parity Checking Logic

Odd Parity (RAM PAR TEST = 0)
  Even number of ones gives Error = 1 (ERROR)
  Odd number of ones gives Error = 0 (NO ERROR)

Even Parity (RAM PAR TEST = 1)
  Even number of ones gives Error = 0 (NO ERROR)
  Odd number of ones gives Error = 1 (ERROR)

If a RAM parity error is detected, the controller halts and an interrupt is generated. The Error flip-flop (bit 15 of CSRA) and the RAM PAR ERR flip-flop (bit 03 of CSRB) are set to indicate a RAM parity error occurred.

RAM Control Bits and Delimiter Hold – The control bits in the RAM and the Delimiter Hold flip-flop (DELHOLD) determine if the character is translated or not (see Chapter 4). If it is, the RAM data character, RAM DAT (07:00), is sent to the printer except for three cases: if the RAM data is "no action" (ASCII 000); if the character is horizontal tab; or if the character is the 133rd character and is not a paper motion command.

If the RAM translation and interrupt bits are set high and LPD5 DEL HOLD (1) H is high, LPD5 TRANS RAM OUT H goes low, and translation does not take place. However, LPC4 ESCAPE INT H goes high and LPC4 ESCAPE INT L goes low. If the DAVFU is not being loaded, then, when LPC3 NPR CLKD H goes high, LPC4 GO RESET L goes low, resetting the LPC6 GO flip-flop. At the same time, the LPC4 Interrupt flip-flop is set, with the end result that LPC8 UBUS BR4 is asserted.

The DEL HOLD flip-flop stays set until LPD6 DEM ACK is asserted on the first character which does not have its associated delimiter bit set in the RAM. Each character is translated in turn until no DEL bit is seen. Then only the next character is translated and the DEL HOLD flip-flop is cleared out.

"No-action" characters (ASCII 000) will also clear the DEL HOLD flip-flop if they follow the delimiter character (See the following section).

"No Action" Character – If the eight data bits to the printer multiplexer are all 0s, then LPD1 LPT DAT (07:00) H are all low, signifying that this is a "no-action" character. In this case, the character is not strobed into the printer and an NPR is executed immediately for another data character.

In the LPD5 carriage control, LPD1 LPT DAT (07:00) H are ANDed with LPD1 SEND PAPER INST L and LPC6 DAVFU LOAD (1) L. This means that, if the DAVFU is not being loaded and if a paper instruction (PI) is not being sent to the printer, the LPD5 NO ACTION L and LPD5 NO ACTION H are asserted. When LPD5 NO ACTION L goes low, the clock input to the LPD6 Data Strobe flip-flop is disabled. When LPD5 NO ACTION H goes high, LPD6 NPR SET L goes low on the leading edge of LPC3 NPR CLKD, provided that LPC9 ZERO L is high (the byte counter is not 0 and the page counter is not empty), LPC4 ESCAPE INT L is high (this is not an escape sequence), and LPD6 NO ERROR H is high (no errors are present). Asserting LPD6 NPR SET L causes LPC4 UBUS NPR L to go low, signifying a controller request for another DATI transfer.

On the trailing edge of LPC3 NPR CLKD, the LPD5 Delimiter Hold Clear one-shot is triggered, so that LPD5 DEL HOLD CLEAR H goes high. If the delimiter bit in the RAM is not asserted, then LPR1 RAM DAT10 H is low. These two signals are ANDed in LPD5, with the result that the LPD5 Delimiter Hold flip-flop is cleared.

If LPD5 NO ACTION H is high and LPC9 ZERO H is high, then LPC4 GO RESET L is asserted and the LPC4 Interrupt flip-flop is set when LPC3 NPR CLKD H goes high. This means that, when the byte counter is overflowing or the page counter is empty, a vector interrupt will be requested rather than an NPR when the last character is "no action."

Horizontal Tab Character – If the character is horizontal tab (ASCII 011_8), this is decoded and LPC5 FORCE SPACE L is asserted. This signal, together with the fact the HT (011_8) still resides in the printer multiplexer, causes a space code (ASCII 040_8) to be forced onto the printer data lines.

When NPR CLKD causes data strobe to be asserted, a space code is seen by the printer. The number of space codes sent to the printer is determined by the count stored in the column counter at the time horizontal tab is decoded. If the current column count is 8N + 1, then eight space codes are sent to the printer. In any case, HT is held in the printer multiplexer for the duration of the HT function and no further NPR cycles are performed until all necessary space codes have been sent to the printer.

NPR cycles that would have occurred on NPR CLKD signals that transmit space codes to the printer are suppressed by the assertion of LPD5 TABOVER, which indicates that an HT conversion or line overflow condition exists. This signal also causes the assertion of data strobe in place of LPD5 NPR SET L to transmit the needed space codes.

133rd Character in Line Overflow – If the 133rd character in the current line is not a paper motion command (CR, LF, FF, or PI from the RAM), then the controller will set the Line Overflow flip-flop. The assertion of this flip-flop asserts the signal LPD5 LINE OVERFLOW (1) H, which causes an LF code to be forced to the output of the printer multiplexer. The force space logic is disabled also, ensuring that the LF code reaches the printer data lines. On LPC3 NPR CLKD, the LF code is strobed into the printer.

The LPD5 DEMAND ACKNOWLEDGE H pulse created on the falling edge of DEMAND clears the Data Strobe flip-flop. The Data Strobe flip-flop being cleared clocks the Overflow Hold flip-flop to a 1 and asserts LPD5 TABOVER L. LPD5 DEM ACK also clocks the Line Overflow flip-flop, which clears, since the D input is no longer true. This causes the original 133rd character to reappear at the output of the printer multiplexer. In this case, it is LPD5 DEM REQ from the reassertion of DEMAND, which acts in the same manner as LPC3 NPR CLKD to immediately create another data strobe to the printer, another NPR if the character is "no action" (ASCII 000_8), or a bus interrupt if the RAM control bits or byte count so dictate.

If a horizontal tab character occurs at or beyond column 128, spaces are sent until the column count equals 132. An LF is sent as character 133 and eight space codes are then sent to move the carriage to column nine in the new line. Another NPR is then executed to fetch the next character after horizontal tab.

If the character in question does not fall within the three exceptions stated above, the transfer operation completes with the checksum being updated on NPR CLKC H and the assertion of LPD5 NPR SET L (if the character is 000), LPC4 GO RESET L (for conditions causing a bus interrupt), or LPD6 DSTRB (1) H by LPC3 NPR CLKD.

Escape Sequence – As described in Section 4.9, bit 10 of a translation RAM word is the delimiter bit. When this bit is asserted, its associated DEL HOLD flip-flop in LPD5 is set, translation is forced, and the logic is set up for an escape sequence.

Consider the case where bit 10 of the RAM word is asserted; that is, LPR1 RAM DATI0 H is high. If LPC7 ERROR (0) H is high (no errors), then the LPD5 DEL HOLD flip-flop will be set when LPC3 NPR CLKC H goes high, so that LPD5 DEL HOLD (1) H goes high. Hence, LPD5 TRANS RAM OUT H goes high, and the LPD1 printer multiplexer selects the RAM character, even if RAM translation bit 09 is not set.

Illegal or Undefined Characters – As mentioned in Chapter 4, the user has the option of loading any characters or control codes into the translation RAM. Generally, all unused RAM locations are loaded with the interrupt bit set to 1 and the other RAM bits set to all 0s. In this case, any illegal or undefined characters will stop the transfer and, if the CSRA interrupt enable (INT ENB) bit is set, cause the controller to generate a bus request (UBUS BR4) interrupt to the processor instead of generating a data strobe to the line printer. The current character will not be sent to the printer, but rather will be held in the character buffer available for inspection by the processor. Also, the Undefined Character (UNDCHAR) flag will set bit 13 of the data multiplexer register associated with CSRA. Detailed operation is described below.

The character in the RAM address register selects its corresponding RAM location, and LPR1 RAM DAT (11,09) are routed to AND gates in LPC4. If LPR1 RAM DAT11 H and LPR1 RAM DAT09 L are high, then LPC5 ESCAPE INT is asserted. Assuming the RAM is not being loaded, then in LPD6, LPC6 TRANS RAM LOAD L is high, so that the UNDCHAR flip-flop is set on the trailing edge of LPC3 NPR CLKB L, and this is reflected in bit 13 of CSRA.

Assuming that the DAVFU is not being loaded, then in LPD4, LPC6 DAVFU LOAD (0) H is high. When LPC3 NPR CLKD H goes high, LPC4 GO RESET L goes low and the LPC4 Interrupt flip-flop is set. Asserting LPC4 GO RESET L clears the LPC6 GO flip-flop. Setting the LPC4 Interrupt flip-flop causes LPC8 UBUS BR4 to go low, signifying an interrupt request to the processor.

LPD7 DATA00 H and LPC9 SEL CSRA L01 H are both ANDed in LPC6, so that the UNDCHAR flip-flop is reset whenever the GO bit is set in LPC6. Similarly, LPD6 GO ERR SET L is asserted when LPC9 SEL CSRA L01 H and LPD7 DATA00 H are both high, and LPC7 ERROR (0) H is low or LPD6 DEMAND H is low. Asserting LPD6 GO ERR SET L causes the LPC7 Error flip-flop to be set and also sets the LPC7 GO ERR (1) flip-flop.

Paper Instructions – Paper instructions are vertical format instructions to the DAVFU or optical VFU. They fall into two categories: line slew commands and channel select commands. See Chapter 4 for appropriate codes.

A paper instruction is recognized by the printer when the paper instruction (PI) line is raised at the time data strobe is sent.

PI functions only occur when translation is taking place and RAM bit 08 (PI) is asserted. This causes the signal LPC1 SEND PAPER INSTRUCTION L to be asserted and the printer sees the PI line as being in a true state. In all respects other than the PI line being raised, the transfer is the same as any other printing character.

DEMAND is negated until the print completes the paper instruction.

5.3.13 Error Conditions

If an error is detected during a loading or normal printing operation, then the Error flip-flop in the LPC7 error status logic will be set, an error flag will be raised in CSRB, and an interrupt request will be sent to the processor if LPC6 INT ENB is true. The error signals from various circuits in the controller are combined in the LPC7 detection logic and are the means for setting the Error flip-flop and the flags, and consequently initiating the interrupt request by presetting the Interrupt flip-flop in the LPC4 interrupt logic. Refer to the LPC7 logic diagram for the following discussion.

5.3.13.1 Printer Off-Line – When LPD6 ON LINE H goes low, its associated 85-ns one-shot is triggered, so the LPC7 ON LINE ERR SET L goes low. As a result, LPC7 ERROR SET L goes low and the LPC7 Error flip-flop is set (bit 15 of CSRA).

When LPC7 ERROR SET L goes low, then LPC4 GO RESET L goes low and the LPC4 Interrupt flip-flop is set. If a power-fail condition does not exist, then LPC8 ACLO RECV H is low, so that LPC4 BUS BR L and LPC8 UBUS BR4 L go low.

5.3.13.2 Printer Parity Error (Printers with Parity Logic Only) – When LPD6 LPT PAR ERR H goes high, then LPC7 LPT PAR ERR SET L goes low, and effects an interrupt in the same manner as when the printer goes off-line.

5.3.13.3 DAVFU Not Ready (DAVFU-Equipped Printers Only) – When LPD6 DAVFU RDY H goes low, then LPC7 VFU RDY ERR SET L goes low, and effects an interrupt in the same manner as when the printer goes off-line. DAVFU READY H going false indicates an operational failure in the DAVFU, an incorrect DAVFU load, or a printer power failure.

5.3.13.4 Demand Time-Out Error – When this error occurs, LPC3 DEM ACK ERR SET L goes low, and effects an interrupt in the same manner as when the printer goes off-line. The Demand Time-Out flag is set when the printer fails to acknowledge the receipt of data strobe by the negation of DEMAND within 10 μs after data strobe is sent.

The flag is also set if the user attempts to set the GO flip-flop if DEMAND is false. In this case, GO Error (bit 00 of CSRB) is also set.

5.3.13.5 GO Error, RAM Parity Error, or Memory Parity Error Set – When any one of these three error conditions is asserted low, LPC7 ERROR SET L goes low and the LPC7 Error flip-flop is set. At the same time, the associated D flip-flop is set and the flip-flop output is applied to the data multiplexer CSRB, as follows:

LPC7 GO ERR (1)	Bit 00
LPC7 RAM ERR (1)	Bit 03
LPC7 MEM PAR ERR (1)	Bit 04

5.3.13.6 Error Reset – When LPC8 CLEAR4 L goes low (controller initialization) or LPD7 DATA09 H and LPC9 SEL CSRA HI H are asserted (error reset condition), then LPC7 ERROR RESET X is asserted. At this time, the LPC7 RAM PAR ERR (1), MEM PAR ERR (1), and GO ERR (1) flip-flops are clocked to the zero state.

When LPC7 ERROR RESET H goes high, the LPC9 Empty flip-flop is set to the one state, so LPC9 ZERO H goes high and LPC9 ZERO L goes low. When LPC7 ERROR RESET L goes low, the LPC3 MSYN TIME ERR (1), DEM TIME ERR (1), and LPC6 GO flip-flops are cleared.

5.3.14 Test Mode

Programming the controller in Test mode disables any data from reaching the line printer, as in RAM Load. The controller simulates the DEMAND signal which the printer normally generates to request and acknowledge receipt of data. Hence, the controller operates normally, except that there is no simulation of the Top-of-Form signal, so the page counter will not decrement. The page counter can be tested by setting the test type bits in CSRB to 6_8 and writing a 1 into bit 00 of CSRB (GO ERR). The page counter will decrement by one each time bit 00 is set.

The CSRB test type bits also cause error states in the controller to allow testing of the error detection logic. Table 4-3 describes these tests. Operational details are provided in the following paragraphs.

5.3.15 Testing the Controller

Three test type bits (10:08 in CSRB) allow testing certain functions in the controller that normally are only exercised when an error condition occurs. These tests work by inhibiting various signals, so that time-outs and error conditions occur on each attempt to perform the function under test.

5.3.15.1 DEMAND Time-Out Test – Assume LPD6 DATA08 H is high. When LPC9 SEL CSRB HI H goes high, the LPC6 TEST00 flip-flop is set, so that LPC6 TEST00 (1) H goes high. The output of the associated decoder is asserted so that LPC6 DEM TIME TEST L is asserted. This signal disables the LPD6 Time Test one-shot, thereby preventing the LPD6 TEST DEMAND H signal from being negated. As a result, LPD6 DEMAND H remains high, so that the LPD6 DEM ACK one-shot is not triggered and the LPD6 DSTRB flip-flop is not cleared. Consequently, when the output of the LPC3 10-μs DEM TIM ERR one-shot goes high, it sets the DEM TIME ERR flip-flop, causes LPC3 DEM TIM ERR (1) H to go high, and also triggers the LPC3 85-ns DEM ACK ERR SET one-shot. When LPC3 DEM ACK ERR SET L goes low, LPC7 ERROR SET L goes low and the LPC7 Error flip-flop is set. This test operates in Test mode only.

5.3.15.2 MSYN Time-Out Test – Assume LPD6 DATA09 H is high. When LPC9 SEL CSRB HI H goes high, the LPC6 TEST 01 flip-flop is set, so the LPC6 TEST 01 (1) H goes high. The output of the associated decoder is asserted so that LPC6 MSYN TIME TEST L is asserted. This signal inhibits the LPC8 SSYN RECV H input to the 200-ns Clock one-shot. As a result, SSYN is not seen and the LPC3 MSYN TIMEOUT flip-flop is set, so that LPC3 MSYN TIME ERR (1) H goes high and the LPC3 85-ns MSYN ERROR one-shot is triggered, causing LPC3 MSYN ERR SET L to go low. When MSYN ERR SET L goes low, the 200-ns Clock one-shot is triggered to complete the NPR cycle (Section 5.3.8). In addition, LPC7 ERROR SET L goes low, so that the LPC7 Error flip-flop is set. This test does not depend on the controller operating in Test mode.

5.3.15.3 RAM Parity Test – In this case, LPD7 DATA08 and DATA09 are both asserted, so that the output of the LPC6 decoder asserts LPC6 RAM PAR TEST H.

LPC6 RAM PAR TEST H is applied to both the LPC5 RAM parity generating logic and the LPC5 RAM parity checking logic. This signal causes the controller to generate and check for even instead of odd RAM parity on all data transfers which load the RAM. Writing odd parity (RAM Parity Test off) and checking even parity (RAM Parity Test on) or writing even parity and checking odd parity causes a RAM parity error on each transfer. When LPC5 RAM PAR ERR SET L goes low, LPC7 ERROR SET L goes low, LPC7 RAM PAR ERR (1) H goes high, and the LPC7 Error flip-flop is set. This test operates only in the Printing mode.

5.3.15.4 Memory Parity Test – Assume LPD7 DATA10 H is high. When LPC9 SEL CSRB HI H goes high, the LPC6 TEST02 flip-flop is set in the one state, so that LPC6 TEST02 (1) H goes high. The output of the associated decoder asserts LPC6 MEM PAR TEST L. This signal is applied to the LPC5 memory parity checking logic and has the same effect as asserting LPC8 PB RECV H. If LPC8 PA RECV H is low and the LPC6 PAR ENB (1) H flip-flop is set, then LPC5 MEM PAR ERR SET L will go low during LPC3 NPR A CLKB H. When LPC5 MEM PAR ERR SET L goes low, then LPC7 ERROR SET L is asserted, the LPC7 Error flip-flop is set, and the MEM PAR ERR flip-flop is set. This test operates in any mode.

5.3.15.5 LPT Parity Test – This test causes the controller to send even rather than odd parity to the line printer. Assume LPD7 DATA08 H and LPD7 DATA10 H are both high, when LPC9 SEL CSRB HI H goes high, the LPC6 TEST00 and TEST02 flip-flops are set, so that LPC6 TEST00 (1) H and LPC6 TEST02 (1) H both go high. The output of the associated decoder is asserted so that LPC6 LPT PAR TEST L is asserted. This signal is applied to the parity generator for the line printer parity bit. Since this test involves transfers to the printer, LPC6 TEST MODE (1) H is negated and enables the printer parity error line receiver if the parity error defeat jumper is not removed.

When the printer detects the parity error, LPD6 LPT PAR ERR H goes high; this triggers the associated 85-ns one-shot in LPC7, so that LPC7 LPT PAR ERR SET L goes low and the LPC7 Error flip-flop is set.

5.3.15.6 Page Counter Test – In LPC6, PAG CTR TEST H goes high when LPD7 DAT09 H and LPD7 DATA10 H are high and LPC9 SEL CSRB HI is asserted. If a one is now written into CSRB bit 00 (GO ERROR), the page counter is decremented by one.

5.3.15.7 Loading the Column Counter for Maintenance Purposes – The column counter may be written into for diagnostic purposes. LPD7 DATA (15:08) are written into the counter when the register selection logic asserts SEL COL CTR L.

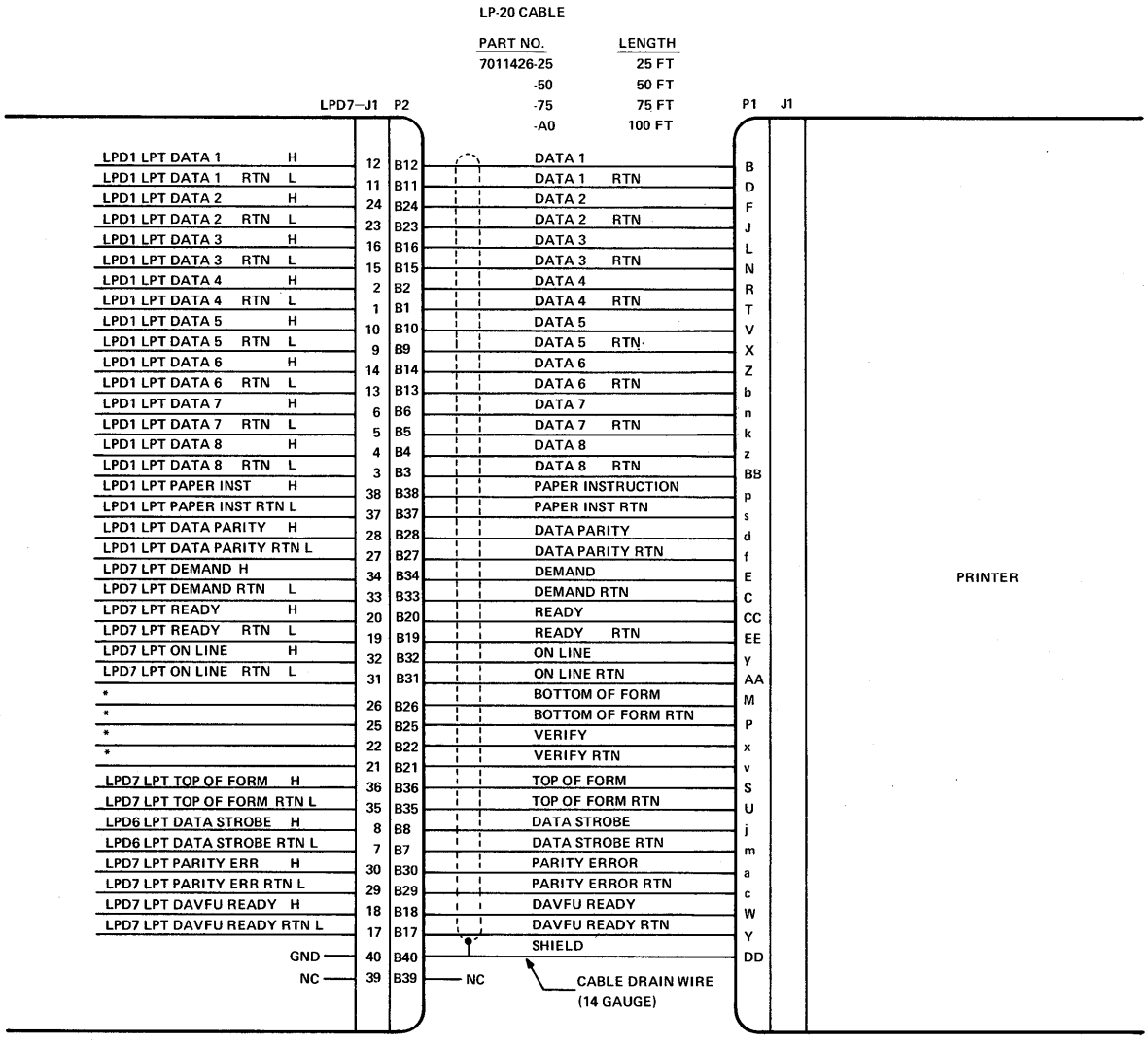
CHAPTER 6
PREVENTIVE MAINTENANCE

The LP20 Controller is completely solid-state and requires no preventive maintenance other than periodic inspection of cables. Running the LP20 diagnostic on a scheduled basis will assist in verifying print quality. The LP20 diagnostic permits failures to be isolated to the unit at fault since the controller is capable of simulating the physical output device even if one is not connected.

CHAPTER 7
PRINTER DESCRIPTIONS

This chapter briefly describes the line printers that can be interfaced to and controlled by the LP20 Line Printer Controller. Detailed descriptions of these printers are contained in the appropriate manuals referenced in this chapter.

The printer interface consists of the signal lines as shown in Figure 7-1. Data transfer between the system and the printer is accomplished by means of a handshaking process via the DEMAND and DATA STROBE lines.



*THESE SIGNALS ARE NOT USED BY THE LP20 CONTROLLER.

11-4098

Figure 7-1 Printer Interface Signals

7.1 LP05 LINE PRINTER

7.1.1 LP05 Line Printer General Description

DEC LP05 (modified DPC 2230) printers (Figure 7-2) are used with printer systems Model LP20-AA, AD, BA, and BD and have a line length of 132 columns. Refer to Table 1-1 for line printer option designations.

Models LP20-AA and -AD use the ASCII 64-character set and print at a nominal rate of 300 lines per minute.

Models LP20-BA and -BD use the ASCII 96-character set and print at a rate of 230 lines per minute.

LP05 printers driven by the LP20 controller incorporate the direct access vertical format unit (DAVFU) and long line interface (LLI). The DAVFU provides program-loadable control of vertical forms movement. The LLI contains differential line drivers/receivers which allow the line printer to be located up to 100 feet from the controller.

Table 7-1 lists the applicable documents for the LP05 printer.

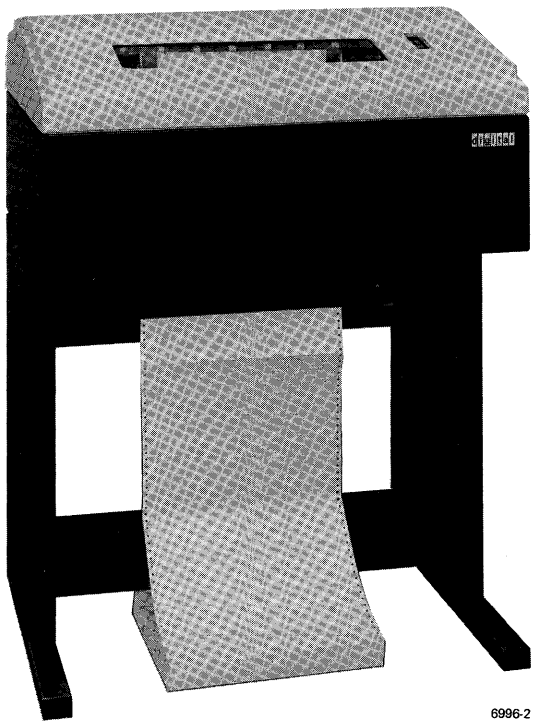


Figure 7-2 Model LP05 Line Printer

Table 7-1 LP05 Applicable Documents

Title	Number	Description
Model 2230 Line Printer Technical Manual, Volume I	DPC 241735	Detailed description of the Dataproducts Model 2230 Line Printer. Includes installation, operation, principles of operation, maintenance and troubleshooting, and standard options.
Model 2230 Line Printer Technical Manual, Volume II	DPC 241735	Detailed logic diagrams of the printed circuits, power distribution schematics, engineering drawings, mechanical drawings, and parts lists for Dataproducts Model 2230 Line Printer.
Dataproducts Engineering Drawings		
1000 r/min Drum Speed Addendum	234897	Description of the changes made to the DPC Model 2230 line printer configuration which make it a DEC LP05. Includes changes in adjustment procedures.
Control Logic Card Addendum	239522	Description of changes to DPC 2230 control logic for LP05.
I/O Harness Configuration	241689	I/O harness changes for long line interface.
Long Line Interface	239539	Description of long line interface I/O option.
Direct Access Vertical Format Unit	234898	Description of DAVFU option.
Active Ribbon Control System	239543	Description of ribbon deskew option.
Forms Length Selector Switch	234899	Description of manual forms length option.

7.1.2 LP05 Interface Signals

The LP05 printer interface signals are described in Table 7-2. The printer neither checks parity nor flags parity errors; therefore DATA 8, DATA PARITY, and PARITY ERROR signals are not used.

Table 7-2 LP05 Printer Interface Signals

Signal	Function
DATA (7:1)	Seven-bit ASCII data to the printer for printing and DAVFU load.
READY	This signal indicates when the printer is ready to be put on-line by the operator. When READY is high, the following are true: 1. Power and dc voltages are on. 2. No fault conditions exist.
ON LINE	This signal indicates when the printer has been put on-line. When ON LINE is high, the following are true: 1. The READY signal is true; READY light is on. 2. The printer operator has actuated the ON LINE switch. 3. The PRINT INHIBIT switch is OFF.
DEMAND	The DEMAND line signifies the printer is ready to accept a character; it remains high until a data strobe is received. It is disabled while the character is stored in memory and during the print operation. The DEMAND line can only come high after the operator has placed the printer on-line. DEMAND will not be asserted if DATA STROBE is true.
DATA STROBE	This line is controlled by the system to determine when the information on the data lines is to be accepted by the printer. Each time a data strobe occurs, the printer samples the data lines, and the DEMAND line is made low while the character is stored. Once a carriage control character has been transferred to the printer, the DEMAND line remains low while the characters are printed.
DAVFU READY	This signal is high when the DAVFU has been loaded correctly and no operational errors have been detected.
TOP-OF-FORM	This signal goes high when the top-of-form paper position is reached.
PAPER INSTRUCTION	This signal is high when the DAVFU is being loaded or used.

NOTE

The LP05 printer does not accept data parity or 8-bit ASCII data characters; therefore, DATA (8), data parity, and parity error are not used. The LP20 controller does not use the bottom-of-form or connector verify signals.

Interface signal timing is contained in Volume I of DPC 234875 (Table 7-1).

7.1.3 LP05 Printer Specifications

Specifications for the LP05 printer are listed in Table 7-3. These specifications are for information purposes only and are subject to change without notice.

Table 7-3 LP05 Printer Specifications Summary

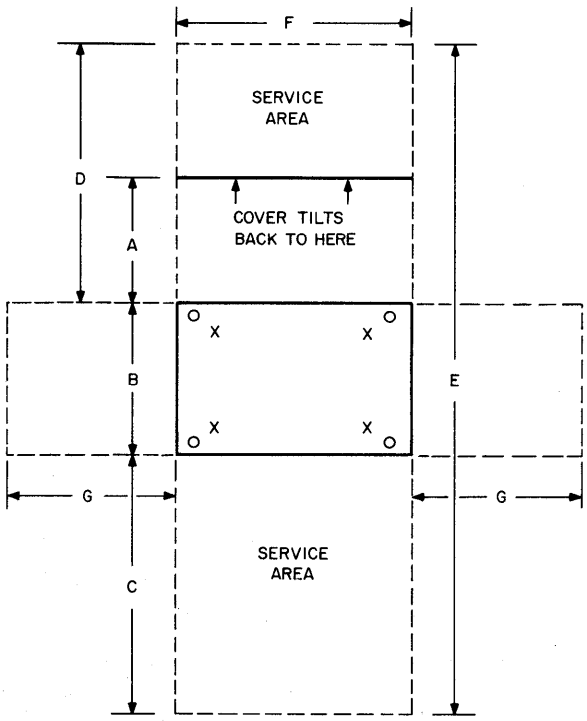
Item	Specifications
Power Requirements	
Input Voltage	115, 220, 230, or 240 Vac (± 10%)
Input Frequency	50 or 60 Hz (± 2%), single phase (see technical manual for proper configuration)
Power Consumption	700 W max at 60 Hz 525 W max at 50 Hz
Heat Dissipation	2400 Btu/hr (60 Hz) 1800 Btu/hr (50 Hz)
Surge	64 A p-p, 20 A E-frame breaker with curve 1 rating
Environmental Requirements	
Operating Temperature	16° C (60° F) min 27° C (80° F) max
Non-operating Temperature	-18° C (0° F) min 66° C (150° F) max
Humidity (non-condensing)	
Operating	20% min 60% max
Non-operating	5% min 95% max
Physical Description	
Dimensions	
Height	1.14 m (45 in)
Width	0.81 m (32 in)
Depth	0.56 m (22 in)
Weight	154 kg (340 lb)
Paper Requirements	
Paper	
Type	Standard fan-folded and edge-punched
Dimensions	4 in to 16.75 in wide, with 4 to 24 in between folds
Weight	
Single copy	15 lb bond min
Multi-copy	12 lb bond with single shot carbon for up to 6 parts

Table 7-3 LP05 Printer Specifications Summary (Cont)

Item	Specifications
Performance Characteristics	
Printable Characters	
Number	64/96
Type	ASCII code, DEC standard font: EDP/Scientific
Size	Typically 0.095 in high and 0.065 in wide
Characters Per Line	132
Character Drum	
Drum Speed	1000/660 r/min
Print Rates	300/240 lines/min
Character Spacing (horizontal)	0.100 (± 0.005) in between centers
Line Advance Time	41 ms (max)
Line Spacing	0.167 (± 0.010) in (6 line per in) 0.125 (± 0.010) in (8 line per in)
Paper Slew Speed	20 in per second (min)
Character Synchronization	Variable reluctance pick-up sensing drum position
Vertical Format	DAVFU controlled
Interface Signals	
Input	7 Data lines 1 Data Strobe line 1 Paper Instruction line for DAVFU
Output	1 DAVFU Ready line 1 Ready line 1 Demand line 1 On-line line 1 Top-of-Form line
Paper Loading	Paper loaded directly on tractors from the supplier box
Paper Tensioning	1 Paper tensioner bar located just below print station

7.1.4 LP05 Space Requirements

Service space requirements for the LP05 printer are shown in Figure 7-3.



DIMENSIONS	A	B	C	D	E	F	G
METERS	0.46	0.84	0.91	0.91	2.39	0.81	0.6
INCHES	18	28	36	36	94	32	24

Figure 7-3 LP05 Printer Space Requirements

7.2 LP07 LINE PRINTER

7.2.1 LP07 Line Printer General Description

DEC LP07 (DPC 2550) (Figure 7-4) printers are used with Model LP200-BA, -BB line printer systems and have a line length of 132 columns.

Models LP200-BA use the ASCII 64-character set and print at a rate of 1220/990 lines per minute (Table 1-1 for printer option designations).

Models LP200-BB use the ASCII 96-character set and print at a rate of 905/715 lines per minute.

LP07 printers contain the direct access format unit (DAVFU) and a long line interface (LLI). The DAVFU provides loadable program control for vertical forms movement and the LLI allows the line printer to be located from 25 to 200 feet from the controller.

Table 7-4 lists the applicable documents for the LP07 printer.

8056-2

Figure 7-4 Model LP07 Line Printer

Table 7-4 LP07 Applicable Documents

Title	Number	Description
Model 2550 Line Printer Technical Manual, Volume I	DPC 238811E	Detailed description of the Dataproducts Model 2550 Line Printer. Includes installation, operation, principles of operation, maintenance, troubleshooting, and standard options.
Model 2550 Line Printer Technical Manual, Volume II	DPC 238811E	Detailed logic diagrams of the printed circuits, power distribution schematics, engineering drawings, and mechanical drawings.
Model 2550 Line Printer Technical Manual, Volume III	DPC 238811E	Illustrated parts list.
Dataproducts Engineering Drawings		
Direct Access Vertical Format Unit	242854	Description of DAVFU option
Model 2550 Configuration Addendum, Charaband Kit #241850-13	242850	Charaband Configuration for DEC LP07-YX
DEC 2550 Special Features Addendum (LL I/O, DAVFU, and Built-in Self-Test)	242853	Special Modifications to the DPC 2550 for DEC

7.2.2 LP07 Interface Signals

The LP07 printer interface signals are described in Table 7-5.

Table 7-5 LP07 Printer Interface Signals

Signal	Function
DATA (7:1)	Seven-bit ASCII data to the printer for printing and DAVFU load.
READY	This signal indicates when the printer is ready to be put on-line by the operator. When READY is high, the following are true: 1. Power and dc voltages are on. 2. No fault conditions exist.
ON LINE	This signal indicates when the printer has been put on-line. When ON LINE is high, the following are true: 1. The READY signal is true; READY light is on. 2. The printer operator has actuated the ON LINE switch. 3. The PRINT INHIBIT switch is OFF.
DEMAND	The DEMAND line signifies the printer is ready to accept a character; it remains high until a data strobe is received. It is disabled while the character is stored in memory and during the print operation. The DEMAND line can only come high after the operator has placed the printer on-line. DEMAND will not be asserted if DATA STROBE is true.
DATA STROBE	This line is controlled by the system to determine when the information on the data lines is to be accepted by the printer. Each time a data strobe occurs, the printer samples the data lines and the DEMAND line is made low while the character is stored. Once a carriage control character has been transferred to the printer, the DEMAND line remains low while the characters are printed.
DAVFU READY	This signal is high when the DAVFU has been loaded correctly and no operational errors have been detected.
TOP-OF-FORM	This signal goes high when the top-of-form paper position is reached.
PAPER INSTRUCTION	This signal is high when the DAVFU is being loaded or used.

NOTE

The LP07 printer does not accept data parity or 8-bit ASCII data characters; therefore, DATA (8), data parity, and parity error are not used. The LP20 controller does not use the bottom-of-form or connector verify signals.

7.2.3 LP07 Printer Specifications

Table 7-6 contains the specifications for the LP07 printer. These specifications listed are for informational purposes only and are subject to change without notice.

Table 7-6 LP07 Printer Specifications Summary

Item	Specifications
Power Requirements	
Input Voltage	200, 210, 215, 220, 225, 235, 250 Vac (± 10%)
Input Frequency	50 or 60 Hz (± 2%), single phase
Power Consumption	1235 W max at 50 Hz 1300 W max at 60 Hz
Heat Dissipation	4220 Btu/hr (50 Hz) 4440 Btu/hr (60 Hz)
Surge	120 A p-p, 30 A E-frame breaker with curve 1 rating
Environmental Requirements	
Operating Temperature	10° C (50° F) min 43° C (110° F) max
Non-operating Temperature	-23 C (-10° F) min 50° C (122° F) max
Humidity (non-condensing)	
Operating	10% to 90% with static eliminator
Non-operating	5% to 95%
Physical Characteristics	
Dimensions	
Height	1.17 m (46 in)
Width	1.23 m (48.5 in)
Depth	0.62 m (24.5 in)
Weight	363 kg (800 lb)
Paper Requirements	
Paper	
Type	Standard fan-folded and edged punched
Dimensions	5-1/8 to 18-3/4 in wide, with 4 to 22 in between folds (standard length forms of 11 in can be stacked within printer cabinet with door closed: forms greater than 11 in will require center cabinet doors of printer to remain open.
Weight	
Single copy	15 lb bond minimum
Multi-copy	12 lb bond with 6 to 8 lb single-shot carbon for up to 6 parts

Table 7-6 LP07 Printer Specifications Summary (Cont)

Item	Specification
Performance Characteristics	
Printable Characters	
Number	64/96
Type	ASCII code, DEC standard font: EDP/Scientific
Size	Typically 0.095 in high and 0.065 in wide
Characters Per Line	132
Print Rates	1220/900 lines/min (64-character set) 905/715 lines /min (96-character set)
Character Spacing (horizontal)	0.100 (± 0.005) in between centers
Line Advance Time	12.5 ms
Line Spacing (vertical)	0.125 (± 0.010) in (8 lines/in) 0.167 (± 0.010) in (6 lines/in)
Paper Slew Speed	60.0 in/s
Character Synchronization	Transducer pick-up sensing band position
Vertical Format	DAVFU controlled
Interface Signals	
Input	8 Data lines 1 Data Strobe line 1 Paper Instruction line 1 Data Parity line 1 Interface Connector verification line
Output	1 Ready line 1 Demand line 1 On-line line 1 Parity Error line 1 Top-of-form line 1 Interface Connector verification line
Paper Loading	Paper loaded directly on tractors from the supplier box
Paper Tensioning	1 set of lower tractors

Printer options do not include Charaband®. Band is ordered separately under the designation LP07-YX, where X specifies the character set (Table 7-7).

®Charaband is a registered trademark of Dataproducts Corporation.

Table 7-7 LP200 Charaband and Ribbon Options

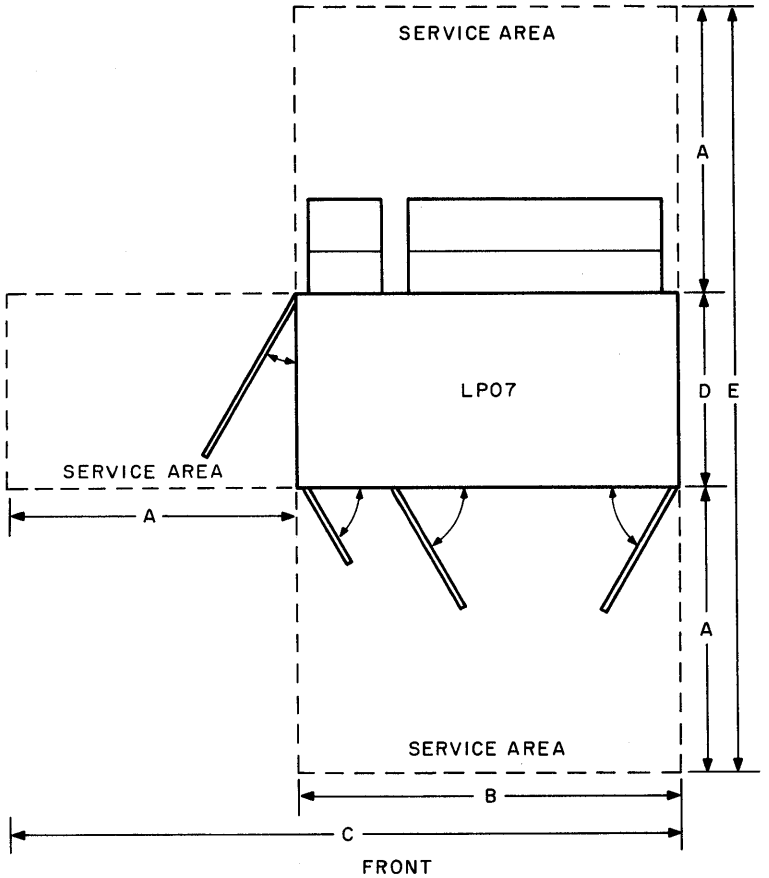
Dataproducts Part No.	DEC P/N	Option Designation	Description
241850-040	30-14280-00	LP07-YA	64/64 EDP
241850-035	30-14280-01	LP07-YB	96/96 EDP
241850-013	30-14280-02	LP07-YC	64/96 EDP* "Standard" Base
241850-030	30-14280-03	LP07-YD	EDP/Kata Kana (Japanese)
	30-14280-04	LP07-YE	Reserved
241850-043	30-14280-05	LP07-YF	64/96 OCR-A
241850-044	30-14280-06	LP07-YH	96/96 Scientific
241850-048	30-14280-07	LP07-YJ	96/96 EDP/Scientific
241850-056	30-14280-08	LP07-YK	96/96 Swedish/Finnish

The base number assigned for LP07 (2550) ribbons is 36-14281. Current variations are:

239385-6	30-14281-00	2 mil Mylar	LP07 Ribbon - 40 yd
239385-3	30-14281-01	3 mil Nylon	LP07 Ribbon - 20 yd
239385-5	30-14281-02	4 mil Nylon	LP07 Ribbon - 20 yd
239385-1	30-14281-03	5 mil Nylon	LP07 Ribbon - 15 yd

7.2.4 LP07 Space Requirements

Service space requirements for the LP07 printer are shown in Figure 7-5.



DIMENSIONS	A	B	C	D	E
METERS	0.91	1.23	2.13	0.62	2.45
INCHES	36	48.5	84.5	24.5	96.5

10-3012

Figure 7-5 LP07 Printer Space Requirements

7.3 LP10 LINE PRINTER

7.3.1 LP10 Line Printer General Description

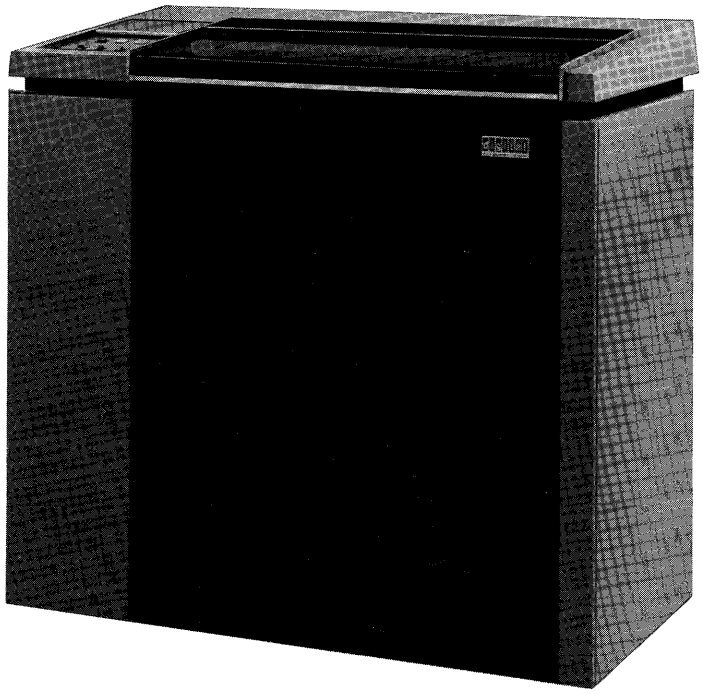
Printer system models LP20-FA, FB, FC, FD, HA, HB, HC, and HD use a DEC LP10 (modified DPC 2470) Line Printer (Figure 7-6) having a line length of 132 columns (see Table 1-1 for option designations).

Models LP20-FA, -FB, -FC, and -FD use the ASCII 64-character set and print at a nominal rate of 1250 lines per minute.

Models LP20-HA, -HB, -HC, and -HD use the ASCII 96-character set and print at a rate of 925 lines per minute.

LP10 printers incorporate a paper tape vertical format unit (VFU), a long line interface, and line printer parity circuitry.

The paper tape VFU is transparent to the user and appears equivalent to a similarly loaded DAVFU. The long line interface allows the printer to be located up to 100 feet from the user system (except LP10 F and H) and reliability is enhanced by the use of parity logic in the printer to detect data errors which the printer then flags to the controller. A list of applicable documents for the LP10 printer is contained in Table 7-8.



6476-1

Figure 7-6 Model LP10 Line Printer

Table 7-8 LP10-J, -K Applicable Documents

Title	Number	Description
Model 2470 Line Printer Technical Manual, Volume 1	DPC 233730 Volume I	Detailed description of the Dataproducts Model 2470 Line Printer. Includes installation, operation, principles of operation, maintenance and Troubleshooting.
Model 2470 Line Printer Technical Manual, Volume II	DPC 233730 Volume II	Mnemonics, flow charts, detailed logic diagrams of the printed circuits, power distribution schematics, engineering drawings, mechanical drawings, and parts lists for Dataproducts Model 2470 Line Printer.
Dataproducts Engineering Drawings		
Addendum to DEC Model 2470 Line Printer	233564	Supplementary information for the DEC version of DPC 2470. Includes logic implementation, signal changes, logic diagram sheets, circuit card complement, mnemonics, options, parts lists, and wirelists.

7.3.2 LP10 Interface Signals

The LP10 printer interface consists of the signal lines shown in Figure 7-1. Table 7-9 lists the LP10 interface signals and describes their functions. Interface signal line timing is contained in Volume I of DPC 233730 (see Table 7-8).

Table 7-9 LP10-J, -K Printer Interface Signals

Signal	Function
DATA (7:1)	7-bit ASCII data to the printer for printing (by the controller).
DATA (8)	Parity is generated on all eight bits and DATA (8) is sent to the printer to permit correct parity checking.
READY	This signal indicates when the printer is ready to be put on-line by the operator. When READY is high, the following are true: 1. Power and dc voltages are on. 2. No fault conditions exist.
ON LINE	This signal indicates when the printer has been put on-line. When ON LINE is high, the following are true: 1. The READY signal is true; READY light is on. 2. The printer operator has actuated the ON LINE switch. 3. The PRINT INHIBIT switch is OFF.
DEMAND	The DEMAND line signifies the printer is ready to accept a character and remains high until a data strobe is received. It is disabled while the character is stored in memory and during the print operation. The DEMAND line can only come high after the operator has placed the printer on-line. DEMAND will not be asserted if DATA STROBE is true.
DATA STROBE	This line is controlled by the system to determine when the information on the data lines is to be accepted by the printer. Each time a data strobe occurs, the printer samples the data lines, and the DEMAND line is made low while the character is stored. Once a carriage control character has been transferred to the printer, the DEMAND line remains low while the characters are printed.

Table 7-9 LP10-J, -K Printer Interface Signals (Cont)

Signal	Function
DAVFU READY	This signal is not used since the printer uses a paper tape VFU. The controller must be configured accordingly.
TOP-OF-FORM	This signal goes high when the top-of-form paper position is reached.
PAPER INSTRUCTION	This signal is high when the VFU is being used.
DATA PARITY	Parity bit generated on DATA (8:1) and sent to the LP10 Printer.
PARITY ERROR	Signal from the LP10 Printer that a parity error has occurred. Negated on receipt of the next carriage control character.

NOTE

The LP10 Printer uses an optical VFU and does not generate a DAVFU READY signal. The LP20 controller does not use the bottom-of-form or connector-verify signals.

7.3.3 LP10 Printer Specifications

A summary of the LP10 specifications is contained in Table 7-10. These specifications are for informational purposes only and are subject to change without notice.

Table 7-10 LP10 Printer Specifications Summary

Item	Specification
Power Requirements	
Input Voltage	115, 220, 230, or 240 Vac (± 10%)
Input Frequency	50 or 60 Hz (± 2%), single phase (see technical manual for proper configuration)
Power Consumption	1950 W max at 60 Hz (Model 2470) 1855 W max at 50 Hz
Heat Dissipation	6700 Btu/hr (60 Hz) 6335 Btu/hr (50 Hz)
Surge	120 A p-p, 30 A E-frame breaker with curve 1 rating
Environmental Requirements	
Operating temperature	16° C (60° F) min 27° C (80° F) max
Non-operating temperature	-18° C (0° F) min 66° C (150° F) max
Humidity (non-condensing)	
Operating	30% to 60% without static eliminator 10% to 60% with static eliminator
Non-operating	5% to 95%

Table 7-10 LP10 Printer Specifications Summary (Cont)

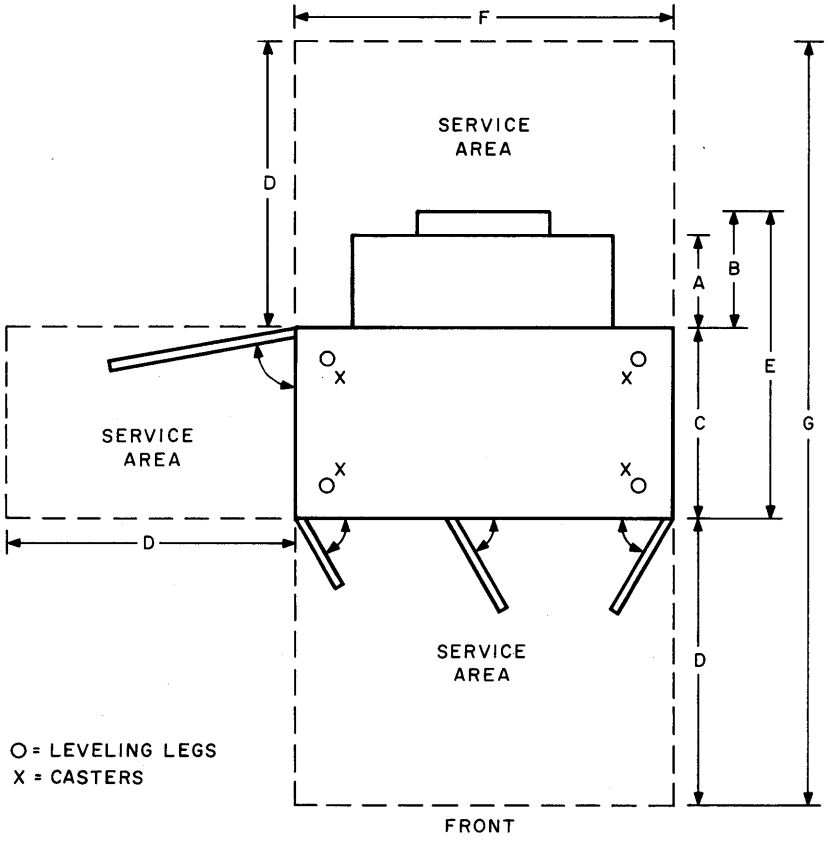
Item	Specifications
Physical Characteristics	
Dimensions	
Height	1.17 m (46.0 in)
Width	1.23 m (48.5 in)
Depth	0.93 m (36.5 in)
Weight	Model 2470: 363 kg (800 lb)
Paper Requirements	
Paper	
Type	Standard fanfold, edge-punched with hole spacing 1/2-in apart from center-to-center
Dimensions	5-1/4 in to 19 in wide, with 4 to 22 in between folds (standard length forms of 11 in can be stacked within printer cabinet with doors closed: doors can be opened to stack paper and operate printer with forms in excess of 11 in length).
Weight	
Single copy	15 lb bond (min)
Multi-copy	12 lb bond with single-shot carbon for up to six parts
Special forms, max	0.020 in
Performance Characteristics	
Printable characters	
Number	64/96
Type	ASCII code, DEC standard font: EDP/Scientific
Size	Typically 0.095 in high and 0.065 in wide
Characters per line	132
Character drum	
Characters	64/96
Drum speed	1800/1200 r/min (64 char set: high/low) 1200/800 r/min (96 char set: high/low)
Print rates	Refer to Table 1-1
Character spacing (horizontal)	0.100 (± 0.005) in between centers
Line Advance Time	14 ms (max)
Line Spacing (vertical)	0.167 (± .010) in (6 lines/in) 0.125 (± .010) in (8 lines/in) Each character within ± 0.010 in from mean line through the characters
Paper Slew Speed	35 in/s (min)
Character Synchronization	Variable reluctance pick-up sensing drum position
Vertical Format	12 channel paper tape reader with step-count feature (0–15 lines)

Table 7-10 LP10 Printer Specifications Summary (Cont)

Item	Specifications
Performance Characteristics (Cont)	
Interface Signals	
Input	8 Data lines
	1 Data Strobe line
	1 Paper Instruction line
	1 Data Parity line
Output	1 Ready line
	1 Demand line
	1 On-line line
	1 Parity Error line
	1 Top-of-Form line
Paper Loading	Paper loaded directly on tractors from the supplier box
Paper Tensioning	1 set of lower tractors

7.3.4 LP10 Space Requirements

Space requirements for servicing the LP10 printer are shown in Figure 7-7.



DIMENSIONS	A	B	C	D	E	F	G
INCHES	11.5	14	24.5	36	38.5	48.5	96.5
METERS	0.29	0.36	0.62	0.91	0.98	1.23	2.44

10-0935

Figure 7-7 LP10 Printer Space Requirements

7.4 LP14 LINE PRINTER

7.4.1 LP14 Line Printer General Description

DEC LP14 (DPC 2290) printers (Figure 7-8) are used with printer systems Model LP20-CA, -CB, -DA, and -DB and have a line length of 132 columns (see Table 1-1 for printer option designations).

Models LP20-CA and -CB use ASCII 64-character sets and print at a nominal rate of 890 lines per minute.

Models LP20-DA and -DB use ASCII 96-character sets and print at a nominal rate of 650 lines per minute.

LP14 printers, used with the LP20 controller, incorporate the direct access vertical format unit (DAVFU) and long line interface (LLI). The DAVFU provides program-loadable control of vertical forms movement and the LLI allows the line printer to be located from 20 to 500 feet from the controller.

Documents pertaining to the LP14 printer are listed in Table 7-11.

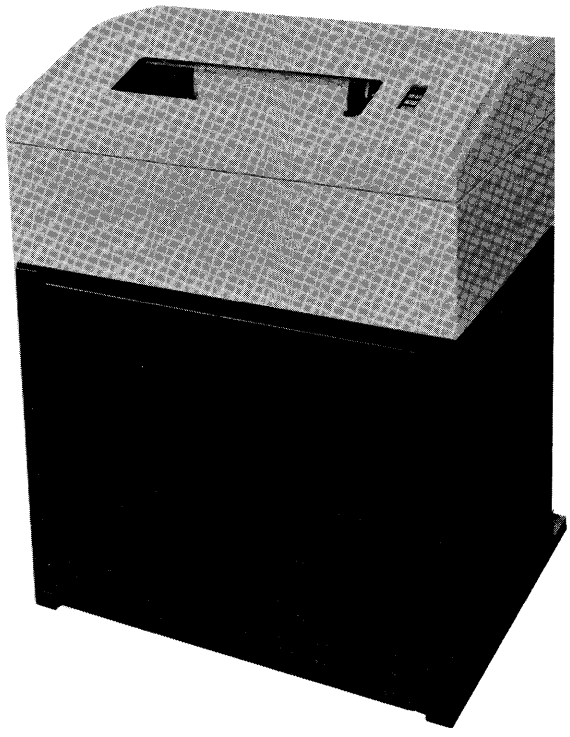


Figure 7-8 Model LP14 Line Printer

Table 7-11 LP14 Applicable Documents

Title	Number	Description
Model 2290 Line Printer Technical Manual Volume I	DPC 241746 Volume I	Detailed description of the Dataproducts Model 2290 Line Printer. Includes installation, operation, principles of operation, maintenance and troubleshooting, and microcode listing/flowchart.
Model 2290 Line Printer Technical Manual, Volume II	DPC 241746 Volume II	Detailed logic diagrams of the printed circuits, power distribution schematics, engineering drawings, mechanical drawings, and parts lists for Dataproducts Model 2290 Line Printer.
Dataproducts Engineering Drawings		
Control Logic Addendum	242869	Description of wire configuration for DEC LP14.
Print Processor Options Kit	238091	Jumper list for print processor and parts numbers list.
Direct Access Vertical Format Unit	234898	Description of DAVFU option.
Long Line Interface	239539	Description of LLI option.
Paper Motion Sensor	240682	Description of paper motion sensor option.
Form Length Selector Switch	234899	Description of forms length switch option.
Paper Puller	244671	Description of paper puller option.

7.4.2 LP14 Interface Signals

A description of the LP14 Printer interface signals is contained in Table 7-12. The printer does not check parity and does not flag parity errors, therefore DATA 8, DATA PARITY, and PARITY ERROR signals are not used.

Table 7-12 LP14 Printer Interface Signals

Signal	Function
DATA (7:1)	7-bit ASCII data to the printer for printing and DAVFU load.
READY	This signal indicates when the printer is ready to be put on-line by the operator. When READY is high, the following are true: 1. Power and dc voltages are on. 2. No fault conditions exist.
ON LINE	This signal indicates when the printer has been put on-line. When ON LINE is high, the following are true: 1. The READY signal is true; READY light is on. 2. The printer operator has actuated the ON LINE switch. 3. The PRINT INHIBIT switch is set to ONLN.
DEMAND	The DEMAND line signifies the printer is ready to accept a character; it remains high until a data strobe is received. It is disabled while the character is stored in memory and during the print operation. The DEMAND line can only come high after the operator has placed the printer on-line. DEMAND will not be asserted if DATA STROBE is true.
DATA STROBE	This line is controlled by the system to determine when the information on the data lines is to be accepted by the printer. Each time a data strobe occurs, the printer samples the data lines, and the DEMAND line is made low while the character is stored. Once a carriage control character has been transferred to the printer, the DEMAND line remains low while the characters are printed.
DAVFU READY	This signal is high when the DAVFU has been loaded correctly and no operational errors have been detected.
TOP-OF-FORM	This signal goes high when the top-of-form paper position is reached.
PAPER INSTRUCTION	This signal is high when the DAVFU is being loaded or used.

NOTE

The LP14 Printer does not accept data parity or 8-bit ASCII data characters; therefore, DATA (8), data parity, and parity error are not used. The LP20 Controller does not use the bottom-of-form or connector verify signals.

Interface signal timing is contained in Volume I, DPC 241746 (see Table 7-11).

7.4.3 LP14 Printer Specifications

A summary of LP14 printer specifications is contained in Table 7-13. The material contained in the table is for informational purposes and is subject to change without notice.

Table 7-13 LP14 Printer Specifications Summary

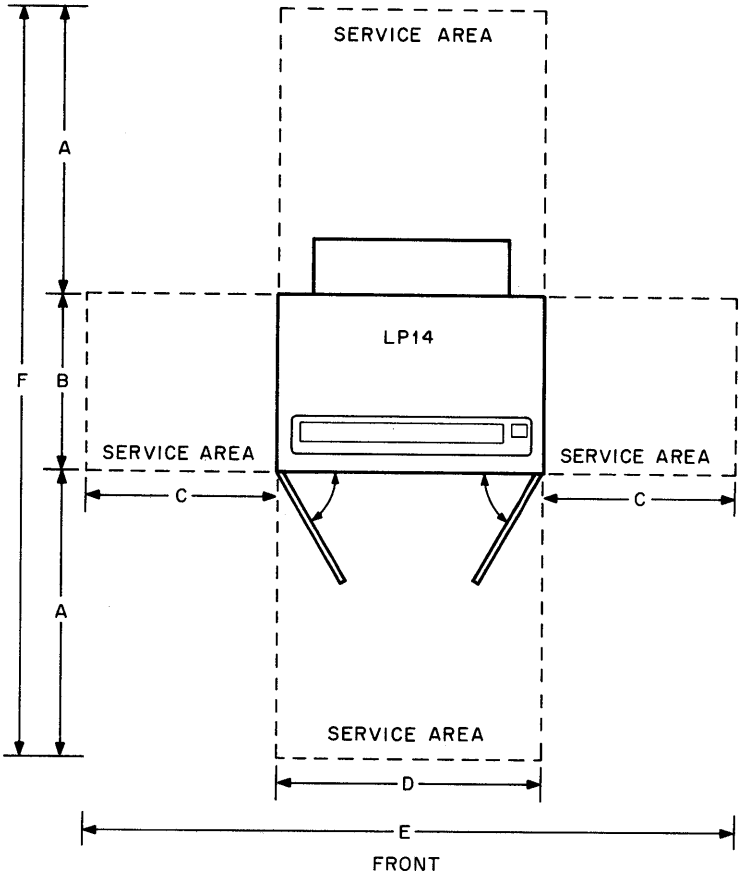
Item	Specification
Power Requirements	
Input Voltage	100, 115, 125, 200, 220, 240 Vac (± 10%)
Input Frequency	50 or 60 Hz (± 2%) (see technical manual for proper configuration)
Power Consumption	825 W max at 60 Hz 785 W max at 50 Hz
Heat Dissipation	2817 Btu/hr (60 Hz) 2681 Btu/hr (50 Hz)
Surge	120 A p-p, 30 A E-frame breaker with curve 1 rating
Environmental Requirements	
Operating Temperature	16° C (60° F) min 27° C (80° F) max
Non-operating Temperature	–18° C (0° F) min 66° C (150° F) max
Humidity (non-condensing)	
Operating	10% to 60% with static eliminator
Non-operating	5% to 95%
Physical Characteristics	
Dimensions	
Height	1.13 m (44.5 in)
Width	0.84 m (33.0 in)
Depth	0.7 m (27.5 in)
Weight	191 kg (420 lb)
Paper Requirements	
Paper	
Type	Standard fan-folded and edge-punched
Dimensions	4 in to 16.75 in wide, with 4 to 24 in between folds
Weight	
Single copy	15 lb bond (min)
Multi-copy	12 lb bond with single shot carbon for up to 6 parts

Table 7-13 LP14 Printer Specifications Summary (Cont)

Item	Specifications
Performance Characteristics	
Printable Characters	
Number	64/96
Type	ASCII code, DEC standard font: EDP/Scientific
Size	Typically 0.095 in high and 0.065 in wide
Characters Per Line	132
Character Drum Speed	
64 Character Drum	1280 r/min (min)
96 Character Drum	857 r/min (min)
Print Rates	
64 Character Drum	890 lines/min (min)
96 Character Drum	650 lines/min (min)
Character Spacing (horizontal)	0.100 (± 0.005) in between centers
Line Spacing (vertical)	0.167 (± 0.005) in (6 lines/in) 0.125 (± 0.050) in (8 lines/in)
Line Advance Time	20 ms (max)
Paper Slew Speed	30.0 in/s (min at 6 lines/in) 22.5 in/s (min at 8 lines/in)
Vertical Format	DAVFU controlled
Character Synchronization	Variable reluctance pick-up sense drum position
Interface Signals	
Input	7 Data lines 1 Data Strobe line 1 Paper Instruction line for DAVFU
Output	1 Ready line 1 Demand line 1 On-line 1 Top-of-form line 1 DAVFU Ready line
Paper Loading	Paper loaded directly on tractors from the supplier box
Paper Tensioning	1 paper tensioner bar located just below print station

7.4.4 LP14 Space Requirements

Service area space requirements for the LP14 printer are shown in Figure 7-9.



DIMENSIONS	A	B	C	D	E	F
METERS	0.9	0.6	0.6	0.8	2.1	2.4
INCHES	36	23	24	33	81	95

10-2991

Figure 7-9 LP14 Printer Space Requirements

APPENDIX A
ASCII CHARACTER SET

7-Bit Octal Code	Character	Remarks
000	NUL	Null, Tape Feed.
001	SOH	Start of Heading; also SOM, Start of Message.
002	STX	Start of Text; also EOA, End of Address.
003	ETX	End of Text; also EOM, End of Message.
004	EOT	End of Transmission (END); shuts off TWX machines.
005	ENQ	Enquiry (ENQRY); also WRU.
006	ACK	Acknowledge; also RU.
007	BEL	Rings the bell.
010	BS	Backspace; also FEO, Format Effector; backspaces some machines.
011*	HT	Horizontal Tab
012**	LF	Line Feed or Line Space (New Line); advances paper to next line.
013	VT	Vertical Tab (VTAB)
014**	FF	Form Feed to Top of Next Page.
015**	CR	Carriage Return
016	ELONG	Elongate; doubles size of horizontal printing axis.
017	SI	Shift In; changes ribbon color to black.
020	DLE	Data Link Escape
021	DC1	Device Control 1; turns transmitter (reader) on.
022	DC2	Device Control 2; turns punch or auxiliary on.
023	DC3	Device Control 3; turns transmitter (reader) off.
024	DC4	Device Control 4; turns punch or auxiliary off.
025	NAK	Negative Acknowledge; also ERR, Error.
026	SYN	Synchronous Idle (SYNC)
027	ETB	End of Transmission Block; also LEM, Logical End of Medium.
030	CAN	Cancel (CANCL)
031	EM	End of Medium
032	SUB	Substitute
033	ESC	Escape
034	FS	File Separator
035	GS	Group Separator
036	RS	Record Separator
037	US	Unit Separator

*Horizontal tab is decoded by controller which then forces a number of space codes onto the LPT data lines in succession.

**Print commands recognized by LP05-V, W line printers.

7-Bit Octal Code	Character	Remarks
040**	SP	Space
041	!	
042	”	
043	#	
044	$	
045	%	
046	&	
047	’	Accent Acute or Apostrophe
050	(	
051	)	
052	*	
053	+	
054	,	Comma
055	-	Minus
056	.	
057	/	
060	0	
061	1	
062	2	
063	3	
064	4	
065	5	
066	6	
067	7	
070	8	
071	9	
072	:	
073	;	
074	<	
075	=	
076	>	
077	?	
100	@	
101	A	
102	B	
103	C	
104	D	
105	E	
106	F	
107	G	
110	H	
111	I	
112	J	
113	K	
114	L	

7-Bit Octal Code	Character	Remarks
115	M	
116	N	
117	O	
120	P	
121	Q	
122	R	
123	S	
124	T	
125	U	
126	V	
127	W	
130	X	
131	Y	
132	Z	
133	[	
134	\	
135	]	
136	↑	
137	←	
140	`	Accent Grave
141	a	
142	b	
143	c	
144	d	
145	e	
146	f	
147	g	
150	h	
151	i	
152	j	
153	k	
154	l	
155	m	
156	n	
157	o	
160	p	
161	q	
162	r	
163	s	
164	t	
165	u	
166	v	
167	w	
170	x	

7-Bit Octal Code	Character	Remarks
171	y	
172	z	
173	{	
174	|	
175	}	This code generated by Alt mode.
176	~	This code generated by ESC key (if present).
177	DEL	Delete, Rubout

APPENDIX B
64 DATA PROCESSING (EDP) CHARACTER SET

Code (Octal)	Symbol
040	(&) or (space)
041	! (exclamation)
042	" (double quote)
043	#
044	$
045	%
046	&
047	' (single quote)
050	(
051	)
052	*
053	+
054	, (comma)
055	- (minus)
056	. (period)
057	/ (slash)
060	0 (Ø)*
061	1
062	2
063	3
064	4
065	5
066	6
067	7
070	8
071	9
072	: (colon)
073	; (semi-colon)
074	<
075	=
076	>
077	?
100	@
101	A
102	B
103	C
104	D

*Used on (SCI) scientific drums.

Code (Octal)	Symbol
105	E
106	F
107	G
110	H
111	I
112	J
113	K
114	L
115	M
116	N
117	O
120	P
121	Q
122	R
123	S
124	T
125	U
126	V
127	W
130	X
131	Y
132	Z (~~Z~~)*
133	[
134	\ (reverse slash)
135	]
136	^ (circumflex)
137	_ (underscore)

*Used on (SCI) scientific drums.

APPENDIX C
96 DATA PROCESSING (EDP) CHARACTER SET

Code (Octal)	Symbol
040	(&) or (space)
041	! (exclamation)
042	" (double quote)
043	#
044	$
045	%
046	&
047	.
050	(
051	)
052	*
053	+
054	, (comma)
055	- (minus)
056	. (period)
057	/ (slash)
060	0 (Ø)*
061	1
062	2
063	3
064	4
065	5
066	6
067	7
070	8
071	9
072	: (colon)
073	; (semi-colon)
074	<
075	=
076	>
077	?
100	@
101	A
102	B

*Used on (SCI) scientific drums.

Code (Octal)	Symbol
103	C
104	D
105	E
106	F
107	G
110	H
111	I
112	J
113	K
114	L
115	M
116	N
117	O
120	P
121	Q
122	R
123	S
124	T
125	U
126	V
127	W
130	X
131	Y
132	Z (Ƶ)*
133	[
134	\ (reverse slash)
135	]
136	^ (circumflex)
137	_ (underscore)
140	` (accent grave)
141	a
142	b
143	c
144	d
145	e
146	f
147	g
150	h
151	i
152	j
153	k
154	l
155	m
156	n
157	o
160	p
161	q
162	r

*Used on (SCI) scientific drums.

Code (Octal)	Symbol
163	s
164	t
165	u
166	v
167	w
170	x
171	y
172	z
173	{ (brace)
174	| (vertical bar)
175	} (brace)
176	~ (tilde)
177	←

APPENDIX D
PRINTER CODE CHART

CODE CHART

Printer Instruction 2^6 2^5 2^4	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1	1 0 0	1 0 1
2^3 2^2 2^1 2^0							(1)	(1)	(2)	(2)
0 0 0 0		SPACE	0	@	P			p	CH 1	STEP 0
0 0 0 1		!	1	A	Q		a	q	CH 2	STEP 1
0 0 1 0		”	2	B	R		b	r	CH 3	STEP 2
0 0 1 1		#	3	C	S		c	s	CH 4	STEP 3
0 1 0 0		$	4	D	T		d	t	CH 5	STEP 4
0 1 0 1		%	5	E	U		e	u	CH 6	STEP 5
0 1 1 0		&	6	F	V		f	v	CH 7	STEP 6
0 1 1 1		'	7	G	W		g	w	CH 8	STEP 7
1 0 0 0		(	8	H	X		h	x	CH 9	STEP 8
1 0 0 1		)	9	I	Y		i	y	CH 10	STEP 9
1 0 1 0	PF	*	:	J	Z		j	z	CH 11	STEP 10
1 0 1 1		+	;	K	[		k	{	CH 12	STEP 11
1 1 0 0	FF	,	<	L	\		l	|	ILLEGAL	STEP 12
1 1 0 1	CR	-	=	M	]		m	}	ILLEGAL	STEP 13
1 1 1 0		.	>	N	↑		n	¬	ILLEGAL	STEP 14
1 1 1 1		/	?	O	←		o	□	ILLEGAL	STEP 15

Data Bit Magnitudes	**Line Printer Data Bit**
Not Used	DATA 8
2^6	DATA 7
2^5	DATA 6
2^4	DATA 5
2^3	DATA 4
2^2	DATA 3
2^1	DATA 2
2^0	DATA 1

(1) 96-character drums only. These codes print as “spare” when 64-character drums are installed.

(2) VFU Format Codes

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