DEC-11-HGTVA-B-D

GT40 graphic display terminal volume 1

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CHAPTER 1
INTRODUCTION

1.1 PURPOSE AND SCOPE

This manual describes the purpose and use of the GT40 Graphic Display Terminal. The following information is also included: installation, theory of operation, diagnostic programming, and maintenance information and procedures.

1.1.1 Related Documents

The reader must have access to the applicable engineering drawings listed in Chapter 5. Volume 2 of this manual contains the description of the PDP-11/05, the central processor unit for the GT40; the *GT40 User's Guide* features material of interest primarily to the operator and programmer.

1.2 GENERAL DESCRIPTION

The GT40 Graphic Display Terminal (Figures 1-1 and 1-2) is a high-performance graphic display system that operates through a VT40 (PDP-11/05) computer. The GT40 is designed for applications that require both a visual display and a computation capability. The system can display either alphanumeric information, graphic data such as drawings, diagrams, and patterns, or any combination of these. It is particularly valuable for displaying dynamic, fast-changing data such as waveforms. The GT40 can function as a general purpose computer when not performing as a display terminal. In this nondisplay mode of operation, it can operate as a stand alone system or initiate communications with a host computer as part of a computer network.

1.3 SYSTEM ORGANIZATION

The GT40 consists of eight basic components organized to form the system described in Paragraph 1.2. These components are:

- KD11-B Central Processor Unit (CPU) (VT40 version of the PDP-11/05/10)
- Display Processor Unit (DPU) in which is included the Bootstrap Read Only Memory (ROM)
- Communications Interface Module
- Memory
- Keyboard
- Cathode Ray Tube (CRT) Monitor
- Light Pen
- Power Supply

1.3.1 Central Processor

The CPU is a KD11-B (PDP-11/05), 16-bit processor with a standard PDP-11 instruction set capability. It is interfaced to the LK40 Keyboard and the Unibus. Any of the standard PDP-11 peripheral devices can be connected to the Unibus; this allows for high versatility when the GT40 operates as a stand alone device. Volume 2 of this manual contains a complete description of the CPU.

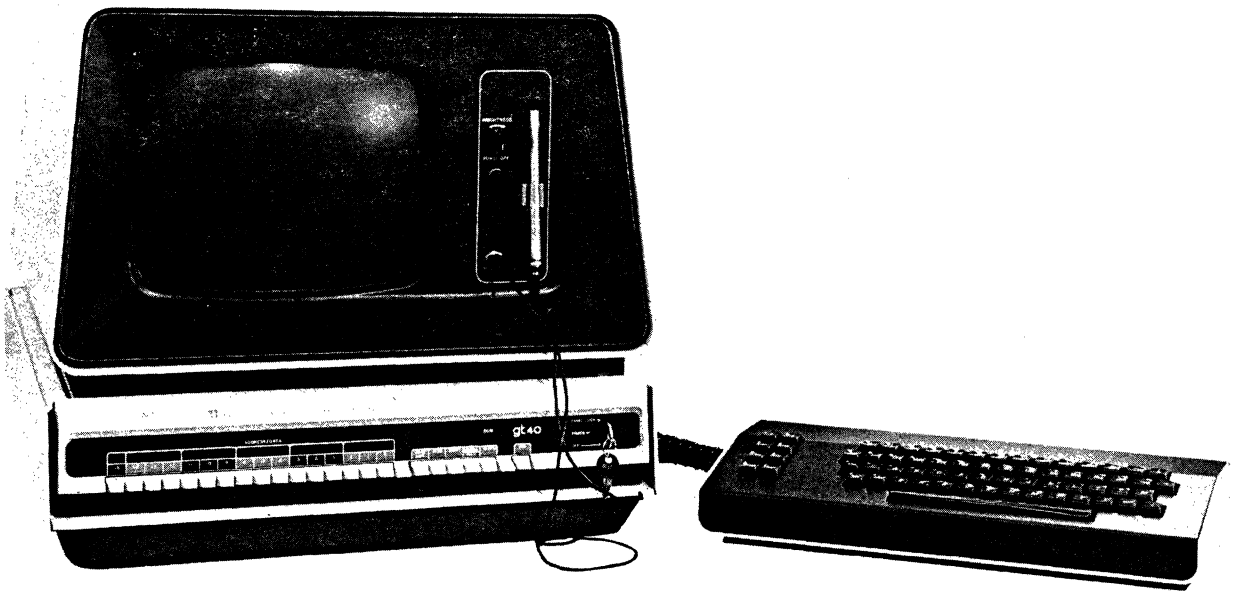


Figure 1-1 GT40 Graphic Display Terminal

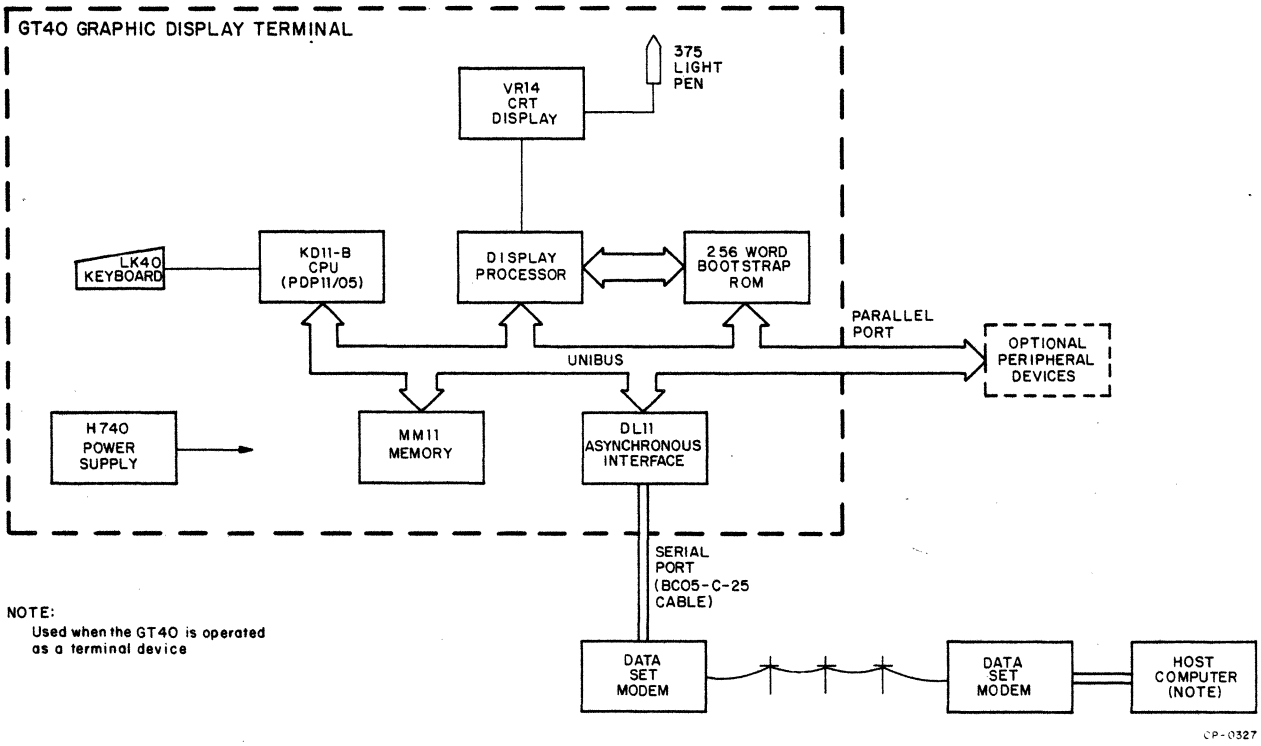


Figure 1-2 GT40 Graphic Display Terminal, System Block Diagram

1.3.2 Display Processor

Considered to be the focal point for GT40 operations, the DPU retrieves display data and commands from the MM11 Core Memory. The DPU decodes and executes this information and carries out all vector and character calculations that are required by the CRT monitor for display presentations. The DPU contains Unibus control, data and instruction processor, vector generator, and character generator circuits. The Bootstrap ROM is physically located in the display processor. It contains the Bootstrap Loader program required to start the display program or initiate communications with a host computer.

1.3.3 Communications Interface Module

The DL11 Asynchronous Line Interface is a character-buffered communications interface designed to assemble or disassemble the serial information required by a communications device for parallel transfer to, or from, the PDP-11 Unibus. The interface consists of a single integrated circuit quad module containing two independent units (receiver and transmitter) capable of simultaneous 2-way communication.

The DL11 Interface provides the logic and buffer register necessary for program-controlled transfer of data between a PDP-11 system requiring parallel data and an external device requiring serial data. The interface also includes status and control bits that can be controlled by the program, the interface, or the external device for command, monitoring, and interrupt functions.

1.3.4 Memory

The core memory is the storage device for both the PDP-11/05 central processor and the GT40 display processor. Stored in it are the instructions and data necessary for the operation of both processors. Although this memory and the Bootstrap ROM perform similar roles in the GT40 operation, they are not physically or logically associated with each other.

The MM11-K provides 4096 (4K) 16-bit words of core storage; the MM11-L provides 8192 (8K) 16-bit words of core storage. Both memory configurations require three standard 8.5-in. wide modules: two are hex height and one is quad height.

The G110 hex height module contains the control logic, inhibit drivers, sense amplifiers, and 16-bit data registers; the G231 hex height module contains the address selection logic, current generator, and switches and drivers. Pin-to-pin compatibility exists between the C, D, E, and F connectors on both these modules and the stack module connectors. The pins on the A and B connectors of both these modules are also compatible with the standard Unibus pin assignments.

The GT40 is capable of storing up to 8192 words internally, with an address range of 28K words.

Volume 2 of this manual contains a detailed description of the memory.

1.3.5 Keyboard

The LK40 Keyboard is a free standing, enclosed assembly consisting of a 58-key major keyboard and an 8-key minor keyboard encoding into either 96 or 128 ASCII codes. The keyboard has both shift and control keys to modify the ASCII bit pattern appropriately.

The output of the keyboard is approximately 110 baud, 10-bit serial, 20 mA current loop.

A keyboard ENABLE/DISABLE switch is provided at the rear of the box for operator convenience.

1.3.6 Cathode Ray Tube Monitor

The VR14 is a completely self-contained CRT display that provides a 6.75 in. by 9 in. viewing area in a compact package. The VR14 requires only analog X and Y position information and intensity signals to generate sharp, bright displays. Except for the CRT itself, the unit is composed of all solid state circuits, utilizing high speed magnetic deflection to enhance brightness and resolution.

In addition, the VR14 construction is modular for easy maintenance. Any subassembly or major component can be replaced in minutes using only a screwdriver.

1.3.7 Light Pen

The 375 Light Pen is a pencil-shaped light detector for use by the operator in a wide range of interactive applications.

The 375 uses a photo-sensitive transistor for high gain and fast response. In addition, an infrared doped phosphor and matching spectral response in the photo-detector used in the 375 yields very good light pen capability, without the normally attendant visual flicker of the fast phosphor component.

The 375 is connected to the GT40 by a flexible cable attached to the front panel of the CRT monitor; it is easily removed by simply unplugging it from the CRT panel.

1.3.8 Power Supply

The H740 Power Supply is a forced air cooled unit that converts single phase, 115V to 230V, nominal 47–63 Hz line voltage to the three regulated output voltages required by the computer. The output voltages and their principal usages and characteristics are: +15V for communications circuits (series regulated, overcurrent protected); +5V for IC logic (switching regulated, overvoltage, and overcurrent protected); and -15V for core memory (switching regulated, overvoltage, and overcurrent protected). The supply is used with the BC05HXX (115V) or BC05JXX (230V) Power Control Assemblies which contain a line cord, circuit breaker, and RFI capacitors.

The power supply circuitry also generates BUS ACLO L and DCLO L power fail early warning signals and the LTC L line frequency clock synchronizing signal. A thermal control mounted on the heat sink will interrupt the AC input if the heat sink temperature becomes excessive due to fan failure or other cause.

The power supply is comprised of three major subassemblies and two cables: the power control, power chassis assembly, dc regulator module, dc cable, and ac cable.

Volume 2 of this manual contains a detailed description of the H740 Power Supply.

1.4 SYSTEM OPERATION

The GT40 is a stable system, that requires only minimum adjustments because it employs a combination of digital and analog techniques as opposed to analog circuits alone. The vector function operates efficiently, providing a good compromise of speed and accuracy and assuring a precise digital vector calculation. The presentation and accumulation of vectors means that every point of a vector is available in digital form.

After plotting each vector, the end-point position is automatically updated, preventing accumulated errors or drift. Four different vector types – solid, long dash, short dash, and dot dash – are possible through standard hardware.

The GT40 character generator has both upper and lower case capability with a large repertoire of displayable characters. The display is the automatically refreshing type rather than the storage type so that a bright, continuous image, with excellent contrast ratio, is provided during motion or while changes are being made in the elements of the picture. A hardware blink feature is applicable to any characters or graphics drawn on the screen. A separate line clock in the display permits the GT40 to be synchronized to a line frequency of 60 Hz. Scope resolution is precise enough to allow overprinting.

The terminal includes logic for descender characters such as "p" and "g", positioning them correctly with respect to the text line. In addition to the 96 ASCII printing characters, 31 special characters are included which are addressed through the shift-in/shift-out control codes. These special characters include some Greek letters, architectural symbols, and math symbols. Characters can be drawn in italics simply by selecting the feature through the status instruction bit. Eight intensity levels permit the brightness and contrast to be varied so that the scope can be viewed in a normally lighted room.

The instruction set consists of four control-state instructions and five data-state formats. The control instructions set the mode of data interpretation, set the parameters of the displayed image, and allow branching of the instruction flow. Data can be interpreted in any of five different formats, allowing multiple tasks to be accomplished efficiently from both a core usage and time standpoint. The graph/plot feature of the GT40 automatically plots the x or y axis according to preset distances as values for the opposite axis are recorded.

1.5 EQUIPMENT SPECIFICATIONS

The GT40 Graphic Display Terminal operating requirements and physical characteristics are listed by component in the following paragraphs. Refer to Volume 2 for the specifications pertaining to the KD11-B Processor (PDP-11/05).

1.5.1 Display Processor

Instruction Word Length	16 bits
Raster Definition	10 bits
Viewable Area	x = 1024 raster unit (1777_8) y = 768 raster units (1377_8)
Paper Size	12 bits
Hardware Blink	Programmable
Hardware Intensity Levels	8
Line Frequency Synchronization	Hardware programmable
Character Font	6 X 8 dot matrix
Characters/Line	73 (85 possible)
Number of Lines	31
Character Set	96 ASCII – upper and lower case plus 31 specials (Greek letters, math symbols, etc.) (Refer to Appendix C)
Control Characters	Carriage return Line feed Backspace
Bell Tone	Programmable
Italics	Hardware programmable
Line Type	Solid Long dash Short dash Dot-dash

Data Formats	Character (2 char/word) Short Vector (1 word) Long Vector (2 words) Point (2 words) Relative Point (1 word) Graphplot x/y (1 word/pt)
DPU Instructions	Set Graphic Modes Jump No operation (NOP) Load Status Register A Load Status Register B

1.5.2 DL11 Communications Interface Operating Specifications

Data Input and Output		Serial data, EIA and CCITT specifications compatible with Bell 103 and 202 Data Sets
Data Format		1 start bit; 5, 6, 7, 8 data bits; 1, 1.5 or 2 stop bits; odd or even parity.
Power Required		1.8A @ +5V 0.150A @ -15V 0.050A @ +9 to +15V
Cable Length	EIA	All baud rates: 50 ft (15.24m)
Noise Margin	EIA	5V

1.5.3 MM11 Core Memory (refer also to Volume 2)

Type	Magnetic core, read/write, coincident current, random-access
Organization Capacity	Planar, 3D, 3-wire
Access Time	
DATI	400 ns
DATIP	400 ns
DATO, DATOB	200 ns
Cycle Time	
DATI	900 ns
DATIP	450 ns
DATO, DATOB (PAUSE L)	900 ns
DATO, DATOB (PAUSE H)	450 ns

1.5.4 LK40 Keyboard

Number of Keystations	58 (Major board) 8 (Minor board)
Encoding Format	1968 USASCII
Number of Codes	Either 96 or 128 codes (internal switch controllable)
Output Data Format	8-bit ASCII 1 start bit 7 data bits 2 stop bits
Baud Rate	Approximately 110 baud
Output Signal	20-mA current loop
Bell	Tone generator
Controls	Enable/Disable transmit

1.5.5 CRT Monitor (refer also to Paragraph 3.5.3)

Viewable Area	6.75 X 9 in. (17.145 X 22.86 cm)
Brightness	> 30 fL (measured using a shrinking raster technique)
Contrast Ratio	> 10:1
Phosphor Type	P39 doped with IR
Pincushion	±1% of full scale to best-fit line
Spot Size	< 20 mils inside the usable screen area at a brightness of 30 fL, full width at half maximum (FWHM)
Jitter	< ±1/2 spot diameter
Repeatability	< ±1 spot diameter (repeatability is the deviation from the nominal location of any given spot)
Gain Change	From a fixed point on the screen, less than ±0.3% gain change for each ±1% line voltage variation
Temperature Range	0 to 50°C (operating)
Relative Humidity	10 to 90% (noncondensing)
Linearity	Maximum deviation of any straight line will be < 1% of the line length measured perpendicular to a best-fit straight line
Deflection Method	Magnetic (70° diagonal deflection angle)
Focus Method	Electrostatic

High Voltage	10.5 kV dc nominal (voltage proportional to input line voltage). Supply is self-contained and equipped with a bleeder resister
Shielding	CRT is fully enclosed in a magnetic shield
Overload Protection	Unit is protected against fan failure or air blockage by thermal cutouts. Power supply and amplifiers are current limited. Phosphor protection is provided against fault conditions

1.5.6 Light Pen

Length	5.0 in. (12.7 cm)
Diameter	0.45 in. (tapered to 0.35 in.) (1.143 cm) (0.889 cm)
Light Sensing	Phototransistor
Connector	Phone Plug
Signal Amplification	G840 Light Pen Amplifier Module in VR14 CRT Display

1.5.7 Power Supply

Refer to Volume 2 for a detailed list of power supply specifications.

1.5.8 Environmental

Shock, Nonoperating	DEC STD 102, 205 at 30 ± 10 ms half-sine
Vibration, Nonoperating	DEC STD 102, Vertical 1.89 G rms 10–300 Hz
Operating Ambient Temperature	DEC STD 102, Class A, 60–95°F (16–35°C)
Relative Humidity (noncondensing)	DEC STD 102, Class 2, 20–80%

1.5.9 Physical

Weight	
CRT Monitor	80 lb (36.24 kg)
Processor Cabinet	60 lb (27.18 kg)
Keyboard	6.25 lb (2.83 kg)

Size	Height	Width	Depth
CRT Monitor	12.5 in. (31.75 cm)	19.75 in. (50.165 cm)	22.25 in. (56.515 cm)
Processor Cabinet	5.25 in. (13.335 cm)	19.75 in. (50.165 cm)	23.25 in. (59.055 cm)
Keyboard	3.0 in. (7.62 cm)	16.625 in. (42.227 cm)	6.625 in. (16.827 cm)

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

This chapter provides installation planning considerations and site preparation recommendations; physical, electrical, and environmental requirements; and installation, inspection, and acceptance procedures.

2.2 SITE PLANNING

The GT40 is housed in a compact, self-contained cabinet that can be placed on a table, desk, or bench top.

The customer should determine the location of the GT40 installation prior to shipment. Items of major importance are: the location of the GT40 in relation to work flow requirements within the work area; provision for and availability of adequate power; type of system to which the GT40 will be interfaced; fire and personnel safety precautions; and proper environmental conditions. Operating, environmental, and physical characteristics and system specifications for the GT40 are provided in Chapter 1.

2.3 INSTALLATION

2.3.1 Unpacking

The GT40 is packed in three (3) specially designed shipping cartons to prevent damage during shipment. The contents of each carton are listed in Table 2-1.

NOTE

Any damage to the GT40 should be noted and reported immediately to the DEC Field Service representative.

The equipment arrangement described in the following paragraphs is intended only for initial acceptance checks and for maintenance tests and adjustments.

Table 2-1
Contents of GT40 Shipping Cartons

Box 1/3 VR14 Cabinet	Box 2/3 PDP-11/05 Cabinet	Box 3/3 Accessories
VR14 CRT Display Monitor Power Control (Attached to VR14)	PDP-11/05 Central Processor Unit MM11 L/K Memory DL11 Asynchronous Line Interface GT40 Display Processor H740 Power Supply BC05-C DL11 Communications Cable 7008993 Display Cable	LK40 Keyboard 375 Light Pen GT40 Print Set, manuals, etc. (Refer to A-AL-GT40-0.)

2.3.1.1 **Unpacking the PDP-11/05 Cabinet (Box 2 of 3)** – The PDP-11/05 should be unpacked first. Open box 2 and carefully remove the PDP-11/05 according to the procedure that follows. Note that the PDP-11/05 has side extrusions and a backplate (Figure 2-1). This one piece assembly slides onto the chassis tracks that are attached to the PDP-11/05 cabinet; the extrusion and backplate assembly is not attached to the cabinet proper.

CAUTION

The PDP-11/05 cabinet will slide out of the extrusion and backplate assembly and be damaged if the front end of the PDP-11/05 is allowed to tilt down when the unit is lifted from the shipping container.

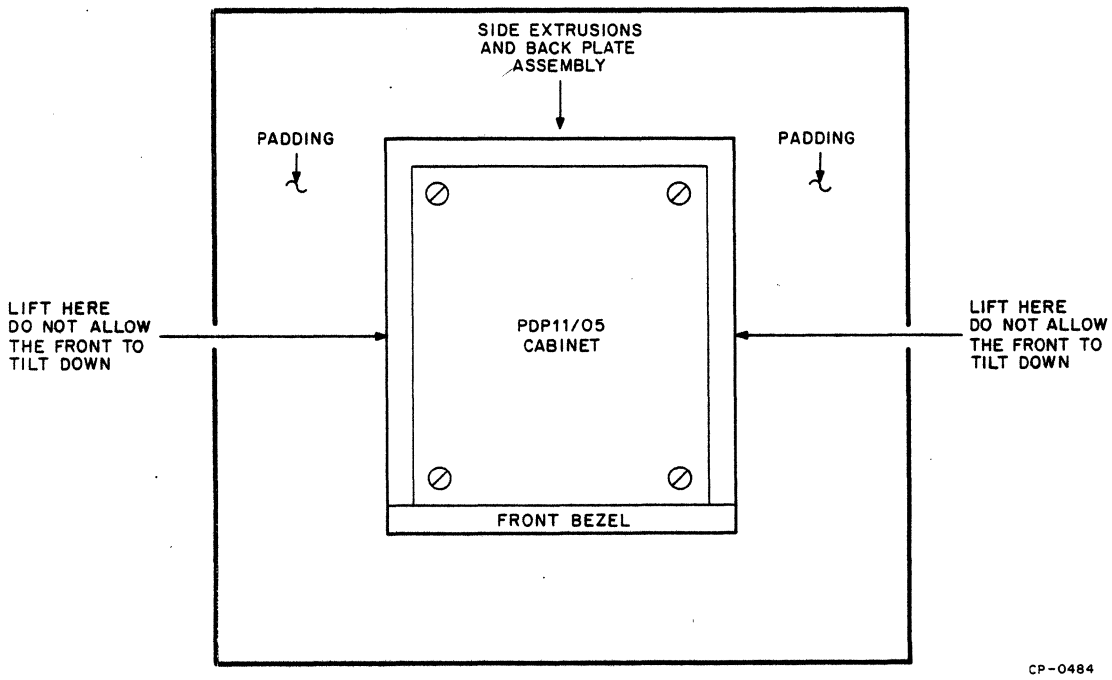


Figure 2-1 GT40 Shipping Container, Box 2 of 3

1. Remove all the padding from around PDP-11/05 cabinet.

2. Locate a sturdy table that is large enough to hold both the PDP-11/05 cabinet and the VR14 cabinet side by side.

NOTE

The total weight of both the PDP-11/05 and VR14 cabinets is about 160 lb.

3. Grasp the PDP-11/05 by the side extrusions and carefully lift it out of the shipping container. Place the cabinet on the left side of the table (Figure 2-2) so that the adjustments are easily accessible.

4. Remove the extrusion and backplate assembly by pulling it away from the rear of the PDP-11/05 cabinet.

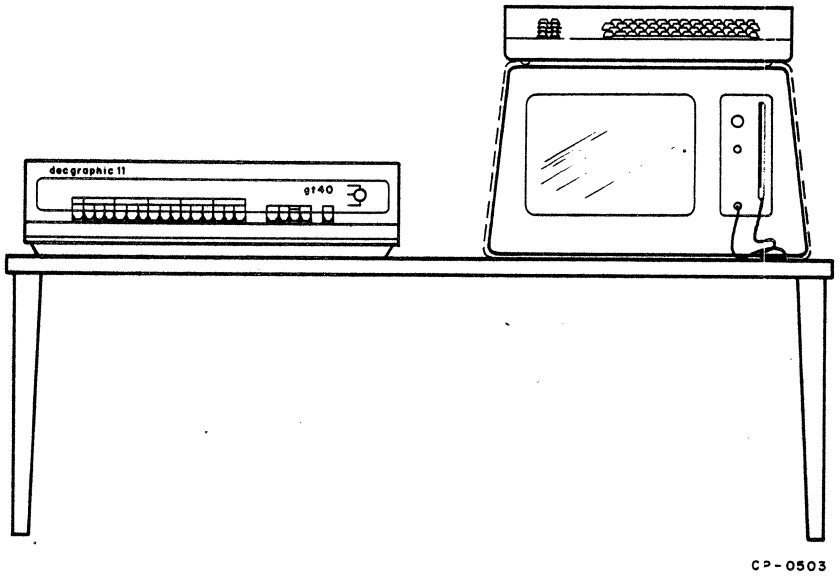


Figure 2-2 Positioning the PDP-11/05, VR14, and LK40 for Adjustments

2.3.1.2 Unpacking the VR14 Cabinet (Box 1 of 3) – The VR14 is the next GT40 component to be unpacked.

WARNING

Installation and maintenance procedures should be performed by qualified service personnel only.

High voltages are present within the unit and, under certain conditions, are potentially dangerous. All electrical safety precautions must be observed.

Inherent implosion protection is employed in the CRT design; however, the tube may be damaged if it is subjected to rough treatment or dropped while being removed from or installed in the display. Exercise caution during these operations (Paragraph 4.4.5).

Open box 1 and unpack the VR14 according to the following procedures:

1. Remove the padding from around the sides and rear of the VR14 cabinet. (Do not remove the protective padding from the face of the CRT at this time.)

2. Carefully remove the VR14 from the shipping box and place it on the table immediately to the right of the PDP-11/05 cabinet (Figure 2-2).

3. Make certain that there is sufficient air flow for both cabinets (the VR14 requires 1 in. below and 2 in. to the rear of free air space).

4. Remove the rear panel (four (4) Phillips head screws) from the VR14.

5. Remove the six (6) Phillips head screws that fasten the sides of the top cover to the VR14 lower extrusions (Tinnerman nuts are wedged into these extrusions). Carefully lift the top cover from the VR14 and place it to one side.

6. Remove the tape and padding from the face of the CRT.

NOTE
Do not turn on any power at this time.

2.3.1.3 Unpacking the Accessories (Box 3 of 3) – The accessories box is unpacked last. Open the box and follow the procedures given below:

1. Locate the smaller box marked LK40 Keyboard. Unpack this box and place the keyboard on top (and to the front) of the VR14 as shown in Figure 2-2.

2. Locate the light pen packed in box 3. Unpack and attach to the VR14 front panel connector.

3. Remove the GT40 print set from box 3 and refer to the interconnect diagram, D-IC-GT40-0-3, for the cable connections described in the following paragraphs. These connections are also shown in Figure 4-26; scope cable connectors are identified in Figure 3-70.

4. Remove the top cover from the PDP-11/05 cabinet. This cover is fastened by four (4) quarter-turn fasteners.

5. Remove the left side panel from the PDP-11/05. This panel is fastened by four (4) Phillips head screws.

6. The A320 GT40 Display Generator module can now be observed in the top slot of the PDP-11/05. A 23-wire cable (part of the scope cable, 7008993), terminated in a 40-pin Berg connector (P-3), is preconnected (letters up) to the left side of the module (Figure 4-1). Check the connector for proper seating. Another group of seven wires in the scope cable is terminated in a second 40-pin Berg connector (P-4). P4 should be connected, letters up, to the PDP-11/05 SCL line at the lower rear of the PDP-11/05 cabinet. Terminations at the opposite end of the scope cable consist of a 24-pin Amphenol connector (P-1) and a 3-pin Mate-N-Lok connector (P-2). P2 is plugged into the GT40 Power Control box mounted on the rear panel of the VR14. P1 is connected to its mate on the rear panel of the VR14. Check all these connections for proper seating.

7. Connect the 14-pin Amphenol connector (P-2) on the keyboard cable (7008959) to its mate on the VR14 rear panel.

8. Power to the PDP-11/05 is via the power cord which should be plugged into the power outlet on the bottom of the power control box on the VR14 rear panel. It is necessary to tilt the VR14 slightly in order to have access to the outlet. Hold the LK40 Keyboard when doing this to prevent it from sliding off the top of the VR14.

9. Determine that the short power cord from the right side of the power control box is connected to the VR14.

10. An M7800 module (DL11) is in slot 4 of the PDP-11/05 cabinet. Connected to this module should be a 27-wire cable (BC05-C-25) terminated in a 40-pin Berg connector. The other end of this cable terminates in a 25-pin Cinch connector. Insert the Cinch connector into a modem test connector during acceptance testing or when performing maintenance checks.

NOTE
Recheck all cable connections for proper seating.

Table 2-2 is a list of all GT40 cables and their use.

Table 2-2
GT40 Cable Interconnections

Cable	Use	Termination	Connect To
7008993	Scope Cable	7 wire, 40-pin Berg 23 wire, 40-pin Berg 24 pin Amphenol 3 pin Mate-N-Lok	PDP-11/05 SCL A320 Display Generator Module VR14 CRT Display Monitor Power Control Box (VR14)
BC05-C-25	DL11 Comm. Cable	40-pin Berg 25-pin Cinch	M7800 Asyn. Line Interface Modem
7008959	LK40 Keyboard Cable	14-pin Amphenol 6-wire #18 AWG	VR14 CRT Display Monitor M7011 Control Module (LK40)
7008960	Keyboard Cable	40-pin Berg 40-pin Berg	M7011 Control Module (LK40) 5409945 Large Keyboard
7008612-10	Intra-Keyboard Cable		5409945 Large Keyboard 5410229 Small Keyboard

2.3.2 GT40 Quick Verify

An initial operational test of the GT40 is performed at this time using GT40 Quick Verify Test, MAINDEC-11-DDGTE-A. The GT40 is shipped from the factory with this program in core memory. The Quick Verify procedure is described in the following paragraphs.

CAUTION
Before proceeding, ensure that the GT40 model on hand is correct for the available site power.

1. **Examine the back of the processor box. Locate the H400 Power Control. The voltage frequency will be written on the power control.**

2. **Examine the back of the CRT monitor. The line voltage will be printed above the ac input receptacle.**

Site power must be capable of 15A at 110V ± 10% or 8A at 220V ± 10%, 47 to 63 Hz.

Computer systems are often sensitive to interference present on some ac power lines. If the GT40 is to be installed in an electrically "noisy" environment, it may be necessary to condition the ac power line. DEC field service engineers can assist in determining if the ac line is satisfactory.

1. Plug the power cable extending from the left side of the VR14 Power Control box into a wall receptacle. Verify that the communication test plug is attached to the BC05-C-25 modem cable.

2. Turn the ON/OFF BRIGHTNESS control on the VR14 front panel clockwise. The VR14 should not turn on at this time because the power control has not yet been energized.

3. Determine that the two maintenance switches on the M7013 module (slot 2 of the PDP-11/05 backplane, Figure 4-27) are in the OFF position. The OFF position is toward the fingers of the module. Figure 2-3 shows the placement of these switches on the M7013 module. Note that a white dot is visible when the switch is in the OFF position.

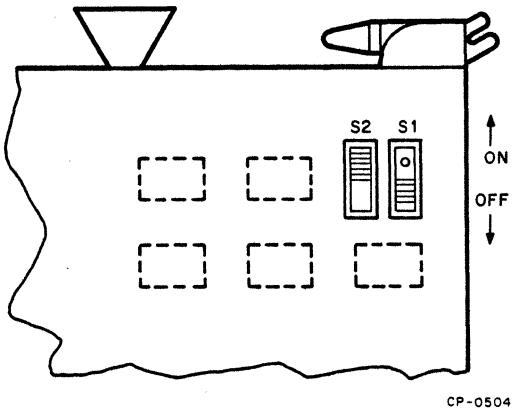


Figure 2-3 Maintenance Switches, M7013 Module

4. Apply power to the GT40 by turning the key switch on the PDP-11/05 front panel to the POWER position. Both the VR14 and the PDP-11/05 should now be turned on.

5. Select the starting address for the program by placing 200_8 in the switch register (SR).

6. Follow Steps 3 through 7 in Paragraph 4.2.6.2.

7. If the program does not run, or the display is incorrect, proceed to Paragraph 2.3.4. If the display is satisfactory proceed to Paragraph 2.3.9.

2.3.3 GT40 Maintenance Restrictions

The GT40 is normally shipped without a teletypewriter. This necessitates the use of the Field Service cassette recorder (PMK02A, PMK02C) and a PDP-11/05, 11/45, M7800 Adapter Cable (Part No. 93-05542) to provide the ability to load programs used during installation and maintenance periods. The adapter cable is terminated in a 50-pin Cinch connector and a 40-pin Berg connector.

Program loading of the GT40 can be accomplished by performing the procedure described in Paragraph 4.2.6.1.

2.3.4 CPU and Memory Diagnostics

All CPU and memory diagnostics should be run at this time. These tests must be run completely and successfully before continuing GT40 installation. (Use of the Field Service cassette loader is described in Paragraph 2.3.3.) When all tests can be run without errors, proceed with the installation by checking the DL11 Asynchronous Line Interface (Paragraph 2.3.5).

2.3.5 DL11-E, C/D Off-Line Test (MAINDEC-11-DZDLA)

This program tests the GT40 interface circuits. Follow the procedure described in Paragraph 4.2.6.6.

Do not remove the modem test connector when testing is completed. Proceed with the installation by performing Instruction Test No. 1 (Paragraph 2.3.6).

2.3.6 Instruction Test No. 1 (MAINDEC-11-DDGTA-A)

Checks of all registers and interrupt vectors are conducted when this program is run. Follow the operating instructions listed in Paragraph 4.2.6.3.

After testing is completed, place the two M7013 module maintenance switches in the OFF position and continue with the installation checks in Paragraph 2.3.7.

2.3.7 Instruction Test No. 2 (MAINDEC-11-DDGTB-A)

This is a continuation of the testing performed in Instruction Test No. 1 (Paragraph 2.3.6). The procedure is described in Paragraph 4.2.6.4. After the tests have been satisfactorily completed, continue with the installation procedure in Paragraph 2.3.8.

2.3.8 ROM Bootstrap Loader Test (MAINDEC-11-DDGTD-A-D)

The Bootstrap Loader program is verified when this test is run. Follow the procedure described in Paragraph 4.2.6.7 and then continue with the installation in Paragraph 2.3.9.

2.3.9 DL11, BC05-C-25, LK40, and ROM Bootstrap Quick Verification (Character Echo)

A reliability check of the GT40 interface is accomplished when this check is performed. The procedure is described in Paragraph 4.2.6.8. Do not remove the modem test connector from the BC05-C-25 cable when the check is finished; continue with the installation in Paragraph 2.3.10.

2.3.10 Display Processor Testing, Visual Display Test (MAINDEC-11-DDGTC-A)

This program generates a wide variety of display patterns with which the operator can evaluate GT40 display functions and make necessary adjustments. The operating procedure is presented in Paragraph 4.2.6.5. (Use of the Field Service cassette loader is described in Paragraph 2.3.3). Allow the program to cycle for 1 hour before turning the LK40 Keyboard switch to the ON position (step 5) and completing the test.

This concludes the testing of the GT40.

2.3.11 Final Preparation for Operational Use

The GT40 is now ready for the final assembly steps which prepare the unit for operational use. These steps are described in the following procedure.

1. Press HALT and turn the PDP-11/05 front panel console key to the OFF position.

2. Disconnect the power input cable to the left side of the power control box (on the VR14 rear panel) from the wall receptacle.

3. Disconnect the keyboard cable on the VR14 rear panel. Lift the LK40 Keyboard off the VR14 and place it to one side.

4. Disconnect the 375 Light Pen and place it to one side.

5. Disconnect the 3-pin Mate-N-Lok connector (P2) from the power control box and the 24-pin Amphenol connector (P1) from the VR14 rear panel. Do not disconnect the other two (Berg) connectors on the scope cable (7008993).

6. Attach the PDP-11/05 cabinet left side panel with the four (4) Phillips head screws that were removed during the initial assembly procedure (Paragraph 2.3.1.3, step 5).

7. Attach the PDP-11/05 top cover with the four (4) quarter-turn fasteners that were removed during the initial assembly procedure (Paragraph 2.3.1.3, step 4).

8. Locate the chassis tracks mounted on the sides of the PDP-11/05 cabinet. Slide the extrusion and backplate assembly onto these tracks.

9. Carefully lift the VR14 and place it into the guides on the extrusion and backplate assembly. (Refer to drawing D-IC-GT40-0-3.) Make sure both lower extrusions on the VR14 fit properly into the extrusion and backplate assembly. No bolts are required, the weight of the VR14 is sufficient to hold the extrusion and backplate assembly in the proper position.

10. At this time, place the GT40 Cover Assembly on the VR14 so that it rests on the VR14 lower extrusions.

11. Position the cover so that the six holes in the cover line up with the Tinnerman nuts wedged into the VR14 lower extrusions.

12. Fasten the cover assembly to the VR14 lower extrusions with the six (6) screws previously removed (Paragraph 2.3.1.2, step 5).

13. Connect the 14-pin Amphenol connector on the keyboard cable to the proper connector on the VR14 rear panel. Plug the phone plug on the 375 Light Pen Cable into the VR14 front panel and connect the 3-pin Mate-N-Lok connector on the scope cable into the receptacle on the power control box.

14. Check all cable connections for proper seating.

15. Attach the VR14 rear panel with the four screws previously removed (Paragraph 2.3.1.2, step 4).

16. Plug the ac power cord on the power control box into the wall receptacle and turn the console key switch to the ON position.

17. The Visual Display Test (MAINDEC-11-DDGTC) is still resident in memory. Place 200_8 in the SR, press LOAD ADDRESS and START. All or part of this test can now be run as a final GT40 operational check.

18. Press HALT. Remove the modem test connector and connect the BC05-C-25 cable as required. The GT40 is now ready for the customers use.

CHAPTER 3
THEORY OF OPERATION

3.1 INTRODUCTION

This chapter provides the user with the operational theory needed to understand and maintain the GT40 Graphic Display Terminal. The *GT40 User's Guide* contains programming information relating to the material in this chapter and should be referred to as required.

The description in the following paragraphs is separated at the major GT40 component level, i.e., display processor, keyboard, CRT display, etc. It is intended to present the reader with the information necessary to understand normal system operation. Understanding this information is a prerequisite in analyzing trouble symptoms and determining necessary corrective action.

A complete set of engineering drawings and circuit schematics is provided in *GT40 Engineering Drawings,* DEC-11-HGTEA-A-D. The general logic symbols used on these drawings are described in the *DEC Logic Handbook,* 1971. Specific symbols and conventions are also included in the *PDP-11 Conventions Manual,* DEC-11-HR6B-D, and in certain PDP-11 system manuals. Instruction flow diagrams for both control instructions and data words are also included in the engineering drawing set. The purpose of the flow diagrams is to illustrate the sequential operations that take place when instructions and data words are executed. The individual steps in the diagrams itemize events or conditions that are necessary to complete the entire instruction. They also provide keys as to where the applicable logic is located in the drawing set. Only the main operations and decisions are shown, however, in order that the diagrams not be overdetailed and therefore cumbersome. More detailed flow diagrams are also included in this manual, where necessary, to explain complex procedures. The following paragraphs describe the signal nomenclature conventions used on the drawing set.

Signal names in the GT40 print set are in the following basic form:

SOURCE SIGNAL NAME POLARITY

SOURCE indicates the drawing number of the print set where the signal originates. The drawing number of a print is located in the lower right-hand corner of the print title block (DL-1, DL-2, SABR, DCR, etc.).

SIGNAL NAME is the name proper of the signal. The names used on the print set are also used in this manual for correlation between the two.

POLARITY is either H or L to indicate the voltage level of the signal: H means +3V; L means ground.

For example, the signal:

DL-4 RCVR DONE H

originates on sheet 4 of the M7800 module drawing and is read, "when RCVR DONE is true, this signal is at +3V."

Unibus signal lines do not carry a SOURCE indicator. Except for the grant lines, these signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exist. Each Unibus signal name is prefixed with the word BUS.

In text references to a specific engineering drawing are in abbreviated form. For example "drawing M7014-LEI" refers to drawing D-CS-M7040-0-1, sheet 9, Light Pen Edge and Intensity Logic.

3.2 GT40 DISPLAY PROCESSOR

3.2.1 Introduction

The GT40 Display Processor, the controlling element in the GT40 Graphic Display Terminal, consists of three hex-height modules: A320, M7013, and M7014. The M7013 contains most of the display processor logic and the A320 possesses the vector generator logic, analog circuitry, and interfaces with the other display terminal components. The M7014 module contains the Unibus interface, Bootstrap Read Only Memory (ROM), control logic, and the timing pulse generator. The functions of the three modules are so integrated that separate descriptions are precluded; in an operational sense they can be considered to be one module.

Capable of executing its own display program, the display processor, once started, can function independently. It requires only the granting of non-processor requests (NPR) by the PDP-11/05. The display program is updated by the PDP-11/05, as dictated by the overall objective of the program, in order to effect a timely display. However, this function is not necessary, in itself, for display processor operation.

The graphic oriented set of five versatile instructions provides the basis for a very proficient display program. This program, containing the data and commands necessary to produce a CRT display, is stored in the MM11-K Core Memory. It is transferred, as the result of NPRs, one word at a time via the Unibus to the display processor.

Once brought into the display processor, the data words and instructions are decoded and stored. The signals necessary to execute the instructions are developed, vector and character calculations are made, and outputs to the CRT display are generated. This, in brief terms, is the primary role of the GT40 Display Processor. Drawing D-BD-GT40-0-4 is a block diagram of the display processor.

3.2.2 Initialization

The first signal input to the GT40 Display Processor is BUS INIT L. It is asserted, when power is applied to the system, by pressing the START switch on the PDP-11/05 console, or by issuing a programmed RESET instruction. This signal sets all logic to the appropriate initial states, e.g., clears the Display Program Counter (DPC) and any flags that are set.

3.2.3 Starting the Display Processor

Starting the display only requires the addressing of the display computer's DPC followed by the transfer of data into the DPC. Briefly, the start sequence begins when the PDP-11/05 places the address of the DPC (772000) on the Unibus address lines and data on the Unibus data lines; the data is then loaded into the DPC. Decoding the DPC address in the M7014 address selection logic automatically starts the display. The GT40 is subsequently granted an NPR, becomes bus master, and the data that was loaded into the DPC is placed on the Unibus address lines to the MM11-K Core Memory. This results in the retrieval and transfer to the GT40 of the first instruction in the display program; display operation has begun. A more detailed description of this operation, and the particular signals generated, is contained in the following paragraph.

3.2.4 Address Selection

Decoding of Unibus addresses is the function of the M7014 address selection logic (drawing M7014-ASL). The only recognizable addresses are those of the four hardware registers in the GT40 (Table 3-1); all other bus addresses, except that of the Bootstrap ROM (Paragraph 3.2.14), are invalid as far as the GT40 is concerned. The initiation by the CPU of any display processor operation is dependent on the decoding of a valid address from the Unibus.

The CPU can read the contents of all four hardware registers, but only the DPC can be written into. Bus control bit C1 determines whether the operation is a read (Bus C1 a logic high) or write (Bus C1 a logic low). As indicated in Table 3-1, address bits 1 and 2 are used to identify the particular registers; the other bits are the same for all four registers.

Read and write functions begin when the CPU places the display processor register address on the bus address lines and transmits BUS MSYN L. As originated in the PDP-11/05, the GT40 address equals 17200X. However, the two high-order address bits are forced to a 1 on the Unibus, asserting an address of 77200X. Of the 17 address bits that are decoded (bit 0 is not considered), eleven, BUS A (12:11, 09:01) L, are input to the display processor through three 8838 Bus Transceivers and six, BUS A (17:13, 10) L, bypass the transceivers. (The bit 10 input to the transceivers is not used.)

As shown on drawing M7014-ASL, the bus transceivers are also employed when the GT40 becomes bus master and places the first twelve bits of the DPC [PCC PC (12:01) H] on the bus address lines. The routing of the Unibus address and data bits is shown in Figure 3-1.

The lower order address bits [ASL (12, 9:3) H] are input to 8242 Exclusive-NOR comparator gates in the decoding circuit. These gates require the correct address jumper configuration at their second inputs. Table 3-2 lists the jumpers and shows their relationship to the addressing scheme. The common output of the Exclusive-NOR gates must be a logic high in order for the Unibus address to be recognized. Therefore, none of the gates can be enabled. If a jumper is in place, a 0 input (a logic low at this point) disables the gate. Likewise, 1 bits disable those gates where the jumper has been removed. Note that address bits 10 and 11 are not decoded with address jumpers. BUS A 10 L is decoded directly from the Unibus; ASL BA 11 L enters the decoder circuit at a later point.

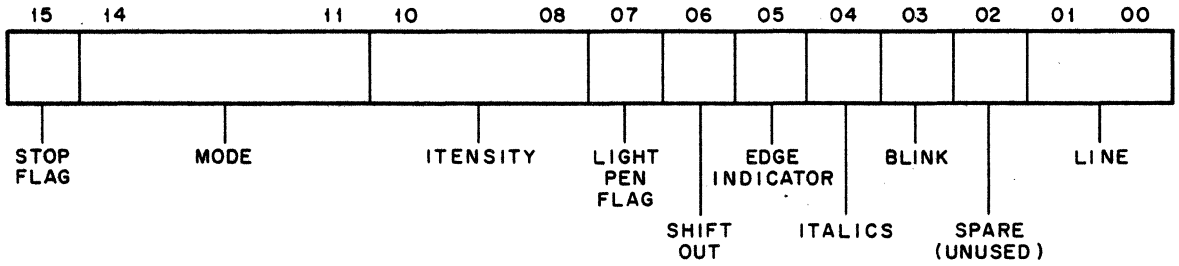
The remaining address bits [BUS A (17:13, 10) L], along with BUS MSYN L, are sent directly from the Unibus to a type 314, 7-input AND gate in the decoder. The output of this gate is ANDed with the high common output of the Exclusive-NOR gates to assert ASL DISPLAY ENABLE L. BUS MSYN L is sent by the PDP-11/05 (about 150 ns after the address is placed on the Unibus) to initiate a read or write operation in the GT40 Display Processor.

ASL DISPLAY ENABLE L performs two functions: first, it causes ASL SET SSYN L, and consequently BUS SSYN L, to be asserted; second, it is ANDed with BUS C1 L to generate several internally used signals necessary to execute a read or write request from the PDP-11/05. BUS SSYN L notifies the PDP-11/05 that the request (BUS MSYN L) and address have been accepted and that data has been received from the Unibus data lines (write to DPC) or placed on the Unibus lines (read). In generating BUS SSYN L, ASL SET SSYN L is input to a circuit (drawing M7014-BCL) consisting of a 74123 Monostable Multivibrator and a 7474 D-type flip-flop that function together as a 100-ns delay. The delay allows time for read data to be transferred through the transceiver gates and become settled on the Unibus before it is strobed by the PDP-11/05. Similarly, during a write operation the delay is needed before the display processor acknowledges receipt of data from the Unibus. BUS SSYN L, during both read and write operations, causes the PDP-11/05 to drop BUS MSYN L from the Unibus; this terminates the transfer operation. However, other events take place in the display processor while this delay is timing out.

Table 3-1
GT40 Hardware Registers

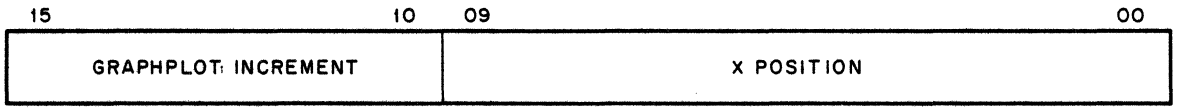
Register	Unibus Address*	CPU Operation
Program Counter	772000	Read/Write
Status Register	772002	Read Only
X Position & Graphplot Increment	772004	Read Only
Y Position & Character	772006	Read Only

*The two high order bits are forced to a 1 to assert an MSD = 7.



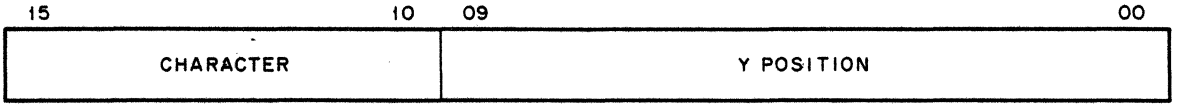
STATUS REGISTER

11-2155



X POSITION AND GRAPHPLOT INCREMENT REGISTER

11-2157



Y POSITION AND CHARACTER REGISTER

11-2156

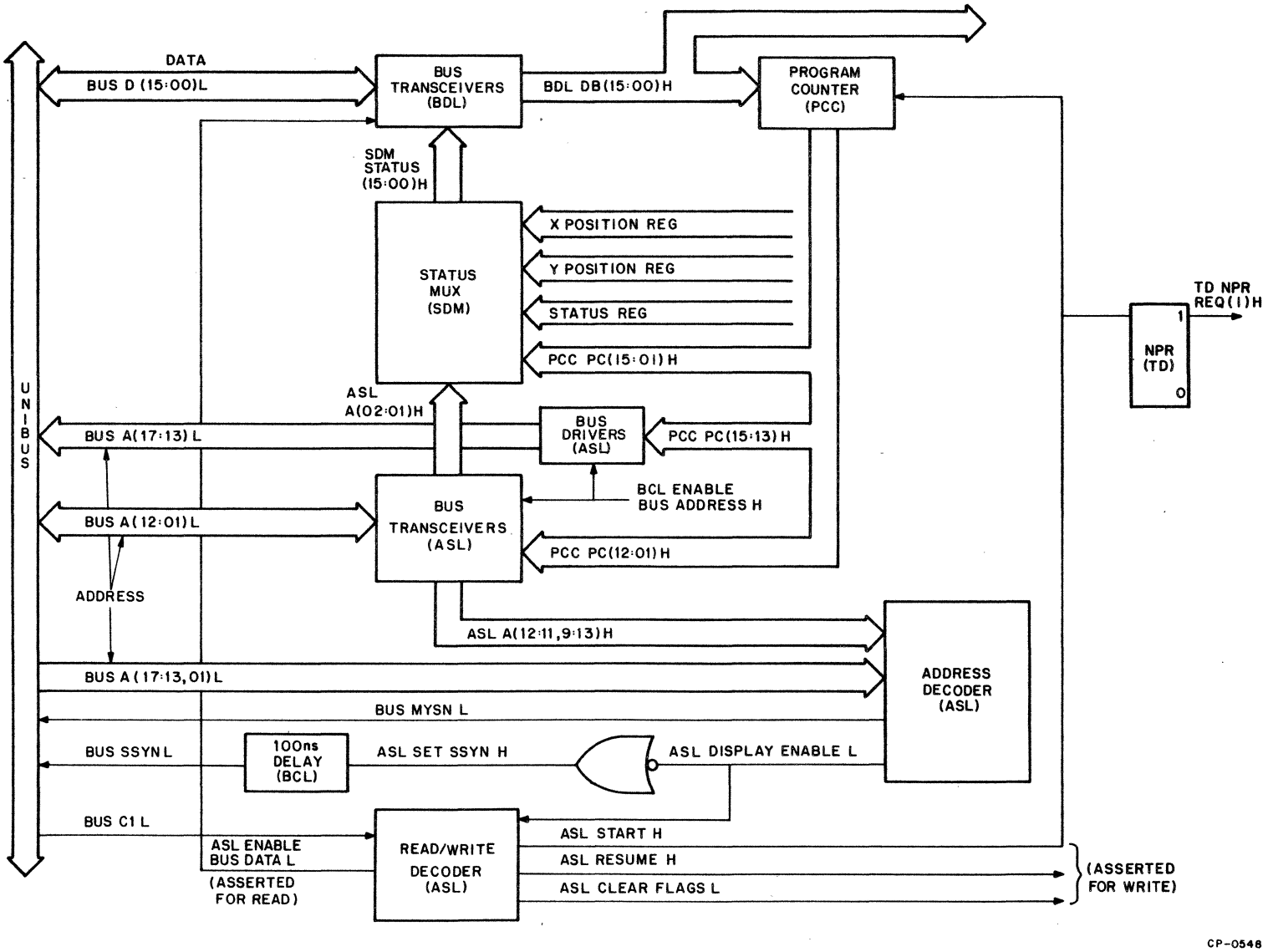


Figure 3-1 Unibus Address and Data, Block Diagram

Table 3-2
Address Jumper Configuration

Unibus Address	Address Bits	State	Address Jumper	Jumper Condition
7	BUS A 17 L	1		
	16	1		
	15	1		
7	14	1		
	13	1		
	12	1	W11	OUT
2	11	0		
	10	1		
	9	0	W13	IN
0	8	0	W16	IN
	7	0	W19	IN
	6	0	W17	IN
0	5	0	W18	IN
	4	0	W14	IN
	3	0	W12	IN
X	2	X		
	1	X		
	0	X		

ASL START H, one of the signals generated when the condition of BUS C1 L (a low) specifies a write operation, causes the data on the Unibus data lines to be gated into the DPC and sets the NPR flip-flop in the M7013 module in preparation for an NPR request to the PDP-11/05. Note that ASL START H can only be asserted when address bits 1 and 2 [BUS A (02:01) L] both equal 0, which specifies the DPC, and data bit 0 = 0 (BDL DB 00 L), because only even data inputs to the DPC are valid (this data, in turn, becomes an address directed to the memory). When BUS C1 L is a logic high, indicating a read is to take place, ASL DISPLAY ENABLE L generates ASL ENABLE BUS DATA L. This latter signal gates the data (DPC, Status Register, X Position Register, or Y Position Register) from the Status Multiplexer onto the Unibus data lines by way of the bus transceivers (Paragraph 3.2.4.1). Figure 3-2 shows the timing for these operations and signals.

3.2.4.1 Reading Status – Although capable of writing to only one register (DPC) in the GT40, the PDP-11/05 can read the contents of four registers (DPC, X Position Register, Y Position Register, and Graphplot Increment Register) and the state or status of 21 other flip-flops and signals. Called reading status, the CPU uses this operation to determine the condition of GT40 registers and signals.

As stated previously, read and write operations are decided by the state of control bit C1. When reading status, the PDP-11/05 places the address (Table 3-1) and BUS C1 L on the Unibus followed by BUS MSYN L. The address is decoded and, if valid in the GT40, is ANDed with BUS MSYN L to assert ASL DISPLAY ENABLE L. The latter signal is then ANDed with BUS C1 L, a logic high, to assert a second signal, ASL ENABLE BUS DATA L. The two low-order address bits [ASL A (02:01) H] are used to select which of the four, 16-bit inputs to the Status Multiplexer (M7013-SDM) are to generate SDM STATUS (15:00) H. These 16 bits are then gated to the Unibus, via the bus transceivers (M7014-BDL), by ASL ENABLE BUS DATA L. The Status Multiplexer is composed of eight Type 74153, dual, 4-to-1 multiplexer chips. They are shown as the top two rows of chips in drawing M7013-SDM; Figure 3-3 is a simplified diagram of the reading status logic including the multiplexer.

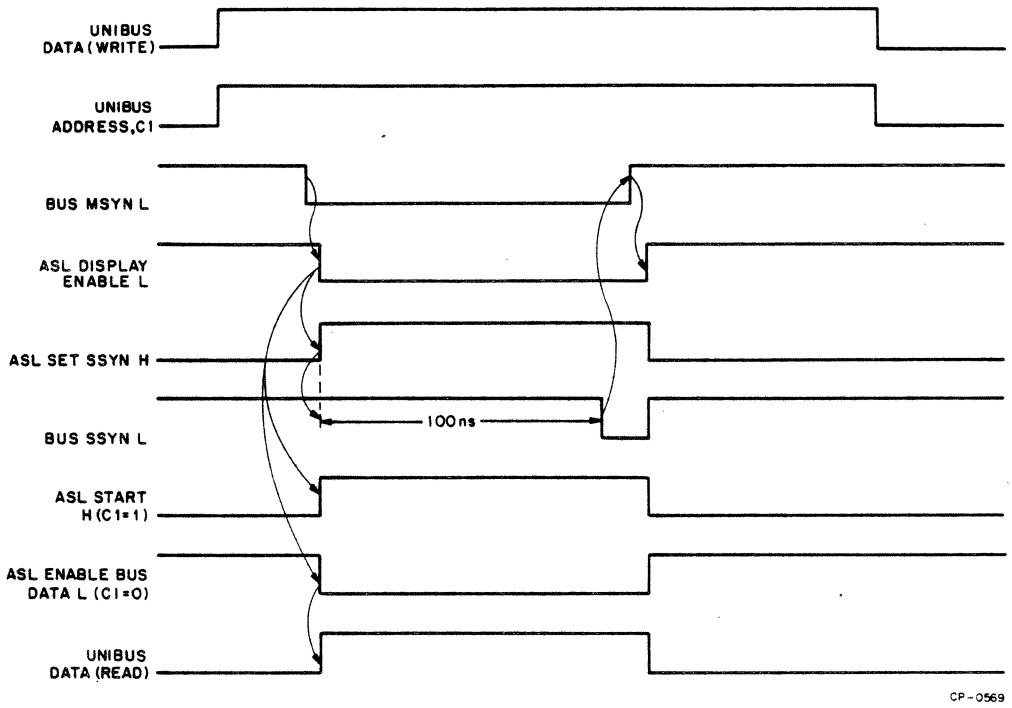


Figure 3-2 Unibus Transfer Timing

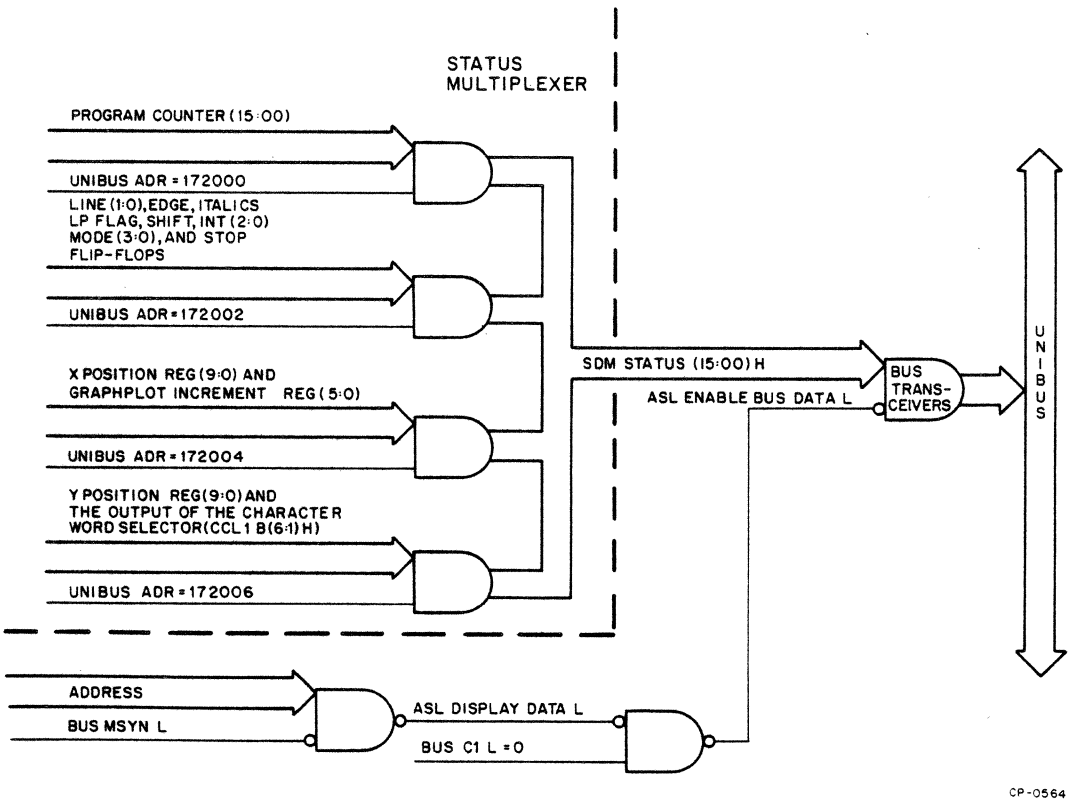


Figure 3-3 Reading Status, Block Diagram

3.2.5 NPR Data Requests

Operation of the GT40 Display Processor is a function of the display program stored in the MM11 Core Memory. Retrieval of instructions in this program is effected when the PDP-11/05 responds to NPRs that originate in the display processor and allows the display processor to become bus master. At this time, the display processor transmits, via the Unibus, a request for data (BUS MSYN L) and the memory address of the data. The arrival of the data from memory initiates a timing sequence that terminates in the assertion of the next NPR and the process is repeated.

The initial NPR is generated when the signal ASL START H sets the NPR flip-flop (drawing M7013-TD). ASL START H also loads the DPC with the memory address of the first instruction in the display program (drawing M7014-PCC). (This sequence is described in Paragraph 3.2.4.) With the NPR flip-flop set, BCL NPR (1) H is ANDed with the outputs from two 7474 flip-flops (S+BSY and $\overline{S}$·BSY) to assert BUS NPR L (drawing M7014-BCL and Figure 3-4). This signal on the Unibus indicates that the display processor desires control of the bus, i.e., to become bus master. The PDP-11/05 acknowledges the NPR by placing a grant signal, BUS NPG IN H, on the Unibus to denote that control is relinquished to the requestor (the display processor in this case).

The GT40 Display Processor now obtains control of the Unibus and can issue control signals and addresses to other (slave) devices on the Unibus. The MM11 Memory, where the display program is stored, is the device that is communicated with when an NPR is granted to the display processor. Controlling the handshaking that ensues are two 7474 flip-flops, S+BSY and $\overline{S}$·BSY (SACK OR BUSY, $\overline{SACK}$ AND BUSY) shown on drawing M7014-BCL. The direct reset to both flip-flops is dropped when the NPR flip-flop is reset. S+BSY is then set on receipt of BUS NPG IN H. Because there is an NPR pending [BCL NPR REQ (1) H], the bus grant is not passed on to the next device on the Unibus ($\overline{BUS\ NPG\ OUT\ H}$). The 1 output of S+BSY, now high, causes BUS NPR L to be dropped from the Unibus and asserts BUS SACK L (Selection Acknowledge) to acknowledge the bus grant signal. The PDP-11/05 responds to BUS SACK L by dropping the grant signal, BUS NPG IN H, from the bus. With this input low, $\overline{S}$·BSY is clocked set, provided there is no coincident BUS SSYN L or BUS BBSY L signal from any other device on the Unibus. Several results occur now that both 7474 flip-flops are set. Of primary importance is the assertion of BUS BBSY L (Bus Busy) on the Unibus. This signal notifies all devices on the Unibus that the display processor has assumed control of the bus (it has become bus master). Coincident with BUS BBSY L, BCL MINE L is generated to perform a similar role within the display processor. This latter signal, in effect, indicates to the M7013 and M7014 modules that "the bus is mine." An immediate result of BCL MINE L is to generate a signal, BCL ENABLE BUS ADDRESS H, which gates the DPC [PCC PC (15:00) H] onto the Unibus address lines (drawing M7014-ASL).

At the same time, SET MSYN, a 74123 Monostable Multivibrator (drawing M7014-BCL), is triggered generating a 100-ns output pulse to the clock input to the MSYN flip-flop. MSYN sets on the trailing edge of this pulse to assert BUS MSYN L. This signal, delayed 100 ns to allow time for the bus address lines to settle, instructs all devices connected to the Unibus to respond to the address presently on the Unibus address lines. However, the address is recognized in only one device, core memory in this case, and ignored by the others. Consequently, the MM11 Core Memory responds to the MSYN address combination, fetches the data at the specified location, places it on the Unibus data lines, and then notifies the display processor (after a 100-ns delay) of this operation by asserting BUS SSYN L.

The signal BUS SSYN L is input to the M7014 module and asserts BCL SSYN H that is ANDed with BCL MSYN (1) H to generate BCL DATA READY L. This latter signal is used to start the timing in the M7013. One of these timing signals (Paragraph 3.2.6), TD LOAD PULSE H, asserts BCL DATA CLEAR H. This signal asserts BCL REQ CLR L which resets the MSYN and NPR flip-flops. Consequently, TD NPR REQ (0) H resets the S+BSY and $\overline{S}$·BSY flip-flops to drop BUS BBSY and BCL MINE L; the display processor is no longer bus master.

The sequence described above is the normal chain of events when an NPR is issued. However, it is possible that the signals to the slave can go unanswered, e.g., if the address sent to memory is nonexistent. The time out circuit on the M7014 module (drawing M7014-BCL) is designed to generate a time out interrupt if this situation should occur. At the time BUS MSYN L was placed on the Unibus, BCL MSYN (1) H allowed a 22 μs, type 74123 delay (Time Out Delay) to trigger. If BUS SSYN L is not returned within 22 μs after MSYN is asserted, the delay times out and the

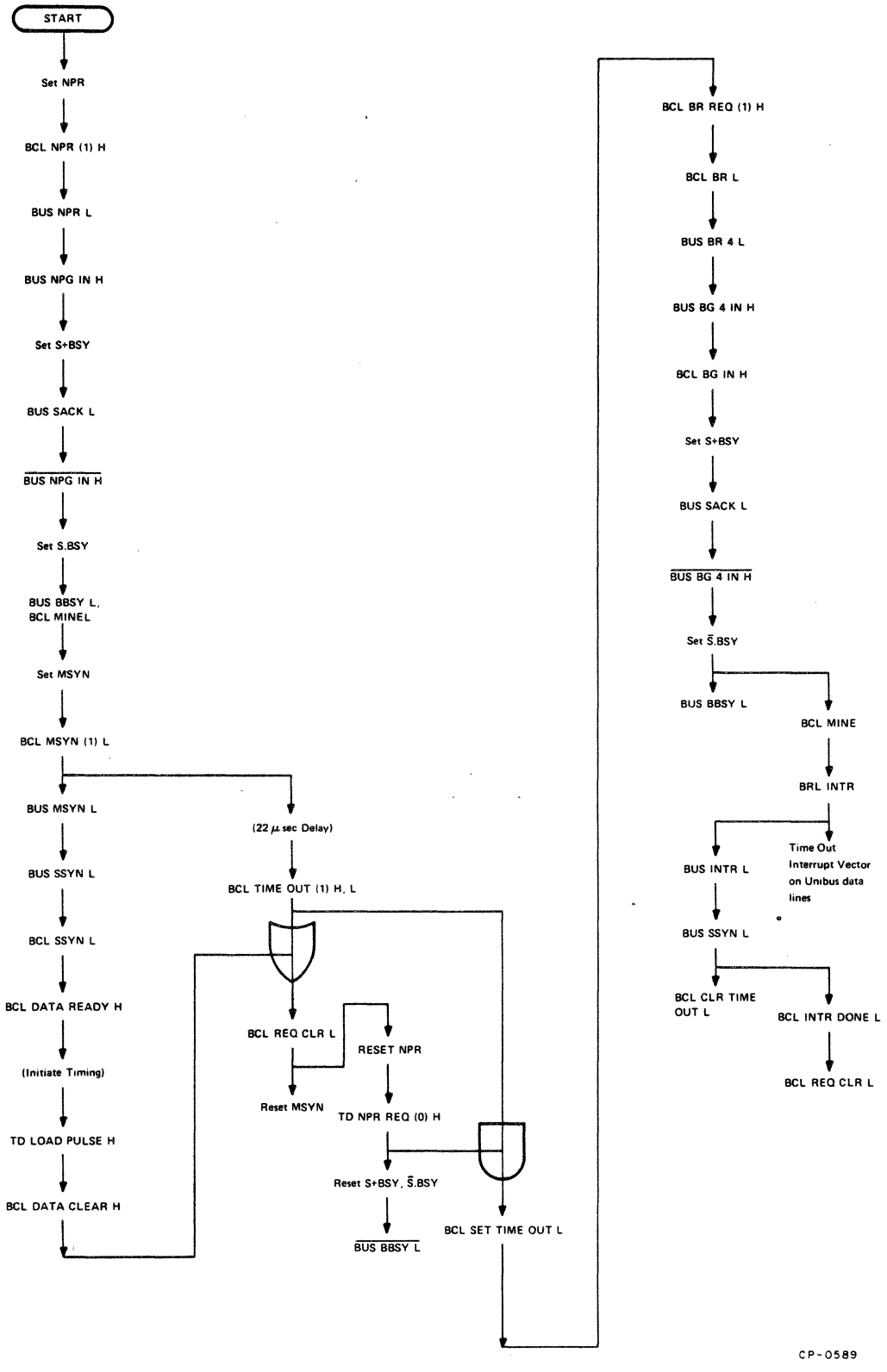


Figure 3-4 NPR/Time Out Interrupt, Flow Diagram

BCL Time Out flip-flop is set. The NPR and MSYN flip-flops are then reset, as is normally the case, freeing the bus. In addition, the BCL SET TIME OUT L signal is asserted to initiate the bus request sequence via the priority jumper plug on the M7014 module; this concludes with BUS BR 4 L being output to the PDP-11/05 (Figure 3-5). The bus request is evaluated in the CPU priority arbitration logic, and if found to have the highest priority, causes a bus grant (BUS BG 4 IN H) to be issued to the Unibus. The bus grant enters the display processor through the same priority jumper plug to generate BCL BG IN H which sets the S+BSY flip-flop. With this flip-flop set, and a BR in effect [BCL BR (1) H], BUS BG OUT H to the Unibus is inhibited; a delay in this circuit allows time for B+BSY to set. (If there was a priority jumper plug for a priority level other than 4 present, BUS BG 4 IN H would be direct wired to BUS BG 4 OUT H.)

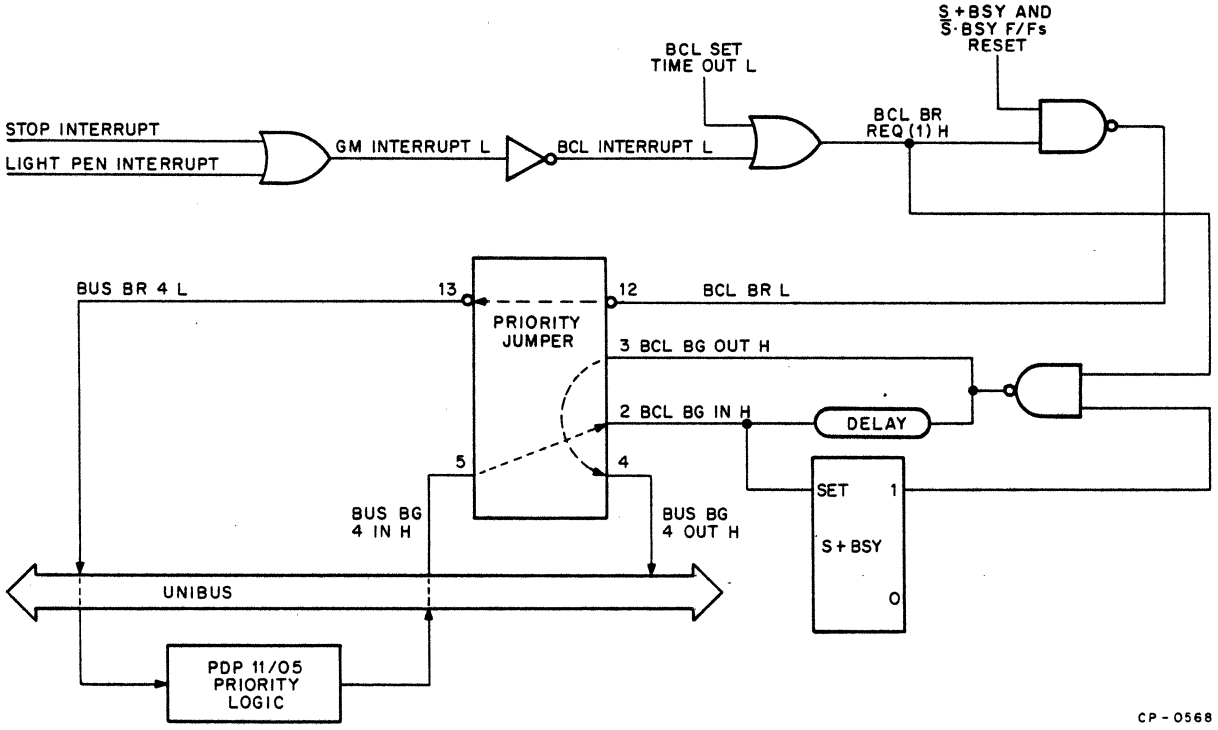


Figure 3-5 Bus Request and Bus Grant, M7014 Module

Another output to the Unibus, BUS SACK L, is asserted by the display processor when BCL BG IN H sets S+BSY. On receipt of this bus grant acknowledgment, the PDP-11/05 drops BUS BG 4 IN H and $\overline{S}$·BSY is set. With both S+BSY and $\overline{S}$·BSY set, the display processor again becomes bus master; BUS BBSY L and BCL MINE L are asserted. Because a bus request is pending, BCL MINE L asserts BRL INTR H and BUS INTR L (Figure 3-47). BRL INTR H is gated with BCL TIME OUT (1) H (drawing M7014-BRL) to generate an interrupt vector address of 330 on the Unibus data lines [BUS D (08:00) L]. Jumpers W7, W8, W9, W10, and W15 must also be of the correct configuration (Table 3-3) before any vector address can be output to the Unibus. The PDP-11/05 reads in the vector address, which results in entry into a particular software routine, and transmits BUS SSYN L to the display processor. BCL SSYN H is then ANDed with BRL INTR H (drawing M7014-BCL) to generate BCC INTR DONE H and BCL CLR TIME OUT H; this concludes the time out interrupt operation.

3.2.6 Timing

Internal timing for the GT40 Display Processor is initiated by the BCL DATA READY L signal generated during an NPR operation (Paragraph 3.2.5) or by TD RESTART H. The resultant stream of pulses, listed in Table 3-4, is used to gate data, increment the DPC, and effect other controlled functions that are required in the display processor. Timing logic is shown on drawings M7013-TD and M7014-PCC; Figure 3-6 is a timing diagram for the timing pulses and related signals.

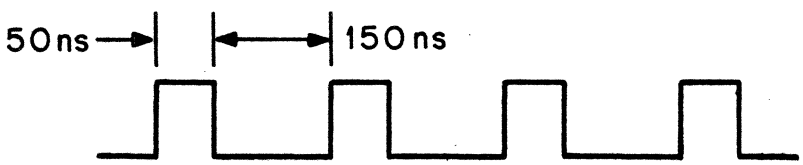
Table 3-3
Interrupt Vector Addresses

Jumpers	Bus DXX L	Stop INT Vector	Light Pen INT Vector	Char INT and Time Out INT Vector
W8-OUT	08	0	0	0
W7-IN	07	1	1	1
W10-IN	06	1	1	1
W15-OUT	05	0	0	0
W9-IN	04	1	1	1
–	03	0	0	1
–	02	0	1	0
–	01	0	0	0
–	00	0	0	0
Interrupt Vector Address		320_8	324_8	330_8

Table 3-4
GT40 Display Processor Timing Pulses

Signal	Use
TD LOAD MODE A	Strobe data from Unibus data lines.
TD LOAD PULSE H	Gate data into the Data Mode, Control Mode and other registers; resets MSYN.
TD TP1 H	Increment the DPC.
TD TP2 H	Generates another NPR (if not inhibited) or initiates a character, point, graph, or vector.

Signals BCL DATA READY L or TD RESTART H are used to start a timing pulse stream. Either of these two signals will set a 7474 D-type flip-flop to assert TD SYNC UP H. This signal, in turn, primes a 7473 J-K flip-flop whose output, TD TIME ON H, is used to synchronize the display clock signal PCC DIS CLOCK H. PCC DIS CLOCK H originates in a 20-MHz, crystal controlled, clock pulse generator in the M7014 module (drawing M7014-PCC). Input through a jumper (W24) to the first of two 74H74 D-type flip-flops that operate as frequency dividers, the 20-MHz signal generates PCC ANALOG CLOCK H (10 MHz). The second flip-flop outputs a 5-MHz free-running pulse stream, PCC DIS CLOCK H, illustrated below.



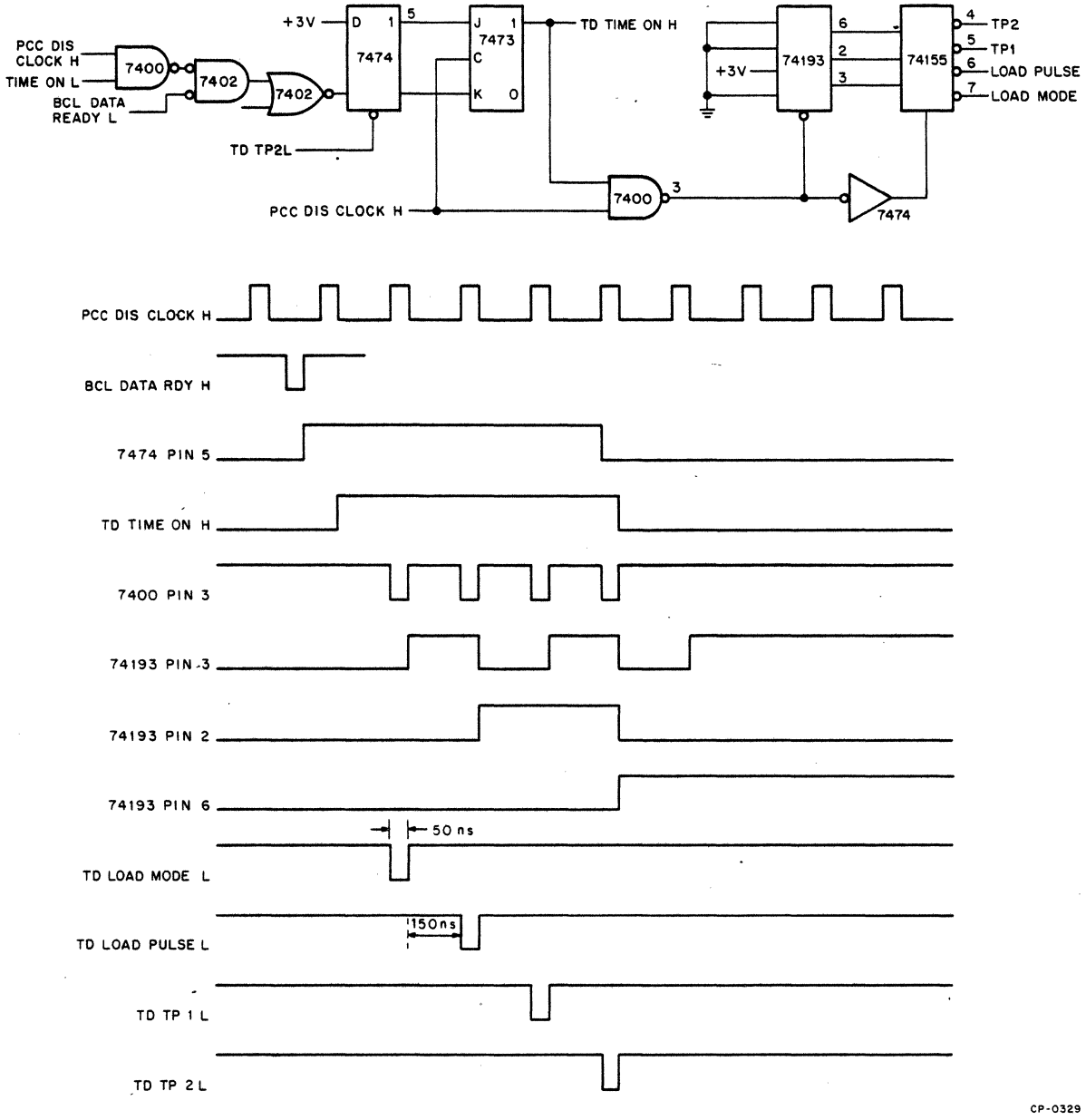


Figure 3-6 Display Processor Timing Diagram, M7013 Module

Signal PCC DIS CLOCK H, now gated by TD TIME ON H, up clocks a previously reset (SDM DATA READY L) 74193 4-Bit Binary Counter, TIME CNT UP, in the M7013 Timing Decoder. The R0, R1, and R2 outputs from the counter, along with the gated PCC DIS CLOCK H, activate a 74155 1-line to 4-line demultiplexer to produce the four time states: LOAD MODE, LOAD PULSE, TP1, and TP2. [TD RESTART H does not cause LOAD MODE or LOAD PULSE (Paragraph 3.2.12.6).] TD TP2 H, in addition to the uses listed, resets the 7474 D-type flip-flop that was set at the beginning of the operation; TD SYNC UP H and TD TIME ON H are terminated and PCC DIS CLOCK H is inhibited from further up counting of the binary counter. The timing decoder will now remain in a quiescent state until the next DATA READY or RESTART signal.

3.2.7 Display Processor Mode Control

The mode control logic in the M7013 module (drawing M7013-MD and Figure 3-7) is used to identify the information currently on the Unibus data lines and generate the appropriate signal required to execute the specified operation. A series of timing pulses is generated (Paragraph 3.2.6) when an instruction or data in the display program is read from core memory and placed on the Unibus data lines. One of these pulses, TD LOAD MODE H, gates the data on the Unibus into the mode decoding logic. Depending on the bit configuration (Table 3-5) of the five high order bits [BDL DB (15:14) H and SDM DB (14:11) L] the bus data is decoded as an instruction or as data; an instruction is further defined as a control instruction or a data instruction.

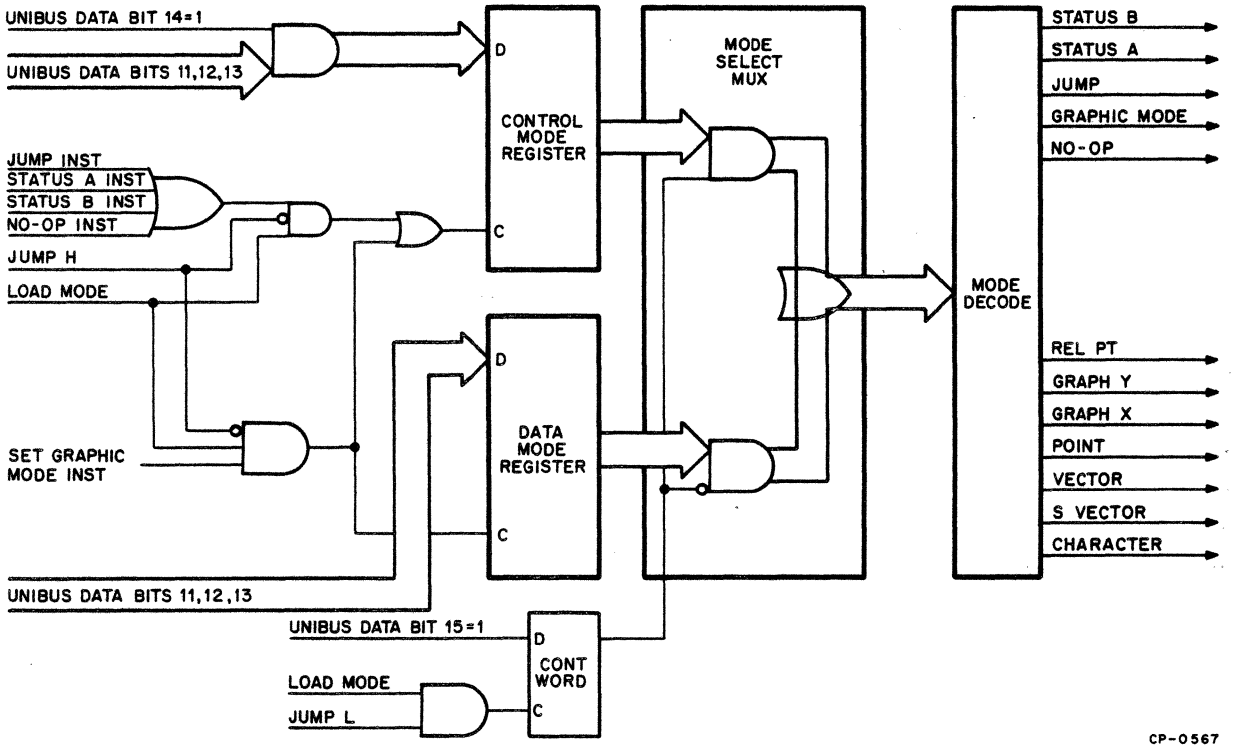


Figure 3-7 Mode Control

Unibus data bit 15 determines whether data on the bus is an instruction (bit 15 = 1) or strictly data (bit 15 = 0), e.g., the X, Y coordinates that follow an instruction, is presently on the bus data lines. If an instruction is on the Unibus, bit 14 is used to denote if it is a control instruction (bit 14 = 1) or a data instruction (bit 14 = 0).

The Control Mode and Data Mode Registers hold the codes for the current operation. These codes cause signals to be asserted that will establish the operational parameters or display data on the CRT. When a control instruction (Jump, No-op, Load Status A, Load Status B) is on the Unibus, the bus bits [SDM DB (13:11) L] are clocked into the Control Mode Register; the Data Mode Register remains unchanged. However, if a data instruction, i.e., one of the Graphic Mode instructions, is decoded, the bus bits [BDL (13:11) H] are clocked into the Data Mode Register. The Control Mode Register is also clocked but all three D inputs are inhibited because bit 14 = 0. This results in the code for Set Graphic Mode (000) being stored in this register. Note that if a Jump is in effect neither of the two registers are clocked; their previous contents remain unchanged. This allows a graphic mode operation to be resumed after a Jump (which is executed for the purpose of reading data from another memory area) without requiring that the Graphic Mode instruction be respecified; the Data Mode Register still contains the code for the graphic instruction. This can result in a significant decrease in the number of instructions required in a program.

Table 3-5
Unibus Instruction and Data Codes

Instruction/Data	Unibus Data Bit				
	15	14	13	12	11
All Data Words	0	X	X	X	X
Set Graphic Mode	1	0	—	—	—
(Set Character Mode)			0	0	0
(Set Short Vector Mode)			0	0	1
(Set Long Vector Mode)			0	1	0
(Set Point Mode)			0	1	1
(Set Graph X Mode)			1	0	0
(Set Graph Y Mode)			1	0	1
(Set Relative Point Mode)			1	1	0
(Spare)**			1	1	1
*	1	1	0	0	0
SPARE**	1	1	0	0	1
SPARE**	1	1	0	1	0
SPARE**	1	1	0	1	1
JUMP	1	1	1	0	0
NO-OP	1	1	1	0	1
LOAD STATUS REG A	1	1	1	1	0
LOAD STATUS REG B	1	1	1	1	1

*Serves no function except to assert MD GRAPHIC MODE H and set NPR; Data Mode Register is not loaded.

**The display processor hangs when a spare code is decoded.

Two other decoder functions take place when Unibus data bit 15 (= 1) is ANDed with the same TD LOAD MODE H pulse that clocked the two mode registers. Unless the second word of a Jump instruction is about to be read (MD JUMP WORD 1 L is asserted at this time) the signal MD CLR WORD L is generated when any instruction is on the Unibus data lines (bit 15 = 1). MD CLR WORD L clears the Word flip-flop (drawing M7013-TD); coincident with this the Cont Word flip-flop is clocked set. (The flip-flop is already set if the previous word was a control instruction.) MD CONT WORD (1) H is asserted and the contents of the Control Mode Register are gated into the multiplexer. As a result, one of the control signals (STATUS A, STATUS B, JUMP, GRAPHIC MODE, or NO-OP) is output from the mode decoder. The Cont Word flip-flop is clocked reset when one of the data words (bit 15 = 0) that follow a Graphic Mode instruction is on the Unibus. The set output from the flip-flop is now low (MD CONT WORD (1) H) and the contents of the Data Mode Register are gated into the Mode Select Multiplexer; one of the graphic mode signals (POINT, VECTOR, GRAPH X, etc.) is then asserted. The Cont Word flip-flop cannot be clocked if the second word of a Jump instruction (MD JUMP WORD 1 L) is being read. This word, an address on the bus data lines, could cause the Cont Word flip-flop to change states and, therefore, the C input is inhibited.

The Mode Select Multiplexer outputs four signals [MD MODE (3:0) H] that are decoded in the 74154 4-Line to 16-Line Demultiplexer (mode decode) to generate a single output signal. Table 3-6 lists all the decoder outputs along with their requisite input signals.

The mode decoder outputs serve many functions in carrying out the explicit steps required by a particular instruction. For example, MD STATUS A H is used to clock Unibus data bits into the Status A Register flip-flops (drawing M7013-SABR) to establish certain operating parameters. The state of one of these flip-flops, LP INT HIT ENA, determines if future light pen hits are to be accepted or not.

Table 3-6
Mode Decoder Outputs

74175 Control Mode Register Outputs			74175 Data Mode Register Outputs			Mode Select MUX Output* (MD MODE X H)				74175 Mode Decode Asserted Output	
R1(1) (DB13)	R2(1) (DB12)	R3(1) (DB11)	R1(1) (DB13)	R2(1) (DB12)	R3(1) (DB11)	3	2	1	0		
L	L	L				H	L	L	L	MD GRAPHIC MODE L	Control Instructions
L	L	H				H	L	L	H	(No connection)**	
L	H	L				H	L	H	L	(No connection)**	
L	H	H				H	L	H	H	(No connection)**	
H	L	L				H	H	L	L	MD JUMP L	
H	L	H				H	H	L	H	MD DNOP L	
H	H	L				H	H	H	L	MD STATUS A L	
H	H	H				H	H	H	H	MD STATUS B L	
			L	L	L	L	L	L	L	MD CHARACTER L	Data Instructions
			L	L	H	L	L	L	H	MD S VECTOR L	
			L	H	L	L	L	H	L	MD VECTOR L	
			L	H	H	L	L	H	H	MD POINT L	
			H	L	L	L	H	L	L	MD GRAPH X L	
			H	L	H	L	H	L	H	MD GRAPH Y L	
			H	H	L	L	H	H	L	MD REL PT L	
			H	H	H	L	H	H	H	(No connection)**	

*Mode Select MUX accepts inputs from the Data Mode Register when bit 15 = 0.
Mode Select MUX accepts inputs from the Control Mode Register when bit 15 = 1.
**The display processor will hang if these outputs are asserted.

In conclusion, several points should be reviewed. Unibus data bit 15 = 1 denotes an instruction on the Unibus. Bits 11, 12, and 13 are gated into the Mode Control Register and one of five control instruction signals is concurrently output from the mode decode. The information on the Unibus is data (as opposed to an instruction) when bit 15 = 0; the two mode registers remain unchanged. At the same time, the previously loaded Data Mode Register is read and one of the graphic mode signals is asserted from the mode decode. Unibus bit 14 = 1 when a control instruction (except for Set Graphic Mode) is on the Unibus; the Data Mode Register is not changed at this time. When bit 14 = 0, the mode control contains the code for Set Graphic Mode and the Data Control Register is loaded with the particular op code for the graphic mode.

3.2.8 Control Instructions

The five instruction repertoire of the GT40 Display Processor is capable of effecting all display, control, and interrupt functions required for GT40 operation. These instructions, read from the display file in the MM11 Core Memory as the result of NPRs and then decoded, generate those signals necessary to carry out the specified operations.

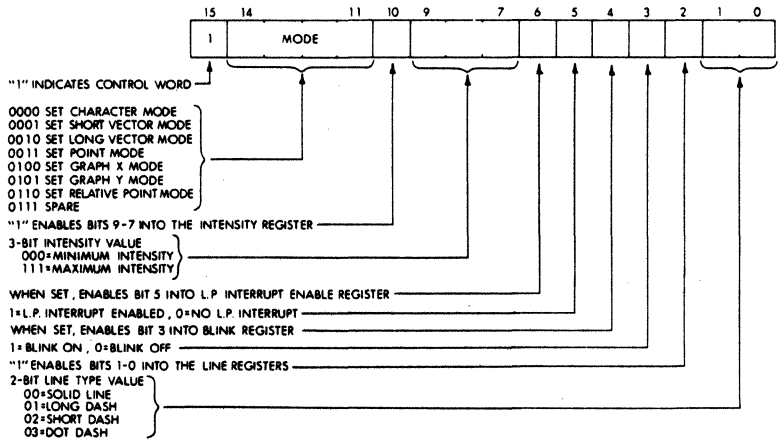
Purposes for the display instructions are distinctive – although there is some overlap in this respect (three of the instructions are used to establish operating parameters). In determining the type of display, the Set Graphic Mode instruction is the most important of this small, though powerful, instruction set. This instruction initiates the graphic or display mode of operation, in a general sense, and at the same time clearly defines one of the seven types of displays (op codes). Several display qualifications are also specified. The Jump instruction allows the display program flow to be changed to a noncontiguous memory area; the second word of this instruction is retrieved from memory and inserted into the DPC to become the address of the next memory location to be read. No-op also performs in the classic manner. Aside from incrementing the DPC, no-op does not affect the GT40 display or change the display parameters; it is used primarily as a "filler" between the other instructions or data. The operating parameters are specified by the Load Status Register A, Load Status Register B, and Set Graphic Mode instructions. The first two are devoted solely to such functions as determining whether the character font is to be normal or italics and whether to generate an interrupt to the PDP-11/05 when the display stops. Figure 3-8 is a breakdown of each of the instruction words.

3.2.8.1 Load Status Register A – This instruction, decoded (Paragraph 3.2.7) when Unibus data bits (15:11) = 11110_2, sets or clears five flip-flops shown on drawing M7013-SABR. Figure 3-9 picks up the instruction flow where the signal MD STATUS A H is asserted by the mode decoder.

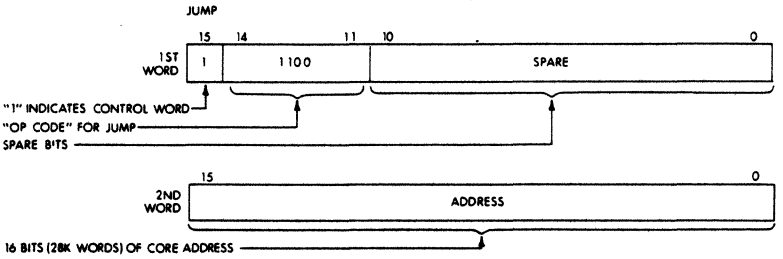
Depending on the parameters to be established, one or more of the five flip-flops controlled by Load Status Register A can be set/cleared by TD LOAD PULSE H when the instruction is decoded. Three of the flip-flops (SABR Stop Interrupt Enable, SABR Italics, and SABR Light Pen Hit Enable) can be set or cleared as determined by the instruction's bit configuration (Figure 3-8). The other two (SABR Stop and SABR Sync) can only be set when this instruction is decoded; they are automatically cleared at some later point.

The SABR Stop Int Ena flip-flop performs its function of initiating a stop interrupt only in the presence of a set SABR Stop flip-flop. (Normal NPR assertion occurs if Stop is not set.) However, the SABR Stop flip-flop can produce a usable output regardless of the state of Stop Int Ena. In either configuration further NPRs are temporarily inhibited, thus halting the display program. This is to allow time for the PDP-11/05 to update the display file in core memory. Assertion of stop interrupt on the Unibus (both flip-flops must be set) is the more positive means of informing the CPU of the stop condition. There is no stop interrupt generated when only SABR Stop is set; the DPU depends on the CPU reading status to ascertain the stop condition. In both cases the CPU alters the display file and then flags the display processor by asserting BUS MSYN L on the Unibus. The CPU also sets Unibus data bit 0 to a 1. This serves two functions: first, it inhibits the assertion of ASL START H and, therefore, the DPC is not loaded (changed); second, ASL RESUME H is generated and an NPR is asserted (drawing M7013-TD). Display program execution now resumes at the point it was stopped. In the meantime, the display processor responds to MSYN by asserting BUS SSYN L. The PDP-11/05 now drops BUS MYSN L which, in turn, inhibits ASL RESUME H and SABR Stop is cleared. SABR Stop Int Ena is reset when the CPU answers the interrupt with BUS SSYN L.

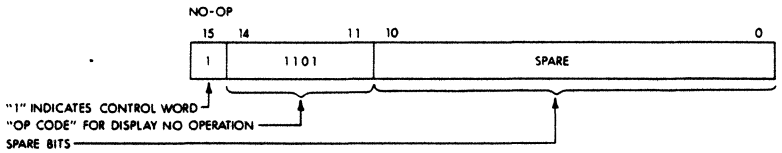
SET GRAPHIC MODE



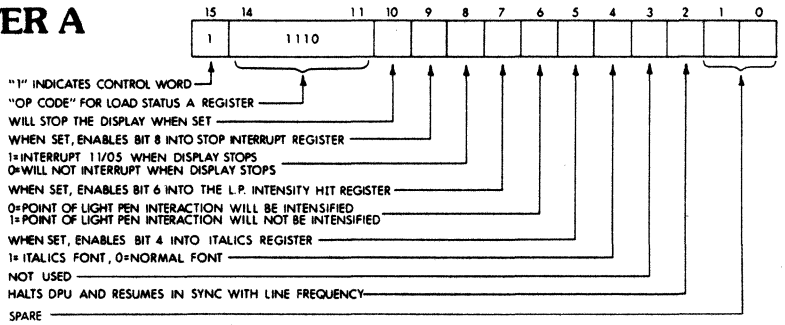
JUMP



NO-OP



LOAD STATUS REGISTER A



LOAD STATUS REGISTER B

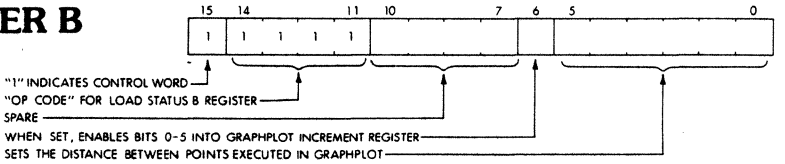


Figure 3-8 Instruction Word Functions

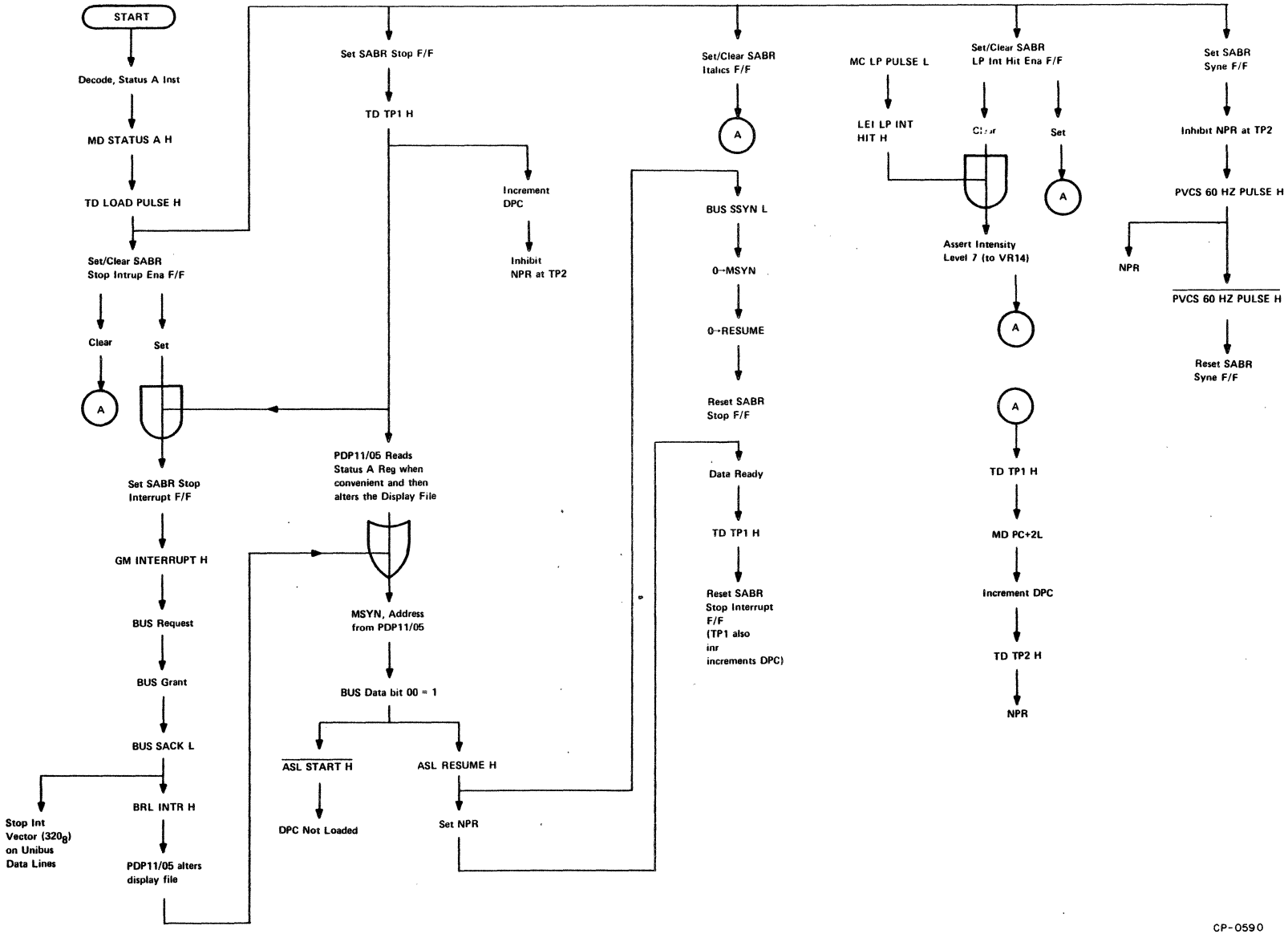


Figure 3-9 Status A Instruction Flow Diagram

NOTE

Do not stop the display (bit 10 = 1) and synchronize the display (bit 2 = 1) with the same Load Status Register A instruction. To do so causes the display to stop and then start again immediately, i.e., before the PDP-11/05 acts on the Stop Interrupt.

The Italics flip-flop can be set or cleared with a Load Status Register A instruction to control the font of the displayed characters. Briefly, when the Italics flip-flop is set the VR14 X and Y drive signals are mixed and thus produce the italics effect. The DPC is incremented and another NPR placed on the Unibus in the usual manner as a function of timing.

The third flip-flop that can either be set or cleared is SABR LP Int Hit Ena. Each light pen hit (MC LP PULSE L) triggers a 74123 single-shot to assert the 2 μs signal LEI LP INT HIT H. If this pulse finds the SABR LP Int Hit Ena flip-flop in a reset condition (drawing M7013-GM and Figure 3-10) signals GM INT (3:0) L are asserted. This forces intensity level 7 to be generated in the VR14 (unless already asserted by the display program) for 2 μs at the point where the light pen is aimed; image brightness increases to the highest level possible for the particular setting of the VR14 front panel BRIGHTNESS control.

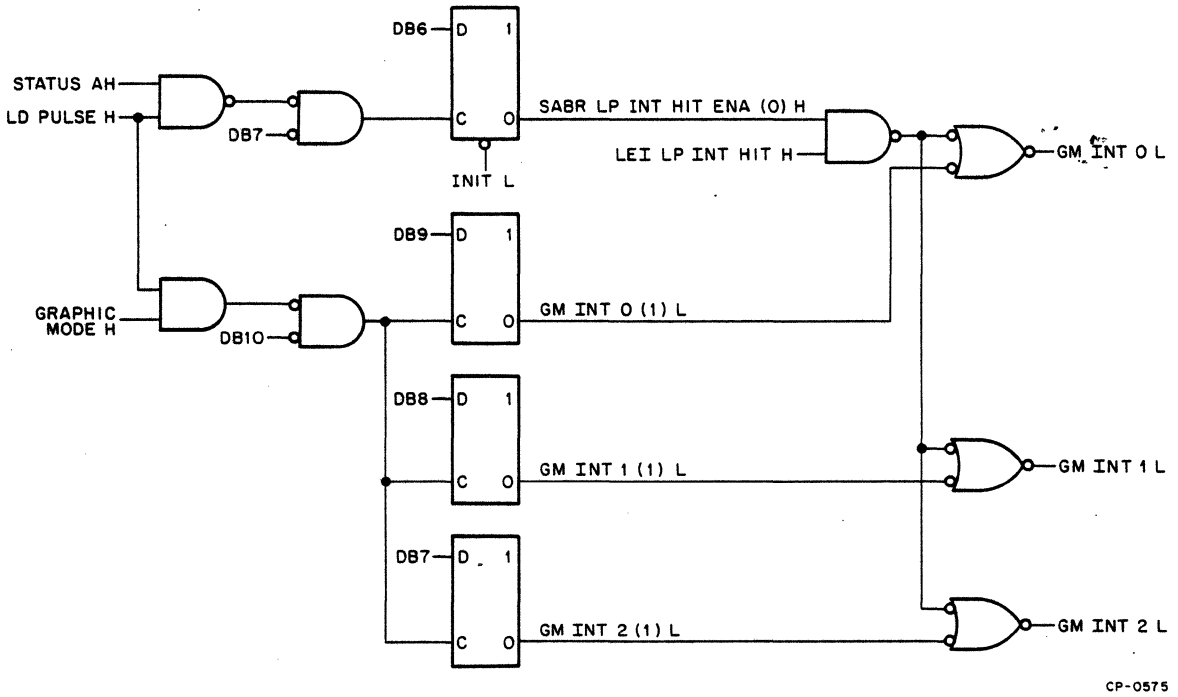


Figure 3-10 M7013 Intensity Level Control

One of the factors controlling the brightness of a given CRT display is the repetition rate at which the display is intensified. This rate depends on the display program execution time, i.e., the size of the display program; a relatively large display of many characters and/or vectors is intensified less often than a smaller display program. Consequently, a smaller display, intensified at a faster rate, appears brighter because there is insufficient time for the CRT fluorescence to decay. Figure 3-11 shows this relationship between image brightness and display execution time. This variance in brightness can be eliminated for all displays that take less than 16.67 ms to intensify by establishing a single program repetition rate. With the SABR Sync flip-flop set by the Load Status Register A

instruction, the next NPR is inhibited (drawing M7013-TD) until PVCS 60 Hz PULSE H is asserted. This 70-ns pulse is the output of a 74123 Monostable Multivibrator that is triggered by a 60-Hz signal from the PDP-11/05 power supply. Therefore, those display program routines that contain a Load Status Register A instruction with Sync specified can have an NPR repetition rate of no faster than 60 Hz; the brightness level is uniform when all display programs with an execution time of less than 16.67 ms are so structured. The brightness level is halved for longer programs. The SABR Sync flip-flop is reset on the trailing edge of PVCS 60 Hz PULSE H.

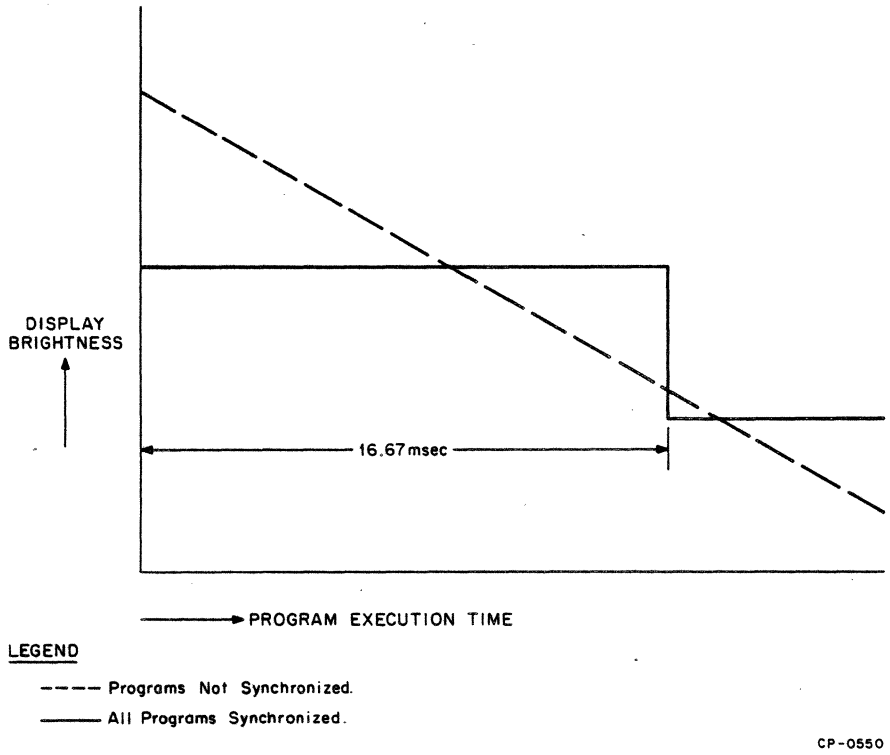


Figure 3-11 Relationship of CRT Brightness to Program Length

3.2.8.2 Load Status Register B – Decoding this instruction results in a relatively simple operation. Unibus data bits (15:11) = 11111_2 denote a Load Status Register B instruction when an NPR from the GT40 Display Processor causes the MM11 Core Memory to be read. As the result of this bit configuration, the mode decode logic generates MD STATUS B H. This signal, on the assertion of timing signal TD LOAD PULSE H and, provided bit 6 of the instruction is a 1, gates bits 0 through 5 of the instruction (BDL DB 05:00 L) into the Graphplot Increment Register (drawing M7013-SABR). This register, type 74174 (five D-type flip-flops), outputs SABR INC (5:0) H to the Graph or Character Multiplexer (drawing A320-DCR) when the display processor is in the Graph X or Graph Y mode. These five bits define the distance between intensified points in a graphplot. Figure 3-12 illustrates the relationship of the Graphplot Increment Register to the A320 Display module.

Timing proceeds in the normal manner and another NPR is issued (drawing M7013-TD) when TD TP 2 H is asserted.

3.2.8.3 Jump Instruction – Of the five instructions used by the GT40 Display Processor, Jump is the only one that consists of two words. The first word uses bits 11 through 15 (= 11100_2) to specify the op code; the eleven low-order bits are spares. However, all 16 bits of the second word are used. This part of the instruction contains an address that identifies the next core memory location to be read. Replacing the current address in the DPC, this new

address interrupts the normal retrieval of sequential (contiguous) memory locations and causes a new memory area to be accessed. The Jump instruction is thus used to connect sections of a program, e.g., instructions and data, that are located in separate areas of memory and to cause certain routines in a program (or the entire program itself) to be repeated.

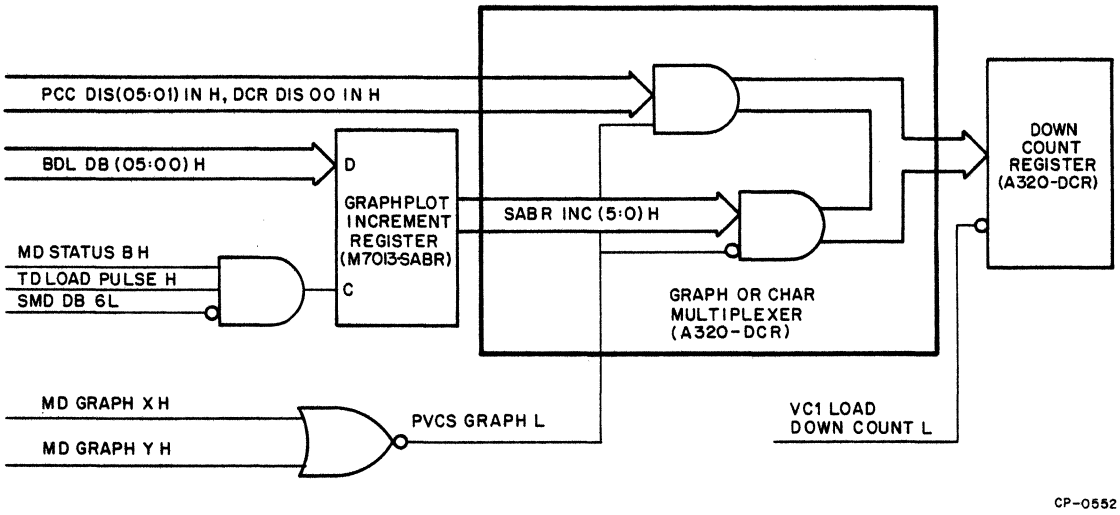


Figure 3-12 Graphplot Logic

As a result of the handshaking that takes place between the GT40 Display Processor and the MM11 Core Memory, BCL DATA READY L initiates the generation of a timing pulse stream. The first of these, TD LOAD MODE H (Figure 3-13), clocks bits 11 through 13 of the first word of the Jump instruction into the Control Mode Register and asserts MD JUMP H. As is the case when any instruction is decoded (bit 15 = 1), TD LOAD MODE also asserts MD CLR WORD L, which resets the Word flip-flop (drawing M7013-PVCS). At TP1 time the DPC is incremented by two when MD PC + 2 L is generated; the DPC now contains the core memory address of the second word of the Jump instruction. This is placed on the Unibus address lines and on the leading edge of TD TP2 H an NPR is issued. The specified memory location is then read and the contents placed on the Unibus data lines; this data is the address of the next memory location to be accessed. The Word flip-flop is set at the trailing edge of TD TP2 H 50 ns after the NPR is issued. Signal PVCS WORD (1) H, indicating the second word of an instruction/data word is on the Unibus, is ANDed with MD JUMP H to assert MD JUMP WORD (1) L (drawing M7013-MD). This latter signal will inhibit the forthcoming TD LOAD MODE H signal from clocking the Control Mode and Data Mode Registers and the Cont Word flip-flop; their contents and output will remain unchanged when the second word of the instruction is accepted by the display processor. MD JUMP WORD 1 L will also inhibit the assertion of MD CLR WORD L and the Word flip-flop is not cleared (if BDL DB15 = 1).

When the second word of the Jump instruction is read, the ensuing four-signal series of timing pulses are generated by the timing logic. With the advent of TD LOAD PULSE L, MD JUMP LOAD PULSE H is asserted. This signal gates the data on the Unibus [BDL DB (15:01)] into the DPC (drawing M7014-PCC) replacing the current address. The DPC is not incremented by the subsequent TD TP1 H because MD JUMP WORD 1 L continues to be true. At the leading edge of TD TP2 H another NPR is issued and the display program now "jumps" to the new memory address. The operation concludes with the clearing of the Word flip-flop at the trailing edge of TD TP2 H.

3.2.8.4 No-Op Instruction – No-op is the simplest of the display processor instructions in that there is no resultant display function or change of parameters. No-op is used as a core filler in the display program or to replace another unwanted instruction.

In response to an NPR, the instruction is input to the GT40 Display Processor via the Unibus data lines. The accompanying BUS SSYN L signal asserts BCL DATA RDY L which triggers the stream of timing pulses. MD DNOP L is generated by the decoding logic when the op code (bus bits 11 through 15 = 11101_2) is decoded at TD LOAD MODE time. The display program counter is then incremented by MD PC + 2 L when TD TP1 H is asserted. To complete the operation, an NPR is generated by TD TP2 L and the next memory location is read.

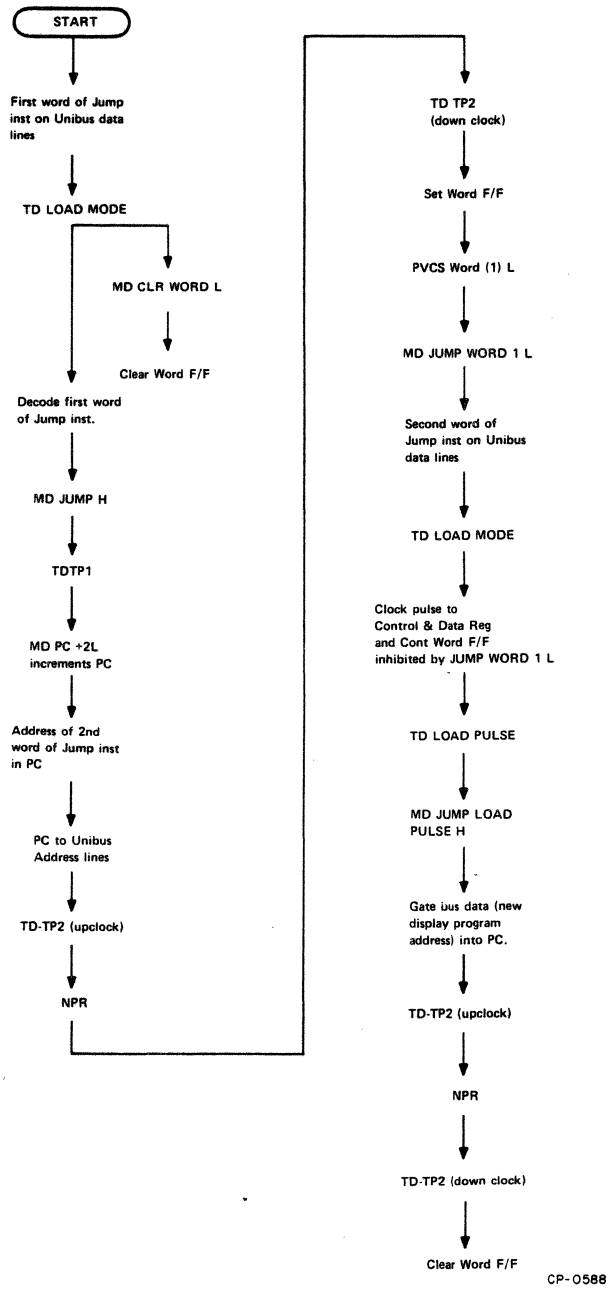


Figure 3-13 Jump Instruction Flow Diagram

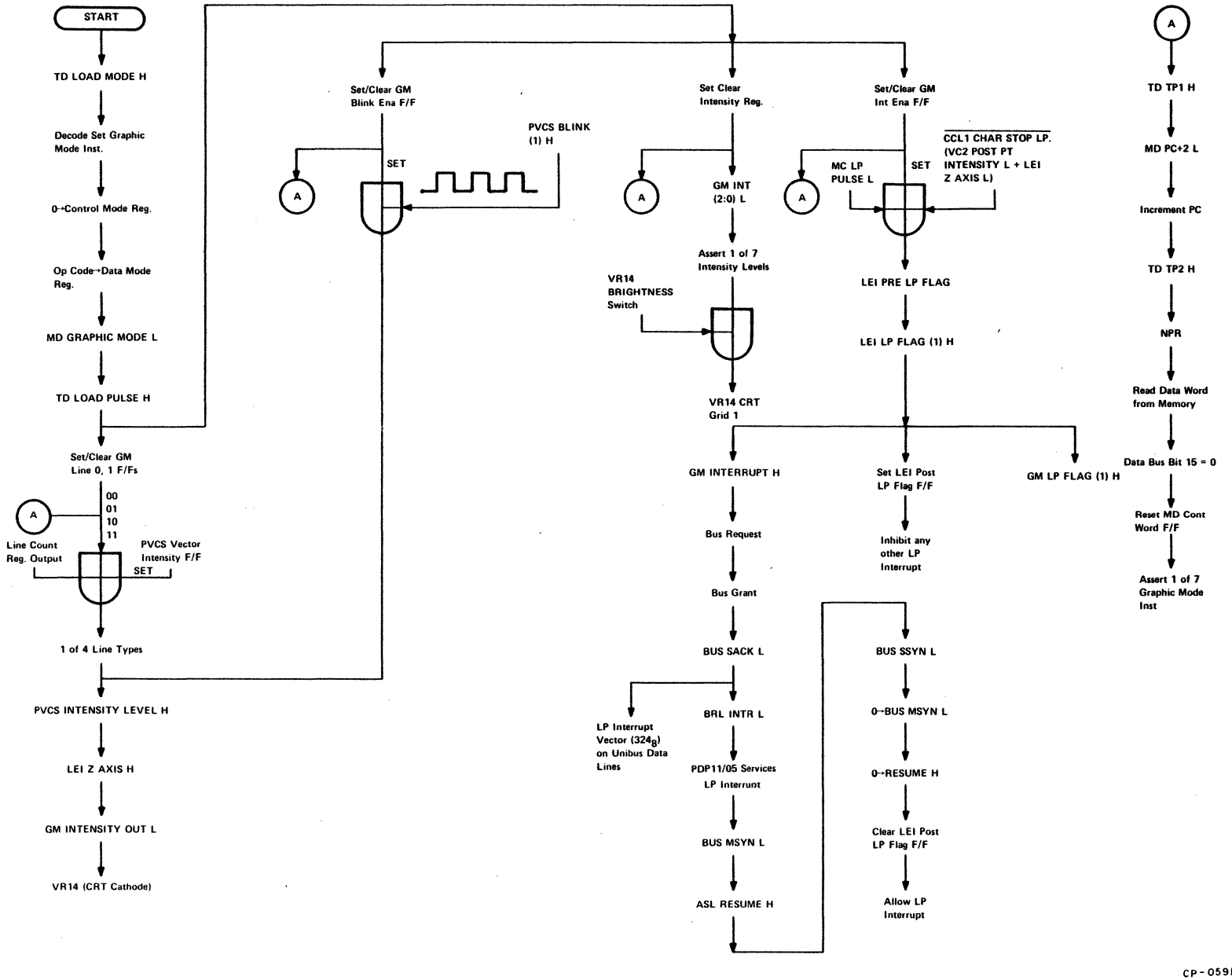


Figure 3-14 Set Graphic Mode Instruction, Flow Diagram

3.2.8.5 **Set Graphic Mode Instruction** – This instruction could be termed the data instruction in that it contains the code (bits 14:11 = $0XXX_2$) that identifies one of the graphic or data mode instructions (Table 3-5 and Paragraph 3.2.7). This data mode op code denotes the type of CRT display that will be generated, i.e., vector, point, character, etc. The eleven low-order bits (bits 0 through 10) of the Set Graphic Mode instruction are used to specify certain display parameters: intensity level, light pen interrupt enable, blink, and line type.

When an NPR results in a Set Graphic Mode instruction being read from memory, bit 15 = 1 and bit 14 = 0 are decoded at Load Mode time and the Control Mode Register is loaded to 000 (drawing M7013-MD and Figure 3-14). The MD Cont Word flip-flop is set at this time (if not already set) and the contents (000_2) of the Control Mode Register are output from the Mode Select Multiplexer to the 74154 Mode Decode, which asserts the signal MD GRAPHIC MODE L.

The signal TD LOAD MODE L also clocks the data mode bits (Unibus bits 13:11) into the Data Mode Register. However, the data mode instruction is not asserted because the Control Mode Register is selected at this time.

The assertion of TD LOAD PULSE H causes one or more of the four control flip-flops and three Intensity Register flip-flops to be set or cleared as determined by bus data bits 0 through 10. At TD TP1 time the DPC is incremented by two (MD PC + 2 L) and then with TD TP2 H the next NPR is generated. A data word (or a Jump and then a data word) is read from the MM11 core memory as the result of this NPR. The type of data word that should be read now was determined by the op code specified in the Set Graphic Mode instruction previously read and presently stored in the Data Mode Register. However, all data words have bit 15 = 0 and at Load Mode time the clock inputs to the Control Mode and Data Mode Registers are inhibited (the two registers remain unchanged) and the Cont Word flip-flop is cleared. The (1) H output from this flip-flop, now low, gates the contents of the Data Mode Register into the Mode Select Multiplexer and then to the Mode Decode Register. Therefore, at Load Mode time of the data word the signal MD GRAPHIC MODE L is dropped and one of the seven graphic mode instructions is asserted.

The flip-flops controlled by the Set Graphic Mode instruction are GM Line 0, GM Line 1, GM Blink Ena, GM Int Ena, and the three in the Intensity Register. All are shown on drawing M7013-GM.

The two line flip-flops are used to generate one of four vector line types (Table 3-7) that are shown in Figure 4-13. The output from these flip-flops gate one of four data inputs into the 74153 Line Decoder, shown on drawing M7013-PVCS, when the PVCS Vector Intensity flip-flop is set. Both line flip-flops must be in the reset state if a solid line is to be displayed; this configuration selects the +3 VB input. The other three line types require one or more inputs from the 74193 Line Count Register, shown on the same drawing.

Table 3-7
Line Decoder Signals

GM Line Flip-Flop		Selected Input(s)	Type of Line Generated
1 (1) H	0 (1) H		
L	L	+3VB	Solid
L	H	PVCS LC 4 H	Long Dash
H	L	PVCS LC 3 H	Short Dash
H	H	(PVCS LC (2:1) H• PVCS LC 3 L) + PVCS LC 4 L	Dot Dash

The Line Count Register, a 4-bit binary counter, is preset to 15_{10}, i.e., all outputs are asserted, at the beginning of the vector (PVCS LD LINE CT REG L). VC2 DOWN COUNT CLK L is divided by a single stage frequency divider and this divided clock is used to clock the Line Count Register. Timing for this operation is shown in Figure 3-15. VC2 DOWN COUNT CLK L is used because its instantaneous frequency is the same as the frequency of the vector being drawn.

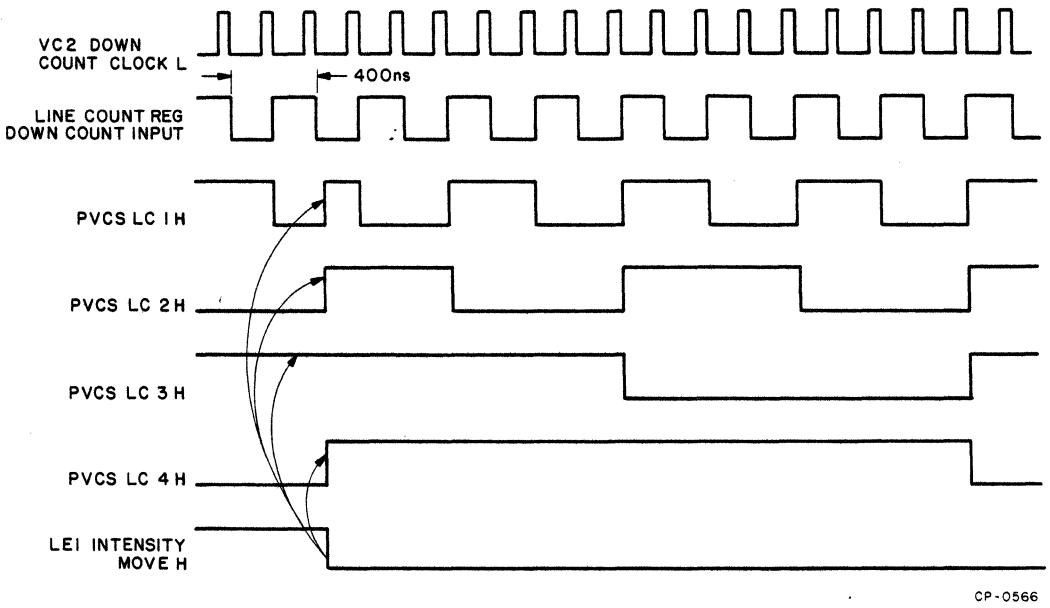


Figure 3-15 Line Count Register, Timing Diagram

The line counter output becomes PVCS INTENSITY LEVEL H, which is sent to the M7014 module where it enables LEI Z AXIS H. LEI Z AXIS H is then returned to the M7013 module where it becomes GM INTENSITY OUT L. This latter signal is routed through the A320 module to the VR14 where it causes the CRT cathode to go from ≃ + 62V to 0V and thus go into conduction. Any of the four line types can also be made to blink because the blink function, if selected, overrides the output of the line decoder.

The blink operation, where the display is repeatedly blanked and unblanked, is a means for gaining the operators attention. The two bits (3 and 4) in the Set Graphic Mode instruction that control the blink operation are used to set or reset the GM Blink Ena flip-flop. The (1) H and (0) H outputs of this circuit are input to two NAND gates in the PVCS INTENSITY LEVEL H circuit where the (1) H output gates PVCS BLINK (1) H and the output of the line decoder to assert the intensity level. Therefore, when Blink Ena is set, the intensity level to the VR14 is controlled by the output of the PVCS Blink flip-flop. This flip-flop, clocked by the high-order output of a 7493 frequency divider (Divide By Four Register), is set for 266 ms and then reset for 266 ms. Consequently, all, or a selected portion of the CRT display, repeatedly flashes on and off (about twice each second) as long as the GM Blink Ena flip-flop is set. Figure 3-16 is a timing diagram for this and the bell tone circuits.

The 7493 Frequency Divider (drawing M7013-PVCS) is clocked by a repeatedly asserted (60 Hz) output from a 7413 Schmitt trigger. (The input to the 7413 is derived from the power supply.) Outputs from the frequency divider are divisions of the input: 30, 15, 7.5, and 3.75 Hz. Only two outputs are used, however, the R1 (1), termed PVCS STROBE BELL L, and the R3 (1), used to clock the Blink flip-flop.

The bell tone operation, although it is not a function of the Set Graphic Mode instruction, is described at this point because the initiating signal, PVCS STROBE BELL L, is an output of the 7493 Frequency Divider. The bell tone sequence begins with the assertion of ASL BELL CHAR L when the PDP-11/05 addresses the GT40. This signal is generated when the CPU tries to write in location 172002, the Status Register (Unibus control bit C1 is low, BUS A 01 = 1, and BUS A 02 = 0). The PDP-11/05 flags the GT40 with BUS MSYN L, which asserts ASL DISPLAY ENABLE L. Nothing occurs until the PDP-11/05 drops BUS MSYN L in response to BUS SSYN L from the GT40. At this time the ASL BELL CHAR L signal goes false and a 7474 D-type flip-flop in the bell tone circuit (drawing M7013-CCL-2) is clocked set. The (1) H output now primes the J input to the Bell flip-flop, which is then set on the

next negative-going transition of PVCS STROBE BELL L. The resultant CCL2 BELL L signal is sent to the A320 module (drawing A320-MC) where it is delivered to the LK40 Keyboard via the scope cable, the VR14 back panel, and the keyboard cable. In the LK40, CCL2 BELL H, now called SPK IN, generates an audible, 1000-Hz signal (Paragraph 3.4.3.4).

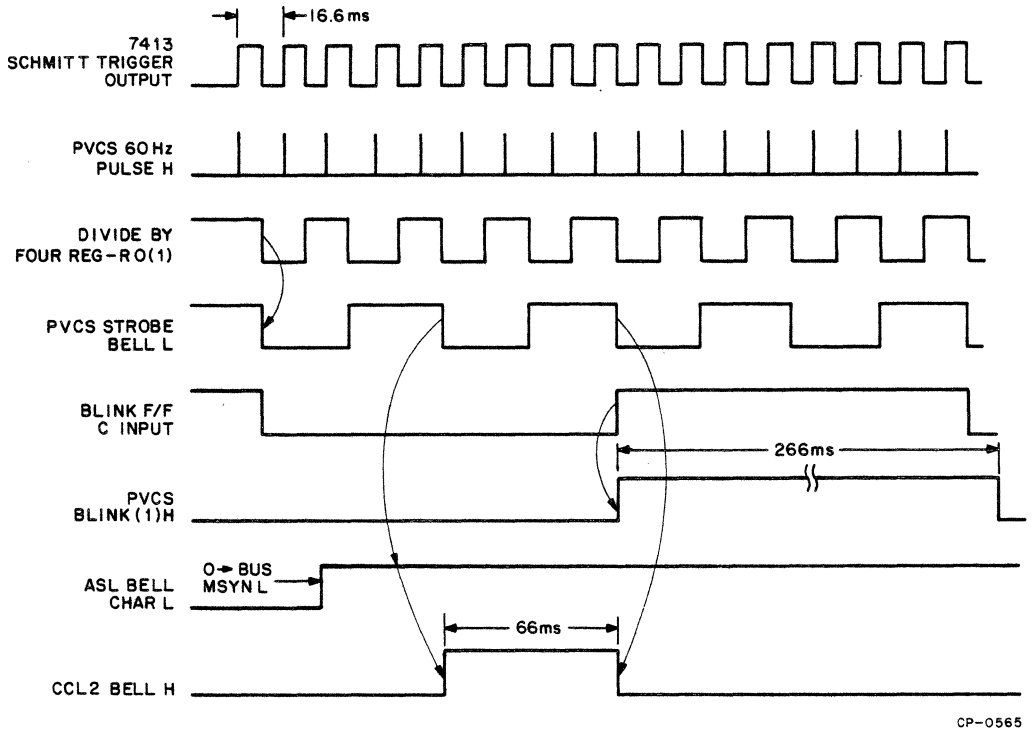


Figure 3-16 Bell Tone and Blink Timing Diagram

On the next negative-going transition of PVCS BELL STROBE L the Bell flip-flop is reset and CCL2 BELL H is terminated; the audible tone from the LK40 speaker also stops. As shown in Figure 3-16, the bell tone is sounded for one 66-ms period each time the PDP-11/05 causes ASL BELL CHAR L to be asserted.

The parallel output of the three flip-flop Intensity Register (Figure 3-10 and drawing M7013-GM) is used in the VR14 to generate one of seven intensity levels to grid 1 in the CRT. This is the method employed, together with the VR14 front panel BRIGHTNESS switch, for controlling the CRT brightness level (Paragraph 3.5.9.5). Unibus bits 7, 8, and 9 are clocked into the register at Load Pulse time by the enabling bus bit (SDM DB 10 L) to assert GM INT (2:0) (0) H. As previously described, any configuration of the three signals from the Intensity Register is momentarily overridden (all three are asserted) if a light pen hit occurs after the SABR LP Int Ena flip-flop has been cleared by a Load Status Register A instruction.

One other flip-flop is controlled by the Set Graphic Mode instruction. When the GM LP Int Ena flip-flop is set by this instruction a subsequent light pen (LP) hit (MC LP PULSE L) causes an LP interrupt (flag) to the PDP-11/05. Only one LP flag is allowed on any one point, vector, or character and LP interrupts for other areas of the display are inhibited until the interrupt operation in progress is completed.

The LEI Pre LP Flag flip-flop in the light pen logic is primed by two conditions: GM LP Int Ena flip-flop set and CCL1 CHAR STOP LP H must be false indicating the LP hit is not on the first or last column of a character. When intensification occurs at the position (point, vector, or character) where the LP is aimed, the signal MC LP PULSE L is asserted (Paragraphs 3.5.9.6 and 3.5. 9.7) and the LEI Pre LP Flag flip-flop is clocked.

LEI PRE LP FLAG H primes the LP Flag flip-flop which is then set, if the LP hit is on a vector, on the trailing edge of VC1 VEC CLK H, or after the end of the operation (VC2 OP DONE L) if the hit was on a point, relative point, or character. In the case of a point or relative point operation, VC2 OP DONE L is caused by the 100 ns VC2 POINT DONE L that was initiated by VC2 POST PT INTENSITY L. The purpose of this sequence of signals is to incorporate a 3.2 μs delay in the LP circuit to compensate for an inherent delay in the light pen pulse from the 375 Light Pen. (Timing relative to this operation is shown in Figure 3-27.)

With the LEI LP Flag flip-flop set, LEI LP FLAG (0) H (low) asserts GM INTERRUPT H and LEI LP FLAG (1) L (true) presets the LEI POST LP FLAG flip-flop. At the same time, LEI LP FLAG (1) H is used to load the DACs (VC1 LOAD DAC H) with the coordinates of the LP hit. LEI POST LP FLAG (1) H halts the VC1 VEC CLK H signals and all further light pen flags are inhibited until the LEI POST LP FLAG flip-flop is reset. This occurs when the PDP-11/05 issues a resume (ASL RESUME H) or a start (VC1 RESET L). If ASL RESUME L is asserted the vector continues from the point where it was stopped. The start operation (Paragraph 3.2.3) causes the DPC to be loaded with a new display program address. The GM INTERRUPT H signal generates a bus request and subsequently a bus interrupt to the PDP-11/05. The ensuing sequence is similar to a stop interrupt (shown in the Status A instruction flow diagram, Figure 3-9). The most notable exception is that a light pen interrupt vector (324_8), instead of a stop interrupt vector, is placed on the Unibus data lines. The PDP-11/05 reads in the vector address, enters into a particular software routine, and transmits BUS SSYN L to the display processor. The consequent BCL SSYN H signal is ANDed with BRL INTR H (drawing M7014-BCL) to generate BCL INTR DONE H and BCL REQ CLR L. This latter signal generates ASL CLR FLAGS L which resets the LEI LP Flag flip-flop. The circuit is again receptive to LP hits until such time as the LP Int Ena flip-flop is reset.

Figure 3-17 sums up the routing of the LP pulse from the LP through the VR14 to the GT40 where an LP interrupt, if enabled, is asserted on the Unibus. The LP hit is also shown returning to the VR14 as an increased intensity level if SABR LP Int Ena is not set.

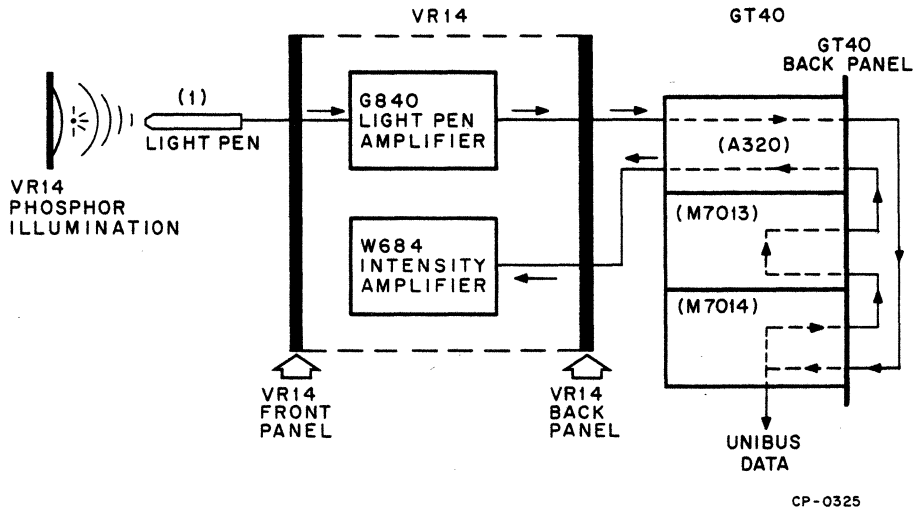
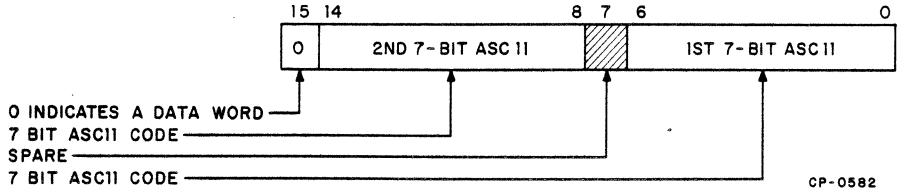


Figure 3-17 Light Pen Signal Path

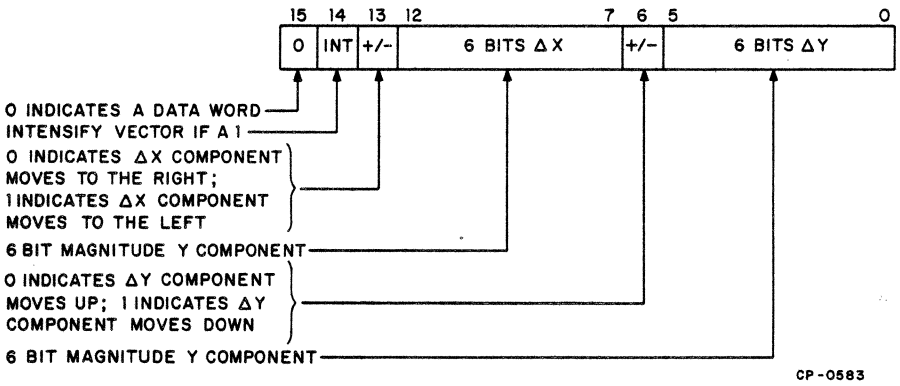
3.2.9 Data Words

Each of the seven display modes that can be initiated by the Set Graphic Mode instruction requires a distinctive data word. These data words convey information such as vector length, vector and point screen position (coordinates), and the direction a vector or relative point is to move.

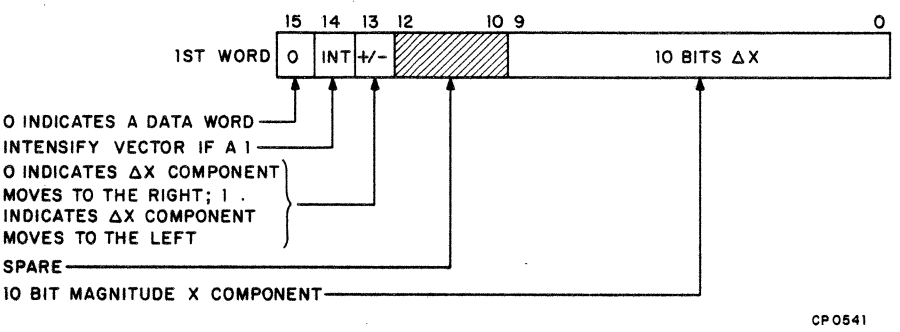
CHARACTER DATA FORMAT- Mode 0000



SHORT VECTOR MODE- Mode 0001



LONG VECTOR DATA FORMAT- 0010



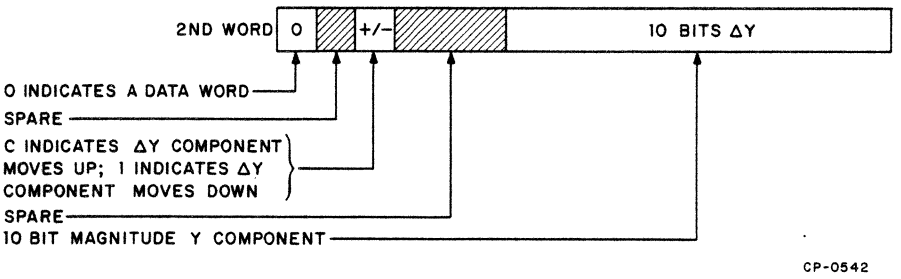
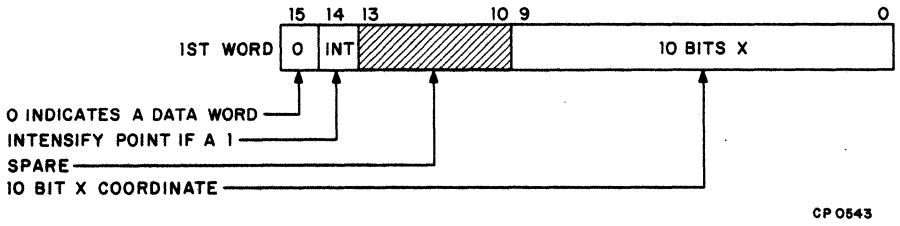
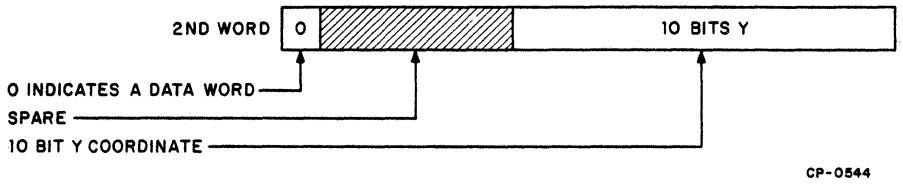


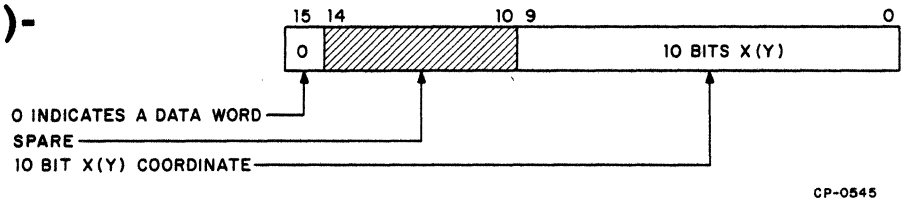
Figure 3-18 Data Word Formats (Sheet 1 of 2)

POINT DATA MODE- Mode 0011





GRAPHPLOT X(Y)- Mode 0100(0101)



RELATIVE POINT MODE- Mode 0110

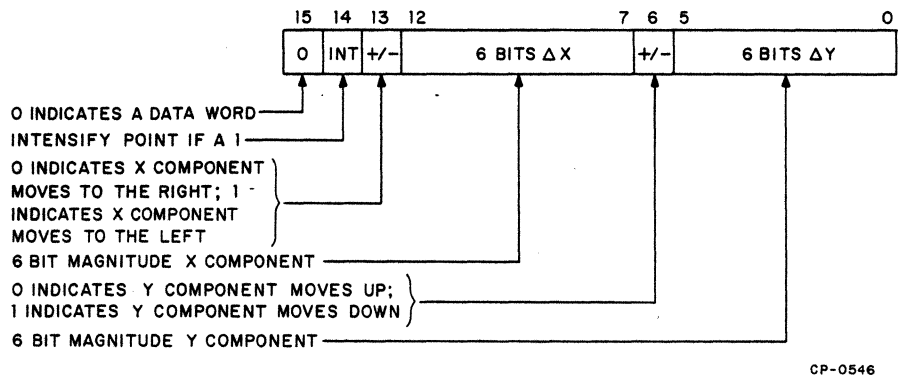


Figure 3-18 Data Word Formats (Sheet 2 of 2)

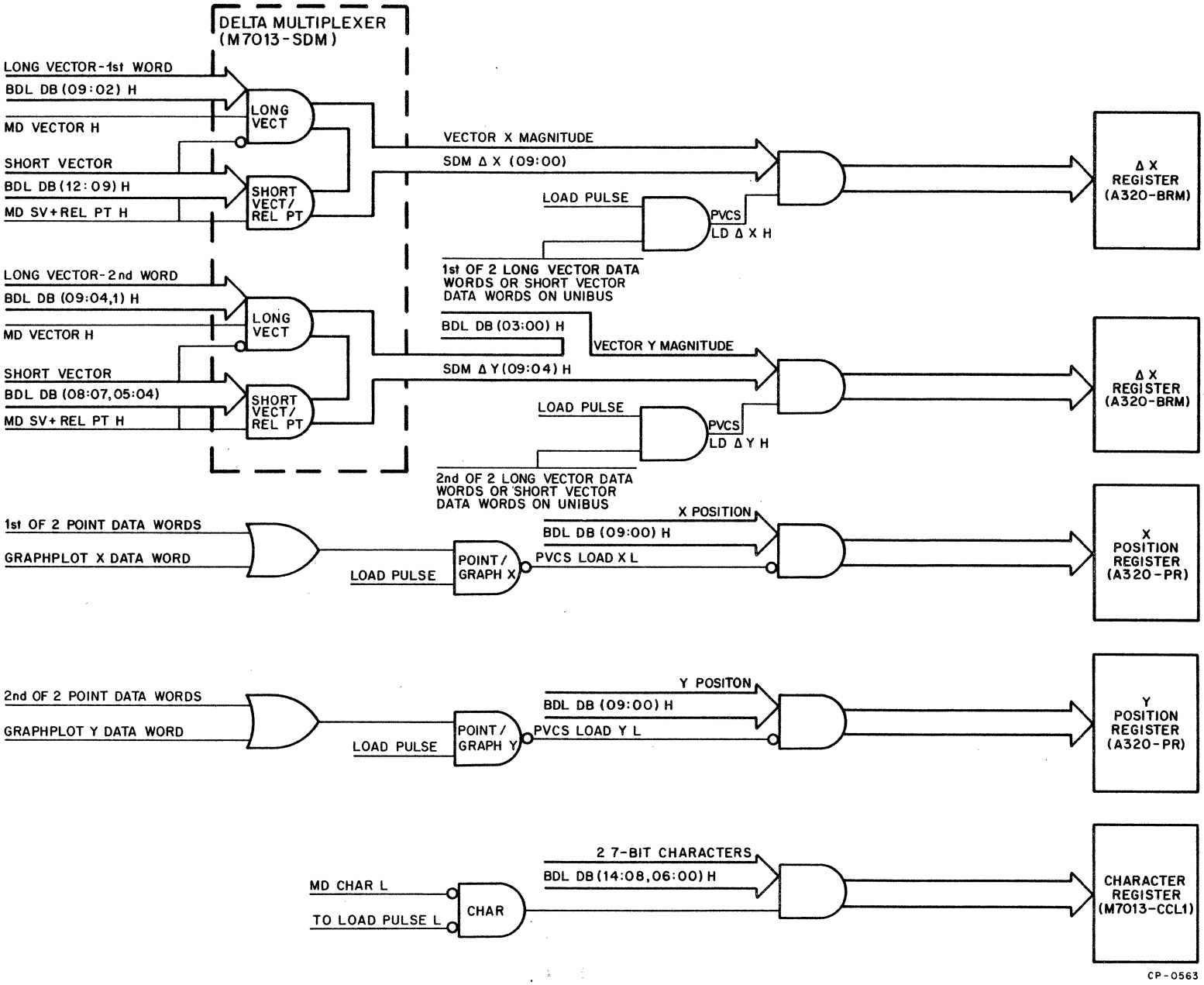


Figure 3-19 Data Word Storage

Data words are 16 bits long and are identified by bit 15 = 0. Two word types, long vector and point, are always read in pairs; the first word contains X information and the second (following) word contains Y information. In the other modes all data relative to a single coordinate or expression of magnitude is contained in one 16-bit word.

Figure 3-18 shows the format and bit functions for each type of data word. The different data words, when received from the Unibus data lines, are delivered to specific destinations. Figure 3-19 shows data word routing from the bus to the initial storage register. In brief, short and long vector and relative point words go to the ΔX and ΔY Registers in the A320 module, point and Graphplot X/Y words are input to the X and Y Position Registers, also in the A320 module, and character words are gated into the Character Register. The specific gating signals required to transfer a data word into these registers are a function of the data mode in effect at the time the data word is placed on the Unibus.

3.2.9.1 Data Word Functions – Use of the data words is determined by the particular graphic mode instruction being executed, i.e., that mode presently stored in the Data Mode Register.

Character data words contain the codes for two 7-bit characters that are decoded and display two 6 X 8 dot format characters. The characters are selected from the 127 (96 ASCII and 31 special characters) available in the GT40 print repertoire. A simplified program example of the type used to display a group of characters is listed in Table 3-8; Figure 3-20 shows the result of this sequence (Paragraph 4.2.7).

Long and short vector data words contain information that defines the magnitude or length of the vector (termed ΔX and ΔY) and the angle at which the vector is to be drawn (left-right, up-down). The ΔX and ΔY components and the direction bit are algebraically added to produce a vector of definite length and direction. The long vector data requires two words; they are read back to back. Table 3-8 and Figure 3-20 show a programming example and the resultant display, respectively, for a long vector. A second vector can be drawn in a similar manner; the starting point is the termination point of the first vector, which has been retained following completion of the first vector.

Table 3-8
Control and Data Word Applications

Display Type	Typical Program Sequence	Purpose for the Control/Data Word
Character	Set Graphic Mode Instruction (Point Mode)	Establishes the mode for the data that follows.
	2 Point Data Words	Not intensified; defines the screen location of the first character displayed.
	Set Graphic Mode Instruction (Character Mode)	Establishes the operational mode for the data that follows.
	Character Data Word	Contains the codes for the first two characters that are displayed. Screen positioning is automatically moved (to the right) after each character is displayed.
	Character Data Word	Contains the codes for the second two characters.
	etc.	This sequence is repeated until the message is completed at which time the mode is changed. A second line of characters can be displayed if carriage return (CR) or line feed (LF) is sensed.

Table 3-8 (Cont)
Control and Data Word Applications

Display Type	Typical Program Sequence	Purpose for the Control/Data Word
Long Vector	Set Graphic Mode Instruction (Point Mode)	Sets the mode for the data that follows.
	2 Point Data Words	May be intensified; defines the screen location for the start of the vector to be displayed.
	Set Graphic Mode Instruction (Long Vector Mode)	Establishes the operational mode for the data that follows. The GT40 uses the data in 2 word groups.
	Long Vector Data Word (1st word)	Contains the ΔX component, intensify, and X direction bits for the 1st vector.
	Long Vector Data Word (2nd word)	Contains the ΔY component and the Y direction bit. The first vector is now displayed.
	Long Vector Data Words (1st and 2nd)	Display the second vector.
	etc.	Repeat the above sequence, until the mode is changed.
GRAPH Y	Load Status Register B Instruction	Contains the X constant that is stored in the Graphplot Increment Register.
	Set Graphic Mode Instruction (Point Mode)	Establishes the mode for the data that follows.
	2 Point Data Words	Intensified; locates and displays the first point and provides the starting (X) location for subsequent Graph Y data words.
	Set Graphic Mode Instruction (Graph Y Mode)	Establishes the mode for the Graph Y data words that follow.
	Graph Y Data Word	Contains the Y coordinate for the next point displayed. The X coordinate is derived from the previous X coordinate to which is added the constant in the Graphplot Increment Register. If the Point instruction is omitted, the first point is displayed at the left edge of the CRT.
	etc.	Repeat until mode is changed.

One application of the point data word has been described – to specify the starting point when characters or vectors are displayed. The data word can also be displayed as a single intensified point on the CRT. Subsequent data words in the same mode display other points in any relationship (distance, position) to each other (this is in contrast to a Graphplot display described below). Point data words are read in pairs. The first word contains a 10-bit X coordinate; the Y coordinate follows in the next word. The point may or may not be intensified as specified by bit 14 (first word); no magnitude or direction bits are included in either word.

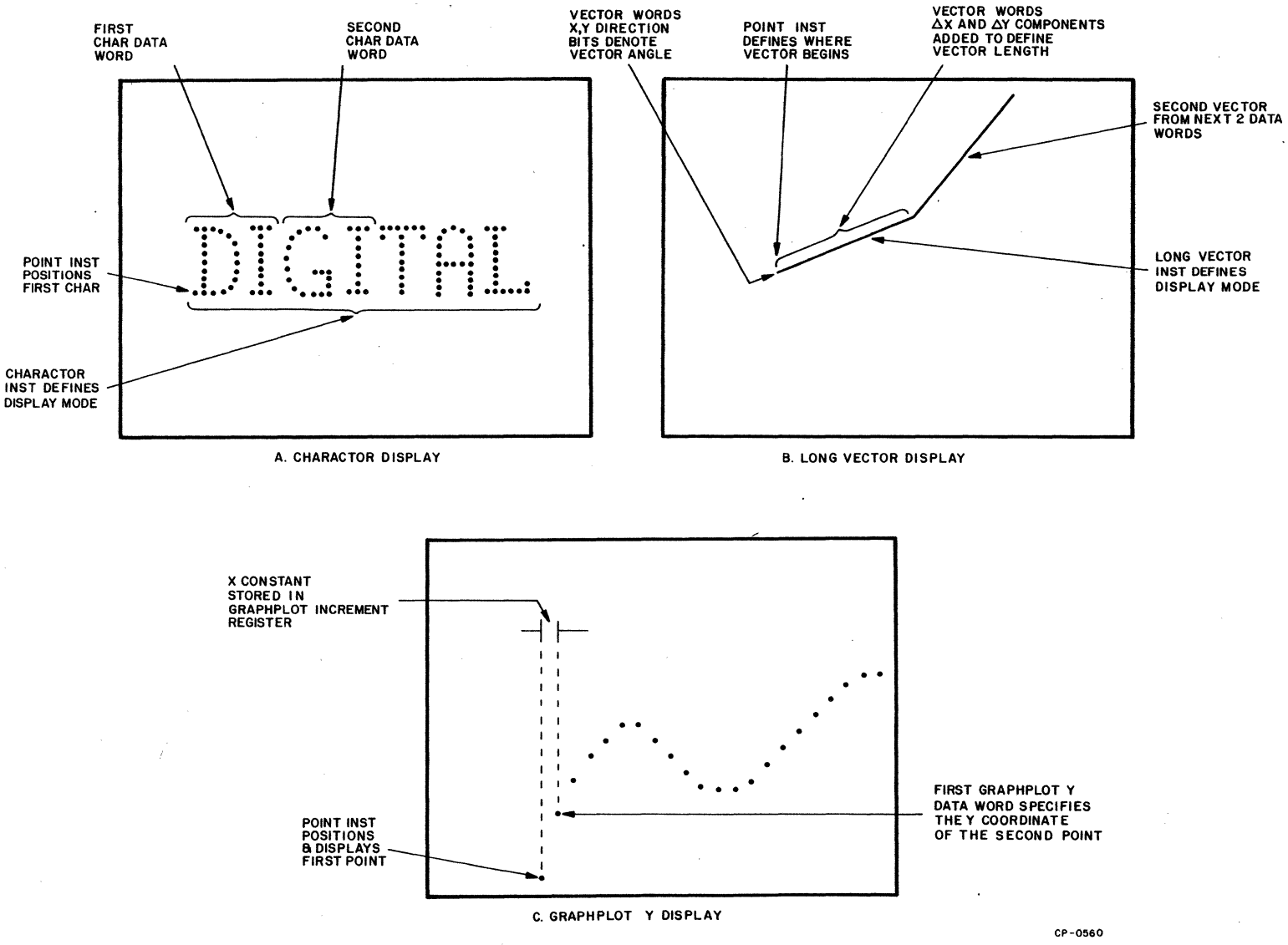


Figure 3-20 Display Examples

Graph (Graphplot) X and Graph Y words cause a series of points to be displayed that are equidistant in the opposite plane. For example, Graph Y data words (Figure 3-20) define variable positions in the Y dimension that are equidistant in the X dimension. The X coordinate is incremented after each point is displayed by a constant that was specified in a previous Load Status Register B instruction and now stored in the Graphplot Increment Register (Paragraph 3.2.8.2 and Figure 3-12). In the Graph X display the constant is used for equal increases in the Y direction.

Relative point data words have the same format as short vector data words. They function in the same manner except that intensification is inhibited until end of the "vector"; the consequent display appears as an intensified point.

3.2.10 Vector Generation

A vector is a line, drawn on the CRT screen, that represents a quantity having direction and magnitude. Both direction and magnitude are specified by two mathematical components, one for the X dimension and one for the Y dimension. It is the addition of these two vector components that produces the resultant vector on the CRT.

The long vector instruction is used to draw a line, the magnitude and direction of which are specified in two data words. The first word defines ΔX (X magnitude or length) and the second defines ΔY (Paragraph 3.2.9). The short vector instruction is similar to a long vector instruction except that the former requires only a single data word to convey both the ΔX and ΔY information. The following discussion assumes a long vector is being executed.

Figure 3-21a shows the bit position for the vector mode instruction. The first word specifies the magnitude of the X component (bits 0 through 9), bit 13 specifies the direction of this component, and bit 14 indicates if the vector is to be intensified. The second word is identical to the first except that it specifies the Y component and the intensification bit is omitted. Figure 3-21b shows the two components of a typical vector: an X magnitude of 1777_8 in the positive direction and the same magnitude and direction for the Y dimension. The resultant vector is the sum of the two and is drawn relative to the initial beam position on the CRT. Figure 3-21c illustrates the resultant if the ΔY component is halved to 1000_8; the angle of the vector from the horizontal decreases. Figure 3-21d shows the results if a negative value is specified in the Y axis (word 2, bit 13 = 1). In this case the vector is drawn in the negative Y direction relative to the starting point.

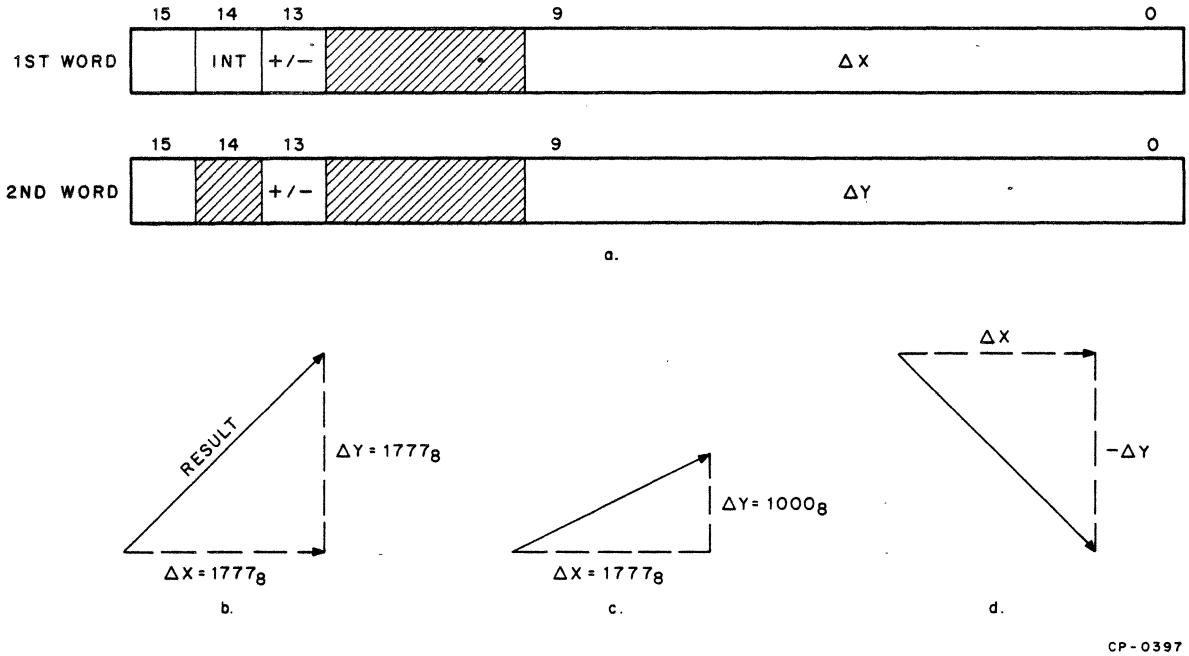


Figure 3-21 Vector Instructions and Examples

If the vector in Figure 3-21d is drawn on the CRT and the starting point is 0,0 the line is entirely cut off and cannot be seen. This is illustrated in Figure 3-22, which also depicts the situation where vector components of $\Delta X = 1777_8$ and $\Delta Y = 1777_8$, both being of the maximum magnitude, result in a partially cut-off display when the starting point is $1000_8, 1000_8$.

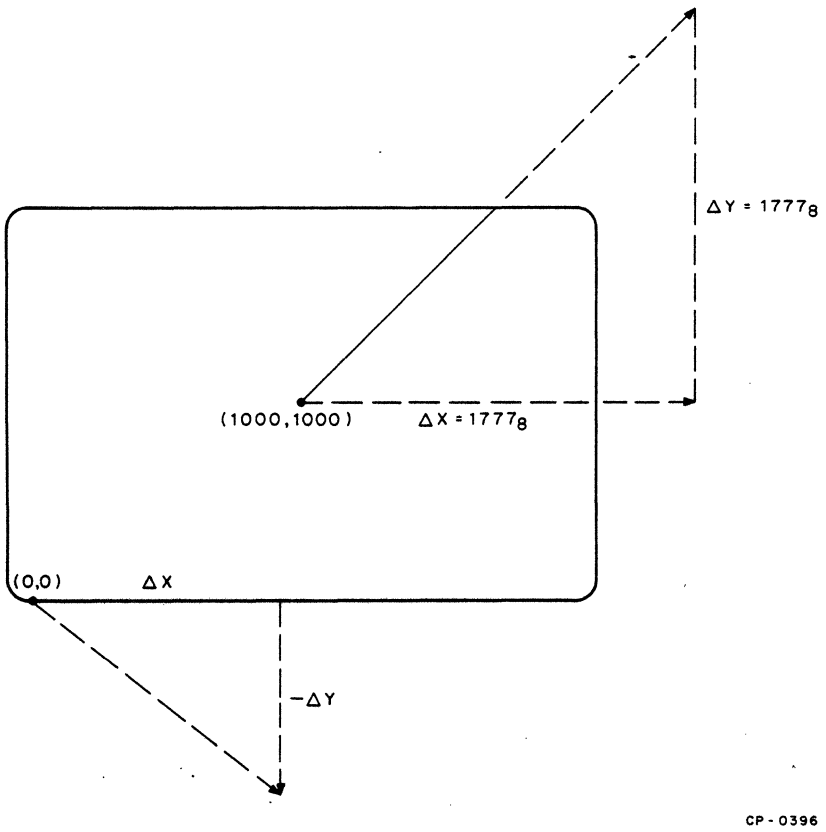


Figure 3-22 Cut-Off Vector Displays

3.2.10.1 General Description – Figure 3-23 is a simplified block diagram of the vector generating logic in the A320 module. The X and Y analog signals to the X and Y CRT deflection drivers are the summed output of the respective DACs and ramp generators. The DACs generate the analog equivalent of the digital contents of the holding registers. At the start of a vector the holding registers contain coordinates of the starting point. These might be the coordinates for the end of the previous vector, if several vectors are to be joined, or an initial set of coordinates brought in by a Point instruction, if an unconnected vector is to be drawn. At the conclusion of the present vector, the holding registers are updated by the X and Y Position Registers to reflect the termination coordinates. The ramp generators, not the DACs, generate the X and Y outputs. The DACs simply hold the basic beam position. This is the initial beam position while the vector is being drawn and the final beam position after the vector is completed. The outputs from the ramp generators are two ramps, X and Y, whose slopes are proportional to the frequency of the COUNT X and COUNT Y clocks. Therefore, in determining the dimensions of the X and Y slopes, COUNT X and COUNT Y, in effect, control the angle of the displayed vector.

The COUNT X and COUNT Y pulses are equal to or less than the input clock signal (VC1 COUNT CLOCK L derived from PCC DIS CLOCK L) which is controlled by the X and Y Binary Rate Multipliers (BRM). The BRMs, in turn, are controlled by the "normalized" magnitude components in the ΔX and ΔY Registers. The contents of the ΔX and ΔY Registers are also compared with each other and the larger of the two is loaded into the Down Count Register to control vector length. As the vector is being drawn the Down Count Register is clocked by either COUNT X or COUNT Y; the vector stops when the Down Count Register = 0.

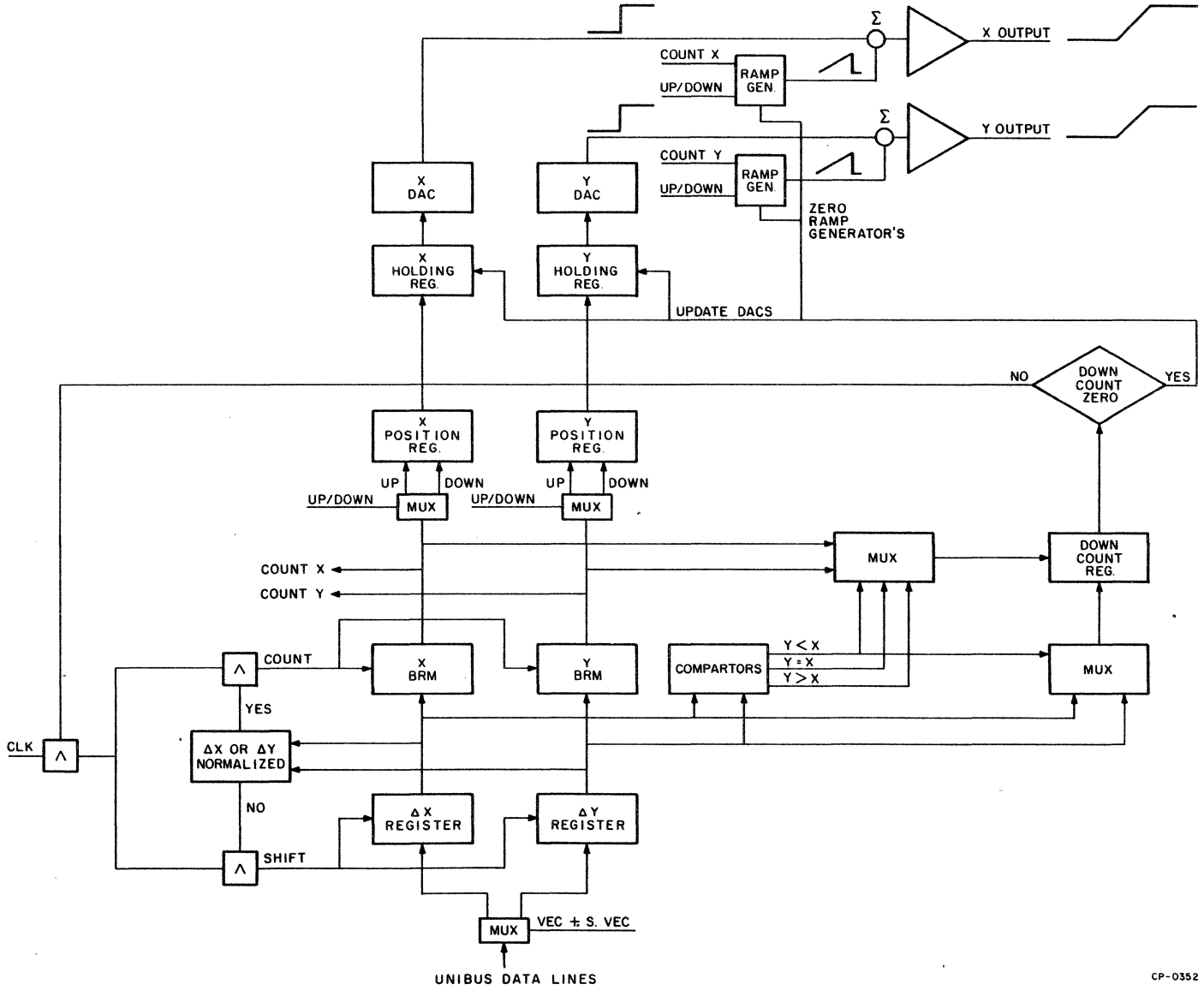


Figure 3-23 Vector Generator, Block Diagram

The X Position and Y Position Registers are continually being up-counted or down-counted while the vector is being drawn; therefore, they are dynamic registers in that they reflect the current beam position. (In the event of an LP interrupt while the vector is being drawn, the exact coordinates of the LP hit are available to the PDP-11/05.) These two registers, shown on drawing A-320-PR, can be direct set as the result of a Point instruction. As in the programming example given in Table 3-8, this instruction could be used to pre-position the beam prior to intensifying a vector. At the end of the vector the value held in the X and Y Position Registers is gated into the X and Y Holding Registers. As a result, the DACs outputs hold the unintensified beam at the point where the vector stopped.

3.2.10.2 Normalization – As noted previously, the angle of the vector on the CRT is a function of the relative frequency of the COUNT X and COUNT Y clock pulses. With the occurrence of each pulse, current is injected into a capacitor in the respective ramp generator and the output ramp rises proportionally as shown in Figure 3-24. It can be seen that it takes twice the time to attain a particular capacitor charge when the clock rate is halved. Therefore, the faster the clock rate the faster the capacitor is charged and the sooner the vector is drawn. Since one of the primary objectives is to draw the vector in the shortest possible time, it can be concluded that the fastest possible clock rate should be used. This is the purpose of the normalization process in the ΔX and ΔY Registers: to decrease the time it takes to draw a vector as much as possible and still retain the same X to Y magnitude ratio.

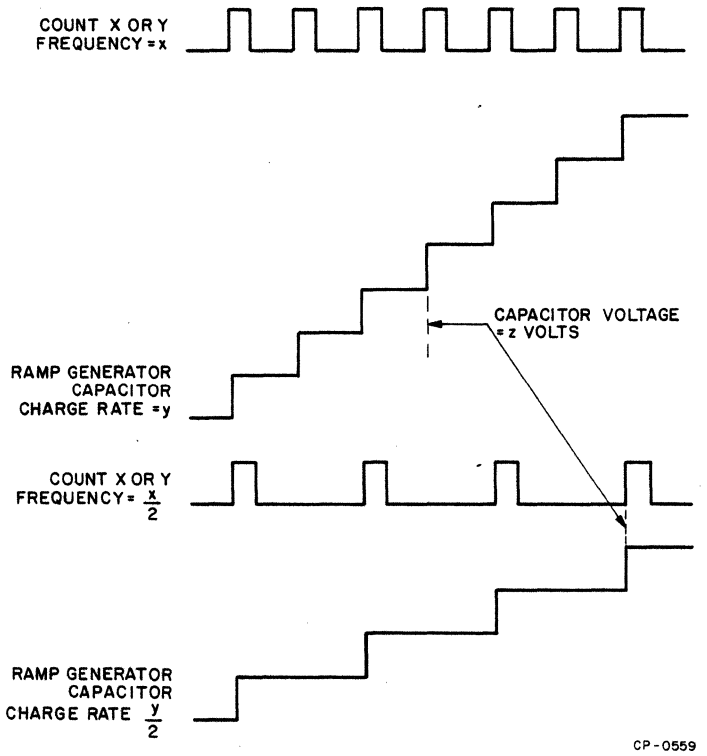


Figure 3-24 Relationship of Clock Frequency to Ramp Generator Output

The longest possible vector has a magnitude of 1777_8. It is clocked at a 5-MHz rate and takes about 200 μs to draw. A vector of half that length (1000_8) also takes about 200 μs to draw because it is clocked at a 2.5-MHz rate. If it were possible to clock the 1777_8 length vector at the 2.5-MHz rate it would take twice as long for the vector to be completed. This is not desirable (nor is it done) because time is critical; it shows, however, the relationship between the clock rate and the time it takes to display the vector.

When the two long vector data words are read from core memory, the ΔX and ΔY magnitude bits are loaded into the ΔX and ΔY Registers (drawing A320-BRM and Figure 3-19). Assume, for example, that ΔX = $+0177_8$ and ΔY = 0017_8, a 4:1 ratio. The ΔX component, being the larger of the two, is loaded into the Down Count Register to establish the absolute vector length and then the contents of the two Δ registers are simultaneously shifted left until the high order bit of one of them = 1; in this example the ΔX component becomes 1770_8 and the ΔY component becomes 0170_8. Now normalized, they are the largest possible figures that retain the 4:1 relative size ratio. However, the higher figures allow higher COUNT X and COUNT Y clock rates from the BRMs and consequently the vector is drawn in the shortest possible time.

3.2.10.3 Binary Rate Multipliers – The 7497 Binary Rate Multiplier chips, two for X and two for Y, are shown on drawing A320-BRM. This circuit performs a fixed-rate division of the 5-MHz input clock pulse, VC1 COUNT CLK L. The output of the BRMs is the input clock multiplied by the binary number in the ΔX and ΔY Registers after normalization. At this time the maximum vector magnitude component (1777_8) is unchanged because the MSD already equals 1. However, the smallest magnitude (0001_8) is 1000_8 after normalization. Therefore, within the ΔX and ΔY pair for a single vector the larger (controlling) magnitude component is within the $1777–1000_8$ range after normalization. Consequently, all vectors assert a COUNT X (or COUNT Y, as determined by which is the larger Δ component) at a rate between 2.5 and 5.0 MHz; even very short vectors are drawn at a relatively fast rate, never at less than half the maximum 5 MHz rate. (The smaller Δ component of the vector word can, of course, be $< 1000_8$ after normalization; it does not affect the drawing rate.)

3.2.10.4 Vector Generator Synchronization – The adjusted clock pulses, COUNT X and COUNT Y, from the BRMs are used to synchronize the internal operation of the vector generator. They simultaneously cause additional current to be input to the ramp generator capacitors, increment (or decrement if the data word bit 13 = 1) the X and Y Position Registers (absolute vector length), and decrement the Down Count Register (COUNT X performs this last function if the register was loaded with ΔX data; COUNT Y if loaded with ΔY data). Therefore, the output analog ramp is increased, the Y and X Position Registers are updated to reflect the current beam position, and the remaining count in the Down Count Register becomes less – all in unison, as controlled by the COUNT X and COUNT Y pulses.

Figure 3-25 is a timing diagram for two consecutive vectors. The first has a ΔX = +1000 and a ΔY = +1777. The second has a ΔX = +1000 and a ΔY = −1777. (All figures represent normalized magnitude components.) The COUNT Y clock is the same frequency as the system clock and the COUNT X frequency is one-half the COUNT Y frequency. Thus the X ramp slope is one-half the Y ramp slope. When the Down Count Register = 0 the first vector is concluded. The ramp generator output returns to zero and the DACs are updated from the X and Y Position Registers to hold the now unintensified beam at the point where the vector stopped. The signal VC2 VEC GEN OP DONE H is now asserted signifying the completion of the operation. This signal sets the NPR flip-flop and the data words for the second vector are read from core memory.

The second vector, which has a negative Y ramp, starts at the point where the first vector terminated. Since the magnitude of the two vectors are the same, the second will be the same length as the first. However, it will be drawn in the top to bottom direction. Again, at the conclusion of the vector, the ramp generator returns to zero and the DACs are updated to hold the unintensified beam at the new location. Note that during the first vector both position registers were incremented, but during the second vector the Y Position Register was decremented while the Y Position Register was being incremented.

Three consecutive vectors are shown in Figure 3-26. Vector 3 also shows the result of normalization; although shorter than the first two vectors it is drawn at almost the same rate.

A unique condition exists if both ΔX and ΔY components indicate zero length vectors. If normalization were attempted the logic would be caught in an endless loop. Therefore, the Down Count Register, loaded before normalization, is checked for a zero length vector; if this is indicated the vector instruction is aborted.

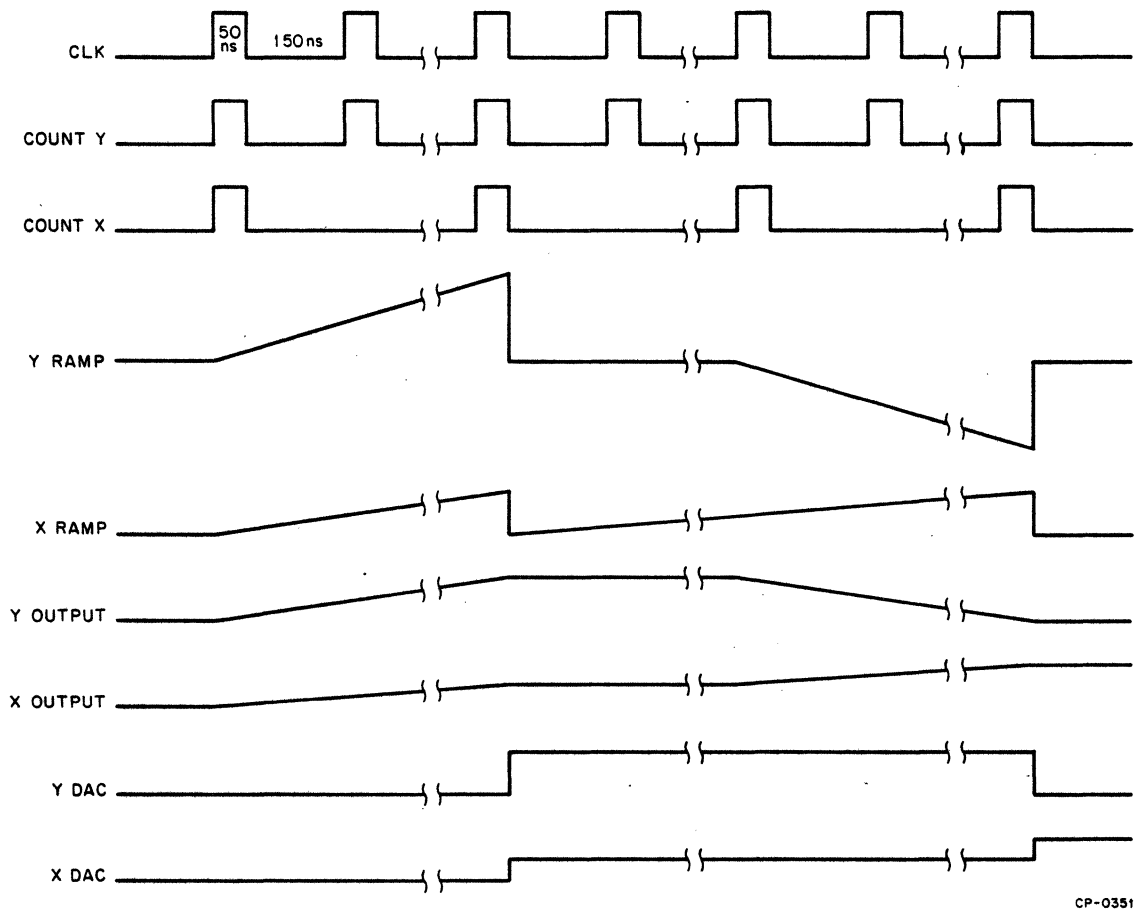


Figure 3-25 Vector Generator, Timing Diagram

3.2.11 Point Intensification

After a Set Graphic Mode instruction has placed the GT40 Display Processor in the graphic mode and loaded the Data Mode Register with the Point code (Paragraph 3.2.8.5) the first of the two Point data words is read from the MM11 Core Memory (Paragraph 3.2.9). At this point the mode decode logic asserts MD POINT H indicating how the present and successive data words on the Unibus are to be treated.

The PVCS Word flip-flop, reset by MD CLR WORD L when the Set Graphic Mode instruction was read, and MD POINT L, assert PVCS POINT WORD 0 H. This signal performs two functions: first, it generates the PVCS LOAD X L signal at TD LOAD PULSE time, and then it sets the NPR flip-flop at TD TP2 time. PVCS LOAD X L loads the 74193 4-bit binary counters of the X Position Register (drawing A320-PR) with the X coordinates from the bus data lines (BDL DB (09:00) L).

The second Point data word is placed on the Unibus in response to the NPR. The PVCS Word flip-flop, which was set on trailing edge of the first data word TP2 pulse, now asserts PVCS LOAD Y L at TD LOAD PULSE time and the Y coordinates are loaded into the Y Position Register. The X and Y Position Registers now contain the two 10-bit position coordinates that will shortly be converted, in the DACs, to an analog voltage for the VR14.

At TP2 time of the second data word the NPR request is inhibited because PVCS POINT WORD 0 H went false when the PVCS Word flip-flop was set. On the trailing edge of TD TP2 H, PVCS POINT + GRAPH GO H goes low

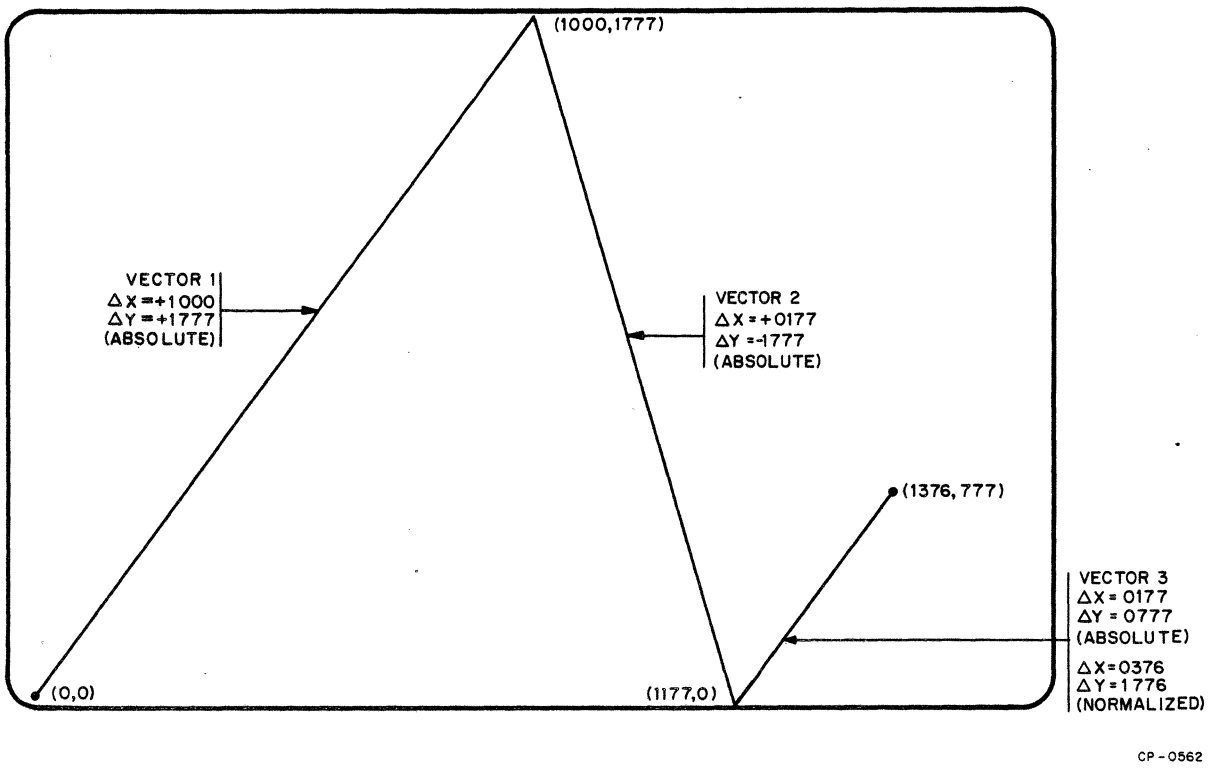


Figure 3-26 Absolute and Normalized Magnitude

(Figure 3-27) to trigger a 74123 Single Shot (drawing M7014-VC2) which asserts VC2 22 μs DELAY H. At the trailing edge of the 800 ns VC1 LOAD DAC H signal asserted by this signal, the data in the X and Y Position Registers is gated into the respective DACs (drawing A320-DAC). The DACs analog outputs are summed in the X and Y summers (drawing A320-CGS), which assert CGS X OUT and CGS Y OUT to the VR14 via the scope cable. These signals are then employed in generating the X and Y deflection voltages to the CRT yokes. About 21 μs after the DACs are loaded and the CRT yokes have had time to settle, the LEI POINT INTENSITY H and LEI Z AXIS H signals are brought up. The latter signal is transmitted to the VR14 as GM INTENSITY OUT L where it causes the CRT cathode to go low and unblank the beam.

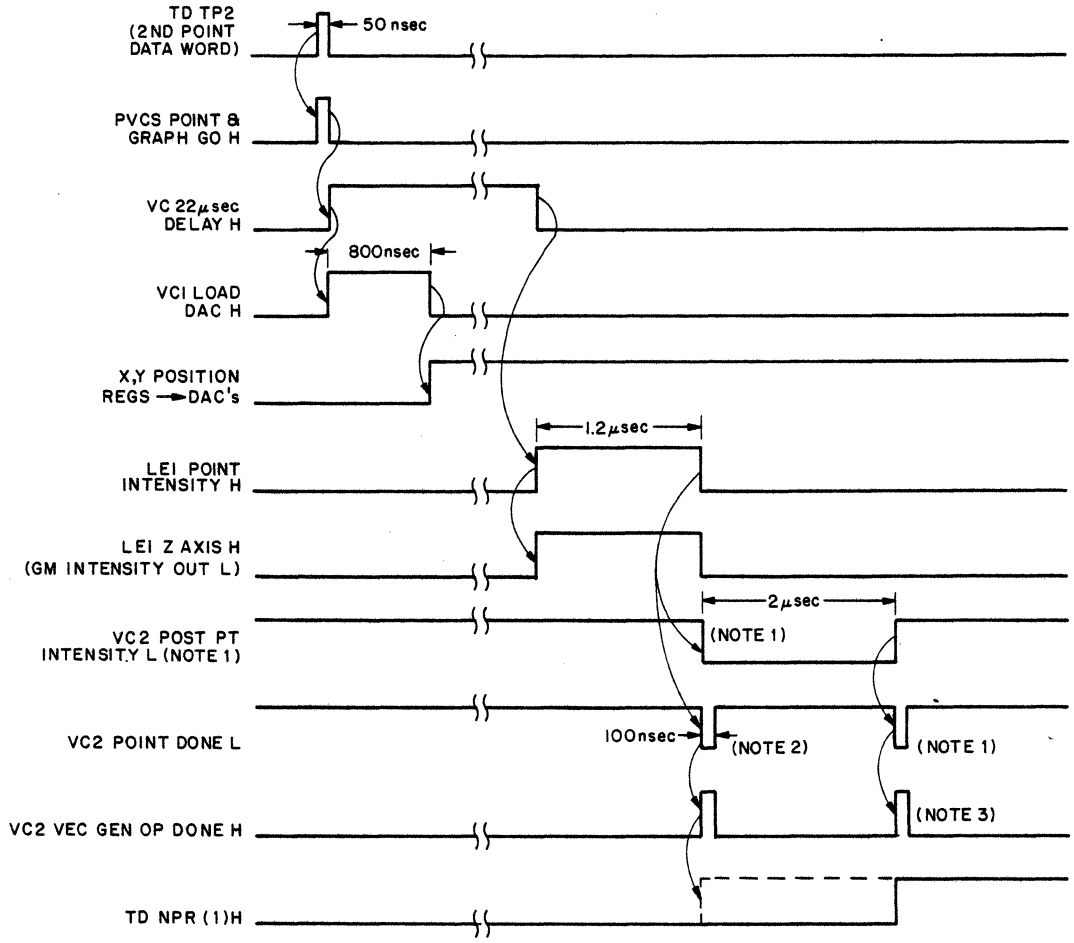
One of two signals is asserted at the trailing edge of the 1.2 μs LEI POINT INTENSITY H signal. If LP interrupts are not allowed (GM LP INTRUP ENA (0) H is high) VC2 POINT DONE L is generated immediately (drawing M7014-VC2). However, if LP interrupts are allowed VC POINT DONE L is delayed an additional 2 μs by a 74123 single shot (VC2 POST PT INTENSITY L, Paragraph 3.2.8.5). In either case, VC2 POINT DONE L asserts VC2 VEC GEN OP DONE H which, in turn, sets the NPR flip-flop and the next word (point data word or control instruction) is read. If there was a LP hit on this point VC2 VEC GEN OP DONE H is inhibited until the LEI PRE LP FLAG flip-flop is reset by ASL CLR FLAGS L.

3.2.12 Character Generation

The 127 different characters and symbols (Appendix C) that can be displayed on the GT40 CRT result from the decoding of character data words in the M7013 module (Paragraph 3.2.9.1 and Figure 3-19).

The character generation logic uses six 256 X 4 ROM chips as the source for character display data. Directed by the M7013 character control circuits, this data develops the X and Y analog deflection signals and the intensity pulses required by the VR14. Similar to vector generation, the character generator uses the same summers in the A320

module to produce the analog voltages that are sent to the X and Y deflection circuits. The output of these circuits then goes to the X and Y CRT yokes to position the beam. The enabling signal to the CRT cathode, GM INTENSITY OUT L, is derived from CCL1 CHAR INTENSITY H which is asserted each time a character dot is to be intensified.



NOTE 1: Asserted if LP INT is enabled.
NOTE 2: Asserted if LP INT is not enabled.
NOTE 3: Inhibit until LEI PRE LP FLAG if there is an LP hit.

CP-0561

Figure 3-27 Point Instruction (Termination), Timing Diagram

All characters are intensified in the manner illustrated in Figure 3-28. The unintensified or blanked beam is pre-positioned near the lower left corner of the character to be displayed (the bottom of column 1) either by a Point instruction, if this is the first character displayed, or after the previous character is completed if several characters are being displayed. The display starts with the beam being moved right and then vertically as a result of the X step and Y ramp to the summers. Dot intensification is determined by the ROM output and control circuits. At the top of the first column the X input to the X summer is stepped again and the Y ramp reverses direction. The beam now sweeps down the second column and the required dots are intensified. This sequence continues until the beam traverses all six columns and then, unintensified, is moved right a predetermined distance in preparation for the start of the next character.

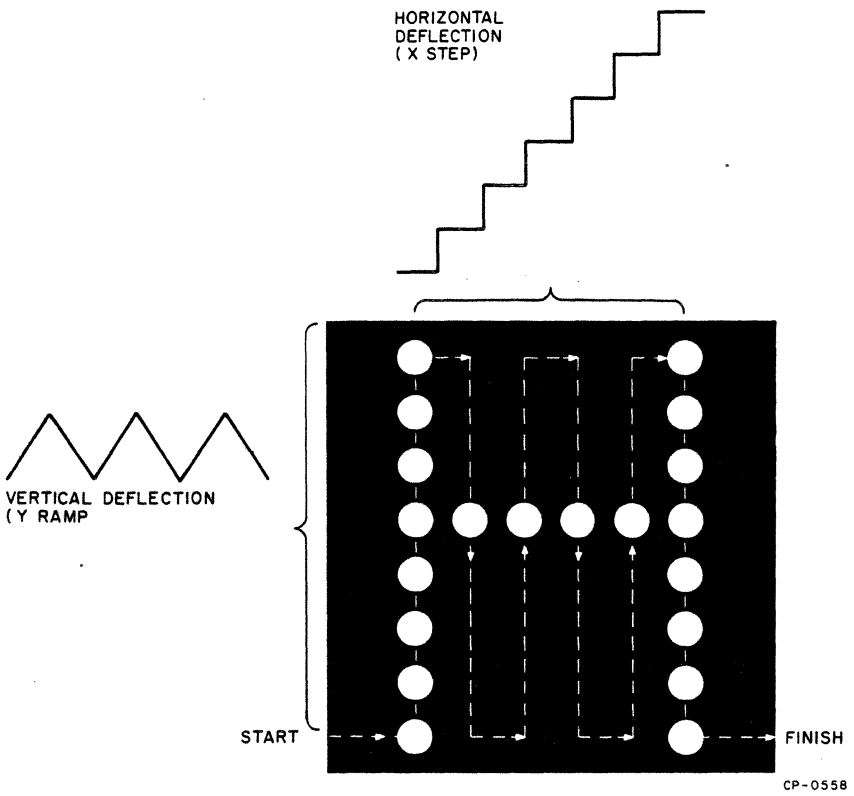


Figure 3-28 Path of Electron Beam as Influenced
By X and Y Deflection Signals

3.2.12.1 General Description – The character generator (Figure 3-29) consists of a bit (Y) counter, a column (X) counter, the ROM, an input character register and word selector, an output shift and intensity circuit, and timing and control circuits. The majority of the logic is shown on drawings M7013-CCL1 and CCL2. Drawing D-FD-GT40-0-14 is a flow diagram for the character generator operation; drawing D-TD-GT40-0-16 is a timing diagram for this circuit. Figure 3-30 is an abbreviated version of the flow diagram.

3.2.12.2 Character Bit Counter and Decoder – The function of this circuit (drawing M7013-CCL2) is to determine the correct time to:

a. load the output shift registers with the column intensity information;

b. trigger the 0.98 to 1.4 μs scope delay single-shot to reverse the Y axis ramp and step the X axis ramp;

c. advance the column counter;

d. reset itself to a decimal count of zero.

The bit counter, following a power clear or when a character is completed, is preset by CCL2 EOC L to a decimal count of 12 to synchronize the X, Y, and Z delays in the VR14 CRT. The scope delay is equal to four times the CCL2 CHAR CLK H period (4 X 4 μs) minus the single-shot delay period (0.98 to 1.4 μs). This variable delay allows the delay period to be adjusted to the particular scope. Nominal setting of the single-shot delay is 1.2 μs. However, the adjustment range allows for scope delays of from 0 to 620 ns.

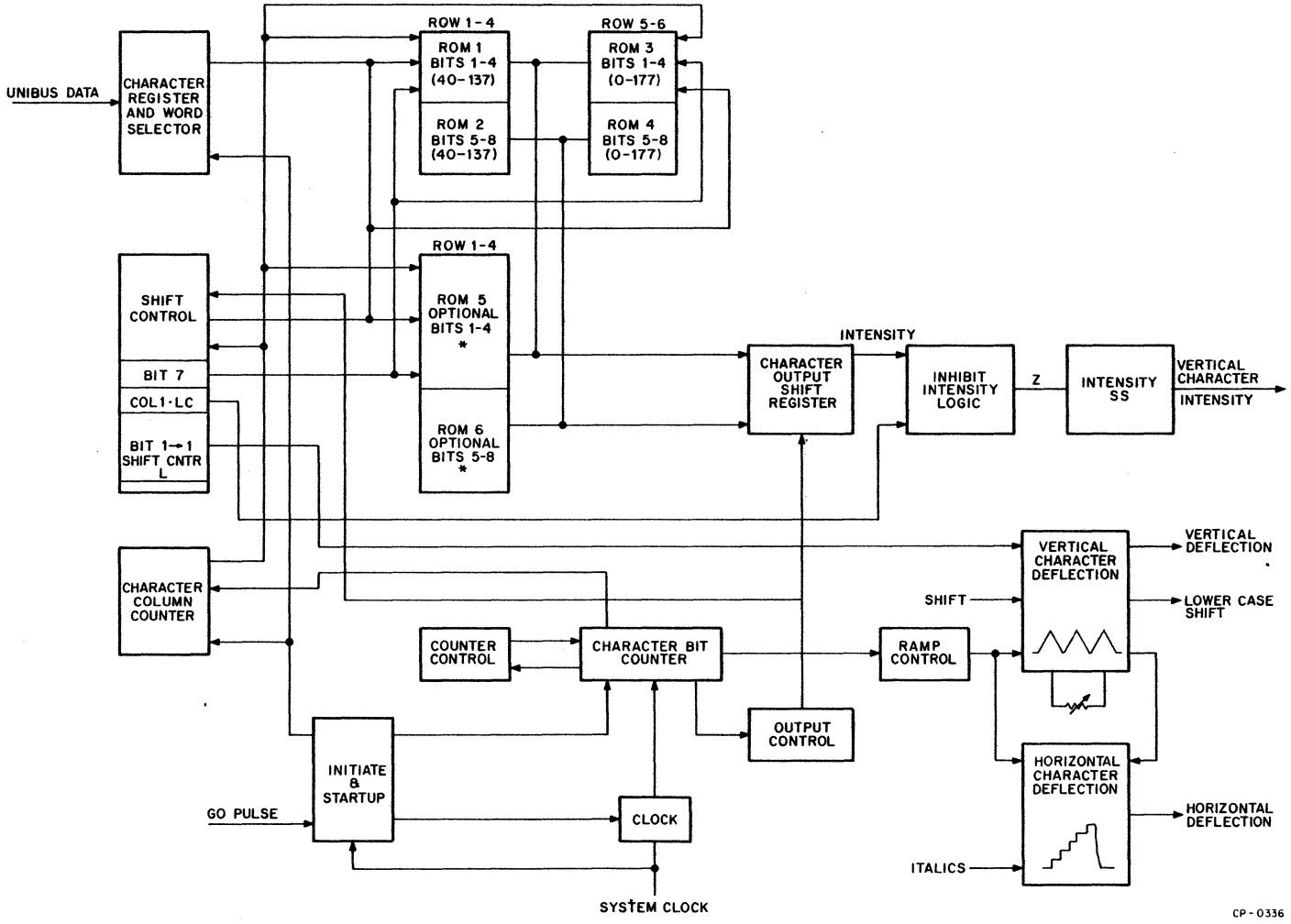


Figure 3-29 Character Generator, Block Diagram

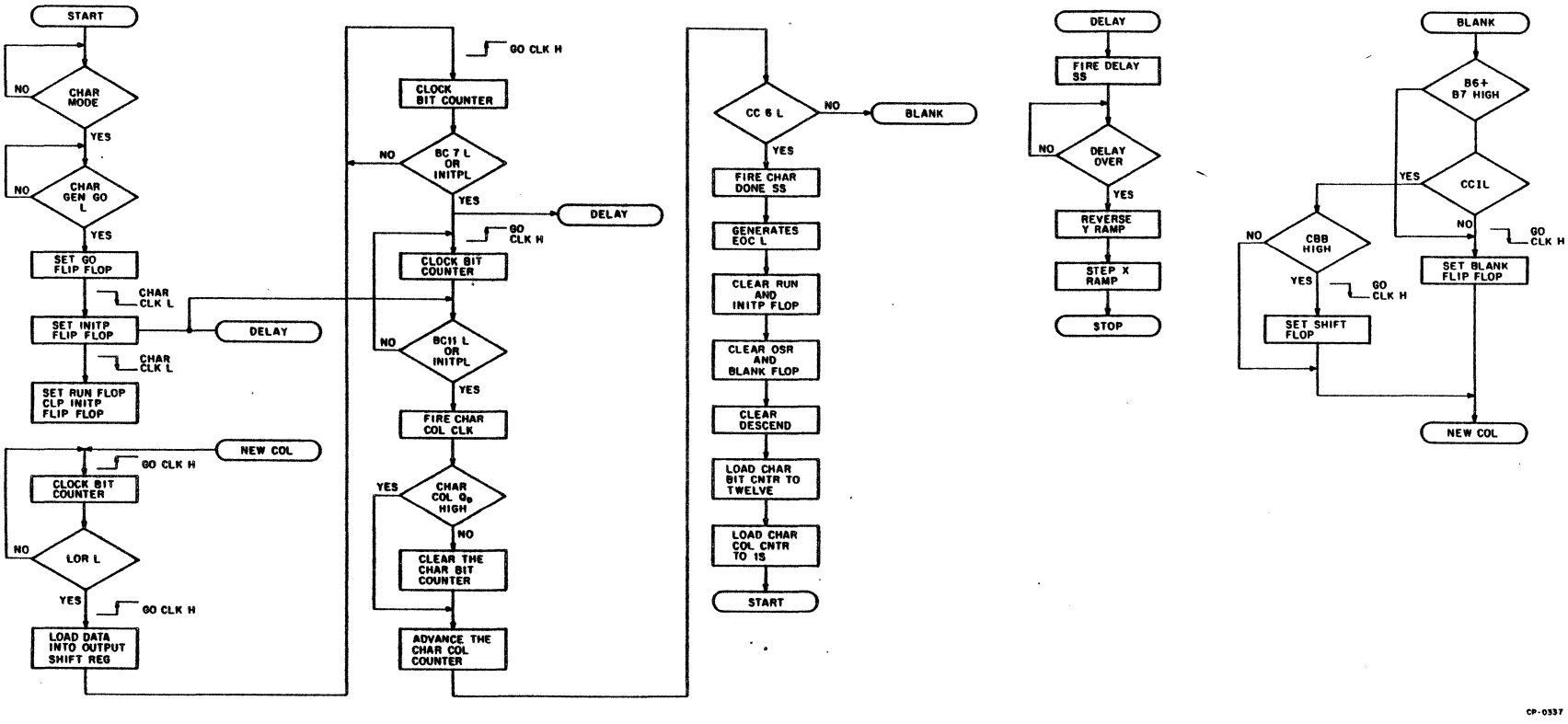


Figure 3-30 Character Generator, Flow Diagram

With the advent of CCL2 GO CLK H pulses after the Run flip-flop has been set, the counter counts from 12 to 15_{10}, overflows naturally to zero, then counts to 10_{10} and resets on the eleventh pulse. This count (0–11) is repeated for each of the six character columns. The final count of 11_{10} is gated with a column count of 6 to assert CCL1 CHAR GEN DONE H, which signifies the completion of the character.

3.2.12.3 Character Column Counter and Decoder – Consisting of a 4-bit synchronous counter and a 4 to 10 line decoder, this circuit (drawing M7013-CCL1) is preset to a count of 15_{10} at the end of each character (and during power initiation) by a CCL2 EOC L pulse. Signals generated during the timed operation are shown in Table 3-9. The counter outputs are used to select which pair of ROMs are read to the Character Output Shift Register. The CCL1 COUNT 4 L signal is low when the Character Column Counter contains a count of 0 through 7. This condition allows the Character Bit Counter to be cleared by CCL2 CLK H when it reaches a count of 11_{10}. (There is no count of 11_{10} during the time the first column is displayed; therefore, the Character Bit Counter cannot be cleared during this period.) The CCL1 CC1 L output from the decoder is used in the shift and unblank circuits described below. CCL1 CC6 L, the last output for each character, asserts CCL1 CHAR GEN DONE H (Paragraph 3.2.12.2).

Table 3-9
Character Column Counter and Decoder

Character Column	Counter Outputs CCL1 COUNT				Asserted Decoder Output
	4L	3L	2L	1L	
(EOC)	H	H	H	H	
1	L	L	L	L	(CCL1 CC1 L)
2	L	L	L	H	(Pin 2-low)
3	L	L	H	L	(Pin 3-low)
4	L	L	H	H	(Pin 4-low)
5	L	H	L	L	(Pin 5-low)
6	L	H	H	L	(CCL1 CC6 L)

3.2.12.4 ROM Organization – The intensity information for the 127 ASCII characters is stored in six 256 X 4 bit ROMs (drawing M7013-CRD). The outputs of these ROMs are of the open-collector type that allow all outputs to be connected in a wired-OR configuration.

Two ROMs are read simultaneously to obtain intensity data for an 8-bit character column. This is repeated for each column until the character is displayed. A total of four ROMs are accessed for any one character. To address the ROMs, the six by eight bit character matrix is divided into blocks that are related to individual ROMs. Figures 3-31 and 3-32 illustrate this division of the ROMs; Table 3-10 lists the contents of all six ROMs. ROM outputs can be verified by using Table 3-10 and Appendix C to determine which two ROMs a character column is associated with and then observing the ROM outputs on an oscilloscope. Synchronize the oscilloscope on the character column decoder output (Table 3-9) corresponding to the column that is being checked. Determine that each bit in that column is correct.

Each of the ROMs used has eight address lines and two chip enable lines. Manipulation of these ten lines produces the organization described above. ROMs 1 and 2 are used for columns 1–4, bits 1–8. Both receive identical address codes. The two chip enables are connected to ASCII bit 7 (CCL1 B7 H) and the CCL1 COUNT 3 L output of the column counter. This means that the chip is only enabled when both are low; this is true during columns 1–4 for these two ROMs. The remaining address lines, beginning with the MSD, are then controlled by ASCII bits 6–1 and the CCL1 COUNT (2:1) L outputs of the column counter. This provides a unique address for each column of intensity data.

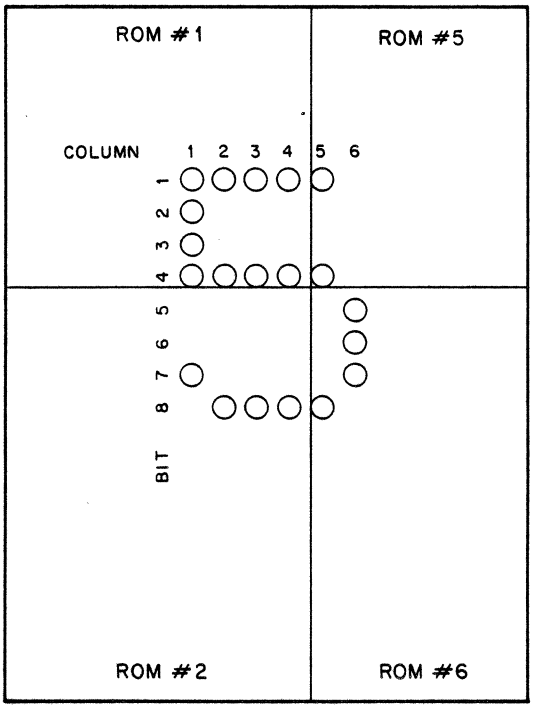


Figure 3-31 ROM/Character Relationship

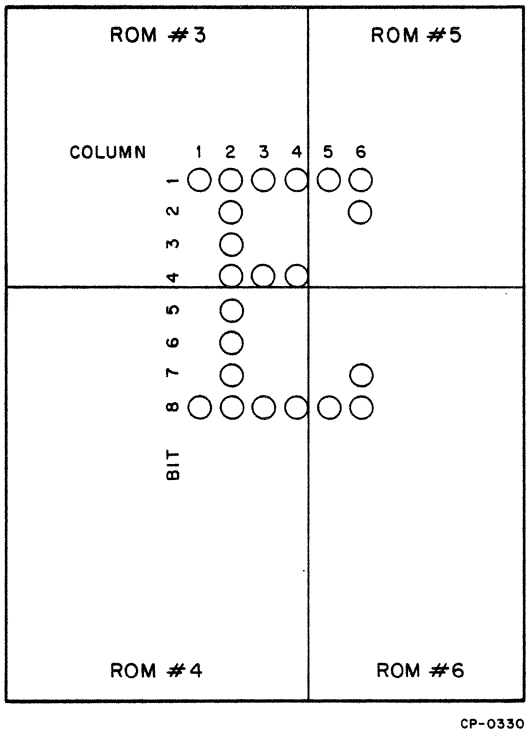


Figure 3-32 ROM/Character Relationship

Table 3-10
Character ROM Contents

ROM	Character Columns	ASCII Bits	ASCII Codes (Octal)
1	1–4	1–4	000–077
2	1–4	5–8	000–077
3	1–4	1–4	100–177
4	1–4	5–8	100–177
5	5–8	1–4	000–177
6	5–6	5–8	000–177

ROMs 3 and 4 are addressed in exactly the same manner as ROMs 1 and 2 except that an inverted ASCII bit 7 (CCL1 B7 L) controls one of the chip enable lines. This results in these two chips being enabled for columns 1–4 of ASCII codes $100–177_8$. ROMs 5 and 6 have both chip enable lines connected to the inverted 2^2 output (CCL1 COUNT 3 H) of the column counter. These two chips are enabled for columns 5 and 6 because CCL1 COUNT 3 H goes low when the count exceeds 4. The address lines are connected, in addition to CCL1 COUNT 1 L, to all seven ASCII bits and therefore decode the full set of codes ($000–177_8$).

3.2.12.5 Intensity Output and Control – This circuit (drawing M7013-CCL1 and Figure 3-33) consists of two type 74194 Shift Registers connected in tandem, a 7473 J-K Mode Control flip-flop, a 74123 Intensity Pulse Single Shot, a 7474 D-type Edge Detector flip-flop, and associated AND and OR gates.

The two bidirectional shift registers form a parallel-to-serial converter for the ROM data. This data is input, one column at a time in parallel format, shifted at the bit clock rate, and output as serial data to the VR14. The operation begins, for each character, when the Character Bit Counter reaches a count of two and the load output register (CCL2 LOR L) signal forces both S0 and S1 mode control lines high (the required configuration for loading the register). The rising edge of the same CCL2 GO CLK H signal that asserted CCL2 LOR L also loads the input from ROM into the shift register.

The Mode Control flip-flop, reset by CCL2 INIT P L at the beginning of each character, is ORed with CCL2 LOR L to control the S0 and S1 control lines. When CCL2 LOR L goes high and the mode control output causes the control lines to assume the shift right configuration, S0 = H and S1 = L. If the first bit (8) to be displayed is a 1, the trailing edge of CCL2 GO CLK L (the reciprocal of the CCL2 GO CLK H pulse that loaded the register) triggers the character intensity single shot. The resultant 350 ns CCL1 CHAR INTENSITY H pulse is sent to the VR14 (as GM INTENSITY OUT L) and the lower-left character dot is intensified. This would be the case, for example, if the character is an "H" as in Figure 3-28. Note that the Unblank flip-flop must be set and the unintensified beam positioned in the visible portion of the CRT (LEI EDGE H) before any serial data can be transmitted.

The shift register is shifted right on the leading edge of the next CCL2 GO CLK H pulse. Bit 7 is now on the output line from the register and is transmitted on the trailing edge of CCL2 GO CLK L. This shift-transmit sequence is repeated for each dot in the first column that is to be intensified (0 bits are shifted but the single shot is not triggered when they are output from the shift register). At the completion of the first column CCL2 CHAR COL CLK L sets the Mode Control flip-flop and advances the Character Column Counter to the second column. The mode control lines are now in the shift-left configuration: S0 = L and S1 = H. The shift is changed from shift-right to shift-left operation because the first column of dots is displayed as the beam moves toward the top of the character and the next column is displayed as the beam moves downward. This alternating between shift-left and shift-right continues until the character is completed, at which time the Unblank flip-flop is reset and further CCL1 CHAR INTENSITY H pulses are inhibited.

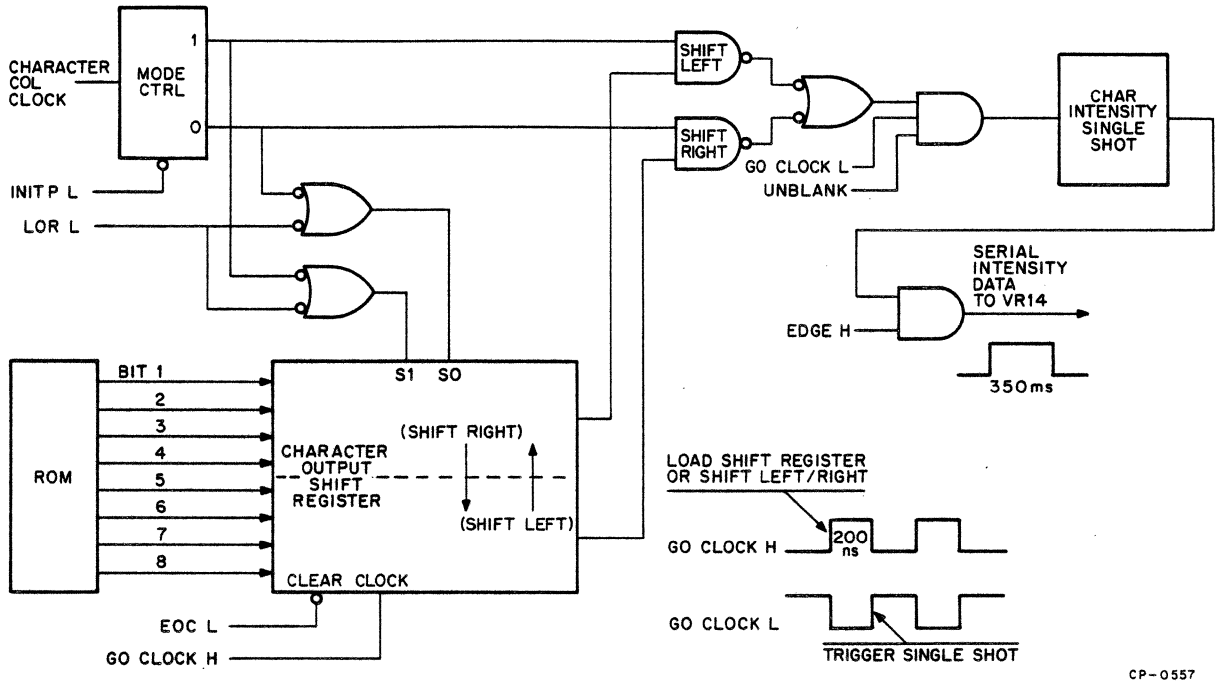


Figure 3-33 Generation of Intensity Data to the VR14

The period of the single shot is adjusted for a duty cycle of 75 percent (350 ns). This provides an intensity pulse that produces maximum character brightness. The use of a single shot also prevents burning of the phosphor in the event of a failure, e.g., clock pulse failure, in the logic prior to that point.

3.2.12.6 Operational Sequence – Character generation begins with the assertion of the end of character (CCL2 EOC L) signal in the M7013 module (drawing M7013-CCL2). This signal, generated at the conclusion of each character display (CCL1 CHAR GEN DONE H) or when power is first brought up (BCL INIT H), performs certain housekeeping functions to ensure that the logic is in the correct state when next character display is started. These functions are listed in Table 3-11.

The character generation logic remains quiescent until the first character data word following a Set Graphic Mode instruction asserts MD CHARACTER L. At TD LOAD PULSE time the two 7-bit characters on the Unibus data lines are clocked into the Character Register (drawing M7013-CCL1). (Succeeding data words are treated identically.) PVCS WORD 1 H is low at this time and therefore the output [CCL1 B (7:1) H] of the Character Word Selector is determined by the contents of the first character on the bus data lines [BDL DB (06:00) H]. The Character Word Selector output provides the memory address for the ROM. Consequently, the intensity information for the first character column (of the first of two characters) is read from the ROM and sent to the Character Output Shift Register at TD LOAD PULSE time of the data word. Accessing ROM is the first event in the display of any character. At the conclusion of the present character display, the Word flip-flop is toggled by VC2 VEC GEN OP DONE H (derived from VC1 DONE L) and the second 7-bit character in the Character Register [DBL DB (14:08) H] furnishes the memory address for the ROM. This switching from one 7-bit input to the other continues as successive character data words are read from core memory (Figure 3-34).

Table 3-11
EOC Signal Functions

Function	Circuit	Remarks
Clear	Run Flip-Flop	Inhibit erroneous displays following power up. BCL INIT P H also clears the Go flip-flop at this time.
	Character Output Shift Register	
	Ramp Y Flip-Flop	The first sweep of the beam will be from the bottom to the top of the first character column.
	Descend Flip-Flop	
	Unblank Flip-Flop	Inhibit display until 1st or 2nd character column.
Preset	Character Bit Counter	$= 12_{10}$
	Character Column Counter	$= 15_{10}$ (Inhibits clearing the bit counter during the first column.)

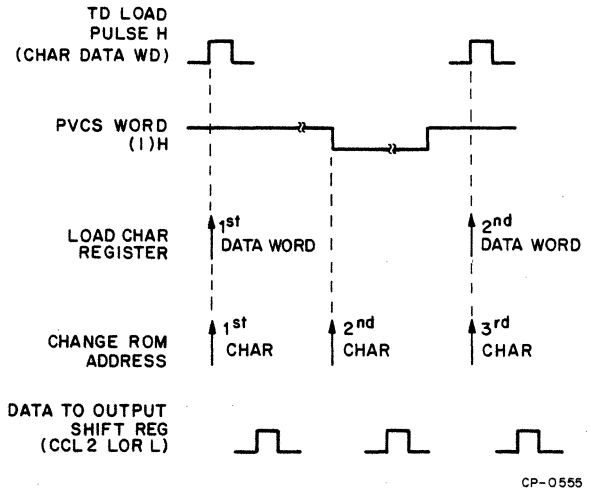


Figure 3-34 Word Selection and ROM Addressing, Timing Diagram

At TD TP2 time of each character data word the signal PVCS CHAR GEN GO H is asserted. Unless a space character is decoded or a control character (codes 000 through 037) is not preceded by Shift Out (CSC SO L), CSC ENABLE PRINT H is asserted and ANDed with PVCS CHAR GEN GO to generate CSC PRINT CHAR L. The leading edge of this signal, which must be asserted before any character can be displayed, sets the Go flip-flop and a synchronization sequence is initiated. Timing for character display is derived from the 5 MHz system clock (PCC DIS CLOCK H) which triggers a J-K flip-flop to assert the 2.5 MHz (400 ns period) signals CCL2 CHAR CLK H and CCL2 CHAR CLK L. The Init P flip-flop is set on the leading edge of the first CCL2 CHAR CLK L pulse after the Go flip-flop is set. This marks the point where the command is synchronized to the character generator clock. CCL2 INIT P L and

CCL2 INIT + INIT P L now clear the Go flip-flop and trigger the 0.98–1.4 μs scope delay (Paragraph 3.2.12.2) and the character clock single shots. The 100 ns CL2 CHAR CLK L signal also steps the Character Column Counter to an all zero output. This causes the Character Column Decoder to assert CCL1 CC1 L (Table 3-9) to denote column one is being displayed.

The Run flip-flop is set and the Init P flip-flop is cleared by the next CCL2 CHAR CLK L signal. CCL2 GO CLK H is now asserted every 400 ns until the Run flip-flop is reset after the last column is displayed. CCL2 GO CLK H pulses, which follow the CCL2 CHAR CLK H pulses, are used to up count the character bit counter; this operation is now started. At a point determined by the setting of the scope delay single shot, the Step single shot is triggered to assert CCL2 STEP X H and the Ramp Y flip-flop is set. The CRT beam is moved (right) to the bottom of the first character column and CCL2 RAMP Y (1) H starts the vertical sweep. The scope delay single shot is adjusted so that this repositioning of the beam coincides with the assertion of CCL2 LOR L; this occurs when the bit counter = 2_{10}. Provided a lower-case character is not decoded (ASCII bits 6 and 7 = 1), the Unblank flip-flop is set on the leading edge if the next CCL2 GO CLK L pulse. On the trailing edge of the same signal the character intensity single shot is triggered if the lower left dot is to be displayed. The beam is now sweeping up and the Character Output Shift Register is shifted right; the display of the first character column is underway.

The Character Bit Counter continues to up count and the CCL1 CHAR INTENSITY H pulses are asserted when a dot is to be displayed. Both of these functions occurs at a rate determined by the CCL2 GO CLK pulses (Figure 3-35). When the bit counter reaches a count of 7, CCL2 DEFL DONE is asserted and the 0.98–1.4 μs scope delay single shot is triggered again in preparation for the second column display. The signal CCL2 CBC11 L, generated when the bit counter reaches a count of 11, triggers a 100-ns single shot to assert CCL2 CHAR COL CLK L and CCL2 CLK H. The Character Bit Counter, cleared by this latter signal, now restarts the 1–11 count sequence.

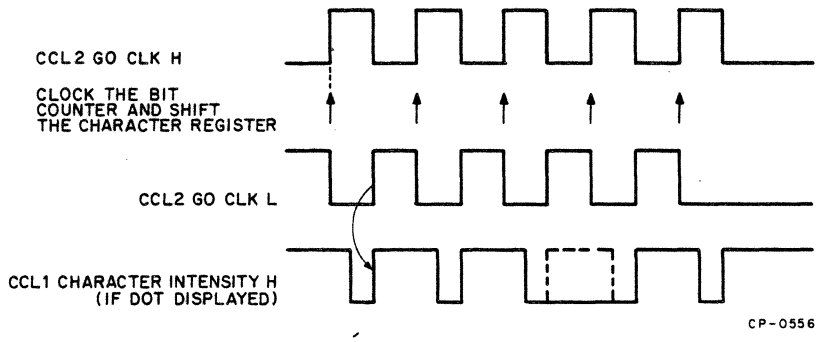


Figure 3-35 Character Bit Timing

The signal CCL2 CHAR COL CLK L up clocks the Character Column Counter to cause the second column intensity data to be read from ROM; at the same time it toggles the Mode Control flip-flop in the character intensity circuit. This results in the Character Output Shift Register performing a shift-left for each dot position (intensified or not) in the second column.

The scope delay times out at approximately the same time that the Character Column Counter is up-clocked. This causes the signal CCL2 STEP X H to be asserted again, moving the beam to the right, and the Ramp Y flip-flop is reset; the downward sweep for the second column is started. The second column intensity pulse stream is generated in the same manner as when the first column was displayed except that it emanates from the opposite end of the Character Output Shift Register because the register is in a shift-left configuration.

At the end of the second column the Character Column Counter is clocked again and the third column display begins. The sequence continues until all six columns have been displayed at which time the seventh CCL1 CHAR

COL CLK L pulse is ANDed with CCL1 CC6 L to assert CCL1 CHAR GEN DONE H (Figure 3-36). The first of two characters contained in the data word has been displayed. A timed sequence now starts. At the termination of this sequence the second character (if present) will be displayed.

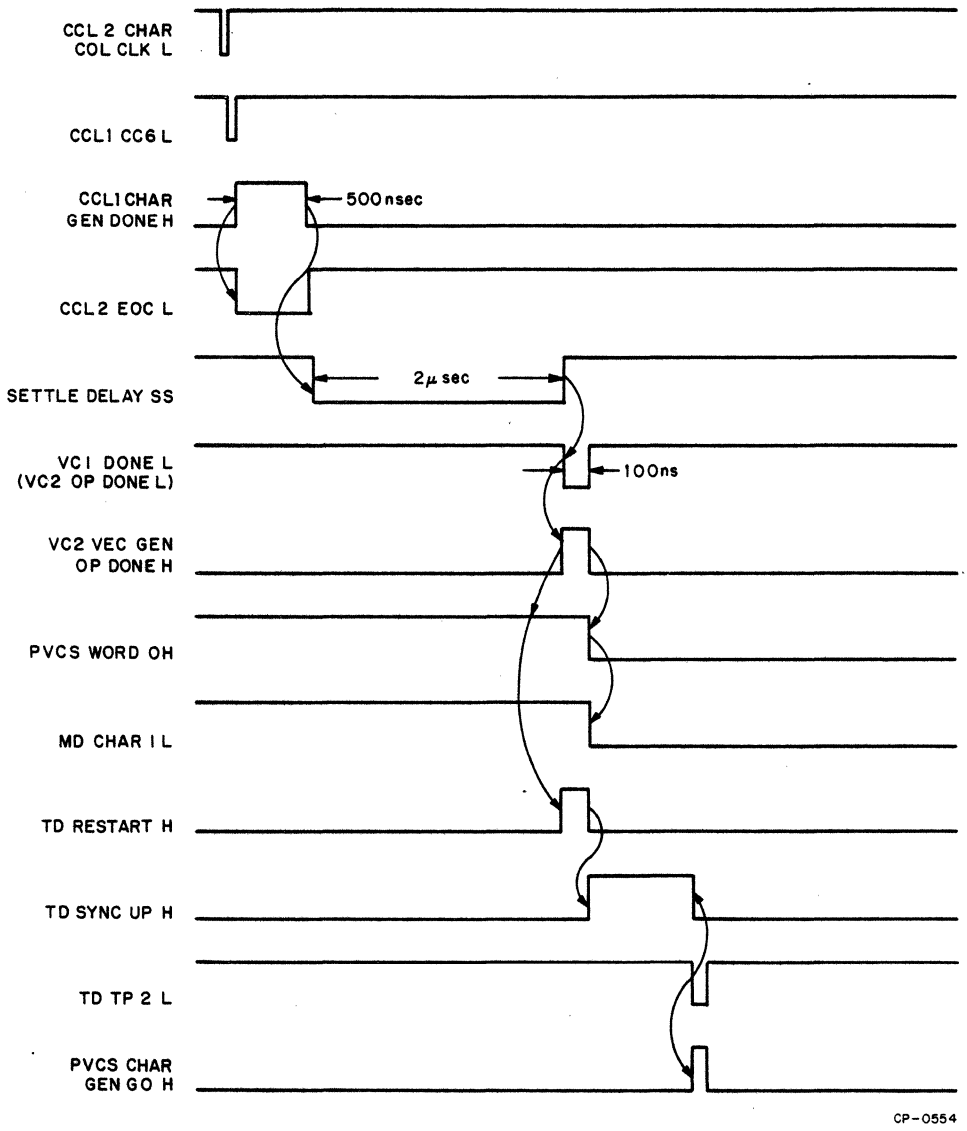


Figure 3-36 Character Timing Between Characters in a Single Data Word

After a 2.5-μs delay to allow time for the yokes to settle, CCL1 CHAR GEN DONE H causes the assertion of a 100 ns signal, TD RESTART H (drawing M7013-TD). This signal is only generated after the display of the first of two characters in a data word when PVCS WORD 0 H is high. The resultant TD SYNCH UP H synchronizes the system clock to the timing pulse generation logic and two, as opposed to the normal four (Paragraph 3.2.6), timing pulses are asserted. This is because TD RESTART L presets the 74193 4-Bit Binary Counter, Time Cnt Up, to a count of two. This causes the 74155, 1–4 line demultiplexer S1 input to be high and the S0 input to be low. Consequently, the next two PCC DIS CLOCK H pulses assert TD TP1 and TD TP2; TD LOAD MODE L and TD LOAD PULSE L are not generated. At TD TP2 L time the signal PVCS CHAR GEN GO H is asserted and display of the second character is initiated with CSC PRINT CHAR L.

When display of the second character is completed the same termination signals are repeated except that TD RESTART H (and subsequent signals) is inhibited. However, the NPR flip-flop is set by VC2 GEN OP DONE H because MD CHAR WORD 1 L went low after the first character was isplayed. The NPR will cause the next character data word to be read from core memory if additional characters are to be displayed.

3.2.12.7 Character Spacing – After each character is displayed the unintensified CRT beam is positioned near the bottom of column 1 of the next character (Paragraph 3.2.12). This intercharacter positioning sequence begins at TD TP2 time of each character when PVCS CHAR GEN GO L is asserted (Figure 3-37). This signal actuates the Time Shift Register (drawing M7014-VC1), which outputs a pair of timed pulses (VC1 TIME 1 H and VC1 TIME 2 H, Figure 3-38) and loads the Down Count Register (VC1 LOAD DOWN COUNT L) with a character space constant that represents the distance the beam is to be moved in X direction.

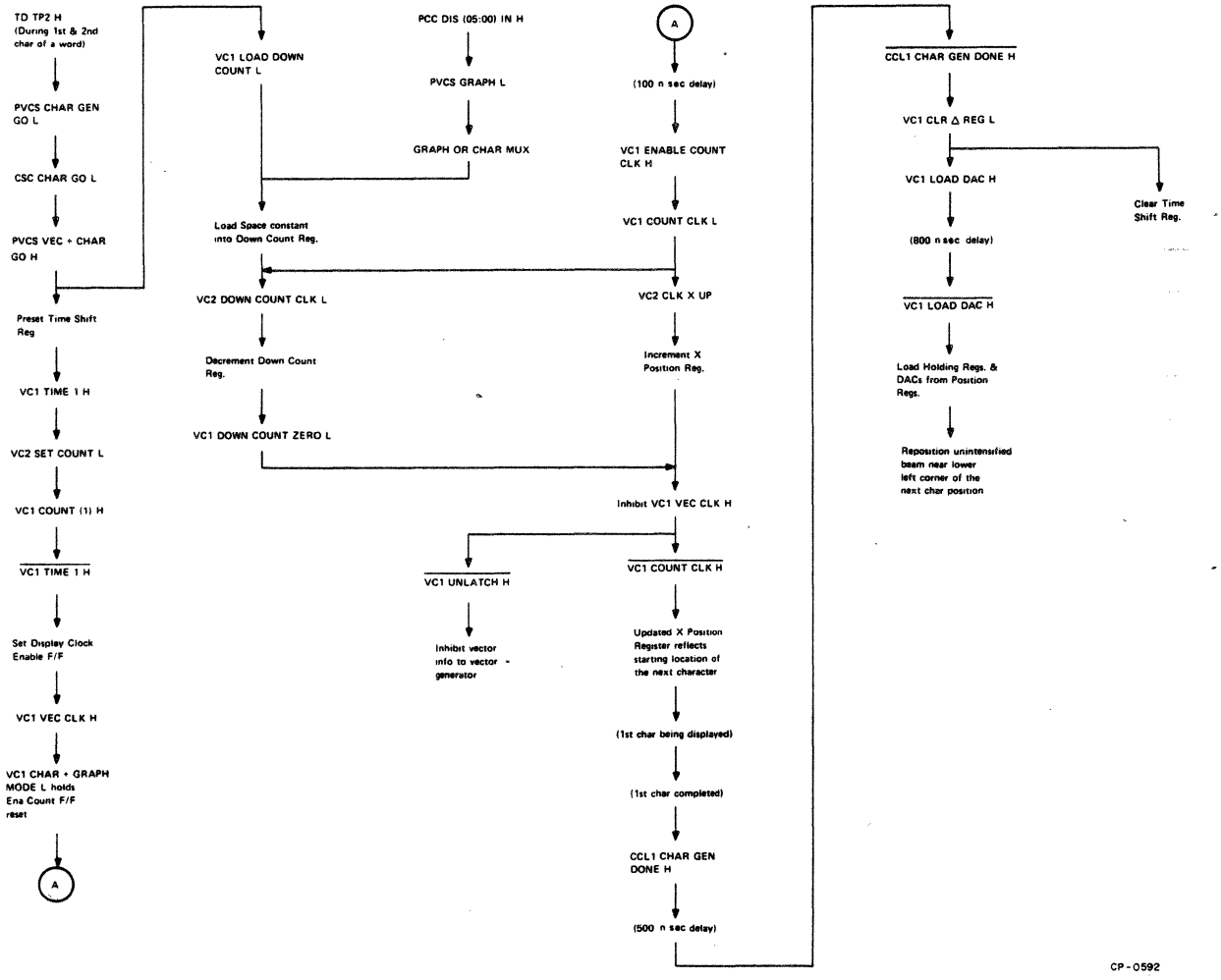


Figure 3-37 Intercharacter X Position Update, Flow Diagram

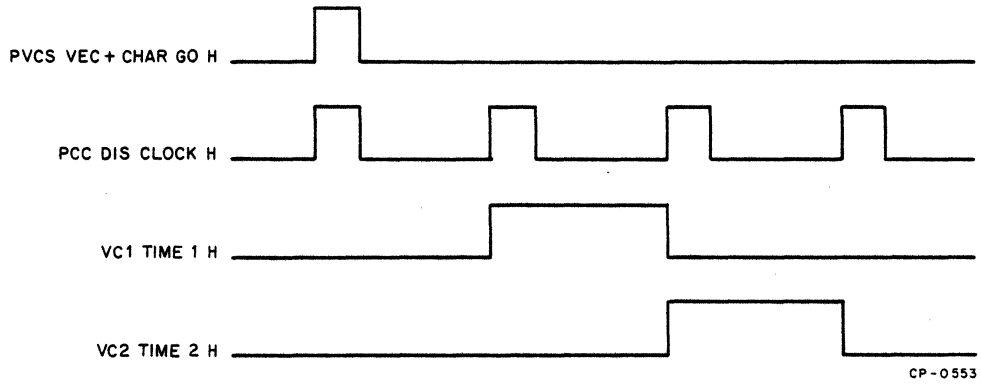


Figure 3-38 Time Shift Register, Timing Diagram (M7014-VC1)

The constant (always a 14 or 16_8 unless LF or CR are specified) is derived from the character spacing logic (drawing M7014-PCC). Table 3-12 shows the output of this circuit as determined by the jumper configuration (W3, W4, W5, and W6) on the M7014 module.

Table 3-12
Character Spacing Jumpers

Jumper In Place	Characters/Row	Rows	Asserted Output* PCC			
			4 IN H	3 IN H	2 IN H	1 IN H
W3	86	30	L	H	H	L
W4	72	30	L	H	H	H
W5	72	32	L	H	H	H
W6	86	32	L	H	H	L

*Unless CR or LF are asserted.

The space constant is loaded into the Down Count Register via the Graph or Character Multiplexer (drawing A320-DCR and Figure 3-12) because PVCS GRAPH L is high. After a delay, VC1 COUNT CLK L simultaneously increments the X Position Register contents and decrements the constant in the Down Count Register. This takes place at the 5-MHz system clock rate. When VC1 DOWN COUNT ZERO L is asserted (the count = 0) VC1 VEC CLK H goes low and incrementing of the X Position Register halts. This register now contains the X component of the starting location of the next character. No further action occurs in this operation until the conclusion of the character display when CCL2 EOC L is asserted. This signal ensures that the Y ramp is returned to the starting point and, unless LF is asserted, the Y Position Register remains unchanged. 500 ns later the trailing edge of CCL1 CHAR GEN DONE H asserts the 800 ns VC1 LOAD DAC H. (The 2 μs settle delay, whose function was previously mentioned, is also triggered at this time.) The holding registers and DACs are then loaded from the X and Y Position Registers on the trailing edge of VC1 LOAD DAC H. Since this occurs approximately 1.2 μs before VC2 VEC GEN OP DONE L is asserted, the CRT yokes have sufficient time to settle before TD RESTART H is asserted or an NPR is issued.

3.2.12.8 Descending Characters – The Descend flip-flop and the gating necessary to detect a descending lower case character, i.e., j, g, p, q, and y, constitute the digital portion of the descend control (drawing M7013-CCL2). ASCII bits 6 and 7 (CCL1 B6 H and CCL1 B7 H) are examined during character column 1 (CCL1 CC1 L) to determine if a

lower case character is to be printed and then the ROM output is tested (CRD CB 8 H) for a descending character. If all conditions are met, the Descend flip-flop is set on the trailing edge of the first CCL2 GO CLK H pulse. That portion of the descend circuit on the analog module (drawing A320-CSG) consists of a resistor and a diode that form a voltage divider. The voltage at their juncture provides one of the inputs to the Y summer. When a descending character is detected [CCL2 Descend (0) H goes low] the output of the 7417 Buffer forces this point to ground and effectively shifts the vertical position of that character downward by the correct amount.

The method employed to detect a descending lower case character necessitates blanking (deleting) the intensity information contained in the first column of these characters. There are two reasons for this. First, as shown in Figure 3-39, there is an inherent "descend dot" at the lower-left corner (bottom of column 1) of all descending characters that must be blanked; second, during the time normally used to display the first column the Y yoke is shifted for descending characters and needs time to assume the modified starting position before the display begins. The first column of all lower case characters is therefore blanked in order that they be displayed uniformly.

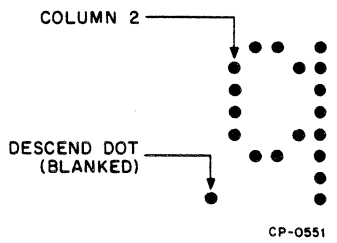


Figure 3-39 Descending Character (EX: Lower Case Q)

3.2.12.9 Y Axis Ramp Generator – This circuit (drawing A320-CGS) consists of a positive and negative current source, an LM302 Buffer, and a zero volt clamp. The positive source is turned on and off by the CCL2 RAMP Y (1) H signal generated in the logic. The negative source provides one-half the current of the positive source and is adjustable to provide for tolerance variation in the circuits, most notably the 5 percent Zener diodes. Figures 3-40 and 3-41 are simplified schematics of the positive and negative sources, respectively. In the positive current source, Zener diode D3, R3 and C1 form a voltage divider and establish the operating potential on the base of Q1. D3 is a 5.6V, ±5% Zener and essentially establishes the current through R4 since the emitter-base drop of Q1 nearly equals the forward voltage drop across D2. D2 provides temperature stabilization to offset changes occurring in Q_1's V_{BE} due to temperature variations. The current through R4 then becomes V_Z/R_{R4}, or approximately 2.06 mA. This current, ±6%, is then the collector current for Q1 (actually I_c = alpha x I_E).

Source switching is accomplished by means of R1, R2, D1, and the SN7417 Open-Collector Buffer. When the output transistor of the buffer is turned on, the collector goes to 0.4V and forces the junction of R1, R2, and D1 to approximately 6V. D1 is now forward biased and places the emitter of Q_1 at approximately 6.6V. This turns Q1 off since the base emitter junction is now reverse biased with the base setting at approximately 8.8V. When the output transistor of the SN7417 turns off, the junction of R1, R2, and D1 rises at an exponential rate toward +15V. D1 will again become reverse biased allowing Q1 to turn on and deliver current to the capacitor. The rise time of the signal on the output of the buffer is less than 100 ns, even with the addition of the scope probe capacitance (less than 13 pF). The fall time is much less since the point is actively pulled down by the buffer, less than 20 ns. R5, D4, and D5 form a clamp that prevents the voltage on the capacitor from going more negative than 0V. 0V was chosen as the clamp point for two reasons. First, no offset would be introduced into the summing amplifier due to the character generator signal. Second, the LM302 Buffer is capable of delivering more current when operating between 0V and +15V than when it operates in the negative region. This allows the use of smaller resistors in the voltage divider following the buffer and minimizes the resistance change due to the italics switch. This resistance change had to be minimized to reduce as much as possible the gain change when the character display alternates between italicized and normal type.

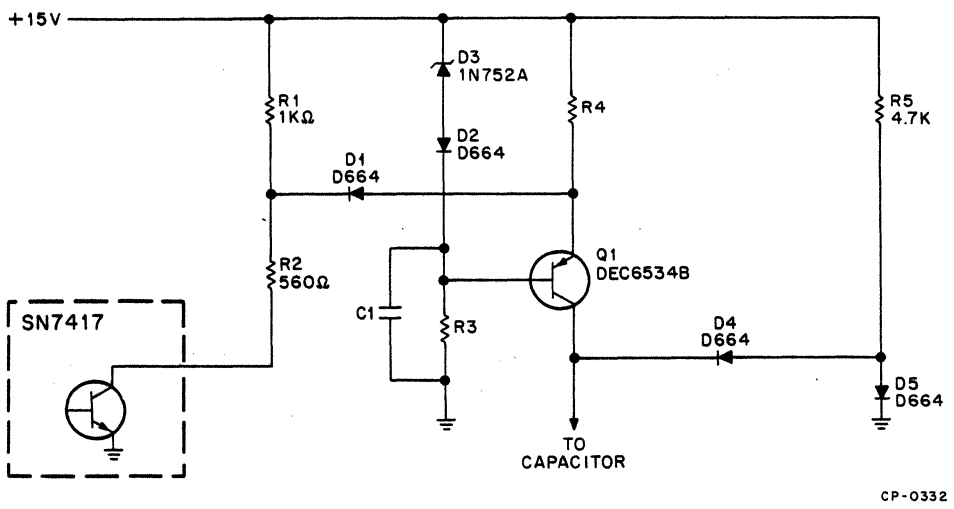


Figure 3-40 Positive Current Source

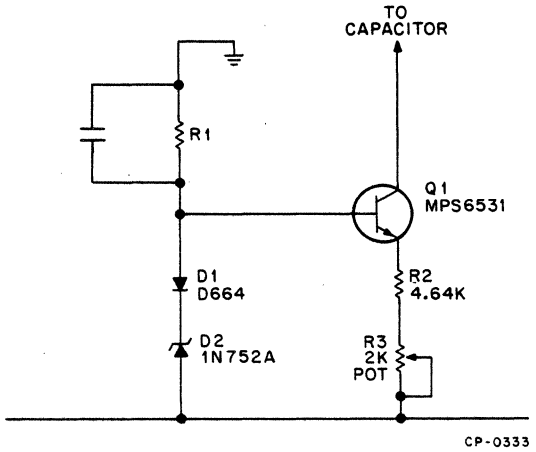


Figure 3-41 Negative Current Source

The negative current source, Figure 3-41, remains on at all times and supplies one-half the current of the positive source. When no character is being printed, the positive source is off and the negative source is on.

The ramp capacitor is discharged until the clamp activates and delivers the 1.04 mA necessary to keep the capacitor at 0V. When character writing begins, the positive source turns on and delivers 2.08 mA of current to the capacitor. Half of this goes to the negative source, while the remaining half deposits a charge on the capacitor. The charge rate may be determined from the formula $\Delta e/\Delta t = I/C$ and is about 1.04V/μs. The negative source is identical to the positive source except for polarities and values. R3 is necessary to allow for Zener tolerance and provides approximately +12 percent adjustment of the negative current from the nominal value.

An LM302, Figure 3-42, buffers the voltage appearing on the capacitors in the X axis and Y axis ramp generators. The 15K resistor, used in series with the input, protects the buffer should a short circuit condition exist on its output. The output signal is reduced in amplitude by a voltage divider and summed with other signals in the summing amplifier. The gain of the summing amplifier with respect to the character generator signal is approximately unity.

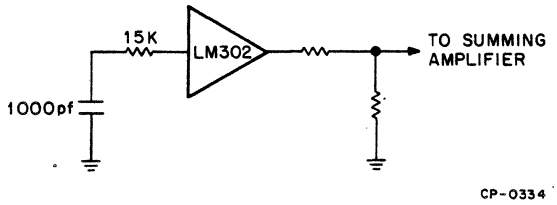


Figure 3-42 LM302 Diagram

3.2.12.10 X Axis Ramp Generator – The X axis ramp generator is identical to the positive source for the Y axis ramp generator. The input to it is a 200-ns positive pulse, CCL2 STEP X H, each time a new character column is to be displayed. This produces a stair-step voltage on the capacitor rather than a ramp as in the Y axis. At the completion of each character, the logic signal, CCL2 RUN (0) H, goes high turning on the transistor switch across the capacitor and discharging it to ground.

3.2.12.11 Italics Switch – The italics control consists of two transistors, four resistors, and three diodes (Figure 3-43). R45, D23, D24, and D25 form a voltage divider that biases the emitter of Q17 at 1.8V and allows the transistor to operate from a TTL level output. A logic 1 on the base of Q17 turns it off since the emitter is at 1.8V. With Q17 off, no base current is supplied to Q16 and it is also turned off. R45 serves to bypass some of the current supplied by Q17 so that a smaller stored charge is produced thus enabling Q2 to turn off more quickly. With Q16 off, the Y axis deflection is summed with the X axis deflection and sent to the X summing amplifier. This action produces the italics effect. A low level on the italics input turns both Q16 and Q17 on and grounds the Y axis deflection at the junction of R42 and R43. Figure 3-43 also shows the waveforms that appear at various points in the circuit.

3.2.13 Analog Circuits

3.2.13.1 General Description – The digital quantities generated in the GT40 Display Processor must be converted to a corresponding analog value for the VR14 CRT Display to perform its required function. This operation is termed digital-to-analog (D/A) conversion. There are several factors consistent with all D/A conversion methods:

- The conversion must be performed as a bit parallel operation because at a given instant the analog equivalent of a binary number available at the same instant must be produced.
- Conversion always produces an analog voltage or analog current that is the equivalent of the digital input.
- The basic method of conversion is to produce for each 1 bit a voltage (or current) magnitude that is a function of the proportional weight of that bit and then add the several voltages (currents) to produce a summed analog output.

The GT40 A320 module analog circuit uses two LM318 Current Summers (Figure 3-44) to produce the required analog voltages to the VR14. The inputs to the summers are the X and Y DACs, vector generators, and character generators, and the descend circuit. These circuits, with the exception of the descend and character analog circuits (Paragraphs 3.2.12.8 through 3.2.12.11) are described in the following paragraphs.

3.2.13.2 Voltage Regulators – This circuit provides the regulated +15 and -15V power for the analog circuits (Figure 3-44 and drawing A320-VR). Another output, VR INTENSITY ENA H, indicating a power-up condition, is ANDed with the intensity signal (LEI Z AXIS H) to assert GM INTENSITY OUT L. This signal turns on the CRT to intensify the beam.

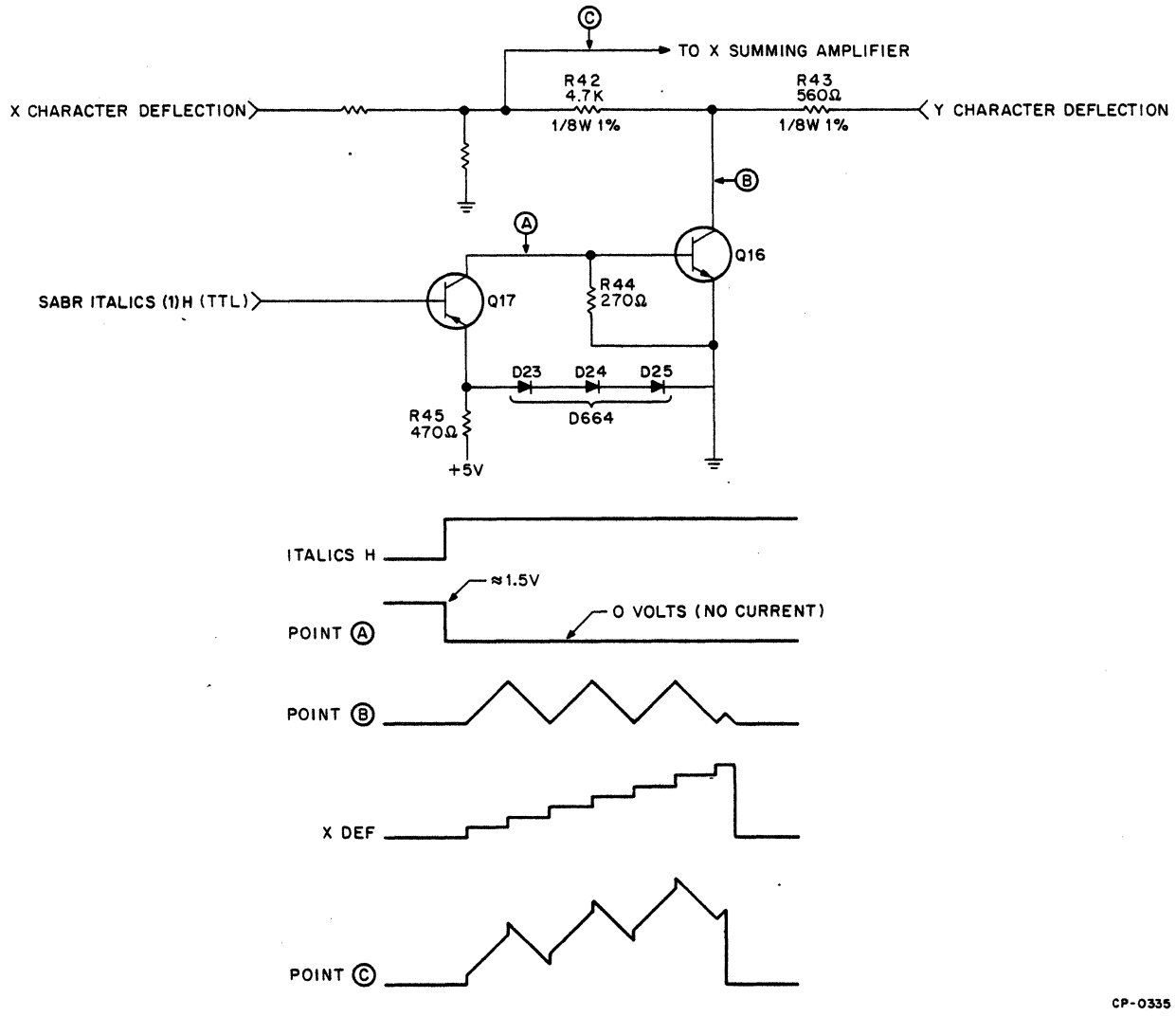


Figure 3-43 Italics Control Circuit

Input power to the regulators is MC + 22 V RAW and MC - 22 V RAW that originates in the VR14 and is delivered to the A320 module via the scope cable.

Operation of the +15 Vdc regulator is described below. The -15 Vdc regulator is functionally identical to the +15 Vdc regulator.

A Zener reference, formed by R52 and D28, is applied by R53 to the noninverting terminal of amplifier E2. The output of E2 is buffered by R57 from the current booster transistors Q18 and Q20. The output of Q20 is fed back, through current sense resistors R60 and R156, to the inverting terminal of E2. The feedback signal is attenuated by R61 and R62.

The output voltage will be: $V_z\ (1 + \frac{R61}{R62})$ or approximately +15 Vdc. Current limiting of the +15 Vdc regulator occurs whenever the voltage developed by R60 exceeds the base to emitter turn on voltage (V_{BEon}) of Q21. Once Q21 begins to conduct, it limits the base drive to Q18 the current booster transistor. Current limiting occurs when the output current exceeds 500 mA. A normally reversed biased diode (D7) is in parallel with the +15 Vdc regulator. In the event the +15 Vdc output is connected to a current limited negative voltage, D7 holds the regulator to the current limit and the output at a point just below ground (ground less the voltage drop across D7).

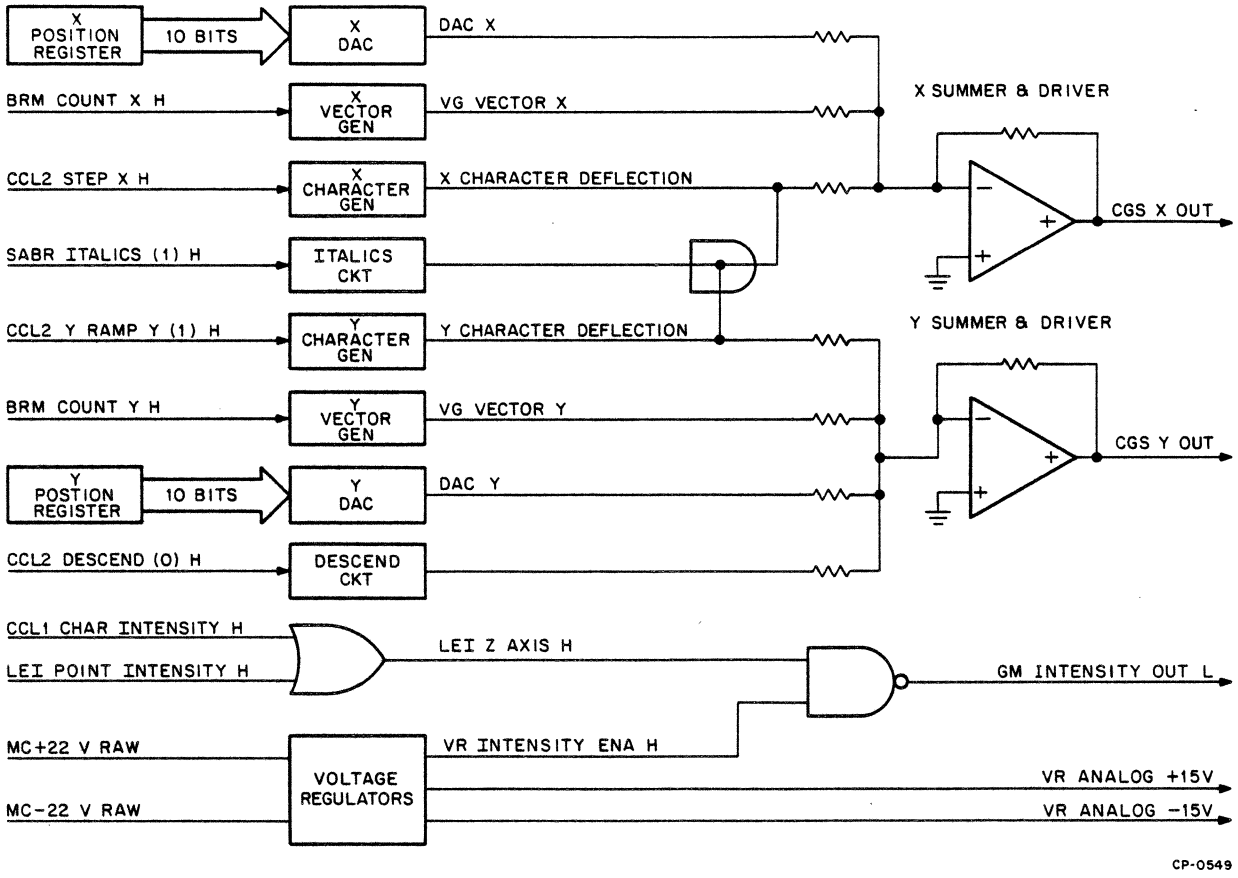


Figure 3-44 Analog Circuit, Block Diagram

The outputs of the 15V regulators are connected by jumpers to the remaining circuitry on the A320. This allows for external power supply connections, requirements are: +15 Vdc ± 1% @ 500 mA, and -15 Vdc ± 1% @ 500 mA.

3.2.13.3 Digital-to-Analog Converters (DAC) – The DACs used in the A320 module analog circuit employ current summing ladder networks similar in operation to the X and Y summers (Paragraph 3.2.13.5). A typical 4-bit ladder is shown in Figure 3-45. The resistor values associated with each input bit produce binary-weighted currents.

The summing function characteristics are:

$$VO = IO \times R$$

where IO is the sum of all the currents through R1, R2, R3, and R4. Thus, if none of the switches are closed, representing a 0000 digital input, VO is 0V. When all the switches are closed, representing a 1111 digital input, VO approaches the reference supply voltage. Assume that SW1 represents the MSB of the digital input register, the reference supply voltage is 10V, and the digital input is 1000. As a result, SW1 is closed and the current flow through R1 is 10/2R. With no other switches closed, this is the total current through R. Therefore, the output voltage is:

$$VO = \frac{10V}{2R} \times R = \frac{10V}{2} = 5V$$

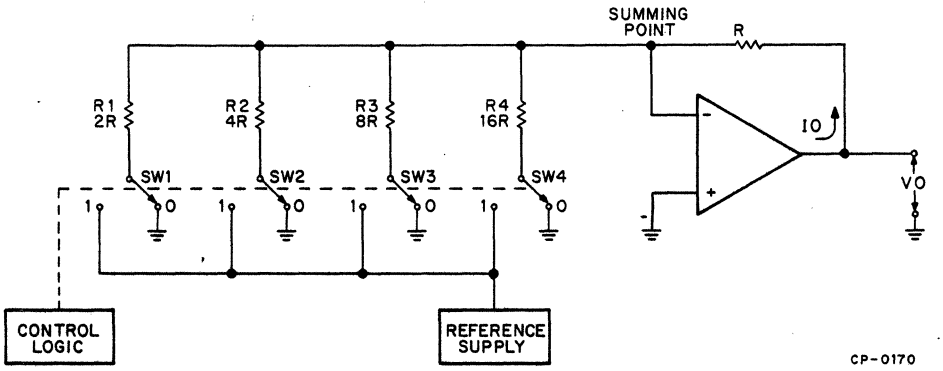


Figure 3-45 Typical Current Summing Ladder

As a second example of the digital-to-analog conversion, assume that the digital input is 0101, causing switches SW2 and SW4 to close. Current through R2 is 10/4R and current through R4 is 10/16R. As a result, the output voltage is:

$$VO = \frac{10V}{4R} \times R + \frac{10V}{16R} \times R = 2.5V + 0.625V = 3.125V$$

The following DAC conversion table lists the 16 possible outputs that can be generated from a 4-bit input.

Digital Input	Analog Output V	Digital Input	Analog Output V
0000	0.0	1000	5.1
0001	0.625	1001	5.625
0010	1.25	1010	6.125
0011	1.875	1011	6.75
0100	2.5	1100	7.5
0101	3.125	1101	8.125
0110	3.75	1110	8.75
0111	4.375	1111	9.375

To have good conversion accuracy, resistor values must be precise and the reference voltage supply must be well regulated.

The two DACs in the GT40 Display Processor generate a voltage (current) reflecting an absolute CRT position that is summed with the vector or character generator output. The type A6000 DACs used have a 12-bit input. However, in this application, they operate as 10-bit input circuits because the two least significant bits (pins 21 and 22) are connected to ground and therefore turned off. Operation is in the bipolar mode because offset pins 1 and 2 are connected together. The 10-bit inputs (from the X and Y Position Registers) exercise the DACs from + full output (+0.5 Vdc) to - full output (-0.5). These outputs are buffered by type LM310 Voltage Followers and then applied to the X and Y summing amplifiers.

Specifications for the A6000 are listed in Table 3-13.

Table 3-13
Type A6000 DAC Specifications (GT40 Configuration)

Specification	Parameter
Current Output	±0.5 mA (offset binary)
Resolution	10 bits
Linearity	±1/2 LSB
Voltage Accuracy	±1/2 LSB (0.0122% of FSR)*
Zero Offset	±1/4 LSB
Impedance	1k (nominal)
Settling Time (to within 1/2 LSB for FS Step)	750 ns for 10 bits
Power Supply Sensitivity	0.005% of FSR/1% change in either supply
Temperature Coefficient	±25 ppm/°C max of FSR
Inputs	1 = +2.75 to +5.5 Vdc @ 50 mA max (current into DAC) 0 = 0.0 to +0.6 Vdc @ 0.8 mA max (current out of DAC)
DC Power	+15 Vdc ± 1% @ 35 mA max -15 Vdc @ 25 mA max
Operating Temperature	+10 to +50°C ambient
Coding (Offset binary) MSB LSB 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	 +0.5 Vdc 0 Vdc (0 mA) -0.5 Vdc

*FSR – Full Scale Resolution.

NOTE

Care should be exercised in maintaining the +15 Vdc supply at the correct level. This supply should not be operated lower than 1 percent below its nominal value, i.e., +14.85 Vdc, to prevent the current switches from saturating. The input logic levels are a function of the +15 Vdc supply. The worst-case low logic level varies with the +15 Vdc supply as follows: maximum logic 0 voltage = 0.75V + (V^+ -15V). Likewise the worst-case high logic level also varies with the +15 Vdc supply: minimum logic 1 voltage = 2.55V + (V^+ -15V).

3.2.13.4 **X and Y Vector Deflection Generators** – This portion of the analog circuit (drawing A320-VG) provides the X and Y ramps necessary to draw a vector on the CRT (Paragraph 3.2.10). Inputs to the vector generators are the BRM COUNT X H and BRM COUNT Y H pulses that are asserted until the Down Count Register = 0 (VC1 DOWN COUNT ZERO L) and PCC ANALOG CLOCK H which is derived from the system clock.

The X and Y circuits operate identically; only the X Vector Generator is described in the following paragraphs.

PCC ANALOG CLOCK H, a 10-MHz clock, is applied to the toggle input of a JK flip-flop, E48. The J input and Q output of E48 are connected to a D flip-flop, E49, in such a fashion as to produce two clocked toggles of E48 following a preset of E49. (If the vector goes beyond the digital edge of the CRT flip-flop, E48 is held clear to prevent unnecessary analog movement outside the screen area.) When E49 is preset by a 50-ns BRM COUNT X pulse, the next two clock pulses generate a 100-ns output pulse. The 100-ns pulse is applied to an inverter E42. The output of E42 drives the base of Q1. The emitter of Q1 is returned to ground through R11. R12 and R13 form a voltage divider that biases Q1's emitter via D3. When the base voltage of Q1 exceeds its emitter bias by the base to emitter turn on voltage, Q1 turns on and reverse biases D3. The magnitude of Q1's emitter current is $(V_{BASE} - V_{BEon})/R11$. D1 and D2 clamp Q1's collector voltage two diode drops below the Zener voltage developed by D44 and its bias resistor R152. Q1 operates in its active region when turned on. The on voltage of D1 cuts off Q2, reverse biasing Q2's base to emitter junction. When A1 is turned on and Q2 cut off the voltage across R5 is $(V_Z - V_{DIODE})$ or approximately +5.6V. When E2 drives the base voltage of Q1 lower than the emitter set bias, Q1's base to emitter junction becomes reversed biased and Q1 is cut off. When Q1 cuts off, its collector uses the voltage set by the divider consisting of R4 and R3, turning Q2 on. When Q2's base-to-emitter becomes forward biased, D1 becomes reversed biased. When Q2 is turned on it operates in the active region; its emitter voltage is then a base-to-emitter drop below the voltage set at its base. When Q2 is on, its output voltage reverse biases D2 and Q2's current is limited by R5 to $(V_{BASE} - V_{BEon})/R5$. When Q1 is cut off and Q2 is turned on, the voltage across R5 is $+15V(R3)/(R3+R4) - V_{be}$, or approximately +12V. The arrangement of Q1 and Q2 is such as to transform the 100-ns output pulse of E48 from logic levels to a 100-ns pulse that switches between +5.6V and +12V.

NOTE

Certain E number references were changed after the C revision etch, i.e., D and higher, of the A320 module. In the following paragraphs these references are shown as: (EXX). For earlier revisions (up through the C revision etch) the circuit references are shown as: EXX.

D27 and E30 (E31) provide a stable Zener reference. R6 and R7 feedback to E30's (E31's) inverting terminal an attenuated version of the voltage at the junction of R6, R8, R9, and R10. E30 (E31) tends to correct for voltage variations at this junction, thus stabilizing the current through R9. With a fixed load across D27 the bias current through D27 will be stable.

The Zener reference created by D27 is applied to the inverting terminal of the amplifier composed of E36 and Q3. Note this is the noninverting terminal of E36 (E26) but the inverting terminal of the composite amplifier [E36 (E26) and Q3]. The noninverting input of E36 (E26) and Q3 is connected by R15 to a variable offset voltage. R131, R17, and R16 form an adjustable attenuator that effectively behaves by varying the voltage at the inverting terminal end of R14, thus varying the voltage drop across R14. When the voltage across R14 is varied the current flowing through R14, supplied by Q3's collector, is varied. A forward-biased, antilatchup diode (D37) and R19 complete the feedback loop to Q3's base. Q3's emitter is returned to +15 Vdc via R20, a resistor that is equal in value to R14. The voltage drop across R20 will be nearly equal to the voltage drop across R14. Q4's base is connected to Q3's base and Q4's emitter is returned to +15 Vdc through R21. If the V_{BEon} drops of Q3 and Q4 match and R21 equals R20, the voltage drop across R21 will equal the voltage drop across R20 when Q4 is on. Because the voltage drops across R21, R20 and R14 are equal and the resistor values are equal, Q4's collector current will be approximately equal to the current through R14 when Q4 is on. Q4's emitter is also connected via D4 to the source of the 100-ns pulse that switches between +5.6V and +12V. When the pulse level is at +5.6V, D4 becomes forward biased and drives Q4's

emitter voltage lower than its base voltage; this action reverse biases Q4's base to emitter junction and cuts off Q4. When the pulse level is at +12V D4 reverse biases and Q4's base to emitter junction becomes forward biased; therefore, Q4 turns on. The 100-ns pulse source, together with D4 and Q4, forms a switchable current source. This switchable current source drives C32. Each pulse of current linearity charges C32 a voltage increment that is: $\Delta V = (I_{source})(T_{pulse})/C$, or approximately 5 mV. The continuously incremental charging of C32 is the source of an "X" vector deflection.

C32 is discharged by three parallel FETs, Q7, Q8 and Q9. E42 drives the base of Q5. Q5's emitter is biased by the voltage divider of R24 and R23. When the base voltage is greater than the emitter bias (VC1 UNLATCH H) Q5 is cut off. When Q5's base voltage is lower (VC1 UNLATCH H is asserted) than its emitter voltage by V_{BEon}, Q5 acts as a current source to Q6's base and R25, and causes Q6 to switch on, its collector saturating at approximately -15V. When Q5 is cut off no current is delivered to Q6's base and R25; thus, Q6 turns off and R22 pulls Q6's collector up to +5 Vdc. The switching action of Q6 either reverse or forward biases D5. When D5 is forward biased the gates of Q7, Q8, and Q9 are at -15V, while their sources are at ground, causing the three FETs to be pinched off. When D5 is reversed biased, R26 pulls the gates of the three FETs to the same voltage as their sources, causing the FETs to turn on and discharge C32.

C32, which is the X vector deflection source, is buffered by a voltage follower, E21 (E12). R135 provides for offset trim of E21 (E12), allowing the output voltage of E21 (E12) to be set to zero when the input voltage is zero. The amplifier E15 (E10), following the buffered X vector deflection source, provides for a means to alter the polarity of the X vector deflection. FET switches Q12 and Q15 operate in a series shunt fashion to provide a gain from E15 of either +1 or -1. Drive for the anode of D26 and D6 is provided by circuits that are identical to the drive circuit for the D5 anode. When D26's drive forward biases it, D6's drive holds it reverse biased. With D26 forward biased, Q12's gate is at -15V while its source is at the same potential as the X vector deflection (A 0 to +5V signal) causing Q12 to be pinched off. When D26 is forward biased, D6 is reversed biased and R35 pulls the gate of Q15 to the same potential as Q15's source (ground), turning Q15 on. When Q15 is on and Q12 is off, the noninverting terminal of E15 is at ground, and the X vector deflection signal is applied to E15's inverting terminal via R33 with R36 providing feedback from the output of E15 (E10), which operates in the inverting mode with a gain magnitude of R36/R33 or approximately one. When D26's drive reverse biases it, D6's drive holds it forward biased. With D6 forward biased, Q15's gate is at -15V while its source is at ground, pinching Q15 off. When D6 is forward biased D26 is reversed biased and R32 pulls the gate of Q12 to the same potential as its source, turning Q12 on. When Q12 is on and Q15 is off, the X vector deflection is applied to both the noninverting terminal via Q12 and the inverting terminal via R33. R36 provides feedback from the output of E15 (E10), which operates in the noninverting mode with a gain magnitude of one. The output of E15 (E10), VG VECTOR X, is the horizontal (X) vector deflection signal.

3.2.13.5 X and Y Summing Amplifiers and Output Drivers – These circuits allow several distinct analog signals to be "added" to produce a single analog deflection voltage for controlling the electron beam in the VR14 CRT. The X and Y circuits are nearly identical. The Y summer receives one extra input, CCL2 DESCEND (0) H, which is used to offset several lower case characters (Paragraph 3.2.12.8). Otherwise, they operate in the same manner; only the X circuit will be described.

The typical summing amplifier configuration, shown in Figure 3-46, is a current summing amplifier that is used in applications where several current sources are monitored to yield an output voltage that is proportional to the sum of the inputs. Only three inputs are shown in Figure 3-46 but, theoretically, an infinite number of inputs could be summed. (This is the case in the GT40; the X summer has 3 inputs and the Y summer has 4 inputs.)

If all of the input resistors are of equal value, the circuit functions as a scaling ladder; by selecting various resistance values, the circuit can provide an output that is a weighted average of the inputs. (A description of how the current summing amplifier is used in digital-to-analog applications is provided in Paragraph 3.2.12.3.)

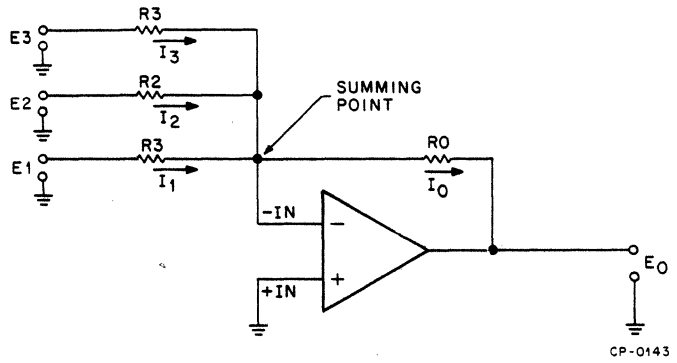


Figure 3-46 Summing Amplifier Configuration

Since the +IN is at ground, the -IN input to the op amp is also virtually at ground. The current drawn by the input is only negligible; thus, the total amount of current flowing through R1, R2, and R3 also flows through R0, and the output voltage is:

EO = IO X R0

Assume that resistors R0, R1, R2 and R3 all have a 1k value. Also, assume that E1, E2, and E3 are +2V inputs; I1, I2, and I3 each have a value of 2 mA, and IO has a value of 6 mA (total). With these defined values, a -6V output will be present at EO (the sum of E1, E2, and E3).

To illustrate how the inputs can be weighted, assume that the resistance values are: R1 = 1K, R2 = 2K, R3 = 3K, R0 = 1K. Apply +2V at E1, E2 and E3. The result will be: I1 = 2 mA, I2 = 1 mA, and I3 = 0.67 mA. Therefore, IO = 3.67 mA and EO = 3.67V.

The X Deflection Summing Amplifier receives inputs from the X DAC, X vector and character deflection circuits, and an attenuated version of Y character deflection signal. These inputs are summed at the inverting input of the summer, E7 (E4) (drawing A320-CSG). The summers output is buffered by an output driver E5 (E3) with feedback provided (R47) to the summers inverting input. The summers noninverting input is returned to ground via jumper W3. E7 (E4) and E5 (E3) function as an inverting mode summing amplifier and driver. The gain assigned to each summer input is determined by the ratio of the feedback resistor to the input resistor as previously described. Table 3-14 lists the components and gain for each input.

Table 3-14
X Deflection Gain

Summer Input	Input Resistor	Gain
X DAC	R38 = 422Ω	$\frac{R47}{R38} \approx 5$
X Vector Deflection	R37 = 2 kΩ	$\frac{R47}{R37} = 1$
X Character Deflection	R39 = 2 kΩ	$\frac{R47}{R39} = 1$

Note: Feedback resistor (R47) = 2 kΩ.

The X summer is also influenced by the Y character deflection current if the italics mode is specified (Paragraph 3.2.12.11). If SABR ITALICS (1) H is asserted (Q16 and Q17 are turned off), Y CHAR DEFLECTION is summed into the X summer, via R39, after it is attenuated by R43 and R42. This modifies the X character deflection signal to produce the italics effect.

3.2.14 Bootstrap Read Only Memory (ROM)

The Bootstrap ROM consists of four, 4-bit by 256 word bipolar memory integrated circuits in the M7014 module (drawing M7014-BRL) arranged to provide a 16-bit by 256 word memory. Although physically located, and accessed through, the GT40 Display Processor, the Bootstrap ROM (not to be confused with the display character ROM described in Paragraph 3.2.12.4) should be considered as a unit separate from the DPU. Although the Bootstrap Loader program bears no direct relationship to the display processor, it does cause the display program to be loaded into the MM11 display file.

The purpose of the Bootstrap ROM is to provide a means of initial communication between the host computer, via the DL11 Asynchronous Line Interface, and the PDP-11/05 in the GT40 Graphic Display Terminal, when the GT40 functions as a terminal device. Access to the ROM Bootstrap Loader program is initiated when its starting address, 166000_8, is placed in the PDP-11/05 Switch Register (SR) and START and LOAD are pressed. Unibus address bits BUS A (17:16) L are forced to a 1, which results in an address of 766000 on the address lines. This address is recognized by the M7014 address selection logic which then asserts a read enabling signal to the ROM; the ROM data is then read directly to the Unibus. Aside from the receipt and generation of appropriate interface signals, the decoding of the Bootstrap ROM starting address does not initiate any internal operations in the GT40 Display Processor.

An optional, upper, 256 word Bootstrap ROM is also contained in the M7014 module. However, the address jumper configuration (Table 3-15) is such that only the lower 256 word area can be accessed by the user.

Table 3-15
Bootstrap ROM Addressing

Memory Area	Address Range*	Address Jumpers				Asserted Output
		W26	W27	W28	W29	
Lower 256 Words	766000–766777	Out	In	Out	In	ASL ENABLE LOW ADDR L
Upper 256 Words**	767000–767777	In	Out	In	Out	ASL ENABLE HIGH ADDR L

*The two high order bits (16 and 17) are forced to 1s on the Unibus.
**Optional memory area.

The Bootstrap ROM address ($766XXX_8$) enters the display processor address selection logic (drawing M7014-ASL and Figure 3-47) in the same manner as the addresses for the GT40 hardware registers (Paragraph 3.2.4). However, in this case address bit 11 (BUS A 11 L yields ASL A 11 H and ASL A 11 L) is equal to a 1. ASL A 11 H provides one input to a 3-input, type 7410, NAND gate. Unibus address bit 12, also unlike the hardware address configurations, is equal to 0. Consequently, ASL A 12 H is ANDed with ASL C1 H (Unibus control bit C1 = 0, indicating a read) to provide a second input to the NAND gate. Therefore, when BUS MSYN L is sent by the PDP-11/05, the signal ASL ROM ENABLE L is asserted and ASL DISPLAY ENABLE L is inhibited. ASL ROM ENABLE L is then ANDed with bus address bit 9 = 0 (ASL A09 H, inverted) through jumper W27 to assert ASL ENABLE LOW ADDR L. (If the optional, upper 256 word ROM is to be selected, Unibus bit 9 must equal 1 to assert ASL ENABLE HIGH ADDR L.)

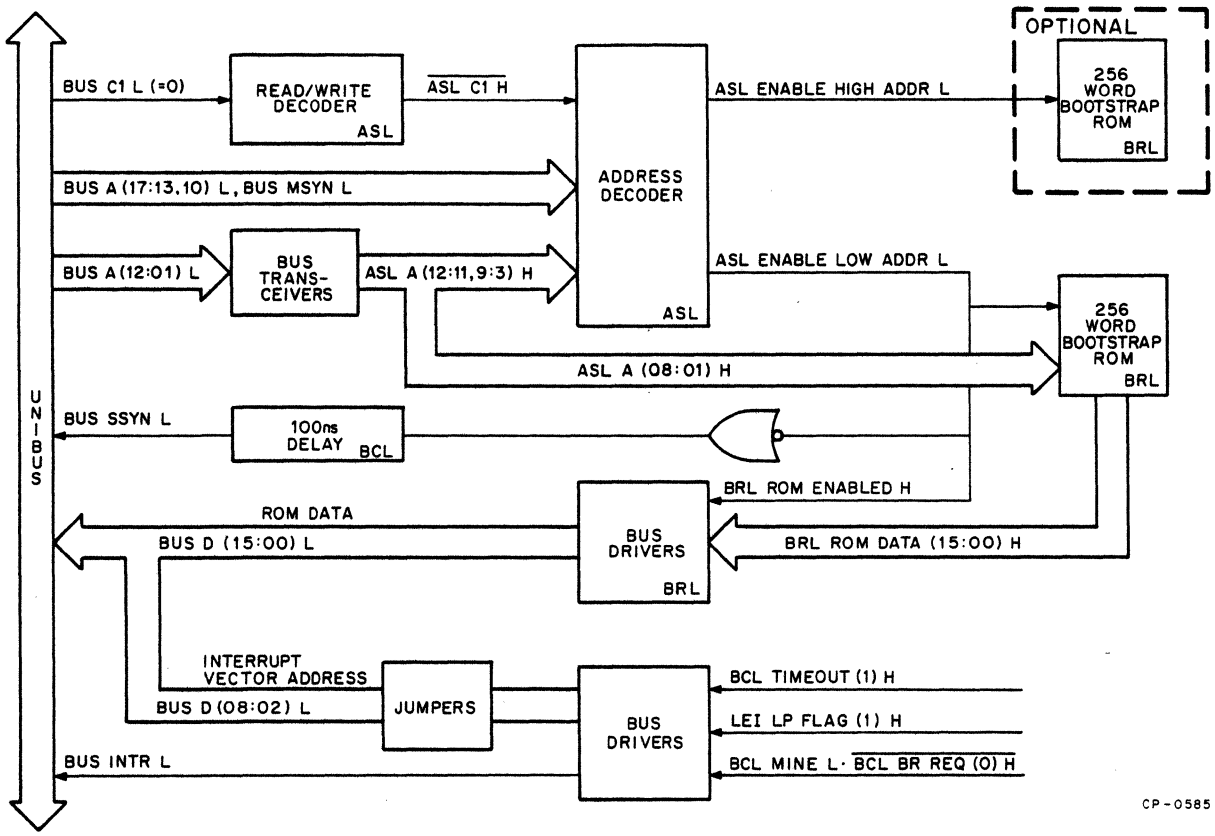


Figure 3-47 Unibus ROM and Interrupt Vector Address and Data, Block Diagram

The signal ASL ENABLE LOW ADDR L performs two concurrent functions:

a. it asserts ASL SET SSYN L which produces, after a 100-μs delay, the BUS SSYN L signal to the Unibus (drawing M7014-BCL); the PDP-11/05 responds to this by dropping BUS MSYN L

b. it provides the enabling signal to the Bootstrap ROM (drawing M7014-BRL).

This latter function results in the reading of the specified ROM location [bus address bits 1 through 8, ASL A (08:01) L]. At the same time the ROM chips are enabled, ASL ENABLE LOW ADDR L asserts BRL ROM ENABLED H. This signal gates the 16-bit read data, through a separate group of data bus drivers, to the Unibus. Successive words are read in the same manner. The handshaking and addressing are repeated for each word (address bits 1 through 8 vary from word to word) until the entire program is read.

Appendix D contains a program listing of the Bootstrap Loader; additional information can be found in the *GT40 User's Guide.*

3.3 DL11 ASYNCHRONOUS LINE INTERFACE

3.3.1 Introduction

The following paragraphs provide the user with the theory of operation and logic diagrams necessary to understand and maintain the DL11 Asynchronous Line Interface. The *GT40 User's Guide* contains programming information pertaining to the DL11.

Interface signals fed to, or received from, the Berg connector on the M7800 module are preceded by the pin number in parentheses. The (H) and (L) suffixes are omitted because these signals are output to the modem cable via level converters (drawing DL-7) at nonstandard voltages:

(DD) EIA DATA TERMINAL READY

3.3.2 General Module Description

The DL11-E option of the DL11 Asynchronous Line Interface is used in the GT40. It differs from the other DL11 options in baud rates, data code, and certain control and monitoring bits in the status registers. Although other DL11 options use the M7800 module, the M7800 module used in the DL11-E is slightly different and cannot be interchanged with M7800 modules designed for the DL11-A, B, C, or D options. Table 3-16 provides a brief description of the DL11 options; Table 3-17 lists available standard baud rates. These baud rates are developed from standard crystals supplied by DEC; however, the user may order special crystals, if desired.

Table 3-16
DL11 Options

Option	Data Code	Typical Use	Baud Rates	Notes	Description
DL11-A	Restricted(1)	Model 33 or 35 Teletype Model VT05 Display Terminal	110 150 300 600 1200 2400	a. No data set bits b. No Break or Error bits c. No 1200/110 split	Uses 20-mA current loop operation for receive, transmit, and reader run.
DL11-B	Restricted(1)	Model VT05 or VT06 Display Terminal	Same as DL11-A	a. No data set bits b. No Break or Error bits c. No 1200/110 split d. DATA TERMINAL READY and Request to Send (REQ TO SEND) bits strapped on permanently e. Null modem usually required for local EIA terminal	Has EIA drivers and receivers for compatability with EIA terminals.
DL11-C	Full Selection(2)	Model 28 Teletype	Crystal and switch selectable(3)	a. No data set bits b. Break and Error bits enabled	Basically identical to DL11-A except has full code and baud rate selection. Also includes both Break and Error bits.

Table 3-16 (Cont)
DL11 Options

Option	Data Code	Typical Use	Baud Rates	Notes	Description
DL11-D	Full Selection(2)	Model 37 Teletype (null modem required)	Crystal and switch select-able(3)	a. No data set bits b. Break and Error bits enabled c. DATA TERMINAL READY and REQ TO SEND bits strapped on permanently	Basically identical to DL11-B except has full code and baud rate selection. Also includes both Break and Error bits.
DL11-E	Full Selection(2)	Model 103 or 202 modems	Crystal and switch select-able(3)	a. Full data set control	Provides complete data set control. Data set lines monitored by this interface are: RING, REC DATA, CARRIER DETECT, CLEAR TO SEND, and Secondary Receive Data (SEC REC DATA). Data set lines controlled by the program are: Transmitted Data (XMIT DATA), REQ TO SEND, Secondary Transmitted Data (SEC XMIT DATA), and DATA TERMINAL READY.

Notes: 1. Restricted data code = 8 data bits, no parity, 1 or 2 stop bits.
2. Full selection data code = 5, 6, 7, or 8 data bits; parity off, even, or odd; and 1, 1.5, or 2 stop bits.
3. Baud rates that may be selected by the crystal and switch are listed in Table 3-17.

Table 3-17
Baud Rates with Standard Crystals

Switch Position	Crystal 1 (844.8 kHz)	Crystal 2 (1.03296 MHz)	Crystal 3 (0.152 MHz)	Crystal 4 (4.608 MHz)
1	36.7	44.8	50	200
2	55	67.3	75	300
3	110	134.5	150	600
4	220	269	300	1200
5	440	538	600	2400
6	880	1076	1200	4800
7	1320	1614	1800	7200
8	1760	2152	2400	9600
9*	–	–	–	–
10*	–	–	–	–

*These switch positions are for external clock inputs and do not tap off the crystal oscillator.

The DL11 mode of operation (A, B, C, D, or E) is determined by the configuration of eight jumpers on the M7800 module. The application of these jumpers is listed below; Table 3-18 contains the same information in more concise form.

J1 – Connects the EIA driver to REQ TO SEND lead (pin 4) of data set cable. Required for DL11-B, D, and E; does not affect DL11-A and C (drawing DL-7).

J2 – Connects the EIA driver, normally used for the REQ TO SEND lead, to the FORCE BUSY lead (pin 25) for use with the Bell 103E modem. Unless requested by the user, this jumper is excluded for all DL11s (drawing DL-7).

J3 – When inserted, this jumper allows the REQ TO SEND lead (pin 4) to be controlled by bit 2 of the Receiver Status Register. Excluded for the DL11-B and C and included for the DL11-E; J3 does not affect the DL11-A and C (drawing DL-4).

J4 – The DATA LEADS ONLY mode of EIA operation is forced when this jumper is inserted. DATA TERMINAL READY (pin 20) and REQ TO SEND (pin 4) are turned on. It is included for the DL11-B and D, and excluded for the DL11-E. This jumper does not affect the DL11-A and C (drawing DL-4).

J5 – When this jumper is inserted (DL11-C, D, and E) the Break bit is allowed to function. J5 is excluded for the DL11-A and B (drawing DL-4).

J6 – DATASET INT is allowed to cause interrupts when J6 is inserted (DL11-E). The jumper is excluded for the DL11-A, B, C, and D (drawing DL-4).

J7 – When J7 is inserted (DL11-E) the data set control bits are read as part of the Receiver Status Register. The jumper is excluded for the DL11-A, B, C, and D (drawing DL-2).

J8 – The Error bits are read as part of the Receiver Status Register when J8 is inserted (DL11-C, D, and E). In the DL11-A and B, the jumper is excluded (drawing DL-2).

Table 3-18
DL11 Mode Control Jumper Configurations

Jumper	DL11 Options					Reference Drawing
	A	B	C	D	E	
J1	*	IN	*	IN	IN	DL-7
J2	OUT	OUT	OUT	OUT	OUT	DL-7
J3	*	OUT	*	OUT	IN	DL-4
J4	*	IN	*	IN	OUT	DL-4
J5	OUT	OUT	IN	IN	IN	DL-4
J6	OUT	OUT	OUT	OUT	IN	DL-4
J7	OUT	OUT	OUT	OUT	IN	DL-2
J8	OUT	OUT	IN	IN	IN	DL-2

* = Irrelevant.

3.3.2.1 Cabling – Figure 3-48 illustrates the method of connecting cables between the various DL11 options and associated external devices.

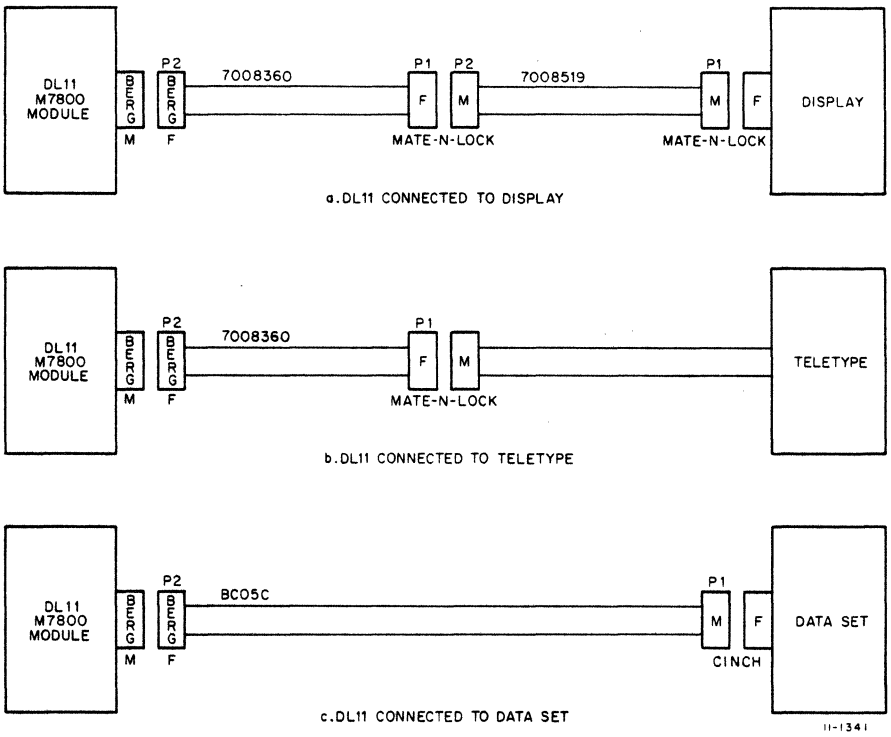


Figure 3-48 DL11 Cable Connections

Table 3-19 lists the signal names and associated pins on the Berg connector mounted on the M7800 module. This table also lists the associated signals supplied on the 7008360 and BC05-C cables. The latter cable is normally supplied with the GT40.

Table 3-19
Pin Connections

Berg Pin	M7800 Module	BC05-C Modem Cable (GT40)	7008360 Cable
A	Ground	Ground	Ground
B	Ground	Ground	
C	Force Busy (EIA)	Force Busy	
D		Secondary Clear to Send	
E	Serial Input (TTL)	Interlock In ←	Interlock In ←
F	Serial Output (EIA)	Transmitted Data	
H	20 mA Interlock		Interlock Out —
J	Serial Input (EIA)	Received Data	
K	Serial Input + (20 mA)		Received Data +
L		External Clock	
M	EIA Interlock	Interlock Out —	
N		Serial Clock Transmitter	
P		Secondary Request to Send	
R		Serial Clock Receiver	

Table 3-19 (Cont)
Pin Connections

Berg Pin	M7800 Module	BC05-C Modem Cable (GT40)	7008360 Cable
S	Serial Input - (20 mA)		Received Data -
T	Clear to Send (EIA)	Clear to Send	
U			
V	Request to Send (EIA)	Request to Send	
W		-Power	
X	Ring (EIA)	Ring	
Y		+ Power	
Z		Data Set Ready	
AA	Serial Output + (20 mA)		Transmitted Data +
BB	Carrier (EIA)	Carrier	
CC	Clock Input (TTL)		
DD	Data Terminal Ready (EIA)	Data Terminal Ready	
EE	Reader Run - (20 mA)		Reader Run -
FF	Secondary Transmitter (EIA)	202 Secondary Transmit	
HH	Berg Clock Enb		
JJ	Secondary Receiver (EIA)	202 Secondary Receive	
KK	Serial Output - (20 mA)		Transmitted Data -
LL		EIA Secondary Transmit	
MM		Signal Quality	
NN		EIA Secondary Receive	
PP	Reader Run + (20 mA)		Reader Run +
RR		Signal Rate	
SS	Serial Output (TTL)		
TT	+5V		
UU	Ground	Ground	Ground
VV	Ground	Ground	Ground

Table 3-20 provides a quick reference of M7800 input/output signals for TTL, EIA, and 20-mA current loop devices.

Table 3-20
Input/Output Signals

Type	Signals		Pin No.
TTL Signals	Input:	Serial Data	E
		Clock	CC
		Clock Enable	HH
	Output:	Serial Data	SS
20-mA Current Loop Signals	Input:	+ Serial Data	K
		- Serial Data	S

Table 3-20 (Cont)
Input/Output Signals

Type		Signals	Pin No.
20-mA Current Loop Signals (cont)	Output:	+ Serial Data	AA
		- Serial Data	KK
		+ Reader Run } (RDR ENB)	PP
		- Reader Run } (RDR ENB)	EE
EIA Signals	Input:	Serial Data	J
		Clear to Send	T
		Ring	X
		Carrier	BB
		Secondary Receive	JJ
	Output:	Serial Data	F
		Force Busy	C
		Request to Send	V
		Data Terminal Ready	DD
		Secondary Transmit	FF

Table 3-21 lists connector pin numbers and signals for the 7008360 cable.

Table 3-21
7008360 Connections

Twisted Pair	Color	Mate-N-Lok Connector P1 (To Device)	Berg Connector P2 (To DL11)	Signal
Black/Red	Black	2	KK	- Transmitted Data
	Red	3	S	- Received Data
Black/White	Black	4	EE	- Reader Run
	White	5	AA	+ Transmitted Data
Black/Green	Black	6	PP	+ Reader Run
	Green	7	K	+ Received Data
			black E	Interlock In
			black H	Interlock Out

Notes: 1. Connector on ASR Teletype uses all pins (2–7).
2. Connector on KSR Teletype does not use pins 4 or 6 (Reader Run - and +).

Table 3-22 lists connector pin numbers and signals for the 7008519 cable connector which is used in conjunction with the 7008360 cable.

Table 3-22
7008519 Connections

7008360 Mate-N-Lok Connector P1	Mate-N-Lok Connector P2 (To 7008360)	Color	Mate-N-Lok Connector P1 (To Device)	Signal
2	2	Black	2	- Transmitted Data
3	3	Red	3	- Received Data
4				
5	5	White	5	+ Transmitted Data
6				
7	7	Green	7	+ Received Data

Table 3-23 lists connector pin numbers for the BC05-C cable connectors.

Table 3-23
BC05-C Connections (GT40 Application)

Color	Cinch Connector P1 (To Device)	Berg Connector P2 (To DL11)	Signal
Blue/White	1	A	Ground
		VV	Ground
White/Blue	2	F	Transmitted Data
Orange/White	3	J	Received Data
White/Orange	4 black	V	Request to Send
Green/White	5	T	Clear to Send
White/Green	6	Z	Data Set Ready
Brown/White	7	B	Ground
		UU	Ground
White/Brown	8	BB	Carrier
Slate/White	9	Y	+ Power
White/Slate	10	W	- Power
Blue/Red	11	FF	202 Secondary Transmit
Red/Blue	12	JJ	202 Secondary Receive
Orange/Red	13	D	Secondary Clear to Send
Slate/Red	14	LL	EIA Secondary Transmit
Slate/Green	15	N	Serial Clock Transmit
Red/Brown	16	NN	EIA Secondary Receive
Slate	17	R	Serial Clock Receive
Red/Slate	18	U	Unassigned
Blue/Black	19	P	Secondary Request to Send
Black/Blue	20	DD	Data Terminal Ready
Orange/Black	21	MM	Signal Quality
Black/Orange	22	X	Ring
Green/Black	23	RR	Signal Rate
Brown/Red	24	L	External Clock
Red/Orange	25	C	Force Busy
		E	Interlock In
		red M	Interlock Out

3.3.3 Data Format

The data format for the DL11 (Figure 3-49) is referred to as "full selection" because there are a number of variables. This format consists of a Start bit, five to eight Data bits, a Parity bit, and one, one and one-half, or two Stop bits.

When less than eight Data bits are selected in the DL11 format, the hardware justifies the bits into the least significant bit positions for characters received by the interface. When transmitting characters, the program provides the justification to the least significant bits. The Parity bit may be either on or off; when on, it can be selected for checking either odd or even parity during receive and for providing an extra Parity bit during transmit.

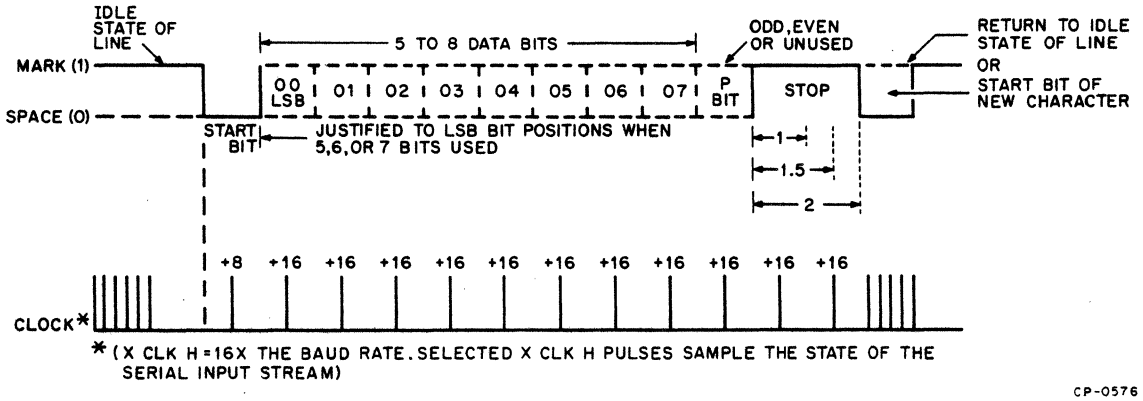


Figure 3-49 DL11 Data Format

All variable items within any data format are selected by jumpers on the M7800 module. None of the variables can be controlled by the program. Split lugs are provided on the module for installation of appropriate data format jumpers. These jumpers are listed in Table 3-24 and described more fully in Paragraph 3.3.6.

Note that a jumper indicates a low (0) and no jumper indicates a high (1). The jumper locations are shown on DL11 drawing DL-4.

Table 3-24
Data Format Jumpers

Name	Jumper*	UART Pin No.*	Function
No Parity	NP	35	Enables or disables the parity bit in the data character. When enabled, the value of the parity bit is dependent on the type of parity (odd or even) selected by the even parity select (EPS) jumper. When disabled, the Stop bits immediately follow the last Data bit during transmission. During reception, the receiver does not check for parity. jumper – parity enabled no jumper – parity disabled

Table 3-24 (Cont)
Data Format Jumpers

Name	Jumper*	UART Pin No.*	Function
Even Parity	EPS	39	Determines whether odd or even parity is to be used. The receiver checks the incoming character for appropriate parity; the transmitter inserts the appropriate parity value. jumper – odd parity no jumper – even parity
Stop Bit	2SB	36	Used in conjunction with three other junpers (J9, J10, and J11) to select the desired number of Stop bits. 1 Stop bit – jumper in 2SB jumper in J10 no jumpers in J9, J11 2 Stop bits – no jumper in 2SB no jumpers in J9, J11 jumper in J10 1.5 Stop bits – jumper in 2SB jumper in J9 or J11 no jumper in J10
Number of Data Bits	NB1	38	These two jumpers are used together to provide a code that selects the desired number of Data bits in the character. Note that in the following code, a 0 indicates a jumper a 1 indicates no jumper: NB2 NB1 No. of Data Bits 0 0 5 0 1 6 1 0 7 1 1 8

*Shown on drawing DL-4.

3.3.4 Functional Description

The DL11 is a character-buffered communications interface that performs two basic operations: receiving and transmitting asynchronous data. When receiving data, the interface converts an asynchronous serial character from an external device into the parallel character required for transfer to the Unibus. This parallel character can then be gated through the bus to the memory, a processor register, or some other device. When transmitting data, a parallel character from the bus is converted to a serial line for transmission to the external device. Because the two data transfer units (receiver and transmitter) are independent, they are capable of simultaneous 2-way communication. The receiver and transmitter each operate through two related registers: a Control and Status Register for command and monitoring functions, and a Data Buffer Register for storing data prior to transfer to the bus or the external device.

3.3.4.1 **DL11 Data Set Interface Operation** – Only the DL11-E (Figure 3-50) option can be used to interface data sets. The DL11 uses call and acknowledge signals from the computer and the data set, translates these signals to set up a handshaking sequence, thus establishing a data communication channel.

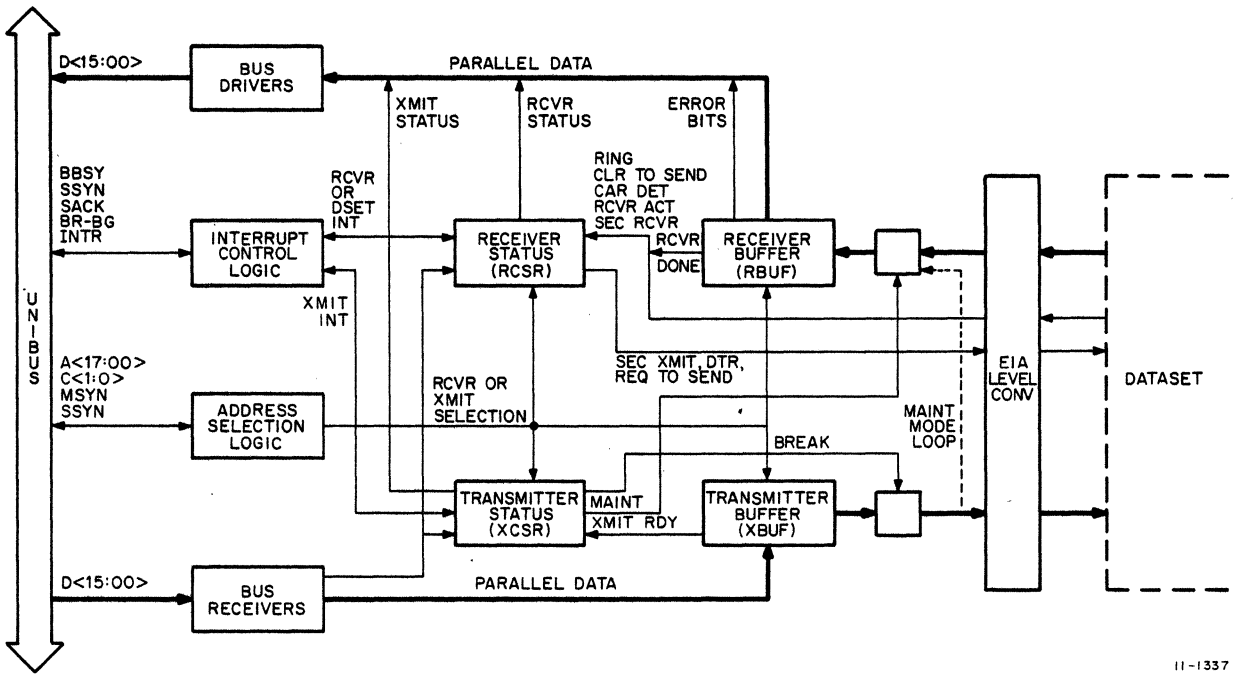


Figure 3-50 DL11-E Block Diagram

A typical method of establishing a data communication channel is as follows: the data set at the PDP-11/05 computer is called by another remote data set and a RING signal is transmitted to the DL11 Interface. This RING signal initiates an interrupt provided the DATASET INT ENB bit in the DL11 Register is set. The resident PDP-11/05 program then determines if the interrupt was caused by RING and, through a service routine, issues DATA TERMINAL READY and REQ TO SEND signals. These signals cause the data set to answer the call and send a carrier signal tone to the caller. The caller acknowledges the carrier signal with its own carrier signal which, when detected by the data set, causes another PDP-11/05 interrupt (CARRIER) sequence to be initiated. Upon recognizing the CARRIER interrupt, the resident PDP-11/05 program can then either receive or transmit data. The only two prerequisites for the handshaking sequence are that the program use appropriate service routines and that the DATASET INT ENB bit in the DL11 Status Register is set prior to setting up the data channel.

Once the data channel is set up, the DL11 receiver accepts incoming serial data from the data set lines for parallel conversion and transfer to the Unibus. The transmitter converts parallel data from the bus and shifts the resultant serial data onto the data set lines.

The receiver offers serial-to-parallel conversion of 5, 6, 7, or 8 data bit level codes. This serial character code is described in Paragraph 3.3.3. Once the character has been received, a parity error flag, if selected, is available to the programmer for testing. An interrupt request (RCVR DONE flag) is initiated in the middle of the first Stop bit of the character being received. This indicates that the character is stored in the receiver holding register. If the program does not transfer the character from the holding register before the middle of the first Stop bit of the next character, a data overflow error (OR ERR) bit is set in the receiver buffer status register. This buffer also provides other error indications such as framing error (FR ERR), which indicates that the character had no valid Stop bit, and parity

error (P ERR), which indicates that the received parity did not agree with the expected parity. It should be noted that both the receiver and transmitter character length and format are controlled by jumpers on the module and are always identical.

The transmitter performs parallel-to-serial conversion of 5, 6, 7, or 8 data bit level codes. Data from the Unibus is loaded in parallel into the holding register. When the transmitter shift register is empty, the content of the holding register is shifted into the transmitter shift register and the XMIT RDY flag comes up. A second character from the bus can then be loaded into the holding register. However, because the shift register is still working on previous data, the shifting operation of the second character is delayed until the previous character has been completely transmitted. Once the last bit of a character is transferred to the data set (because of double-buffering, this is actually the last bit of the first character in a 2-character pair), the interface initiates an interrupt request (XMIT RDY) to indicate that the buffer is empty and can now be loaded with another character for transfer to the data set. The Transmitter Status Register (XCSR) contains a Break bit that can be set to transmit a continuous space to the data set. A maintenance (MAINT) bit is also available to connect the serial output of the transmitter to the input of the receiver and to force the receiver clock speed to be the same as the transmitter speed.

The rest of the control portion of the DL11 is available through the Receiver Status Register (RCSR) and provides the necessary command and monitoring functions for use with Bell 103 and 202 Data Sets. This register monitors such functions as: CLEAR TO SEND, which indicates the operating condition of the data set; CAR DET, which indicates that the carrier is being received; RCVR ACT, which indicates that the receiver is accepting a character; and RCVR DONE, which indicates that a full character is stored in the receiver buffer.

Data set interrupt requests are initiated at the positive-going transition of RING, CAR DET, CLEAR TO SEND, or SEC REC signals. The SEC REC (secondary or supervisory received data) and the SEC XMIT (secondary or supervisory transmitted data) bits provide receive and transmit capabilities for the reverse channel of a remote station. The DATA TERMINAL READY bit functions as a control lead for the data set communication channel and permits the channel to be either connected or disconnected.

The DL11 contains EIA level converters to change bipolar inputs to TTL logic levels and TTL logic level outputs to the bipolar signals required by the data set. The EIA converters provide failsafe operation of the control leads because they appear to be off if the data set loses power.

3.3.5 Physical Description

The DL11 Interface is packaged on a single M7800 Quad Integrated Circuit module that can easily be plugged into the appropriate slot in the GT40 (Figures 3-51 and 4-27).

The M7800 module has a Berg connector for all user input/output signals. The specific signals fed to this connector depend on the particular option used. The signals transferred between the M7800 and the external device are dependent on the specific cable used with the selected option. Mounting, cabling, and connector information is given in Paragraph 3.3.2.1.

The specific baud rate used with the DL11 Interface is selected by a switch that taps off the frequency divider output of a crystal oscillator.

One of four available crystals (1.03296 MHz, 844.8 kHz, 1.152 MHz, or 4.608 MHz) is mounted on the M7800 module as shown on Figure 3-51. A different crystal can be used, if desired, but the DL11 operating speed is limited from 40 baud to 10 kbaud.

Figure 3-51 also shows the position of the two switches used to select the baud rate. Both switches are identical: one is used for the receiver portion of the interface; the other is used for the transmitter. Each switch is a 10-position rotary switch. Positions 9 and 10 are used to select an external clock. Positions 1 through 8 are used to select the baud rate from the crystal. The standard available baud rates selected by each switch position are listed in Table 3-17. A detailed description of the frequency division is given in Paragraph 3.3.6.7.

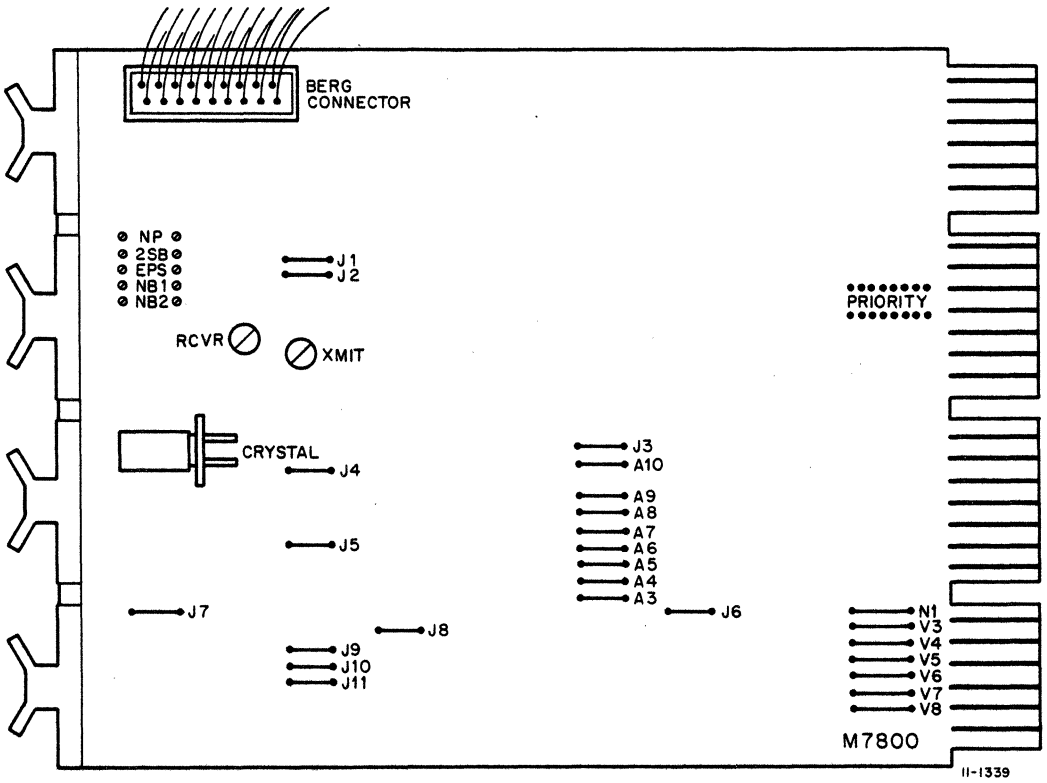


Figure 3-51 Crystal Switch and Jumper Locations, M7800 Module

Specifications – Operating and physical specifications for the DL11-E Asynchronous Line Interface are given in Table 3-25.

Table 3-25
DL11 Operating Specifications

Specification	Description
Registers	Receiver Status Register (RCSR) Receiver Buffer Register (RBUF) Transmitter Status Register (XCSR) Transmitter Buffer Register (XBUF)
Register Addresses (The MSD is forced to a 7 on the Unibus.)	RCSR 175610 RBUF 175612 XCSR 175614 XBUF 175616
Interrupt	300/302 = Receiver Interrupt
Vector Addresses (Floating Vectors [Figure B-1])	304/306 = Transmitter Interrupt

Table 3-25 (Cont)
DL11 Operating Specifications

Specification	Description
Priority Level	BR5
Interrupt Types	Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE) Data Set Interrupt (DATASET INT) which is caused by one of the following: CAR DET (carrier detect) RCV ACT (receiver active) SEC REC (secondary receiver) RING (ringing signal)
Commands	Receiver Interrupt Enable (RCVR INT ENB) Transmitter Interrupt Enable (XMIT INT ENB) Reader Enable (RDR ENB) Maintenance Mode (MAINT) Break (BREAK) Dataset Interrupt Enable (DATASET INT ENB) Secondary Transmit (SEC XMIT) Request to Send (REQ TO SEND) Data Terminal Ready (DTR)
Status Indications	Receiver Active (RCVR ACT) Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE) Error (ERROR) Overrun (OR ERR) Framing Error (FR ERR) Parity Error (P ERR) Clear to Send (CLEAR TO SEND) Carrier Detect (CAR DET) Secondary Receive (SEC REC) Ring (RING)
Data Input and Output	Serial data, EIA and CCITT specifications, compatible with Bell 103 and 202 data sets.
Data Format	1 Start bit; 5, 6, 7, or 8-bit Data character; Parity bit (odd, even, or unused); 1, 1.5, or 2 Stop bits.
Data Rates	Baud rate dependent on crystal used and switch position (Table 4-16).
Clock Rates	Crystal oscillator at one of four standard frequencies: 1.03296 MHz, 844.8 kHz, 1.152 MHz, or 4.608 MHz. External clock can be connected to two switch positions (9 and 10). Special crystal frequencies can be ordered from DEC.

Table 3-25 (Cont)
DL11 Operating Specifications

Specification	Description
Bit Transfer Order	Low-order bit (LSB) first.
Parity	Computed on incoming data or inserted on outgoing data dependent on type of parity (odd or even) used. Parity may be odd, even, or unused.
Size	Consists of a single quad module (M7800) that occupies one slot in the GT40.
Cable	One BC05-C-25 (25-ft length) cable with Berg connector for mating to M7800 and male Cinch connector for mating to device.
Power Required	1.8A at +5V 150 mA at -15V 50 mA at level between +9V and +15V

3.3.6 Detailed Description

This paragraph provides a detailed description of the DL11 Asynchronous Line Interface. The discussions in this chapter are supported by a complete set of engineering drawings contained in DEC-11-HGTEA-A-D.

The complete DL11 Interface can be divided into eleven functional areas; each of these areas is covered separately in subsequent paragraphs. Table 3-26 lists each functional unit and the general purpose of the unit. A description of the prime differences between options (baud rates, code, operation, etc.) is presented in Paragraph 3.3.2.

Table 3-26
DL11 Functional Units

Functional Unit	Purpose
Selection Logic	Determines if the DL11 interface has been selected for use and what type of operation (transmit or receive) has been selected. Permits selection of one of four internal registers and determines if the register is to perform an input or output function.
Interrupt Logic	Permits the interface to gain bus control and perform a program interrupt. Either the receiver or transmitter can issue an interrupt request. The DL11 can issue a data set interrupt in addition to the two other interrupts. Priority level of bus request (BR) line can be changed by the user.
Register Logic	Four internal registers, addressable by the PDP-11/05 program, provide data transfer, command and control, and status monitoring functions for the interface. Although all options have the same registers, the number of bits used may differ from option to option. However, bit positions of specific bits do not change.

Table 3-26 (Cont)
DL11 Functional Units

Functional Unit	Purpose
Transmitter Control Logic	Provides necessary input control signals for the UART when it is used to convert parallel data from the bus to serial data required by the external device. Typical signals include: data strobe, clock frequency, and parity select.
Receiver Control Logic	Provides necessary input control signals for the UART when it is used to convert serial data to the parallel data required for transmission to the bus. Typical signals include: data enable, status word, and clock frequency.
Universal Asynchronous Receiver/Transmitter (UART)	Performs the necessary serial-to-parallel or parallel-to-serial conversion on the data and supplies control and error detecting bits.
Clock Logic	Determines the clock frequency and, therefore, the baud rates for the transmitter and receiver sections of the UART. Eight baud rates are derived from a single crystal. One of four standard crystals is offered with the options.
Maintenance Mode Logic	Performs a closed loop test of the DL11 control logic by tying the serial output of the transmitter to the receiver input and forcing the receiver clock to be the same frequency as the transmitter clock.
Break Generation Logic	Permits the transmission of a continuous space or "break." The duration of the break can be timed by the pseudo-transmission of a specific number of characters.
EIA Logic	Provides necessary level converters for use with EIA levels.
Data Set Logic	Provides full EIA data set control. Monitors such data set lines as REC DATA, SEC REC DATA, CARRIER DETECT, RING, and CLEAR TO SEND. Permits program to control XMIT DATA, DATA TERMINAL READY, REQ TO SEND, and SEC XMIT DATA.

3.3.6.1 Address Selection – The address selection logic (drawing DL-5) decodes the incoming address information from the bus and provides the signals that determine which register has been selected and whether it is to perform an input or output function. Jumpers on the logic can be altered so that the module responds to any address within the range 774000 to 777777. However, standard address assignments for the DL11 in the GT40 fall within the range of 175610 to 175616. Table 3-27 lists the address assignments as used in the DL11 plus those addresses available for 30 additional units. The physical location of the jumpers on the M7800 module is shown in Figure 3-51.

NOTE

The addresses referred to in Table 3-27 are the addresses that are input to the DL11 from the Unibus. Because PDP-11/05 operations are restricted to 16 bits, DL11 addresses developed in the PDP-11/05 have an MSD = 1; the two high-order bits are forced to the Unibus address lines to assert MSD = 7.

Table 3-27
DL11 Address Assignments

Unit	Address*	Use
1	775610	RCSF
	775612	RBUF
	775614	XCSR
	775616	XBUF
2	775620	Unassigned
	775622	↓
	775624	
	775626	
.	.	
.	.	
31	776170	
	776172	
	776174	
	776176	

*Addresses placed on the Unibus have the MSD forced to 7. This is the address recognized by the DL11.

In the GT40, the jumper configuration is such that the M7800 module responds to the addresses of the four registers: RCSR, RBUF, XCSR, and XBUF. Although these addresses have been selected by DEC as the standard assignments for the DL11 when it is used in the GT40, the user may change the jumpers to any address desired. However; any MAINDEC program or other software that references these standard DL11 address assignments must be modified accordingly if other than the standard assignments are used.

The first five octal digits of the address (77561) indicate that the DL11 has been selected as the device to be used. The final octal digit, consisting of address lines A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. The two mode control lines, C00 and C01, determine whether the selected register is to perform a Unibus input or output operation (provided the selected register is a read/write register).

Address decoding is performed by a series of logic gates that provide the inputs to a 4-line to 10-line decoder circuit (7442 IC chip). Basically, the state of the four input lines provides a signal on one of the 10 output lines (only 7 of the 10 output lines are used in the DL11).

Three of the input lines (IC pins 15, 14, and 13) are true or false dependent on the state of input lines BUS A01, BUS A02, and BUS C1, respectively. Lines BUS A01 and BUS A02 are used to select one of four registers, and line BUS C1 controls direction of data transfers, i.e., gate data to the bus (DATI, DATIP) or gate data from the bus (DATO, DATOB). The fourth input line (pin 12) is an address enable signal that must always be true for the decoder to operate. This address enable signal is derived from a series of gates that are true when MSYN is present and when the address line conditions indicate that one of the four valid addresses is present on the bus, and when the Unibus cycle is not a DATOB to the odd byte (i.e., A00 = 1, C1 = 1, and C0 = 1).

Table 3-28 lists the input conditions required to select an appropriate output signal. Note that only one of these output signals can be present at any given time.

Table 3-28
Register Selection Signals

7442 Decoder Pins				Function Selected	Register	Bus Cycle
Pin 15 (A01)	Pin 14 (A02)	Pin 13 (C1)	Output Pin			
0	0	0	1	Receiver status to bus	RCSR	DATI or DATIP
1	0	0	2	Receiver buffer to bus	RBUF	DATI or DATIP
0	1	0	3	Transmitter status to bus	XCSR	DATI or DATIP
1	1	0	4	Not used	–	–
0	0	1	5	Bus to receiver status	RCSR	DATO or DATOB*
1	0	1	6	Bus to receiver buffer	RBUF	DATO or DATOB*
0	1	1	7	Bus to transmitter status	XCSR	DATO or DATOB*
1	1	1	9	Bus to transmitter buffer	XBUF	DATO or DATOB*

Notes: 1. There is no selection signal for XBUF because it is a write only register.

2. The bus to receiver buffer signal is used to produce a SEL 2 signal for KL11 Teletype Control compatability. This signal is not used to load the buffer because RBUF is a read-only buffer.

3. Input pin 12 is not shown since it must be true in all cases (address enable level).

4. Only seven of the possible ten outputs are used in the DL11. Output pins 4, 10, and 11 are unused.

*DATOB to low byte only (A00 = 0).

A simplified block diagram of the address selection logic is shown in Figure 3-52. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the DL11-E Interface is used, an OUT transfer is a transfer of data out of the master (the processor) and into the interface. Similarly, an IN transfer is the operation of the interface furnishing data to the master (processor).

The address selection logic input signals consist of 18 address lines, A (17:00); 2 bus control lines, C (1:0); and a master synchronization (MSYN) line. The address selection logic decodes the incoming address as described below. This address format is shown in Figure 3-53. Note that all input gates are standard bus receivers.

a. Lines A01 and A02 are decoded to select one of the four addressable device registers.

b. Line C1 is decoded to select either an input (DATI) or output (DATO) function. When line C1 is false, an input (read) operation is selected; when it is true, an output (write or load) operation is selected.

c. Decoding of lines A (10:03) is determined by jumpers. When a given line contains a jumper, the address logic searches for a 0 on that line; if there is no jumper, the logic searches for a 1.

NOTE
Connection of jumpers on the M7800 module is identical to the method used on other devices that employ an M105 Address Selector.

d. Address lines A (17:11) must be all 1s. This specifies an address within the top 8K byte address bounds for device registers.

e. Line A00 is used for byte control in such a manner that no control signals are generated when a byte operation is performed on the high-order byte of any register.

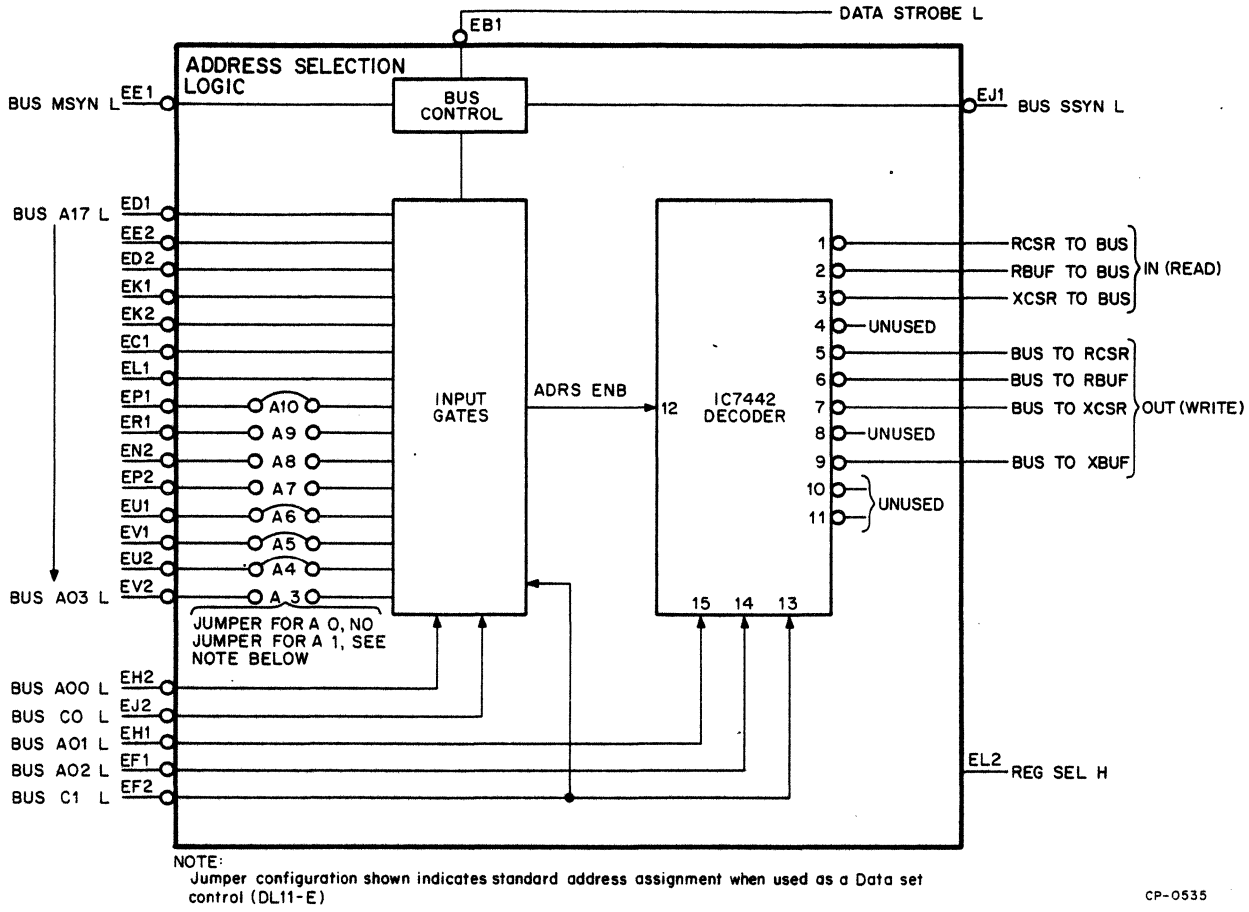


Figure 3-52 Address Selection Logic, Simplified Diagram

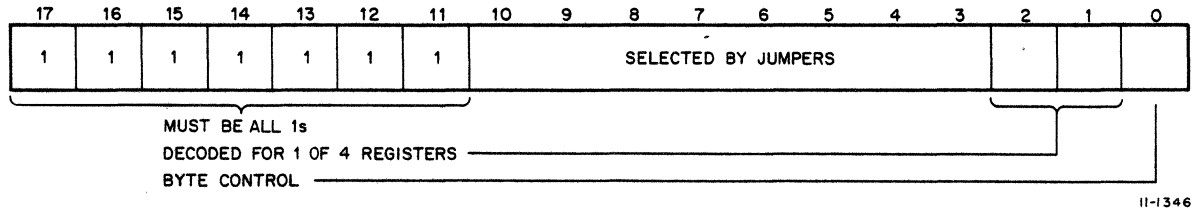


Figure 3-53 Interface Address Format

The address selection logic output signals that are used permit selection of four 16-bit registers and determine whether information is to be gated into or out of the master device. All of these output signals are listed in Table 3-28.

The first three output signals listed in Table 3-28 are used to read (gating data into the master) three of the registers (RCSR, RBUF, and XCSR). There is no signal generated for the fourth register (XBUF) because it is a write only register.

Three of the remaining four signals are used for writing (gating data from the master) into three of the registers (RCSR, XCSR, and XBUF). Although the fourth register (RBUF) is a read only register, which cannot be loaded, a

signal is still produced. However, this signal is not used as a true loading signal but is used to produce SEL 2 L, which is necessary for compatability in those configurations that include the KL11 (the KL11 is not used with the PDP-11/05 in the GT40).

The address selection logic also produces two other outputs: BUS SSYN L, and DL-5 LD XD L.

The BUS SSYN L signal is derived from MSYN and the address line inputs and is the acknowledgment signal that is returned to the master device approximately 400 ns after MSYN becomes true.

When the transmitter buffer (XBUF) is addressed for loading, the address selection logic produces the DL-5 BUS TO XBUF output signal. This signal triggers a monostable multivibrator that generates the DL-5 LD XD L pulse. This pulse strobes data from the bus lines into the UART and is of sufficient duration to allow data to be strobed into the UART. The DL-5 LD XD L pulse also inhibits the assertion of BUS SSYN L, which ensures that the D lines remain stable during strobing. Operation of the UART is described in Paragraph 3.3.6.6.

The purpose of SEL 2 L is to reset the DONE flag. When the RBUF has been addressed for reading or writing, a signal triggers a monostable multivibrator that generates SEL 2 L, which is applied to the UART. The function of this signal is to reset the DL-4 RCVR DONE H line, which indicates that an entire character has been received (DONE flag function).

3.3.6.2 **Interrupt Control** – The interrupt control logic (drawing DL-6) permits the DL11 Interface to gain control of the bus (become bus master) and perform an interrupt operation. Jumpers on the logic can be altered so that the logic has a normal vector address within the 000 to 776 range. However, the specific vector address used in the GT40 is determined by its use within the GT40.

The standard vector address assignments for the DL11 are listed in Table 3-29. Note that the vectors are "floating" and, therefore, are assigned according to the addressing scheme given in Appendix B.

Table 3-29
DL11-E Interrupt Vectors and Priority Levels

Vector Address*	Purpose	Priority
300/302	Receiver Interrupt	BR5
304/306	Transmitter Interrupt	BR5

*Floating vector addresses that are assigned according to a scheme that considers other PDP-11/05 devices in a particular system.

The interrupt control logic consists of a dual-input request and grant acknowledge circuit to establish bus control. One input (referred to as the A input) is connected to the receiver section and provides a vector address of 300. The other input (the B input) is connected to the transmitter section and provides a vector address of 304. The two circuits operate independently; however, if simultaneous interrupt requests occur, the receiver section has priority over the transmitter section.

NOTE
The final octal digit of the vector address is not affected by the jumpers; therefore, regardless of the vector address selected by the jumpers, the final octal digit is always 0 for the receiver and 4 for the transmitter.

Figure 3-54 is a simplified diagram of the interrupt control logic. It is important to note that the DL11-E option has the capability of handling multiple source interrupts in the receiver (A input) portion of the logic. In addition, the data set interrupt (DATASET INT) signal can be set by any one of several conditions such as RING, CARRIER, CLEAR TO SEND, and SEC REC DATA.

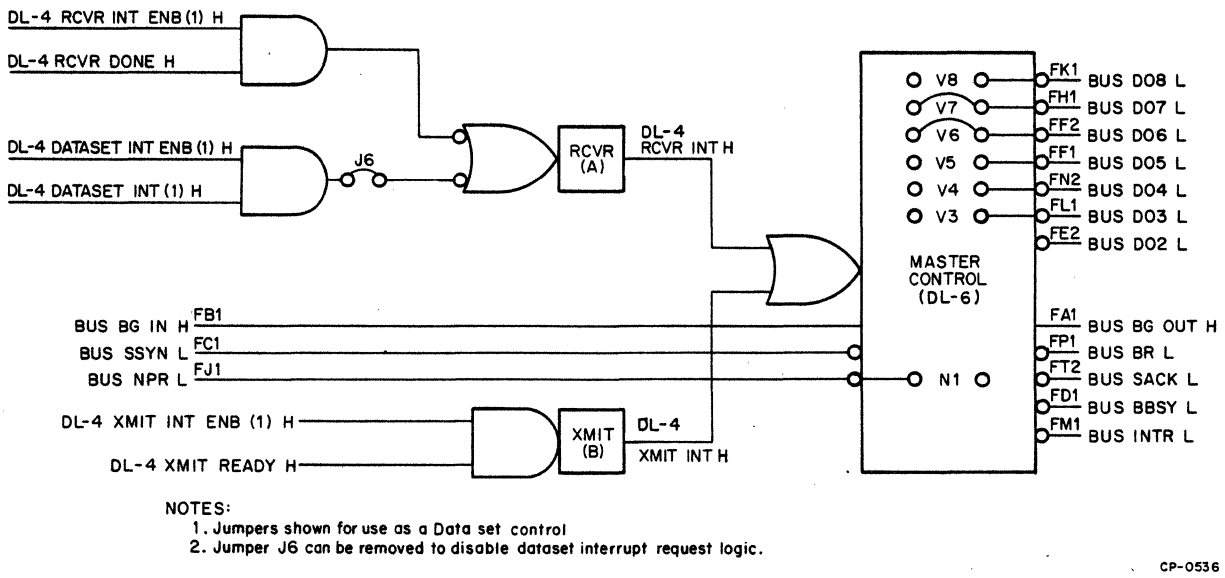


Figure 3-54 Interrupt Control Logic, Simplified Diagram

As shown in Figure 3-54, a receiver (or A input) interrupt request can be generated by either the receiver or the data set. In either case, RCVR INT is generated and sent to the master control logic which initiates the interrupt sequence. Jumper J6 on the DL11-E option can be removed to disable data set interrupt logic.

The receiver interrupt logic is shown on drawing DL-4. When the receiver is issuing an interrupt request, two input signals must be high: RCVR INT ENB (1) and RCVR DONE. When a 1 is loaded into bit 06 of the receiver status register (RCSR), it sets the RCVR INT ENB flip-flop to produce RCVR INT ENB (1). This signal is applied to one leg of a 2-input AND gate as an enabling level. The second input to the gate is RCVR DONE, which comes from the R DONE output line of the UART. When true, this line indicates that an entire character has been received, transferred to a holding register, and is ready for transfer to the bus. With the RCVR INT ENB (1) and RCVR DONE signals both true, the AND gate is qualified and RCVR INT is produced to initiate the interrupt sequence. A detailed explanation of UART operation is given in Paragraph 3.3.6.6.

When the data set is issuing an interrupt, two different input signals must be high: DATASET INT ENB (1) and DATASET INT (1). When a 1 is loaded into bit 05 of the RCSR, it sets the DATASET INT ENB flip-flop to produce DATASET INT ENB (1). This signal is applied to one leg of a 2-input AND gate as an enabling level. The second input to the gate is DATASET INT (1). The logic that generates this signal is shown on drawing DL-7 and described in Paragraph 3.3.6.3. Basically, the signal is generated by a flip-flop that is directly set when any one of the following data set signals is asserted: RING, CARRIER, CLEAR TO SEND, or SEC REC DATA. When this flip-flop sets, DATASET INT (1) is produced, the AND gate is qualified, and RCVR INT is generated, as before, to initiate an interrupt sequence.

The receiver (or A input) section of the interrupt control logic is used to gain bus control. When RCVR INT H is asserted, a bus request is made on the BR level corresponding to the level of the priority plug in the logic. The standard level for the GT40 is BR5. This level may be changed on the priority plug, if desired. When the priority

arbitration logic in the processor recognizes the request and issues a bus grant signal, the interrupt control circuit acknowledges with a SACK signal. When the DL11 interface has fulfilled all requirements to become bus master (BBSY false, SSYN false, and BG false), the interrupt control logic asserts BUS BBSY L (drawing DL-6).

The transmitter (or B input) section of the interrupt control logic operates in a manner similar to the receiver section (or A input). In this case, the two input signals that must be high are: XMIT INT ENB (1) and XMIT READY. When a 1 is loaded into bit 06 of the transmitter status register (XCSR), it sets the XMIT INT ENB flip-flop to produce XMIT INT ENB (1). This signal is applied to one leg of a 2-input AND gate as an enabling level. The second input to the gate is XMIT READY, which comes from the XRDY (transmitter ready) output line of the UART. When true, this line indicates that another character can be loaded into the UART holding register. With the XMIT INT ENB (1) and XMIT READY signals both true, the AND gate is qualified and XMIT INT H is produced to initiate an interrupt sequence. A detailed explanation of UART operation is given in Paragraph 3.3.6.6.

The transmitter control interrupt logic functions in an identical manner to the receiver control interrupt logic except that it generates a different vector address. Although both the receiver and transmitter are at the same BR level (for example, both at BR5), the receiver has a slightly higher priority.

Once the DL11 Interface has gained control by means of a BR request, an interrupt is generated. The interrupt vector address is selected by jumpers on the logic as shown in Figure 3-54. Because the vector is a 2-word (4-byte) block, it is not necessary to assert the states of bits 00 and 01.

The six selectable (jumpered) lines determine the two most significant octal digits of the vector address (drawing DL-6). The least significant octal digit is controlled by bit 02, so that all vector addresses end in either 0 or 4. The input to bit 02 is tied to the V2 flip-flop logic. Whenever an interrupt occurs in the receiver section, bus line D02 is not asserted, and the interrupt causes a vector at location 300. When an interrupt occurs in the transmitter control, bus line D02 is asserted, and the interrupt causes a vector at location 304. Note that the first two digits can be changed by the jumpers but the last digit is always either 0 or 4.

The BG IN signal is allowed to pass through the logic to BUS BG OUT when the interface is not issuing a request. To request bus use, the AND condition of interrupt enable and interrupt must be satisfied (i.e., RCVR INT ENB and RCVR DONE, or DATASET INT ENB and DATASET INT, or XMIT INT ENB and XMIT READY). Both levels must remain true until the interrupt service routine clears one of them. Once bus control has been attained, it is released when the processor has strobed in the interrupt vector. After releasing bus control, the logic inhibits further bus requests even if the interrupt and interrupt enable levels remain asserted. To make another bus request, one of two levels must be dropped and then reasserted to cause the logic to reassert the request line. This prevents multiple interrupts when the control logic is used to generate interrupts.

In the case of the DL11-E option, the receiver section handles a multiple source interrupt (RCVR DONE and DATASET INT). In addition, DATASET INT can be caused by one of many conditions (RING, CARRIER, etc.). If the program is servicing an interrupt for one condition and a second interrupt condition develops, it is possible that this second, and subsequent, interrupt may not occur. To prevent this, all possible interrupt conditions should be checked after servicing a specific condition. An alternative solution is to clear both interrupt enable bits (05 and 06) upon entry to the service routine for vector 300 and reset the bits at the end of the service routine.

Note that the interrupt control used in the DL11-E Interface is not capable of issuing NPR requests. To improve NPR latency, the NPR line is sampled and prevents an interrupt request until all NPRs have been honored. The sampling of the NPR line is controlled by a jumper (N1) on the DL11 Interface module. Jumper N1 is included on the M7800 module because this NPR sampling circuit cannot be used with certain PDP-11 processors; jumper N1 is cut to prevent this circuit from working. However, the sampling circuit can be used in PDP-11/05 applications and should be left in place.

3.3.6.3 Registers – All software control of the DL11-E Asynchronous Line Interface is performed by four device registers. These registers are assigned Unibus addresses and can be read or loaded with any PDP-11 instruction that

refers to their address (with certain exceptions such as load only or unused bits). Table 3-30 lists these registers and the function of each. Subsequent paragraphs discuss each of the registers from a hardware standpoint.

Table 3-30
Device Register Functions

Register	Mnemonic	Function
Receiver Status Register	RCSR	Provides detailed information on the status of the DL11-E receiver logic. Status information includes such flags as receiver active (RCVR ACT) and receiver done (RCVR DONE). Also includes the interrupt enable bit that can be used to initiate interrupt sequences when RCVR DONE sets. The RCSR also contains status and interrupt enable bits for use with data sets. Status bits include such information as carrier detection, ring, secondary transmitter, and clear to send.
Receiver Buffer Register	RBUF	Holds the character received from the external device prior to transfer to the Unibus. The receiver buffer also includes four error bits that are set if a corresponding error condition arises during reading of a character from the device.
Transmitter Status Register	XCSR	Provides the interrupt enable bit and the transmitter ready (XMIT RDY) flag so that transmitter logic can be monitored and an interrupt sequence initiated, if desired. Provides the maintenance bit which can be set under program control to use the maintenance mode of operation. A BREAK bit for continuous generation of a space is also included.
Transmitter Buffer Register	XBUF	Holds the character to be transferred to the external device.

Receiver Status Register (RCSR)

The Receiver Status Register (RCSR) is used to monitor the status of receiver logic operation when the DL11-E accepts a character and is used to initiate interrupt sequences.

The RCSR in the DL11-E option includes nine additional bits for use with data sets.

The DL11-E uses twelve bits for data set operations (Figure 3-55). Each of the bits is discussed separately in the following paragraphs, beginning with the most significant bit.

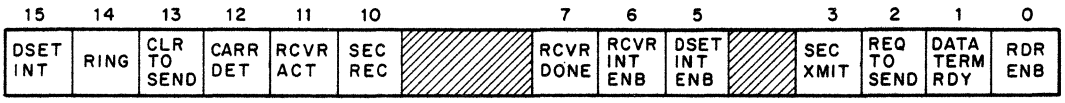


Figure 3-55 Receiver Status Register (RCSR), Bit Assignments

Data Set Interrupt Bit 15 – The data set interrupt (DATASET INT) bit indicates that a data set signal has made a transition. An interrupt sequence is initiated provided the DATASET INT ENB bit (bit 05) is also set. The DATASET INT bit is controlled by a flip-flop that is set whenever RING, CARRIER, CLEAR TO SEND, or SEC REC DATA signals from the data set change states.

The DATASET INT flip-flop (drawing DL-7) is direct set by the output of one of four series of gates; each series of gates is tied to one of four signals from the data set. The first series of gates is qualified by a RING signal from the data set. Note that the initial gate has a differentiating circuit connected in such a way that the gate is qualified only when the RING signal changes from 0 to 1. The remaining three series of gates function similarly except that a delay circuit is connected in such a way that the input gate is qualified on either a 0-to-1 or 1-to-0 transition of the input signal. The three data set signals to these three series of gates are: CARRIER, CLEAR TO SEND, and SEC REC DATA.

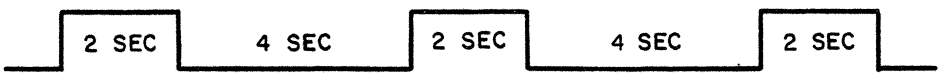
When the DATASET INT flip-flop is set, it produces a DATASET INT H signal, which is applied to the interrupt control logic (Paragraph 3.3.6.2). This signal is also applied to a bus driver for BUS D15 L (drawing DL-2) so that the status of the bit can be read by the program.

The DATASET INT flip-flop is cleared whenever the RCSR is read because of the RCSR TO BUS signal at the clock input. Because the flip-flop is cleared when it is read, bit 15 is, in effect, a read once bit. The flip-flop can also be cleared by an initialize (BINIT) signal.

Data Set Status Bits (14, 13, 12, and 10) – These four bits indicate the status of the data set. All four bits (RING, CLEAR TO SEND, CARRIER, and SEC REC DATA) operate in a similar manner and, when set, set the DATASET INT bit as described.

The RING bit indicates that a ringing signal is being received from the data set. The RING signal from the data set qualifies a series of gates (drawing DL-7) whenever it changes from 0 to 1. The output of the gates direct sets the DATASET INT flip-flop and is also applied to a bus driver for BUS D14 L (drawing DL-2) so that the status of the bit can be monitored by the program.

Note that the RING signal is not a level but an EIA control signal with the cycle time as shown below:



The remaining three data set signals operate similarly except that the related gates are qualified when the signal from the data set changes from 0 to 1 or from 1 to 0. Qualifying the gates sets the DATASET INT flip-flop and applies the appropriate signal to a related bus driver for reading by the program.

The CLR TO SEND bit (bit 13) is activated by the CLEAR TO SEND signal from the data set. When the related gates are qualified, the bit is set to indicate an ON condition; when not qualified, the bit is clear to indicate an OFF condition.

The CAR DET bit (bit 12) is activated by the CARRIER signal from the data set and the related gates are qualified (bit set) when the data carrier is received. When the gates are not qualified (bit clear), it indicates that the data set has either completed the current transmission or that an error condition exists in the data set.

The SEC REC bit (bit 10) is activated by the SEC REC DATA signal from the data set to provide a receive capability for the reverse channel of a remote station. When the related gates are qualified (bit set), it indicates a space (+6V).

Receiver Done (07) – The receiver done (RCVR DONE) flag indicates that a full character has been received. This bit, when set, clears the receiver active (RCVR ACT) flag and initiates an interrupt sequence, provided the associated interrupt enable bit (RCVR INT ENB, bit 06) is also set.

Once an entire character has been received and is stored in the UART holding register, the UART issues a received data available (R DONE) signal (drawing DL-4) which is inverted and fed to the direct clear input of the RCVR ACT flip-flop to clear it, thereby indicating that the receiver is no longer in use and is capable of receiving a new character.

The output of the inverter passes through another inverter to become RCVR DONE H. This signal is ANDed with RCVR INT ENB (1) H, which is true if bit 06 is set, to produce the RCVR INT H signal that indicates an interrupt sequence as described in Paragraph 3.3.6.2. The RCVR DONE H signal is also ANDed with RCSR TO BUS H (drawing DL-2) so that the status of the RCVR DONE bit can be read by the program from bus data line BUS D07.

The RCVR DONE flag can be cleared by the occurrence of one of two conditions. Whenever the reader buffer (RBUF) is addressed, indicating that a new character is to be loaded into the receiver, SEL 2 L is true and enables an OR gate (E31 on DL-4). The OR gate output resets DL-4 RCVR DONE H.

If the reader enable (RDR ENB) flip-flop is set, indicating that the tape reader in a Teletype unit is being advanced, then the 0 side is low and passes through the same OR gate to reset RCVR DONE.

Receiver Interrupt Enable (06) – The receiver interrupt enable bit (RCVR INT ENB) permits an interrupt sequence to be initiated, when the RCVR DONE bit sets, to indicate that a character has been received and is ready for transfer to the Unibus. This bit is set by using the BUS TO RCSR H signal as a load pulse to load a 1 from bus line BD06 H into the RCVR INT ENB flip-flop (drawing DL-4). Note that this flip-flop is shown on the drawing as a 74175 IC chip. This chip is basically four D-type flip-flops with common clock and clear inputs.

The output of the flip-flop, RCVR INT ENB (1) H, is applied to one leg of a 2-input AND gate. The other input to this AND gate is the RCVR DONE H signal, which is produced when the receiver has stored a full character of data. When both inputs to the AND gate are true, the RCVR INT H signal is produced and applied to the interrupt control logic (Paragraph 3.3.6.2) to initiate the interrupt sequence.

The RCVR INT ENB (1) H signal is also ANDed with RCSR TO BUS H so that the program can read the status of this bit position from bus data line BUS D06.

The RCVR INT ENB flip-flop is cleared by BINIT L.

Data Set Interrupt Enable (05) – The data set interrupt enable bit (DATASET INT ENB) permits an interrupt sequence to be initiated when the DATASET INT bit sets, indicating that the data set is interrupting the program. This bit is set by using the BUS TO RCSR H signal as a load pulse to load a 1 from bus line BUS D05 H into the DATASET INT flip-flop (drawing DL-4). This flip-flop is part of a 74175 IC chip. The chip contains four D-type flip-flops with common clock and clear inputs.

The DATASET INT ENB (1) H output of the flip-flop is applied to one leg of a 2-input AND gate. The other input to this gate is the DATASET INT H signal, which is produced when the dataset attempts to interrupt the program. When both inputs to the gate are true, the RCVR INT H signal is produced and applied to the interrupt control logic (Paragraph 3.3.6.2) to initiate the interrupt request. Generation of DATASET INT was described above.

The DATASET INT ENB (1) H signal is also ANDed with RCSR TO BUS H (drawing DL-2) so that the program can read the status of this bit position from bus data line BUS D05.

The DATASET INT ENB flip-flop is cleared by BINIT L.

Secondary Transmit (03) – The secondary transmit (SEC XMIT) bit, which is also referred to as supervisory transmitted data, provides a transmit capability for a reverse channel of a remote station.

The SEC XMIT bit is set by using the BUS TO RCSR H signal as a load pulse to load a 1 from bus line BD03 H into the SEC XMIT flip-flop (drawing DL-4).

The SEC XMIT (1) output of the flip-flop is applied to an EIA driver (drawing DL-7), which provides the +6V level required by the data set. This 6V level is connected to pin FF of the Berg connector (EIA SEC TRANSMIT DATA).

The SEC XMIT (1) output of the flip-flop is also ANDed with RCSR TO BUS H (drawing DL-2) so that the program can read the status of this bit position from bus data line BUS D03.

The SEC XMIT flip-flop is cleared by BINIT L.

Request to Send (02) – The request to send (REQ TO SEND) bit is a control bit for the data set and is required for transmission.

The REQ TO SEND bit is set by using the BUS TO RCSR H signal as a load pulse to load a 1 from bus line BD02 H into the REQ TO SEND flip-flop (drawing DL-4).

The REQ TO SEND (1) output of the flip-flop is applied to an EIA driver (drawing DL-7), which provides the +6V and -6V levels required by the data set. The 6V output of the EIA driver is connected either to pin V of the Berg connector (EIA REQ TO SEND) or to pin C (EIA FORCE BUSY), depending on whether jumper J1 or J2 is installed in the module. Normally, jumper J1 is connected to provide an EIA REQ TO SEND level. However, on certain modems, an EIA FORCE BUSY signal is sometimes required. In this case, jumper J2 is installed. Note that either J1 or J2 is present, but never both.

The REQ TO SEND (1) output of the flip-flop is also ANDed with RCSR TO BUS H (drawing DL-2) so that the program can read the status of this bit position from bus data line BUS D02.

The REQ TO SEND flip-flop is cleared by BINIT L.

Data Terminal Ready (01) – The data terminal ready (DATA TERMINAL READY) bit is a control bit for the data set and permits the interface to be connected to (bit set) or disconnected from (bit clear) the data set communication channel.

The DATA TERMINAL READY bit is set or cleared by using the BUS TO RCSR H signal as a load pulse to load either a 1 or 0 from bus line BUS D01 into the DATA TERMINAL READY flip-flop (drawing DL-4). If a 0 is loaded, the flip-flop is cleared, and the interface is disconnected from the data set communication channel.

If a 1 is loaded into the flip-flop, the flip-flop is set and produces DATA TERMINAL READY (1), which is applied to an EIA driver (drawing DL-7) that provides the +6V level required by the data set. This level (EIA DATA TERMINAL READY) is fed through Berg connector pin DD to the data set, thereby establishing a data communication channel between the data set and the DL11-E Interface.

The DATA TERMINAL READY (1) output of the flip-flop is also ANDed with RCSR TO BUS H (drawing DL-2) so that the program can read the status of this bit position from bus data line BUS D01.

NOTE

The BINIT L signal has no effect on the DATA TERMINAL READY flip-flop. This flip-flop can only be cleared by the program by loading a 0 into bit position 01. Therefore, the DATA TERMINAL READY flip-flop is not cleared when the START key is pressed, a RESET instruction is issued, or a power-up condition occurs.

Reader Enable (00) – The reader enable (RDR ENB) bit, when set, advances the paper tape reader in ASR Teletype units and is available on all DL11 options; however, the DL11-E is not connected to the 20-mA output circuit. The BD00 H signal, which is derived from receiving BUS D00 L, is applied to the data input of the RDR ENB flip-flop (drawing DL-4); the clock input receives the loading signal, BUS TO RCSR H. When the flip-flop is set, the RDR ENB (1) H output is applied to pin PP of the Berg connector (drawing DL-3) for application to the Teletype unit. The 0 side of the flip-flop, which is now low, is gated through an OR gate (drawing DL-4) to produce RESET DATA AVAILABLE L, which resets the RCSR DONE flag as previously described.

The RDR ENB bit is a write only bit; it is not used in the GT40.

The serial input data (SI H) from the Teletype is fed to a 4-bit shift register (IC 8271) as shown on drawing DL-4. The four output lines of this shift register (which is referred to as the "Start bit detector") are connected to a series of gates that are qualified when the Start bit enters the register. Actually, the lines are not qualified until the middle of the Start bit enters the register. This ensures sufficient time to guarantee a valid Start bit. When qualified, the gates produce RESET RDR ENB L, which direct clears the RDR ENB flip-flop.

The RESET RDR ENB L signal is also applied through an inverter to the RCVR ACT flip-flop, thereby setting it to indicate that the interface is now receiving data and the receiver logic circuits are in use.

The RDR ENB flip-flop can also be cleared by BINIT L.

Receiver Buffer Register (RBUF)

The receiver buffer (RBUF), Figure 3-56, is an 8-bit read only register in the UART. Serial information is converted to parallel data by the UART and then gated to the Unibus. The RBUF consists of gating logic rather than a flip-flop register; therefore, the data output lines from the UART must be held until read onto the bus. Because the UART is double-buffered, data on these output lines is valid until the next character is received and assembled. The RBUF is read by a DATI sequence and the data is transmitted to the Unibus for transfer to the processor, memory, or some other PDP-11 device.

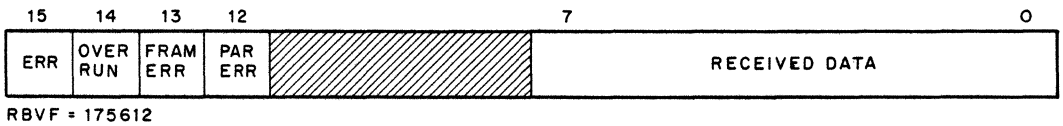


Figure 3-56 Receiver Buffer Register (RBF), Bit Assignments

The low order byte portion of the register is only used for holding data. If, however, a variable data format is used, the buffer is justified into the least significant bit positions. This justification is performed by the UART. The data loaded into the buffer is coded so that binary 0s correspond to spaces and binary 1s correspond to marks (or holes).

The four most significant bits in the high order byte portion of the register are used for error indications.

The four error bits and the data portion of the receiver buffer register are covered separately in the following paragraphs.

Receiver Error Bits – The high order byte of the RBUF contains four error bits that set to indicate improper receiver operation.

Three of the four error bits are generated by the UART as follows:

a. OR ERROR (overrun error, bit 14) – Indicates that R DONE was not reset (previously received character was not read) prior to receiving a new character. When this condition exists, the UART generates an OR ERR H signal.

b. FR ERR (framing error, bit 13) – Indicates that a framing error is present because the character read had no valid Stop bit. When this condition exists, the UART generates an FR ERR H signal.

c. P ERR (parity error, bit 12) – Indicates that the parity received does not agree with the expected parity. If parity has been selected and this condition exists, the UART generates a P ERR H signal.

Bit 15, which is the error (ERR) bit, is the Inclusive-OR of the OR ERR, FR ERR, and P ERR bits. Whenever one of these errors occurs, the appropriate signal from the UART (OR ERR H, FR ERR H, or P ERR H) passes through an inverter and qualifies an OR gate (drawing DL-2). The output of the OR gate is ERROR H. Each of the four error signals (ERROR H, OR ERR H, FR ERR H, and P ERR H) qualifies one leg of an associated 2-input AND gate. The other leg is qualified by RBUF TO BUS L, which is true when the RBUF is addressed for reading. The output of each AND gate is tied to an associated bus data line (BUS D15, BUS D14, BUS D13, and BUS D12) so that the status of each error bit can be monitored by the program.

It should be noted that none of the error bits is tied to the interrupt logic. Therefore, a receiver error does not cause the program to be interrupted for a branch to a handling routine. However, these flags are updated each time a character is received, at which point an interrupt may occur by means of R DONE.

The initialize signal (BINIT) may have an effect on these bit positions depending on the UART used. A bit is cleared by clearing the error-producing condition. When the next character is received by the UART, the error bits are updated and the new status is available when the RBUF is read.

Receiver Data Bits – The RBUF is not a flip-flop register; it consists simply of gates that strobe data from the output lines of the UART to the Unibus. The UART receives the incoming serial data from the external device, converts it to parallel data, and places it on eight parallel output lines. Each of these lines (RD0 through RD7) is fed to one leg of an AND gate as shown on drawing DL-2. When the receiver buffer is addressed for reading (RBUF TO BUS H is true), the levels on these lines are gated through to bus data lines BUS D00 through BUS D07.

Figure 3-57 is a simplified diagram of both receiver and transmitter gating logic showing a single bit position. When the receiver gating is used, the output of the UART is gated through to the Unibus. When the transmitter is used, data from the Unibus is gated through to the transmitter inputs of the UART.

The receiver buffer can only be read by the program; it is loaded by the UART. Note that the initialize signal (BINIT) has no effect on this register.

Transmitter Status Register (XCSR)

The Transmitter Status Register (XCSR), Figure 3-58, consists of control and status monitoring bits for the transmitter portion of the DL11 Interface.

Two bits are associated with transmitter operation: a transmitter ready flag to indicate that the transmitter buffer can be loaded, and an interrupt enable to allow the transmitter to initiate an interrupt sequence. Both of these bits are described in subsequent paragraphs.

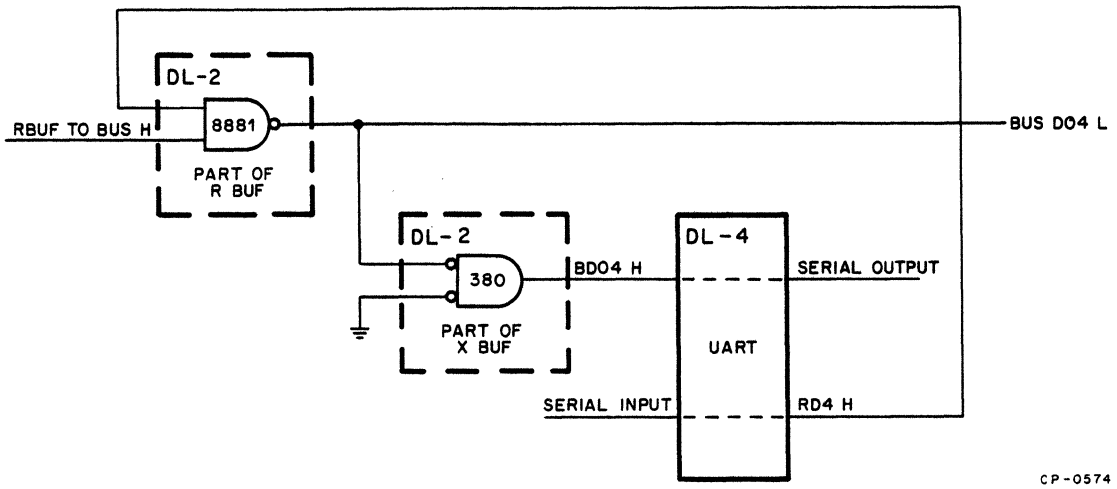


Figure 3-57 RBUF and XBUF Gating Logic, Simplified Diagram
(One Bit Position)

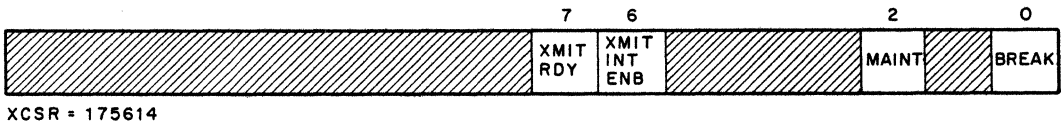


Figure 3-58 Transmitter Status Register (XCSR), Bit Assignments

A maintenance (MAINT) bit is also included so that a closed loop test of DL11 Interface operation can be performed. The maintenance function is covered in detail in Paragraph 3.3.6.8.

A BREAK bit (bit 00) is available to permit transmission of a continuous space to the external device. This logic is described in Paragraph 3.3.6.9.

Transmitter Ready (07) – The transmitter ready (XMIT RDY) flag indicates that the XBUF is ready to accept another character from the Unibus for transfer to the external device. This bit, when set, initiates an interrupt sequence, provided the associated interrupt enable bit (XMIT INT ENB, bit 06) is also set.

This bit is controlled by the XRDY output of the UART, which indicates that the transmitter buffer is empty. It is set by the initialize signal (BINIT) to indicate that the data bits' holding register within the UART may be loaded with another character. It is also set whenever the holding register is empty. Once XBUF loading begins, this bit is cleared. The XRDY output of the UART is gated to produce the XMIT READY H flag.

As shown on drawing DL-4, the XMIT READY H signal is ANDed with XMIT INT ENB (1) H, which is true if bit 06 is set, to produce the XMIT INT H signal that initiates an interrupt sequence as described in Paragraph 3.3.6.2. The interrupt sequence allows the program to branch to a handling routine for loading a character for transmission to the external device.

The XMIT READY H signal is also ANDed with XCSR TO BUS H (drawing DL-2) so that the status of the XMIT READY flag can be read by the program from bus data line BUS D07.

Transmitter Interrupt Enable (06) – The transmitter interrupt enable bit (XMIT INT ENB) permits an interrupt sequence to be initiated when the XMIT RDY bit sets, to indicate that the XBUF can accept another character from the Unibus. This bit is set by using the BUS TO XCSR H signal as a load pulse to load a 1 from bus line BD06 H into the XMIT INT ENB flip-flop (drawing DL-4).

The output of the flip-flop, XMIT INT ENB (1) H, is applied to one leg of a 2-input AND gate. The other input to this AND gate is the XMIT READY H signal, which is produced when the XBUF is clear and capable of receiving a character from the bus. When both inputs to the gate are true, the XMIT INT H signal is produced and is applied to the interrupt control logic (Paragraph 3.3.6.2) to initiate the interrupt sequence.

As shown on drawing DL-2, the XMIT INT ENB (1) H signal is also ANDed with XCSR TO BUS H so that the program can read the status of this bit position from bus data line BUS D06.

The XMIT INT ENB flip-flop is cleared by BINIT L.

Transmitter Buffer Register (XBUF)

The Transmitter Buffer (XBUF) is an 8-bit write-only register (Figure 3-59), that receives the parallel character from the Unibus and loads it into the UART for serial conversion and transmission.

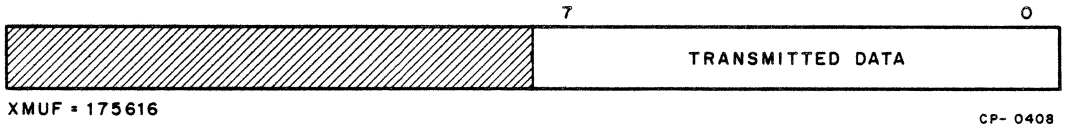


Figure 3-59 Transmitter Buffer Register (XBUF), Bit Assignments

The DL11-E can function with a variable code format of less than eight data bits. In this case, the data character must be justified into the least significant bit positions by the program. Bit positions within the UART itself are enabled or disabled according to the format code employed by a specific option. Thus, for example, if a 5-bit code format is used, bit positions 5, 6, and 7 are disabled in the format. If the program does not justify the character and it is loaded into the most significant bit positions, data loaded into bits 5, 6, and 7 would be lost.

When the interface is initialized, the XMIT RDY flag is set to indicate that the XBUF can be loaded. When the buffer is loaded with the first character, the flag clears and then sets again within a fraction of a bit time. A second character can then be loaded because the UART transmitter section is double-buffered. When the second character is loaded, the flag clears again but this time remains clear for nearly a full character time.

The XBUF (drawing DL-2) is not a flip-flop register but consists simply of a series of gates that strobe data from the Unibus lines to the input lines of the UART. Data transfer is accomplished by a DATO or DATOB bus cycle.

The character to be transmitted to the device is loaded onto bus data lines BUS D07 through BUS D00 and gated to the UART input lines as BD07 through BD00. Once on the input lines, the data is strobed into the UART by the DATA STROBE L signal, which is derived from the BUS TO XBUF signal that occurs when the transmitter buffer is addressed for loading.

Figure 3-57 is a simplified diagram of both receiver and transmitter gating logic showing a single bit position.

XBUF loading is such that a logic 1 causes a mark (or hole) to be transmitted and a logic 0 causes a space.

The UART also generates two signals associated with XBUF operation. An XRDY (indicating XBUF is empty) signal is generated when the UART can be loaded with another character. This signal is the XMIT RDY flag described previously. The second signal is EOC (end of character), which goes high after a full character has been transmitted to the device. It is used to generate the number of Stop bits required by a specific option and is described more fully in Paragraph 3.3.6.7.

3.3.6.4 Transmitter Control Logic – The transmitter control logic provides the necessary input, control, and output logic for the UART when it is used to convert parallel data from the Unibus to the serial data required for output. This logic may be divided into three functional areas: control and input, format selection, and data output.

The control and input logic for the transmitter portion of the UART consists of both input and output control signals, a clock frequency, and an input data character. These signals are listed in Table 3-31 along with a reference to the paragraph containing a detailed description of the logic.

Table 3-31
Transmitter Control and Input Logic

Signal Mnemonic	Signal Name	Paragraph Number	Description
XRDY	Transmitter Ready	3.3.6.3	The XMIT RDY flag that indicates the XBUF is empty and may be loaded with another character from the Unibus.
LD XD	Load Transmitter Data	3.3.6.3	The signal that strobes data from the buffer into the UART when the XBUF is addressed for loading.
EOC	End of Character	3.3.6.6	Signals that a character has been transmitted.
XCLK	Transmitter Clock Pulse	3.3.6.7	Provides the required transmitter clock rate. This rate is 16 times the selected baud rate.
XD0 – XD7	Data Buffer	3.3.6.3	Represents the character (five to eight data bits) loaded from the Unibus into the UART.

The format selection logic basically consists of jumpers that are arranged to select the number of data bits, Stop bits, and type of parity. Format selection is covered in Table 3-24.

The transmitter output logic is described in the following paragraphs.

Once the UART has converted the parallel character from the Unibus (UART operation is described in Paragraph 3.3.6.6), it shifts the character out, one bit at a time, onto the serial output (SO) line. The first bit shifted out is the Start bit, followed by the Data bits (LSB first), then the Parity bit (if selected), and finally, the Stop bits. The output of the line passes through a flip-flop to become SERIAL OUT H. This flip-flop is used to compensate for the different number of Stop bits that can be selected (drawing DL-4).

SERIAL OUT H passes through an EIA level converter (drawing DL-7) to pin F of the Berg connector. The signal is also applied to the MAINT multiplexer (drawing DL-3) for use during the maintenance mode as described in Paragraph 3.3.6.8.

3.3.6.5 Receiver Control Logic – The receiver control logic provides the necessary input, output, and control logic for the UART when it is used to convert serial data to the parallel data required by the Unibus. This logic may be divided into three functional areas: status and control, format selection, and data input.

The status and control portion of the logic consists of both input control and output status signals, a clock frequency, and an output data character. These signals are listed in Table 3-32, along with a reference to the paragraph containing a detailed description of the logic.

Table 3-32
Receiver Status and Control Logic

Signal Mnemonic	Signal Name	Paragraph Number	Description
R DONE	Receiver Done	3.3.6.3	The R DONE flag indicates a full character has been received from the device and is ready for transfer to the Unibus.
P ERR	Parity Error	3.3.6.3	A status signal indicating that the received character has a parity error. Can be read by the program.
FR ERR	Framing Error	3.3.6.3	A status signal indicating that the received character has no valid Stop code. Can be read by the program.
OR ERR	Overrun Error	3.3.6.3	A status signal indicating that the character was not read prior to receiving another character from the device. Can be read by the program.
R CLK	Receiver Clock Pulse	3.3.6.7	Provides the required receiver clock rate. This rate is 16 times the selected baud rate.
RD7 – RD0	Receiver Data Buffer	3.3.6.3	Represent the character (five to eight data bits) transferred from the UART to the Unibus after serial-to-parallel conversion.

The format selection logic is basically the same as that used for the transmitter control and is described in Table 3-24.

The transmitter input logic is described in the following paragraphs.

Regardless of the device used, the serial input from the device is loaded into the DL11 one bit at a time, beginning with the Start bit, then the Data bits (LSB first), the Parity bit (if used), and the Stop bits.

The serial input, referred to as EIA RECEIVE DATA (drawing DL-7), enters pin J and passes through an EIA level converter to pin M of the Berg connector. Because of the cabling, pin M is connected to pin E (TTL input) and the data follows the same path as before.

3.3.6.6 Universal Asynchronous Receiver/Transmitter (UART) – The Universal Asynchronous Receiver/Transmitter (UART) is an LSI subsystem that accepts binary characters from either a terminal device or a computer and receives or transmits these characters, which append control and error detecting bits. In order to make this subsystem universal, the baud rate, bits per word, parity mode, and number of Stop bits are selected by external logic circuits. Figure 3-60 is a simplified block diagram showing the overall UART configuration.

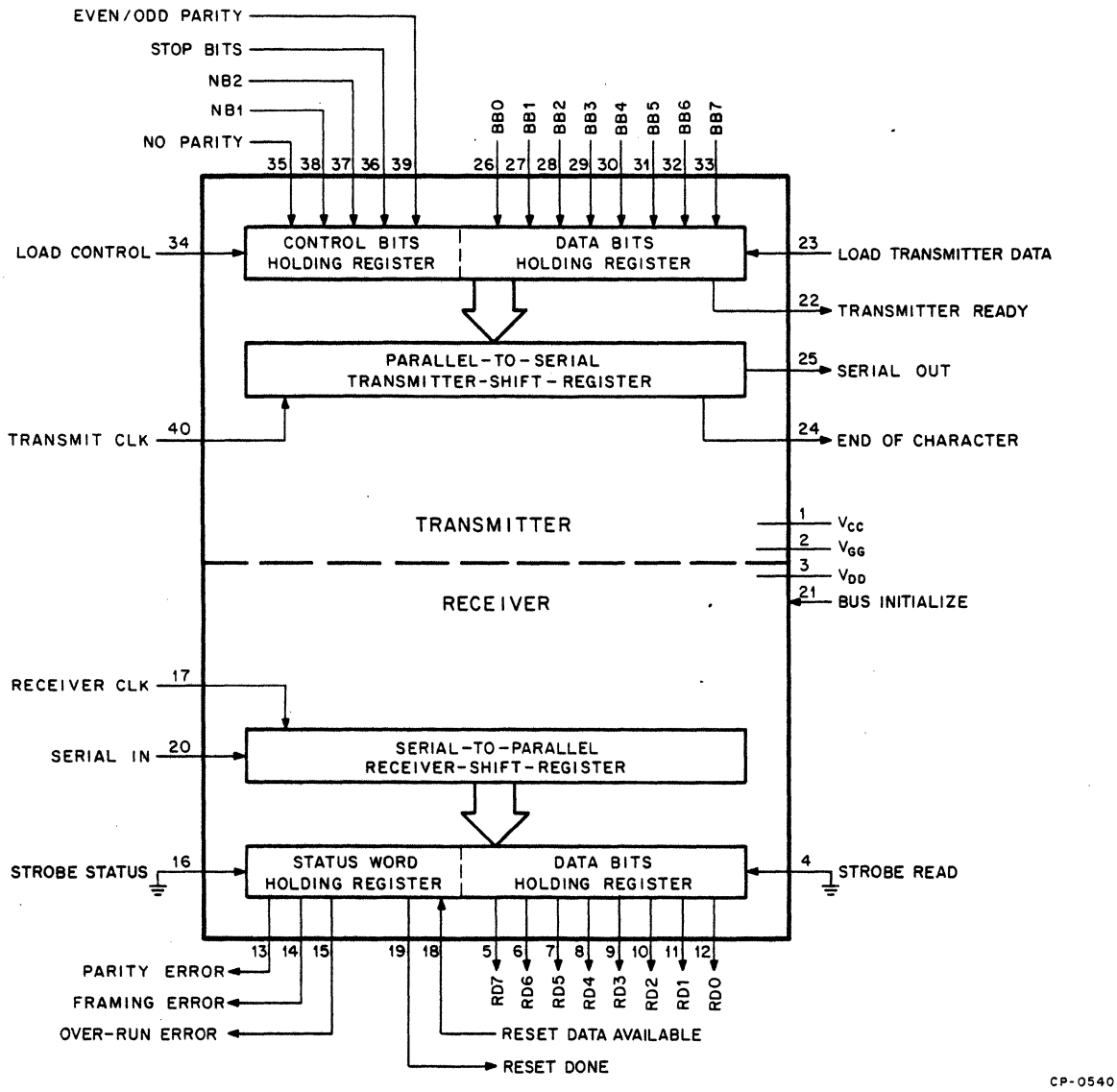


Figure 3-60 Universal Asynchronous Receiver/Transmitter (UART)

The UART is a full duplex receiver/transmitter. The receiver section accepts asynchronous, serial, binary characters and converts them to a parallel format for transmission to the Unibus. The transmitter section accepts parallel, binary characters from the bus and converts them to a serial asynchronous output, with Start and Stop bits added.

All UART characters contain a Start bit, five to eight Data bits, one, one and a half, or two Stop bits, and a Parity bit which may be odd, even, or turned off. The Stop bits are opposite in polarity to the Start bit. This is the maximum format that can be used (Figure 3-49).

Both the receiver and transmitter are double buffered. The UART internally synchronizes the Start bit with the clock input to ensure a full 16-element (clock periods) Start bit independent of the time of data loading. Transmitter distortion (assuming perfect clock input) is less than 3 percent on any bit up to 10 kbaud. The receiver strobes the input bit within ±8 percent of the theoretical center of the bit. The receiver also rejects any Start bit that lasts less than one-half of a bit time.

The UART input and output lines are shown on drawing DL-4. A description of the receiver is given below, followed by a description of the transmitter. Note that in the following discussions, the mnemonic and pin number of UART input and output lines are given in parentheses.

Receiver Operation

A block diagram of the UART receiver is shown in Figure 3-61. When the receiver is in the idle state, it samples the serial input line (SERIAL IN, pin 20) at the selected clock edges (R CLK, pin 17) after the first mark-to-space transition of the serial input line. As indicated in Figure 3-49, the state of the input line is tested 8 clock pulses after the mark-to-space transition and every 16 clock pulses thereafter. If the first sample is a mark (high), the receiver returns to the idle state and is ready to detect another mark-to-space transition. If, however, the first sample is a space (low), then the receiver enters the data entry state.

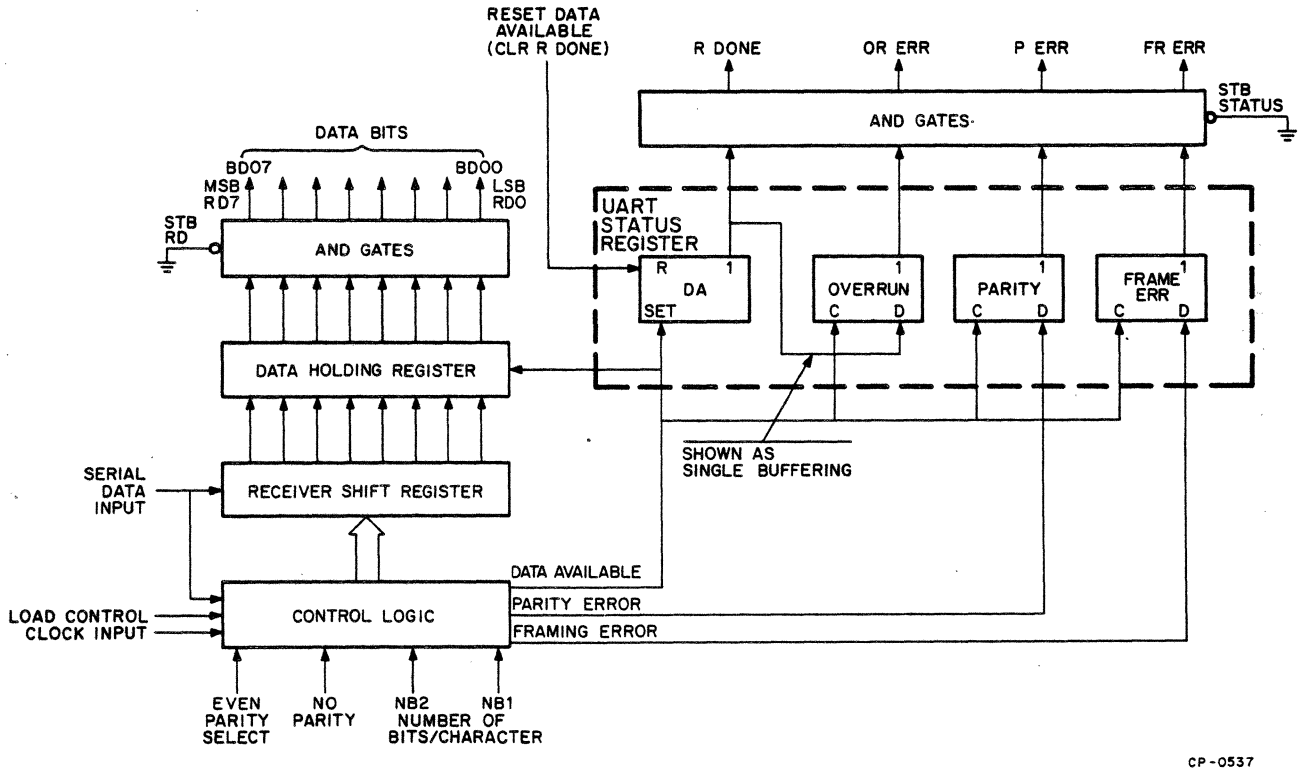


Figure 3-61 UART Receiver, Block Diagram

The load control input is not connected (LDC, pin 34) to an external signal or voltage. This enables entry of the control bits (NB1, NB2, NP, EPS, and 2SB) into the control bits holding register.

If the receiver control logic has not been conditioned to the no parity state (jumper in place = a low in pin 35), then the receiver checks the parity of the data bits, plus the parity bit following the data bits, and compares it with the parity sense on the parity select line (pin 39). If the parity sense of the received character differs from the parity of the UART control logic, then the receive parity error line (P ERR, pin 13) goes high and causes the P ERR bit in the RBUF to set.

If the receiver control logic has been conditioned to the no parity state (no jumper in place = a high on pin 35), then the receiver takes no action with respect to parity and maintains the parity error line (P ERR, pin 13) in the false (low) state. When the control logic senses a parity error, it generates a P ERR signal. The DATA AVAILABLE signal updates the parity error indicator.

The receiver samples the first Stop bit that occurs either after the Parity bit, or after the data bits if no parity is selected. If a valid (high) Stop bit exists, no further action is taken. If, however, the Stop bit is false (low), indicating an invalid Stop code, then the UART control logic provides a framing error indication (a high on FR ERR, pin 13). The status of the framing error bit can also be read from the RBUF.

Because the serial input from the external device is shifted into the UART a bit at a time (SI, pin 20), occurrence of a Stop code indicates that the entire data character has been received and shifted into the receiver shift register. After the Stop bit has been sampled, the receiver control logic parallel transfers the contents of the shift register into the receiver data holding register and then sets the data available (R DONE) flag.

The DATA AVAILABLE signal also functions as the clock input to the FRAME ERR, PARITY, and OVERRUN flip-flops in the UART status register. At this point, the DA flip-flop is set, the OVERRUN flip-flop is a clear bit and has a high on the data input because of the output from the DA flip-flop, and the PARITY and FRAME ERR flip-flops are set or cleared depending on the signal (true or false) strobed in from the control logic.

An OVERRUN condition indicates that another data character is being sent to the UART before the previous character has been transferred to the DL11-E RBUF. If the DA flip-flop is set, indicating a character is stored in the holding register, and the UART control logic attempts to set the DA flip-flop again (indicating a new character has been shifted into the shift register), the DA signal from the control logic provides a clock input to the OVERRUN flip-flop, then sets because the data input is high (DA flip-flop was already set by the previous DA signal).

During normal operation (no OVERRUN condition), the character in the receiver data holding register is strobed onto the Unibus by an RBUF TO BUS H signal (drawing DL-5), which produces SEL 2 L. This signal is applied to the UART reset data available (pin 18) to clear the flip-flop.

Whenever the serial input line goes from a mark (high) to a space (low) and remains at the low level, the receiver shifts in one character, which is all spaces, then sets the FR ERR indicator and waits until the input line goes high (marking) before shifting in another character.

Transmitter Operation

A block diagram of the UART transmitter is shown in Figure 3-62. When the UART transmitter is in the idle state, the serial output line (pin 25) is a mark (high). To transmit data, a parallel character is placed on bus data lines BUS D00 through D07 and strobed into the UART transmitter data buffer (lines connected to pins 26–33) by means of the load transmitter data signal (LD XD L, pin 23). The time between the low-to-high transition of data strobe and the corresponding mark-to-space transition of the serial output line is within one clock cycle (1/16 of a bit time) if the transmitter has been idle. The LD XD L signal is a derivative of BUS TO XBUF (drawing DL-5), which is used to load a character from the Unibus into the XBUF.

After the data has been loaded into the UART data buffer, it is transferred to the transmitter shift register under control of signals from an encoder, which selects the format determined by the control logic. This permits selection of parity or no parity (pin 35), the type of parity (pin 39), the number of Stop bits (pin 36), and the number of Data bits per character (pins 37 and 38).

The transmitter logic converts the parallel character from the Unibus into a serial output that is in a format selected by the control logic.

The clock input to the timing generator (pin 40) is derived from the DL11 clock circuits (Paragraph 3.3.6.7). The other input to the timing generator is the end-of-character (pin 24) signal from the output logic. This line goes high each time a full character (including Stop bits) is transmitted. If this line goes low, it prevents the timing generator from loading another character into the shift register. The line is normally high when data is not being transmitted and goes low at the start of transmission of the next character.

Whenever the transmitter data buffer is loaded while the previous character is being shifted through to the output line, the Start bit of the new character immediately follows the last Stop bit of the previous character.

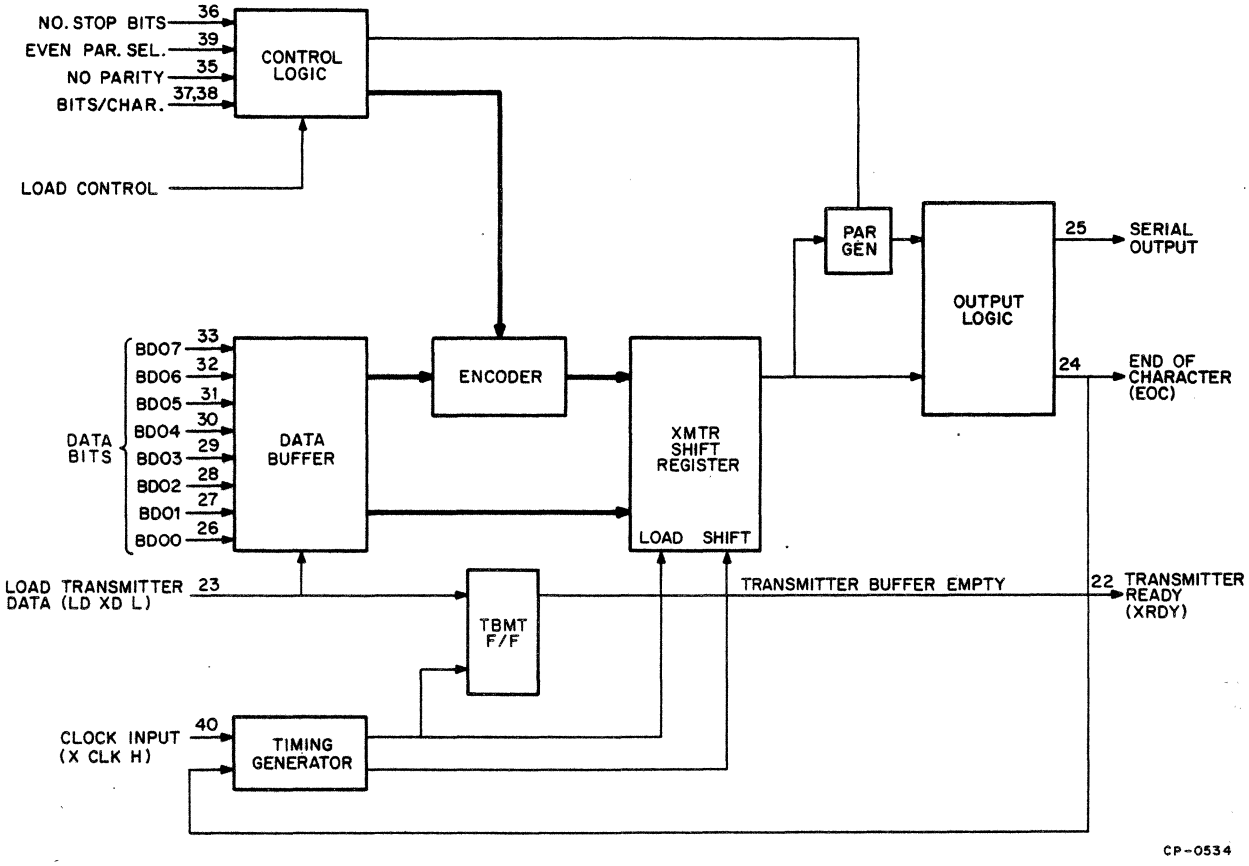


Figure 3-62 UART Transmitter, Block Diagram

The end-of-character signal is applied to a decade counter (drawing DL-4) which the DL11 employs to generate the various Stop codes. This is necessary because the UART generates only 1 or 2 Stop bits but the DL11-E generates 1, 1.5, or 2 Stop bits. Depending on the selection of jumpers J9, J10, and J11 (Table 3-24), the outputs of the decade counter and the XMIT CLK signal are combined to provide the appropriate input to the transmitter clock input at pin 40 of the UART. Note that the end-of-character signal cannot be read by the program.

When LD XD L (pin 23) loads the UART data buffer, the DL11 XBUF is unloaded. Therefore, the LD XD L signal sets the TBMT (transmitter buffer empty) flip-flop to provide a signal that becomes XRDY (transmitter ready). The XRDY signal can be read by the program and indicates that a new character can be loaded in the DL11 XBUF.

3.3.6.7 Clock Logic – The DL11 clock logic (drawing DL-3) provides the clock frequency and, therefore, the baud rates for both the receiver and transmitter sections of the DL11 Interface. The basic frequencies are derived from a single crystal oscillator. Although only one crystal is used, four different crystal types are available from DEC so that the basic frequency range can be selected by simply plugging the appropriate crystal into the M7800 module.

The output of the crystal (Y1) is applied to four frequency divider circuits. A rotary switch taps off various divider outputs to provide selection of one of eight derived frequencies. Two additional switch positions permit application of external clock pulses. There are two rotary switches on the module: one for the receiver, one for the transmitter. Therefore, the receiver can operate at a different baud rate than the transmitter, but both must be within the operating range of the selected crystal.

The specific frequencies selected by the four crystals, the frequencies that can be used with various DL11 options, and the location of the crystal and rotary switches on the module are covered in Table 3-17 and Paragraph 3.3.5. The following paragraphs describe the clock logic. Clock circuits used during the maintenance mode are described in Paragraph 3.3.6.8.

The output frequency of crystal Y1 (drawing DL-3) is applied to four IC chips that function as frequency dividers to provide the eight different frequencies fed to the rotary switches.

Figure 3-63 is a simplified diagram of the frequency divider circuits. The divisor of the circuit is dependent on which IC output line is tapped. For example, four output lines from the 7493 IC provide divide-by-2, divide-by-4, divide-by-8, and divide-by-16 functions. The diagram shows the various divisors, the output frequency, the rotary switch pin to which each frequency is tied, and the baud rate. Note that the clock frequency is 16 times the baud rate. In the example shown in the figure, a 1.152-MHz crystal is used. Any of the other crystals, such as the 4.608-MHz crystal, can also be used. If a different crystal is employed, the resultant output frequencies (and baud rates) are different, but the divider circuits function in an identical manner.

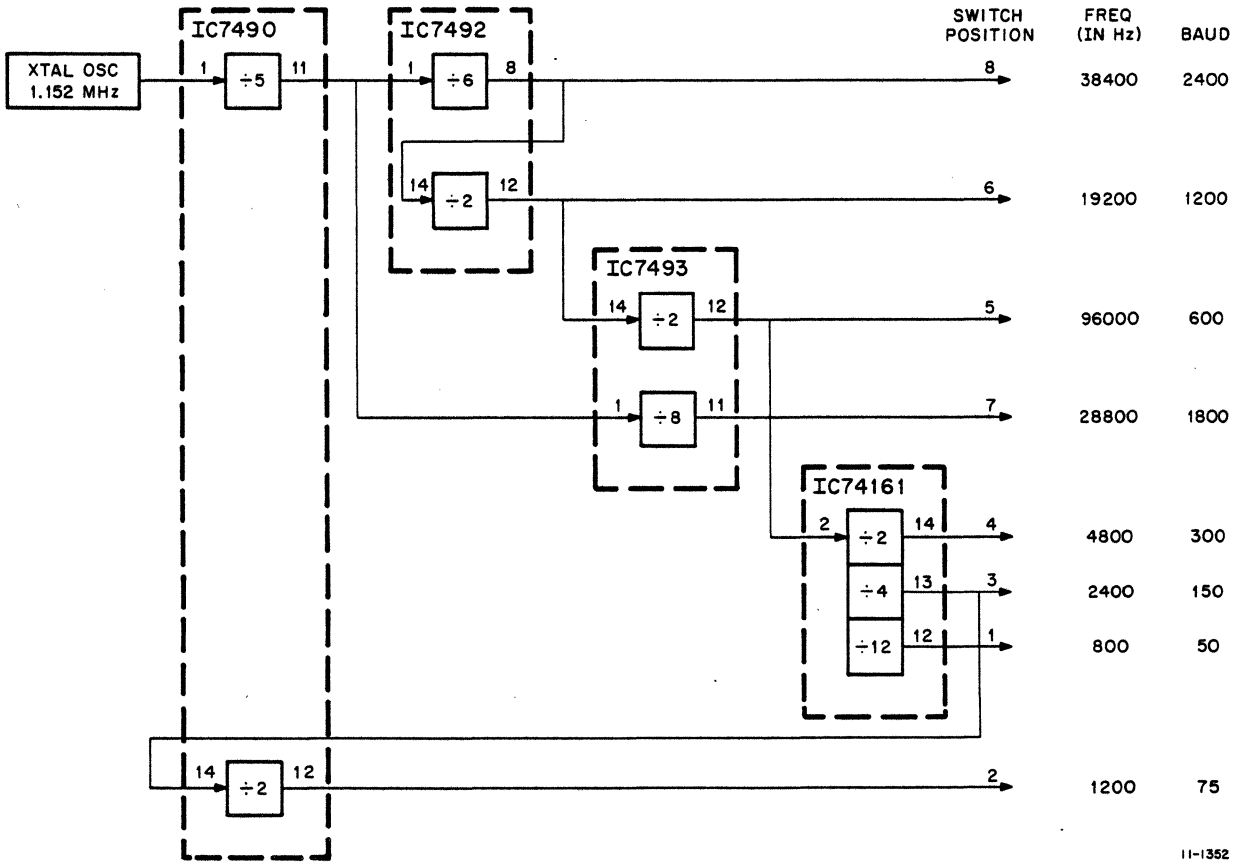


Figure 3-63 Frequency Divider Logic, Simplified Diagram

Note that switch positions 9 and 10 (or 0) are not shown on the figure. Position 9 is used to select an external clock pulse from the Berg connector. In this case, the external clock is applied to pin CC of the Berg connector and serves as a common clock pulse for both the receiver and transmitter.

Switch position 10 is also used for an external clock. However, in this case, the clock pulse is brought in on the back panel wiring and a different pulse can be used for the receiver and for the transmitter. The external transmitter clock is applied to pin DR1; the external receiver clock is applied to pin DS1.

The frequency selected by the transmitter switch is the XMIT CLK H signal, which is used to generate the transmitter clock input (pin 40) of the UART (drawing DL-4).

The frequency selected by the receiver switch is the RCVR CLK H pulse, which is applied to the MAINT multiplexer (drawing DL-3). The output of RCLK H is applied directly to the receiver clock input (pin 17) of the UART. Operation of the UART receiver is described in Paragraph 3.3.6.6.

3.3.6.8 Maintenance Mode Logic – The maintenance mode is used to check operation of the DL11 control logic. Figure 3-64 is a simplified diagram of both the normal and maintenance modes. During normal operation, data from the bus is converted by the receiver and sent to the bus.

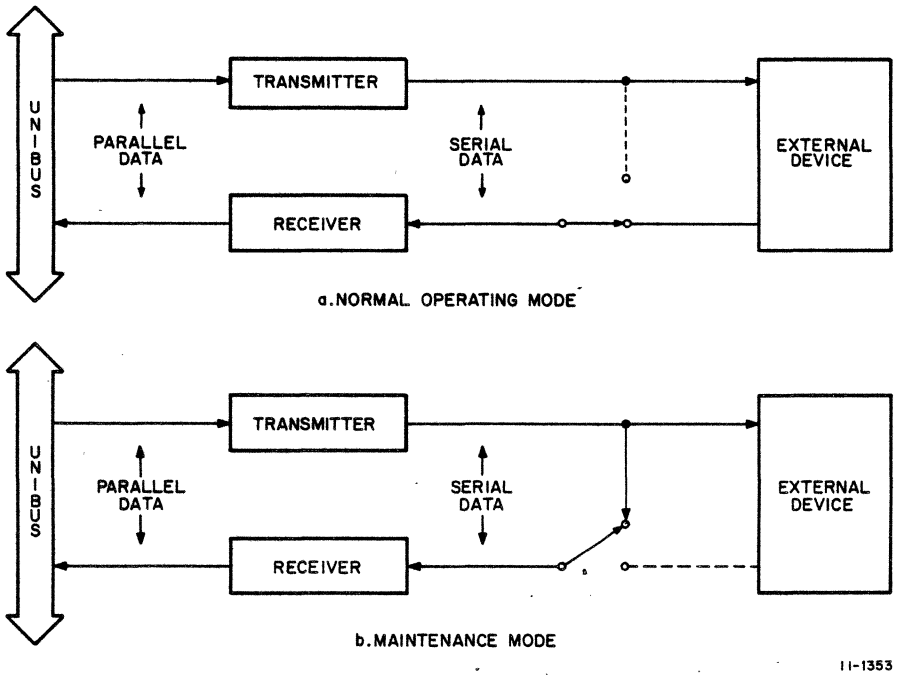


Figure 3-64 Operating Modes

During the maintenance mode, a character is loaded into the XBUF from the Unibus. This parallel character is then converted to a serial output by the UART transmitter section. However, in addition to entering the external device, the serial data is also fed back into the receiver, which converts it back to parallel data and places it on the bus. If the character received by the bus is identical to the character sent out on the bus, then both the transmitter and the receiver are functioning properly.

Before the maintenance loop can be used, the transmitter must be selected for use and the XBUF loaded with a character. The program selects the maintenance mode by setting bit 02 (MAINT bit) in the transmitter status register (XCSR). This sets the MAINT flip-flop in the transmitter logic (drawing DL-4).

The MAINT (1) H output of the flip-flop is used as an enabling level for a 4-line to 1-line multiplexer (IC 74153 on drawing DL-3). A simplified version of this multiplexer is shown in Figure 3-65. Normally, the gates shown enabled by MAINT (1) H in the figure are inhibited and the serial output from the transmitter, as well as the clock signals, are fed to the logic used during the normal operating mode. However, when MAINT (1) H is present, the gates are qualified and perform two basic functions.

The first function is to gate the serial output of the transmitter (SERIAL OUT H) to the serial input line (SI H) of the receiver. The second function is to force the RCVR CLK pulse to be the same as XMIT CLK, regardless of the switch position of RCVR CLK. When MAINT (1) H is present, the gate receiving RCVR CLK H is inhibited and the XMIT CLK H pulse is gated through to the RCLK H line of the receiver. Although not shown in the figure, XMIT CLK H is also applied to the clock line of the transmitter.

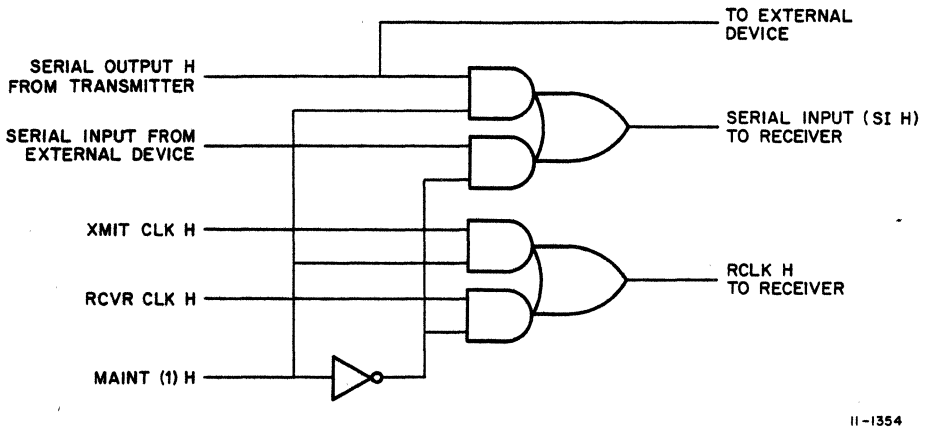


Figure 3-65 Maintenance Logic, Simplified Diagram

Because the receiver logic is activated by a Start bit (regardless of where the Start bit comes from), the receiver is activated as soon as it receives the first input from the transmitter. After the receiver assembles the data, the program can compare the received character with the transmitted character to determine if the DL11 Interface is functioning properly.

3.3.6.9 Break Generation Logic – The break generation logic permits the DL11 Interface to transmit a continuous space to the external device.

When it is desired to transmit a break, the Break bit (bit 00) in the XCSR must be set. This is accomplished by using the BUS TO XCSR H signal as a load pulse to load a 1 (BD00 H) into the BREAK flip-flop (drawing DL-4).

The BREAK (0) H output of the flip-flop, which is low when the flip-flop is set and jumper J5 is in place, is applied to the direct clear input of the SERIAL OUT flip-flop (drawing DL-4). Because the output is a level, it holds the SERIAL OUT flip-flop clear and prevents the UART transmitter output from being sent to the device. In effect, a continual low (space) level is presented on the SERIAL OUT line.

The duration of the break can be timed by the program because the transmitter and XMIT RDY flag continue to function normally; only the transmitter output line is inhibited. For example, the program can continue loading characters into the transmitter and counting the number of characters by monitoring the XMIT RDY flag. At a predetermined count, the program can clear the Break bit and resume normal operation.

Whenever the Break bit is used, a null character (all 0s) should be transmitted before the Break bit is set and immediately after it is cleared. This is necessary because the UART transmitter is double-buffered and it is important to ensure that the previous character has cleared the line.

3.4 LK40 KEYBOARD

3.4.1 Introduction

The LK40 Keyboard is the manual means by which data can be entered into the PDP-11/05 computer. Together with the 375 Light Pen, the LK40 functions as the link between the operator and the GT40 Graphic Display Terminal.

The following paragraphs provide the user with the theory of operation necessary to understand and maintain the LK40 Keyboard.

3.4.2 Keyboard Operation

The LK40 Keyboard can generate 128 ASCII characters (Appendix C). A two-way slide switch, mounted on the keyboard logic board, allows the keyboard to be set for upper/lower case ASCII (128 codes) or upper case ASCII (96 codes). Figure 3-66 shows the major components of the LK40 and their relationship to the PDP-11/05 and VR14; Figure 4-29 shows the interior layout of the device.

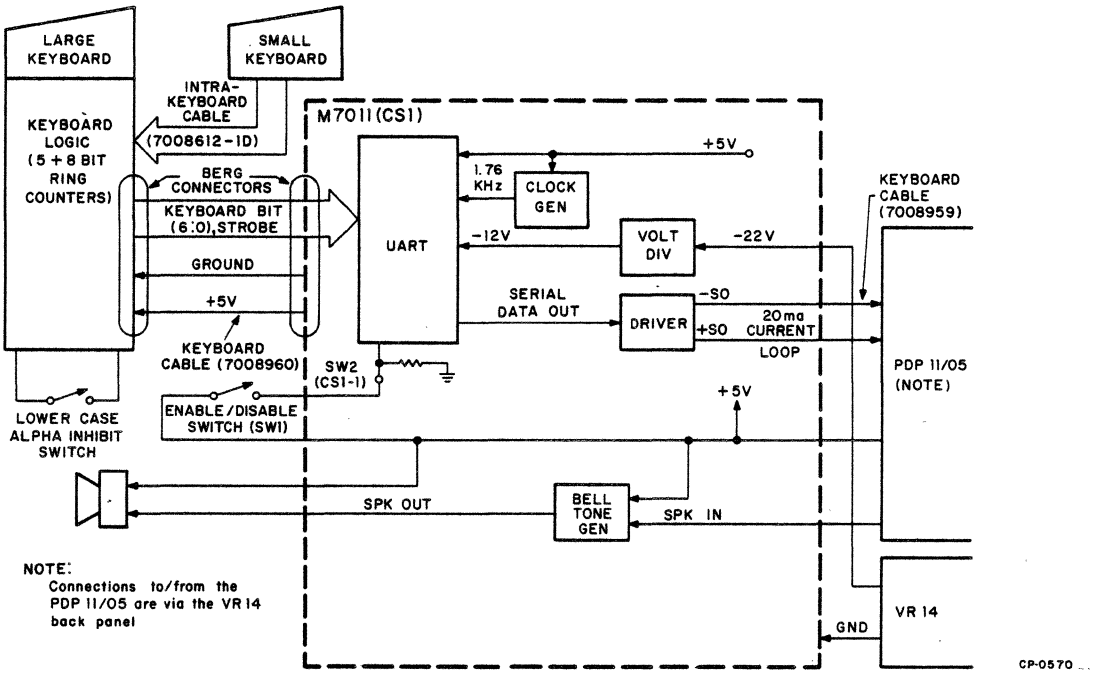


Figure 3-66 LK40 Keyboard, Block Diagram

Each of the 58 major and 8 minor keys has a variable capacitance that is increased when the key is pressed, causing an excitation voltage to be applied to one side of a capacitor and generating base drive for the related transistor amplifier (Figure 3-67 and drawing DCS 5409945-0-1). A sequential scanning technique is employed, using an MOS integrated circuit that consists of an 8-bit and an 11-bit ring counter (to compose an 8 X 11 matrix), and circuitry to sample the conductance of each transistor amplifier (one per key). As the two (8-bit and 11-bit) registers cycle, the 8-bit counter provides a collector voltage to as many as eleven key output amplifiers. Up to eight of the transistor emitters are connected to each of the sensing circuits gated by the 11-bit counter. The two sets of lines that form the 8 X 11 matrix are theoretically capable of sampling up to 88 keys. When an ampliifer is selected, via the 8 X 11 matrix, the clock is stopped; a strobe signal and the applicable ASCII code are output, in parallel, via the keyboard cable (7008960) to the M7011 Serial Transmitter module. This cable is constructed with 40-pin Berg connectors at both ends. Pin assignments (applicable to both connectors) are listed in Table 3-33. LK40 internal connections, including the keyboard cable, are shown on drawing D-UA-LK40-0-0.

NOTE

Old and new versions of the small and the large keyboards cannot be mixed in one installation. Both keyboards must be the older version or both must be the new version. This requirement must be followed when replacing either keyboard. The following part numbers are applicable:

Old Version		
	Small Keyboard	5410224
	Large Keyboard (LK01)	5409945
New Version		
	Small Keyboard	5410613
	Large Keyboard (LK01R)	5410541

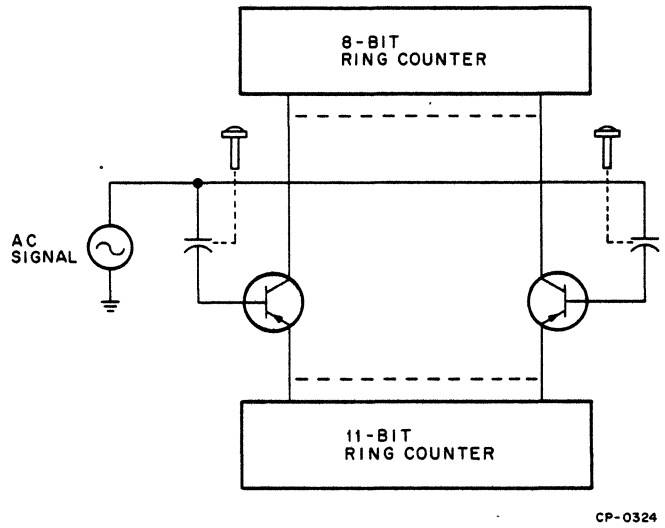


Figure 3-67 LK40 Keyboard, Simplified Diagram

Table 3-33
Berg Connector Pin Assignments (7008960 Keyboard Cable)

Berg Connector Pin*		Signal
Cable Side of Connector	Input/Output	
B	B	Strobe (Load Transmitter Data)
D	D	Keyboard Bit 6 (MSB0)
J	H	Keyboard Bit 5
L	K	Keyboard Bit 4
TT	SS	Keyboard Bit 3
NN	MM	Keyboard Bit 2
RR	PP	Keyboard Bit 1
VV	UU	Keyboard Bit 0
X	W	Ground
Z	Y	+5 Vdc

*The two pins listed for each signal are common.

3.4.3 M7011 Serial Transmitter Module

[redacted] (drawing D-CS-M7011-0-1) accepts the parallel ASCII data from the keyboard logic and serially transmits the same information over a [redacted]. Each serial character transmitted comprises 10 bits: 1 start bit, 7 bits of encoded data, and 2 stop bits. (No parity bit is included; the stop bits immediately follow the data bits.) [redacted]

The M7011 module contains a universal asynchronous receiver/transmitter (UART) that converts parallel data from the keyboard to serial output format, a clock pulse generator, an audio oscillator for the bell signal [redacted] for t[redacted]

3.4.3.1 Universal Asynchronous Receiver/Transmitter (UART) – The UART is a 40-pin metal oxide silicon (MOS) large-scale integrated (LSI) circuit to convert parallel data from the keyboard to serial data for output to the PDP-11/05. The UART used in the M7011 is identical to the UART contained in the DL11 logic. Operation of this IC is described in Paragraph 3.3.6.6. UART pin connections establish the operating parameters; they are listed in Table 3-34.

The UART is compatible with TTL logic on both its input and output terminals. Operation of the UART requires only power (+5 and -12 Vdc), data, a strobe signal to initiate the parallel-to-serial conversion, and a clock pulse train.

3.4.3.2 Clock Circuit – This circuit consists of a 7413 Schmitt trigger and an RC network that functions as a multivibrator. The 1.76-kHz pulse train generated (≅ 568 μs/cycle) is input to the UART at pin 40; it is approximately 16 times the UART transmit baud rate (110).

[redacted]

3.4.3.4 Bell Tone Generator – The LK40 audio tone is produced by a gated multivibrator consisting of a 7413 Schmitt trigger, transistor Q3, and an RC network. The SPK IN input (V1) goes high when a bell command is sensed in the GT40 Display Processor. E2 and Q3 now function as a multivibrator and a 1-kHz signal is generated at the collector of Q3. A speaker, acting as part of the Q3 collector load, converts the electrical square wave to sound (Paragraph 3.2.8.5).

[redacted]

3.4.3.6 Enable/Disable Switch (SW1) – The Enable/Disable switch (SW1), located on the keyboard rear panel, is used to disable the UART by applying +5V to pin 21, the UART clear input. As shown in Figure 3-66, +5V is input to the UART, via terminal SW2 (CS1-1), when the Enable/Disable switch is closed (OFF position). The +5V at pin 21 clears all UART registers and sets the serial output line (pin 25) to a high, the idle (mark) condition. Ground is applied to pin 21, through resistor R11, when SW1 is open (ON position); this enables UART operation.

3.5 VR14 CRT DISPLAY

3.5.1 Introduction

The following paragraphs describe the operation and maintenance of the VR14 CRT Display as an integral component of the GT40 Graphic Display Terminal.

WARNING

Maintenance procedures should be performed by qualified service personnel only.

High voltages are present within the unit and, under certain conditions, are potentially dangerous. All electrical safety precautions must be observed.

Inherent implosion protection is employed in the CRT design; however, the tube may be damaged if it is subjected to rough treatment or dropped while being removed from or installed in the display. Exercise caution during these operations.

Table 3-34
UART Pin Assignments, M7011 Module

Signal/Voltage		Remarks
Pin	Present	
1	+5 Vdc	VCC
2	-12 Vdc	VGG
4	+3 Vdc	Inhibit gates to read output lines RD0–RD7 which are not used.
16	+3 Vdc	Inhibit gating of status bits to output lines.
18	+3 Vdc	Inhibit reset of R DONE which is not used.
20	+3 Vdc	Serial input line (not used) is held high.
21	Ground/+5V	+5V applied via the Enable/Disable Switch, SW1 (closed), resets all registers and sets the serial out line high (mark). Ground (SW1 open) enables UART operation.
23	Serial Out	Serial data output to the 20-mA driver. This line is high when no data is being transmitted.
26	Keyboard Bit 0	7 parallel input lines from the keyboard. (Pin 32 = MSB)
27	Keyboard Bit 1	
28	Keyboard Bit 2	
29	Keyboard Bit 3	
30	Keyboard Bit 4	
31	Keyboard Bit 5	
32	Keyboard Bit 6	
33	+3 Vdc	XD7, not used.
34	+3 Vdc	Enter the control bits into the UART control bits holding register (enable control bits NB1, NB2, 2SB, NP, and EP to function).
35	+3 Vdc	Eliminate the parity bit from the transmitted character. The stop bits will immediately follow the last data bit on transmission.
36	+3 Vdc	Select 2 stop bits.
37	+3 Vdc	Select 7 data bits/character
38	Ground	
39	+3 Vdc	Normally would insert and check parity. However, pin 35 (high) inhibits parity insertion and checking.
40	Transmitter Clock	Clock pulse (1.76 kHz) which is 16 times the baud rate (110).

3.5.2 General Description

The VR14 is a completely self-contained CRT display that provides a 6.75 in. X 9 in. viewing area in a compact 19-in. package. The VR14 requires only analog X and Y position information and intensity signals from the GT40 to generate sharp, bright point-plot displays. Except for the CRT itself, the unit is composed of all solid-state circuits, utilizing high speed magnetic deflection to enhance brightness and resolution.

VR14 construction is modular for easy maintenance. Any subassembly or major component can be replaced in minutes using only a screwdriver.

3.5.3 Specifications (refer also to Paragraph 1.5.4)

Deflection Amplifier

a. Deflection Amplifiers are dc coupled and are capable of sustaining a full screen ac or dc deflection at environmental extremes.

b. Input Specifications

1. Inputs are differential.

2. Differential input impedance, 5 kΩ minimum.

3. Input sensitivity, 500 mV/in. maximum (200 mV/in. with resistor change).

4. Common mode rejection ratio, 40 dB.

5. Maximum operating input, ±6V. (Maximum operating input is the sum of the common mode input and the differential input).

6. Input offset not to exceed ±1/2 peak-to-peak input signal.

7. Maximum nonoperating input, ±50V.

c. Full screen deflection and settling time to within ±1 spot diameter, < 20 μs.

d. Small signal settling time to within 1/2 spot diameter, 1 μs for a 0.1-in. deflection.

e. Small signal linear slew rate, > 0.4 in./1 μs.

f. Velocity error coefficient, 500 ns maximum (Average ramp delay between input and output).

Z Axis Input Signals

a. GM INTENSITY OUT L (Z Input) – This signal, when asserted in the M7013 module, unblanks the CRT by causing the cathode voltage to change from approximately +60V to ground. The duration of GM INTENSITY OUT L, and consequently the unblanked period, is determined by the nature of the display, i.e., point, vector, or character.

b. GM INT 0L, 1L, and 2L – Three negative signals generated in the M7013 module that, together with the Brightness control, generate a voltage of from -80 to 0V on the CRT grid to determine image brightness. The combination of the three intensity levels asserts one of eight possible analog voltages, which, in turn, is ANDed with the output of the Brightness control to generate a grid voltage within the 80V range. Thus, there are eight intensity levels at each of the infinite positions of the Brightness control.

Power

a. All power supplies necessary for operation of the unit are self-contained.

b. Input Requirements

Voltage:	100V ± 10%
	115V ± 10%
	230V ± 10%

Selectable by tap changes.

Frequency:	50 – 60 Hz
Power:	< 500W
Current:	< 5A
Type:	Single Phase

3.5.4 Block Diagram Description

Figure 3-68 is the functional block diagram of the VR14. The X and Y position signals are connected to their respective A225 Deflection Amplifier circuit boards. The A225s boost the input signal to a level sufficient to drive the power transistors, while also providing gain and position controls. In turn, the power transistors drive the deflection yoke that positions the electron beam on the screen. The yoke currents are then passed through a 0.5Ω resistor that converts the yoke currents back into voltages that are used as feedback for each A225 Deflection Amplifier.

This feedback allows the A225 to produce an exact current replica in the yoke of the input signals. The intensity input is applied to the W684 circuit board that converts this input to a 60V pulse that drives the cathode. The cathode pulse is negative going; this pulse turns on the electron beam, creating a spot on the screen. The W684 also accepts three intensity levels and the output of the Brightness potentiometer to establish a grid voltage; image brightness is determined by the W684 output. The G840 fault protection circuit disables the intensity circuit in the event of a -22V failure. This prevents the phosphor screen from burning, as there would be no deflection under these conditions. The primary function of the G840, however, is to shape the light pen signal from the light pen and send it to the DPU.

Line power is passed through a fuse, an on-off switch, and then through a normally closed thermal cutout switch. The switch is located on the ±20V regulator heat sink. In the event of a fan failure or excessive temperature on the heat sink, VR14 input power will be shut off until they cool down. The line power is then connected to the power transformer, the high voltage power supply, and the fans. The high voltage supply converts the input line voltage to 10.5 kV that is connected to the CRT anode. The power transformer has three basic secondaries, a 6.3V for filament, a 35/130 for CRT electrodes, and a 58V center tapped for deflection. The 58 Vac is rectified and filtered to provide ±35 Vdc unregulated. The -35 Vdc is regulated with circuits on the G836 board, along with four power transistors on the regulator heat sink assembly. The regulated output is ±20 Vdc and is distributed to the deflection amplifiers. The 35/130 ac is rectified and filtered on the G836 to generate +80 Vdc and +400 Vdc. The -80 Vdc is used for the G684 brightness circuit which is connected to the grid. The +400 Vdc is supplied directly to G_2 and also to one side of the focus potentiometer on the G836 board. The focus potentiometer wiper goes directly to the focus electrode on the CRT.

3.5.5 Power Connections and Equipment Cooling

The VR14 can operate from a power line frequency between 47 and 63 Hz. The input line voltage, however, is specified by the letter designation after the VR14 (O, C is 115V; A, D is 230V; and B, E is 100V).

This feedback allows the A225 to produce an exact current replica in the yoke of the input signals. The intensity input (INTENSITY OUT L) is applied to the W684 circuit board that converts this input to a 60V pulse which drives the cathode. The cathode pulse is negative-going; this pulse turns on the electron beam, creating a spot on the screen.

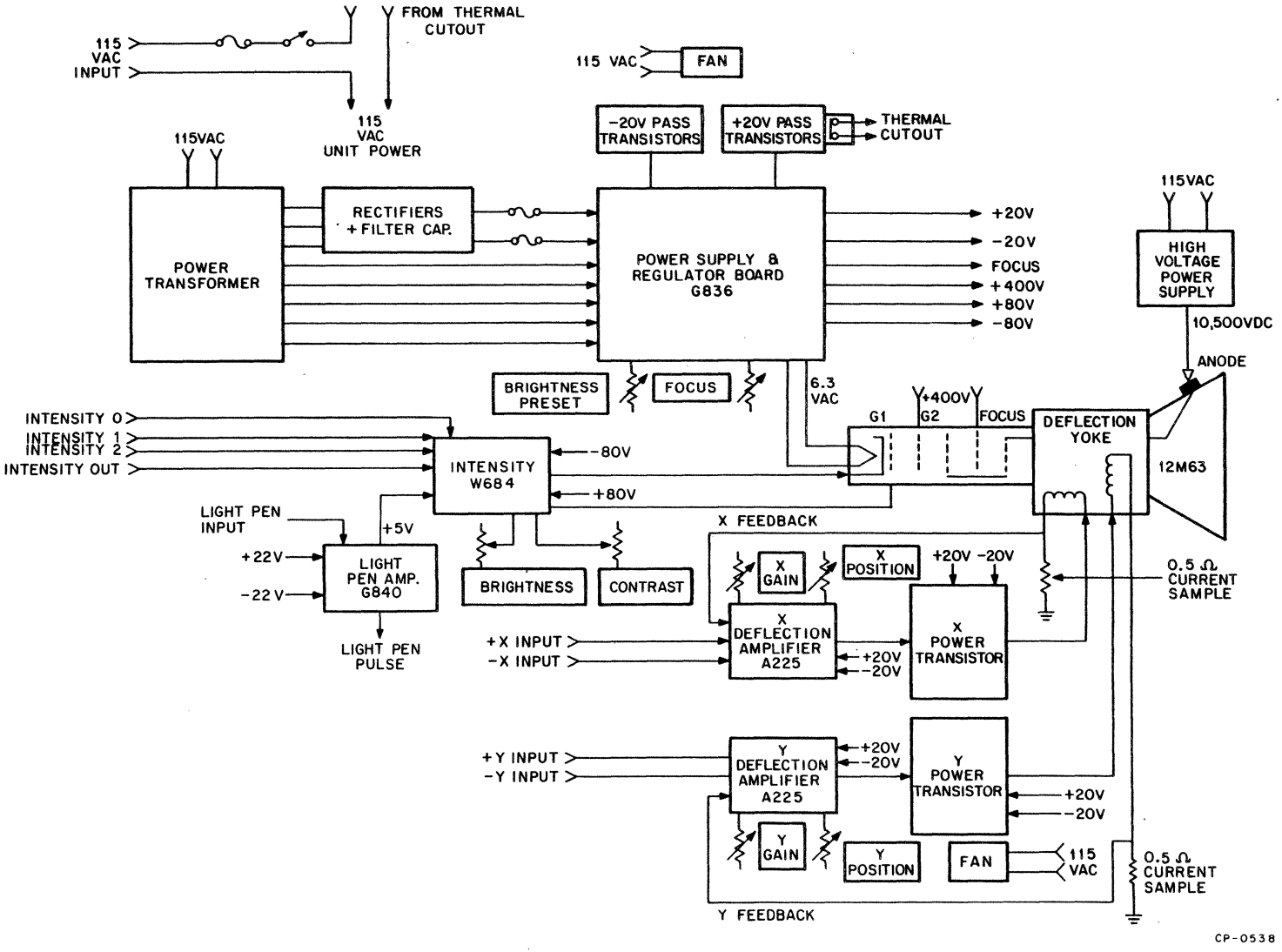


Figure 3-68 VR14 Block Diagram

The W684 also accepts three intensity levels and the output of the Brightness potentiometer to control the grid voltage. This voltage can be varied between -80V and 0V; the closer to 0V the brighter the spot. A low voltage detection circuit disables the intensity circuit in the W684 module in the event of a +5 or +80V failure. This prevents the phosphor screen from burning, as there would be no deflection under these conditions. The VR14 can operate with any of several input line voltages simply by changing the jumpers and interconnections on TB1 and TB2 (Figure 3-69).

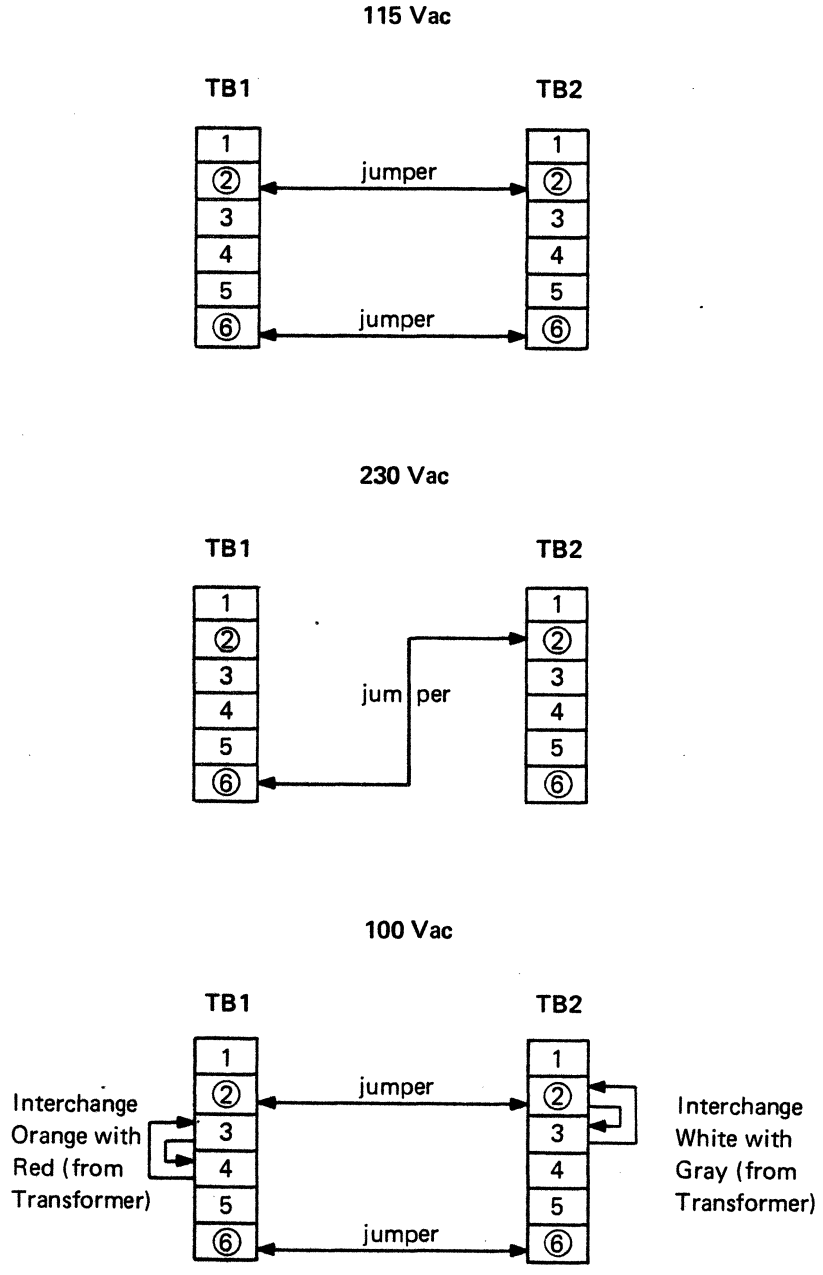


Figure 3-69 Input Power Jumper

Equipment cooling is the most important VR14 installation requirement. Fans draw air from the bottom of the unit; therefore, at least 1 in. of free air space must be provided below the bottom chassis. In the GT40, the VR14 is mounted above the PDP-11/05 with a 1 in. clearance between the two chassis. The cooling air exits from the rear of the unit. Therefore, at least 2 in. of free space must be provided immediately behind the unit. (Do not push the GT40 flush against a wall or solid vertical surface that would cut off air circulation.)

3.5.6 Controls and Connectors

3.5.6.1 Front Panel Controls – The On/Off and Brightness control switch is located on the front panel. The On/Off switch turns on input power to the VR14 when the knob is rotated clockwise from the maximum counter-clockwise off position. Turning the knob clockwise also increases the brightness of the displayed information. A delay of about 30 seconds occurs before information appears on the screen while the CRT filament warms up. In an operating system, it is recommended that power be left on the display even when it is not in continuous use so that the filament warmup delays do not occur.

3.5.6.2 Rear Panel Controls and Connectors – The rear panel (Figure 4-26) has seven BNC connectors, a 24 contact Amphenol connector (P1) and a 14 contact Amphenol connector (P2). The BNC connectors are not used in the GT40. P1 is used to interface the VR14 with the PDP-11/05 and the display processor via the scope cable. The power/signal connection between the VR14 and the keyboard is at P2. Drawing DIC GT40-0-3 and Figure 4-26 show the cable layout at the back of the GT40, while Figure 3-70 is a functional diagram of the scope and keyboard cables showing the pin/signal relationship and signal source/destination. For example, the 20-mA current loop from the keyboard (-KB SIG and +KB SIG) inputs from the keyboard via the keyboard cable at P2 (pins 5 and 6). From P2 the signal is routed to P1 (pins 17 and 18) and then to the PDP-11/05 at.P4 (pins K and S). Note that ±22V is jumped at P2 before being output from P1 to the GT40 logic (A320). P2 thus serves as an interlock for power to the GT40; disconnecting the keyboard cable opens up the ±22V lines to the A320 module.

Power for the VR14 is obtained from a power control box mounted on the VR14 Back Panel. The power control box, shown in drawing DAD 7008930-0-0, contains the power control circuit for the ac input to the PDP-11/05 and the VR14. As shown in the drawing, 120/230 Vac is input to the control box via the ac input power cord which is wired directly to the convenience outlet in the box. The power cord from the PDP-11/05 is plugged into this outlet to provide a direct power connection to the PDP-11/05. When the PDP-11/05 power supply ramps up, +15V is input (P2, pin 1) to the power control relay coil actuating the relay. Normally open contacts 8–6 and 1–3 then close to provide ac to the VR14 via the connecting power cord. This power connection is fused (F1) and the relay contacts are protected by the arc suppressing thyractors D1 and D2. Diode D3 clips any negative spikes developed in the relay circuit. Removing the +15V (P2) would, of course, cause the relay to de-energize and the ac input to the VR14 would be dropped.

3.5.7 Internal Controls

The VR14 internal adjustments include seven potentiometers: X position, X gain, Y position, Y gain, focus, contrast, and brightness preset. Access to the adjustments is gained by removing the case cover (Figure 4-30).

The gain and position adjustments are located on the top, left central portion of the VR14 (as viewed from the front). The two potentiometers on the deflection circuits are the horizontal gain on the left, the vertical gain on the right. The two rear potentiometers are the horizontal position on the left, the vertical position on the right. The contrast potentiometer is located to the right of this group, on the W684 module. It is not accessible from the top of the VR14; the W684 module must first be attached to an extender board before contrast adjustments can be made. This control is used to extend or contract the brightness range of the CRT display. It does not normally have to be changed after an initial adjustment is made to compensate for component variations. The gain adjustments allow the VR14 to accommodate a range of input signal amplitudes and expand or contract the horizontal and vertical deflection to suit full-screen requirements. The position controls accommodate a variety of input signals and allow offset inputs to be centered on the CRT screen. Once initially adjusted for the particular input signals used, the gain and position controls rarely have to be adjusted. Gross positioning off screen or excessive gain deflecting off the extremities of the screen should be avoided, since the deflection amplifiers will go into current limiting and may overheat if allowed to stay in this condition any length of time. Turning the X and Y gain controls clockwise increases the gain or displayed image size. Turning the X and Y positions clockwise moves the displayed information right and up, respectively.

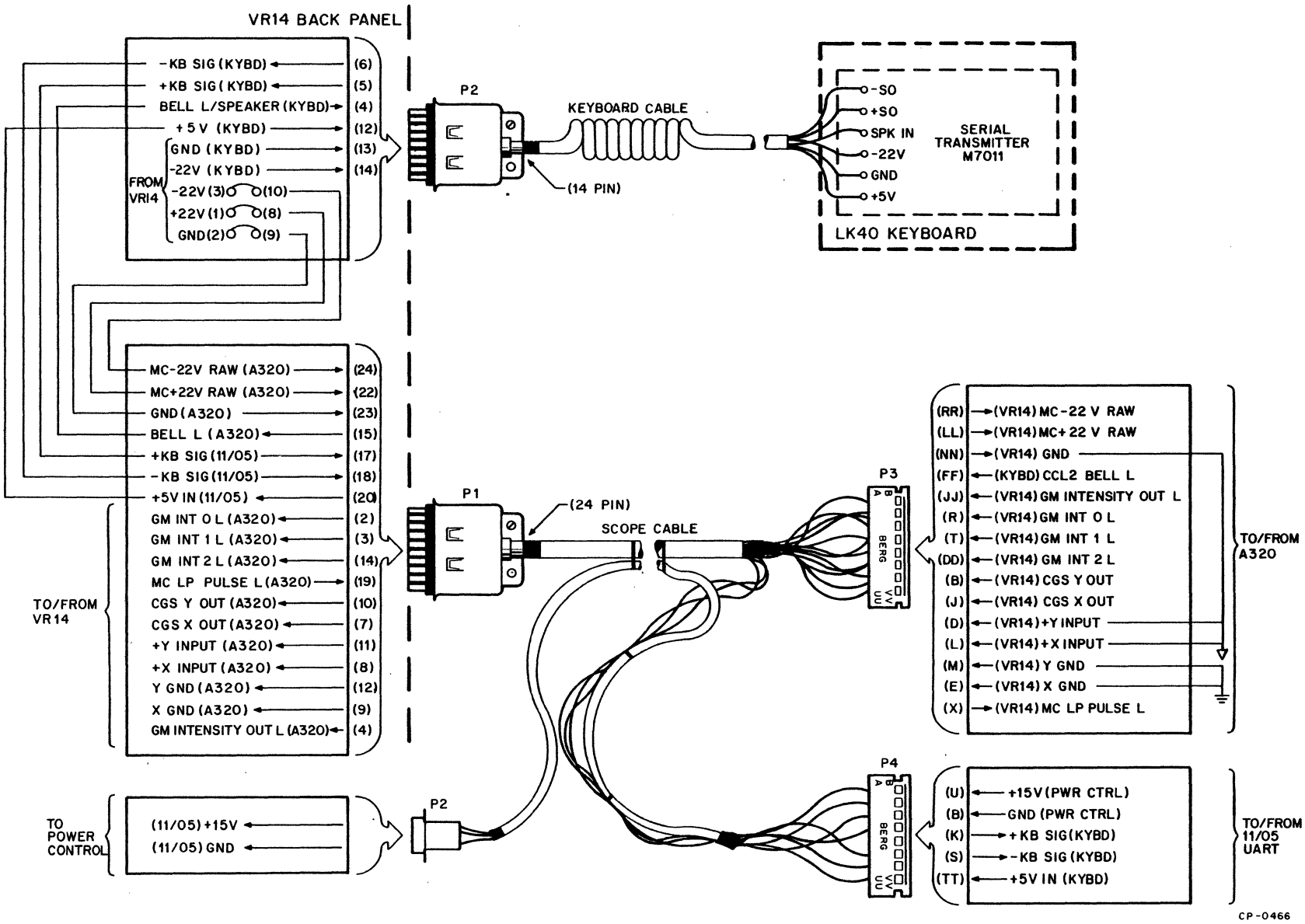


Figure 3-70 Scope and Keyboard Cables

The focus and brightness preset adjustments are located at the top, right central portion of the unit. They are on the power supply regulator circuit (G836) that is somewhat recessed from the top of the unit. The brightness preset is the rear-most of the two. This potentiometer allows the range of the front panel Brightness control to be limited to any maximum brightness desired. Turning the brightness preset counter-clockwise increases the maximum brightness range of the front panel control. Generally, this control is set so that, at maximum brightness setting on the front panel knob, the displayed information does not "bloom" causing a degradation in resolution. The focus potentiometer is in front of the brightness preset. The adjustment is quite insensitive and requires several turns to go through focus.

3.5.8 Input Signal Requirements

NOTE

The deflection amplifiers must not be driven so that the CRT beam is off screen for any length of time or permanent damage may occur. Ensure that input deflection signals fail to a safe, on-screen value.

The VR14 requires analog voltage inputs for X and Y deflection (A225 modules), and a logic level change or pulse for intensify (W684 module). The X and Y inputs are identical, however, because the CRT is a 3 X 4 rectangle, only 3/4 the horizontal deflection is required for full vertical deflection. The deflection inputs are differential but may be driven from single-ended sources.

The VR14 will use the deflection signal with respect to its own ground and not the VR14 ground, which, most likely, will be different and would cause picture ripple and hum. (Never use chassis ground for X and Y input reference; always use signal ground. When using balanced or differential inputs, tie each side of the twisted-pair shielded cable to the two inputs and the shield to the signal ground. The importance of using signal ground cannot be overstated; most noise and washing displays are a result of indiscriminate grounding.)

The positions potentiometers allow the deflection to be offset plus or minus half a screen; thus, a unipolar signal may be completely centered on the screen. Offsets more than half of the full-scale inputs cannot be handled. In other words, if the full-scale deflection is offset from 0V by more than half its full scale value, centering on the screen cannot be accomplished. A 3V peak-to-peak deflection signal, for example, may not be offset from 0 by more than ±1.5V. So ±1.5V, 0V to −3V or +3V are all acceptable, but a deflection input that goes from +1V to +4V cannot be used until it is shifted down a minimum of 1V.

The Z intensify input (GM INTENSITY OUT L) requirement is simply a TTL transition from a high level to a low level. This triggers the intensity circuit.

The brightness level is a function of three intensity levels [GM INTENSITY (2:0) L] and the front panel Brightness control. These signals combine in the W684 module to generate a voltage which is applied to grid 1 establishing a particular brightness level.

At least a 500-ns waiting period must be allowed to intensify a dot before commanding the electron beam to move to its next location. Not giving enough time to intensify a dot after the deflection is settled will also smear the dot, since the deflection amplifier will start "dragging" the dot to the new position. The amount of delay required from the time new X and Y position information is presented to the VR14 and the intensify pulse is requested depends upon how large a position change is requested and how perfectly settled the dot has to be to its final ideal position. Full-scale deflection changes, such as far left to far right or corner to corner, require a 20-μs waiting period for the dot to settle to within 0.01 in. of its final value. If larger errors can be tolerated, 18 μs may be used. Small deflection changes require much less time. A 0.1 in. change can be settled in less than 1 μs.

3.5.9 Detailed Description

3.5.9.1 X and Y Deflection Circuits – The X and Y deflection circuits are identical; therefore, only one axis will be described. The deflection circuit consists of the A225 Circuit Board, two power transistors, and a deflection yoke (Figure 3-71). The input signal is applied to pins E and B on the A225 Circuit Board. The input signal is handled as a differential or balanced signal, even if the input is driven from a single-ended source (the single-ended source being a special case of a balanced input where one side is grounded). R1 and R2 establish the minimum input impedance and form an attenuator with R3, the gain potentiometer. The voltage developed across R3 is amplified and converted from balanced to single-ended by amplifier E1. E1 is an inverting amplifier whose gain is established by the resistor ratios of R7 to R4 and R6 to R5. The bandwidth of the amplifier is tailored by C5 and C6, which act internally on the integrated circuit, and C13 and C14, which act at high frequency to roll off the low frequency gain established by the R7 to R4 and R6 to R5 ratios. A ±6V is generated for both E1 and E2 from the ±20V. This is done by dropping resistors R18 and R19 and Zener diodes D5 and D6.

C1 and C3 and C2 and C4 are local high frequency bypass filters for the ±6V to reduce any high frequency signal noise at each operational amplifier, thus avoiding the possibility of parasitic oscillation. The single-ended output of E1 is connected to R4, which is the input to the actual deflection amplifier; E1 serves more as a signal conditioner-preamplifier.

The amplifier is essentially an inverting voltage to current amplifier, that is, an input voltage is converted to an output current 180° out of phase or inverted with respect to this input. Because the input is a voltage, however, the output current must be converted back into a voltage in order that the feedback compare volts with volts. Current is converted to voltage with a 0.5Ω resistor in series with the yoke. The voltage across this resistor is an exact replica of the current flowing in the yoke; thus, the amplifier compares the input voltage with the yoke current to ensure that the yoke current is an exact replica of the input position signal. E2 compares the input voltage at R4 with the feedback voltage at R33, R10.

Because the amplifier has voltage gain, only a small voltage is needed between pins 10 and 9 of E2 to cause large changes in the output. Pin 9 of E2 is referenced to ground through R13, which is strictly an impedance balancing resistor that minimizes offsets in E2 due to temperature changes. Therefore, pin 9 is essentially grounded. If any voltage appears at pin 10 of E2, the output will immediately respond and reduce the voltage to zero; thus, a null is always achieved at pin 10 of E2. If a variable voltage is present at the input of R4, the output (or yoke current) will vary in such a manner that a continuous null is achieved at pin 10. The only way this can occur is if instantaneously the yoke current undergoes exact equal and opposite changes to those occurring at the input to R4. Therefore, the yoke current will be an exact but opposite polarity replica of the input voltage.

In absolute numbers, the actual yoke current versus input voltage can be determined by comparing resistor ratios. For example, if +1V is applied to the input of R4, 1 mA will flow through R4. This occurs because the amplifier forces pin 10 of E2 to 0V; thus, one side of R4 is 0V, the other is 1V, so 1 mA flows. This current does not flow into pin 10 of E2 because, if it did, pin 10 would rise in voltage because the input of E2 looks like a high impedance. The current must flow through R10 and R33. The only way for this to happen is if the feedback voltage is a negative value, because R10/R33 is tied to pin 10 which is 0V; so pin A must be negative. In fact, if 1 mA flows through R10 and R33, the feedback voltage must be 3.2V and negative. The -3.2V originates from the 0.5Ω resistor in series with the yoke; therefore -3.2V divided by 0.5Ω current is flowing through the yoke. This, of course, is -6.4A, which is an excessive amount of voltage and current limit circuits (explained later) would probably be called into action to limit the output transistors.

The remaining transistors on the A225 boost the current from E2 to a sufficient drive level to operate the power transistors on the large heat sink. The output of E2 drives Q1 through its base resistor R14. Q1 serves two purposes: an inversion stage and a level shifter. Inversion is necessary to get the final output in the proper polarity for negative feedback. Level shifting is required to drive Q2 at its base voltage; E2 cannot do this alone. The Q1 stage has no voltage gain but has current gain. Q2, however, has voltage and current gain and is where the true output voltage is first generated. Q2 is a "grounded" emitter amplifier where, in this case, the emitter, although tied to +20V, can be considered "grounded" and the collector resistor R23 is not tied to -20V but, for analysis, tied to -40V. Q2 has the capability of swinging its collector almost a full ±20V. This large swing is necessary for the yoke and must swing as close as possible to ±20V. The reason for this will be explained later.

The collector of Q2 drives Q3 and Q4, which are emitter followers for the positive and negative outputs. Since a low output impedance is necessary, emitter followers are used; however, Q3 and Q4 are not capable of handling the output power necessary since each can only drive 0.5A. A bootstrap power stage is used to raise the emitter follower current capability to the ±4A required. This is accomplished with two power transistors on an external forced-air cooled heat sink.

These external transistors are essentially "slaved" to the Q3 and Q4 emitter followers. Because the positive swing and negative swing work in the same way, only the positive is described. When the amplifier is required to deliver positive current in the yoke, the circuit responds by turning Q2 on, thus placing a positive voltage on the base of Q3. Q3's emitter responds in a similar manner; however, it cannot supply the necessary yoke current. Still, Q3 attempts to deliver the necessary current. Unlike a normal emitter follower, Q3's collector is not tied to +20V, but instead to the base of the 2N4399 Power Transistor. Thus, when Q3 tries to deliver the output current from its emitter, this very current must flow into Q3's collector from the base of the 2N4399, which will now turn on. Because the 2N4399's collector is also tied to the output (the yoke) it also supports the output current and, in fact, becomes the primary source of output current. Depending on Q3's demands, the 2N4399 is completely slaved to Q3. If Q3 turns on harder, so does the 2N4399. If Q3 shuts off, so does the 2N4399. Therefore, the output looks like it is an emitter follower (Q3) but the 2N4399 delivers all the current and handles the necessary power dissipation requirement.

To minimize power consumption, the output would like to operate in Class B; that is, while positive current is required, no negative current transistors should be turned on and vice versa. However, this approach creates problems at the point where the transition between positive and negative current takes place. The reason is that one set of transistors does not shut off exactly where the other set takes over, but instead shut off prematurely. This creates a dead zone or "no man's land" where neither the positive nor the negative transistors are on and controllable. The appearance on the CRT screen of such a phenomenon is a bunching or nonlinear compression of displayed information where it occurs (usually near the center of the screen). This problem can be solved by not allowing the positive transistors to shut off at zero, but rather conduct somewhat into the opposite side's region. In so doing, the positive transistors would not shut off, for example, until the negative transistors were well turned on. Thus, the amplifier would have control to cancel any nonlinearities that might occur. This task is accomplished with R23, R26, and R27. The major influence is R23, because it places voltage between Q3 and Q4 bases which allow one to be on a little into the region of the other. If R23 were 0, the dead zone would be very abrupt causing a maximum distortion. On the other hand, as R23 is increased, the transistor conducts further and further into the opposite side's operating region. This creates two major problems. The power dissipation causes excessive heating of the output stage and the extra current required overloads the power supply. The value of R23 is chosen, therefore, to minimize dissipation but also to minimize the cross-over distortion.

The output at the yoke has the capability of swinging a full ±20V. This is necessary because even though the yoke is less than 0.1Ω at dc, it has inductance; thus, to force current through at high speeds requires a lot of voltage ($V=L\,\Delta i/\Delta t$). To change 2A through 20 μH in 2 μs requires 20V. That is why the A225 not only has to boost the input signal to a large current but also has to have good voltage capability to force the yoke current to change quickly.

Position control in the A225 is accomplished by adding another input to E2 exactly the way the signal comes in. This is accomplished with R9. The position "signal" is nothing more than an adjustable dc level (from R8) which, through R9, adds or subtracts voltage from the actual input signal. This allows the displayed information to move up/down, left/right on the screen or, in the case of offset input signals, allows the information to be centered on the screen.

The remaining component on the A225 is frequency compensation, which allows the amplifier to operate over its required bandwidth without oscillation. Because the amplifier must operate from dc to beyond 1 MHz, the voltage gain must be reduced continuously at higher and higher frequencies. If this were not done, excessive phase shift between input and output (from feedback) could cause the output to be in phase with the input and thus oscillate. R12, C15, and R32, and C16, R3, and C11 perform the required gain reduction function. R12 reduces the open-loop gain of E2 at all frequencies. C11 reduces the gain of Q2 at high frequencies and is of major significance to the overall bandwidth. The yoke itself represents a major roll off for the amplifier; its high frequency characteristics dominate the stability of the amplifier. An RC network across the yoke enhances the high frequency settling characteristics of the yoke.

The power output stage (2N5302 and 2N4399) is current limited by the +20V and -20V power supply regulators. If the deflection amplifiers are driven way off screen, the power supply limits the maximum current to 11A. If this condition is allowed to exist, eventually either the +20V fuse or the -20V fuse will blow, rendering the circuit safe from such overloads.

(Refer to Paragraph 4.3.3.5 for the deflection amplifier troubleshooting procedure.)

3.5.9.2 Plus and Minus Low Voltage Regulator Supply – The input line voltage is stepped down in the power transformer to approximately 30 Vrms. There are two identical secondary windings to deliver these 30V. Both windings are connected in series making a 60V center-tapped winding. Using full wave bridge rectification, the ac becomes approximately 70 Vdc. By grounding the center tap, these 70 Vdc split evenly with respect to ground; thus, a +35V and a -35V are available with respect to ground. A filter capacitor on each ±35V line smoothes the ripple and finishes the task of generating the raw, unregulated dc for the ±20V regulators. The regulators are contained on the G836 Circuit Board (Figure 3-72) and the heat sink adjacent to the G836. Since the ±20V regulators are symmetrical, only the negative regulator is described. The raw ±20V (actually ±35V) is dropped by R33 and R34 and pre-regulated with D5 and D6 to +12 Vdc and D7 and D8 to -12 Vdc. The ±12 Vdc are the voltages necessary to operate E1 and E2; they are also used to generate the reference voltage with which the output voltage will be compared. The reference for the -20V regulator is made with the +12 Vdc passing through R1 and establishing +6.2V across D1. C1 across D1 reduces the dynamic resistance of the reference by removing high frequency fluctuations. The +5.6V reference voltage is delivered to R2, which ties the summing point (pin 2) of operational amplifier E1.

The feedback from the output regulated voltage through R3 is also applied to the summing point of E1. The nature of the circuit is that a null will be maintained at pin 2 of E1. Therefore, because the voltage on R2 (reference) is stable, the only variable is the output.

Whenever the output changes for any reason, the null is disturbed at pin 2 of E1; E1 then forces the output to change in a manner that returns the null. For example, if the input line voltage increases causing the raw -20V to increase, the -20V regulated output starts to climb. The null would then be disturbed and E1 would shut the output down somewhat so that the null could be maintained. On the other hand, if a heavy load occurred on the -20V regulator causing the -20V to drop, the null would again be disturbed and E1 would act in a way that would turn on the output hard enough to return to its proper level, the level that maintains the null.

This regulating action takes place in a matter of microseconds. The actual output voltage at which the null will be maintained is determined by the ratio of R3 to R2 times the reference voltage. The mechanics of how E1 controls the output can be traced stage by stage. E1 drives an emitter follower, Q1, to give the output, E1, sufficient drive capability to fully turn on Q2, if required. Q2, through R12, controls the base current of the series pass transistors that are external to the G836 board. The pass transistors maintain a constant output, since they are supplied power from the raw dc source. Because of the high open-loop voltage gain, high frequency networks are used to roll off the gain of the regulator to ensure stable nonoscillatory operation. C2, R5, C5 serve this purpose.

The actual point where the output voltage is regulated is determined by where the sense leads are tied. The sense leads are nothing more than the feedback and the reference ground for the regulator. If the regulator simply monitored its regulated voltage at the G836 Circuit Board, voltage drops across the wires carrying the current to the deflection amplifier could not be cancelled. By tying the sense leads at the deflection amplifier, -20V is maintained where it is needed, at the load (deflection amplifier).

The output power transistors are current limited by D13, D14. These diodes conduct whenever excessive collector current is demanded. In so doing, the diodes limit the base drive, thereby limiting the maximum fault current that may flow.

(Refer to Paragraph 4.3.3.3 for the power supply troubleshooting procedure.)

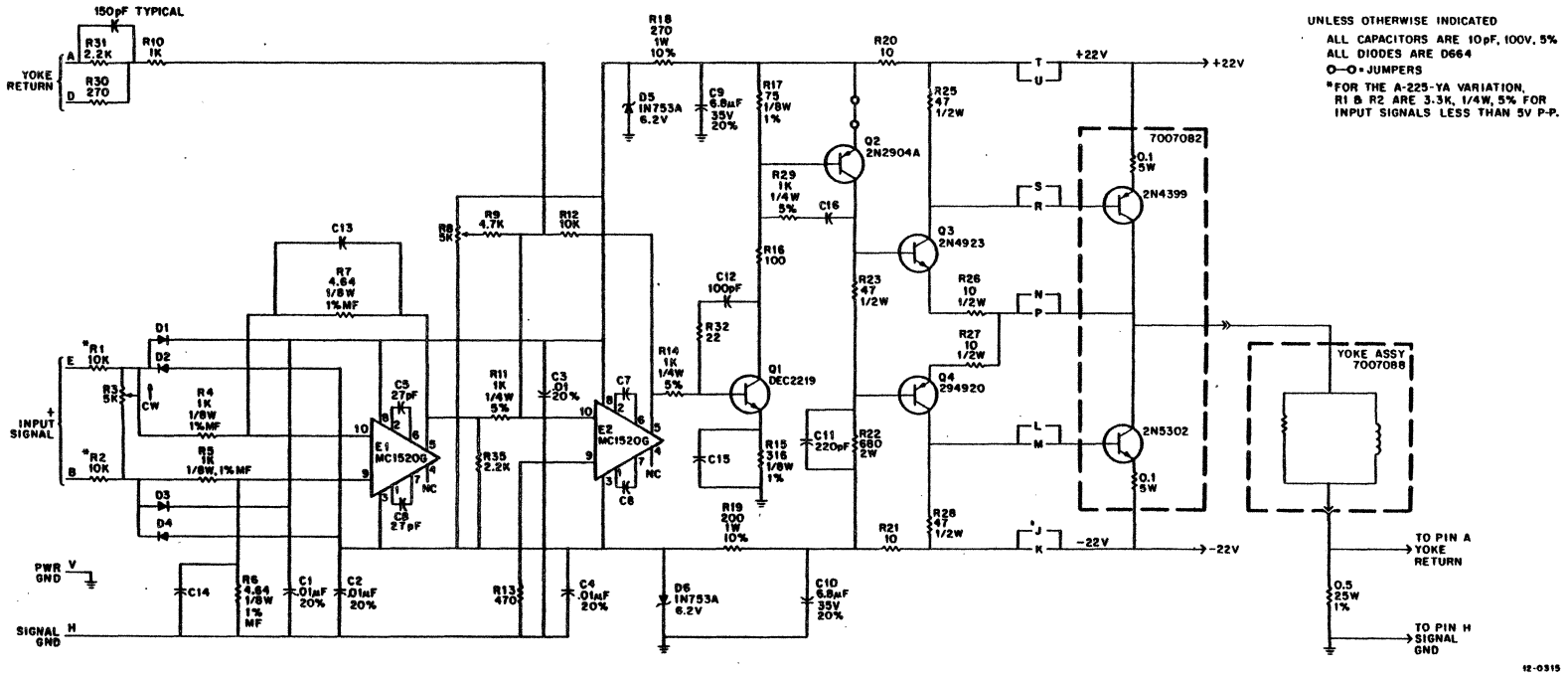


Figure 3-71 X and Y Deflection Circuit

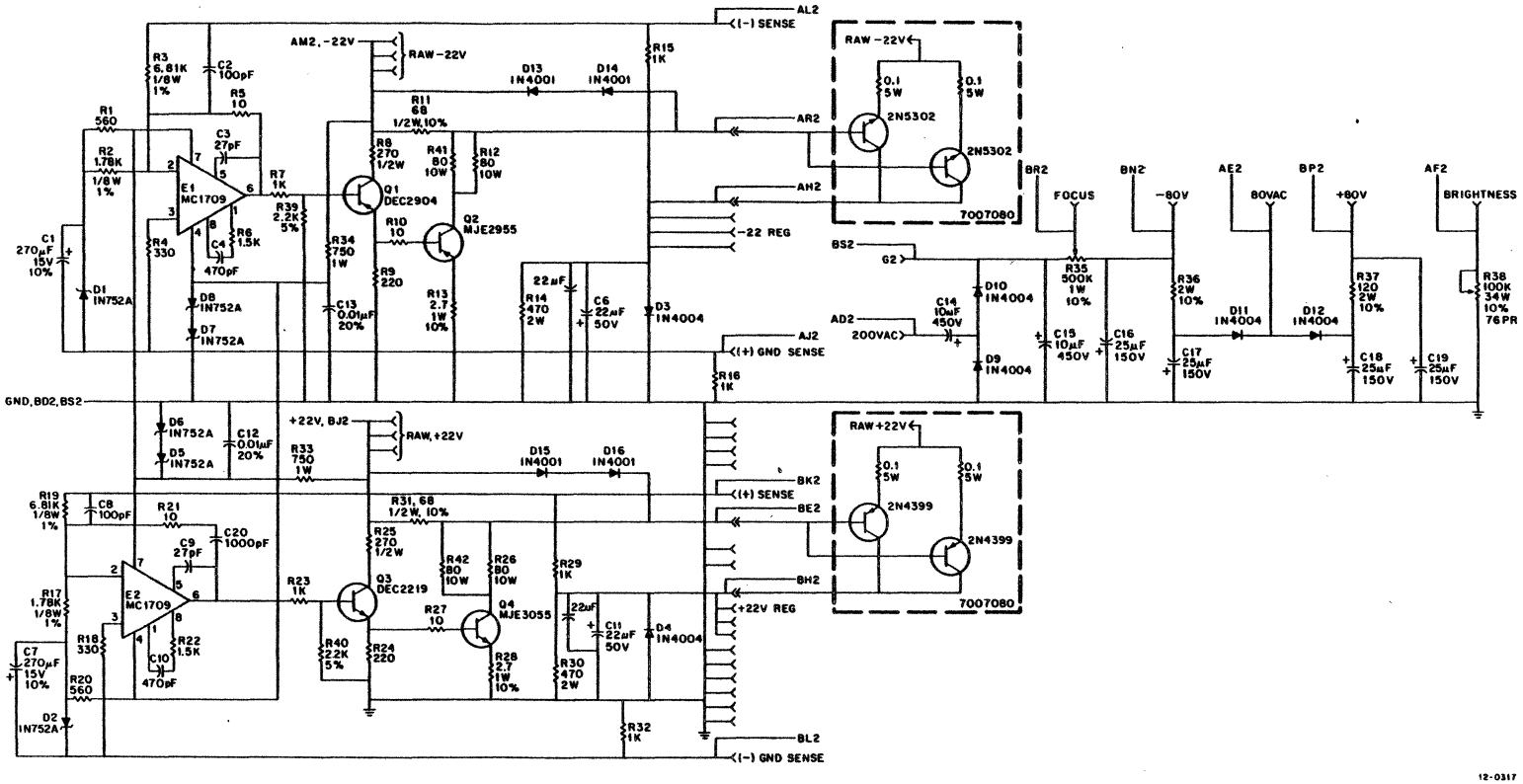


Figure 3-72 G836 Circuit Board,
Part of the 7007165 Power Regulator Assembly

3.5.9.3 **CRT Electrode Voltages** – The CRT electrode voltages are the filament, cathode, grid 1, grid 2, focus, and anode. The filament is simply a step-down winding on the power transformer that delivers 6.3 Vac directly to the filament. The cathode and grid 1 bias voltages are generated on the W684 module from a 35-Vrms winding on the power transformer. This winding terminates on the G836 (Figure 3-72). Through D11, C17, R36, and C16 this winding generates -80 Vdc by half-wave rectification. Likewise, the same winding generates +80 Vdc from D12, C18, R37, and C19. The -80V is applied to one side of the front panel Brightness potentiometer and to the grid voltage generating circuit on the W684 module. The wiper on the front panel Brightness potentiometer also goes to this circuit on the W684 module, while the remaining side of the potentiometer returns to the brightness preset potentiometer, R38. (Brightness (grid 1) control is shown in Figure 3-73). R38 sets the maximum positive value the front panel potentiometer can achieve. The front panel potentiometer, when turned fully counter-clockwise, connects the W684 grid voltage generating circuit (via the wiper) to -80V, cutting the CRT beam off completely. As the potentiometer is turned clockwise, the input to the W684, and consequently to grid 1, becomes more positive, approaching 0V. The maximum positive value is determined by adjusting R38 on the G836. One of eight intensity levels and the contrast level generated in the W684 are also factors in determining the ultimate voltage applied to grid 1; these circuits are described in Paragraph 3.5.9.5.

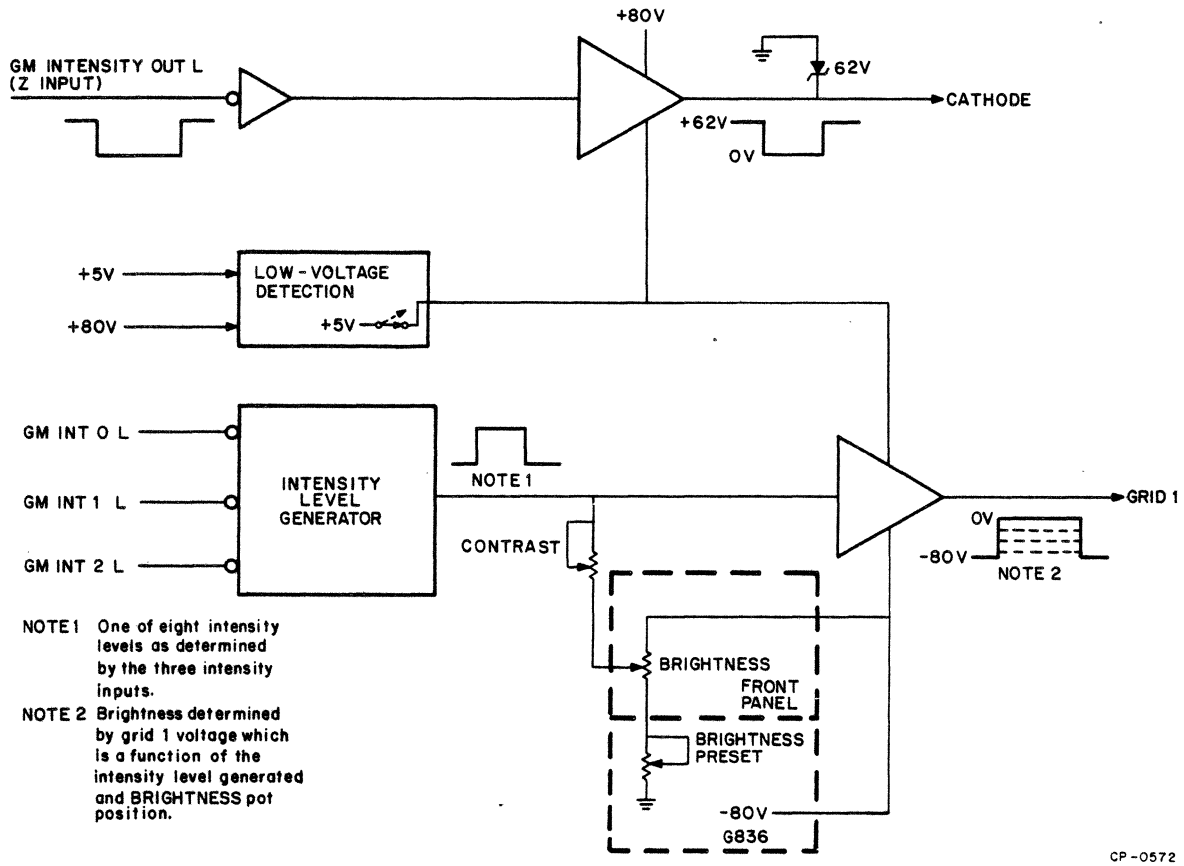


Figure 3-73 W684 Intensity Control

Intensity on the screen is generated by cathode pulses from the W684 card. When not intensifying, the cathode is held at +62V. The +62V is derived from the +80 Vdc at the W684 board (Figure 3-72). When the beam is to be turned on, the +62V on the cathode is "grounded" or made 0V. However, this alone does not determine brightness, since intensity is related to grid-to-cathode voltage. Thus, the cathode is constantly going between +60 and 0V but, depending on where the grid voltage (brightness potentiometer plus intensity level) is set, the beam may never be on, dim, or very bright.

Grid 2 of the CRT is operated at approximately 400 Vdc. The 400V is generated by a voltage doubler on the G836 board. The ac passes through C4 and is prevented from going negative by D9. This causes the entire peak-to-peak voltage to become positive. D10 rectifies this voltage and C15 filters; the resultant output is +400 Vdc. The 400 Vdc goes directly to G2. If G2 is not substantially positively biased, the CRT beam can never be turned on, regardless of how much grid to cathode drive occurs. The 400 Vdc also goes to one side of the focus potentiometer, R35, on the G836 board. The other side of the potentiometer goes to -80 Vdc. The wiper goes to the focus electrode on the CRT. Because of CRT manufacturing tolerances, proper focus may occur from unit to unit anywhere between -80 Vdc and +400 Vdc. The focus potentiometer has sufficient range to accommodate any 12M63 CRT. The anode is supplied 11.5 kV from the high voltage supply.

3.5.9.4 High Voltage Power Supply – The high voltage supply is a self-contained high voltage source that requires only line voltage input. The input is actually the split primary of its own internal step-up transformer. For 115V operation, the primary windings are operated in parallel; for 230V operation, they are operated in series. The step-up transformer delivers high voltage ac to a voltage doubler and filter. The ultimate dc voltage is 10.5 kV and unregulated. Thus, the high voltage is slaved to the line voltage, i.e., when the line is 105 Vac, the high voltage is 10.5 kV; when the line is 125 Vac, the high voltage is 12.5 kV.

Because the electron beam is accelerated by the high voltage, the ability to deflect the beam will change as the high voltage changes. If a constant deflection current flows through the yoke, the amount of deflection is reduced if the anode high voltage is increased (smaller displayed picture); the deflection grows if the anode high voltage decreases (larger displayed picture). The actual deflection factor change is proportional to the square root of the ratio of the old anode voltage to the new anode voltage, i.e., deflection factor = $\sqrt{V1/V2}$. For example, if the high voltage is halved, the deflection would grow 1.414 ($\sqrt{2/1}$). In terms of line voltage, the deflection factor is approximately 0.4 of the change, i.e., a 5 percent line change causes a 2 percent deflection change.

3.5.9.5 Intensity Circuit – The intensification of points on the screen is controlled by the W684 module. The intensity signal, GM INTENSITY OUT L, is input from the A320 module at pin J (drawing DCS W684-0-1). This signal is a transition from high to low. Before GM INTENSITY OUT L is asserted (pin J is above +2.4V) the output of E2 pin 3 is low disabling the two AND gates, E2 pin 6 and E2 pin 11. This causes Q7 to be cut off and Q6 to conduct. Consequently, Q2 is cut off because it's base is low at this time. With Q2 cut off, the cathode voltage at pin U will be positive, approximately +60V, and no beam is generated. The cathode voltage is produced by the Zener action of D4 from +80V input from the G836. When GM INTENSITY OUT L is asserted, E2 pin 3 is disabled and E2 pin 6 and E2 pin 11 are enabled. Now the situation is reversed; Q6 is cut off and Q7 conducts. With Q7 conducting, +5 REG is coupled to the base of Q2 causing it to conduct. The cathode voltage goes from +60 to 0V and a beam can be produced, provided one other condition is satisfied – grid 1 must be sufficiently positive before the grid to cathode voltage results in a beam strong enough to cause screen fluorescence.

Grid voltage can be varied from approximately -80 to almost 0V; brightness increases as the voltage becomes more positive. Q3 controls the grid voltage with the screen brightest when Q3 is cut off. When Q3 conduction increases the image becomes dimmer. Conduction of Q3 is determined, along with the contrast control setting, by the voltages present at the base of Q4 and the emitter of Q5. The voltage at the base of Q4 is established by the front panel Brightness control. Turning this control clockwise causes Q4 to conduct less; the emitter voltage becomes more positive. As a result, the base of Q3 becomes more positive. Coincident with this, the emitter voltage of Q5 is determined by the state of the three intensity level signals from the A320 module, GM INT (2:0) L. These signals forward bias three diodes (D8, D9, and D10) that control the conduction of +5 REG through a voltage divider consisting of R21, R22, and R33. Table 3-35 shows the relationship between the three intensity levels and the resultant brightness level. As the number of levels asserted increases from 0 through 3, the brightness level increases from 0 through 7. The higher the brightness level the more positive the emitter of Q5 and therefore the harder Q5 conducts. As Q5 conducts harder more voltage is dropped over the Q4, R18 and R19 network causing the base of Q3 to become more positive. This, in turn, decreases Q3 conduction and the emitter (grid 1) voltage approaches 0V.

Table 3-35
Brightness Control

Intensity Level			Brightness Level	Front Panel Brightness Control
2L	1L	0L		
H	H	H	0	
H	H	L	1	
H	L	H	2	
H	L	L	3	
L	H	H	4	
L	H	L	5	
L	L	H	6	
L	L	L	7	

Figure 3-74 illustrates the relationship between the eight brightness levels, that are program controlled, and the Brightness control, which can be changed by the operator. Reference A shown the relative brightness, at a particular Brightness control setting, for each of the brightness levels. As the control is turned clockwise, there is a linear increase in brightness at each level (reference B).

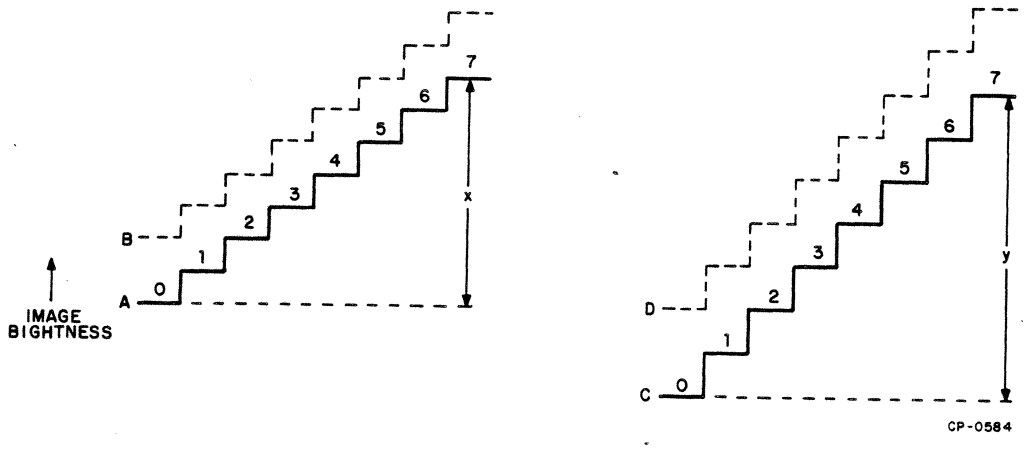


Figure 3-74 Brightness and Contrast Control

The contrast control, R19, is positioned between Q4 and Q5. As the control is turned clockwise, dropping more voltage, the brightness range between brightness level 0 and brightness level 7 is increased; i.e., the image contrast is increased. This is indicated in Figure 3-74 as the change from reference A to reference C; the original brightness spread (x) is increased (y). Actually, level 0 becomes dimmer and level 7 becomes brighter. Therefore, the Brightness control must also be adjusted at the same time to compensate for the descreased lower intensity levels. Reference D shows the result of this final adjustment.

Note that grid 1 voltage is the consequence of the three intensity levels generating a brightness level (one of eight) that is then combined with the particular Brightness control setting. At the same time, the contrast control setting determines the difference in brightness between the brightness levels.

In case of a decrease in the +5 or +80V input to the W684, the cathode and grid circuits described above are disabled. If these circuits were not shut off when this low voltage condition occurred, the phosphor would be burned and the screen damaged. This is because X and Y deflection circuits are disabled by the same power failure and the electron beam would be continually directed to the same spot on the screen. If the +5V input from the G840 at pin A drops to about +4.0V, Q9 loses forward bias and ceases to conduct. Effectively this opens the +5V input to the emitter of Q7 (cathode circuit) and to the R21, R22, and R23 voltage divider (grid 1 circuit). The same result occurs if the +80V input to the cathode circuit fails. In this instance, the base of Q9 becomes more positive; Q9 is cut off and the +5V input opens.

When power is removed from the VR14, the CRT must be prevented from blooming and possibly burning the phosphor. Blooming can occur because the necessary voltages that keep the CRT grid cathode (±80 Vdc) shut off drain to 0V faster than the high voltage supply. When the grid-to-cathode voltage becomes more positive than cut off, the CRT turns on very hard. D2 and C1 prevent this from happening. When power is turned off, the +80V goes to 0V but, in so doing, C1 hangs on to its voltage (+60V) and thus back biases D2, which does not allow C1 to discharge. C1 momentarily acts like Q1's power source, allowing the emitter (and CRT cathode) to hold at +60V, which is the safe or off condition. Eventually C1 discharges; however, by that time the high voltage has also discharged rendering the CRT safe.

3.5.9.6 Light Pen Amplification – The input from the 375 Light Pen that results from detection of beam intensification is not usable in its analog form; it must first be converted to a TTL compatible signal. This is the prime function of the G840 Light Pen Amplifier module (drawing DCS G840-0-1 and Figure 3-75).

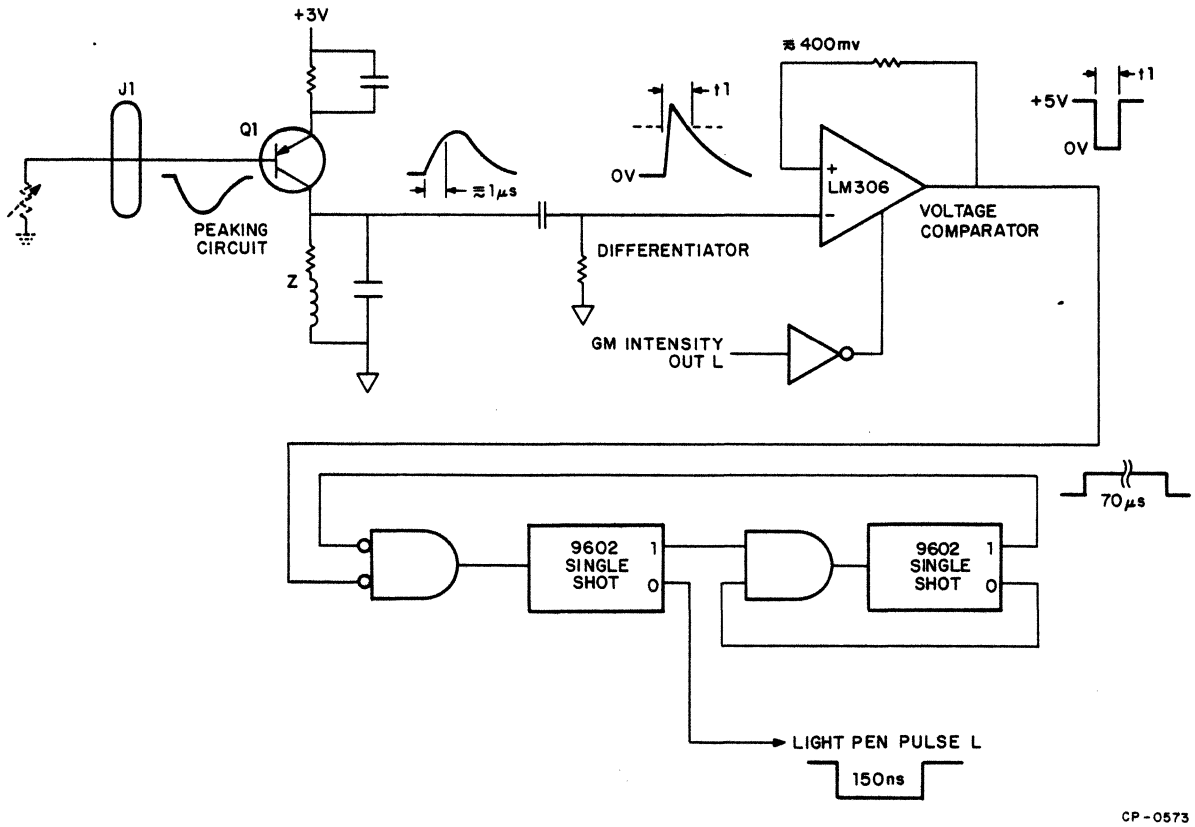


Figure 3-75 Light Pen Amplifier (drawing DCS G840-0-1)

In relation to the G840, the light pen photo transistor acts as a variable resistor that presents a low-going signal at the input (J1, pin 3) to the module when screen intensification occurs within the light pen's angle of acceptance. This negative-going analog signal is inverted by Q1, and peaked by the circuit at the collector of Q1. The signal, now positive-going with a greatly decreased rise time (about 1 μs), is differentiated before being input to the LM 306 Comparator.

The LM 306 is a high-speed voltage comparator designed to produce a sharp-edged, TTL compatible output when the input attains a predetermined threshold voltage. In this application, the (+) input to the LM 306 (pin 2) is held at about 400 mV. When the differentiated input at the (-) input reaches this threshold, a negative-going output signal is produced at pin 7, provided the signal GM INTENSITY OUT L is present at E3 pin 13. This qualifying signal ensures that all light pen "hits" (LIGHT PEN PULSE L) from the G840 are valid, inhibiting those hits that might be generated by spurious noise from the light pen. The LM 306 output occurs about 30 ns after the two input voltages compare (fall time is approximately 20 ns) and remains low as long as the (-) input stays above the 400-mV threshold. This assertion time is indicated in Figure 3-75 as t1. Positive feedback is provided from the output to the (+) input to assist the input signal comparison.

The negative-going output from the LM 306 triggers one stage of a 9602 Monostable Multivibrator, which, in this application, functions as a single-shot to produce an 150-ns output signal, LIGHT PEN PULSE L. Coincident with this signal from the 0 output, the 1 output from the first stage of the 9602 triggers the second stage, also configured as a single-shot. The 1 output of the second stage, high for 70 μs, inhibits a second light pen hit immediately following the first one. Timing for this operation is shown in Figure 3-76. The comparator output assertion time is unimportant because only the negative-going transition is needed to initiate LIGHT PEN PULSE L.

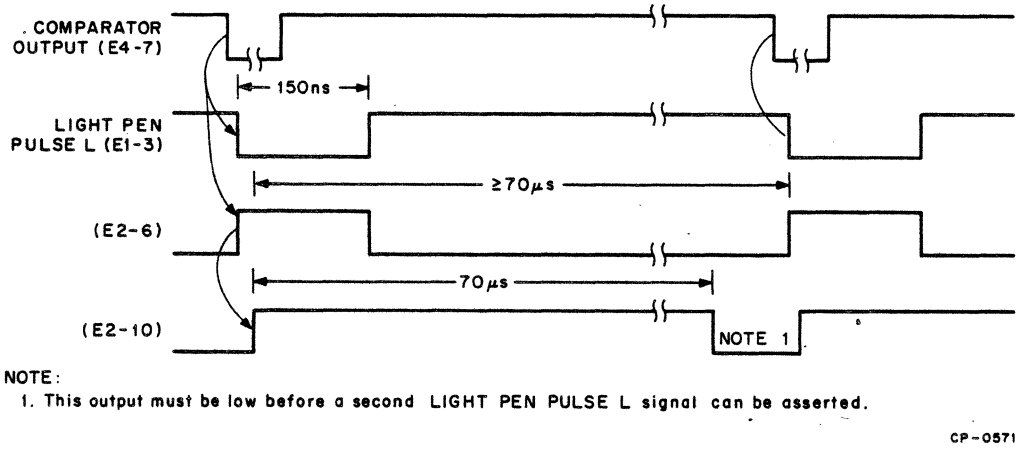


Figure 3-76 Light Pen Pulse Timing, G840 Module

In the event of a failure of either the +22V supplies, deflection ceases and a bright spot occurs on the CRT resulting in a burn. To prevent this, the circuit on the G840 module that produces +5V for the W684 intensity module will be disabled if either the +22V or -22V goes to 0 (in the case of a short circuit or blown secondary fuse). Referring to drawing DCS G840-0-1, if +22V fails, Q3 loses forward bias (at the emitter) and turns off, shutting down the +5V. If the -22V goes to 0, Q2 loses emitter voltage and the base of Q3 goes high. This causes Q3 to turn off and +5V drops. Note that this failure detection circuit is in addition to the W684 low +5V voltage protection circuit previously described (Paragraph 3.5.9.5).

3.5.9.7 375 Light Pen – The Type 375 Light Pen, in allowing a manual operation to be monitored by the GT40 program, functions as an efficient man-machine communication link. By holding the light pen against the face of the CRT so that the light from an intensified point, vector, or character on the phosphor strikes a photo-sensitive transistor, an operator can communicate with the computer program.

The 375 Light Pen is simply constructed. A photo transistor is recess-mounted (drawings CUA 375-0-0 and DCS 5410268-0-0) in a polished cylinder approximately 0.45 X 5.0 in. The output signal connection is via a cable that plugs into the VR14 Front Panel. When an intensified beam strikes the CRT phosphor where the light pen is being aimed, the photo transistor (Q1) conducts and negative-going alternation is output to the G840 Light Pen Amplifier module (Paragraph 3.5.9.6 and Figure 3-75). In the G840, the light pen output is shaped to become the TTL-compatible signal LIGHT PEN PULSE L. This signal is used in the GT40 to set an interrupt flag which can be sensed by the GT40 program, and to increase the brightness level at the light pen position (these applications are described in Paragraphs 3.2.8.5 and 3.2.8.1, respectively).

CHAPTER 4
MAINTENANCE

4.1 INTRODUCTION

Preventive and corrective maintenance procedures that apply to the GT40 Graphic Display Terminal are discussed in this chapter. The most important point in maintenance philosophy is that the user understand the normal operation of the GT40 as described in Chapter 3. A thorough comprehension of this information, plus the maintenance procedures included in this chapter, are the best tools the user has to isolate and correct malfunctions.

4.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed periodically; its major purpose is to prevent failures caused by minor damage or progressive deterioration due to aging. A system log book should be established and necessary entries made according to machine usage.

This data, compiled over an extended period, can be very useful in anticipating possible component failures resulting in module replacement on a projected module or component reliability basis.

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to conditions at the particular installation site which are dependent on environmental conditions, etc. Mechanical checks should be performed as often as required to allow the fan and air filter to function efficiently. All other preventive maintenance tasks should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 600 operating hours or every three months, whichever occurs first.

4.2.1 Mechanical Checks

Perform the following mechanical check and evaluation of the GT40 as required by site conditions and operating policy.

Figures 4-26, 4-27, 4-28, 4-29, and 4-30 show the interior layout and exterior connections of the GT40. They can be used as a reference in locating connectors, modules, adjustment points, and other components when troubleshooting and repairing the device.

1. Turn the VR14 front panel key switch to the OFF position and disconnect the GT40 Power Cable from the power source.

2. Disconnect the scope and keyboard cables from the VR14 rear panel and VR14 Power Control Box. Disconnect the processor box power cord from the VR14 Power Control Box.

3. Carefully lift the VR14 from the guides on the extrusion and backplate assembly (drawing D-IC-GT40-0-3) and place it on the table adjacent to the PDP-11/05.

4. Remove the six screws retaining the VR14 cover assembly; remove the cover and place it to one side.

5. Remove the four Phillips head screws holding the left side panel and the four quarter-turn fasteners that retain the top cover of the PDP-11/05; place the panel and cover to one side.
6. Clean all exterior surfaces, including the removed panels and covers, with a clean cloth moistened with a mild detergent solution. Avoid scratching the CRT face by using only a very soft cloth when cleaning it.
7. Clean the modules and interior areas using a vacuum cleaner and a soft brush. Make certain that the cabinet air exhaust vents are thoroughly clean and unobstructed to ensure adequate cooling. Premature component failure may occur, due to an increase in the GT40 internal temperature, if the vents become obstructed.
8. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
9. Inspect the GT40 modules to ensure that each module is securely seated.
10. Reattach, in reverse order, the panels and covers removed in steps 4 and 5.
11. Carefully lift the VR14 and place it into the guides on the extension and backplate assembly. Make sure both lower extrusions on the VR14 fit properly into the extrusion and backplate assembly.
12. Reconnect the cables removed in step 2.
13. Inspect the following for mechanical security: power supply, jacks, connectors, fans, keyboard, etc. Tighten or replace as required.
14. Attach the GT40 Power Cable to the power source. Turn the VR14 front panel key switch to the POWER position. All or part of the Visual Display Test, MAINDEC-11-DDGTC-A, can now be run as an operational check (Paragraph 4.2.6.5).

4.2.2 PDP-11/05 Checks

The PDP-11/05 should be checked and tested periodically by performing the checks listed in the *GT40 Graphic Display Terminal Manual, Volume 2*.

4.2.3 GT40 Electrical Checks and Adjustments

Perform the power supply checks listed in Table 4-1. Using a multimeter, check the locations indicated for the required values under normal load conditions.

Table 4-1
Power Supply Checks

Voltage	Location(s)	Tolerance
+5V	A01A2, B01A2, C01A2 D01A2, E01A2, F01A2	+4.75V to +5.25V
-15V	F07B2, F09B2	-15.15V to -14.85V
+15V	C04U1, D03R2, F01R2	+14.25V to +15.75V
+22V	PIN LL BERG ON A320	+20V to +24V
-20V	PIN RR BERG ON A320	-22V to -18V
+15 REG	A01D2	+14.85V to +15.15V
-15 REG	A01E2	-15.15V to -14.85V

NOTE

All modules must be properly installed and seated before measuring the voltages listed in Table 4-1.

4.2.4 VR14 CRT Display Monitor Checks

Prolonged off-screen deflection of the CRT beam can damage the VR14. Ensure that the X and Y driving signals into the VR14 never drive the CRT beam off screen because of intermittent incorrect signals.

VR14 checks may be performed with a volt-ohm-milliampere meter and most tests can be done with a VOM; however, more exacting information can be seen with an oscilloscope.

NOTE

When making voltage measurements on a malfunctioning VR14, set the voltmeter (or oscilloscope) to the proper range, connect the leads to the test points, then turn the power on and off very quickly so that the anticipated reading may be taken. Power is only on for a very brief moment. In this way, fault conditions may be discovered without causing further damage. Never leave power on to a malfunctioning or repaired VR14 until all necessary checkpoints are measured and proved nominal (Table 4-2).

Table 4-2
VR14 Voltage Check Points

Circuit Block Pin	Voltage	Signal/Control
A02A	*2.2V nominal	X Current Sample
A03A	*2.2V nominal	Y Current Sample
A02E, B	*	X Input Signal
A03E, B	*	Y Input Signal
A01U, B01V	+22 Vdc (Red)	+ Regulated dc
A01K, B01R	-22 Vdc (Blue)	- Regulated dc
A01P	+5 Vdc	For W684
B04A	3.5 Vrms	1/2 Filament
B04B	3.5 Vrms	1/2 Filament
B04D	+380 Vdc	G2
B04F	0 to -80 Vdc	Brightness (G1)
B04J	-80 Vdc to -400 Vdc	Focus
B04L	*+60V	Cathode With Negative Pulses
Brightness Potentiometer Gray/Green	-80 Vdc	

Deflection Heat Sink Pin X-Axis	Deflection Heat Sink Pin Y-Axis	Voltage	Component
P5 - 2	P5 - 14	+21 Vdc	PNP Base (2N4399)
P5 - 1	P5 - 15	+22 Vdc	PNP Emitter (2N4399)
P5 - 3	P5 - 13	*< 1V	All Collectors
P5 - 4	P5 - 12	-21 Vdc	NPN Base (2N5302)
P5 - 5	P5 - 11	-22 Vdc	NPN Emitter (2N5302)

*Indicates voltage depends upon input signal.

Table 4-2 (Cont)
VR14 Voltage Check Points

Regulator Heat Sink Pin	Voltage	Component
P3 - 1	+43 Vdc Orange	Emitters of 2N4399
P3 - 2	+42 Vdc Gray/Yellow	Bases of 2N4399
P3 - 3	+22 Vdc Red	Collectors of 2N4399
P3 - 12	-43 Vdc Green	Emitters of 2N5302
P3 - 11	-42 Vdc Gray/Blue	Bases of 2N5302
P3 - 10	-22 Vdc Blue	Collectors of 2N5302
7007165 (G836) Regulator Circuit Connectors P1, P2, P4	**Voltage**	**Signal/Control**
P1 - 1	+43 Vdc	Raw + dc
P1 - 3, 6	Ground	
P1 - 4	-43 Vdc	Raw - dc
P2 - 1	3.5 Vrms	1/2 Filament
P2 - 2, 4, 7, 9	Ground	
P2 - 3	3.5 Vrms	1/2 Filament
P2 - 5	70 Vrms (200 P-P)	±80V tap
P2 - 6	150 Vrms (400 P-P)	+400V tap
7007165 (G836) Regulator Circuit Connectors P1, P2, P4	**Voltage**	**Signal/Control**
P4 - 1	+22 Vdc Red	+ Regulated
P4 - 2, 14	Ground Black	
P4 - 3	+22 Vdc Red	Hot + Sense
P4 - 4	0 Vdc Black	Cold ± Sense
P4 - 5	-80 to +400 Vdc Gray/Red	Focus
P4 - 6	+400 Vdc Orange	G2
P4 - 7	3.5 Vrms Brown	Filament
P4 - 8	3.5 Vrms Brown	Filament
P4 - 9	-80 Vdc Gray/Green	To Brightness Potentiometer
P4 - 10	0 to -40 Vdc Gray/Violet	Brightness Preset
P4 - 11	+80 Vdc Gray/Orange	For W684
P4 - 12	-22 Vdc Blue	Hot - Sense
P4 - 13	0 Vdc Black	Cold - Sense
P4 - 15	-22 Vdc Blue	- Regulated

Note: All voltages measured with respect to ground (chassis or B01M, N).

The circuit card connector block, as viewed from the wiring side, is labeled A01 to A04, left to right, on the top section and B01 to B04 on the bottom section.

4.2.4.1 **VR14 Internal Controls** – Seven internal adjustments are provided in the VR14 (Figure 4-30). They are described in Paragraph 3.5.7.

4.2.5 GT40 Display Processor Adjustments

4.2.5.1 Character Display Adjustments – Two adjustments are provided in the character generator. The first is R9, a 10-turn potentiometer in the E slot of the M7013 module (drawing D-CS-M7013-0-1, sheet 2). It is used to adjust the delay from the time the analog Y ramp and X step circuits are started until the actual intensity pulse is generated. Optimum linearity of character rows and columns is obtained with a properly adjusted R9.

The second character display adjustment is the Y ramp character adjust potentiometer, R134, on the A320 module (Figure 4-1). This control ensures that the positive and negative Y ramps will have the same slope (Figure 4-2).

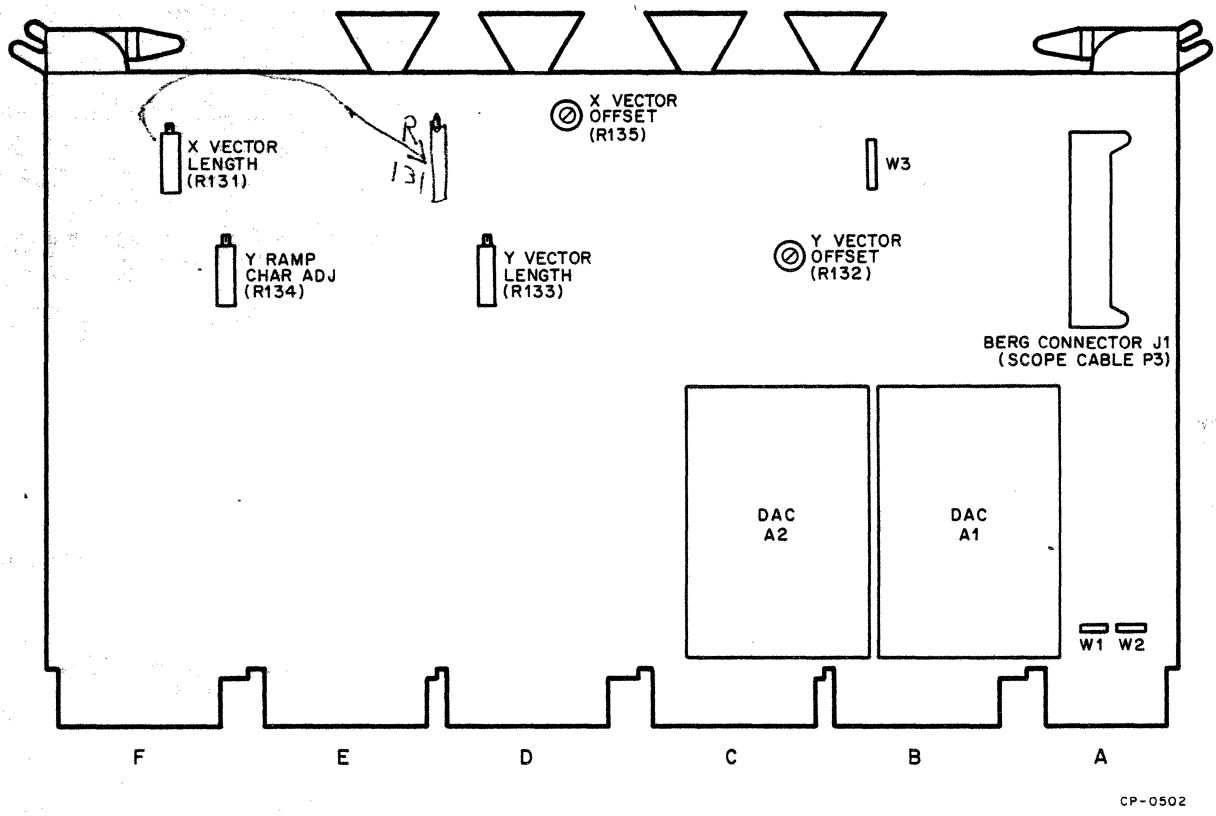


Figure 4-1 Adjustment Locations, A320 Module

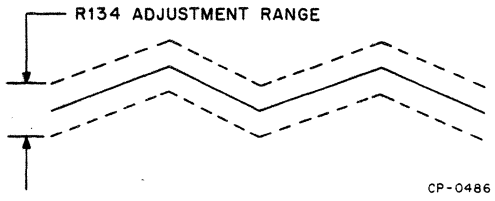


Figure 4-2 Y Character Ramp

An adjustment procedure for these controls is provided in the following paragraphs. Although the two adjustments do not actually interact, they appear to do so on the CRT screen.

1. Display a Rubout character (ASCII code 177_8, Figure 4-3) either by running Instruction Test No. 2, MAINDEC-11-DDGTB-A (Paragraph 4.2.6.4) or by loading the following program into the PDP-11/05:

LOC	Contents	Remarks
1000	12737	MOV
	2000	Display File Addr to
	172000	Display Prog. Cntr
	000001	Wait
2000	117600	Non-Intensified Pt, Level 7
	01000	(1000, 1000)
	01000	
	100000	Character Mode
	177	Rubout
	160000	Display JMP
	2000	

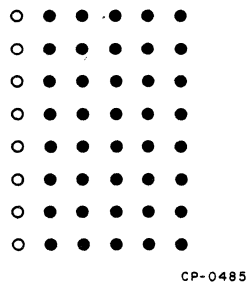


Figure 4-3 Rubout Display Pattern

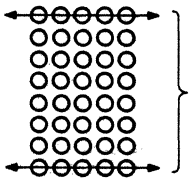
2. Place 1000 in the Switch Register (SR); press LOAD ADRS (Load Address) and START.

3. Adjust R9 on the M7013 module until the top dots in each of the five columns line up horizontally.

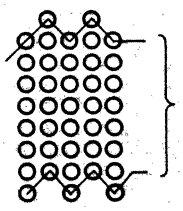
4. Adjust R134 on the A320 module until the bottom dots in each of the five columns line up horizontally.

5. Repeat steps 3 and 4 until both the top and bottom dots of the character are lined up satisfactorily.

6. Examples of correct and incorrect Rubout display are shown in Figure 4-4. Additional information can be found in Paragraph 4.2.6.4.

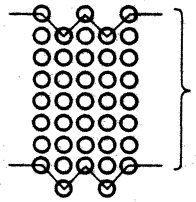


Correct alignment of character dots



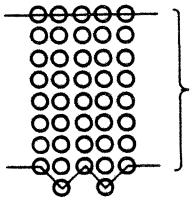
(P) Intensity delay is too long

(S) Increase the period of the delay single shot until dots align. Adjust R9 (M7013 module).



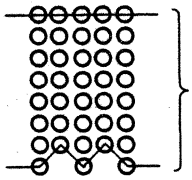
(P) Intensity delay is too short

(S) Decrease the period of the delay single shot until dots align. Adjust R9 (M7013 module).



(P) Negative ramp slope is less than positive slope (see Note)

(S) Increase slope of negative ramp using adjustment provided. Adjust R134 (A320 module).

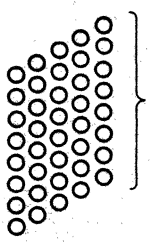


(P) Negative ramp slope is greater than positive slope (see Note)

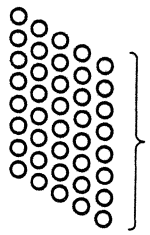
(S) Decrease slope of negative ramp using adjustment provided. Adjust R134 (A320 module).

NOTE

Should the difference between the slope of the positive and negative ramp generators become more extreme than shown, the character may appear to walk up or down as shown below.



Character Walks Up



Character Walks Down

Key: (P) = Problem; (S) = Solution

Figure 4-4 Incorrect Character Display

4.2.5.2 Vector Display Adjustments – There are four adjustments in the vector generator on the A320 module (Figure 4-1). Two are for corrections in the X axis and two are used to correct Y axis problems. In each axis a 10-turn potentiometer adjusts the vector length and a 1-turn potentiometer adjusts the offset value of the analog switch. An adjustment procedure for both vector axes follows.

1. Load and start the Visual Display Test, MAINDEC-11-DDGTC-A (Paragraph 4.2.6.5). Display the Horizontal Vector Angle Pattern (Figure 4-14).

2. Adjust R131 until the ends of the vectors meet the vertical line.

3. Display the Vertical Vector Angle Pattern (Figure 4-15). Adjust R133 until the ends of the vectors meet the horizontal line.

4. Display the Octagons Pattern (Figure 4-12). Adjust R135 until the vectors in the upper right quadrant meet.

5. Adjust R132 until the vectors in the upper left quadrant meet.

6. Additional information can be found in Paragraph 4.2.6.4.

4.2.6 Diagnostic Maintenance Programs

The purpose of diagnostic software is to exercise the GT40 components and to provide the operator with a visual indication of system capability. The available software is divided into several functional tests, some operating automatically, once started, while others require operator intervention during the program run.

The applicable programs (Table 4-3) should be run periodically. General operating instructions are contained in the following paragraphs; however, they may not reflect current procedures due to program operational changes. Therefore, it is recommended that the more complete instructions contained in the program write-ups be referred to if difficulty is encountered, or more detailed information is desired, when running the programs.

NOTE

The Cinch connector on the BC05-C-25 Communication Cable should be disconnected from the modem and connected to a modem test connector prior to running any diagnostic programs. Reconnect the Cinch connector to the modem after testing is completed.

Table 4-3
GT40 Diagnostic Programs

Program	Description
GT40 Quick Verify (MAINDEC-11-DDGTE-A)	This program is a quickly run reliability check of the GT40. The program starts the display and then initiates the communication line; any problem in the system is promptly identified. A ROM verify test and a worst-case noise test are also performed.
GT40 Instruction Test 1 (MAINDEC-11-DDGTA-A)	Using the two maintenance switches on the M7013 module, this logic test evaluates all functional registers and interrupt vectors. Consisting of two parts, it performs both basic and complex logic tests in an automatic single-step mode.

Table 4-3 (Cont)
GT40 Diagnostic Programs

Program	Description
GT40 Instruction Test 2 (MAINDEC-11-DDGTB-A)	Similar to Instruction Test 1, this test examines more closely the registers and interrupt logic; the maintenance switches are not used.
GT40 Visual Display Test (MAINDEC-11-DDGTC-A)	This test causes a series of patterns to be displayed on the CRT that can be used when aligning and adjusting the display.
DL11-E, C/D Off-Line Test (MAINDEC-11-DZDLA)	This test provides a complete check of DL11 interface functions.
ROM Bootstrap Loader Test (MAINDEC-11-DDGTD-A-D)	A data reliability check of the ROM Bootstrap Loader, this test can be used in troubleshooting the ROM Bootstrap hardware in the GT40.
GT40/GTP Overlay Program (MAINDEC-11-DDGTF)	A systems check of the GT40 with other devices.
DL11, BC05-C-25, LK40 and ROM Bootstrap Quick Verification Test (Character Echo)	This test uses the ROM Bootstrap Loader program to exercise the keyboard and interface circuits.

4.2.6.1 Loading Maintenance Programs into the PDP-11/05 – The GT40 is often used in equipment configurations that do not include a teletypewriter. This necessitates the use of the Field Service Cassette Recorder (PMK02A, PMK02C) and a PDP-11/05, 11/45, M7800 Adapter Cable to provide the ability to load programs used during installation and maintenance periods. The adapter cable is terminated in a 50-pin Cinch connector and a 40-pin Berg connector.

Use the following procedure to program load the GT40.

1. Turn off the GT40 with the PDP-11/05 front panel key switch.

2. Disconnect the 40-pin Berg connector on the scope cable (7008993) from the PDP-11/05 SCL connector.

3. Connect the 50-pin Cinch connector on the adapter cable to the cassette recorder and the 40-pin Berg connector on the same cable to the PDP-11/05 SCL connector.

4. Turn the PDP-11/05 front panel key switch to the POWER position. When the 40-pin Berg connector on the scope cable was removed from the PDP-11/05 SCL connector (step 2), the +15V energizing voltage for the relay in the VR14 Power Control Box was also disconnected. This relay is the means whereby ac power is input to the VR14. Therefore, since the relay can no longer be energized, power is not brought up in the VR14 when PDP-11/05 power is turned on.

NOTE
Do not connect the PDP-11/05 cabinet power cord to the VR14 outlet. To do so may result in fuse failure.

5. Reconnect the power cable that was disconnected in step 1 and turn on the PDP-11/05.

6. Load the desired program from the Field Service Cassette Recorder into the PDP-11/05, press HALT, and turn off the PDP-11/05.

7. Remove the PDP-11/05, 11/45, M7800 Adapter Cable and reconnect the 7-wire, 40-pin Berg connector to the PDP-11/05 SCL connector; the 20 mA current loop from the LK40 Keyboard is now connected to the PDP-11/05. The LK40 Keyboard ON/OFF switch (rear panel) should now be placed in the ON position.

8. Turn on the PDP-11/05. The VR14 should also come on at this time because the +15V from the PDP-11/05 is again available to energize the relay in the VR14 Power Control Box.

NOTE

Because there is no hard copy output device supplied with the GT40, all typeouts must be inhibited (SR bit 13 = 1) when executing any program. If the program is directed to stop on an error (SR bit 15 = 1), the failing routine (PC + 2) will be displayed in the address/data lights when the program halts, i.e., an error halt.

9. If the program makes use of a common error halt routine the procedure below should be followed:

   - Change SR switches to:

     Bit 15 = 0 (Inhibit error halt)
     Bit 14 = 1 (Loop on error)
     Bit 13 = 1 (Inhibit error printout).

   - Press HALT and CONT.

   - Follow the program procedure until the failing test is found and then use the program write-up to isolate the failing instruction.

4.2.6.2 GT40 Quick Verify (MAINDEC-11-DDGTE-A) – This test provides a fast go-no go evaluation of the GT40. The display (Figure 4-5) and use of the light pen quickly identify any problem in the system. Two background tests verify the ROM Bootstrap data and provide a worst case memory noise test.

1. Load the program into the PDP-11/05 (Paragraph 4.2.6.1).

2. Determine that the two maintenance switches on the M7013 module are in the OFF position (Figure 2-3 shows their location on the module). Select the starting address for the program by placing 200_8 in the SR.

3. Press LOAD ADRS and START. The program should now be running. The different CRT patterns are displayed automatically during the repetitive 10 second program passes. An LK40 speaker tone signifies the completion of each pass.

4. The display provides a visual test of all GT40 display capabilities: different line type, the character set (normal and italics), different intensity levels, communication line data (echoed), and light pen interaction.

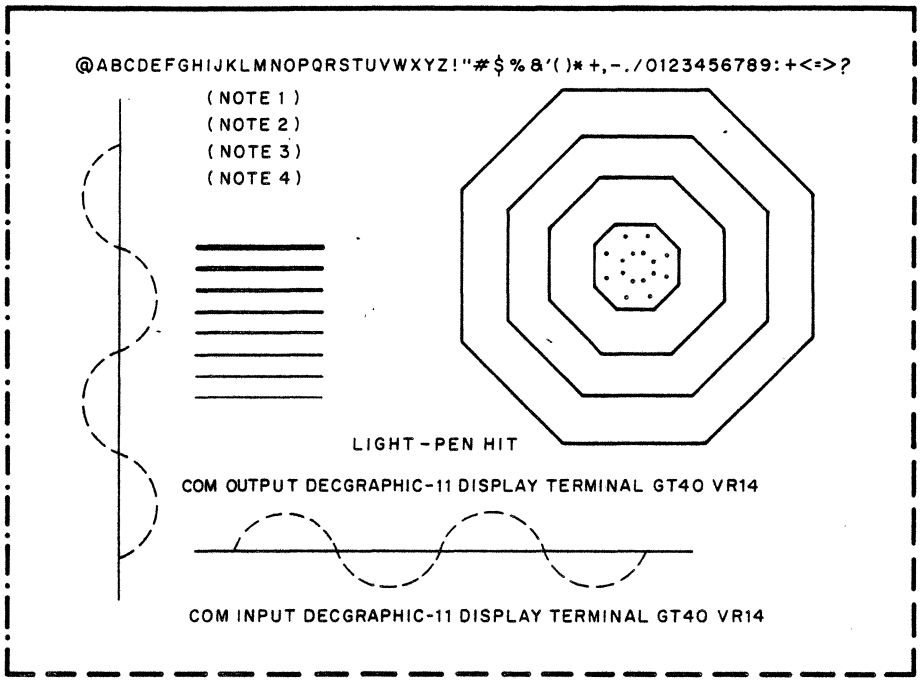


Figure 4-5 Quick Verify Display Pattern

Figure 4-5, as well as the other drawings of CRT displays in this chapter, is a simplified rendition of the actual screen display and is meant to be used only as a guide, not as an accurate portrayal of what the operator should see. Program modifications may also result in a somewhat different display.

5. Observe the data on the screen to the right of the words COM OUTPUT. It should compare with the data to the right of the words COM INPUT.

6. Aim the 375 Light Pen at a line or character. LIGHT PEN HIT should be displayed near the center of the screen. However, a light pen hit should not be generated from the vectors in the largest octagon.

7. The GT40 Quick Verify also reads out the Bootstrap ROM to verify ROM data and performs a worst case noise test of all existing core memory. These tests do not generate specific displays.

4.2.6.3 GT40 Instruction Test 1 (MAINDEC-11-DDGTA-A) – This test is used in those situations where Instruction Test 2 proves to be an inadequate means for troubleshooting the display processor. Instruction Test 1 makes extensive use of the display stop and display resume features of the GT40. The program is automatically executed in the single-step mode. A check is made of all functional registers and interrupt vectors in the alphagraphic display control. The maintenance switches on the M7013 modules are used; satisfactory single-step execution of this diagnostic requires that they be correctly positioned. The following procedure should be adhered to:

1. Load Instruction Test 1 into the PDP-11/05 (Paragraph 4.2.6.1).

2. Place 174_8 in the SR. This selects the Basic Logic Test [Bus Request (BR) only].

3. Set the M7013 module maintenance switches as follows. (Figure 2-3 shows their location on the M7013 module):

Switch	Position
1	ON (Maintenance)
2	OFF (Normal)

4. Press LOAD ADRS and START. Termination of an error free pass will be indicated by a tone signal from the LK40 Keyboard; press HALT and perform step 6.

5. In the event of an error, the program halts with PC + 2 of the failing routine displayed in the address/data lights. If the operator desires the program to restart and loop on the failing test, place SR switch bit 14 to a 1 and press CONT. The program will then halt at the same location. This indicates that the program can successfully loop in the failing routine. At this time insert a NOP (240_8) in the ERROR HALT location (000000) and press CONT. The program will now loop continually in the failing test until HALT is pressed.

6. Place 200_8 in the SR to select the Complex Logic Test (BR, NPR, Interrupt).

7. Set the M7013 module maintenance switches as follows:

Switch	Position
1	OFF (Normal)
2	ON (Maintenance)

8. Press LOAD ADRS and START. Completion of an error free pass is indicated by a tone signal from the LK40 Keyboard; press HALT, and then position both M7013 module maintenance switches in the OFF position.

9. Refer to step 5 if any errors are encountered.

4.2.6.4 Instruction Test 2 (MAINDEC-11-DDGTB-A) – This test is an extension of Instruction Test 1. A complex test, it provides a more detailed examination of the GT40 registers and interrupt operations. Correct positioning of the maintenance switches should be observed. The operating procedure is as follows:

1. Load Instruction Test 2 into the PDP-11/05 (Paragraph 4.2.6.1).

2. Place 200_8 in the SR to select the complex Logic Test (BR, NPR, Interrupt).

3. Set the M7013 module maintenance switches as follows. (Figure 2-3 shows their location on the M7013 module):

Switch	Position
1	OFF (Normal)
2	OFF (Normal)

4. Press LOAD ADRS and START. Termination of an error-free pass is indicated by a tone signal from the LK40 Keyboard; press the HALT switch and perform step 6.

5. In the event of an error, the program halts with PC + 2 of the failing routine displayed in the address/data lights. If the operator desires the program to restart and loop on the failing test, place SR bit 14 to a 1 and press CONT. The program will then halt at the same location. This indicates that the program can successfully loop in the failing routine. At this time, insert a NOP (240_8) in the HALT location (000000) and press CONT. The program will now loop continually in the failing test until HALT is pressed. Depending on the particular situation, the operator can single-step through the failing test and observe various hardware signals on an oscilloscope at the same time.

6. Place 204_8 in the SR to select the Basic Visual Display Patterns Test. This is a check of the GT40 analog circuits that provides a visual indication of equipment condition.

7. The M7013 maintenance switches should be in the following positions:

Switch	Position
1	OFF (Normal)
2	OFF (Normal)

8. Press LOAD ADRS and START. The individual display patterns are selected by SR switches 00 through 02 as listed in Table 4-4.

Table 4-4
Instruction Test 2 Display Patterns

Pattern	SR Switches			Display
	02	01	00	
0	0	0	0	Positive Horizontal Line From Screen Center
1	0	0	1	Negative Horizontal Line From Screen Center
2	0	1	0	Positive Vertical Line From Screen Center
3	0	1	1	Negative Vertical Line From Screen Center
4	1	0	0	Rectangle Around Screen Edge
5	1	0	1	Octagon Pattern in Relative Point & Short Vector
6	1	1	0	Character Set
7	1	1	1	Light Pen Test

9. Set the SR switches to display pattern 0 and press START. Proceed to step 13 if the display appears as shown in Figure 4-6.

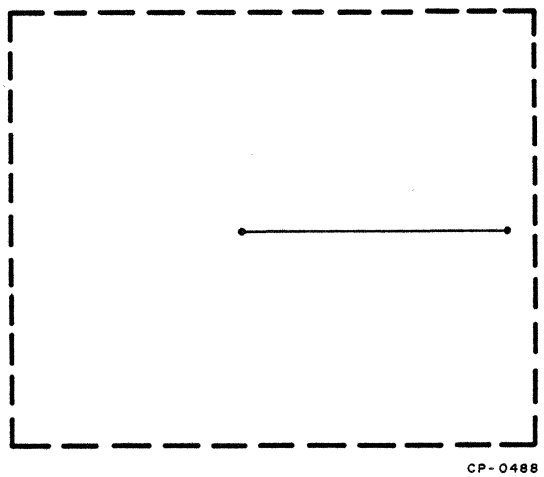


Figure 4-6 Display Pattern 0

10. Check the following if no vector is visible on the screen:

    a. VR14 front panel ON/OFF BRIGHTNESS control is ON and BRIGHTNESS is turned up (clockwise).

b. Check the following signals:

- Z input (GM INTENSITY OUT L, the unblanking signal) at location VR14 A4J. A low level is needed to unblank the CRT.
- X input (X deflection) at location VR14 A2B. A changing voltage (0V → -V) should be observed because a horizontal line is being displayed.
- Y input (Y deflection) at location VR14 A3B. A nonchanging voltage (≈0V) should be observed because a horizontal line is being displayed.

11. If the above signals (step 10) appear to be correct, turn the VR14 ON/OFF switch to OFF.

12. Check the three (3) fuses on the VR14 rear panel. If any are bad, replace and refer to the document *"VR14 and VR20 Troubleshooting Procedures"* which lists step by step procedures for locating the cause of a VR14 failure. If all the fuses are good, check all scope cables for poor solder connections and all connectors for proper seating in the correct receptacles. (Additional VR14 troubleshooting information is contained in Paragraph 4.3.3.)

13. Set the SR switches to display pattern 1 and press START. If a negative horizontal line from the center of the screen is observed, proceed to step 15.

14. Check the following signals if no vector is visible on the screen:

    a. Z input (GM INTENSITY OUT L, the unblanking signal) at location VR14 A4J. A low level is needed to unblank the CRT.

    b. X input (X deflection) at location VR14 A2B. A changing voltage (0V → +V) should be observed because a horizontal line is being displayed.

    c. Y input (Y deflection) at location VR14 A3B. A nonchanging voltage (≈0V) should be observed because a horizontal line is being displayed.

15. Set the SR switches to display pattern 2 and press START. If a positive vertical line from the center of the screen is observed, proceed to step 17.

16. Check for the presence of the following signals:

    a. Z input (GM INTENSITY OUT L). A low level at location VR14 A4J is needed to unblank the CRT.

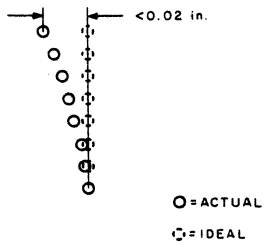
    b. X input (deflection) voltage at location VR14 A2B should be nonchanging (≈0V) because a vertical line is being displayed.

    c. Y input (deflection) voltage at location VR14 A3B should be a changing voltage (0V → -V).

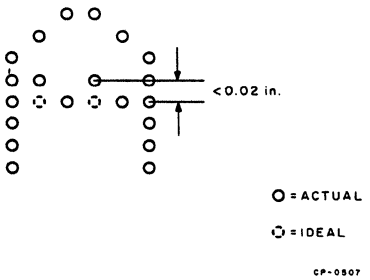
17. Set the SR switches to display pattern 3 and press START. If a negative vertical line from the center of the screen is observed, proceed to step 19.

18. Check the Y input (deflection) voltage at location VR14 A3B. A changing voltage (0V → +V) should be observed because a vertical line is being displayed.

22. Set the SR switches to display pattern 6 and press START. Rubout (Figure 4-3) is considered to be the worst case character because all dots in columns 2 through 6 are intensified. To meet GT40 specifications the centers of all dots in any one column in a character should be less than 0.02 in. (0.0508 cm) from a line running through the center of an ideal display of the same column. This is illustrated below.



The requirement for a row within a character is similar:



23. Two adjustments, R9 on the M7013 module and R134 on the A320 module, control character display. Their function is described in Paragraph 4.2.5.1.

24. Set the SR switches to display pattern 7. Three horizontal vectors are displayed (Figure 4-8).

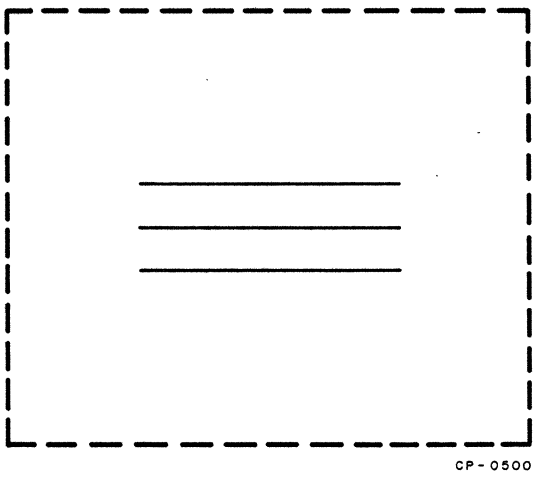


Figure 4-8 Display Pattern 7

25. Turn up the front panel BRIGHTNESS control a moderate amount and point the 375 Light Pen at each vector in succession. Light pen hits should be obtained only from the top two vectors; any additional hits are the result of a failure condition. A light pen hit is indicated by the words LIGHT PEN HIT appearing to the right of the vector generating the hit. Press HALT to stop the program.

4.2.6.5 Visual Display Test (MAINDEC-11-DDGTC-A) – This test provides the user with a visual indication of the different GT40 functions. Refer to Paragraphs 4.2.5.1, 4.2.5.2, and 4.2.6.4 (step 20) for the analog adjustments.

1. Load the GT40 Visual Display Test.

2. Set the SR to 200_8. The LK40 Keyboard switch should be in the OFF position at this time.

3. Press LOAD ADRS and START.

4. The program will commence running all tests.

5. Turn the switch on the LK40 Keyboard to the ON position.

6. The LK40 can now be used to select the individual tests that make up the Visual Display Test; each test displays a distinct pattern on the CRT. Table 4-5 lists these display patterns and the corresponding LK40 key necessary to call it in.

Table 4-5
Visual Display Test

Test	Keyboard Control (Press Character)	SR Control (Set SR Switches to Equal)
Directory	A	000400_8
Repeatability	B	000401_8
Box with X	C	000402_8
Octagons or Squares	D	000403_8
Character Set	E	000404_8
Dash Lines and Blink	F	000405_8
Horizontal Vector Angle	G	000406_8
Vertical Vector Angle	H	000407_8
Horizontal Phosphor	I	000410_8
Vertical Phosphor	J	000411_8
Intensity Levels	K	000412_8
Edge Test	L	000413_8
Short Vector and Relative Point	M	000414_8
Graphplot Increment	N	000415_8
Light Pen Follow	O	000414_8
Keyboard Echo	P	000417_8

7. Pressing RUBOUT after selecting a test will lock-on the display pattern; pressing CR after selecting a test will select a subpicture or stop display motion.

   a. Subpictures can be displayed in the following tests:

      - Octagons or Squares
      - Intensity Levels (SYNC)
      - Graphplot Increment

b. Stop display motion is applicable to the following tests:

- Horizontal Vector Angle
- Vertical Vector Angle
- Horizontal Phosphor
- Vertical Phosphor

8. To continue to another display after pressing RUBOUT or CR, press the key for the desired test (Table 4-5).

9. An error condition may exist if the key actions listed in steps 6, 7, and 8 do not produce the anticipated results or generate a faulty display.

10. [redacted] particularly useful if the operator suspects a keyboard malfunction and wishes to bypass the LK40 to isolate the problem cause. In this case, th[redacted]k [redacted]

11. The [redacted] that must be [redacted] on the right side of the [redacted]. This [redacted] Steps 12 and 13 describe the procedure to set up the LK40 Keyboard by synchronizing the two clocks.

12. Select the [redacted] Observe the screen to see if the selected character is displayed. If the character is not displayed properly, [redacted] is attained.

13. While repeatedly striking the key, turn the clock control on the M7260 clockwise until a faulty display results. Then turn the control counterclockwise until the display again becomes faulty. Set the control midway between these two positions. Recheck the display.

14. If the selected character is never displayed at any clock control setting, check the position of the ON/OFF switch on the LK40 Rear Panel. A problem exists in the keyboard if the switch is in the ON position.

15. Set SR bits 7 = 01 and 8 = 00. Press A on the LK40 to select the Directory display and RUBOUT to lock on the display. Examine the characters for column and row continuity.

16. Press B to select the Repeatability display pattern. Check the display (Figure 4-9) for spot jitter and spot size.

17. Press C to select the Box with X display pattern, shown in Figure 4-10. The display is composed of eight vectors drawn in the following sequence:

$A \rightarrow B$, $A \rightarrow C$, $B \rightarrow D$, $B \rightarrow C$, $C \rightarrow A$, $D \rightarrow B$, $C \rightarrow D$, and $D \rightarrow A$.

18. Check the display for line closure [overshoot/undershoot $<$ 0.06 in. (0.1524 cm)] and vector noise [$<$ 0.01 in. (0.0254 cm)]. The diagonal vectors should appear as single lines, i.e., $C \rightarrow A$ should be superimposed on $A \rightarrow C$ and $D \rightarrow B$ should be superimposed on $B \rightarrow D$. Multiple vectors (Figure 4-11) are considered a faulty display.

19. Check the vectors for straightness and curvature at the beginning and end.

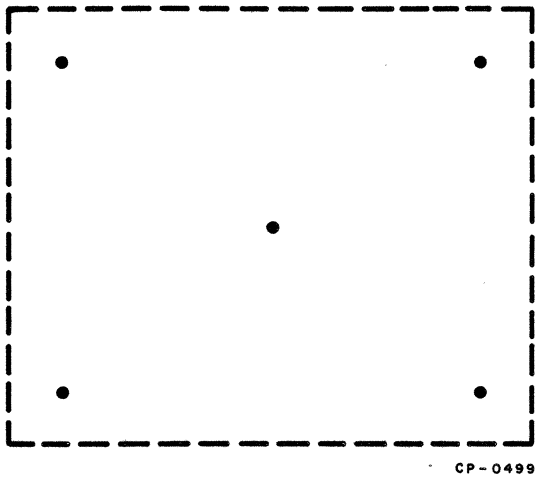


Figure 4-9 Repeatability Display Pattern

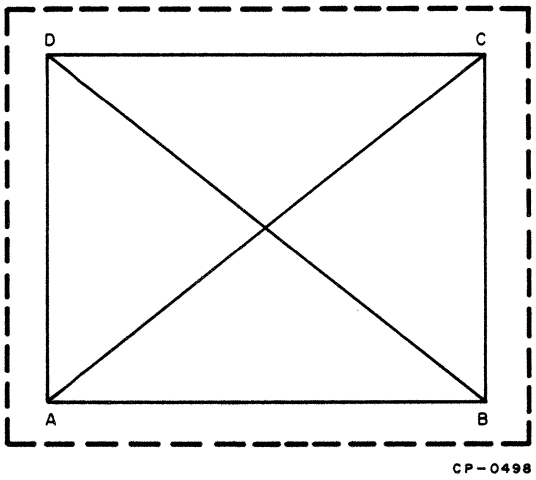


Figure 4-10 Box with X Display Pattern

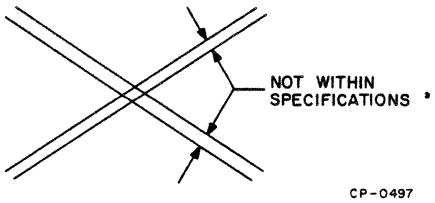


Figure 4-11 Faulty Box with X Display

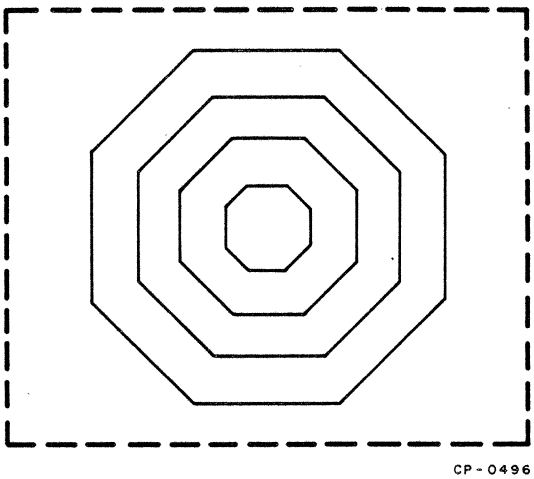


Figure 4-12 Octagons Display Pattern

20. Alternately display Box with X and Repeatability to provide an evaluation of vector position, length, and crossover.

21. Press D to select the Octagons test and RUBOUT to lock on the display (Figure 4-12). All vectors are drawn counterclockwise; this should be kept in mind when making adjustments.

22. Check the display using the criteria described in steps 18 and 19 for the Box with X test.

23. The Squares test can be selected by pressing CR. Evaluate the display, particularly the center squares, for optimum vector quality and note any deviation from the specifications described in steps 18 and 19.

24. Press E to select the Character Set display; press RUBOUT to lock on the display. The character set is divided into four sets of two lines each. Characters are displayed normally on the first line of each set while on the second line they are italicized.

25. Check the column and row lineup of all characters.

26. Press F to display the Dash Lines test and RUBOUT to lock on the display. The GT40 is capable of displaying four line types: solid, long dash, short dash, and dot dash. All are displayed in this test (Figure 4-13).

27. Two sets of the four line types are shown on the screen. The right-hand set flashes on and off as a test of the BLINK function.

28. Press G to display the Horizontal Vector Angle test pattern (Figure 4-14); RUBOUT locks on the display. This test draws vectors from the lower left corner to the right side of the screen. Vector angles vary from 0 to 45°.

29. A vertical vector is drawn from point B to point C to assist in the adjustment of the X vector length; a negative horizontal vector is displayed from point C to point D as an aid in adjusting X offset.

30. The following items should be checked:

    a. The distance between vectors should be equal.

    b. The horizontal vectors should not overshoot or undershoot the vertical vector more than 0.06 in. (0.1524 cm).

    c. Display motion can be halted by pressing CR.

31. Press H to select the Vertical Vector Angle test; press RUBOUT to lock on the display. This test, shown in Figure 4-15, draws vectors from the lower left corner to the top of the screen. Vector angles vary from 90 to 45°. The horizontal vector (C to D) is used to assist in the adjustment of the Y vector length; the vertical vector from C to B aids in adjusting the Y offset control.

32. Refer to step 30 for observations required to ensure proper vector adjustments.

33. Press I to display the Horizontal Phosphor test and RUBOUT to lock on the display. This test draws a group of vertical vectors (Figure 4-16) and moves them horizontally across the screen. Vector motion can be stopped by pressing CR.

34. Inspect the display for the following discrepancies:

    a. Burn spots, glass defects, etc. Note and report any deficiencies.

    b. Digital to Analog Converter (DAC) (A6000) crossover distortion. This distortion is evident at the horizontal and vertical centers of the screen as a variation in intensity. The unit should be rejected if the intensity increases by a factor of two or more at any point on the screen where the intensity should be constant. Since the DACs are bipolar, ranging from -0.5 to +0.5V, nonlinearity may exist at the 0V crossover. This shows as a slight variation in image brightness at this point.

35. Press J to display the Vertical Phosphor test. Press RUBOUT to lock on the display. This test draws a group of horizontal vectors and moves them vertically up the screen (Figure 4-17). Refer to step 34 for required observations.

36. The Intensity Levels test is initiated by pressing K. Pressing RUBOUT locks on the display. Characters, vectors, and relative points are drawn by this test; intensity 0 should be adjusted so that it is barely visible (Figure 4-18).

37. Check the following light pen characteristics:

    a. A vector light pen hit should be obtained at intensity level 4.

    b. A character light pen hit should be obtained at intensity level 6.

    c. A point light pen hit should be obtained at intensity level 7.

38. Check GT40 "sync" by pressing CR. The entire display should become dimmer because a display instruction, following a Status A instruction in the display file, is being synchronized with the line frequency.

39. Press L to select the display pattern for the Edge test. RUBOUT will lock on the display. In this test a rectangle is drawn around the screen edges. Smaller rectangles are then superimposed symmetrically on each leg of the larger rectangle as shown in Figure 4-19.

40. Those portions of the four smaller rectangles that are outside the larger rectangle should be blanked.

41. Press M to select the Short Vector and Relative Point test. RUBOUT will lock on the display. The test is divided into two sections. During the first section a series of short vertical vectors and horizontal relative points (unintensified) are drawn. The sequence is as follows:

    Positive short vertical vector

    Positive horizontal relative point (nonintensified)

    Negative short vertical vector

    Negative horizontal relative point (nonintensified), etc.

    This sequence is continued until the upper left quarter of the screen is covered with intensified short vectors (Figure 4-20).

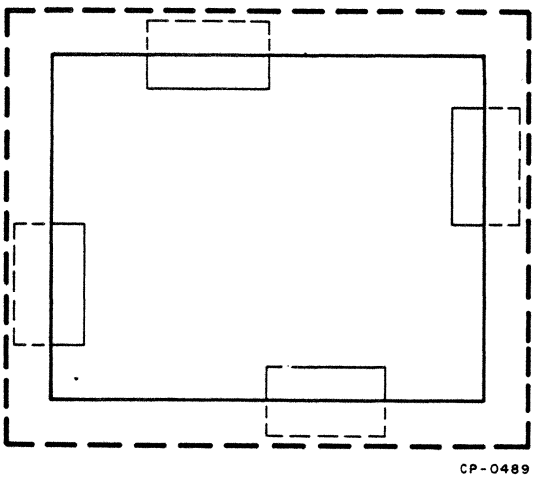


Figure 4-19 Edge Display Pattern

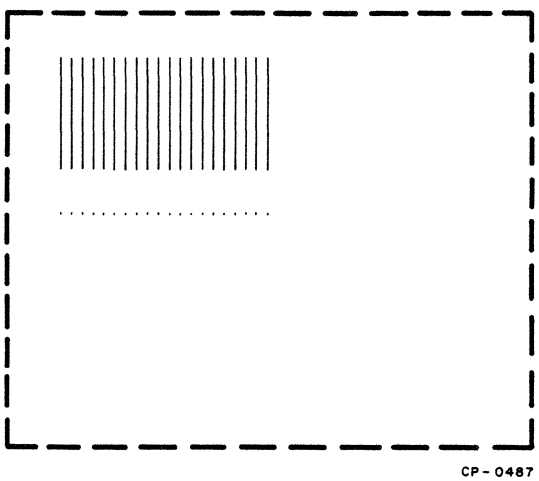


Figure 4-20 Short Vector and Relative Point Display Pattern

37. Check the following light pen characteristics:

    a. A vector light pen hit should be obtained at intensity level 4.

    b. A character light pen hit should be obtained at intensity level 6.

    c. A point light pen hit should be obtained at intensity level 7.

38. Check GT40 "sync" by pressing CR. The entire display should become dimmer because a display instruction, following a Status A instruction in the display file, is being synchronized with the line frequency.

39. Press L to select the display pattern for the Edge test. RUBOUT will lock on the display. In this test a rectangle is drawn around the screen edges. Smaller rectangles are then superimposed symmetrically on each leg of the larger rectangle as shown in Figure 4-19.

40. Those portions of the four smaller rectangles that are outside the larger rectangle should be blanked.

41. Press M to select the Short Vector and Relative Point test. RUBOUT will lock on the display. The test is divided into two sections. During the first section a series of short vertical vectors and horizontal relative points (unintensified) are drawn. The sequence is as follows:

    Positive short vertical vector

    Positive horizontal relative point (nonintensified)

    Negative short vertical vector

    Negative horizontal relative point (nonintensified), etc.

    This sequence is continued until the upper left quarter of the screen is covered with intensified short vectors (Figure 4-20).

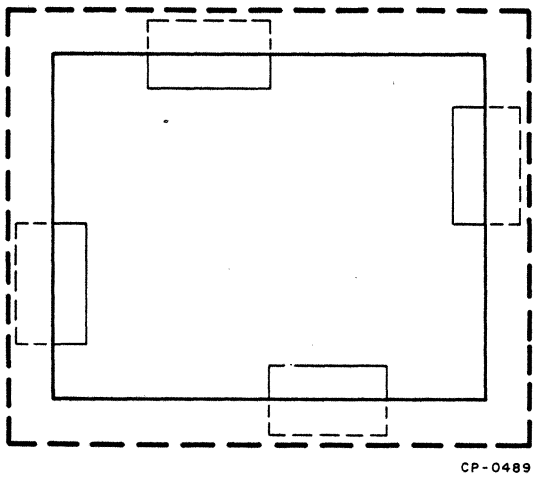


Figure 4-19 Edge Display Pattern

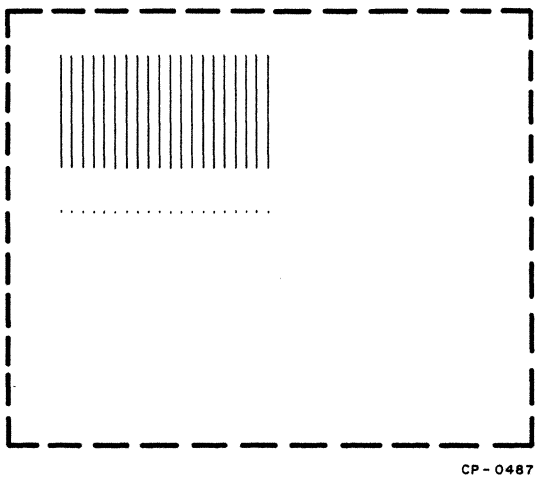


Figure 4-20 Short Vector and Relative Point Display Pattern

42. The sequence in step 41 is repeated. However, this time the short vertical vectors are unintensified and the lower (negative) relative points are intensified. The result appears as a straight line of dots.

43. Press N to select the Graphplot Increment test and RUBOUT to lock on the display. A series of points are plotted at each possible value in the Graphplot Increment Register from 0 through 77_8. The resulting display should appear as a series of points at an increasing angle.

44. Press O to select the Light Pen Follow test and RUBOUT to lock on the display. Two octagons are displayed in this test, one inside the other. When a light pen hit is sensed on any portion of either octagon, both octagons move until their common center is positioned at the point of the light pen hit.

45. Check the following test functions:

    a. Light pen hits should be generated without respect to where on either octagon the light pen is aimed.

    b. The common center of both octagons should move in the direction of the light pen hit.

46. Move the octagons around edges of the screen to determine that correct edge blanking takes place.

47. Press P to select the Keyboard Echo test. Keys depressed on the LK40 Keyboard result in the display of their respective characters on the VR14 screen. Determine that all characters in Appendix C, including the 31 special characters (except for CONTROL C), can be displayed on the CRT. Except for ←, the eight keys on the small keyboard have no affect in this test. Exit from the Keyboard Echo test is accomplished by pressing CONTROL C.

48. Press HALT to stop the program.

4.2.6.6 DL11-E, C/D Off-Line Test (MAINDEC-11-DZDLA) – This program is a full EIA data set control check of the DL11. To run this program, use the following procedure:

1. Turn the front panel key switch to the OFF position. Pull the M7800 module (slot 4 in the PDP-11/05) out far enough so that the following steps can be accomplished.

2. Note the present positions of the transmitter and receiver clock switches on the M7800 module (Figure 3-51). Turn the switches fully clockwise (position 10) and then counterclockwise two positions to position 8. Switch position 8 generates the highest baud rate possible within the M7800 module.

3. Determine that a priority level 5 jumper is installed in the M7800 module; the DL11 operates at priority level BR5 in the GT40.

4. Reinsert the M7800 module and check for proper seating.

5. Place a modem test connector on the BC05-C-25 Modem Cable; check the Berg connector on the other end of the cable for proper seating on the M7800 module. Turn the front panel key switch to the POWER position.

6. Load the DL11-E, C/D Off-Line Test (MAINDEC-11-DZDLA).

7. Change the contents of location 1300 from 040377 to 050377. This allows the program to be run at priority level 5.

8. The DL11 is constructed as a model DL11-E. However, jumper J5 is cut prior to shipment to allow the GT40 ROM Bootstrap to run properly. This, in turn, requires two program changes to inhibit setting the Break bit in the CSR: change the contents of locations 6254 and 13360 from 104003 to 000240.

9. Place 200_8 in the SR and press LOAD ADRS.

10. Set SR 02 = 0 to select program 0.

11. Press START. The program will type the following and halt: "Prg.0 – Input Output Logic Tests. Disconnect D11-E from modem and connect jumper to cable." (If there is no TTY, the program will simply come to a halt.)

12. Press CONT. The program will type the following and halt:

    "Set desired SR options. Normal operation is with SR = 000000."

13. If there is no console TTY, place 120000_8 in the SR (bit 15 = 1 results in a halt when an error is detected; bit 13 = 1 inhibits all printouts).

14. Press CONT. The program will complete one pass in about one minute.

15. Turn the ON/OFF key switch on the PDP-11/05 to the OFF position after approximately 2 minutes. Wait for the fans to stop and then turn the switch to the POWER position. One of two things will happen:

    a. the program will continue running the test, or

    b. the program will halt.

16. If the program halts, press CONT. (The program had been executing a RESET instruction at the time of power fail, i.e., when the switch was turned to OFF.)

17. Allow the program to run for 10 minutes. No errors are permitted.

18. After testing, press HALT and turn the front panel key switch to the OFF position. Reposition the receiver and transmitter clock switches to their original positions (steps 1, 2 and 4). The switch positions must compare with the baud rate indicated on the key sheet. If no baud rate is specified, a baud rate of 300 (switch position 4) is selected at the factory.

19. Remove the modem test connector that is attached to the modem cable (step 5) and reconnect the cable to the data set. Check the seating of all modules and connectors.

4.2.6.7 ROM Bootstrap Loader Test (MAINDEC-11-DDGTD-A-D) – This diagnostic provides a reliability check of the ROM Bootstrap Loader. ROM addressability and data are verified when the four subroutines of program 0 (ROM logic test) are run.

1. Load the ROM Bootstrap Loader Test (Paragraph 4.2.6.1).

2. Set the SR to 200_8.

3. Press LOAD ADRS and START. Program 0 will now run continuously.

4. Allow the program to run for at least ten minutes.

5. If a data dump to the console teletypewriter is desired, press HALT and set the starting address for Program 1 (204_8) in the SR. This program halts automatically. A single ROM address is continuously read when the starting address (210_8) for Program 2 is placed in the SR.

6. Press HALT to stop the program.

4.2.6.8 DL11, BC05-C-25, LK40, and ROM Bootstrap Quick Verification (Character Echo) – This check procedure verifies the operational capability of a GT40 that is used with a null modem and a local EIA terminal. The ROM Bootstrap Loader is used to conduct the check; no diagnostic program is required.

1. Turn the front panel key switch to the OFF position.

2. Pull the M7800 module out (of slot 4 in the PDP-11/05) far enough that the following steps can be accomplished. Determine that a priority level 5 is installed in the M7800 module.

3. Note the present position of the receiver and transmitter clock switches. Turn these switches to position 8. Position 8, two positions less than fully clockwise, generates the highest baud rate possible in the DL11.

4. Re-insert the M7800 module (slot 4 C, D, E and F); check the seating.

5. Disconnect the BC05-C-25 Modem Cable from the null modem. Place a modem test connector on this end of the cable.

6. Check the Berg connector on the BC05-C-25 cable for proper seating on the M7800 module.

7. Turn the LK40 Keyboard ON/OFF switch to the ON position. Turn the PDP-11/05 key switch to the POWER position.

8. Set the SR to 166000_8. This is the starting address of the ROM Bootstrap program. Press LOAD ADRS and START.

9. The ROM Bootstrap program and the modem test connector function to echo data transmitted from the LK40 Keyboard to the GT40; when a key is pressed, the character it represents will be displayed on the VR14. Verify this operation by pressing any key on the keyboard and observing the display.

10. Additional verification of the ROM Bootstrap, DL11, BC05-C-25, and LK40 can be obtained by typing the program listed in step 11.

NOTE

Nothing will be displayed on the screen after } R until) is typed.

11. Type the following exactly:

}	R	}	L	@	@	@	@	@	@	D	@	G
(SP)	@	@	@	@	B	X	@	@	@	@	@	@
B	P	@	D	H	@	@	(sp)	C	(sp)	@	@	C
7	E	P	@	@	:	/	L	A	@	J	,	@
@	@	@	@	@	@	@	A	@	@	X	@	D
@	C	)										

(sp) = space

12. At this time a vector (Figure 4-21) is drawn on the CRT providing there were no typing errors. Retype the program if the display is incorrect.

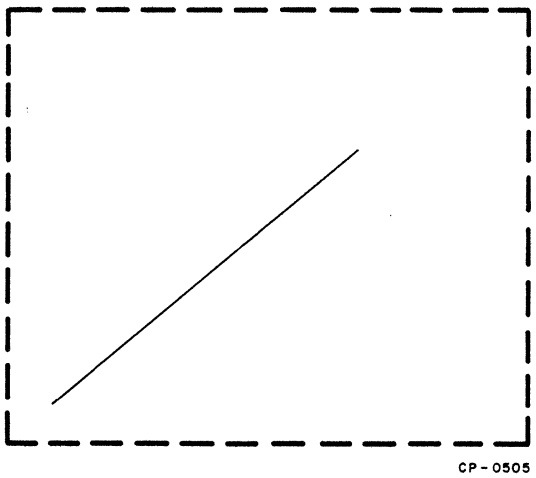


Figure 4-21 DL11, BC05-C-25, LK40, and ROM Bootstrap Quick Verification Display

13. Press HALT and turn the front panel key switch to the OFF position. Reposition the transmitter and receiver clock switches at their original positions (steps 2, 3, and 4). Remove the modem test connector from the BC05-C-25 Modem Cable and reconnect the cable to the null modem. Check all cable connectors and modules for secure connections.

14. Turn the front panel key switch to the POWER position.

4.2.7 Operational Programming

Although GT40 programming is not within the scope of this manual, several examples are presented (Tables 4-6, 4-7, 4-8, 4-9, and 4-10) to introduce the user to software control of the GT40. They are limited in the results obtained and are not meant to illustrate full GT40 capability.

4.2.7.1 Display Full-Size Rectangle – A program that will draw the largest possible size rectangle is presented in Table 4-6. This program is also used as the basis for the program extensions described in Paragraphs 4.2.7.2 through 4.2.7.4. Load the program and place 1000 in the SR; press LOAD ADRS and START. Press HALT if the display is satisfactory and proceed to Paragraph 4.2.7.2.

4.2.7.2 Display Full-Size Rectangle with Vector – This is modification of the display generated by the program in Table 4-6. A blinking dot-dash vector is drawn diagonally from the lower left corner of the rectangle to the upper right corner. With the basic program still in memory, load the additional steps (Table 4-7), place 1000 in the SR, and press LOAD ADRS and START. Note that the display jump in the previous program was deleted; however, the program still concludes with a jump instruction. Press HALT if the display is satisfactory and proceed to Paragraph 4.2.7.3.

4.2.7.3 Display Full-Size Rectangle with Vector and Graphic Data – The program currently in memory is again modified to display several graphic characters. Load the additional steps (Table 4-8) and press LOAD ADRS and START with 1000 in the SR. Press HALT if the display is satisfactory and proceed to Paragraph 4.2.7.4.

Table 4-6
Large Rectangle Program

Address	Instruction/Data	Mnemonic	Comments
1000	12737		Move starting address of display file to
1002	2000	MOV (7) +, @ (7) +	Display Program Counter (DPC).
1004	172000		
1006	000001	WAIT	Wait for interrupt (used here to keep CPU running)
2000	117224		Set point mode, no blink, solid line, intensity 5
2002	0		Unintensified point at 0,0 X=0
2004	0		Y = 0
2006	110000		Set long vector
2010	041777		X = 1777_8, intensify
2012	000000		Y = 0
2014	40000		X = 0, intensify
2016	1377		Y = 1377
2020	061777		X = -1777, intensify
2022	0		Y = 0
2024	40000		X = 0, intensify
2026	21377		Y = -1377
2030	160000		Display JMP to beginning of display file
2032	2000		

Table 4-7
Large Rectangle with Vector Program Modification

Address	Instruction Data	Comments
2030	110037	Long vector, dot-dash, blink
2032	041777	X = 1777_8, intensify
2034	1377	Y = 1377
2036	160000	Display JMP to beginning of display file
2040	2000	

Table 4-8
Large Rectangle with Vector and Graphic Data

Address	Instruction Data	Comments
2036	114024	Point mode, no blink
2040	1050	Unintensified point, X = 1050
2042	577	Y = 577
2044	100000	Character mode, no blink
2046	42506	E F
2050	42105	D E
2052	46440	M (sp)
2054	105	E
2056	160000	Display JMP to beginning of display file
2060	2000	

Table 4-9
Large Rectangle with Vector, Graphic, and Graphplot Data

Address	Instruction Data	Comments
2056	114000	Point mode
2060	40000	X = 0, intensify
2062	577	Y = 577
2064	174150	Load Status B, increment = 50
2066	124000	GRAPH Y mode
2070	700	Y data
2072	800	Y data
2074	900	Y data
2076	1000	Y data
2100	900	Y data
2102	800	Y data
2104	700	Y data
2106	600	Y data
2110	160000	Display JMP to beginning of display file
	2000	

Table 4-10
Ring Keyboard Bell Program

Address	Instruction/Data	Comments
1000	12737	Attempt write (0) to
1002	0	Status Register
1004	172002	
1006	137	
1010	1000	JMP to 1000

4.2.7.4 Display Full-Size Rectangle with Vector, Graphic, and Graphplot Data – The final modification to the program, started in Paragraph 4.2.7.1, causes graphplot data to be displayed in addition to the previously programmed data. Load the additional steps (Table 4-9) and press LOAD ADRS and START with 1000 in the SR. Press HALT if the display is satisfactory.

4.2.7.5 Program to Ring Keyboard Bell – This short program (Table 4-10) causes the keyboard bell to sound repeatedly. It is accomplished by attempting to write into the GT40 status register.

4.3 FAULT ANALYSIS AND REPAIR

4.3.1 Introduction

It is not possible to categorize and list all conceivable malfunctions that could occur in the GT40. However, the more obvious problems and their solutions can be stated. The fact that the majority of equipment failures result from the most likely causes should be considered when analyzing a problem. Finally, as noted previously, the best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the GT40.

4.3.2 Procedures and Equipment Required

If a malfunction occurs, the condition should be analyzed, isolated, and corrected as prescribed in the following paragraphs. No special test equipment or tools are required other than a Type 453 Tektronix oscilloscope, or equivalent, and a standard multimeter.

Table 4-11 lists common GT40 malfunctions and their repair.

CAUTION
Do not remove cables or modules with power on.

4.3.3 VR14 CRT Display Malfunctions and Repair

CAUTION
Due to the presence of high voltage, use extreme care when working on VR14 circuits.

4.3.3.1 No CRT Display – Probably the most common failure mode with this type of equipment is "no picture". Unfortunately, this condition can be caused by almost any malfunction such as a loss of input intensity pulse, incorrect input deflection signals driving the beam off the screen, a power supply fuse, or fan failure (thermal cutout). The following sequence of events leads to the isolation of the fault(s):

1. Check fuses. If they are in good condition, continue. If not, replace any that are blown and then continue. (If a blown fuse is replaced, leave power on only long enough to complete each check in this procedure.)

2. Remove all input signals at the rear of the unit and all modules except W684 and G836.

3. With a voltmeter (or oscilloscope) measure the +20 Vdc (20 Vdc to 22 Vdc is acceptable). This can be measured between B01-V (red wire) and B01-M, which is ground. Momentarily apply and shut down power. If the +20V is above +22V, the regulator has a fault (Paragraph 4.3.3.3). If 0V or below +20 Vdc occurs, the +20V is overloaded; continue to the next step.

4. Set up to measure -20V. This can be found between B01-R (blue wire) and B01-M, which is ground. Momentarily apply and shut down power. If the -20 Vdc is above -22 Vdc, the -20V regulator has a fault (Paragraph 4.3.3.3). If 0V or below -20 Vdc, the -20V is overloaded; continue to next step.

Table 4-11
Fault Analysis and Repair

Fault	Procedure	Repair
No picture on CRT monitor	1. Check the rear panel circuit breaker.	1. Reset the circuit breaker if it is tripped.
	2. Ensure proper CPU operation by running appropriate CPU diagnostics.	2. Replace or repair CPU boards.
	3. Ensure proper DPU logic operation by running instruction tests.	3. Replace or repair DPU boards.
	4. Ensure proper DPU analog operation by running Visual Display test (MAINDEC-11-DDGTC-A) and observing the analog waveforms on pins B (CGS Y OUT) and J (CGS X OUT) of the Berg connector on the A320 (drawing A320-MC).	4. Replace or repair the A320. If Z axis (GM INTENSITY OUT L) is not correct, check intensity logic in the M7014 module. (This signal is also routed through the M7013 module.)
	5. Check CRT monitor operation (Paragraph 4.3.3).	5. Replace or repair as required.
Keyboard not working	1. Check ON/OFF switch on rear of keyboard.	1. Switch to ON position.
	2. Check cables on the VR14 rear panel.	2. Seat cables properly.
	3. Open the LK40 and check for +5V on the M7011 module.	3. Check cables run back to the CPU box.
	4. Measure -22V on the M7011 module.	4. Check cable run to VR14.
	5. Measure -12V on pin 2 of the UART on the M7011 module.	5. Check Zener diode D2 on the M7011 module.
	6. Check serial data line for data when key is pressed.	6. Check continuity back to the CPU box.
	7. Check TTY clock in the CPU and LK40.	7. Adjust for proper timing.
	8. Strike a "Shift A" on the keyboard. Check location 177562_8 for a 301_8 code.	8. Check CPU for proper operation.

Table 4-11 (Cont)
Fault Analysis and Repair

Fault	Procedure	Repair
CRT monitor does not turn on with system (red front panel light is off)	1. Ensure ON/OFF switch on the front panel is on.	1. Turn to the Power position.
	2. Ensure AC plug is securely seated in AC receptacle.	2. Seat AC plug.
	3. Check 5 amp SB fuse (115V systems) on rear chassis of CRT monitor (3 ASB for 230V systems).	3. Replace fuse.
	4. Check 10A (5A for 220V) fuse on the VR14 power control box.	4. Replace fuse.
	5. Ensure Berg connector is securely seated in TTY connector on the processor box.	5. Properly seat Berg connector.
	6. Check for +15V at pin U of the TTY Berg connector.	6. Trace power from supply to cable in processor box.
Light pen does not operate	1. Check for tight connection of the light pen, cable, and front panel jack.	1. Seat connectors properly.
	2. Load Instruction Test 2 (MAINDEC-11-DDGTB-A) and display pattern 7. Aim light pen at the top line (intensity 7) and check for pulse at pin JJ (GM INTENSITY OUT L) of the Berg connector on the A320 module.	2. Check the G840 module in the VR14. Check scope cable (Figure 3-70).
	3. Check for light pen flag (drawing M7014-LEI).	3. Check and repair the light pen circuitry in the DPU.
No communication with host computer	1. Ensure transmit and receive baud rate switches on the DL11 module are set properly.	1. Set switches to equal line baud rate.
	2. Set 166000_8 into the SR. LOAD ADRS and START. Ensure CPU is running.	2. Run CPU diagnostics.
	3. Check ROM Bootstrap program by comparing memory contents with Appendix D.	3. Check bootstrap logic on M7014.

Table 4-11 (Cont)
Fault Analysis and Repair

Fault	Procedure	Repair
No communication with host computer (cont)	4. Set transmit and receive switches to same baud rate. Disconnect BC05-C-25 cable from modem and place a modem test connector on the end of the cable. Perform the Character Echo Check (Paragraph 4.2.6.7). Type on LK40; characters should appear on the screen.	4. Run DL11 diagnostics. Check BC05-C-25 cable. Check LK40.

5. With an oscilloscope or meter, measure ±2.2V maximum at A02-A with respect to ground (B01-M). This point (A02-A) is the X axis deflection coil current sample. Because coil current flows through a 0.5 ohm resistor, voltage measured at A02-A multiplied by two equals the current flowing. With the A225 circuit cards removed, no coil current should flow. Momentarily turn on power to the VR14. If A02-A has any voltage plus or minus (Paragraph 4.3.3.4), a deflection power transistor is shorted.

6. Measure the same as in step 5 for the Y axis deflection coil current at A03-A with respect to ground (B01-M). Again, momentarily turn VR14 power on and off. No voltage should be read; this indicates no Y axis deflection coil current is flowing. If any voltage is observed, refer to Paragraph 4.3.3.4, since a Y axis deflection transistor is probably shorted.

7. Replace the G840 circuit into A01 and the A225 circuit into A02. (Still leave the Y axis, A03 board out.) Measure less than ±2.2V at pin A02-A with respect to ground (B01-M). Momentarily apply power. If the voltage is within safe limits (less than ±2.2V), leave power on and adjust the position potentiometer on the A225 circuit. Doing this should change the voltage reading on A02-A, proving the A225 indeed is controlling the coil current. Return the position potentiometer to its original position. If the voltage at A02-A is beyond ±2.2V, shut down immediately. Because the position potentiometer on the A225 can drive more current than the ±2.2V limit, it is possible that it (the position potentiometer) has been adjusted to one extreme or the other. To prove whether this is the case or if the A225 circuit board is faulty, turn the position potentiometer as follows: clockwise if the voltage at A02-A was very negative; counterclockwise if the voltage at A02-A was very positive. If no change is noted at A02-A after adjusting the position potentiometer, the A225 board is faulty and should be replaced or repaired (Paragraph 4.3.3.5).

8. Repeat the same tests as in step 7 for the Y axis deflection circuit A225 plugged into A03. Monitor A03-A. Refer to Paragraph 4.3.3.5 for A225 repair.

9. If the fault has not been isolated, the intensity circuit, W684, the electrode voltages, and the high voltage supply are suspect. The output of the W684 drives the cathode. At rest, it should be +60V and, when triggered, go to approximately 0V. Apply a proper input to the W684 (+3V to 0V transitions) and check to see that the signal reaches A04-J. See that +5V is being supplied to A04-A. If A04-A is less than +4V, replace or repair the G840 module as this is where the +5V is developed. If the two preceding measurements are good and the W684 output (measured at B04-L) is not going from +60V to 0V for at least 300 ns, repair or replace the W684 module.

10. Measure 6.3 Vac between B04-A and B and observe the flowing filament on the CRT. No 6.3 Vac can be traced back to the G836 circuit which routes the 6.3 Vac from the transformer.

11. Measure the grid 1 voltage at B04-F. It should vary from -80 Vdc to between -20V and 0V when the front panel brightness control is varied. The -80 Vdc comes from the G836 board. Trace back to the G836.

12. Measure G2 at B04-D. It should be at least +300V. Trace back to the G836.

13. The final problem source for a no picture condition is the high voltage supply itself. Generally, all other measurements should be made before considering the high voltage, since the majority of "no picture" conditions will not be caused by the high voltage supply. Measuring the high voltage is extremely dangerous and not recommended. Instead, a quick method is to take a long screwdriver and ground the blade with two separate clip leads for safety. Turn the VR14 on for 5 seconds and then **SHUT IT OFF**. After it is off, ground out the anode cap on the CRT with the **GROUNDED** screwdriver. If done within 5 to 10 seconds after power is turned off, an arc, to the screwdriver, should occur, indicating that the CRT was charged with high voltage. If no arc occurs, replace the high voltage supply.

4.3.3.2 Faulty Picture –

a. No Focus – Check the range of the focus potentiometer on the G836 by monitoring the focus voltage at B04-J while adjusting the focus potentiometer through its range. Minimum range is +350 Vdc to -60 Vdc. See G836 for repair.

b. Half or Quarter of the Picture Missing – Generally, this condition represents the fact that one of the two deflection transistors is not working; thus, only half deflection is available. The transistor in question can be identified by observing which side of the screen is not working. The left and bottom portions of the screen are controlled by the PNP (2N4399) power transistors on the deflection heat sink. These are the two lower transistors; the left side of the screen is controlled by the left lower transistor (if the deflection heat sink is viewed from the front of the VR14), the lower part of the screen is controlled by the right lower power transistor. Of course, the upper and right are controlled by the NPN (2N5302), the right side of the heat sink controlling the upper screen, the left side of the heat sink controlling the right screen.

c. The remaining possible faulty picture patterns such as picture swim (60 Hz), oscillations, distortion, etc., will be restricted generally to improper input signals (especially grounding techniques) or faults on the A225 circuit board. If input signals are not suspected, a faulty A225 may be isolated by swapping X and Y A225s with one another to see if the problem changes axis.

d. If a weak picture that is deflected off the screen on all sides is encountered, with excessive jitter and ripple, replace the high voltage supply.

4.3.3.3 Power Supply and Regulator Troubleshooting –

NOTE

The power regulator heat sink contains a thermal cutout connected to the input line voltage. Always remove the line cord before handling the heat sink.

Generally, if the ±20V reads above ±25V, one or both of the regulator transistors has shorted. The +20V is controlled by the PNPs (2N4399) that are the front set of transistors on the regulator heat sink (as viewed from the front of the VR14). The -20V is controlled by the NPNs (2N5302) on the rear section of the regulator heat sink. If, after replacing the power transistors, the problem is not corrected, the G836 board itself is suspect. If the regulator circuits are not working, the output could be beyond its nominal value. The MC1709 is most likely suspect, followed by the drive transistors, 2N4923 for +20V and 2N4920 for -20V.

If, on the other hand, the ±20V reads zero, the same power transistors are still suspect (they may be open). Also, in this case, if the two 1N4001 diodes used as current limiting for the power transistors are shorted, the power transistors cannot receive base current and thus will not turn on, rendering their output 0V. To check for this condition, turn off the power and measure resistance with a VOM set at RX1 across D15 and D16 if the +20V was 0, and D13 and D14 if the -20V was 0. The resistance with the VOM lead connected either way should always be above 5Ω.

4.3.3.4 Deflection Power Transistors Troubleshooting – When the deflection circuit cards (A225) are removed, their respective power transistors receive no drive and, therefore, are off. When monitoring A02-A (X yoke current sample) and A03-A (Y yoke current sample) no reading should be observed. Any voltage at these points indicates a power transistor is on by itself. Generally this transistor is shorted. To determine which transistor is faulty, observe which pin, A02-A or A03-A, has voltage. The A02-A (X axis) transistors are on the right side of the heat sink assembly when viewed from the front of the VR14; A03-A (Y axis) transistors are on the left side. In both cases, a plus voltage at A02-A or A03-A means the PNP (2N4399) is at fault. This is the lower transistors on both sides. If the voltage at A02-A or A03-A is minus, the NPNs (2N5302) are faulty. These are the upper transistors on both sides.

If no readings are observed at A02-A or A03-A when the A225 boards are removed, then the deflection fault is on the boards themselves (assuming, of course, proper input signals are applied and all power supply voltages are nominal). If the yoke current goes full negative only when the A225 card is plugged into that axis, the most likely suspect is the 2N2904A, Q2. If one axis is faulty, a quick check can be made by swapping the X and Y deflection boards (A225) to see if the faulty axis follows the circuit board in question.

4.3.3.5 Deflection Amplifier (A225) Troubleshooting – After the power supply and deflection power transistors have been proven sound, incorrect deflection coil current readings may be isolated to the A225 circuit board itself. If, when the A225 is plugged in, the deflection current goes full negative (about -4V as measured at A02-A for X, A03-A for Y) and not controllable, Q2 has probably opened and should be replaced. If only half deflection is working (no positive current or no negative current capability) and the power transistors are operating properly, Q3 should be replaced for no positive current and Q4 for no negative current. Also, check R26 and R27 for burns. These resistors overheat if the deflection amplifier is operated in the fault current limit condition for any length of time. Finally, if C9 or C10 become shorted, R9 or R10, respectively, will burn out. Check C9 or C10 with an ohmmeter to verify this type of failure.

4.4 ASSEMBLY REPLACEMENT INSTRUCTIONS

4.4.1 VR14 CRT Display

Other than the G840, A225s, and W684 circuit modules, most repair and replacement will involve the G836 Regulator Subassembly; the regulator heat sink assembly; and the deflection heat sink assembly; and, in rare cases, the high voltage assembly, yoke, and CRT. It cannot be stressed too strongly that the VR14 line cord be removed from the line before doing any maintenance. Turning power off or removing fuses does not render the unit safe from shock hazards, since the power switch and fuse interrupt only one side of the ac input line voltage, the other side is permanently connected as long as the line cord is plugged in. Do not take chances, unplug the line cord.

NOTE

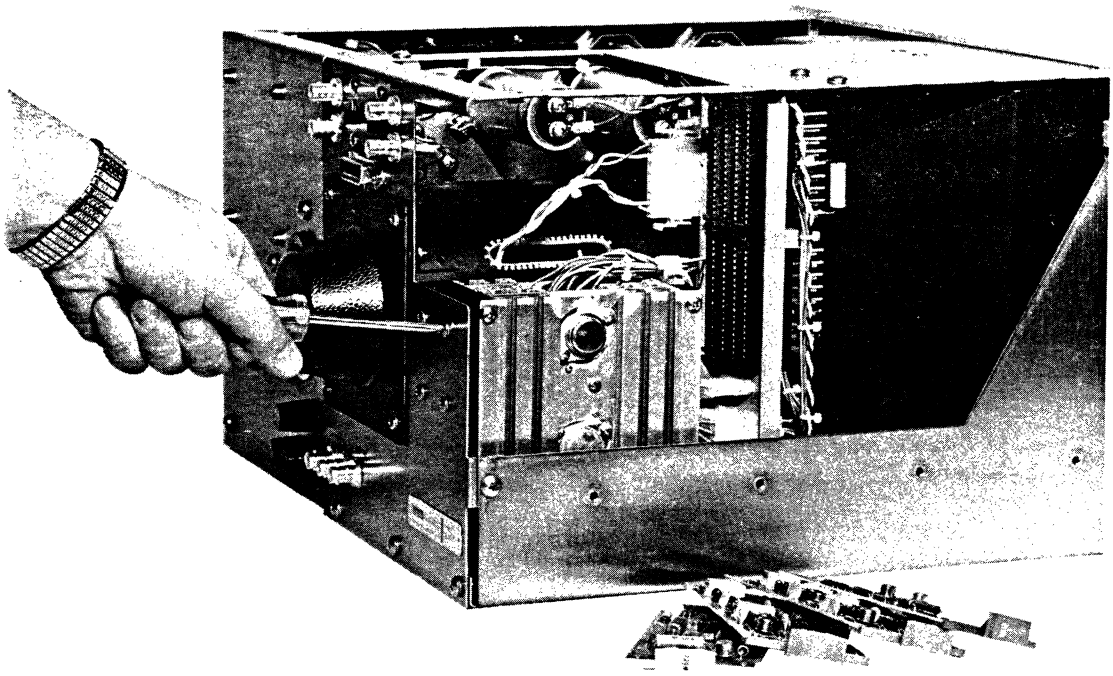
Although the accompanying photographs (Figures 4-22, 4-24, and 4-25) show a VR14 without GT40 modifications, they are still applicable to these procedures.

4.4.2 Deflection Heat Sink Removal (Figure 4-22)

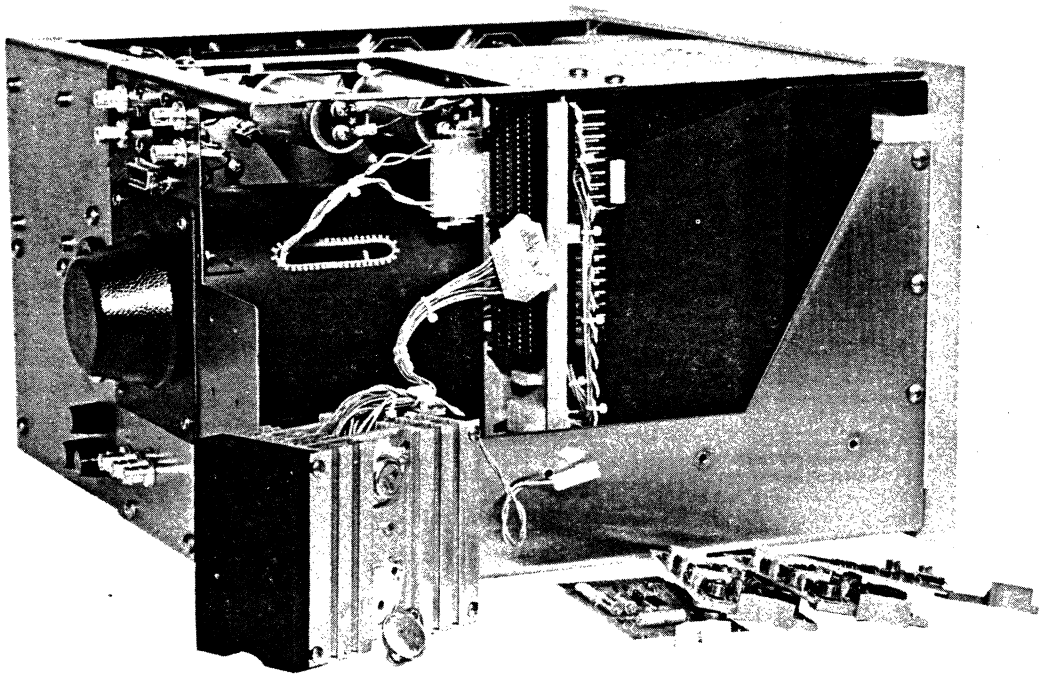
To remove the deflection heat sink, proceed as follows:

1. Remove the line cord and all circuit modules above the deflection heat sink assembly (G840, A225, A225, W684).

2. Remove the four 6-32 screws that hold the heat sink assembly to the rear chassis plate.



a. Remove circuit boards and the four 6-32 screws holding the deflection heat sink to the rear panel.



b. Remove heat sink assembly (and its connectors, if necessary) and remove faulty power transistor.

Figure 4-22 Deflection Heat Sink Removal

3. Lift the assembly out to make room for removing the assembly cable connector. The 15-pin connector is removed by squeezing the retaining tabs on each side of the connector so that when the connector is pulled, the tabs pass through square holes that they were butted against. Do not pull the connector by its wires, only by its plastic body.

4. To remove a faulty transistor, unscrew the two 6-32 screws that hold the transistor down. Then pull the transistor straight out from the socket. Apply an even coat (approximately 1/32 in. thick) of thermal compound to all mating surfaces of the new transistor. Replace the new transistor, making sure that the base and emitter pins are oriented properly; otherwise, the transistor case will not align with the two screw holes. Also, ensure that the insulating washer is between the transistor and the heat sink and each mounting screw has a star washer.

4.4.3 7007165 Power Regulator Assembly Removal

The 7007165 Power Regulator Assembly comprises a G836 regulator printed circuit board with a mounting frame for J1, J2, J3, and J4. To remove the 7007165 Power Regulator Assembly proceed as follows:

1. Remove the line cord and all circuit modules (G840, A225, W684).

2. Remove all four cable connectors (Figure 4-23) coming into the connector bracket on the 7007165 by squeezing the two locking tabs on the sides of each connector, while pulling the connector straight up, allowing the locking tab to pass through the square holes they were butted against. Do not pull the connector by its wires; only by its plastic body.

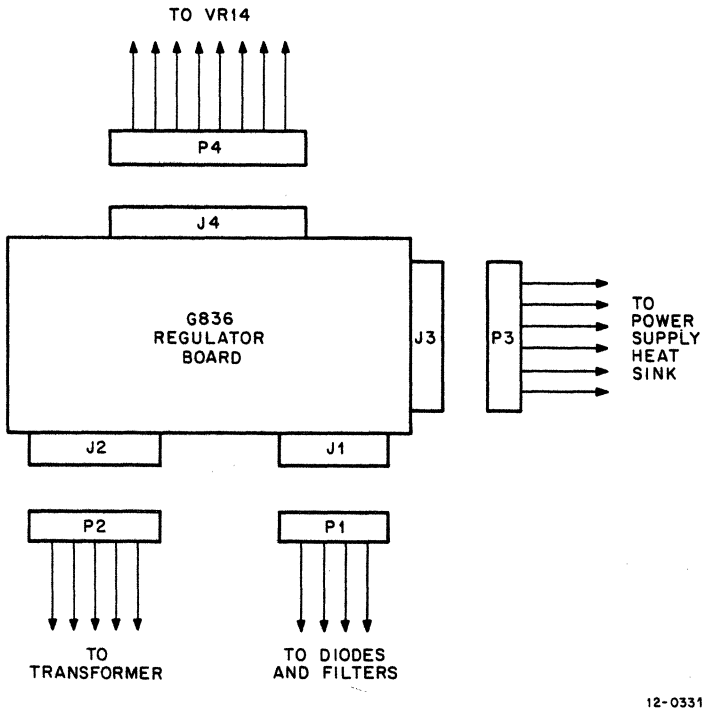


Figure 4-23 7007165 Power Regulator Assembly

3. Remove the two mounting screws for the 7007165 from the opposite side of the 7007165 chassis wall.

4. The 7007165 is now free and can be pulled straight out.

NOTE

When placing the 7007165 back into the unit, ensure that the bottom of the circuit board rests in the slotted groove insulator block provided on the bottom chassis.

5. For troubleshooting, the 7007165 may be operated outside its normal mounted position by laying the board flat and reconnecting the four cable connectors. Ensure that the etch side of the module does not touch the chassis causing short circuits by insulating the board with a book or a piece of cardboard as shown in Figure 4-24b.

NOTE

The 7007165 has +80 Vdc, -80 Vdc, and +400 Vdc available. Use extreme caution when troubleshooting the board. Also, these voltages do not disappear immediately when power is shut off.

4.4.4 Regulator Heat Sink Removal (Figure 4-25)

To remove the regulator heat sink, proceed as follows:

1. Remove the 7007165 (Paragraph 4.4.3).

2. Remove the four heat sink mounting screws on the right chassis wall (when viewed from front).

3. Lift the heat sink assembly straight out.

4. To remove a faulty transistor(s), unscrew the two 6-32 screws holding the transistor(s) down; then pull the transistor(s) straight out from the socket. Apply an even coat (approximately 1/32 in. thick) of thermal compound to all mating surfaces of the new transistor. Replace the new transistor, ensuring that the base and emitter pins are oriented properly; otherwise, the transistor case will not align with the two screw holes. Also, ensure that the insulating washer is between the transistor and the heat sink and that each mounting screw has a star washer.

4.4.5 Yoke and CRT Removal

To remove the yoke, proceed as follows:

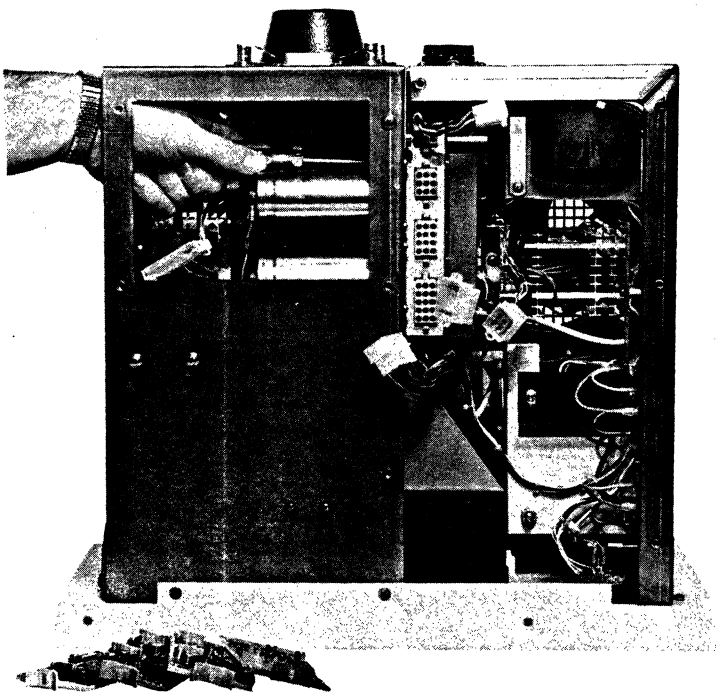
1. Remove the line card and all the circuit modules (G840, A225, W684) along with the plastic CRT socket cover.

2. Carefully remove the yoke cable connector from its mating connector on the inner side of the circuit card mounting bracket.

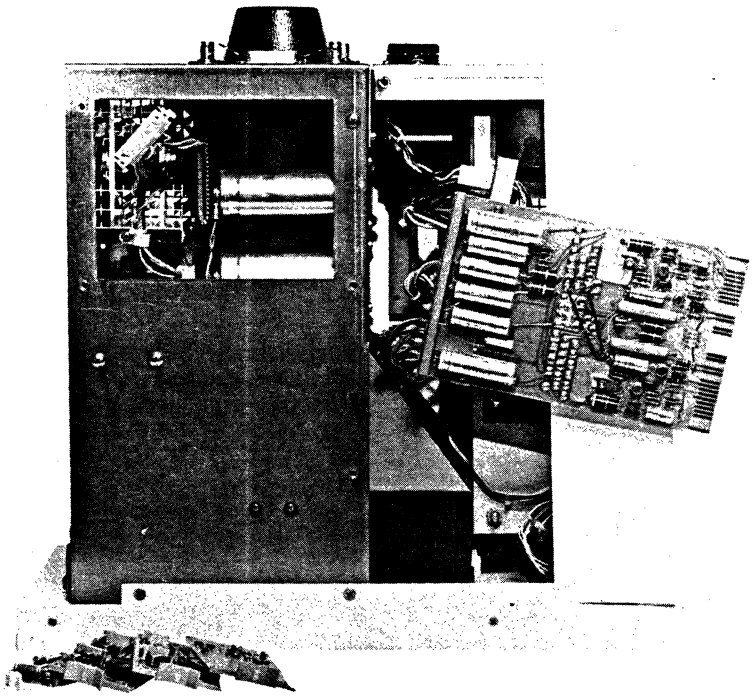
3. Using a 1/4-in. nut driver, loosen the screw that holds the yoke neck clamp by inserting the nut driver through the access slot provided in the CRT shield. Loosen sufficiently for the yoke clamp to be slipped off the yoke.

4. Carefully remove the CRT socket connector and slide the yoke clamp off the CRT neck.

5. Slip the yoke connector through the access slot in the CRT shield and pass it, along with the entire yoke assembly, off the CRT neck and out the rear. Sometimes the yoke gets stuck at the socket end of the CRT because the yoke plastic mounting piece hugs the CRT neck tightly and must be spread to pass over the CRT socket.

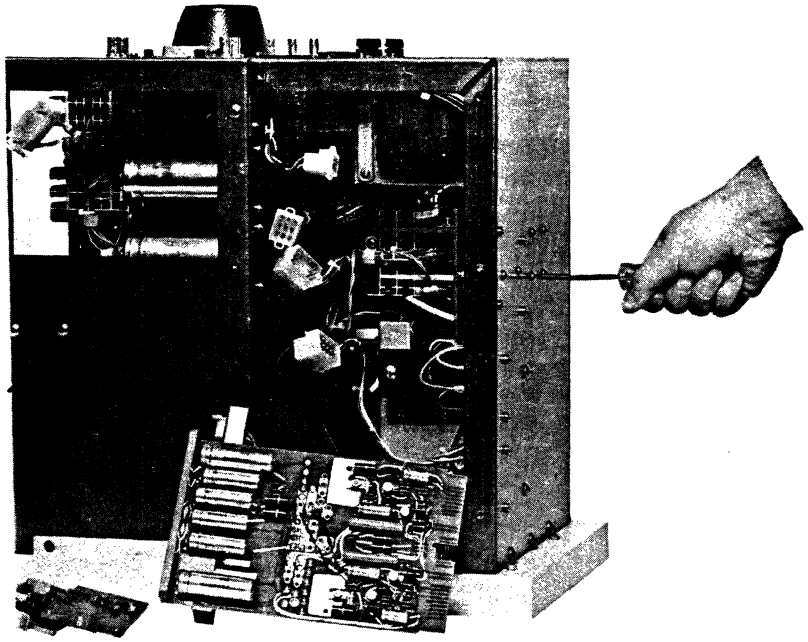


a. Remove power cord and all connectors to the 7007165. Unscrew mounting screws from the opposite side of the vertical chassis wall.

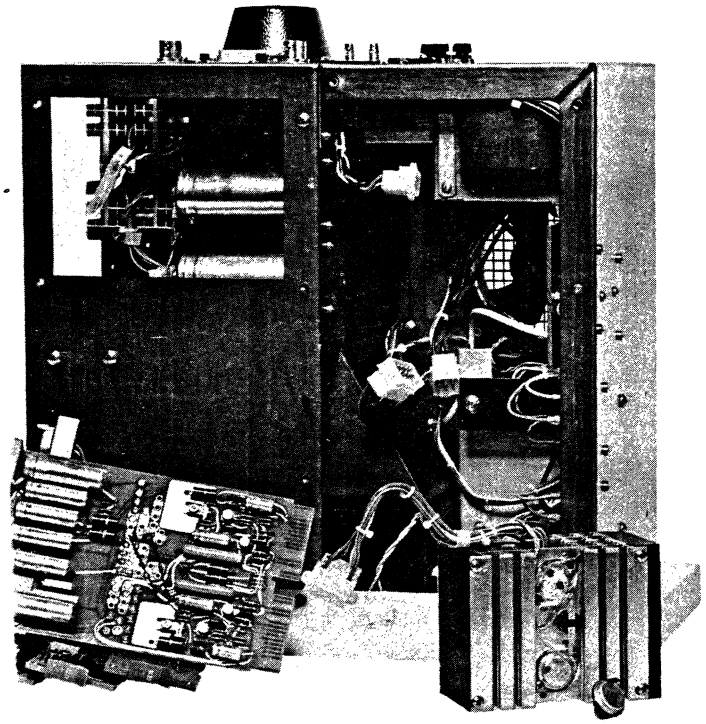


b. Reconnect connectors and place a cardboard under the 7007165 to prevent shorting out the circuit against the chassis when troubleshooting the board outside the unit.

Figure 4-24 7007165 Removal



a. Remove the 7007165 as shown in Figure 4-4 and unscrew the four 6-32 heat sink mounting screws from the side chassis. Remove two pin connector from high voltage bracket.



b. Lift heat sink straight out and repair faulty transistor.

Figure 4-25 Regulator Heat Sink Removal
(Note: Thermal cutouts have 115 Vac on them – be sure line cord is removed)

To remove the CRT, proceed as follows:

1. Remove the yoke first as described above and double check that the line cord is removed.

2. With a long-bladed screwdriver, that is grounded to the chassis (a clip lead between the screwdriver blade and chassis plus a second clip lead for safety is adequate), slide the blade under the rubber cup on the high voltage connection at the CRT and touch the anode connection to discharge any remaining high voltage. At the same time, remove the high voltage connection. The connection is made by two stiff wires that each have a bend or hook on the end. The connection at the CRT is made by squeezing these two wires together so they can fit in the CRT metallic hole. Then these two wires are let go so they can expand and grab the inner lip of the CRT with the hooked ends. The connection is removed by squeezing the "hook wires" together and, at the same time, pulling them out so that the wires can clear the anode hole.

3. Remove the CRT plastic mask by removing the top and bottom screws from the front bezel casting.

4. The CRT is held by four screws, one in each corner of its shell bond frame. As each screw is removed, support the weight of the CRT.

CAUTION

The CRT is under high vacuum and may implode if subjected to sharp blows or very rough handling.

Also, to avoid dropping the CRT accidentally, never place your hand over the anode high voltage button while picking up or carrying the CRT, in case the CRT has residual charge. The shock is not, in itself, dangerous but the surprise may cause the user to drop the CRT. Never hold the CRT by the neck (the thin cylindrical portion) alone since it can break off.

4.4.6 High Voltage Supply Removal

To remove the high voltage supply, proceed as follows:

1. Remove the yoke and CRT as outlined in Paragraph 4.4.5. Ensure that the line cord is unplugged.

2. Disconnect the two red and two white wires from the high voltage supply from the TB1 and TB2 of the right side chassis.

3. Remove the cast bezel by removing the three right and left retaining screws.

4. Remove the two side and two bottom high voltage assembly mounting bracket screws and move the high voltage assembly out toward the front of the unit.

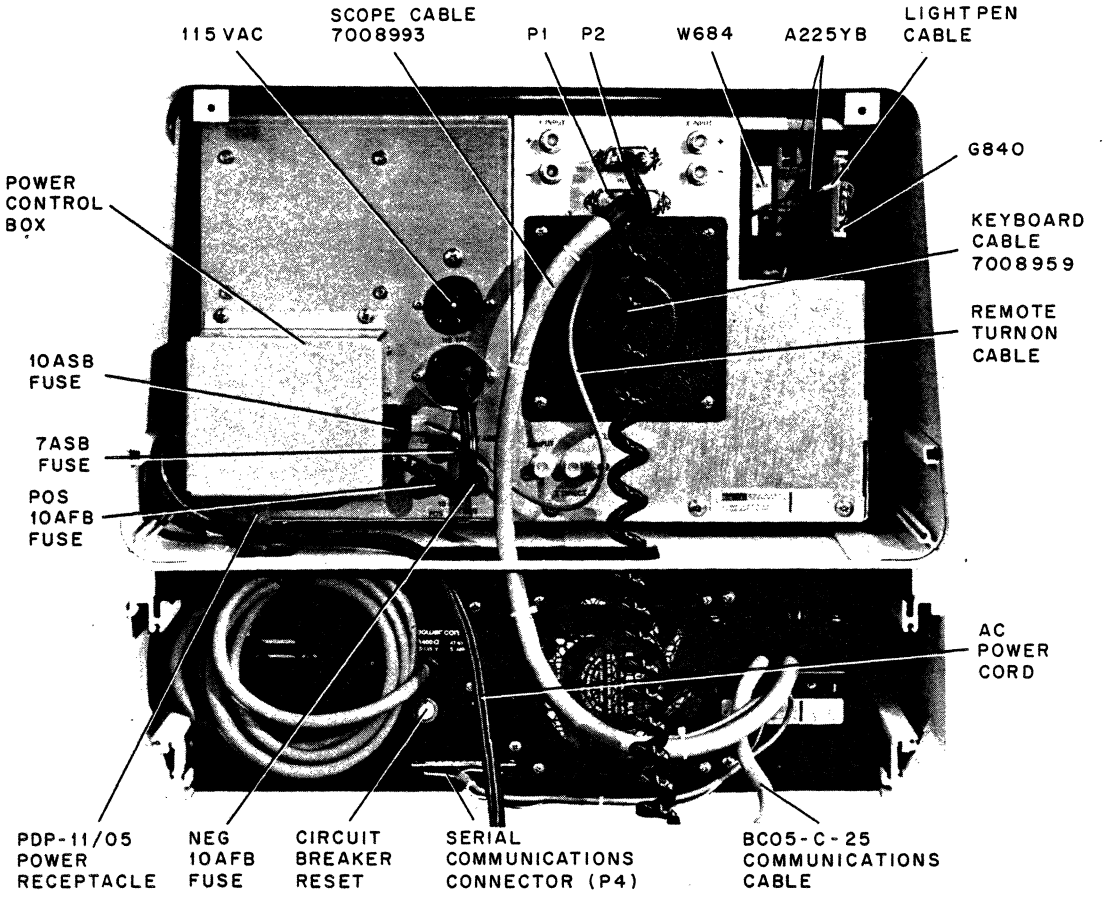


Figure 4-26 GT40 Exterior View, Rear

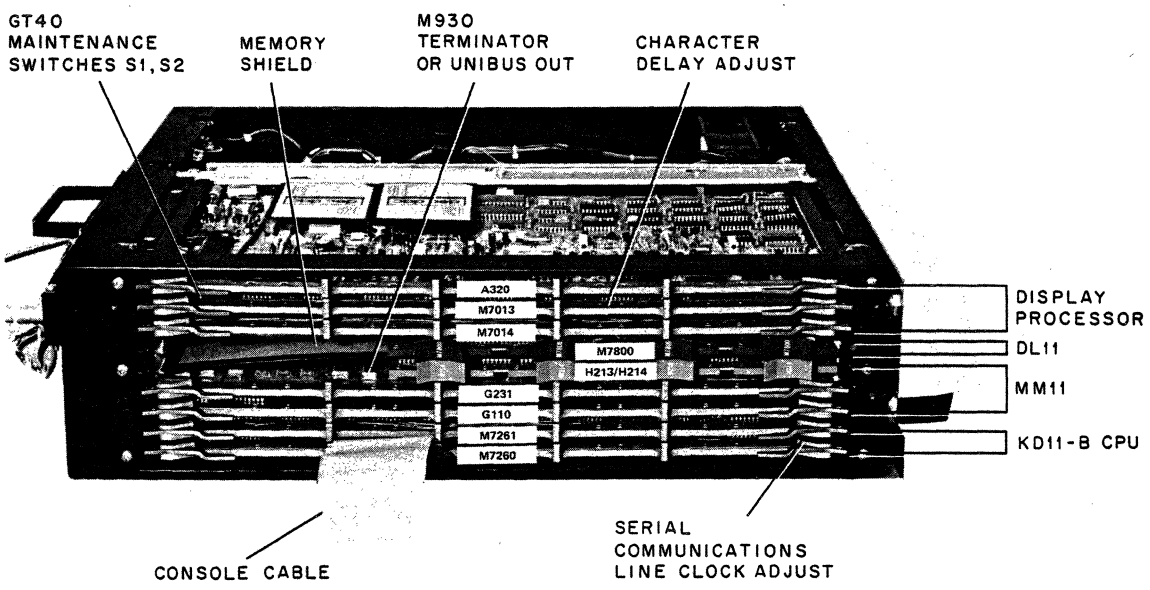


Figure 4-27 GT40 Interior View, Left

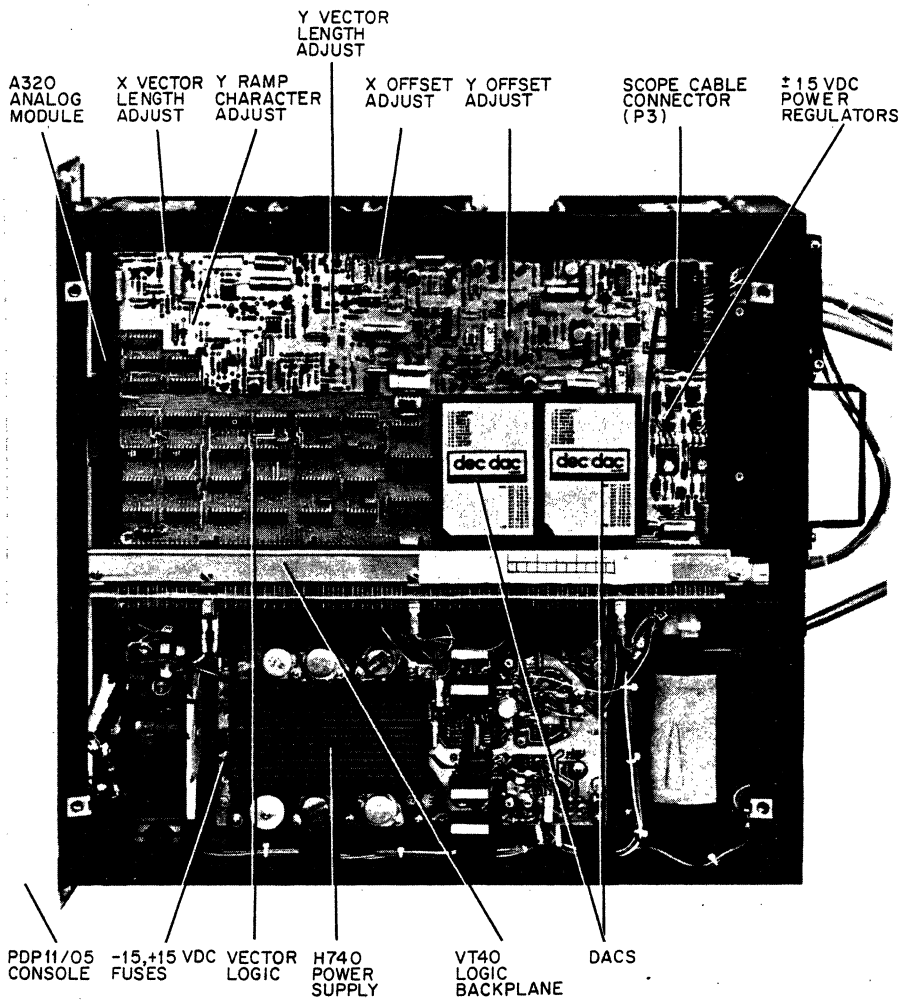


Figure 4-28 GT40 Interior View, Top

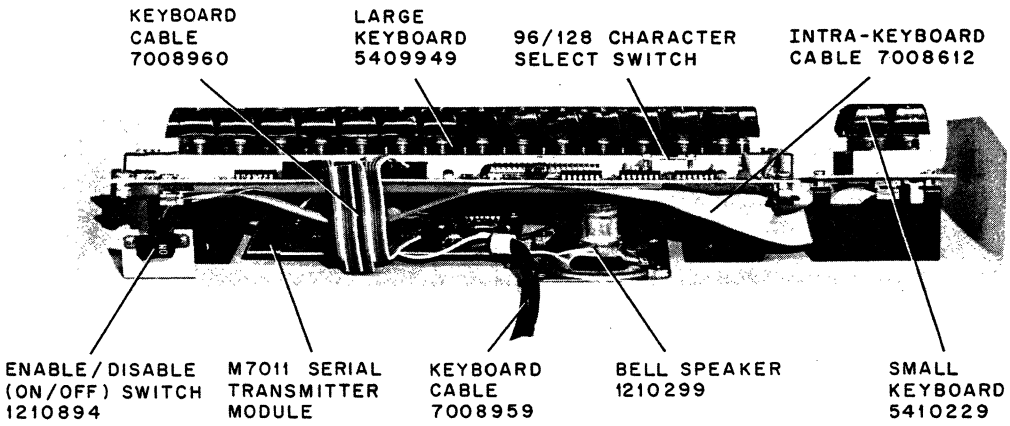


Figure 4-29 LK40 Keyboard Interior View, Rear

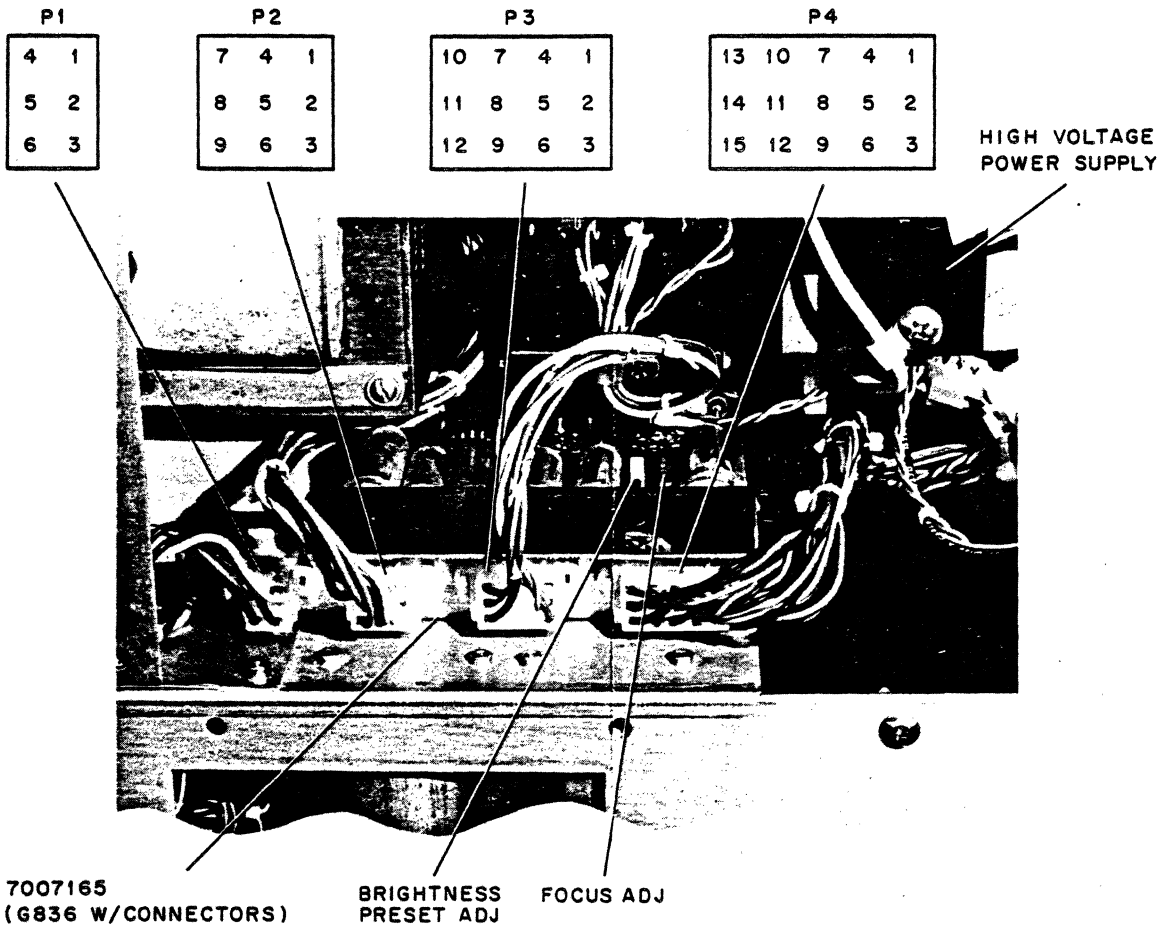
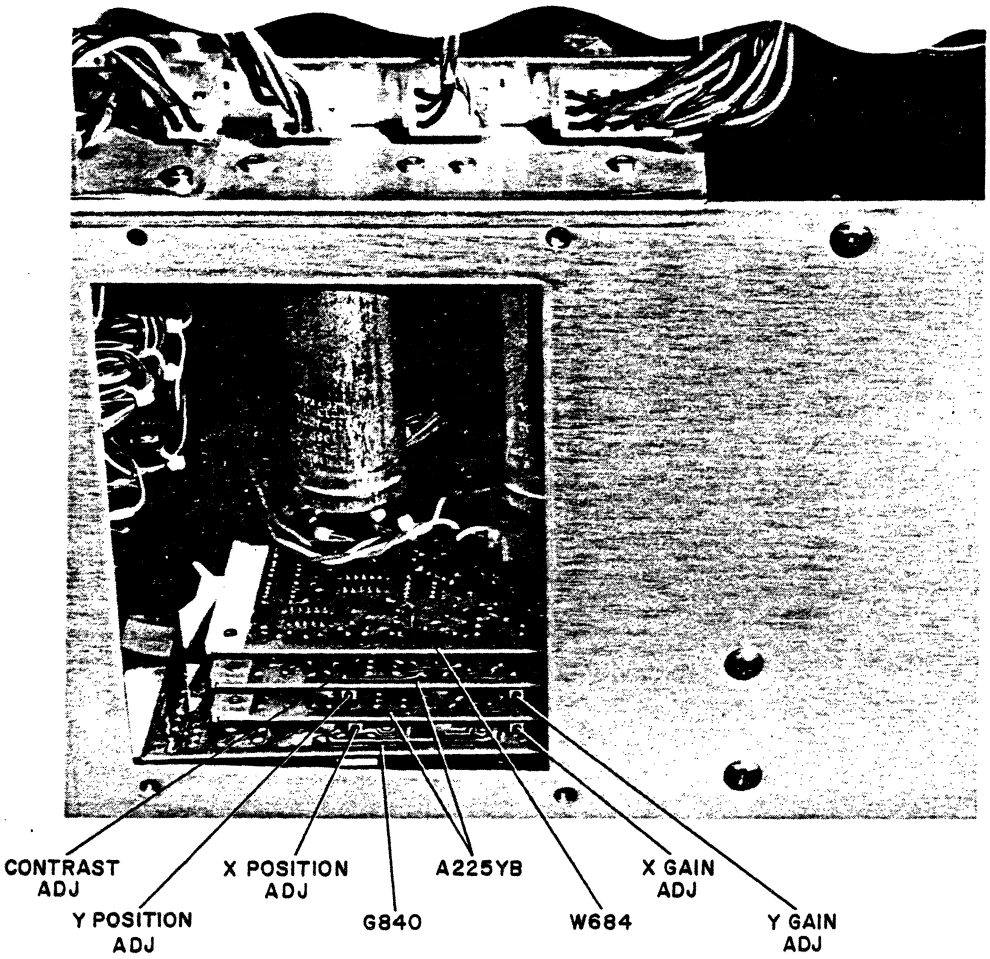


Figure 4-30 VR14 CRT Display Interior View, Top


CONTRAST ADJ
Y POSITION ADJ
X POSITION ADJ
G840
A225YB
W684
X GAIN ADJ
Y GAIN ADJ

CHAPTER 5
GT40 ENGINEERING DRAWINGS AND RELATED DOCUMENTS

5.1 APPLICABLE ENGINEERING DRAWINGS

A complete set of drawings is supplied with each GT40 Graphic Display Terminal. If any discrepancies are noted between the description in this manual and the drawings supplied with the equipment, consider the drawing set supplied with the equipment as reflecting the most accurate equipment representation.

5.2 DRAWING CODE

DEC's engineering drawings are coded to designate drawing type, major assembly, and series. A drawing number such as D-CS-M7013-0-1 reveals the following information.

D	–	Drawing Size
CS	–	Drawing Type (Circuit Schematic)
M7013	–	Equipment Type
0	–	Equipment Variation
1	–	Drawing Number of a Series

5.3 GT40 ENGINEERING DRAWINGS

Table 5-1 lists the major drawings for the GT40. Refer to the current Drawing Directory for a complete, up-to-date

Table 5-1
GT40 Engineering Drawings

Drawing Number	Title
D-MU-VT40-0-1	Module Utilization
D-BD-GT40-0-4	GT40 Block Diagram
D-IC-GT40-0-3	GT40 Back Panel Connections
D-UA-VR14-0-0	VR14 Assembly
D-AD-7008930-0-0	VR14 Power Control Box
D-IC-VR14-0-1	VR14 Block Schematic
D-CS-W684-0-1	VR14 Intensity Module
D-CS-G840-0-1	Light Pen Amplifier
D-CS-A320-0-1	GT40 Display Generator
D-CS-M7013-0-1	GT40 Display Control
D-CS-M7014-0-1	GT40 Bus Control and Bootstrap
D-SP-GT40-0-2	GT40 Base Diagrams
D-CS-M7800-0-1	DL11 Asynchronous Interface
D-TD-GT40-0-16	Character Generator Timing
D-FD-GT40-0-5 through -14	GT40 Flow Diagrams
D-UA-LK40-0-0	LK40 Keyboard Assembly
D-CA-M7011-0-1	Keyboard Serial Transmitter

5.4 RELATED PUBLICATIONS

Table 5-2 lists those publications that contain related information of interest to the GT40 user.

Table 5-2
Related Documentation

Title	Number	Subject
Paper-Tape Software Programming Handbook	DEC-11-GGPC-D	Programming
PDP-11 Processor Handbook		Programming
MACRO-11 Assembler Program Manual	DEC-11-OMACA-A-D	Programming
GT40 Users Guide	DEC-11-HGTGA-A-D	Programming and Operation
GT40 Users Manual	DEC-11-GGTGA-A-D	Programming
Introduction to Communications		Communications (Basic)
Peripherals and Interfacing Handbook		Interfacing

APPENDIX A
KEYBOARD CONFIGURATION

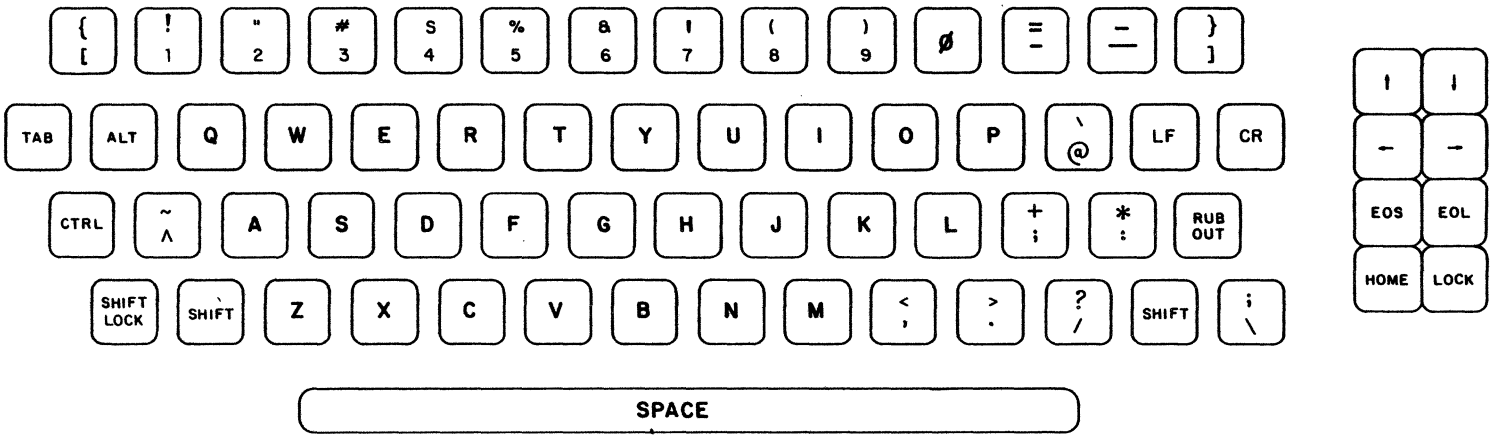


Figure A-1 Keyboard Key Configuration

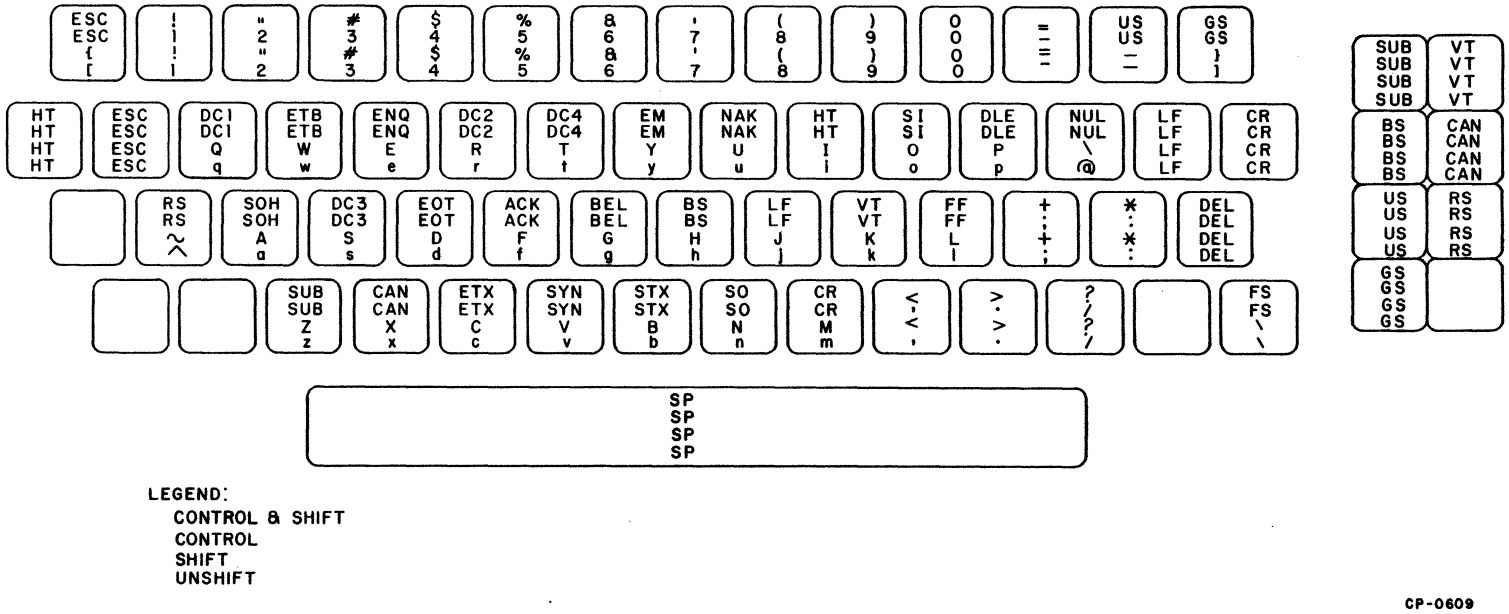


Figure A-2 128-Character Keyboard (Position 1)

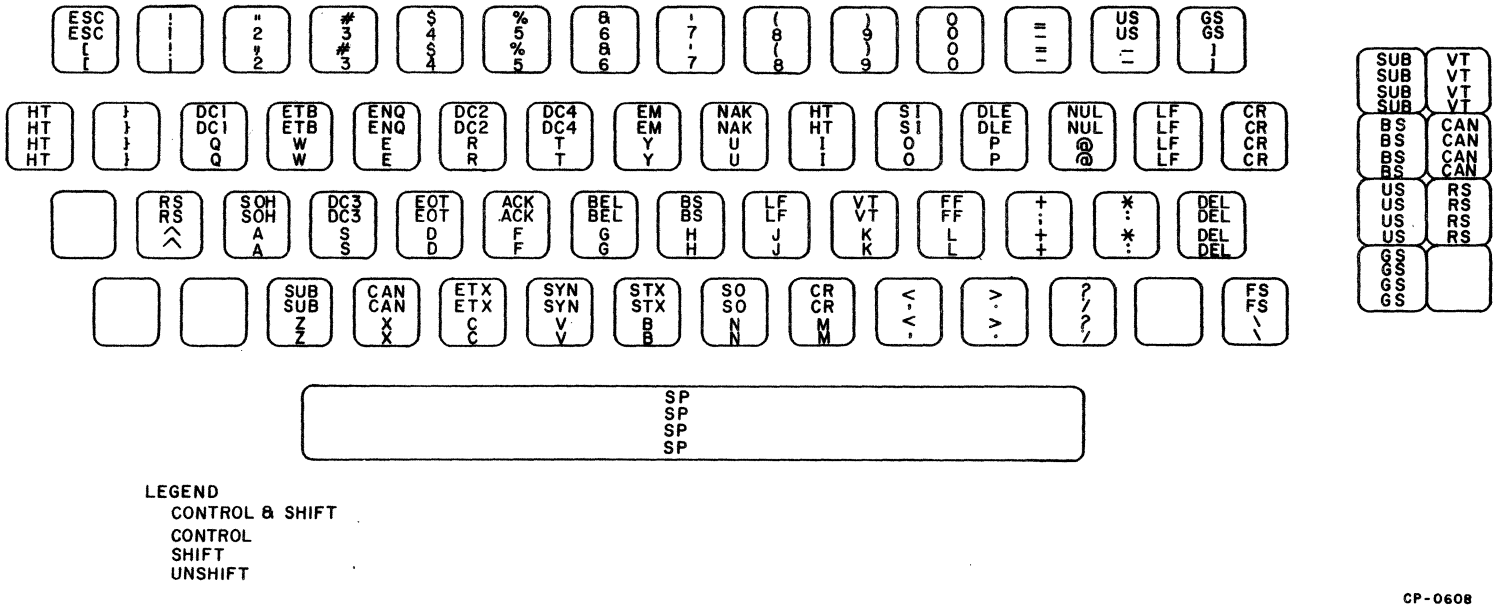


Figure A-3 64-Character Keyboard (Position 2)

APPENDIX B
ADDRESS MAPPING

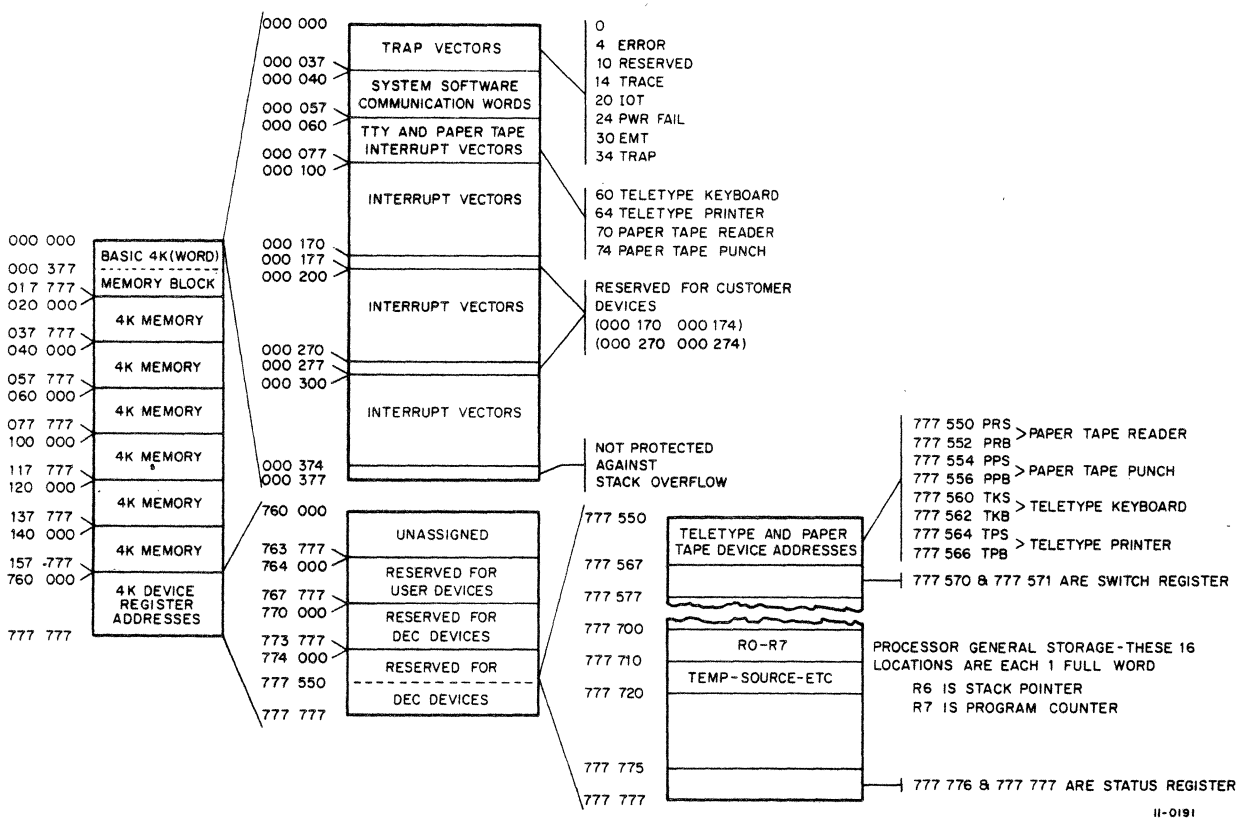


Figure B-1 Address Mapping

APPENDIX C
CHARACTER CODES

7 Bit (octal)	ASCII Representation	Keyboard	GT40 Printing	GT40 Printing When Preceded By Shift-Out = 016
000	NUL	CTRL @		λ
001	SOH	CTRL A		α
002	STX	CTRL B		ϕ
003	ETX	CTRL C		Σ
004	EOT	CTRL D		δ
005	ENQ	CTRL E		Δ
006	ACK	CTRL F		⌜
007	BEL	CTRL G		∂
010	BS	CTRL H	Backspace	⊓
011	HT	CTRL I (TAB)		ψ
012	LF	CTRL J (LF)	Line Feed	÷
013	VT	CTRL K		o
014	FF	CTRL L		∴
015	CR	CTRL M (CR)	Carriage Return	μ
016	SO	CTRL N		£
017	SI	CTRL O		Shift In
020	DLE	CTRL P		π
021	DC1	CTRL Q		‖
022	DC2	CTRL R		Ω
023	DC3	CTRL S		σ
024	DC4	CTRL T		ϒ
025	NAK	CTRL U		ϵ
026	SYN	CTRL V		←
027	ETB	CTRL W		→
030	CAN	CTRL X		↑
031	EM	CTRL Y		↓
032	SUM	CTRL Z		⌜
033	ESC	CTRL [(ALT)		⊥
034	FS	CTRL \		≠
035	GS	CTRL]		≈
036	RS	CTRL ~		∨
037	US	CTRL –		□
40	SP	SPACE BAR	Space 1 character	
41	!	SHIFT 1	!	
42	"	SHIFT 2	"	
43	#	SHIFT 3	#	

7 Bit (octal)	ASCII Representation	Keyboard	GT40 Printing	GT40 Printing When Preceded By Shift-Out = 016
44	$	SHIFT 4	$	
45	%	SHIFT 5	%	
46	&	SHIFT 6	&	
47	'	SHIFT 7	'	
50	(	SHIFT 8	(	
51	)	SHIFT 9	)	
52	*	SHIFT :	*	
53	+	SHIFT ;	+	
54	,	,	,	
55	- (minus)	-	-	
56	.	.	.	
57	/	/	/	
60	0	0	0	
61	1	1	1	
62	2	2	2	
63	3	3	3	
64	4	4	4	
65	5	5	5	
66	6	6	6	
67	7	7	7	
70	8	8	8	
71	9	9	9	
72	:	:	:	
73	;	;	;	
74	<	SHIFT ,	<	
75	=	SHIFT -	=	
76	>	SHIFT .	>	
77	?	SHIFT /	?	
100	@	@	@	
101	A	SHIFT A	A	
102	B	SHIFT B	B	
103	C	SHIFT C	C	
104	D	SHIFT D	D	
105	E	SHIFT E	E	
106	F	SHIFT F	F	
107	G	SHIFT G	G	
110	H	SHIFT H	H	
111	I	SHIFT I	I	
112	J	SHIFT J	J	
113	K	SHIFT K	K	
114	L	SHIFT L	L	
115	M	SHIFT M	M	
116	N	SHIFT N	N	
117	O	SHIFT O	O	
120	P	SHIFT P	P	
121	Q	SHIFT Q	Q	
122	R	SHIFT R	R	
123	S	SHIFT S	S	
124	T	SHIFT T	T	

7 Bit (octal)	ASCII Representation	Keyboard	GT40 Printing	GT40 Printing When Preceded By Shift-Out = 016
125	U	SHIFT U	U	
126	V	SHIFT V	V	
127	W	SHIFT W	W	
130	X	SHIFT X	X	
131	Y	SHIFT Y	Y	
132	Z	SHIFT Z	Z	
133	[	[	[	
134	\	\	\	
135	]	]	]	
136	^	^	^	
137	-	-	-	
140	`	SHIFT @	`	
141	a	A	a	
142	b	B	b	
143	c	C	c	
144	d	D	d	
145	e	E	e	
146	f	F	f	
147	g	G	g	
150	h	H	h	
151	i	I	i	
152	j	J	j	
153	k	K	k	
154	l	L	l	
155	m	M	m	
156	n	N	n	
157	o	O	o	
160	p	P	p	
161	q	Q	q	
162	r	R	r	
163	s	S	s	
164	t	T	t	
165	u	U	u	
166	v	V	v	
167	w	W	w	
170	x	X	x	
171	y	Y	y	
172	z	Z	z	
173		SHIFT [	{	
174		SHIFT \	|	
175		SHIFT]	}	
176	~	SHIFT ^	~	
177	RUB OUT	R.O.	■	

Function Key Codes

← 10	↑ 32	Home 35	EOS 37
→ 30	↓ 33	EOL 36	