INSTRUCTION MANUAL

DECTAPE CONTROL UNIT
TYPE TC01

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

DEC-08-I3AB-D

DECTAPE CONTROL UNIT
TYPE TC01
INSTRUCTION MANUAL

April 1968

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Printing September 1968
2nd Printing (Rev) April 1968
3rd Printing March 1969
4th Printing July 1969

Instruction times, operating speeds and the like are included in this manual for reference only; they are not to be taken as specifications.

CONTENTS

CHAPTER 1
INTRODUCTION

CHAPTER 2
OPERATION AND PROGRAMMING

CONTENTS (continued)

CHAPTER 3
PRINCIPLES OF OPERATION

CONTENTS (continued)

CONTENTS (continued)

CHAPTER 6
ENGINEERING DRAWINGS

ILLUSTRATIONS

CONTENTS (continued)

TABLES

ENGINEERING DRAWINGS

CHAPTER 1
INTRODUCTION

This manual, together with the referenced documents, provides information on the installation, operation, and maintenance of the Type TC01 DECtape Control, manufactured by Digital Equipment Corporation, Maynard, Massachusetts. The TC01 buffers and controls information transfers between a TU55 DECtape Transport and its associated data processor. This document assumes use of the TC01 in conjunction with either a DEC PDP-8 or PDP-8/I Programmed Data Processor. Except where specifically noted otherwise, all references to the PDP-8 also apply to the PDP-8/I. The level of discussion provided in this document assumes a prior knowledge and understanding of the TU55 DECtape Transport and the particular processor (PDP-8 or PDP-8/I) provided with the user's system.

1.1 GENERAL DESCRIPTION

The Type TC01 DECtape control is used to buffer and control the transfer of binary data between the PDP-8 processor and up to eight Type TU55 DECtape transports. The system configuration is shown on Figure 1-1.

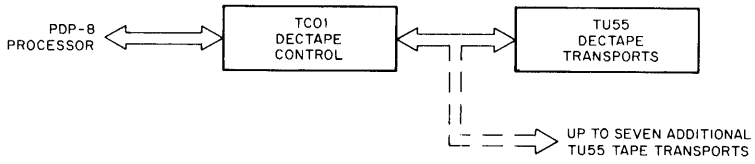


Figure 1-1 TC01 System Configuration

The TU55 DECtape transport is a bidirectional device consisting of a magnetic tape transport and solid state logic.

During both input and output operations, the TC01 receives data and control information from the processor and generates the appropriate signals to the selected transport to execute the programmed commands. Binary information is transferred between the tape transport and the computer as one 12-bit computer word every 133-1/3 μs. In writing, the TC01 disassembles the 12-bit computer word into four successive 3-bit words to be written on tape. During reading the TC01 assembles the four successive 3-bit words into one 12-bit word for transfer to the computer. Transfers between the computer and the control always occur in parallel for a 12-bit word. Data transfers use the 3-cycle data-break (high-speed channel) facility of the computer. As the start and end of each block are detected, the TC01 generates a DECtape control flag signal (DTCF) which causes a program interrupt in the computer. The program interrupt is used by the computer program to determine the block number. When it determines that the forthcoming block is the one selected for a data transfer, it selects the read or write control function. Each time a word is assembled or DECtape is ready

to receive a word from the computer, the control produces a data flag signal (DF) to request a data break. Therefore, when each 12-bit computer word is assembled, the data break initiates a transfer.

1.2 REFERENCED DOCUMENTS

The DEC documents listed in Table 1-1 contain material which supplements the information in this manual. These documents may be obtained from the nearest DEC field office or from the main office.

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts

Table 1-1
DEC Documents

Doc. No.	Title	Description
C105	Digital Logic Handbook	Specifications and descriptions of the FLIP CHIP modules and a simplified explanation of selection and use of these modules in various applications.
C100	System Modules	Specifications and descriptions of basic system modules and power supplies. This manual provides a simplified explanation of selection and use of these modules in system applications.
F-85	PDP-8 User Handbook	Programming and operating information for the computer, including brief instructions on the TC01 DECtape Control.
F-87	PDP-8 Maintenance Manual	Complete information on the internal operations of PDP-8 logic, memory basic in/out, and processor options.
Digital 8-27-U	PDP-8 Programming Manual	Programs for PDP-8. Complete descriptions of DECtape subroutines designed for assembly with an object program, the DECtape library system, and the DECtape utility routines.
H-TU55	Type TU55 DECtape Transport Maintenance Manual	Transport drive logic and internal operations, plus preventive and corrective maintenance instructions.
C-800	Small Computer Handbook	Handbook of basic functions of PDP-8/I computer.
DEC-8/I-HMAA	PDP-8/I Maintenance Manual	Complete information on the internal operation of PDP-8/I logic, memory, basic in/out, and processor options.

In addition to the documents listed in Table 1-1, a complete set of library programs are available.

1.3 PHYSICAL DESCRIPTION

The Type TC01 DECtape control logic is mounted in three FLIP CHIP mounting panels which can be installed together with up to three TU55 DECtape transports in a standard DEC cabinet. For detailed information on the mounting panels and cabinets, refer to the hardware section of the Digital Logic Handbook (C105).

The standard DEC computer cabinet is constructed with a welded steel frame and sheet steel covering. Double doors on the front and rear are held closed by magnetic latches. Power supplies and power controls are mounted inside the rear double doors on a full-width plenum door latched by a spring-loaded pin at the top. Module mounting panels are mounted behind the double door in front with the wiring side facing outward. Fans at the bottom of the bay draw cooling air through dust filters, pass it over the electronic components, and exhaust it through the wiring and other openings in the front and top of the cabinet. Four casters provide mobile support for the system. The rear plenum door contains blank panels in the space not occupied by components. The TC01 control and DECtape units receive power from the Type 779 Power Supply and a Type 834 Power Control. These units are mounted near the bottom of the plenum door.

The cabinet has an access door which extends 8-3/4 in. to the front of the cabinet and a plenum door which extends 13-3/4 in. to the rear. At least a 3-ft clearance should be allowed at both front and rear for access and maintenance. Cabinets may be bolted together at the sides to form contiguous units.

1.3.1 Equipment Characteristics

A summary of the characteristics of the TC01 control and associated equipment is listed in Table 1-2.

Table 1-2
Summary of Equipment Characteristics
for the TC01 DECtape Control

Equipment	Characteristics
TC01 Control	15-3/4 in. high, 19 in. wide for equipment which operates up to eight Type TU55 transports
TU55 Transport	10-1/2 in. high, 19-1/2 in. wide, 9-3/4 in. deep. Chassis can be extended 16-3/4 in. beyond the mounting surface for maintenance
Cabinet	69-1/8 in. high, 22-1/4 in. wide, 27-1/6 in. deep. Will hold a maximum of one TC01 control and three TU55 transports
Weight	
TC01 Control	30 lb
TU55 Transport	65 lb (rack mounted)
Cabinet	555 lb (with maximum equipment mounted)
Power Requirements	
TC01 Control	115V, 60 c/s, 4A A Type 834 Power Control and a Type 729 Power Supply are included with the Type TC01 Control (N9M transformer used for 50 c/s)
TU55 Transport	115V ±10%, 60 c/s, 2A maximum, 1.5A idle
Cabinet	115V, 60 c/s source capable of delivering 20 A
Tape Characteristics and Density	
a. 260 ft of 0.75 in., 1.0 Mylar tape per 3.5 in. reel	
b. 350 ±55 lines per inch	
c. 849,036 usable lines per tape	
d. 60 lines of control information	

Table 1-2 (Cont)
Summary of Equipment Characteristics
for the TC01 DECtape Control

Equipment	Characteristics
e. 4096 is the maximum number of addressable blocks per reel	
f. Number of words in a block must be divisible by 3	
g. $N_B = \frac{212112}{N_W + 15} - 2$	N_B = decimal number of blocks N_W = number of words per block
h. Capacity for 190,000 12-bit words in blocks of 129 words	

Word Transfer Rate

a. One tape line is read or written every 33-1/3 μs and one 12-bit word is read and assembled or disassembled and written in 133-1/3 μs.

b. In reverse direction, the transfer rate varies by 20% as the effective reel diameter changes.

c. Transfers require 1.2% of PDP-8 cycles after the initial 200-ms start time.

Addressing

a. Mark and timing tracks allow searching for a particular block.

Time

a. Start time is <375 ms, stop time is <375 ms, turn-around time is <375 ms.

b. Start and stop distances are approximately 8 in.

Input Signals to Transport from Control		
Commands	FORWARD REVERSE	Normally complementary levels
	GO STOP	Normally complementary levels
	ALL HALT	(stops transport when computer halts)
Unit Select		Select unit 1 through select 8
Information		Analog write signals to the recording head
Output Signal from Transport to Control		
Control	WRITE ENABLE	(ground level assertion)
Information		Analog read signals from the recording head
Environmental Conditions		
Thermal Dissipation		2150 Btu/hr
Operating Temperature		50° - 95°F ambient
Humidity		10% - 90% relative humidity

NOTE

The magnetic tape manufacturer recommends 40% - 60% relative humidity and 60° - 80°F as an acceptable operating environment for DECtape.

1.3.2 Electrical Requirements

A cable rated at 115V, 60 c/s, 30A furnishes power for the TC01 DECtape Control. This cable is terminated by a Hubbell Twist Lock plug rated at 30A, 125 Vac.

Signals between the TC01 DECtape Control and the computer are the standard voltage levels for the DEC FLIP CHIP modules, as stated in the Digital Logic Handbook (C105). Command signals between the TC01 and the tape transport are also standard FLIP CHIP levels except for the SINGLE UNIT signal which is a dc level between 0 and -9V. During writing, the information carries 200 ma in either direction with a 20V peak-to-peak waveform, symmetrical with respect to ground. When reading, the peak-to-peak head-voltage waveform is between 8 and 12 mV when the tape is up to speed. The internal logic for the TC01 consists of DEC FLIP CHIP modules. All internal signals are standard FLIP CHIP levels and pulses, except those for the read/write amplifiers and the SINGLE UNIT signals.

CHAPTER 2
OPERATION AND PROGRAMMING

This chapter contains the information required for the operation and programming of the TC01 DECtape Control unit. Included in this chapter is a description of the format of information on the DECtape magnetic tape, and the modes of operation used in the programming of TC01 operations. The general operating information for the TU55 DECtape transport is contained in the TU55 maintenance manual listed in Table 1-1.

2.1 DECTAPE FORMAT

The format of the DECtape (Figure 2-1) used in the DECtape transports provides ten tracks, of which three pairs of tracks are available for data and two pairs for timing and mark information. A 10-track recording head reads and writes the five duplexed channels of the DECtape. Duplication of each track by nonadjacent read/write heads, wired in series, eliminates most dropouts due to noise and dust, and minimizes skew problems. The location of the redundant tracks eliminates most cross talk between tracks. In addition, the location of the timing tracks along the edges of the tape permits strobing on the analog sum of the timing-track signals and reading of the data tracks, when they are in the most favorable position. The location of the data tracks in the middle of the tape also minimizes the effects of skew.

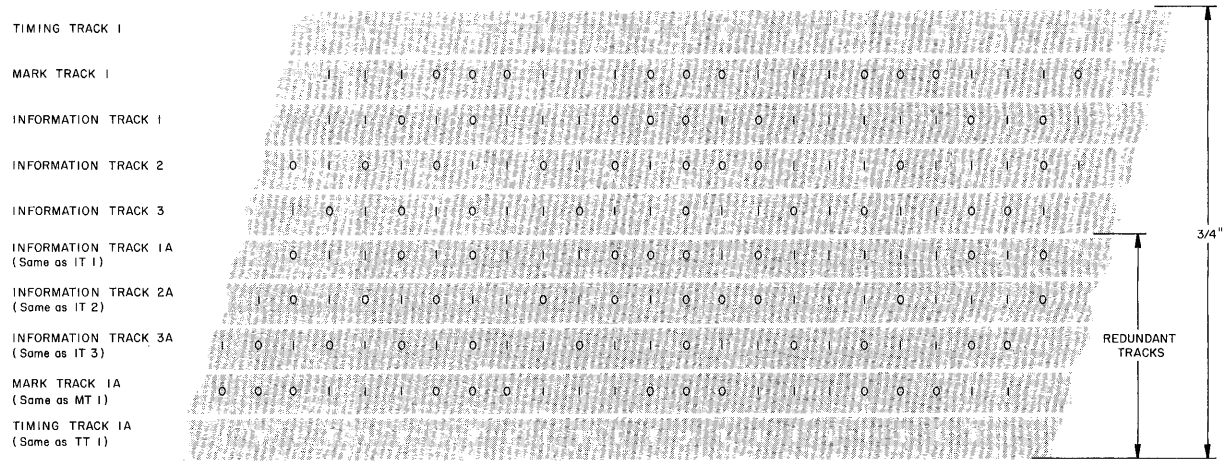


Figure 2-1 DECtape Track Allocation

Data is recorded by the Manchester method in which a prerecorded timing track synchronizes read/write operations. When writing on the tape, the write amplifiers supply the maximum current in either one direction or the other (non-return to zero, NRZ). To write a pulse, the polarity of the write current is reversed. The timing track is prerecorded with alternate positive and negative transitions at fixed time intervals. The negative transition is used during writing to load the write buffer and during

reading to shift data. The positive transition is used during both reading and writing. During writing, this transistion is a signal to switch the polarity of the write current in all write heads. If a ZERO is being written, the current, which starts out positive for writing ZEROs, is switched to negative resulting in a negative transition. If a ONE is being written, the current starts out negative and generates a positive transition when switched to positive. During reading, the positive transition of the timing track is a signal to strobe the data and mark track read-amplifier outputs into the read buffer. If a positive transition is sensed at strobe time, a ONE is placed in the buffer; otherwise a ZERO is strobed in.

Because the strobe is a relatively narrow pulse, the system is not affected by noise outside the strobe time. At strobe time, all data signals are negative pulses representing ZEROs or positive pulses representing ONEs. These pulses are all at their peaks. To have any effect, a noise pulse must be large enough to reverse the polarity of a data pulse. Data can be written over previously written data because the timing is controlled by the timing track that is written on the tape.

Information is stored on the tape in block form (Figure 2-2). Block length is flexible and determined by information on the mark-track. A complete reel of tape (849,036 lines) can be divided into any number of blocks up to 4096. A uniform block length can be established over the entire length of a reel of tape by a program which writes mark and timing information at specific locations. However, the ability to write variable-length blocks is useful for certain formats, for example, where small blocks containing index or tag information need to be alternated with the large blocks of data.

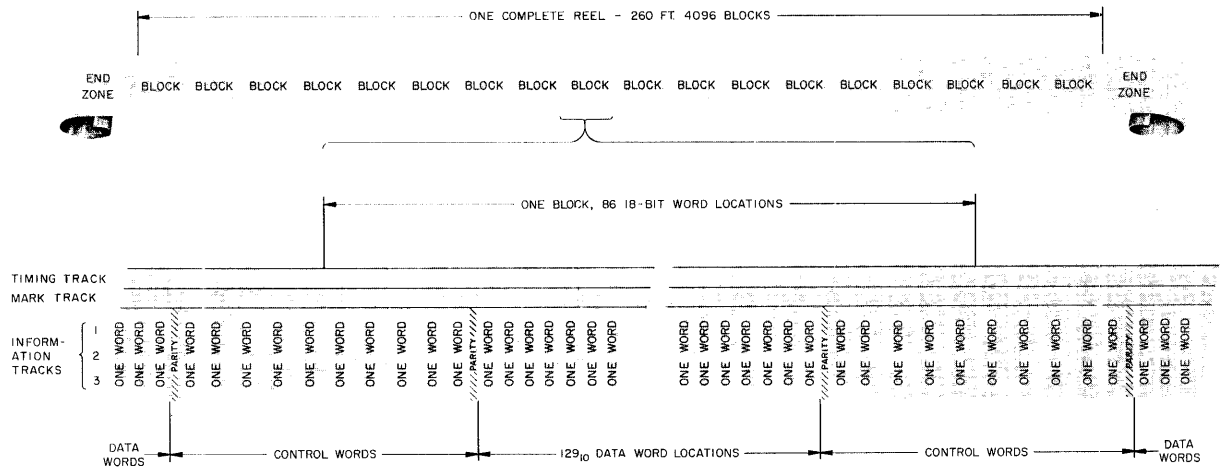


Figure 2-2 DECtape Control and Data Word Assignments

Each block contains data and control words as shown on Figure 2-3 which are assembled by the TC01 DECtape Control. Control words separate the data portions of adjacent blocks and record address and checking information. Although control words usually occupy six lines, only the last four lines are used. Data words contain stored information and occupy four lines on tape (12 bits). To maintain

compatibility with the mark-track format, data words are recorded in 12-line segments (which is the lowest common multiple of 6-line marks and 4-line data words) corresponding to three 12-bit data words. Therefore the number of words per block must be evenly divisable by 3.

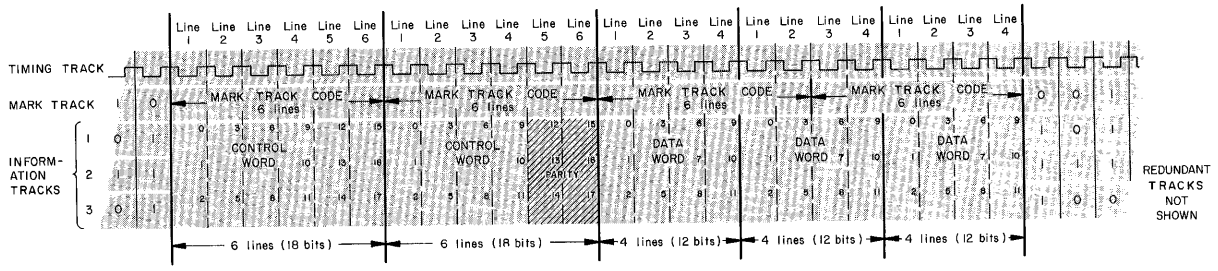


Figure 2-3 DECtape Recording Format

Block numbers normally occur in sequence from 1 to n. There is one block numbered 0 and one block n+1. Programs are entered with a statement of the first block number to be used and the total number of blocks to be read or written. The maximum number of blocks is determined by the following equation.

$$N_B = \frac{212112}{N_W + 15} - 2$$

N_B = decimal number of blocks

N_W = decimal number of words per block (N_W must be divisible by 3.)

2.1.1 Mark-Track Format

The mark track contains six-bit serially stored codes which initiate controls to raise flags in the program, request data breaks, detect block mark numbering and block ends, and protect control portions of the tape (Figure 2-4). The DECtape control unit automatically identifies these codes. The mark track also provides for automatic bidirectional compatibility, variable block formatting, and end-of-tape sensing.

In all tape processing functions except the recording of the timing and mark tracks, a single mark track bit is read from each line of tape regardless of whether the information is being read or written into the data tracks. Each tape line in both the information and mark tracks is positioned at the center of the timing track as shown on Figure 2-3. The mark track code is contained within six lines of the mark track.

A change of polarization on tape read in one direction produces a pulse opposite in polarity to that produced by the same change read in the opposite direction. Consequently, a mark code read in reverse has the order of bits reversed and the bits complemented.

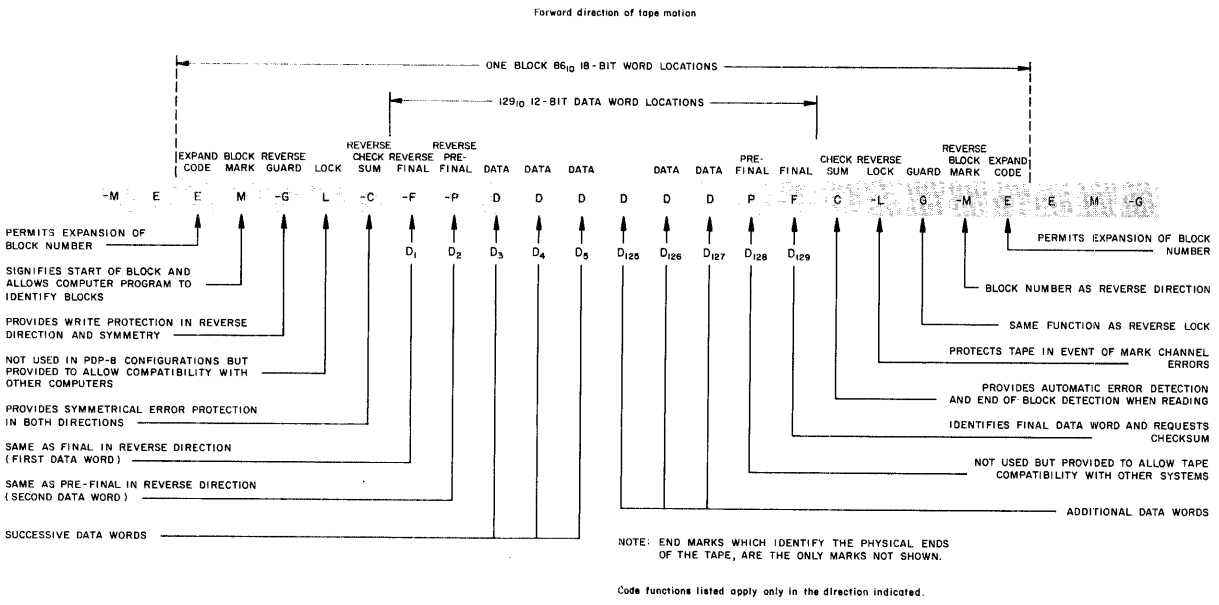


Figure 2-4 DECtape Mark Track Format

For example, the mark read forward as 100101 is read as 010110 in reverse. This correspondence is termed the complement obverse or the complement image. Every 6-bit code has one and only one complement obverse which is constructed by complementing all bits and reversing their order. Therefore, the complement obverse of the complement obverse is the original code itself. In octal notation, the complement obverse of any pair of digits is constructed by reversing the order of digits, then performing the following transformation on each:

$$0 \longrightarrow 7 \qquad 1 \longrightarrow 3 \qquad 2 \longrightarrow 5 \qquad 3 \longrightarrow 1$$
$$4 \longrightarrow 6 \qquad 5 \longrightarrow 2 \qquad 6 \longrightarrow 4 \qquad 7 \longrightarrow 0$$

The transformations indicate that there are eight octal codes which are their own complement obverses: 07, 13, 25, 31, 46, 52, 64, and 70. All other possible combinations of two octal digits (there are 56) are different from their complement obverses. As shown in Table 2-1, the complement obverse of any mark is designated by the minus sign (e.g., mark G = 51 has the complement obverse -G = 32).

Since the DECtape system allows reading and writing in both directions of tape motion, the mark-track must be coded to present the same information when entering a block from either direction. The marks at the end of a block are the complement obverses of the marks at the beginning, in reverse order. For example, if the control reads the marks E, M, -G as the first three marks beginning a block in forward motion, then it will read G, -M, -E, in that order, as the last three marks of the same block. In reverse motion, however, the control sees the complement obverse of the contents of the mark track; thus the first information, when reading the block in reverse, is -(-E), -(-M), -(G), which is identical to E, M, -G.

All marks used in the standard DECtape format are listed in Table 2-1. Only ten valid codes exist even though a given code may have different designations. Some of these marks are not required for the operation of the Type TC01 DECtape Control.

Table 2-1
Mark Track Coding

Mark	Octal Code	Function
C (Check)	73	Signifies the end of a mark frame whose first two lines were the forward parity check group.
-C (Reverse Check)	10	Signifies that the 6-bit reverse longitudinal parity check group is contained in the control unit read/write buffer and that the beginning of the data portion of a block is in the forward direction.
D, -D (Data)		In both forward and reverse tape motion, the data mark occupies all mark frames in the data portion of the block except for the final and prefinal marks. The number of data marks is limited only by the length of tape.
E, -E (Extension)	25	The first and last mark of every block (no-op mark).
End (Forward End)	22	Indicates the end zone of tape in forward direction. The forward end mark is positioned approximately 10 ft from actual tape end.
-END (Reverse End)	55	Indicates the end zone of tape in reverse direction. The reverse end mark is positioned approximately 10 ft from end of tape.
F (Final)	73	Signifies that the last word read from the data portion of the block is in the read/write buffer and data buffer. Signals that the next frame begins with the 6-bit forward longitudinal parity check group.
-F (Reverse Final)	10	Signifies that the last word read from the block, in the reverse direction, is in the read/write buffer and data buffer.
G (Guard)	51	Performs same function as -L (reverse lock).
-G (Reverse Guard)	32	Not used.
L (Lock)	10	Indicates the first of four octal 10 marks.
-L (Reverse Lock)	73	Protects subsequent records in the event of mark-track errors.
M (Forward Block)	26	Signifies the start of a block and indicates that the block number is contained in the TC01 control.
-M (Reverse Block)	45	Not used.
P (Prefinal)	73	In the forward tape direction, the prefinal mark is the next to last mark in the data portion of a block. It is the first of four marks using octal code 73.
-P (Reverse Prefinal)	10	In the reverse tape direction, signifies the next to last mark in the data portion of a block.

The standard mark-track uses the serial code of 6-bit characters to divide the tape into words. Codes are written on the mark track opposite word locations to identify the type of information stored at that location on tape. Block addresses are written for both forward and reverse directions and identified by two types of mark codes. A checksum is written at each end of the block. The hardware computed

checksum is the six bit logical equivalent (i.e., the complement of the "exclusive OR") of each six bits written on tape plus the reverse checksum previously recorded. By including the reverse checksum in the computation, the block may be read in either direction at a later time without an error. The control uses the final marks to establish synchronism and raise block-end flags. Data marks locate data words.

2.2 DECTAPE INSTRUCTIONS

The six basic IOT instructions used in the programming of the PDP-8 for TC01 DECtape operations are listed in Table 2-2, with the octal code assignments and a description of the instruction operation. These instructions apply to two functional groups within the TC01, designated as status A and status B, and are used to clear, read, and load the status registers A and B. These two registers are used to govern tape operations and provide status information to the computer program.

Table 2-2
TC01 DECtape Instruction List

Mnemonic	Octal Code	Operation
DTRA (read status register A)	6761	The contents of status register A are loaded into the accumulator by an OR transfer. Refer to Table 2-3 for the AC bit assignments.
DTCA (clear status register A)	6762	Status register A is cleared. The DECtape and error flags are undisturbed.
DTXA (load status register A)	6764	The exclusive OR of the contents of bits 0 through 9 of the accumulator is loaded into status register A, and bits 10 and 11 of the accumulator are sampled to control the clearing of the error and DECtape flags, respectively. Loading status register A from AC 0 through 9 establishes the transport unit select, motion control, function, and enables or disables the DECtape control flag to request a program interrupt as described in DTRA. Refer to Table 2-3 for AC10 and AC11 bit assignments.
DTSF (skip on flags)	6771	The content of both the error and DECtape flags is sampled. If any flag is set, the content of the program counter is incremented by one to skip the next sequential instruction.
DTRB (read status register B)	6772	The content of status register B is loaded into the accumulator by an inclusive OR transfer. The AC bit assignments are as follows. AC0 = Error flag (EF) AC1 = Mark-track error (MKTRK) AC2 = End-of-tape error (END) AC3 = Select error (SE) AC4 = Parity error (PI) AC5 = Timing error (TIM) AC6 - 8 = Memory field (MF) AC9-10 = Not used AC11 = DECtape flag (DTF)

Table 2-2 (Cont)
TC01 DECtape Instruction List

Mnemonic	Octal Code	Operation
DTLB (load status register B)	6774	The memory field portion of the accumulator (AC6-8) is loaded into the memory field register. The accumulator is cleared and the error flags are undisturbed.

2.2.1 Status Register A Functions

Figure 2-5 is the format for the status register A. This register contains three unit select bits, two motion bits, one mode bit, three function bits and three bits which control the flags. The bit assignments for the status register A are provided in Table 2-3.

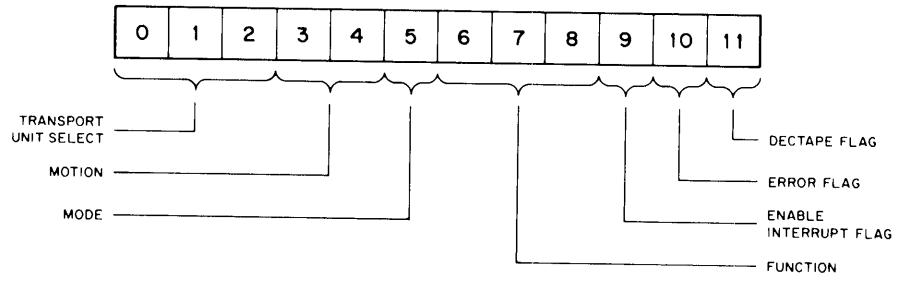


Figure 2-5 Status Register A, Format

Table 2-3
Status A-bit Assignments

Function	AC Bit	Conditions
Transport Unit Select	0-2	Octal Code / Unit 000 / 8 001 / 1 010 / 2 011 / 3 100 / 4 101 / 5 110 / 6 111 / 7
Motion	3	0 = Forward (FWD) 1 = Reverse (REV)
	4	0 = Stop motion (STOP) 1 = Start motion (GO)
Mode	5	0 = Normal mode (NM) 1 = Continuous mode (CM)

Table 2-3 (Cont)
Status A-bit Assignments

Function	AC Bit	Conditions	
Function	6,7,8	Code	Operation
		000	Move
		001	Search
		010	Read data
		011	Read all
		100	Write data
		101	Write all
		110	Write timing
		111	Unused (causes select error)
Enable the interrupt	9	1 = Enable DECtape control flag (DTCF) to the program interrupt	
Error flag	10	0 = Clear all error flags 1 = Error flags undisturbed	
DECtape flag	11	0 = Clear DECtape flag 1 = DECtape flag undisturbed	

2.2.2 Status Register B Functions

Figure 2-6 shows the format of the information in the status register B. This register contains 6 bits of error status information, 3 memory field bits and the DECtape flag bit. Table 2-4 lists the function of the bit assignments.

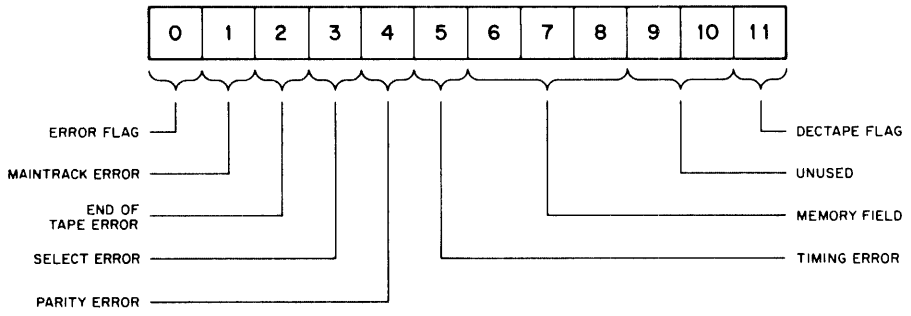


Figure 2-6 Status Register B, Format

Table 2-4
Status B, Bit Assignment

Function	AC Bit	Conditions
Error Flag (EF)	0	1 = Detection of any nonoperative condition by the control as listed in the error functions described in AC bits 1 through 5 of this table. These conditions stop transport motion except for parity errors.
Mark-Track Error (MKTRK)	1	1 = Information read from mark track was erroneously decoded.
End of Tape Error (END)	2	1 = the end zone on either end of tape is over read head.
Select Error (SE)	3	This error occurs 5 μs after loading status register A to indicate one or more of the following conditions. (a) The unit select code specified does not correspond to any transport select number or is set to more than one transport. (b) A write function was specified when the WRITE ENABLE/WRITE LOCK switch is in the WRITE LOCK position. (c) Specifies on unused function code (111) bits 6 through 8 of the status register A. (d) Specified a function other than Read All with the maintenance control panel RDMK/WRTM/NORMAL switch in the RDMK position. (e) Specified a function other than Write Timing and Mark Track with the RDMK/WRTM/NORMAL switch in the WRTM position. (f) Specified the Write Timing and Mark-Track function with the RDMK/WRTM/NORMAL switch in a position other than WRTM.
Parity Error (PAR)	4	1 = Error occurs during a Read Data function if the longitudinal parity over entire data block including reverse checksum and checksum, is not equal to 1. If a parity error is to be set at the end of a block, it will be set at the same time the DTF is set. During CM if a word count overflow does not occur at the end of a block, the parity error is set at the end of the block in which the word count overflow occurs. The parity error cannot be set after the DTF is set.
Timing Error (TIM)	5	1 = Program fault caused by one of the following conditions: (a) A data break request is not answered within 66 μs ±30% of the data break request. (b) The DTF was not cleared by the program before the control attempted to set it. (c) The read data or write data function was specified after the current data block has been entered to prevent incomplete data block transfers.

Table 2-4 (Cont)
Status B, Bit Assignment

Function	AC Bit	Conditions
Memory Field (MF)	6, 7, 8	Indicates the memory field from or to which data transfers take place.
	9-10	Unused
DECtape Flag (DTF)	11	1 = DECtape operation complete

2.3 CONTROL MODES AND FUNCTIONS

The TC01 control unit operates in either the normal mode (NM) or continuous mode (CM) as determined by the mode bit (5) in the status register A. In the normal mode, the data transfer and flag indications are controlled by the format of the information on tape. In the continuous mode, data transfer and flag indications are controlled by a word count (WC) read from core memory during the first cycle of each three cycle data break, and by the tape format.

The normal mode differs from the continuous mode primarily in the time at which the DECtape flag (DTF) is set. The DECtape flags which occur in the normal mode are inhibited in the continuous mode until a word count overflow has occurred. In both modes, data break requests occur only when a word count overflow has not occurred during the specified current function.

2.4 CONTROL FUNCTIONS

The DECtape system performs one of the seven following functions during either the normal or continuous mode, as determined by the octal digit loaded into the status register A during a DTXA command. A summary of the procedures and possible errors which may occur are listed in Table 2-5.

2.4.1 Move

Initiates motion, in either direction, of the specified tape transport. The mark-track is read but mark-track errors are inhibited except for end of tape errors. The move function is used to rewind tape.

2.4.2 Search

Provides random access to the data blocks on tape. As the tape is moving in either direction, the sensing of a block mark causes a data transfer of the block number. In normal mode the DTF is set, causing a program interrupt at each block number. In continuous mode the DTF is set only at the block number which causes the word count overflow. After the first block number is found, the continuous mode can be used to avoid all intermediate interrupts between the current and desired block number. The block number is read into the memory location specified by the current address register (Memory location 7755). The current address register is not incremented.

2.4.3 Read Data

This function reads data in either direction and transfers blocks of data into core memory with the transfer controlled by tape format. In the normal mode, DTF is set at the end of each block causing a program interrupt. In the continuous mode, transfer stops when the word count overflows; however, the remainder of the block is read for parity checking and the DTF is then set.

2.4.4 Read All

This function allows the reading of all bits on tape after the tape motion reaches up to speed. The three information tracks are continuously read and transferred to the computer. The mark-track is used to check only for mark-track and end of tape errors. During the normal mode, the data tape flag is set at each data transfer. During continuous mode, the data tape flag is set only when a word count overflow occurs.

2.4.5 Write Data

This function is used to write blocks of data in either direction with the transfer controlled by the standard tape format. When a word count overflow occurs during the writing of a block of data, zeros are written in all the remaining lines of tape until the end of a block and then the checksum over the entire block is written. The DTF is set in a similar manner as that for the Read Data function.

2.4.6 Write All

This function allows the writing of all bits on tape even though the information is not in the standard tape format. The mark-track will only check for mark-track and end of tape errors. The DTF is set for the same conditions described in Paragraph 2.4.4. This mode is used to write block numbers on tape.

2.4.7 Write Timing and Mark Tracks

This function is used to write timing and mark-tracks to establish or change the lengths of blocks.

2.4.8 Enable to the Interrupt

The TC01 control has an Enable-to-Interrupt (ENI) function which permits the program to remove the TC01 from the program interrupt of the PDP-8 processor.

Table 2-5
Control Function Procedures and Errors

Octal No.	Control Function	Procedures		Possible Errors
		Normal Mode (NM)	Continuous Mode (CM)	
0	MOVE	Not involved	Not involved	SE, END
1	SEARCH	Block number read into core location specified by contents of CA	Same as NM	SE END TIM
		CA is not incremented	Same as NM	MK TRK
		WC is incremented	Same as NM	
		DTF is set at each block number	DTF is set only at the block number causing WCO	
2	READ DATA	Transfer data as long as WCO has not occurred. If WCO occurs in middle of block, the block is read for parity checking but no more data transfers are made.	Same as NM	SE END TIM PAR MK TRK
		Both WC and CA are incremented.	Same as NM	
		DTF is set at each block end.	DTF is set only at end of block in which WCO occurs.	
3	READ ALL	Transfer data until WCO occurs.	Same as NM	SE END
		Both WC and CA are incremented.	Same as NM	TIM MK TRK
		DTF is set at each word transfer.	DTF is set at WCO	
4	WRITE DATA	Transfer data as long as WCO has not occurred. If WCO occurs in middle of block, zeros are written to end of block and checksum is written.	Same as NM	SE END TIM MK TRK
		Both WC and CA are incremented.	Same as NM	
		DTF is set at end of each block. If no new function is specified, the tape continues to move but the write heads are disabled. (TIM will occur at the end of next block if DTF is not cleared.)	DTF is set at end of block in which WCO occurred. When WCO occurs and if no new function is specified, the tape continues to move but the writers are disabled.	

Table 2-5 (Cont)
Control Function Procedures and Errors

Octal No.	Control Function	Procedures		Possible Errors
		Normal Mode (NM)	Continuous Mode (CM)	
5	WRITE ALL	Transfer data as long as WCO has not occurred. Word which causes WCO is last one written. Tape continues to move but the writers are disabled.	Same as NM	SE END TIM MK TRK
		Both WC and CA are incremented	Same as NM	
		DTF is set at each word transfer	DTF is set at WCO	
6	WRITE TIMING AND MARK TRACK (WRTM)	Transfer data as long as WCO has not occurred. After WCO, the writers are not disabled and zeros are written.	Same as NM	SE TM
		Both WC and CA are incremented.	Same as NM	
		DTF is set at each word transfer.	DTF is set at WCO	

2.5 PROGRAMMED OPERATION

Prior to using the Type TC01 DECtape Control for data storage, the prerecording of a reel of DECtape is accomplished in two passes. In the first pass, the timing and mark-tracks are placed on the tape. During the second pass and the forward and reverse block, mark numbers are written. These functions can be performed by the PDP-8 program. Prerecording utilizes the WRTM control function and the manual switch on the maintenance control panel of the Type TC01 DECtape Control to write on the timing and mark tracks, to activate a clock which produces the timing track recording pattern, and to enable flags for program control. Unless the WRTM control function and switch are used simultaneously, the writing on the mark or timing channels is inhibited. A red indicator lights on the control maintenance panel when the manual switch is in the RDMK or WRTM position. The mark-track can be written only when the switch is in the WRTM position. Only one prerecording operation is required for each reel of DECtape.

The six basic IOT instructions are generated as required by the PDP-8 program to clear, read and load the status A and clear and read the status B elements. The IOT skip instruction is available to test the status of the DECtape control. Since all data transfers between the Type TC01 DECtape Control and the PDP-8 memory are controlled by the data break facility, the PDP-8 program sets the word count (WC) and current address (CA) registers (location 7754 and 7755 respectively) using the memory reference instruction in the processor initializing a block transfer. Before and after a DECtape operation, the PDP-8 program checks for error conditions. A program interrupt is initiated if the TC01 is enabled to the interrupt

system and if the interrupt is on. The DECtape system is started with the search function to locate the block number selected for transfer; then when the correct block is found, the transfer is accomplished by setting the WC, CA, and the STATUS A and STATUS B elements.

When searching, the DECtape control reads only block numbers. These are used by the operating program to locate the correct block number. In NM, the DTF is raised at each block number. In CM, the DTF is raised only after the WC reaches zero. The CA is not incremented during searching, and the block number is placed in core memory at the location specified by the contents of the CA. Data is transferred to or from PDP-8 memory from locations specified by the CA which is incremented before each transfer.

When the start of the data position of the block is detected, DF is raised to initiate a data break request to the data break facility each time the DECtape system is ready to transfer a 12-bit word. Therefore, the main computer program continues running but 3 memory cycles are stolen approximately every 133-1/3 μs for the transfer of a word. Transfers occur between the DECtape and successive core memory locations specified by the CA. The initial transfer address-1 is stored in the CA by an initializing routine. The number of words transferred is determined by the tape format, if in NM, or by the tape format and WC, if in CM. At the conclusion of the data block transfer, the DTF is raised and a program interrupt occurs. The interrupt subroutine checks the DECtape error bits to determine the validity of the transfer and either initiates a search for the next information to be transferred or returns to the main program.

During all normal writing transfers, a checksum (the 6-bit logical equivalent of the words in the data block) is computed automatically by the control and is automatically recorded as one of the control words immediately following the data portion of the block. The same checksum is used during reading to determine that the data playback and recognition takes place without error.

Any one of the eight tape transports may be selected for use by the program. After using a particular transport, the program can stop the drive currently being used and select a new drive, or can select another transport while permitting the original selection to continue running. This allows rapid searching, since several transports may be used simultaneously. Caution must be exercised because, although the original transport continues to run, no tape-end detection or other sensing take place. All functions provide for automatic end sensing, but this feature stops tape in the selected tape drive only. The timing for the TC01 operations are summarized in Table 2-6.

Table 2-6
Summary of Timing Data for TC01 Operation

Operation	Time
Time to Answer Data Break Request	Up to 66 μs (±30%)
Data Break Transfer Rate	4.5 μs (3 cycles) per word
Word Transfer Rate	1 - 12 bit word every 133 μs (±30%)
Block Transfer Rate	1 - 129 word block every 18.2 ms (±30%)
Start Time	< 375 ms (±20%)
Stop Time	< 375 ms (±20%)
Turn Around Time	< 375 ms (±20%)
Search Read Data Function change for present block	Up to 400 μs (±30%)
Search Write Data Function change for present block	Up to 400 μs (±30%)
Read Search Function change for next block #	Up to 1000 μs (±30%)
Write Search Function change for next block #	Up to 1000 μs (±30%)
DTF Occurrence:	
Move: NM, CM	None
Search: NM Read Data: NM Write Data: NM	Every 18.2 ms (±30%)
Search: CM	(WC) X18.2 ms (±30%)
Read Data: CM Write Data: CM	(#block) X18.2 ms (±30%)
Read All: NM Write All: NM Write Timing and Mark Tracks: NM	Every 133 μs (±30%)
Read All: CM Write All: CM Write Timing and Mark Tracks: CM	(WC) X133 μs

2.5.1 Simplified Search Procedure

The use of the following procedure simplifies the search operation.

a. Search in NM and find the first block mark.

b. Compute the difference (d) between this block mark and the desired block number.

c. Load the 2s complement of this difference into the WC.

d. Change to CM and continue search.

e. The next DTF interrupt is the desired block. The block number is in the address specified by the CA, if a program check is desired. This procedure results in only two interrupts compared to d + 1 interrupts found in the method which interrupts at each block mark.

2.5.2 Bootstrap Loading

The CA specifies the address into which the data is loaded. The CA points to the WC, and the first word that is transferred specifies the number of words to transfer. Then, the CA points to itself, and the second word that is transferred determines where the subsequent data is to be loaded. This technique requires the use of the 3-cycle break, which contains the WC and the CA. No program interrupts, timing, or computation is needed for the location of data.

2.5.3 Upper Bound Protection for Data Transfer

The WC controls all data transfers and, after a word count overflow occurs no further data transfers take place. To protect the memory, when reading a block of unknown length, the WC is set to the upper bound. Similar action prevents writing beyond a predetermined point on the tape.

2.5.4 Write/Read in Opposite Direction

Writing or reading in opposite directions can be accomplished with the TC01, but two steps are required to return the data to the original memory format. One step is necessary because the CA only increments and does not invert the reverse order of the words. The other step is necessary because the word returned from the TC01 is in the following format compared with the original. For example

Original bit positions:	0	1	2	3	4	5	6	7	8	9	10	11
Returned bit positions:	$\overline{9}$	$\overline{10}$	$\overline{11}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{0}$	$\overline{1}$	$\overline{2}$

The reorganization procedure that is required can be performed in real time, provided that sufficient time is available. This procedure should be avoided when other program interrupts are too frequent and where using the fastest possible data rate of 133 μs ±30% per word.

2.5.5 Turn Around Specifications

During a search operation a turn around command can be issued, to change the tape motion without affecting the other command parameters. This requires two standard block lengths of tape to enable the transport to reach "up to speed" before searching for the block in the opposite direction.

To search for blocks No. 0 next to the tape end zone, the tape must be moved into the end zone at least two block lengths before changing tape direction. To search for block No. 1, the tape is moved into the end zone at least one block length before changing direction. This provides sufficient tape to allow the transport to reach up to speed before searching for the block. To eliminate this operation the TOG-8 program provides two block lengths of enter-block zone-marks (NO-OP marks) at the end of tape so that the tape can reverse motion at the end zone and still locate block 0 or block 1.

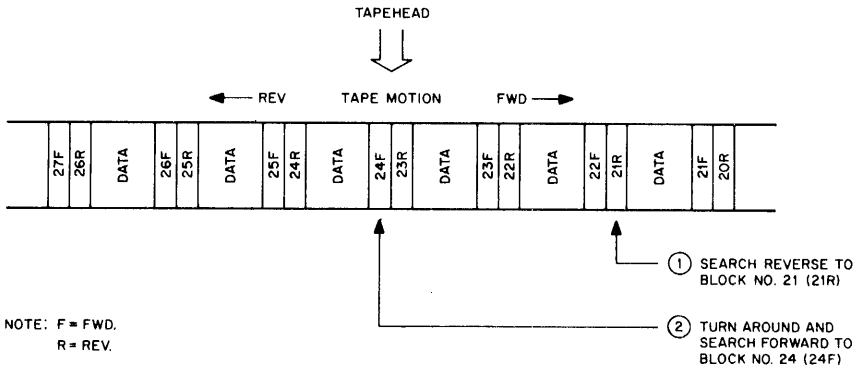


Figure 2-7 Turn Around Sequence Diagram

A length of tape equal to two standard block lengths (129_{10} - 12-bit words) must pass the tape transport heads before a turn around command is issued. This is equivalent to approximately 4 in. of tape. The formula for calculating, the nonstandard block delay that is required for turn around is listed as follows.

EXAMPLE

Turn around delay calculation for 72_{10} words per block

$$\frac{129 \text{ (words/block)}}{72 \text{ (words/block)}} \quad X\,2 = 3.6 \text{ block delay}$$

(4.0 block delay used for simplified search operations)

2.6 AVAILABLE SOFTWARE

The software available for use with the PDP-8 is described in the following paragraphs.

2.6.1 Subroutines

Subroutines may easily incorporate into a program for data storage, logging, data acquisition, data buffering (queuing), etc.

The subroutines include a series that will read or write any number of DECtape blocks, read any number of 129-word blocks as 128 words (or one memory page) in which 200 octal locations equal 128 decimal locations; or search for any block that is used by read and write or to position the tape. These programs are assembled with the user's program and are called by a jump-to-subroutine (JMS) instruction. The program interrupt is used to detect the setting of the DECtape (DTF) flag thus allowing the main program to proceed while the DECtape operation is being completed. A program flag is set when the operation has been completed. The program, therefore, allows effective and concurrent operation of several input/output devices as well as the DECtape.

2.6.2 Library Calling System

A Library Calling System is used for storing named program on DECtape and provides a means of calling them with a minimal size loader.

The Library Calling System leaves the state of the computer unchanged when it exits and is capable of calling programs by name from the keyboard and allowing for expansion of the program file stored on the tape. It also conforms to existing system conventions by allowing all of memory except for the last memory page (7600_8 ____ 7777_8) to be available. This convention permits the binary loader (paper tape) and/or future versions of this loader to reside in memory at all times. The PDP-8 Library System is loaded by a 17_{10} instruction bootstrap routine that starts at 7600_8. This loading calls a larger program into the last memory page. The function of the larger program is to preserve on the tape the contents of memory from 6000_8 - 7577_7, and then load the INDEX program and the directory into those same locations. Because the information in this area has been preserved, it can be restored when the operations have been completed. The skeleton library tape contains the following programs.

INDEX	Typing this program causes the names of all programs currently on file to be typed out.
UPDATE	Allows the user to add a new program to the files. UPDATE queries the operator about the program's name, its starting address, and its location in core memory.
GETSYS	Generates a skeleton library tape on a specified DECtape unit.
DELETE	Causes a named file to be deleted from the tape.

Starting with the skeleton library tape, the user can build a complete file of active programs and continuously update them. For example, a program that is to be used repeatedly is written on library tape. The library tape can be used by the programmer to call the FORTRAN compiler. The compiler, in turn, can be used to compile a program to obtain the object program. Then, the FORTRAN Operating System can be called from the library tape and used to load the object program. At this time, the library UPDATE program is called and the operator defines a new program file (consisting of the FORTRAN Operating System and the object program) and adds it to the library tape. As a result, the entire operating program and the object program are available on the DECtape library tape.

2.6.3 Preformatting Tape Programs

There are available programs for preformatting tapes which are controlled from the Teletype to write the timing and mark tracks, to write block formats, to exercise the tape and check for errors, and to provide ease of maintenance.

2.6.4 Maintenance Programs

A package of maintenance programs are available which exercise the DECtape system. One set of programs exercises the various functions separately and provides scope loop operation. A system test, using a program which does random transport selection, searching, and data checking while running a central processor test, is provided.

2.7 SYMBOLS AND ABBREVIATIONS

Table 2-7 lists the symbols and abbreviations used throughout this manual and on the logic drawings contained in Chapter 6.

Table 2-7
Symbols and Abbreviations

AC	Accumulator
ADDRESS ACC	Address accepted
BAC	Buffered accumulator
B BREAK	Buffered break signal supplied by PDP-8 (PDP-8/I)
BLK	Block of DECtape data
BMB	Buffered memory buffer
BMR	Buffered motion register
B RUN	Flip-flop located in PDP-8 (PDP-8/I) which indicates whether processor is performing instructions.
BTC	Block transfer control
+1⟶CA INH	Signal which inhibits incrementing the CA
C_0, C_2, C_3, C_4	Control clock flip-flops
CA	Current address register
CK	Check
CK_1, CK_2	Clock counter
CLEAR STATUS A	400-ns control pulse initiated by IOP 2
CM	Continuous mode
COMP RWB 0-2	Complement RWB bits 0 through 2
C SYNCH	Level indicating whether control clock is synchronized with DECtape marks
CXA	Clear status A pulse or exclusive OR status A pulse
DATA	Data flip-flop of state register
DB	Data buffer
DCD	Diode capacitor gate
DF	Data flag
DTF	DECtape flag
DTCF	DECtape control flag
EF	Error flag
EN	Enable
END	End of tape
ENI	Enable-to-the-interrupt
EOT	End-of-tape error
ES	Error stop

Table 2-7 (Cont)
Symbols and Abbreviations

FD	Function decoder
FR	Function register
FR_0, FR_1, FR_2, FR_3	FR flip-flops
IM	Input mixer
IN	Inclusive
INH	Inhibit
I/O	Input/output
ION	Interrupt on
IOP	Input/output pulse
IOR	Inclusive OR
IOT	Input/output transfer
IOT SKIP ON DTCF (1)	400-ns status B SKIP command
LOAD STATUS B	400-ns control pulse initiated by IOP 4
LPB	Longitudinal parity buffer
MA	Memory address register
MB	Memory buffer register
MK BLK END	Flag marking end of a data block
MK BLK START	Flag marking start of a data block
MK DATA	Flag marking the data portion of a block
MK END	End flag indicating that the end zone has been entered
MCP	Maintenance control panel
MF	Memory field register
MK(—)	Serially stored codes on DECtape
MK TK	Mark track error flip-flop
MR	Motion register
PA	Pulse amplifier
PAR	Parity error
PC	Program counter
PI	Program interrupt
PWR CLR	Power clear pulses
RATE DY	Rate delay
RD MK	Read mark level output from MCP switch
RD + WD	Read data or write data
READ STATUS A	400-ns control pulse initiated by IOP 2
READ STATUS B	400-ns control pulse initiated by IOP 2
REV CH	Reverse check
ROTATE DB/RWB	Rotate contents of DB and RWB

Table 2-7 (Cont)
Symbols and Abbreviations

RWB	Read-write buffer
RWB ⊬ LPB	Computes parity check in LPB
RWB SHIFT LEFT	Shift contents of RWB to the left and read next line of tape
SAD	Status A delay
SE	Select error enable
SEL	Select error flip-flop
SHIFT ST	Shift state pulse
SP	Speed of DECtape
ST	State or start
STB	Strobe
ST BLK MK	State in which control senses block numbers
ST CK	State in which automatic error detection (when reading)is provided
ST FINAL	Final data word of block state
ST IDLE	State in which DECtape transport is stopped or not up to speed or between blocks
ST REV CK	State in which reverse checksum is over head
SWTM	Switch timing and mark level output of MCP switch
SYNC	Synchronize
T	Time
T1	PDP-8 time state 1
T2	PDP-8 time state 2
T3	PDP-8 time state 3
TIM	Timing error
T/M ENABLE	Timing mark ENABLE
TP0	DECtape timing pulse which designates instant that center of left polarization of timing track passes the head inductors (beginning of a line on tape)
TP1	DECtape timing pulse which designates instant that center of right polarization of timing track passes the head inductors (center of a line on tape)
TRK	Track
TT	Timing track
U + M	Unit or motion
UP TO SPEED	Signal indicating DECtape transport is running at operating speed
USR	Unit select register
W	Window register
WC	Word count flip-flop

Table 2-7 (Cont)
Symbols and Abbreviations

WCO	Word count overflow pulse
WD - EN	Write data enable
W - INH	Write inhibit
WREN	Write enable
WRITE OK	WRITE ENABLE/WRITE LOCK switch sensing from selected TU55
WRTM	Write timing and mark
XOR	Exclusive OR
XOR STATUS A	400-ns control pulse initiated by IOP 4
XSAD	XOR STATUS A delayed 400 ns
X SA DY	Delayed CXA pulse
0 ⟶ STATUS A	400-ns CLEAR STATUS A pulse for clearing USR
0 ⟶ (device symbol)	Clears all bits of device designated
1 ⟶ (device symbol)	Sets all bits of device designated
C ⟶ (device symbol)	Complements all bits of device designated
(4 digits) ⟶ C0- C3	Each 1 or 0 of 4-digit word designates 1 or 0 output of respective control clock flip-flop C0, C1, C2, or C3
+1 ⟶ (device symbol)	Increment the contents of device designated by 1
V	Inclusive OR
⊻	Exclusive OR
⋀	AND
$\overline{A}$	ONEs complement of the content of A
A5	Content of bit 5 of register A
A5(1)	Bit 5 of register A contains a 1
A6-11	Contents of bits 6 through 11 of register A
overbar e.g., $\overline{(SWTM)}$	Negation of signal level. Also refers to complement of signal
FLIP-FLOP (0)	ZERO output of designated flip-flop
FLIP-FLOP (1)	ONE output of designated flip-flop

CHAPTER 3
PRINCIPLES OF OPERATION

This section includes a brief description of the basic functional elements of the TC01 DECtape control, together with the general information on data and control information transfer. It also contains a detailed description of the TC01 control operation, with reference to the block schematic diagrams contained in Chapter 6 of this manual. For detailed information on the PDP-8 and PDP-8/I processors, and TU55 DECtape Transport, refer to the documents listed in Table 1-1.

3.1 FUNCTIONAL DESCRIPTION

The basic functional elements of the TC01 control, the PDP-8 (PDP-8/I) processors, and TU55 transport interface blocks are shown on Figure 3-1. The numerals in the lower right-hand corner of the blocks indicate the bit capacity of the element. The numerical subscripts on the signal flow lines indicate the bit assignments of the signals. Blocks that represent the Status A and Status B functions are indicated by an A or B, respectively, in the top right-hand corner of the block.

3.1.1 Information Flow

A description of the registers associated with the information flow are listed, as follows.

a. Data Buffer (DB) - The data buffer is a 12-bit register used as a storage buffer to synchronize data transfers as a function of tape timing between the memory buffer register of the computer and the read/write register.

b. Read/Write Buffer (R/WB) - The read/write buffer is a 6-bit register consisting of three, 2-bit shift registers. During read operations, one bit from each of the three data channels on tape is read into the read/write buffer and shifted right or left depending on the tape direction.

c. Write Amplifiers - The five write amplifiers receive timing signals, mark-track, and data information from the read/write buffer and provide the necessary current to the tape heads to write the data on tape.

d. Read Amplifiers - The five read amplifiers transfer timing signals, mark-track and data information from the tape heads to the window register and read/write buffer.

3.1.2 Command Flow Registers

The registers and signals which control the transport operations and the data flow are described as follows.

a. Longitudinal Parity Buffer (LPB)- The longitudinal parity buffer is a 6-bit register used to perform a parity check on the three information channels. The operation is performed by setting the 6-bits of information read from two consecutive lines on tape into the LPB and complementing each stage of the LPB if the corresponding bit of the R/WB contains a zero.

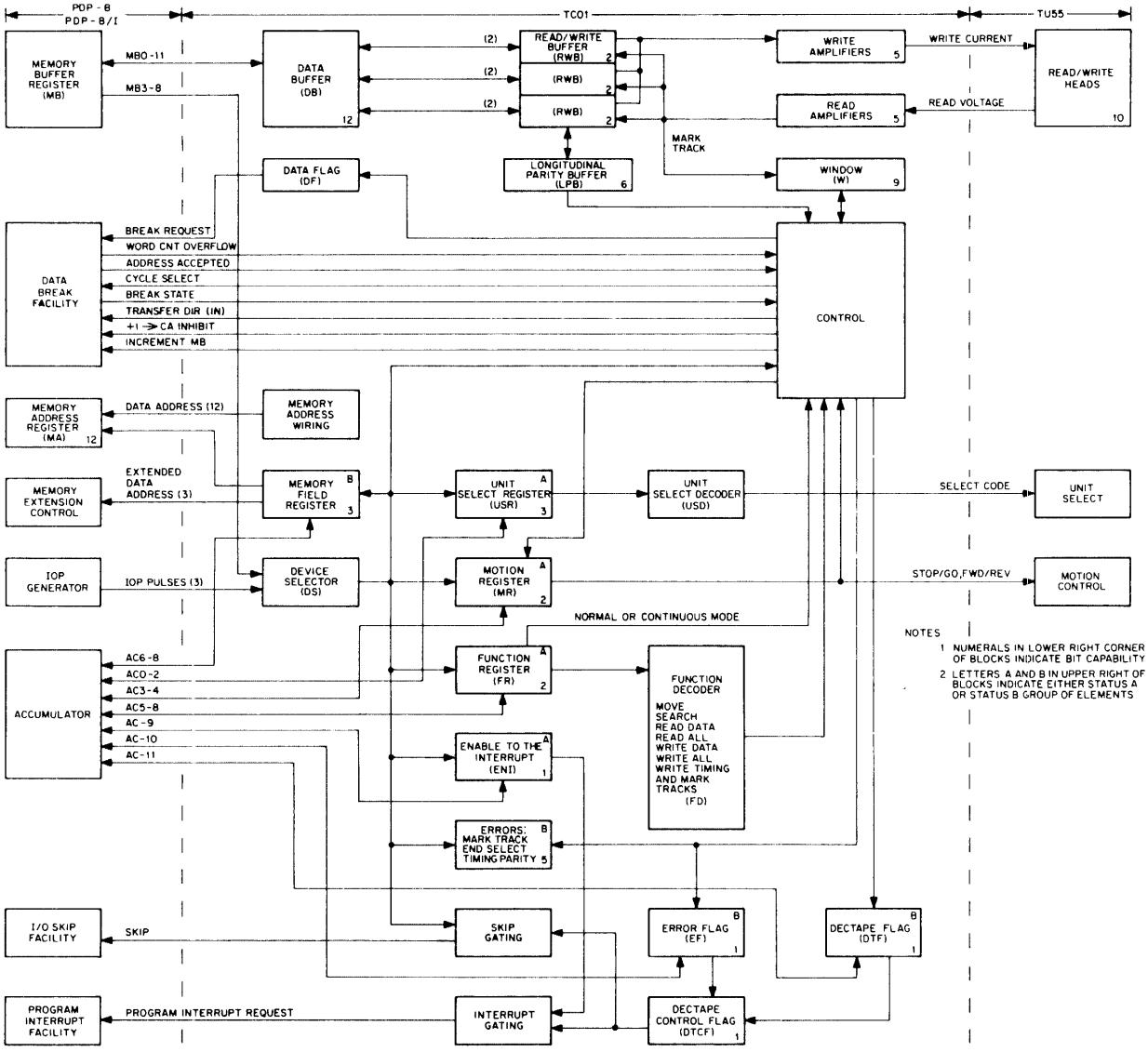


Figure 3-1 Type TC01 DECtape Control Functional Block Diagram

b. Window (W) - The window is a 9-bit register through which mark-track information is serially shifted to generate control signals for the DECtape system.

c. Data Flag (DF) - The data flip-flop requests a data break from the processor when a word is ready to be transferred to or from the TC01.

d. Memory Address - The memory address are 12-bits which constitute a fixed memory address for data transfers during the 3-cycle data break.

e. Memory Field (MF) - The memory field register is a 3-bit register which is loaded by program control when a data transfer operation is specified and constitutes bits 6, 7 and 8 of the status register B. This information, together with the address supplied during the current address cycle, provides a 15-bit address for the actual data transfer during the third cycle of the 3-cycle data break.

f. Word Count Overflow Pulse - This pulse is received at the end of the first cycle of the 3-cycle data break when a word count overflow occurs and clears the WC flip-flop to indicate that the current data transfer is complete. The pulse is used primarily during continuous mode. It stops data transfer, however, during the normal mode.

g. Address Accepted Pulse - This pulse is generated each time a 3-cycle data break is granted. It clears the DF signifying that the data transfer has occurred.

h. Control - The control logic generates the timing and synchronizing pulses to perform the functions specified in the function register and to coordinate the operations between processor and TU55 transport.

i. Device Selector - The device selector decodes the IOT instructions for the DECtape and generates the necessary pulses to load status registers, read status registers and generate SKIP pulses.

j. Unit Select Register - Unit select register is a 3-bit register which is loaded under program control from the accumulator bits 0 through 2, and specified a particular TU55 transport.

k. Unit Select Decoder - This device decodes the number in the unit select register and activates a select line to a specific TU55 transport.

l. Motion Register - The motion register is a 2-bit register loaded from the accumulator, bits 3 and 4, with the appropriate command of GO or STOP (bit 4), FORWARD or REVERSE (bit 3).

m. Function Register - The function register is a 4-bit register, which specified the operation to be performed by the DECtape. The first bit of this register is a mode bit which selects either normal or continuous mode. The remaining three bits are used to specify one of the seven functions.

n. Function Decoder - The function decoder decodes the contents of the function register, bits 1 through 3, and transfers the decoded information to the control.

o. Enable to the Interrupt - This is a 1-bit register loaded from the accumulator, bit 9, to enable or disable the DECtape from the program interrupt.

p. Error Register - A 5-bit register each section of which may be set by the TC01 control to indicate one of five error conditions.

q. Error Flag - The error flag is set by one or more errors indicated by the error register.

r. DECtape Flag - The DECtape flag is set at the completion of the currently specified operation.

s. WC Flip-Flop - The WC flip-flop is set on an XOR Status A command.

t. DECtape Control Flag - The DECtape control flag is set by the error flag and/or the DECtape flag. This flag is skipped on the SKIP IOT instruction and is also gated into the interrupt to request program interrupts.

u. Skip Gating - Skip gating logic generates a pulse from the DECtape control flag and the SKIP IOT to request a skip from the PDP-8. This gating is not affected by the enable to the interrupt.

v. Interrupt Gating - The interrupt requests the program interrupt from the PDP-8 when the DECtape control flag is set and the DECtape is enabled to the interrupt.

3.2 DETAILED LOGIC OPERATIONS

The information contained in the following paragraphs is a detailed description of the operations of TC01 DECtape control and is supported by the instruction flow diagrams Figures 3-2 and 3-3, and the engineering drawings located in Chapter 6 of this manual. The engineering drawings are referenced only by the last number of the drawing designation and the signal and module locations on the drawings are referenced according to the coordinates on the margin of the drawings.

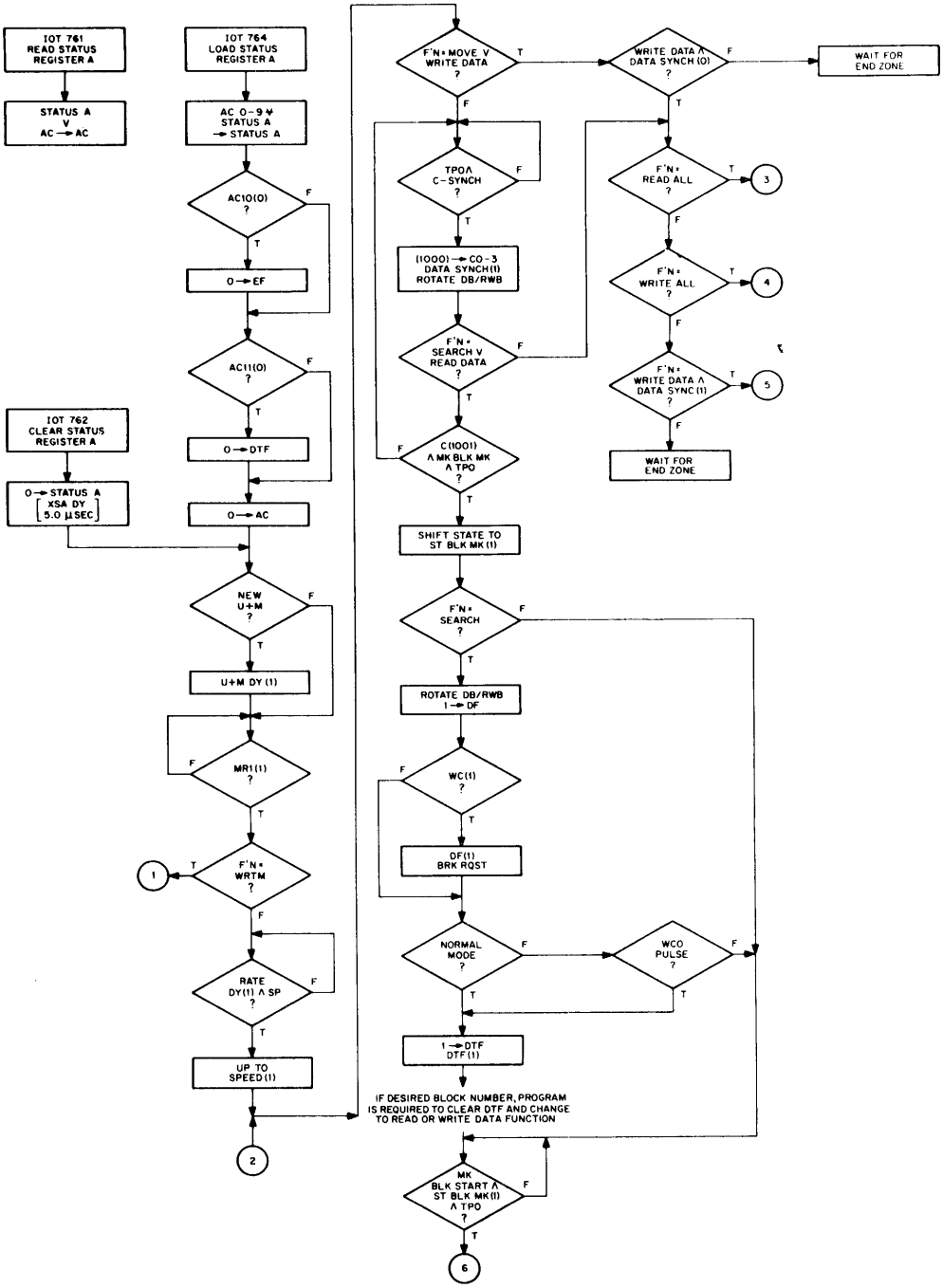


Figure 3-2 Status Register A, Instruction Flow Diagram (Part I)

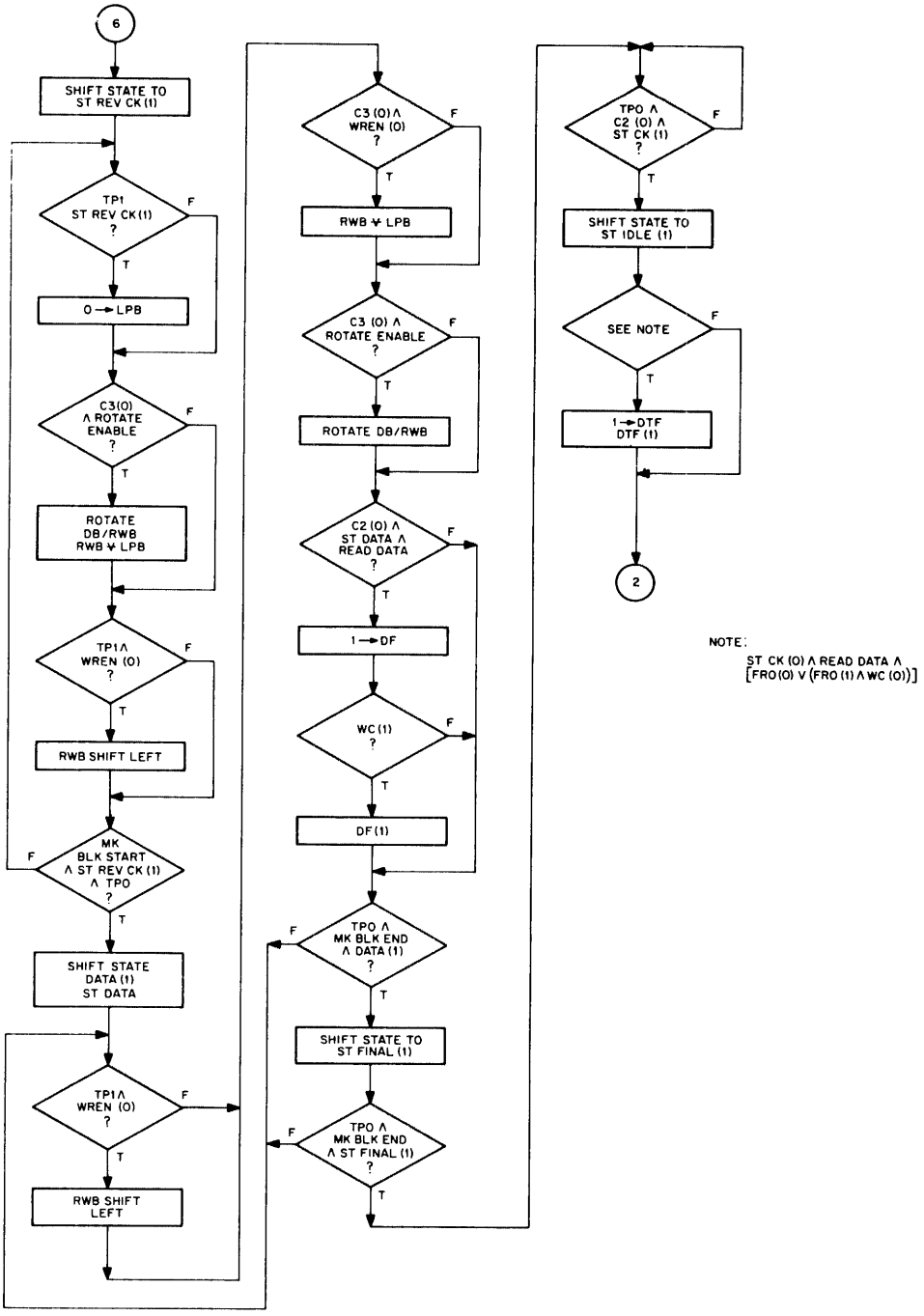


Figure 3-2 Status Register A, Instruction Flow Diagram (Part II)

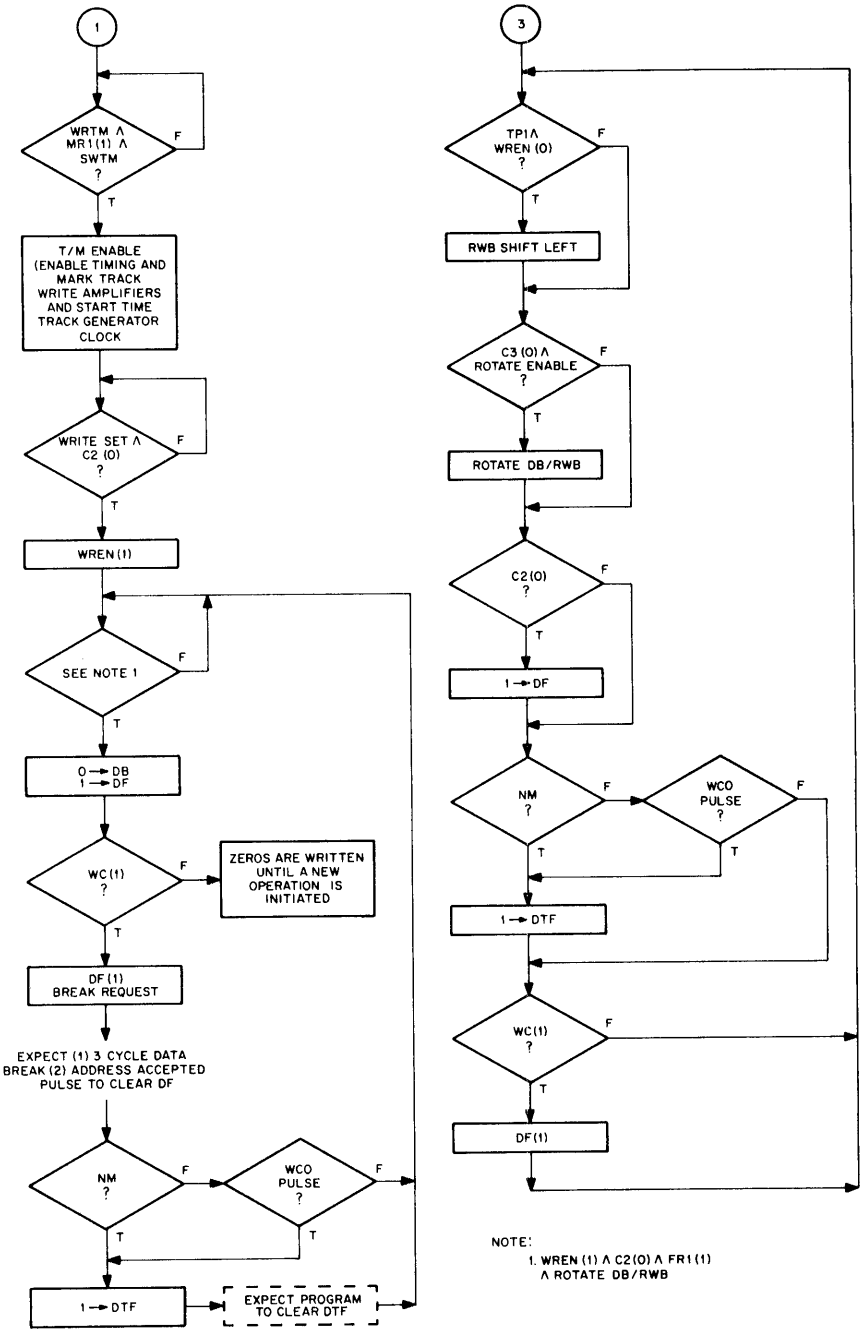


Figure 3-2 Status Register A, Instruction Flow Diagram (Part III)

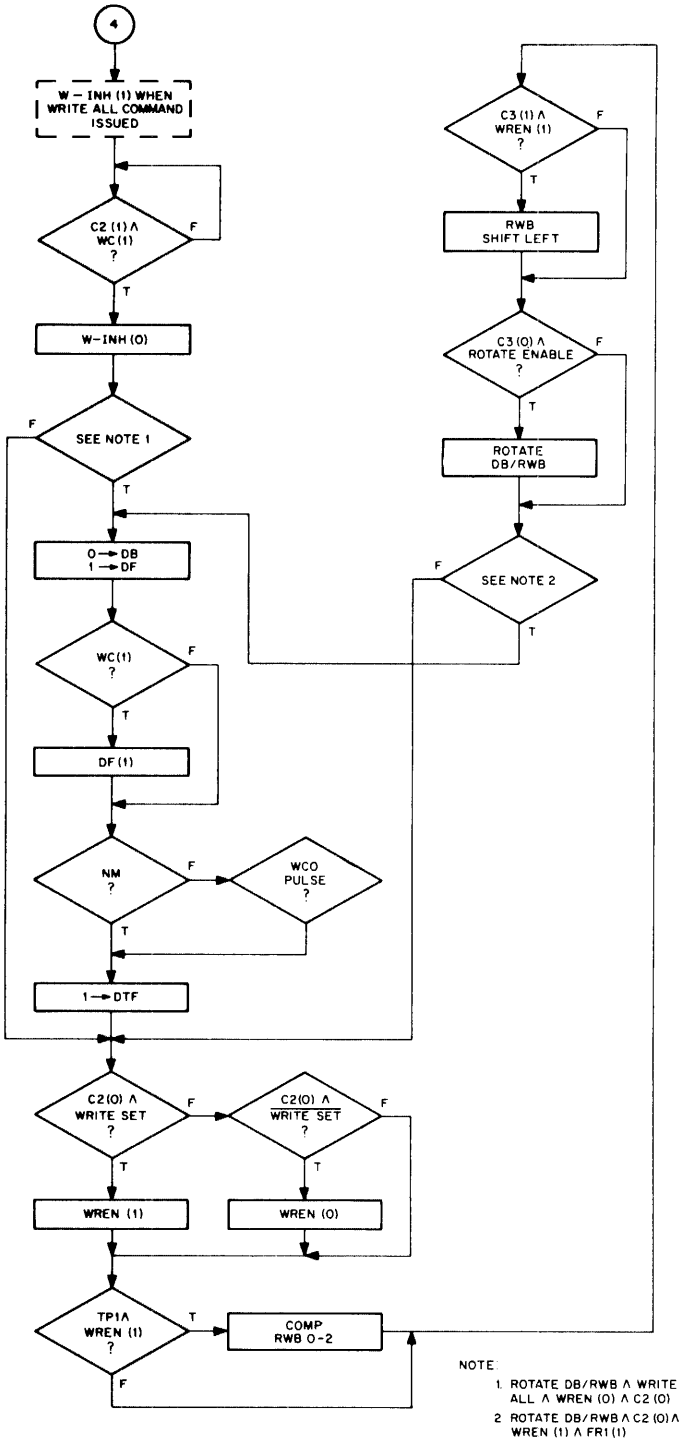


Figure 3-2 Status Register A, Instruction Flow Diagram (Part IV)

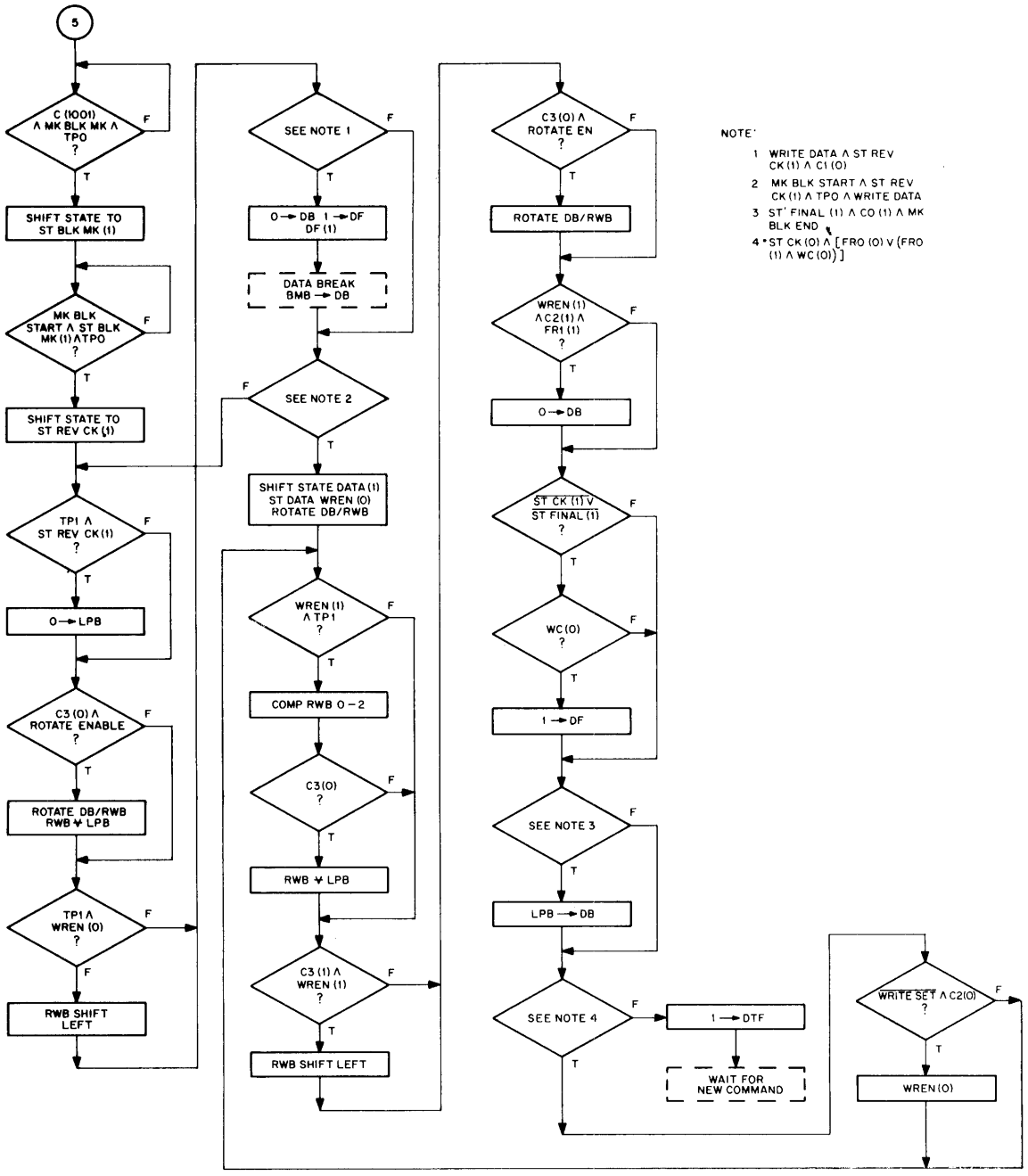


Figure 3-2 Status Retister A, Instruction Flow Diagram (Part V)

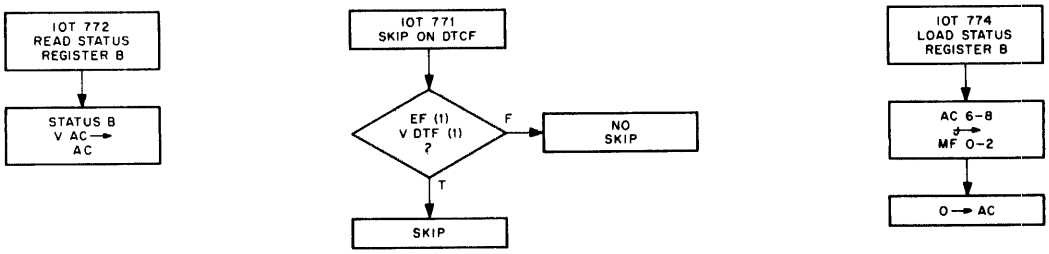


Figure 3-3 Status Register B, Instructions Flow Diagram

3.2.1 Basic Read/Write Logic

The basic read/write logic for the Type TC01 DECtape control is shown on the left-hand side of Figure 3-4. Each channel of the read/write circuit contains a flip-flop and input gates, a write amplifier governed by the flip-flop outputs and a read amplifier. Read inputs are paralleled with the write amplifier outputs across the head allowing the read amplifier to respond to signals from both the head and the write amplifier.

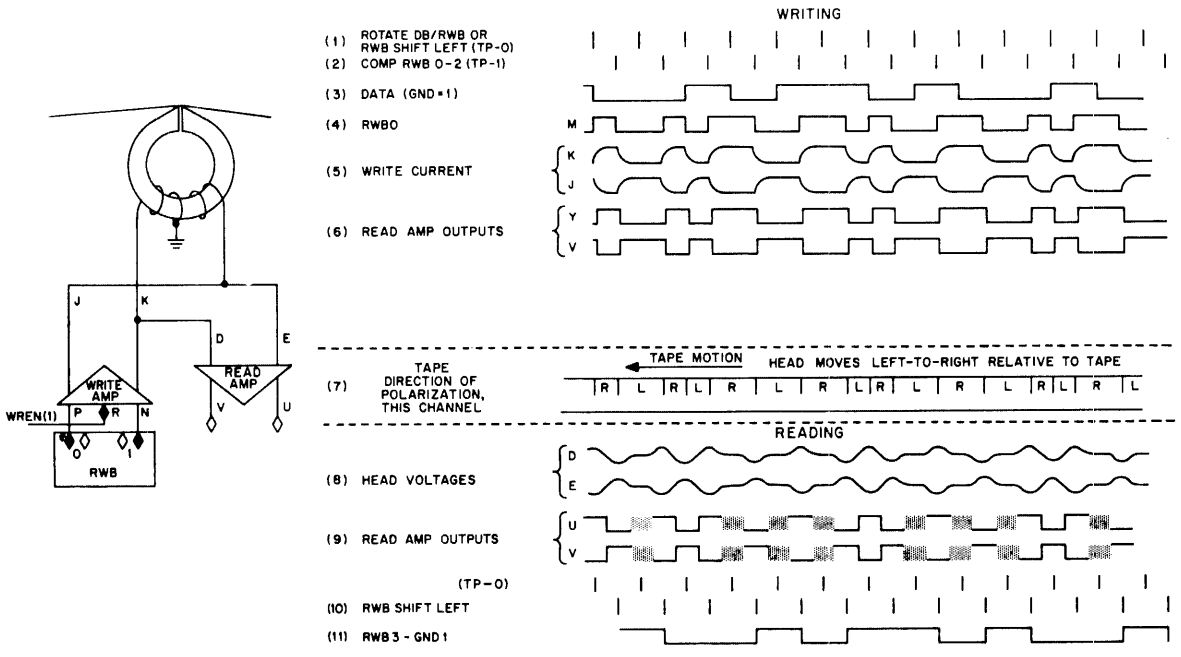


Figure 3-4 Read/Write Logic and Waveforms

The read amplifier is a high gain differential amplifier augmented by a transient positive feedback. When a signal of either polarity is sensed by the head, the read-amplifier outputs switch immediately and are asserted unambiguously regardless of noise which prevents head cross talk resulting

from simultaneous writing, in the data channels and reading in the timing-and-mark channels. The read amplifier outputs U and V are standard DEC logic levels of -3V and ground. When input E is more positive than D, the output V is asserted at ground and U is negative; when D is more positive, the output levels are reversed. Due to the positive feedback, the read amplifier oscillates in the absence of input signals. The read amplifier output waveforms therefore are rectangular whenever the differential input signal is indeterminate.

The write amplifier is a saturated grounded-emitter push-pull amplifier with its output collectors connected through resistances to pins J and K. If the enable level is asserted negative, the write amplifier is governed entirely by the state of the flip-flop. When the flip-flop is 1, K floats while J is returned through the resistance and saturated output collector to -13V. When the flip-flop is 0, J floats while K is negative. In the two tracks corresponding to each channel on tape, information is recorded in a manner that makes read signals from the two head inductors reinforce on playback. The two inductors can be considered as a single head inductor whose winding is center-tapped to ground, reading and writing in a single track.

When a write flip-flop contains 0, current flows from ground through the head inductor into K, and the polarization of the head core is oriented clockwise. The tape polarization, as the tape moves across the head, is oriented toward the left regardless of the direction of tape motion. Similarly when the flip-flop contains 1, tape polarization is oriented to the right regardless of the direction of tape motion. When reading, the current induced in the head by a change in polarization flows opposite to the current required to cause the same change; consequently, the current induced by a left-to-right (L-R) tape-polarization change is a current flowing out of the head toward pin E. The head is a source, and when a terminal is a current source it is positive. Thus an L-R tape-polarization change causes the read amplifier input E to be positive; consequently V is ground and U is negative. By the same reasoning the right-to-left (R-L) polarization change induces a positive signal at D and results in V being asserted negative and U at ground.

The Manchester recording system used in the Type TC01 DECtape Control requires two pulses to write each bit in a channel. The first pulse, ROTATE DB/RWB or RWB SHIFT LEFT, loads the write flip-flop with the value of the bit to be written, the second pulse, RWB 0-2, complements the flip-flop. Depending on the state of the flip-flop, the ROTATE DB/RWB pulse may or may not cause a polarization change on the tape. The RWB 0-2 pulse, however, causes a tape polarization change because the complement always changes the state of the flip-flop. When reading, the value of a recorded bit is detected by observation of the head inductor output as the polarization change (corresponding to the complement) passes over the head. The RWB 0-2 pulse produces a R-L tape polarization change when the flip-flop is loaded with 1; and produces a L-R change when the flip-flop is loaded with 0.

In Figure 3-4, the ROTATE DB/RWB or RWB SHIFT LEFT and RWB 0-2 pulses alternate. The first pulse sets the flip-flop to the assertion of the 1 level, the second pulse sets the flip-flop to the opposite state. The RWB 0-2 and the ROTATE DB/RWB or RWB SHIFT LEFT occur at 16.6 ms intervals. This relationship is shown in lines 1 and 2 of Figure 3-4. Since the flip-flop is loaded through capacitor-diode gates, the data input is free to change at each ROTATE DB/RWB or RWB SHIFT LEFT pulse. Line 3 shows a string of consecutive bits to be written on tape. In line 4, the write flip-flop receives each bit at a ROTATE DB/RWB or RWB SHIFT LEFT pulse and assumes the opposite state on a RWB 0-2 pulse.

In line 9 of Figure 3-4, the direction of tape polarization is labeled as R and L for right and left, respectively. The R-L and L-R transitions are detected by the read amplifier as negative and positive half sinusoids at pin E (opposite polarity at D). If the tape is read in the same direction as written, the tape positions corresponding to the time that the write flip-flop was complemented will show an R-L change as a 1; an L-R change as a 0. The head voltages at read amplifier inputs E and D are shown in line 10; the read amplifier outputs are shown in line 11. In reading, the shift pulses in line 12 for the RWB coincide with those in line 2 which complemented the write flip-flop in writing. The R-L polurization change representing a 1 results in a ground level at U at the time of the shift pulse. Consequently, as shown in line 13, a 1 is shifted into the shift register as the first bit read.

If the tape is read opposite to the direction in which it was written, the polarizations reach the head gap in reverse order; that is, the head senses an L-R change where a 1 was written, etc. The contents of the mark channel are selected to take advantage of this condition. Data written in one direction and read in the opposite direction will be complemented.

3.2.2 Read and Write Amplifiers

The read and write amplifiers are shown on Drawing No. 15.

The READ T TRK and READ MK TRK read amplifiers produce timing and mark-track outputs. The associated write amplifiers are only used to format tape. The D and E inputs to the READ T TRK read amplifier also serve as inputs to a sense amplifier which provides an SP input for the generation of an UP TO SPEED signal.

The READ D0, READ D1 and READ D2 read amplifiers and corresponding write amplifiers on Drawing No. 15 produce the outputs necessary for the transfer of data between their associated RWB bits (RWB 3-5) and the DECtape. Appropriate inputs and outputs for this purpose are described in later sections of the manual.

3.2.3 Device Selector Logic

The device selector logic decodes the output of the memory buffer, bits 3 through 8, and generates IOT pulses used to initiate the status A and status B operations listed in Table 2-2. STATUS A pulses are produced by the circuit shown on the left-hand side of Drawing No. 14; STATUS B pulses by the circuit on the upper right-hand side of Drawing No. 6.

3.2.3.1 STATUS A Decoding - The control operations which are initiated by computer instructions and which involve status register A are shown on Figure 3-2. These instructions are Read Status Register A (DTRA), Clear Status Register A (DTCA), and Load Status Register A (DTXA). The status A instructions contain an octal 76 in bits 3 through 8 of the memory buffer register and are decoded by device selector W103, location B7 of Drawing No. 14. Read Status Register A at event time 1, IOP1 is gated with the device selector to produce the 400 ns READ STATUS A pulse. The information on status register A (shown on Drawing No. 2), consisting of unit select (USR0-2), motion control (MR0 and MR1) function register (FR0-FR3), enable interrupt (ENI), and DECtape Flag (DF) is gated with READ STATUS A pulse location

B2-B8 to produce outputs (IM0-8) which are loaded into the PDP-8 accumulator through connector DT05 or DTA05.

Instruction IOT 6762, Clear Status A, is also decoded by the device selector on Drawing No. 14 and during Event Time 2. Pulse IOP2 is produced and gated with the decoded output to generate the 400 ns CLEAR STATUS A signal. The CLEAR STATUS A output produces the 0 ⟶ STATUS A, location D1, to clear the status register A functions, on Drawing No. 2 and the ground CXA pulse location D8, Drawing No. 14. The positive going CXA pulse triggers the 5 μs delay at R302 providing a -3V XSA DY output for the duration of the delay. Clearing status register A selects tape unit (8) by the 000 configuration of the unit select register. The negative XSA DY level at location B1 of Drawing No. 2 holds both the STOP and GO levels at ground to prevent a change of motion to tape unit previously specified. The positive going end of the XSA DY pulse jams the contents of MR1 into BRM1 motion. Either the BRM1(0) output or MR1(0) pulse will provide a ground level at both the FWD and REV outputs of S107, preventing a direction change from occurring to insure that only the newly selected unit receives the new command.

IOT 7764, Load Status Register A, is decoded at the device selector and gated with the IOP4 pulse at event time 3 to generate the 400-ns XOR STATUS A pulse. The ground XOR STATUS A pulse output performs an exclusive OR function with the buffered accumulator outputs shown at the center of Drawing No. 2, complementing the data in the status register A when the buffered input level (BAC0-8) goes to ground at least 400 μs before the XOR STATUS A pulse is received. This permits specific information in the status register to be changed without affecting the remaining information.

The negative XOR STATUS A pulse is amplified by PA603 (center right of Figure 5-1) to produce a negative XSAD pulse at S107 and a positive XSAD pulse at the amplifier output. The positive XSAD pulse is gated into PA603 (bottom right of Figure 5-1) to provide a 0 ⟶ AC pulse which will clear the information in the accumulator.

3.2.4 Status Register B and Skip Instructions

The status register B and skip-on-flag instructions, which are selected by an octal 77 in bits 3 through 8 of the memory buffer register in the PDP-8, are decoded by W-103, location D1-D3 and C1-C3 of Drawing No. 6. These instructions are Skip on Flags (DTSF), Read Status Register B (DTRB) and Load Status Register B (DTLB). The flow diagram is shown on Figure 3-5.

At event time 1, when a programmed IOP1 pulse is received, the PA produces the IOT SKIP ON DTCF (1), 400 ns pulse outputs. The output pulse is NANDed with the output of R113, location B2. If either an error flag exists or the DECtape flag is set, then the output of S111 will generate a ground SKIP pulse at pin K of W021. The SKIP pulse causes the program counter in the PDP-8 to be incremented by one and skip to the next sequential instruction.

When a programmed IOP2 pulse appears at event time 2, the next PA will produce the 400 ns READ STATUS B outputs. The READ STATUS B pulse is a common pulse input to the NAND gates associated with R123 modules shown on Drawing No. 2, location B1-B8.

A -3V level on any of the gate inputs which indicates that an error exists, the DECtape flag is set, or the bit configuration of the MEMORY FIELD register, will result in ground IM outputs from the

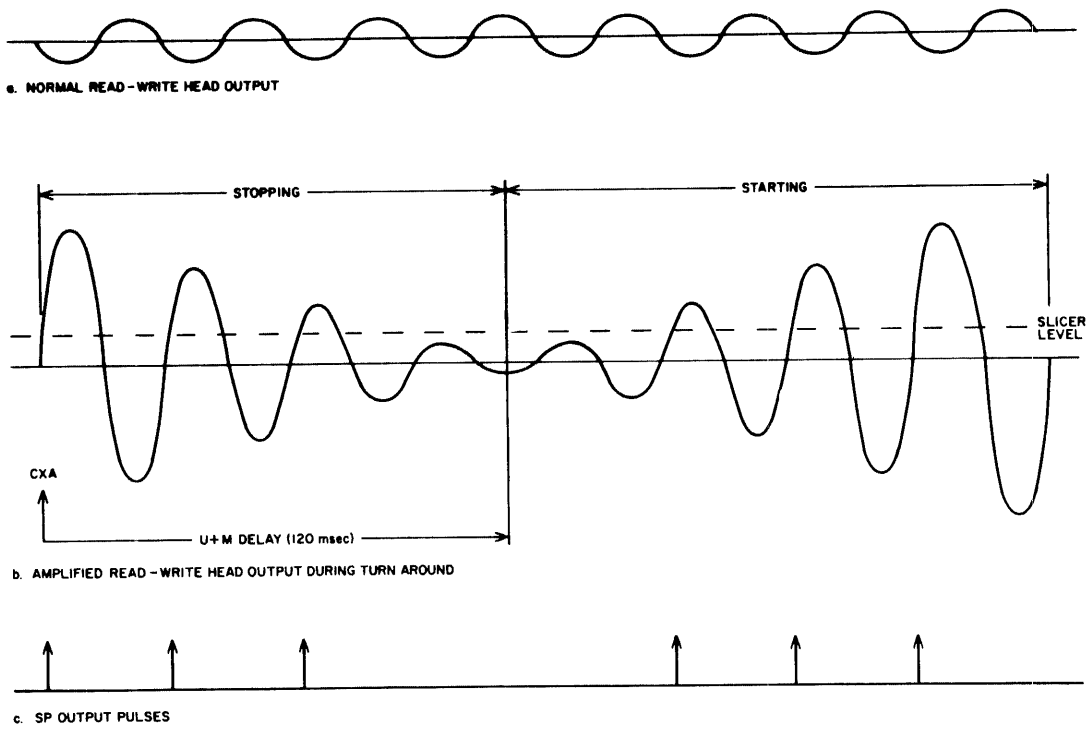


Figure 3-5 Slicer Network Waveforms

associated gate at connection W021. This information is loaded into the PDP-8 accumulator by an OR transfer.

If a load status B instruction is programmed at event time 3, an IOP4 pulse will be generated resulting in 400 ns, LOAD STATUS B pulse outputs from the amplifier on Drawing No. 6, location D1. The -3V pulse outputs are applied to the DCD gates associated with the 3-bit memory field register (MF), shown on Drawing No. 2, location D1 and D2, causing the memory field information from the buffered outputs BAC6-BAC8 to be loaded into MF0-MF2, respectively.

3.2.5 Unit Select Logic (Drawing No. 2)

The unit select information USR0-2 in status register A is decoded by the Binary to Octal Decoder S151, Drawing No. 14, location C7 and C8. A ground level on one of the eight outputs will enable a SELECT level within the specified TU55 DECtape transport.

3.2.6 Motion Control (Drawing No. 2)

The motion control information in MR0 and MR1 of status register A determines when the selected TU55 transport will be activated and the direction of tape travel. The output of MR0 will produce either a FWD or REV level at location D1 which is gated into the TU55 and to determine the motion of the tape. Only one direction signal can be active at a given time. The MR1 flip-flop output is gated with the XDA DY delay level at C2 and determines as previously discussed the STOP or GO levels to the selected tape unit.

3.2.7 Function Selection (Drawing No. 2)

The outputs of the function registers (FR1-3) are decoded by the Binary-to-Octal decoder R151, at location C3 and C4, Drawing No. 2, resulting in a ground level output on one of the selected function lines. If an octal 7 is indicated, all FR flip-flops set, a select error level will condition the DCD gate at the SEL flip-flop, Drawing No. 14 location D5 and allow the negative XSA DY pulse to set the SEL flip-flop.

3.2.8 Interrupt Enable (Drawing No. 2)

Bit 9 of the AC determines the status of the DECtape Control flip-flop (ENI) which enables ENI(1) or disables ENI(0), the DECtape Control Flag, from causing a program interrupt. The output of ENI(1) will cause an interrupt request to be sent to the PDP-8 at location B1, Drawing No. 6.

3.2.9 New Unit/Motion Select (Drawing No. 6 and No. 14)

The buffered accumulator outputs, BAC0-4, are sampled by the OR gate, Drawing No. 14, location B6, to determine whether a new unit or motion has been specified. A ground level on any BAC0-4 input or at buffered memory bit BMB9(0) which indicates a change on bits 0-4 of the status A will result in a ground level NEW U+M output. This level allows the negative going CXA pulse (Drawing No. 6) to be produced by XOR STATUS A or CLEAR STATUS A, to trigger the 120 ms U+M delay. The U+M(1) output from the delay is used to reset the up-to-speed flip-flop, location D8. The output of the up-to-speed flip-flop, when reset, disables the READ T TRK (0) inputs, location B6 and C6, from generating the timing pulse outputs TP0 and TP1.

When the U+M delay is set, the negative output prevents the timing track pulses (SP) read from tape during the up to speed operation from triggering the RATE DY flip-flop.

The SP signals are produced by a slicer network consisting of a sense amplifier and a slice control circuit at location C8 (Drawing No. 15). When the transport is running at normal speed, the sense amplifier input from the read/write head is a sinusoid of constant amplitude, as shown on Figure 3-5. When the transport stops or starts or changes direction of motion, the sine wave amplitude and frequency varies as a function of speed. This variation is illustrated by the amplified read/write head output on Figure 3-5. The slicer level shown in this illustration is preset and controlled by the slicer control circuit G008.

The sense amplifier uses the slicer level as a bottom clamp for the positive excursions of the sine wave. Since the amplitudes and frequency of the positive loops vary with the transport speed, the loop crossover at the slicer level provides a measure of the transport speed, and this information is contained in the SP output pulses generated at the first crossover of each loop.

When the U+M delay is reset, the ground level output conditions the DCD gate to allow the first SP pulse to set the rate delay. The ground level output of the rate delay conditions the DCD gate associated with the up-to-speed flip-flop to allow the next SP pulse which occurs within a 70 μs interval to set the up-to-speed flip-flop and start the TC01 operations. The up-to-speed flip-flop is reset by the positive transition of the BRM1(0) level which indicates a stop motion and by the ground output of the timing mark enable level (T/M ENABLE) generated at S107, location D5. Resetting this flip-flop produces a 0 ⟶WINDOW pulse which clears the window register on Drawing No. 3 while the tape is not up to speed.

3.2.10 Timing Pulse Generation (Drawing No. 6)

Timing pulses are required for both formatting the tape and for reading information from tape. During WRTM function the T/M ENABLE level activates the clock and allows timing pulses TP0 and TP1 to be generated, provided that the maintenance control panel switch (location B4), is in the WRTM position. This position causes the WRTM/RDMK indicator to light and generates the SWTM level. The SWTM level is ANDed with MR1(1) and WRTM level, to produce TM/ENABLE which starts the 120 kc clock. On the positive transition of the clock pulse, the CK1 flip-flop is complemented. The positive transitions of the CK1 flip-flop output complements the CK0 flip-flop. The outputs of CK1 and CK0 at location C5, result in the generation of 100 ns timing pulses TP0 and TP1 which occur alternately every 16.6 μs. The CK0 output is also applied to the timing track write amplifier, Drawing No. 15, to produce the timing track pattern written on tape.

Timing pulses are also enabled by the SWTM output from the maintenance control panel switch and by the WREN level at location C4 and B4.

During the write function when the C2 flip-flop goes to zero, the negative transition sets the WREN flip-flop and generates the WREN(1) output. The WREN flip-flop is reset again at C2(0) when any one of the ANDed inputs, that is associated with the write functions, is removed. This flip-flop allows a full data word to be written, even though one of the enabling level inputs have been removed before the end of a word had been reached.

Timing pulses TP0 and TP1 are generated during read operations when the UP-TO-SPEED(1) flip-flop is set at location B7, Drawing No. 6. The inverted output is gated with $\overline{\text{SWTM}}$ level which is present, when the maintenance control panel switch is any position other than WRTM, to provide a ground conditioning level to the DCD gates associated with the TP1 and TP0 power amplifiers. When the timing track signals READ T TRK are received at location C6 and B6, the positive going pulse to the DCD gate, generates the timing signals. The TP0 and TP1 outputs are applied to PA, location A5. The output of the power amplifier triggers a 10-μs delay during reading and writing data, producing a -3V output to inhibit any extraneous timing signals which may be generated as a result of cross talk between data and timing channels.

3.2.11 Counter Register (C) (Drawing No. 5)

The counter register, location D5-D7, Drawing No. 5, consists of four flip-flops used to control the blocks of information on the tape, as shown on the timing diagram (Figure 3-6). The outputs of the C2 and C3 flip-flops provide a four count used in formatting a data word on tape. Outputs C0, C1, and C3 provide a count of six for the mark-track information. Initially the counter register is set to 1000 by the 1000 ⟶ C0-3 pulse produced by the ground C-SYNCH and the positive transition of TP0. This count presets the counter in synchronization with the tape and starts the first count of both the four and six counts. The count sequence is shown on Table 3-1. The word count sequence (C2 and C3) repeats every four TP0 pulses and mark-track count (C0, C1, and C3) repeats every six TP0 pulses.

Table 3-1
Counter Register Sequence

C0	C1	C2	C3	TP0 Pulse
1	0	0	0	1 (C-SYNCH - TP0)
1	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
1	0	1	0	7
1	0	1	1	8
0	0	0	0	9
0	0	0	1	10
0	1	1	0	11
0	1	1	1	12

3.2.12 Window Register (W) (Drawing No. 3)

The window register W1-9, shown on Drawing No. 3, location D4-D8 provides a temporary storage for the mark-track information read from tape during all tape functions except WRTM. At the start of the loading operations all flip-flops are cleared by the 0 ⟶ WINDOW pulse generated by resetting the UP-TO-SPEED flip-flop on Drawing No. 6. When the tape is up to speed, the READ MK TRK information conditions the DCD gates associated with W9 flip-flop to allow the TP1 timing pulses to shift the mark track information through the window register. The next TP1 pulse which appears after the W2 flip-flop is set, will set the W1 flip-flop which will remain set until cleared by the 0 ⟶ WINDOW pulse. The outputs of the window register are applied as inputs to six separate AND gates which decode the inputs and generate specific mark-track level outputs.

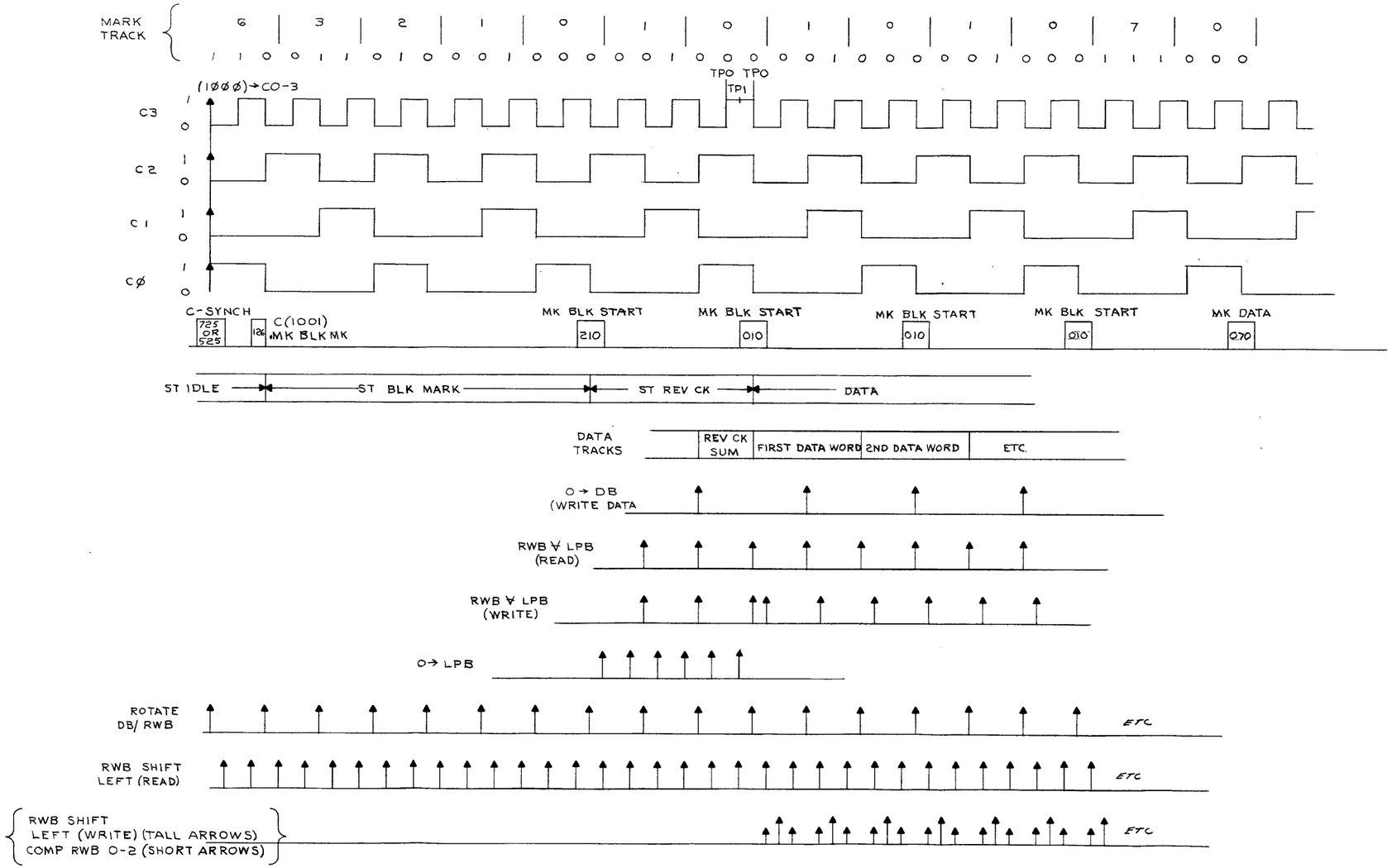


Figure 3-6 Timing and State Sequence Diagram (sheet 1)

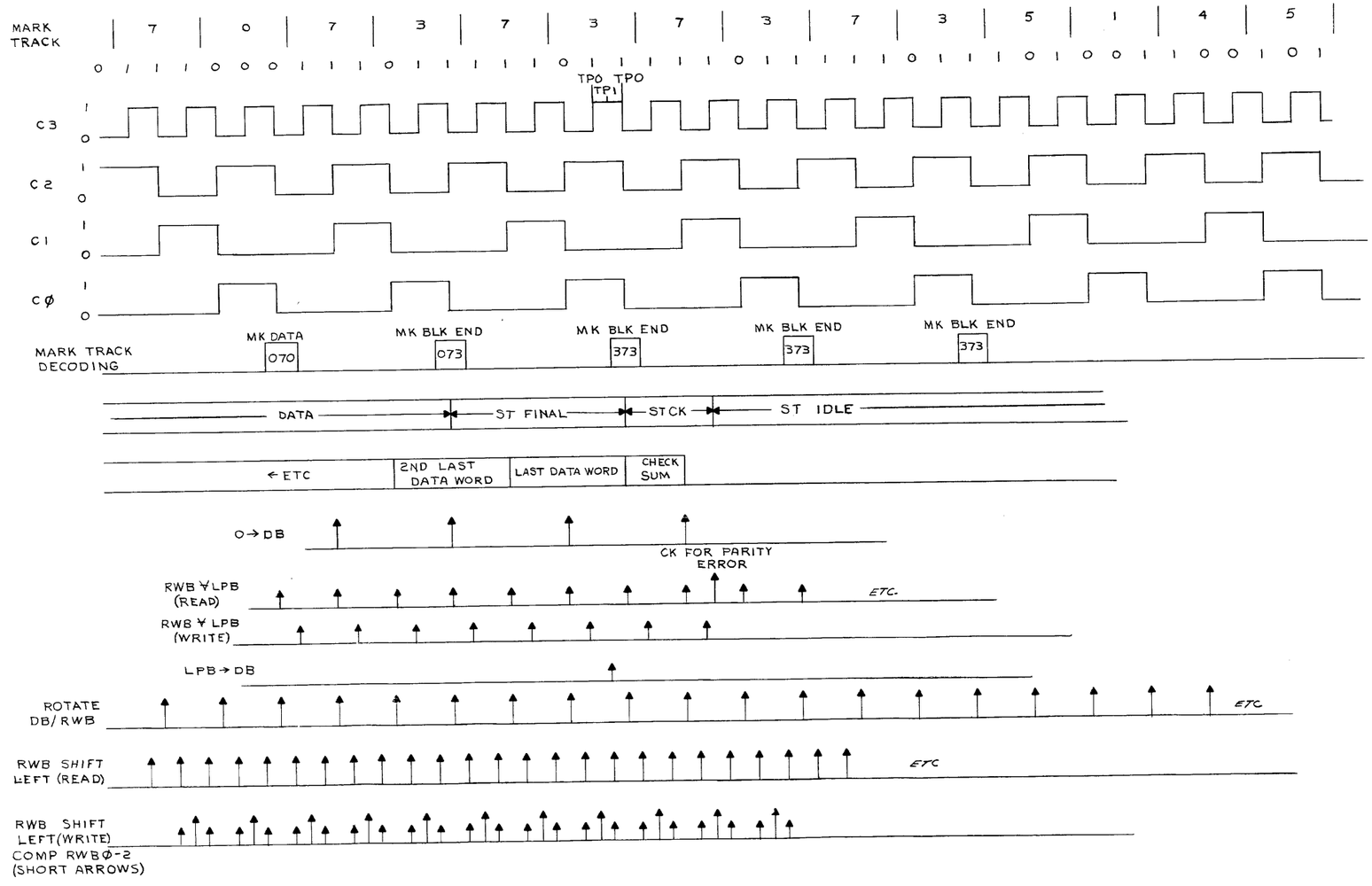


Figure 3-6 Timing and State Sequence Diagram (sheet 2)

3.2.12.1 Counter Synch Level (C-SYNC) - Initially, when reading mark-track information either in the forward or reverse direction, the first code to be recognized and used for synchronization is a result of the bit information formed by octal 525 or 725. This information appears after the reverse end mark codes sequence through the W-register. The bit configurations (shown on Figure 3-7) is decoded by the C-SYNCH gating logic (location C1), to produce a series of C-SYNCH level outputs which condition the control register. For the specific mark-track codes refer to Table 2-1.

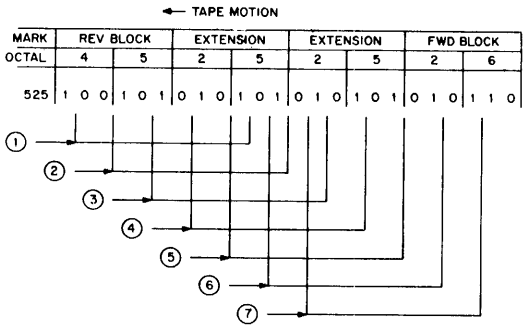


Figure 3-7 Mark-Track Decoding (C-SYNCH)

The first code recognized by the C-SYNCH gating appears at (1). These nine bits are decoded with the -3V output of S111 (location D2) and with $\overline{\text{WRTM}}$ and generate the C-SYNCH levels for all operations except write timing mark.

With two extension marks (E) inserted in the mark-track information, the C-SYNCH signal will appear six times at the input to the AND gate and produce the C-SYNCH level to reset the control clock. Only at the last decoding (6), however, will the control clock initiate a count and synchronize the counter with the mark-track information.

3.2.12.2 Start Block Marks (MK BLK MK) - The next bit configuration in the W-register, which is recognized, is the forward or reverse block mark. This information appears during the next TP1 pulse after the C-SYNCH level is generated, as shown on Figure 3-6. The positive transition of the TP0 pulse which precedes the TP1 pulse sets the counter register to (1001). The W-register information is gated with the $\overline{\text{WRTM}}$ level and the counter register outputs, C0(1), and C1(0), to generate the MR BLK MK outputs, as shown on Figure 3-8.

The octal 2 position of the reverse guard mark, in the forward tape direction, or octal 5 portion of the guard mark in the reverse tape direction is recognized together with the lock marks to generate the next mark-track signal MK BLK START as shown in Figure 3-9.

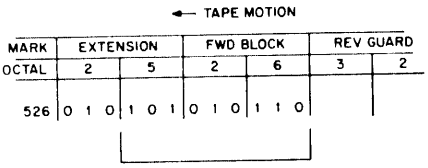


Figure 3-8 Mark-Track Decoding (MK BLK MK)

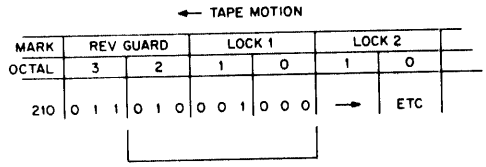


Figure 3-9 Mark-Track Decoding (MK BLK START-210)

The outputs from the W-register, except for W2, are AND gated and inverted resulting in the MK BLK START outputs at location C5. This occurs at the next 1000 count of the control register, as shown on Figure 3-6. This lock mark is the first of four that are programmed on tape. Each will generate the MK BLK START levels. The bit configuration required for the next three lock marks are shown in Figure 3-10.

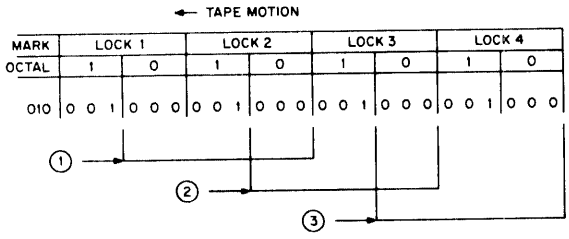


Figure 3-10 Mark-Track Decoding (MK BLK START-010)

The same AND gate which decoded the (210_8) W-register configuration will decode the (010_8) and produce the additional MK BLK START level, as shown on Figure 3-6.

3.2.12.3 Data Marks - The data mark follows the last lock mark and is decoded by AND gate R002, location B5 and C5. The W-register configuration is shown on Figure 3-11.

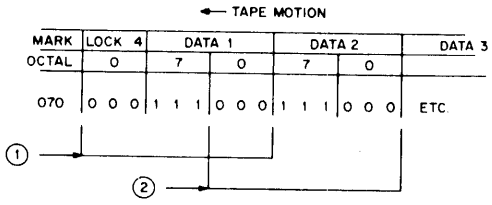


Figure 3-11 Mark-Track Decoding (MK DATA 070)

The -3V inputs are inverted and generates the MK DATA output levels as shown on Figure 3-6.

After the last data mark has been decoded, AND gate (location B7 and C7) decodes an octal 073 and three octal 373s from the W-register to generate a series of four mark block end signals (MK BLK END) as shown on Figure 3-12. This is accomplished by not decoding inputs from the W2 or W3 flip-flops.

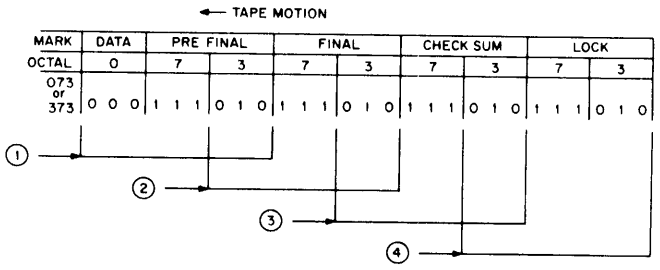


Figure 3-12 Mark-Track Decoding (MK BLK END)

The next two mark-track codes, guard mark (51) and block mark (45), which follow the lock mark, are not decoded and the decoding continues through the same sequence, as previously specified, until the end marks (222) are decoded by AND gate (location C8), which generates the MK END level.

3.2.13 State Register (Drawing No. 3)

The state register (Drawing No. 3, location B5-B7) is a ring counter which indicates the control states of the TC01 as determined by the mark-track decoding sequence. The state register is cleared each time the UP-TO-SPEED flip-flop (Drawing No. 6) is reset. The control states are sequenced through the state register by the positive transition of the SHIFT ST pulses which are produced by monitoring both the decoded outputs of the mark-track and by the outputs of the state register at location D3. The outputs of the state register are connected to the maintenance control panel to provide a visual indication during DECtape operations. Table 3-1 lists in sequence the various block marks and control states that are generated. The first five events occur prior to the generation of the first SHIFT ST pulse.

At event 6, the first block mark is decoded. The ground MK BLK MK level is inverted by S107 at location C3, and applied as one input to the two-input AND gate, location C3. The other input is held at -3V. This signal results in the first SHIFT ST pulse at event time 7, which sets the ST BLK MK flip-flop. At event time 10, the mark-track decoded output MK BL START is gated with the -3V ST BLK MK (1) output and generates the second SHIFT ST pulse. This pulse sets the ST REV CK flip-flop and resets the ST BLK MK flip-flop. The second MK BL START level produced by the mark-track decoding network, is gated with the -3V output of ST REV CK flip-flop to produce the third SHIFT ST pulse at event time 13, which sets the DATA flip-flop. The DATA flip-flop remains set for all data words and until the MK BLK END level is decoded which allows the SHIFT ST pulse at event time 17 to set the ST FINAL flip-flop. The second MK BLK END pulse is ANDed with the ST FINAL (1) output producing a SHIFT ST pulse, at event time 20, and sets the ST CK flip-flop. The ST CK (1) -3V output AND gated with the counter register output C2(1) sets the ST IDLE flip-flop at event time 23 which will allow the sequence of events, starting at event time 6, to repeat for the next block.

Table 3-2
Sequence of Block Marks and Control States

Event No.	Block Mark or State	Block Mark Code (Octal)
1	Tape Stopped (ST IDLE)	
2	Start Tape	
3	UP TO SPEED (1)	
4	C SYNCH	725 or 525
5	DATA SYNCH (1)	
6	C (1001) · MK BLK MK	126
7	SHIFT ST	
8	ST BLK MK (1)	
9	MK BLK START	210
10	SHIFT ST	
11	ST REV CK (1)	
12	MK BLK START	010
13	SHIFT ST	
14	DATA (1)	
15	MK DATA	070
16	MK BLK END	073
17	SHIFT ST	
18	ST FINAL (1)	
19	MK BLK END	373
20	SHIFT ST	
21	ST CK (1)	

Table 3-2 (Cont)
Sequence of Block Marks and Control States

Event No.	Block Mark or State	Block Mark Code (Octal)
22	C2 (1)	
23	SHIFT ST	
24	ST IDLE (1)	
25	Start at Event No. 6	126

3.2.14 Memory Field Register (MF) (Drawing No. 2)

The 3-bit memory field register (Drawing No. 2, location D1 and D2) uses data in the one outputs of BAC bits 6 through 8 to provide extended data addresses for the memory extension control of the PDP-8. The MF function requires a ground 0⟶MF pulse input to clear each flip-flop and a -3V LOAD STATUS B pulse input to load each flip-flop. The 0⟶MF pulse is applied to clear the MF at the end of each LOAD STATUS B pulse. The required delay is introduced by the LOAD STATUS B pulse from device selection (Drawing No. 6) as an input to PA location C2. The desired ground 0⟶MF pulse output is delayed until the trailing edge of the -3V LOAD STATUS B pulse appears at the PA input. When the MF has been cleared, the LOAD STATUS B input at event time three produces either a -3V or ground level $MF_0(1)$, $MF_1(1)$, and $MF_2(1)$ depending upon whether the flip-flop has been enabled by its BAC input. This information is returned to the PDP-8 memory extension control through NAND gates (Drawing No. 2, location B3 and B4). Upon receipt of a READ STATUS B pulse from the device selector, the -3V or ground level NAND outputs are transferred to their corresponding memory extension control addresses IM6, IM7, and IM8. Information contained in these NAND outputs represents the programmed extended address initially loaded into the MF by BAC6 (1) through BAC 8 (1).

3.2.15 Function Operations (Drawing No. 2)

Function bits FR1-FR3 of the status register A are decoded to provide one of the seven function levels which are used to select the tape unit operations. A description of the logical operations within the control unit for each function is described in the following paragraphs.

3.2.15.1 Move Tape - The move tape function (MOVE) used to reposition or rewind tape is implemented by a Load Status Register instruction which specifies all zeros in the Function Register FR1 through FR3 (Drawing No. 2). The move function allows the tape unit selected to move in the direction specified by the motion register (MR0) until the end of tape zone is detected, without allowing data transfers to occur.

The MR1(1) level from the motion register allows the BRM1 flip-flop to be set at the end of the XSA DY delay and starts the tape motion in the direction specified by MR0. When "up-to-speed" is reached the mark-track information is read from the tape. If no select error is detected, the tape ·

motion continues and the mark-track information is read without effect on the operation until the end zone is detected. The decoded end zone generates a MK END level (Drawing No. 3) which allows the END flip-flop (Drawing No. 14) to be set by the TP0 timing.

3.2.15.2 Search - The Search function is used to locate block numbers on tape. During this function, all information is read from the tape, however, only block numbers are transferred to the PDP-8 where the program performs a comparison of the information received with a specified block number to determine whether the two are the same.

The search function is initiated by an octal 1 in the function register FR1-FR3. When the tape transport comes "up to speed," the timing track pulses READ T TRK generate the TP0 and TP1 pulses, (Drawing No. 6). The control operations performed are similar to the READ function. The WREN (0) output allows the TP1 pulses to generate RWB SHIFT LEFT pulses which assemble the information from tape in the RWB. The decoded mark-track information produces up to seven C-SYNCH levels, the last of which generates the first ROTATE DB/RWB pulse and rotates the first half of the block number into the DB. Two more shift pulses are then generated at TP1 times to assemble the next half of the block number into the RWB, and the MK BLK MK signal is decoded to shift the state to ST BLK MK. At the C3 (0) transition another ROTATE DB/RWB pulse loads the data buffer with the block mark information and, at the same time, the TP0 pulse generates a 1 ⟶ DF pulse (Drawing No. 5 at location D1) to set the data flag generating a break request. In the normal mode, the DTF flip-flop is also set to request a program interrupt to determine whether the block number transferred is the block number desired. In the continuous mode the DTF is only set if a word count overflow WCO pulse is received.

Unless another function is specified, the control continues in the search function, the mark-track decoding is performed and the data is assembled and shifted in the DB/RWB. The 1 ⟶ DF pulse which sets the data flag will not be generated, however, until the next MK BLK is decoded.

During the ST REV CK state, the 0 ⟶ LPB and RWB ⩛ LPB are generated for the parity computation. The parity has no significance, however, during search and the PAR flip-flop is inhibited.

During the search function, the +1 ⟶ CA INH level, at location B6, will prevent the incrementing of the current address cycle in the PDP-8.

3.2.15.3 Read Data - The read data function is normally performed after the program has searched and and located the desired block number. Read data is specified by an octal 2 in function register FR1-FR3. After the search function is completed, the control is normally in the ST BLK MK state. When the mark-track information is decoded as a MK BLK START, the SHIFT ST pulse (Drawing No. 3) changes the state to ST REV CK. During the previous states of the search function the ROTATE DB/RWB and RWB SHIFT LEFT pulses were generated. No data read, however, was allowed to be transferred to the processor. The ST REV CH level enables the TP1 pulses to generate the 0 ⟶ LPB pulses (Drawing No. 5) which clears the LPB. The RWB ⩛ LPB pulses, which exclusive ORs the 6-bit RWB information into the LPB, are also produced during the ST REV CH. This permits the reverse check word (the last 6-bit read) to be included in the parity computation, and the last 0 ⟶ LPB pulse clears the LPB before the first data word is read. The ST DATA is entered and the data is assembled and shifted by the RWB SHIFT LEFT

and ROTATE DB/RWB pulses as described in the read and write sequence (Paragraph 3.2.16). Each time a ROTATE DB/RWB pulse is generated, a RWB $\forall$ LPB pulse allows the parity computation to be performed.

If the WC register is set, indicating that a word-count overflow has not occurred, the 1⟶DF pulse (Drawing No. 5, location D2) at the C2(0) transition will set the Data Flag (DF) requesting the 3-cycle data break to transfer the word in the DB to the PDP-8. When the request is granted, the ADDR AC pulse (location B5) clears the DF. The data-break request must be granted before the next ROTATE DB/RWB or the information in the DB is no longer valid, and a timing error will occur as a result of the ROTATE RWB/DB pulse and the DF (1) level.

This sequence continues until the end of the data portion of a block occurs which is signified by the ST CK state. When the ST CK flip-flop is reset, the contents of the LPB should contain all "ones" or the parity error will be indicated by the LPB$\neq$1 input which sets the PAR flip-flop. At this time in the normal mode, the ST CK(1) pulse will generate 1⟶DTF pulse which will set the DTF flip-flop. In the continuous mode, the DTF flip-flop will be set if a word-count overflow had been issued during the previous data block. If the DTF flip-flop is set, the programs must specify a new operation. If it is not set and the continuous mode is specified, the operation will continue as previously described. When a word-count overflow occurs during the middle of a data block, the data transfers will stop. The remaining words, however, are read and parity is computed.

3.2.15.4 Read All Function - The real-all function, specified by an octal 3 in the function register FR1-FR3, allows all information written in the data tracks on tape, including reverse check, block numbers, etc. to be read and transferred to the PDP-8 processor. Read all can be programmed initially or after a search function which locates a specific block on tape before reading begins. When the tape had reached speed, only one C-SYNCH level is required to set the DATA SYNCH flip-flop and the information on tape is read even though it may not be synchronized. This can occur in the middle of a data word on tape.

The operations within the DB/RWB during the read all function are similar to the operations which occur during the read-data function. The RWB SHIFT LEFT pulses (Drawing No. 5) are produced at time TP1 enabled by the WREN(0) output to assemble the information into the RWB. The ROTATE DB/RWB pulse then occurs as a result of the ROTATE ENABLE level and C3(0) transition, causing the information in the RWB to be transferred to the DB. The same enable level and pulse transition also generate anRWB $\forall$ LPB pulse which allows the parity computation. However, the parity flip-flop (Drawing No. 14) is disabled during the read-all function. The next two RP1 pulses again produce two RWB SHIFT LEFT pulses followed by another ROTATE ENABLE and RWB $\forall$ LPB pulse. At this time, the C2(0) input (Drawing No. 5), enabled by the READ ALL input will generate 1⟶DF pulse which sets the DF flip-flop, requesting a data break.

In the normal mode, with the FR0(0) V WRTM input applied, the 1⟶DF pulse will also set the DTF flip-flop requesting the program to specify a new operation. Although the next word is not transferred, the setting of the data flag may result in a timing error requiring a new function to be specified or a similar operation to be performed. In the continuous mode with FR0(1), the DTF flip-flop is set when the WCO pulse occurs from the PDP-8. The tape motion will continue, but no additional data transfers will occur.

During the read-all function, although parity is computed, mark-track information is decoded, and the state register changes, these operations have no effect on data transfer.

3.2.15.5 Write Data Function - The write data function, specified by an octal 4 in the function register FR1-FR3, is used to write data on tape in the data areas assigned by the mark-track coding. The write data function is normally initiated following a search operation which determines the block position on tape where the data will be written. The initialization process allows the tape to reach speed, the DATA SYNC flip-flop to be set, and the counter to be synchronized with the mark-track information. Specifying write data before the DATA SYNCH flip-flop has been set will result in no operation.

When the write data function is specified after a search function, the control is normally in the START BLOCK MARK state. The ST BLK MK (1) level is gated with the decoded window register output MK BLK START level (Drawing No. 3, location D3) to generate a SHIFT ST pulse which sets the ST REV CK flip-flop, changing the state of the control. Pulses 0⟶LPB and RWB ∀ LPB, a sequence of pulses (Drawing No. 5) will load and clear the LPB during the reverse check state. However, the reverse checksum which occurs one 6-bit word before the data state will be included in the parity computation. Pulse A0⟶DB generated during the ST REV CK by the C1 (0) transition, clears the DB and generates a 1⟶DF pulse at location C3 which sets the DF flip-flop and requests a data break. The ST REV CK (1) level is gated with C0 (1), location B2, to generate the WD EN level. This level allows the WREN flip-flop to be set at the C2 (0) transition and enable the data to be written. During the transition of C2 (0), the control enters ST DATA. The WREN (1) output, gated with TP1 at location B7 produces the first COMP RWB 0-2 pulse, which is required for the write sequence. With the WREN (1) flip-flop set, the RWB SHIFT LEFT pulses are produced at the C3 (1) transition. The sequence for the write operation is described in Paragraph 3.2.16. If a word count overflow has not occurred during the previous word, the data flag (DF) will be set each time the 0⟶DB pulse is produced. If a word count overflow is issued during a previous word, the write sequence continues, but the DF flip-flop is not set with the result that all zeros are written in the remaining block on tape.

At the end of a data block, the parity check character is loaded into the DB by the LPB DB0-5 pulse that is produced by the positive transition of the second MK BLK END level which is enabled by ST FINAL, C0 (1), and WRITE DATA. The LPB information is written on tape in the checksum slot the same as a data word.

In the normal mode at the end of a data block, the positive transition of the ST CK (0) level will set the DTF flip-flop and in the continuous mode the same transition will also set the DTF flip-flop provided that a word-count overflow WC (0) has occurred during the previous data block. The writers are disabled after the parity is written by the WREN flip-flop which is reset by the ground WD EN level produced when the data state is changed. The control continues to change states if DTF is not set and begins writing again in the block and the operations repeat in the same sequence.

3.2.15.6 Write all Function - The write-all function, specified by an octal 5 in the bits FR1-FR3 of the function register, allows nonstandard formats to be written on tape, such as the insertion of block numbers or codes at unusual locations on tape.

This function can be preceded by the search function which determines the position on tape where the information will be written and can be implemented at any time after the tape has come "up-to-speed" after only one C-SYNCH level has been generated, which may cause the writing to be displaced by a half word.

The positive transition of the WRITE ALL level, sets the W INH flip-flop (Drawing No. 5). This prevents the WREN flip-flop from being set and inhibit writing at this time. The timing sequence for the WRITE ALL function is shown in Figure 3-13. The positive transition when counter flip-flop C2 is set, will reset W INH provided that the WC flip-flop (Drawing No. 2), was previously set. The 0 ⟶ DB pulse is also generated at this time resulting in a 1 ⟶ DF pulse requesting a data break to write the first word.

If the write all function is specified before the middle of the area assigned on tape for a data word, the first word will be written in the next data area which follows. If the function is specified after the middle of the current data word position, the next data-word position will be skipped before the data word is written. The write sequence then continues. Parity is computed during this function, however, the LPB ⟶ DB0-5 pulse which is required to write parity is not produced. The state register continues to shift but has no effect on the operation.

In the normal mode, the 1 ⟶ DF pulse will set the DTF flip-flop generating an interrupt request when enabled by ENI (1). During continuous mode, when a word-count overflow occurs, the WCO pulse will set the DTF flip-flop. The WC (0) level at this time will also set the W INH flip-flop inhibiting the writing of future words on tape; however, the tape motion will continue.

3.2.15.7 Write Timing and Mark-Track - The write timing and mark-track functions, specified by an octal 6 in the function register is used to format a new tape by recording the timing and mark-tracks prior to the recording of data.

This function is only enabled with the WRTM/RDMK/NORMAL switch on the TC01 control panel in the WRTM position and with the WRITE ENABLE/WRITE LOCK switch of the TU55 transport in the WRITE ENABLE position. The control panel switch (Drawing No. 6) generates a SWTM level which is gated with MR1 (1) and the WRTM level to produce the TM ENABLE levels. The TM ENABLE level activates the 120 kc clock producing the CK1 and CK0 outputs which generate the TP0 and TP1 timing pulses.

The CK0 and CK1 and TM ENABLE outputs are applied to the T TRK write amplifier (Drawing No. 15) to generate the pattern to be written on the timing track.

The TM ENABLE level (Drawing No. 6) resets the UP-TO-SPEED flip-flop resulting in a 0 ⟶ WINDOW level which prevents mark-track information from being decoded. It also resets the DATA SYNCH flip-flop preventing synchronization of the control operations.

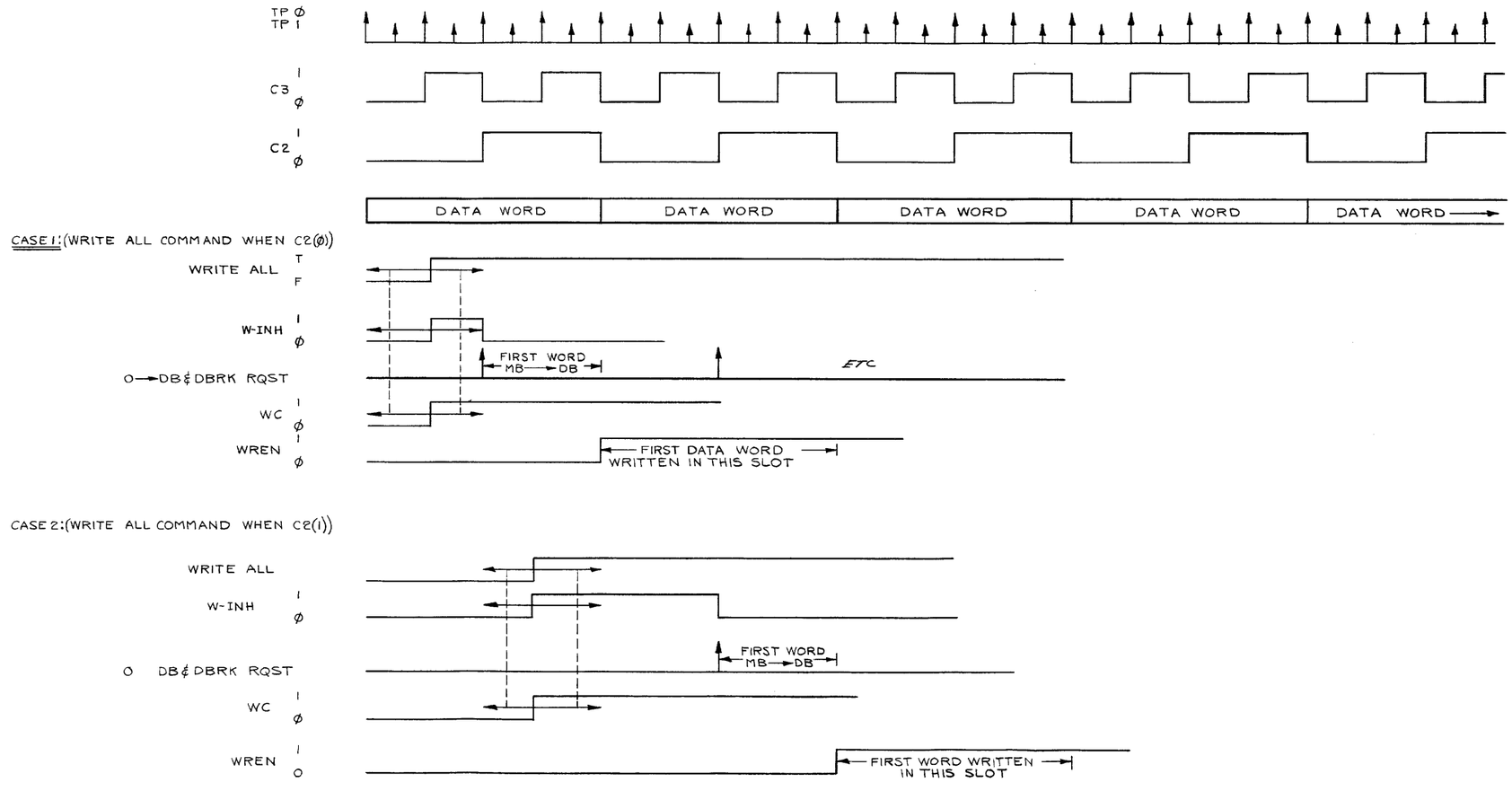


Figure 3-13 Write all Function, Timing Sequence Diagram (sheet 1)

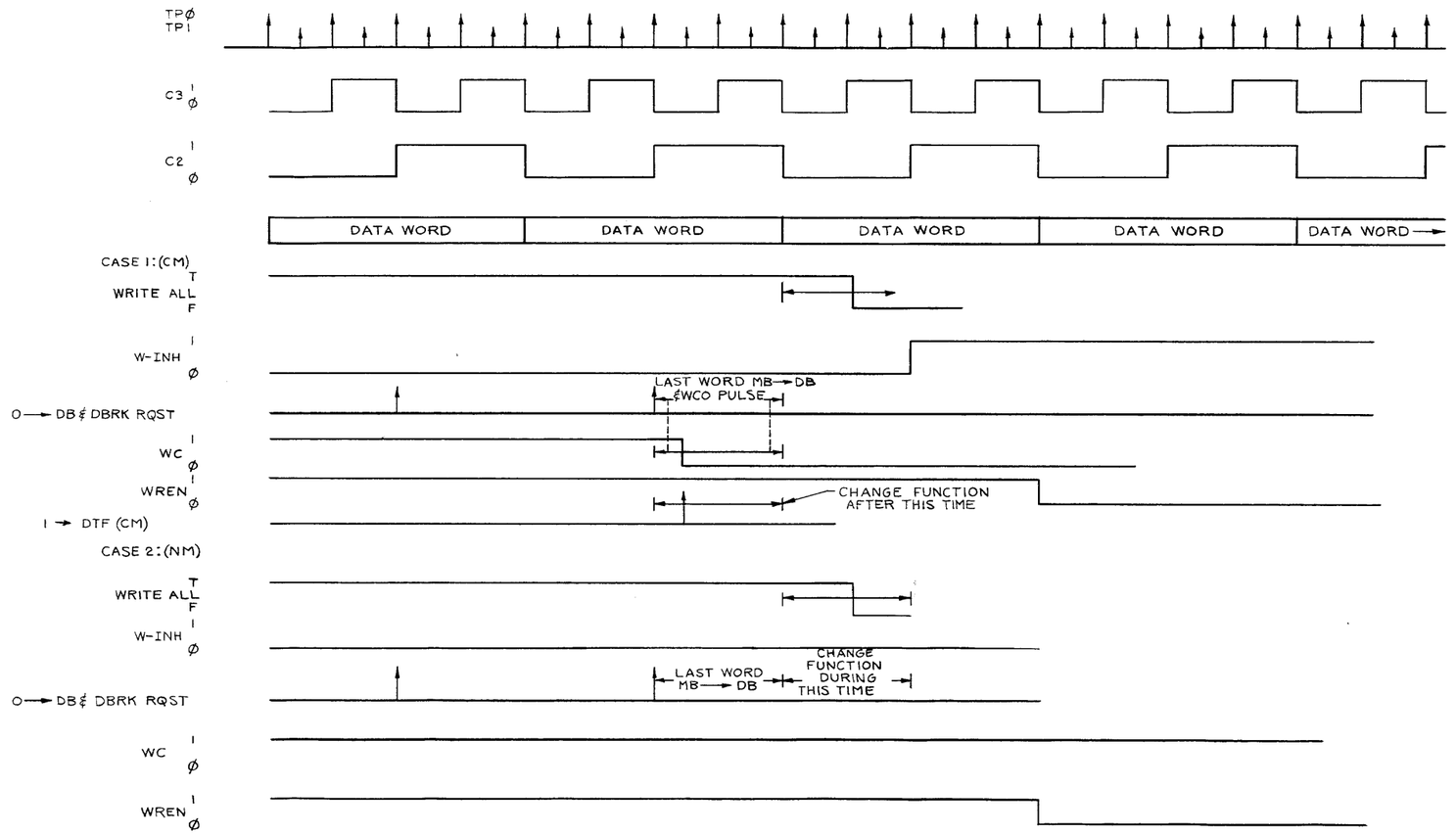


Figure 3-13 Write all Function, Timing Sequence Diagram (sheet 2)

The WRTM and SWTM levels are gated with associated outputs to produce the WRITE SET level (Drawing No. 5). At the C2 (0) transition, the WREN flip-flop is set and enables the data track amplifiers (Drawing No. 15) to write the information contained in the RWB. The first word that is written on tape, however, will be within the 10 ft of tape designated for the reverse end code and will not be read during the read tape function.

The WREN (1) level allows the RWB SHIFT LEFT pulses, the ROTATE DB/RWB pulses, and the COMP RWB 0-2 pulses to perform the write operation as described in Paragraph 3.2.16. The ROTATE DB/RWB at the C2 (0) transition generates the 0 ⟶ DB pulse which clears the DB and sets the DF flip-flop, requesting the first word.

The programming format for the mark-track requires that the mark-track information appear in bits 0, 3, 6, and 9 of the data word. The information received by the mark-track write amplifiers (Drawing No. 15) is from RWB0 (Drawing No. 4). Therefore, the only data bits which appear in this buffer are bits 0, 3, 6, and 9. This information also appears in data track 1 on tape which also receives information from RWB0.

When the WRTM function is completed, the TM ENABLE levels are held active by the SWTM and WREN (1) inputs (Drawing No. 6). Enough TP0 pulses are produced to cause the C2 (0) transition necessary to reset the WREN flip-flop (Drawing No. 5) and prevents the disabling of the write amplifiers with write current.

3.2.16 Read and Write Sequences

The sequence of events that occur during the read and write functions are summarized in Tables 3-2 and 3-3, respectively. Abbreviations and symbols used in these tables are defined in a list of abbreviations in Chapter 2. The times of each event are specified in terms of control clock pulses C2, C3 and timing pulses TP1. Illustrations of the bit contents of the RWB and DB sections after each event has occurred are shown in the diagrams in the last column of the tables. The DB/RWB registers are shown on Drawing No. 2.

The events for the read operation in Table 3-2, are programmed to assemble a 12-bit data word in the DB for subsequent transfer to the MB of the PDP-8 during a data break. At the start of the assembly, the first three bits 0 through 2 of the data word are strobed from the read amplifiers into the right half of the RWB (RWB 3-5). Bits 0 through 2 are then shifted left into the left half of RWB (RWB0-2) and the second three bits (bits 3 through 5) of the data word are strobed into RWB3-5. At this time, a parity check is performed on the first half of the 12-bit data word. The next event rotates the first half of the data word from the WRB into one half of the DB (DB6-11). The same sequence is followed to strobe the last six bits (bits 6 through 11) into the WRB and to perform a parity check on them. Another rotation transfers bits 0 through 5 from DB6-11 to another half of the DB (DB0-5) and bits 6 through 11 from the WRB to DB6-11. The 12-bit word is completely assembled in the respective halves of the DB and is ready for transfer to the BMB of the PDP-8.

Table 3-3
Sequence of Events During Write Operation[1]

Event No.	Event	Time of Event	Initiating Input[2]	Resulting Operation[3]
1	Begin assembly of first half of data word	C3(0) · C2(0) · TP1	RWB SHIFT LEFT (4A4)	First three bits from R/W amplifier outputs strobed into RWB 3-5. RWB: 0 1 2 3 4 5 Word Bits: x x x 0 1 2
2	Complete assembly of first half of data word	C3(1) · C2(0) · TP1	RWB SHIFT LEFT (4A5)	Bits 0 through 2 shifted left to RWB 0-2 and bits 3 through 5 from R/W amplifier outputs strobed into RWB 3-5. RWB: 0 1 2 3 4 5 Word Bits: 0 1 2 3 4 5
3	Perform parity check of first half of data word. Rotate first half of data word from RWB to DB	C3(0) transition from 1 to 0	RWB $\not\vee$ LPB (3B5) ROTATE DB/RWB (5D8)	Compute parity of RWB contents (i.e., bits 0 through 5). Rotate RWB 0-5 into DB 6-11 DB 0-5: x x x x x x DB 6-11: 0 1 2 3 4 5 RWB 0-5: x x x x x x
4	Begin assembly of last half of data word	C3(0) · C2(1) · TP1	RWB SHIFT LEFT (4A4)	Word bits 6 through 8 from R/W amplifier outputs strobed into RWB 3-5. Contents of DB same as in event 3. RWB: 0 1 2 3 4 5 Word Bits: x x x 6 7 8
5	Complete assembly of last half of data word	C3(1) · C2(1) · TP1	RWB SHIFT LEFT (4A5)	Bits 6 through 8 shifted left into RWB 0-2 and word bits 9 through 11 from R/W amplifier outputs strobed into RWB 3-5. Contents of DB same as in event 3. RWB: 0 1 2 3 4 5 Word Bits: 6 7 8 9 10 11

Table 3-3 (Cont)
Sequence of Events During Write Operation[1]

Event No.	Event	Time of Event	Initiating Input[2]	Resulting Operation[3]
6	Perform parity check of last half of data word	C2 (0) transition from 1 to 0	RWB ∀ LPB (3B5)	Compute parity of RWB contents (i.e., bits 6 through 11 in event 5).
	Rotate contents of RWB and DB		ROTATE DB/RWB (5D8)	Rotate data bits 0 through 5 into RWB 0-5, DB 6-11 into DB 0-5, and RWB 0-5 into DB 6-11 DB 0-5: 0 1 2 3 4 5 DB 6-11: 6 7 8 9 10 11 RWB 0-5: x x x x x x
7	Transfer complete assembled word in DB to PDP-8		1 ⟶ DF	

Notes:
1. The read sequence in table is assumed to start at the reading of a word in the middle of a data block.
2. Numeral-letter-numeral combination (e.g., 5C3) indicates location of initiating input on its respective engineering drawing (see Chapter 6).
3. Diagrams show contents of RWB and DB after event is completed.

Table 3-4
Sequence of Events During Write Operation(1)

Event No.	Event	Time of Event	Initiating Input(2)	Resulting Operation(3)
1	Request data word	ROTATE DB/RWB · C2(0) · WREN (1)	0 → DB (5D8) 1 → DF (5D2)	Clear data buffer and set DF flip-flop to request data word "n" from BMB. DB 0-5: 0 0 0 0 0 0 DB 6-11: 0 0 0 0 0 0 RWB 0-5: last half of word "n-1"
2	Data word "n" transferred from BMB to DB	At completion of PDP-8 instruction in progress	BMB → DB (5C8)	12-bit data word "n" transferred to DB. DB 0-5: 0 1 2 3 4 5 DB 6-11: 6 7 8 9 10 11 RWB 0-5: last half of word "n-1"
3	Rotate contents of RWB and DB and write bits 0 through 2 of word "n"	C2(0) transition from 1 to 0	ROTATE DB/RWB (5D8)	DB 0-5 rotated into RWB 0-5, and DB 6-11 into DB 0-5. RWB 0-2 provides bits 0, 1, 2 as inputs to write amplifiers. DB 0-5: 6 7 8 9 10 11 DB 6-11: x x x x x x RWB 0-5: 0 1 2 3 4 5
4	Complement bits 0 through 2 and write complemented bits	C3(0) · C2(0) · TP1	COMP RWB 0-2 (4A8)	Complement contents of RWB 0-2 to provide complement bits $\overline{0}, \overline{1}, \overline{2}$ as inputs to write amplifiers. Contents of DB remain same as in event 3. RWB 0-5: $\overline{0}$ $\overline{1}$ $\overline{2}$ 3 4 5
	Computes parity of bits 0 through 5 or word "n" (see Section 3.14)		RWB ∀ LPB (3B5)	Compute parity of RWB contents (i.e., bits 0 through 5) at end of event 3.

Table 3-4 (Cont)
Sequence of Events During Write Operation (1)

Event No.	Event	Time of Event	Initiating Input(2)	Resulting Operation(3)
5	Shift contents of RWB to left and write RWB bits 3-5	C3 (1) · C2 (0)	RWB SHIFT LEFT (5A8)	Contents of RWB 0-5 shifted left and bits 3, 4, 5 provided as inputs to write amplifiers. Contents of DB remain same as in event 3. RWB 0-5: 3 4 5 x x x
6	Complement bits 3 through 5 and write complemented bits.	C2 (0) · C3 (1) · TP1	COMP RWB 0-2 (4A8)	Complement contents of RWB 0-2 to provide complement bits 3, 4, 5 as inputs to write amplifier. Contents of DB remain same as in event 3. RWB 0-5: $\overline{3}$ $\overline{4}$ $\overline{5}$ x x x
7	Rotate contents of RWB and DB and write contents of RWB 0-2.	ROTATE DB/RWB · C2 (1) · WREN (1)	ROTATE DB/RWB (5D8)	DB 0-5 rotated into RWB 0-5 and contents of RWB 0-2 provide bits 6, 7, 8 as inputs to write amplifier.
	Request next data word		0 → DB (5D8) 1 → DF (5D2)	Clear data buffer and set DF flip-flop to request data word "n+1" from BMB. DB 0-5: 0 0 0 0 0 0 DB 6-11: 0 0 0 0 0 0 RWB 0-5: 6 7 8 9 10 11
8	Data word "n+1" transferred from BMB to DB	At completion of PDP-8 instruction in progress.	BMB → DB (5C8)	12-bit data word "n+1" transferred to DB. "n+1" bits DB 0-5: 0 1 2 3 4 5 "n+1" bits DB 6-11: 6 7 8 9 10 11 "n" bits RWB 0-5: 6 7 8 9 10 11

Table 3-4 (Cont)
Sequence of Events During Write Operation(1)

Event No.	Event	Time of Event	Initiating Input(2)	Resulting Operation(3)
9	Complement bits 6 through 8 of word "n" and write complemented bits.	C3(0) · C2(1) · TP1	COMP RWB 0-2 (4A8)	Complement contents of RWB 0-2 to provide complement bits $\overline{6}$, $\overline{7}$, $\overline{8}$ to write amplifiers. Contents of DB remain the same as in event B. RWB 0-5: $\overline{6}$ $\overline{7}$ $\overline{8}$ 9 10 11
	Perform parity check of bits 6 through 11 of word "n"		RWB $\forall$ LPB (3B5)	Compute parity of RWB contents (i.e., bits 6 through 11) in event 8.
10	Shift contents of RWB to left and write bits 9 through 11 of word "n"	C3(1) · C2(1)	RWB SHIFT LEFT (5A8)	Contents of RWB 0-5 shifted left and bits 9 through 11 of word "n" provided as inputs to write amplifiers. Contents of DB remain same as in event 8. RWB 0-5: 9 10 11 x x x
11	Complement bits 9 through 11 of word "n" and write complemented bits. This event completes writing of word "n"	C3(1) · C2(1) · TP1	COMP RWB 0-2 (4A8)	Complement contents of RWB 0-2 to provide complement bits $\overline{9}$, $\overline{10}$, $\overline{11}$ of word "n" as inputs to write amplifiers. Contents of DB remain same as in event 8. RWB 0-5: $\overline{9}$ $\overline{10}$ $\overline{11}$ x x x
12	Repeat step 3 and continue sequence of write word n+1	C2(0) transition from 0 to 1	ROTATE DB/RWB (5D8)	DB 0-5 rotated into RWB 0-5 and DB 6-11 into DB 0-5. RWB 0-2 provide bits 0, 1, 2 of word "n+1" to write amplifiers. "n+1" bits DB 0-5: 6 7 8 9 10 11 obsolete "n" bits DB 6-11: 9 10 11 x x x "n+1" bits RWB 0-5: 0 1 2 3 4 5

Notes:
1. The write sequence in the table is assumed to be operation for the writing of a word "n" while in middle of a data block.
2. Numeral-letter-numeral combination (e.g., 5B4) indicates location of initiating input on its respective engineering drawing.
3. Diagrams show bit contents of RWB and DB after event is completed.

The events for the write operation in Table 3-4 are programmed to request a 12-bit data word from the PDP-8, store it temporarily in the DB, and transfer it in 3-bit segments to the write amplifiers. The first half of the 12-bit data word is stored in one section of the DB (DB 0-5) and the second half (DB 6-11) in another section. A DB/RWB rotation transfers the first half of the 12-bit word into the RWB and makes the first three bits (bits 0 through 2) available to the write amplifiers. A parity check is then performed on the first half of the data word. In addition, bits 0 through 2 are complemented and supplied to the write amplifiers. Then the contents of RWB are shifted left so that bits 3 through 5 replace bits 0 through 2 in RWB 0-2. Bits 3 through 5 are now available to the write amplifiers in normal and complement form in the same manner as bits 0 through 2.

Event 7 on Table 3-4 rotates the second half of the data word into the RWB, where it is available to the write amplifiers in the same sequence as that used for the first half of the word. During this event, the next data word is requested and each half is temporarily stored in its appropriate section of the DB as at the start of the sequence. The sequence for writing the stored data word can be started as soon as the writing of the preceding data word is completed.

3.2.16.1 Read/Write Control Signals - The control signals which cause the read/write sequence to occur are produced by the logic shown on Drawing No. 5. The timing sequence in relation to the information transfer is shown on Figure 3-6, sheets 1 and 2.

The following paragraphs are descriptions of the control signals and their origin.

a. RWB SHIFT LEFT

The RWB SHIFT LEFT pulses are required to shift the RWB register to the left during the read and write operations. Although several conditions must be satisfied to generate these pulses, the RWB SHIFT LEFT pulses for reading occur at every TP1, those for writing at every other TP0.

The network for generating RWB SHIFT LEFT pulses (shown on Drawing No. 4, location B7) includes two DCD input gates. One gate initiates pulses for the read operation and is enabled when the write-enable (WREN) flip-flop is reset. When the ground TP1 pulses appear at the input to the DCD gate, the PA produces corresponding ground WRB SHIFT LEFT pulses. The other DCD gate initiates pulses for the write operation and is enabled when the WREN flip-flop is set during the write functions.

The RWB SHIFT LEFT pulses generated are supplied as inputs to Drawing No. 4.

b. COMP WRB 0-2

Ground COMP RWB 0-2 pulses are required to complement RWB flip-flops 0 through 2 in Drawing No. 4, to convert the bits contained in the flip-flops to the complementary form. This operation is performed because of the phase recording method used which requires that the word bits be furnished in complementary as well as in normal form. The COMP RWB 0 through 2 pulses occur at every TP1.

The DCD input gate (Drawing No. 5, location B7) for the PA which generates COMP RWB 0-2 pulses is enabled when the write-enable (WREN) flip-flop is set. When TP1 pulses appear at the gate input, the PA produces ground COMP RWB 0-2 pulses for application to RWB 0-2 (Drawing No. 4.) The COMP RWB 0-2 output is also used as an enabling input for the generation of RWB $\forall$ LPB pulses.

c. Rotate DB/RWB

The ROTATE DB/RWB pulse, location B7, is required to transfer the contents of the RWB to DB 6-11, the contents of DB 6-11 to DB 0-5, and the contents of DB 0-5 to RWB 0-5.

The pulse is generated when the counter register is reset by the 1000 ⟶ C3 pulse and by the C3 (0) transition when the ROTATE ENABLE level is present. Before the counter is in synchronization with the mark-track information, no ROTATE DB/RWB pulses will occur during the search or read data functions. During the search function, this allows the ROTATE DB/RWB pulse to be synchronized with the first six bits of the block number preventing the block numbers from being out of sequence.

d. 0 ⟶ DB

The 0 ⟶ DB pulse, location C6 (Drawing No. 5) is generated to clear the DB and to request the next word for data transfer during write operations. During the write data function, the ST REV CK (1) gated with the WRITE DATA level to generate the 0 ⟶ DB during the reverse check state to allow the first word to be available when the ST DATA is entered. The 0 ⟶ DB pulses are then produced at the second gate circuit by the ROTATE DB/RWB when pulse WREN flip-flop is set.

During the write-all function the first data word is made available by the 0 ⟶ DB pulse enabled by the third gate when the ROTATE DB/RWB pulse is produced. The subsequent 0 ⟶ DB pulses during this function are produced by the second gating circuit previously described.

e. BMB ⟶ DB

The ground BMB ⟶ DB pulse (Drawing No. 5, location B2) is used to load the DB register in Drawing No. 4 with the data bits, BMB 0-BMB 11 from the PDP-8 memory buffer.

The BMB-DB ground pulse is produced by the T2 timing pulse input, from the PDP-8 at pin T of connector W021, location A3. The T2 pulse is inverted by S107 and gated into PA603 when the ground DATA OUT level is produced. When a PDP-8 Data break has been granted, the -3V B(BREAK) level at pin P of connector W021, location B5, is gated with -3V FR1 (1) level, produced during a write function or select error, to produce the DATA OUT levels.

3.2.17 Longitudinal Parity Buffer Operation

The longitudinal parity buffer (LPB) (Drawing No. 3, location B1-B4) performs the parity check of the information in the data tracks. Essentially the parity check reads the number of binary zeros in each half of 12-bit data words and forms a parity bit which is recorded in the checksum control word at the end of the data block. The checksum is computed by complementing the bits of the LPB when the respective bit of the RWB is a 0. The LPB register outputs are gated at location B2 (Drawing No. 3) to produce the LPB=1 and LPB≠1 levels. If all LPB register flip-flops are not set during a read data operation, the LPB≠1 level will set the parity flip-flop (PAR)(Drawing No. 14) indicating a parity error has occurred.

At the end of a write data operation, the contents of the LPB is gated into DB 0-5 to be written after the last data word.

3.2.17.1 LPB Control Signals - The signals which control the LPB operations are defined in the following paragraphs and are produced by the logic shown on Drawing No. 5. The timing sequence for these signals are shown on Figure 3-6, sheets 1 and 2.

a. 0 ⟶ LPB Pulse

The 0 ⟶ LPB pulse clears the LPB at the beginning of each block. Six pulses are generated by TP1 during the reverse check state, ST REV CK (1) to initialize the LPB register for computation of the parity character. However, only the last pulse is required for the operation.

b. RWB ∀ LPB Pulse

The RWB ∀ LPB pulse is used to perform the parity computation from the RWB to the LPB. The parity is computed at the same time the ROTATE DB/RWB pulse is generated during a read operation and at the same time the COMP 0-2 pulse is produced during the write operation.

c. LPB ⟶ DB 0-5

A LPB ⟶ DB 0-5 pulse, location C7, is required at the end of the ST FINAL block to initiate the formation of a parity bit for recording the checksum control word at the end of the data block.

The enabling conditions used for the generation of the LPB ⟶ DB 0-5 pulse are a WRITE DATA level from the function decoder, ST FINAL (1) level from the state counter, and a C0 (1) level from the control clock. When a ground MK BLK END pulse from the mark-track decoding network appears at the gate 603, LPB ⟶ DB 0-5 pulse is produced. This pulse is transferred to the RWB and DB registers in Drawing No. 4 for use in gating information received from LPB 0 (1) through LPB 5 (1) into corresponding DB 0-5.

3.2.18 Power Clear (Initialize) and Error Stop Logic

The PDP-8 Processor produces, and transmits to the TC01 control logic, a series of power clear (PWR CLR) pulses whenever the processor is started or stopped. The PDP-8/I, under these same conditions, generates a single pulse called INITIALIZE. These pulses, inverted at location A3, Drawing No. 14, are applied to the PA, location C2, together with the error stop signal, to generate the PWR CLR + ES pulses. The error stop signal is produced by monitoring the outputs of the error flip-flops MKTK, SEL, TIM, and END at location C4. When a (1) condition exists on any input to the NOR gate, as a result of an error, the ERROR STOP level will be produced. The ground PWR CLR pulses are used to reset the DATA SYNC flip-flop, WREN flip-flop, MF 0-2, DTF flip-flop, and the DF flip-flop when power is initially applied or removed from the PDP-8. In addition, the ground PWR CLR + ES signal will continually set the U + M flip-flop (Drawing No. 6) enabling the delay to prevent UP-TO-SPEED flip-flop from being set during the detection of an error or when the PWR CLR (INITIALIZE) pulse(s) are received.

3.2.19 Increment CA Inhibit (+1 → CA INH)

The +1 → CA INH signal (Drawing No. 5, location B6) is generated during the search function to prevent the incrementing of the current address. When the current address (CA) is not incremented, the block number is placed in core memory at the same location for each block number transferred.

3.2.20 Address Accepted

The address accepted pulse (ADDR ACC) (Drawing No. 5, location B5) is received at connector W021 from the PDP-8 during the 3-cycle data break. This pulse clears the DF flip-flop when the fixed data address, specified by the control, has been accepted for data transfer.

3.2.21 Transfer Direction

Function bit FR1 is used to indicate to the PDP-8 processor the direction of data transfer. During write functions, bit FR1 of the function register is "one," indicating transfer out of the PDP-8.

3.2.22 B RUN Level

The B RUN level input is received from the PDP-8 at location A2, Drawing No. 14. The B RUN (0) input, indicating that the PDP-8 is stopped, is used to reset the motion register flip-flops MR1 and BMR1 (Drawing No. 2) and is applied to the TU55 transports to halt all transport motion.

3.2.23 Fixed Address

The fixed address is a preselected (wired) memory address specified by the TC01 control. The address is determined by logic levels applied to DATA ADDR (0-11) at connector W021 location A5-A8, Drawing No. 2. This address determines the memory location of the data which is transferred to the memory buffer in the PDP-8 during the 3-cycle data break.

3.2.24 Interrupt Request

The INTERRUPT REQUEST level (location B1, Drawing No. 6) from the control is used to initiate a program interrupt in the PDP-8 processor. The interrupt enable is determined by the status of the ENI flip-flop (Drawing No. 2). When ENI is set, either an error flag EF (1) input or DECtape flag DTF (1) will result in the request for a program interrupt.

3.2.25 ERROR FLAGS (EF)

The five flip-flops (Drawing No. 14) produce error signals at the occurrence of any of the errors listed under the STATUS B functions in Table 2-4. When a specific type of error occurs, the error detection circuits shift the appropriate flip-flops to a 1 state.

The error input conditions that initiate a specific type of error signal are as shown in Figure 3-14. All error flip-flops are cleared by either a ground B PWR CLR pulse or a ground pulse from the output at location C6. These pulses are produced when a BAC 10 (0) level from the PDP-8 and a XOR STATUS A pulse from the device selector appear simultaneously at the gate input.

When any error signal except PAR appears at one of the inputs to NOR gate location B4, the gate produces an ERROR STOP output level. This output is used in forming the PWR CLR+ES signal. The same output is also passed through an inverter to produce an error flag EF (1) or EF (0) level. EF (1) and EF (0) levels are also provided when a PAR error signal appears at the input of inverter at location B3.

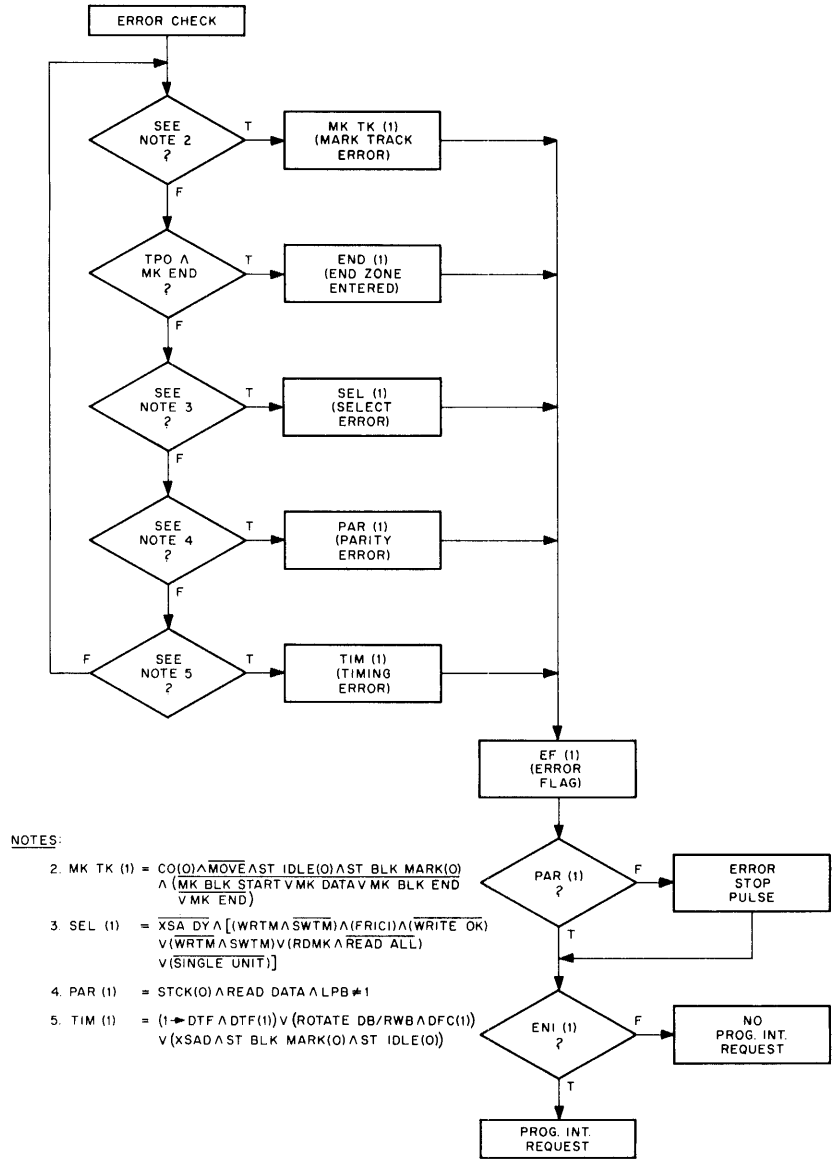


Figure 3-14 Error Check Flow Diagram

The EF (1) level resulting from any of the error signals is passed through another inverter to produce a corresponding complementary EF (1) level. Ground level EF (1) serves as one of the inputs to the NAND gate (Drawing No. 6, location B2) for generating an INTERRUPT REQUEST level while the -3V EF (1) level is used as one of the inputs to the NAND gate (Drawing No. 2, location B8). This gate, and similar ones for specific errors, are enabled by a PDP-8 READ STATUS B instruction to provide outputs which show the status of the TC01.

3.2.25.1 Mark-Track Error (MK TRK) - A MK TRK error signal is produced by MK TRK flip-flop (Drawing No. 14, location D6) when information read from the mark channel is erroneously recorded. When MK TRK errors are detected by the input gating, the gating output enables the DCD input gate of the flip-flop. A ground C0 (0) pulse from the control clock will set the flip-flop to a 1 state. A ground C0(0) pulse indicates that a 6-bit character has been read from the mark-track and is in the window.

One input to the MK TRK gating circuit represents one of four mark-track codes which is MK BLK START. These codes appear at times throughout the reading of the DECtape.

Other inputs to the gating circuit prevent MK TRK error indications during a MOVE function and during the ST IDLE and ST BLK MARK intervals. These intervals are indicated by -3V ST IDLE (0) and ST BLK MARK (0) levels. The MK TRK decodings are not valid during the ST IDLE and ST BLK MARK intervals because the control may not be synchronized with the DECtape at these times.

3.2.25.2 Select Error (SE) - A select error (SE) is produced by SEL flip-flop (Drawing No. 14) when any of the select errors listed in Table 2-4 are detected. After the input gate is enabled by an SE detection signal, the flip-flop is set by a ground XSA DY pulse at the gate input.

The following conditions will result in an SE error:

a. WRTM · $\overline{\text{SWTM}}$: MCP switch is not set on WRTM while PDP-8 program is attempting to write timing and mark data on new tape.

b. $\overline{\text{WRTM}}$ · SWTM: MCP switch is set on WRTM while PDP-8 program has specified another function.

c. FR3 (1) · $\overline{\text{WRITE OK}}$: DECtape transport control switch is set on WRITE LOCK while PDP-8 program is attempting to write.

d. RD MK · $\overline{\text{READ ALL}}$: MCP switch is set on RD MK but READ ALL function is not specified by PDP-8.

e. The function register contains a binary 111 which is not a legal function.

In addition to the conditions listed, the single unit comparator circuits shown on Drawing No. 14, (location A5) monitors the single unit line from the TU55 transports and generates a select error (SE) output if the line indicates either no units or more than one unit have been selected. This is effectively accomplished by noting the resistance of the SINGLE UNIT line and generating a ground select error level (SE) if the resistance is not within the specified limits.

With no units connected, the voltage at pins E and K of comparator W520 is -9V. The voltage at pin D and pin L is held constant at -7.5V and -5V, respectively, by the resistance network consisting of R1, R2, and R3. When this condition exists, pin D being more positive than pin E will cause a ground level SE output at pin H indicating a select error. When one unit is selected, the resistance of the line which is effectively in parallel with resistor R5, results in a voltage at pin K which is between the constant voltage at pin D of -7.5V and pin E of -5V. This voltage condition prevents the difference amplifiers from conducting, and the output at pin H and N will be -3V indicating a no-error condition. If more than one unit is selected on the line, the resistance in parallel with R5 will be decreased resulting in a voltage at pin K more positive than the -5V at pin L and the difference amplifier will conduct, resulting in a ground SE output at pin N.

3.2.25.3 Parity Error (PAR) - A PAR error signal is produced by PAR flip-flop (Drawing No. 14, location D4), during a READ DATA function if the LPB check at the end of the data block does not equal 1. The READ DATA and LPB $\neq$ 1 levels at the inputs of NAND gate (location C4) indicate the error condition and enable the DCD input gate to the flip-flop. Then a ground ST CK (0) pulse at the gate input will set the flip-flop. A ST CK (0) pulse occurs at the end of a data block.

3.2.25.4 Timing Error (TIM) - A timing error (TIM) is produced by the TIM flip-flop (Drawing No. 14) when any of the TIM error conditions listed in Table 2-4 are detected.

One operation that produces a timing error is to ROTATE DB/WRB when a DF (1). An error occurs because the data in the DB is no longer the same as it was at the instant the DF was set. The illegal operation is indicated to the TIM flip-flop when a ROTATE DB/WRB ground pulse appears at the DCD input gate at a time when the gate is enabled by a DF (1) ground level.

Another TIM occurs when a 1 ⟶ DTF ground pulse appears at the input to the DCD input gate of PA S603 (location D4) at a time when this gate is enabled by a DTF (1) ground level. This illegal condition means that the TC01 is attempting to set the DTF at the end of a current operation but that the program did not clear the DTF at the end of the last operation. The error is indicated to the TIM flip-flop by collector triggering its 1 output with the ground level generated by the amplifier.

A third TIM occurs when -3V levels appear simultaneously at each input to 4-input NAND gate (location D3). This condition is illegal because it indicates that an attempt is being made to READ DATA or WRITE DATA while passing over the data position on the tape. The -3V ST BLK MARK (0) and ST IDLE (0) input levels indicate that the head is not passing over the ST BLK MARK and ST IDLE blocks and therefore is passing over the data position. The -3V XSAD input is a standard 100-ns pulse which is generated by PA S603 (location C1 (14C1)) 400 ns after receipt of an XOR STATUS A pulse. When all inputs to the NAND gate are -3V, the resulting ground level is used for collector triggering the 1 output of the TIM flip-flop.

3.2.25.5 End Error (END) - In normal operation the window register contains an end zone code (222) when the end zone of the DECtape is reached. At this time the ground level at the window decoder output serves to enable the DCD input gate to the END flip-flop (Drawing No. 14, location D3). When the next TP0 appears at the gate input, the flip-flop is set. A ground level at the 0 output of the END flip-flop indicates an error it it is not expected by the program but is legitimate if used to indicate the end of a normal operation (e.g., rewind).

3.2.26 DECtape Flag (DTF)

The DECtape flag (DTF) network in the top center of Drawing No. 5 provides appropriate DTF output control levels which indicate the completion of specific operations.

DTF flip-flop is cleared by either collector triggering its 0 output with a ground level from NAND gate R123 (location D5) or by the appearance of a PWR CLR ground pulse at its direct clear input. A ground level for clearing through the 0 output is provided when a -3V BAC 11 (0) level from the PDP-8 and a -3V XOR STATUS A pulse appear simultaneously at the input to the NAND gate. When cleared, a ground 1⟶ DTF pulse from one of three input gating circuits will set the flip-flop to a 1 state.

The inputs to gating circuit location C6 indicate the following conditions:

a. FR3 (1): selection of any one of the SEARCH, READ ALL or WRITE ALL functions by function register.

b. WRTM: selection of WRTM function by function register.

c. FR0 (1): selection of CM of operation.

When a FR3 (1) or WRTM ground level and a -3V FR0 (1) level appear at the gating circuit input, the resulting ground level enables the DCD input gate to PA S603 (location C5). A ground WCO pulse input at the DCD input gate will produce the desired PA output pulse. The ground WCO input pulse is necessary because DFT settings in the NM are inhibited in the CM until a WCO has occurred.

One of the DCD input gates to PA S602 (location C4) is enabled when a -3V WRTM + FR3 (1) and a -3V FR0 (0) (indicating NM) appear simultaneously at the inputs to the NAND gate. Then when a ground 1⟶DF pulse is applied to the DCD gate, the PA generates the desired 1⟶DTF pulse.

Another input gating network controls the generation of a 1⟶DTF pulse at the start of the parity check in the NM or CM. In the NM, either a ground level READ DATA or WRITE DATA input from the function decoder plus a FR0 (0) level input enables DCD input gate (5D4). Then the appearance of a ground ST CK (0) from the state register (Drawing No. 3) at the start of the parity check causes the desired 1⟶DTF pulse to be generated. In the CM, an enabling input is applied to the DCD input gate when the RD + WD, FR0 (1) and WC (0) inputs are at -3V.

3.2.27 Panel Indicator Drivers

The indicator drivers in Drawing No. 12 control the indicator lamps on the Maintenance Control Panel. These lamps are remote indicators of various TC01 flip-flops and are lighted when a -3V level from the 1 output of the respective flip-flop appears at the input of the indicator driver.

CHAPTER 4
INSTALLATION

This section contains general information on the installation and maintenance of the TC01 DECtape control. The installation procedures refer to a single cabinet installation of both TC01 control and two TU55 DECtape transports. Installation information for mounting additional TU55 transports or TC01 control in an existing cabinet is available upon request.

4.1 INSTALLATION PROCEDURES

The TC01 DECtape control and associated TU55 transports are shipped either as a single unit cabinet mounted and crated or as individual units to be installed in an existing cabinet. The installation information in this chapter refers primarily to cabinet mounted units as the requirements for separate units vary according to the specific existing system.

Upon receipt of the unit, an initial visual inspection should be performed to insure that no obvious physical damage has been incurred during shipment.

4.1.1 Site Preparation

No special site preparation is required for the installation of the TC01 unit. Adequate clearance must be provided for proper installation and for servicing. Figure 4-1 shows the installation dimensions required by the unit.

When the cabinet is not physically attached to the PDP-8 console, both the power and signal cables enter through holes provided in the base of the cabinet. Casters are mounted on the cabinet base to enable the unit to be easily positioned and to allow sufficient clearance for the cables. No subflooring is normally required.

4.1.2 Environmental Conditions

The environmental conditions for the proper operation of the TC01 control unit are limited by the magnetic tape used with DECtape. The acceptable environmental conditions for the magnetic tape are an ambient air temperature between +60°F and +80°F with a relative humidity level between 40% and 60%. The TC01 DECtape control operating environment is the same as that required by the PDP-8 processor.

The installation site must also be as free as possible from excess dirt and dust, corrosive fumes and vapors, and strong magnetic fields

4.1.3 Power and Cable Requirements

The TC01 control and associated TU55 transports operate from single phase line voltage of 105V to 125V, 60 c/s. The maximum current requirement is dependent on the number of TU55 transports

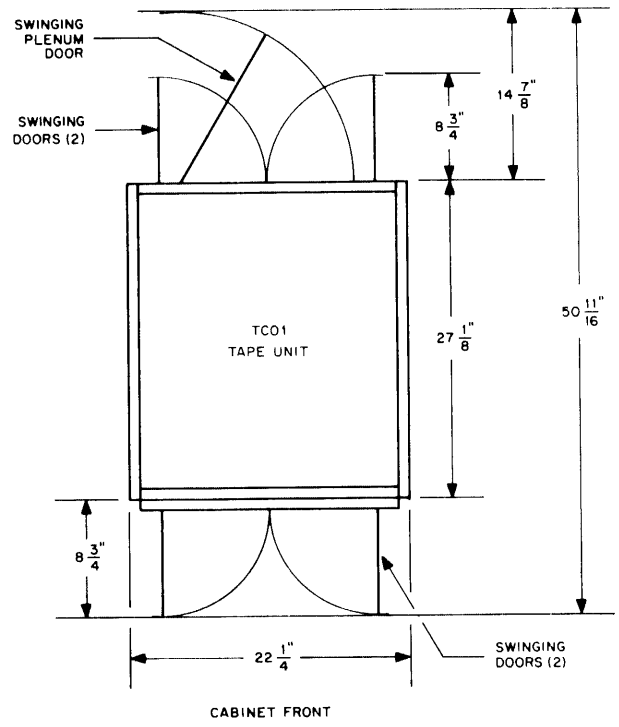


Figure 4-1 TC01 Unit Single Cabinet Installation Dimensions

included in the system. The maximum current requirement for the TC01 control is 4A, and each transport requires approximately 2A maximum. A Hubble, 3-terminal, 220V twist-lock flush receptical rated at 30A with ground neutral should be installed near the site of the cabinet to allow connection to the power cable supplied.

Figure 4-2 shows the internal and external cable interconnections as viewed from the rear of the cabinet. All other interconnections between TC01 panel assemblies are facilitated by the panel wiring which is exposed to the front of the cabinet.

Panel locations DTA01 through DTA11 are connected by panel wiring to panel locations DTF01 through DTF11. This allows the interconnecting cables to the PDP-8 processor to be attached to the bottom of the TC01 unit and the cables to additional peripheral units to be connected to the DTA locations.

4.1.4 DECtape Signal Connectors

The following cable connectors are used to interface the TC01 control to the TU55 transport and PDP-8 processor. A description of the cable connectors are listed in the Digital Logic Handbook C-105.

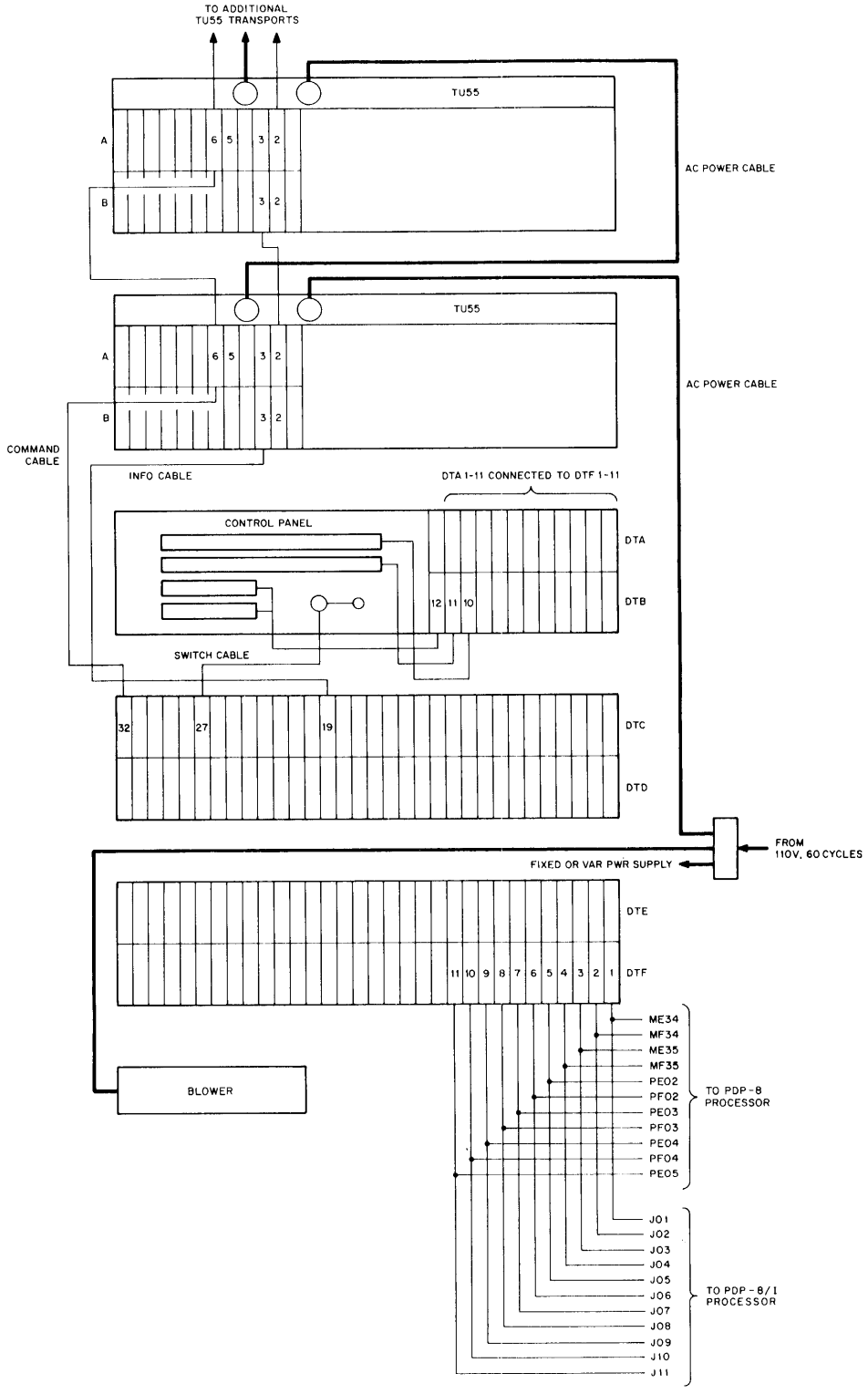


Figure 4-2 TC01 Control, Cable Diagram

a. Connector W021 - 16 pin card connector to interface the PDP-8 and TC01 control.

b. Connector W023 - 18 pin card connector which provides signals to the maintenance control panel and to the TU55 transport.

c. Connector W032 - 32 pin double card connector which provides analog read/write signals to and from the heads of the TU55 transport.

CHAPTER 5
MAINTENANCE

The information contained in the following paragraphs is required for servicing the TC01 DECtape control. Information pertaining to the TU55 transport is contained in the TU55 DECtape Instruction Manual listed in Paragraph 1.3.

The maintenance procedures contain a description of the switches and indicators on the maintenance control panel and general preventive maintenance instructions. When used in conjunction with the PDP-8 operating program and the TC01 maintenance programs, the control panel provides a visual indication of the operating state and content of the TC01 control.

5.1 MAINTENANCE EQUIPMENT

Table 5-1 is a list of the equipment recommended for servicing the TC01 control in addition to the standard hand tools normally required.

Table 5-1
Maintenance Equipment

Equipment	Manufacturer	Model
Multimeter	Triplett or Simpson	630-MA or 260
Oscilloscope	Tektronix	Series 540 or 580, with Type CA differential amplifier
Head Cleaner kit (8705)	Potter	P/N A 425 484
Variable Power supply	DEC	730 or 765
Module extender*	DEC	1954

*Furnished with the PDP-8 Processor

5.2 MAINTENANCE CONTROL PANEL

The maintenance control panel on the DTA/DTB mounting panel is located at the cabinet front, behind the access doors. The panel contains a switch used in the operation of the TC01 and indicators which display the status and information in the control.

Table 5-2 lists the function and panel designation of the switch and indicators shown on Figure 5-1. The number of indicators for each designation is enclosed in parenthesis in Table 4-2.

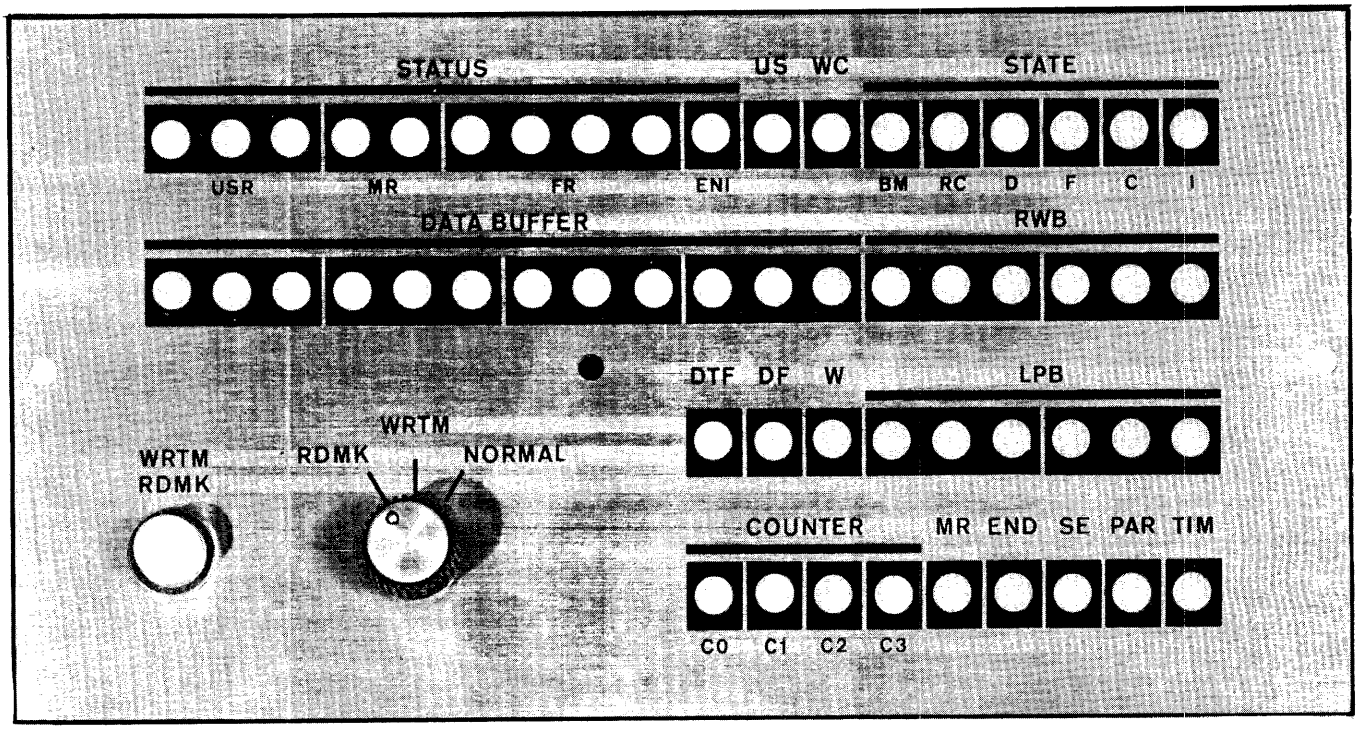


Figure 5-1 Maintenance Control Panels (Switch and Indicators)

Table 5-2
Switch and Indicators
(Maintenance Control Panel)

Designation	Function
STATUS (Indicators)	
USR (3)	Indicates the contents of the unit select register.
MR (2)	Indicates the status of the motion control registers which selects; stop, go, forward, reverse.
FR (4)	Indicates the contents of the function register.
	FR (0) Normal/Continuous Mode.
	FR (1-3) Octal code of the selected function.
ENI (1)	Lights to indicate that the TC01 is enabled to the PDP-8 program interrupt.
US (1)	Lights to indicate that the selected TU55 transport has reached the required speed for reading or writing.
WC (1)	Lights to indicate a word count overflow has not yet occurred.
MR (Indicator)	
(1)	Lights to indicate that a mark-track error has been detected.
END (Indicator)	
(1)	Lights to indicate that the end of tape has been detected.
SE (Indicator)	
(1)	Lights to indicate that a function select error, or no transport selected, or more than one transport selected.
PAR (Indicator)	
(1)	Lights to indicate that a parity error has been detected.
TIM (Indicator)	
(1)	Lights to indicate a program timing fault.
STATE (Indicators)	
BM (1)	Lights to indicate that the Block Mark state is activated.
RC (1)	Lights to indicate that the Reverse Check state is activated.
D (1)	Lights to indicate that the Data State is activated.
F (1)	Lights to indicate that the Final State is activated.
C (1)	Lights to indicate that the Check State is activated.
I (1)	Lights to indicate that the Idle State is activated.

Table 5-2 (Cont)
Switch and Indicators
(Maintenance Control Panel)

Designation	Function
DATA BUFFER (Indicators) (0-2)(3-5)(6-8)(9-11)	Indicates the content of the data buffer register.
RWB (Indicators) (0-2)(3-5)	Indicates the content of the read/write buffer register.
DTF (Indicator) (1)	Lights to indicate that the DECtape flag is set.
DF (Indicator) (1)	Lights to indicate that a data flag is set requesting a data break.
W (Indicator) (1)	Lights to indicate that the write enable level is activated.
LPB (Indicators) (0-2)(3-5)	Indicates the content of the longitudinal parity buffer.
COUNTER (Indicators) C0, C1, C3	Provides indication of the 6-count function of the counter register used for mark-track decoding.
C2, C3	Provides an indication of the 4-count function of the counter register used for assembling data words.

5.3 DEC MODULES

The standard DEC modules used on the TC01 control are described in Digital Logic Handbook C-105 except for modules G882, G008, and G009, which are described in the following paragraphs. One spare module of each type is generally recommended to facilitate maintenance of the TC01 control.

5.3.1 Module Locations and Complement

The position of the modules within the mounting panels, as viewed from the wiring side, is shown in Drawing D-MU-TC01-9 (sheets 1 and 2)of Chapter 6. In this drawing, each module is represented by a rectangle with the module type designation at the top. Each rectangle in turn is subdivided to show the circuits that are contained on the module. In general, the circuits are identified by the logic signal(s) available at the circuit outputs.

Table 5-3 lists the type and quantity of modules used in the TC01 and references the figure number of the module schematic diagrams (Figures 5-5 through 5-24).

5.3.2 Circuit Descriptions

The following circuit descriptions are provided to supplement the information in the Digital Logic Handbook C-105.

a. MANCHESTER READER/WRITER G882

The Manchester Reader/Writer G882 is a standard size FLIP CHIP module for use in reading and writing one channel of DECtape Type 55 Microtape. Each module contains two write amplifiers and one high-gain differential read amplifier. The read amplifier saturates with a 1 mV input.

b. MASTER SLICE CONTROL, G008, and Sense Amplifier G009

The Master Slice Control, G008, is a standard size FLIP CHIP module which supplies slice and clamp voltages for the 2-input Sense Amplifier G009. The schematic diagram for the G008 and G009 modules are shown on Figures 5-2 and 5-3, respectively.

Terminal connections between modules G008 and G009 are as follows.

Voltage	G008 Terminals	G009 Terminals
1st stage clamp	M, B	K, B
2nd stage clamp	N, B	N, B
slice	H, A	S, D

Each voltage circuit contains a zener diode network with silicon diodes for temperature compensation. Emitter follower stages provide current drawing capability and low impedance outputs. The first stage clamp voltage is fixed while the second stage clamp voltage and the slice voltage are adjustable.

The output characteristics are as follows.

1st Stage Clamp M,B is fixed at +3.9V with respect to -15V.
2nd Stage Clamp N,B is variable from +0.6 to +11.3V with respect to -15V.
Slice Level H,A is variable from 0 to -11.6V with respect to +10V.

The power requirements of the module are -15V/45 ma; +10V(A)/0 ma; and +10V (B)/70 ma.

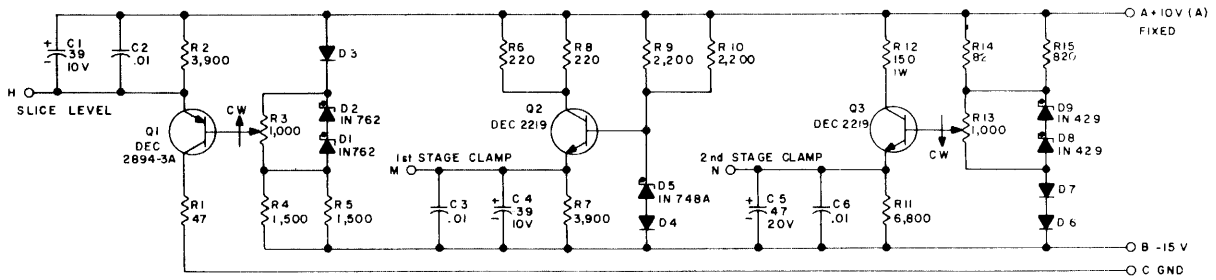


Figure 5-2 Master Slice Control, G008

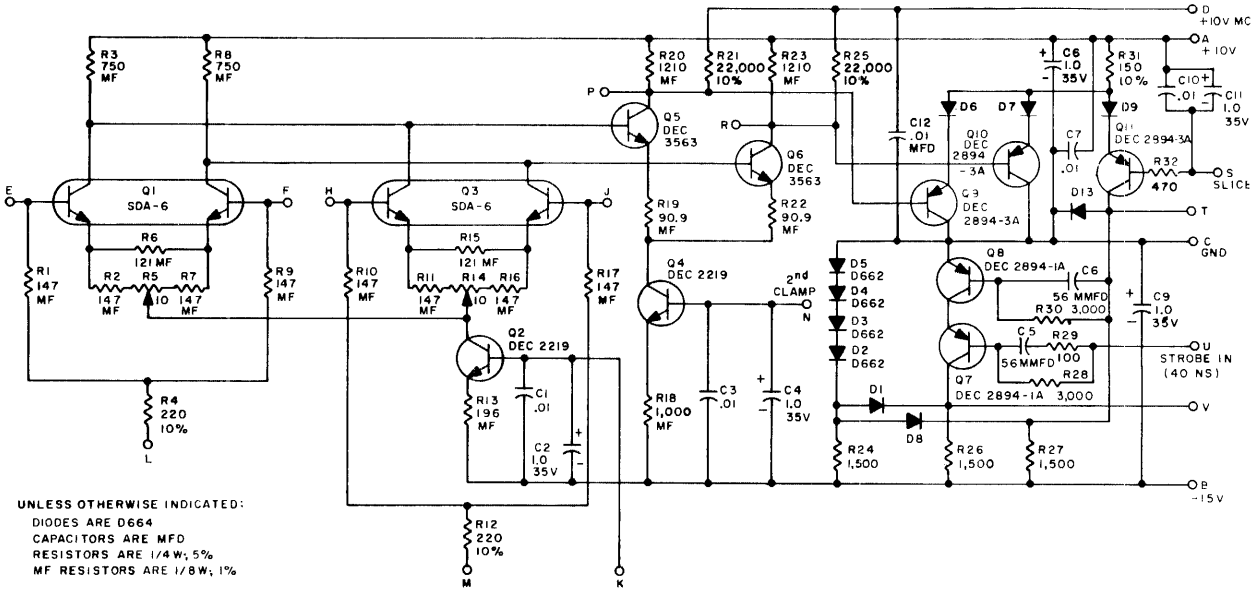


Figure 5-3 Sense Amplifier, G009

Table 5-3
TC01 Module Complement

Number Required	Type	Description	Figure
1	G008	Master Slice Control	5-2
1	G009	Sense Amplifier	5-3
5	G882	Manchester Reader/Writer	5-4
11	R002	Diode Network	5-5
9	S107	Inverter	5-6
9	S111	Diode Gate	5-7
4	R113	Diode Gate	5-8
7	R123	Diode Gate	5-9
1	R141	Diode Gate	5-10
2	S151	Binary-to-Octal Decoder	5-11
3	R201	Flip-Flop	5-12
20	S202	Dual Flip-Flop	5-13
4	S203	Triple Flip-Flop	5-14
8	S205	Dual Flip-Flop	5-15
1	R302	Delay (One Shot)	5-16
2	R303	Integrating (One Shot)	5-17
1	R401	Variable Clock	5-18
4	S602	Pulse Amplifier	5-19
7	S603	Pulse Amplifier	5-20
1	W005	Clamped Load	5-21
8	W050	30 MA Indicator Driver	5-22
2	W103	Device Selector	5-23
1	W520	Comparator	5-24

Module Characteristics

The terminals for the module are shown in Figure 5-4. The input and output characteristics are as follows.

Reader Inputs E, D - are differential signals centered at ground. The input impedance is approximately 400 ohms to ground. A nominal input signal is a sine wave between 5 kc and 30 kc.

Reader Outputs U, V - are standard DEC levels of -3V and ground. The outputs can drive 10 ma of load at ground.

Writer Inputs - N, R, and P are standard DEC levels of -3V and ground. The input load of 2 ma is shared by the inputs at ground level.

Writer Outputs - J and K, are nominal 180-ma current pulses from ground to -15V.

The power requirements of the module are +10 (A)/18 ma and -15 (B)/235 ma. The marginal check limits in both cases are ±20%.

Both the reader and the writer circuits are returned to a common C, F ground.

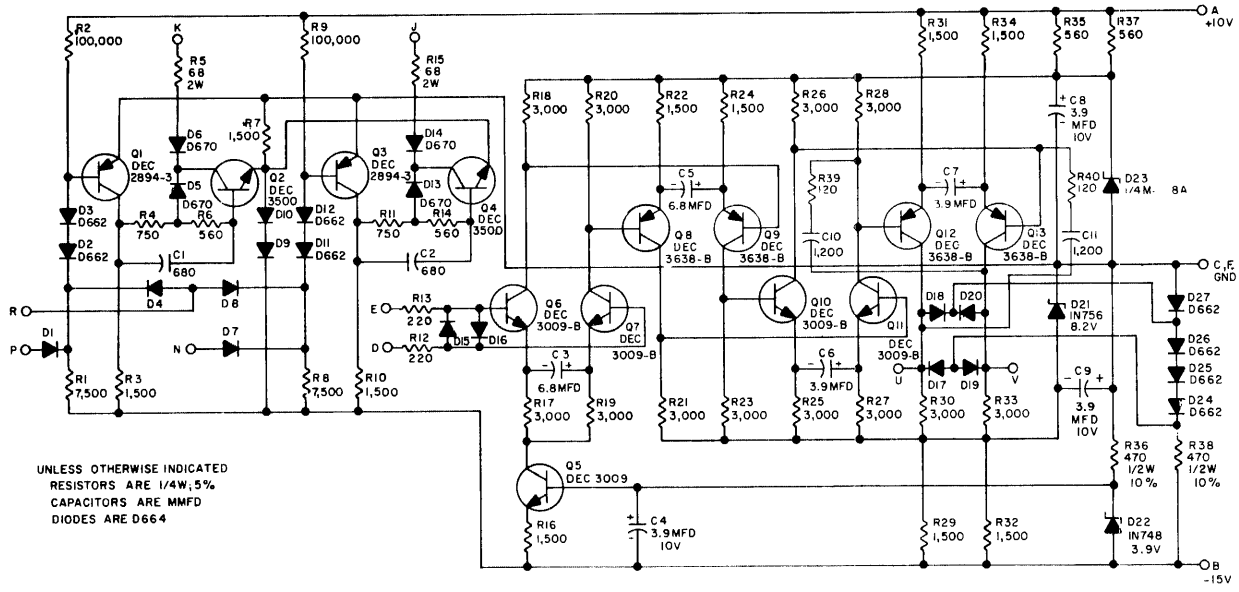


Figure 5-4 Manchester Reader/Writer, G882

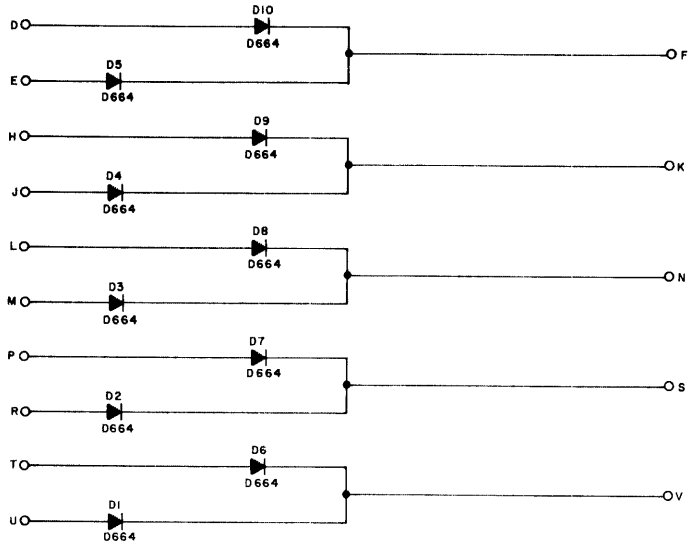


Figure 5-5 Diode Network, R002

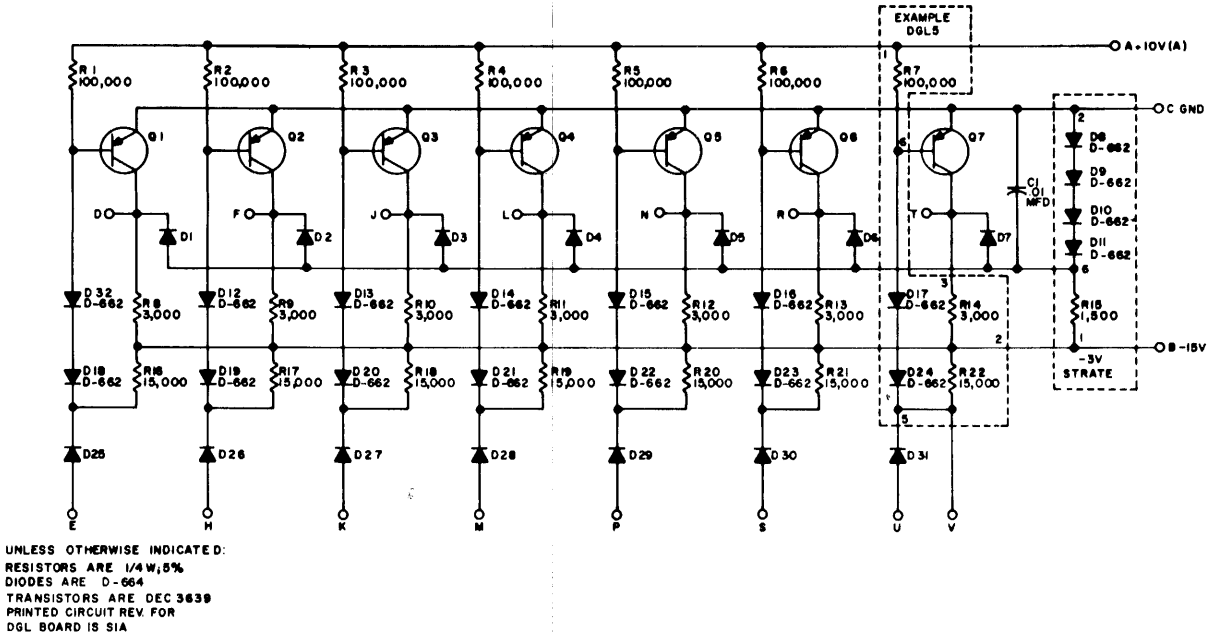


Figure 5-6 Inverter, S107

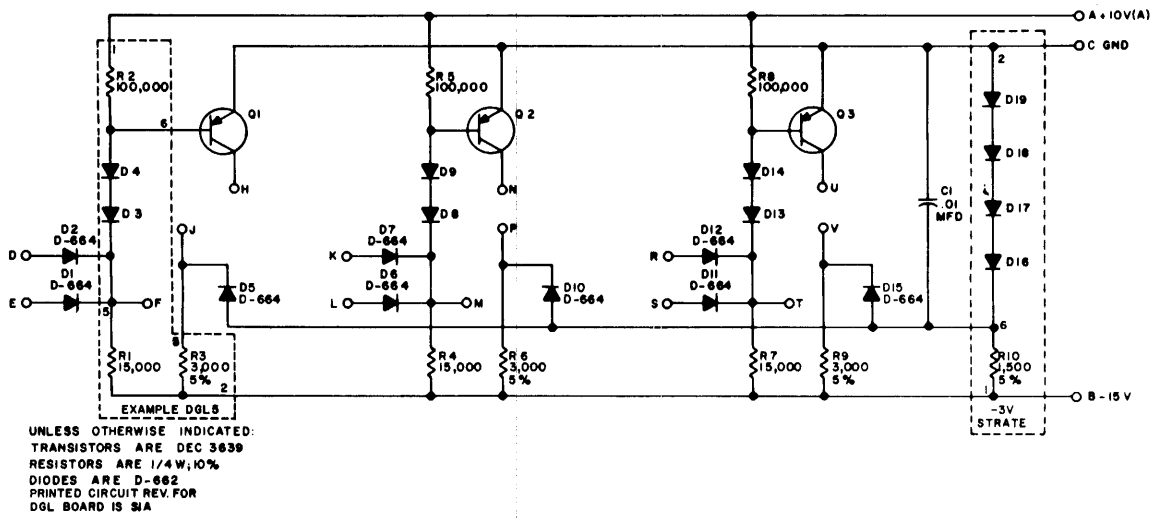
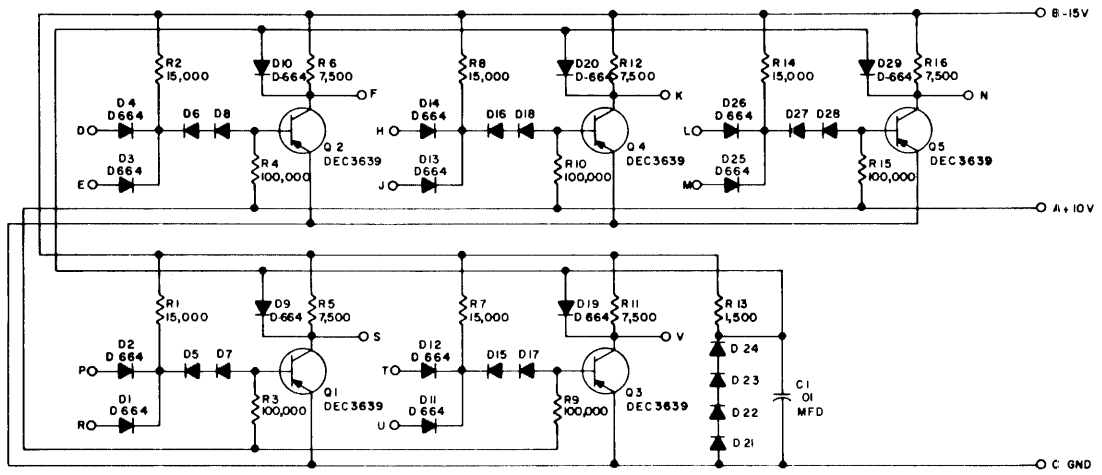
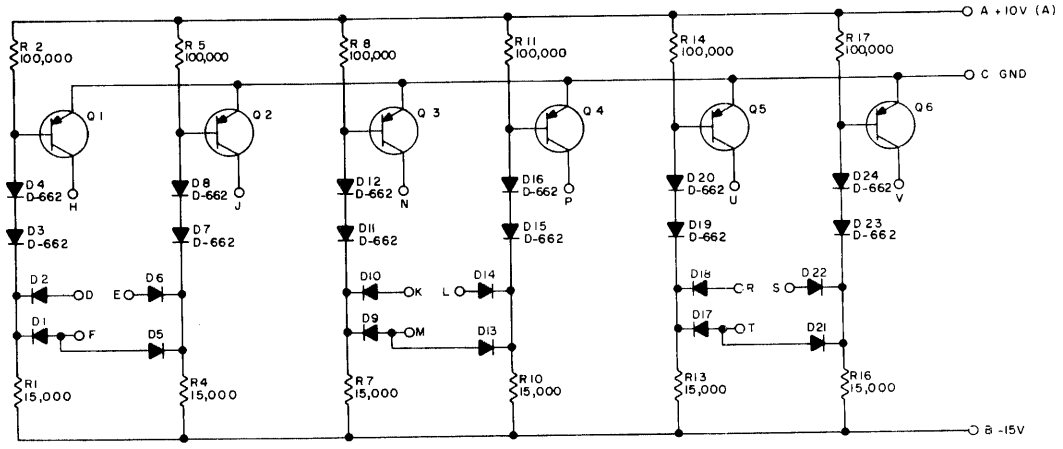


Figure 5-7 Diode Gate, S111



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
DIODES ARE D 662

Figure 5-8 Diode Gate, R113



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639-0
RESISTORS ARE 1/4 W, 5%
DIODES ARE D-664

Figure 5-9 Diode Gate, R123

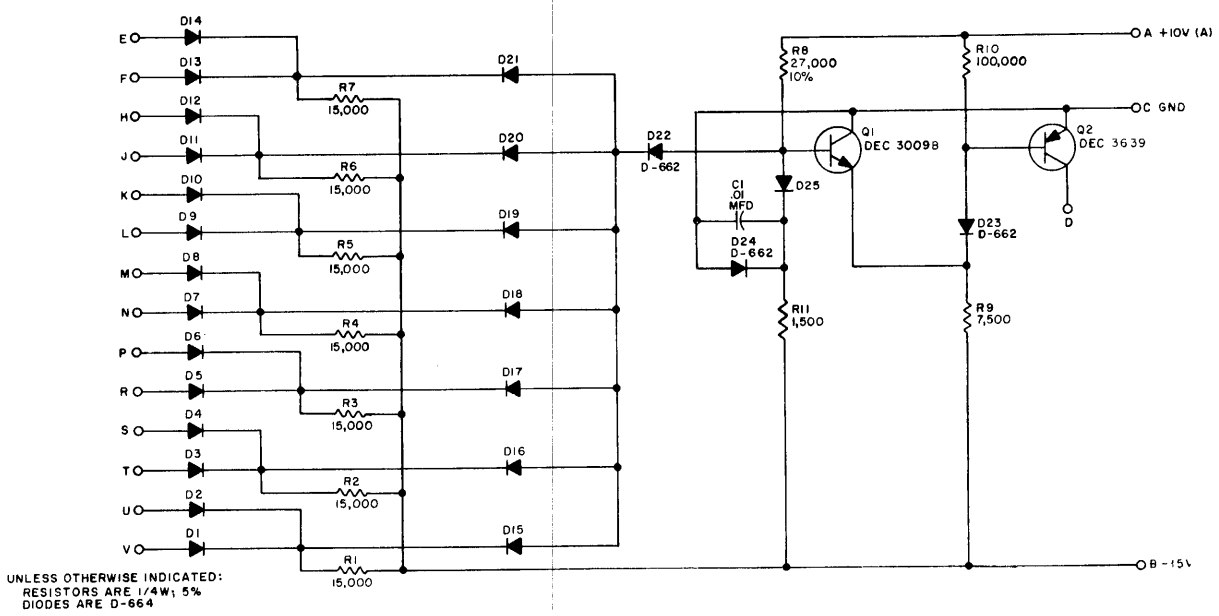


Figure 5-10 Diode Gate, R141

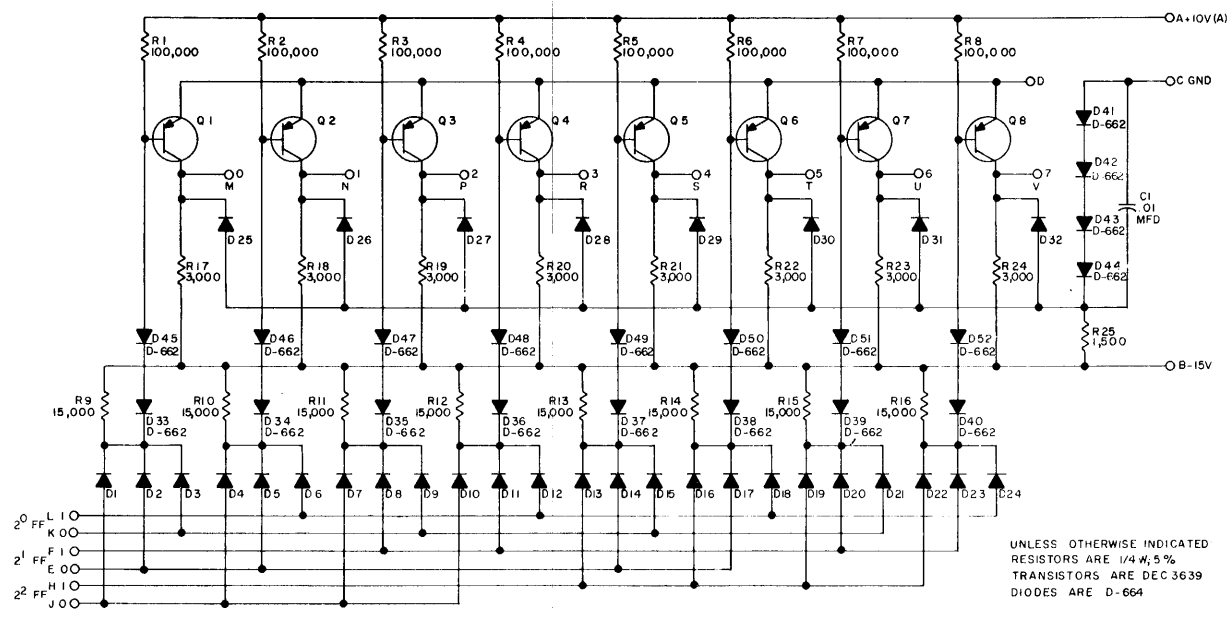


Figure 5-11 Binary-to-Octal Decoder, S151

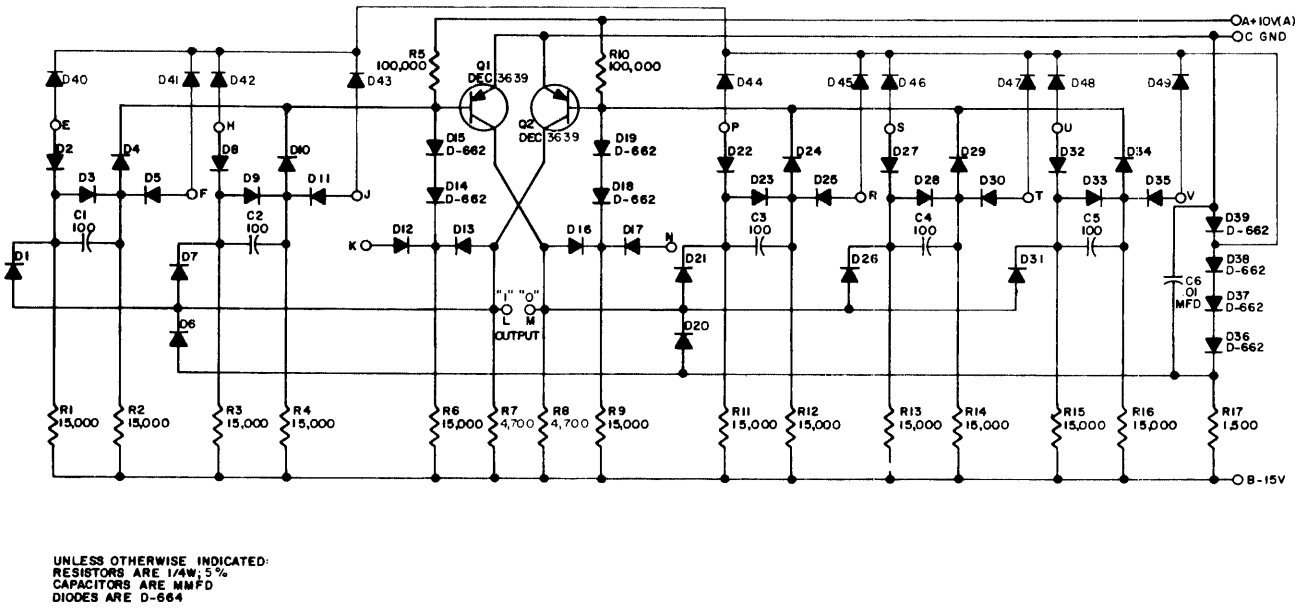


Figure 5-12 Flip-Flop, R201

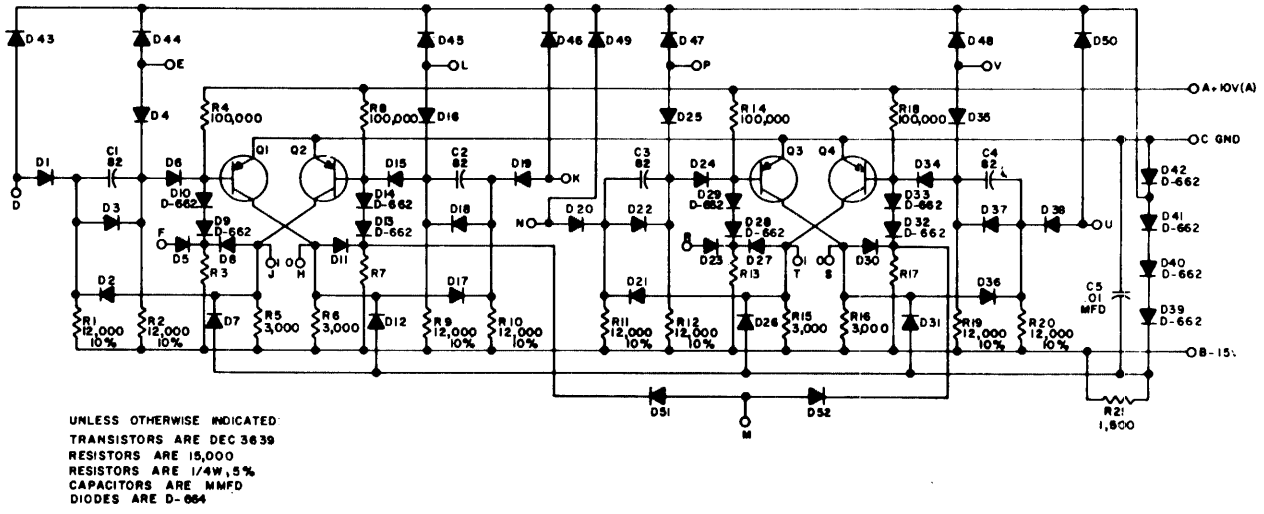


Figure 5-13 Dual Flip-Flop, S202

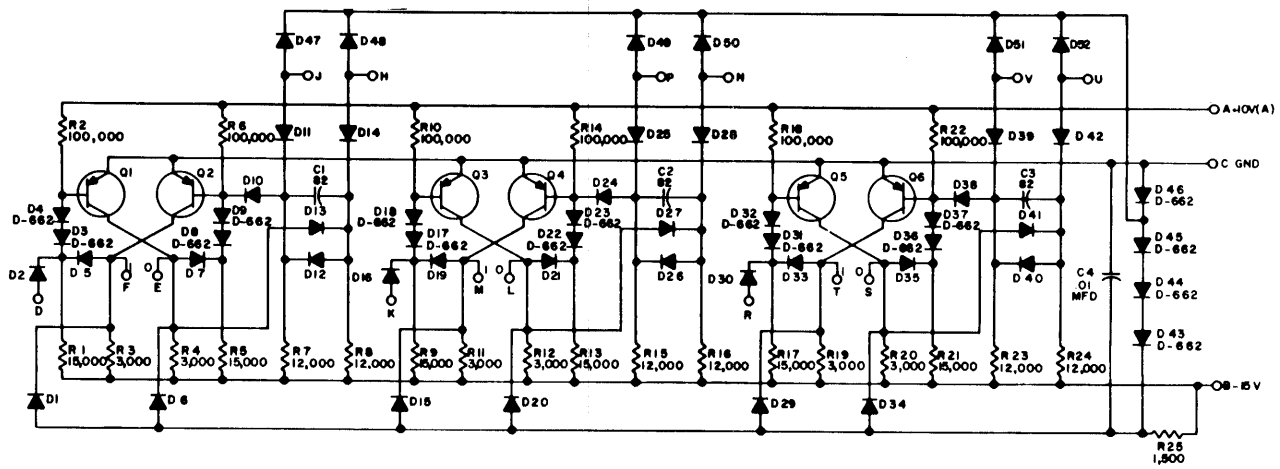


Figure 5-14 Triple Flip-Flop, S203

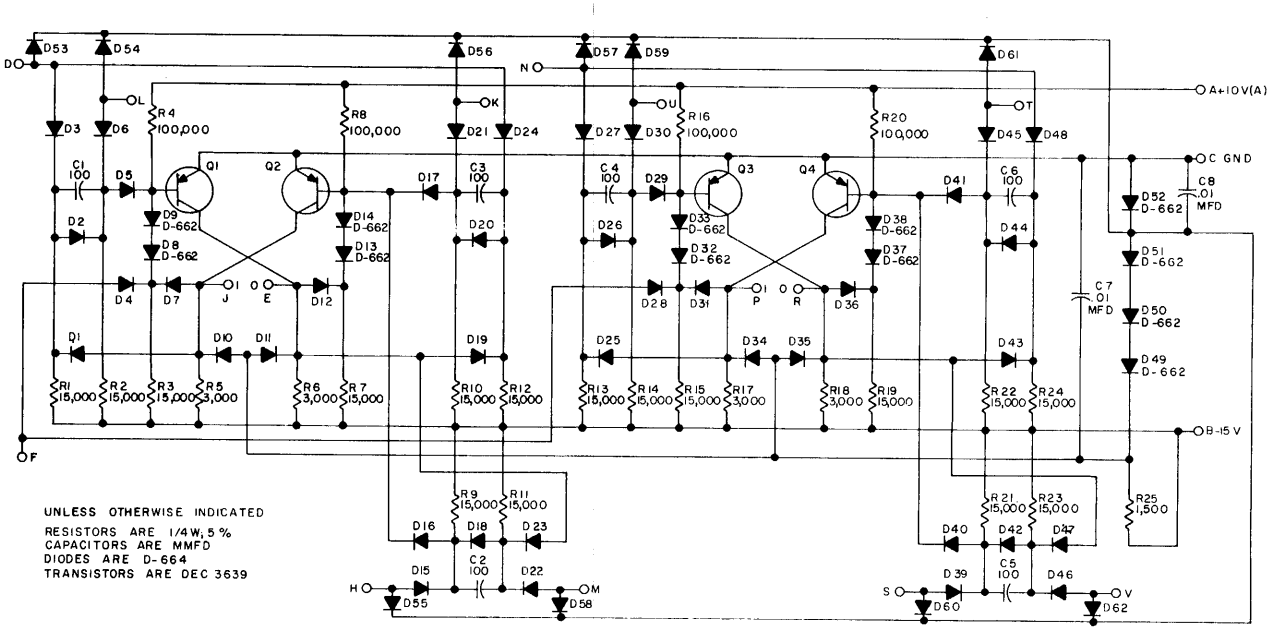
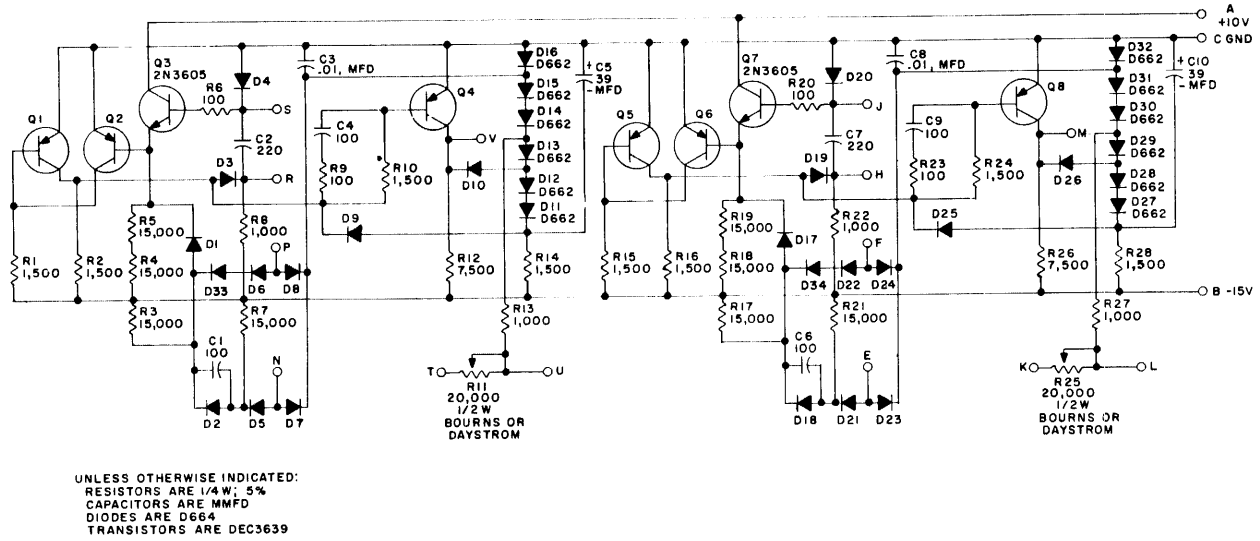
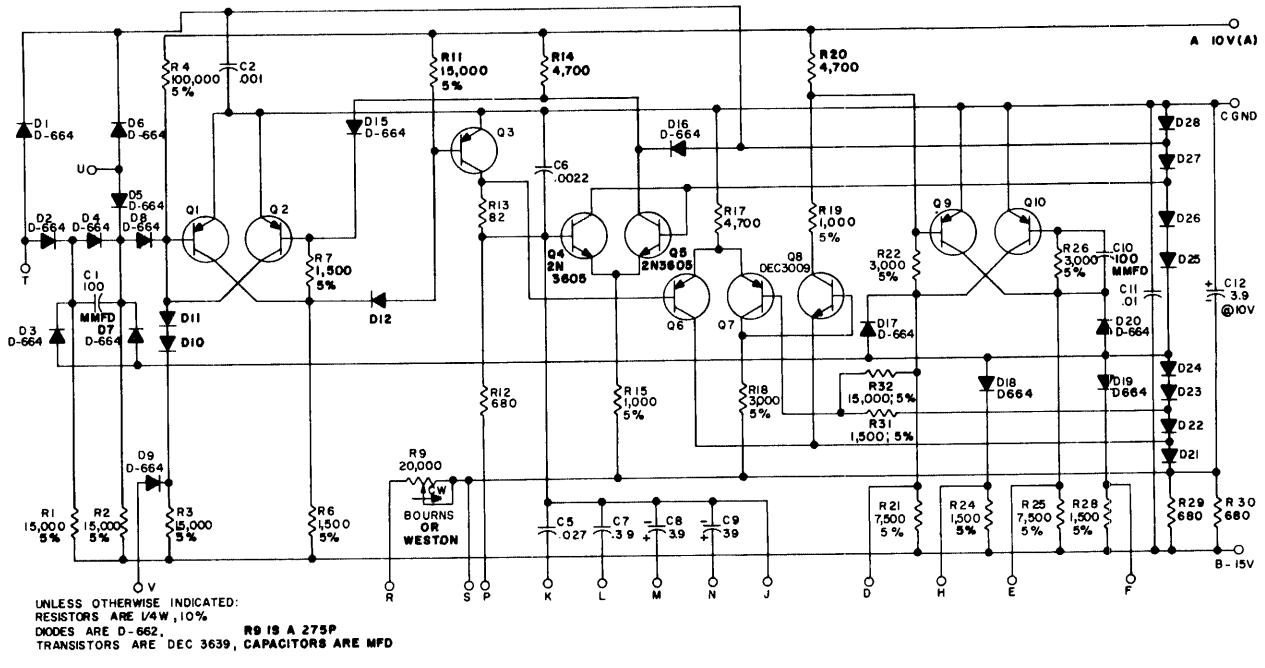


Figure 5-15 Dual Flip-Flop, S205



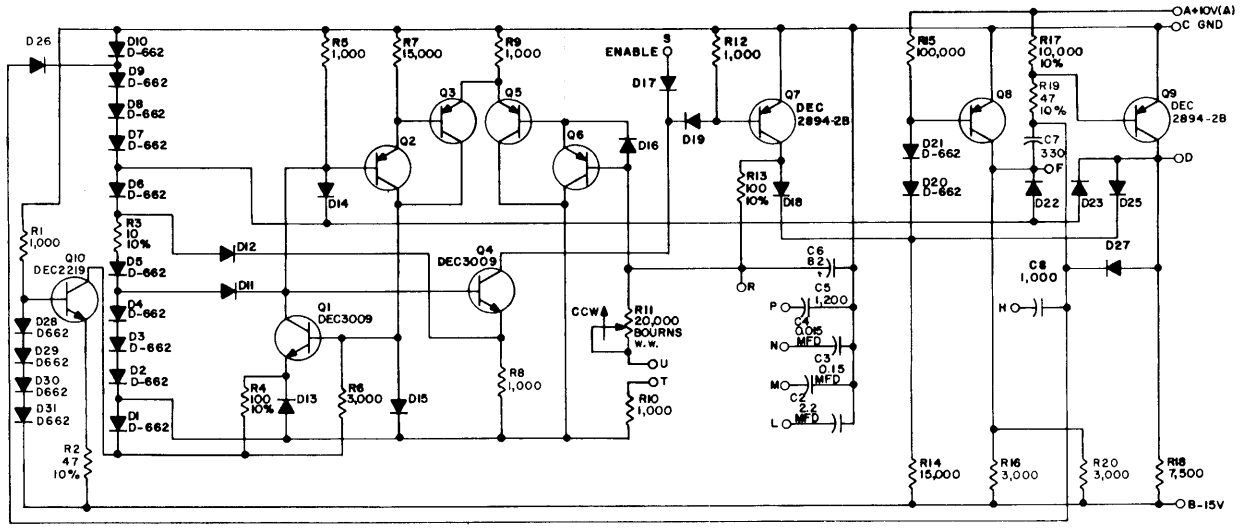
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D664
TRANSISTORS ARE DEC3639

Figure 5-16 Delay (One Shot), R302



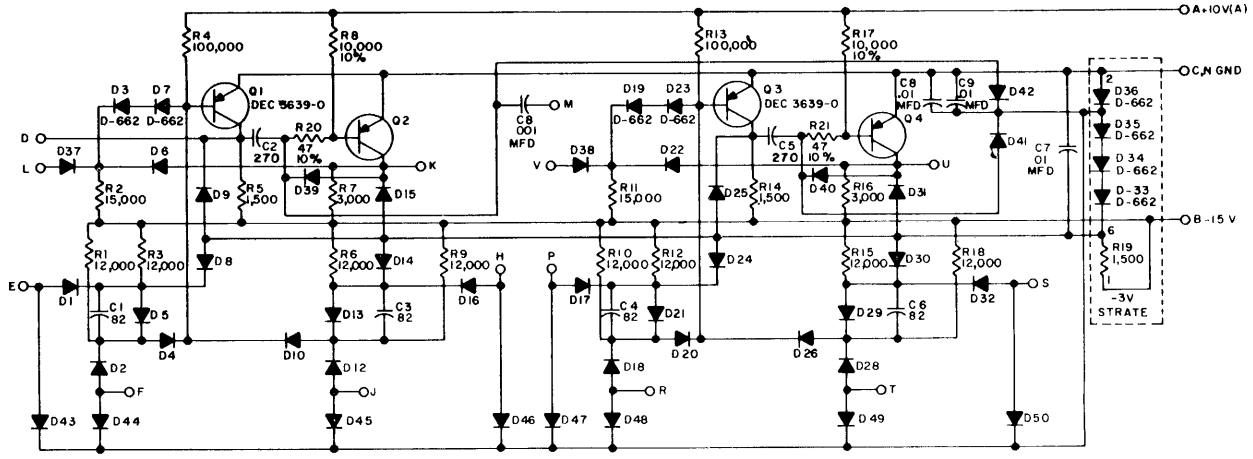
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
DIODES ARE D-662, R9 IS A 275P
TRANSISTORS ARE DEC 3639, CAPACITORS ARE MFD

Figure 5-17 Integrating (One Shot), R303



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639-0
R11 IS A #275P

Figure 5-18 Variable Clock, R401



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC2894-2B

Figure 5-19 Pulse Amplifier, S602

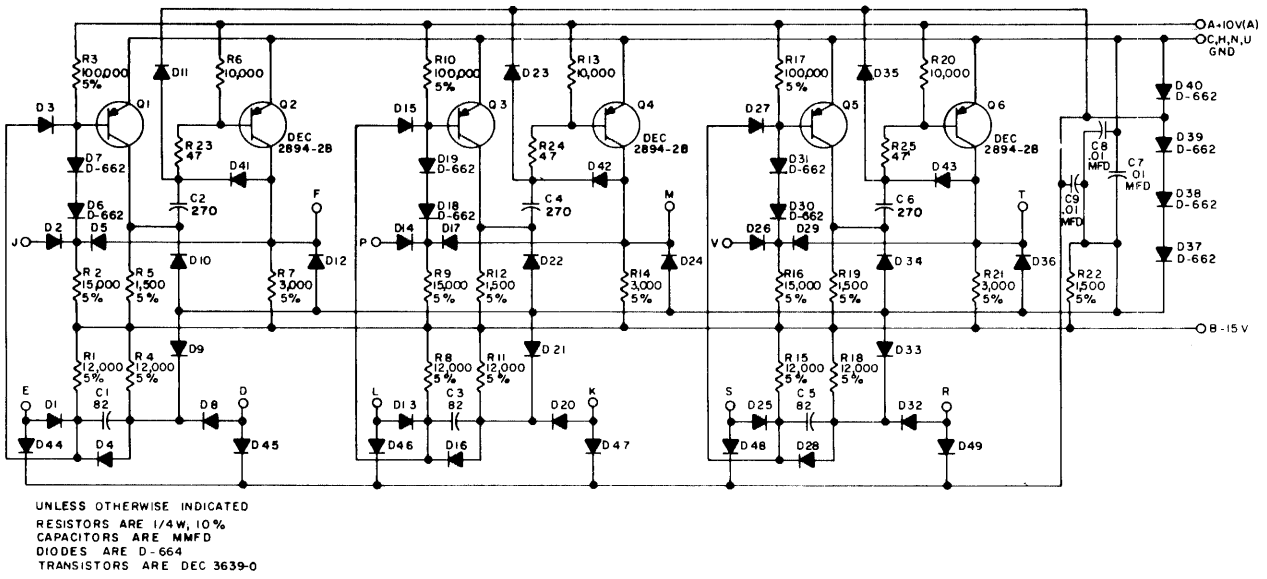


Figure 5-20 Pulse Amplifier, S603

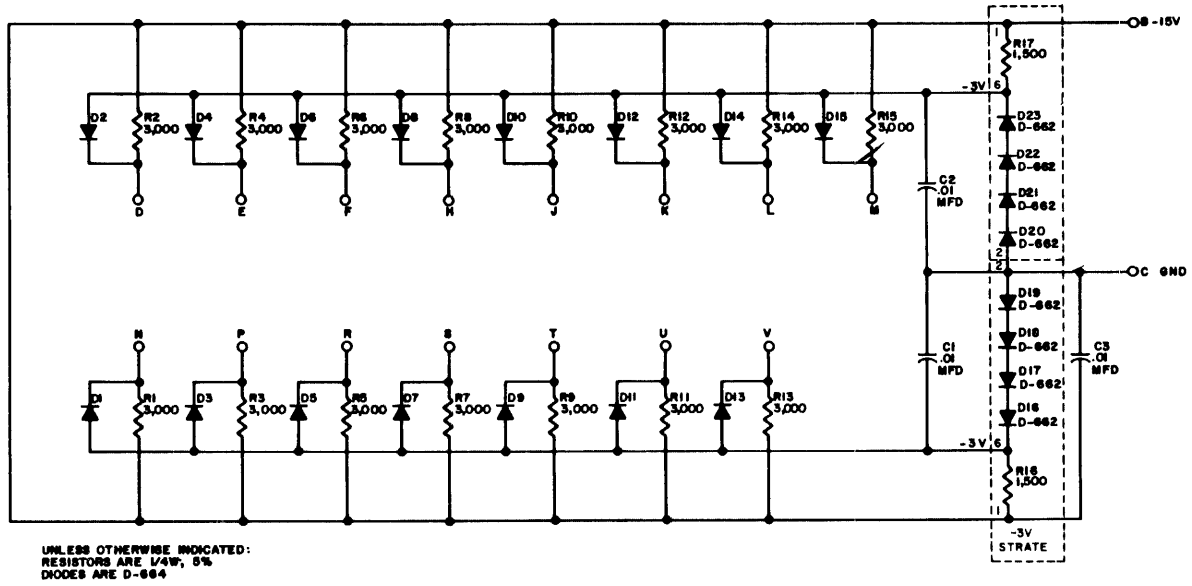
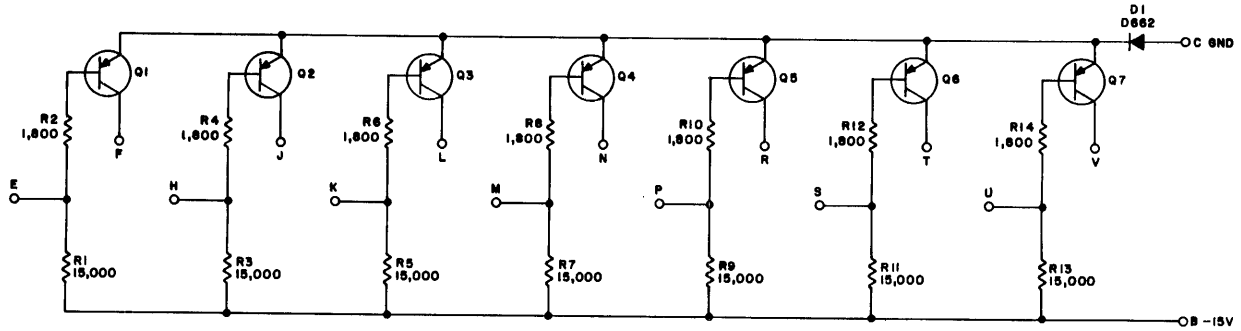
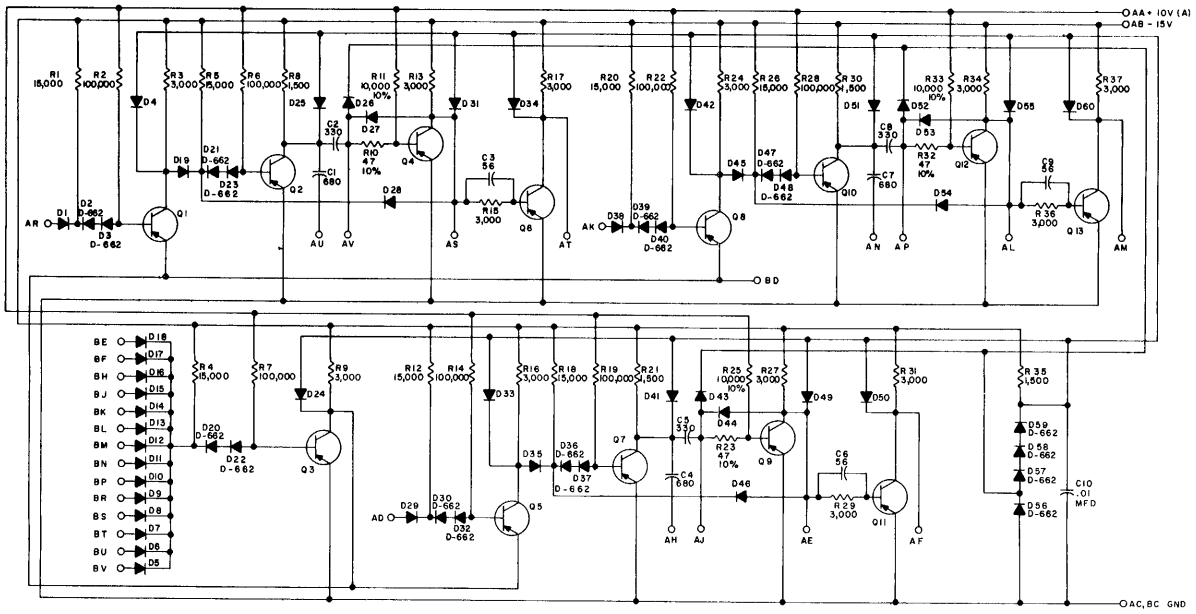


Figure 5-21 Clamped Load, W005



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
TRANSISTORS ARE DEC6534D (DEC6534B MAY BE SUBSTITUTED)

Figure 5-22 30 MA Indicator Driver, W050



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Figure 5-23 Device Selector, W103

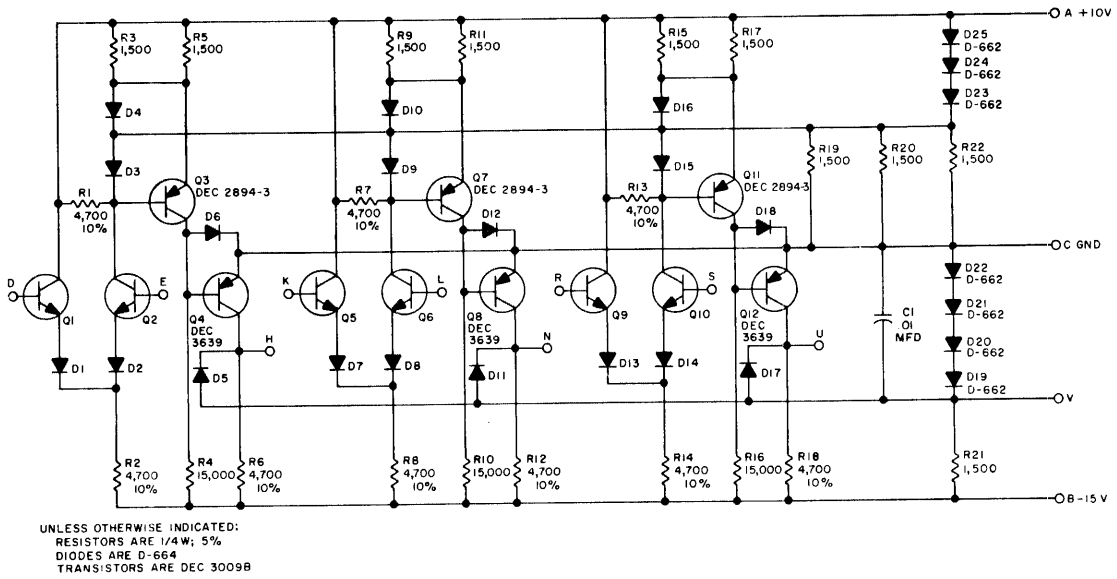


Figure 5-24 Comparator, W520

5.3.3 Module Replacement Procedure

When necessary to remove modules, the procedure is as follows.

a. Turn off all power to the Type TC01 DECtape Control.

b. Gently pull the module from the mounting panel. Use a straight even pull to avoid damage to plug connections and the printed-wiring board.

Access to adjustment controls on the module or access to signal tracing points can be gained by removing the module, connecting a Type W980 Module Extender into the mounting panel, and inserting the module into the extender.

5.4 POWER SUPPLY 779

Power Supply 779 is a dual power supply unit designed for installation on a plenum door. One of the supplies furnished +10V and -15V suitable for logic power; the other is a lightly filtered, center-tapped 30V floating supply suitable for furnishing power to solenoids, etc. The -15V outputs of the power supply are connected in parallel to supply logic power to both the TC01 and TU55 transports. The schematic diagram of this power supply is shown in Figure 5-25 and the electrical characteristics are listed in DEC System Module Handbook C-100.

Input voltages:	115 Vac, 60 c/s (105V to 125V)
Output voltages:	+10V; -15V; center-tapped 30V (+15V -15V)
Maximum output current:	8A (limited by curve)
Line load regulation: (under all line and load conditions)	+10V regulated to 9-11V; all +15V supplies regulated to 14-16V

Ripple:	1V at +10V; 500 mV at -15V; 2.5V at 30V
Size frequency regulation:	±3%
Maximum voltage between output and chassis:	300V

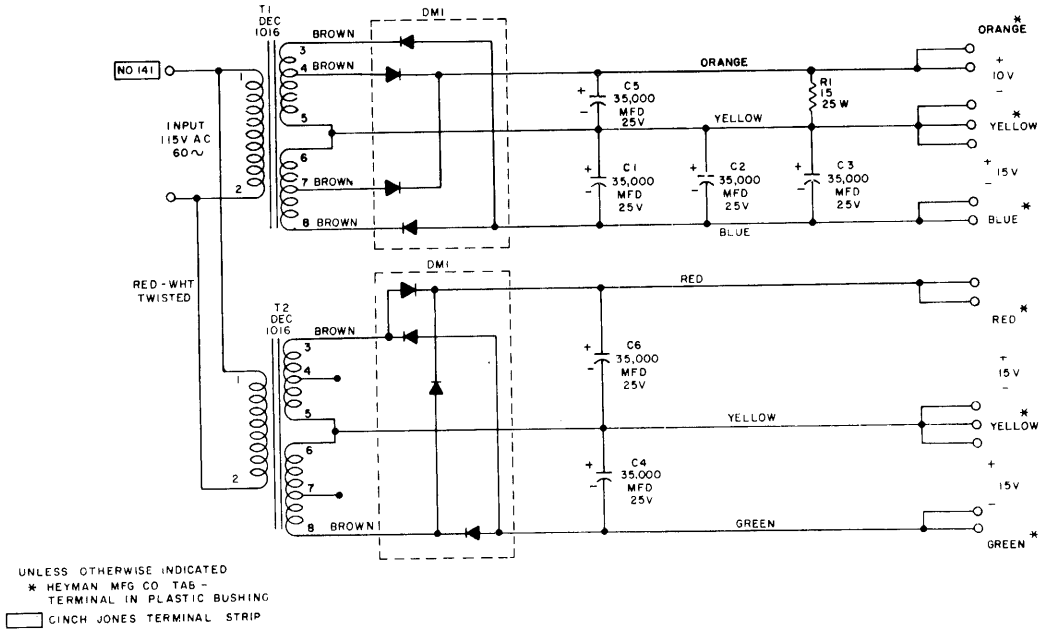


Figure 5-25 Power Supply Type 779, Schematic Diagram

5.4.1 Mechanical Characteristics

Pertinent mechanical characteristics of Power Supply 779 are as follows.

Panel width:	16-5/8 in.
Finish:	Chromate conversion, coating
Power input plug:	Jones No. 141 strip
Power output plug:	Heyman tab terminals

5.4.2 Power Supply Checks

The use of a multimeter permits output voltage measurements to be made on the Type 779 power supply without disconnecting the power supply. An oscilloscope should be used to measure the peak-to-peak ripple content of each dc output voltage. Because the power supply is not adjustable, a unit that does not meet the following tolerances should be considered defective and steps should be taken to correct the deficiency!

Nominal Voltage Outputs (volts)	Output Voltage Range (volts)	Maximum Peak-to-Peak Output Ripple Voltage (volts)
+10	9-11	1
-15	14-16	0.5

±15 (for center tapped 30V circuit)

5.4.3 Marginal Checks

Marginal checks are performed to aggravate borderline circuit conditions within the control logic and thus produce observable faults. By recording the bias voltage levels at which circuits fail, progressive deterioration can be plotted and expected failure dates can be predicted. This procedure provides a means for planned replacement. Marginal checks are also useful as a troubleshooting aid to locate marginal or intermittent components (e.g., deteriorating transistors).

Marginal checks are performed by operating the logic circuits from an adjustable external power supply located in the PDP-8 or a DEC Type 734B Dual Variable Power Supply. PDP-8/I supply is not varied for marginal checks; marginal checks however, can be made with an external supply. Raising the bias level above +10V increases the transistor cutoff required to be overcome by the preceding transistor, thus causing a below-par transistor to fail. Lowering the bias level below +10V reduces the transistor base bias and noise rejection. This procedure provides detection of high-leakage transistors and simulates high-temperature conditions for checking thermal runaway. Raising and lowering the -15V supply has little effect on the logic circuits because the collector load voltage of most modules is clamped at -3V. It does, however, increase and decrease the output pulse amplitude of the pulse amplifier circuits (e.g., the delay circuits) and then provides a sensitivity check of the circuits which follow.

CAUTION

Increasing the -15V power to a value more negative than -18V will cause damage within the logic circuits.

The panel for conducting marginal checks of the Type TC01 DECtape Control is located at the left-hand side of the wired panel assembly. When switched on (up), switches 1A through 1F apply power from the marginal check bus; when switched off (down), normal power is applied. The "up" position of the top switch on each panel selects the marginal check voltage of +10V. The "down" position selects the fixed voltage of +10V. The lower switch of each panel performs the same function with the -15V.

A color-coded connector on the right side of each panel connects the normal and marginal operating voltages to the marginal check panel. The normal and marginal power buses are common to all panels. The normal power bus is connected to the Type 779 Power Supply, the marginal power bus to the marginal check power supply on the PDP-8.

A marginal check is performed as follows.

a. Set selector switch on marginal-check power supply to +10 Mc and adjust the power supply output for +10V.

b. Start DECtape operation in a normal program or in a routine which fully utilizes the circuits in the rack to be tested. If no suitable program is available in the normal system application, select an appropriate maintenance routine. The maintenance programs provide basic exercises of specific functions and scope loops for these functions as well as a routine which redundantly exercises all functions.

c. Set the top normal/marginal check switch on the panel to be tested to its "up" position.

d. Decrease the marginal-check power supply output voltage until normal system operation is interrupted. Record the marginal-check voltage. If desired, locate and replace the marginal transistors at this time.

e. Restart DECtape operation and increase the marginal-check power supply output voltage until normal operation is interrupted. Record the marginal-check voltage. If desired, locate and replace the marginal transistors at this time.

f. Set the top normal/marginal check switch in step c to its "down" position.

g. Repeat steps a through f for the center normal/marginal switch on the panel being tested.

h. Set selector switch on the marginal-check power supply to -15 mc and adjust the power supply output for -15V.

i. Repeat step b.

j. Set the bottom normal/marginal switch on the panel being tested to its "up" position.

k. Repeat steps d and e and then return the bottom normal/marginal switch to its "down" position.

l. Adjust the output of the marginal-check power supply to 0V and set the selector switch to its "off" position.

5.5 POWER CONTROL PANEL (Type 834)

The Power Control Panel is mounted on the plenum door at the rear of the cabinet and is used in conjunction with the Type 779 Power Supply. The schematic diagram of the panel is shown on Figure 5-26.

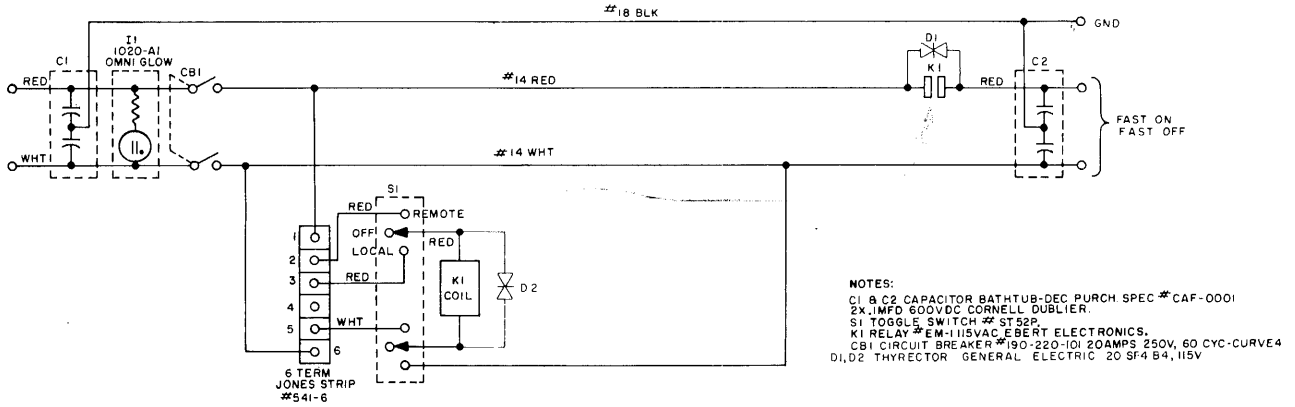


Figure 5-26 Power Control Panel Type 834

5.6 PREVENTIVE MAINTENANCE

Preventive maintenance consists of procedures performed prior to the initial operation of the equipment and periodically during its operating life. These procedures include visual inspections, cleaning, mechanical checks, and circuit element checks. Marginal checks are also conducted when considered necessary to aggravate border-line conditions or intermittent failures so that they can be detected and corrected. A log book should be available for recording specific data which indicates the rate of performance deterioration and provides information for determining when components should be replaced.

Except for marginal checks all preventive maintenance procedures should be performed once a month or every 200 operating hours, whichever occurs first.

5.6.1 Mechanical Checks

The following mechanical checks should reveal any substandard conditions in the mechanical operation of the control unit.

a. Clean the exterior and the interior of the control by means of a vacuum cleaner or by using clean cloths moistened in a nonflammable solvent.

b. Clean the air filter at the bottom of each cabinet. Remove the filter by removing the fan and housing which are held in place by two knurled and slotted screws. Wash the filter in soapy water, dry in an oven or by spraying with compressed gas, and spray with Filter-kote (Research Products Corp., 1015 E. Washington Ave., Wisconsin, 53703).

c. Clean all rotary switches with a spray cleaner such as Contactene.

d. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

e. Visually inspect the TC01 for completeness and general condition.

f. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Repair or replace any defective wiring.

g. Inspect switches, controls, knobs, jacks, connectors, transformers, fans, capacitors, lamp assemblies, etc. Tighten or replace as required.

h. Inspect switches for binding, scraping, misalignment, and positive action. Adjust, align, or replace as necessary.

i. Inspect all racks of logic to assure that each module is securely seated in its connector.

j. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors exhibiting these signs of malfunction.

CHAPTER 6
ENGINEERING DRAWINGS

This chapter contains the logic block diagrams and module location diagrams of the TC01 DECtape Control. The equivalent drawings for the TU55 DECtape transport are contained within the TU55 Instruction Manual.

6.1 SYMBOLS AND DESIGNATIONS

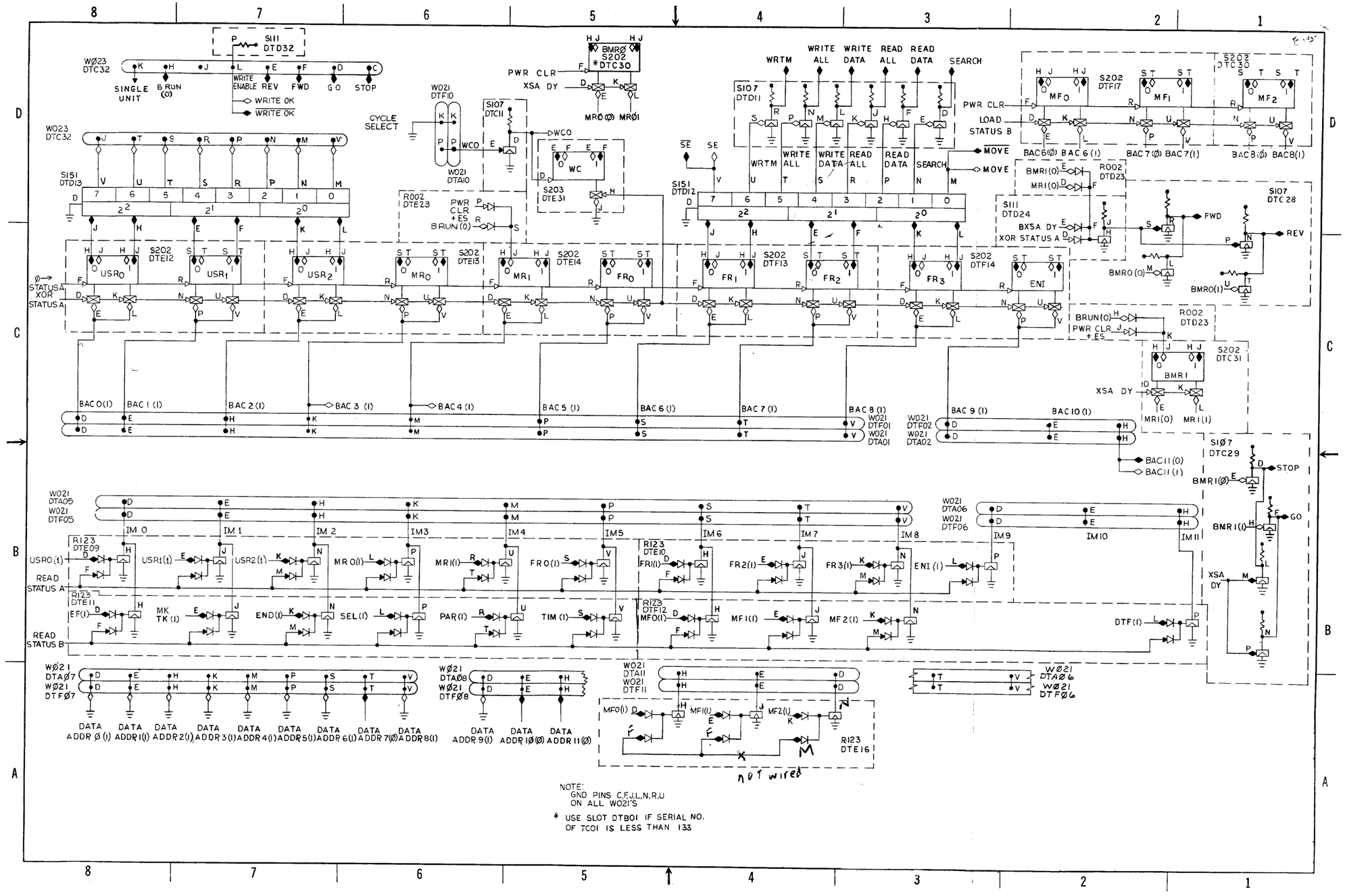
The block and signal symbols used on the logic diagrams are defined in Chapter 10 of the PDP-8 Maintenance Manual together with a description of standard DEC logic levels. The signal designations assigned are defined in Table 2-6 of this manual.

6.2 Drawing List

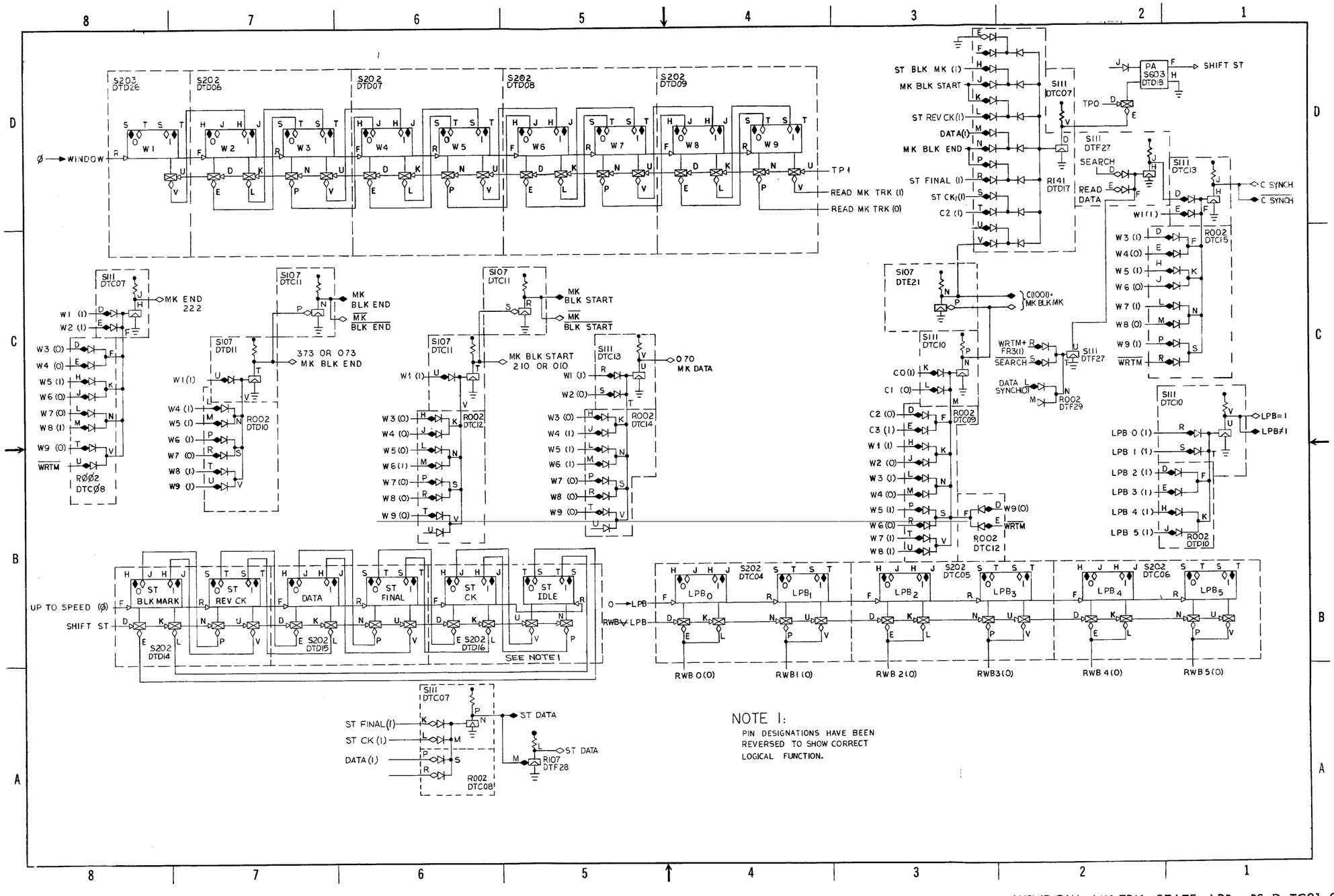
Table 6-1 lists the pertinent engineering drawings referenced in this manual. These drawings relate to the discussions in this manual and do not necessarily reflect the latest revisions incorporated in the equipment. When discrepancies exist between the drawings contained in this manual and the drawings shipped with the device, the latter should be assumed to be the correct drawing set.

Table 6-1
Engineering Drawing List

Number	Revision	Title
BS-D-TC01-0-2	E	MF, USR, MR, FR
BS-D-TC01-0-3	B	WINDOW, MD TRK, STATE, LPB
BS-D-TC01-0-4	C	Error Flags
BS-D-TC01-0-5	D	Control
BS-D-TC01-0-6	E	TP GEN TT GEN
MU-D-TC01-0-9 (Sheet 1)	F	Utilization Module List
MU-D-TC01-0-9 (Sheet 2)	F	Utilization Module List
BS-D-TC01-0-12		Panel Indicator Drivers
BS-D-TC01-0-13		Maintenance Control Panel
BS-D-TC01-0-14	E	Error Flags
BS-D-TC01-0-15	E	R/W AMPS, SP GEN, TEST CONN.

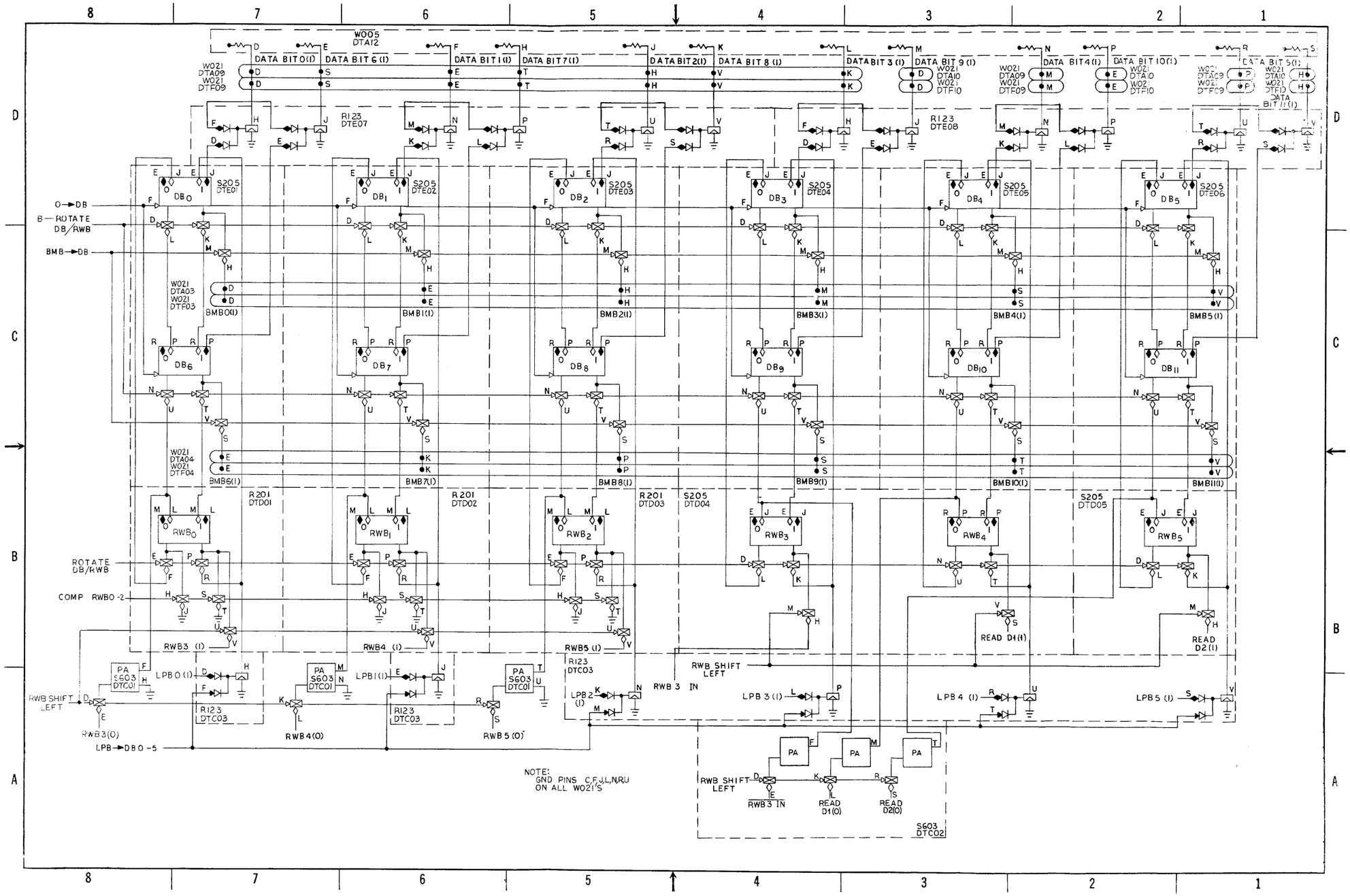


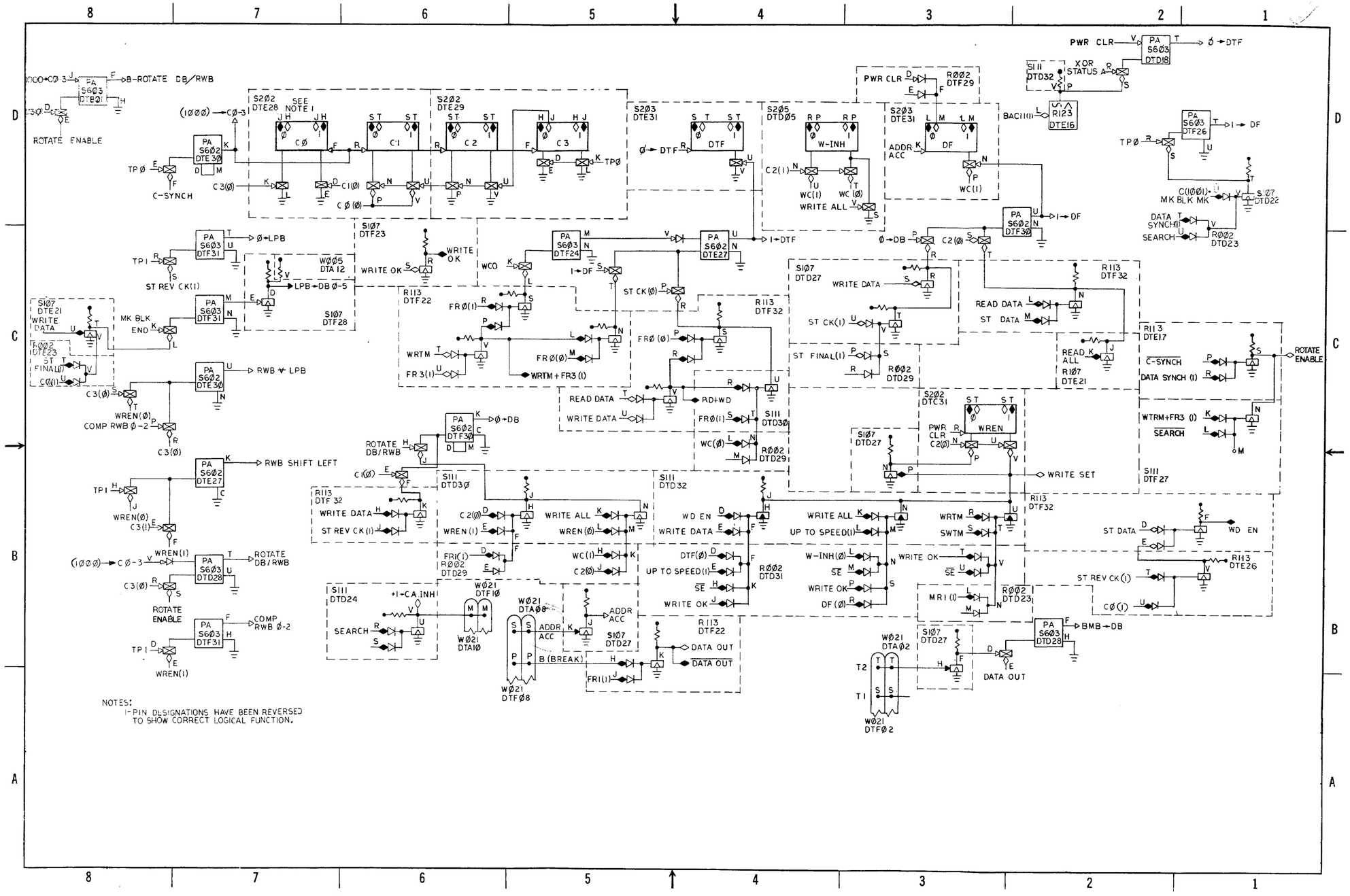
MF, USR, MR, FR BS-D-TC01-0-2 Rev. E

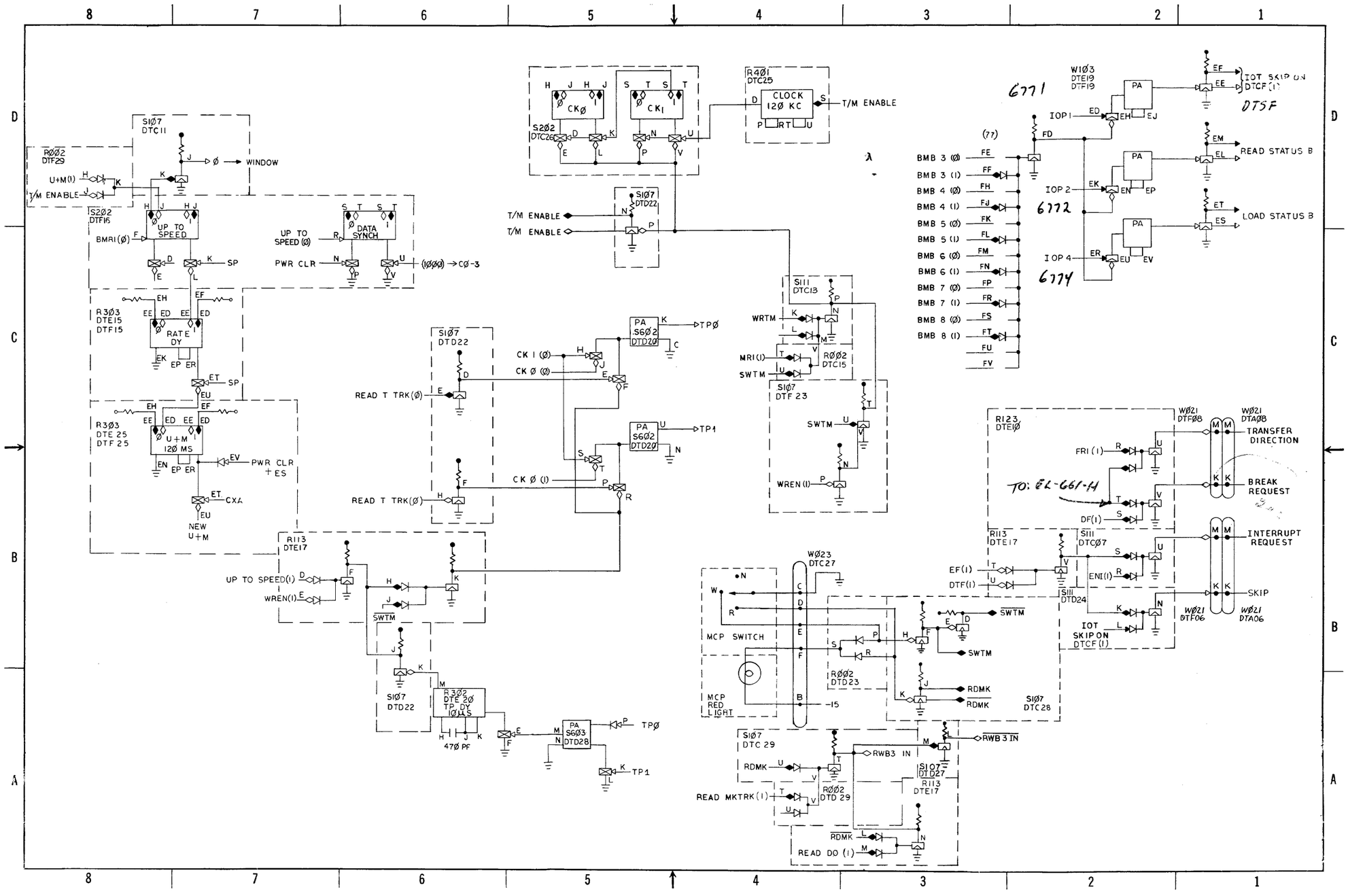


NOTE 1:
PIN DESIGNATIONS HAVE BEEN REVERSED TO SHOW CORRECT LOGICAL FUNCTION.

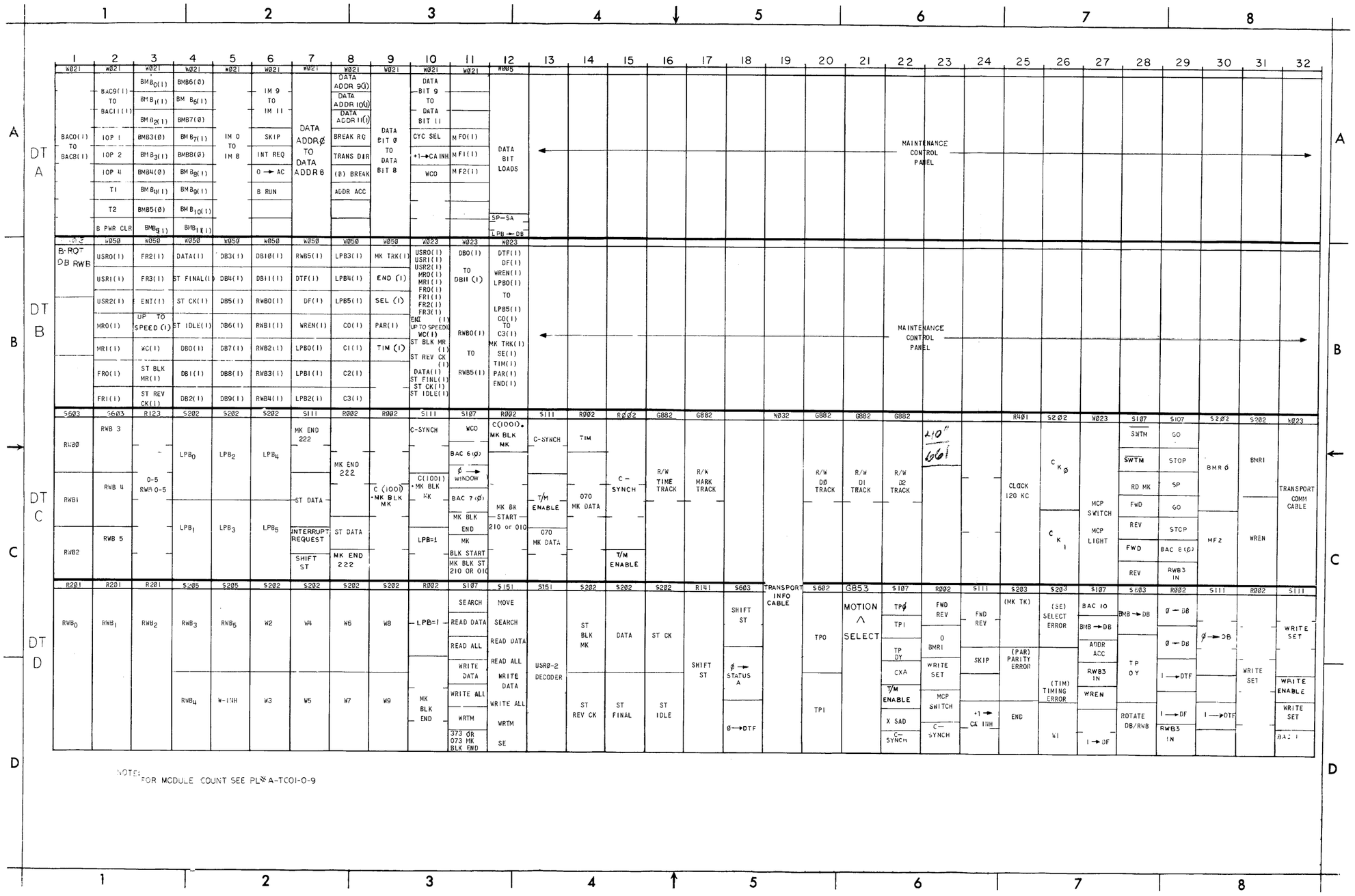
WINDOW, MK TRK, STATE, LPB BS-D-TC01-0-3
Rev. B


W005 DTA12
DATA BIT 0(I)
DATA BIT 6 (I)
DATA BIT 1(I)
DATA BIT 7(I)
DATA BIT 2(I)
DATA BIT 8 (I)
DATA BIT 3 (I)
DATA BIT 9 (I)
DATA BIT 4(I)
DATA BIT 10(I)
DATA BIT 5(I)
DATA BIT 11(I)
W021 DTA09
W021 DTF09
W021 DTA10
W021 DTF10
W021 DTA03
W021 DTF03
W021 DTA04
W021 DTF04
R123 DTE07
R123 DTE08
S205 DTE01
S205 DTE02
S205 DTE03
S205 DTE04
S205 DTE05
S205 DTE06
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
O→DB
B—ROTATE DB/RWB
BMB→DB
BMB0(I)
BMB1(I)
BMB2(I)
BMB3(I)
BMB4(I)
BMB5(I)
BMB6(I)
BMB7(I)
BMB8(I)
BMB9(I)
BMB10(I)
BMB11(I)
R201 DTD01
R201 DTD02
R201 DTD03
S205 DTD04
S205 DTD05
RWB0
RWB1
RWB2
RWB3
RWB4
RWB5
ROTATE DB/RWB
COMP RWB0-2
RWB3 (I)
RWB4 (I)
RWB5 (I)
PA S603 DTC01
LPB0 (I)
LPB1(I)
LPB2 (I)
LPB 3 (I)
LPB 4 (I)
LPB 5 (I)
RWB SHIFT LEFT
RWB3(0)
RWB4(0)
RWB5(0)
LPB→DB0-5
R123 DTC03
RWB 3 IN
READ D1(I)
READ D2(I)
READ D1(0)
READ D2(0)
S603 DTC02
NOTE:
GND PINS C,F,J,L,N,R,U
ON ALL W021'S

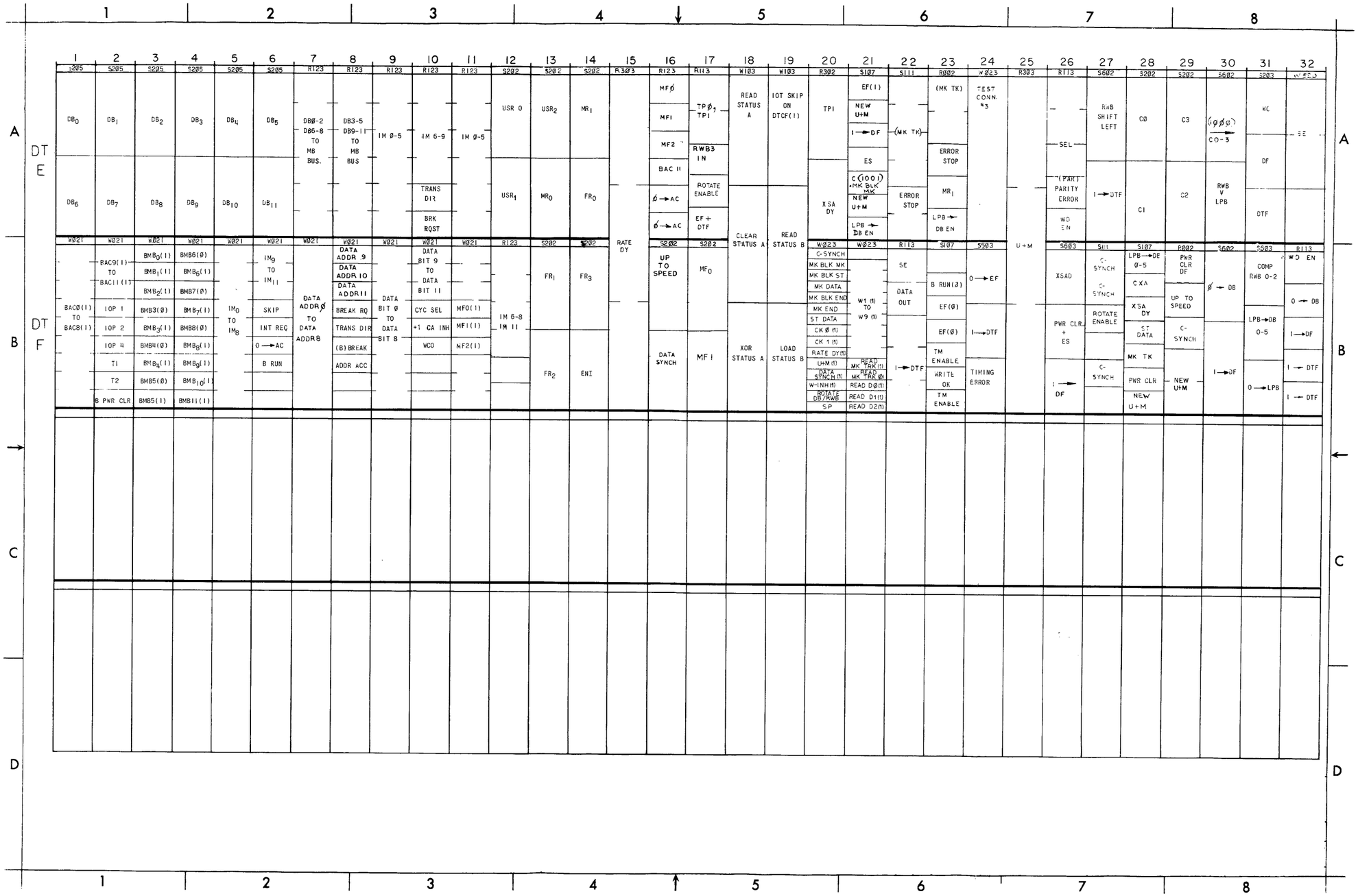

NOTES:
1-PIN DESIGNATIONS HAVE BEEN REVERSED TO SHOW CORRECT LOGICAL FUNCTION.



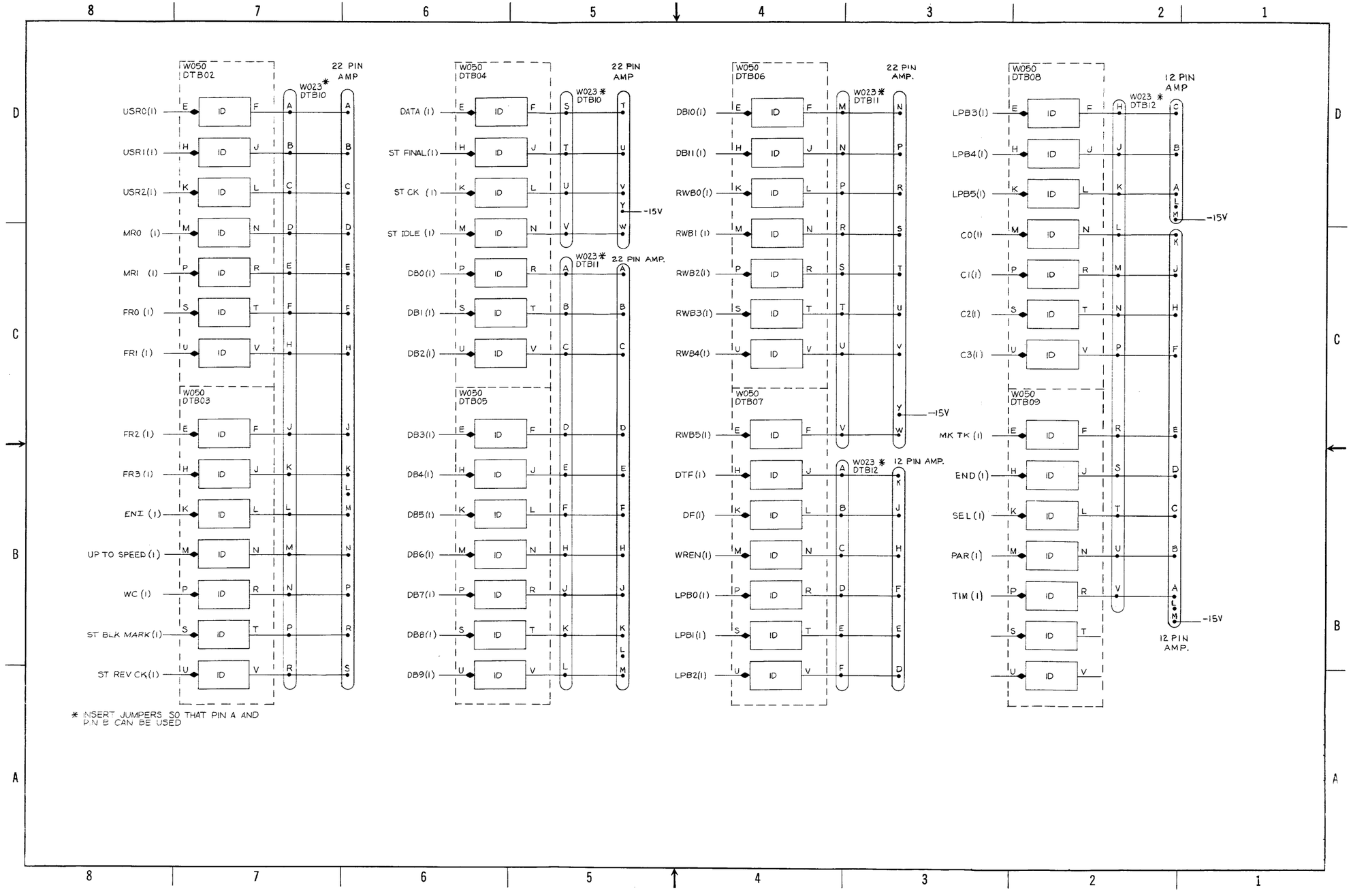
TP GEN TT GEN BS-D-TC01-0-6 Rev. E

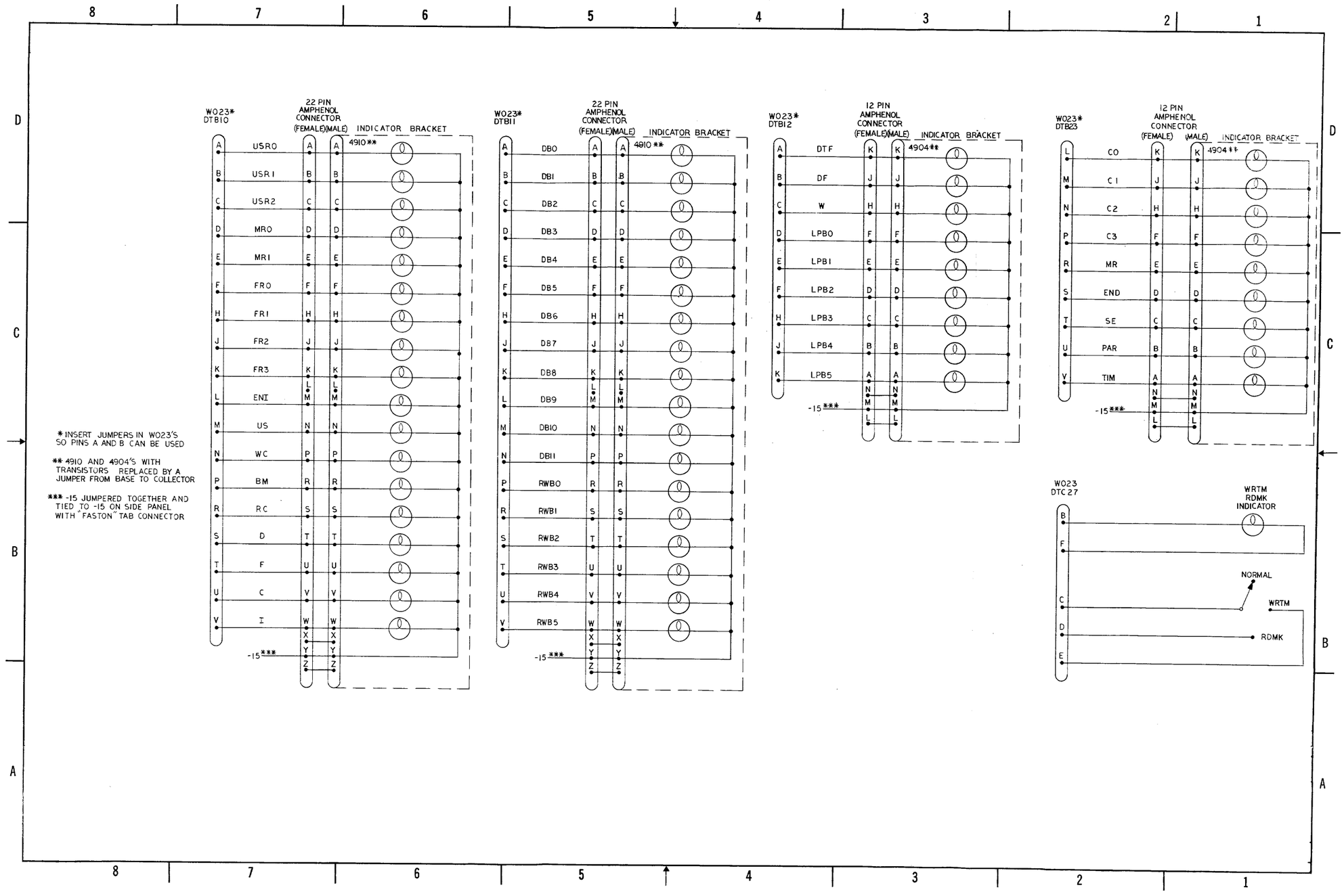


Utilization Module List MU-D-TC01-0-9 Rev. F
(Sheet 1)

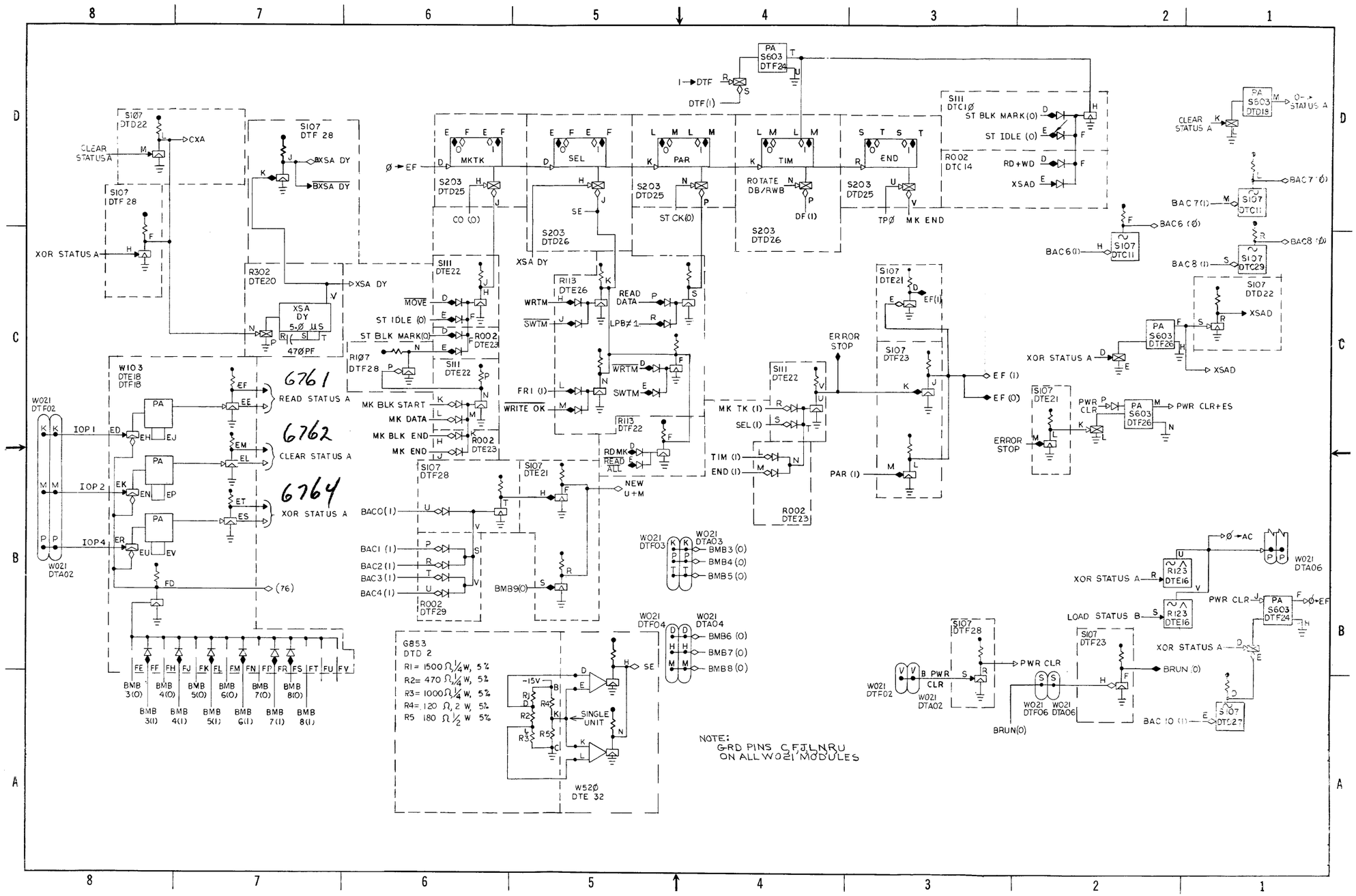


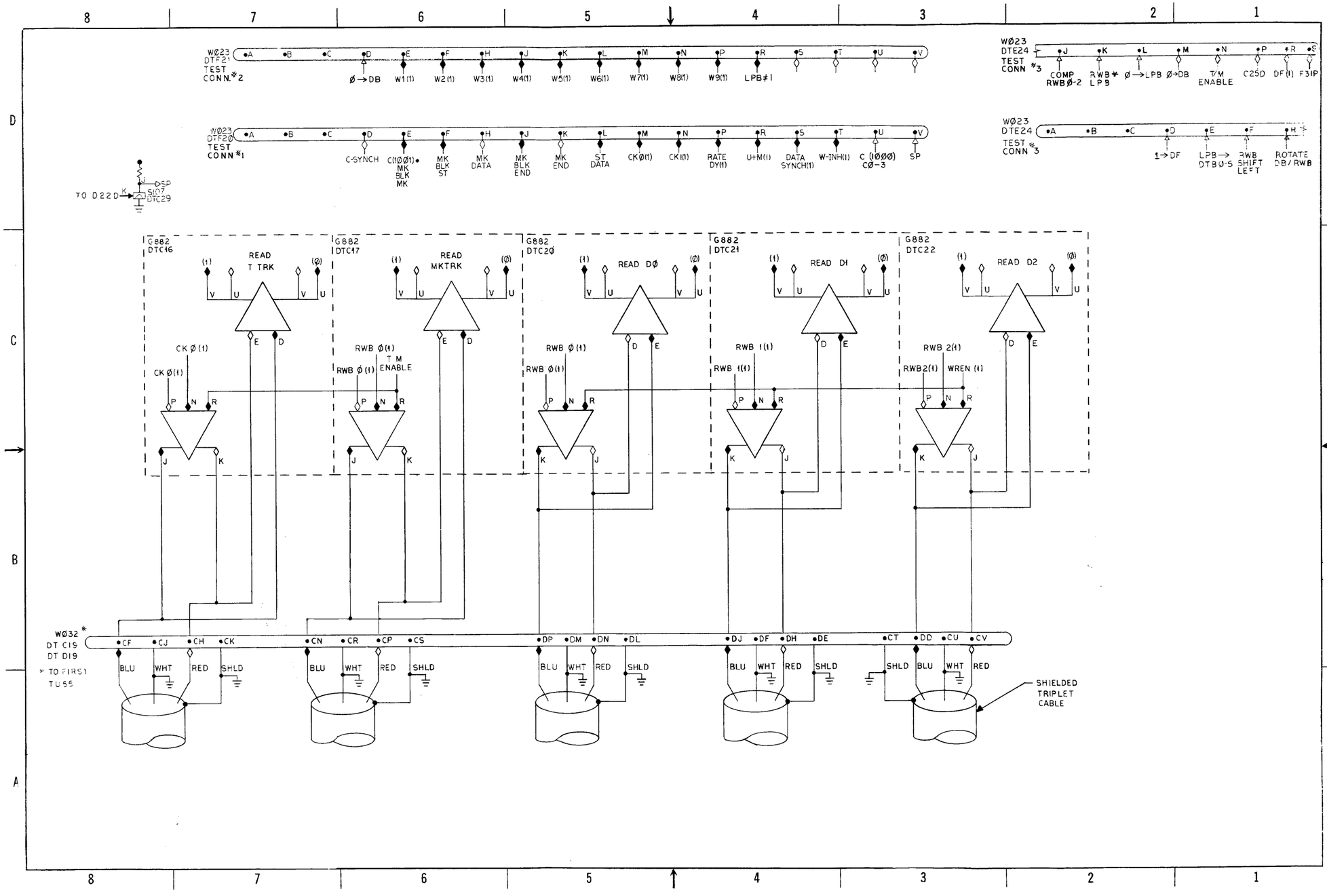
Utilization Module List MU-D-TC01-0-9 Rev. F
(Sheet 2)


W050 DTB02
W050 DTB03
W050 DTB04
W050 DTB05
W050 DTB06
W050 DTB07
W050 DTB08
W050 DTB09
W023 * DTB10
W023 * DTB11
W023 * DTB12
22 PIN AMP
12 PIN AMP
USR0(1)
USR1(1)
USR2(1)
MR0 (1)
MR1 (1)
FR0 (1)
FR1 (1)
FR2 (1)
FR3 (1)
ENI (1)
UP TO SPEED (1)
WC (1)
ST BLK MARK (1)
ST REV CK (1)
DATA (1)
ST FINAL (1)
ST CK (1)
ST IDLE (1)
DB0(1)
DB1(1)
DB2(1)
DB3(1)
DB4(1)
DB5(1)
DB6(1)
DB7(1)
DB8(1)
DB9(1)
DBI0(1)
DBI1(1)
RWB0(1)
RWB1(1)
RWB2(1)
RWB3(1)
RWB4(1)
RWB5(1)
DTF(1)
DF(1)
WREN(1)
LPB0(1)
LPB1(1)
LPB2(1)
LPB3(1)
LPB4(1)
LPB5(1)
C0(1)
C1(1)
C2(1)
C3(1)
MK TK (1)
END (1)
SEL (1)
PAR (1)
TIM (1)
-15V
ID
* INSERT JUMPERS SO THAT PIN A AND P.N B CAN BE USED



Maintenance Control Panel BS-D-TC01-0-13

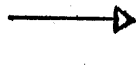

6761
READ STATUS A
6762
CLEAR STATUS A
6764
XOR STATUS A
MKTK
SEL
PAR
TIM
END
MK BLK START
MK DATA
MK BLK END
MK END
MOVE
ST IDLE (0)
ST BLK MARK(0)
WRTM
SWTM
READ DATA
LPB≠1
FRI (I)
WRITE OK
RD MK READ ALL
NEW U+M
XSA DY
BXSA DY
CLEAR STATUS A
XOR STATUS A
IOP 1
IOP 2
IOP 4
BAC1 (I)
BAC2 (I)
BAC3 (I)
BAC4 (I)
BACO (I)
BMB9(0)
BMB 3(0)
BMB 4(0)
BMB 5(0)
BMB 6(0)
BMB 7(0)
BMB 8(0)
BMB 3(I)
BMB 4(I)
BMB 5(I)
BMB 6(I)
BMB 7(I)
BMB 8(I)
CO (0)
ST CK(0)
TPØ
MK END
DF (I)
ROTATE DB/RWB
RD+WD
XSAD
ST BLK MARK(0)
ST IDLE (0)
ERROR STOP
MK TK (I)
SEL (I)
TIM (I)
END (I)
PAR (I)
EF (I)
EF (0)
PWR CLR
PWR CLR+ES
BAC7 (Ø)
BAC7 (I)
BAC6 (Ø)
BAC6 (I)
BAC8 (Ø)
BAC8 (I)
BAC 10 (I)
LOAD STATUS B
BRUN (0)
B PWR CLR
R1 = 1500 Ω, 1/4 W, 5%
R2 = 470 Ω, 1/4 W, 5%
R3 = 1000 Ω, 1/4 W, 5%
R4 = 120 Ω, 2 W, 5%
R5 = 180 Ω, 1/2 W 5%
SINGLE UNIT
-15V
NOTE:
GRD PINS C,F,J,L,N,R,U
ON ALL W021 MODULES



R/W AMPS, SP GEN, TEST CONN.
BS-D-TC01-0-15 Rev. E

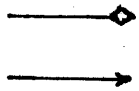
PDP-8 LOGIC SYMBOLS

Negative pulse

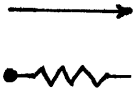


Positive going pulse

Negative level

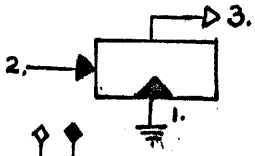


Ground level



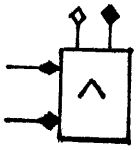
Flow

- 15v Load clamped at - 3v

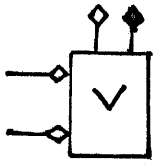


PNP Transistor inverter

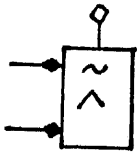
1. emitter
2. base
3. collector



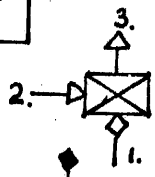
And gate



Or gate

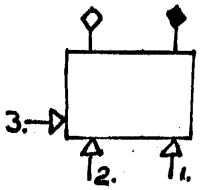


Nand gate



Diode-capacitor-diode gate

1. level input
2. trigger input
3. pulse output



Flip-flop

1. set to one
2. set to zero
3. direct clear

Inverting bus driver

Pulse amplifier

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

Printed in U.S.A.