Digital Equipment Corporation
Maynard, Massachusetts

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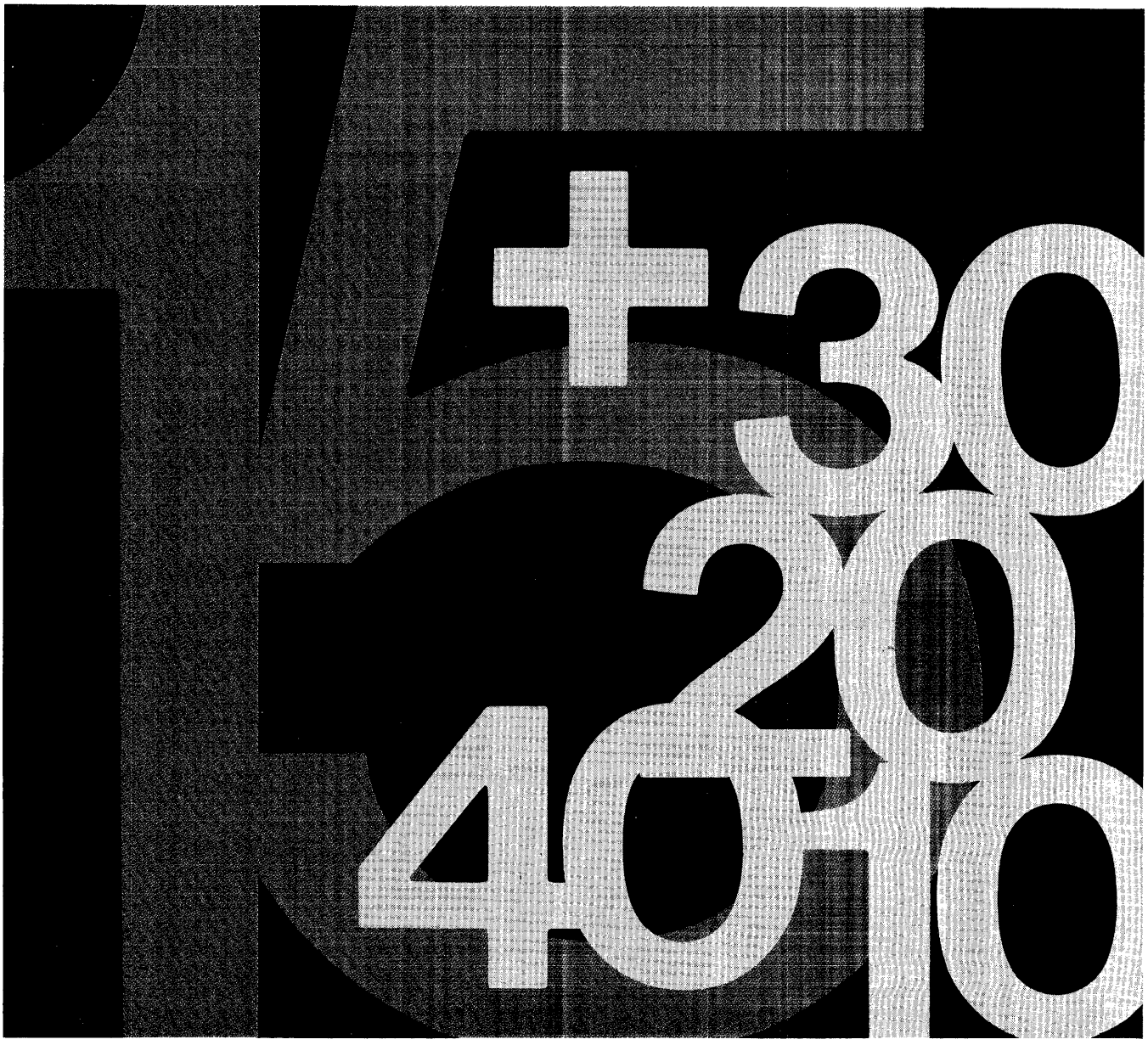
PDP-15 Systems

TC15 DECtape Control Maintenance Manual



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TC15
DECTAPE CONTROL MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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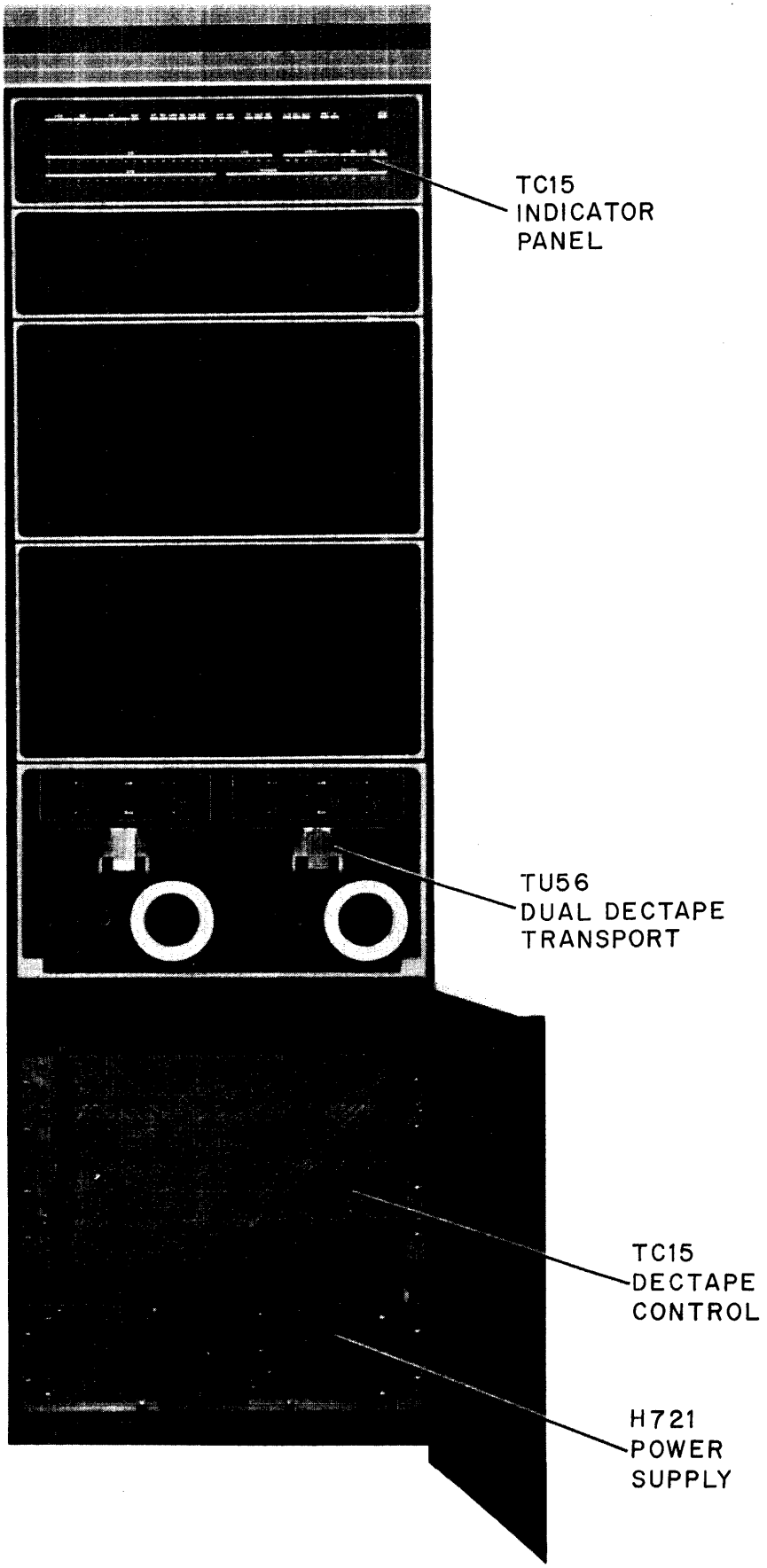
TC15
INDICATOR
PANEL
TU56
DUAL DECTAPE
TRANSPORT
TC15
DECTAPE
CONTROL
H721
POWER
SUPPLY

CHAPTER 1
THE DECtape SYSTEM

1.1 INTRODUCTION TO DECtape

The DECtape system is a computer peripheral device that stores digital data on .75-in. magnetic tape in a three-track parallel/serial format. The tape, called DECtape, is wound on 3-1/2 in. pocket-size reels, which are easy to carry and load. Each reel has a capacity of 3 million bits for 260 ft of tape.

1.1.1 A Computer Peripheral

The DECtape device is a fast, convenient, reliable, low-cost input/output data storage facility and updating device. Each DECtape system consists of a controller and from one-to-eight TU55 DECtape Transports or from one-to-four TU56 Dual DECtape Transports (see Figure 1-1). The controller is connected to the computer I/O bus and communicates with the processor for control and status information and with memory through the I/O processor for data information. Each drive is connected to the controller through a parallel bus; both control and data information pass through this bus.

There are two controller models and two tape drive models. Table 1-1 lists the models and compatible computer systems. Note that the TC15 and TC09 are functionally identical. Any significant differences are pointed out in the text.

Table 1-1
DECtape Model Numbers

Controller Model	DECtape Drive Model	Computer System
TC09	TU55, TU56	PDP-9, PDP-9/L
TC15	TU56, TU55	PDP-15

1.1.2 Storage Medium

Each transport contains motors, tape heads, and the logic necessary for selection, motion control, and data transfer. Each drive can handle 260-ft reels of .75-in., 1-mil magnetic tape. Bits are recorded

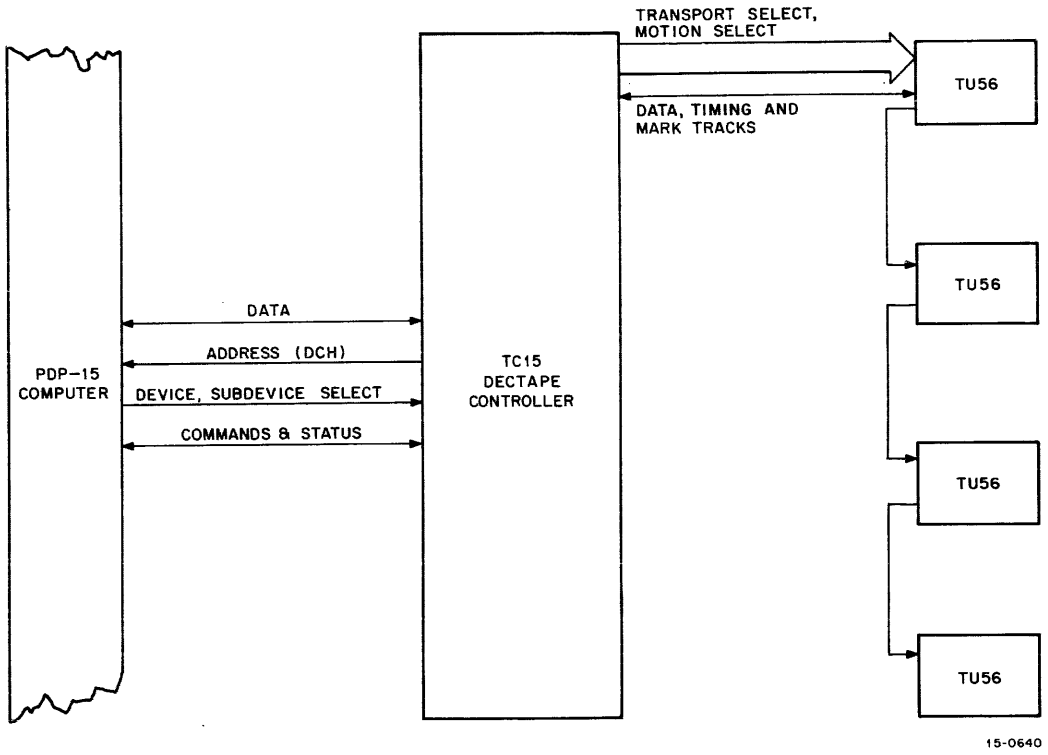

Figure 1-1 DECtape System Simplified Block Diagram

at a density of 350 ±55 bits per track inch. The tape moves 93 ± 12 in. per second and can store up to 147,968 18-bit words. The TU55 has one drive, and the TU56 two drives (see Figures 1-2 and 1-3).

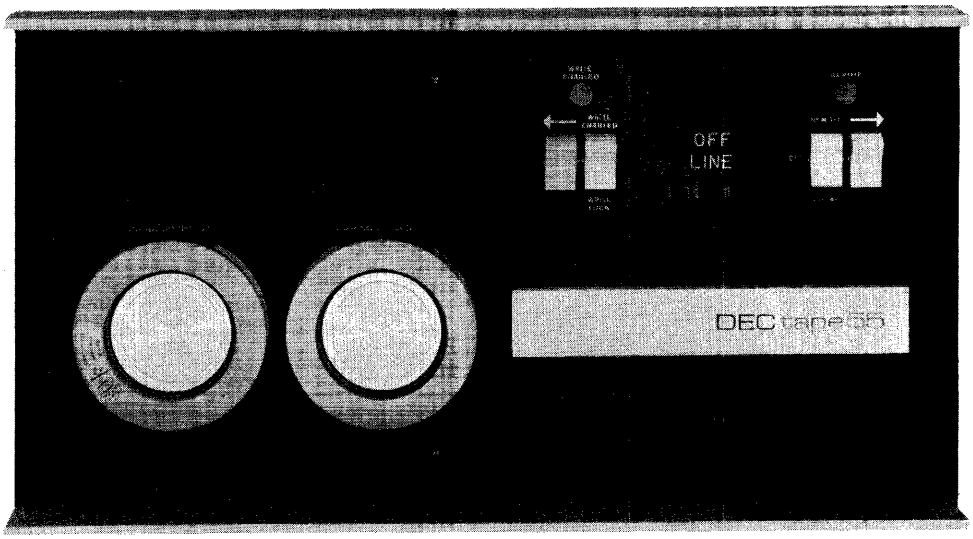

Figure 1-2 TU55 DECtape Transport

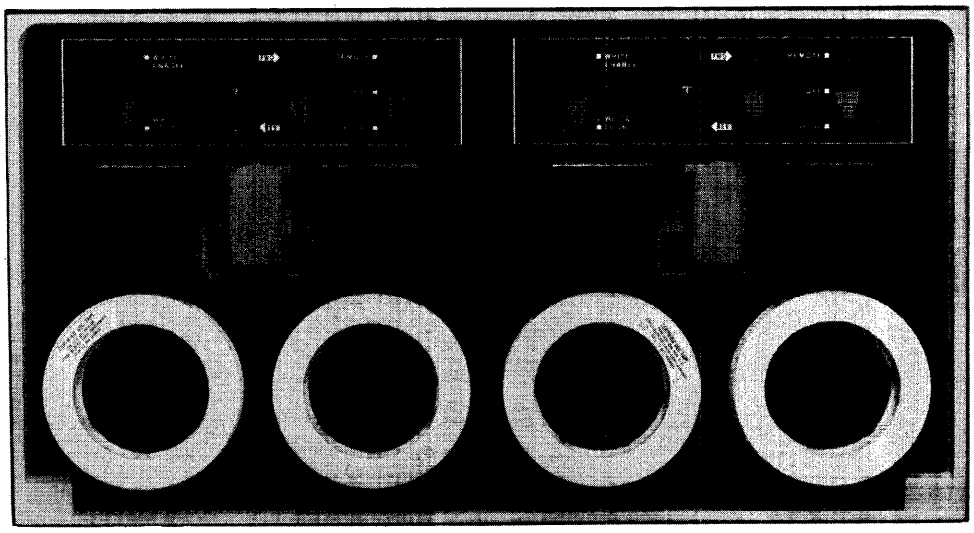

Figure 1-3 TU56 Dual DECtape Transport

1.1.3 Data Storage Format

The DECtape system stores data in a parallel format; each 18-bit data word is divided into six 3-bit bytes, which are stored in parallel across three data tracks. The system stores the complete 18-bit word serially along the tape in six 3-bit bytes.

1.1.4 Data Blocks

DECtape stores data in blocks (or groups), utilizing prerecorded, fixed-position addressing that allows selective updating of tape information; this feature is also used in magnetic disk or drum storage devices. Each data block is uniquely addressable and is numbered to provide random accessing. Another DECtape feature is bidirectional operation; i.e., each block can be identified by the computer regardless of the direction in which the tape is moving. Consequently, the tape can be read from or written on in either direction. This feature provides the programmer with a relatively fast search time, because the tape does not have to be rewound before a block can be found, and, thus, the programmer can begin to write at either end of the block as soon as the correct block number is found. It is important that the programmer read and write data in the same direction, however, or be prepared to unscramble it in the computer.

1.1.5 Block Length

The number of words in each block (block length) is predetermined when the tape is formatted. A standard block consists of 256 18-bit words. Tape formatting involves the writing of a timing track (which furnishes timing pulses to the controller) and the writing of a mark track (which contains codes to inform the controller where the tape is within a given block). Special timing and mark tracks are contained on the tape for this purpose. Formatting also involves numbering of the data blocks and also specifying the length of the data blocks. When the block lengths are established by the programmer, they cannot be changed without destroying the data on the tape.

1.2 TAPE SURFACE RECORDING FORMAT

1.2.1 DECtape Heads and Tape Tracks

The data, timing, and mark tracks are written on or read from the magnetic tape through read/write heads; these heads magnetize the tape in one of two directions to represent a 0 or a 1 and read the same information back. There are 10 read/write heads distributed along the 3/4-in. wide tape. Each head covers a narrow path called a tape track or channel. Figure 1-4 shows a tape stretched over the 10 heads and shows how the width is divided into 10 tracks.

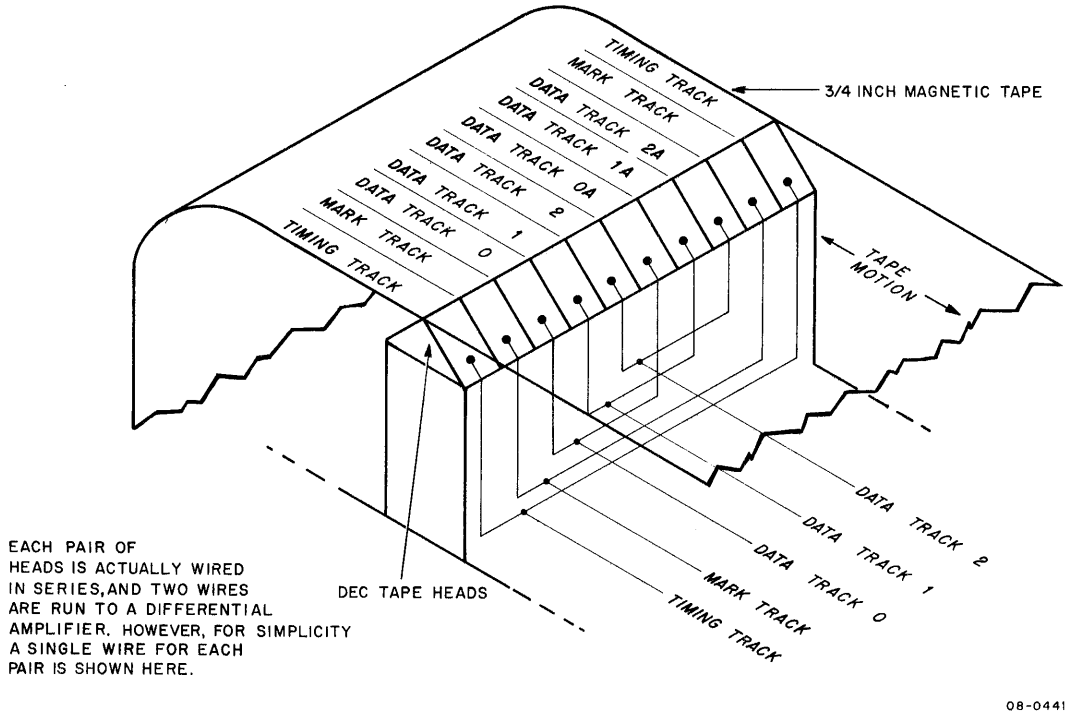

Figure 1-4 DECtape Heads and Tape Tracks

The 10 tracks and heads are divided functionally into 5 redundant pairs. The two outside tracks, called timing tracks, furnish the main timing to the controller. The two tracks next to the timing tracks (toward the center of the tape) are the mark tracks, which tell the TC15 controller where the tape is and what type of data is stored in the associated information tracks. The three pairs of information or data tracks are placed in the middle of the tape where the effect of skew is minimized.

This recording/reading system has a high reliability, because the 10 tracks are divided into 5 redundant pairs; i.e., the two heads for each track are wired in series and record and write the same information. When reading, the analog sum of the two heads is used to determine the correct value of the bit. Therefore, a bit cannot be misread unless the noise on the tape is sufficient to change the polarity of the sum of the signals being read. When writing, the two heads record the same information.

In summary, the five pairs of tracks consist of the timing track, the mark track, and three data tracks. An 18-bit PDP-15 word uses 6 lines of 3 data bits each (1 frame).

1.2.2 Tape Recording Format

Before a reel of tape can be used on the DECtape system, it must be formatted. This process involves logically dividing the 260-ft length into 3 zones: two end zones and a recording zone. The end zones are approximately 11-ft long, never contain data, and are used to wind tape around the heads onto the take-up reel.

The recording zone, which contains the data, is divided into blocks. Each block stores a specific number of data words and several control words, including its own address or block number. The number of words each data block can store is determined when the tape is formatted. Normally, one reel is formatted with 578 blocks, each with 256 18-bit data words. The total length of the tape is equivalent to 884,736 lines, which can be divided into any number of blocks, up to 4096. Complete instructions on how to format a tape are provided in the DECtape Format Generator Program Manual.

Each data block on the tape (see Figure 1-5) has the following characteristics:

a. Each block is numbered. This number is contained in the data tracks at the block number frame at either end of the block. The computer can identify a block by its number when approaching the block from either direction. Thus, data can be read from or written on the tape in the direction of approach.

b. A longitudinal parity checksum is automatically calculated by the controller and deposited into the parity check frame of the block. There is a parity check frame at either end of the block so that the checksum can be deposited on the end of the write operation in the direction data has been written. When the data is read back, this checksum is recalculated and compared with the original. Any discrepancy is reported to the computer.

c. Spaces are established to delineate blocks and to delineate between the block number and data area within a block, thus giving the computer time to react to the number (i.e., set up for the transfers). The different areas of a block, as well as the different zones on the tape, are identified by the controller from special codes prerecorded on the mark track. These codes are not seen by the computer and are of no interest to the programmer except for the function that they perform. A more detailed description of the mark track is provided in Chapter 2.

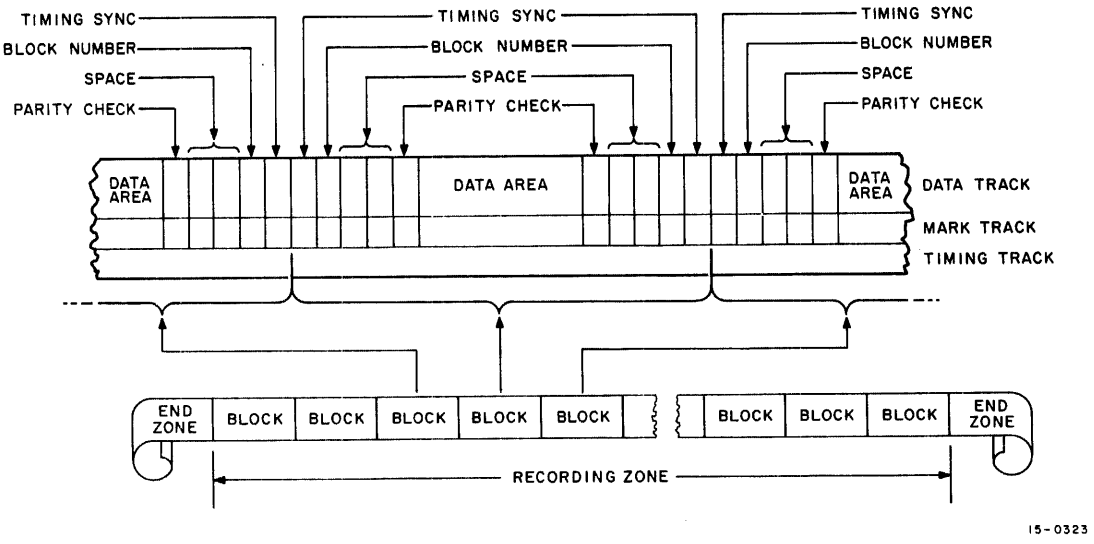

Figure 1-5 DECtape Recording Format

Figure 1-6 shows the bits (0, 3, 6, 9, 12, and 15) used for the write timing and mark track functions.

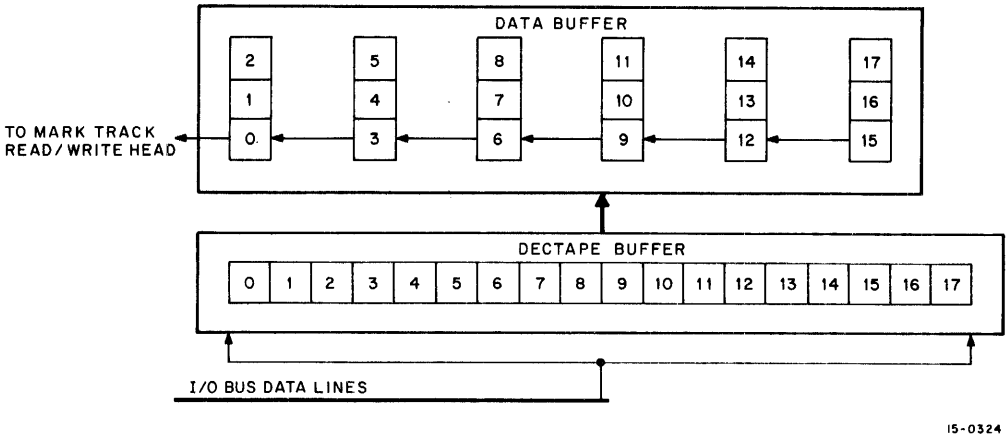

Figure 1-6 Logic for the Write Timing and Mark Track Operation

1.3 DECtape ORGANIZATION

The organization of the hardware in the TC15 controller consists of three parts: the control section, the data transfer section, and the format section, as shown in Figure 1-7.

1.3.1 Control Section

The control section, which consists of Status A and Status B registers and associated logic, is under program control. The following paragraphs describe the Status A and Status B registers.

1.3.1.1 Status A Register - The Status A register contains a Unit Select Register, Motion Register, Function Register, and an Enable-the-Interrupt flip-flop (refer to Table 1-2).

Unit Select Register - A 3-bit register that feeds a binary-to-octal decoder, which, in turn, drives eight select lines to the control cable. Each transport can be dialed into a particular selection address, using a switch on the front of the transport. If the number decoded from the Unit Select Register corresponds to the number selected on the switch, then that transport accepts motion commands from the controller. If more than one transport is on the same number or none is selected, an error flag is posted as soon as an attempt is made to initiate operation.

Table 1-2
Status A Bit Assignments

Register	AC Bit	Register Bit	Octal Code	Decoding
Unit Select Register (USR)	0-2	0-2		Unit
			000	0
			001	1
			010	2
			011	3
			100	4
			101	5
			110	6
			111	7
Motion Register (MR)	3	0	0 =	Forward (FWD)
			1 =	Reverse (REV)
	4	1	0 =	Stop motion (STOP)
			1 =	Start motion (GO)
Function Register (Mode)	5	0	0 =	Normal mode (NM)
			1 =	Continuous mode (CM)
(Function)	6,7,8	1,2,3		Operation
			000	Move
			001	Search
			010	Read data
			011	Read all
			100	Write data
			101	Write all
			110	Write timing
			111	Unused (causes select error)
Enable the Interrupt (ENI)	9	0	1 =	Enable DECtape control flag (DTCF) to the program interrupt
Error flag (EF)	10		0 =	Clear all error flags
			1 =	Error flags undisturbed
DECtape flags (DTF)	11		0 =	Clear DECtape flag
			1 =	DECtape flag undisturbed

Motion Register - A 2-bit, double-buffered register that commands the selected transport to stop, go, move forward, or move in reverse. Note that each transport remembers its motion, and if it is subsequently unselected without being stopped, it will continue until it is reselected and stopped, or until it runs out of tape.

Function Register - A 4-bit register. The first bit of this register is a mode bit, which selects either continuous or normal mode for each operation of the function register. The difference in response for each function in the two modes is explained in Table 1-3. The remaining three bits are decoded by a

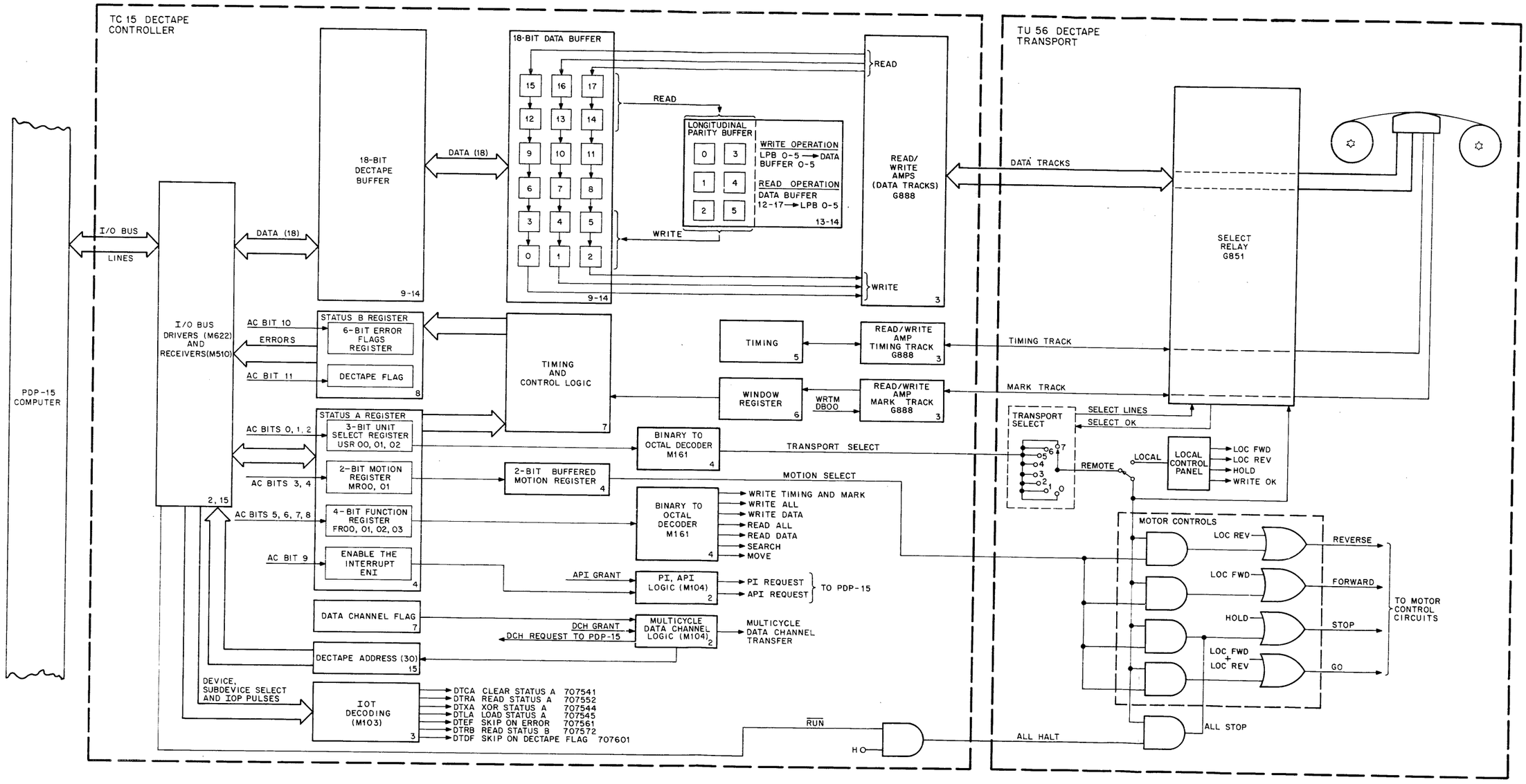

Figure 1-7 TC15 DECtape Control Block Diagram

binary-to-octal decoder to select one of seven possible functions. These functions are explained in Table 1-3.

Table 1-3
DECtape Functions

Function	Operation
MOVE	The MOVE function is used to rewind tape. Code 000 of bits 6, 7, and 8 initiates tape motion in the selected direction, provided GO is also on. The mark track is read, but only the end-of-tape instruction is decoded. End-of-tape sets an error flag and causes an interrupt to the computer. If the tape control is unselected but not stopped, it continues to run; however, the end of tape is not detected. The state of mode is irrelevant.
SEARCH	The SEARCH function is used to search for blocks. When a block number is detected by the mark track, the three-cycle, data-channel facility transfers the number into the address specified by the content of the current address location. The content of the current address location is not incremented, so that successive block numbers always go to the same address. The content of the word count location is incremented as each block number is passed. If the mode is set to normal, the DECtape flag is set each time a block number is detected. This causes an interrupt, and the program can identify the block number. In continuous mode, no interrupt occurs until the word count location overflows. This search operation is most efficient when both modes are used as follows: 1. The current block number is detected in normal mode. 2. The difference between it and the desired block number is computed, and the direction corrected, if necessary. 3. If the direction is reversed, read the current block again and compute the new difference; otherwise go to 4. 4. The 2's complement of the difference is loaded into the word count location. 5. The function is changed to continuous mode. 6. On the next interrupt, the transport is over the desired block. The block number is in the address specified by the current address register.
READ DATA	READ DATA is used to transfer blocks of data into core memory. The standard block length is 256 18-bit words. For this and all following functions, the CA location initially must be set to the transfer memory location minus one, because the CA location is incremented just prior to each word transfer. The WC location is also incremented prior to each word transfer, thus it must be set to the 2's complement of the number of words to be transferred prior to the transfer. Data may be transferred in forward or reverse direction.

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Table 1-3 (Cont)
DECtape Functions

Function	Operation
READ DATA (cont)	Any number of words equal to or less than a block may be transferred in NM. The DTF is raised, and interrupt occurs at the end of each block. The DTF must be cleared before the beginning of the next block (i.e., 1.7 ms) to avoid an erroneous timing error. When partial blocks are transferred, data transmission will end with WC overflow (i.e., the word that causes the WC overflow is the last one transferred). However, the remainder of the block is read and parity checked before the DTF and interrupt occur. Tape motion continues until the GO bit is reset to 0 by the program. If the GO bit is not reset to a 0 or a new function specified before the end of the next block, a timing error will occur. READ DATA in NM is intended primarily for single, 256-word block transfers. If any other number of words is to be transferred, it is advantageous to use CM because no interrupt (DTF) will occur in NM as a result of word count overflow. When WC overflow occurs, it is essential that the function be changed or the GO bit set to 0. Otherwise, transfer begins again (the IOT to clear the DTF specifies the same function again) at the next block (or next word for the ALL functions) since WC = 000000_8 is valid. Any number of words may be transferred in CM. However, the DTF and an interrupt occur only once after a WC overflow (at the end of a block). The comments concerning tape continuation apply in CM as well as NM.
READ ALL	The READ ALL function allows information to be read from an unusually formatted tape by reading all data tracks recorded on DECtape regardless of the mark track value. During the READ ALL function, the DECtape control does not distinguish between different marks recorded on the mark track except to check for mark track errors (MKTK). In normal mode (NM), the DTF is raised and causes an interrupt at the end of each 18-bit word transfer. Data transfer stops after WC overflow, but tape motion continues until the GO bit is set to 0 or a new function is specified (in both NM and CM). If the DTF is not cleared after each word transfer, a timing error occurs at the end of the next word (i.e., 200 μs later). For continuous mode, the DTF is raised and causes an interrupt at WC overflow only. If this interrupt is ignored, no more data transfers occur, but tape motion continues to EOT.
WRITE DATA	The WRITE ENABLE switch on the TU55 or TU56 must be in WRITE ENABLE position for all WRITE functions. All the details of the READ DATA function description apply with the following exceptions. In normal mode, the DTF is set to a 1 at the end of each block. If WC overflow did not occur in the block just ended and a new function is specified, the next block is processed provided the DTF has been cleared. If WC overflow did occur in the block just ended and no

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Table 1-3 (Cont)
DECtape Functions

Function	Operation
WRITE DATA (cont)	new function is specified, the tape continues to move, but the writers are disabled, and a timing error occurs. The remainder of the block is written with 0s. In both CM and NM when partial blocks are written, data transfer from core to DECtape stops at WC overflow. All 0s are written in the remaining data words of the block, and the parity check character is computed over the entire block and recorded. In continuous mode, the DTF is set at the end of the block in which WC overflow occurred. Therefore, if no new function is specified, the tape continues to move but the writers are disabled, and a timing error occurs.
WRITE ALL	All the details of the READ ALL function description apply. The WRITE ALL function is used to write an unusual format, such as block numbers, on DECtape after timing and mark tracks have been recorded. The word that causes WC overflow is the last one written in NM or CM. The tape continues to move, but the writers are disabled. NOTE Change of function must be delayed for 90 μs to ensure recording of the last word. An alternative method is to set WC to one greater than desired number of word transfers and change the function within 40 μs after WC overflow. The WC is in location 30. The CA is in location 31. API traps to 44 on level 1.
WRITE TIMING AND MARK TRACK	WRITE TIMING AND MARK TRACK is similar to the WRITE ALL function. In addition, this function is used to write timing and mark track information on their respective tracks.

Enable the Interrupt - A 1-bit register, which when set, allows the controller to use its API or PI interrupt system, and when reset, disconnects DECtape from the interrupt lines. In the disconnect state, none of the error condition or DECtape flags can cause an interrupt. However, Status B is affected in no other way.

1.3.1.2 Status B Register - The Status B Register contains an error flag register and a DECtape flag.

ERROR Flags - These are flip-flops that continually examine possible error conditions during the operation of the transport. Each condition is explained in Table 1-4.

DECtape Flag - This is a single flip-flop that sets when an operation has been successfully completed or if it has been aborted as the result of an error.

Table 1-4
Error Flags

Flag	Description
ERROR FLAG BIT 0	Five types of errors can be detected in the use of DECtape: Timing Error Parity Error Select Error End of Tape Mark Track Error For all errors the EF is set, a bit is set in the status register, and an interrupt occurs if the enable-to-interrupt bit has been set. The DTEF instruction skips on the inclusive-OR of those error bits. Therefore, each status bit must be checked to determine the kind of error. For all but the parity error, the selected transport is stopped and the EF set at the time of the error detection. No DTF occurs. For a parity error, the GO bit remains 1 (i.e., motion continues), and the EF is set simultaneously with the DTF in NM. Only one interrupt occurs; hence the program must check the EF. A parity error in CM sets the EF at the end of the block in which the parity occurs, causing an interrupt (if enabled). If no program action is taken, e.g., stop transport or reverse and reread, data transfer continues, and the DTF is raised and causes an interrupt at WC overflow and end-of-final-block read.
MARK TRACK ERROR BIT 1	A mark track error occurs if the DECtape control fails to recognize a legitimate mark on the mark track. The error may occur in all but the MOVE or WRITE TIMING and MARK TRACK functions. In both CM and NM, the EF is set, the tape transport stops, and an interrupt occurs.
END OF TAPE ERROR BIT 2	An EOT error occurs when the DECtape enters either end zone with the GO bit = 1 and also when the forward/reverse direction bit is set to continue in the same direction. In NM and CM, data transfer stops at the last legitimate block, the EF is set, the tape transport stops, and an error interrupt occurs.
SELECT ERROR BIT 3	Select Error* - A select error results under any of the following conditions: 1. Selection of none or more than one transport. 2. Attempt to write on DECtape transport with WRITE ENABLE/WRITE LOCK switch in the WRITE LOCK position. 3. Attempt to select unit for any function with DECtape transport REMOTE/OFF/LOCAL switch in the OFF or LOCAL (off-line) position. 4. Attempt to write timing and mark tracks with the DECtape controls switch in any position other than write timing and mark track.

*No-tape or tape-run-off reel conditions are not detectable.

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Table 1-4 (Cont)
Error Flags

Flag	Description
SELECT ERROR BIT 3 (cont)	5. Attempt to perform any function other than write timing and mark tracks with the DECtape control switch in the write timing and mark track position. 6. Attempt to execute unused function (Octal Code 7).
PARITY ERROR	Parity Error - A parity error occurs only during the READ DATA function for a hardware-computed parity check character (PCC) failure.
TIMING ERROR	Timing Error - A timing error (program malfunction) is a 'data miss' or program failure to clear the DTF status bit. A timing error occurs also if the program switches to a READ or WRITE DATA function while the DECtape is currently passing over a data area on tape.

The Unit Select, Motion, Function (including Mode) and Enable registers are all set from the accumulator by the XOR Status A IOT (DTXA) or Load Status A IOT instruction (DTLA). Figure 1-7 shows the accumulator bit that sets each flip-flop. The two bits not shown, bit 10 and bit 11, clear the error flags and the DECtape flag, respectively, if they are set to 0 in the AC during an XOR or Load instruction. The word from 0 to 9 is called Status A. All of these bits (0 through 9) can be read back into the computer by executing the IOT instruction Read Status A (DTRA). Table 1-5 provides definitions of DECtape IOT instructions.

The error flags can also be read into the accumulator as AC bits, which correspond to the bits shown in Figure 1-7. Furthermore, the DECtape flag is read into accumulator bit 11. Bits 0 through 6 and bit 11 are collectively called Status B. The IOT instruction that reads them is called Read Status B (DTRB).

In summary, the Status A registers are set under IOT command; they determine the operation to be performed, the transport which is to perform that operation, the direction of motion, and the mode. Any errors are communicated to the computer through the interrupt logic. When an operation is successful, that fact is communicated back to the computer, which then takes further action. The actual information transfers are performed by the multi-cycle data channel facility under the direction of the data transfer logic.

Table 1-5
DECtape IOT Instructions

Mnemonic	Octal Code	Description
DTCA	707541	Clear Status Register A. The DECtape control and error flags are undisturbed (DTF and EF).

(continued on next page)

Table 1-5 (Cont)
DECtape IOT Instructions

Mnemonic	Octal Code	Description
DTRA	707552	Read Status Register A. The AC is cleared and the content of Status Register A is OR'd into the accumulator.
DTXA	707544	XOR Status Register A. The exclusive OR of the content of bits 0 through 9 of the accumulator and Status A is loaded into Status Register A, and bits 10 and 11 of the Accumulator are sampled to control clearing of the error and DECtape flags, respectively. Anytime this command is given with any AC bit from 0 through 4 set to 1, the select delay of 140 ms will be incurred. The WC flip-flop is set to allow subsequent DCH Break Requests.
DTLA	707545	Load Status Register A. Combines action of DTCA and DTXA to load AC0-9 into Status Register A. Bits 10 and 11 control clearing of error and DECtape flags, respectively. The select delay of 140 ms is incurred when this instruction is issued.
DTEF	707561	Skip on error flag. The state of the error flag (EF) is sampled. If it is set to 1, the content of the PC is incremented by 1 to skip the next sequential instruction.
DTRB	707572	Read Status B. The AC is cleared and the content of Status B is OR'd into the accumulator.
DTDF	707601	Skip on DECtape flag. The state of the DECtape flag (DTF) is sampled. If it is set to a 1, the content of the PC is incremented by 1 to skip the next sequential instruction.

1.3.2 Data Transfer Section

The data transfer section processes the flow of data between the multi-cycle data channel facility of the computer and the magnetic read/write heads. There are two types of information: data, and instructions from the tape (which tell the controller what to do with the data). The instructions are recorded on the mark track, which feeds the window register and, subsequently, the data control logic. This combination scans the mark track codes and from them determines whether the tape heads are over end zones or recording zones; if the tape heads are over recording zones, their position in any particular block is determined. At the same time, data from the three data heads and timing pulses from the timing track heads are feeding information to the data buffer and the data control logic, respectively. The timing pulses are used to strobe the mark track and data track information at the proper time. Because data comes into the controller in three bytes, the data buffer is basically three 6-bit shift registers.

As the data is shifted in, the longitudinal parity buffer calculates the parity of each track. When a complete block has been read, this buffer should be all 1s if no error has been detected. If it is not all 1s, then a parity error flag is set.

During a Read operation, the data buffer accumulates a complete 18-bit word and transfers it to the DECtape buffer for temporary storage. The Data Channel flag is then set, and a multi-cycle data channel break is initiated. During the break, this word is transferred out of the DECtape buffer into the location specified by the current address register at location 30. The word count value at location 31 is incremented. The computer is allowed a maximum of 200 μs to complete this operation. If the computer has not responded in time, an error flag is set to show the timing error.

Alternately, if a Write operation is required, the TC15 requests a multi-cycle data channel break; the computer transfers the word to be written into the DECtape buffer, which is then transferred into the data buffer at the right time. From the data buffer, it is shifted out and written onto the tape. At the same time, the TC15 requests another word from the computer as soon as the DECtape buffer is emptied into the data buffer, and the TC15 is ready to write the next portion of data.

At the end of a transfer, the word counter overflows, and the DECtape flag is set. An API break to location 44 is initiated, or a PI break to location 0, as explained in Table 1-3.

1.3.3 Format Section

Before a reel of DECtape can be used in a system, it must first be formatted. Formatting involves writing the proper mark track codes, numbering the data blocks, and writing in the timing track on the tape. A program called the DECtape Format Generator is available to do this. The program specifies the WRITE TIMING and MARK TRACK function and transfers the correct mark track code through the data channel into the DECtape buffer, as shown in Figure 1-6. The controller switch must be on WRTM. Only bits 0, 3, 6, 9, 12, and 15 are used; these bits are loaded into the proper shift register of the data buffer, which then shifts them into the mark track write head and to the tape. In normal mode, the DECtape flag is set after each word is transferred to the mark track. In continuous mode, the DECtape flag is set when the word counter overflows. At the same time, the timing track writer records clock pulses on the timing track. The block numbers are written in WRITE ALL mode after the mark and timing tracks have been written.

1.4 OPERATOR CONTROLS AND INDICATORS

DECtape transport control and indicator functions are described in the appropriate DECtape transport instruction manuals. Operator controls and indicators for the TC15 DECtape Control include a WRTM/NORMAL switch and an array of indicator lamps on the TC15 indicator panel (see Figure 1-8).

The WRTM/NORMAL switch is located on the left side of the TC15 logic panel. This switch places the TC15 in the write timing or mark track mode (WRTM) or normal (NORMAL) for every other mode of operation.

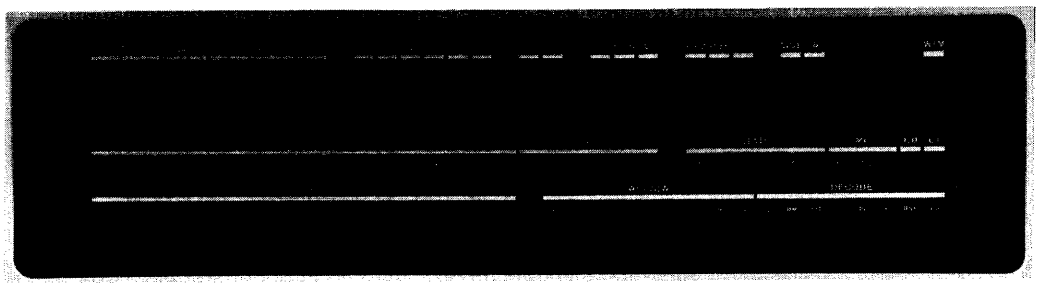

Figure 1-8 TC15 Indicator Panel

Table 1-6 summarizes the function of each indicator on the TC15 indicator panel. Individual bit assignments are defined in Table 1-2.

Table 1-6
Indicator Functions

Indicator	Function
USR	The unit select register specifies which DECtape transport is to be activated.
MR	The motion register specifies stop, go, forward, or reverse.
FR	This 4-bit function register specifies one of seven possible operations in either of two modes.
ENI	Enable the interrupt indicates (when on) that the controller can cause a program interrupt when an error flag or the DECtape flag is set.
EF	This flag is set if any one of the five following error flags come up. These conditions stop transport motion, except for the parity error of bit 4, and all cause a program interrupt if the facility is enabled.
MK	The output from the mark track instruction register is tested every time an instruction appears. If no instruction appears, this indicates that the mark track is not recorded properly and, therefore, an error has occurred. MK and, therefore, EF are set.
END	If the instruction register of the mark track decodes an end zone indicator, this flag and EF are set. A subsequent program interrupt simulates the computer to determine the cause of the interrupt.
SE	This flag indicates select errors on comparison of the control switch states and Status A function states.
PAR	When this light is ON, it indicates that a parity error has occurred at the end of a block after a read data function.
TIM	This flag indicates timing errors.
DTF	This light indicates the state of the DECtape flag. (A 1 indicates a completed operation.)

(continued on next page)

Table 1-6 (Cont)
Indicator Functions

Indicator	Function
API	When ON, this light indicates that the controller is making a request for interrupt on its API channel.
DF	The data flag is set when the controller needs to transfer a data word through the three-cycle break.
DCH	This light indicates that the controller is requesting a data transfer on the multi-cycle data channel.
WC	The word count flag is zeroed whenever the word count register overflows.
U+M	This is the output of the up-to-speed delay. When the light is ON, it indicates that the tape is not yet up to speed.
RDY	This level is set if the repetition rate from timing track is high enough to set UTS.
UTS	This Up-to-Speed flip-flop is set as soon as the tape transport reaches an acceptable speed.
WST	This level indicates that conditions to enable writing exist.
W	This flag, when set, indicates that the writers are enabled.
WTM	This means the SWTM/NORMAL switch is in write timing and mark track mode (SWTM).
DB	These lights reflect the states in the 18-bit data buffer.
LPB	These six indicators reflect the state of the Longitudinal Parity Buffer.
STATE	These bits make up the state generator, a ring counter, which steps from an idle state through five other states and back to idle as a block passes the tape heads.
BM	Block mark is the first bit to which the state generator moves; it is set when forward block mark is in the data buffer.
RC	The reverse checksum state occurs when the Reverse PCC Mark cell is encountered.
D	The data state starts with the first block that contains data (the Reverse Final Mark) and finishes when the next-to-last data block (the Prefinal Mark) passes the read heads.
F	The final state occurs during the last cell that contains data (the Final Mark).
CK	The checksum state occurs when the PCC Mark cell passes the heads. During this state, the checksum is deposited in the PCC Mark, if the TC15 is writing; it checks for a parity error, if the TC15 is in a read operation.
I	The idle state.
MC	These three bits represent a 3-bit counter composed of bits MC00, MC01, and MC02.

(continued on next page)

Table 1-6 (Cont)
Indicator Functions

Indicator	Function
C0, C1	These are the flip-flops that comprise the counters of the timing generator.
DTB	These lights reflect the states of the 18-bit DECtape buffer.
WINDOW	The window register is a simple shift register that receives the instruction codes from the mark track and uses the codes to set the State Generator.
DECODE	The following eight indicators display the outputs of the decode logic from the window register. When ON, the mark track code indicated is in the window register. S MK SYNC BM MK BLK MK BST MK BLK ST D MK DATA BE MK BLK END E MK END BSY MK BLK SYNC DS MK DATA SYNC

1.5 PROGRAMMING EXAMPLES

The following examples illustrate how several DECtape functions can be programmed. In the first example, a specific block is searched out and found, and in the second example, data is read from this block. The subroutines are written in PDP-15 Basic Symbolic Assembler language. Because no indirection is used, the example is intended for Page 0 operation.

1.5.1 Automatic Search

```
BEGIN   LAC (CBLK       /GET THE ADDRESS WHERE THE
                        /BLOCK NO. GOES
        DAC 31          /PUT IT INTO THE CA
        DZM 30          /ZERO OUT THE WC TO AVOID
                        /OVERFLOW
        LAC (JMP SEARCH /GET THE EXIT POINT
        DAC SWITCH      /PUT IT INTO SWITCH
        LAC (321400     /GET THE STATUS A
        DTLA            /LOAD STATUS A REGISTER
44      JMS DECTAP      /API SETUP
DECTAP  0               /SAV PC, LINK, EXTEND MODE
                        /AND MEM. PROTECT BITS
        DAC ACSAV       /SAVE THE AC
        DTEF            /SKIP ON ERROR FLAG
        SKP             /SKIP
```

(continued on next page)

```
        JMP DECER       /GO TO ERROR ROUTINE (NOT SHOWN
        DTDF            /SKIP ON DECTAPE FLAG
        SKP             /SKIP
SWITCH  JMP SEARCH      /GO TO SEARCH ROUTINE
SEARCH  LAC (BLK        /GET THE CURRENT BLOCK NUMBER
        AND (007777     /MASK OUT ALL BUT THE LAST
                        /12 BITS
        SAD RBLK        /SKIP IF DIFFERENT FROM
                        /DESIRED BLOCK
        JMP RBLKS       /SAME BLOCK, GO TO READ DATA
                        /EXAMPLE
        TCA             /DIFFERENT BLOCK, CALCULATE
                        /THE DIFFERENCE BY SUBTRACTING
        DAC TEMP        /THE DESIRED BLOCK FROM THE
        LAC RBLK        /CURRENT BLOCK.  IF THE RESULT
        TCA             /IS NEGATIVE, THEN THE TAPE
        ADD TEMP        /DRIVE IS MOVING TOWARD THE
        SMA             /DESIRED BLOCK.  THE RESULT OF
                        /THIS CALCULATION IS THE TWO'S
                        /COMPLEMENT OF THE COUNT TO
                        /THE DESIRED BLOCK.
        JMP TEST        /GO TO TEST IF TAPE WAS REVERSED
GO      DAC30           /MOTION OK SET UP WC
        LAC (010000     /GET STATUS A CHANGE
        DTXZ            /XOR CHANGE TO STATUS A
                        /(PUT INTO CONTINUOUS)
                        /THE XOR INSTRUCTION IS USED INSTEAD OF THE CLEAR
                        /AND LOAD TO AVOID SETTING THE SELECT DELAY, WHICH
                        /COULD PREVENT ANY ACTION FOR 120 MS
        DBR             /DEBREAK AND RESTORE
        JMP* DECTAP     /RETURN TO MAIN PROGRAM
TEST    ISZ TAG         /CHECK TO SEE IF THE TAG WAS SET
        JMP REV         /IT WAS NOT; GO AND REVERSE
                        /THE TAPE
        TCA             /IT WAS, COMPLEMENT THE AC
                        /TO GENERATE WC
        JMP GO          /GO BACK AND SET UP THE WORD
                        /COUNT
REV     DZM TEMP        /SET UP A DELAY WHICH WILL
        ISZ TEMP        /ALLOW THE TRANSPORT TO MOVE
        JMP .-1         /SEVERAL BLOCKS PAST THE CURRENT
                        /ONE.
        LAC (361400     /GET THE NEW STATUS A WORD
                        /WHICH REVERSES THE TAPE.
        DTLA            /LOAD THE NEW STATUS A WORD
        CLC             /CLEAR AND COMPLEMENT THE AC
        LAC TAG         /PUT RESULTS IN TAG TO REMEMBER
                        /THAT REV HAPPENED.
        JMP* DECTAP     /RETURN TO MAIN PROGRAM UNTIL
                        /THE NEXT NUMBER IS PICKED
                        /UP WHILE THE TAPE IS
                        /TRAVELLING IN THE REVERSE
                        /DIRECTION.
TAG     0
```

NOTE

It is necessary to remember that the tape had been reversed and was travelling towards the desired block. In this way, the previous subroutine could be used when the tape again found the current block while travelling in the reverse direction.

1.5.2 Read Data

```
RBLKS   LAC ADDR        /GET THE ADDRESS
        DAC 31          /PUT IT INTO CA REGISTER
        LAC WDCNT       /GET THE WORD COUNT
        TCA             /TWO'S COMPLEMENT IT
        DAC 30          /PUT IT INTO THE WC REGISTER
        LAC (003000     /GET THE UPDATED FUNCTION
        DTXA            /XOR IT INTO THE CONTROLLER
        LAC (JMP REDE   /GET THE EXIT POINT
        DAC SWITCH      /PUT IT INTO SWITCH
```

1.6 DECtape TECHNICAL DATA SUMMARY

Table 1-7 summarizes the various types of errors that may be detected and reported while performing DECtape functions in normal or continuous mode. Table 1-8 indicates the effect of each DECtape function on the DECtape flag, and the current address and word count locations in normal or continuous modes of operation. Table 1-9 summarizes DECtape timing characteristics. Table 1-10 designates the word count and current address location for data channel and also designates API trap address locations.

Table 1-7
Summary of Errors

Function	Error (Normal or Continuous Mode)	Function	Error (Normal or Continuous Mode)
Move	Select Error EOT	Write Data	Select Error EOT Timing Error MK TRK Error
Search	Select Error EOT Timing Error	Write All	Select Error EOT Timing Error MK TRK Error
Read Data	Select Error EOT Timing Error Parity Error MK TRK Error	Write Timing and Mark Tracks	Select Error Timing Error
Read All	Select Error EOT Timing Error MK TRK Error		

Table 1-8
Summary of Functions

Function	Normal Mode (NM)	Continuous Mode (CM)
Move	DTF: No Interrupt CA*: Ignored WC**: Ignored	Same as NM
Search	DTF: Interrupt at each block mark	DTF: Interrupt at each block mark if WC has over-flowed.
	CA: Not incremented WC: Incremented at each block mark	CA: Not incremented WC: Incremented at each block mark
Read Data	DTF: Interrupt at end of each block	DTF: Interrupt at end of block if WC has over-flowed.
	CA: Incremented at each word transfer	CA: Incremented at each word transfer
	WC: Incremented at each word transfer	WC: Incremented at each word transfer
Read All	DTF: Interrupt at each word transfer	DTF: Interrupt at WC overflow
	CA: Incremented at each word transfer	CA: Incremented at each word transfer
	WC: Incremented at each word transfer	WC: Incremented at each word transfer
Write Data	Same as Read Data	Same as Read Data
Write All	Same as Read All	Same as Read All
Write Timing and Mark Tracks	Same as Read All	Same as Read All
Unused***		

*Current Address (CA) is in location 31.
**Word Count (WC) is in location 30.
***If used by mistake, the control gives a Select Error (SE).

Table 1-9
Summary of Timing

Operation	Time
Time to answer data channel request	Up to 200 μs
Word Transfer Rate	One 18-bit word every 200 μs
Block Transfer Rate	One 256 word block every 53 ms

(continued on next page)

Table 1-9 (Cont)
Summary of Timing

Operation	Time
Start Time	375 ms (±20%)
Stop Time	375 ms (±20%)
Turn Around Time	375 ms (±20%)
Search - Read Data Function change for present block	Up to 400 μs
Search - Write Data Function change for present block	Up to 400 μs
Read - Search Function change for next block number	Up to 1000 μs
Write - Search Function change for next block number	Up to 1000 μs
DTF to beginning of next data block	1.7 ms
DTF Occurrence:	
Move: NM, CM	Never
Search: NM Read Data: NM Write Data: NM	Every 54 ms
Search: CM	(WC) X53 ms
Read Data: CM	(No. of blocks)
Write Data: CM	X53 ms
Read All: NM Write All: NM Write Timing and Mark Tracks: NM	Every 200 ms
Read All: CM Write All: CM Write Timing and Mark Tracks: CM	(WC) X200 ms

Table 1-10
Data Channel and API Summary

Location	Content of Location
30	Word Count
31	Current Address
44 on level 1	API Trap Address

CHAPTER 2
PRINCIPLES OF OPERATION

2.1 INTRODUCTION

This chapter first describes the control logic in the TC15 DECtape Control. This logic consists of device and subdevice decoding, I/O bus drivers and receivers, the functional registers comprising the Status A register, enable-the-interrupt feature, and the error flags. The data transfer logic of the controller is next described and functionally consists of the timing pulse generator, window register, state generator, data buffer, record and replay logic, DECtape buffer, longitudinal parity buffer, and I/O control logic. Finally, each of the DECtape major functions such as read data and write data is described.

Each functional section of the description includes a list of references that complement the text. These references are block schematics that show related logic, figures, or tables. Block schematics are referenced by number only; for example, block schematic 4 refers to either TC15-0-04 or TC09-0-04. If the two block schematics are not logically identical, the differences are indicated. Following the references, each subsection outlines the purpose of the logic, followed by a short analysis of the logic itself.

Signals that appear on a logic drawing are named with a code that has three parts. The first part indicates signal origin, the second is a signal mnemonic, and the last is either an H or an L, indicating that it is true (high) or true (low). For example, signal code TC10 DB05 (1) H means that it originated on block schematic 10 from Data Buffer bit 5 on a 1, and it is true when high.

2.2 CONTROL SECTION DESCRIPTION

2.2.1 Device and Subdevice Logic

The device and subdevice codes (refer to block schematic 3) of each IOT instruction are decoded with the IOP pulses to produce internal control pulses for the controller according to Table 2-1. The decoders are M103s that accept bus signals after they have been buffered by the appropriate receivers.

Table 2-1
Summary of IOT Control Signals

Control Signal		IOT Code	IOT Mnemonic	Function
TC03	CSTA	707541	DTCA	Clear Status Register A
TC03	RSTA	707552	DTRA	Read Status Register A
TC03	XSTA	707544	DTXA	XOR Status Register A, clear WC Flag
TC03	SEF	707561	DTEF	Skip on Error Flag
TC03	RSTB	707572	DTRB	Read Status Register B
TC03	SDTF	707601	DTDF	Skip on DECtape Flag

2.2.2 I/O Bus Drivers and Receivers

All I/O bus control and data signals are received and transmitted at the controller by modules designed specifically for this purpose (refer to block schematics 2 and 15). The TC15 controller receives I/O bus signals with M510 modules and transmits them with the M622.

2.2.3 Unit Select Register

The code, loaded into this register, specifies which transport is to be selected. It forms the first three bits of the Status A register, which is controlled by the XSTA signal (refer to block schematics 4 and 16). Table 1-3 summarizes the decoding. The three bits called USR00, USR01, and USR02 drive an M161 binary-to-octal decoder. The outputs of the decoder are cabled to each DECtape transport. Whenever the select switch of any DECtape transport corresponds to the enabled output of the decoder, then that transport will respond to command signals from the controller. If none or more than one transport is selected, an error is set in the controller. Refer to the TU55 or TU56 Maintenance Manual for details of the unit select logic located in each transport.

2.2.4 Motion Register

The motion register forms two bits of the Status A register and is used to select one of four possible motions by the transport — STOP, GO, FORWARD, and REVERSE, decoded according to Table 1-2. The output of this register is cabled to each transport on the system. The selected transport will accept the commands and react accordingly (refer to block schematics 4 and 16).

The 2-bit motion register, designated MR00 and MR01, is loaded from the I/O bus with the XSTA control pulse. After 5 μs, a second motion register buffer, designated BMR00 and BMR01, is loaded from the first. This 5-μs interval allows the select logic time to enable the next transport before decoding

the motion command. Thus, the output of the second buffer is cabled to each DECtape transport. The START/STOP bit is cleared to STOP by the signal TC08 PC+ES L, which occurs if there is an error, a power clear signal, the computer stops, or if the control signal CSTA is issued by the central processor.

2.2.5 Function Register

The mode register selects one of two operating modes: normal or continuous. The outputs are used internally by the controller and are not seen by the DECtape Transports. The function register, constituting three bits of the Status A word, selects one of seven operations performed by the DECtape system, decoded according to Table 1-2.

The mode register (FR00) is a 1-bit register, which is part of the Status A word. K is loaded by the XSTA IOT pulse. The function register bits are designated FR01, FR02 and FR03. These bits drive a binary-to-octal decoder that outputs eight complementary pairs. Of these, seven pairs are interpreted as the seven different operations that the system can perform. The register is loaded by the XSTA control pulse (refer to block schematic 4).

2.2.6 Enable the Interrupt

The 'enable the interrupt' flag is gated with the error flags and the DECtape flag and must be set before an automatic priority interrupt or program interrupt can take place. This flag is part of the Status A word (refer to block schematics 3 and 4). The enable the interrupt flag is a 1-bit register set by the XSTA control pulse. The flag is gated with the error and DECtape flags shown on drawing 3, at coordinates A-8.

2.2.7 Error Flags

The purpose of each error flag is summarized in Table 1-4. The conditions under which an error flag is set are summarized in Table 2-2. Compare the error flag conditions listed in Table 1-4 with the input signal descriptions listed in Table 2-2 to determine how the error flag logic, shown on block schematic 8, functions.

Table 2-2
Input Signals of the Error Flags

Input Signal	Gate	Signal Description
THE MARK TRACK ERROR		
TC06 MK BLK START L TC06 MK DATA L TC06 MK BLK END L TC06 MK END L	OR	One of these window register codes must be present at the beginning of each cell during the data transfer area of a block in all but a Move Function.
TC08 ST BLK MK (0) H TC08 ST IDLE (0) H -TC04 MOVE H	AND: Output to Data Input of Flip-Flop	The AND of these two signals defines the data area of a block for all operations but Move. Note that during Write Timing and Mark, IDLE is always set.
MC01 (1) H	CLOCK Input of Flip-Flop	This point clocks the error flag at the beginning of each cell.
END OF TAPE ERROR		
TC06 MK END H	CLOCK Input to Flip-Flop	Window code, indicating that the end of tape is approaching.
TC05 TP0 H		Timing pulse 0.
SELECT ERROR		
TC16 T SINGLE UNIT H	INVERTER	If high, this signal indicates that no transport or more than one transport is selected. The G879 detects these conditions.
TC04 FR01 (1) H	AND	Specifies Write, Write All, Write Timing and Mark.
-TC08 WRITE OK H		Write enable switch not turned on.
TC04 WR TM H	AND	Function is Write Timing and Mark.
-TC08 SW TM H		Switch not set to Write Timing and Mark.
TC08 SW TM H	AND	Switch set to Write Timing and Mark.
-TC04 WR TM H		Function not set to Write Timing and Mark.
TC08 XSA DY H	CLOCK Input	IOT DTXA - XOR STATUS A.

(continued on next page)

Table 2-2 (Cont)
Input Signals of the Error Flags

Input Signal	Gate	Signal Description
PARITY ERROR		
TC04 READ DATA H	AND to Data Input of Flip-Flop	Read Data Function specified.
TC08 LPB NOT EQ 77 H		On the clock that is ST CK, the LPB should be all 1s if no errors have been made. This signal should be high.
TC07 ST CK (0) H	CLOCK Input of Flip-Flop	As this state goes to a 0, the parity checksum stored in the PCC will have been assembled into the LPB, which must then equal all 1s.
TIMING ERROR		
TC07 DF (1) H		Data flag is on a 1.
TC05 MC00 (1) H		These three timing signals occur at the end of a cell when a new word is assembled. If the DF is not down, then a word is lost, and an error occurs.
TC05 MC01 (0) H	AND	
TC05 TP1 H		
TC08 ST BLK MK (0) H		These three signals delineate the data area on a block during a read or a write operation.
TC08 ST IDLE (0) H	AND	
TC04 RD+WD H		
TC03 XSTA H		A change status IOT is issued. If it falls during the above condition, then an error occurs.
TC07 DTF (1) H	CLOCK	The DECtape flag is set.
TC07 1 to DTF H	Input of Flop	An attempt is made to set the DTF while it is up. The flag was not processed between interrupts, and an error occurs.

2.3 DATA TRANSFER DESCRIPTION

2.3.1 Timing Pulse Generator

Refer to block schematics 3 and 5, and Figure 2-1. The timing pulse generator logic receives, conditions, delays, and counts incoming timing track pulses. This logic also writes the clock pulses onto the timing track and supplies the controller with an aritficial timing pulse during the Write Timing and Mark Track operation. The timing pulse generator logic contains write, read, up-to-speed, and counter logic.

2.3.1.1 Write Logic - The write logic consists of:

a. A 120-kHz Type M401 Clock, which is enabled during a valid Write Timing and Mark Track operation only.

b. A 2-bit switch-tail counter designated CK0, CK1 and driven by the clock.

c. A G888 writer driven by one bit of the counter, CK0.

Bits CK0 and CK1 are 90 degrees out of phase with one another. While CK0 is driving the G888 driver and writing the timing track, CK1 is supplying the controller with an artificial tape timing pulse, which the controller needs to write the mark track. Although CK1 is 90 degrees out of phase with CK0 during this operation, its pulses are in phase with the timing track pulses when they are read back, because the signal read is the derivative of the signal written.

2.3.1.2 Read Logic - The read logic consists of:

a. A G888 reader that accepts the output of the timing track tape head and amplifies, limits, and conditions them. The G888 reader generates from this two separate output pulse trains, which are 16 μs apart at full tape speed, and 90 degrees out of phase. These two outputs feed two parallel logic circuits.

b. Two parallel noise suppression networks, consisting of two M302 delays whose outputs are cross-coupled into their counterpart's network. When a delay fires, it ignores all further inputs and inhibits its opposing input at gate 2 during its delay (10 μs). In this way, noise, particularly from cross-talk, is suppressed.

c. Miscellaneous logic which follows gates and delays, inverts, drives, and combines the pulse trains.

2.3.1.3 Up-to-Speed Logic - The up-to-speed logic consists of:

a. Start-up delay, which is 140-ms long and fires whenever the controller requests a change of motion or unit selection.

b. An up-to-speed delay that monitors one of the timing pulses and fires when the pulse train is sufficient to be considered valid.

c. An up-to-speed flip-flop that fires after the two delays have signaled that the tape is moving properly.

During the start-up-delay period, the selected transport reaches a tape speed that is fast enough to deliver valid inputs to the G888 reader. The G888 will oscillate at inputs below 55 μV. The up-to-speed delay is enabled after the start-up-delay times out. The up-to-speed delay examines the timing pulses and fires when the tape has reached an operational speed. In other words, the up-to-speed delay fires when the timing pulse frequency is high enough. When the up-to-speed delay fires, it also sets the up-to-speed flip-flop, which gates the two pulse chains at 2 of Figure 2-1, allowing them to

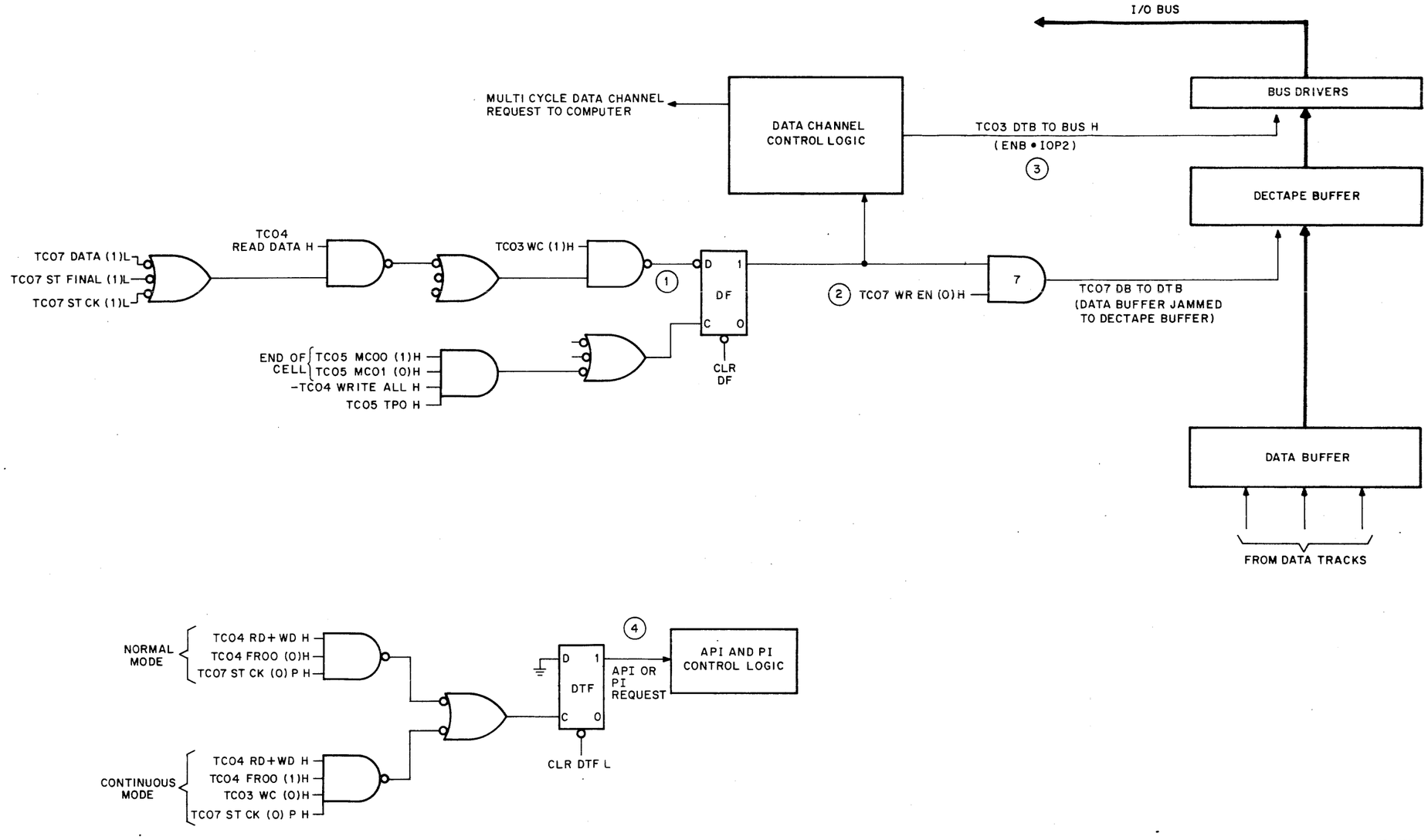

Figure 2-1 Timing Pulse Generator

enter the main timing train of the controller. During Write Timing and Mark Track, the up-to-speed flip-flop is bypassed at 2 of Figure 2-1, and the signal TM EN L enables the gates.

2.3.1.4 Counter Logic - The counter logic consists of:

a. A 4-bit ring counter (called MC0, MC1, MC2 and MC3) driven by TP0 L.

b. A 1-bit counter (called C1) driven by TP1 L.

The ring counter counts to 12; it is synchronized from the mark track and keeps track of the number of 3-bit bytes recorded in a cell. The ring counter also forms the main timing chain for activities within a word cell. The second counter divides the number of TP1 pulses by 2.

2.3.2 Window Register

The window register (refer to block schematic 6) is a 9-bit shift register, which receives the prerecorded instructions or codes from the mark track and decodes them for the controller. The Mark Track codes divide the magnetic tape into zones, blocks, and cells. Table 2-3 lists each code, how the code is seen by the window register, and what it means to the controller.

Table 2-3
Mark Track and Window Codes

Mark Track Code	Name	Window Code	Name	Function
55	REV END	555	None	This code requires no operation. It indicates that tape is leaving an end zone.
25	INTERBLOCK SYNC	725 525	SYNC H	This code is used by the timing generator to synchronize its counters with the beginning of a block. It occurs between blocks and at either end of the tape.
26	FORWARD BLOCK MARK	526	MK BLK MK	This code occurs when the block number is in the data register. During a search, the DF is set and a transfer is carried out. This code also steps the state generator from IDLE to ST BLK MK.
32	REVERSE GUARD MARK	632	MK DATA SYNC	This is a no-operation code, which gives the computer time to respond to the block number it has found in 26.
10	LOCK MARK	610	MK BLK START	This code steps the state generator from ST BLK MK to ST REV CK (Reverse Checksum).

(continued on next page)

Table 2-3 (Cont)
Mark Track and Window Codes

Mark Track Code	Name	Window Code	Name	Function
10	REVERSE PCC MARK	410	MK BLK START	The same code also steps the state generator to DATA; the controller then carries out data transfers. During this state, the LPB is initiated.
10	REVERSE FINAL MARK	410	MK BLK START	This is the first data cell.
10	REVERSE PREFINAL	410	MK BLK START	This is the second data cell.
70	DATA MARK	470	MK DATA	These codes indicate that a data cell is under the heads.
73	PREFINAL MARK	473	MK BLK END	This code indicates the next to last data word of block. The state generator switches to ST FINAL.
73	FINAL MARK	773	MK BLK END	This indicates that the last data cell has passed the heads. The state generator switches to ST CK (Checksum) to deal with the parity checksum. Then the state generator goes to IDLE.
73	PCC MARK	773	MK BLK END	The longitudinal parity checksum is stored in the PCC Mark cell. No operation occurs when MK BLK END is decoded.
73	REVERSE LOCK MARK	773	MK BLK END	No operation.
51	GUARD MARK	751	---------	No operation. This code becomes 32 when the tape is travelling in the opposite direction. In this direction, it does nothing.
45	REVERSE BLOCK MARK	545	---------	No operation.
22	FORWARD END MARK	622	MK END	An error is set to indicate that the tape is running out.

DECtape is able to read or write data in either direction of tape motion, because the control cells of each block are symmetrical about the data area. Identical control cells appear on either side of the data area; thus, the heads can approach from either direction and encounter the same control codes on the mark track. This condition occurs because the codes of the mark track on one side of a data area are the obverse complement of the codes on the other side. Obverse complement means that if a code, (e.g., 42_8) is assembled by the controller as the tape travels from left to right over the heads, then that same code (in this example) would be seen as its obverse complement (e.g., 56_8) when assembled in the reverse direction. Obverse complement assembly is illustrated in Figure 2-2.

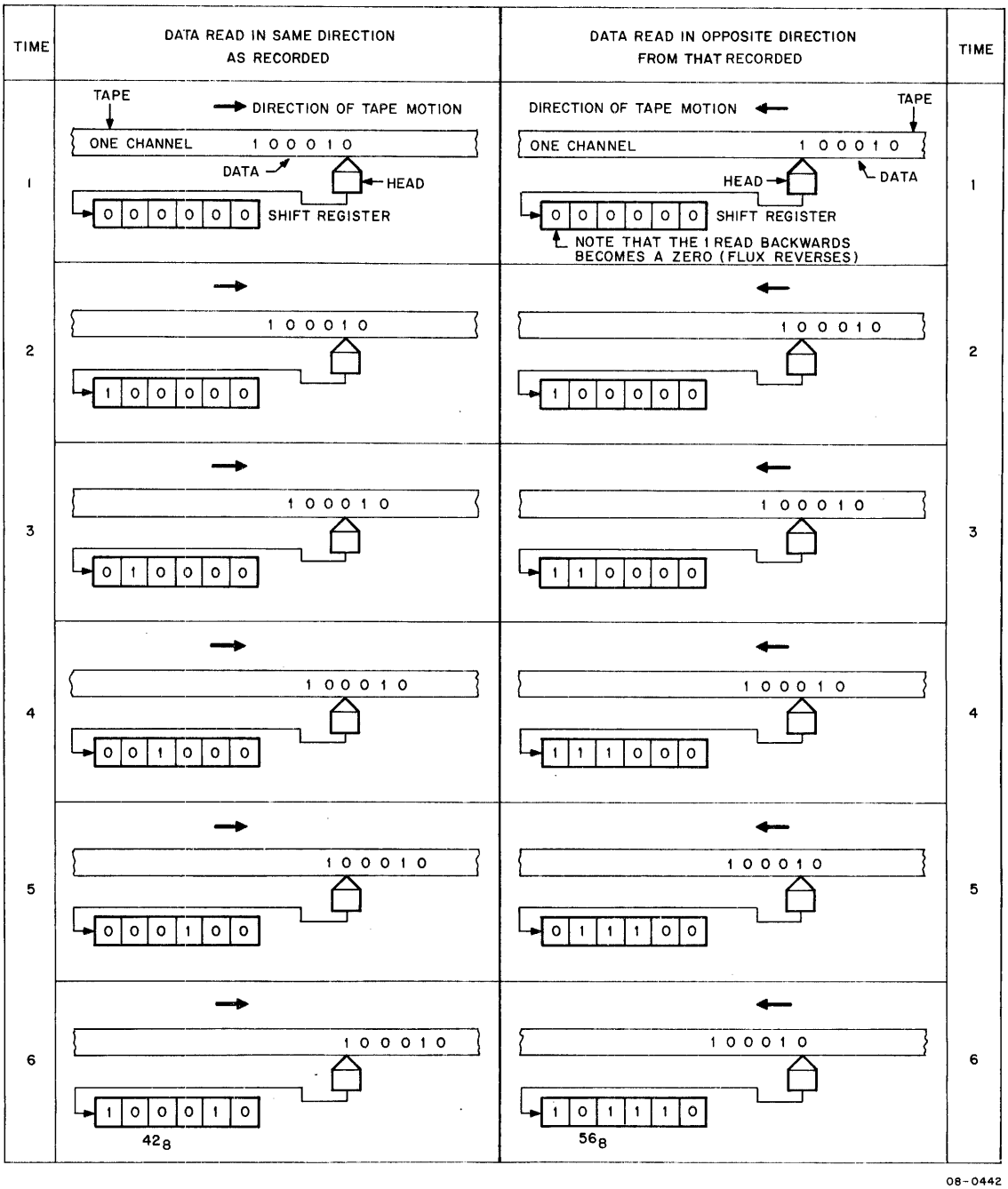

Figure 2-2 Bidirectional Reading and Writing

By placing obverse complements of control cells at either end of the block and numbers that are their own obverse complement in data areas (i.e., 70 maps to 70), a block can be made to look the same to the controller regardless of the direction it is approached from. An interesting exercise is to convert all the codes of Figure 2-6 to their obverse complement, and see how a change of direction maps the Mark Track into a mirror image of itself, with the center of the data area as the mirror.

The window register is clocked by TP01 and cleared when the up-to-speed flip-flop clears. Decoding does not begin until the last bit W01 sets, ensuring that at least nine bits have shifted in, and that the code must be valid. Decoding is performed by a series of AND and OR gates that are used to step the state generator, described in Paragraph 2.3.3.

2.3.3 State Generator

As the window register decodes the mark track instruction that identifies each cell of any block, the state generator sequences through six different states, IDLE, BLK MK, REV CK, DATA, ST FINAL, and ST CK. These states correspond to five different areas of a block plus interblock space: the approach, the block number, the checksum initialization, the data, the end of the block, and the checksum verification (refer to block schematic 6). In order for the controller to transfer data, the state generator must sequence through all six states, and is initialized when IDLE is set and all other states are cleared.

2.3.4 Data Buffer

The data buffer, which consists of three 6-bit shift registers, receives data from the three data tracks during read operations and transmits data to the same tracks during write operations (refer to block schematics 9 through 14). For a read operation, data from the data tracks is transferred to data buffer bits 15, 16 and 17. The data is then transferred to the DECtape buffer when full for a write operation, the data buffer is loaded with 18-bits from the DECtape buffer. Bits are shifted out of bits 0, 1, and 2 of the data buffer in bytes of three and are applied to the read/write heads via the read/write amplifiers.

2.3.5 Record and Replay Logic

Figure 2-3 shows a simplified version of the logic used by DECtape to write and read data. The recording technique is called phase modulation and is implemented as follows. Assume data buffer bits 00 and 03 have been loaded from the DECtape buffer at TP1 (refer to Figure 2-4). The TP1 pulse occurs at the same frequency but 90 degrees out of phase with TP0. This pulse complements DB00, which, in turn, causes the G888 writer to write a flux reversal onto the tape (refer to block schematic 3).

On the next TP0 pulse, DB03 is shifted into DB00. The following TP1 again complements DB00 to force another flux reversal onto the tape. Note that the direction of the flux reversal is determined by TP0 forcing a 0 or a 1 into DB00.

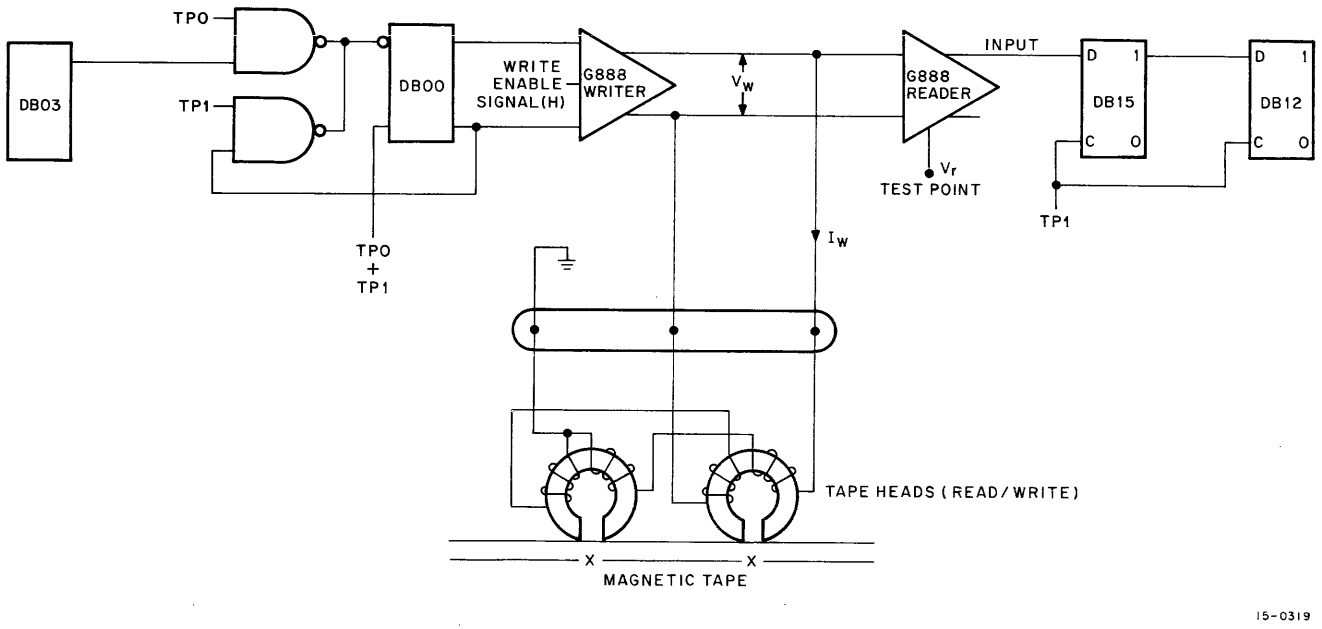

Figure 2-3 Record and Replay Logic

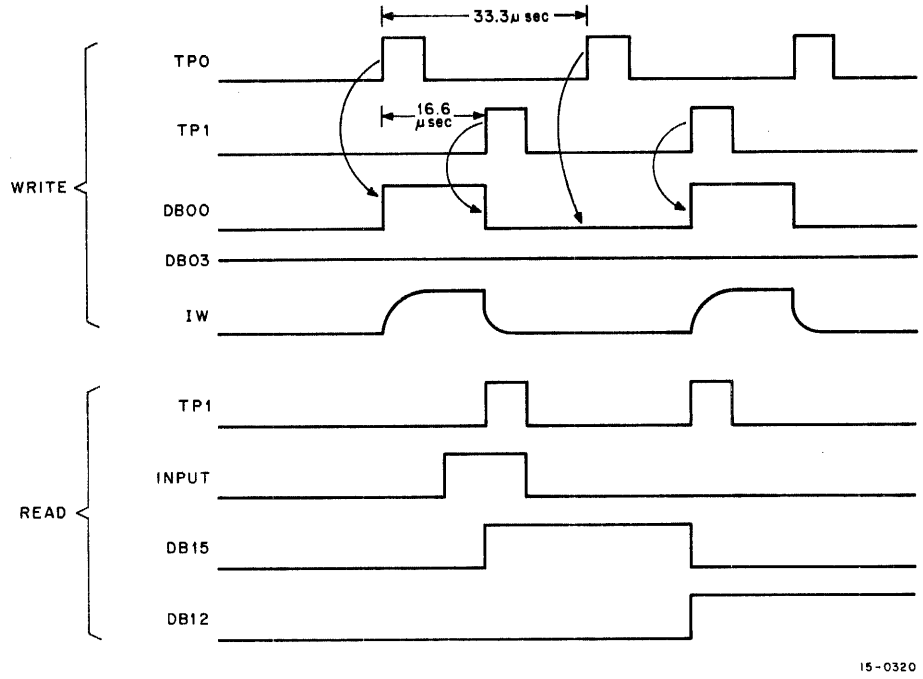

Figure 2-4 Record and Replay Timing Diagram

During read, DB15 samples the output of the G888 reader at TP1 time. If a 1 has been written at that point, then the flux reversal will be seen by the reader as 1, and a 1 will be clocked into DB15. If the flux reversal was for a 0, then the DB15 will not be set to a 1. On the next TP1 clock, the contents of DB15 are shifted to DB12, and the next bit is sampled by DB15.

The G888 reader/writer is described in detail in the PDP-15 Module Manual. Specifications for the read/write heads are available in the applicable DECtape transport maintenance manual.

2.3.6 DECtape Buffer

The DECtape buffer (refer to block schematics 9 through 14) is an intermediate 18-bit storage register for data transfers between the data buffer and memory. During a read operation, the data buffer accumulates an 18-bit word and immediately transfers it to the DECtape buffer for eventual transfer to memory. During a write operation, the data word is transferred to the DECtape buffer, and at the correct moment, into the data buffer for writing. The transfer control is straightforward and is described in Paragraph 2.4

2.3.7 Longitudinal Parity Buffer

The longitudinal parity buffer (LPB) (refer to block schematics 13 and 14) calculates a longitudinal parity checksum on the three data tracks during any block transfer. For example, in a write operation, at the beginning of the block, during the ST REV CK state, the LPB register is initialized to 0. As each 6-bit byte is assembled into the data buffer or onto the tape, the longitudinal parity buffer calculates the checksum. Alternate bits of the buffer complement when the input is a logic 0. At the end

of the block, during writing, this checksum is deposited in the PCC MARK during the ST CK state. On reading, this same checksum is repeated, except the final calculated sum is considered a data word by the LPB. If the new calculation is equal to the old, then the final result in the LPB must be all 1s. The hardware checks for this in state ST CK. If the answer is not all 1s, then a parity error is generated.

The LPB can be considered as a 6-bit register that alternately examines the incoming 3-bit bytes and complements each bit that sees a logic 0. The LPB is fed from the data buffer during read and write and, in turn, feeds bits 0, 1, 2, 3, 4, and 5 of the DECtape Buffer when the checksum is to be written onto the tape at the end of the block during write.

2.3.8 I/O Control Logic

The I/O control logic performs two functions: it requests processor API or PI breaks, and it requests and executes multi-cycle data channel transfers (refer to Figure 2-5). The DECtape flag sets the API or PI request to appropriate control logic. The data flag performs the same function to cause the data channel control logic to start transfers. The actual functions that set these two flags are the most complex part of the operation. The input gates that enable and/or strobe these flags are shown in block schematic 7. Block schematic 3 shows additional I/O control. An analysis of each input is given in Tables 2-4, 2-5, and 2-6. The information presented in these tables provides a better understanding of the functions summarized in Table 1-8.

A detailed description of the I/O control logic is provided in the PDP-15 Interface Manual. A flag sets the request to an M104 (PDP-15) module, which sets the appropriate signal, waits for grant, and generates the needed address.

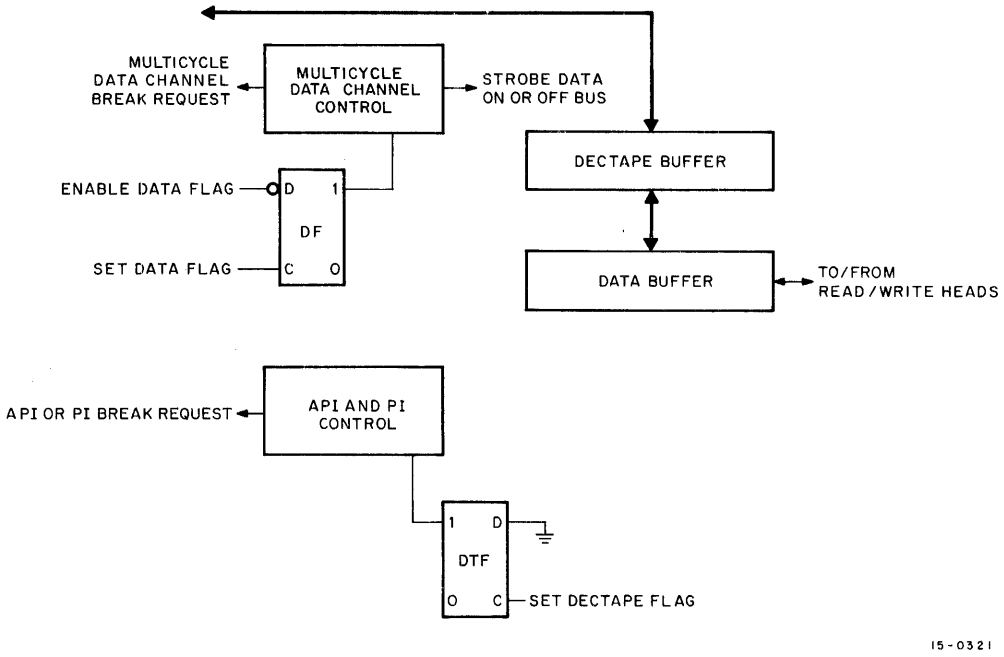

Figure 2-5 The I/O Control Logic

Table 2-4
DECtape Flag Input Functions

Inputs	Gate	Input Signal Description
TC02 WC0 H TC02 DCH ENB H TC02 FR00 (1) H TC04 WRTM+FR03 H	AND	Word count overflow pulse from computer. Indicates a data channel transfer is in progress. Continuous Mode. Write Timing and Mark Track, Search, Read All, Write All.
TC04 WRTM+FR03H TC04 FR00 (0) H TC02 DCH CLR DF H	AND	Search Write Timing and Mark, Read All, Write All. Normal Mode. From DCH Grant acknowledging the Data channel request.
TC04 RD+WD H TC04 FR00 (0) H TC07 ST CK (0) P H	AND	Read Data or Write Data Operations. Normal Mode. Set after the last word of the block has been transferred.
TC04 RD+WD H TC04 FR00 (1) H TC03 WC (0) H TC07 ST CK (0) P H	AND	Read Data or Write Data Operations. Continuous Mode. WC overflow from computer. Set after the last word of the block has been transferred.

Table 2-5
Data Flag Input Functions

Inputs	Gate	Input Signal Description
-TC04 WRITE DATA H TC04 FR01 (1) H	AND	Every function except Write Data. Write Timing and Mark, Write Data, Write All.
TC04 WRITE DATA H TC07 MBS+MD H	AND	Write Data function. MK BLK START or MK DATA, which set the DF to request a word from the computer.
TC04 SEARCH H TC07 BLK IN SYNC H	AND	Search function. Point where the block number is assembled into the buffer and ready for transfer.
TC04 READ DATA H TC07 WD EN H	AND	Read Data function. The OR of DATA, ST FINAL and ST CK, which is the total data area of a block.
READ ALL H	INVERT	Read All function.

Table 2-6
Data Flag Clock Functions

Inputs	Gate	Input Signal Description
TC05 TP0 H TC07 WRITE ALL H TC05 MC00 (0) H TC05 MC01 (1) H	AND	Timing Pulse. Write All function. Counter 0 on a 0. Counter 1 on a 1.
TC05 MC00 (1) H TC05 MC01 (0) H -TC04 WRITE ALL H TC05 TP0 H	AND	Counter 0 on a 1 occurs at beginning Counter 1 on a 0 of each word. All functions except Write All. Timing Pulse 0.

2.4 FUNCTIONAL DESCRIPTION

In the following paragraphs, the Read Data and Write Data functions are described in detail. The descriptions are supported with simplified block schematics and a detailed timing diagram. Each step in an operation is numbered, and each number corresponds to a specific section of logic on the related block schematic.

2.4.1 Write Data Functions

Refer to Figure 2-6, Tables 2-4, 2-5, and 2-6 and the block schematics provided in the engineering drawings.

Step	Procedure
1	The DF is set when the block hits TC06 MK BLK START code. TP0 clocks the flag. A multi-cycle data channel break from memory to the controller begins. (See interface manual for details.)
2	When DCH ENB and IOP-4 occur during the break, the signal TC03 BUS TO DTB H is generated, and the contents of the memory bus (an 18-bit word) are jammed into the DECtape Buffer.
3	Just before the first data cell appears under the heads, the DECtape buffer is jammed into the data buffer with the signal TC07 XFER EN H.
4	Simultaneously with 3, the WR EN flip-flop is set, and the write amplifiers to the heads are enabled.
5	TP0 and TP1 perform the write operation from the data buffer onto the tape following the technique described in Paragraph 2.3.5.
6	At the end of the block, in normal mode, the DECtape flag is always set to inform the processor that a complete block has been written. In the continuous mode of operation, the DECtape flag does not set until the end of the block in which word count overflow occurs. This allows the programmer to write several blocks without having to re-initiate the Word Count and Current Address locations for each block.

2.4.2 Read Data Functions

Refer to Figure 2-7, Tables 2-4, 2-5, and 2-6, and the block schematics.

Step	Procedure
1	The Data flag is enabled as soon as the DATA state appears. The first data word is assembled in bytes of three into the data buffer, using the techniques described in Paragraph 2.3.5.
2	The Data flag is set when the end of the first cell occurs. When it sets, indicating that the word has been completely assembled into the data buffer, it generates the signal TC07 DB TO DTB H, which jams the contents of the Data Buffer into the DECtape Buffer. At the same time, the DF requests a multi-cycle data break into computer memory.
3	During this break, when DCH ENB and IOP 2 occur, the signal TC03 DTB TO BUS H is generated, which places the contents of the DECtape Buffer onto the I/O bus, and from there it goes to the I/O Processor into memory.
4	At the end of the block in normal mode, the DECtape flag is always set, indicating to the central processor that a new block must be set up. If this were a continuous mode operation, the DECtape flag would be set at the end of the block, provided the word counter had overflowed.

2.4.3 Search Functions

Refer to Tables 2-4, 2-5, and 2-6, and to the block schematics.

During SEARCH, the Data flag is set every time the signal TC07 BLK IN SYNC H is high at the beginning of the cell which holds the block number. The rest of the sequence is identical to a Read operation. The number is transferred to the DECtape buffer, a multi-cycle DCH break request is initiated, and the number is transferred to the specified memory location. The current address is not incremented. In normal mode, the DECtape flag is set during the data channel break, and in continuous mode, during the data channel break after the word counter has overflowed.

2.4.4 Write Timing and Mark Track Functions

Refer to Figure 2-1, Tables 2-4, 2-5, and 2-6 and the block schematics.

The DECtape flag is set during Write Timing and Mark at the same times as it is set during Write All; this is also true for the Data flag. The primary difference between Write Timing and Mark Track and Write All is that the former writes on the mark track only from bits 0, 3, 6, 9, 12, and 15 of the data buffer rather than across three data tracks. The timing pulses during this operation come from the clock of the TP Generator logic (refer to Paragraph 2.3.1) rather than from pre-recorded timing tracks. The codes that are loaded into the data buffer for writing the mark track are listed in Table 2-3. A program called the DECtape Format Generator is available to perform this function. The program explains in detail how each block is recorded.

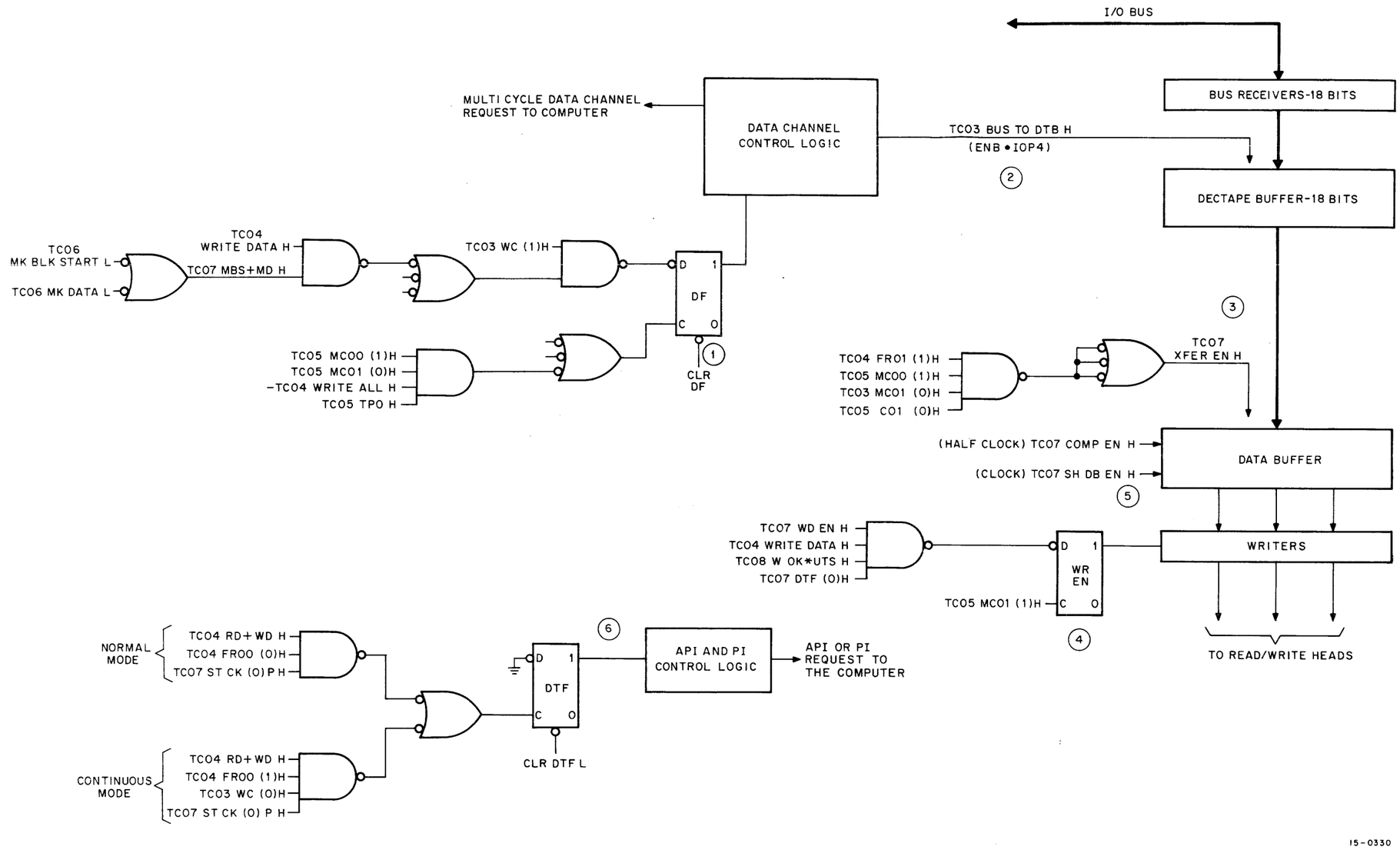

Figure 2-6 Simplified Schematic of Write Operation

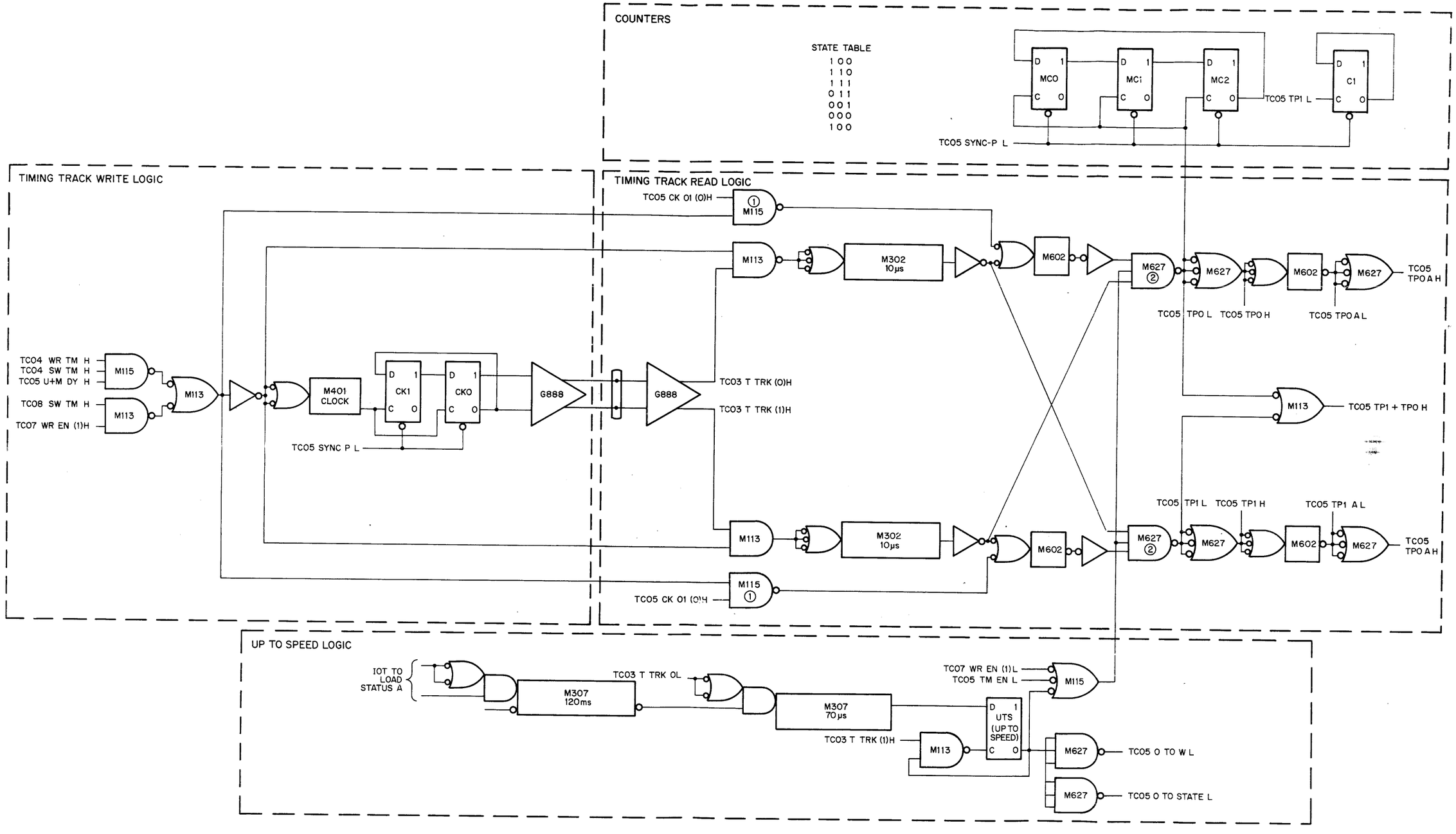

Figure 2-7 Simplified Schematic of Read Operation

2.4.5 Write All Functions

Refer to Tables 2-4, 2-5, and 2-6, and the block schematics.

The Write All Functions operation allows the program to write anywhere on the data tracks of the tape, regardless of what cell it is in. This operation is used to write the block numbers onto the tape during formatting. The primary difference between Write All and Write Data is in the time that the Data and DECtape flags are set. The Data flag is set after 6 bits have passed the read heads, indicating 18 bits could have been read or written. The DECtape flag is set every time the Data flag is set during normal mode, and only after the word counter has overflowed and the Data flag is set during continuous mode.

2.4.6 Read All Functions

Refer to Tables 2-4, 2-5, and 2-6, and the block schematics. Read All is similar to Write All, except that the data flow is reversed. Data is read from any area on the tape, whether it is in a data cell or not.

2.4.7 Move Functions

The Move operation's function is to post an error flag if the selected transport enters the end zone. It is used to wind or rewind a tape transport.

CHAPTER 3
INSTALLATION

Refer to the PDP-15 Installation Manual, DEC-15-H2AB-D, for site preparation instructions.

3.1 UNPACKING AND INSTALLATION

The equipment may arrive either as a complete system with controller, DECtape transports, and power supplies mounted in their appropriate cabinet, or as an add-on where only DECtape transports are shipped and must be mounted in cabinets already available at the site.

3.1.1 Cabinet Unpacking

If the equipment arrives in cabinets, perform the following steps to unpack and position.

Step	Procedure
1	Remove the outer shipping container, which may be either heavy, corrugated cardboard or plywood. Remove all straps first, and then any fasteners and cleats securing the container to the skid. Remove any wood framing and supports.
2	Remove the polyethylene covers from all cabinets.
3	Remove the tape or plastic shipping pins from the rear access doors.
4	Unbolt the cabinets from their shipping skids. The bolts can be reached through the rear doors.
5	Raise the leveling feet so that they are above the level of the roll-around castors.
6	Form a ramp with wooden blocks and planks from each cabinet skid to the floor, and roll each cabinet down this plank.
7	Roll the system to its proper location.

3.1.2 Cabinet Installation

The cabinets are equipped with roll-around castors and adjustable leveling feet. They do not have to be bolted to the floor. In multiple cabinet installations, cabinets are shipped either individually or in pairs. All cabinets should be connected together at the site.

Step	Procedure
1	Cabinets are joined by filler strips (see Figure 3-1). After they are positioned, butt the cabinets together and bolt both filler strips and cabinets together. Do not tighten the bolts securely for the moment.
2	Lower the leveling feet until they support the cabinet. Check that all cabinets are level with a spirit level, and the feet are firm against the floor.
3	Tighten the bolts that hold the cabinets together and check the leveling again.
4	Remove the shipping bolts and tape from the slide runners of each DECtape transport.
5	Connect a ground strap between any free-standing cabinets and the PDP-15 cabinet.

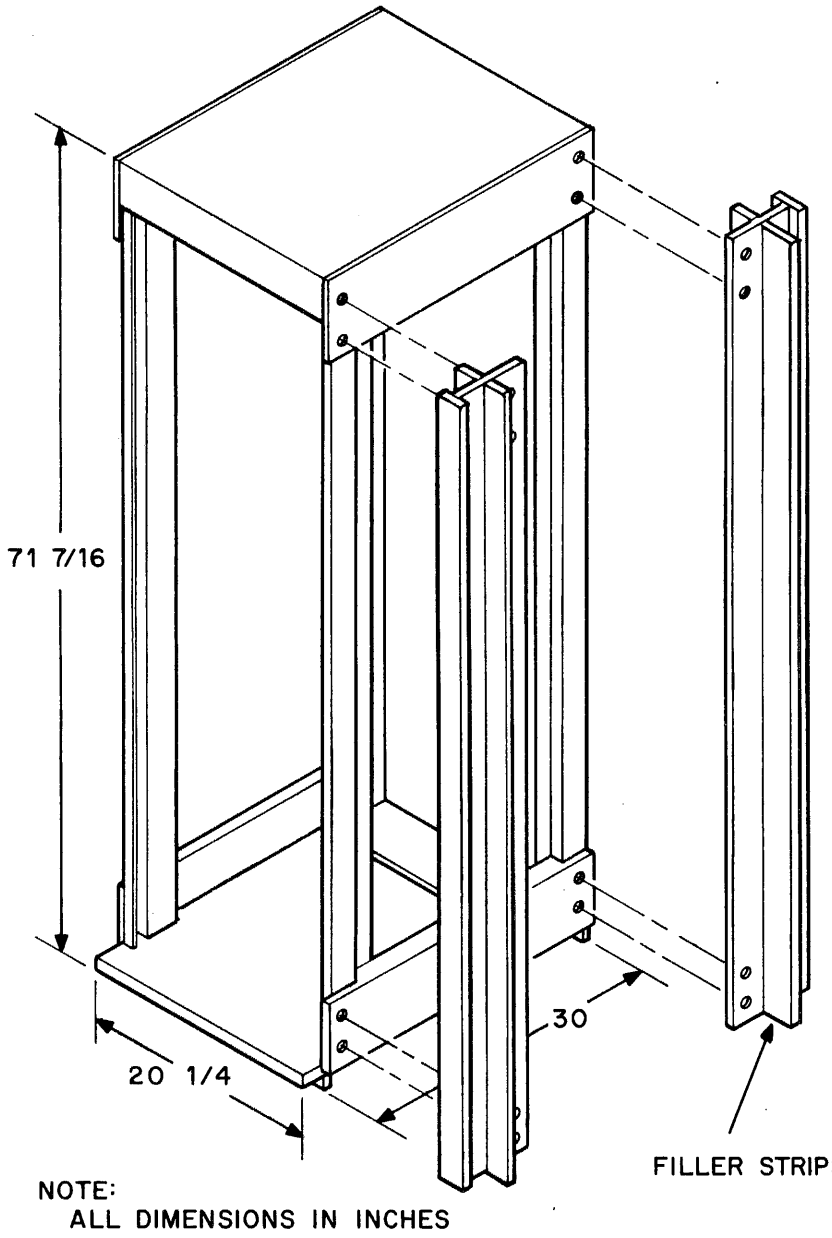

Figure 3-1 Cabinet Bolting Diagram

3.1.3 TC15 DECtape Control Installation

The controller is always shipped mounted in a cabinet with at least one DECtape transport. Install the TC15 as follows:

Step	Procedure
1	Remove any tape from the modules and check that existing wiring is good, the hold-down bars are in place, and that no modules have fallen out.
2	Install the I/O bus cables as indicated in Figure 3-2, and Table 3-1.
3	Connect the ac remote turn-on cable between the computer and the 841B Power Control unit on the left side of the cabinet (see Figure 3-3). Be sure the circuit breaker on the power control is OFF. Use a voltmeter to check for correct line voltage. Refer to D-IC-TC15-0-19 in the engineering drawings to determine that the transformer has been properly wired. Then plug the primary power cable into the line voltage.

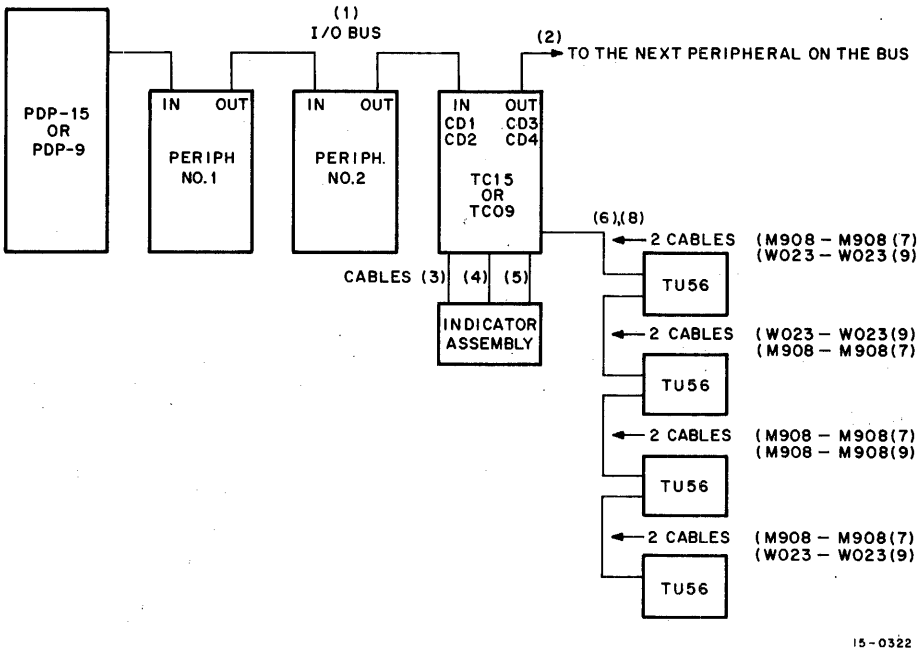

Figure 3-2 DECtape Cables

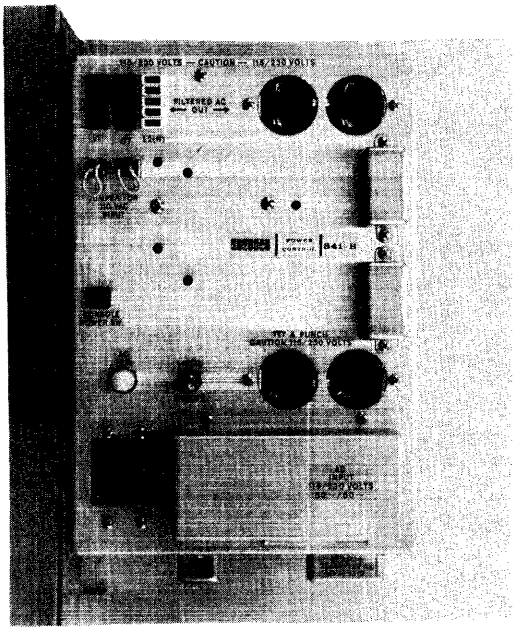

Figure 3-3 841B Power Control

Table 3-1
DECtape Cabling

Cable No.	Type of Cable	From		To	
		Equipment	Cable Slot	Equipment	Cable Slot
1	BC09B	PDP-15*	M02,N02:M03,N03	TC15	C01,D01:C02,D02
2	BC09B	TC15	C03,D03:C04,D04	Next Peripheral	
3	Indicator	TC15	C22	Indicator Panel	Hard-Wired
4	Indicator	TC15	C23	Indicator Panel	Hard-Wired
5	Indicator	TC15	C24	Indicator Panel	Hard-Wired
6	Control Cable	TU56	A27	TU56	A06
7	Control Cable	TU56	A07	TU56	A06
8	Signal Cable	TC15	A21, B21	TU56	A10, B10
9	Signal Cable	TU56	A11, B11	TU56	A10, B10

*For cabling positive logic devices on the PDP-9. Refer to Paragraph 6.4 in the PDP-15 Interface Manual.

3.1.4 TU56 Dual DECtape Transport

Complete installation instructions for the TU56 are given in the TU56 Maintenance Manual.

3.2 POWER-UP SEQUENCE

Before starting the power-up sequence, check all wiring, test the primary ac power for the correct voltage, and verify the positions of all relevant controls. Apply power to the system in the following sequence:

Step	Procedure
1	Turn off the 841B Power Control circuit breaker and all power switches on the transports. Turn the REMOTE switch to OFF. Plug in the 841B power cord and turn on the circuit breaker.
2	Turn the POWER switch of the first TU56 to ON.
3	Check that the transport winds and rewinds, and the blower is operating. If any unusual noises are heard, turn off the transport immediately and notify the local office that depot repair is necessary.
4	Repeat this sequence for each transport. Do not apply power to all transports simultaneously or the surge current may trigger the circuit breaker.
5	Turn the LOCAL/REMOTE switch on the 841B to the REMOTE position.

3.3 ACCEPTANCE PROCEDURE

3.3.1 Acceptance Forms

After the system is properly installed, it is demonstrated to the customer by running diagnostics and the system software. There are three forms contained in the accessory kit in a large envelope that are used during the acceptance procedure.

3.3.1.1 Customer Acceptance Form - Record any exceptions from the norm found in the system during the acceptance procedure on the Customer Acceptance Form. Include such items as missing parts, manuals or engineering drawings.

3.3.1.2 Software Check List - The Software Check List indicates all software that is normally supplied with the system.

3.3.1.3 Accessory Check List - The Accessory Check List indicates all of the hardware items normally supplied with the system. Each should be checked off with the customer.

3.3.2 Diagnostics

There are two diagnostics that test the DECtape system:

a. DECtape Random Exerciser, which exercises the different functions by randomly selecting the function, direction, transport number, number of blocks, and data pattern generation.

b. DECtape Basic Exerciser, which consists of several basic test routines that can be individually selected for troubleshooting or to acquire confidence in the equipment.

Each is available with a complete description from the DEC program library.

3.3.3 System Software

The system is run using the checkout procedure in the Advanced Software System Checkout Package For Bulk Storage Systems. This package includes a complete set of advanced software manuals, a DECtape monitor, and peripheral routines for bulk storage on DECtape.

The successful demonstration of both the diagnostics and the system software constitutes the acceptance procedure. Any discrepancies must be listed in the Customer Acceptance Form.

3.4 SHIPPING A DECtape SYSTEM

If a DECtape System is to be shipped from one point to another, together or in parts, it should be prepared and packed according to DEC instructions.

CHAPTER 4
MAINTENANCE

This chapter contains preventive maintenance instructions, adjustment procedures, and diagnostics.

4.1 PREVENTIVE MAINTENANCE

Preventive maintenance involves visual inspection of the system according to the list in Table 4-1, and adherence to the practices listed below.

4.1.1 Handling DECtape

When tape is handled (during splicing), the operator's hands should be clean to prevent contamination of the tape by body oils and salts. The use of sticky masking tape or celluloid tape as splicing or tail-end hold-down is not recommended, because small deposits of the adhesive will stick to the tape.

Clean heads and guides regularly to remove accumulations of foreign matter.

4.1.2 Cleaning DECtape Reels

If the tape is contaminated by dust, carefully wipe the surface and backing of the tape with a lint-free cloth, such as a soft chamois. Contamination that does not brush off easily can be washed off with a cloth slightly moistened with Freon TF.

WARNING

Aliphatic hydrocarbon-type solvents (heptane, gasoline, naphtha) can also be used, but care should be exercised because they are flammable.

CAUTION

Do not use carbon tetrachloride, ethyl alcohol, trichlorethylene, or other unknown cleaning agents, because they may soften the oxide, deform the backing, or both.

4.1.3 Storing Tapes

The best method of storage is to place the reel of tape in a self-sealing plastic case supplied for this purpose by DEC and store it on edge in a storage bin equipped with partitions between each two reels. The plastic case protects tape from dust and sudden changes in humidity and temperature. It also guards both tape and reel from damage in handling when the tape is transported between work and storage areas.

If the tape must be stored in the presence of magnetic fields, produced by ac or dc, special containers are available that will protect the data from erasure in all but extremely high fields. Isolate tape storage locations from such fields, if at all possible.

Avoid extremes of temperature and humidity. In general, recommended storage conditions are:

Relative humidity: 40 to 60%
Temperature: 60 to 80°F

When extremes in temperature are encountered during storage or transit, tape should be brought to equilibrium before it is used.

Table 4-1
Visual Inspection Checklist

Item	Check
Mechanical Connections	a. Check that all screws are tight and that all mechanical assemblies are secure.
	b. Check that all crimped lugs are secure and that all lugs are properly inserted in their mating connectors.
Wiring and Cables	a. Check all wiring and cables for breaks, cuts, frayed leads or missing lugs. Check wire wraps for broken or missing pins.
	b. Check that no wire or cables are strained in their normal positions or have severe kinks. Check that cables do not interfere with doors and that they do not chafe when doors are opened and closed.
Air Filters	Check all airfilters for cleanliness and for normal air movements through cabinets.
Modules and Components	Check that all modules are properly seated. Look for areas of discoloration on all exposed surfaces. Check all exposed capacitors for signs of discoloration or leakage, or corrosion. Check power supply capacitors for bulges.
Indicators and Switches	Check all indicators and switches for tightness. Check for cracks, discoloration or other visual defects.

4.1.4 Physical Distortion

Most signal dropouts in digital recordings are caused by specks of dust and other contaminants that lift the tape away from the head. However, two other significant causes are dents and creases in the base material. Dents are caused by particles wound up tightly in the roll or by roughness in the surface of the hub on which the tape is wound. These may cause permanent dents or creases in many layers of the tape that cannot be stretched out flat as the tape passes over the head. Stresses in the roll, which stretch the backing 5 percent, will usually leave a permanent impression. Stresses below the 5 percent level are usually not permanent. Creases are caused by handling the tape (i.e., threading, splicing, removing the tape from the guides, etc.) or by damage to the edges of the tape caused by uneven winding.

4.1.5 Accidental Erasure or Saturation

The magnetic properties of instrumentation tapes are extremely stable. The magnetic retention is permanent unless altered by magnetic fields, such as those generated by permanent magnets or electromagnets. These will probably cause partial erasure if placed within a few inches of the tape.

Both unrecorded and recorded tapes should be kept away from electromagnetic bulk erasures and storage cabinets with magnetic latches. Unrecorded tapes should not be placed near dc magnetic fields, such as traveling-wave tubes or magnetron magnets, because they may become heavily biased or even create gross distortion in the record process (i.e., the resultant signal-to-noise ratio will be reduced).

4.1.6 Head Care and Head Life

The following factors must be considered when maintaining tape heads.

a. Cleanliness of tapes, the transport, and their environment.
b. Maintenance procedures that involve the checking of tape tension, tracking, etc.
c. The abrasiveness of the tape being used.
d. Solvents used for cleaning the heads.

Cleanliness in and around the head area is important in all tape machines. Dirt particles become a serious threat to the data "take", because they cause spacing loss. Particles can also become minute scrapers, gougers, and cutters to the head and tape surfaces when dragged between them.

Care must be taken not to touch the heads with any metallic or hard object to avoid scratching, gouging, or magnetizing the heads. For cleaning the heads, use only alcohol, naphtha, Freon TF, or gasoline. Freon TF is the best all-around cleaner. Note that most head cleaners will also dissolve lubricating greases and tape binders and should be used carefully, especially around bearings and the tape. Cotton swabs make good disposable cleaning tools.

4.2 DECtape CONTROL CHECKS AND ADJUSTMENTS

4.2.1 Test Equipment and Materials Required

The following is a list of test equipment and materials:

a. Oscilloscope, Tektronix Type 453, or equivalent.

b. Diagnostic programs supplied with TC15.

c. PDP-15 (or PDP-9) with TU56, or TU55, and tapes.

d. Engineering drawings (Refer to Chapter 5).

4.2.2 XSTA Delay Adjustment

NOTE

Do not attempt to adjust the potentiometers on the G888 module. These are adjusted at the factory.

a. Manually load the following program from the console:

Address	Octal Code	Instruction
000000	750004	Load AC from switches
000001	707545	Load Status A
000002	600000	Jump to 0

b. Connect oscilloscope to measure delay output of delay 2 on the M302 module at D18. Pin T2 at D18 is the output.

Adjust the bottom potentiometer on the M302 module so that the XSTA signal has a positive duration of 5 μs.

c. Connect oscilloscope to measure BXSTA delay at D18F2. Adjust top potentiometer for a positive duration of 100 ns.

4.2.3 Status A Register Check

a. Place all console data switches to 1.

b. Observe that all Status A register bits are 1.

4.2.4 Unit Select and Tape Motion Checks

a. Set data switches 0, 1, and 2 to select a DECtape transport. Unit assignments are listed in Table 1-3.

b. Set data switches 3 and 4 to select tape motion and direction. Motion register bit assignments are listed in Table 1-3.

c. Observe that proper tape motion occurs for each combination of Motion register bits that are selected.

4.2.5 M401 Clock Adjustment

Manually load the following program from the console data switches:

Address	Octal Code	Instruction
000000	750004	Load AC from switches
000001	707541	Clear Status A
000002	707544	XOR Status A
000003	140030	DZM 30
000004	140031	DZM 31
000005	600003	Jump To 3

a. Remove tape from DECtape transport and place the transport on-line and write enabled.

b. Turn the WRTM/NORMAL switch to WRTM.

c. Set console data switches 4, 5, 6, and 7 to 1.

d. Press I/O RESET and START. A WRTM function is initiated on DECtape transport 8 and the clock starts.

e. Connect the oscilloscope to measure the clock output at pin D2, location C17.

f. Adjust the potentiometer on the M401 module at C17 to obtain a pulse repetition rate of 8.33 μs.

4.2.6 Unit or Motion Delay Adjustment

a. Load the DECtape Basic Exerciser program (Part I) and run Test 0 to cause the tape to rock.

b. Connect the oscilloscope to measure the U + M DY signal delay at pin K1, location A19.

c. Adjust the upper potentiometer on the M307 module at location A19 to obtain a positive signal with a pulse duration of 140 ms.

4.2.7 Rate Delay Adjustment

Perform this adjustment under the same conditions specified in Paragraph 4.2.6.

a. Connect oscilloscope to measure rate delay at pin H2, location A19.

b. Adjust the lower potentiometer on the M307 module at location A19 to obtain a positive signal with a pulse duration of 70 μs.

4.2.8 Cross Talk Delays

Perform these adjustments under the same conditions specified in Paragraph 4.2.6.

a. Connect the oscilloscope to measure the TP0 XTLK delay at pin F2, location D12.

(continued on next page)

b. Adjust the upper potentiometer on the M302 module at location D12 to obtain a positive signal with a pulse duration of 10 μs.

c. Connect the oscilloscope to measure the TP1 XTLK delay at pin T2, location D12.

d. Adjust the lower potentiometer on the M302 module at location D12 to obtain a positive signal with a pulse duration of 10 μs.

4.3 DIAGNOSTICS

There are two diagnostic tests for a DECtape system with from one to eight transports. These tests are available from the program library along with listings and complete descriptions.

4.3.1 DECtape Random Exerciser

The DECtape Random Exerciser exercises the different functions by randomly selecting a function, direction, transport number, number of blocks, and data pattern generation.

4.3.2 DECtape Basic Exerciser

The DECtape Basic Exerciser consists of a group of basic tests that can be individually selected for troubleshooting or testing and adjustment procedures.

The DECtape Basic Exerciser test programs are arranged in a logical sequence, starting with basic search, read/write data, and parity tests. Follow this sequence and be sure that all tests operate correctly. When the tests are performed in the proper sequence, a minimum amount of time will be spent in checkout.

4.4 TROUBLESHOOTING

4.4.1 TC15 Maintenance Concept

Two rules must be followed if the TC15 is to be properly maintained:

a. Carry out the preventive maintenance routines regularly. Unless cables, wiring, panels, and modules are regularly checked for mechanical problems, and unless the heads are free of dirt and the tape is properly handled, even the most reliable tape system will fail.

b. Always perform a complete checkup on the equipment after troubleshooting and correcting a particular fault.

A DECtape system must be completely tested during any troubleshooting, because the system is so reliable that a marginal fault may not be detected until a primary fault is corrected. Checking all parts of the system may reveal marginal problems that can be repaired immediately. Unless a thorough

examination is performed, these faults may occur shortly thereafter, needlessly shortening the mean time between failures on the system.

4.4.2 General Troubleshooting

Begin with a thorough check of the most obvious problems; whether the power is on, all cables properly connected, all modules plugged in, and all switches, dials, lights, etc., in their proper state.

The next step is to define the problem, which involves locating it. Is the computer, the DECtape, or the DECtape transport at fault? Can any one or all be replaced with working equivalents? Usually a system has more than one transport, so that the responsibility of that unit is easily defined. If the computer is failing, the fault will usually affect other peripherals.

When the problems have been located in the controller, a similar procedure should be used to locate the subsystem within the unit (the module) that is at fault. One approach is to record a series of relevant inputs and outputs; then, using the block schematics and the functional descriptions, try to correlate the various symptoms with a possible cause. This method usually leads to speculation, more tests, and a solution.

When the fault is located and corrected, the controller should be given a complete examination. All diagnostics should be run, and all delays and the clock properly set up.

The key to efficient troubleshooting is a thorough knowledge of the machine and of the diagnostics that test it. The diagnostics are described in their respective publications.

4.4.3 Troubleshooting the Mark Track Decoder

The mark track decoder (contained within the M228 module) is the most important single subsystem within the TC15 controller.

a. If the controller is capable of performing a search, the following procedure can be used to locate the possible cause of the fault:

Step	Procedure
1	Load the basic exerciser into the computer.
2	Have the exerciser rock the tape in search mode.
3	Check the output of the mark track reader.
4	Check each window flip-flop to determine if all are being set. This can be done by examining the indicator panel or scoping each bit.

(continued on next page)

Step	Procedure
5	Scope each mark track code. Compare the number of times the code appears against the format.
6	The timing pulses are also critical inputs to the mark track decoder. Thoroughly check the timing circuitry.

b. If the controller cannot search properly, check the following areas of possible fault:

(1) Are the Data flag and the DECtape flag being set properly?

(2) Is the +1 - CA INH operating during search?

(3) Is the TC15 reacting properly to data channel transfers from the computer?

(4) Is the computer responding properly to the data channel request?

CHAPTER 5
TC15 ENGINEERING DRAWINGS

Volume 2 of this manual contains the engineering drawings for the TC15. These drawings are under DEC revision control and are updated as required by ECOs (Engineering Change Orders).

5.1 DRAWING CODES

Digital Equipment Corporation's engineering drawings are coded to designate drawing type, major assembly, and series. A drawing number such as D-BS-TC15-0-01 contains the following information:

D	Size
BS	Type (Block Schematic)
TC15	Equipment designation
0	Manufacturing variation
01	The drawing number of a series

The drawing type codes are designated as follows:

AD	Assembly drawing
BS	Block schematic
DI	Drawing index
IC	Interconnecting cabling
MU	Module utilization drawing
PL	Parts list
TD	Timing diagram

5.2 DRAWING NUMBER INDEX

Table 5-1 is an index to the engineering drawings.

Table 5-1
Drawing Number Index

Size	Type	Number	Title	Page
D	AD	7006701-0-0	Wired Ass'y (TC15)	5-3
D	DI	TC15-0-01	Dwg Index TC15	5-5
D	BS	TC15-0-02	I/O Bus Receivers	5-7
D	BS	TC15-0-03	I/O Control and R/W Amps	5-9
D	BS	TC15-0-04	Status Register A	5-11
D	BS	TC15-0-05	TP Gen	5-13
D	BS	TC15-0-06	Mark Track Decode	5-15
D	BS	TC15-0-07	Control	5-17
D	BS	TC15-0-08	Errors	5-19
D	BS	TC15-0-09	DB00-02 DTB00-02	5-21
D	BS	TC15-0-10	DB 3-5 DTB 3-5	5-23
D	BS	TC15-0-11	DB 6-8 DTB 6-8	5-25
D	BS	TC15-0-12	DB 09-11 DTB 09-11	5-27
D	BS	TC15-0-13	DB 12-14 DTB 12-14	5-29
D	BS	TC15-0-14	DB 15-17 DTB 15-17	5-31
D	BS	TC15-0-15	Bus Drivers	5-33
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D	MU	TC15-0-17	Rev A Module Utilization	5-37
D	IC	TC15-0-19	AC/DC PWR Wiring TC15	5-39
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