CONNER
PERIPHERALS™

CP-3104
TECHNICAL MANUAL

THE INSIGHT AND THE DRIVE.

CONNER PERIPHERALS, INC.

CP3104

PRODUCT MANUAL

REVISION 1
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3.3 PERFORMANCE

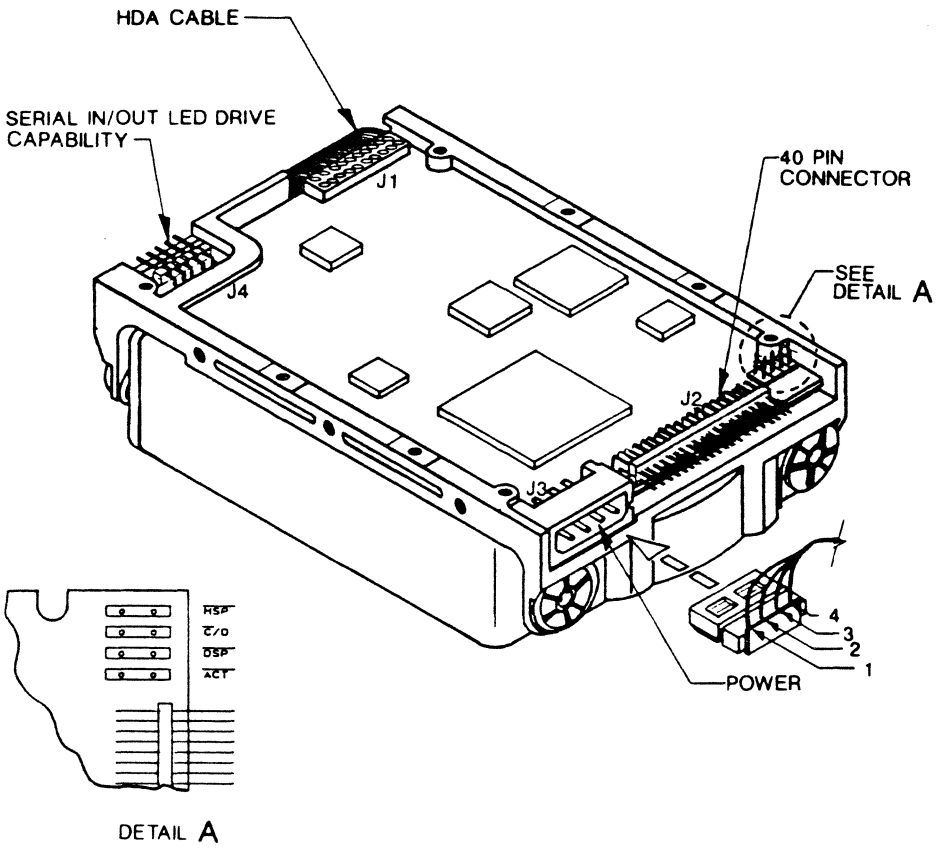
Seek Times*	Track to Track: 8 ms Average: 25 ms** Maximum: 45 ms
Average Latency	8.4 ms
Rotation Speed (± .1%)	3575 RPM
Controller Overhead	1ms
Data Transfer Rate (To /From Media)	1.25 MByte/second
Data Transfer Rate (To /From Buffer)	3.75/4.75 MByte/second
Start Time	typical: 15 seconds maximum: 20 seconds
StopTime	typical: 15 seconds maximum: 20 seconds
Interleave	1:1
Buffer Size	32KB

*At nominal D.C. input voltages.
**Average seek time is determined by dividing the total time required to seek between all possible ordered pairs of track addresses, by the total number of these ordered pairs.

3.4 READ/WRITE

Interface	Task File
Recording Method	2 of 7 RLL code
Recording Density (ID)	23,441 bits per inch
Flux Density (ID)	15,627 flux reversals per inch

Figure 1. Connector Locations



3.5 POWER REQUIREMENTS (typical)

	+12V DC ±5%	+5V DC ±5%	POWER
R/W MODE	350 ma	300 ma	5.7 W
SEEKING MODE	260 ma	180 ma	4.0 W
IDLE MODE	175 ma	160 ma	2.9 W
SPIN-UP MODE	1800 ma max (7 seconds)	180 ma	n/a

NOTES:

1) READ/WRITE mode occurs when data is being read from or written to the disk.

2) SEEKING MODE occurs while the actuator is in motion.

3) IDLE MODE occurs when the drive is not reading, writing, or seeking. The motor is up to speed and DRIVE READY condition exists. Actuator is residing on last accessed track.

4) Maximum noise allowed (DC to 1 MHZ, with equivalent resistive load): +12V DC: 1%, +5V DC: 2%.

4.0 PHYSICAL CHARACTERISTICS

Outline Dimensions	1.62" X 4.00" x 5.75" (with shock frame)
Weight	1.8 pounds

5.0 ENVIRONMENTAL CHARACTERISTICS

Temperature	
Operating	5°C to 55°C
Non Operating	-40°C to 60°C
Thermal Gradient	20°C per hour maximum

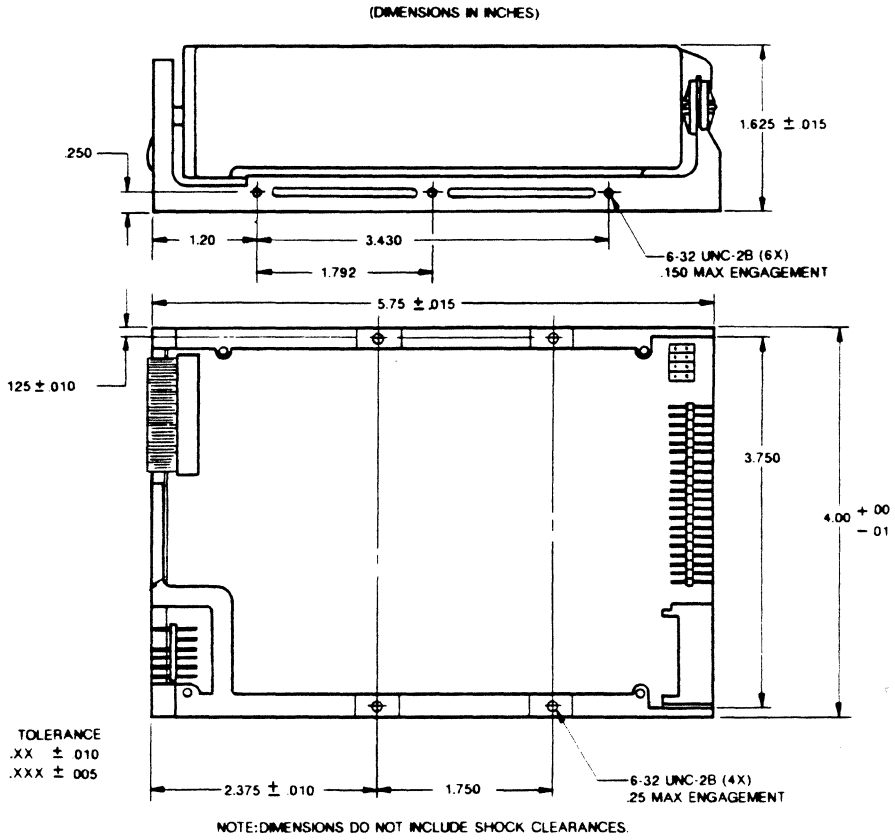
Humidity

Operating	8% to 80% non condensing
Non Operating	8% to 80% non condensing
Maximum Wet Bulb	26°C

Altitude (relative to sea level)

Operating	-200 to 10,000 feet
Non-operating (maximum)	40,000 feet

Figure 2. Mounting Configuration



5.1 RELIABILITY AND MAINTENANCE

MTBF	20,000 hours (POH)**
MTTR	10 minutes typical
Preventative Maintenance	None
Component Design Life	5 years
Data Reliability	<1 non recoverable error in 10^{12} bits read

**population is minimum of 100 units

5.2 SHOCK AND VIBRATION

Shock (1/2 sine pulse, 11 msecond duration)
Vibration (swept sine, 1 octave per minute)

Non operating shock	50 G's
Non operating vibration	
5-62 HZ	.020" (double amplitude)
63-400 HZ	4 G's (peak)
Operating shock	10 G's (without non recoverable errors)
Operating vibration	
5-22 HZ	.010" (double amplitude)
23-500 HZ	.25 G's peak (without non recoverable errors)

5.3 MAGNETIC FIELD

The externally induced magnetic flux density may not exceed 6 gauss as measured at the disk surface.

5.4 ACOUSTIC NOISE

40 dBA max. at 1 meter

5.5 SAFETY STANDARDS

The CP3104 disk drive is designed to comply with relevant product safety standards such as:

- o UL 478 Electronic Data Processing Units and Systems
- o CSA C22.2 No. 154 Data Processing Equipment
- o VDE 0804 Regulations for Telecommunications Apparatuses including Information Processing Equipment
- o IEC 435 Safety Requirements for Data Processing Equipment.

6.0 FUNCTIONAL DESCRIPTION

The CP3104 contains all necessary mechanical and electronic parts to interpret control signals, position the recording heads over the desired track, read and write data, and provide a contaminant free environment for the heads and disks.

6.1 READ/WRITE AND CONTROL ELECTRONICS

One integrated circuit is mounted within the sealed enclosure in close proximity to the read/write heads. Its function is to provide one of eight head selections, read preamplification, and write drive circuitry.

The single microprocessor controlled circuit card provides the remaining electronic functions which include:

- o Read/Write Circuitry
- o Rotary Actuator Control
- o Interface Control
- o Spin Speed Control
- o Dynamic Braking

At power down the heads are automatically retracted to the inner diameter of the disk and are latched and parked on a landing zone that is inside the data tracks.

6.2 DRIVE MECHANISM

A brushless DC direct drive motor rotates the spindle at 3575 RPM. The motor/spindle assembly is dynamically balanced to provide minimal mechanical runout to the disks. A dynamic brake is used to provide a fast stop to the spindle motor and return the heads to the landing zone when power is removed.

6.3 AIR FILTRATION SYSTEM

Within the sealed enclosure, a .3 micron filter provides a clean environment to the heads and disks.

6.4 HEAD POSITIONING MECHANISM

The eight read/write heads are supported by a mechanism coupled to the voice coil actuator.

6.5 READ/WRITE HEADS AND DISKS

Data is recorded on four 95mm diameter disks through eight 3370 type heads.

6.6 ERROR CORRECTION

The CP3104 performs internal error correction. The error correction polynomial is capable of correcting one error burst with a maximum of 8 bits per 512 byte block. The following polynomial is used:

ECC: $X^{56}+X^{52}+X^{50}+X^{43}+X^{41}+X^{34}+X^{30}+X^{26}+X^{8}+1$

CRC: $X^{16}+X^{12}+X^{5}+1$

6.7 CUSTOMER OPTIONS

There are four jumper options available for configuration, -HSP, -C/D, -DSP, and -ACT. -HSP, when jumpered connects a ground to -HOST SLV/ACT signal on the interface for those systems that require the slave drive to provide -SLAVE PRESENT signal from the slave drive to a two drive. system. -C/D is the address jumper. When jumpered, the master or C drive is selected. -DSP, when jumpered, indicates to the drive that a slave is present. In a two drive system, this jumper option must be installed in the master, or C drive. the last jumper, -ACT, connects the active signal to the -HOST SLV/ACT signal on the interface. This signal provides the capability to drive an external LED. An external current limiting resistor is required.

There is another way to connect the drive LED. J4, pins 1 and 2, provide both an open collector drive signal and a current limiting resistor connected on the other end to +5V.

The following table shows what the jumper settings should be for various system configurations.

Jumper Config.	1 drive Master	2 drive master	2 drive slave
-ACT	J	Note 1	Note 1
-C/D	J	J	NJ
-HSP	NJ	NJ	Note 2
-DSP	NJ	J	NJ

Note 1. In a two drive system, it is possible to drive one LED with both drives. An external current limiting resistor is required. The -ACT and HSP signals both connect to pin 39, -HOST SLV/ACT. They are therefore mutually exclusive.

Note 2. If the model CP3104 is connected to some drive that requires that the signal, -DRIVE SLAVE PRESENT be supplied from the slave drive via

the interface signal -HOST SLV/ACT, then this jumper must be installed. If this jumper is installed, the -ACT jumper must not be installed because the two jumpers are mutually exclusive.

7.0 ELECTRICAL INTERFACE

7.1 POWER CONNECTOR

The CP3104 has a 4 pin DC power connector (J3) mounted on the PCB. For the location and pin assignments for J3 see figure 1. The recommended mating connector is AMP part number 1-480424-0 utilizing AMP pins part number 350078-4 or equivalent.

7.2 CABLING

Connect the power cable to J3. Connect the Task File interface cable to J2.

7.3 DIAGNOSTIC ROUTINES

The microprocessor performs diagnostics upon application of power. If an error is detected the CP3104 will not come ready.

8.0 RECOMMENDED MOUNTING CONFIGURATION

The CP3104 drive is designed to be used in applications where the unit may experience shock and vibrations at greater levels than larger and heavier disk drives.

The features which allow greater shock tolerance are the use of rugged media and shock mounts. To take full advantage of the shock mounts, it is necessary to provide a minimum of 0.1 inch clearance on both the top and sides of the drive. This clearance allows for movement of the drive during acceleration. The drive may be mounted in any attitude.

8.1 MECHANICALLY ISOLATED MOUNTING POINTS

Ten base mounting points are provided to the customer. Each mounting point is mechanically isolated from the head/disk assembly. The drive is mounted using 6-32 screws; 1/8" max. insertion for the sides, and 1/4" max. insertion for the bottom. The system integrator should allow ventilation to the drive to ensure reliable drive operation over the operating temperature range.

9.0 INTERFACE DESCRIPTION

9.1 PHYSICAL DESCRIPTION

The CP3104 user interface is a 40 conductor cable with Molex p/n 15-47-3401 female header or equivalent. The interface allows up to two drives to be daisy chained together. The maximum cable length is two feet.

9.2 CONNECTOR

The CP3104 connector is a 40 conductor connector which consists of two rows of 20 male pins on 100 mil centers. The header part number is Molex p/n 7723 40A587, or equivalent.

10.0 ELECTRICAL DESCRIPTION

10.1 SIGNAL LEVELS

All signal levels are TTL compatible. A logic "1" is > 2.0 Volts. A logic "0" is from 0.00 Volts to .70 Volts. The drive capability of each of the inbound signals is described below.

10.2 SIGNAL CONVENTIONS

The interface between the drive adapter and the drive is called the Host Interface. The set of registers in the I/O space of the Host is known as the Task File.

All signals on the Host Interface shall have the prefix HOST. All negatively active signals shall be further prefixed with a "-" designation. All positive active signals shall be prefixed with

a "+" designation. Signals whose source are the Host, are said to be "outbound" and those whose source is the drive, are said to be "inbound".

10.3 PIN DESCRIPTIONS

The following table describes all of the pins on the Task File Interface (J1).

I/O PIN SIGNAL	I/O PIN SIGNAL
01 - -HOST RESET	02 - GND
03 - +HOST DATA 7	04 - +HOST DATA 8
05 - +HOST DATA 6	06 - +HOST DATA 9
07 - +HOST DATA 5	08 - +HOST DATA 10
09 - +HOST DATA 4	10 - +HOST DATA 11
11 - +HOST DATA 3	12 - +HOST DATA 12
13 - +HOST DATA 2	14 - +HOST DATA 13
15 - +HOST DATA 1	16 - +HOST DATA 14
17 - +HOST DATA 0	18 - +HOST DATA 15
19 - GND	20 - KEY
21 - RSVD	22 - GND
23 - -HOST IOW	24 - GND
25 - -HOST IOR	26 - GND
27 - RSVD	28 - +HOST ALE
29 - RSVD	30 - GND
31 - +HOST IRQ14	32 - -HOST IO16
33 - +HOST ADDR 1	34 - -HOST PDIAG
35 - +HOST ADDR 0	36 - +HOST ADDR 2
37 - -HOST CS0	38 - -HOST CS1
39 - -HOST SLV/ACT	40 - GND

SIGNAL NAME	DIR	PIN	DESCRIPTION
-HOST RESET	O	01	Reset signal from the Host system which is active low during power up and inactive thereafter.
GND	O	02	Ground between the drive

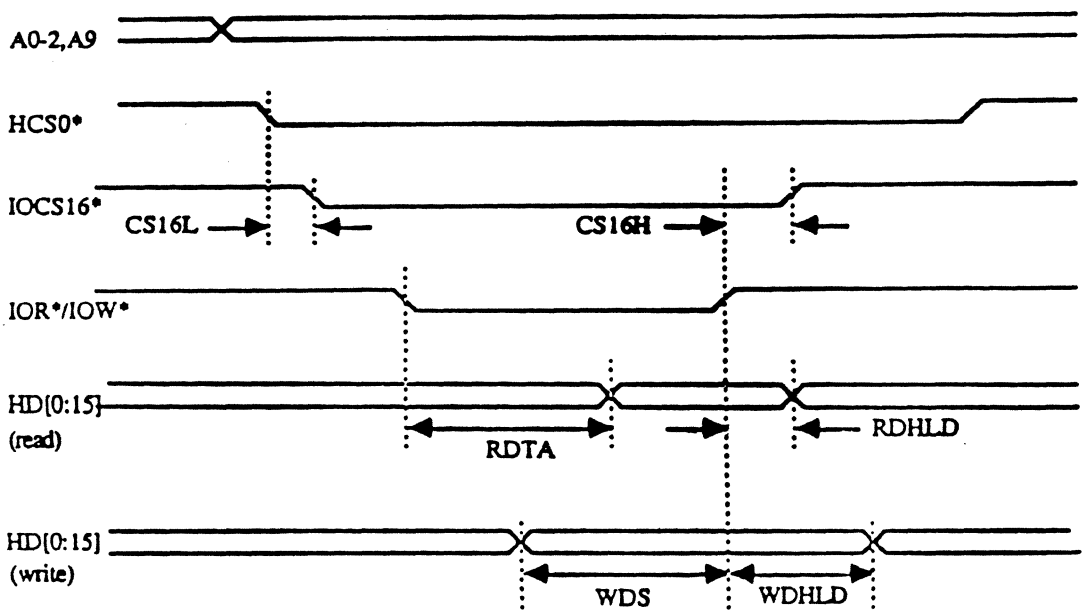
			and the Host.
+HOST DATA	I/O	03-18	16 bit bi-directional data bus between the Host and the drive. The lower 8 bits, HD0-HD7, are used for register & ECC access. All 16 bits are used for data transfers. These are tri-state lines with 24 mA drive capability.
GND	O	19	Ground between the drive and the Host.
KEY	N/C	20	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
RSVD	N/C	21	A pin reserved for future use.
GND	O	22	Ground between the drive and the Host.
-HOST IOW	O	23	Write strobe, the rising edge of which clocks data from the Host Data Bus, HD0 through HD15, into a register or the data register of the drive.
GND	O	24	Ground between the drive and the Host.
-HOST IOR	O	25	Read strobe, which when low enables data from a register or the data register of the drive onto the Host Data Bus, HD0 through HD15. The rising edge of -HOST IOR latches data from the drive at the

			Host.
GND	O	26	Ground between the drive and the Host.
RSVD	N/C	27	A pin reserved for future use.
+HOST ALE	O	28	Host Address Latch Enable. A signal used to qualify the address lines. This signal is presently not used by the drive.
RSVD	N/C	29	A pin reserved for future use.
GND	O	30	Ground between the drive and the Host.
+HOST IRQ14	I	31	Interrupt to the Host system, enabled only when the drive is selected, and the Host activates the -IEN bit in the Digital Output register. When the -IEN bit is inactive high, or the drive is not selected, this output in a high impedance state, regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a Host read of the Status register or a write to the command register. This signal is a tri-state line with 24 mA drive capacity.
-HOST IO16	32		Indication to the Host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word.

			This line is tri-state line with 24 mA drive capacity.
-HOST PDIAG	I	34	Passed diagnostic. Output by the drive if it is the slave drive. Input to the drive if it is the master drive. This low true signal indicates to a master that the slave has passed its internal diagnostic command. This line is only inactive high during execution of the diagnostic command. This line is a tri state line with 24 mA drive capability.
+HOST A0, A1, A2	O	35,33, 36	Bit binary coded address used to select the individual registers in the task file.
-HOST CS0	O	37	Chip select decoded from the Host address bus. Used to select some of the Host accessible registers.
-HOST CS1	O	38	Chip select decoded from the Host address bus. Used to select three of the registers in the Task File.
-HOST SLV/ACT	I	39	Signal from the drive used either to drive an SLV/ACT active LED whenever the disk is being accessed or as an indication of a second drive present. (See the Customer Options section for further information.) When jumpered as -ACTIVE, this signal is active low when the drive is busy and has a drive capability of

			20 ma. When jumpered as - SLAVE PRESENT signal, it is an indication of the presence of a second drive when low. It is connected to ground in this case.
GND		O	40 Ground between the drive and the Host.

11.0 TIMING REQUIREMENTS



11.1 HOST INTERFACE TIMING
(All times are in ns)

SYMBOL	PARAMETER	MIN	MAX
CS16L	-HCSO low to -IOCS16 low		20
CS16H	-IOR/-IOW high to -IOCS16 high		60
RDTA	-IOR low to HD (0:15) valid		60
RDHLD	-IOR high to HD (0:15) invalid	0	20
RDTRI	-IOR high to HD (0:15) tri-state		20
WDS	-IOW setup to HD (0:15) high	40	
WDHLD	-IOW hold from HD (0:15) high	10	
RWPULSE	-IOR / -IOW pulse width	80	

12.0 HOST ADDRESS DECODING

The Host addresses the drive using programmed I/O. This method requires that the desired register address be placed on the three Host address lines HA2 - HA0, a proper chip select is asserted and a read or write strobe, (-HOST IOR/-HOST IOW), given to the chip.

The Host generates two independent chip selects on the interface. The high order chip select, -HOST CS1, is valid only when the Host is accessing the three separate register addresses; alternate status register, digital output register, and drive address register. The low order chip select, -HOST CS0, is used to address all other registers.

The Host data bus 15-8 is only enabled when -IO16 enable is active and the Host is addressing the data register for transferring data and not the ECC bytes which are only transferred if the operation is a read or write long.

The following I/O map defines the all of the register addresses and functions for these I/O locations. A description of each register follows.

Address -CS0	-CS1	HA2	HA1	HA0	READ FUNCTION	WRITE FUNCTION
1	1	X	X	X	No operation	No operation
0	0	X	X	X	Invalid addr.	Invalid addr.
1	0	0	X	X	High Impedance	Not used
1	0	1	0	X	High Impedance	Not used
0	1	0	0	0	Data register	Data register
0	1	0	0	1	Error register	Write Precomp. Register
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	SDH register	SDH register
0	1	1	1	1	Status register	Command register
1	0	1	1	0	Alt. Status reg	Dig Output register
1	0	1	1	1	Drive Addr. reg.	Not used

where X is a don't care

13.0 REGISTER DESCRIPTION

In the following register descriptions, unused write bits should be treated as "don't cares", and unused read bits should be read as zeroes.

13.1 DATA REGISTER

(-HOST CS0, address 0, R/W). The data register is the register through which all data is passed on read and write commands. It is also the register to which the sector table is transferred during format commands and the data associated with the identify command is transferred. All transfers are high speed 16 bit I/O operations except for ECC bytes transferred during R/W long commands, which are slower 8 bit operations that occur after the transfer of the

data.

Data is stored on the disk with the least significant byte first, then the most significant byte for each word. This is important to remember when testing the ECC circuitry.

13.2 ERROR REGISTER

(-HOST CS0, address 1, Read only). This error register contains status from the last command executed by the drive. The contents of this register are only valid when the error bit (ER) is set in the Status register, unless the drive has just powered up or completed execution of its internal diagnostic,in which case the register contains a status code. The error bits in the register are defined below. The status codes are discussed later in the description of the DIAGNOSTIC Command.

b7							b0
BBK	UNC	--	IDNF	--	ABRT	TK0	--

where:

BBK indicates that a bad block mark was detected in the requested sector's ID field. A bad block is not created in the factory, but only when requested in the format command.

UNC indicates that an non-correctable data error has been encountered.

IDNF indicates that the requested sector's ID field could not be found.

ABRT indicates that the requested command has been aborted due to a drive status error (not ready, write fault, etc.) or because the command code is invalid.

TK0 indicates that track 0 has not been found during a recalibrate command.

-- not used. These bits are reset to zero.

13.3 WRITE PRECOMPENSATION

(HOST CS0, address 1, Write only). An 8 bit register used in previous disk drives to define the cylinder at which precompensation would begin. This register is used for other purposes for the CP3104. Also see the description of the Set Buffer command.

13.4 SECTOR COUNT

(-HOST CS0, address 2, R/W). The sector count defines the number of sectors of data to be read or written. If the value in this register is zero, a count of 256 sectors is specified. This count is decremented as each sector is read such that the register contains the number of sectors left to access in the event of an error in a multi-sector operation. The contents of this register define the number of sectors per track when executing an initialize drive command.

13.5 SECTOR NUMBER

(-HOST CS0, address 3, R/W). This register contains the starting sector number for any disk access. At the completion of each sector, and at the end of the command this register is updated to reflect the last sector read correctly, or the sector on which an error occurred. During multiple sector transfers, this register is updated to point at the next sector to be read/written if the previous sector's operation was successful.

13.6 CYLINDER LOW

(-HOST CS0, address 4, R/W). The cylinder low register contains the low order 8 bits of the starting cylinder number for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number, as described above in the Sector Number description.

13.7 CYLINDER HIGH

(-HOST CS0, address 5, R/W). The cylinder high register contains the two high order bits of the starting cylinder number for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number. As described above in the Sector Number description.

13.8 SDH REGISTER

(-HOST CS0 address 6, R/W). This register contains the drive and head numbers, as defined below:

b7				b3 b0
RSVD	RSVD	RSVD	DRV	HEAD

where:

RSVD this bit is used by the Host.

DRV is the binary encoded drive select number. When this bit is reset, the master drive is selected, and when this bit is set, the slave drive is selected.

HEAD is the four bit binary encoded head select number.

At the completion of each sector, and at the end of the command, this register is updated to reflect the currently selected head.

13.9 STATUS REGISTER

(-HOST CS0, address 7, Read only). This register contains the drive/controller status. The contents of this register are updated at the completion of each command. If the busy bit is active, no other bits are valid. The Host reading this register when an interrupt is pending is considered to be the interrupt acknowledge, and any pending interrupt is therefore cleared whenever this register is read.

The bits in this register are defined below:

b7							b0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

where:

BSY is the busy bit, which is activated whenever the drive has access to the Task File registers, and the Host is locked out from accessing the Task File. This bit is activated under the following circumstances:

1) At activation of the HOST RESET pin in the interface, or at activation of the software bit in the digital output register.

2) Immediately upon Host write of the command register with a read, read long, read buffer, seek recal, initialize drive parameters, verify, identify, or diagnostic command.

3) Immediately following transfer of 512 bytes of data after Host write of the command register with a write, format track, or write buffer command, or 512 bytes of data and the seven ECC bytes after a Host write of the command register with a write long command. When BSY is active, any HOST read of a task file register is inhibited and the status register is read instead.

DRDY is the drive ready indication. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current readiness of the drive. This bit will be inactive at power up and remain inactive until the drive is up to speed and ready to accept a command.

DWF is the drive write fault bit. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current write fault status.

DSC is the drive seek complete bit. This bit is active when the

disk drive heads are settled over a track. When there is an error, this bit lis not changed until the Status register is read by the Host, at which time the bit again indicates the current seek complete status.

DRQ is the data request bit, which indicates that the drive is ready for transfer of a word or byte of data between the Host and the Data register.

CORR is the corrected data bit, which is active when a correctable data error has been encountered and the data has been corrected. This condition will not terminate a multi-sector read operation.

IDX is the index bit which is active once per disk revolution.

ERR is the error bit, which indicates that the previous command ended in some type of error. The other bits in the Status register, and the bits in the error register will have additional information as to the cause of the error.

13.10 COMMAND REGISTER

(-HOST CS0, address 7, Write only). The eight bit code written to this register passes the drive the command from the Host. Command execution begins immediately after this register is written. A list of executable commands with the command codes and necessary parameters for each command follows.

COMMAND NAME	COMMAND CODE b7 b0	PARAMETERS USED SC	SN	CY	SDH
Recalibrate	0 0 0 1 x x x x	n	n	n	d
Read Sector(s)	0 0 1 0 0 0 l r	y	y	y	y
Write Sector(s)	0 0 1 1 0 0 l r	y	y	y	y
Read Verify Sector(s)	0 1 0 0 0 0 0 r	y	y	y	y
Format Track	0 1 0 1 0 0 0 0	n	n	y	y
Seek	0 1 1 1 x x x x	n	n	y	y
Exec. Drv Diagnostic	1 0 0 1 0 0 0 0	n	n	n	d
Initialize Drv Parms	1 0 0 1 0 0 0 1	n	n	n	y
Read Multiple	1 1 0 0 0 1 0 0	y	y	y	y
Write Multiple	1 1 0 0 0 1 0 1	y	y	y	y
Set Multiple mode	1 1 0 0 0 1 1 0	y	n	n	d
Read Sector Buffer	1 1 1 0 0 1 0 0	n	n	n	d
Write Sector Buffer	1 1 1 0 1 0 0 0	n	n	n	d
Identify Drive	1 1 1 0 1 1 0 0	n	n	n	d
Set Buffer Mode	1 1 1 0 1 1 1 1	n	n	n	d

Where:

l is the long bit, if 1, R/W long commands are executed, if 0, normal R/W commands are performed.

r is the retry bit; = 0, retries are enabled, = 1, retries are disabled. Retries that may be enabled/disabled are those on ECC and data errors. When retries are disabled at the start of a command, they are always automatically enabled at the end of the command.

SC is the sector count register.

SN is the sector number register.

CY is the cylinder registers.

SDH is the drive/head register.

y means the register contains a valid parameter for this command. For the drive/head register, y means that both the drive and head parameters are used.

n means the register does not contain a valid parameter for this command.

d means only the drive parameter is valid and not the head parameter.

x is a don't care.

For the command decode, the "1's" and "0's" are important. Failure to comply will result in an Aborted Command response or misinterpretation of the command.

13.11 ALTERNATE STATUS REGISTER

(-HOST CS1, address 6, Read only). This register contains the same information as the Status register in the Task File. The only difference being that reading this register does not imply interrupt acknowledge to reset a pending interrupt.

b7							b0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

See the description of the Status register for definitions of the bits in this register.

13.12 DIGITAL OUTPUT REGISTER

(-HOST CS1, address 6, Write only). This register contains two control bits as follows:

b7							b0
--	--	--	--	--	SRST	-IEN	--

where:

-IEN is the enable bit for this disk drive interrupt to the Host. When this bit is active, and the drive is selected, the Host interrupt, HOST IRQ14, is enabled, through a tri-state buffer, to the Host. When this bit is inactive, or the drive is not selected the HOST IRQ14 pin will be in a high impedance state, regardless of the presence or absence of a pending interrupt.

SRST is the Host software reset bit. The drive is held reset when this bit is active, and enabled when this bit is inactive. If

two drives are daisy chained on the interface, this bit will reset both drives simultaneously.

-- these bits are not used.

13.13 DRIVE ADDRESS REGISTER

(-HOST CS1, address 7, Read only). This register loops back the drive select and head select addresses of the currently selected drive. The bits in this register are as follows:

b7							b0
RSVD	-WTG	-HS3	-HS2	-HS1	-HS0	-DS1	-DS0

where:

RSVD is reserved and undriven by the drive. When the Host reads the drive address register, this bit must be in a high impedance state.

-WTG is the write gate bit, which is active when writing to the disk drive is in progress.

-HS3 through -HS0 are the one's complement of the binary coded address of the currently selected head. For example, if -HS3 through -HS0 are 1 1 0 0, respectively, head 3 is selected. -HS3 is the most significant bit.

-DS1 is the drive select bit for drive 1, and should be active when drive 1 is selected and active. -DS0 is the drive select bit for drive 0, and should be active when drive 0 is selected and active. It is important to note that Bit 7 is not driven for compatibility with the floppy drive address space. NOTE: If your system is different, you may have to drive this bit when this register is read.

14.0 COMMAND DESCRIPTION

All commands are decoded from the COMMAND Register. The Host interface shall be programmed by the Host computer to perform commands and will return status to the Host at command completion. When two drives are daisy

chained on the interface, commands are written in parallel to both drives, only the selected drive will execute the command, except for the diagnostic command. In that case, both drives execute the command and the slave drive reports its status to the master via the -HOST PDIAG signal.

Drives are selected by the DRV bit in the drive/head register and by a jumper, -C/D, on the drive designating it as either a master or slave. See the section on Customer Options. When the DRV bit is reset, the master drive is selected. When the DRV bit is set, the slave drive is selected. When drives are daisy chained, one must be jumpered as the master and one as the slave. When a single drive is attached to the interface, it must be jumpered as the master. Throughout this document, drive selection always refers to the state of the DRV bit, and position of the master/slave jumper.

To issue a command, load the pertinent registers in the Task File, activate the interrupt enable bit, -IEN in the digital output register, and then write the command code to the command register. Execution begins as soon as the command register is written. Also see the section on retries.

14.1 RECALIBRATE - 10

This command will move the R/W heads from anywhere on the disk to cylinder 0. Upon receipt of the command,the drive sets BSY and executes a seek to cylinder 0. The drive then waits for the seek to complete before updating status, resetting BSY and generating an interrupt. If the drive cannot reach cylinder 0, the error bit is set in the Status register and the track 0 bit set in the error register. An aborted command response will be given if the drive is not spinning or is not on track. Upon successful completion of the command, the Task File registers will be as follows:

Error Register	-	00
Sector Count	-	Unchanged
Sector Number	-	Unchanged
Cylinder Low	-	00
Cylinder High	-	00
SDH	-	Unchanged

14.2 READ SECTOR(s) - 2X

This command will read from 1 to 256 sectors as specified in the Task File (sector count equal to 0 requests 256 sectors), beginning at the specified sector. As soon as the command register is written, the drive sets the BSY bit and begins execution of the command. An aborted command is set if bits 2 & 3 are not equal to zero. An ID not found error is returned if incorrect task file parameters are passed. If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive begins searching for the appropriate ID field. If the ID is read correctly, the data field is read into the sector buffer, error bits are set if an error was encountered, the DRQ bit is set and an interrupt is generated. The DRQ bit is always set regardless of presence or absence of an error condition at the end of the sector. Upon command completion, the Task File registers contain the cylinder, head, and sector number of the last sector read. The sector count is zero after successful execution of the command.

Multiple sector reads set DRQ and generate an interrupt when the sector buffer is filled at the completion of each sector, and the drive is ready for the data to be read by the Host. DRQ is reset and BSY is set immediately when the Host empties the sector buffer. If an error occurs during a multiple sector read, the read will terminate at the sector where the error occurs. The Task File registers will contain the cylinder, head, and sector number of the sector where the error occurs. The Host may then read the Task File to determine what error has occurred, and on which sector. If the error was either a correctable data error or an non-correctable data error, the flawed data is loaded into the sector buffer. The read does not terminate if the error was a correctable

data error. If no error is detected, the cylinder, head, and sector registers are updated to point to the next sequential sector.

A read long may be executed by setting the long bit in command code. The read long command returns the data and the ECC bytes contained in the data field of the desired sector. During a read long, the drive does not check the ECC bytes to determine there has been any type of data error. Data bytes are 16 bit transfers and ECC bytes are eight bit transfers. Seven ECC bytes are transferred. Also see the section on 1:1 operations.

14.3 WRITE SECTOR(s) - 3X

This command will write from 1 to 256 sectors as specified in the Task File (sector count equal to 0 requests 256 sectors), beginning at the specified sector. As soon as the command register is written, the drive waits for the Host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. Once the buffer is full, the drive sets BSY and begins command execution. If bits 2 & 3 are on, the command terminates with aborted command. An ID not found error is returned if incorrect task file parameters are passed. If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive begins searching for the appropriate ID field. If the ID is read correctly, the data loaded in the buffer is written to the data field of the sector, followed by the ECC bytes. Upon command completion, the Task File registers contain the cylinder, head, and sector number of the last sector read. The sector count is zero after successful execution of the command.

Multiple sector writes set DRQ and generate an interrupt each time the buffer is ready to be filled. DRQ is reset and BSY is set immediately when the Host fills the sector buffer. If an error occurs during a multiple sector write, it will terminate at the sector where the error occurs. The Task File indicates the location of the sector where the error occurred. The Host may then read the Task File to determine what error has

occurred, and on which sector. If no error is detected, the cylinder, head, and sector registers are updated to point at the next sequential sector.

A write long may be executed by setting the long bit in the command code. The write long command writes the data and the ECC bytes directly from the sector buffer; the drive will not generate the ECC bytes itself for the write long command. Data byte transfers are 16 bits, ECC bytes are 8 bit transfers. Seven bytes must be transferred even though only the first four are used for ECC. Also see the section on 1:1 operations.

14.4 VERIFY SECTORS - 4X

This command works exactly the same as the Read Sectors command except that no data is transferred. Up to 256 sectors will be read into the sector buffer and ECC bytes verified, beginning at the location specified by the task file. When each sector has been verified, the Task File is updated but no data request or interrupt is set to indicate that the sector has been verified. When all sectors have been verified, an interrupt is generated to indicate that all sectors have been transferred. A value of 00 in the sector count register indicates that 256 sectors are to be verified.

Read look-aheads are enabled for this command. Also see the description of 1:1 operations.

14.5 FORMAT TRACK - 50

This command formats the track specified in the Task File. As soon as the command register is written, the drive waits for the Host to fill the buffer with the format data. When the buffer is full, the drive resets DRQ, sets BSY and begins command execution. An aborted command is set if any bits 0-3 are "1". If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, formatting begins using the data in the sector buffer. A sector my be formatted Good/Bad or an alternate Assigned/Unassigned. At the completion of the track, the drive resets BSY and

generates an interrupt.

The format information is made up of two bytes per sector on the track. The most significant byte is the sector number. The second byte is the descriptor byte. After writing the information for all the sectors on the logical track, the remaining bytes of the sector should be filled with zeroes. The sectors may be arranged in any order but they must contain two bytes per sector as previously described and they must be transmitted as the first 66 bytes to the sector buffer.

If a sector that was previously formatted bad is requested to be formatted good, an attempt will be made to format it good. For format Good/Bad the least significant byte is 00 if the sector is to be formatted normally, or 80h if the sector is to be formatted bad.

A DESCRIPTOR BYTE OF 40h will cause the drive to logically assign the sector to an alternate sector in its set of spares. A descriptor byte of 20h will cause the drive to logically un-assign the spare sector and recover the primary sector. The spare sector is lost. This provides the capability to replace a bad sector. Diagnostic programmers please note that since when the un-assign alternate function is performed, the spare sector is NOT recovered, it is wrong to write a diagnostic that will assign and then un-assign alternates across the entire drive.

If a zero sector or sector number greater than the maximum for the mode is transmitted, be it native or logical, an ID Not Found error will be set. If there are multiple bad sector numbers, the smallest illegal sector number will be stored in the sector number register in the Task File. However, all legal sectors will be formatted according to the descriptor byte before the error is posted.

14.6 SEEK - 70

This command initiates a seek to the track and selects the head specified in the Task File. The drive need not be

formatted for a seek to execute properly. When the command is issued, the drive sets BSY in the Status register, initiates the seek, resets BSY, and generates an interrupt. Only the cylinder register is valid for this command. The drive does not wait for the seek to complete before returning the interrupt. Seek complete will be set upon completion of the command. If a new command is issued to a drive while a seek is being executed, the drive will wait, with BSY active, for the seek to complete before executing the new command. No checks are made on the validity of the sector number or head value in the task file. If the cylinder value is incorrect, the seek is not performed and seek complete is set. The error bit is not set.

14.7 EXECUTE DRIVE DIAGNOSTIC - 90

This command performs the internal diagnostic tests implemented by the drive. The diagnostic tests shall only be executed upon receipt of this command. The drive sets BSY immediately upon receipt of the command. If the drive is a master, -C/D jumpered, the drive performs the diagnostic tests and saves the results. It then checks to see if a slave drive is present and waits up to 5 seconds for the slave to complete its diagnostics. If the slave successfully completes its diagnostics, it asserts -HOST PDIAG. If unsuccessful, it sets its error register as described below. The master drive resets BSY, and generates an interrupt. The value in the error register should be viewed as a unique 8 bit code and not as the single bit flags defined previously. The interface registers are set to initial values except for the error register if an error has occured.

The table below details the codes in the error register and a corresponding explanation:

Error code	Description
01	no error detected
03	sector buffer error
8x	slave drive failed (see note below)

NOTE: If the slave drive fails diagnostics, the master drive shall "OR" 80 hex with its own status and load that code into the error register. If the slave drive passes diagnostics or there is no slave drive connected, the master drive shall reset bit 7 of the Error Register in the Task File to 0.

Additional codes may be implemented at the manufacturer's option.

14.8 INITIALIZE DRIVE PARAMETERS - 91

This command enables the Host to set the head switch and cylinder increment points for multiple sector operations. The sector head, and cylinder values in the Task File are not checked for validity by this command. Therefore, if they are invalid, no error will be reported until an illegal access is made by some other command. Cylinder and head increments on subsequent commands will occur after access of the maximum sector and maximum head specified by this command. If the initialize drive parameters command is not issued at power up, the drive will default to 33 sectors per track, 8 heads, and 776 cylinders. Upon receipt of the command, the drive sets BSY, saves the parameters, resets BSY, and generates an interrupt. To specify maximum heads, write 1 less than the maximum, e.g. write 4 for a 5 head drive. To specify maximum sectors specify the actual number of sectors, e.g. 33 for a maximum of 33 sectors/track.

In order to facilitate the CP3104's use in systems for which there may be no exact device type, this command has been changed slightly. Any head and sector value will be accepted. From these two values, the drive will compute the maximum cylinder. This is done by dividing the product of the number of heads and the number of sectors into 204,864 (the total number of sectors in the drive). One must be careful when selecting a device type so that the total number of cylinders expected by the particular device type does not exceed that possible by the drive. This could cause errors at boot time. Where possible, it is recommended that the device type that matches the CP3104's native parameters is used or put into the BIOS.

14.9 READ MULTIPLE COMMAND - C4

The read multiple command is identical to the read sectors operation but several sectors are transferred the the Host as a block without intervening interrupts and only requiring DRQ qualification of the transfer at the start of the block count on each sector. Long transfers are not permitted. The block count, which is the number of sectors to be transferred as a block, is programmed by the set multiple mode command which must be executed prior to the read multiple command. When the read multiple command is issued, the sector count register will contain the number of sectors (not the number of blocks or the block count) requested. If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer will be for N sectors, where

N = (sector count) modulo (block count).

If the read multiple command is attempted before the set multiple mode command has been executed or when read multiple commands are disabled, the read multiple operation will be rejected with an aborted command error.

Disk errors encountered during read multiple commands will be reported at the beginning of the block or partial block transfer, but DRQ will still be set and the transfer will take place as it normally would, including transfer of corrupt data, if any. Subsequent blocks or partial blocks will only be transferred if the error was a correctable data error. All other errors will cause the command to stop after transfer of the block which contained the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block. Read look-aheads are not active for this command.

14.10 WRITE MULTIPLE COMMAND - C5

The write multiple command performs similarly to the write sectors command except that the controller sets BSY

immediately upon receipt of the command, data transfers are multiple sector blocks, and the long bit is not valid. Several sectors are transferred to the Host as a block without intervening interrupts and only requiring DRQ qualification of the transfer at the start of the block, not on each sector. There is no IRQ prior to the first block transfer. The block count, which is the number of sectors to be transferred as block, is programmed by the set multiple mode command, which must be executed prior to the write multiple command. When the write multiple command is issued, the sector count register will contain the number of sectors (not the number of blocks or the block count) requested. If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer will be for N sectors, where

N = (sector count) modulo (block count).

If the write multiple command is attempted before the set multiple mode command has been executed or when write multiple commands are disabled, the write multiple operation will be rejected with an aborted command error.

All disk errors encountered during write multiple commands will be reported after the attempted disk write of the block or partial block is transferred. The write operation will end with the sector in error, even if it was in the middle of a block. Subsequent blocks will not be transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

14.11 SET MULTIPLE MODE - C6

This command enables the controller to perform read and write multiple operations and establishes the block count for these commands. Prior to command issuance, the sector count register should be loaded with the number of sectors per block. Block sizes supported are 1, 2, 4, 8, 16, 32 and 64. Upon receipt of the command, the controller sets BSY and looks at the sector count register contents. If the register

contents are valid and supported block count is supplied, that value is loaded for all subsequent read and write multiple commands and execution of these commands is enabled. Any unsupported block count in the register will result in an aborted command error and read and write multiple commands being disabled. If the sector count register contains 0 when the command is issued, read and write multiple commands will be disabled. Once the appropriate action has been taken, the controller resets BSY and generates an interrupt. At power up, or after a hardware or software reset, the default mode is to have read and write multiple disabled.

14.12 READ BUFFER - E4

The read buffer command allows the Host to read the current contents of the drive's sector buffer. Only the command resister is valid for this command. When this command is issued, the drive will set BSY, set up the sector buffer for a read operation, set DRQ, reset BSY, and generate an interrupt. The Host may then read up to 512 bytes of data from the buffer.

14.13 WRITE BUFFER - E8

The write buffer command allows the Host to overwrite the contents of the drive's sector buffer with any data pattern desired. Only the command register is valid for this command. When this command is issued the drive hardware sets up the sector buffer for a write operation and sets DRQ. The Host may then write up to 512 bytes of data to the buffer.

14.14 IDENTIFY DRIVE - EC

The identify command allows the Host to receive parameter information from the drive. When the command is issued, the drive sets BSY, stores the required parameter information in the sector buffer, sets the DRQ bit, and generates an interrupt. The Host may then read the information out of the sector buffer. The parameter words in the buffer are

arranged as follows; all numbers are given in hexadecimal format right justified, all reserved bits or words are zeroes.

Word 00	-	A constant 0A5A
Word 01	-	Number of fixed cylinders
Word 02	-	Number of removable cylinders
Word 03	-	Number of heads
Word 04	-	Number of unformatted bytes/physical track
Word 05	-	Number of unformatted bytes/sector.
Word 06	-	Number of physical sectors/track
Word 07	-	Number of bytes in the inter-sector gaps
Word 08	-	Number of bytes in the sync fields
Word 09	-	0000
Word 10-19	-	Serial number
Word 20	-	Controller type 0003 dual ported multiple sector buffer with look ahead-read.
Word 21	-	Controller buffer size in 512 byte increments
Word 22	-	Number of ECC bytes passed on read/write long commands
Word 23-26	-	Controller firmware revision
Word 27-46	-	Model number
Word 47	-	Number of sectors/interrupt (0 = does not support >1)
Word 48	-	Double word transfer flag (0 = not capable, 1 = capable)
Word 49	-	Assign Alternate (0 = not capable, 1 = capable) (See Format Description)
Word 50-255	-	Reserved

14.15 SET BUFFER MODE COMMAND - EF

This command allows enabling or disabling of the read look-ahead feature. Prior to command issuance, the write precompensation register should be loaded with either AAh, to enable, or 55h to disable read look-ahead operation.

Upon receipt of the command the controller sets BSY and looks at the write precompensation register contents. If the register contents are either AAh or 55h, the appropriate mode is selected. Any other value in the register will result in an aborted command. At command completion, the controller resets BSY and generates an interrupt. At power up, or after a software or hardware reset, the default mode

is read look-ahead enabled. Also see the description of 1:1 operations.

15.0 OPERATIONS DESCRIPTION

The following paragraphs describe operations that span several commands or are not covered sufficiently in the preceding paragraphs.

15.1 RESET

A RESET condition will set the drive busy, allowing the drive to perform the proper initialization required for normal operation.

A RESET condition can be generated in three ways. There are two hardware resets, one from the Host (- HOST RESET) and one from the drive power sense circuitry. These are set high when the system and the drive respectively acknowledge good power. The other reset is software generated. The Host can write to the digital output register and set the reset bit. This Host software reset condition will persist until the reset bit is written to a zero.

Once the reset has been removed and the drive has been re-enabled, with BSY still active, the drive will perform any necessary hardware initialization, clear any previously programmed drive parameters and revert to the defaults, load the Task File registers with their initial values, and then reset BSY. No interrupt is generated when initialization is complete. The initial values (hex) for the Task File registers are as follows:

Error register	= 01
Sector Count	= 01
Sector Number	= 01
Cylinder Low	= 00
Cylinder High	= 00
Drive/Head register	= 00

15.2 BUSY OPERATION

"BUSY" is set in a number of ways. A RESET condition described above is one way. Another method occurs when the Host issues a command. For a non-write type command, the register is clocked BUSY on the Host write of the command register. The disk controller and microprocessor prepare the data to return and set the drive not BUSY to allow the Host access of the data requested.

On a write type command, the command is issued, setting the IO16 enable and Data Request, but, BUSY is not set until the data to be written is put into the RAM buffer. This is accomplished by setting BUSY on the condition of the buffer becoming full in write. Write type commands include Write Sector (s), Format, and Write Sector Buffer. A write multiple command will set BUSY immediately. Sometime later BUSY will drop and Data Request will be set.

In addition, the drive microprocessor has the ability to set/reset BUSY. This is the only way that BUSY can be cleared. This means that the only way a drive can respond properly to a command is for the drive microprocessor to be active. When BUSY is active, the drive has read and write access to the Task File registers, the Host can only read the Status Register and Alternate Status Register of the Task File. Any attempted "Host" read of a Task File register while BUSY is active, results in reading the Status register.

When BUSY is inactive, the Host has read and write access to all Task File registers.

15.3 RETRIES

DATA RETRY ALGORITHM

When an ECC error is detected in the data field during a read operation, the following retry algorithm is used:

Step 1.	read retry
Step 2.	read retry
Step 3.	read retry
Step 4.	apply ECC to step 3
Step 5.	read retry with +65 micro inch offset
Step 6.	apply ECC to step 5
Step 7.	read retry
Step 8.	apply ECC to step 7
Step 9.	read retry with -65 micro inch offset
Step 10.	apply ECC to step 9
Step 11.	read retry
Step 12.	read retry
Step 13.	read retry
Step 14.	read retry
Step 15.	read retry
Step 16.	read retry

In the event of a hard error, steps 1-16 are repeated eight times for a total of 128 retries. Allowing 17 msec for each read retry and 75 msec for each ECC correction, this is a total time of 4.0 seconds (17*12*8/1000 + 75*4*8/1000) to return a non-recoverable error condition to the Host. With the exception of disabling retries (i.e. retry count = 0) the retry count of 128 is currently not changeable.

If there is a successful read or ECC in any of the above steps, the retry process is aborted and the data is returned to the Host.

When the R/W heads are switched or a seek is completed, the drive will attempt an offtrack read when less than 200 micro inches from the center of the track. If this attempt is successful, 17 msecs of latency is saved and seek

performance of the drive will exceed the specification. When this attempt is not successful, the drive will read the sector on the next pass as in a normal read operation (100 micro inch) and the seek specification is met.

HEADER RETRY ALGORITHM

When an ECC error is detected while reading the header field, 20 read retries are attempted before a header error is returned to the Host. If a header is successfully read before the 20 retries are completed, the header retry counter is reset and the data field is processed. For a hard error in the header field, the total amount of time for 20 retries is 340 msec (17*20/1000). Header retries can not be disabled from the interface, nor can the header retry count be changed.

15.4 1:1 OPERATIONS

Previous Conner AT interface drives were 3:1 interleave. The CP3104, while compatible, requires some explanation of the idiosyncracies of 1:1 operations. For write operations, sequential single sector operations will be slower due to missing the interleave. Multiple block operations will be faster because after receiving all blocks except the last, the next block is requested while the data is being written to the disk. After the last block is received, the drive goes BUSY until it is done processing all the data. In case of error, the task file registers will point to the actual failing block.

The 1:1 interleave and the 32kb buffer are combined to provide read look-ahead capability. For this drive, with read look-aheads active, any read will cause the drive to read a minimum of 64 contiguous sectors of data. All subsequent read operations will test if the data is already in the buffer before going to the disk. If any other command other than a read is issued following the first read, the buffer will be purged before the operation takes place.

It is important to remember that the overall throughput of the drive is a combination of the drive's ability to provide data and the Host computers ability to take it. For those customers requiring a faster transfer rate than the standard 3.75MB provided, it is possible to provide a 4.75MB transfer rate.

15.5 AC HYSTERISIS

All inputs have AC hysterisis so that at signal rise/fall times of 25ns, the drive will have .55 volt hysterisis and at rise/fall time of 10ns, the hysterisis will be .95 volts.

15.6 FORMATTING

Conner drives are different from previous ST506 type drives in that they do not require a low level format. This low level format is done in the factory as part of the extended burn in process and it is not possible to do via the Host interface, therefore to put a drive on a system, it is only necessary to FDISK and then do a system FORMAT.

16.0 ERROR REPORTING

In general, errors are detected in the following fashion by the drive microprocessor. At the start of the execution of the command, the command register is checked for conditions that would lead to an aborted command. Then the operation is attempted. The errors that are valid for each command are summarized below. Any subsequent error terminates the command at the point that it is discovered.

COMMAND	ERROR TYPE VALID
RECALIBRATE	ABRT, TK0, DRDY, DWF, DSC, ERR
READ SECTOR	BBK, UNC, IDNF, ABRT, DRDY, DWF, DSC, CORR, ERR
READ LONG	BBK, IDNF, ABRT, DRDY, DWF, DSC,

	ERR
WRITE SECTOR	BBK, IDNF, ABRT, DRDY, DWF, DSC, ERR
WRITE LONG	BBK, IDNF, ABRT, DRDY, DWF, DSC, ERR
READ VERIFY	BBK, UNC, IDNF, ABRT, DRDY, DWF, DSC, CORR, ERR
FORMAT TRACK	IDNF, ABRT, DRDY, DWF, DSC, ERR
SEEK	IDNF, ABRT, DRDY, DWF, DSC, ERR
DRIVE DIAG	ABRT, ERR
INIT DRIVE PARMS	ABRT, ERR
READ MULTIPLE	BBK, UNC, IDNF, ABRT, DRDY, DWF, DSC, CORR, ERR
WRITE MULTIPLE	BBK, IDNF, ABRT, DRDY, DWF, DSC, ERR
SET MULTIPLE	ABRT, ERR
READ BUFFER	ABRT, ERR
WRITE BUFFER	ABRT, ERR
IDENTIFY DRIVE	ABRT, ERR
SET BUFR MODE	ABRT, ERR
INVAL CMD CODE	ABRT, ERR

where:

BBK is bad block detected

UNC	is non-correctable data error
IDNF	is requested ID not found
ABRT	is aborted command error
TK0	is track 0 not found error
DRDY	is disk Drive not ready detected
DWF	is disk Drive write fault detected
DSC	is disk Drive seek complete not detected
CORR	is corrected data error
ERR	is the error bit in the Status register

APPENDIX A: Evaluation Adapter Board

INTRODUCTION

In order to facilitate evaluation and aid those manufacturers interested in quickly getting the CP3104 drive running, Conner Peripherals has developed an adapter board to be used in conjunction with the drive on an AT or equivalent system. The drive requires no special driver program as it works with the existing AT Bios or equivalent. It is hoped that the interface will be incorporated into the motherboard of the AT device or on some other multi-function adapter. The artwork and Bill of Materials are available upon request.

DESCRIPTION

The AT Task File Interface is a set of registers that allows execution of a set of commands via the Host Computer BIOS. The CP3104 drive implements the Task File on the drive. The adapter board buffers the drive from the Host and does the address decode.

The adapter card decodes the Host I/O addresses IF0-1F7 and 3F6-3F7. These addresses are set aside for disk drive use in the AT BIOS. The drive will respond to the commands issued by the BIOS.

The floppy drive also responds to address 3F7, bit 7. The adapter card does not drive this bit.

REQUIREMENTS

The following is required to run the drive:

- Host adapter board
- CP3104 Drive
- 40 pin flat cable

INSTALLATION OF THE DRIVE & ADAPTER CARD

1. Pick a device type that is equal to or less than the CP3104 in capacity and update the PC's CMOS.

2. Remove power to the computer

3. If another hard disk controller is installed, it is necessary to prevent it from responding the addresses 1F0-7 and 3F6-7. It is also necessary to ensure that the controller is electrically disconnected or tri-stated from IRQ14 of the motherboard bus. This may be done either by removing the board, by electrically disconnecting the signals from the interface, or by setting the jumpers of the board to disable the hard disk controller.

4. Insert the board into any available card slot.

5. Configure the Host adaptor for the correct configuration of your computer BIOS (See Table 1).

Table 1: Jumpers

E1 - Always not installed

E2 - Always in

E3 - Always not installed

E4 - Always in

Note: E3 and E4 are located in a straight line with a pin between them, as shown below. Jumper in refers to the pin jumpered to the center pin.

6. Connect power to the CP3104

7. Run the DOS Fdisk program (or equivalent) to establish DOS partitions.

   NOTE: DOS 3.2 and below have limitations of 32 megabytes unless a software utility is used to overcome this.

8. Run the DOS format program by typing "Format C:/S". The volume may be named with the addition of the "/V". The format will be completed and the system transferred if the "/S" option was used. The system will ask for a volume name if the "/V" option is used.

9. Files can then be copied to the C: drive from the floppy.

10. When the system is rebooted, the system should boot from the hard drive (drive C:) if the floppy is removed.

BOARD SCHEMATIC AND LAYOUT

See Figure figures A-1 and A-2.

Figure A-1 AT Adapter Schematic

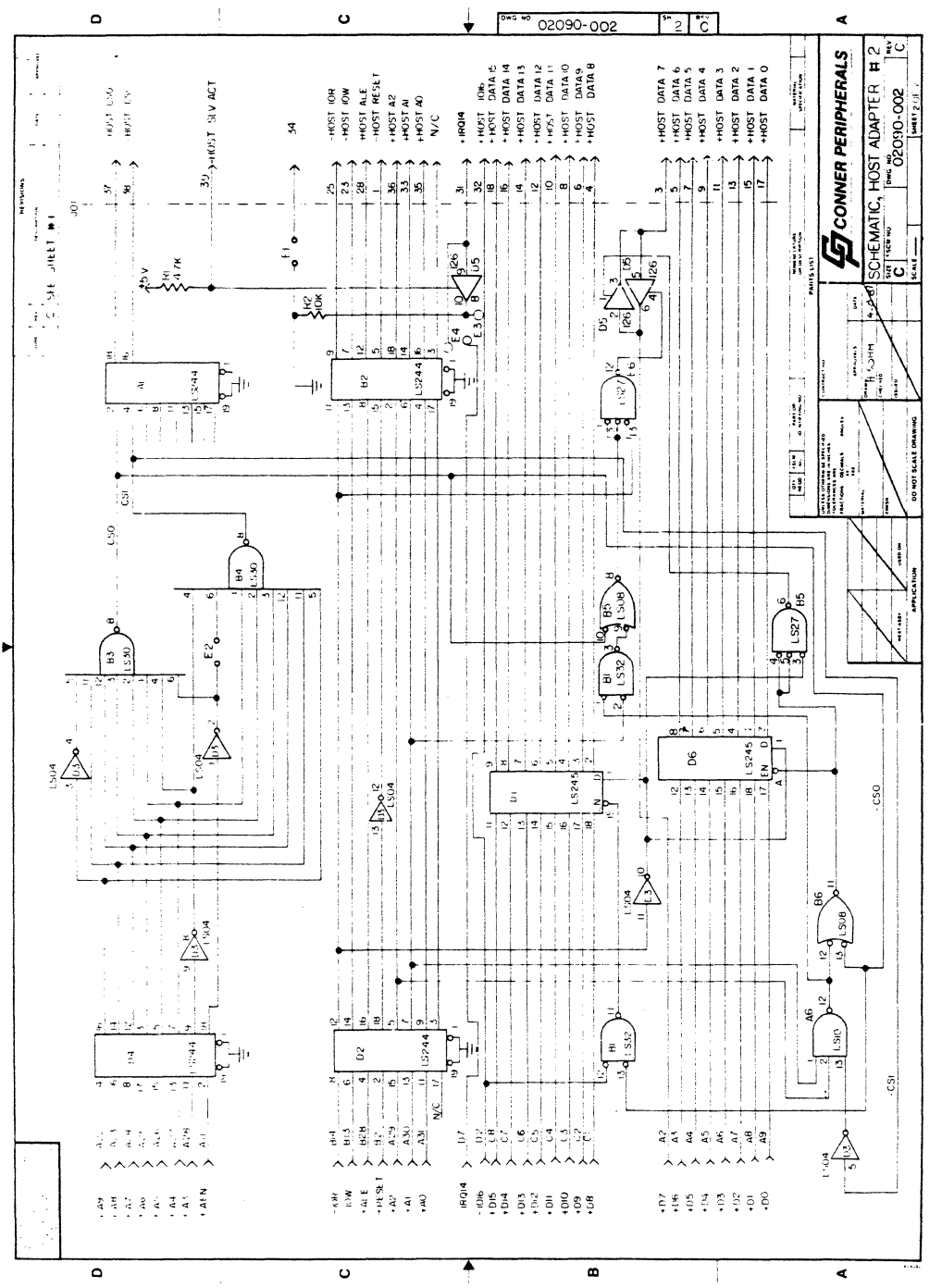
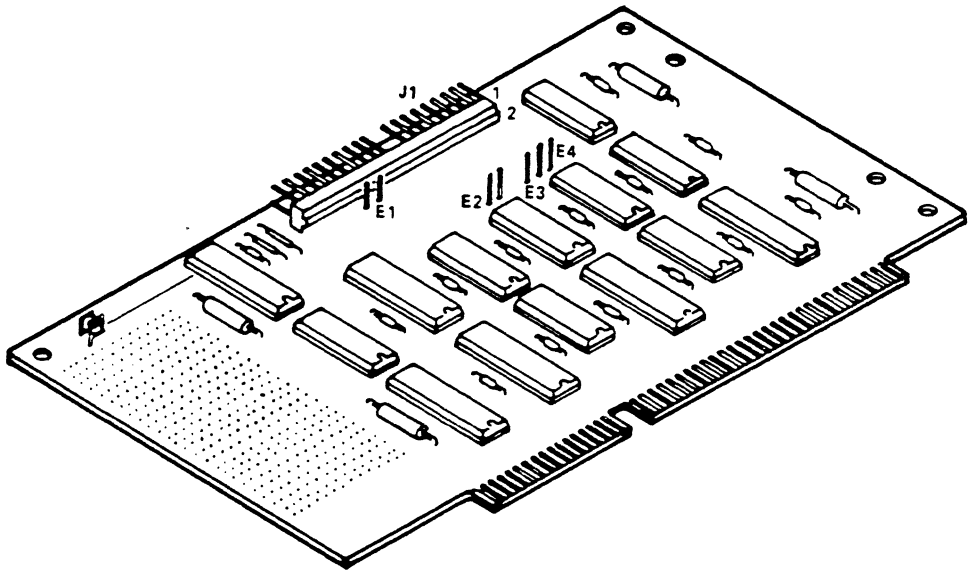


Figure A-2 AT Adapter Card Layout



SYSTEM BOARD I/O

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A01	N/C	B01	GND	C01	N/C	D01	N/C
A02	D7	B02	RST DRV	C02	N/C	D02	-I016
A03	D6	B03	+5V	C03	N/C	D03	N/C
A04	D5	B04	N/C	C04	N/C	D04	N/C
A05	D4	B05	-5V	C05	N/C	D05	N/C
A06	D3	B06	N/C	C06	N/C	D06	N/C
A07	D2	B07	-12V	C07	N/C	D07	IRQ14
A08	D1	B08	N/C	C08	N/C	C08	N/C
A09	D0	B09	+12V	C09	N/C	D09	N/C
A10	N/C	B10	GND	C10	N/C	C10	N/C
A11	AEN	B11	N/C	C11	D8	D11	N/C
A12	N/C	B12	N/C	C12	D9	D12	N/C
A13	N/C	B13	-IOW	C13	D10	D13	N/C
A14	N/C	B14	-IOR	C14	D11	D14	N/C
A15	N/C	B15	N/C	C15	D12	D15	N/C
A16	N/C	B16	N/C	C16	D13	D16	+5V
A17	N/C	B17	N/C	C17	D14	D17	N/C
A18	N/C	B18	N/C	C18	D15	D18	GND
A19	N/C	B19	N/C				
A20	N/C	B20	N/C				
A21	N/C	B21	N/C				
A22	A9	B22	N/C				
A23	A8	B23	N/C				
A24	A7	B24	N/C				
A25	A6	B25	N/C				
A26	A5	B26	N/C				
A27	A4	B27	N/C				
A28	A3	B28	ALE				
A29	A2	B29	+5V				
A30	A1	B30	N/C				
A31	A0	B31	GND				

PROBLEMS

If at power on, the drives spins up but is ignored by the system (indicated by the system taking a long time to boot) it is possible the IRQ14 is not becoming active. Check to make sure that the interrupt is isolated electrically from the original hard disk controller's IRQ14.

If at power on, the drive does not ever spin up or does not spin up until after the computer completes power on, it is

possible that RESET is either continually active or is electrically connected to some other signal.

If when reading a directory, it is inaccurate or does not change, it is possible that the adapter board is connected to the bit 7 when address 3F7 is read.

If the computer completes its power on sequence before the drive is up completely and subsequently gets a 17xx error of some sort, and if a subsequent warm boot is successful, it is possible the BIOS is expecting a different status at power on before the system is ready. Either delay the power on sequence or change the BIOS to expect a 00 status before the drive become ready.

NON SYSTEM DISK OR DISK ERROR. This could occur if no partition was made active by FDISK.