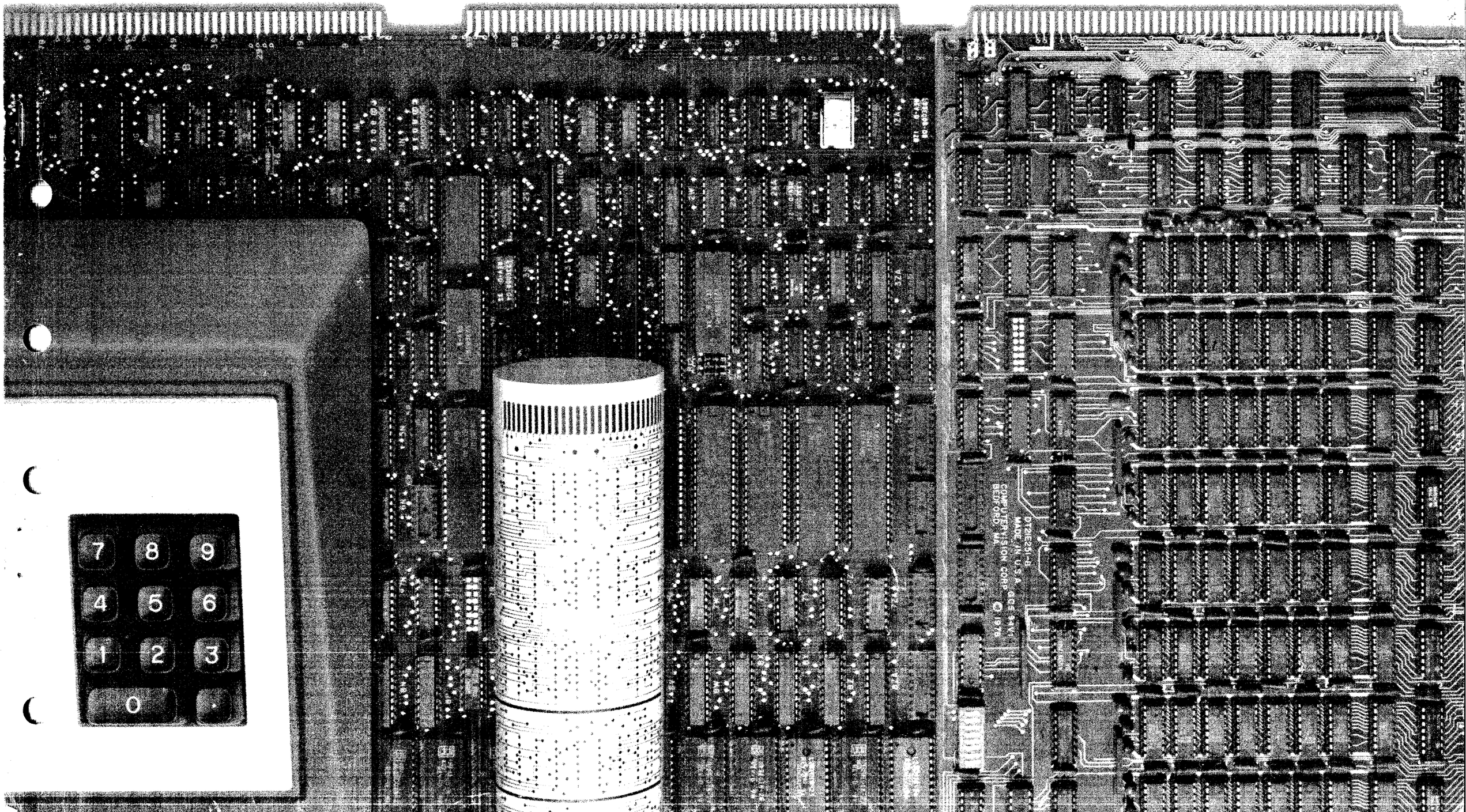
COMPUTERVISION

Technical

Computervision Graphics Processor (CGP)
(CGP 80/180/100/200)
Logic Diagrams



Document control number: 73-00406

Name _____

Computervision Graphics Processor (CGP)
(CGP 80/180/100/200)

Logic Diagrams

Logic diagrams pertain to:

- CGP 80*
- CGP 180*
- CGP 100 (A, B, and C)
- CGP 200 (A and B)
- CGP 200 (C)*

*Also need EACPU/ICP Logic Diagrams

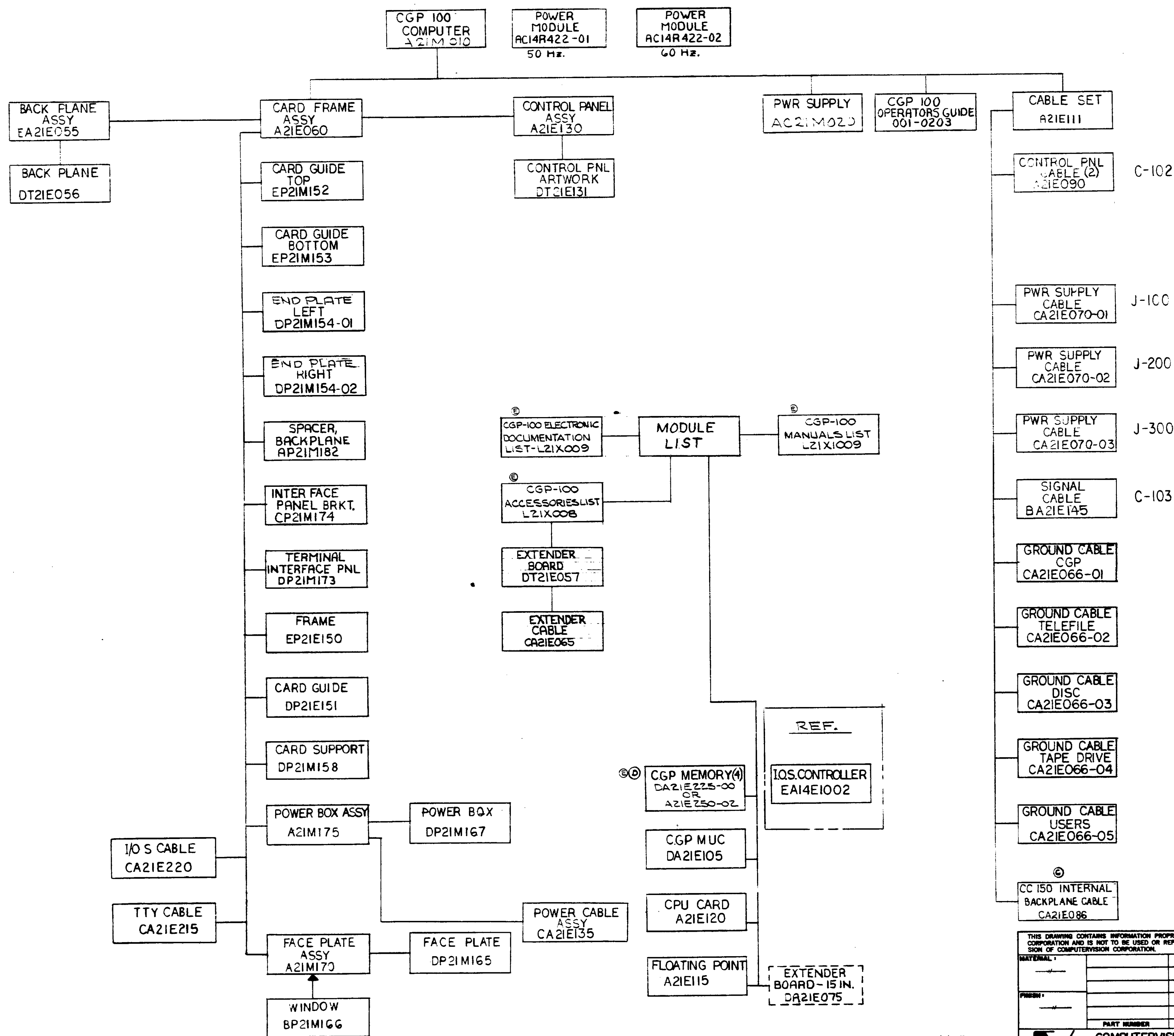
Order No. 001-00573

Table of Contents

Introduction

This manual contains the logic diagrams for the current models of the CGP line of Computervision Graphics Processors. This line includes the CGP-100 A, B. and C, CGP-180, and CGP-200 A, B, and C. To use this manual first determine which machine you are working on. Consult the family tree for a listing of boards that are part of that system. Next determine which boards (modules) you are interested in and then refer to the diagrams for the particular module. These are listed in the Table of Contents. The logic diagrams for the Extended Address Central Processing Unit (EACPU) and the Intelligent Control Panel (ICP) are shown in a separate publication "Extended Address Central Processing Unit (EACPU)/Intelligent Control Panel (ICP) Logic Diagrams". Order No. 001-00567.

Section 1
Computervision Graphics Processors (CGP) Family Trees



DX21Y007 E

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SYM	REVISION DESCRIPTION
E	ECO# 3386
D	ECO# 3195
C	ECO# 3126
B	ECO# 3004
A	REL ECO # 2594

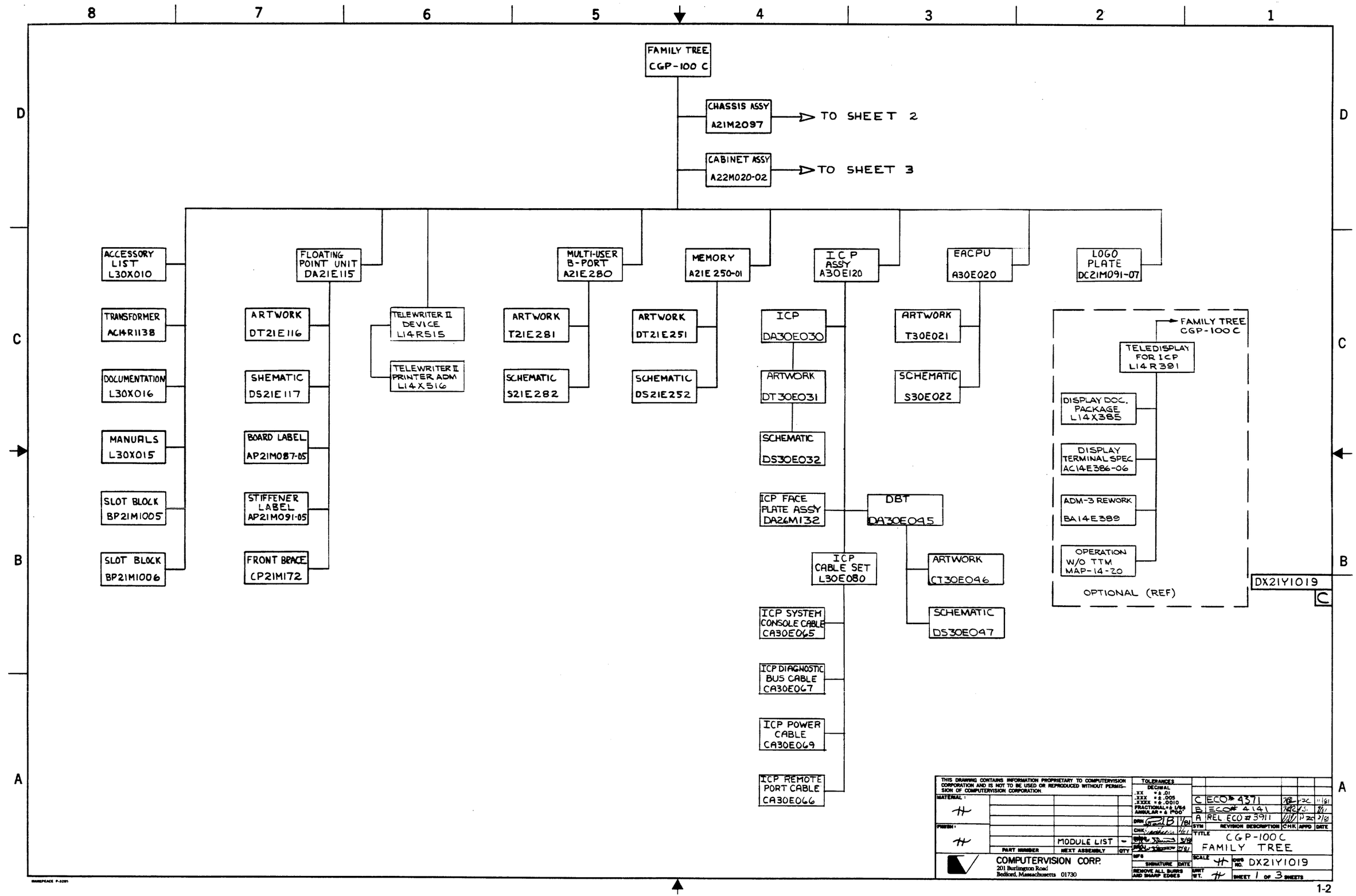
TITLE: FAMILY TREE CGP

COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803

DWG NO. DX21Y007

REV A = REV 4

1-1



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MATERIAL: #

FINISH: #

PART NUMBER	NEXT ASSEMBLY	QTY
	MODULE LIST	-

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN JB 1/81
CHK
ENGR
MFG
SIGNATURE DATE

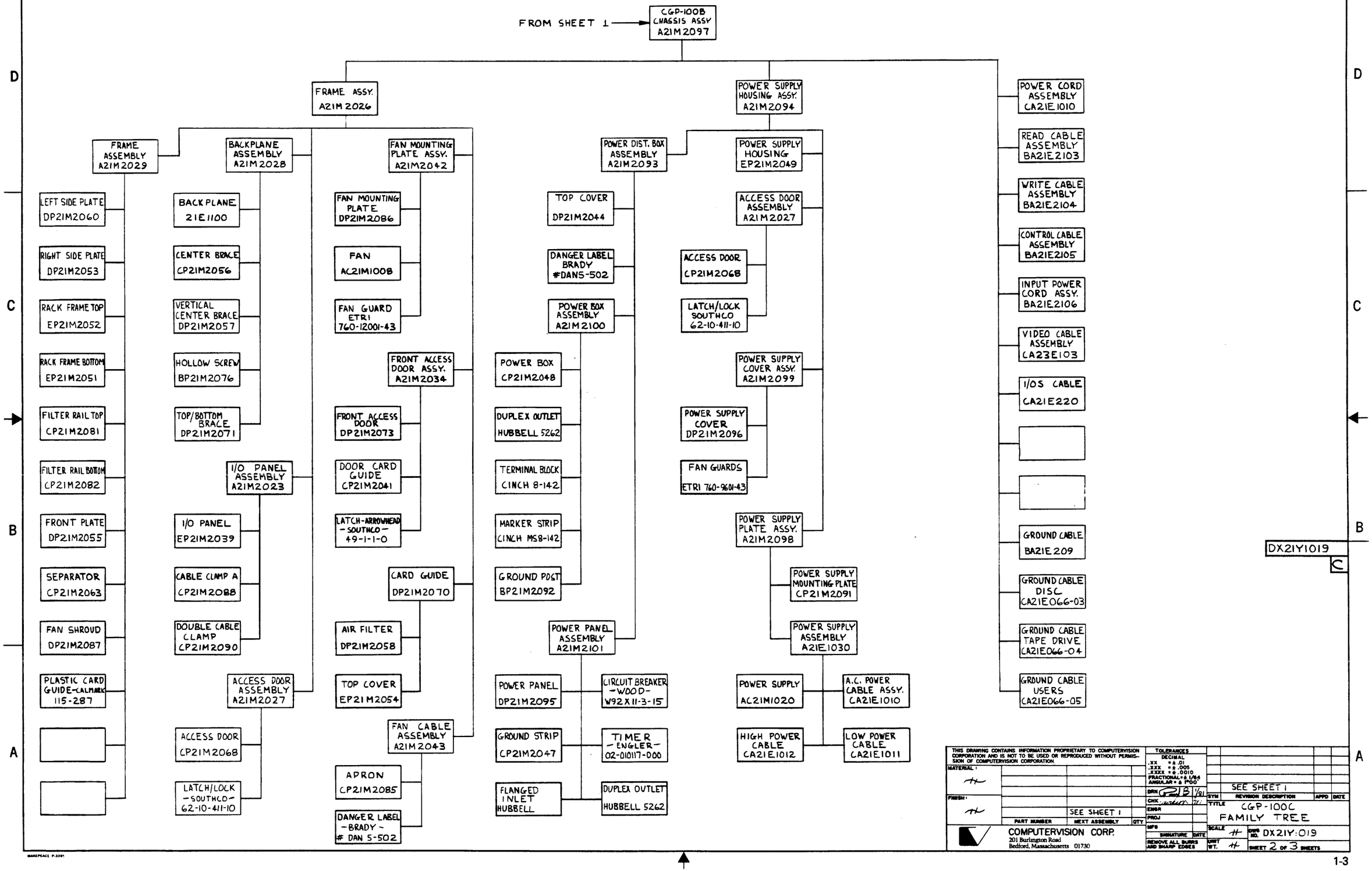
REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
C	ECO# 9371			11/81
B	ECO# 4141			7/81
A	REL ECO# 3911			2/81

TITLE
CGP-100C
FAMILY TREE

SCALE # DWG NO. DX21Y1019

SHEET 1 OF 3 SHEETS



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PART NUMBER	NEXT ASSEMBLY	QTY
	SEE SHEET 1	

TOLERANCES DECIMAL .XX ± .01, .XXX ± .005, .XXXX ± .0010, FRACTIONAL ± 1/64, ANGULAR ± 1°00'

REMOVE ALL BURRS AND SHARP EDGES

DRN RJB 1/91
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

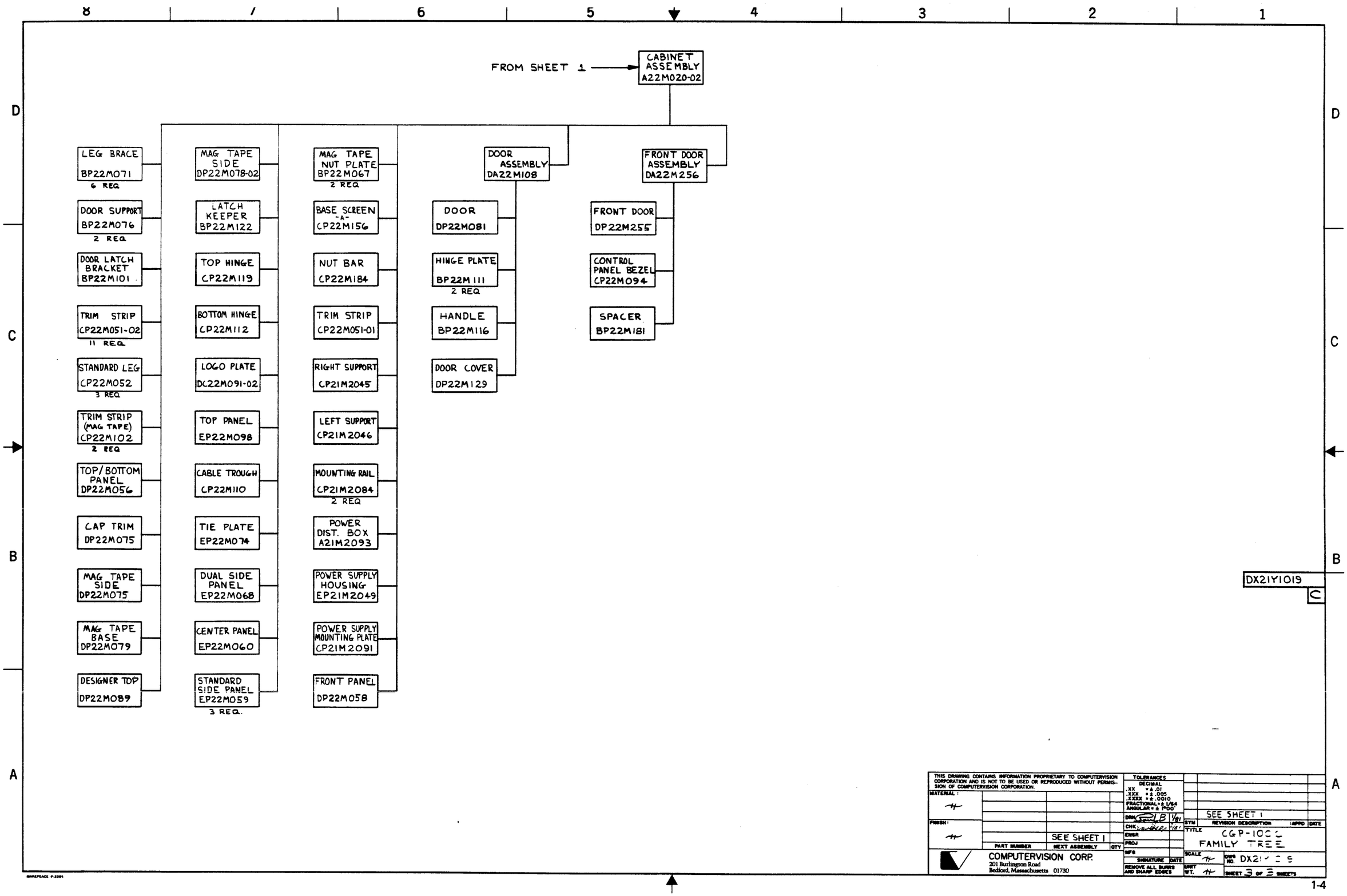
SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHEET 1		

TITLE CGP-100C FAMILY TREE

SCALE H DWG NO. DX21Y1019

UNIT WT. H SHEET 2 OF 3 SHEETS

MAKEPEACE P-3291



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MATERIAL: —

FINISH: —

PART NUMBER	NEXT ASSEMBLY	QTY
	SEE SHEET 1	

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN [illegible] 1/81
CHK [illegible] 1/81
ENGR
PROJ
MFG
SIGNATURE DATE

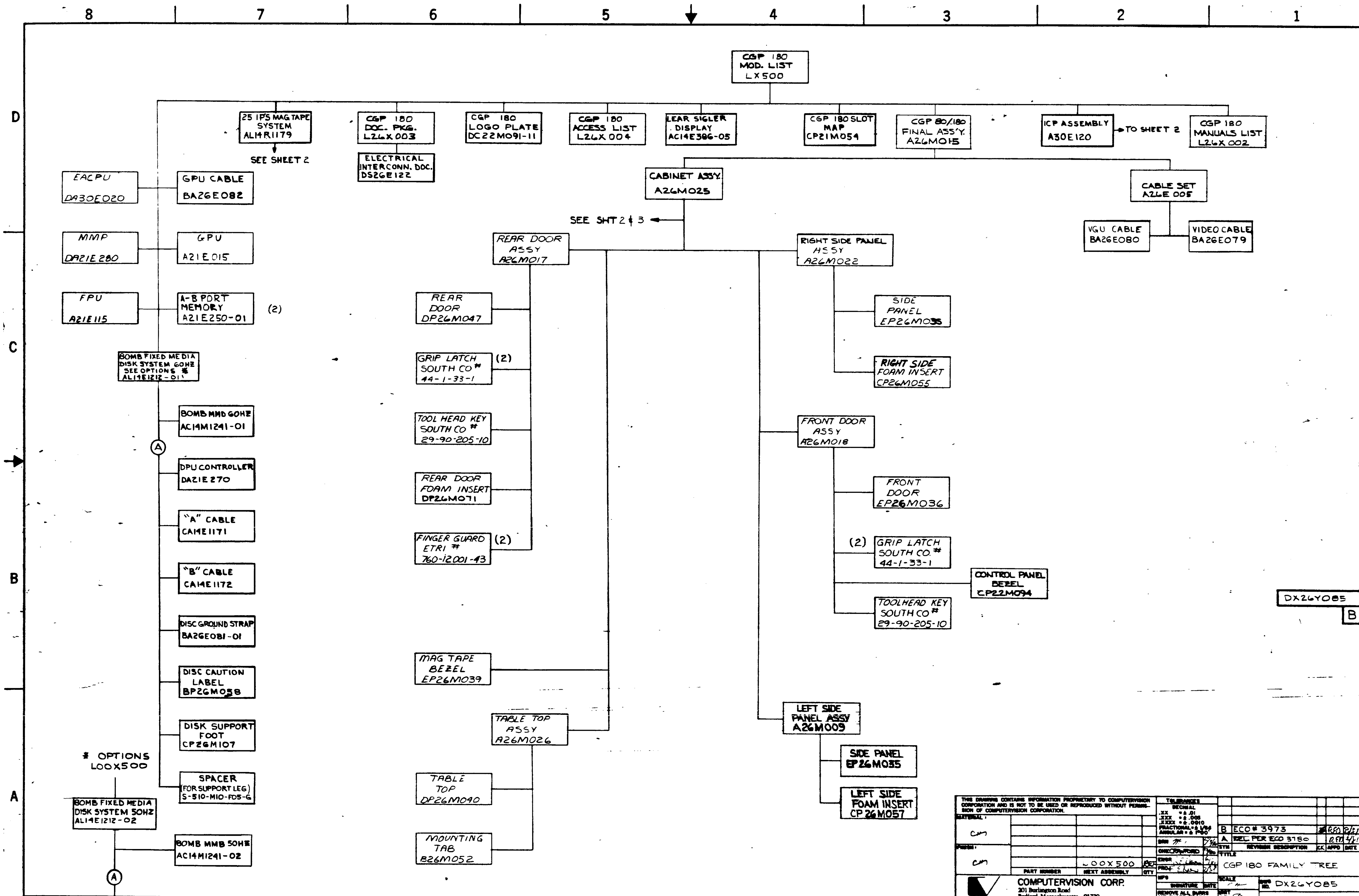
REMOVE ALL BURRS AND SHARP EDGES

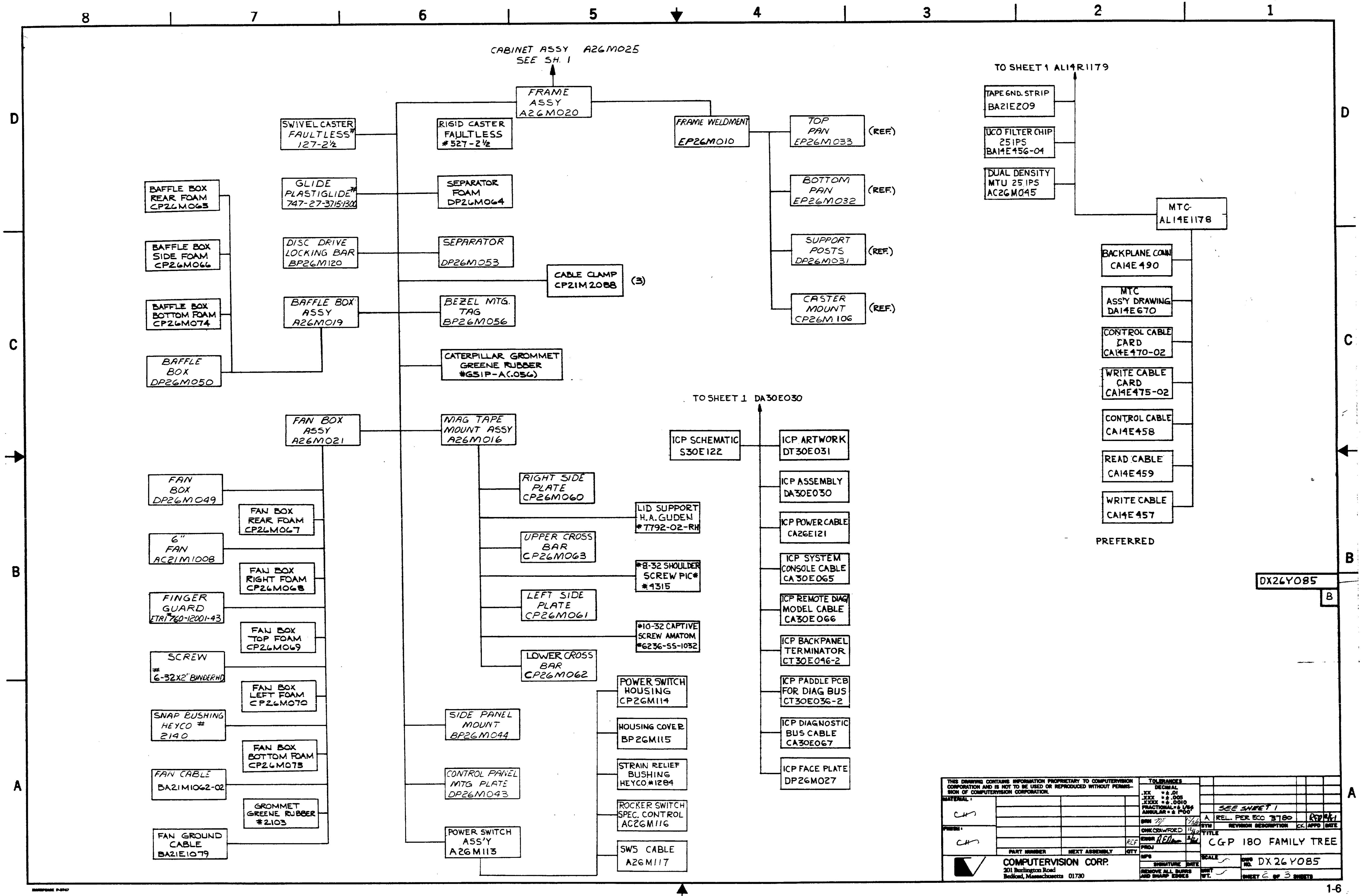
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHEET 1		

TITLE: CGP-100C FAMILY TREE

SCALE —
DWG NO. DX21Y1015
UNIT WT. —
SHEET 3 OF 3 SHEETS


CGP 180 MOD. LIST LX500
25 IPS MAG TAPE SYSTEM AL14R1179
SEE SHEET 2
CGP 180 DOC. PKG. L26X003
ELECTRICAL INTERCONN. DOC. DS26E122
CGP 180 LOGO PLATE DC22M091-11
CGP 180 ACCESS LIST L26X004
LEAR SIGLER DISPLAY AC14E386-05
CGP 180 SLOT MAP CP21M054
CGP 80/180 FINAL ASS'Y. A26M015
ICP ASSEMBLY A30E120
TO SHEET 2
CGP 180 MANUALS LIST L26X002
EACPU DA30E020
GPU CABLE BA26E082
MMP DA21E280
GPU A21E015
FPU A21E115
A-B PORT MEMORY A21E250-01
(2)
80MB FIXED MEDIA DISK SYSTEM 60HZ SEE OPTIONS * AL14E1212-01
80MB MMD 60HZ AC14M1241-01
A
DPU CONTROLLER DA21E270
"A" CABLE CA14E1171
"B" CABLE CA14E1172
DISC GROUND STRAP BA26E081-01
DISC CAUTION LABEL BP26M058
DISK SUPPORT FOOT CP26M107
SPACER (FOR SUPPORT LEG) S-510-M10-F05-G
* OPTIONS L00X500
80MB FIXED MEDIA DISK SYSTEM 50HZ AL14E1212-02
80MB MMB 50HZ AC14M1241-02
A
CABINET ASSY. A26M025
SEE SHT 2 & 3
REAR DOOR ASSY A26M017
REAR DOOR DP26M047
GRIP LATCH SOUTH CO # 44-1-33-1
(2)
TOOL HEAD KEY SOUTH CO # 29-90-205-10
REAR DOOR FOAM INSERT DP26M071
FINGER GUARD ETRI # 760-12001-43
(2)
MAG TAPE BEZEL EP26M039
TABLE TOP ASSY A26M026
TABLE TOP DP26M040
MOUNTING TAB B26M052
RIGHT SIDE PANEL ASSY A26M022
SIDE PANEL EP26M035
RIGHT SIDE FOAM INSERT CP26M055
FRONT DOOR ASSY A26M018
FRONT DOOR EP26M036
(2)
GRIP LATCH SOUTH CO. # 44-1-33-1
CONTROL PANEL BEZEL CP22M094
TOOLHEAD KEY SOUTH CO # 29-90-205-10
LEFT SIDE PANEL ASSY A26M009
SIDE PANEL EP26M035
LEFT SIDE FOAM INSERT CP26M057
CABLE SET A26E005
VGU CABLE BA26E080
VIDEO CABLE BA26E079
DX26Y085
B
B ECO# 3973
A REL PER ECO 3180
L00X500
CGP 180 FAMILY TREE
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730
DX26Y085
SHEET 1 OF 3 SHEETS


CABINET ASSY A26M025
SEE SH. 1
FRAME ASSY A26M020
SWIVEL CASTER FAULTLESS# 127-2½
RIGID CASTER FAULTLESS #527-2½
FRAME WELDMENT EP26M010
TOP PAN EP26M033 (REF.)
BOTTOM PAN EP26M032 (REF.)
SUPPORT POSTS DP26M031 (REF.)
CASTER MOUNT CP26M106 (REF.)
BAFFLE BOX REAR FOAM CP26M065
BAFFLE BOX SIDE FOAM CP26M066
BAFFLE BOX BOTTOM FOAM CP26M074
BAFFLE BOX DP26M050
GLIDE PLASTIGLIDE# 747-27-3715130
SEPARATOR FOAM DP26M064
DISC DRIVE LOCKING BAR BP26M120
SEPARATOR DP26M053
CABLE CLAMP CP21M2088 (3)
BAFFLE BOX ASSY A26M019
BEZEL MTG. TAG BP26M056
CATERPILLAR GROMMET GREENE RUBBER #G51P-A(.056)
FAN BOX ASSY A26M021
MAG TAPE MOUNT ASSY A26M016
FAN BOX DP26M049
FAN BOX REAR FOAM CP26M067
6" FAN AC21M1008
FAN BOX RIGHT FOAM CP26M068
FINGER GUARD ETRI #760-12001-43
FAN BOX TOP FOAM CP26M069
SCREW #6-32X2" BINDERHD
FAN BOX LEFT FOAM CP26M070
SNAP BUSHING HEYCO #2140
FAN BOX BOTTOM FOAM CP26M073
FAN CABLE BA21M1062-02
GROMMET GREENE RUBBER #2103
FAN GROUND CABLE BA21E1079
RIGHT SIDE PLATE CP26M060
LID SUPPORT H.A. GUDEN #T792-02-RH
UPPER CROSS BAR CP26M063
#8-32 SHOULDER SCREW PIC# #4315
LEFT SIDE PLATE CP26M061
#10-32 CAPTIVE SCREW AMATOM #6236-SS-1032
LOWER CROSS BAR CP26M062
SIDE PANEL MOUNT BP26M044
CONTROL PANEL MTG PLATE DP26M043
POWER SWITCH ASS'Y A26M113
POWER SWITCH HOUSING CP26M114
HOUSING COVER BP26M115
STRAIN RELIEF BUSHING HEYCO #1284
ROCKER SWITCH SPEC. CONTROL AC26M116
SWS CABLE A26M117
TO SHEET 1 DA30E030
ICP SCHEMATIC S30E122
ICP ARTWORK DT30E031
ICP ASSEMBLY DA30E030
ICP POWER CABLE CA26E121
ICP SYSTEM CONSOLE CABLE CA30E065
ICP REMOTE DIAG MODEL CABLE CA30E066
ICP BACKPANEL TERMINATOR CT30E046-2
ICP PADDLE PCB FOR DIAG BUS CT30E036-2
ICP DIAGNOSTIC BUS CABLE CA30E067
ICP FACE PLATE DP26M027
TO SHEET 1 AL14R1179
TAPE GND. STRIP BA21E209
UCO FILTER CHIP 25 IPS BA14E456-04
DUAL DENSITY MTU 25 IPS AC26M045
MTC AL14E1178
BACKPLANE CONN CA14E490
MTC ASS'Y DRAWING DA14E670
CONTROL CABLE CARD CA14E470-02
WRITE CABLE CARD CA14E475-02
CONTROL CABLE CA14E458
READ CABLE CA14E459
WRITE CABLE CA14E457
PREFERRED
DX26Y085
B
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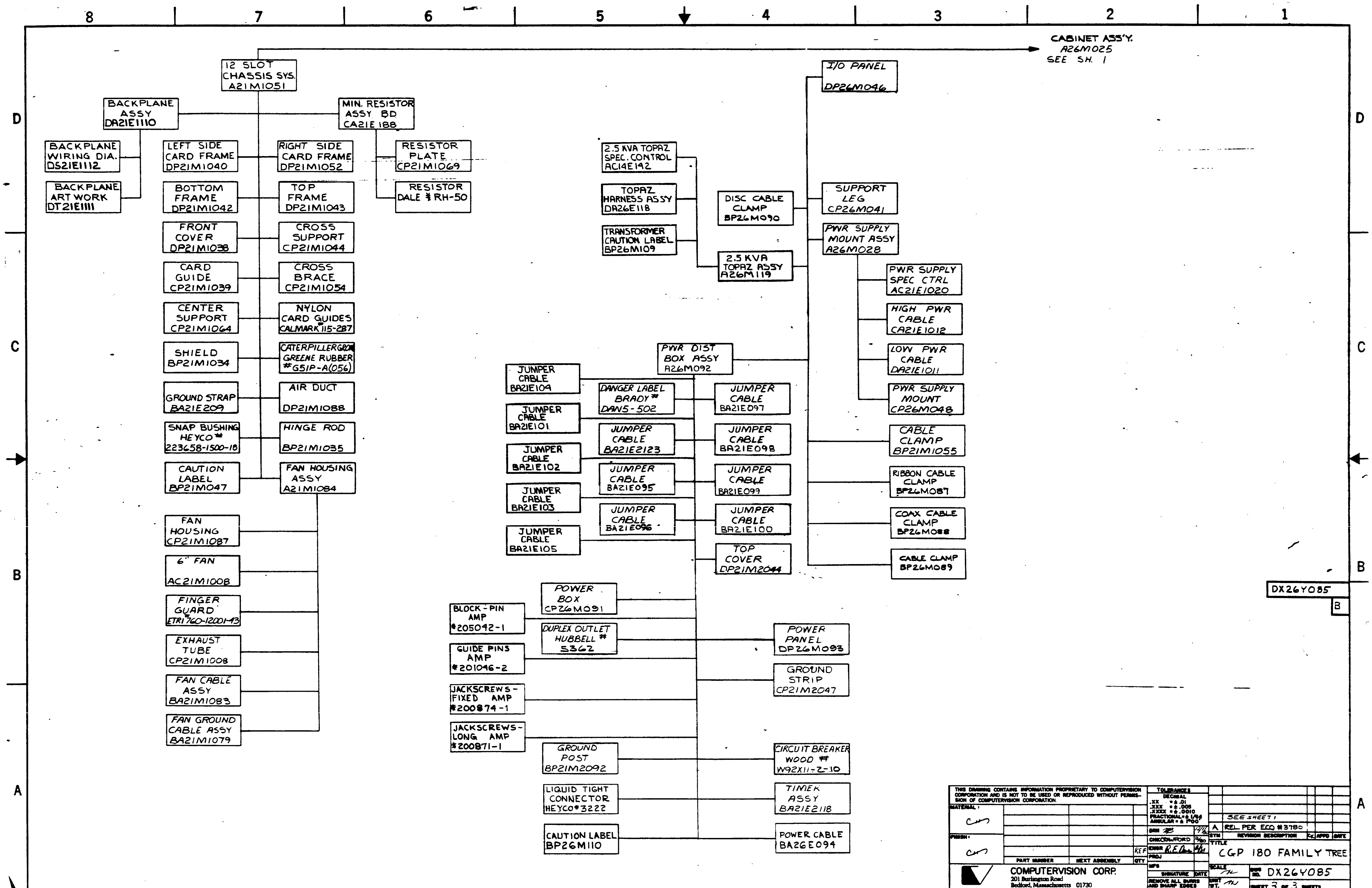
SEE SHEET 1
A REL. PER ECO 3780
CGP 180 FAMILY TREE
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730
DX26Y085
SHEET 2 OF 3 SHEETS



8 7 6 5 4 3 2 1
D C B A
CABINET ASS'Y. A26M025 SEE SH. 1
12 SLOT CHASSIS SYS. A21M1051
BACKPLANE ASSY DA21E1110
MIN. RESISTOR ASSY BD CA21E188
BACKPLANE WIRING DIA. DS21E1112
BACKPLANE ART WORK DT21E1111
LEFT SIDE CARD FRAME DP21M1040
RIGHT SIDE CARD FRAME DP21M1052
RESISTOR PLATE CP21M1069
RESISTOR DALE # RH-50
BOTTOM FRAME DP21M1042
TOP FRAME DP21M1043
FRONT COVER DP21M1038
CROSS SUPPORT CP21M1044
CARD GUIDE CP21M1039
CROSS BRACE CP21M1054
CENTER SUPPORT CP21M1064
NYLON CARD GUIDES CALMARK#115-287
SHIELD BP21M1034
CATERPILLER GROM GREENE RUBBER #G51P-A(056)
GROUND STRAP BA21E209
AIR DUCT DP21M1088
SNAP BUSHING HEYCO # 223658-1500-18
HINGE ROD BP21M1035
CAUTION LABEL BP21M047
FAN HOUSING ASSY A21M1084
FAN HOUSING CP21M1087
6" FAN AC21M1008
FINGER GUARD ETRI 760-1200I-43
EXHAUST TUBE CP21M1008
FAN CABLE ASSY BA21M1083
FAN GROUND CABLE ASSY BA21M1079
I/O PANEL DP26M046
2.5 KVA TOPAZ SPEC. CONTROL AC14E192
TOPAZ HARNESS ASSY DA26E118
TRANSFORMER CAUTION LABEL BP26M109
DISC CABLE CLAMP BP26M090
2.5 KVA TOPAZ ASSY A26M119
SUPPORT LEG CP26M041
PWR SUPPLY MOUNT ASSY A26M028
PWR SUPPLY SPEC CTRL AC21E1020
HIGH PWR CABLE CA21E1012
LOW PWR CABLE DA21E1011
PWR SUPPLY MOUNT CP26M048
CABLE CLAMP BP21M1055
RIBBON CABLE CLAMP BP26M087
COAX CABLE CLAMP BP26M088
CABLE CLAMP BP26M089
PWR DIST BOX ASSY A26M092
JUMPER CABLE BA21E104
JUMPER CABLE BA21E101
JUMPER CABLE BA21E102
JUMPER CABLE BA21E103
JUMPER CABLE BA21E105
DANGER LABEL BRADY # DAN5-502
JUMPER CABLE BA21E2123
JUMPER CABLE BA21E095
JUMPER CABLE BA21E096
JUMPER CABLE BA21E097
JUMPER CABLE BA21E098
JUMPER CABLE BA21E099
JUMPER CABLE BA21E100
TOP COVER DP21M2044
POWER BOX CP26M091
BLOCK-PIN AMP #205092-1
DUPLEX OUTLET HUBBELL # 5362
GUIDE PINS AMP #201046-2
JACKSCREWS-FIXED AMP #200874-1
JACKSCREWS-LONG AMP #200871-1
POWER PANEL DP26M093
GROUND STRIP CP21M2047
GROUND POST BP21M2092
LIQUID TIGHT CONNECTOR HEYCO #3222
CAUTION LABEL BP26M110
CIRCUIT BREAKER WOOD # W92X11-2-10
TIMER ASSY BA21E2118
POWER CABLE BA26E094
DX26Y085 B
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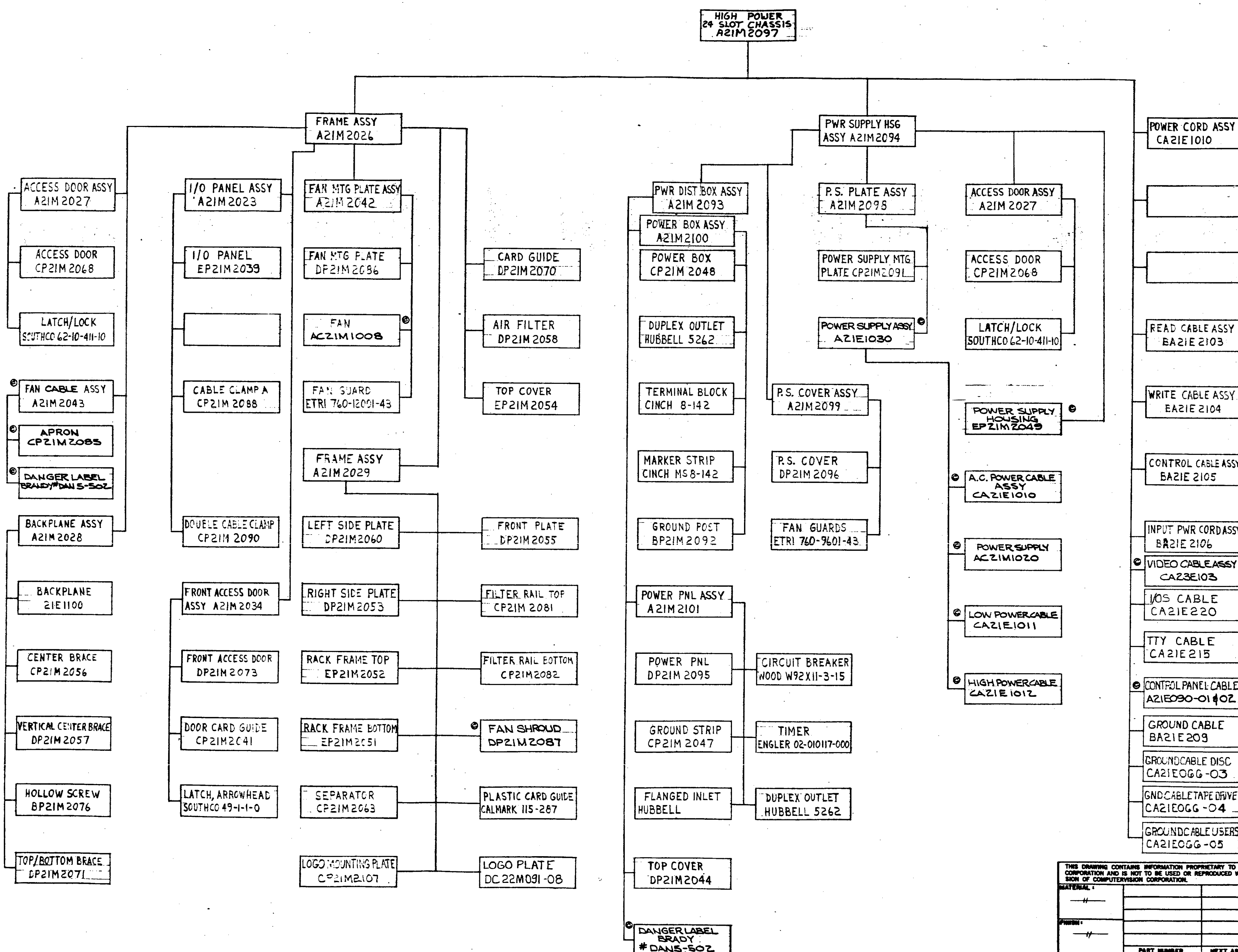
MATERIAL:
FINISH:
PART NUMBER
NEXT ASSEMBLY
QTY
TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ± 1/64 ANGULAR ± 0°30'
REF
SEE SHEET 1
A REL. PER ECO #3780
SYM REVISION DESCRIPTION
TITLE CGP 180 FAMILY TREE
COMPUTERVISION CORP. 201 Burlington Road Bedford, Massachusetts 01730
REMOVE ALL BURRS AND SHARP EDGES
DWG NO. DX26Y085
SHEET 3 OF 3 SHEETS



DX2IY2007 C

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SYM	REVISION DESCRIPTION	CHK	APPD	DATE
C	ECO# 3586		RED	9/80
B	ECO# 3568		RC	8/80
A	REL. ECO 3538	RED	RED	4/80

TOLERANCES: DECIMAL .XX ±.01, .XXX ±.005, .XXXX ±.0010; FRACTIONAL ±1/64; ANGULAR ±1/2°

MATERIAL: —
FINISH: —
PART NUMBER | NEXT ASSEMBLY | QTY

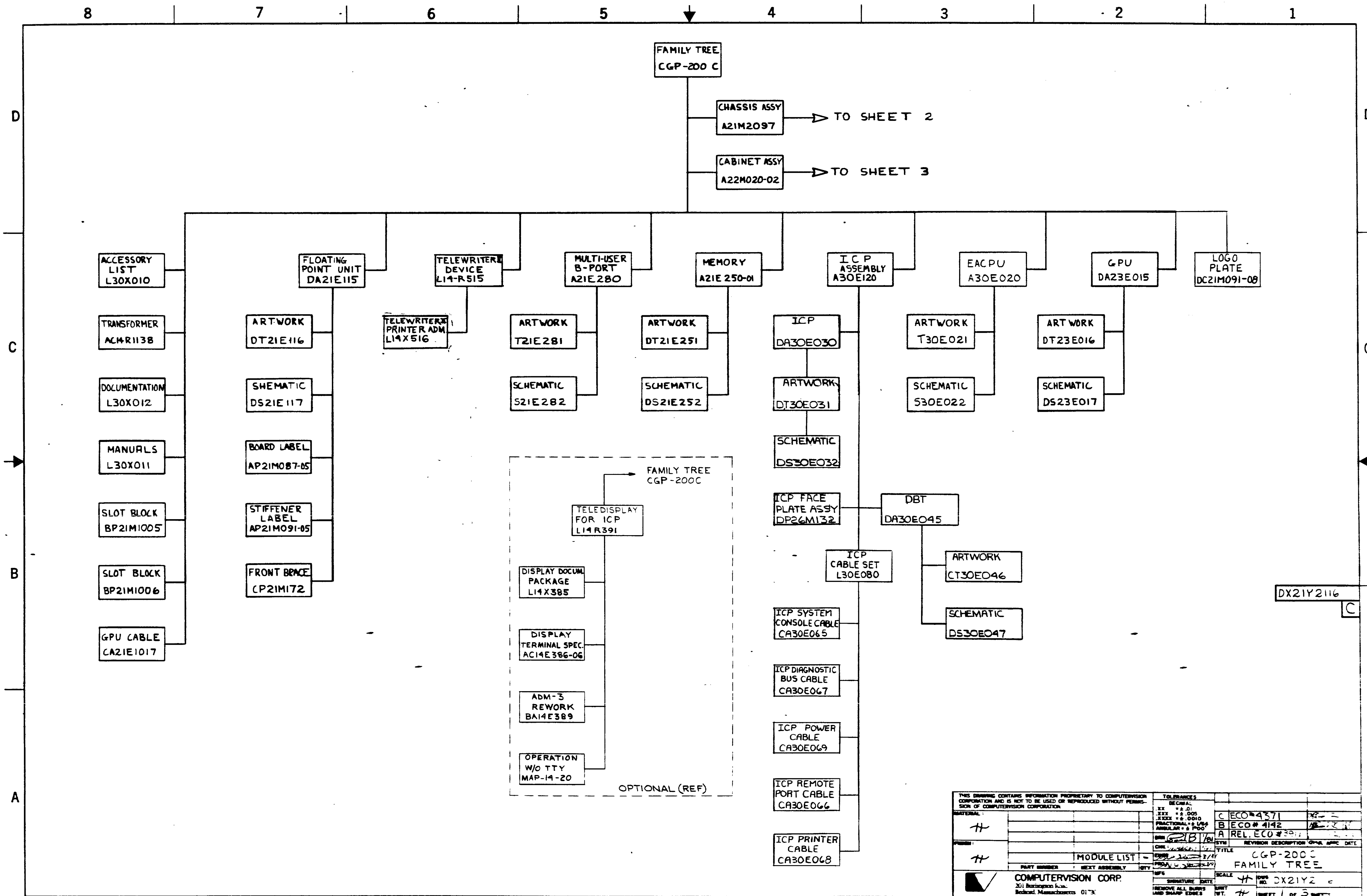
DRN R. Fortier | CHK | ENGR | PROJ

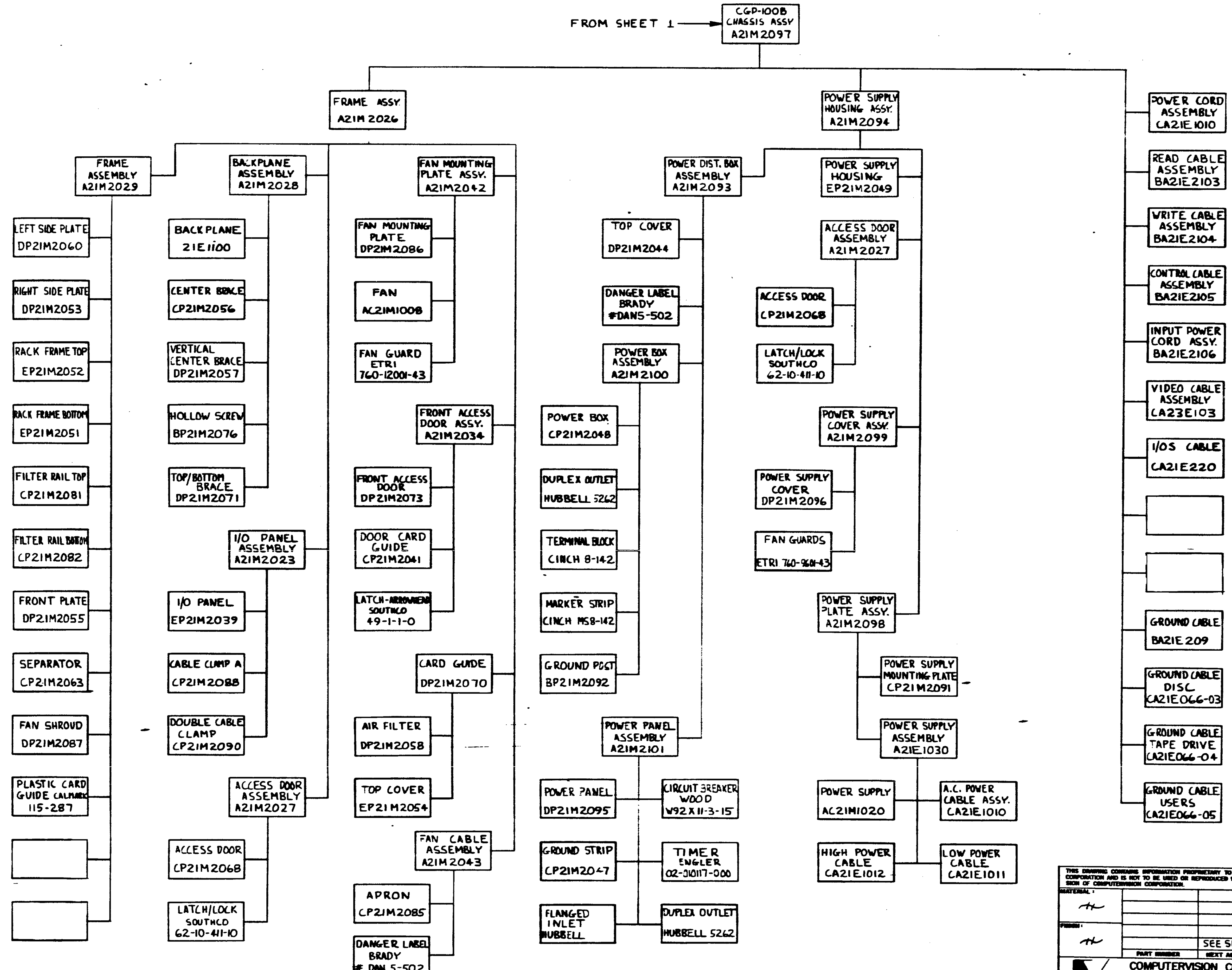
TITLE: FAMILY TREE CGP-200

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

SCALE — | DWG NO. DX2IY2007 | SHEET 1 OF 1

REMOVE ALL BURRS AND SHARP EDGES


FAMILY TREE CGP-200 C
CHASSIS ASSY A21M2097
TO SHEET 2
CABINET ASSY A22M020-02
TO SHEET 3
ACCESSORY LIST L30X010
TRANSFORMER AC14R1138
DOCUMENTATION L30X012
MANUALS L30X011
SLOT BLOCK BP21M1005
SLOT BLOCK BP21M1006
GPU CABLE CA21E1017
FLOATING POINT UNIT DA21E115
ARTWORK DT21E116
SHEMATIC DS21E117
BOARD LABEL AP21M087-05
STIFFENER LABEL AP21M091-05
FRONT BRACE CP21M172
TELEWRITER II DEVICE L14-R515
TELEWRITER II PRINTER ADM L14X516
MULTI-USER B-PORT A21E280
ARTWORK T21E281
SCHEMATIC S21E282
MEMORY A21E250-01
ARTWORK DT21E251
SCHEMATIC DS21E252
ICP ASSEMBLY A30E120
ICP DA30E030
ARTWORK DT30E031
SCHEMATIC DS30E032
ICP FACE PLATE ASSY DP26M132
DBT DA30E045
ARTWORK CT30E046
SCHEMATIC DS30E047
ICP CABLE SET L30E080
ICP SYSTEM CONSOLE CABLE CA30E065
ICP DIAGNOSTIC BUS CABLE CA30E067
ICP POWER CABLE CA30E069
ICP REMOTE PORT CABLE CA30E066
ICP PRINTER CABLE CA30E068
EACPU A30E020
ARTWORK T30E021
SCHEMATIC S30E022
GPU DA23E015
ART WORK DT23E016
SCHEMATIC DS23E017
LOGO PLATE DC21M091-08
FAMILY TREE CGP-200C
TELEDISPLAY FOR ICP L14R391
DISPLAY DOCUM. PACKAGE L14X385
DISPLAY TERMINAL SPEC. AC14E386-06
ADM-3 REWORK BA14E389
OPERATION W/O TTY MAP-14-20
OPTIONAL (REF)
DX21Y2116
C
COMPUTERVISION CORP.
MODULE LIST
TITLE CGP-200C FAMILY TREE
DWG NO. DX21Y2
SHEET 1 OF 3 SHEETS



DX21Y2116 C

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SEE SHEET 1

TITLE: CGP-200C FAMILY TREE

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

DWG NO. DX21Y2116

SHEET 2 OF 3 SHEETS

FROM SHEET 1

CABINET ASSEMBLY
A22M020-02

- LEG BRACE BP22M071 — 6 REQ
- DOOR SUPPORT BP22M076 — 2 REQ
- DOOR LATCH BRACKET BP22M101
- TRIM STRIP CP22M051-02 — 11 REQ
- STANDARD LEG CP22M052 — 3 REQ
- TRIM STRIP (MAG TAPE) CP22M102 — 2 REQ
- TOP/BOTTOM PANEL DP22M056
- CAP TRIM DP22M075
- MAG TAPE SIDE DP22M075
- MAG TAPE BASE DP22M079
- DESIGNER TOP DP22M089
- MAG TAPE SIDE DP22M078-02
- LATCH-KEEPER BP22M122
- TOP HINGE CP22M119
- BOTTOM HINGE CP22M112
- LOGO PLATE DC22M091-02
- TOP PANEL EP22M098
- CABLE TROUGH CP22M110
- TIE PLATE EP22M074
- DUAL SIDE PANEL EP22M068
- CENTER PANEL EP22M060
- STANDARD SIDE PANEL EP22M059 — 3 REQ.
- MAG TAPE NUT PLATE BP22M067 — 2 REQ
- BASE SCREEN -A- CP22M156
- NUT BAR CP22M184
- TRIM STRIP CP22M051-01
- RIGHT SUPPORT CP21M2045
- LEFT SUPPORT CP21M2046
- MOUNTING RAIL CP21M2084 — 2 REQ
- POWER DIST. BOX A21M2093
- POWER SUPPLY HOUSING EP21M2049
- POWER SUPPLY MOUNTING PLATE CP21M2091
- FRONT PANEL DP22M058

DOOR ASSEMBLY
DA22M108

- DOOR DP22M081
- HINGE PLATE BP22M111 — 2 REQ
- HANDLE BP22M116
- DOOR COVER DP22M129

FRONT DOOR ASSEMBLY
DA22M256

- FRONT DOOR DP22M255
- CONTROL PANEL BEZEL CP22M094
- SPACER BP22M181

DX21Y2116
C

MATERIAL: AS

FINISH: AS

PART NUMBER: SEE SHEET 1 — NEXT ASSEMBLY — QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN RLB 1/91
CHK 1/91
DSGN
PROJ
MFG
ENGINEERING — DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: CGP-200C FAMILY TREE

SCALE: AS — SIZE: D — DWG NO. DX21Y2116

WGHT: AS — SHEET 3 OF 3 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

Section 2
Backplanes

	CENTRAL PROCESSOR UNIT (CPU)	MULTIUSER CONTROLLER (MUC)	FLOATING POINT UNIT (FPU)	SYSTEM MEMORY 0	SYSTEM MEMORY 2	SYSTEM MEMORY 3	MAGNETIC TAPE CONTROLLER	DISK PROCESSING UNIT (DPU)	PROGRAMMABLE COMM UNIT (PCU)	OPTION SLOT 1	OPTION SLOT 2	ELECTROSTATIC PLOTTER	BOARD TYPE	200 ONLY: GPU MEMORY 1	200 ONLY: SYSTEM MEMORY 1 / GPU MEMORY 0	200 ONLY: GRAPHICS PROCESSOR UNIT (GPU)	VGU 8 / IOS 8	VGU 7 / IOS 7	VGU 6 / IOS 6	VGU 5 / IOS 5	VGU 4 / IOS 4	VGU 3 / IOS 3	VGU 2 / IOS 2	VGU 1 / IOS 1	OPTION SLOT 3
1	2	3	4	5	6	7	8	9	10	11	12	SLOT	13	14	15	16	17	18	19	20	21	22	23	24
												REV												
												DEVICE CODE												
												BAUD RATE												

7.50

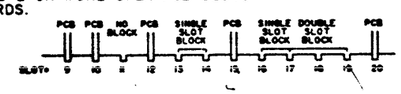
CGP-100 OR CGP-200 STANDARD SLOT CONFIGURATION

CGP S.N. _____

CAUTION:

1. USE ONLY COMPUTERVISION APPROVED PLASTIC CARD EJECTORS
THE USE IN THIS EQUIPMENT OF PRINTED CIRCUIT CARDS NOT EQUIPPED WITH AN EJECTOR APPROVED BY COMPUTERVISION CAN LEAD TO SERIOUS DAMAGE AND WARRANTY CANCELLATION.

2. TO INSURE AN OPTIMUM COOLING ENVIRONMENT IN THIS EQUIPMENT, USE COMPUTERVISION STANDARD SLOT BLOCKS. (CV P/N BP2IM1006 SINGLE, OR CV P/N BP2IM1005 DOUBLE) WHENEVER A SYSTEM HAS 2 OR MORE OPEN PCB SLOTS BETWEEN ADJACENT BOARDS.
FOR EXAMPLE:



P/N CP2IM044 REV A
S/N 081-10075
MADE IN U.S.A.

CP2IM044
A

16.90

NOTES:
1. VENDOR:
TECHPRINT INC
15 SIXTH ROAD
WOBURN, MA. 01801
2. COLOR: BLACK LETTERS ON WHITE BACKGROUND
3. .004 T-ICK FLEXIBLE VINYL ADHESIVE BACK
4. ARTWORK MASTER WILL BE SUPPLIED TO VENDOR BY DRAFTING DEPT.

MATERIAL: SEE NOTE 3
FINISH: SEE NOTE 2

PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

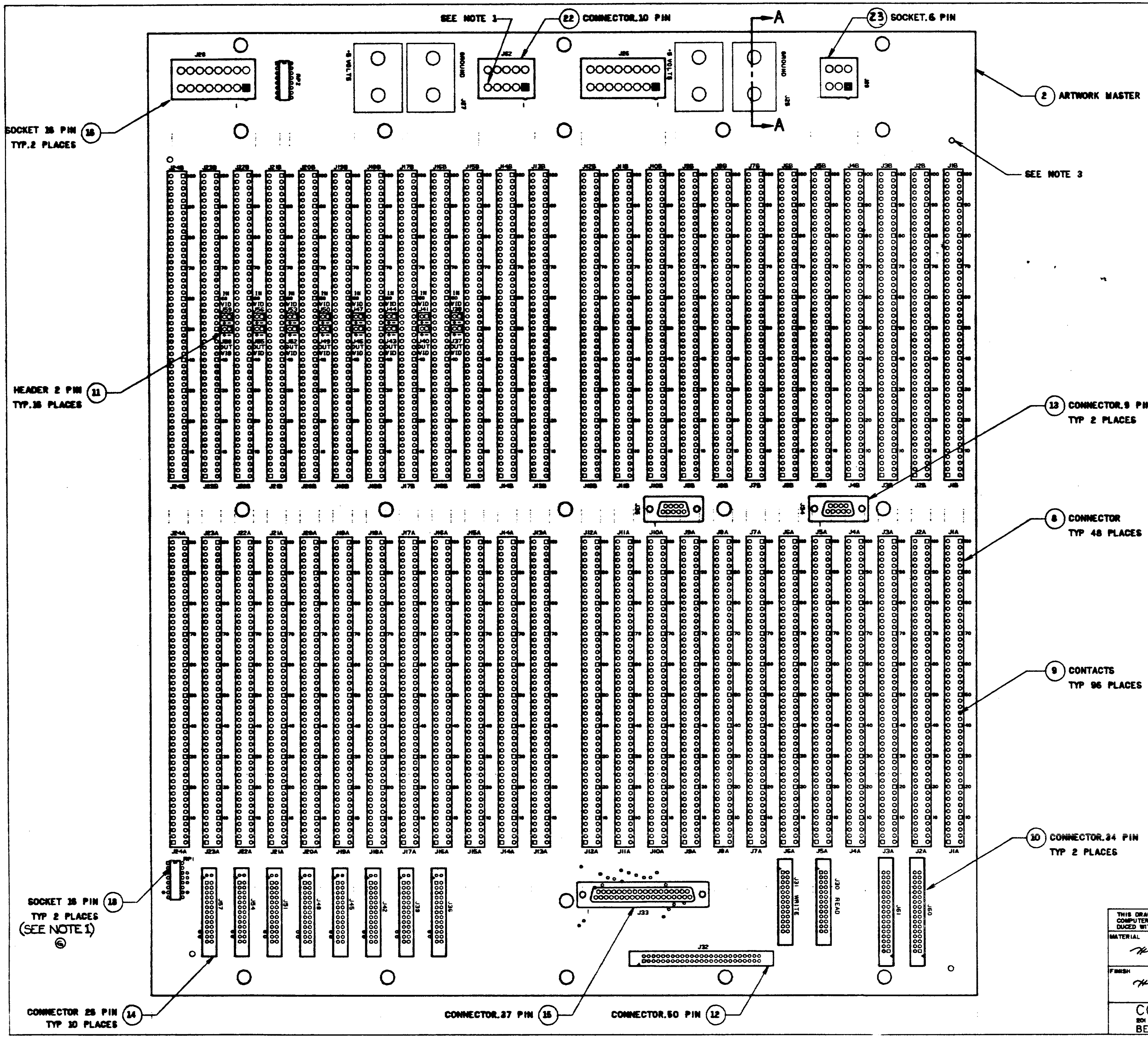
DRN
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

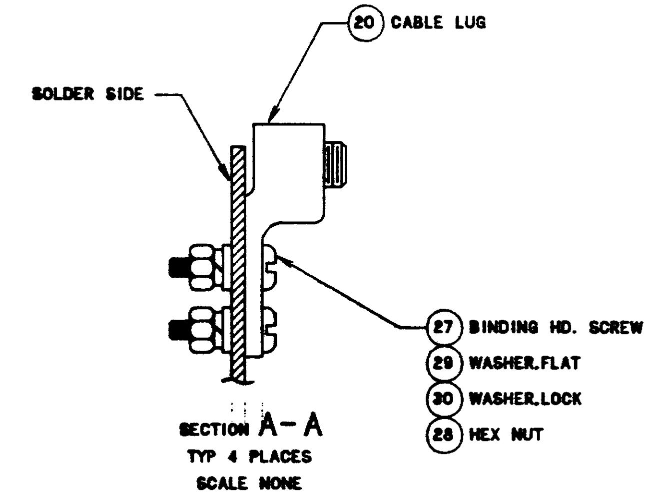
SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: CGP-100 OR CGP-200 STANDARD SLOT MAP

COMPUTERVISION CORP.
201 BURLINGTON RD ROUTE 62
BEDFORD, MASS 01730

SCALE: 1-1
UNIT WT.
DWG NO. CP2IM044
SHEET 01 SHEETS





NOTES:
1. DO NOT DESOCKET RP1 & RP2

CUTS FOR A&B ARTWORK
1. JA15-92

DA21E1100
G

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION				TOLERANCES DECIMAL .XX ±+.01 .XXX ±+.005 .XXXX ±+.0010 FRACTIONAL=±1/64 ANGULAR=± 1°00								
MATERIAL						G	ECO# 4169					
						F	ECO 3675					
				DRWN ROBINSON	6/80	E	ECO 3875					
FINISH		A21M2028	1	CHK R BRUCE		SYM	REVISION DESCRIPTION	CHK	APPD	DATE		
				ENGR N.TIDD	6/80	TITLE 24 SLOT BACKPLANE ASSEMBLY						
	PART NUMBER	NEXT ASSEMBLY	QTY	PROJ R. McAnday	6/80							
COMPUTERVISION CORP. 201 BURLINGTON ROAD ROUTE 62 BEDFORD, MASS. 01730				MFG		SCALE	DWG NO. DA21E1100					
				SIGNATURE	DATE							
				REMOVE ALL BURRS AND SHARP EDGES		UNIT WT.	SHT 1 OF 2 SHTS					

DA21E1100 G

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL

SEE SHT 1

PART NUMBER NEXT ASSEMBLY NEXT

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1 DEG

DRAWN

CHK

ENGR

PROJ

MFG

ENGINEERING DEPT

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP
201 BURLINGTON RD ROUTE 62
BEDFORD, MASS 01730

SEE SHT 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE 24 SLOT BACKPLANE ASSY

SCALE

SIZE C DWG NO. DA21E1100

WT.

SHEET 2 OF 2 SHEETS

J8B			
SIGNAL	PIN	PIN	SIGNAL
GND	99	100	GND
+5V/1	97	98	+5V/1
DATA6/L	95	96	
WRITPROT/L	93	94	PARITYER/L
	91	92	GND
GND	89	90	DCPOK/H
MRST/L	87	88	
MEMWRT/L	85	86	
LDMAR/L	83	84	+12V/1
-5V/1	81	82	DATA2/L
MBUSD0/L	79	80	
MBUSI1/L	77	78	
DATA10/L	75	76	
DATA3/L	73	74	MBST/L
-12V/1	71	72	-12V/1
	69	70	MCLK/L
	67	68	
DATA1/L	65	66	DATA15/L
DATA9/L	63	64	DATA13/L
DATA4/L	61	62	DATA0/L
DATA12/L	59	60	DATA8/L
DATA5/L	57	58	DATA11/L
DATA7/L	55	56	DATA14/L
	53	54	
	51	52	
	49	50	GND
ACCESSPROT/L	47	48	
READMEM/L	45	46	+12V/1
MBUS3/L	43	44	MBUS2/L
RQENB/L	41	42	MBUS4/L
OVFLO/H	39	40	
DCHL/H	37	38	
DCHR/L	35	36	
DCHD/H	33	34	
	31	32	MBUSS/L
INTR/L	29	30	
	27	28	
	25	26	
	23	24	
DCHM/L	21	22	
	19	20	
DCHM0/L	17	18	
	15	16	MBUS8/L
	13	14	MBUS7/L
	11	12	MBUS6/L
MBUS9/L	9	10	
	7	8	MBUS10/L
MBUS11/L	5	6	
+5V/1	3	4	+5V/1
GND	1	2	GND
SIGNAL	PIN	PIN	SIGNAL

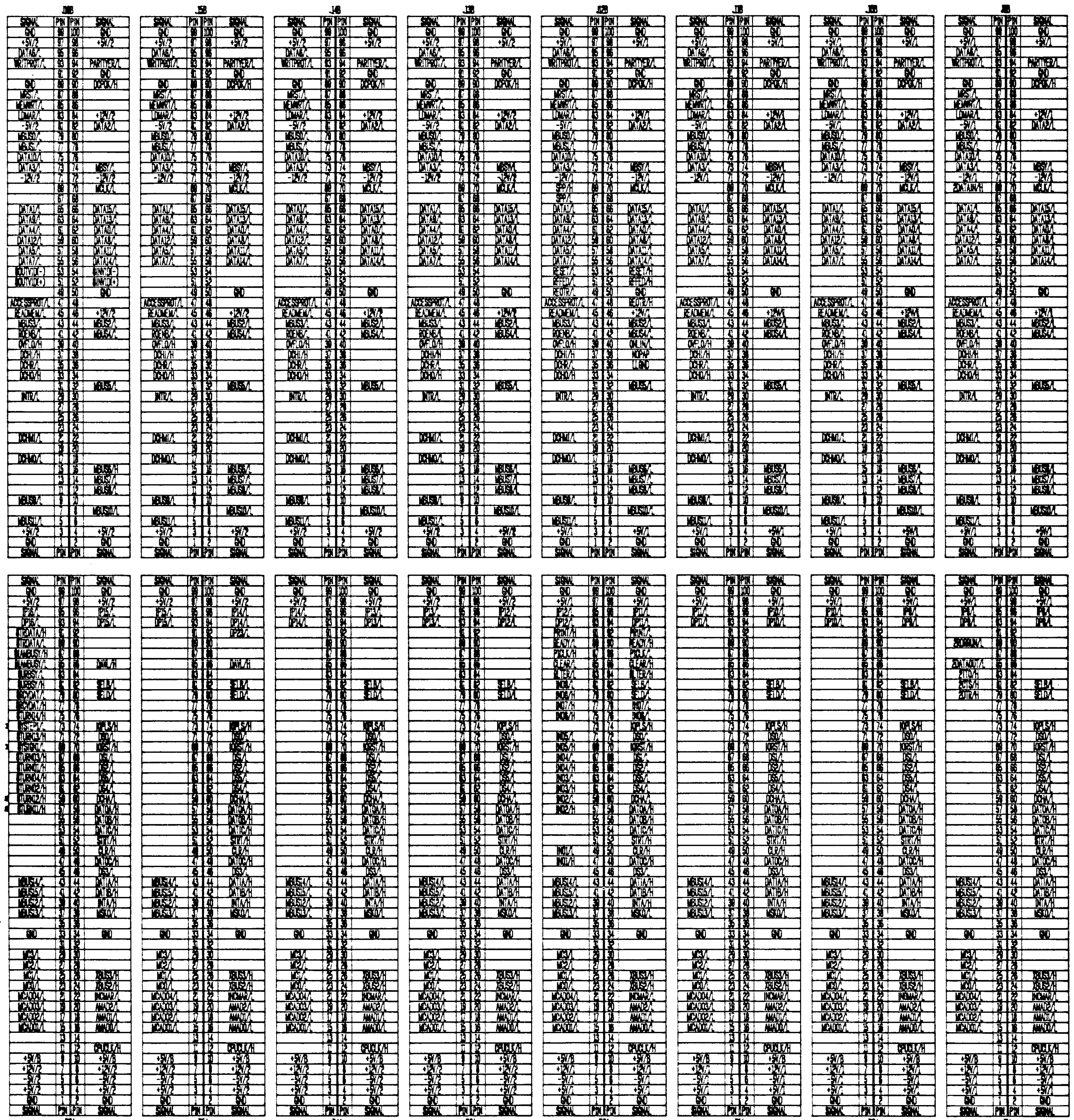
J7B			
SIGNAL	PIN	PIN	SIGNAL
GND	99	100	GND
+5V/1	97	98	+5V/1
DATA6/L	95	96	
WRITPROT/L	93	94	PARITYER/L
FC1/L	91	92	GND
GND	89	90	DCPOK/H
MRST/L	87	88	FC2/L
MEMWRT/L	85	86	FC3/L
LDMAR/L	83	84	+12V/1
-5V/1	81	82	DATA2/L
MBUSD0/L	79	80	FSP0/L
MBUSI1/L	77	78	FBS1/L
DATA10/L	75	76	FBP0/L
DATA3/L	73	74	MBST/L
-12V/1	71	72	-12V/1
	69	70	MCLK/L
	67	68	
DATA1/L	65	66	DATA15/L
DATA9/L	63	64	DATA13/L
DATA4/L	61	62	DATA0/L
DATA12/L	59	60	DATA8/L
DATA5/L	57	58	DATA11/L
DATA7/L	55	56	DATA14/L
	53	54	
	51	52	
	49	50	GND
ACCESSPROT/L	47	48	
READMEM/L	45	46	+12V/1
MBUS3/L	43	44	MBUS2/L
RQENB/L	41	42	MBUS4/L
OVFLO/H	39	40	XMAP/L
DCHL/H	37	38	XRST/H
DCHR/L	35	36	RADL/H
DCHD/H	33	34	RADH/H
	31	32	MBUSS/L
INTR/L	29	30	DCFER/L
ITRAP1	27	28	MCLK/L
RADL/H	25	26	RADL/H
CALBST/L	23	24	RADH/H
DCHM/L	21	22	RAD3/H
MAPTSS/H	19	20	CLRINTER/L
DCHM0/L	17	18	RAD2/H
	15	16	MBUS8/L
	13	14	MBUS7/L
	11	12	MBUS6/L
MBUS9/L	9	10	CPURST/L
LOADR/L	7	8	MBUS10/L
MBUS11/L	5	6	RAD7/H
+5V/1	3	4	+5V/1
GND	1	2	GND
SIGNAL	PIN	PIN	SIGNAL

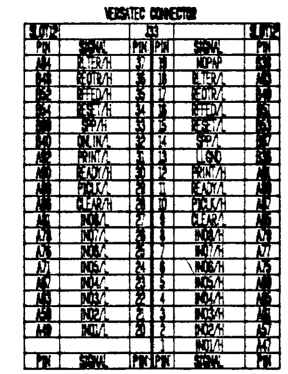
J8A			
SIGNAL	PIN	PIN	SIGNAL
GND	99	100	GND
+5V/1	97	98	+5V/1
IP7/L	95	96	IP6/L
IP8/L	93	94	IP7/L
	91	92	
	89	90	
	87	88	
	85	86	
	83	84	
	81	82	SELB/L
	79	80	SELD/L
	77	78	
	75	76	
	73	74	IOPLS/H
	71	72	IS0/L
	69	70	IOBS1/H
	67	68	IS1/L
	65	66	IS2/L
	63	64	IS4/L
	61	62	IS4/L
	59	60	DCHA/L
	57	58	DATOA/H
	55	56	DATOB/H
	53	54	DATIC/H
	51	52	STRT/H
	49	50	CLR/H
	47	48	DATOC/H
	45	46	IS3/L
MBUS14/L	43	44	DATIA/H
MBUS15/L	41	42	DATIB/H
MBUS12/L	39	40	IRTA/H
MBUS13/L	37	38	MSK0/L
	35	36	
GND	33	34	GND
	31	32	
	29	30	
MCA/L	27	28	
MCB/L	25	26	
MCC/L	23	24	
MCD/L	21	22	XBUS3/H
MCA004/L	19	20	XBUS2/H
MCA003/L	17	18	IMCMAR/L
MCA002/L	15	16	AMA02/L
MCA001/L	13	14	AMA01/L
	11	12	AMA00/L
	9	10	CPUCLK/H
+5V/8	7	8	+5V/8
+12V/1	5	6	+12V/1
-5V/1	3	4	-5V/1
+5V/1	1	2	+5V/1
SIGNAL	PIN	PIN	SIGNAL

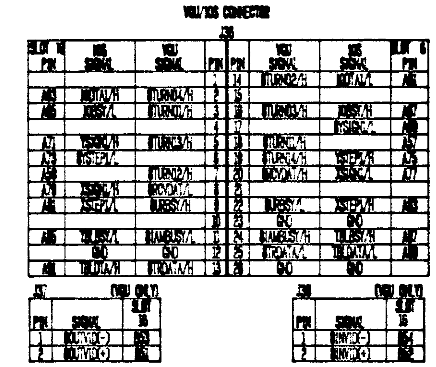
J7A			
SIGNAL	PIN	PIN	SIGNAL
GND	99	100	GND
+5V/1	97	98	+5V/1
DATA6/L	95	96	
WRITPROT/L	93	94	PARITYER/L
	91	92	GND
GND	89	90	DCPOK/H
MRST/L	87	88	
MEMWRT/L	85	86	
LDMAR/L	83	84	+12V/1
-5V/1	81	82	DATA2/L
MBUSD0/L	79	80	
MBUSI1/L	77	78	
DATA10/L	75	76	
DATA3/L	73	74	MBST/L
-12V/1	71	72	-12V/1
	69	70	MCLK/L
	67	68	
DATA1/L	65	66	DATA15/L
DATA9/L	63	64	DATA13/L
DATA4/L	61	62	DATA0/L
DATA12/L	59	60	DATA8/L
DATA5/L	57	58	DATA11/L
DATA7/L	55	56	DATA14/L
	53	54	
	51	52	
	49	50	GND
ACCESSPROT/L	47	48	
READMEM/L	45	46	+12V/1
MBUS3/L	43	44	MBUS2/L
RQENB/L	41	42	MBUS4/L
OVFLO/H	39	40	7TRACE/L
DCHL/H	37	38	RDL
DCHR/L	35	36	RDST/L
DCHD/H	33	34	RADL/H
	31	32	MBUSS/L
INTR/L	29	30	
	27	28	
	25	26	
	23	24	
DCHM/L	21	22	
	19	20	
DCHM0/L	17	18	
	15	16	MBUS8/L
	13	14	MBUS7/L
	11	12	MBUS6/L
MBUS9/L	9	10	
	7	8	MBUS10/L
MBUS11/L	5	6	
+5V/1	3	4	+5V/1
GND	1	2	GND
SIGNAL	PIN	PIN	SIGNAL

J8A			
SIGNAL	PIN	PIN	SIGNAL
GND	99	100	GND
+5V/1	97	98	+5V/1
IP6/L	95	96	IP5/L
IP7/L	93	94	IP6/L
	91	92	
	89	90	
	87	88	
	85	86	
	83	84	
	81	82	SELB/L
	79	80	SELD/L
	77	78	
	75	76	
	73	74	IOPLS/H
	71	72	IS0/L
	69	70	IOBS1/H
	67	68	IS1/L
	65	66	IS2/L
	63	64	IS4/L
	61	62	IS4/L
	59	60	DCHA/L
	57	58	DATOA/H
	55	56	DATOB/H
	53	54	DATIC/H
	51	52	STRT/H
	49	50	CLR/H
	47	48	DATOC/H
	45	46	IS3/L
MBUS14/L	43	44	DATIA/H
MBUS15/L	41	42	DATIB/H
MBUS12/L	39	40	IRTA/H
MBUS13/L	37	38	MSK0/L
	35	36	
GND	33	34	GND
	31	32	
	29	30	
MCA/L	27	28	
MCB/L	25	26	
MCC/L	23	24	
MCD/L	21	22	XBUS3/H
MCA004/L	19	20	XBUS2/H
MCA003/L	17	18	IMCMAR/L
MCA002/L	15	16	AMA02/L
MCA001/L	13	14	AMA01/L
	11	12	AMA00/L
	9	10	CPUCLK/H
+5V/8	7	8	+5V/8
+12V/1	5	6	+12V/1
-5V/1	3	4	-5V/1
+5V/1	1	2	+5V/1
SIGNAL	PIN	PIN	SIGNAL

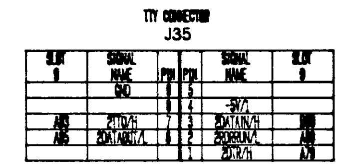
J8B			
SIGNAL	PIN	PIN	SIGNAL
GND	99	100	GND
+5V/1	97	98	+5V/1
DATA6/L	95	96	
WRITPROT/L	93	94	PARITYER/L
	91	92	GND
GND	89	90	DCPOK/H
MRST/L	87	88	
MEMWRT/L	85	86	
LDMAR/L	83	84	+12V/1
-5V/1	81	82	DATA2/L
MBUSD0/L	79	80	
MBUSI1/L	77	78	
DATA10/L	75	76	
DATA3/L	73	74	MBST/L
-12V/1	71	72	-12V/1
	69	70	MCLK/L
	67	68	
DATA1/L	65	66	DATA15/L
DATA9/L	63	64	DATA13/L
DATA4/L	61	62	DATA0/L
DATA12/L	59	60	DATA8/L
DATA5/L	57	58	DATA11/L
DATA7/L	55	56	DATA14/L
	53	54	
	51	52	
	49	50	GND
ACCESSPROT/L	47	48	
READMEM/L	45	46	+12V/1
MBUS3/L	43	44	MBUS2/L
RQENB/L	41	42	MBUS4/L
OVFLO/H	39	40	
DCHL/H	37	38	
DCHR/L	35	36	
DCHD/H	33	34	
	31	32	MBUSS/L
INTR/L	29	30	
	27	28	
	25	26	
	23	24	
DCHM/L	21	22	
	19	20	
DCHM0/L	17	18	
	15	16	MBUS8/L
	13	14	MBUS7/L
	11	12	MBUS6/L
MBUS9/L	9	10	
	7	8	MBUS10/L
MBUS11/L	5	6	
+5V/1	3	4	+5V/1
GND	1	2	GND







NOTES:
1. IOS SIGNAL ONLY: J16 PIN 69 AND 73.
2. VGU SIGNAL ONLY: J16 PIN 57 AND 59.



J82

+5V/2	2	1	+5V/2
GND	4	3	GND
+12V/2	6	5	+12V/2
GND	8	7	GND
-12V/2	10	9	DCPOK/H

HIGH POWER CONNECTOR
J27

GND (+5VOLTS RETURN)	2	1	(+5VOLTS OUTPUT) 5V/2

LOW POWER CONNECTOR
J28

	2	1	(+5V OUT SEN) +5V/2
	4	3	(+5V RET SEN) GND
+12V/2 (+12V OUTPUT)	6	5	(+12V OUT SEN) +12V/2
GND (+12V RETURN)	8	7	(+12V RET SEN) GND
GND (-12V RETURN)	10	9	(-12V RET SEN) GND
-12V/2 (-12V OUTPUT)	12	11	(-12V OUT SEN) -12V/2
GND (-5V RETURN)	14	13	ACPF/L
-5V/2 (-5V OUTPUT)	16	15	DCPOK/H

NOTE:
J27 AND J28 SUPPLY POWER TO SLOTS 13 THRU 24

DS21E1102
D

MATERIAL —//—
FINISH —//—

A21E1100 | 1
PART NUMBER | NEXT ASSEMBLY | QTY

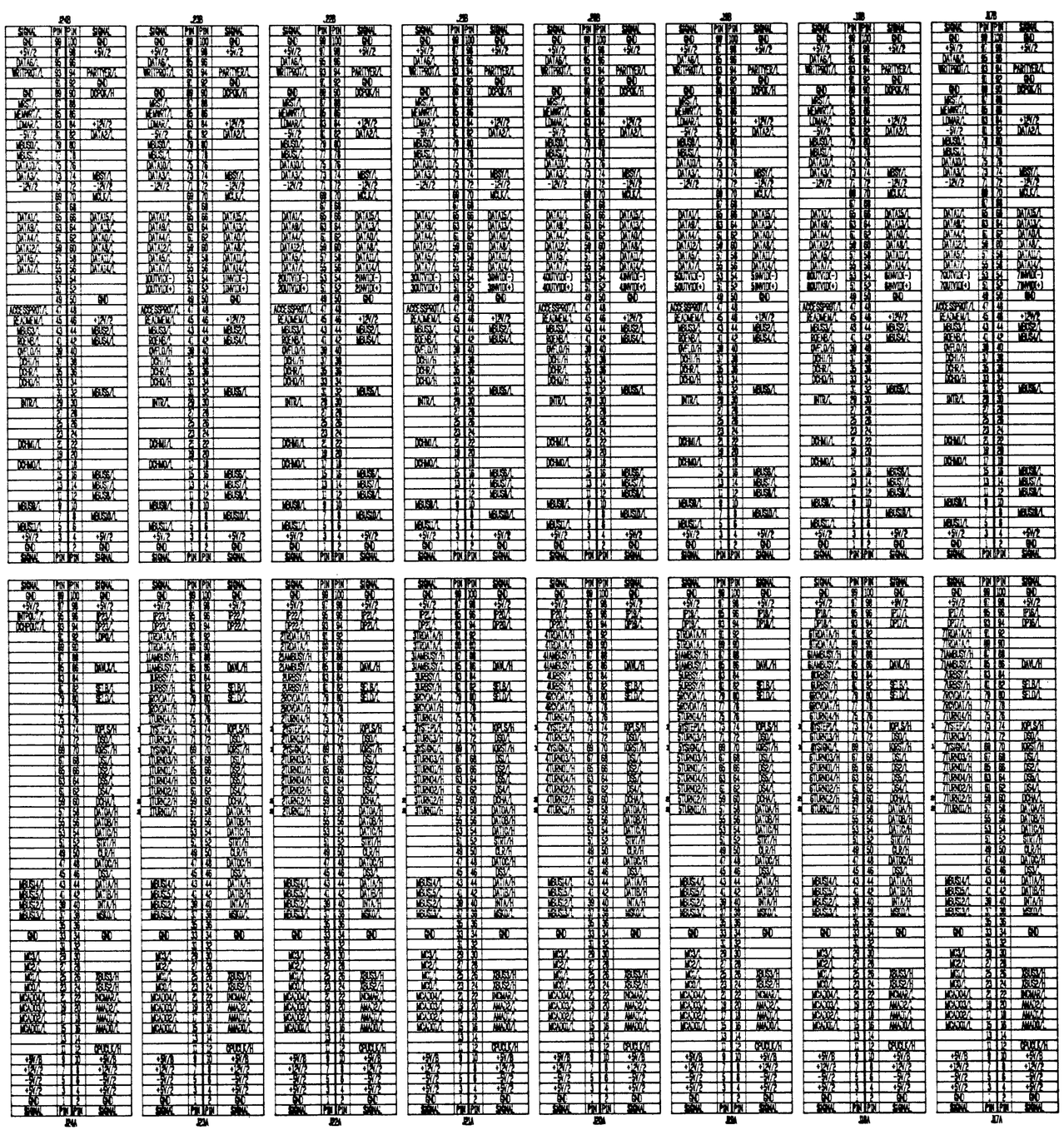
COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

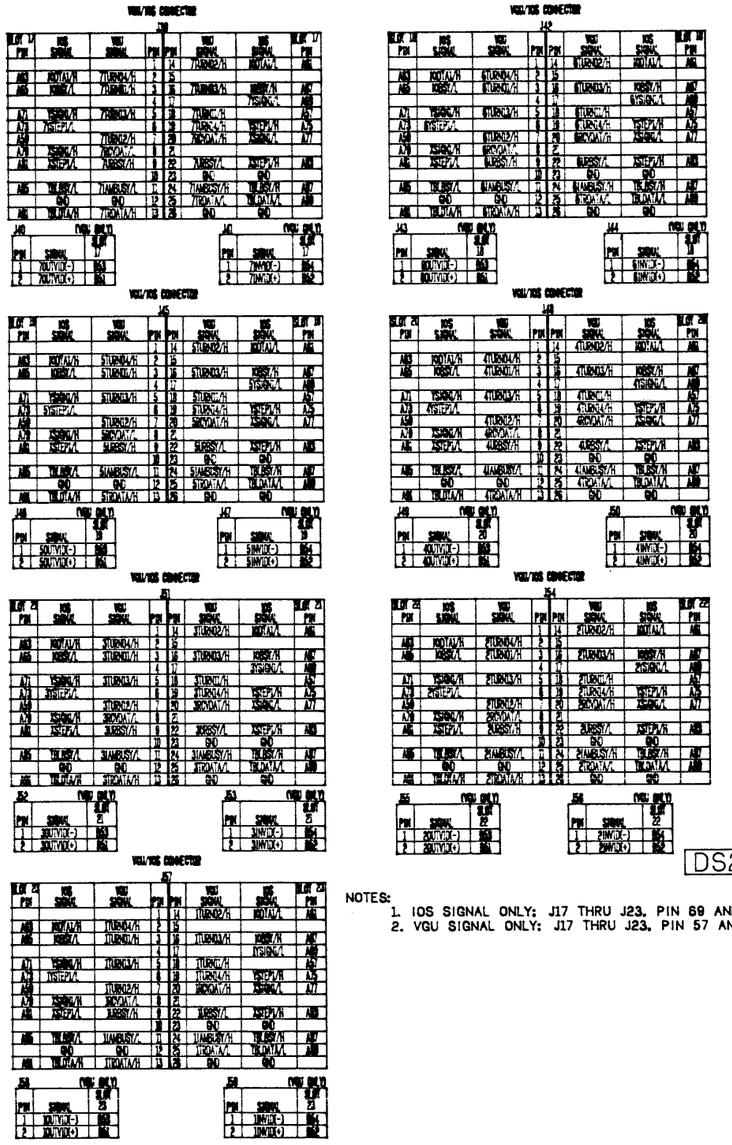
TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ±1/64 ANGULAR ±.100

DRN P. MAGEE 6-12
CHK
ENGR H. TIDD 6-12
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

D | SEE SHT 1
SYM | REVISION DESCRIPTION | CHK | APPD | DATE

TITLE 24S SCHEMATIC CGP100/200 BACKPLANE
SCALE —//— | DWG NO. DS21E1102
UNIT WT. —//— | SHT 2 OF 4 SHTS





NOTES:
1. IOS SIGNAL ONLY: J17 THRU J23, PIN 69 AND 73.
2. VGU SIGNAL ONLY: J17 THRU J23, PIN 57 AND 58.

DS21E1102
D

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

TOLERANCES
DECIMAL
XX ±=.01
XXX ±=.005
XXXX ±=.0030
FRACTIONAL ±=1/64
ANGULAR ±=.100

MATERIAL
FINISH
PART NUMBER A21E1100
NEXT ASSEMBLY
QTY 1

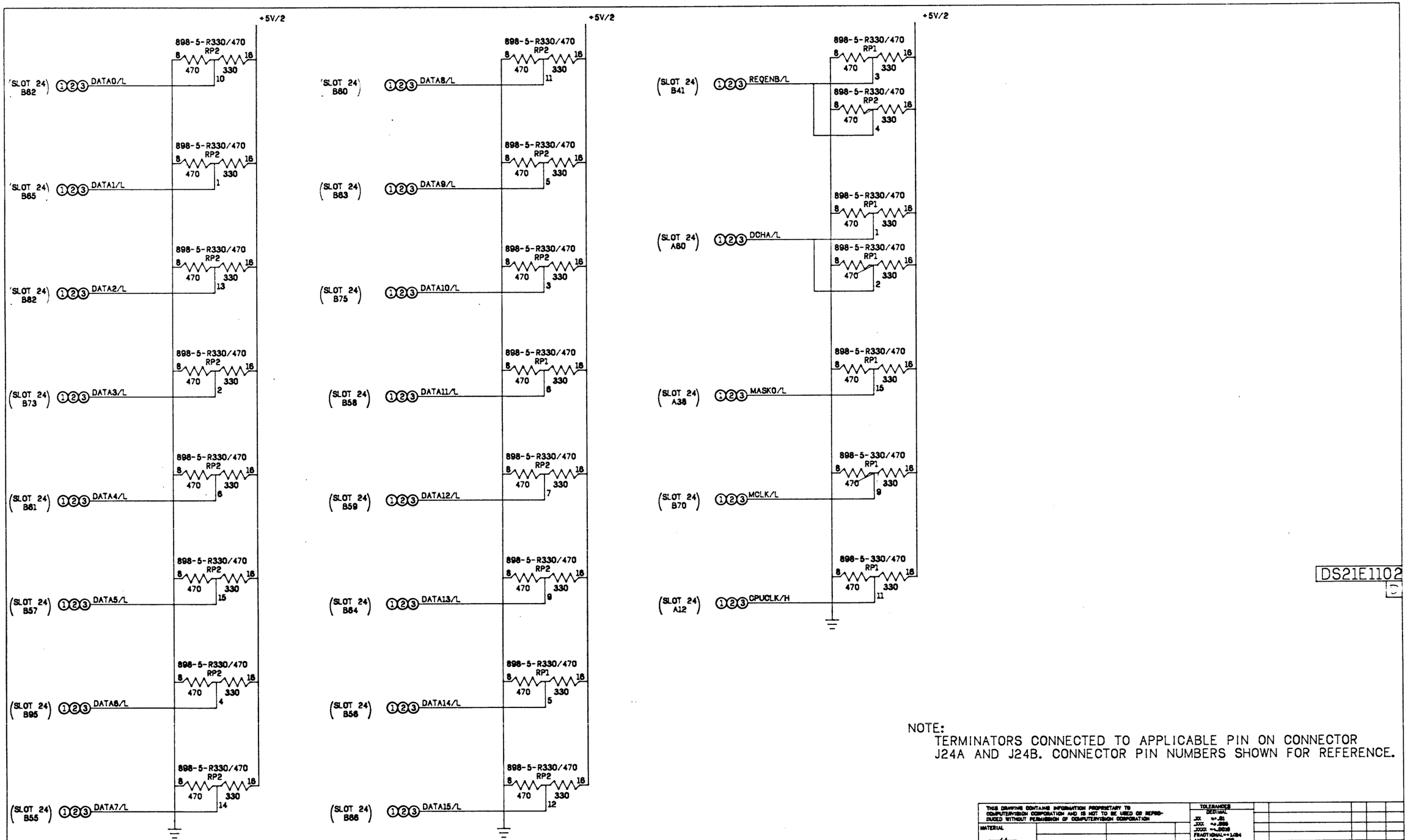
DRN P. MAREZ 9-12
CHK
ENGR M. TIDD 9-12
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
C	SEE SHT 1			

TITLE 24S SCHEMATIC
CGP100/200 BACKPLANE

SCALE — DWG NO. DS21E1102
UNIT WT. — SHT 3 OF 4 SHTS



DS21E1102

NOTE:
TERMINATORS CONNECTED TO APPLICABLE PIN ON CONNECTOR J24A AND J24B. CONNECTOR PIN NUMBERS SHOWN FOR REFERENCE.

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0025 FRACTIONAL ±1/64 ANGULAR ±.125

MATERIAL

FINISH

PART NUMBER A21E1100 NEXT ASSEMBLY 1 QTY

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
	SEE SHT 1			

DRN P. MAREK 9-12
CHK
ENGR N TODD 9-12
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

TITLE 24S SCHEMATIC
CGP100/200 BACKPLANE

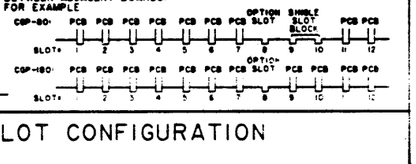
SCALE -/- DWG NO. DS21E1102

UNIT WT. -/- SHT 4 OF 4 SHTS

BOARD TYPE	EA CPU	MEMORY-MAP	FPU	MAGNETIC TAPE CONTROLLER	DISK CONTROLLER	PCU	A-B PORT MEMORY #0	OPTIONAL SLOT	*A-B PORT MEMORY #1	*GPU	VGU #2	VGU #1
SLOT	1	2	3	4	5	6	7	8	9	10	11	12
REV.												
DEVICE CODE												

CAUTION: 1. TO AVOID SERIOUS DAMAGE TO THE ELECTRONICS, REMOVE POWER BEFORE REMOVING ANY PC CARDS.

2. TO INSURE AN OPTIMUM COOLING ENVIROMENT IN THIS EQUIPMENT, USE COMPUTERVISION STANDARD SLOT BLOCKS. (CV P/N SP21M005 SINGLE, OR CV P/N SP21M005 DOUBLE) WHENEVER A SYSTEM HAS 2 OR MORE OPEN PCB SLOTS BETWEEN ADJACENT BOARDS FOR EXAMPLE



* OPTIONAL SLOTS IN CGP-80

SYSTEM S.N._____

CGP-80
CGP-180

12 SLOT CONFIGURATION

P/N CP21M054 REV A S/N 993-02090 MADE IN USA

6.90

8.45

CP21M054
A

NOTES:

1. VENDOR: TECHPRINT INC.
   15 SIXTH ROAD
   WOBURN, MA. 01801
2. COLOR: BLACK LETTERS ON WHITE BACKGROUND
3. ARTWORK MASTER WILL BE SUPPLIED TO VENDOR BY DRAFTING DEPT.
4. MATERIAL: .004 THICK FLEXIBLE VINYL ADHESIVE BACK.

MATERIAL: SEE NOTE 4

FINISH: SEE NOTE 2

PART NUMBER	NEXT ASSEMBLY	QTY
	MODULE LIST	1

TOLERANCE UNLESS OTHERWISE SPECIFIED: DECIMAL .XX ±0.1 .XXX ±0.05 .XXXX ±0.005 FRACTIONAL ± 1/64 ANGULAR ± 0° 30'

DRN [illegible] 7/81
CHK [illegible] 7/81
ENGR [illegible] 7/81
PROJ [illegible] 7/81
MFG
QUALITY ENG.

REMOVE ALL BURRS AND SHARP EDGES

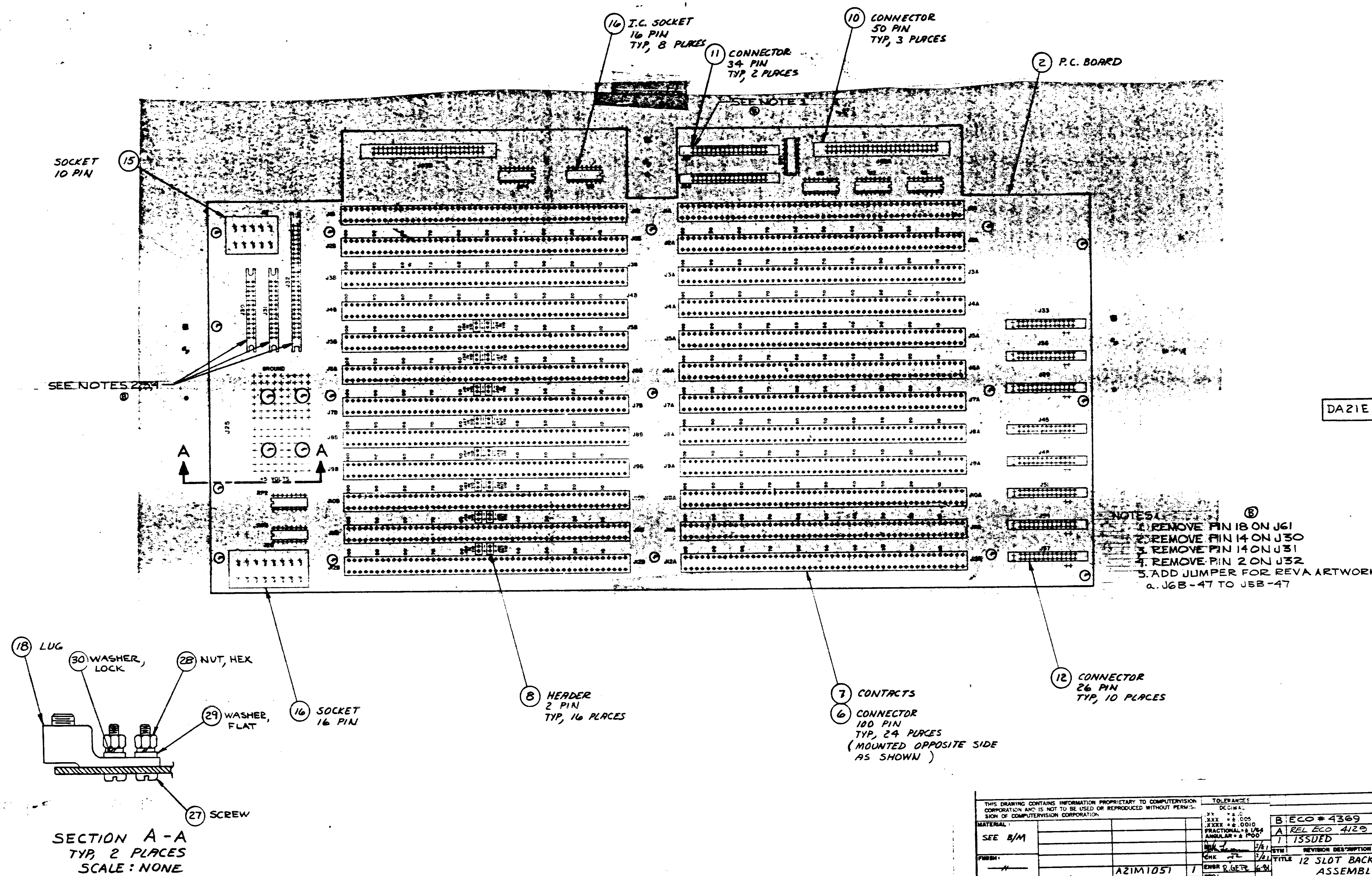
SYM	REVISION DESCRIPTION	CHK	APPD	DATE
A	REL ECO # 3935	[illegible]	[illegible]	

TITLE: CGP
12 SLOT CONFIGURATION

SCALE: 1:1 SIZE: B DWG NO. CP21M054

WT. — SHEET 1 OF 1 SHEETS

COMPUTERVISION CORP.
201 BURLINGTON RD ROUTE 62
BEDFORD, MASS 01730



MATERIAL: SEE B/M

FINISH: —

PART NUMBER	NEXT ASSEMBLY	QTY
	A21M1051	1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
B	ECO # 4369			
A	REL ECO 4129			
1	ISSUED			

TITLE: 12 SLOT BACKPLANE ASSEMBLY

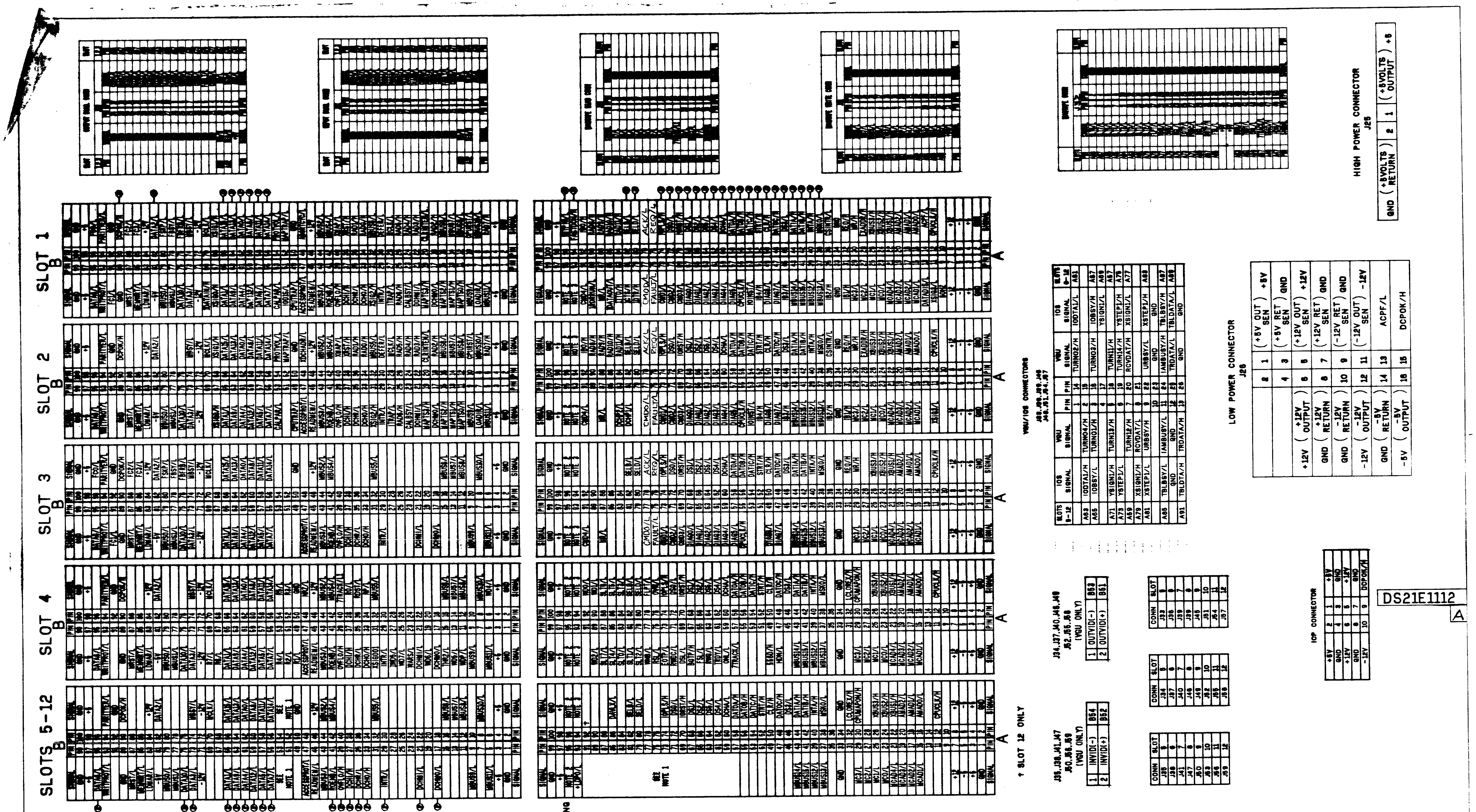
SCALE 1:1

DWG NO. DA21E1110

SHEET 1 OF 1 SHEETS

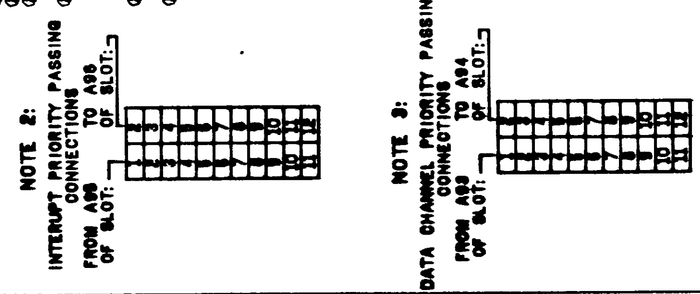
COMPUTERVISION CORP.
201 BURLINGTON RD ROUTE 62
BEDFORD, MASS 01730

REMOVE ALL BURRS AND SHARP EDGES



NOTE 1:

SLOTS 5,6,7,8,9,10,11 AND 12 HAVE PROVISIONS FOR EITHER VGU OR IOS INTERFACES. BOTH USE THE CORRESPONDING 26 PIN CONNECTORS J27,J30,J33,J36, AND J39. CONNECTORS J28, J29,J31,J32,J34,J35,J37,J38,J40, AND J41 ARE USED WITH VGU INTERFACES ONLY.



MATERIAL		
FINISH		
PART NUMBER	NEXT ASSEMBLY	QTY
	DA21E1110	1

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ±1/64 ANGULAR ±.100

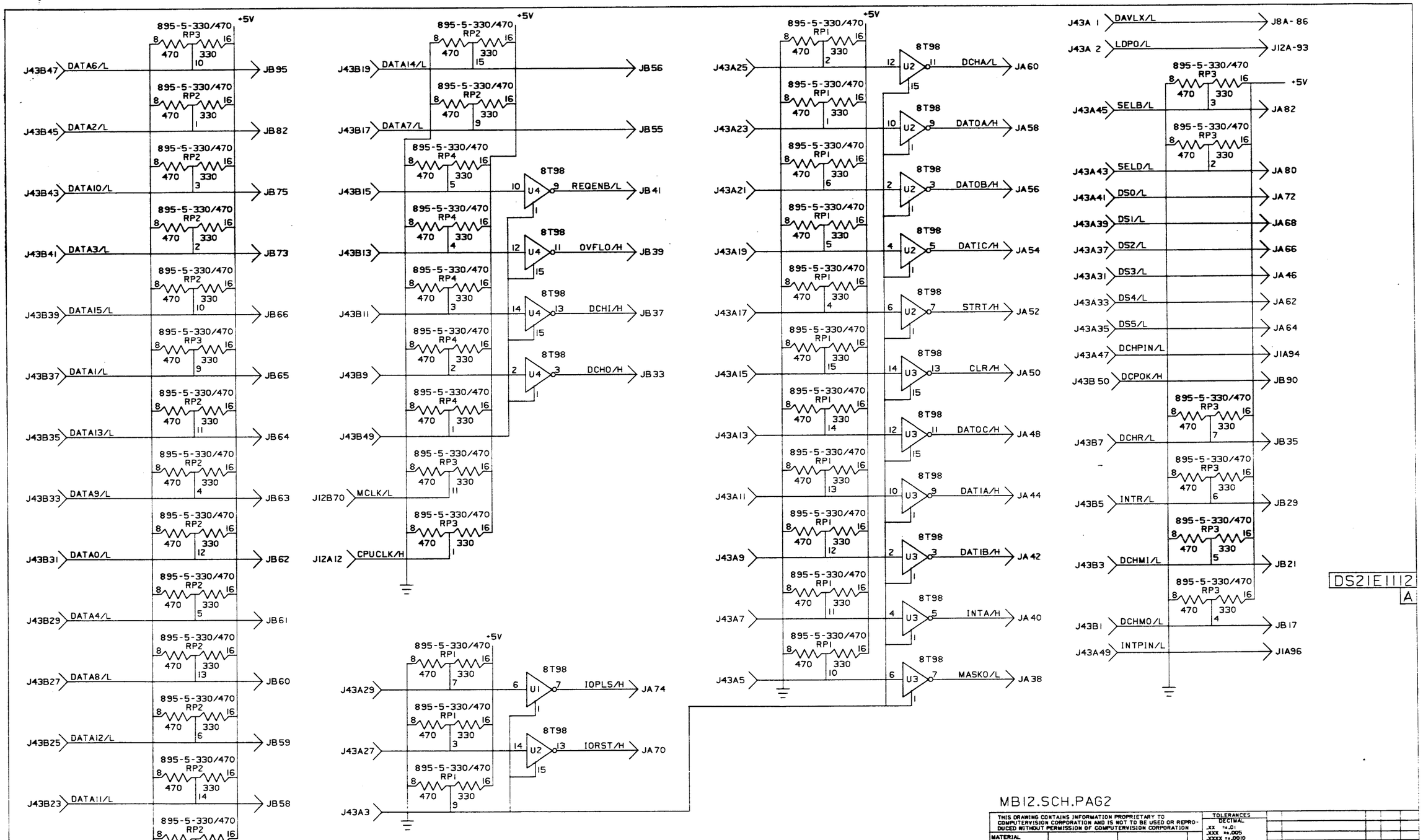
SYM	REVISION DESCRIPTION	CHK	APPD	DATE
A	REL ECO 4129	RB	RG	6-81
1	ISSUED			

TITLE 12 SLOT BACKPLANE SCHEMATIC DIAGRAM

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

DWG NO. DS21E1112

SHT 1 OF 2 SHTS



NOTES:

1. ALL RESISTORS AND ICS USED WITH EXPANSION CONFIGURATION ONLY.
2. CONNECTOR J43B ALL EVEN PINS (2 THRU 48) ARE GROUND PINS.
3. CONNECTOR J43A ALL EVEN PINS (4 THRU 50) ARE GROUND PINS.

DS21E1112
A

MB12.SCH.PAG2

TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ± 1°00

MATERIAL
FINISH

PART NUMBER	NEXT ASSEMBLY	QTY
	DA21E1110	1

DRN STURDEVANT 8-10
CHK
ENGR TODD 8-10
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

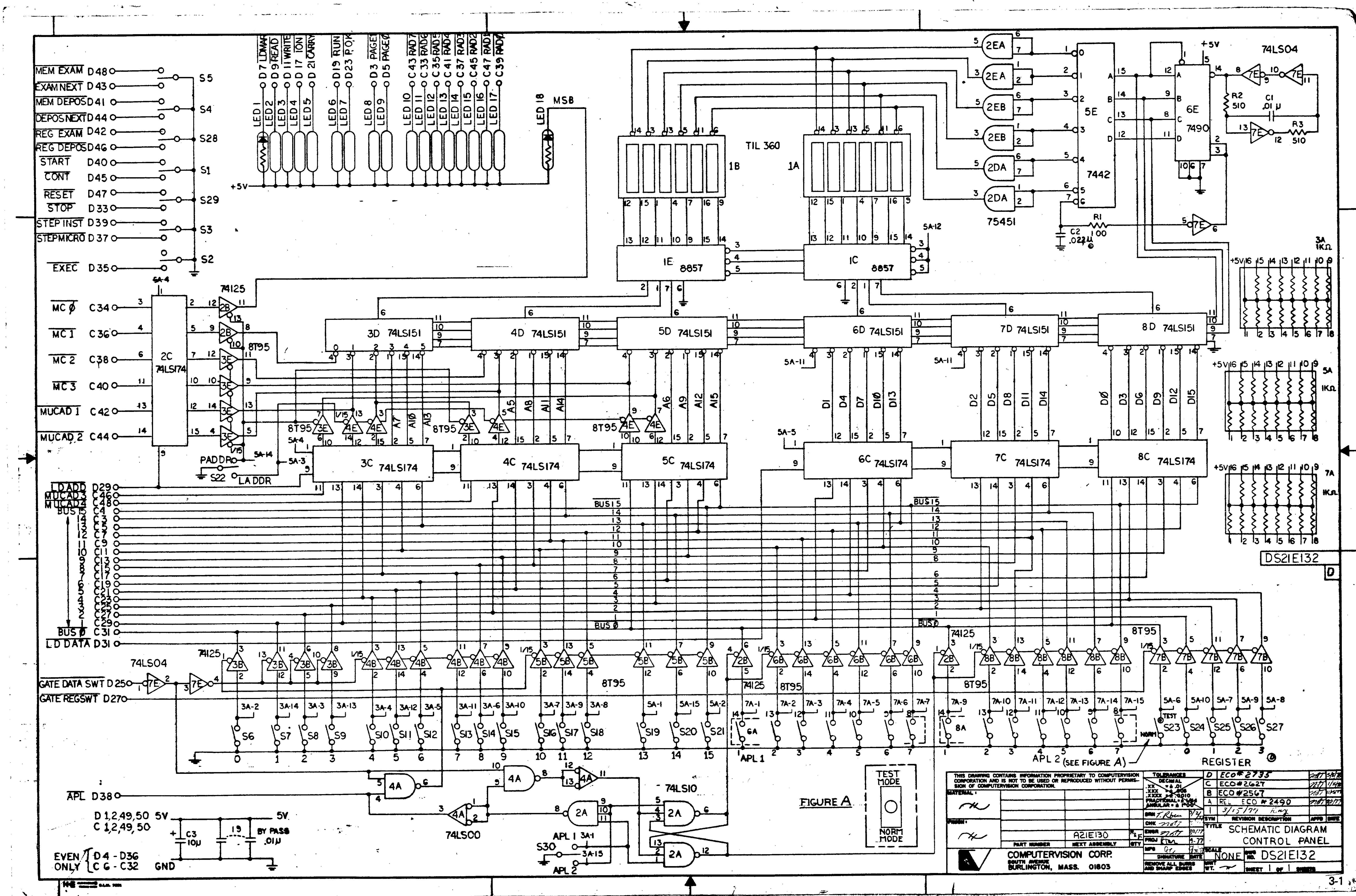
SYM	REVISION DESCRIPTION	CHK	APPD	DATE
A	SEE SHT 1			
1	SEE SHT 1			

TITLE 12 SLOT BACKPLANE SCHEMATIC DIAGRAM

SCALE
DWG NO. DS21E1112
UNIT
WT.
SHT 2 OF 2 SHTS

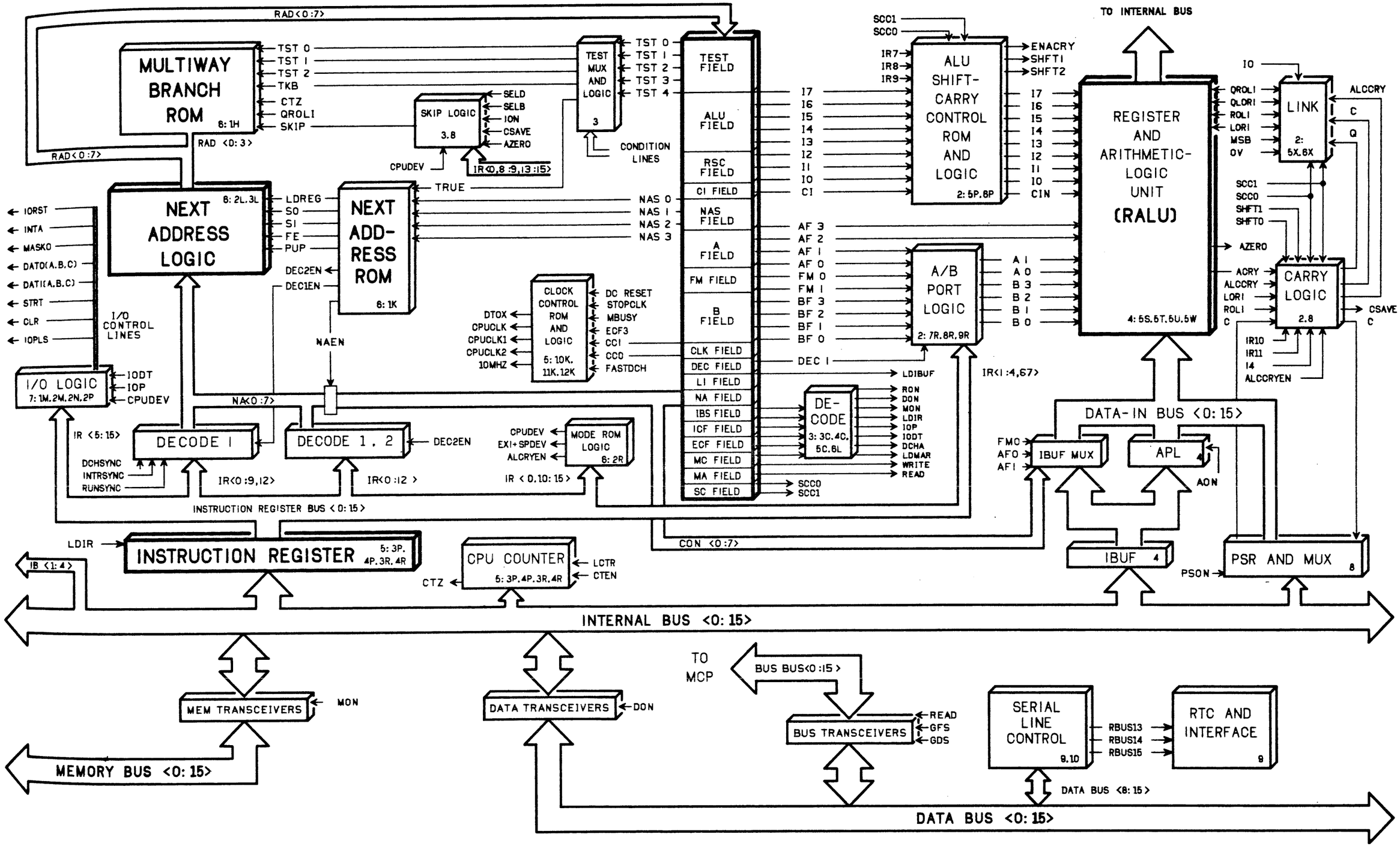
COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

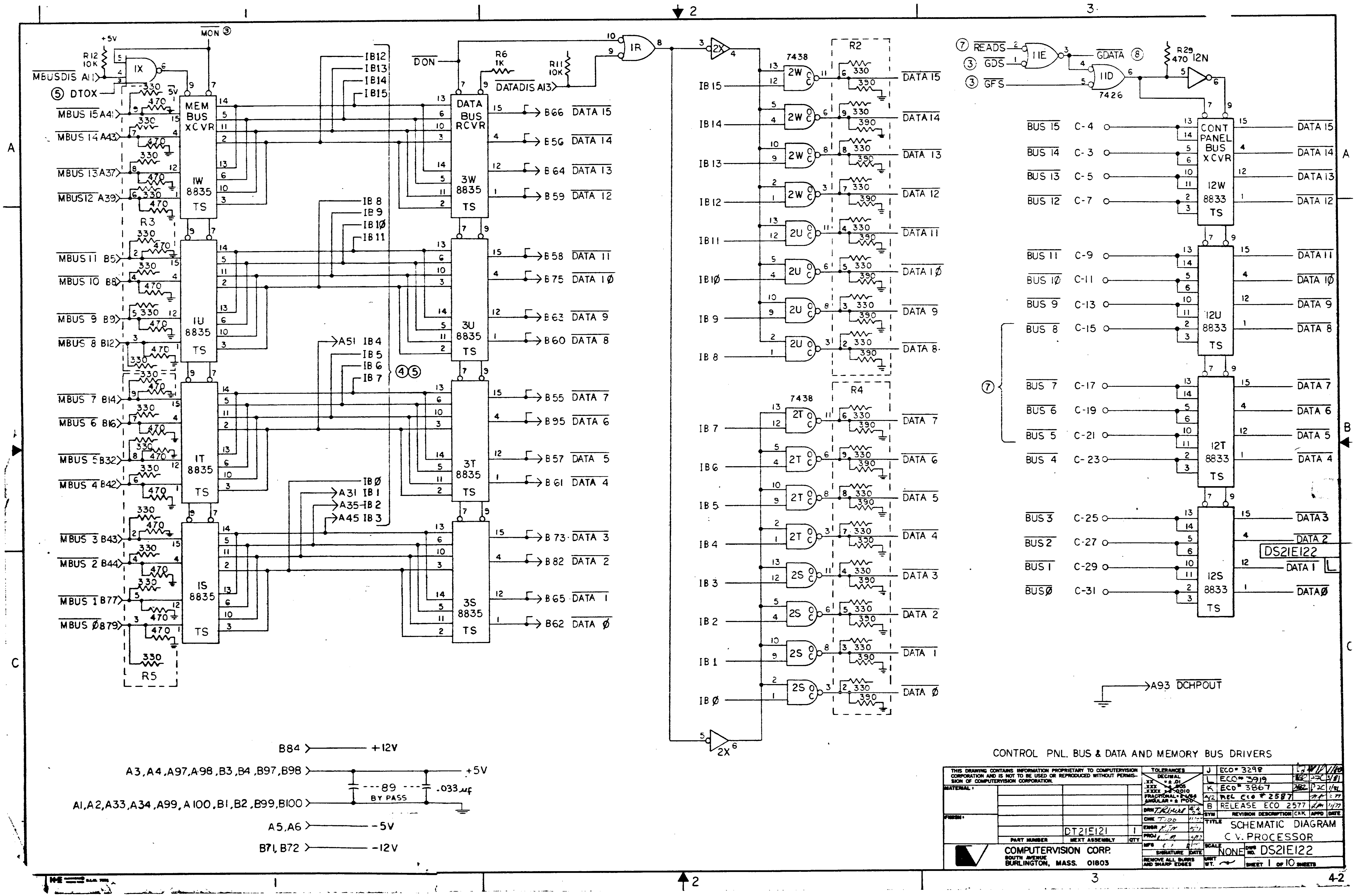
Section Three
Control Panel


SCHEMATIC DIAGRAM
CONTROL PANEL
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
DS21E132
A21E130
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.
D ECO #2735
C ECO #2627
B ECO #2567
A REL. ECO #2490
FIGURE A
TEST MODE
NORM MODE
TIL 360
75451
7442
7490
74LS04
74125
8T95
74LS151
74LS174
8857
74LS10
74LS00
MEM EXAM D48
EXAM NEXT D43
MEM DEPOS D41
DEPOS NEXT D44
REG EXAM D42
REG DEPOS D46
START D40
CONT D45
RESET D47
STOP D33
STEP INST D39
STEP MICRO D37
EXEC D35
GATE DATA SWT D25
GATE REG SWT D27
APL D38
LD ADD D29
LD DATA D31
REGISTER
APL 1
APL 2 (SEE FIGURE A)
EVEN ONLY D4 - D36 C6 - C32 GND
3-1

Section 4
Modules

Computervision Processor, Schematic Diagram


RAD<0:7>
MULTIWAY BRANCH ROM
6: 1H
TST 0
TST 1
TST 2
TKB
CTZ
QROLI
SKIP
RAD <0: 3>
SKIP LOGIC
3.8
SELD
SELB
ION
CSAVE
AZERO
CPUDEV
IR<0,8:9,13:15>
TEST MUX AND LOGIC
3
CONDITION LINES
TEST FIELD
ALU FIELD
RSC FIELD
CI FIELD
NAS FIELD
A FIELD
FM FIELD
B FIELD
CLK FIELD
DEC FIELD
LI FIELD
NA FIELD
IBS FIELD
ICF FIELD
ECF FIELD
MC FIELD
MA FIELD
SC FIELD
I7
I6
I5
I4
I3
I2
I1
I0
CI
NEXT ADDRESS LOGIC
6: 2L.3L
IORST
INTA
MASKO
DATO(A.B.C)
DATI(A.B.C)
STRT
CLR
IOPLS
I/O CONTROL LINES
LDREG
SO
SI
FE
PUP
DEC2EN
DEC1EN
NAEN
NEXT ADD-RESS ROM
6: 1K
TRUE
NAS 0
NAS 1
NAS 2
NAS 3
CLOCK CONTROL ROM AND LOGIC
5: 10K. 11K. 12K
DTOX
CPUCLK
CPUCLK1
CPUCLK2
10MHZ
DC RESET
STOPCLK
MBUSY
ECF3
CCI
CCO
FASTDCH
I/O LOGIC
7: 1M.2M.2N.2P
IODT
IOP
CPUDEV
NA<0:7>
IR <5:15>
DECODE 1
DECODE 1, 2
DEC2EN
DCHSYNC
INTRSYNC
RUNSYNC
IR<0:9,12>
IR<0:12>
CPUDEV
EXI+SPDEV
ALCRYEN
MODE ROM LOGIC
6: 2R
IR <0.10:15>
INSTRUCTION REGISTER BUS <0:15>
LDIR
INSTRUCTION REGISTER
5: 3P. 4P.3R.4R
IB <1:4>
CPU COUNTER
5: 3P.4P.3R.4R
LCTR
CTEN
CTZ
CON <0:7>
SCC1
SCC0
IR7
IR8
IR9
ALU SHIFT-CARRY CONTROL ROM AND LOGIC
2: 5P.6P
ENACRY
SHFT1
SHFT2
CIN
AF 3
AF 2
AF 1
AF 0
FM 0
FM 1
BF 3
BF 2
BF 1
BF 0
DEC 1
A/B PORT LOGIC
2: 7R.8R.9R
A 1
A 0
B 3
B 2
B 1
B 0
LDIBUF
RON
DON
MON
LDIR
IOP
IODT
DCHA
LDMAR
WRITE
READ
DE-CODE
3: 3C.4C. 5C.6L
SCC0
SCC1
IR<1:4,67>
TO INTERNAL BUS
REGISTER AND ARITHMETIC-LOGIC UNIT (RALU)
4: 5S.5T.5U.5W
IO
QROLI
QLORI
ROLI
LORI
MSB
OV
LINK
2: 5X.6X
ALCCRY
C
Q
SCC1
SCC0
SHFT1
SHFT0
AZERO
ACRY
ALCCRY
LORI
ROLI
C
CARRY LOGIC
2.8
CSAVE
C
IR10
IR11
I4
ALCCRYEN
DATA-IN BUS <0:15>
FMO
AFO
AF1
IBUF MUX
APL
4
AON
IBUF 4
PSR AND MUX
8
PSON
INTERNAL BUS <0:15>
MEM TRANSCEIVERS
MON
MEMORY BUS <0:15>
DATA TRANSCEIVERS
DON
TO MCP
BUS BUS<0:15>
BUS TRANSCEIVERS
READ
GFS
GDS
SERIAL LINE CONTROL
9.10
RBUS13
RBUS14
RBUS15
RTC AND INTERFACE
9
DATA BUS <8:15>
DATA BUS <0:15>


MEM BUS XCVR
IW 8835 TS
IU 8835 TS
IT 8835 TS
IS 8835 TS
DATA BUS RCVR
3W 8835 TS
3U 8835 TS
3T 8835 TS
3S 8835 TS
CONT PANEL BUS XCVR
12W 8833 TS
12U 8833 TS
12T 8833 TS
12S 8833 TS
MBUSDIS A11
DTOX
MON
DON
DATADIS A13
R6 1K
R11 10K
R12 10K
R29 470
7438
7426
READS
GDS
GFS
GDATA
A93 DCHPOUT
B84 +12V
A3, A4, A97, A98, B3, B4, B97, B98 +5V
A1, A2, A33, A34, A99, A100, B1, B2, B99, B100
89 BY PASS
.033 uf
A5, A6 -5V
B71, B72 -12V
CONTROL PNL. BUS & DATA AND MEMORY BUS DRIVERS
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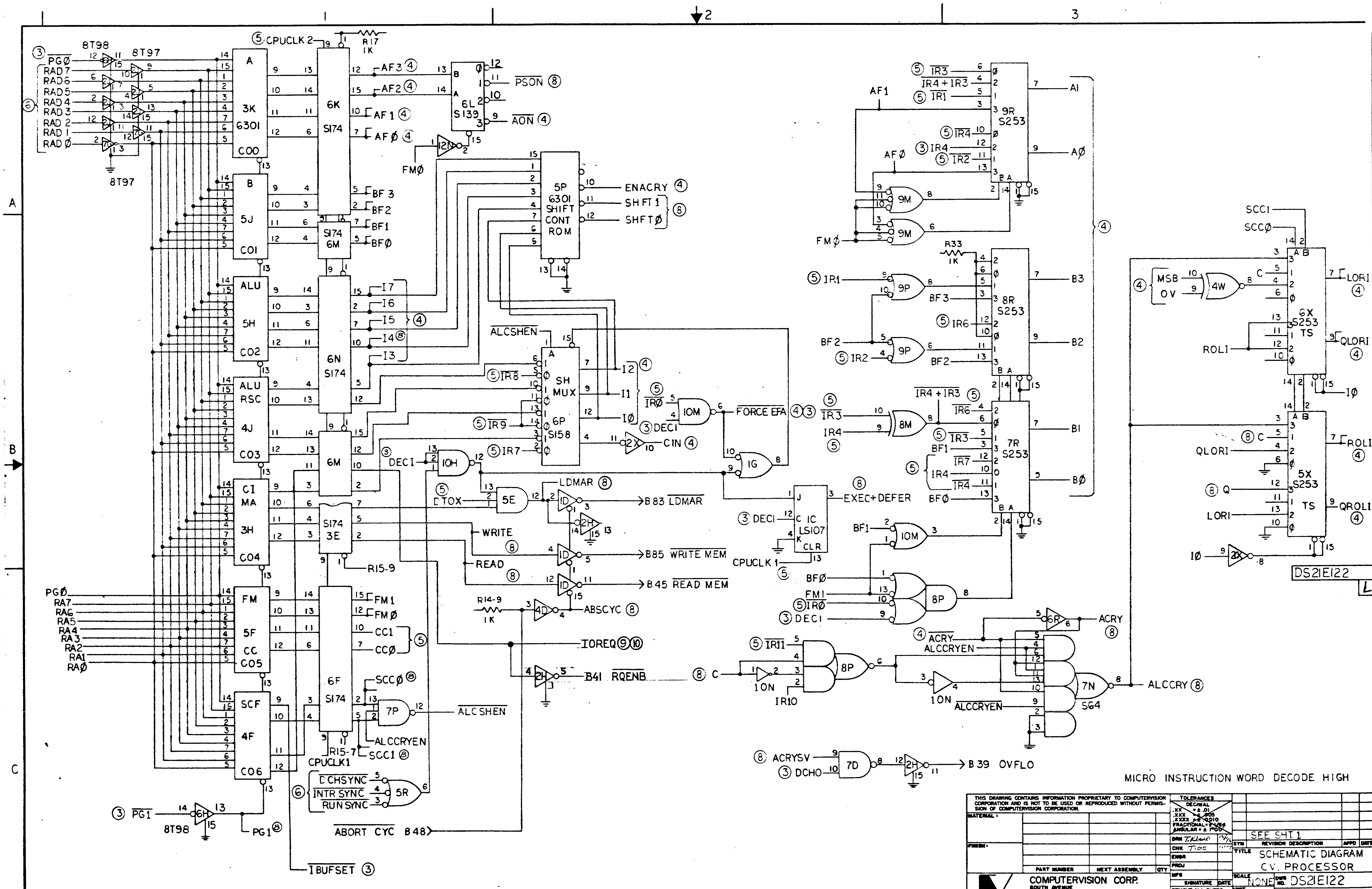
ECO 3298
ECO 3919
ECO 3867
REL ECO 2587
RELEASE ECO 2577
DT21E121
SCHEMATIC DIAGRAM C.V. PROCESSOR
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803
SCALE NONE
DS21E122
SHEET 1 OF 10 SHEETS
4-2



MICRO INSTRUCTION WORD DECODE HIGH

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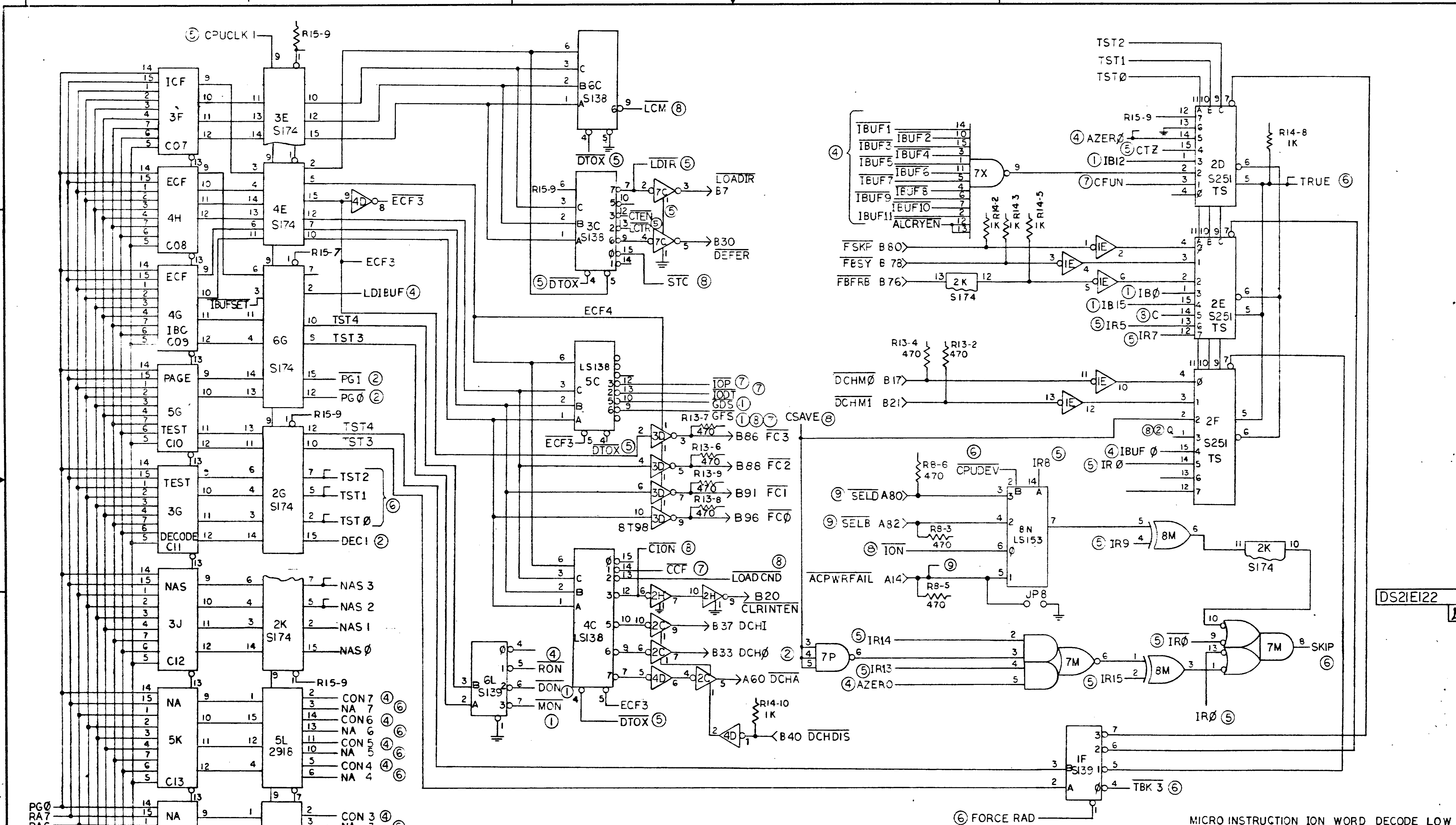
SEE SHT 1

TITLE SCHEMATIC DIAGRAM C.V. PROCESSOR

COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803

SCALE NONE DWG NO. DS21E122

SHEET 2 OF 10 SHEETS



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SEE SHT 1

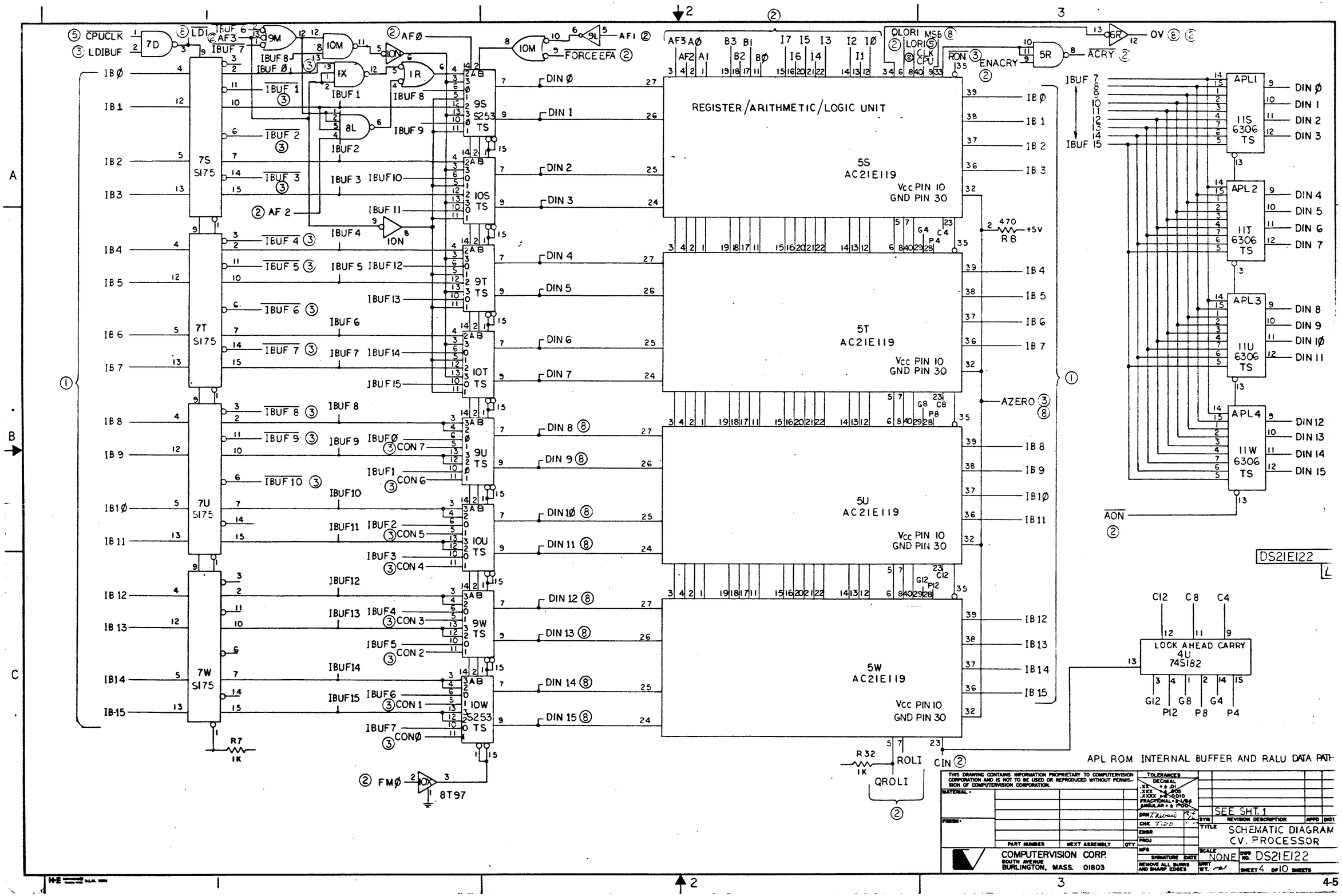
TITLE: SCHEMATIC DIAGRAM CV. PROCESSOR

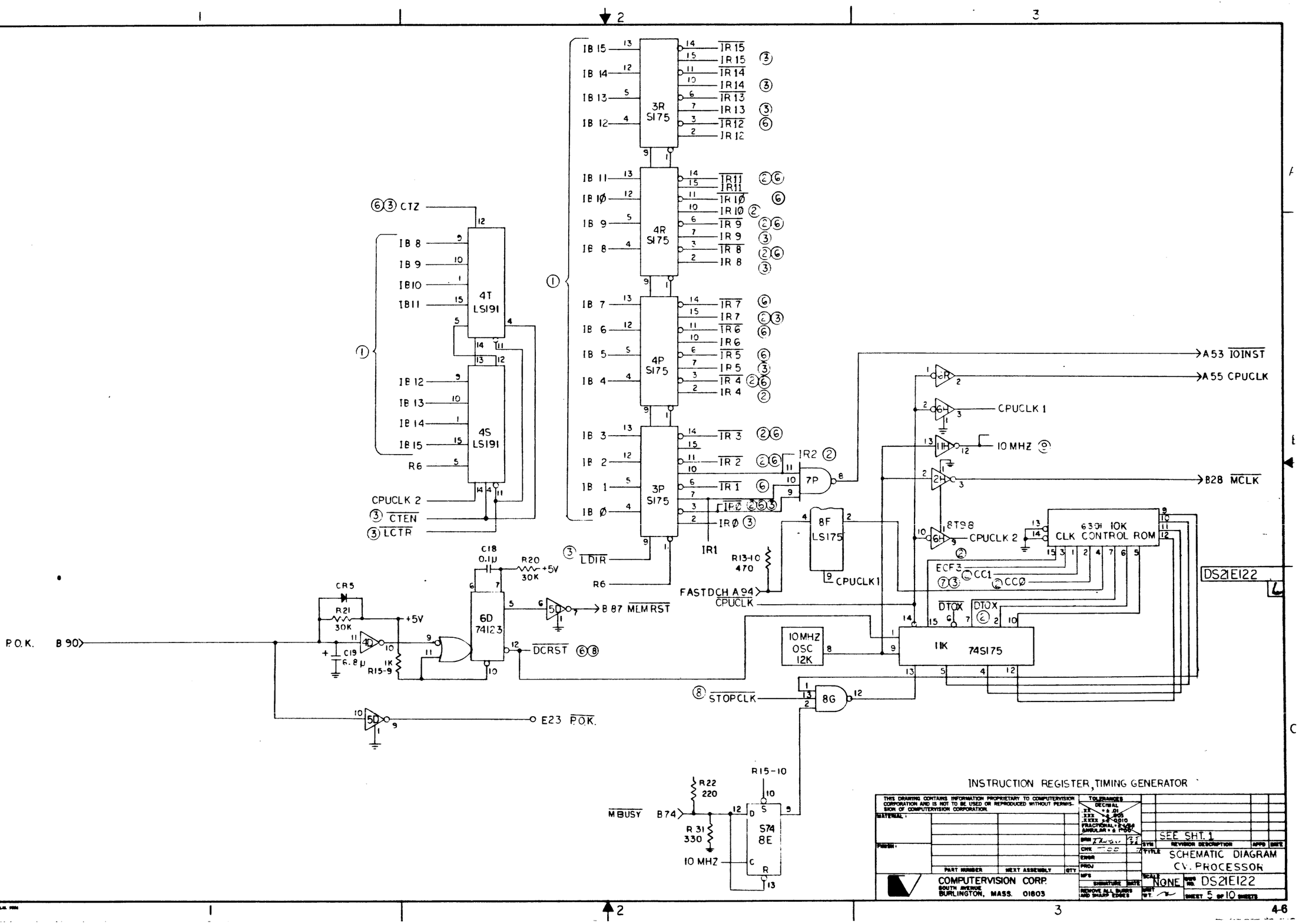
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803

SCALE NONE DWG NO. DS21E122

SHEET 3 OF 10 SHEETS

4-4


REGISTER/ARITHMETIC/LOGIC UNIT
5S AC21E119 Vcc PIN 10 GND PIN 30
5T AC21E119 Vcc PIN 10 GND PIN 30
5U AC21E119 Vcc PIN 10 GND PIN 30
5W AC21E119 Vcc PIN 10 GND PIN 30
7S SI75
7T SI75
7U SI75
7W SI75
9S S253 TS
10S TS
9T TS
10T TS
9U TS
10U TS
9W TS
10W S253 TS
11S 6306 TS
11T 6306 TS
11U 6306 TS
11W 6306 TS
LOOK AHEAD CARRY 4U 74S182
8T97
R8 470 +5V
R7 1K
R32 1K
DS21E122
APL ROM INTERNAL BUFFER AND RALU DATA PATH
SCHEMATIC DIAGRAM CV. PROCESSOR
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803
SEE SHT. 1
SCALE NONE
SHEET 4 OF 10 SHEETS


IB 15
IB 14
IB 13
IB 12
3R S175
IR 15
IR 15
IR 14
IR 14
IR 13
IR 13
IR 12
IR 12
IB 11
IB 10
IB 9
IB 8
4R S175
IR11
IR11
IR 10
IR 10
IR 9
IR 9
IR 8
IR 8
IB 7
IB 6
IB 5
IB 4
4P S175
IR 7
IR 7
IR 6
IR 6
IR 5
IR 5
IR 4
IR 4
IB 3
IB 2
IB 1
IB Ø
3P S175
IR 3
IR 2
IR 1
IRØ
IR2
7P
IR1
LDIR
R6
CTZ
IB 8
IB 9
IB10
IB11
4T LS191
IB 12
IB 13
IB 14
IB 15
R6
4S LS191
CPUCLK 2
CTEN
LCTR
C18 0.1μ
R20 30K
+5V
CR5
R21 30K
C19 6.8μ
1K R15-9
6D 74123
B 87 MEMRST
DCRST
P.O.K.
B 90
E23 P.O.K.
FASTDCH A 94
CPUCLK
R13-10 470
8F LS175
CPUCLK1
A53 IOINST
A55 CPUCLK
CPUCLK 1
10 MHZ
B28 MCLK
8T98
CPUCLK 2
630H 10K CLK CONTROL ROM
ECF3
CC1
CCØ
DS21E122
DTOX
DTOX
10MHZ OSC 12K
11K 74S175
STOPCLK
8G
MBUSY
B74
R22 220
R 31 330
10 MHZ
R15-10
S74 8E
INSTRUCTION REGISTER, TIMING GENERATOR
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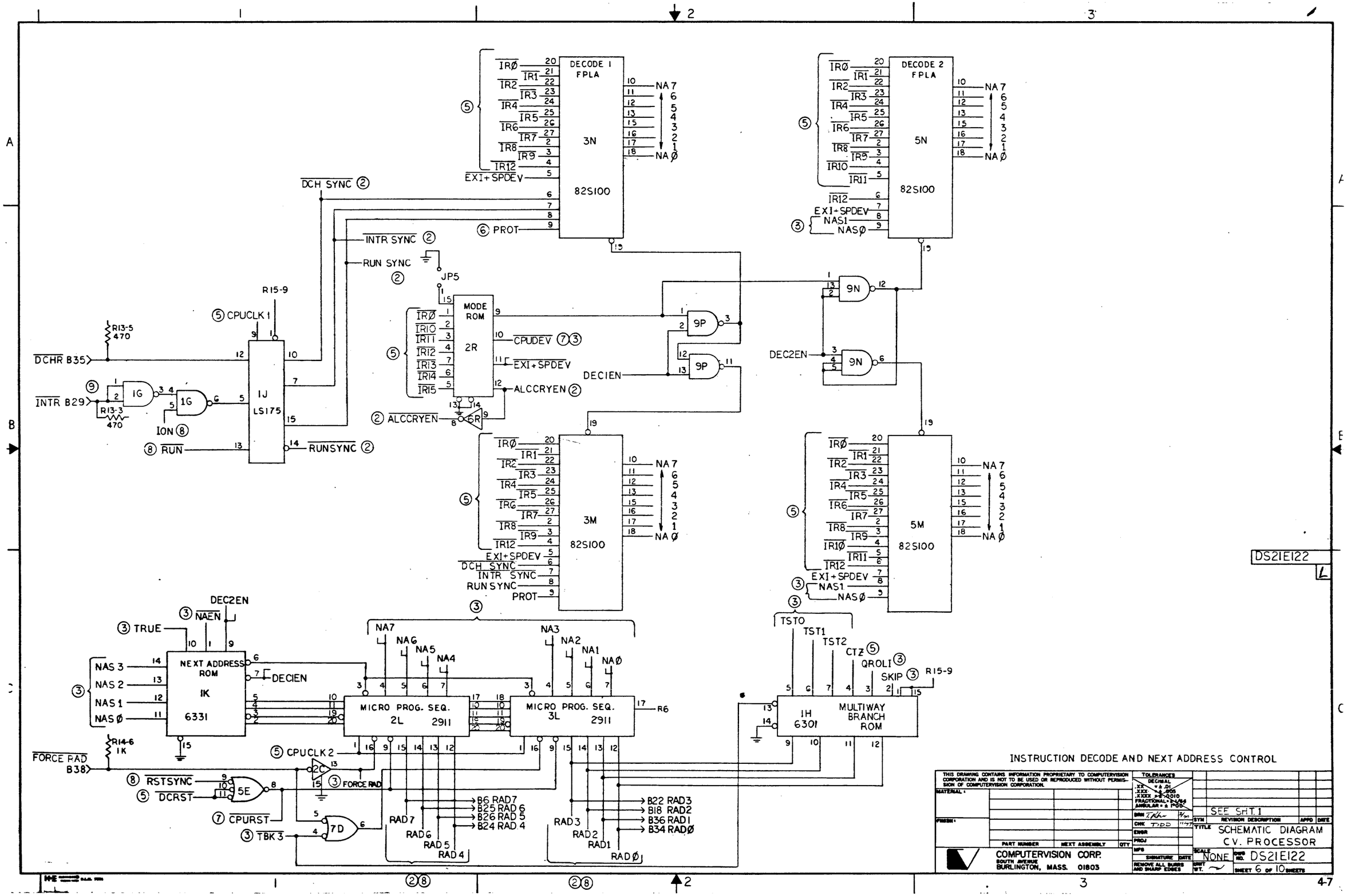
TOLERANCES
DECIMAL
FRACTIONAL ± 1/64
ANGULAR ± 5 MIN.
PART NUMBER
NEXT ASSEMBLY
QTY
SIGNATURE
DATE
REMOVE ALL BURRS AND SHARP EDGES
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
SEE SHT. 1
SYM
REVISION DESCRIPTION
APPD
DATE
TITLE
SCHEMATIC DIAGRAM
CV PROCESSOR
SCALE NONE
SIZE
DWG NO. DS21E122
SHEET 5 OF 10 SHEETS
4-6



INSTRUCTION DECODE AND NEXT ADDRESS CONTROL

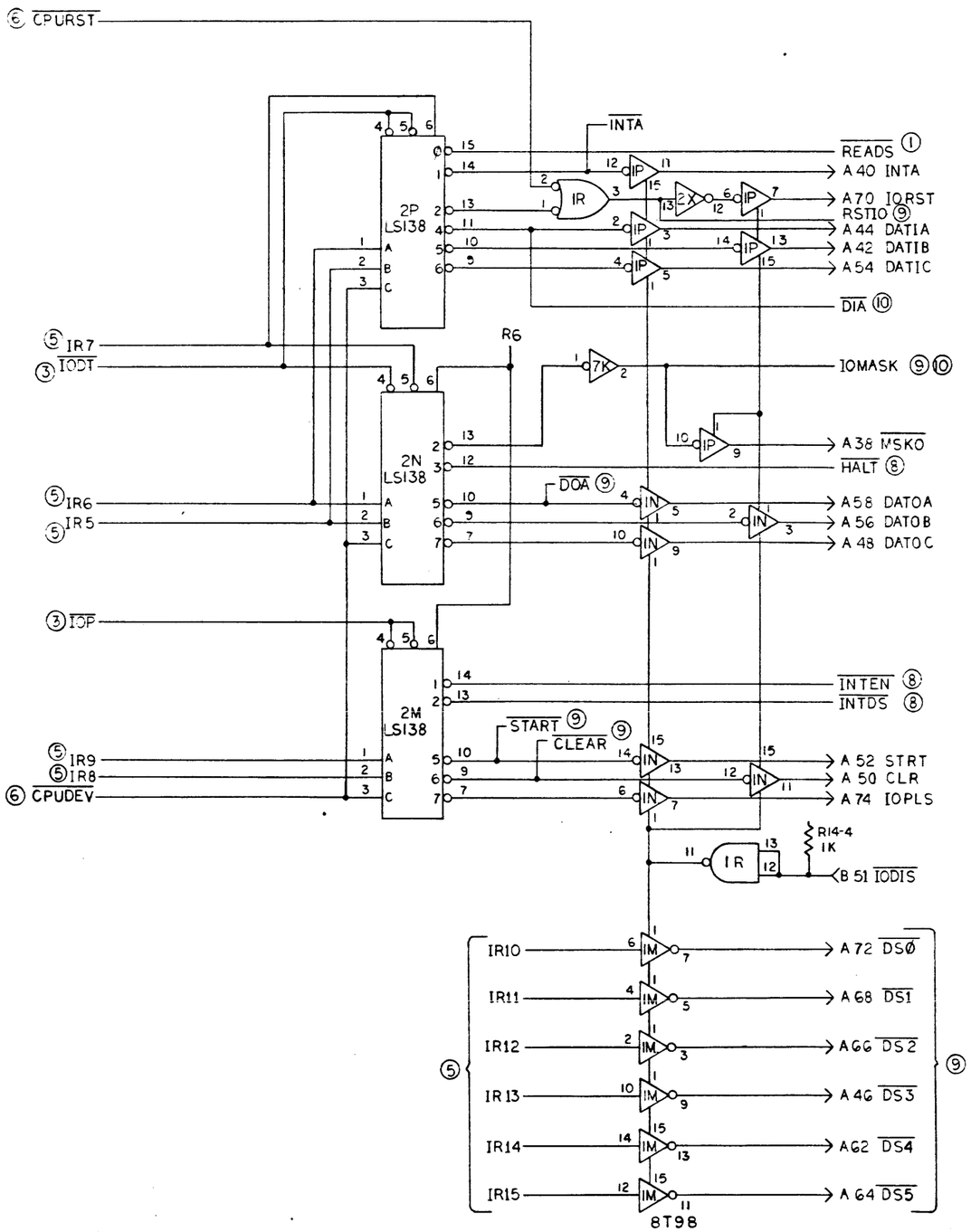
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

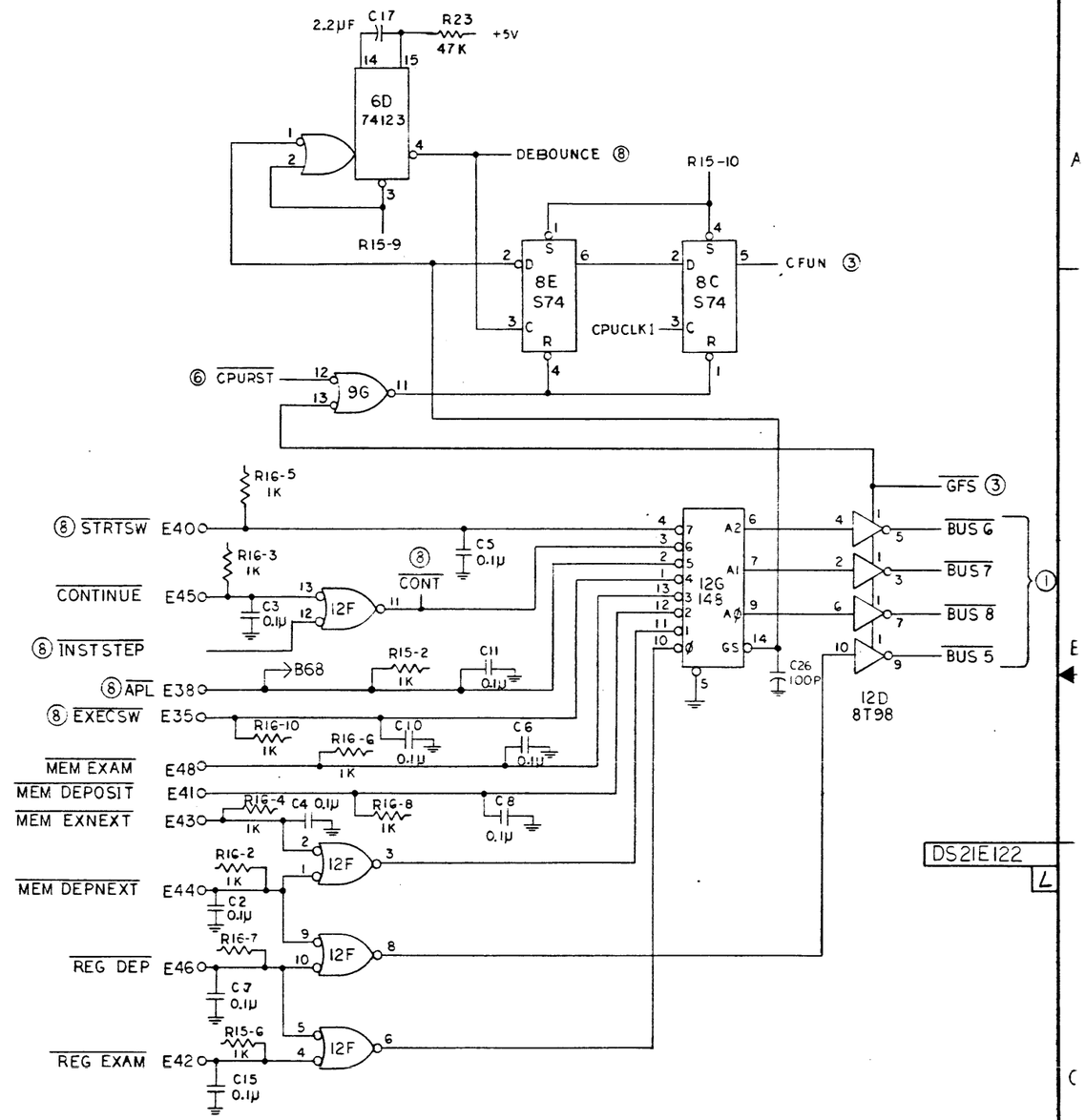
SEE SHT. 1

SCALE NONE

DWG NO. DS21E122

SHEET 6 OF 10 SHEETS





CONTROL PANEL FUNCTION ENCODE I/O PULSE GENERATOR

MATERIAL · FINISH · PART NUMBER · NEXT ASSEMBLY · QTY

TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 .XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 1°00'

DRN · CHK · ENGR · PROJ · MFG · SIGNATURE · DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SH.T.1

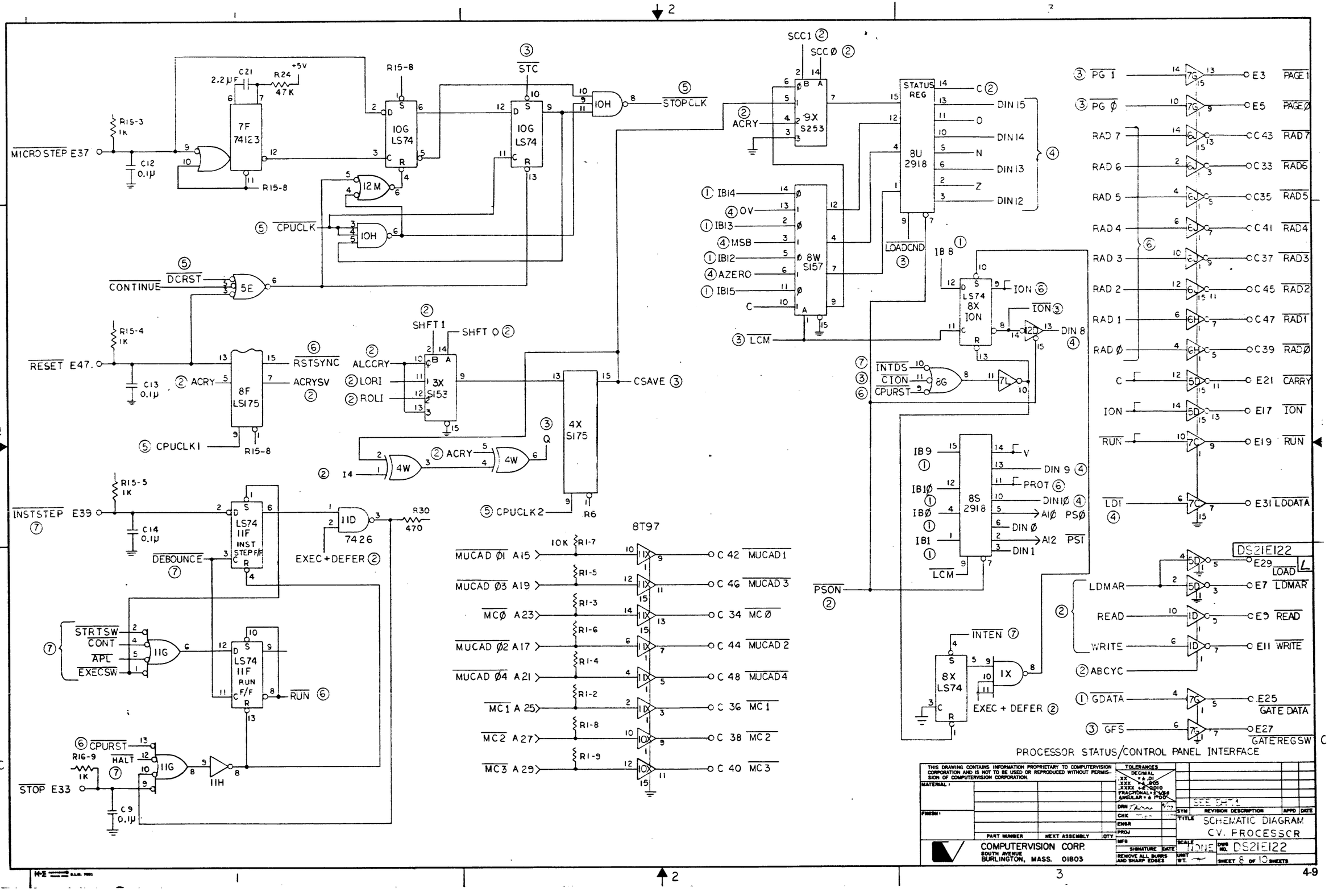
SYM	REVISION DESCRIPTION	APPD	DATE

TITLE SCHEMATIC DIAGRAM CV. PROCESSOR

SCALE NONE DWG NO. DS21E122

UNIT WT. SHEET 7 OF 10 SHEETS

COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803



TOLERANCES
DECIMAL
XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHT 1		

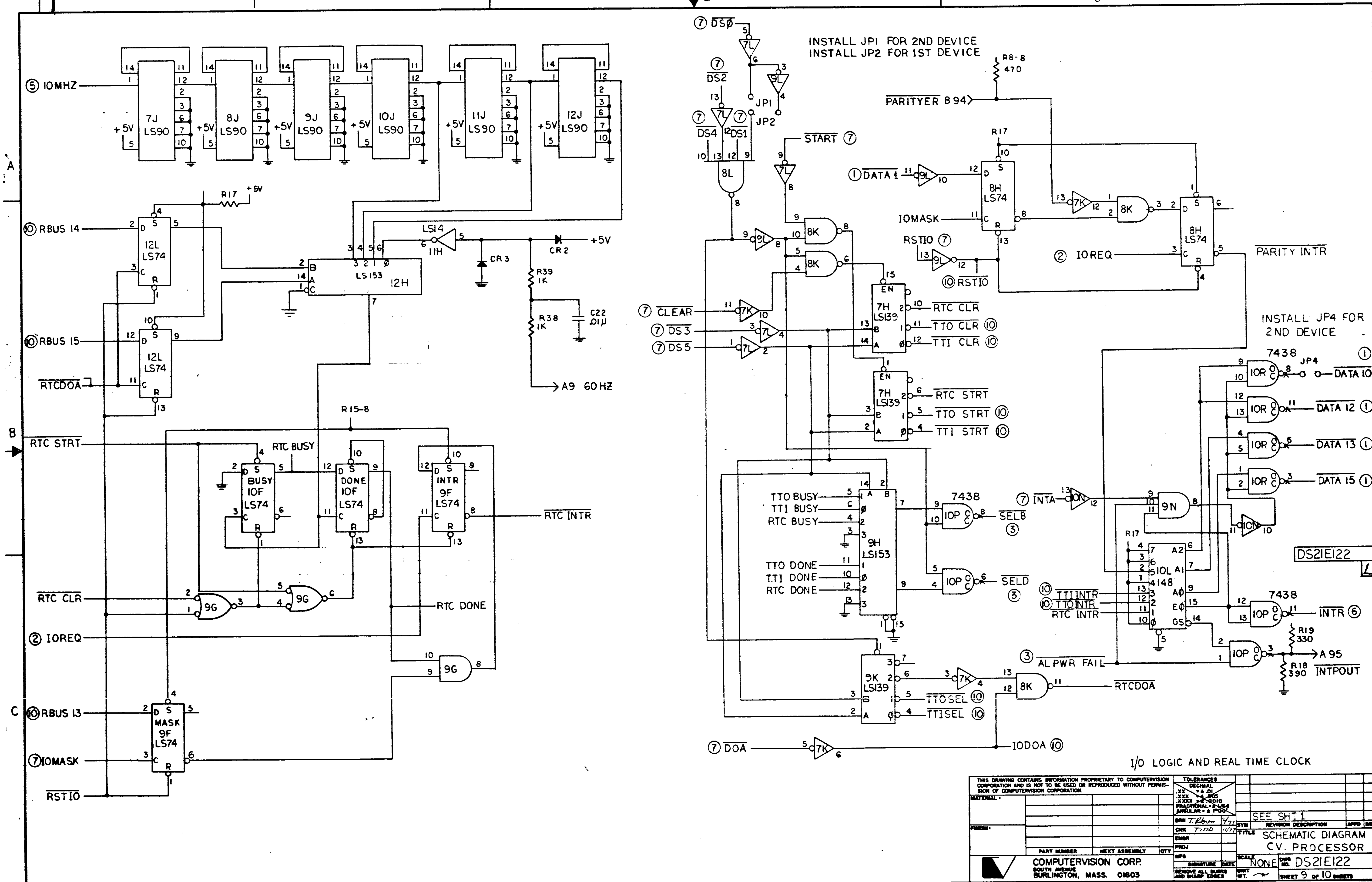
DRN
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

MATERIAL
FINISH
PART NUMBER NEXT ASSEMBLY QTY

TITLE SCHEMATIC DIAGRAM
CV. PROCESSOR

SCALE NONE
DWG NO. DS21E122
SHEET 8 OF 10 SHEETS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803



INSTALL JP1 FOR 2ND DEVICE
INSTALL JP2 FOR 1ST DEVICE
INSTALL JP4 FOR 2ND DEVICE
10MHZ
7J LS90
8J LS90
9J LS90
10J LS90
11J LS90
12J LS90
RBUS 14
RBUS 15
RBUS 13
RTCDOA
RTC STRT
RTC CLR
IOREQ
IOMASK
RSTIO
12L LS74
LS153 12H
LS14 11H
CR2
CR3
R39 1K
R38 1K
C22 .01μ
A9 60HZ
+5V
R17
R15-8
RTC BUSY
BUSY 10F LS74
DONE 10F LS74
INTR 9F LS74
MASK 9F LS74
RTC INTR
RTC DONE
9G
DS0
DS2
DS4
DS1
DS3
DS5
JP1
JP2
7L
9L
8L
8K
START
CLEAR
7H LS139
RTC CLR
TTO CLR
TTI CLR
RTC STRT
TTO STRT
TTI STRT
TTO BUSY
TTI BUSY
RTC BUSY
TTO DONE
TTI DONE
RTC DONE
9H LS153
7438
SELB
SELD
9K LS139
TTOSEL
TTISEL
DOA
IODOA
RTCDOA
7K
R8-8 470
PARITYER B94
DATA 1
8H LS74
IOMASK
RSTIO
IOREQ
PARITY INTR
JP4
DATA 10
DATA 12
DATA 13
DATA 15
10R
INTA
9N
10N
10L 4148
TTI INTR
TTO INTR
RTC INTR
AL PWR FAIL
10P
INTR
R19 330
R18 390
A95
INTPOUT
DS21E122
I/O LOGIC AND REAL TIME CLOCK
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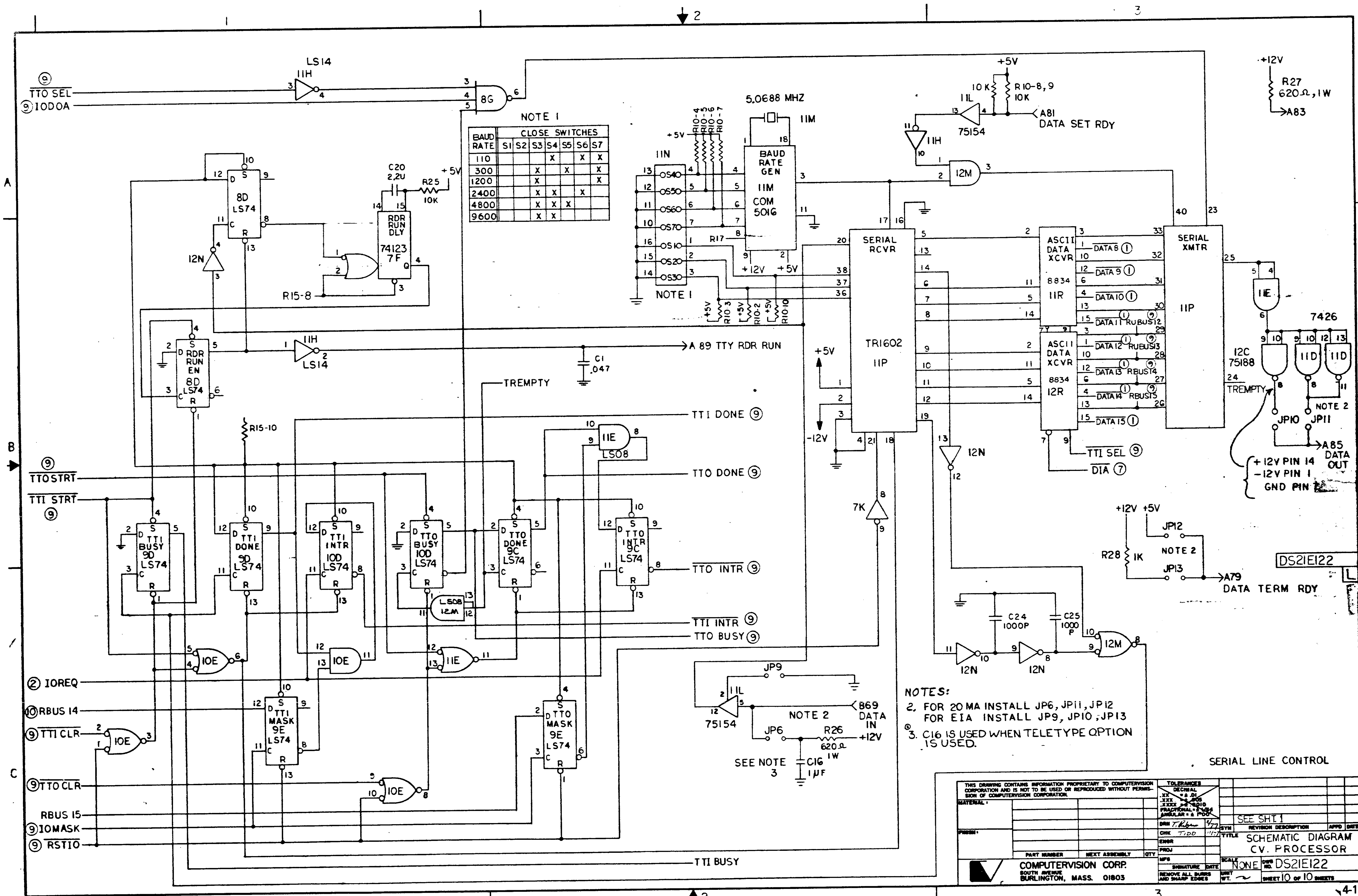
MATERIAL:
FINISH:
PART NUMBER
NEXT ASSEMBLY
QTY
TOLERANCES
DECIMAL
.XX = ±.01
.XXX = ±.005
.XXXX = ±.0010
FRACTIONAL = ±1/64
ANGULAR = ± 1°00'
SEE SHT 1
REVISION DESCRIPTION
TITLE SCHEMATIC DIAGRAM CV. PROCESSOR
COMPUTERVISION CORP.
SOUTH AVENUE BURLINGTON, MASS. 01803
REMOVE ALL BURRS AND SHARP EDGES
SCALE NONE
DWG NO. DS21E122
SHEET 9 OF 10 SHEETS



BAUD RATE	CLOSE SWITCHES S1	S2	S3	S4	S5	S6	S7
110				X		X	X
300			X		X		X
1200			X				X
2400			X	X		X	
4800			X	X	X		
9600			X	X			

NOTE 1

NOTES:

2. FOR 20 MA INSTALL JP6, JP11, JP12
   FOR EIA INSTALL JP9, JP10, JP13
3. C16 IS USED WHEN TELETYPE OPTION IS USED.

SERIAL LINE CONTROL

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SEE SHT 1

TITLE: SCHEMATIC DIAGRAM CV. PROCESSOR

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

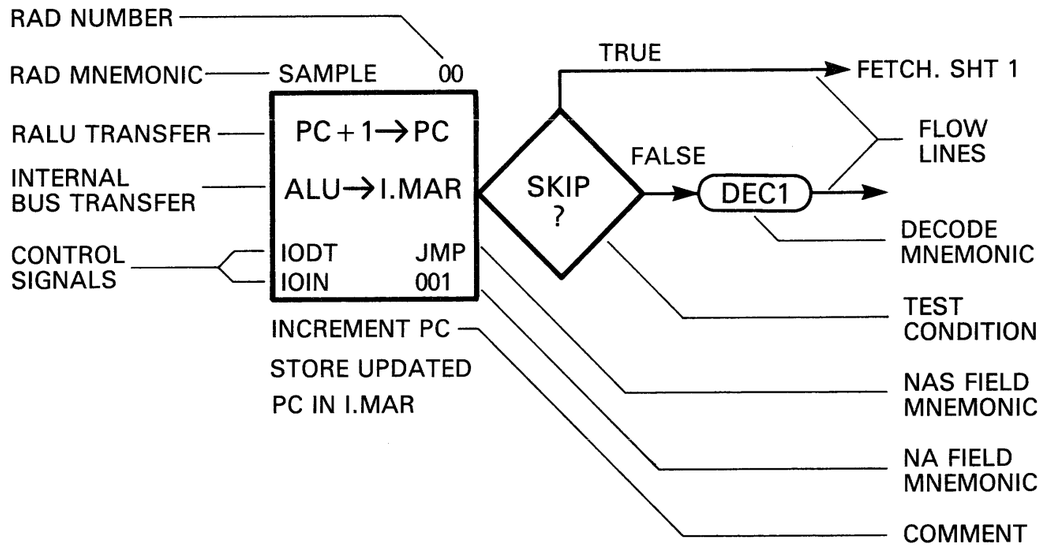
SCALE NONE | DWG NO. DS21E122 | SHEET 10 OF 10 SHEETS

Microprogram Flow Chart

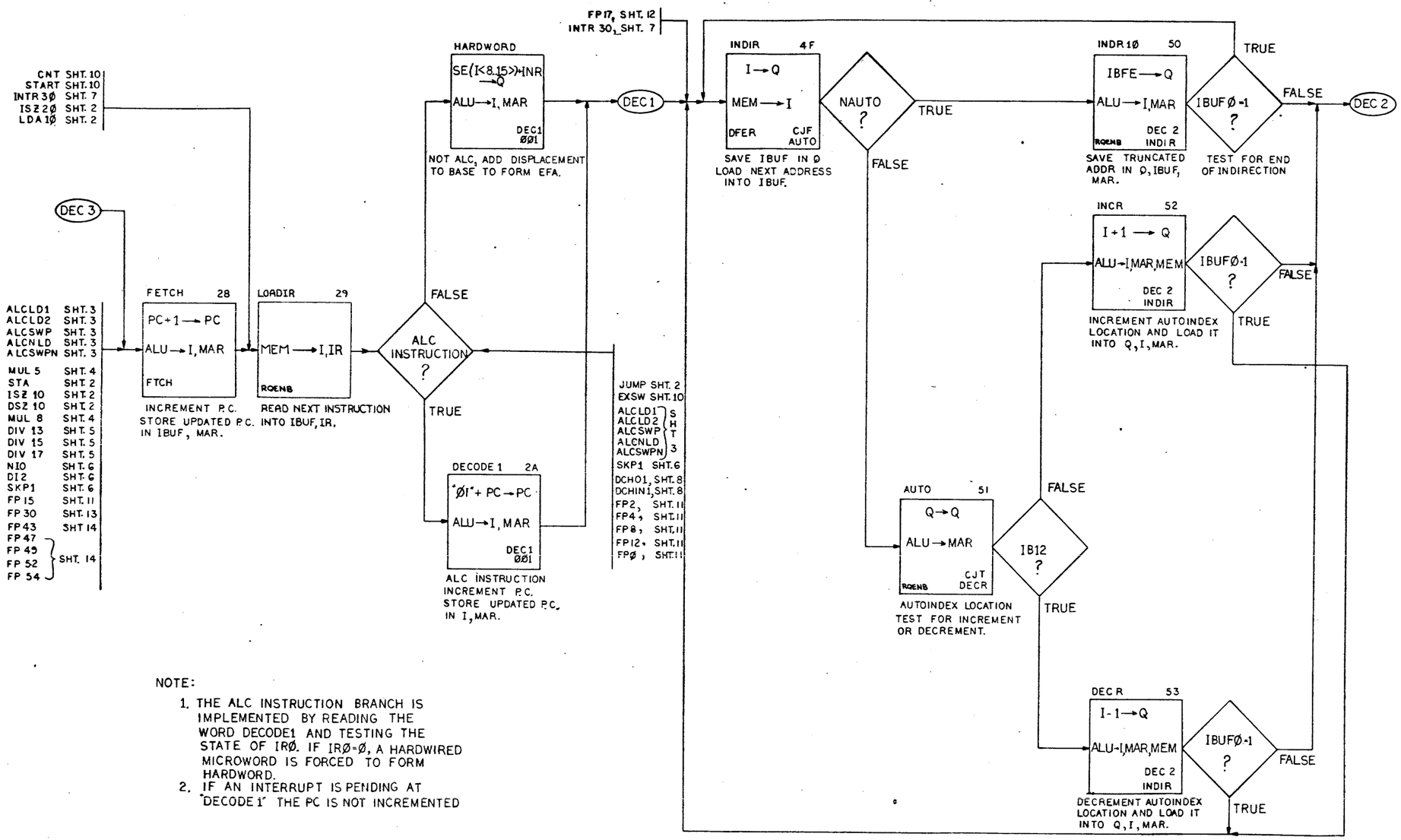
Interpreting the Flow Charts

The flow charts are divided into three sections. The first 10 pages (Sheets 1-10) show the operation code for the CPU. The next four pages (Sheets 11-14) show the operation code for the FPU. And the last 13 pages (Sheets 15-27) show the code for the microdiagnostics.

Symbols. The flow charts use three symbols: squares, diamonds, and ovals. The square represents the RAD currently being executed. The diamond represents a test condition. The oval indicates a decoding of the instruction. Flow lines connect these three symbols to indicate their sequential relationship. Mnemonics and comments accompanying each square also help to indicate the flow.



Flow Chart Symbols



NOTE:

1. THE ALC INSTRUCTION BRANCH IS IMPLEMENTED BY READING THE WORD DECODE1 AND TESTING THE STATE OF IRØ. IF IRØ=Ø, A HARDWIRED MICROWORD IS FORCED TO FORM HARDWORD.
2. IF AN INTERRUPT IS PENDING AT "DECODE 1" THE PC IS NOT INCREMENTED

DS21E015
E

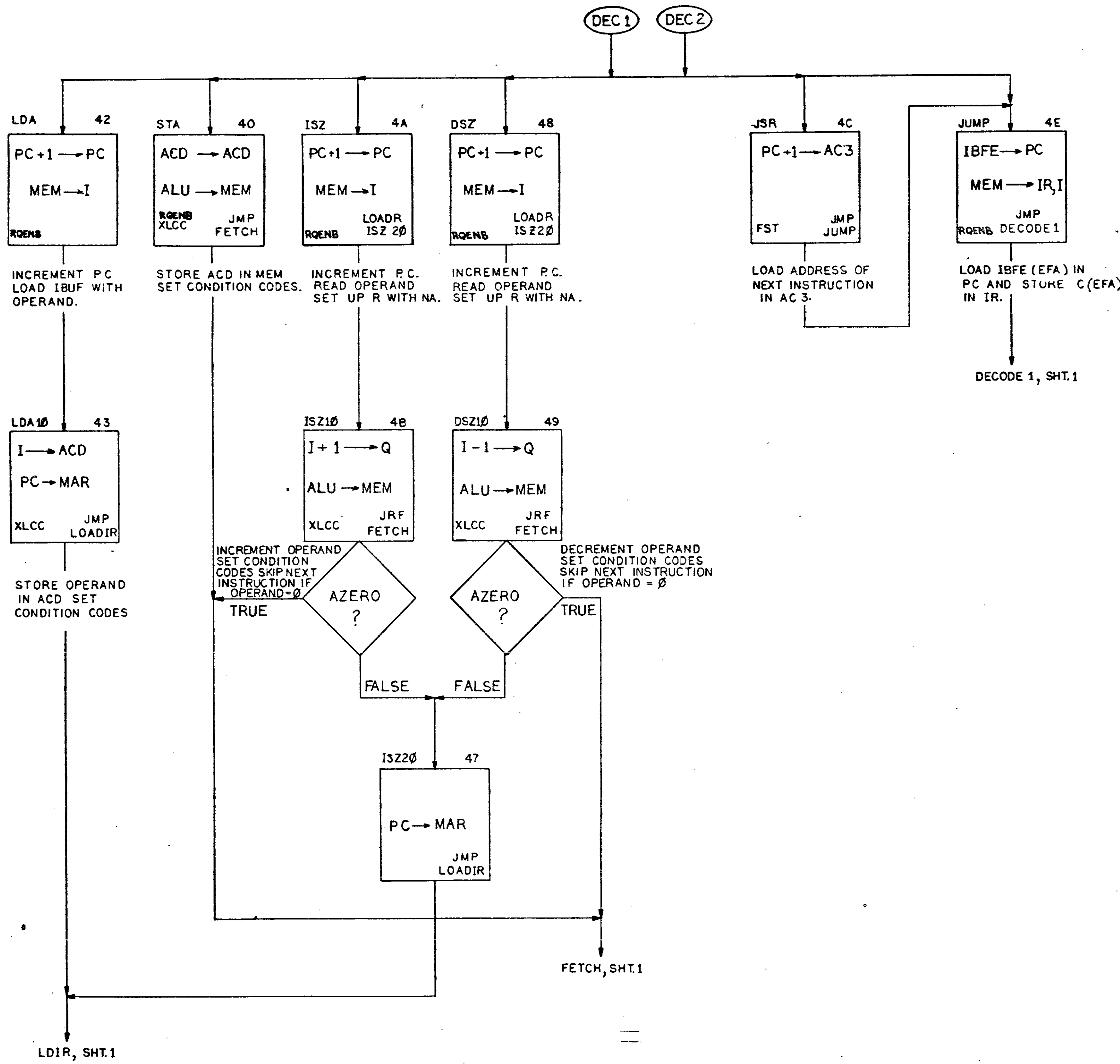
INSTRUCTION FETCH
INDIRECT ADDRESSING

SYM	REVISION DESCRIPTION	CK	APPD	DATE
E	ECO #3433			
D	ECO #3298			
B	ECO #2779			
A	RELEASE ECO 2578			

TITLE: CVP MICROPROGRAM FLOW CHARTS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

SCALE: NONE | DWG NO. DS21E015 | SHEET 1 OF 27 SHEETS



DS21E015
E

MOVE DATA MODIFY MEMORY
AND JUMP INSTRUCTIONS

MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

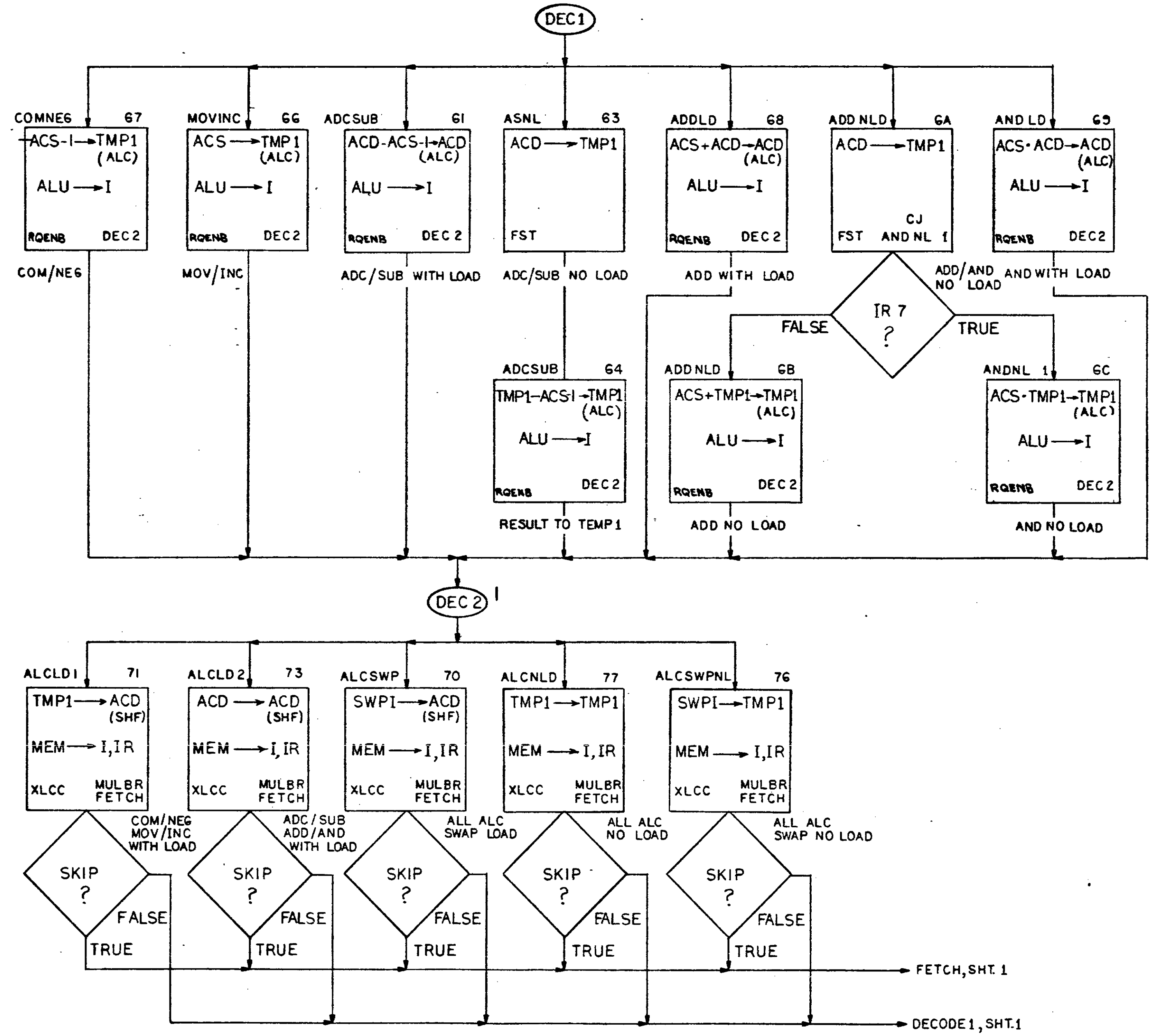
TOLERANCES: DECIMAL .XX ± .01, .XXX ± .005, .XXXX ± .0010, FRACTIONAL ± 1/64, ANGULAR ± 1°00'

DRN T. Rizzo 3/77
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1
SYM | REVISION DESCRIPTION | APPD | DATE

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

TITLE CVP MICROPROGRAM FLOW CHARTS
SCALE NONE
DWG NO. DS21E015
UNIT WT. —
SHEET 2 OF 27 SHEETS



DS21E015

E

ALC INSTRUCTIONS

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TITLE	CVP MICROPROGRAM FLOW CHARTS
SEE SHT. 1	
SCALE	NONE
DWG NO.	DS21E015
SHEET	3 OF 27 SHEETS

COMPUTERVISION CORP.
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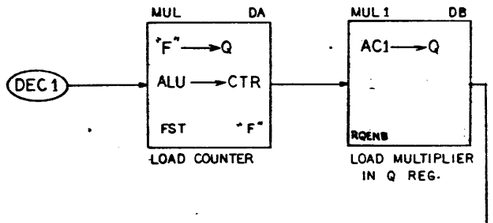
BURLINGTON, MASS. 01803

INPUT:

AC2 = MULTIPLICAND
AC1 = MULTIPLIER
ACØ = ADDITIVE CONSTANT

OUTPUT:

AC2 = UNCHANGED
AC1 = LOW ORDER WORD OF ACØ + (AC1 * AC2)
ACØ = HIGH ORDER WORD OF ACØ + (AC1 * AC2)
ZBIT = ((AC1 EQ.Ø) .AND. (ACØ .EQ.Ø))
N = MSB OF ACØ
C = NO CHANGE
O = Ø



MUL DA
"F" → Q
ALU → CTR
FST "F"
LOAD COUNTER

MUL 1 DB
AC1 → Q
RQENB
LOAD MULTIPLIER IN Q REG.

MUL 2 DI
AC2+ACØ → ACØ (RSLBQ, ALC)
DECTR MULBR MUL4
Q ODD: ADD AC2 THEN SHIFT.

MULC (COUNT=Ø, Q15-1)
(0,1)
(0,0)
(1,*)

MUL 3 DØ
ACØ → ACØ (RSLBQ, ALC)
DECTR MULBR MUL 4
Q EVEN: SHIFT

MUL 9 DC
(RSLBQ)
MULBR MUL 2
RIGHT SHIFT Q

MUL C (COUNT=Ø, Q15-1)
(0,1)
(0,0)

MUL 4 D2
Q → AC1
CJT MUL5
RQENB
STORE LOW RESULT IN AC1.

AZERO ?
TRUE
FALSE

MUL 5 DG
ACØ → ACØ
XLCC FST JMP FETCH
SET Z,N BITS FROM HIGH RESULTS CLEAR O

FETCH SHT. 1

MUL 6 D3
ACØ → ACØ
XLCC FST
SET N BIT FROM HIGH RESULT.

MUL 7 D4
"F5" → TMPØ
FST "F5"
LOAD PS MASK IN TMPØ.

MUL 8 D5
PS·TMPØ → TMPØ
ALU → PS
FST JMP FETCH
SET PS

DS21E015
E

UNSIGNED INTEGER MULTIPLICATION

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 .XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 1°00'

DRN T. Reuss 4/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

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BURLINGTON, MASS. 01803

SEE SHT 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE CVP MICROPROGRAM FLOW CHARTS

SCALE NONE DWG NO. DS21E015

UNIT WT.

SHEET 4 OF 27 SHEETS

DEC1

DIV 2C — "F" → Q; ALU → CTR; FST; "F"
LOAD COUNTER

DIV1 2D — AC1 → Q; FST; LOAD R; DIV 16
LOAD LOW ORDER DIVEDEND IN Q.
RESET CSAVE
SET QBIT.

DIV 3 2E — ACØ-AC2→ACØ (LSLBQ1, MD); ALU → I; RQENB; CJF DIV 7
DO 1RST SUBTRACTION

QBIT-1 ?
TRUE
FALSE

DIV 5 2F — I → ACØ; FST; JMP DIV 14
ERROR POSITIVE RESULTS.

DIV14 3A — ACØ+AC2→ACØ; FST
RESTORE ACØ

INPUT:
ACØ HIGH ORDER DIVIDEND
AC1 LOW ORDER DIVIDEND
AC2 DIVISOR

OUTPUT:
IF ACØ ≥ AC2 (ERROR)
C=1 O=Ø
Z=(AC2 .EQ. Ø) N=MSB OF AC2
ELSE
AC1= QUOTIENT
ACØ= REMAINDER
AC2 UNCHANGED
C=Ø
Z= (AC1 .EQ. Q) AND (ACØ .EQ. Ø)
N= MSB OF AC1
O= Ø

DIV 6 3B — TMPØ-TMPØ→TMPØ (MDV); XLCC; FST
SET CARRY

DIV15 3C — AC2 → AC2; XLCC; FST; JMP FETCH
SET Z BIT OF PS IF DIVISOR = 0
SET N BIT IF AC2Ø = 1
CLEAR O BIT.

→ FETCH, SHT. 1

(0,0) (1,0) (0,1) (1,1)

DIV 7 30 — AC2-ACØ→ACØ (LSLBQ MDV); ALU → I; DECTR; MULBR DIV1Ø
ADD CYCLE

DIVC (COUNT=Ø, QBIT=1)

DIV 8 31 — ACØ-AC2→ACØ (LSLBQ MDV); ALU → I; DECTR; MULBR DIV1Ø
SUBTRACT CYCLE

DIV C (COUNT=Ø, QBIT=1)

DIV10 36 — AC2 → ACØ; FST; LOADR DIV 16
COUNT=0, NEGATIVE REMAINDER
SET UP FOR REMAINDER RESTORE
LOAD R

DIV11 37 — I+ACØ → ACØ; RQENB; JRF DIV 13
RESTORE REMAINDER

AZERO ?
TRUE
FALSE

DIV13 38 — Q → AC1 (MDV); XLCC; FST; JM FETCH
STORE QUOTIENT IN AC1
SET Z BIT OF PS IF QUOTIENT=Ø
SET N BIT OF PS IF QØ=1
CLEAR O AND C.

DIV 9 32 — I → ACØ; RQENB; JRF DIV 13
COUNT=0 POSITIVE REMAINDER
RESTORE REMAINDER.

AZERO ?
TRUE
FALSE

DIV16 33 — Q → AC1; XLCC; FST
SET N BIT OF PS IF Q Ø=1

DIV12 34 — "F4" → TMPØ; FST; "F4"
LOAD CONSTANT IN TMPØ

DIV17 35 — PS·TMPØ→TMPØ; ALU → PS; FST; JMP FETCH
AND CONSTANT WITH PS TO FORM CC BITS.

UNSIGNED INTEGER DIVISION

DS21E015
E

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN T. Rivera 7/77
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

SEE SHT. 1

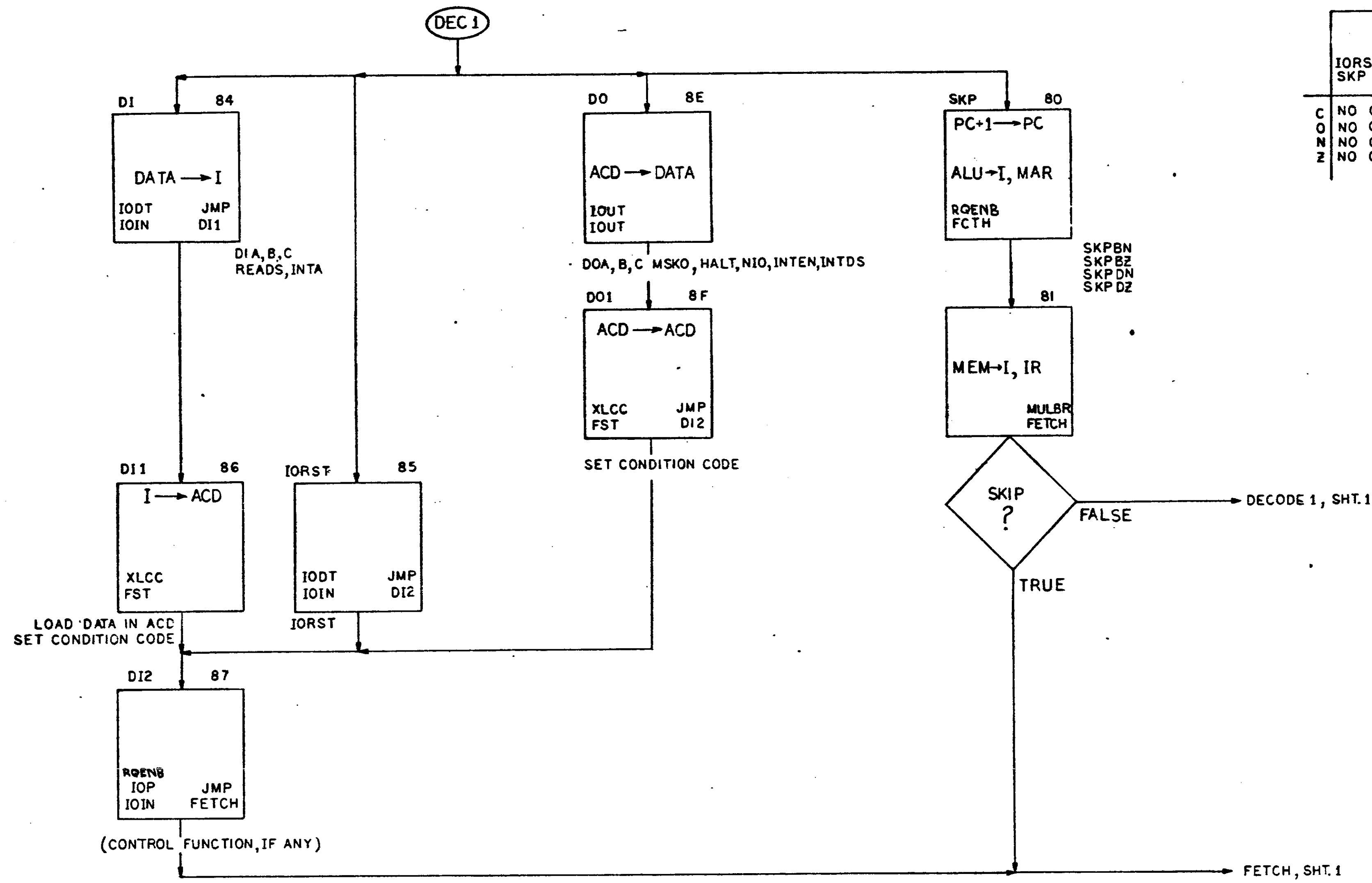
SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: CVP MICROPROGRAM FLOW CHART

SCALE: NONE
SIZE: E
DWG NO. DS21E015
UNIT WT.
SHEET 5 OF 27 SHEETS

CONDITION CODE BITS FOR I/O

	IORST SKP	DIA,B,C READS INTA	DO A,B,C MSKO HALT NIO INTEN INTDS
C	NO CHANGE	NO CHANGE	NO CHANGE
O	NO CHANGE	Ø	Ø
N	NO CHANGE	MSB DATA IN	MSB DATA OUT
Z	NO CHANGE	DATA IN = Ø	DATA OUT = Ø



D??21E015

E

I/O INSTRUCTIONS

MATERIAL:

FINISH:

PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES DECIMAL .XX = ±.01 .XXX = ±.005 .XXXX = ±.0010 FRACTIONAL = ± 1/64 ANGULAR = ± 1°00'

DRN T.K... 4/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1
SYM | REVISION DESCRIPTION | APPD | DATE

TITLE CVP MICROPROGRAM FLOW CHART

SCALE NONE
DWG NO. D??1E015
UNIT WT. —
SHEET 6 OF 27 SHEETS

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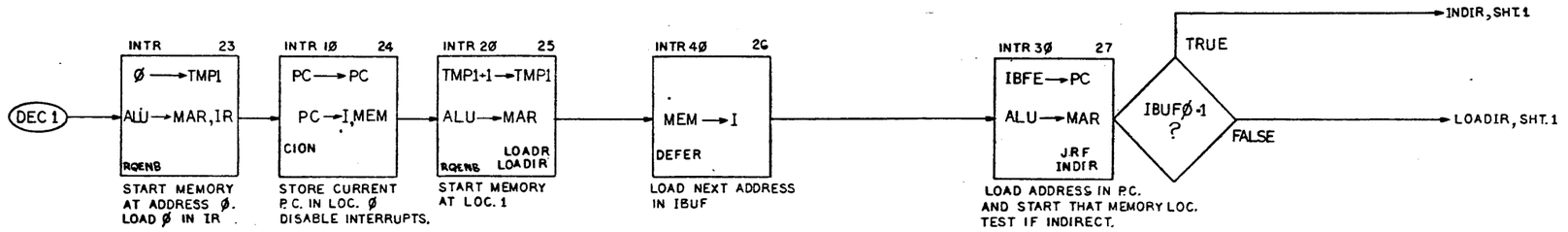
SOUTH AVENUE
BURLINGTON, MASS. 01803



DS21E015 E

INTERRUPT

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MATERIAL:

FINISH:

PART NUMBER | NEXT ASSEMBLY | QTY

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN T. Rivera 4/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

UNIT WT.

SEE SHT. 1

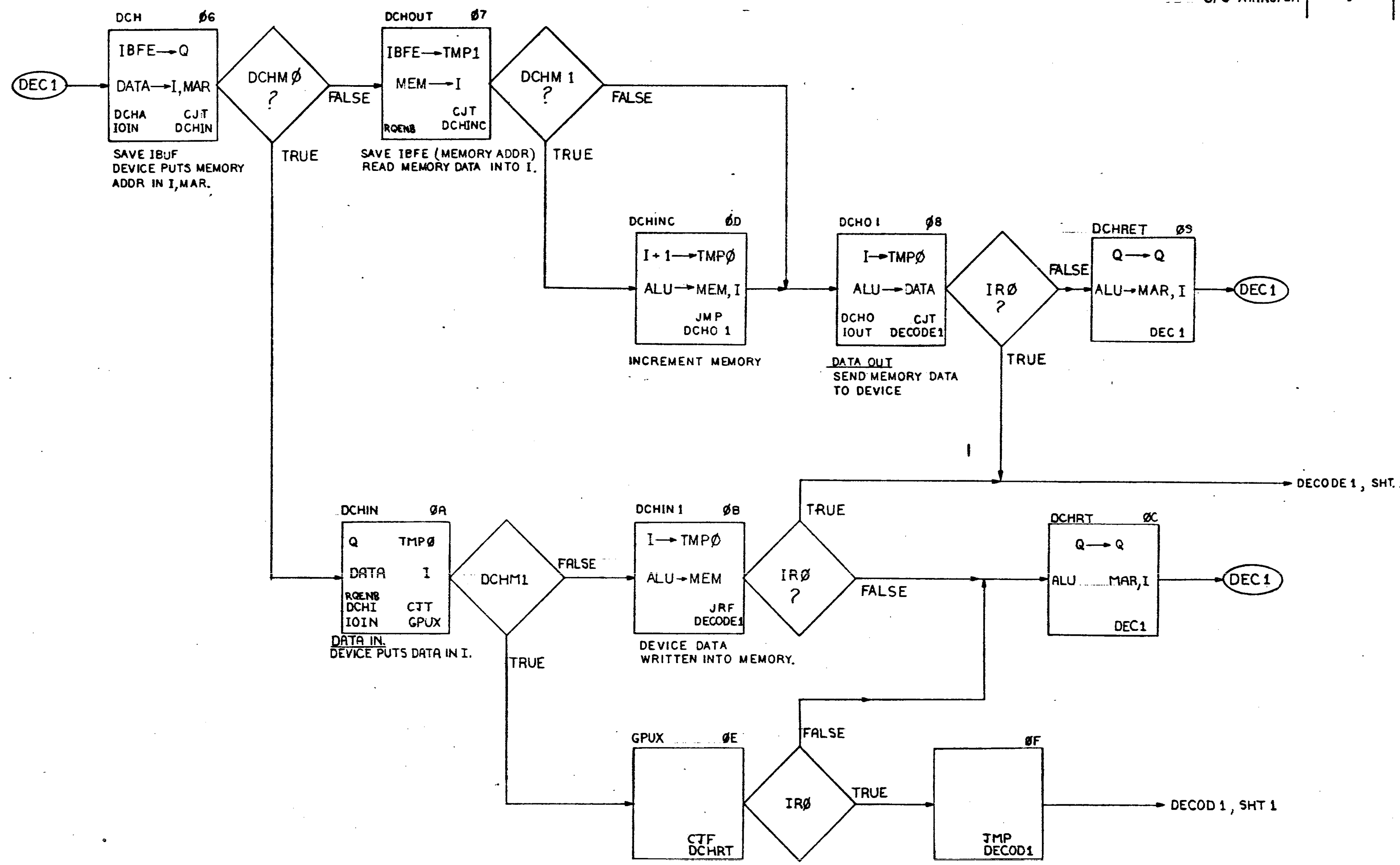
SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: CVP MICROPROGRAM FLOW CHART

SCALE: NONE DWG NO. DS21E015

SHEET 7 OF 27 SHEETS

FUNCTION	DCHMØ	DCHM1
DATA OUT	Ø	Ø
INCREMENT MEMORY	Ø	1
DATA IN	1	Ø
GPU TRANSFER	1	1



DS21E015 E

DATA CHANNEL

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MATERIAL:

FINISH:

PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ±1/64 ANGULAR ±1°00'

DRN T. Ribeiro 4/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT.1

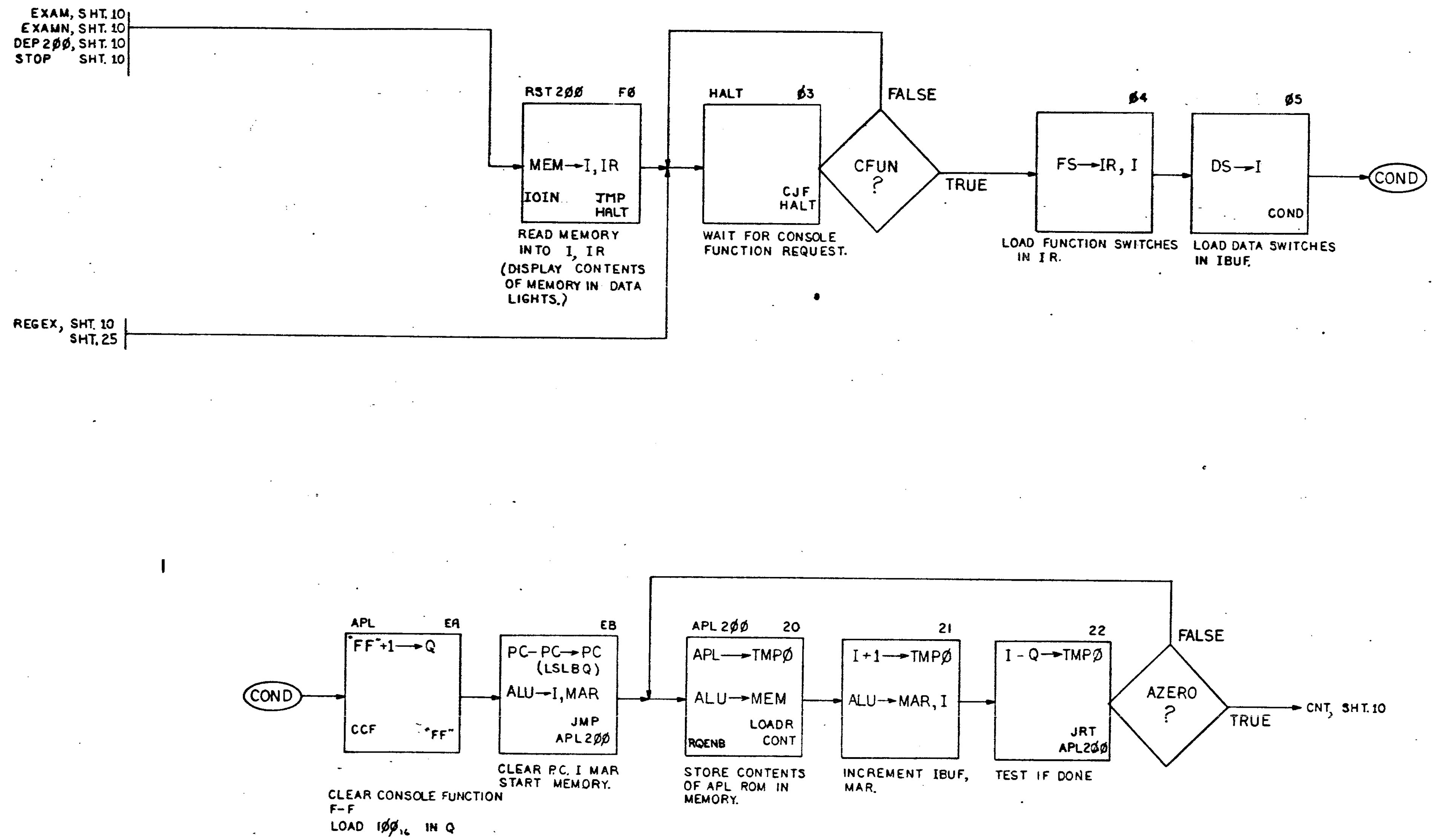
SYM | REVISION DESCRIPTION | APPD | DATE

TITLE CVP MICROPROGRAM FLOW CHART

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

SCALE NONE DWG NO. DS21E015

UNIT WT. — SHEET 8 OF 27 SHEETS



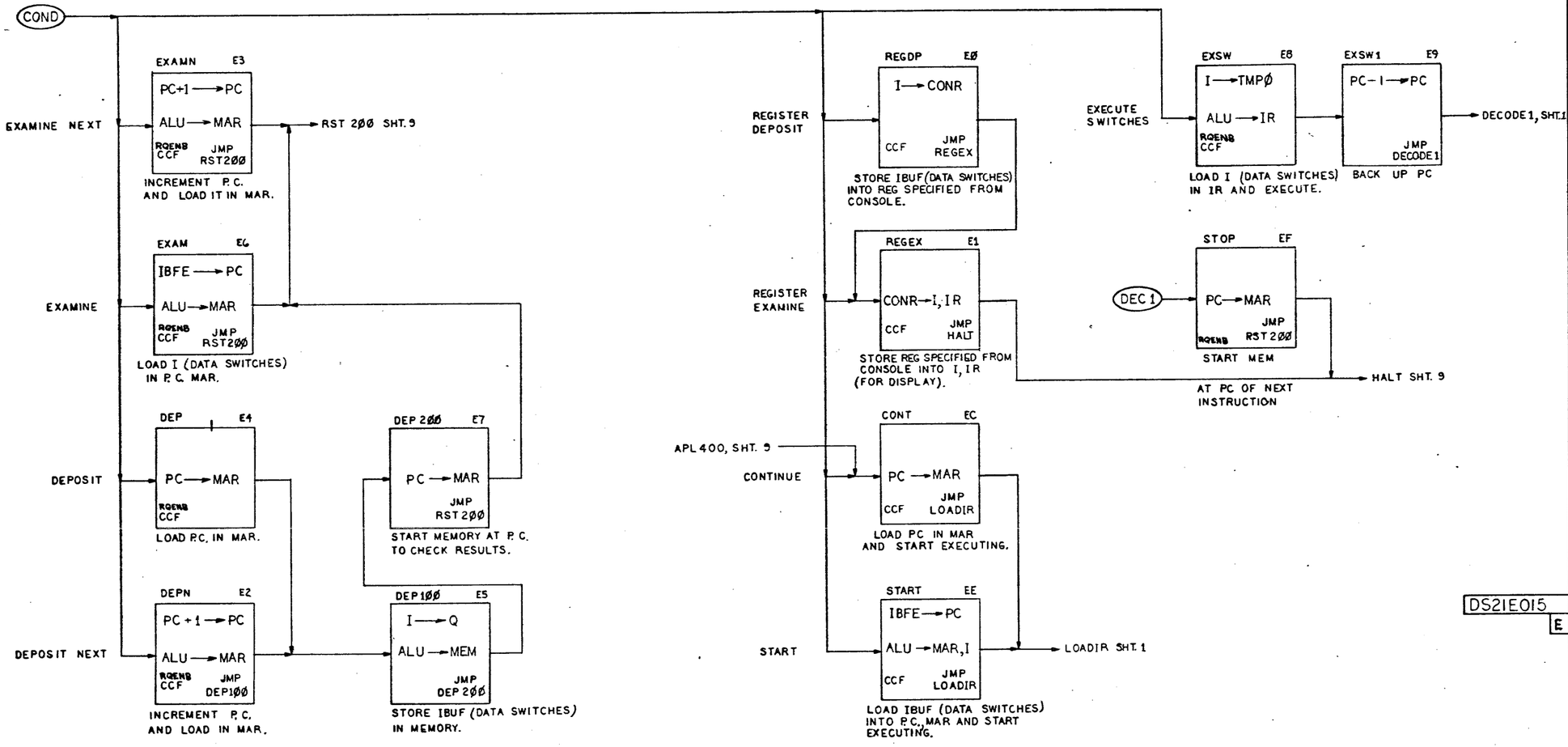
DS21E015

E

CONSOLE FUCNCTIONS I
(RESET, HALT STATE, APL)

MATERIAL:	PART NUMBER	NEXT ASSEMBLY / QTY
FINISH:		
TOLERANCES: DECIMAL .XX = ± .01, .XXX = ± .005, .XXXX = ± .0010, FRACTIONAL = ± 1/64, ANGULAR = ± 1°00'	DRN T. Pibus 4/77	CHK / ENGR / PROJ / MFG
SYM	REVISION DESCRIPTION: SEE SHT. 1	APPD / DATE
TITLE	CVP MICROPROMGRAM FLOW CHART	
SCALE NONE	DWG NO. DS21E015	SHEET 9 OF 27 SHEETS
UNIT WT. —	REMOVE ALL BURRS AND SHARP EDGES	

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803



DS21E015
E

CONSOLE FUNCTIONS II

TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 .XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 1 POINT

MATERIAL

FINISH

PART NUMBER | NEXT ASSEMBLY | QTY

DRN T. Kline 9/17
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

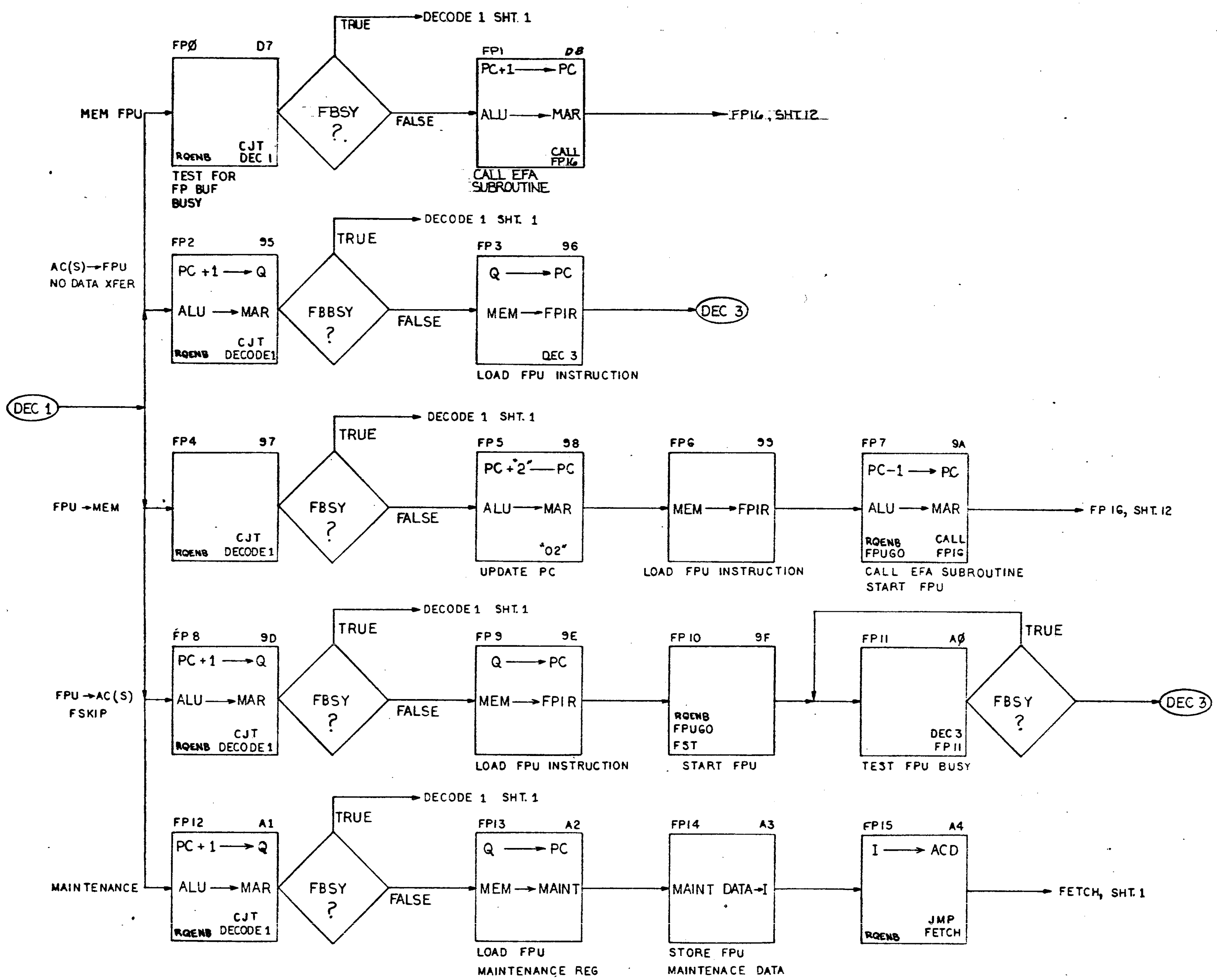
SEE SHT. 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: CVP MICROPROGRAM FLOW CHART

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 10 OF 27 SHEETS



DS21E015 E

FLOATING POINT INTERFACE
(ENTRY POINTS)

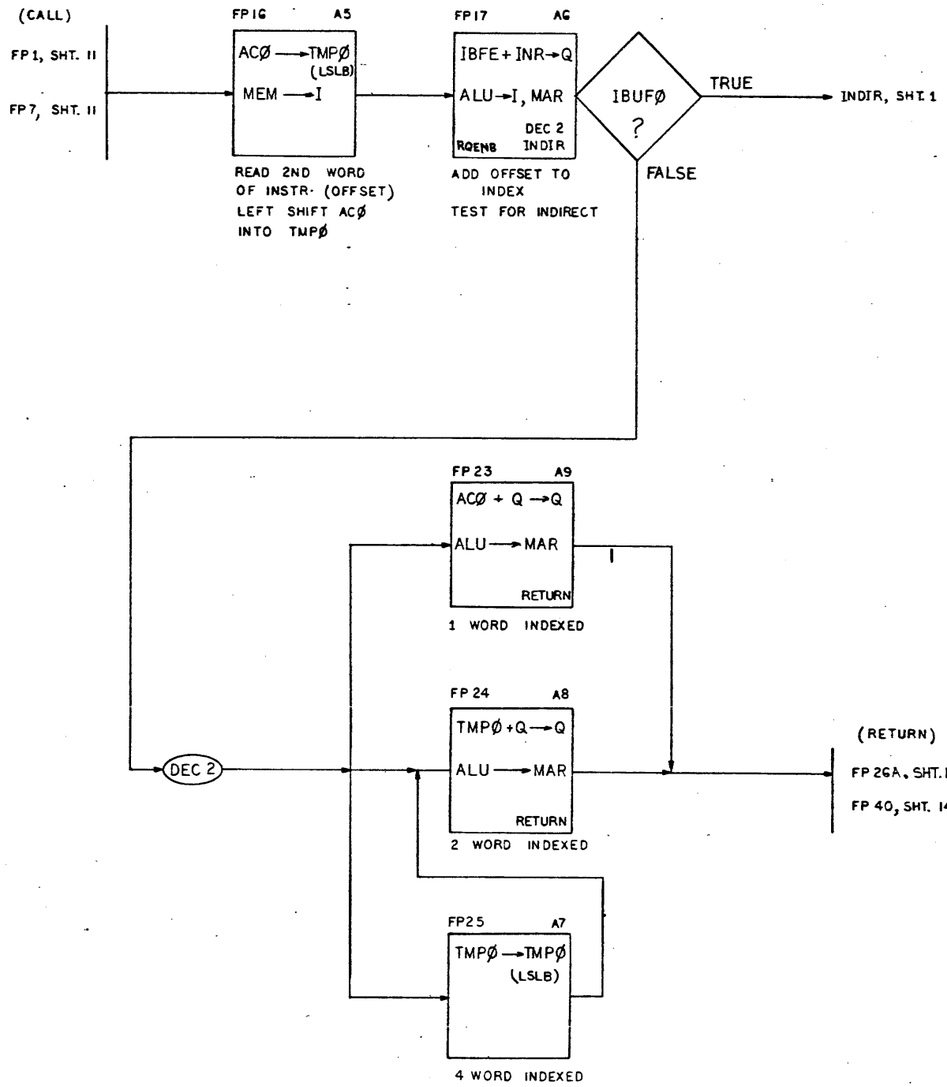
SEE SHT. 1

TITLE: CVP MICROPROGRAM FLOW CHART

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

SCALE NONE DWG NO. DS21E015

SHEET 1 OF 27 SHEETS



DS21E015
E

FLOATING POINT INTERFACE
(EFA)

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 0° 30'

DRN T. Kilburn 8/77
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

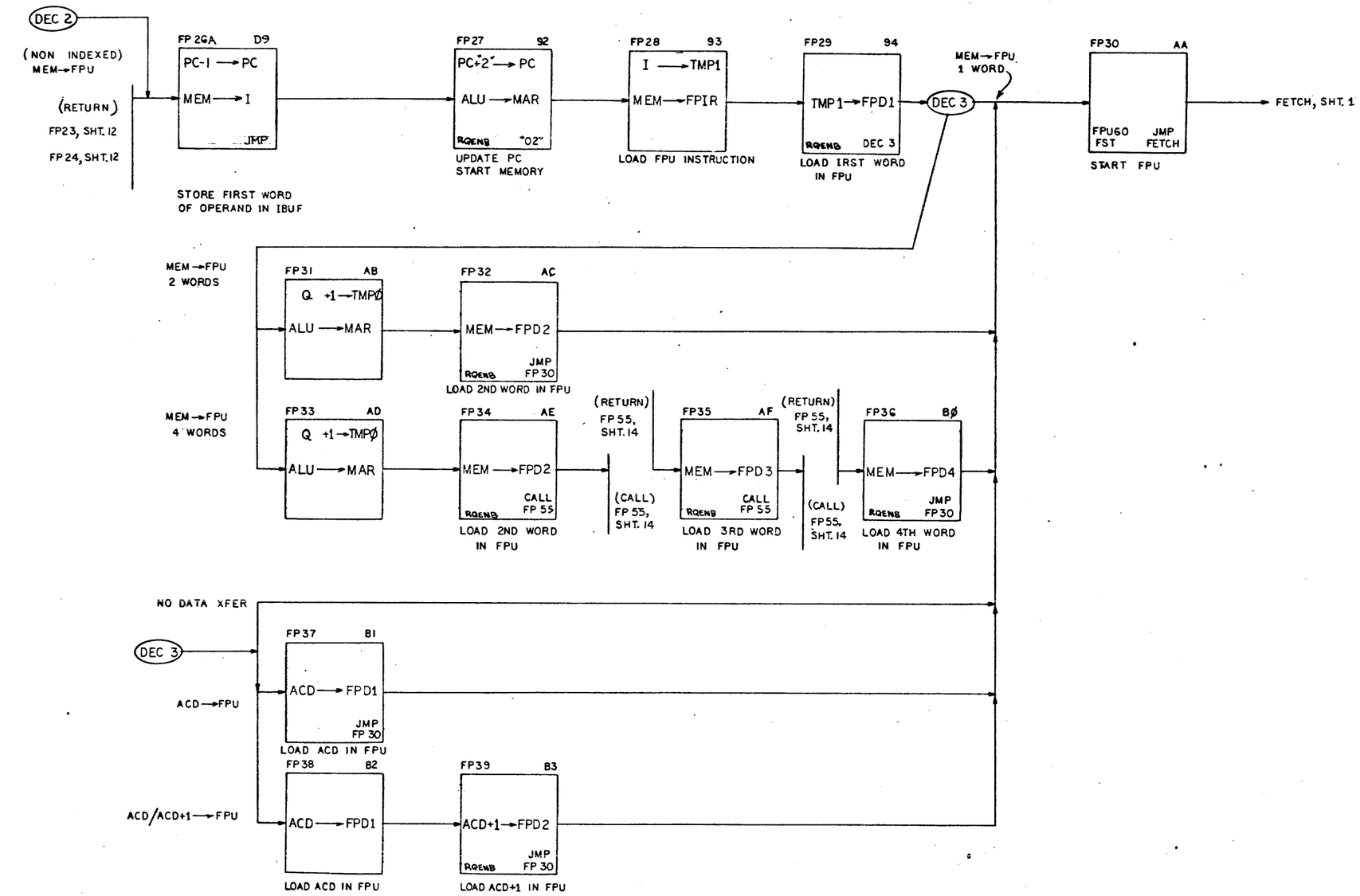
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE CVP MICROPROGRAM FLOW CHART

SCALE NONE
DWG NO. DS21E015
UNIT WT. —#—
SHEET 12 OF 27 SHEETS



DSEE1E015
E

FLOATING POINT INTERFACE
(MEM→FPU, ACS (S)→FPU,
NO DATA XFER)

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 6 MOC

BRN T.Nelson 9/77
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

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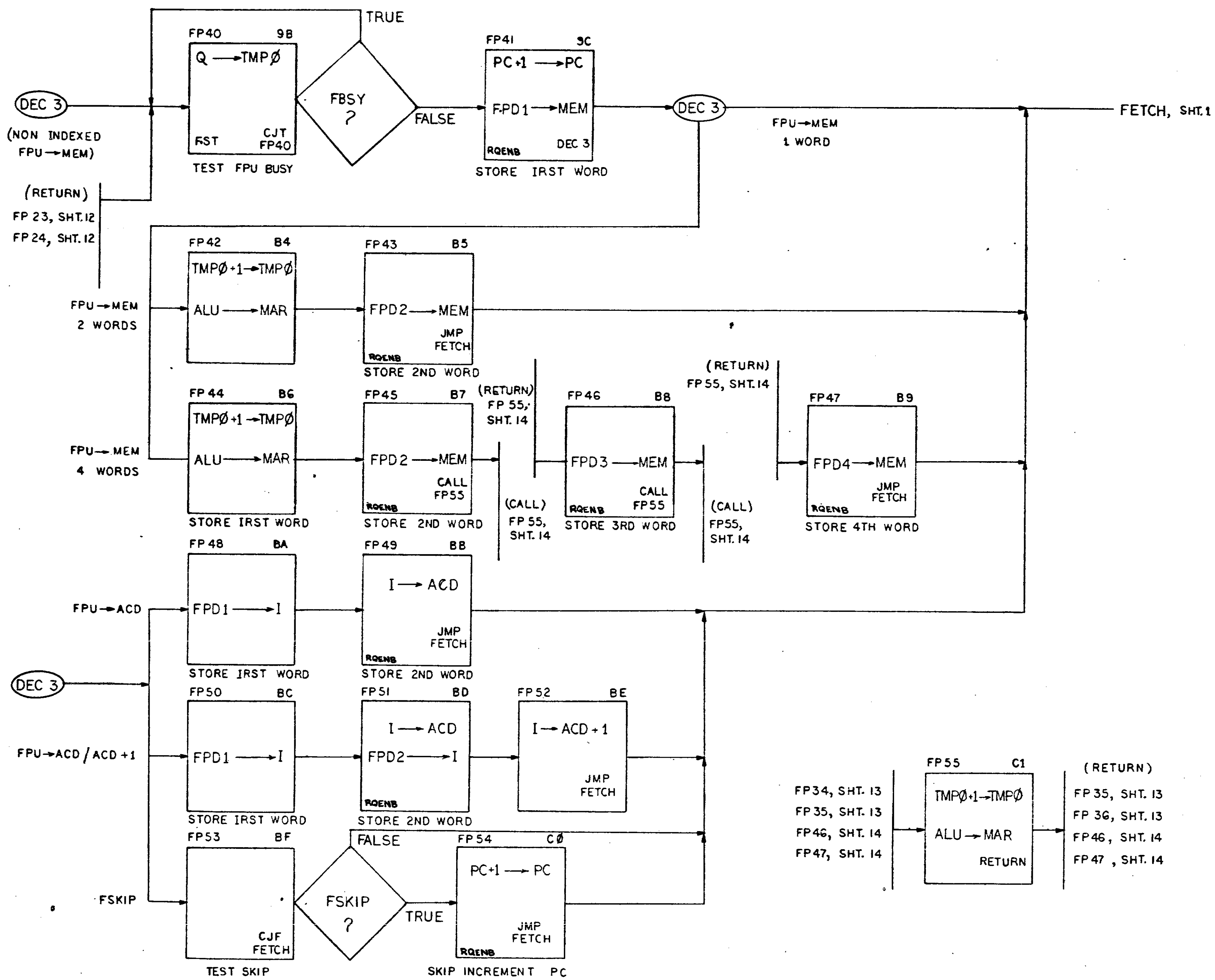
SEE SHT 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE CVF MICRO PROGRAM FLOW CHART

SCALE NONE | DWG NO. DSEE1E015 | REV

SHEET 13 OF 27 SHEETS



DS21E015 E

FLOAT POINT INTERFACE
(FPU→MEM, FPU→ACD(S), FSKIP)

TITLE: CVP MICROPROGRM FLOW CHART

COMPUTERVISION CORP.
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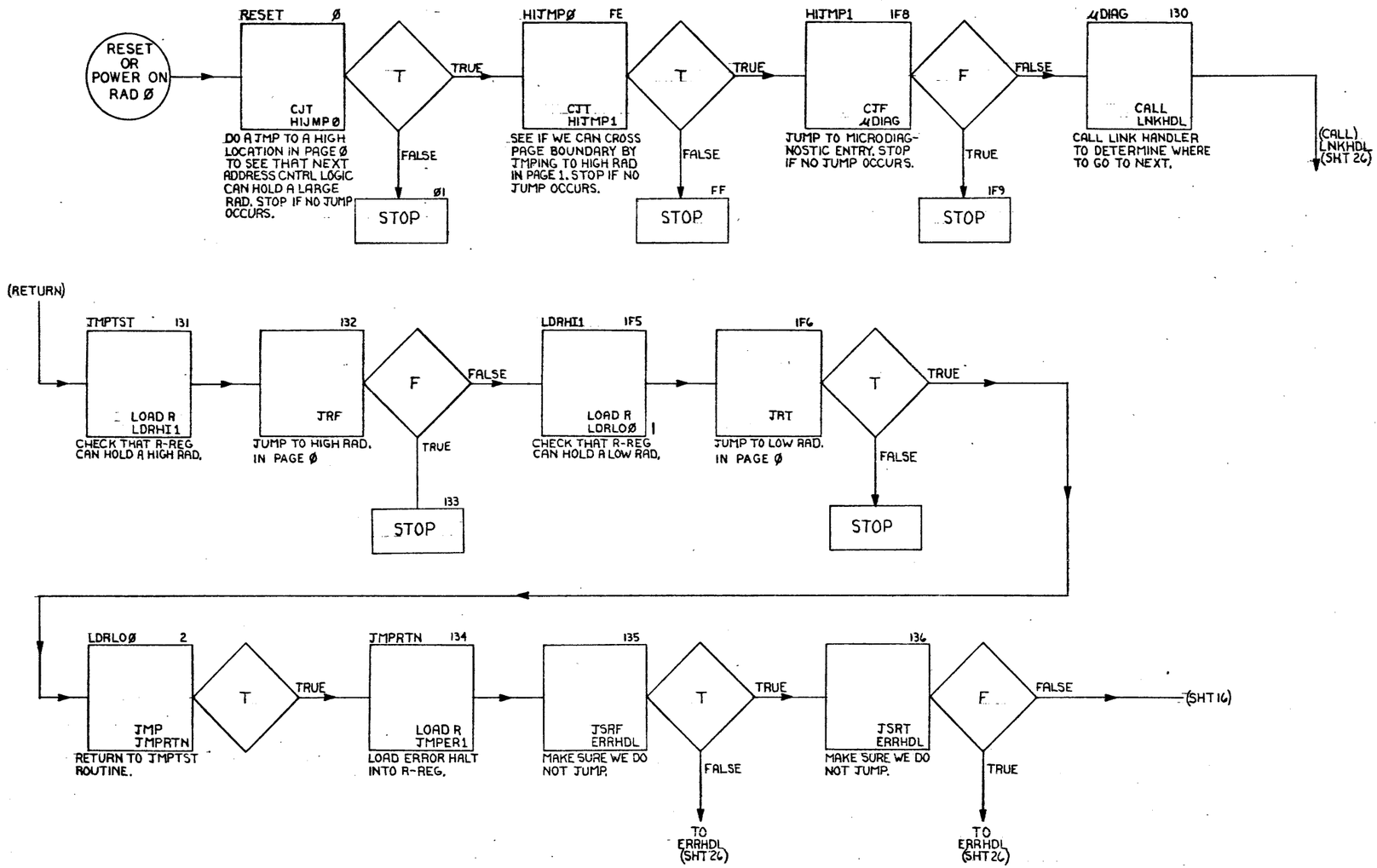
Bedford, Massachusetts 01730

SCALE: NONE — DWG NO. E015 — SHEET of 27 SHEETS



DS2IE015
E

MICRODIAGNOSTIC ENTRY
NEXT ADDRESS CONTROL
LOGIC TEST

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL
FINISH

PART NUMBER	NEXT ASSEMBLY	QTY

DRN D.DAVIDSON 3-78
CHK
ENGR
PROJ
MFG

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

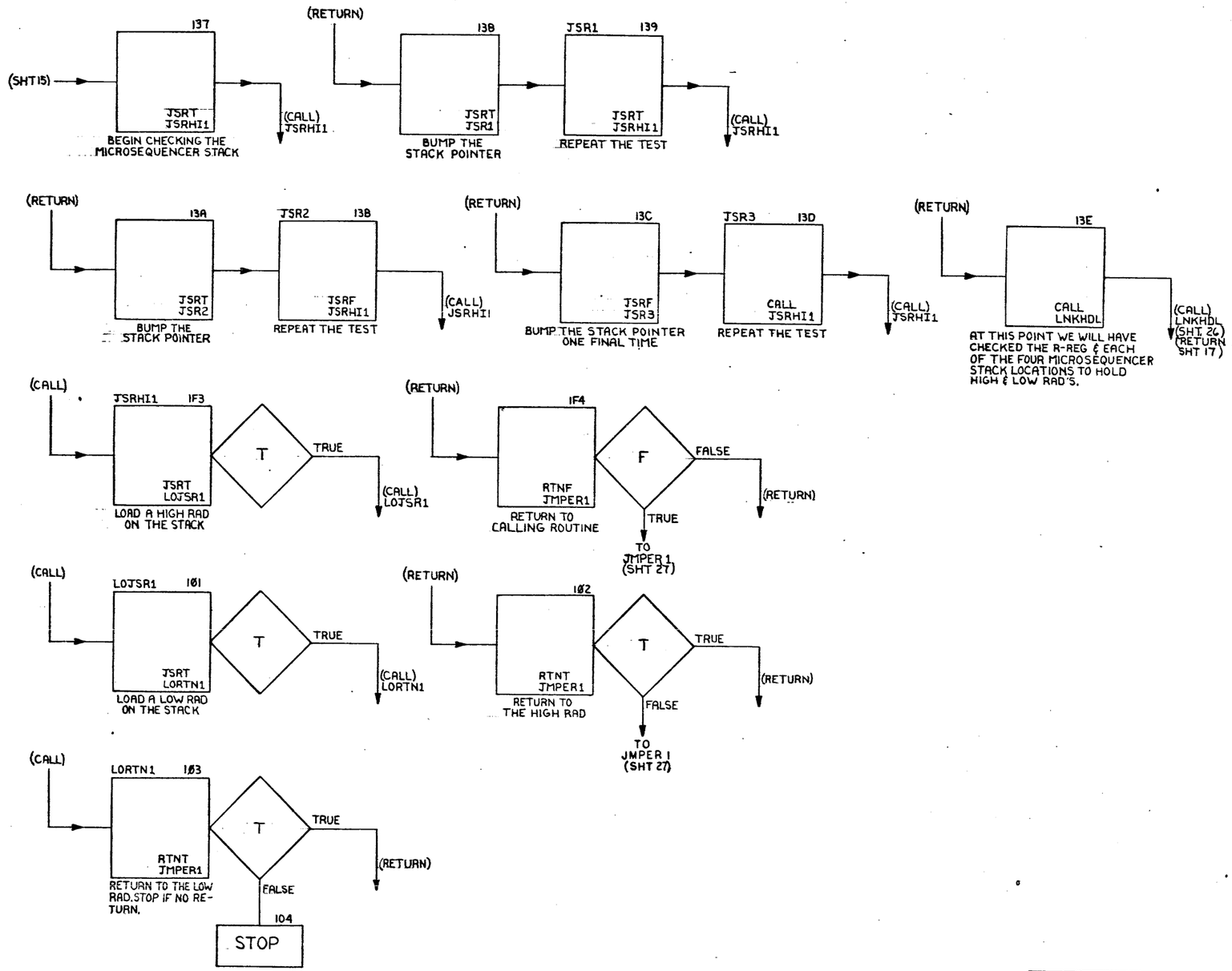
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE FLOW CHARTS
CVP MICROPROGRAM

SCALE NONE
DWG NO. DS2IE015
UNIT WT.
SHEET 15 OF 27 SHEETS



DS21E015
E

NEXT ADDRESS CONTROL LOGIC TEST

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

BRN D.DAVIDSON 3-78
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: FLOW CHARTS CVP MICROPROGRAM

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

SCALE: NONE
DWG NO. DS21E015
UNIT WT.
SHEET 16 OF 27 SHEETS

THIS SUBTEST CHECKS THE AZERO TEST CONDITION AND SOME BASIC ALU FUNCTIONS & DATA PATHS.

(RETURN)

AZRTST 13F
LOAD R ALUER1
LOAD R WITH ERROR HALT ADDRESS.

-1 TO BØ
ALU→I
JSRT ERRHDL
INIT BØ & IBUF AND CHECK AZRO ON A NON-ZERO ALU CONDITION.

AZRO
FALSE
TRUE
TO ERRHDL (SHT 26)

CLR BØ
ALU→I
JSRF ERRHDL
CLEAR BØ & IBUF AND CHECK AZRO FOR A ZERO ALU OUTPUT CONDITION. WE NOW HAVE SOME CONFIDENCE THAT AZRO CONDITION WORKS. A MORE EXTENSIVE TEST WILL BE DONE LATER, ON AZRO.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

THE FOLLOWING SERIES OF TESTS CHECKOUT THE DATA PATH FROM THE ALU TO THE IBUF THRU THE INTERNAL BUS FOR BIT PICK-UPS AND DROPS. B-PORT LOADS ARE ALSO TESTED. ALSO SOME BASIC ALU FUNCTIONS, INVERT, NEGATE (2'S COMPLIMENT), INCREMENT AND DECREMENT ARE TESTED.

DATA1 142
IBUF→Q (IBUF=Ø)
ALU→IBUF
JSRF ERRHDL
CHECK DATA PATH FROM IBUF TO ALU OUT WITH ALL ZEROES. BRANCH IF ERROR.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

BØ+1→BØ (BØ=1)
ALU→IBUF
JSRT ERRHDL
CHECK INCREMENT INSTRUCTIONS WITH NO CARRY. BRANCH IF ALU OUT=Ø; ERROR.

AZRO
FALSE
TRUE
TO ERRHDL (SHT 26)

NEGTS1 144
-BØ→BØ (BØ=-1)
ALU→I
JSRT ERRHDL
CHECK NEGATE INSTRUCTIONS FOR BITS STUCK AT "Ø," BRANCH IF RESULT IS ZERO; ERROR.

AZRO
TO ERRHDL (SHT 26)

BØ+1→BØ (BØ=Ø)
ALU→I
JSRF ERRHDL
CHECK INCREMENT INSTRUCTIONS WITH ALL CARRIES. BRANCH IF ALU OUT ≠Ø; ERROR.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

NEGTST2 146
-BØ→BØ (BØ=Ø)
ALU→I
JSRF ERRHDL
CHECK NEGATE INSTRUCTIONS FOR BITS STUCK AT "1." BRANCH IF RESULT IS ≠ZERO; ERROR.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

DATA2 147
-1→BØ
ALU→I
JSRT ERRHDL
INIT IBUF WITH ALL "1S."

AZRO
FALSE
TRUE
TO ERRHDL (SHT 26)

IBUF+1→Q (Q=Ø)
ALU→I
JSRF ERRHDL
CHECK DATA PATH FROM IBUF TO ALU OUT WITH ALL "1'S." INCR DATA & BRANCH IF ≠Ø; ERROR.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

DECTS1 149
B-1→BØ (BØ=-2)
ALU→I
JSRT ERRHDL
CHECK DECREMENT INSTRUCTIONS WITH CARRIES, IE, 11111+11111=111110=-2 BRANCH IF =Ø; ERROR.

AZRO
FALSE
TRUE
TO ERRHDL (SHT 26)

NOT BØ→BØ (BØ=1)
ALU→I
JSRT ERRHDL
CHECK "1'S" COMPLIMENT INSTRUCTIONS, BRANCH IF RESULT = Ø; ERROR.

AZRO
FALSE
TRUE
TO ERRHDL (SHT 26)

DECTS2 148
BØ-1→BØ (BØ=Ø)
ALU→I
JSRF ERRHDL
CHECK DECREMENT INSTRUCTION WITH NO CARRY.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

14C
CALL LNKHDL

(CALL) LNKHDL (SHT 26) (RETURN SHT 18)

DS21E015
E

AZRO TEST
DATA PATH AND BASIC
ALU FUNCTION TEST

MATERIAL: —
FINISH: —
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

BRN D DAVIDSON 3-78
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

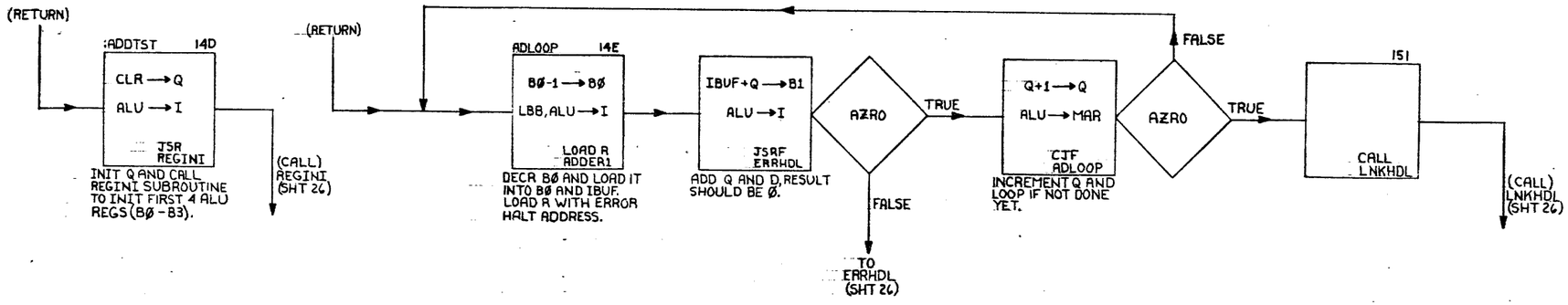
SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

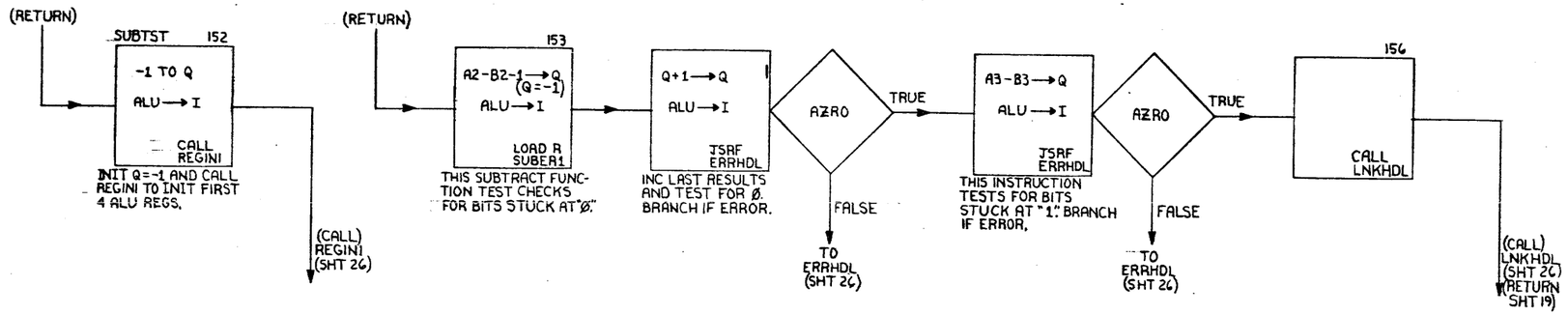
TITLE: FLOW CHARTS
CVP MICROPROGRAM

SCALE: NONE
DWG NO. DS21E015
UNIT WT. —
SHEET 17 OF 27 SHEETS

ROUTINE TO CHECK THE D+Q FUNCTION AND THE B-LATCH TO IBUF DATA PATH. AFTER RUNNING THIS TEST, WE WILL HAVE CONFIDENCE IN THE ARITHEMETIC ADD, IN AZRO CONDITION, AND IN THE ABILITY OF BØ AND Q TO HOLD ANY DATA PATTERN.



TEST TO CHECK THE ALU SUBTRACT FUNCTION.



DS21E015
E

ADD TEST
SUBTRACT TEST

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

BRND DAVIDSON 3-78
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ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

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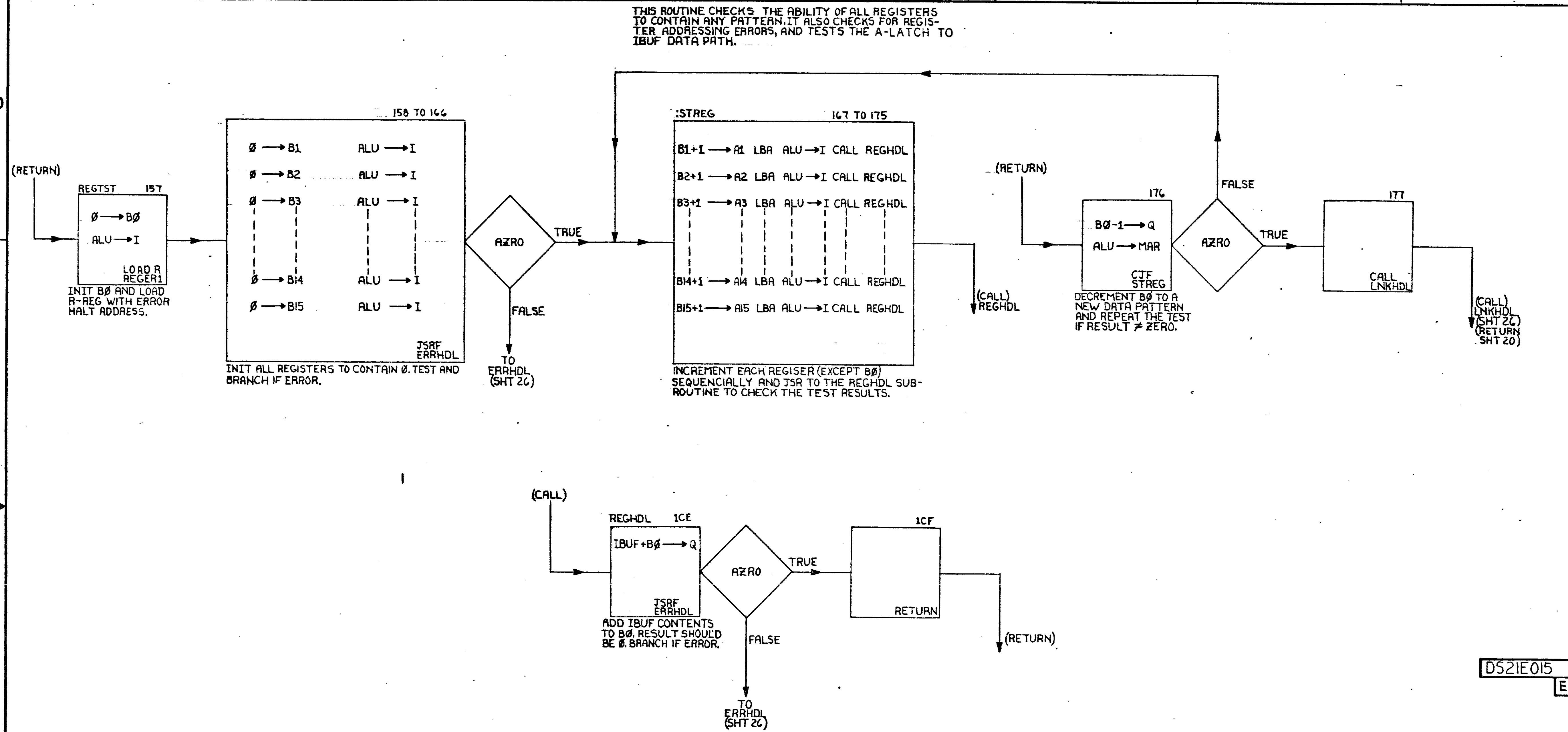
Bedford, Massachusetts 01730

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: FLOW CHARTS
CVP MICROPROGRAM

SCALE: NONE
DWG NO.: DS21E015
UNIT WT.:
SHEET 18 OF 27 SHEETS



DS21E015 E

ALU INTERNAL REGISTER TEST

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TOLERANCES: DECIMAL .XX = ±.01, .XXX = ±.005, .XXXX = ±.0010, FRACTIONAL = ±1/64, ANGULAR = ±1°00'

DRN D. DAVIDSON 3-78

SEE SHEET 1

TITLE: FLOW CHARTS CVP MICROPROGRAM

SCALE: NONE

DWG NO. DS21E015

SHEET 19 OF 27 SHEETS

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THE FOLLOWING TESTS CHECK THE LOGICAL FUNCTIONS OF THE ALU.

(RETURN)

LOGIC 178

-1 TO Q

ALU → I

CALL REGINI

INIT Q AND THE FIRST 4 ALU REGISTERS.

(CALL) REGINI (SHT 2C)

(RETURN)

ORTST 179

A2 V B3 → Q

ALU → I

LOAD R LOGER1

CHECK FOR BITS STUCK AT "Ø." LOAD R WITH ERROR HALT LOCATION.

Q+1 → Q

ALU → I

JSRF ERRHDL

INCREMENT PREVIOUS RESULT TO SEE IF IT WAS -1. BRANCH IF ERROR.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 2C)

AØ V BØ → Q

ALU → I

JSRF ERRHDL

CHECK FOR BITS STUCK AT "1" BY ORING Ø WITH ITSELF.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 2C)

XORTST 17C

A1 ⊻ B1 → Q

ALU → I

JSRF ERRHDL

XOR ALL 1'S WITH ITSELF TO CHECK FOR BITS STUCK AT "1." RESULT SHOULD = Ø. BRANCH IF ERROR.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 2C)

A2 ⊻ B3 → Q

ALU → I

XOR "125" & "252 PATTERN TO CHECK FOR BITS STUCK AT "Ø." RESULT SHOULD = -1.

AZRO

FALSE

TRUE

TO ERRHDL (SHT 2C)

Q+1 → Q

ALU → I

JSRF ERRHDL

INCREMENT Q TO CHECK THAT LAST RESULT YIELDED THE EPECTED DATA. BRANCH IF ERROR.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 2C)

ANDTST 17F

A2 ∧ B3 → Q

ALU → I

JSRF ERRHDL

AND "125" & "252" PATTERN = Ø, CHECKS FOR BITS STUCK AT "1." BRANCH IF ERROR.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 2C)

A1 ∧ B1 → Q

ALU → I

JSRT ERRHDL

AND ALL 1'S WITH ITSELF TO GET -1. THIS CHECKS FOR BITS STUCK AT Ø.

AZRO

FALSE

TRUE

TO ERRHDL (SHT 2C)

Q+1 → Q

ALU → I

JSRF ERRHDL

INCREMENT PREVIOUS RESULT TO SEE IF IT WAS -1. BRANCH IF ERROR.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 2C)

182

CALL LNKHDL

(CALL) LNKHDL (SHT 2C) (RETURN SHT 21)

DS21E015

E

LOGICAL ALU FUNCTION TEST

TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 .XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± Ø0'

DRN D.DAVIDSON 3-78

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ENGR

PROJ

MFG

SIGNATURE DATE

UNIT WT.

MATERIAL

FINISH

PART NUMBER | NEXT ASSEMBLY | QTY

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE FLOW CHARTS CVP MICROPROGRAM

SCALE NONE

DWG NO. DS21E015

SHEET 20 OF 27 SHEETS

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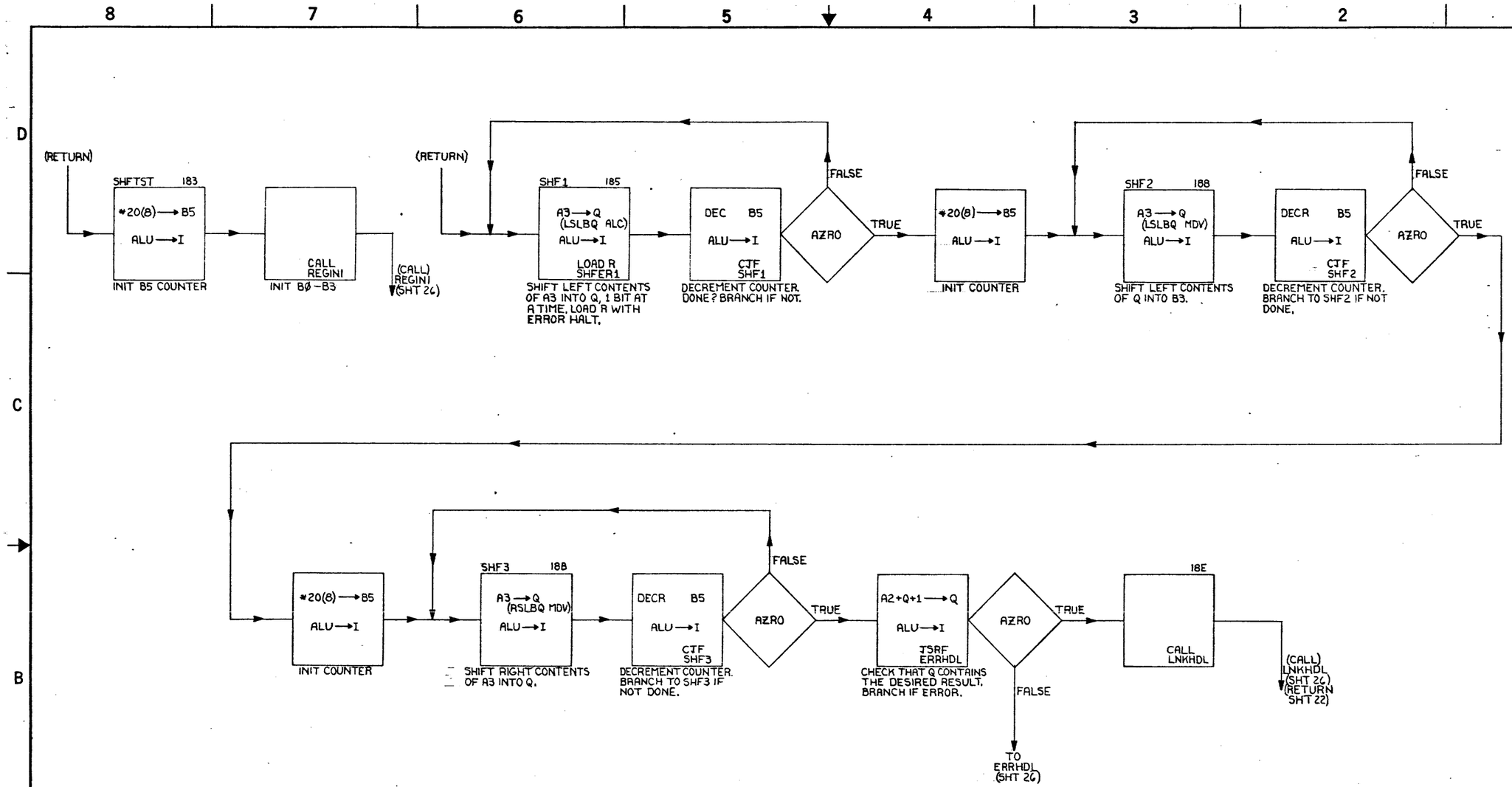

DS21E015
E

SHIFT TEST

TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

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CHK
ENGR
PROJ

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE FLOW CHARTS CVP MICROPROGRAM

SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 21 OF 27 SHEETS

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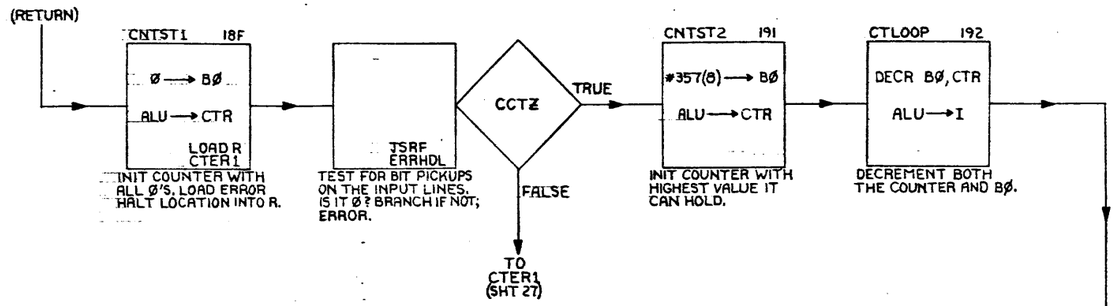
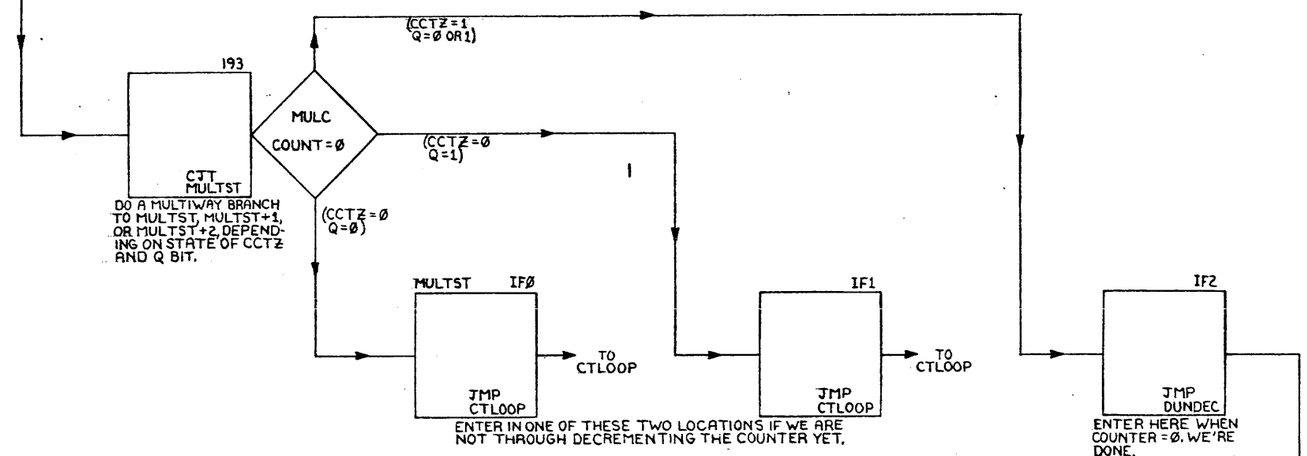
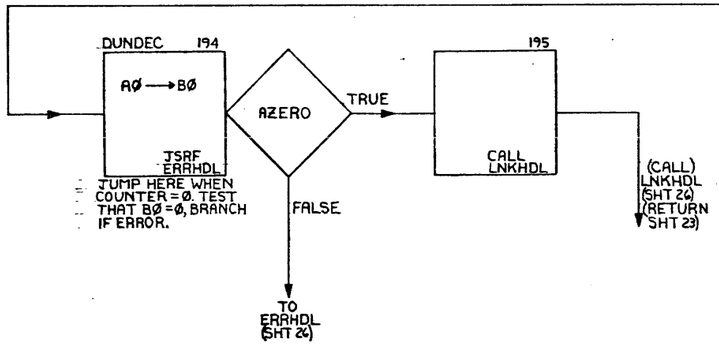
THIS SUBTEST INSURES THE INTEGRITY OF THE CPU COUNTER.







DS21E015
E

CPU COUNTER SUBTEST

TOLERANCES DECIMAL	
.XX	± .01
.XXX	± .005
.XXXX	± .0010
FRACTIONAL ± 1/64	
ANGULAR ± 1° 00'	

MATERIAL: *
FINISH: *

DRN	D.DAVIDSON	4-78	
CHK			
ENGR			
PROJ			
MFG			

PART NUMBER | NEXT ASSEMBLY | QTY

SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

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Bedford, Massachusetts 01730

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: FLOW CHARTS CVP MICROPROGRAM

SCALE: NONE
DWG NO. DS21E015
UNIT WT. *
SHEET 22 OF 27 SHEETS

TEST TO CHECK THE MEM/DATABUS "Ø" STATE, CHECK THE IR BITS Ø-7, AND CHECK THE "C" AND "CSAVE" TEST CONDITIONS.

(RETURN)

MISTST 19G

MEMBUS → I

LOAD R MISER 1

IBUF → Q

JSRF ERRHDL

AZERO — TRUE

FALSE → TO ERRHDL (SHT 24)

DATABUS → I

IBUF → Q

JSRF ERRHDL

AZERO — TRUE

FALSE → TO ERRHDL (SHT 24)

IRTST1 19A

#3Ø(8) → Q

ALU → I

19B

SWPI D → Q

ALU → I, IR

CALL REGINI

REGINI, 5H26

LOAD IR TO CHOOSE AØ AS THE SOURCE REGISTER, B3 AS THE DESTINATION REGISTER, AND TO FORCE IRØ FALSE.

RETURN ICD, SH26

19C

ACS → BACD (AØ → B3)

JSRT ERRHDL

TRANSFER CONTENTS OF AØ TO B3, TEST IRØ CONDITION, BRANCH IF TRUE; ERROR.

IRØ — FALSE

TRUE → TO ERRHDL (SHT 24)

-1 → BØ

INIT BØ TO PREPARE FOR NEXT TRANSFER.

#140(8) → Q

ALU → I

LOAD IR TO CHOOSE A3 AS THE SOURCE REGISTER, BØ AS THE DESTINATION REGISTER, AND TO FORCE IR5 FALSE TEST CONDITION.

SWPI D → R

ALU → I, IR

1AØ

ACS → BACD (A3 → BØ)

JSRT ERRHDL

TRANSFER CONTENTS OF A3 TO BØ. TEST IR5 CONDITION, BRANCH IF TRUE; ERROR.

IR5 — FALSE

TRUE → TO ERRHDL (SHT 24)

BØ → Q

JSRF ERRHDL

TEST BØ = Ø. BRANCH IF NOT; ERROR.

AZERO — TRUE

FALSE → TO ERRHDL (SHT 24)

#26Ø(8) → Q

ALU → I

SET A-SOURC = A1, B-DESTINATION = B2, FORCE IRØ = TRUE.

1A3

SWPI D → Q

ALU → I, IR

1A4

ACS → BACD (A1 → B2)

JSRF ERRHDL

TRANSFER CONTENTS OF A1 TO B2. TEST IRØ TRUE, BRANCH IF ERROR.

IRØ — TRUE

FALSE → TO ERRHDL (SHT 24)

Ø → B1

ALU → I

INIT B1 TO PREPARE FOR NEXT TRANSFER.

#114(8) → Q

ALU → I

TOSTAT

SWPI D → R

ALU → I, IR

JSRT ERRHDL

SET A-SOURCE = A2, B-DESTINATION = B1, FORCE IR5 = TRUE, AND FORCE "C" FALSE TEST CONDITION, TEST "C" AND BRANCH IF ERROR.

C — FALSE

TRUE → TO ERRHDL (SHT 24)

ACS → BACD (A2 → B1)

ALU → I

JSRF ERRHDL

TRANSFER CONTENTS OF A2 TO B1. TEST IR5 TRUE, BRANCH IF ERROR.

IR5 — TRUE

FALSE → TO ERRHDL (SHT 24)

1A9

B1+1 → Q

ALU → I, IR

JSRF ERRHDL

TEST B1 FOR EXPECTED CONTENTS. BRANCH IF ERROR. THIS ALSO INITS IR FOR THE NEXT PART OF THIS TEST.

AZERO — TRUE → TO IRTST2 (SHT 24)

FALSE → TO ERRHDL (SHT 24)

DS21E015

E

MISCELLANEOUS TESTS

TOLERANCES DECIMAL .XX ± .01, .XXX ± .005, .XXXX ± .0010, FRACTIONAL ± 1/64, ANGULAR ± 0° 30'

MATERIAL

FINISH

PART NUMBER | NEXT ASSEMBLY | QTY

DRN D. DAVIDSON 4-78

CHK

ENGR

PROJ

MFG

SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
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Bedford, Massachusetts 01730

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

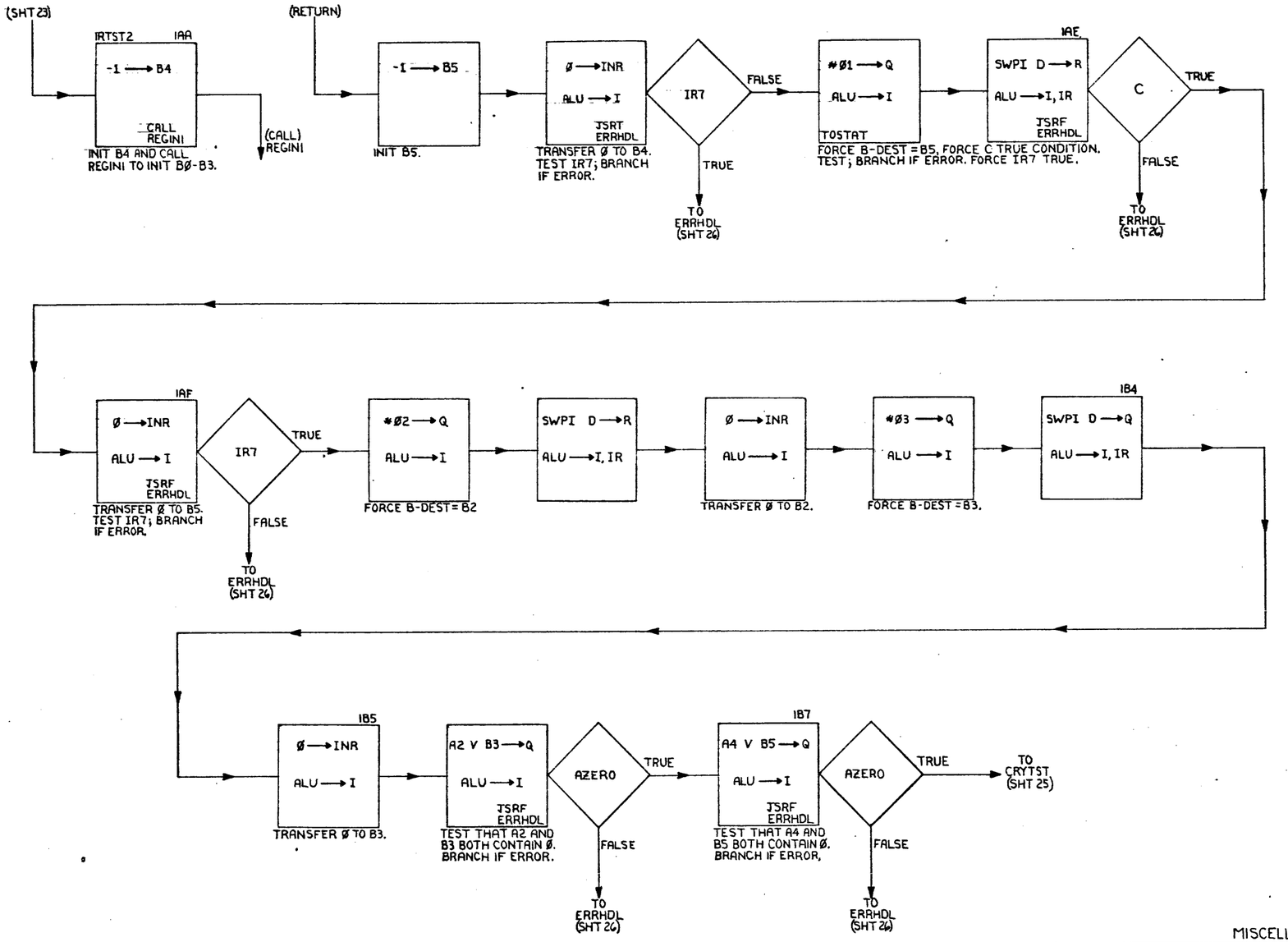
TITLE: FLOW CHARTS CVP MICROPROGRAM

SCALE: NONE

DWG NO. DS21E015

UNIT WT.

SHEET 23 OF 27 SHEETS



DS21E015
E

MISCELLANEOUS TESTS

TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

DRN D.DAVIDSON 5-78
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

PART NUMBER	NEXT ASSEMBLY	QTY

MATERIAL
FINISH

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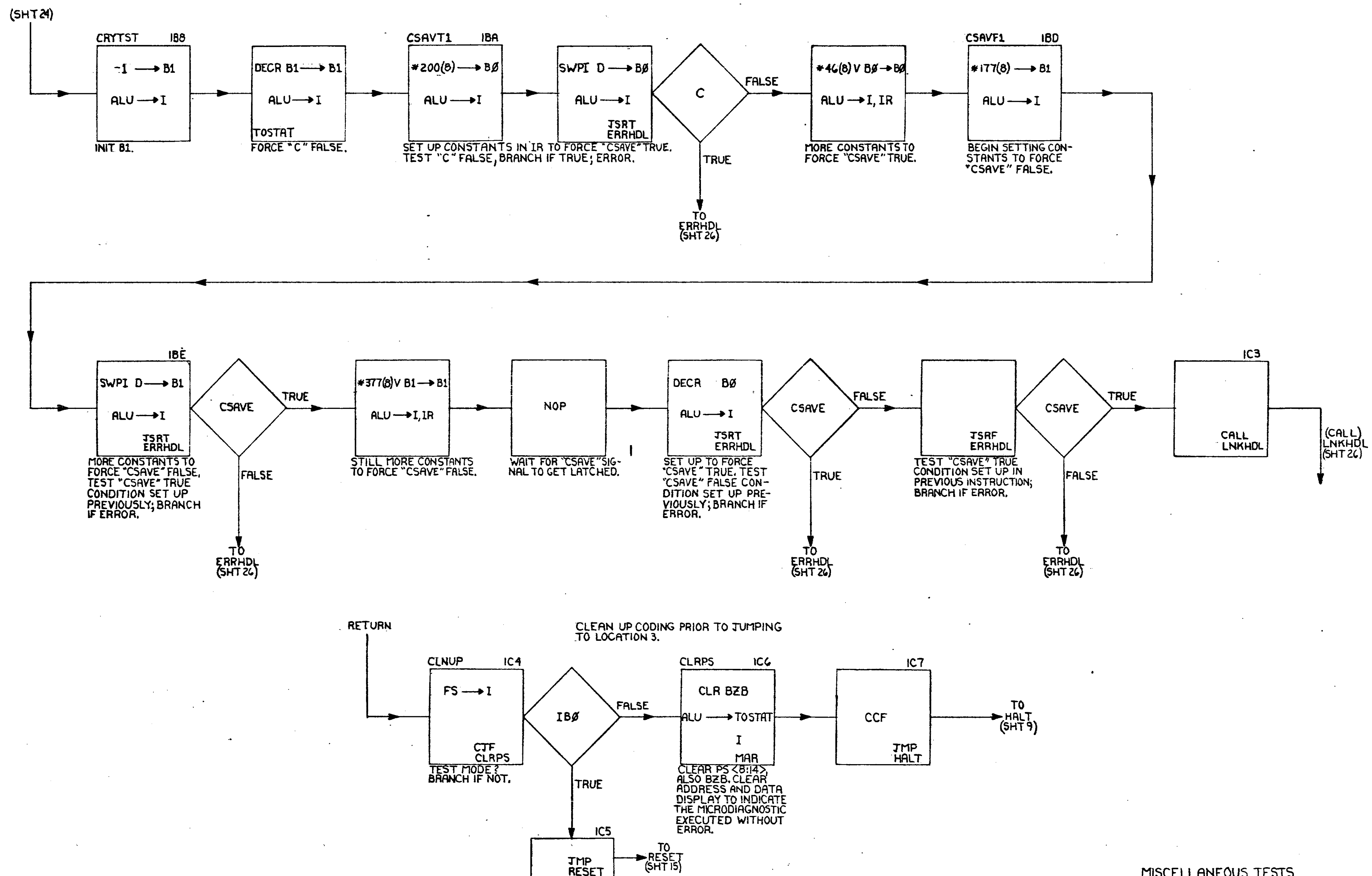
Bedford, Massachusetts 01730

TITLE FLOW CHARTS
CVP MICROPROGRAM

SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 24 OF 27 SHEETS



DS21E015
E

MISCELLANEOUS TESTS
CLEAN UP CODING

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TOLERANCES	DECIMAL .XX ±.01, .XXX ±.005, .XXXX ±.0010, FRACTIONAL ± 1/64, ANGULAR ± 1°00'
DRN	D. DAVIDSON 5-78
SYM / REVISION DESCRIPTION / APPD / DATE	SEE SHEET 1
TITLE	FLOW CHARTS CVP MICROPROGRAM
SCALE	NONE
DWG NO.	DS21E015
SHEET	25 OF 27 SHEETS

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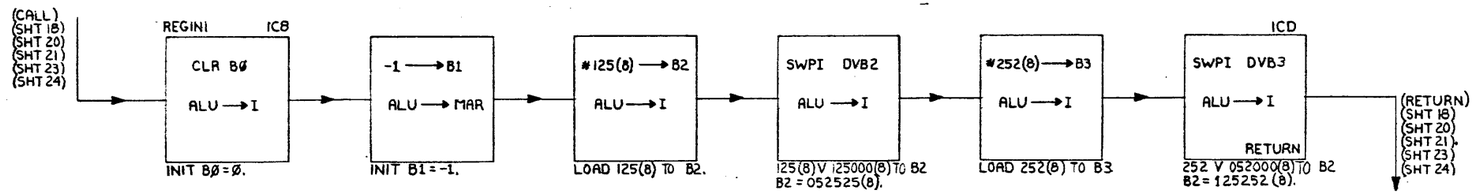
Bedford, Massachusetts 01730

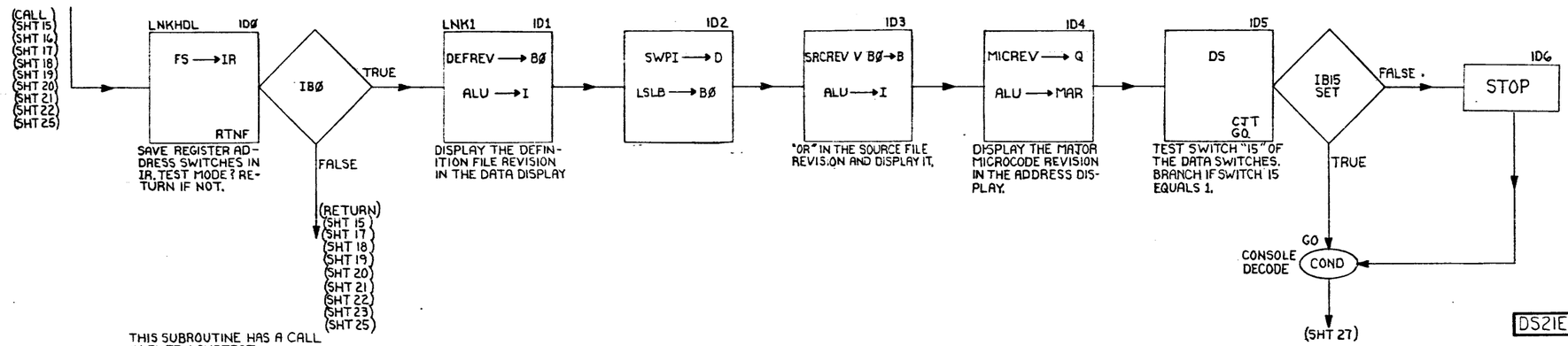
REMOVE ALL BURRS AND SHARP EDGES

DIAGNOSTIC SUBROUTINES

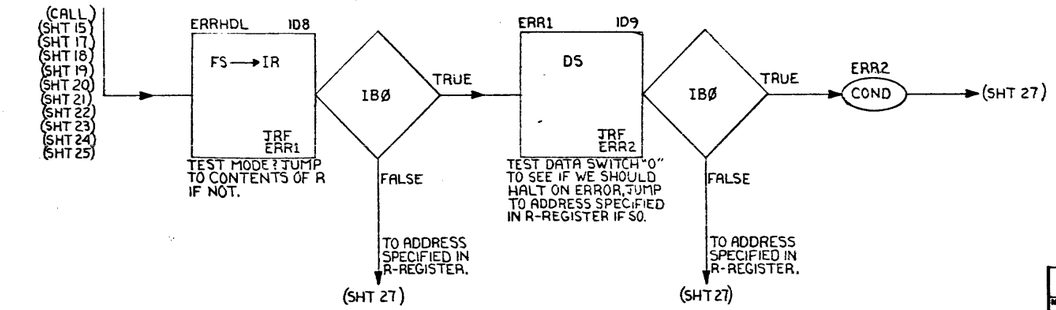
SUBROUTINE TO INITIALIZE ALU REGISTERS BØ THRU B3.



THIS SUBROUTINE HAS A CALL AT THE END OF EVERY SUBTEST.



THIS SUBROUTINE HAS A CALL IN EVERY SUBTEST.



DS21E015

E

DIAGNOSTIC SUBROUTINE

TOLERANCES UNLESS DECIMAL .XX ± .01, .XXX ± .005, .XXXX ± .0010, FRACTIONAL ± 1/64, ANGULAR ± 1°00'

MATERIAL

FINISH

PART NUMBER | NEXT ASSEMBLY | QTY

DRN D.DAVIDSON 5 78

CHK

ENGR

PROJ

MFG

SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE FLOW CHARTS CVP MICROPROGRAM

SCALE NONE

DWG NO. DS21E015

WT.

SHEET 26 OF 27 SHEETS

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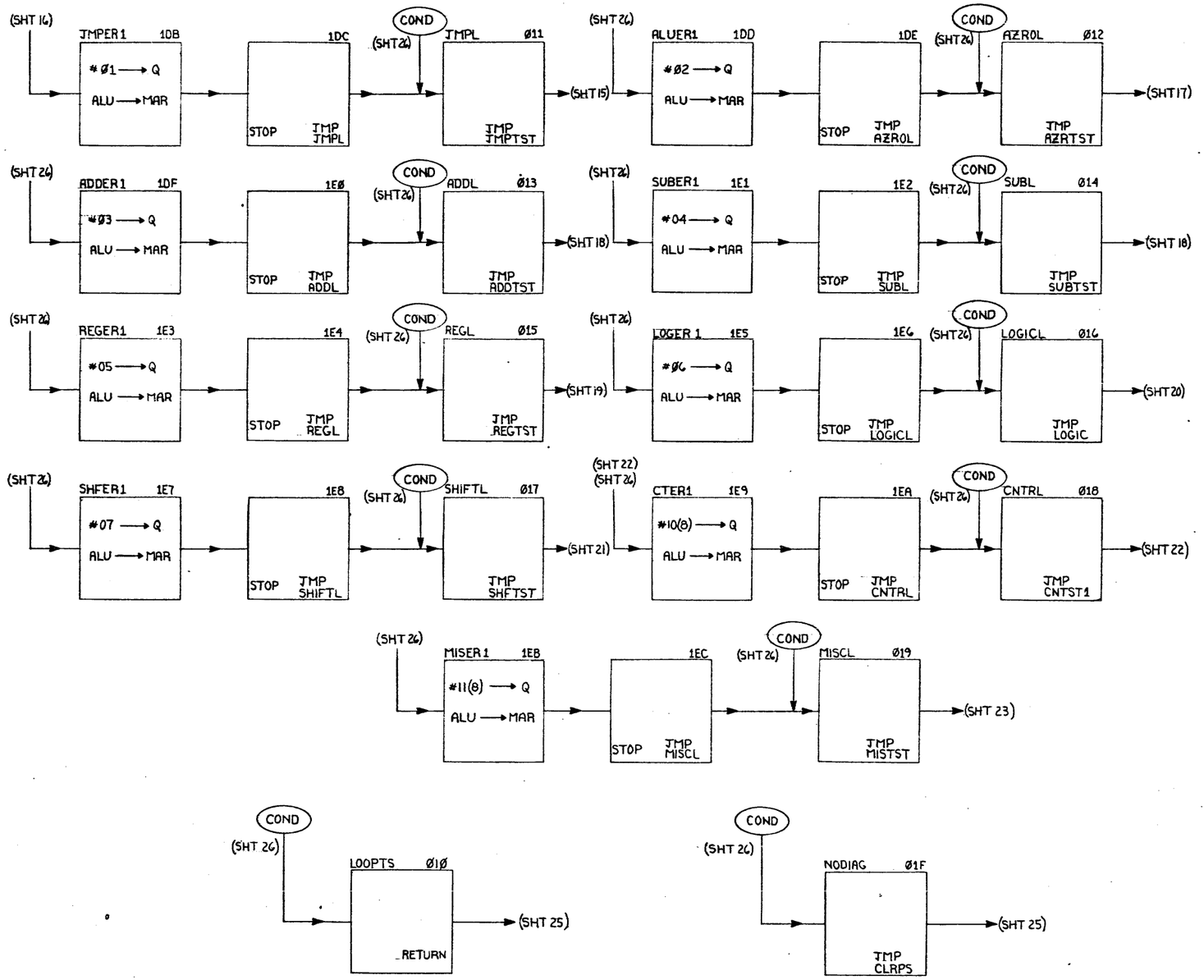
Bedford, Massachusetts 01730



DS21E015
E

ERROR HALTS AND COND LINKS

TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 .XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 1°00'

MATERIAL

FINISH

PART NUMBER | NEXT ASSEMBLY | QTY

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

DRN D.DAVIDSON 5/8

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

TITLE FLOW CHARTS CVP MICROPROGRAM

SCALE NONE

DWG NO. DS21E015

UNIT WT.

SHEET 27 OF 27 SHEETS

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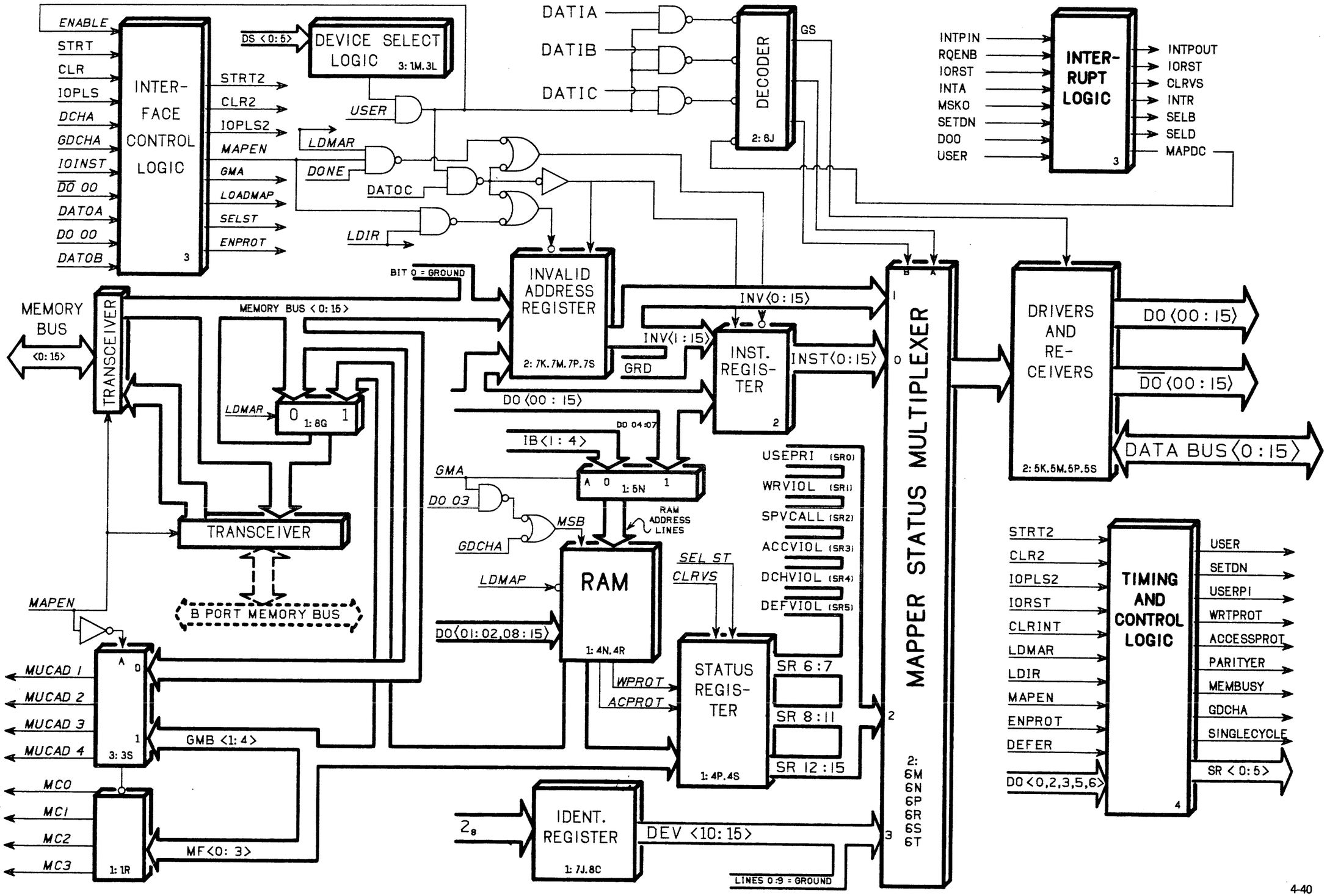
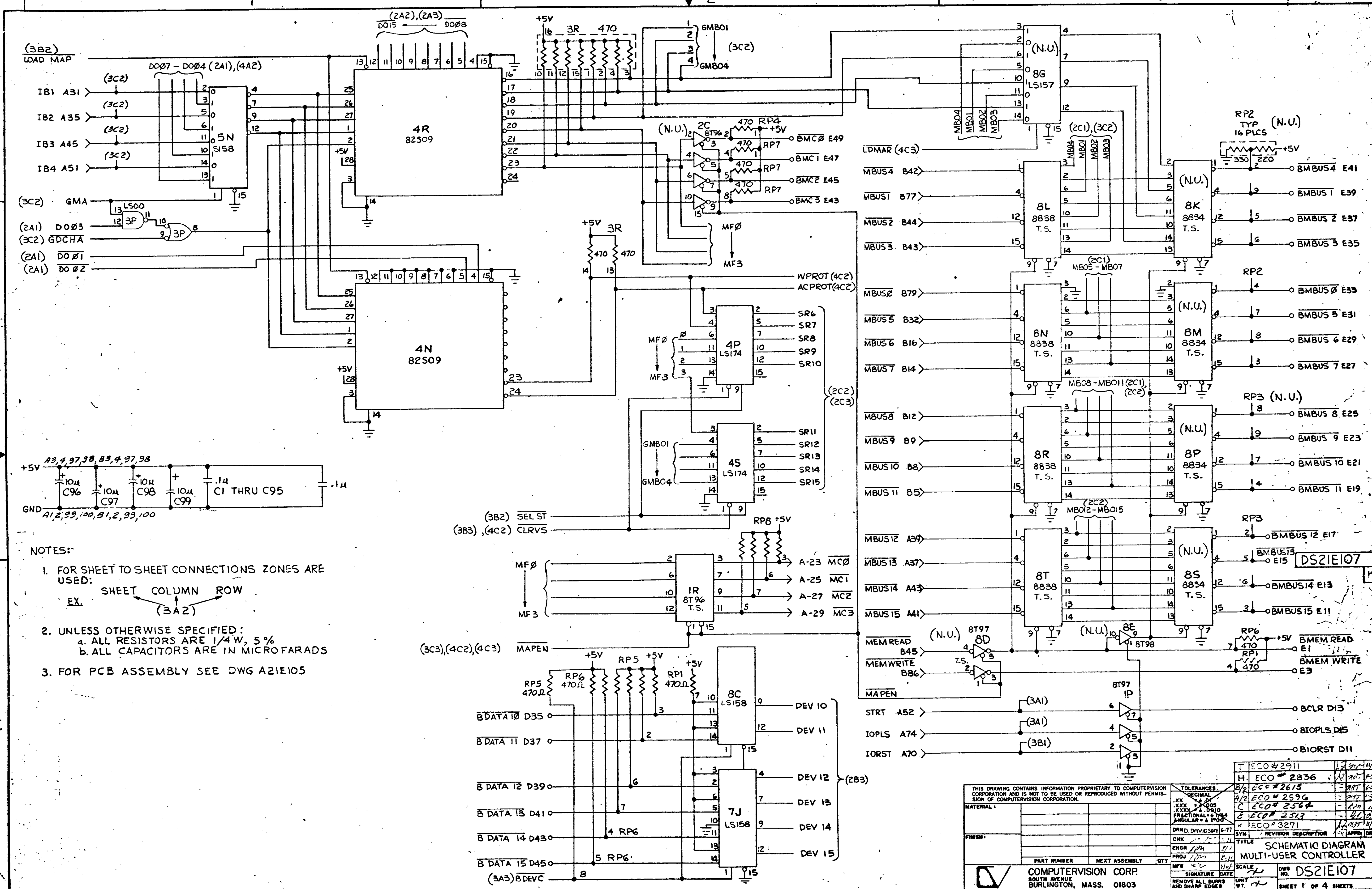
Memory Management and Protection Unit


ENABLE
STRT
CLR
IOPLS
DCHA
GDCHA
IOINST
DO 00
DATOA
DO 00
DATOB
INTER-FACE CONTROL LOGIC
3
DS <0:5>
DEVICE SELECT LOGIC
3: 1M.3L
STRT2
CLR2
IOPLS2
MAPEN
GMA
LOADMAP
SELST
ENPROT
USER
LDMAR
DONE
DATOC
LDIR
DATIA
DATIB
DATIC
DECODER
2: 6J
GS
INTPIN
RQENB
IORST
INTA
MSKO
SETDN
DOO
USER
INTER-RUPT LOGIC
3
INTPOUT
IORST
CLRVS
INTR
SELB
SELD
MAPDC
BIT 0 = GROUND
INVALID ADDRESS REGISTER
2: 7K.7M.7P.7S
INV<0:15>
INV<1:15>
GRD
INST. REGIS-TER
2
INST<0:15>
MEMORY BUS
<0:15>
TRANSCEIVER
MEMORY BUS <0:15>
DO <00:15>
DO 04:07
IB<1:4>
LDMAR
0 1
1: 8G
TRANSCEIVER
B PORT MEMORY BUS
GMA
DO 03
MSB
GDCHA
A 0 1
1: 5N
RAM ADDRESS LINES
LDMAP
RAM
1: 4N.4R
DO<01:02,08:15>
SEL ST
CLRVS
WPROT
ACPROT
STATUS REGIS-TER
1: 4P.4S
USEPRI (SR0)
WRVIOL (SR1)
SPVCALL (SR2)
ACCVIOL (SR3)
DCHVIOL (SR4)
DEFVIOL (SR5)
SR 6:7
SR 8:11
SR 12:15
MAPEN
MUCAD 1
MUCAD 2
MUCAD 3
MUCAD 4
A 0
1
3: 3S
GMB <1:4>
MC0
MC1
MC2
MC3
1: 1R
MF<0:3>
2₈
IDENT. REGISTER
1: 7J.8C
DEV <10:15>
LINES 0:9 = GROUND
B
A
1
0
MULTIPLEXER
2
3
2: 6M 6N 6P 6R 6S 6T
MAPPER STATUS
DRIVERS AND RE-CEIVERS
2: 5K.5M.5P.5S
DO <00:15>
DO <00:15>
DATA BUS <0:15>
STRT2
CLR2
IOPLS2
IORST
CLRINT
LDMAR
LDIR
MAPEN
ENPROT
DEFER
DO <0,2,3,5,6>
TIMING AND CONTROL LOGIC
4
USER
SETDN
USERPI
WRTPROT
ACCESSPROT
PARITYER
MEMBUSY
GDCHA
SINGLECYCLE
SR <0:5>



NOTES:

1. FOR SHEET TO SHEET CONNECTIONS ZONES ARE USED:
   EX. SHEET COLUMN ROW (3A2)
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTORS ARE 1/4 W, 5%
   b. ALL CAPACITORS ARE IN MICROFARADS
3. FOR PCB ASSEMBLY SEE DWG A21E105

SYM	REVISION DESCRIPTION
J	ECO #2911
H	ECO # 2836
B/2	ECO #2615
A/2	ECO # 2596
C	ECO # 2564
B	ECO # 2513
	ECO # 3271

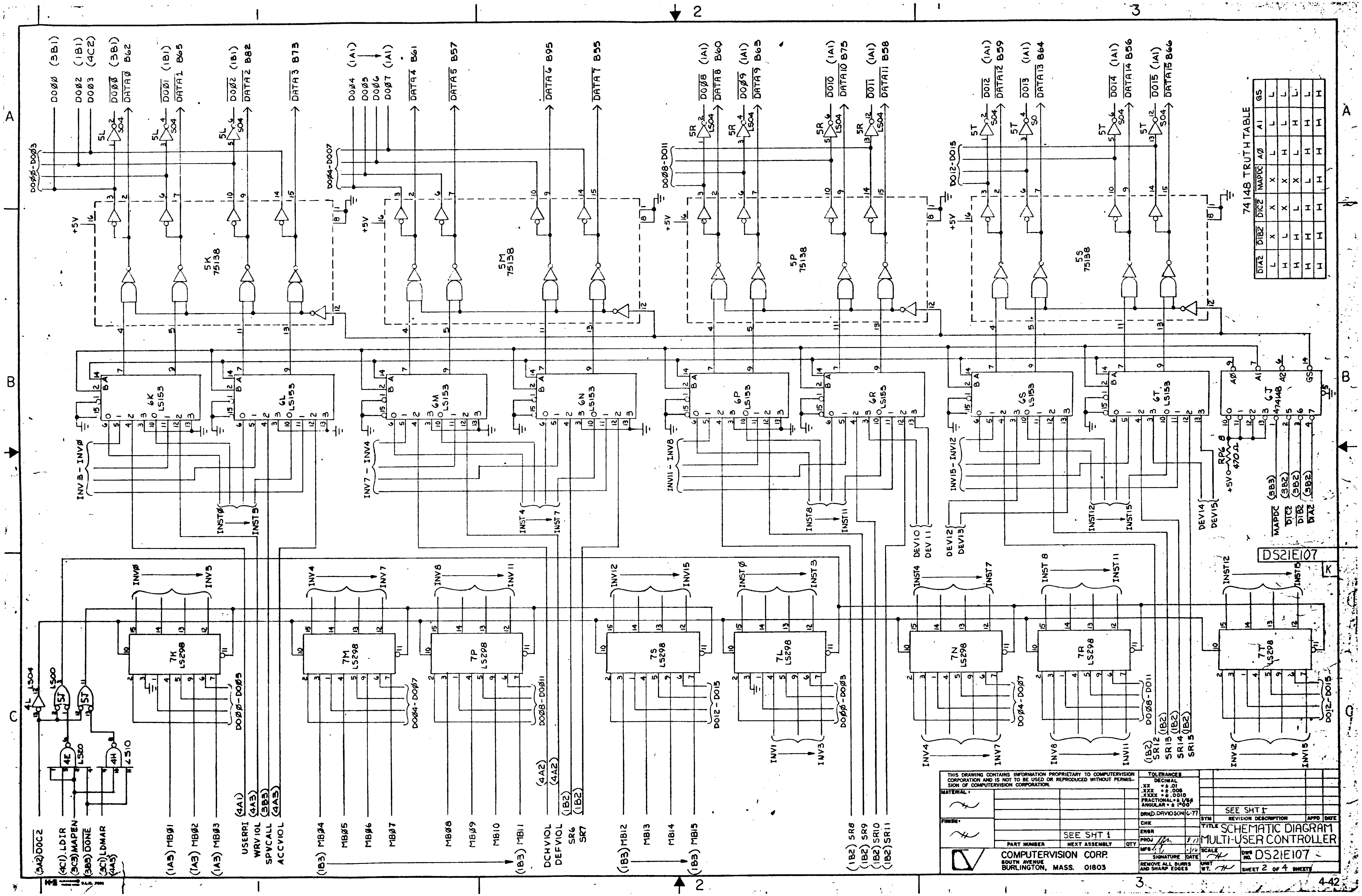
TITLE: SCHEMATIC DIAGRAM MULTI-USER CONTROLLER

DRN D. DAVIDSON 6-77

COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803

DWG NO. DS21E107

SHEET 1 OF 4 SHEETS


74148 TRUTH TABLE
DIA2 DIB2 DIC2 MAPDC A0 A1 GS
L X X X L L L
H L X X H L L
H H L X L H L
H H H L H H L
H H H H H H H
5K 75138
5M 75138
5P 75138
5S 75138
6K LS153
6L LS153
6M LS153
6N LS153
6P LS153
6R LS153
6S LS153
6T LS153
6J 74148
7K LS298
7M LS298
7P LS298
7S LS298
7L LS298
7N LS298
7R LS298
7T LS298
DATA0 B62
DATA1 B65
DATA2 B82
DATA3 B73
DATA4 B61
DATA5 B57
DATA6 B95
DATA7 B55
DATA8 B60
DATA9 B63
DATA10 B75
DATA11 B58
DATA12 B59
DATA13 B64
DATA14 B56
DATA15 B66
DOC2
LDIR
MAPEN
DONE
LDMAR
MB01 MB02 MB03 MB04 MB05 MB06 MB07 MB08 MB09 MB10 MB11 MB12 MB13 MB14 MB15
USERPI
WRVIOL
SPVCALL
ACCVIOL
DCHVIOL
DEFVIOL
SR6 SR7 SR8 SR9 SR10 SR11 SR12 SR13 SR14 SR15
MAPDC DIC2 DIB2 DIA2
DS21E107
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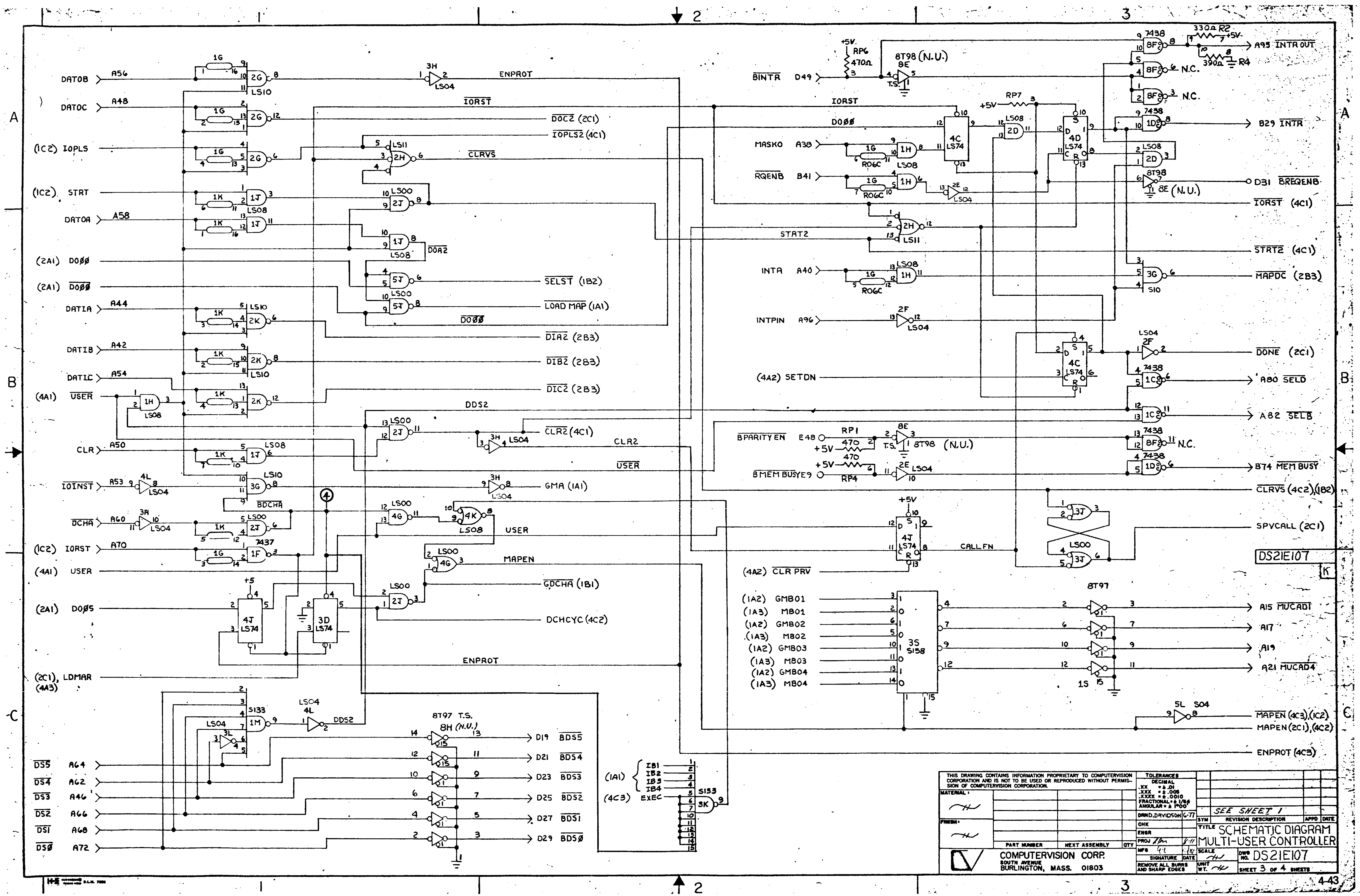
MATERIAL:
FINISH:
PART NUMBER
NEXT ASSEMBLY
QTY
SEE SHT 1
TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'
DRN D. DAVIDSON 6-77
CHK
ENGR
PROJ
MFG
SIGNATURE
DATE
REMOVE ALL BURRS AND SHARP EDGES
SEE SHT 1
SYM
REVISION DESCRIPTION
APPD
DATE
TITLE SCHEMATIC DIAGRAM MULTI-USER CONTROLLER
SCALE
UNIT WT.
DWG NO. DS21E107
SHEET 2 OF 4 SHEETS
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803



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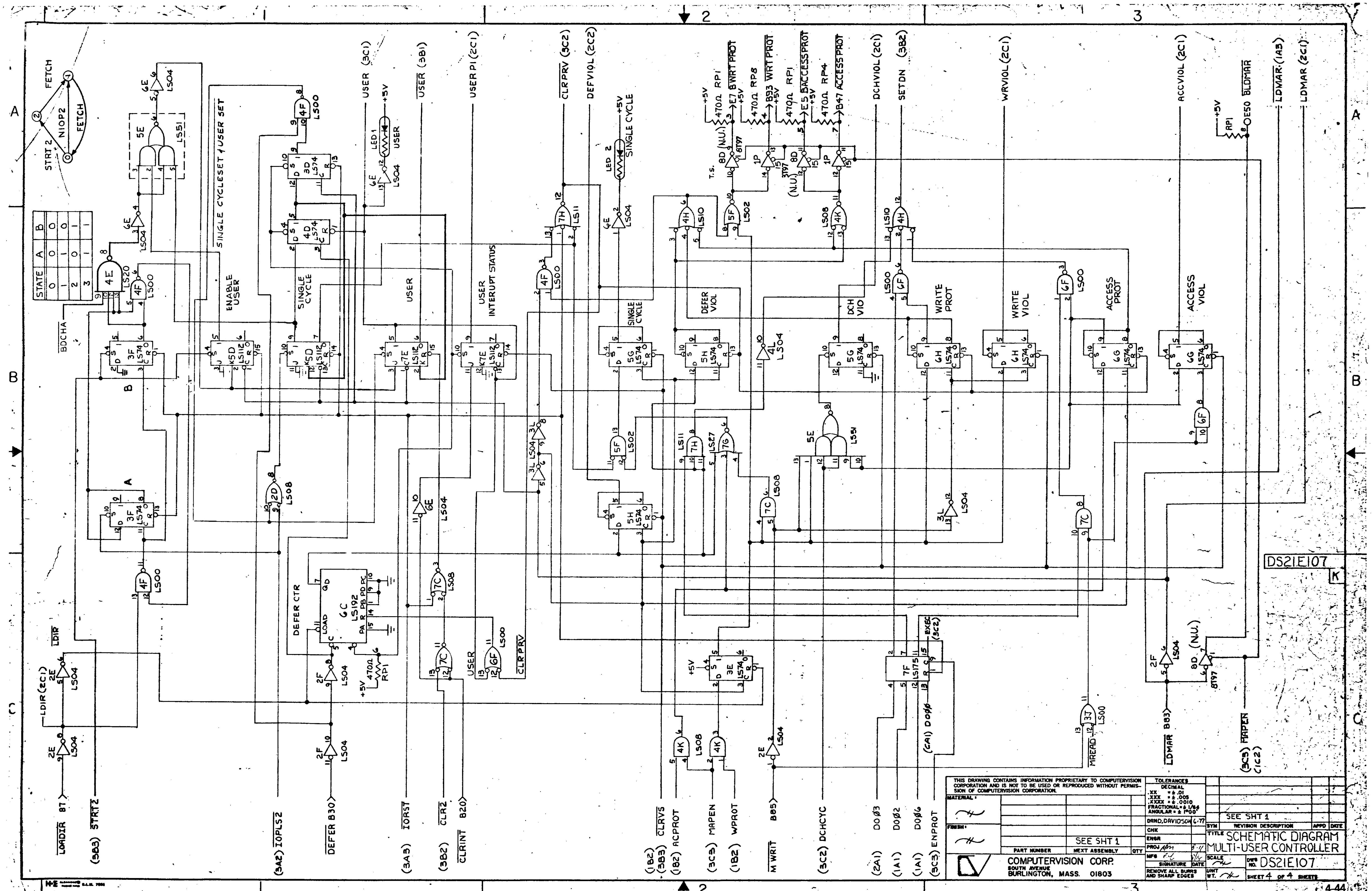
TOLERANCES
SEE SHEET 1
TITLE SCHEMATIC DIAGRAM MULTI-USER CONTROLLER
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
DWG NO. DS21E107
SHEET 3 OF 4 SHEETS
DS21E107
4-43



DS21E107

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TOLERANCES
DECIMAL
.XX = ±.01
.XXX = ±.005
.XXXX = ±.0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1/2°

SEE SHT 1

SEE SHT 1

PART NUMBER | NEXT ASSEMBLY | QTY

DRWN. DAVIDSON 6-77

TITLE SCHEMATIC DIAGRAM MULTI-USER CONTROLLER

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

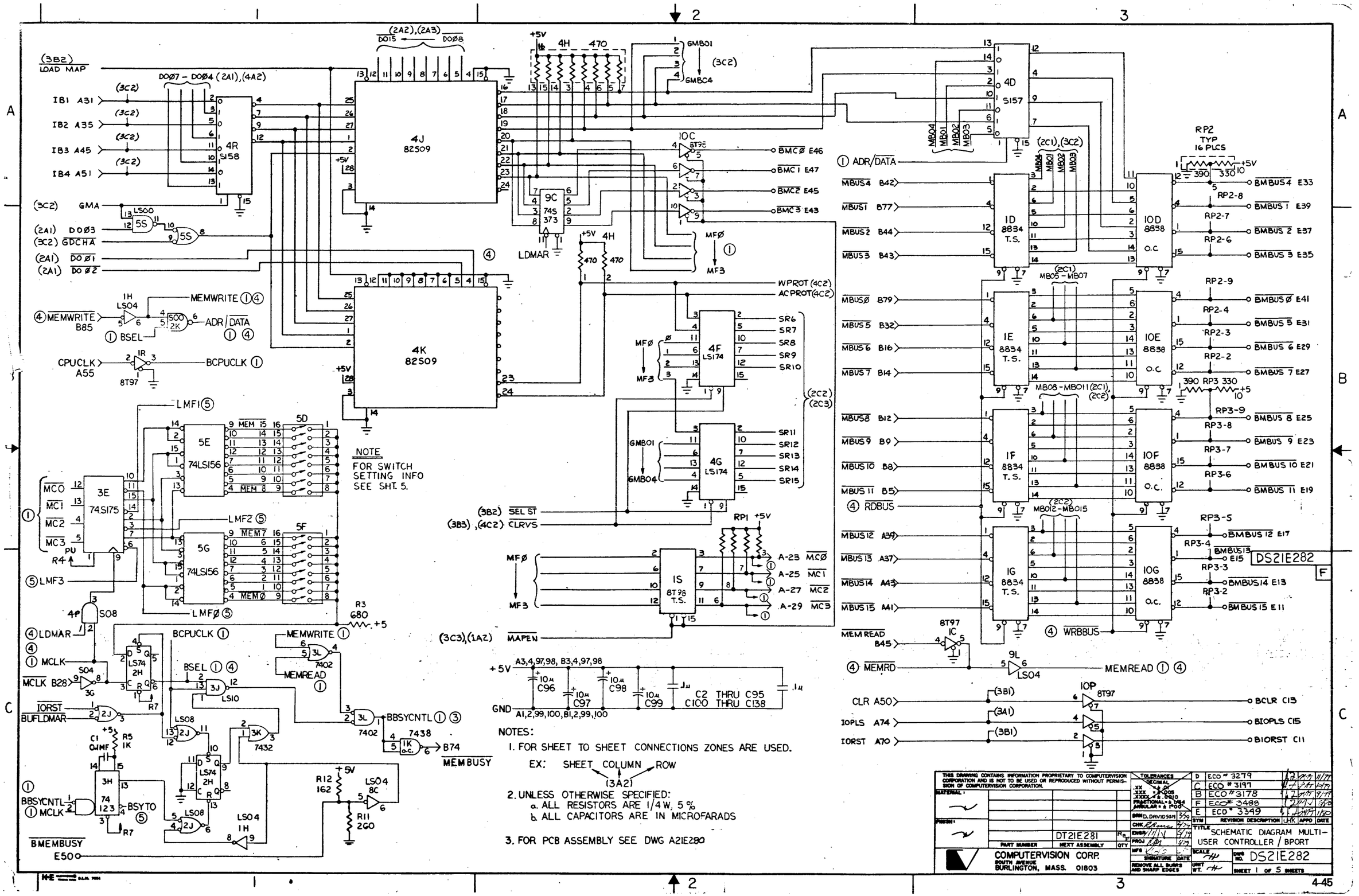
REMOVE ALL BURRS AND SHARP EDGES

DWG NO. DS21E107

SHEET 4 OF 4 SHEETS

4-44

B-Port Memory Managment and Protection Unit


(3B2) LOAD MAP
DØ07 - DØØ4 (2A1),(4A2)
(2A2),(2A3) DØ15 - DØØ8
IB1 A31
IB2 A35
IB3 A45
IB4 A51
4R SI58
4J 82S09
4K 82S09
9C 74S 373
LDMAR
4H 470
+5V
GMB01
GMB04
(3C2)
IOC 8T98
BMCØ E46
BMC1 E47
BMC2 E45
BMC3 E43
MFØ
MF3
4F LS174
4G LS174
WPROT (4C2)
ACPROT (4C2)
SR6
SR7
SR8
SR9
SR10
SR11
SR12
SR13
SR14
SR15
(2C2) (2C3)
GMA
DØØ3
GDCHA
DØØ1
DØØ2
LS00
5S
MEMWRITE ①④
ADR/DATA ① ④
MEMWRITE B85
BSEL ①
1H LS04
CPUCLK A55
BCPUCLK ①
8T97
LMF1 ⑤
LMF2 ⑤
LMF3 ⑤
LMFØ ⑤
5D
5E 74LS156
5F
5G 74LS156
3E 74S175
MC0
MC1
MC2
MC3
R4
R3 680
+5
4P S08
LDMAR ④
MCLK ①
MCLK B28
S04
LS74 2H
BSEL ① ④
3J LS10
MEMWRITE ①
3L 7402
MEMREAD ①
BBSYCNTL ① ③
7438
1K o.c.
B74
MEMBUSY
IORST
BUFLDMAR
2J
LS08
3K 7432
C1 .01MF
R5 1K
R7
3H 74123
BSYTO ⑤
BBSYCNTL ①
MCLK ①
R12 162
R11 260
LS04 8C
LS04 1H
E50
NOTE
FOR SWITCH SETTING INFO SEE SHT. 5.
RP1 +5V
IS 8T98 T.S.
A-23 MCØ
A-25 MC1
A-27 MC2
A-29 MC3
(3B3),(4C2) CLRVS
(3B2) SEL ST
(3C3),(1A2) MAPEN
+5V A3,4,97,98, B3,4,97,98
GND A1,2,99,100, B1,2,99,100
C96 10µ
C97 10µ
C98 10µ
C99 10µ
C2 THRU C95
C100 THRU C138 .1µ
4D S157
ADR/DATA ①
MBUS4 B42
MBUS1 B77
MBUS2 B44
MBUS3 B43
MBUSØ B79
MBUS5 B32
MBUS6 B16
MBUS7 B14
MBUS8 B12
MBUS9 B9
MBUS10 B8
MBUS11 B5
MBUS12 A39
MBUS13 A37
MBUS14 A43
MBUS15 A41
RDBUS ④
WRBBUS ④
MEMREAD B45
MEMRD ④
8T97 IC
9L LS04
MEMREAD ① ④
1D 8834 T.S.
IE 8834 T.S.
IF 8834 T.S.
IG 8834 T.S.
IOD 8838 O.C
IOE 8838 O.C.
IOF 8838 O.C.
IOG 8838 O.C.
(2C1),(3C2)
MB04 MB01 MB02 MB03
MB05 - MB07
MB08 - MB011 (2C1), (2C2)
MB012 - MB015 (2C2)
RP2 TYP 16 PLCS
390 330 +5V 10
BMBUS4 E33
BMBUS1 E39
BMBUS2 E37
BMBUS3 E35
RP2-8
RP2-7
RP2-6
RP2-9
RP2-4
RP2-3
RP2-2
BMBUSØ E41
BMBUS5 E31
BMBUS6 E29
BMBUS7 E27
390 RP3 330 +5 10
RP3-9
RP3-8
RP3-7
RP3-6
RP3-5
RP3-4
RP3-3
RP3-2
BMBUS8 E25
BMBUS9 E23
BMBUS10 E21
BMBUS11 E19
BMBUS12 E17
BMBUS13 E15
BMBUS14 E13
BMBUS15 E11
IOP 8T97
CLR A50
IOPLS A74
IORST A70
(3B1)
(3A1)
BCLR C13
BIOPLS C15
BIORST C11
DS21E282
F
NOTES:
1. FOR SHEET TO SHEET CONNECTIONS ZONES ARE USED.
EX: SHEET COLUMN ROW (3A2)
2. UNLESS OTHERWISE SPECIFIED:
a. ALL RESISTORS ARE 1/4 W, 5 %
b. ALL CAPACITORS ARE IN MICROFARADS
3. FOR PCB ASSEMBLY SEE DWG A21E280
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TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 .XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 2 MOS
MATERIAL
FINISH
PART NUMBER DT21E281
NEXT ASSEMBLY
QTY
D. DAVIDSON 3/74
CHK 4/74
ENGR 5/74
PROJ 6/74
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES
SCALE
UNIT WT.
D ECO # 3279
C ECO # 3197
B ECO # 3178
F ECO # 3488
E ECO # 3349
SYM REVISION DESCRIPTION CHK APPD DATE
TITLE SCHEMATIC DIAGRAM MULTI-USER CONTROLLER / BPORT
COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803
DWG NO. DS21E282
SHEET 1 OF 5 SHEETS
4-45

DIA2	DIB2	DIC2	MAPDC + DIA3	A0	A1	GS
L	X	X	X	L	L	L
H	L	X	X	L	L	L
H	H	L	X	L	H	L
H	H	H	L	H	H	L
H	H	H	H	H	H	H

74148 TRUTH TABLE

INSERT JPI FOR BPORT OPERATION

DS21E282

SEE SH 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

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TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ± 1/64 ANGULAR ± 1°00'

MATERIAL:

FINISH:

PART NUMBER | NEXT ASSEMBLY | QTY

DRWN D. DAVIDSON 4/84

CHK

ENGR

PROJ

MFG

SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

TITLE: SCEMATIC DIAGRAM MULTI-USER CONTROLLER / BPORT

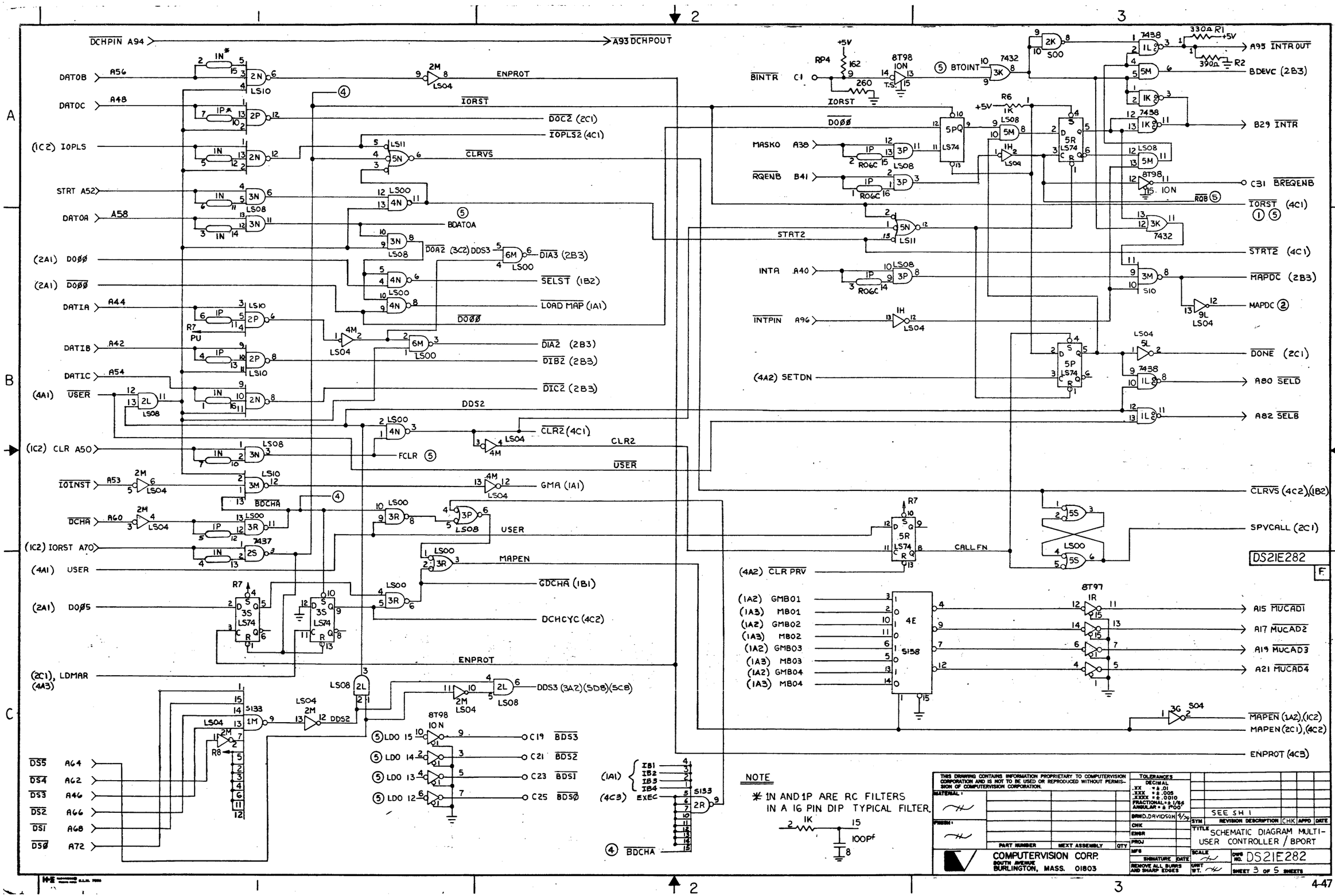
SCALE

SIZE C | DWG NO. DS21E282

UNIT WT.

SHEET 2 OF 5 SHEETS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803


DCHPIN A94
A93 DCHPOUT
DATOB A56
DATOC A48
(1C2) IOPLS
STRT A52
DATOA A58
(2A1) DOØØ
(2A1) DOØØ
DATIA A44
DATIB A42
DATIC A54
(4A1) USER
(1C2) CLR A50
IOINST A53
DCHA A60
(1C2) IORST A70
(4A1) USER
(2A1) DOØ5
(2C1), LDMAR (4A3)
DS5 A64
DS4 A62
DS3 A46
DS2 A66
DS1 A68
DSØ A72
ENPROT
IORST
DOC2 (2C1)
IOPLS2 (4C1)
CLRVS
BDATOA
DOA2 (3C2) DDS3
DIA3 (2B3)
SELST (1B2)
LOAD MAP (1A1)
DOØØ
DIA2 (2B3)
DIB2 (2B3)
DIC2 (2B3)
DDS2
CLR2 (4C1)
CLR2
FCLR
USER
GMA (1A1)
BDCHA
USER
MAPEN
GDCHA (1B1)
DCHCYC (4C2)
ENPROT
DDS3 (3A2)(5D8)(5C8)
LDO 15
LDO 14
LDO 13
LDO 12
C19 BDS3
C21 BDS2
C23 BDS1
C25 BDSØ
(1A1) IB1 IB2 IB3 IB4
(4C3) EXEC
4 BDCHA
BINTR C1
5 BTOINT
IORST
DOØØ
MASKO A38
RQENB B41
STRT2
INTA A40
INTPIN A96
(4A2) SETDN
R6
A95 INTROUT
BDEVC (2B3)
B29 INTR
C31 BREQENB
RQB 5
IORST (4C1) 1 5
STRT2 (4C1)
MAPDC (2B3)
MAPDC 2
DONE (2C1)
A80 SELD
A82 SELB
CLRVS (4C2),(1B2)
SPYCALL (2C1)
DS21E282
F
CALLFN
(4A2) CLR PRV
(1A2) GMB01
(1A3) MB01
(1A2) GMB02
(1A3) MB02
(1A2) GMB03
(1A3) MB03
(1A2) GMB04
(1A3) MB04
A15 MUCAD1
A17 MUCAD2
A19 MUCAD3
A21 MUCAD4
MAPEN (1A2),(1C2)
MAPEN (2C1),(4C2)
ENPROT (4C3)
+5V
330Ω R1
390Ω R2
260
1K
NOTE
* 1N AND 1P ARE RC FILTERS IN A 16 PIN DIP TYPICAL FILTER.
1K
100pf
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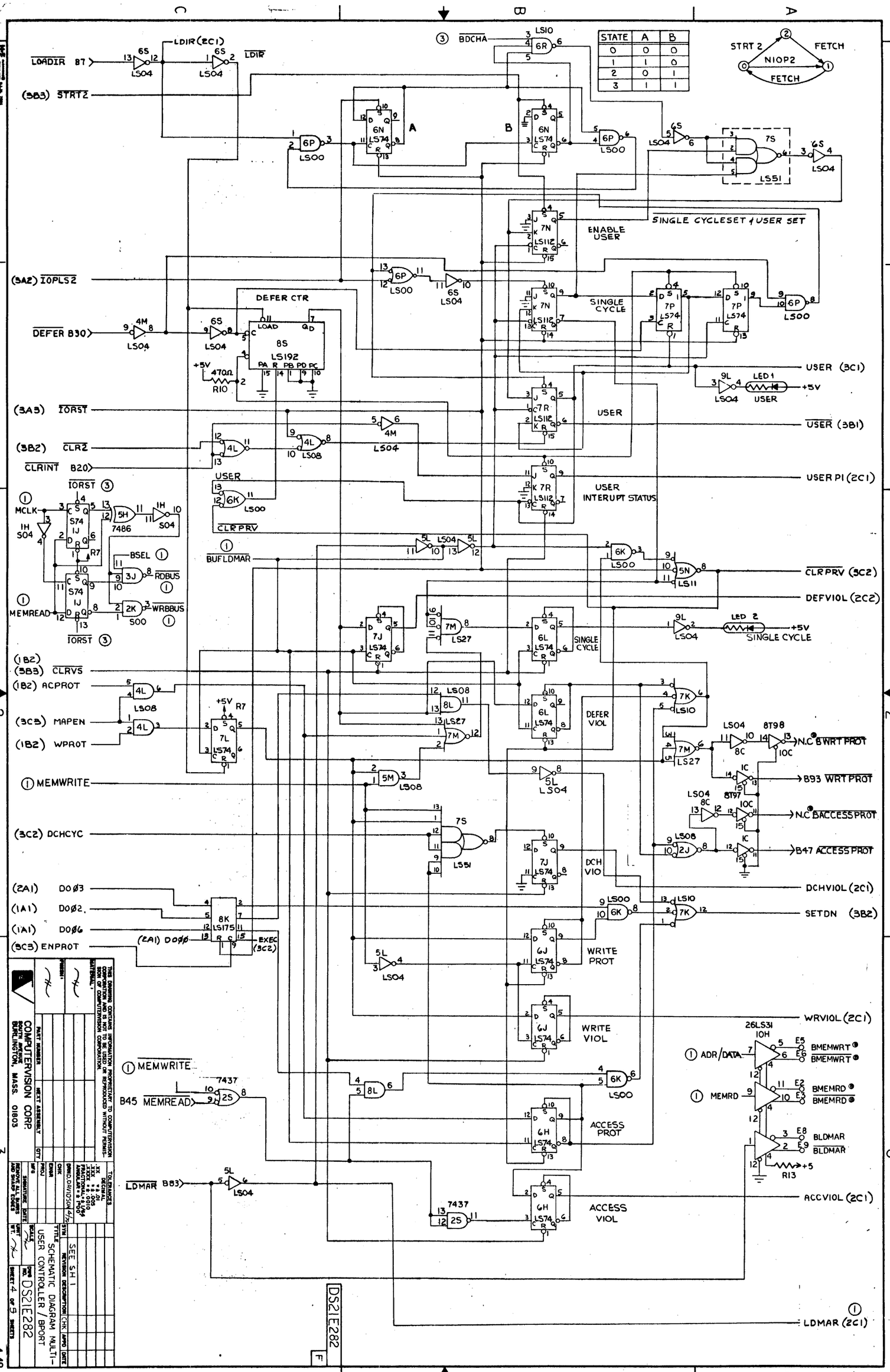
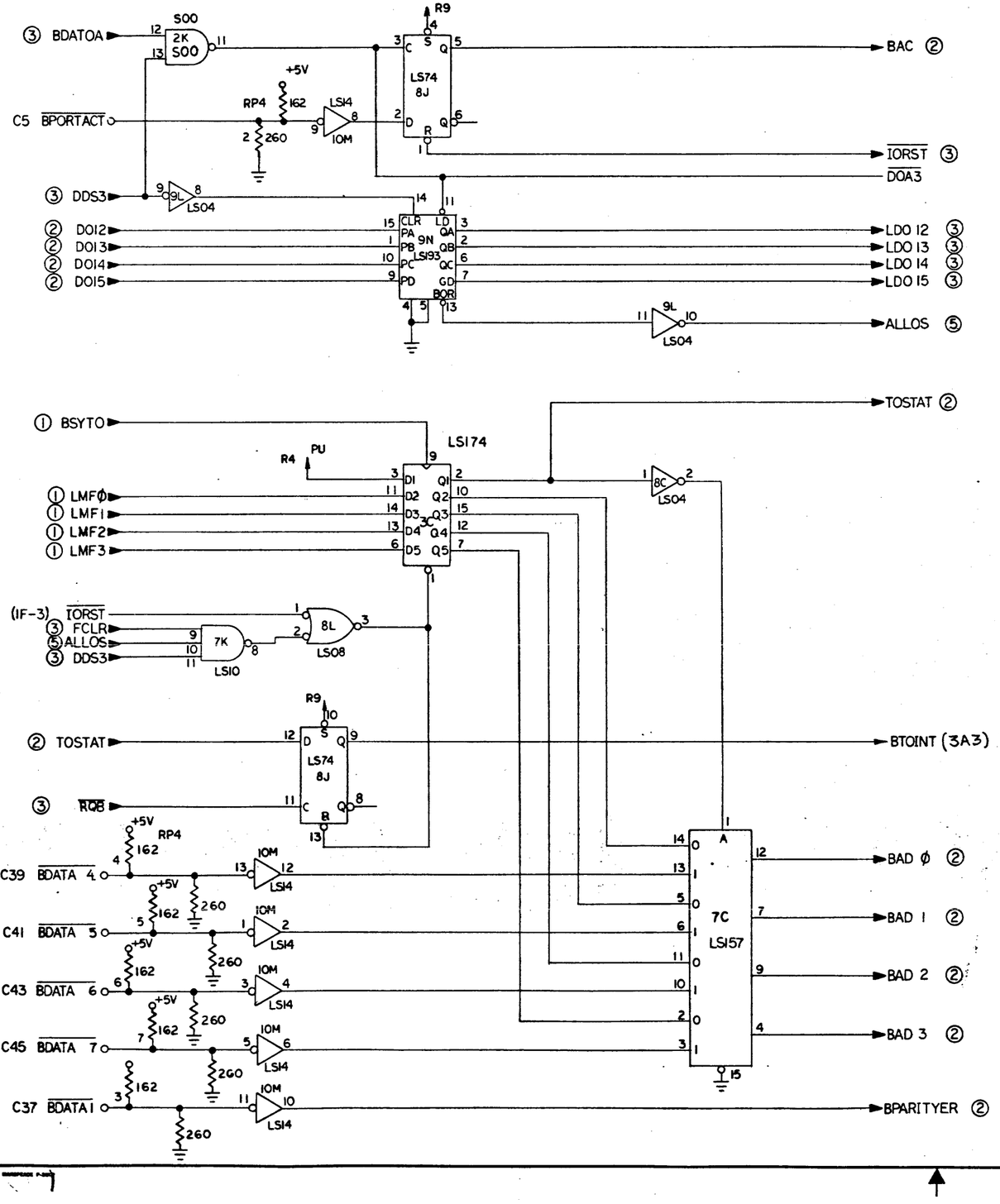
TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL ± 1/64
ANGULAR = ± 1°00
MATERIAL
FINISH
BRND. DAVIDSON 4/77
CHK
ENGR
PROJ
MFG
PART NUMBER
NEXT ASSEMBLY
QTY
SIGNATURE
DATE
REMOVE ALL BURRS AND SHARP EDGES
SEE SH 1
SYM
REVISION DESCRIPTION
CHK
APPD
DATE
TITLE
SCHEMATIC DIAGRAM MULTI-USER CONTROLLER / BPORT
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
SCALE
DWG NO. DS21E282
UNIT WT.
SHEET 3 OF 5 SHEETS
4-47


LOADIR B7
LDIR(2C1)
LDIR
(5B3) STRT2
BDCHA
STATE A B
0 0 0
1 1 0
2 0 1
3 1 1
STRT 2
FETCH
NIOP2
FETCH
ENABLE USER
SINGLE CYCLESET / USER SET
(5A2) IOPLS2
DEFER CTR
DEFER B30
SINGLE CYCLE
USER (3C1)
LED 1
USER
(5A3) IORST
USER
USER (3B1)
(5B2) CLR2
CLRINT B20
USER PI (2C1)
USER INTERUPT STATUS
MCLK
BSEL
RDBUS
MEMREAD
WRBBUS
CLR PRV
BUFLDMAR
CLR PRV (3C2)
DEFVIOL (2C2)
LED 2
SINGLE CYCLE
(1B2)
(5B3) CLRVS
(1B2) ACPROT
(3C3) MAPEN
(1B2) WPROT
DEFER VIOL
N.C B WRT PROT
B93 WRT PROT
N.C B ACCESS PROT
B47 ACCESS PROT
MEMWRITE
(3C2) DCHCYC
DCH VIO
DCHVIOL (2C1)
(2A1) DØØ3
(1A1) DØØ2
(1A1) DØØ6
(3C3) ENPROT
(2A1) DØØØ
EXEC (3C2)
SETDN (3B2)
WRITE PROT
WRVIOL (2C1)
WRITE VIOL
ADR/DATA
MEMRD
BMEMWRT
BMEMRD
BLDMAR
MEMREAD B45
ACCESS PROT
LDMAR B83
ACCESS VIOL
ACCVIOL (2C1)
LDMAR (2C1)
DS21E282
F
COMPUTERVISION CORP
SOUTH AVENUE
BURLINGTON, MASS. 01803
USER CONTROLLER / BPORT
SCHEMATIC DIAGRAM MULTI-
SEE SH 1
SHEET 4 OF 5 SHEETS
4-48



SWITCH PACKS 5D & 5F

THE PRORER SWITCHES IN SWITCH PACKS 5D & 5F MUST BE CLOSED WHEN THE MUC IS DRIVING B PORT MEMORIES. ONE SWITCH MUST BE CLOSED FOR EVERY 32K BPORT FIELD SEGMENT ADDRESS THAT IS BEING USED IN A CONFIGURED SYSTEM.

BPORT FIELD ADDR*	CLOSED SWITCH POSITION 5D	5F
0		8
1		7
2		6
3		5
4		4
5		3
6		2
7		1
8	8	
9	7	
10	6	
11	5	
12	4	
13	3	
14	2	
15	1	

* THE BPORT FIELD ADDR REPRESENTS ONE 32K SEGMENT OF MEMORY.

REF SHT. 2, JP1 MUST BE INSERTED WHEN THE MUC IS DRIVING BPORT MEMORIES.

B PORT CONNECTOR PINOUTS

CONN C

1	BINTR		2
3			4
5	BPORTACT		6
7			8
9			10
11	BIORST		12
13	BCLR		14
15	BIOPLS		16
17			18
19	BDS3		20
21	BDS2		22
23	BDS1		24
25	BDS0		26
27			28
29			30
31	BRQENB		32
33			34
35			36
37	BDATA1		38
39	BDATA4		40
41	BDATA5		42
43	BDATA6		44
45	BDATA7		46
47			48
49			50

CONN E

1		BMEMRD	2
3	BMEMRD		4
5	BMEMWRT	BMEMWRT	6
7		BLDMAR	8
9	BLDMAR		10
11	BMEMBUS15		12
13	14		14
15	13		16
17	12		18
19	11		20
21	10		22
23	9		24
25	8		26
27	7		28
29	6		30
31	5		32
33	4		34
35	3		36
37	2	FREE	38
39	1	FREE	40
41	BMEMBUSØ		42
43	BMC3	FREE	44
45	BMC2	BMC Ø	46
47	BMCT		48
49		BMEMBSY	50

ALL UNUSED PINS GROUNDED

DS21E282 E

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ± 1/64 ANGULAR ± 1°-0'

MATERIAL:

FINISH:

PART NUMBER	NEXT ASSEMBLY	QTY

BRM P. Trapp 2/78
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

SEE SH 1

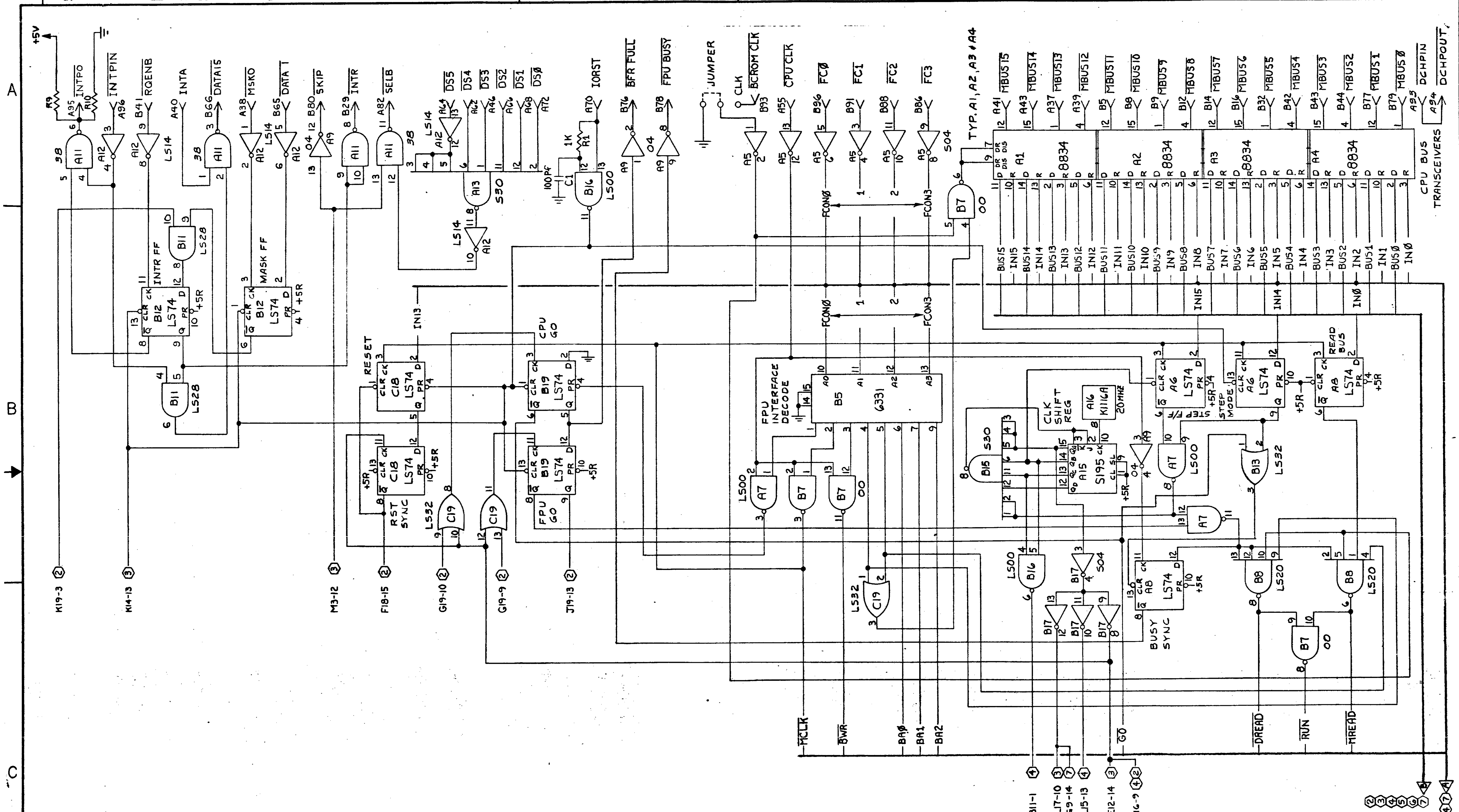
SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE: SCHEMATIC DIAGRAM MULTI-USER CONTROLLER / BPORT

SCALE: NONE DWG NO. DS21E282

UNIT WT. NONE SHEET 5 OF 5 SHEETS

Floating Point Unit



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MATERIAL:	
FINISH:	
PART NUMBER	NEXT ASSEMBLY: A21E115

TOLERANCES
DECIMAL
.XX = ±.01
.XXX = ±.005
.XXXX = ±.0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
C	ECO # 3396			
B	ECO # 2904			
A/2	REL. ECO # 2646			

DRN D. DAVIDSON

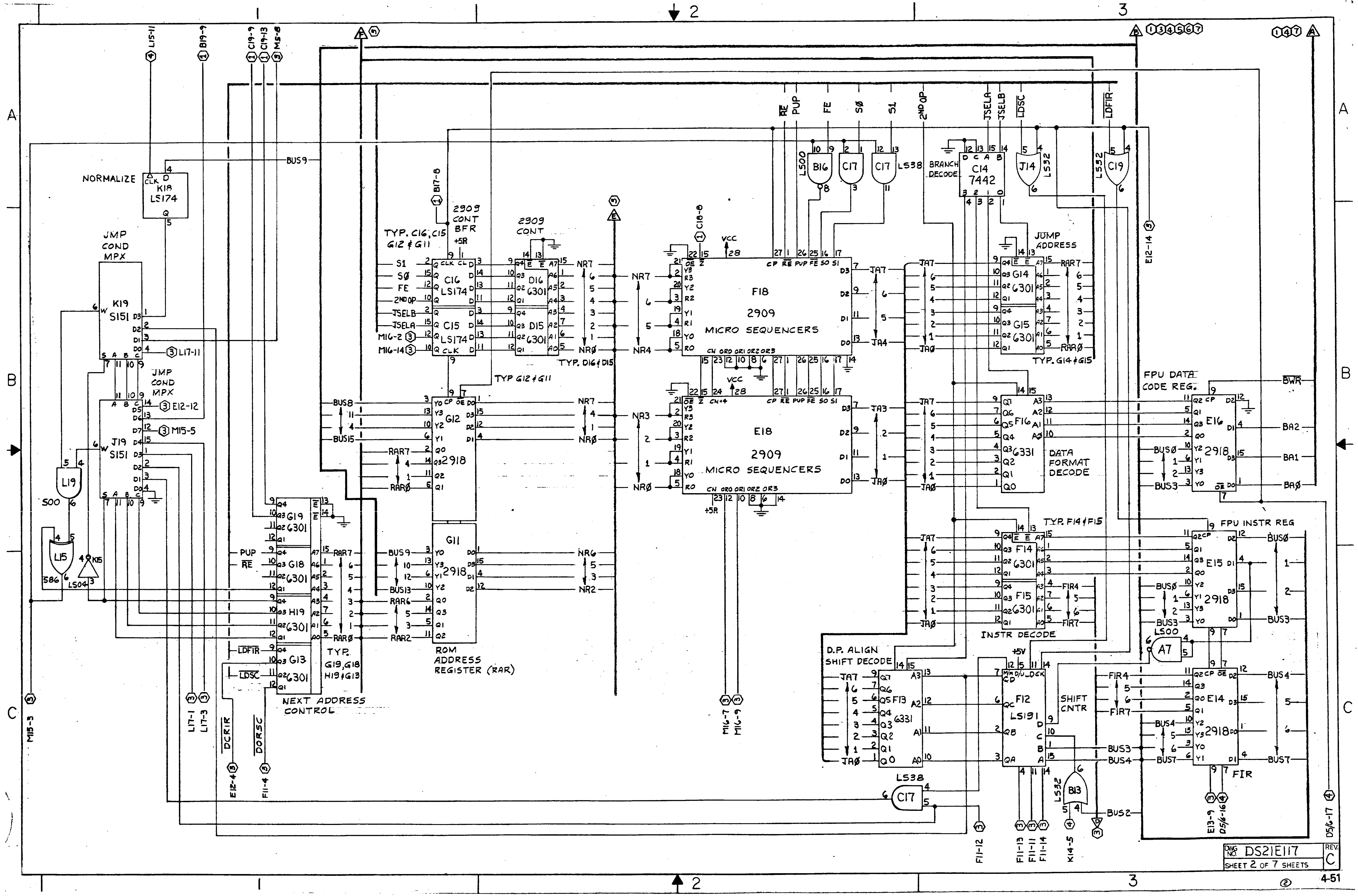
TITLE SCHEMATIC DIAGRAM FLOATING POINT UNIT

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

DWG NO. DS21E117 REV C

SHEET 1 OF 7 SHEETS

REMOVE ALL BURRS AND SHARP EDGES


NORMALIZE
K18 LS174
JMP COND MPX
K19 S151
J19 S151
L19 S00
L15 S86
LS04
G19 6301
G18 6301
H19 6301
G13 6301
TYP. G19, G18 H19 & G13
NEXT ADDRESS CONTROL
2909 CONT BFR
TYP. C16, C15 G12 & G11
C16 LS174
C15 LS174
2909 CONT
D16 6301
D15 6301
TYP. D16 & D15
TYP G12 & G11
G12 2918
G11 2918
ROM ADDRESS REGISTER (RAR)
F18 2909 MICRO SEQUENCERS
E18 2909 MICRO SEQUENCERS
BRANCH DECODE
C14 7442
JUMP ADDRESS
G14 6301
G15 6301
TYP. G14 & G15
F16 6331
DATA FORMAT DECODE
FPU DATA CODE REG.
E16 2918
TYP. F14 & F15
F14 6301
F15 6301
INSTR DECODE
FPU INSTR REG
E15 2918
D.P. ALIGN SHIFT DECODE
F13 6331
F12 LS191
SHIFT CNTR
E14 2918
FIR
DWG NO. DS21E117
SHEET 2 OF 7 SHEETS
REV. C

NEXT ADDRESS OR

SKIP DECODE

SKIP REG.

A SIGN

B SIGN

STATUS LD MPX

OVER-FLOW SAVE

UNDERFLOW SAVE

STATUS BUS GATE

CLOCK AND STATUS CONTROL

TYP. G16, G17, H14, H15, H16, H17 & H18

RALU CLOCK CONTROL

TYP. D17, D18 & D14

2901 SOURCE CONTROL

B SELECT MULTIPLEX

A SELECT MULTIPLEX

SHIFT COUNTER

FIR & REG COUNTER

FIR GATE

BUS CONTROL

TYP. D13, D11 & D12 2901 ADDRESS CONTROL

TYP. C9 & C11

TYP. C12 & C13

DWG. NO. DS21E117 REV. C

SHEET 3 OF 7 SHEETS

3 4-52

DIVIDE CONT.
B18 LS153
3A-5R
F3 LS174 C16
BUFFER
+5R
M14 174
ALU_FLAGS
M19 LS157
STATUS MPX
BUS15
BUS14
K16 S04
K18 LS174
HID BIT
L19 S00
J14 LS532
K15 LS04
L18 S04
M18 125
K15 LS04
L16 125
M18 125
M18 125
K14 LS08
K14
K15 LS04
LS532
H10/12-15
J16
J17
H17-12
J10/12-15
J16
J17
H17-11
K10/12-15
J15
J17
H17-10
L4/6-15
J15
J17
H17-9
M10/12-15
J15
J16
H16-12
J15
J16
H16-11
D12-9
J14
H16-10
LS532
LS532
L15 S86
M/D CONT.
A17 LS153
J18 LS153
TYP. A17&J18
K17 LS174
K18 LS174
TYP. K17&K18
C6-9
L19-1
2901 INSTRUCTION BUFFER
+5R
B ADDRS
E9 2918
C8 2918
A ADDRS
S04
A MONITOR
MREAD
IN 8
7
6
IN 5
C7 2918
BUS MONITOR
MCLK
IN 4
3
2
IN 1
D7 2918
S04
MREAD
RUN
D8 2918
D9-12
D9-11
D9-10
D9-9
BUS CONTROL
DREAD
C5
FCON3
2
1
FCON0
NOVA I/O CONTROL
B11 LS08
D5-6 154
BUS DECODE
E16-7
E11-15
M1 1&15
E15-7
L10-12 2901 EXPONENT (0:3)
L7-9 2901 EXPONENT (4:7)
DB1
DB2
DB3
DB4
DB5
DB8
BUS2
BUS3
BUS4
BUS1
BUS5
BUS8
B9 S86
S04 L18
M18 125
L4/6-22
L13-11
K10/12-31
L4/6-11
L4/6-31
M10/12-8
L4/6-8
M10/12-31
H1/3-21
M10/12
H1/3-29
K10/12-40
J10/12-40
H10/12-40
E1&2-13
E5&6-15
E37&8-15
C4,3,2&1-9

DWG. NO. DS21E117	REV. C
SHEET 4 OF 7 SHEETS	

4-53

M14-14 · H4/3-9 · M14-3 · (1)(2)(3)(4)(6)(7) · M18-3 · K15-1 · M14-13 · J15-3 · L16-8 · M19-5 · J15-11 · L7-9 · L18-13 · K18-10 · L18-3 · J14-9 · (7)(C)(4) · J14-3

VCC

BUSØ

+5 — 510Ω R2

M10-12 SIGN
2901

DBØ

CARRY LOOK-AHEAD
L13
182

BUS9 · BUS10 · BUS11

L4-6 MANTISSA (0:3)
2901

DB9 · DB10 · DB11

BUS12 · BUS13 · BUS14 · BUS15

L1-3 MANTISSA (4:7)
2901

DB12 · DB13 · DB14 · DB15

J15-6 · D5/6-2

BUSØ · BUS1 · BUS2 · BUS3

K10-12 MANTISSA (8:11)
2901

DBØ · DB1 · DB2 · DB3

CARRY LOOK-AHEAD
M13
182

BUS4 · BUS5 · BUS6 · BUS7

K7-9 MANTISSA (12:15)
2901

DB4 · DB5 · DB6 · DB7

CARRY LOOK-AHEAD
K13
182

BUS8 · BUS9 · BUS10 · BUS11

K4-6 MANTISSA (16:19)
2901

DB8 · DB9 · DB10 · DB11

BUS12 · BUS13 · BUS14 · BUS15

K1-3 MANTISSA (20:23)
2901

DB12 · DB13 · DB14 · DB15

J10/12

500 — L19 · L19

DB8 · DBH

TYP. D1, D2, D3 & D4
+5R 2901 DATA BFR
D2 LS174 → BUS8
D1 LS174

2901 DATA BFR
D4 LS175 · D3 LS175
DB1 · DB1 · DB2 · Ø · 4 · 5 · 6 · DB7 → BUS1 · 2 · 3 · Ø · 4 · 5 · 6 · BUS7

D2 LS174 · D1 LS174
DB9 · 10 · 11 · 12 · 13 · 14 · DB15 → BUS9 · 10 · 11 · 12 · 13 · 14 · BUS15

2901 DATA BFR

DWG NO. D52IE117 REV. C
SHEET 5 OF 7 SHEETS
(5)
4-54

CARRY LOOK-AHEAD

M13

J13

182

H13

182

182

CARRY LOOK-AHEAD

VCC

BUSØ 1 2 BUS3

BUS4 5 6 BUS7

BUS8 9 10 BUS11

BUS12 13 14 BUS15

J10-12 2901 MANTISSA (24:27)

J7-9 2901 MANTISSA (28:31)

J4-6 2901 MANTISSA (32:35)

J1-3 2901 MANTISSA (36:39)

H10-12 2901 MANTISSA (40:43)

H7-9 2901 MANTISSA (44:47)

H4-6 2901 MANTISSA (48:51)

H1-3 2901 MANTISSA (52:55)

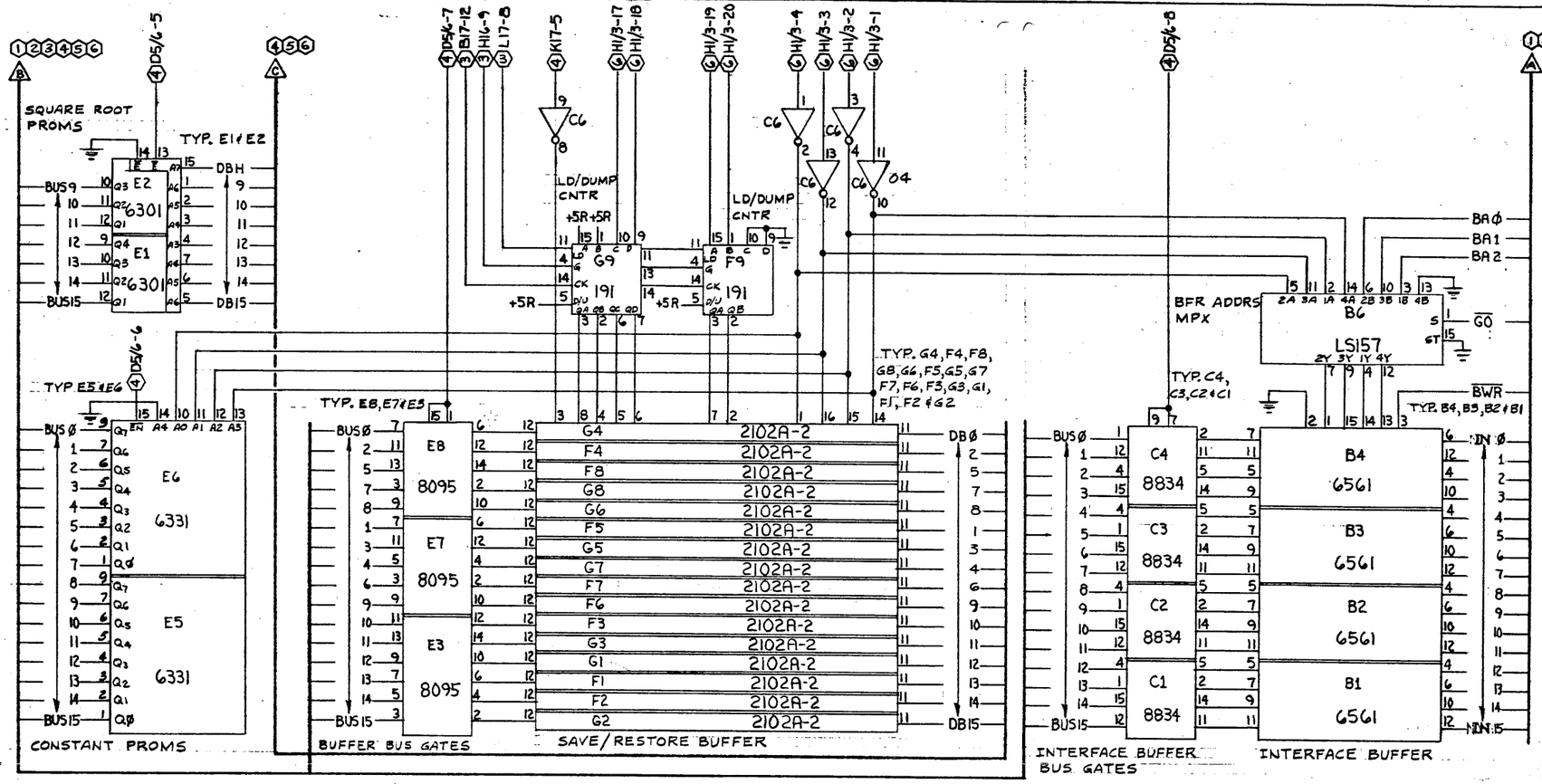
DBØ 1 2 DB3

DB4 5 6 DB7

DB8 9 10 DB11

DB12 13 14 DB15

DWG. NO.	REV.
DS21E117	C
SHEET 6 OF 7 SHEETS	



DWG. NO. DS21E117 REV. C
SHEET 7 OF 7 SHEETS

DA21E250-X CONFIGURATION TABLE

	SINGLE PORT	DUAL PORT. DISTRIBUTED MODE	DUAL PORT. GPU MODE	SINGLE PORT 32K
POPULATED WITH 4K RAMS (MK 4027-3)	USE CONFIGURATION BLOCKS A.A1.B	USE CONFIGURATION BLOCKS A.A1.C.D.E	USE CONFIGURATION BLOCKS A.C.D.E	
POPULATED WITH 16K RAMS (MK 4116-3)	DA21E250-02 USE CONFIGURATION BLOCKS B.F	DA21E250-01 USE CONFIGURATION BLOCKS D.E.F.G	DA21E250-01 USE CONFIGURATION BLOCKS E.F.H	DA21E250-03 USE CONFIGURATION BLOCKS A1.I

CONFIGURATION BLOCK A) 32K HARDWARE CONFIGURATION (USING 4K RAMS)

1) REMOVE R22
2) ADJUST POT R31 SUCH THAT TP HAS A 29 μS REP RATE
3) INSERT JUMPERS: JP9-2 . JP11-2 . JP13-2
4) POPULATE MEMORY ARRAY WITH MK4027-3 MEMORY CHIPS

CONFIGURATION BLOCK A1) APORT 32K ADDRESSING CHART

*APORT FIELD	AMC0	AMC1	AMC2	AMC3	**CLOSED CONTACTS ON SWITCH PACK 1V
0	H	H	H	H	8
1	H	H	H	L	7.8
2	H	H	L	H	6.8
3	H	H	L	L	6.7.8
4	H	L	H	H	5.8
5	H	L	H	L	5.7.8
6	H	L	L	H	5.6.8
7	H	L	L	L	5.6.7.8
8	L	H	H	H	4.8
9	L	H	H	L	4.7.8
10	L	H	L	H	4.6.8
11	L	H	L	L	4.6.7.8
12	L	L	H	H	4.5.8
13	L	L	H	L	4.5.7.8
14	L	L	L	H	4.5.6.8
15	L	L	L	L	4.5.6.7.8

* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
** ALL OTHER CONTACTS ON SWITCH PACK 1V OPEN

CONFIGURATION BLOCK B) SINGLEPORT CONFIGURATION

1) DEPOPULATE PC BOARD AS PER BM21E250-02
2) ADD JUMPERS JP3 . JP5 . JP7

CONFIGURATION BLOCK C) BPORT 32K MEMORY ROW SELECT

1) INSERT JUMPERS: JP10-2 . JP12-2 . JP14-2

CONFIGURATION BLOCK D) BPORT 32K ADDRESSING AND I/O DEVICE CODE CHART

*BPORT FIELD OR I/O DEVICE CODE	$\overline{BMC0}$ OR $\overline{BDS0}$	$\overline{BMC1}$ OR $\overline{BDS1}$	$\overline{BMC2}$ OR $\overline{BDS2}$	$\overline{BMC3}$ OR $\overline{BDS3}$	**CLOSED CONTACTS ON SWITCH PACK 12S
0	H	H	H	H	6
1	H	H	H	L	4.6
2	H	H	L	H	3.6
3	H	H	L	L	3.4.6
4	H	L	H	H	2.6
5	H	L	H	L	2.4.6
6	H	L	L	H	2.3.6
7	H	L	L	L	2.3.4.6
8	L	H	H	H	1.6
9	L	H	H	L	1.4.6
10	L	H	L	H	1.3.6
11	L	H	L	L	1.3.4.6
12	L	L	H	H	1.2.6
13	L	L	H	L	1.2.4.6
14	L	L	L	H	1.2.3.6
15	L	L	L	L	1.2.3.4.6

* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
** ALL OTHER CONTACTS ON SWITCH PACK 12S AND 9C OPEN

CONFIGURATION BLOCK E) LAST BOARD IN DAISY CHAIN

THE LAST DUAL PORT MEMORY BOARD IN A DAISY CHAIN MUST TERMINATE BPORT BUS SIGNALS. THE LAST DUAL PORT MEMORY IN A DAISY CHAIN ONLY MUST HAVE THE FOLLOWING RESISTORS: RP6.RP7.RP8. RP12 . RES PACK 12F

CONFIGURATION BLOCK F) 128K HARDWARE CONFIGURATION/APORT 128K ADDRESSING M

1) R20 AND R22 INSERTED
2) INSERT JUMPER JP4
3) ADJUST POT R31 SUCH THAT TP HAS A 14.5 μS REP RATE
4) INSERT JUMPERS JP9 . JP11 . JP13
5) POPULATE MEMORY ARRAY WITH MK4116-3 MEMORY CHIPS
6) APORT 128K ADDRESSING CHART

*APORT FIELD NO.	$\overline{AMC0}$	$\overline{AMC1}$	$\overline{AMC2}$	$\overline{AMC3}$	$\overline{AMC3}$	**CLOSED CONTACTS ON SWITCH PACK 1V
0.1.2.3	H	H	H	H	H	
4.5.6.7	H	H	H	H	L	5
8.9.10.11	H	H	H	L	H	4
12.13.14.15	H	H	H	L	L	4.5
16.17.18.19	H	H	L	H	H	3
20.21.22.23	H	H	L	H	L	3.5
24.25.26.27	H	H	L	L	H	3.4
28.29.30.31	H	H	L	L	L	3.4.5
32.33.34.35	H	L	H	H	H	2
36.37.38.39	H	L	H	H	L	2.5
40.41.42.43	H	L	H	L	H	2.4
44.45.46.47	H	L	H	L	L	2.4.5
48.49.50.51	H	L	L	H	H	2.3
52.53.54.55	H	L	L	H	L	2.3.5
56.57.58.59	H	L	L	L	H	2.3.4
60.61.62.63	H	L	L	L	L	2.3.4.5
64.65.66.67	L	H	H	H	H	1
68.69.70.71	L	H	H	H	L	1.5
72.73.74.75	L	H	H	L	H	1.4
76.77.78.79	L	H	H	L	L	1.4.5
80.81.82.83	L	H	L	H	H	1.3
84.85.86.87	L	H	L	H	L	1.3.5
88.89.90.91	L	H	L	L	H	1.3.4
92.93.94.95	L	H	L	L	L	1.3.4.5
96.97.98.99	L	L	H	H	H	1.2
100.101.102.103	L	L	H	H	L	1.2.5
104.105.106.107	L	L	H	L	H	1.2.4
108.109.110.111	L	L	H	L	L	1.2.4.5
112.113.114.115	L	L	L	H	H	1.2.3
116.117.118.119	L	L	L	H	L	1.2.3.5
120.121.122.123	L	L	L	L	H	1.2.3.4
124.125.126.127	L	L	L	L	L	1.2.3.4.5

* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
(TO EXPAND BEYOND 15 FIELDS . IC 2X AND 2V . SHT.7 . MUST BE ADDED)
** ALL OTHER SWITCH CONTACTS ON SWITCH 1V ARE OPEN

CONFIGURATION BLOCK G) 128K APORT/32K BPORT COMMON MEMORY

WITH JUMPERS JP10. JP12. JP14. INSERTED

$\overline{BMC2}$	$\overline{BMC3}$	COMMON SEGMENT OF APORT 128K MEMORY
H	H	1ST 32K
H	L	2ND 32K
L	H	3RD 32K
L	L	4TH 32K

2) TO FORCE COMMON APORT/BPORT MEMORY INDEPENDENT OF BMC2 AND BMC3

$\overline{BMC2}$	$\overline{BMC3}$	COMMON SEGMENT OF APORT 128K MEMORY	JUMPERS INSERTED
X	X	1ST 32K	JP10. JP15. JP16
X	X	2ND 32K	JP10. JP16
X	X	3RD 32K	JP10. JP15
X	X	4TH 32K	JP10

WHERE X = DONT CARE

CONFIGURATION BLOCK H) BPORT 128K ADDRESSING CONFIGURATION

1) INSERT JUMPERS JP10. JP12. JP14
2) BPORT 128K ADDRESSING CHART

BPORT FIELD NO.	BMAD0	BMAD1	BMAD2	BMC0	BMC1	**CLOSED CONTACTS ON SWITCH PACKS 9C	12S
0.1.2.3	H	H	H	H	H		8
4.5.6.7	H	H	H	H	L		2.8
8.9.10.11	H	H	H	L	H		1.8
12.13.14.15	H	H	H	L	L		1.2.8
16.17.18.19	H	H	L	H	H	7	8
20.21.22.23	H	H	L	H	L	7	2.8
24.25.26.27	H	H	L	L	H	7	1.8
28.29.30.31	H	H	L	L	L	7	1.2.8
32.33.34.35	H	L	H	H	H	6	8
36.37.38.39	H	L	H	H	L	6	2.8
40.41.42.43	H	L	H	L	H	6	1.8
44.45.46.47	H	L	H	L	L	6	1.2.8
48.49.50.51	H	L	L	H	H	6.7	8
52.53.54.55	H	L	L	H	L	6.7	2.8
56.57.58.59	H	L	L	L	H	6.7	1.8
60.61.62.63	H	L	L	L	L	6.7	1.2.8
64.65.66.67	L	H	H	H	H	5	8
68.69.70.71	L	H	H	H	L	5	2.8
72.73.74.75	L	H	H	L	H	5	1.8
76.77.78.79	L	H	H	L	L	5	1.2.8
80.81.82.83	L	H	L	H	H	5.7	8
84.85.86.87	L	H	L	H	L	5.7	2.8
88.89.90.91	L	H	L	L	H	5.7	1.8
92.93.94.95	L	H	L	L	L	5.7	1.2.8
96.97.98.99	L	L	H	H	H	5.6	8
100.101.102.103	L	L	H	H	L	5.6	2.8
104.105.106.107	L	L	H	L	H	5.6	1.8
108.109.110.111	L	L	H	L	L	5.6	1.2.8
112.113.114.115	L	L	L	H	H	5.6.7	8
116.117.118.119	L	L	L	H	L	5.6.7	2.8
120.121.122.123	L	L	L	L	H	5.6.7	1.8
124.125.126.127	L	L	L	L	L	5.6.7	1.2.8

EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
ALL OTHER CONTACTS ON SWITCH PACK 12S AND 9C OPEN
(9C-2 MAY BE CLOSED TO DISABLE APORT)

CONFIGURATION BLOCK I) 32K SINGLE PORT CONFIGURATION (USING 16K RAMS)

1) DEPOPULATE BOARDS AS PER ASSEMBLY DA21E250-03

DS21E252 G

MISCELLANEOUS JUMPERS

1) FOR LDMAR STARTING APORT MEMORY CYCLE INSERT JP-2
2) FOR MEMREAD STARTING APORT MEMORY CYCLE INSERT JP-1
3) FOR GPU MODE REQUIRING DISABLED APORT . CLOSE SWITCH 9C-2
4) APORT MUC/NON MUC OPERATION

JUMPER PLUG 4D	
MUC OPERATION	1-16 2-15 3-14 4-13
NON MUC OPERATION	5-12 6-11 7-10 8-9

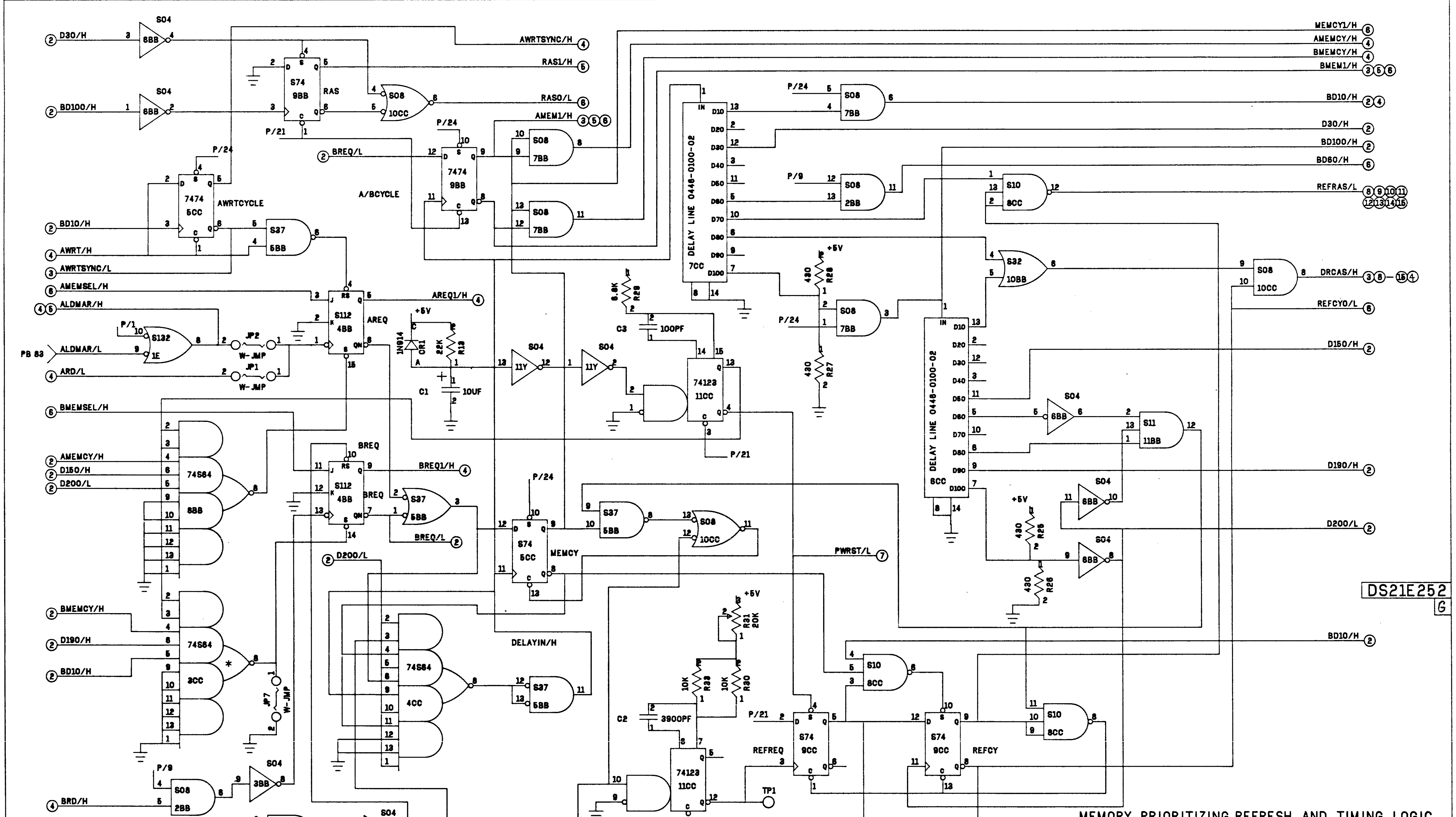
5) APORT I/O DEVICE CODE

1) STANDARD 24_8. INSERT JP8 FOR 25_8

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
G	ECO 4149			8/81
F	ECO 4016			4/81
E	ECO 3423			
D	ECO 3318			

MATERIAL
FINISH
DA21E250 | 1
PART NUMBER | NEXT ASSEMBLY | QTY
TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0030 FRACTIONAL ±1/64 ANGULAR ±.100
REMOVE ALL BURRS AND SHARP EDGES
TITLE 128/32K MEMORY A/B PORT SCH. DIAGRAM
DWG NO. DS21E252
SHT 1 OF 16 SHTS

COMPUTERVISION CORP.
BEDFORD, MASS. 01730



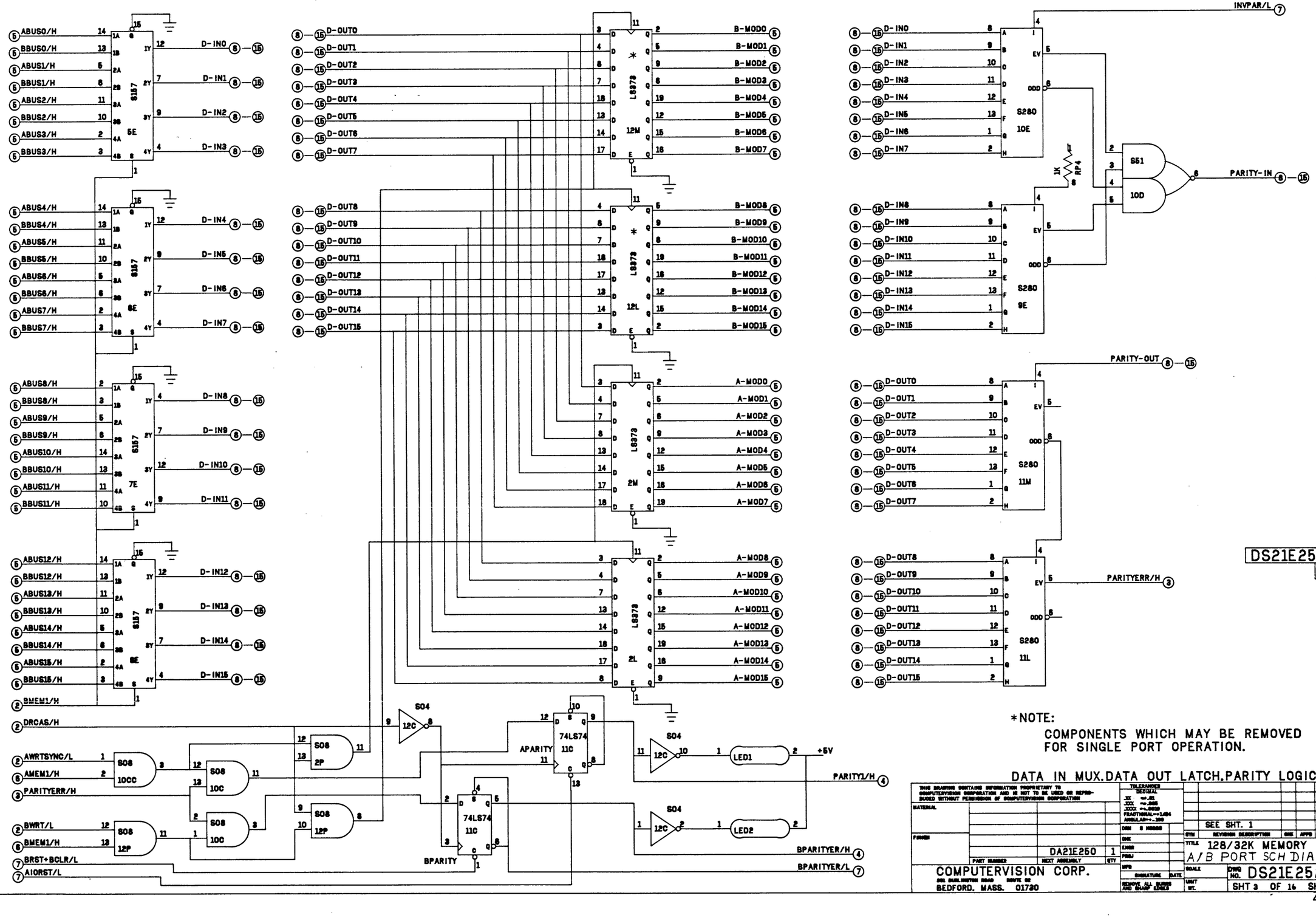
MEMORY PRIORITIZING, REFRESH AND TIMING LOGIC

*NOTE

COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

TITLE	128/32K MEMORY A/B PORT SCH DIA
NEXT ASSEMBLY	DA21E250
DWG NO.	DS21E252
SHEET	SHT 2 OF 14 SHTS
SEE SHT. 1	
DRN	S HOBBS

COMPUTERVISION CORP.
BEDFORD, MASS. 01730



DS21E252
G

*NOTE:
COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

DATA IN MUX.DATA OUT LATCH.PARITY LOGIC

MATERIAL
FINISH
PART NUMBER DA21E250 NEXT ASSEMBLY 1 QTY

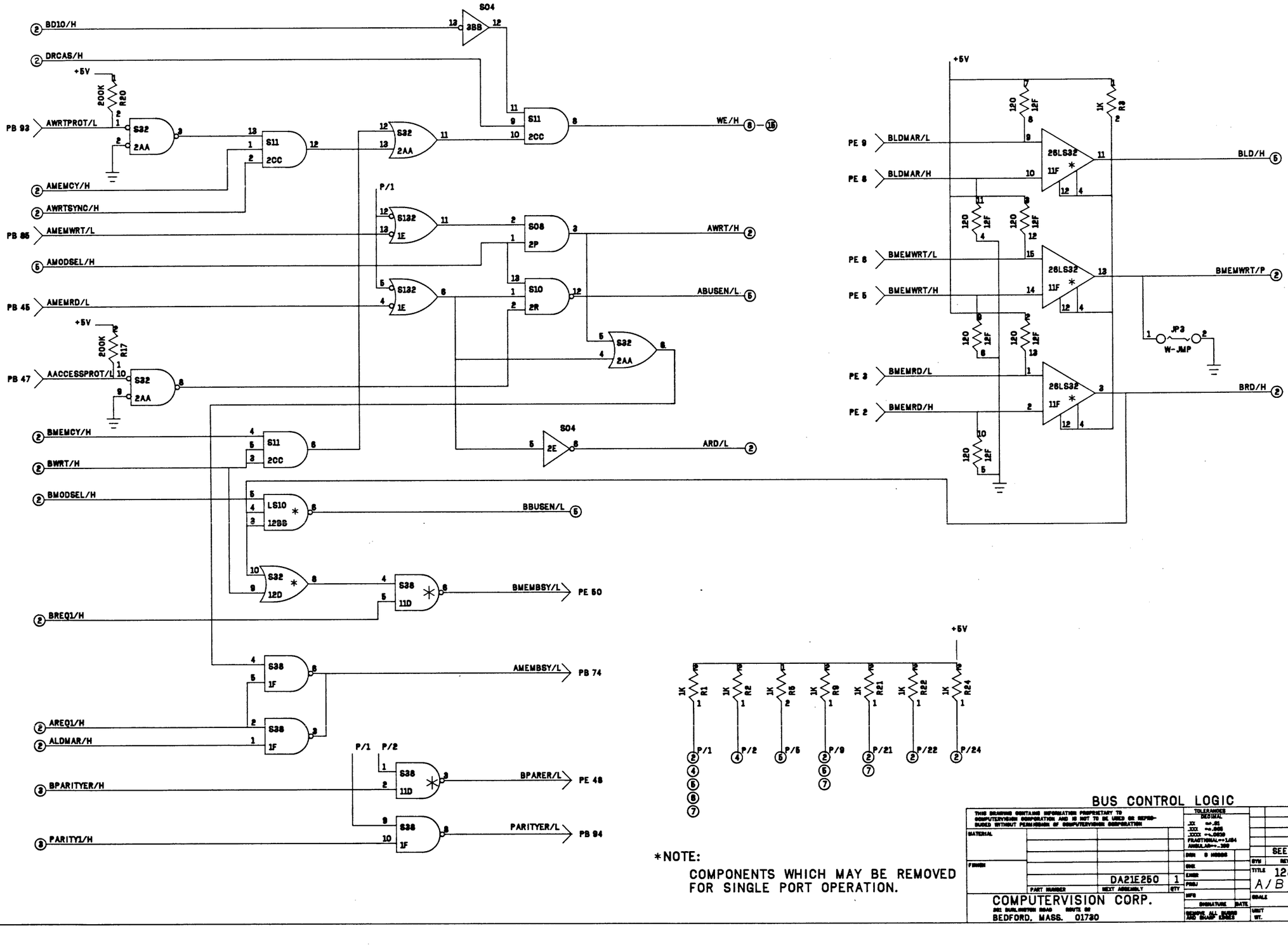
TOLERANCES UNLESS DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0050 FRACTIONAL ±1/64 ANGULAR ±.30
DRN
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY A/B PORT SCH DIA
SCALE
DWG NO. DS21E252
UNIT WT.
SHT 3 OF 16 SHTS

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730



DS21E252
G

*NOTE:
COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

BUS CONTROL LOGIC

TOLERANCES DECIMAL .XX +-.01 .XXX +-.005 .XXXX +-.0050 FRACTIONAL +-1/64 ANGULAR +-.30'

MATERIAL

FINISH

PART NUMBER DA21E250 NEXT ASSEMBLY 1 QTY

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

SIGNATURE DATE

BREAK ALL SHARP EDGES

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

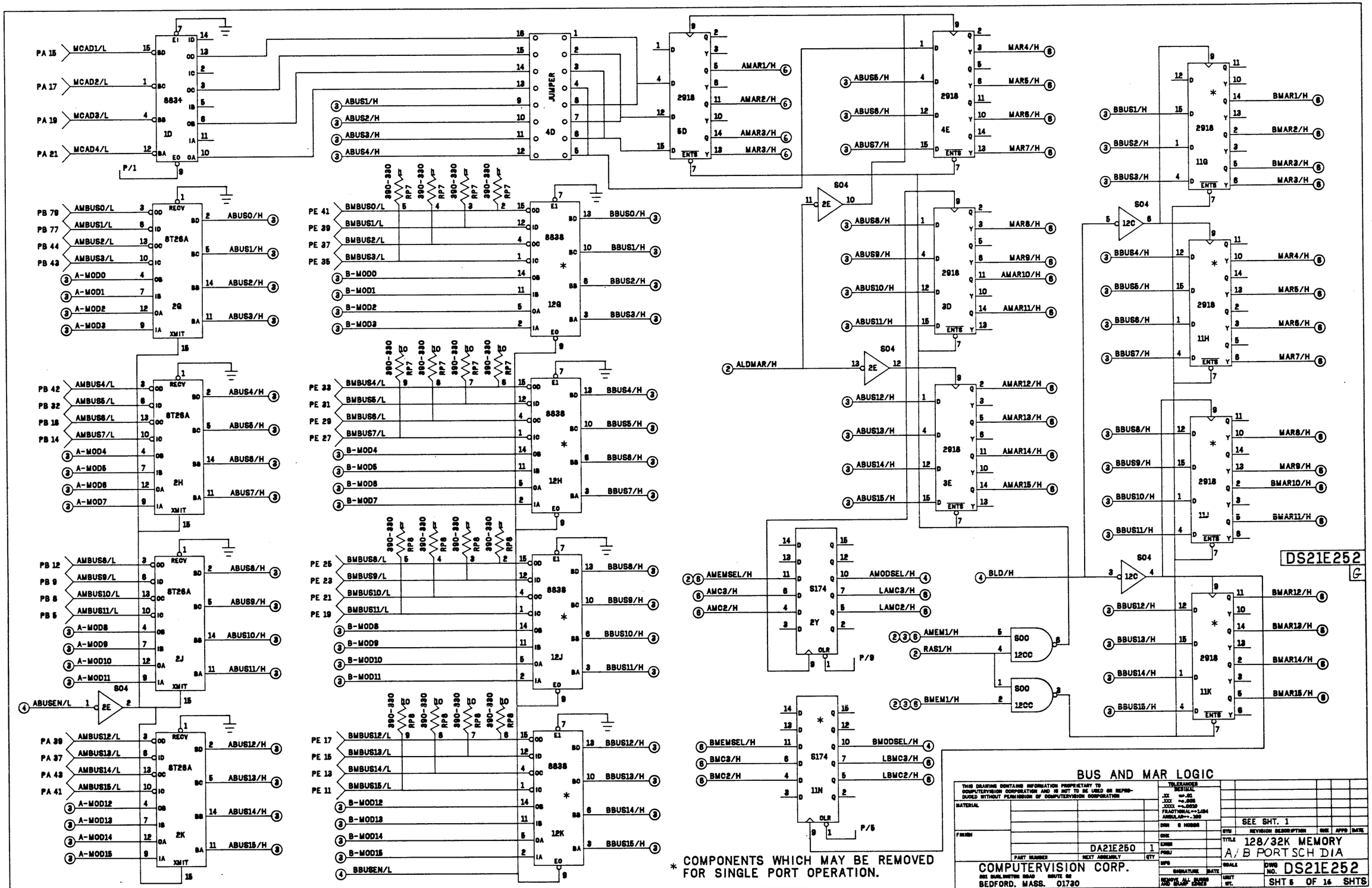
TITLE 128/32K MEMORY A/B PORT SCH DIA

SCALE

DWG NO. DS21E252

UNIT WT.

SHT 4 OF 16 SHTS


BUS AND MAR LOGIC
DS21E252
G
SEE SHT. 1
128/32K MEMORY
A/B PORTSCH DIA
DS21E252
SHT 5 OF 16 SHTS
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DA21E250
* COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

STANDARD JUMPERS (FOR OTHER CONFIGS. SEE SHT. 1)

128K MEM . GPU JP9, JP10, JP11, JP12, JP13, JP14

128K MEM . DIST MODE - JP9, JP10, JP11, JP13, JP15, JP16

ADDR MUX CONTROL		
B	A	RAM ADDR
L	L	CAS ADDR
L	H	APORT RAS ADDR
H	L	BPORT RAS ADDR
H	H	REFRESH ADDR

2X AND 2Y TO BE ADDED FOR FUTURE EXPANSION

* = COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

APORT/BPORT SELECT, ADDR MUX, REFRESH CNTR, RAS CLOCK

DS21E252 G

SEE SHT. 1

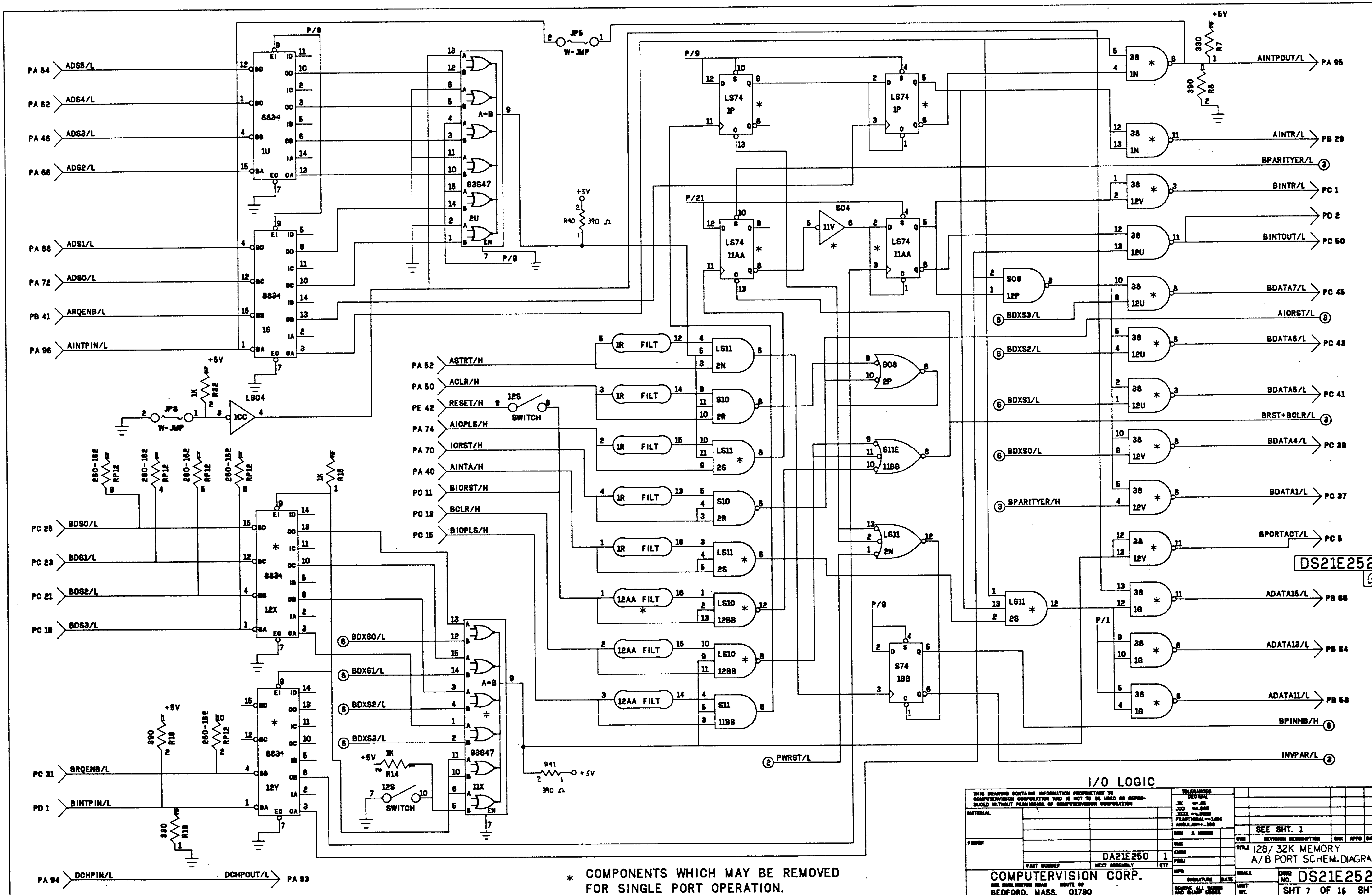
128/32K MEMORY A/B PORT SCHDIA

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

DA21E250 1

DWG NO. DS21E252

SHT 6 OF 16 SHTS



* COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

I/O LOGIC

SEE SHT. 1

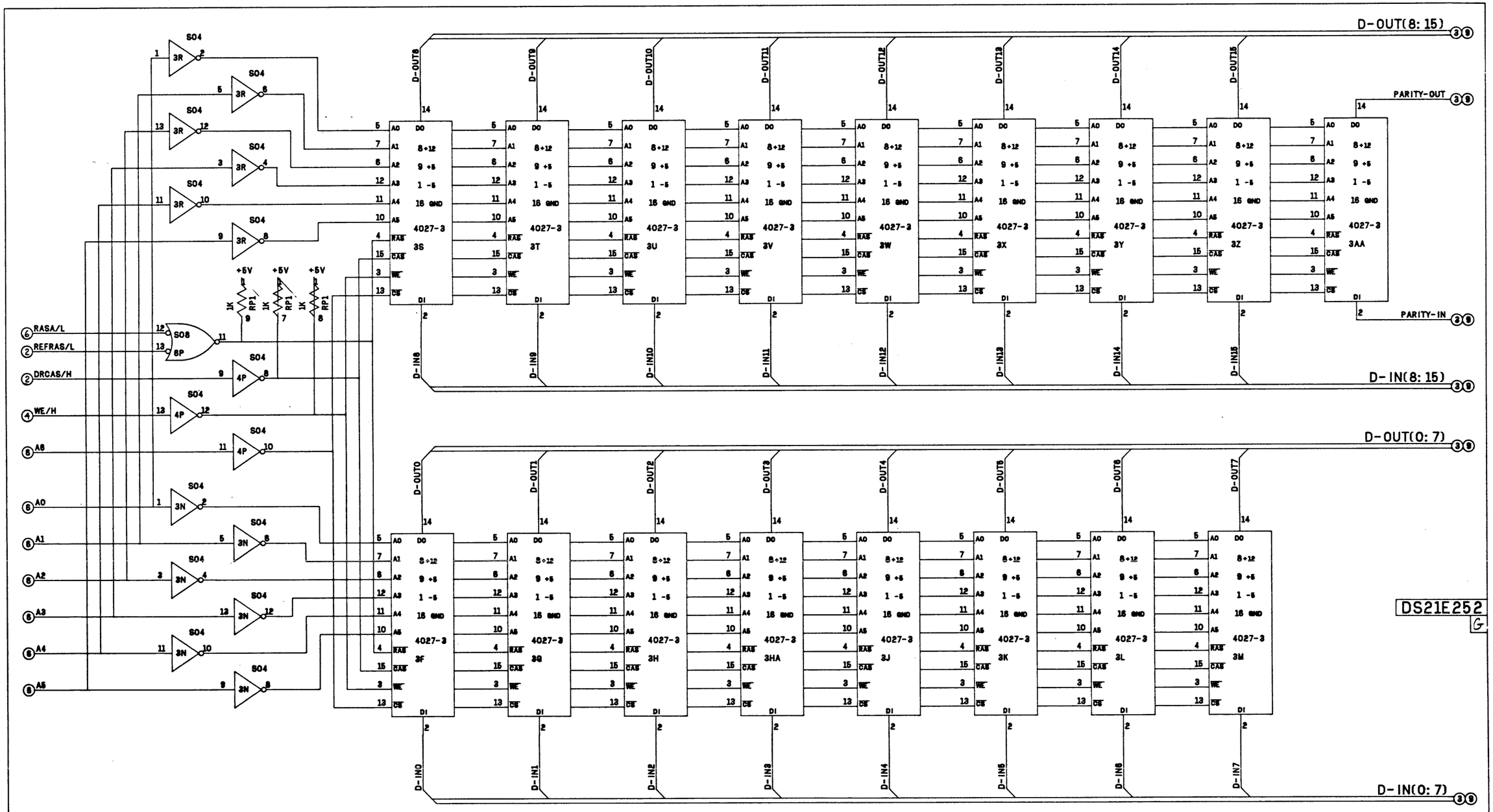
DA21E250

128/32K MEMORY A/B PORT SCHEM. DIAGRAM

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

DWG NO. DS21E252

SHT 7 OF 16 SHTS



MEMORY CHIPS 3S THRU 3AA
AND 3F THRU 3M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
G

MEMORY ROW A

MATERIAL

FINISH

DA21E250 1
PART NUMBER NEXT ASSEMBLY QTY

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL
.XX +-.01
.XXX +-.005
.XXXX +-.0050
FRACTIONAL +-1/64
ANGULAR +-.25°

DRN
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

BREAK SHARP EDGES AND BURRS

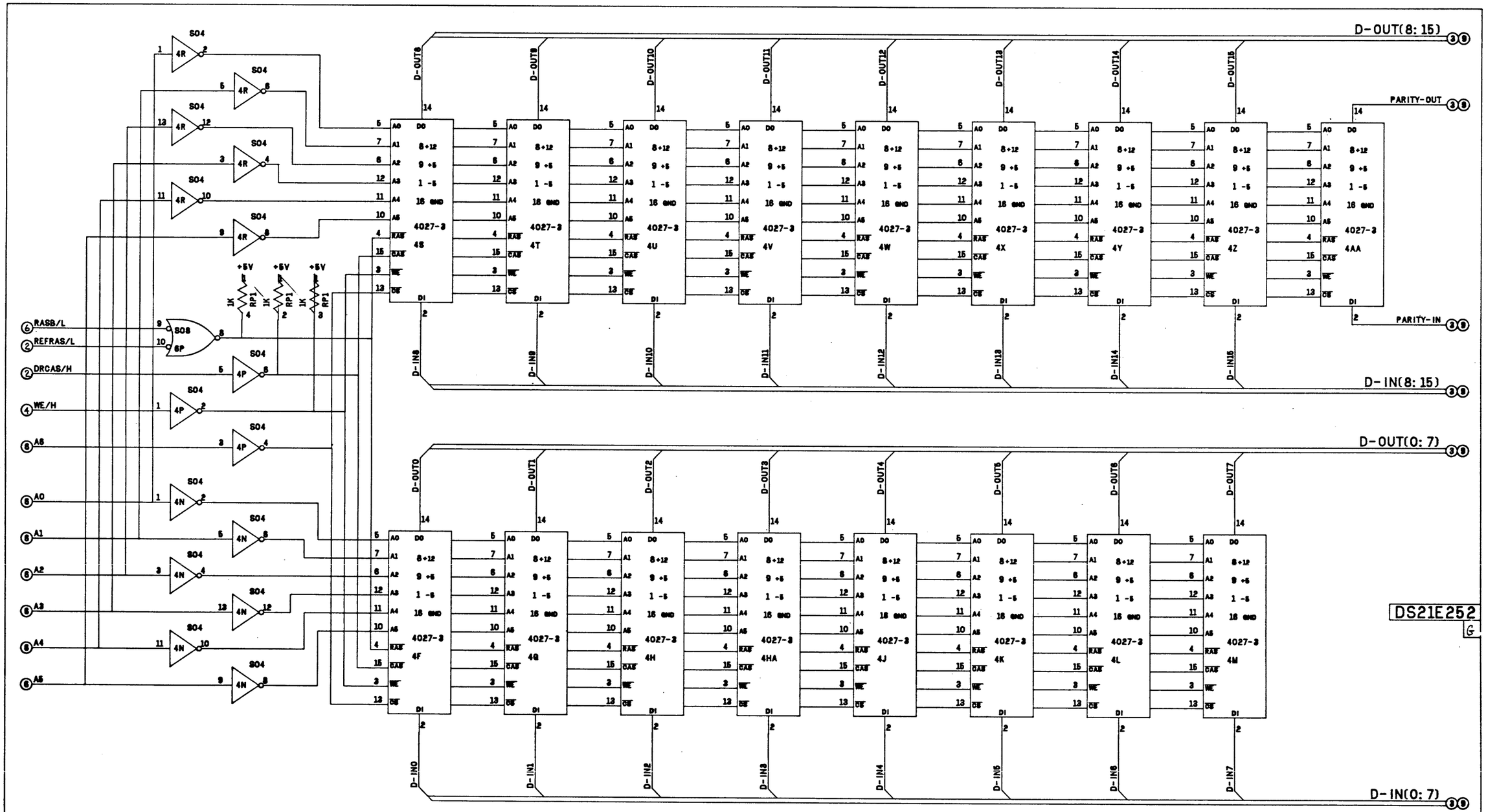
COMPUTERVISION CORP.
201 BURLINGTON ROAD SUITE 02
BEDFORD, MASS. 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCHEM. DIAGRAM

SCALE
DWG NO. DS21E252
SHT WT.
SHT 8 OF 16 SHTS



MEMORY CHIPS 4S THRU 4AA
AND 4F THRU 4M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
G

MEMORY ROW B

SEE SHT. 1

REVISION DESCRIPTION	DWN	APPD	DATE

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONAL +-1/64
ANGULAR +-.30

MATERIAL

FINISH

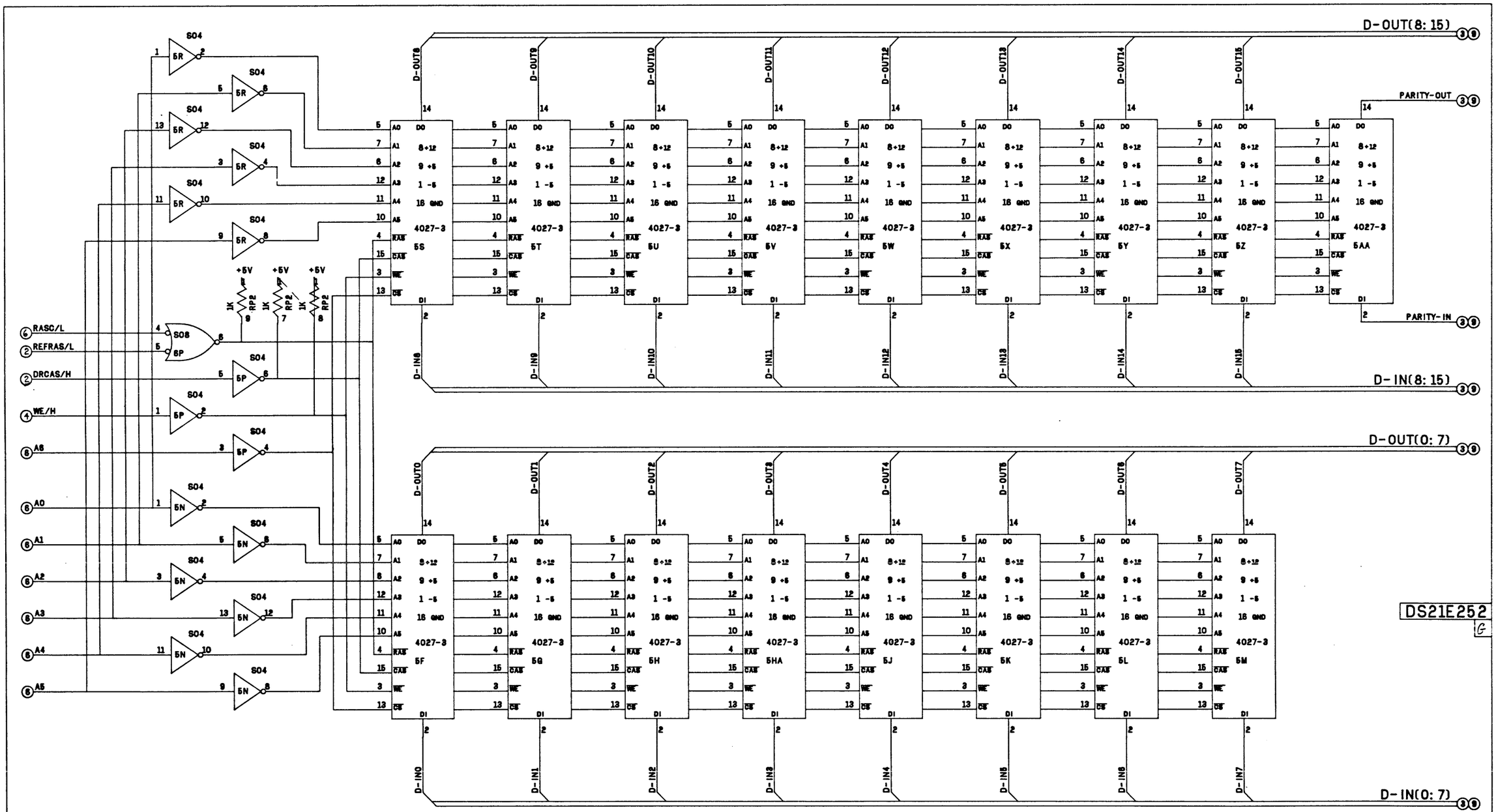
PART NUMBER: DA21E250 1
NEXT ASSEMBLY | QTY

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TITLE: 128/32K MEMORY
A/B PORT SCHEM. DIAGRAM

SIZE: DWG NO. DS21E252

SHT 9 OF 16 SHTS



DS21E252 G

MEMORY CHIPS 5S THRU 5AA
AND 5F THRU 5M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MEMORY ROW C

SEE SHT. 1

DWG	REVISION DESCRIPTION	CHK	APPD	DATE

MATERIAL

FINISH

PART NUMBER DA21E250 | NEXT ASSEMBLY | QTY 1

TOLERANCES UNLESS DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0050 FRACTIONAL ±1/64 ANGULAR ±.30

DRN | CHK | ENGR | PROJ | MFG

SIGNATURE | DATE

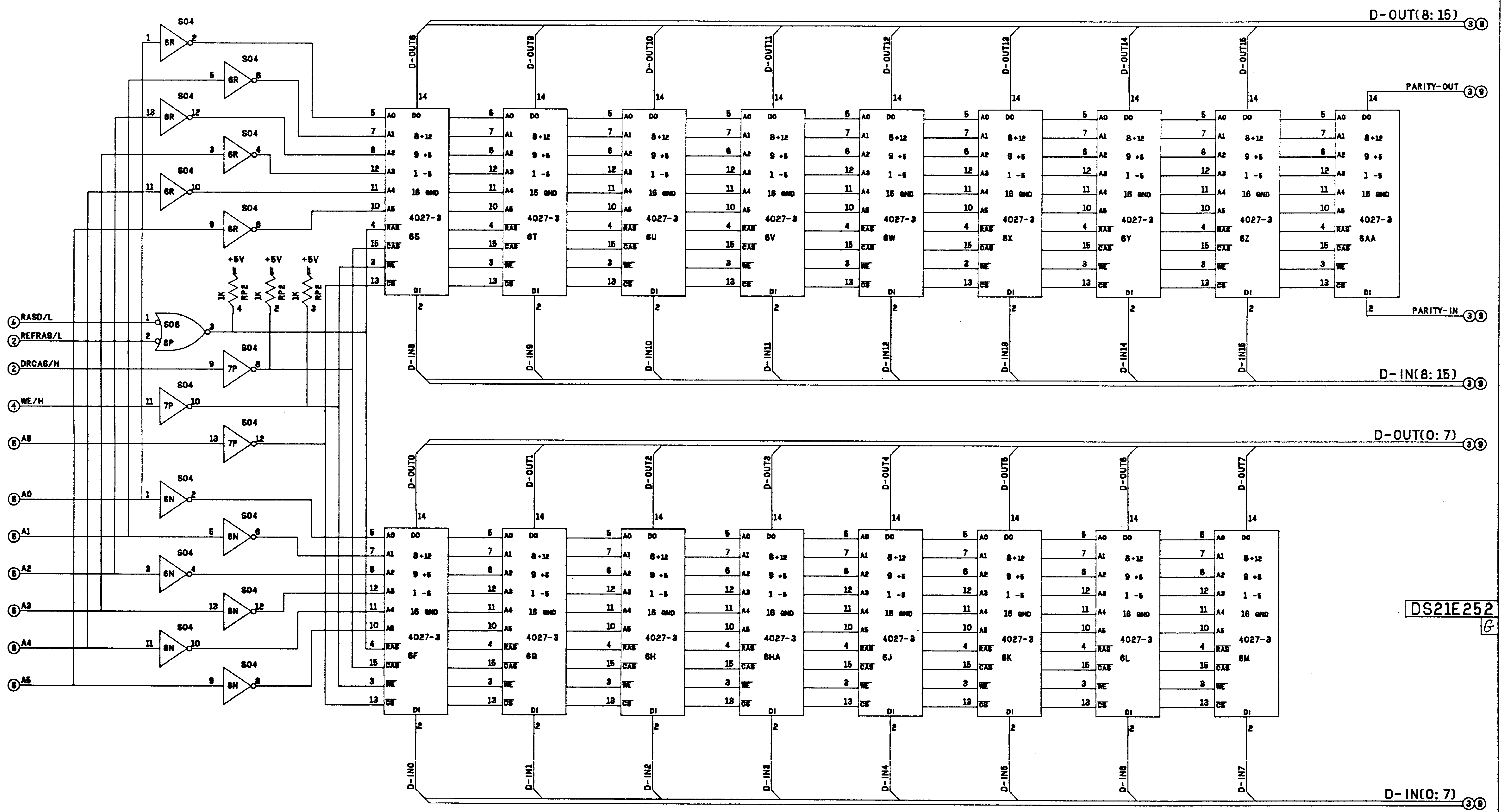
REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TITLE 128/32K MEMORY
A/B PORT SCHEM. DIAGRAM

SCALE | DWG NO. DS21E252

WEIGHT | SHT 10 OF 16 SHTS



MEMORY CHIPS 6S THRU 6AA
AND 6F THRU 6M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MEMORY ROW D

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MATERIAL	
FINISH	
PART NUMBER	
NEXT ASSEMBLY	DA21E250
QTY	1
TOLERANCES DECIMAL	.XX ±.01; .XXX ±.005; .XXXX ±.0020; FRACTIONAL ±1/64; ANGULAR ±.100
REVISION	SEE SHT. 1
TITLE	128/32K MEMORY A/B PORT SCHEM. DIAGRAM
DWG NO.	DS21E252
SHT	SHT 11 OF 16 SHTS

REMOVE ALL BURRS AND SHARP EDGES

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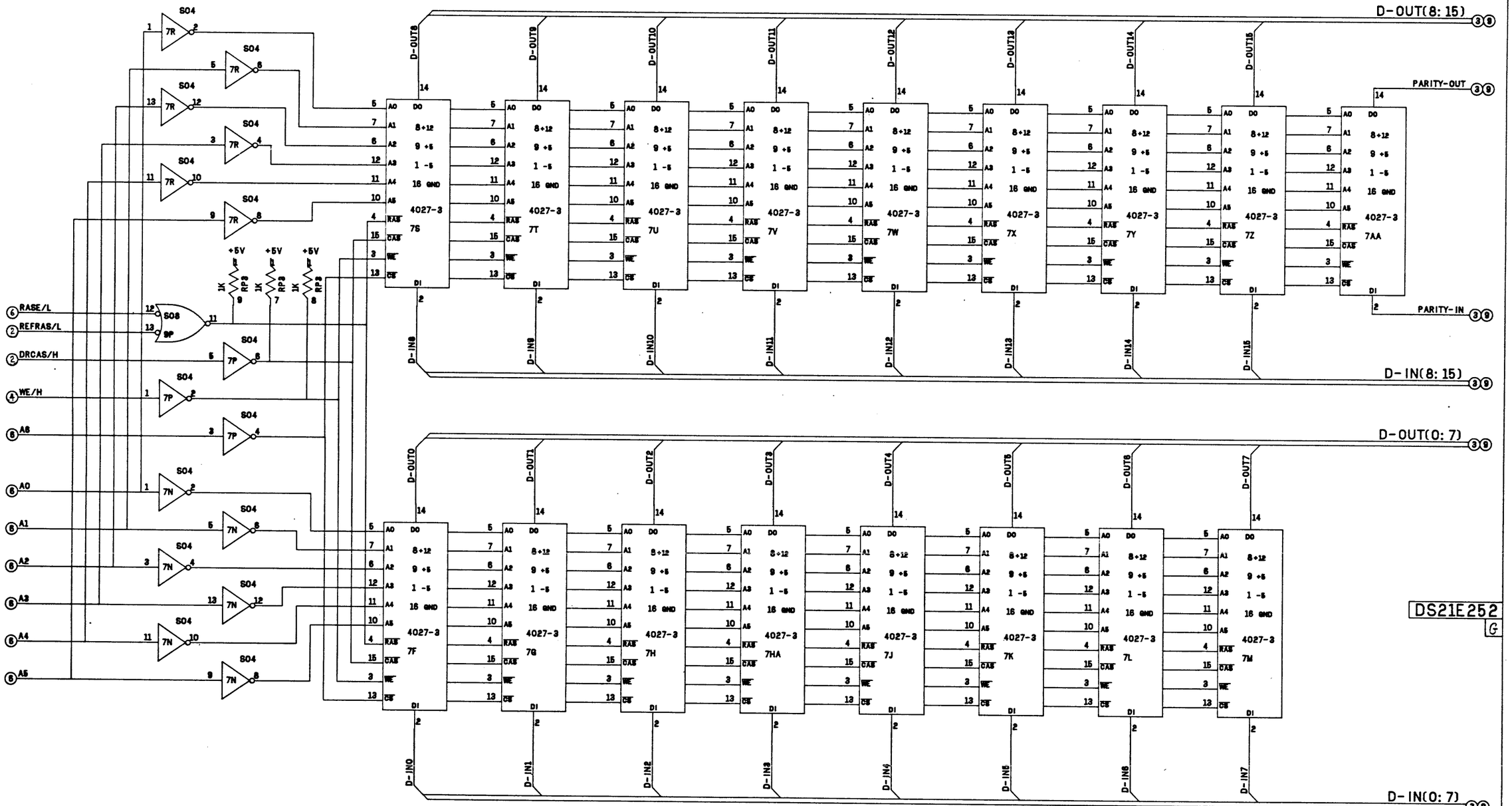
BEDFORD, MASS. 01730



MEMORY CHIPS 7S THRU 7AA
AND 7F THRU 7M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
G

MEMORY ROW E

SEE SHT. 1

TITLE	128/32K MEMORY A/B PORT SCH DIA
DWG NO.	DS21E252
SHT 12 OF 16 SHTS	

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TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL
.XX = ±.01
.XXX = ±.005
.XXXX = ±.0050
FRACTIONAL = ±1/64
ANGULAR = ±.30°
BREAK ALL SHARP EDGES

MATERIAL

FINISH

PART NUMBER DA21E250 | NEXT ASSEMBLY | 1 QTY

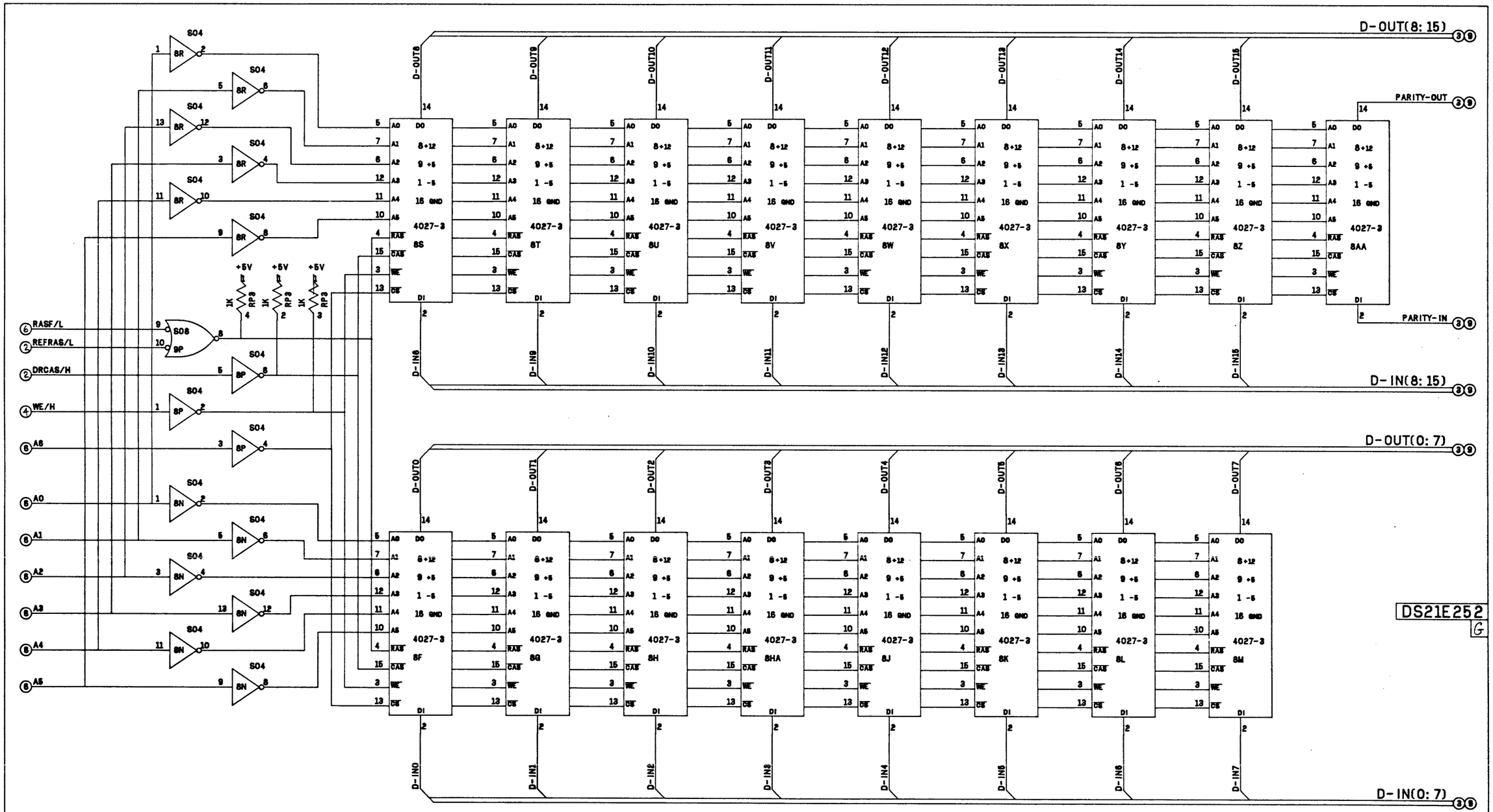
SIGNATURE DATE

COMPUTERVISION CORP.
201 BURLINGTON ROAD BLDG 02
BEDFORD, MASS. 01730

SYM | REVISION DESCRIPTION | CHK | APPD | DATE

SCALE

UNIT WT.



DS21E252 G

MEMORY CHIPS 8S THRU 8AA AND 8F THRU 8M MAY BE EITHER ALL 4027-3 OR 4116-3 PARTS

MEMORY ROW F

MATERIAL

FINISH

PART NUMBER DA21E250 NEXT ASSEMBLY QTY 1

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES UNLESS OTHERWISE SPECIFIED
.XX ±.01
.XXX ±.005
.XXXX ±.0050
FRACTIONAL ±1/64
ANGULAR ±.30

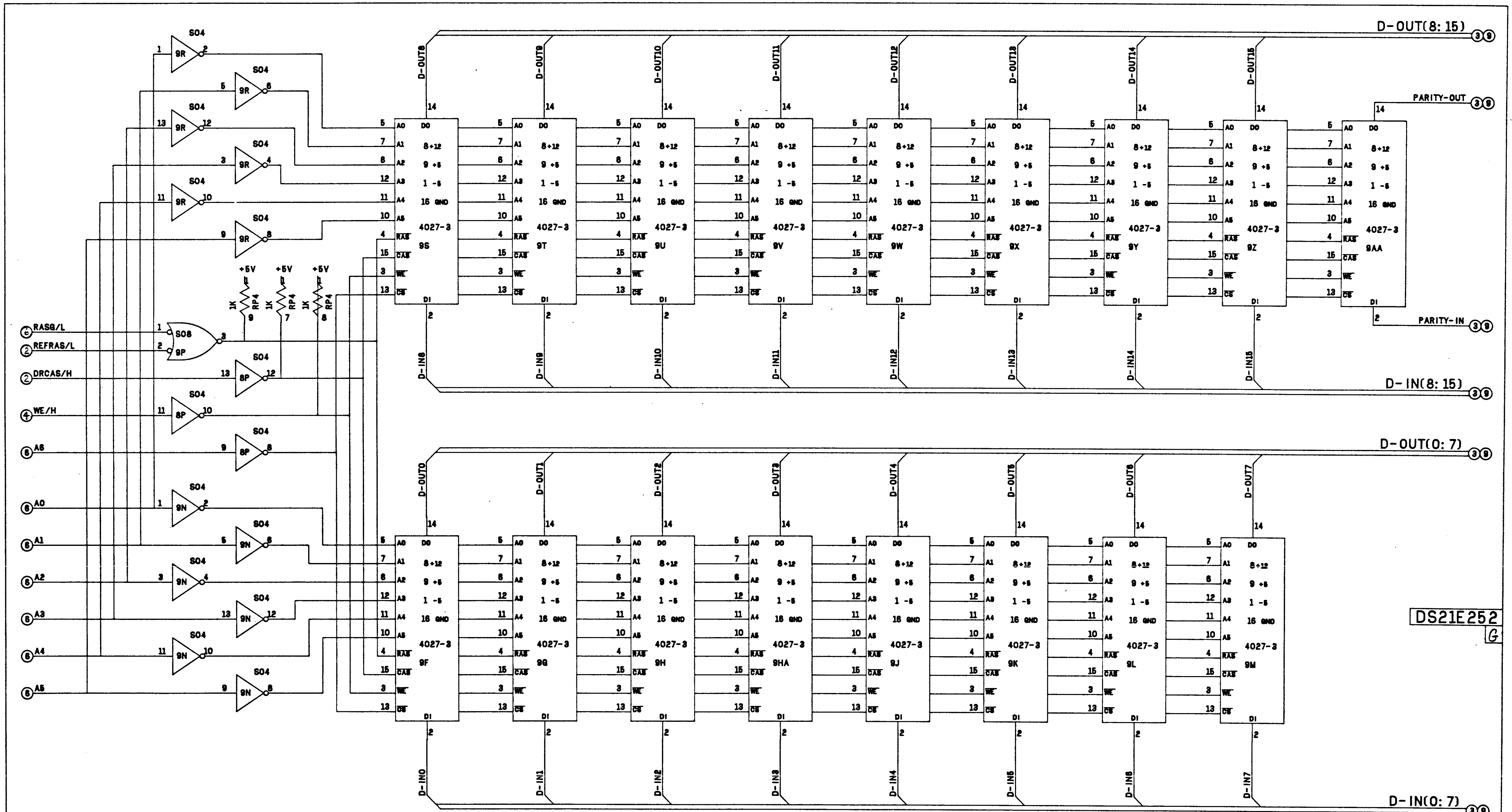
DRN S HIBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

SYS	REVISION DESCRIPTION	ENG	APPD	DATE

TITLE 128/32K MEMORY A/B PORT SCH DIA

SCALE
DWG NO. DS21E252
SHT 13 OF 16 SHTS
UNIT WT.



MEMORY CHIPS 9S THRU 9AA
AND 9F THRU 9M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MEMORY ROW G

MATERIAL

FINISH

DA21E250 1

PART NUMBER | NEXT ASSEMBLY | QTY

SEE SHT. 1

TITLE 128/32K MEMORY
A/B PORT SCH DIA.

DWG NO. DS21E252

SHT 14 OF 14 SHTS

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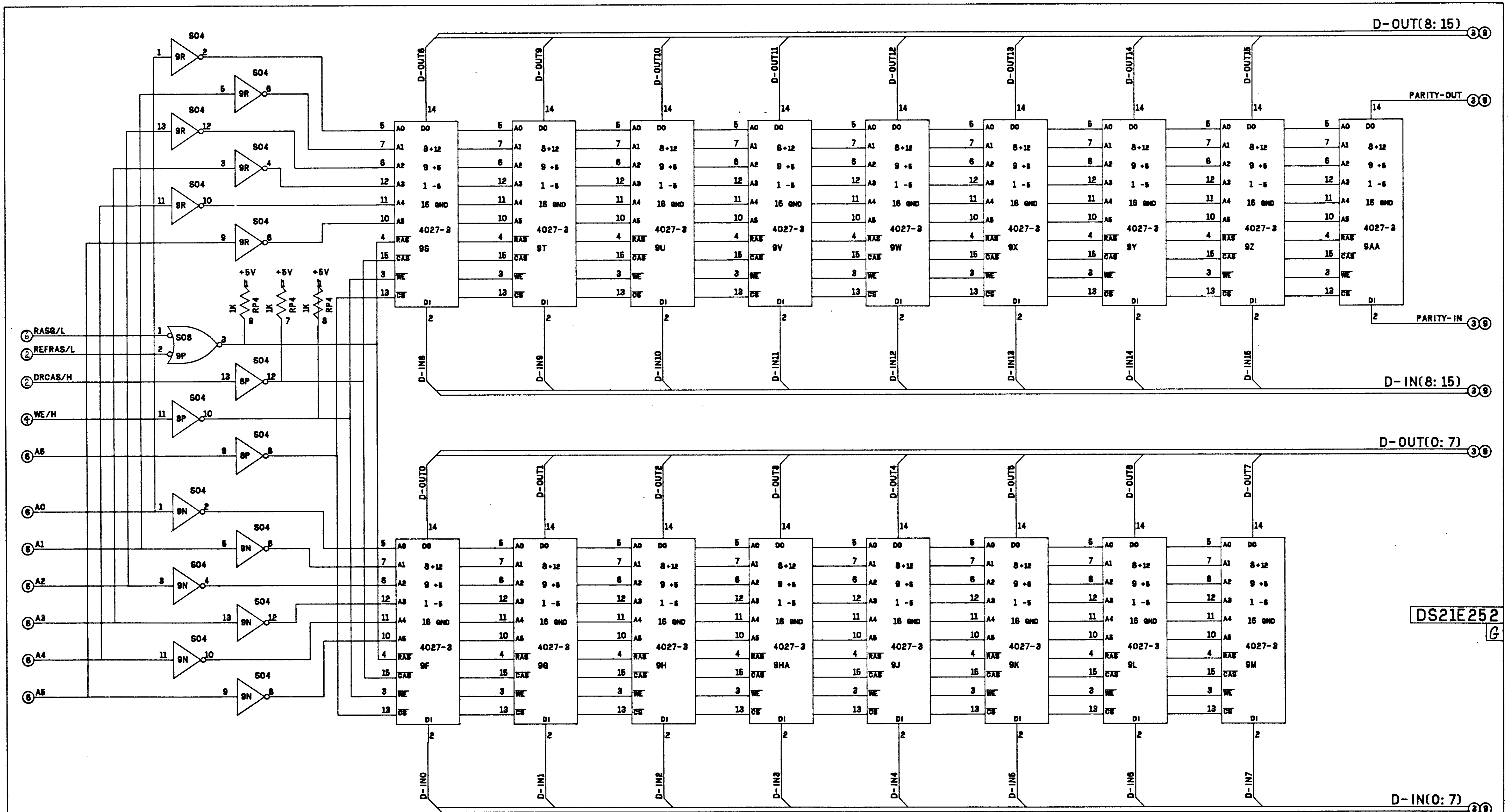
BEDFORD, MASS. 01730

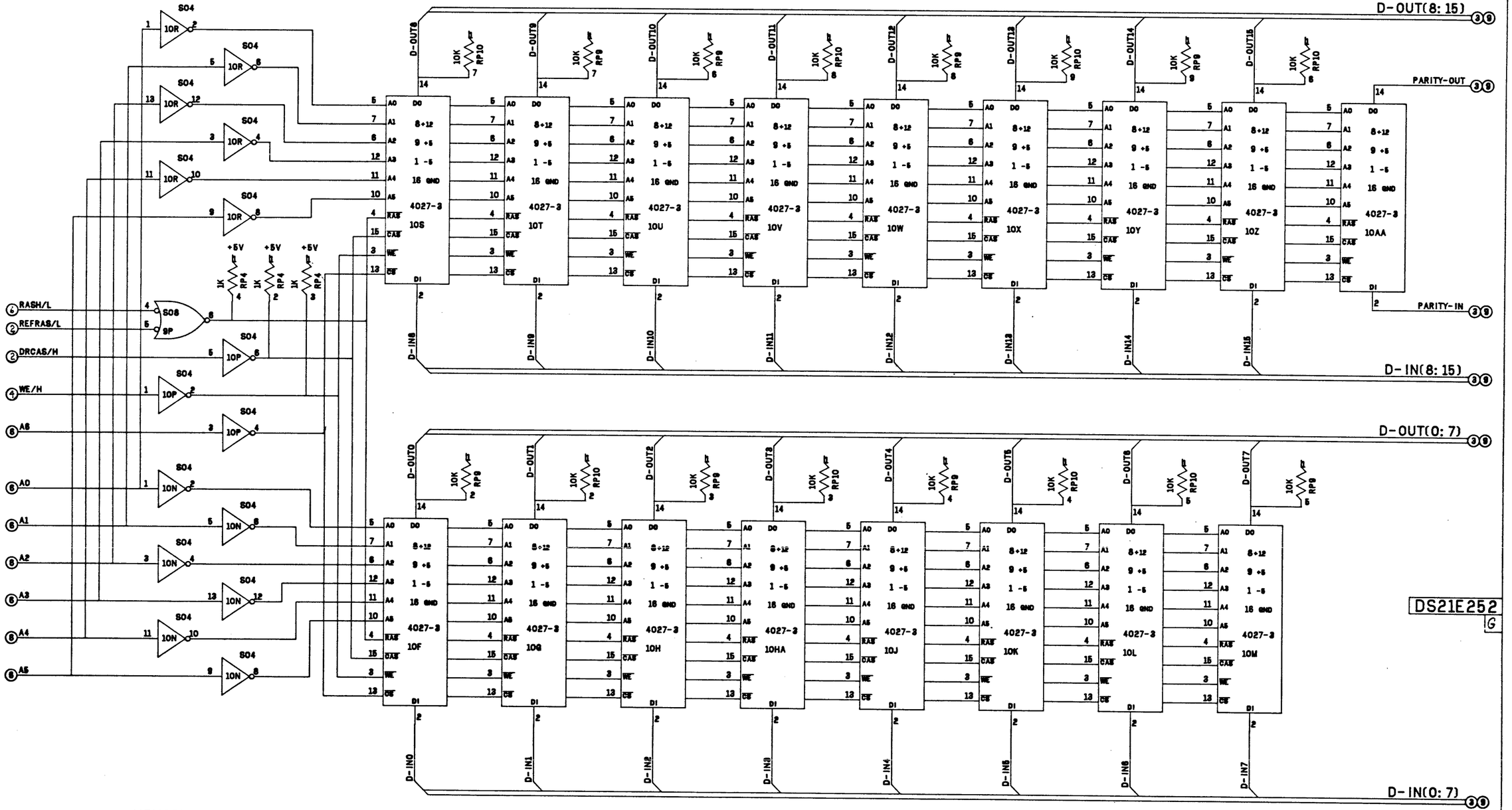


MEMORY CHIPS 9S THRU 9AA
AND 9F THRU 9M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MEMORY ROW G

PART NUMBER	DA21E250
NEXT ASSEMBLY	1
	SEE SHT. 1
TITLE	128/32K MEMORY AZB BOARD SCH DIA.
DWG NO.	DS21E252
	SHT 14 OF 14 SHTS

COMPUTERVISION CORP.
BEDFORD, MASS. 01730



MEMORY CHIPS 10S THRU 10AA
AND 10F THRU 10M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MATERIAL

FINISH

DA21E250 1

PART NUMBER NEXT ASSEMBLY QTY

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONAL ±1/64
ANGULAR ±1°

DRN S MEEKS
CHK
ENGR
PROJ
APP
SIGNATURE DATE

MEMORY ROW H

SEE SHT. 1

SYM	REVISION DESCRIPTION	ENG. APPD	DATE

TITLE 128/32K MEMORY
A2,B PORT SCH DIA

SCALE DWG NO. DS21E252

WEIGHT SHT 15 OF 16 SHTS

B PORT CONNECTORS

CONN C

1	BINTR		2
3			4
5	BPORTACT		6
7			8
9			10
11	BIORST		12
13	BCLR		14
15	BIOPLS		16
17			18
19	BDS 3		20
21	BDS 2		22
23	BDS 1		24
25	BDS 0		26
27			28
29			30
31	BRQENB		32
33			34
35	BDATA 10		36
37	BDATA 1		38
39	BDATA 4		40
41	BDATA 5		42
43	BDATA 6		44
45	BDATA 7		46
47	FREE		48
49		BINTPOUT	50

CONN E

1		B MEM RD	2
3	B MEM RD		4
5	B MEMWRT	BMEMWRT	6
7		BLDMAR	8
9	BLDMAR		10
11	B MEM BUS 15		12
13	B MEM BUS 14		14
15	B MEM BUS 13		16
17	B MEM BUS 12		18
19	B MEM BUS 11		20
21	B MEM BUS 10		22
23	B MEM BUS 9		24
25	B MEM BUS 8		26
27	B MEM BUS 7		28
29	B MEM BUS 6		30
31	B MEM BUS 5		32
33	B MEM BUS 4		34
35	B MEM BUS 3		36
37	B MEM BUS 2	BMAD2	38
39	B MEM BUS 1	BMAD1	40
41	B MEM BUS 0	RESET	42
43	BMC 3	BMAD0	44
45	BMC 2	BMC0	46
47	BMC 1	BPARER	48
49		B MEM BUSY	50

ALL UNUSED PINS GROUNDED

VOLTAGE FEEDS FOR CONNECTORS PA,PB	
+12 VOLTS	B46,A7,A8
-5 VOLTS	B81
-12 VOLTS	B71,B72
+5 VOLTS	A/B3,A/B4,A/B97,A/B98
GND	A/B1,A/B2,A/B99,A/B100

DS21E252
G

MATERIAL

FINISH

DA21E250 1
PART NUMBER NEXT ASSEMBLY QTY

COMPUTERVISION CORP.
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TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0050
FRACTIONAL ±1/64
ANGULAR ±1°

DRN B HIBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

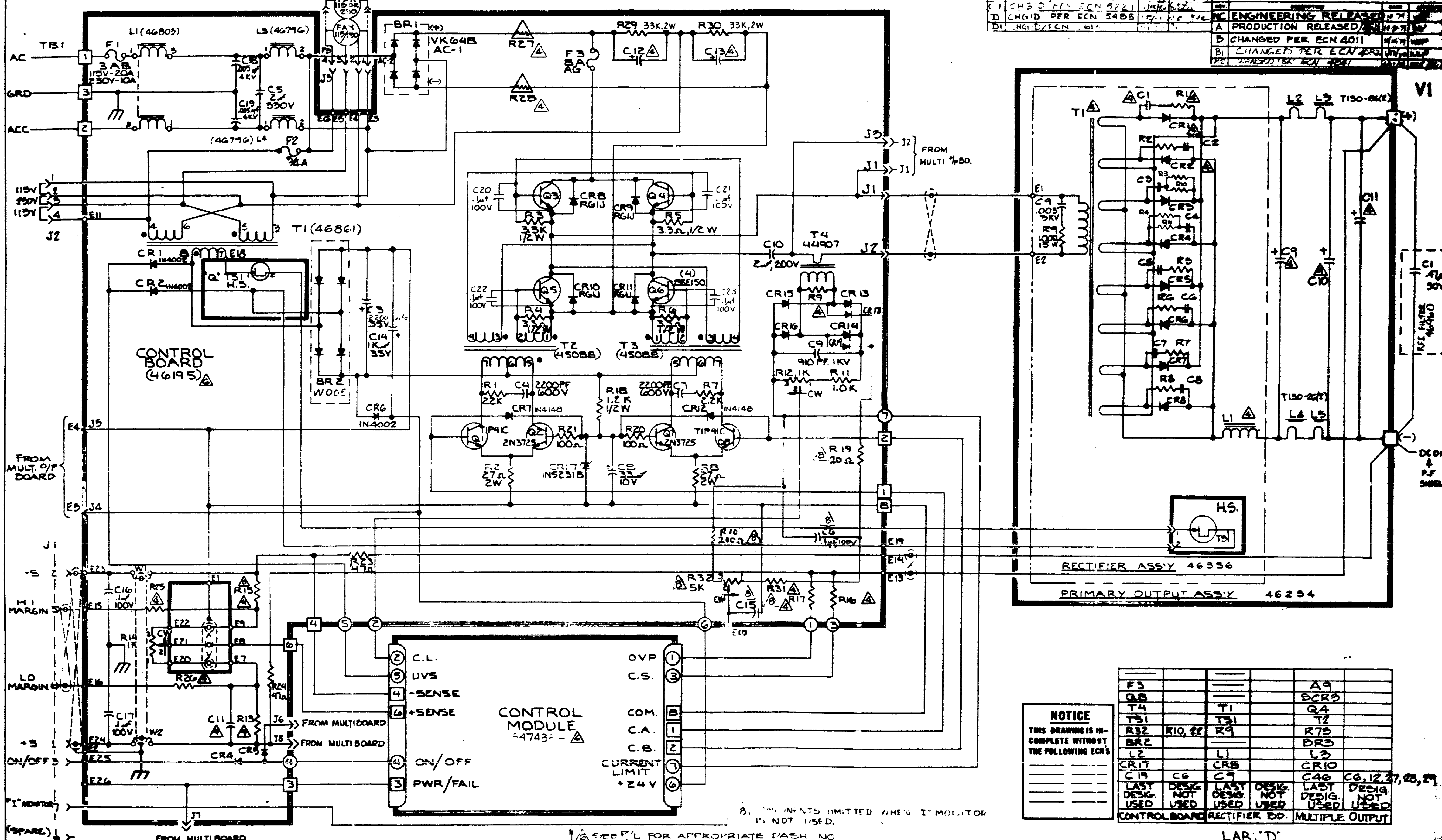
SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCH DIA

SCALE
DWG NO. DS21E252
WGHT
SHT 16 OF 16 SHTS

Power Supply

REV.	DESCRIPTION	DATE	APPROVED
NC	ENGINEERING RELEASED	[illegible]	[illegible]
A	PRODUCTION RELEASED	[illegible]	[illegible]
B	CHANGED PER ECN 4011	[illegible]	[illegible]
B1	CHANGED PER ECN 4082	[illegible]	[illegible]
B2	CHANGED PER ECN 4[illegible]	[illegible]	[illegible]
C	CHG'D/ECN [illegible]	[illegible]	[illegible]
C1	CHG'D PER ECN 5221	[illegible]	[illegible]
D	CHG'D PER ECN 5485	[illegible]	[illegible]
D1	CHG'D/ECN [illegible]	[illegible]	[illegible]



NOTICE

THIS DRAWING IS INCOMPLETE WITHOUT THE FOLLOWING ECN'S

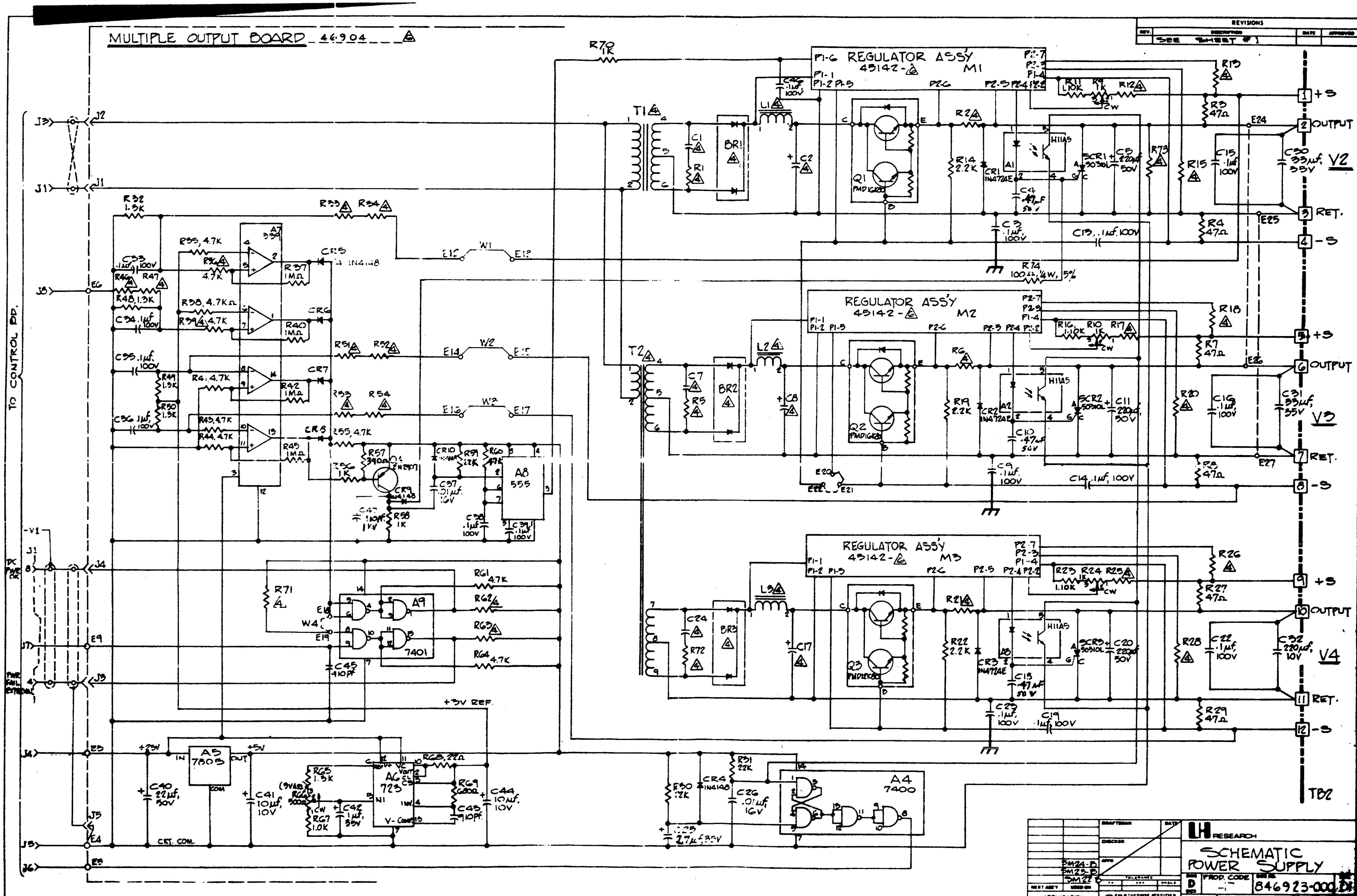
—		—			
F3		—		A9	
Q8		—		SCR3	
T4		T1		Q4	
TS1		TS1		T2	
R32	R10, 22	R9		R75	
BR2		—		BR3	
L2		L1		L3	
CR17		CR8		CR10	
C19	C6	C9		C46	C6, 12, 27, 28, 29
LAST DESIG. USED	DESIG. NOT USED	LAST DESIG. USED	DESIG. NOT USED	LAST DESIG. USED	DESIG. NOT USED
CONTROL BOARD		RECTIFIER BD.		MULTIPLE OUTPUT	

LAR: "D"

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ○ THIS SYMBOL INDICATES P1, □ THIS SYMBOL INDICATES P2 CONTROL MODULE.
2. ALL DIODES ARE IN4148.
3. △ THIS SYMBOL INDICATES COMPONENT NOT USED.
4. △ THIS SYMBOL INDICATES COMPONENT VARIES WITH OUTPUT VOLTAGE, FOR CORRECT VALUE SEE APPROPRIATE DASH NO.
5. ALL RESISTORS ARE 1/4 W 5%
6. △ SEE P/L FOR APPROPRIATE DASH NO.
7. A. FOR NORMAL OPERATION OF TWO INDEPENDENT SECONDARY OUTPUTS (V2 & V3); JUMPER E1 TO E2 - #22 BUSS.
   B. FOR PARALLEL OPERATION OF SECONDARY OUTPUTS (V2 & V3).
      1. DERATE TOTAL PARALLELED OUTPUT POWER TO 80%.
      2. JUMPER OUTPUTS; E24 TO E26 & E25 TO E27 - #16 GA. BUSS.
      3. JUMPER E21 TO E22, #22 GA BUSS.
   △ COMPONENTS NOT USED - REG MOD. # 2 C10, 19, SCR 2 & R18
8. COMPONENTS OMITTED WHEN "I" MONITOR IS NOT USED.

5M24-D	DRAFTSMAN T/N	DATE [illegible]	LH RESEARCH
5M23-D	CHECKED [illegible]	[illegible]	SCHEMATIC POWER SUPPLY
5M22-D	APPR. [illegible]	[illegible]	SIZE D
NEXT ASSY / USED ON	TOLERANCE	PRODUCT CODE 47	DWG NO. 846923-[illegible] REV D
APPLICATION	UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES	SCALE 1/1	SHEET [illegible]


MULTIPLE OUTPUT BOARD 46904
REVISIONS
SEE SHEET #1
REGULATOR ASSY 45142- M1
REGULATOR ASSY 45142- M2
REGULATOR ASSY 45142- M3
T1
T2
BR1
BR2
BR3
H11A5
A8 555
A9 7401
A5 7805
A6 723
A4 7400
TO CONTROL BD.
+5V REF.
+S
OUTPUT
RET.
-S
V2
V3
V4
TB2
LH RESEARCH
SCHEMATIC POWER SUPPLY
PROD. CODE
846923-000
APPLICATION

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