

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

OCTOBER 1976



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MAGNETIC BUBBLE SYSTEMS APPROACH PRACTICAL USE

SOFTWARE SUPPORT FOR MICROPROCESSORS POSES NEW DESIGN CHOICES

CLEARING UP THE CONFUSION: VIRTUAL VS MEMORY MAPPING

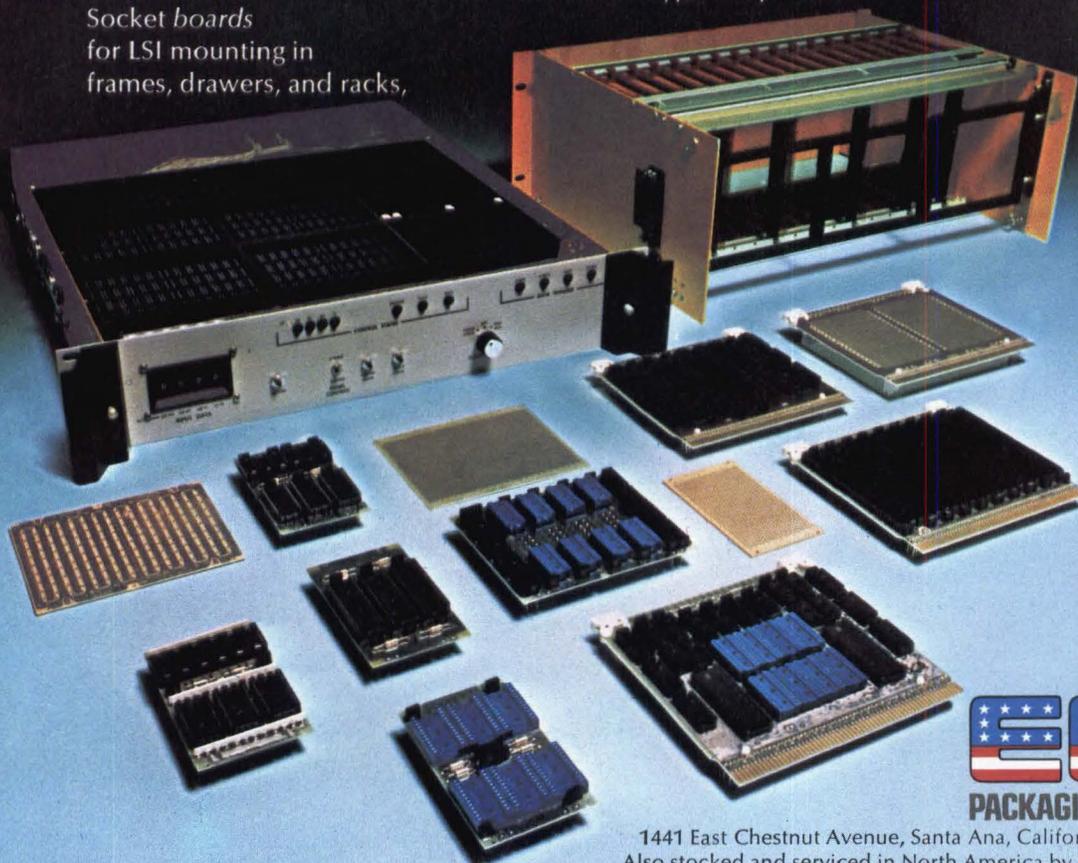
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REP	YR	CUST CODE	INVOICE	DATE	S.O. NO	AREA	TOTAL INVOICE	REP. NO.	DT	NOTES
00731	AA	TAD05	IN38259	11/08/74	14482-1	58	1,500.00			1103
00732	AC	1 NODEL BP30-24V			4	375.00				1103
00733						2-11201	1,500.00			1103
00742						2-11410	276.00-			1103
00743						2-11411	484.00-			1103
00744						2-11400	592.00-			1103
00747						2-11601	108.00-			1103
00740						R/DTY=603300004 58 2-46000	2,000.00-			1103
00741						R/DTY=603300004 58 2-46008	500.00			1103
00744						R/DTY=603300004 2-56001	276.00			1103
00745						R/DTY=603300004 2-56002	484.00			1103
00746						R/DTY=603300004 2-56003	592.00			1103
00749						R/DTY=603300004 2-56004	108.00			1103
TOTAL INVOICE IN38259										
00750	AA	TAD05	IN38260	11/08/74	14423	3	834.00			1103
01191	AC	1 NODEL BP30-48V PERFORATOR			2	375.00				1103
00751						2-11201	750.00			1103
00754						2-11410	114.00-			1103
00755						2-11411	252.00-			1103
00758						2-11600	246.00-			1103
00759						2-11601	84.00-			1103
00752						R/DTY=603300002 58 2-46000	1,000.00-			1103
00753						R/DTY=603300002 58 2-46008	250.00			1103
00756						R/DTY=603300002 2-56001	114.00			1103
00757						R/DTY=603300002 2-56002	232.00			1103
00760						R/DTY=603300002 2-56003	246.00			1103
00761						R/DTY=603300002 2-56004	34.00			1103
TOTAL INVOICE IN38261										
00762	AA	N0999	IN38262	11/08/74	14623	3	834.00			1103
01194	AC	1 DRIVE ELECTRONICS			1	294.00				1103
00763	AC	1 E D T OPTION			1	40.00				1103
01192	AC	1 NODEL BP30-48V			1	500.00				1103
00762						2-11201	834.00			1103
00763						2-11410	78.00-			1103
00764						2-11411	181.00-			1103
00774						2-11600	167.00-			1103
00775						2-11601	39.00-			1103
00764	BLN=PLG	CR=1980	INVTOT=00008360			2-21401	129.10-			1103
00764						R/DTY=103300001 03 2-40000	300.00-			1103
00770						R/DTY=103400001 03 2-40000	324.00-			1103
00771						R/DTY=103300001 2-50001	35.00			1103
00772						R/DTY=103400001 2-50001	22.00			1103
00773						R/DTY=103300001 2-50002	124.00			1103
00774						R/DTY=103400001 2-50002	87.00			1103
00775						R/DTY=103300001 2-50003	118.00			1103
00776						R/DTY=103400001 2-50003	49.00			1103
00778						R/DTY=103300001 2-50004	27.00			1103

THE MAGAZINE OF DIGITAL ELECTRONICS

COMPUTER DESIGN

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Magnetic bubble memories possess many characteristics which suit them to applications that range from microcomputer mass memories to electronic discs for mainframe computers

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There are numerous alternative methods available for use in generating microprocessor software, but careful thought and planning permit the design engineer to select the most advantageous for his problem

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Although confusion reigns regarding virtual and mapped memories, problems of what each does and does not provide can be cleared up by study of how they are implemented

106 A METHOD OF HIGH DENSITY RECORDING ON FLEXIBLE MAGNETIC DISCS

by Robert C. Franchini and Donald L. Wartner

Since flexible discs now operate at high densities, the best way to increase the amount of data recorded is with a better encoding scheme which offers the greatest system margin and data handling reliability

110 NEW ERROR-CORRECTING TECHNIQUE FOR SOLID-STATE MEMORIES SAVES HARDWARE

by Gary R. Basham

Implemented with less hardware and less impact on throughput, an improved code uses a new technique of check-bit generation, while retaining the same error correction and detection capabilities of other codes

140 PORTABLE CRT PANEL PERFORMS ONLINE DEBUGGING AND EDITING OF PROGRAMMABLE CONTROLLERS

Control engineers can develop and program multiple-element circuits directly from their relay ladder diagrams on this universal programming panel, without disturbing operation of the associated programmable controller

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Prints 3 lines per second, 11 character locations per column with a capacity up to 16 columns. Print mechanism is small (5¼" x 10" x 8").

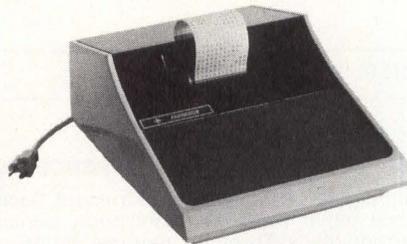
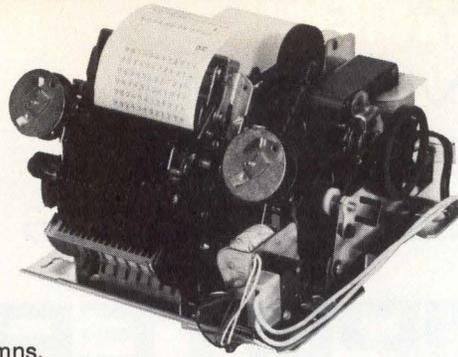
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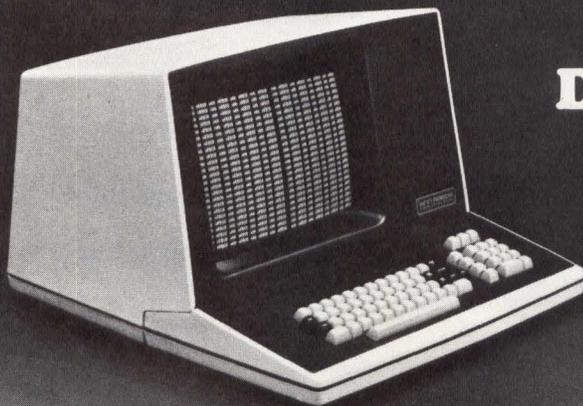
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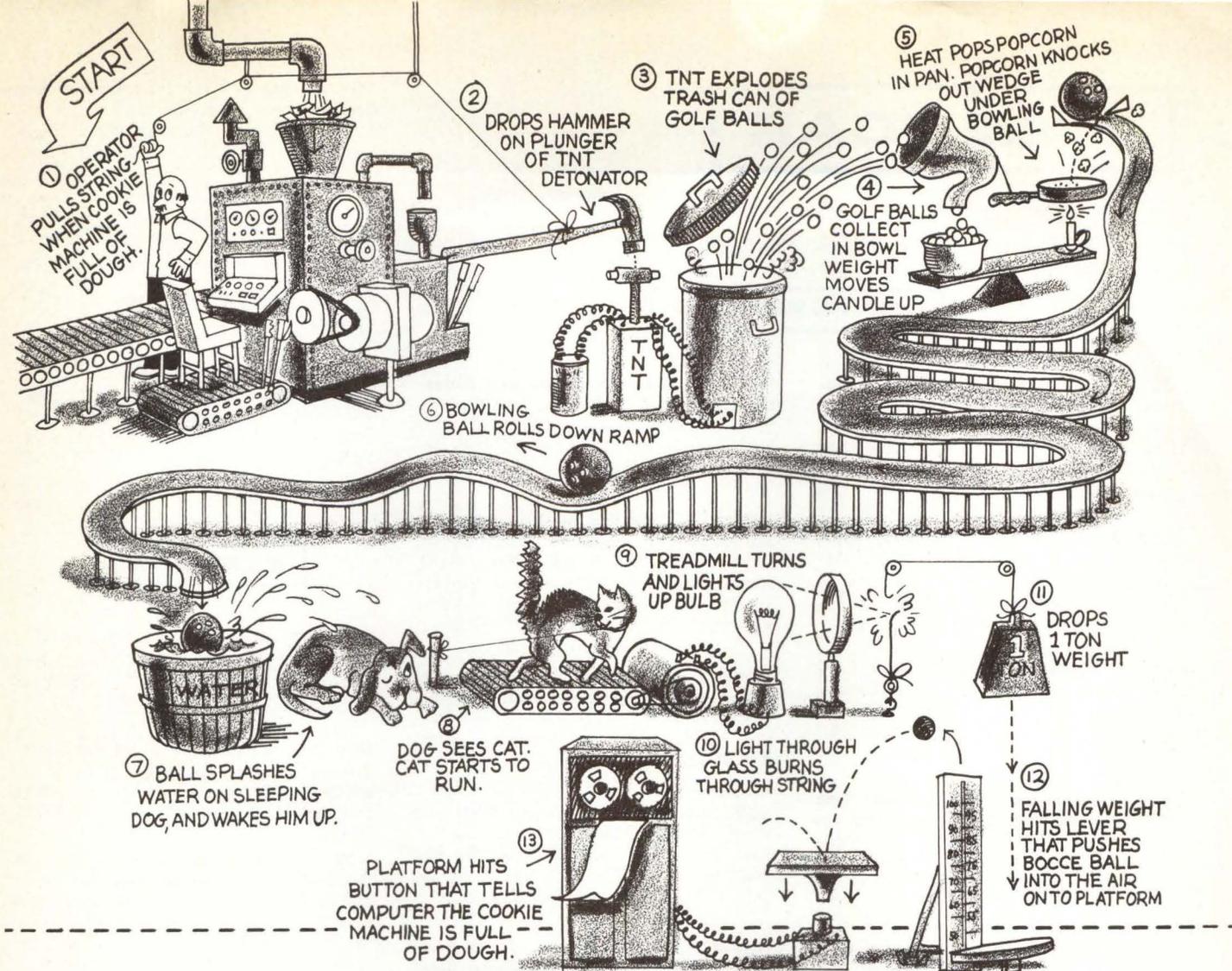
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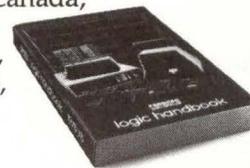
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CONFERENCES

OCT 19-21—IEEE Semiconductor Test Equipment Sym, Cherry Hill Inn, Cherry Hill, NJ. INFORMATION: Annual Test Symposium Committee, IEEE Philadelphia Section, U of Pennsylvania, Moore School of EE, Philadelphia, PA 19174

OCT 20-21—9th Annual Connector Sym, Hyatt House, Cherry Hill, NJ. INFORMATION: Electronic Connector Study Group, Inc, PO Box 1428, Camden, NJ 08101. Tel: (609) 424-4014

OCT 21-22—IEEE Canadian Conf on Communications and Power, Montreal, Canada. INFORMATION: Jean Jacques Archambault, Chm, IEEE Conf, CP/PO 958, Succ "A," Montreal, Quebec H3C 2W3 Canada

OCT 24-27—Info/Expo '76, Internat'l Data Processing Conf and Business Exposition, Las Vegas Hilton, Las Vegas, Nev. INFORMATION: Data Processing Management Assoc, 505 Busse Highway, Park Ridge, IL 60068. Tel: (312) 825-8124

OCT 25-27—17th Annual Sym on Foundations of Computer Science, Houston, Tex. INFORMATION: Prof Michael J. Fischer, Program Chm, Dept of Computer Science, FR-35, U of Washington, Seattle, WA 98195

OCT 26, OCT 28, NOV 18, and JAN 18—1976/77 Invitational Computer Conferences, Chicago, Ill; Minneapolis, Minn; Dallas, Tex; and Orange County, Calif. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 204, Newport Beach, CA 92660. Tel: (714) 644-6037

NOV 1-3—Cybernetics and Society Internat'l Conf, Mayflower Hotel, Washington, DC. INFORMATION: W. H. vonAlven, FCC, 1919 M St, NW, Washington, DC 20554

NOV 8-9—ISA Instrument Show, Toronto, Canada. INFORMATION: R. G. Wirth, Show Chm, c/o Fluidynamic Devices Ltd, 3216 Lenworth Dr, Mississauga, Ontario L4X 2G1 Canada

NOV 8-11—Third Internat'l Joint Conf on Pattern Recognition, Hotel Del Coronado, Coronado, Calif. INFORMATION: A. Rosenfeld, U of Maryland, Computer Science Center, College Park, MD 20742

NOV 8-11—Mini and Microcomputers, Hotel Toronto, Toronto, Canada. INFORMATION: Mini and Microcomputers—Hamza, PO Box 3243, Station B, Calgary, Alberta T2M 4L8 Canada

NOV 8-12—Computer Performance Evaluation Users Group, San Diego, Calif. INFORMATION: Dick Dunlavey, A265 Technology Bldg, National Bureau of Stds, Washington, DC 20234. Tel: (301) 921-3485

NOV 8-12—Exhibition of U.S. Computers and Peripheral Equipment, U.S. Trade Center, Sydney, Australia. INFORMATION: Irwin D. Nathanson, Office of International Marketing, DIB-233, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-4957

NOV 9-11—Government Microcircuit Applications Conf, Lake Buena Vista, Fla. INFORMATION: Konrad H. Fischer, Conf Chm, U.S. Army Electronics Command, Attn: AMSEL-TL-IC, Fort Monmouth, NJ 07703

NOV 10-12—Automatic Testing Conf, Fort Worth, Tex. INFORMATION: G. C. Sumner, Sym Gen'l Chm, General Dynamics, PO Box 748, Mail Zone 2420, Fort Worth, TX 76101. Tel: (817) 732-4811, X4258/4259

NOV 15-18—CAD/CAM IV (Fourth Computer-Aided Design and Computer-Aided Manufacturing Conf and Exposition), Dallas Hilton Hotel, Dallas, Tex. INFORMATION: CAD/CAM IV, Society of Manufacturing Engineers, 20501 Ford Rd, PO Box 930, Dearborn, MI 48128

NOV 17—Trends and Applications: Computer Networks, Gaithersburg, Md. INFORMATION: Marshall Abrams, B212 Technology Bldg, National Bureau of Stds, Washington, DC 20234. Tel: (301) 921-2601

NOV 23-25—COMPEC'76 (Computer Peripheral, Small Computer, and Systems Exhibition), Wembley Conf Centre, Wembley, Middlesex, England. INFORMATION: Trident Conferences and Exhibitions Ltd, Abbey Mead House, 23a Plymouth Rd, Tavistock, Devon PL19 8AU England

NOV 23-27—Conf-Exhibition of Automation and Instrumentation, Milan, Italy. INFORMATION: Federation of Scientific and Technical Associations, Piazzale Rodolfo Morandi, 2 (Piazza Cavour)-20121 Milano, Italy

NOV 25-DEC 1—electronica 76 (7th Internat'l Trade Fair for Components and Production Facilities), Munich Fairgrounds, Munich, Germany. INFORMATION: Münchener Messe- u. Ausstellungsgesellschaft mbH, München 12, Postfach 12 10 09, Messengelände, Germany

NOV 29-DEC 1—Nat'l Telecommunications Conf, Fairmont Hotel, Dallas, Tex. INFORMATION: J. H. Tilley, Gen Chm, Collins Radio Group, 1200 N Alma Rd, Richardson, TX 75080

DEC 6-8—Winter Simulation Conf, Nat'l Bureau of Stds, Gaithersburg, Md. INFORMATION: Dr Harold J. Highland, Chm, Data Processing Dept, State U Technical College, Farmingdale, NY 11735. Tel: (516) 420-2190

DEC 6-8—IEEE International Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. INFORMATION: C. Neil Berglund, Bell-Northern Research, POB 3511, Station C, Ottawa, Ontario K1Y 4H7 Canada

SEMINARS

OCT 29-30—Microprocessors, U of Nebraska, Lincoln. INFORMATION: Jim Hanna, Nebraska Public Power, PO Box 499, Columbus, NE 68601. Tel: (402) 564-8561

NOV 3-5—Workshop on Distributed Fault-Tolerant Computer Systems, San Juan, PR. INFORMATION: Jack Goldberg, SRI, Menlo Park, CA 94025. Tel: (415) 326-6200, X2784

NOV 4-6—Workshop on Operating and Database Management Systems, Northwestern U, Evanston, Ill. INFORMATION: Prof E. J. McCauley III, Program Chm, Center for Advanced Computation, U of Illinois, Urbana, IL 61801. Tel: (217) 333-4910

NOV 8-11—Internat'l Purdue Workshop on Industrial Computer Systems, Purdue U, West Lafayette, Ind. INFORMATION: Dr T. J. Williams, 102 Michael Golden, Purdue U, West Lafayette, IN 47907. Tel: (317) 494-8425

SHORT COURSES

OCT 26-28, NOV 2-4, NOV 9-11, and NOV 16-18—Designing with Microprocessors, Alexandria, Va; Philadelphia, Pa; Indianapolis, Ind; and Denver, Colo. INFORMATION: Edwin Lee, Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940

OCT 30—Microprocessors, NOV 12-13—Microcomputers and Minicomputers, Santa Monica, Calif. INFORMATION: Educational Registrar, IEEE, 445 Hoes Lane, Piscataway, NJ 08854

NOV 3-5—Minicomputer Systems; NOV 15-17 and DEC 15-17—Applied Data Communications Design, Washington, DC; Washington, DC, and Chicago, Ill. INFORMATION: The Institute for Professional Education, Suite 601, 1901 N Fort Myer Dr, Arlington, VA 22209. Tel: (703) 527-8700

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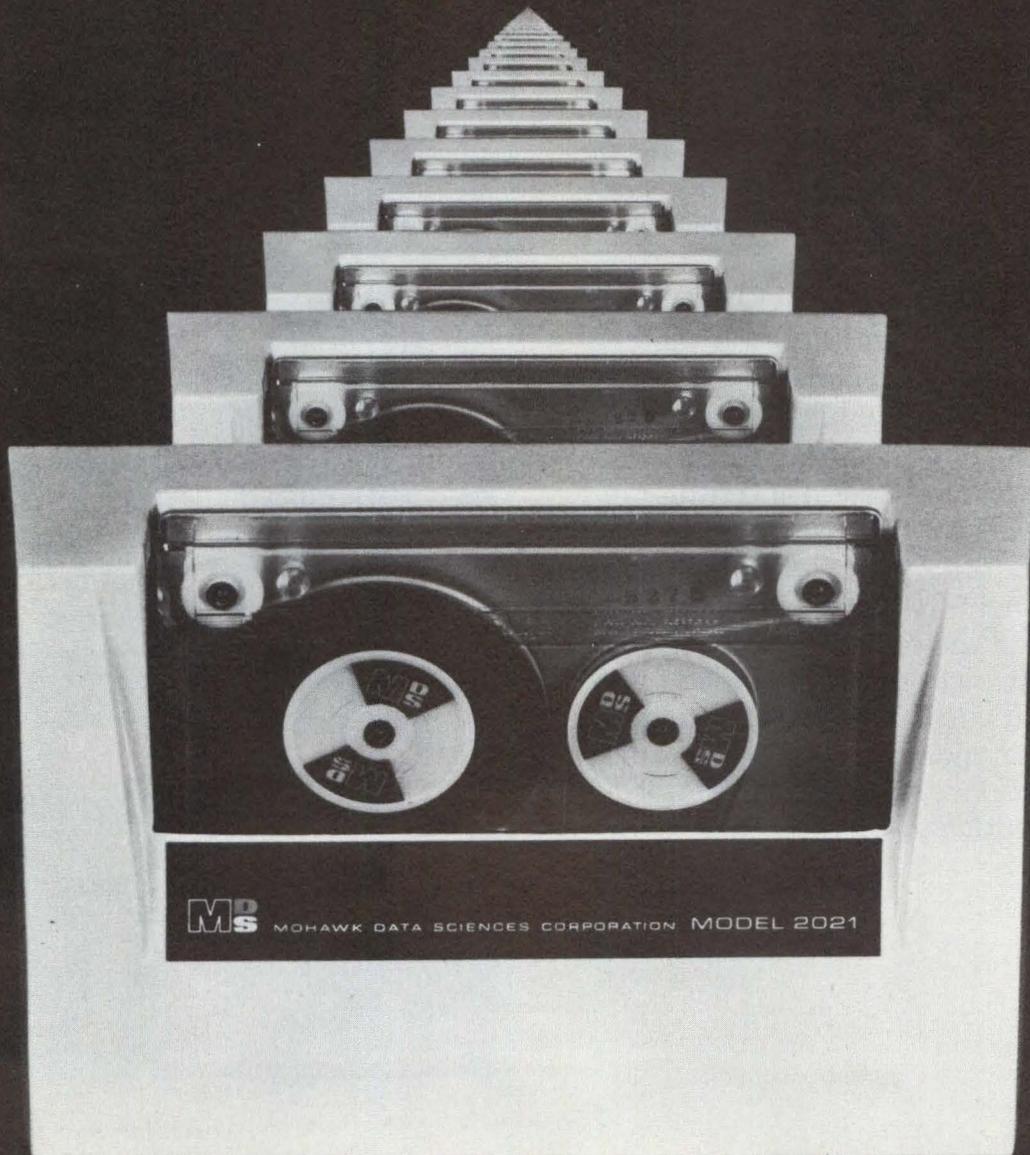
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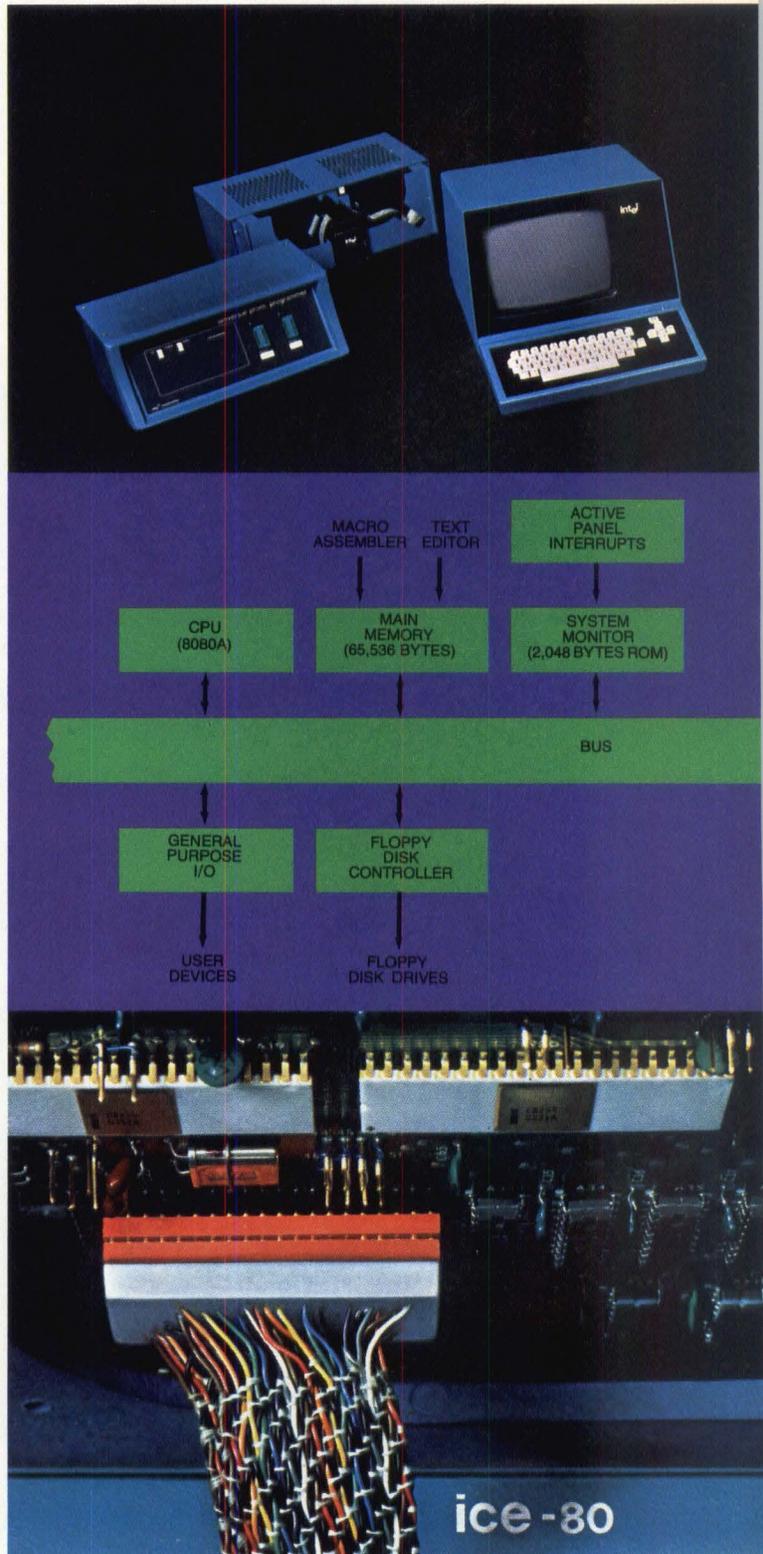
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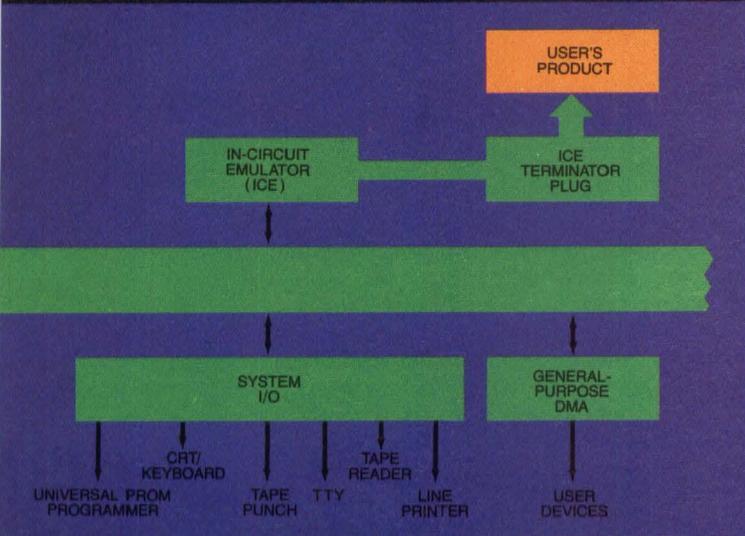
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lets you see what your it's still on the bench.



```
*GO FROM START UNTIL RSLT WRITTEN
EMULATION BEGUN

*DISPLAY CYCLES
STAT-ADR-DATA STAT-ADR-DATA STAT-ADR-DATA S
A2H-1326H-CDH 82H-1327H-E3H 82H-1328H-01H 0

*CHANGE DOUBLE REGISTER SP=13FFH
*BASE HEX
*EQUATE STOP=1333H
*GO FROM START UNTIL STOP EXECUTED THEN DUMP
EMULATION BEGUN
B=01H C=41H D=00H E=00H H=00H L=00H F=56H A=
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by **John E. Buckley**
Telecommunications Management Corp
Cornwells Heights, Pa.

Computer Communications Inquiry

In addition to the more mundane activities, Bicentennial Year 1976 will be noted for significant communications developments which will directly shape the future of telecommunications information systems. For instance, Congressional legislation has been proposed to replace the Communications Act of 1934, the cornerstone of the various FCC decisions and rulings that have permitted the present maturation of telecommunications in the United States (see "Implications of the Communications Reform Act," "Communication Channel," *Computer Design*, Sept 1976, pp 14, 19). In addition, the FCC announced in August that it was initiating a new inquiry into the use of computers by communications common carriers to provide information services.

This latest inquiry can be considered an updating of the FCC's 1971 Computer/Communications Inquiry decision which established the policy of separation for regulated communications services and nonregulated data processing services when provided by the same organization. The original decision, however, did not define "data processing" and "communications" in a manner that is totally pertinent to today's information environment, something the new inquiry is intended to do.

At the time of the original inquiry, data processing service organizations questioned the legitimacy of a regulated communications common carrier also providing data processing services as a nonregulated service. Their argument was that in such an organization it would be a relatively simple accounting procedure to permit revenues from the regulated communications services to subsidize the nonregulated data processing services. Subsidized data processing services could then be priced at a level that would destroy competition from independent data processing service companies.

A number of policies were established as a result of that earlier inquiry. The FCC ruled that communications common carriers could provide nonregulated data processing services but only by a totally separate subsidiary organization with individual accounting. In this context,

however, the FCC ruled that AT&T and its associated operating companies were prohibited from marketing any data processing services even though they were a subsidiary organization by virtue of the existing AT&T Consent Decree of 1955. In that Consent Decree, a settlement between AT&T and the U.S. Department of Justice resulting from an antitrust action, AT&T and its associated operating companies agreed not to participate in or provide any services or products that were not exclusively communications.

Revision of any of the 1971 decisions is not necessarily intended; the purpose of the inquiry is to specifically establish the definition of "data processing." The extent to which data processing services were defined by the FCC was limited to a basic distinction between message switching and data processing applications. It was ruled that message switching was primarily communication and, therefore, within the jurisdiction of the regulated common carriers. Independent data processing service organizations were prohibited from providing message or data switching services. This created considerable concern among data processing service companies offering time-sharing and interactive capabilities.

If a number of data collection terminals transmit source data to a common data base at the data processing service company and that data base is then transmitted to the customer's computer for analysis and processing, the procedure is primarily data switching and not data processing. This can be easily rendered more arbitrary if the central processor modifies the collected data base by performing data reformatting or calculating summary statistics prior to transmission. The rhetorical question then centers on the purpose of this centralized processing: Is that processing necessary for the performance of the application or is it merely a superficial action to cloud the distinction between data processing and data switching?

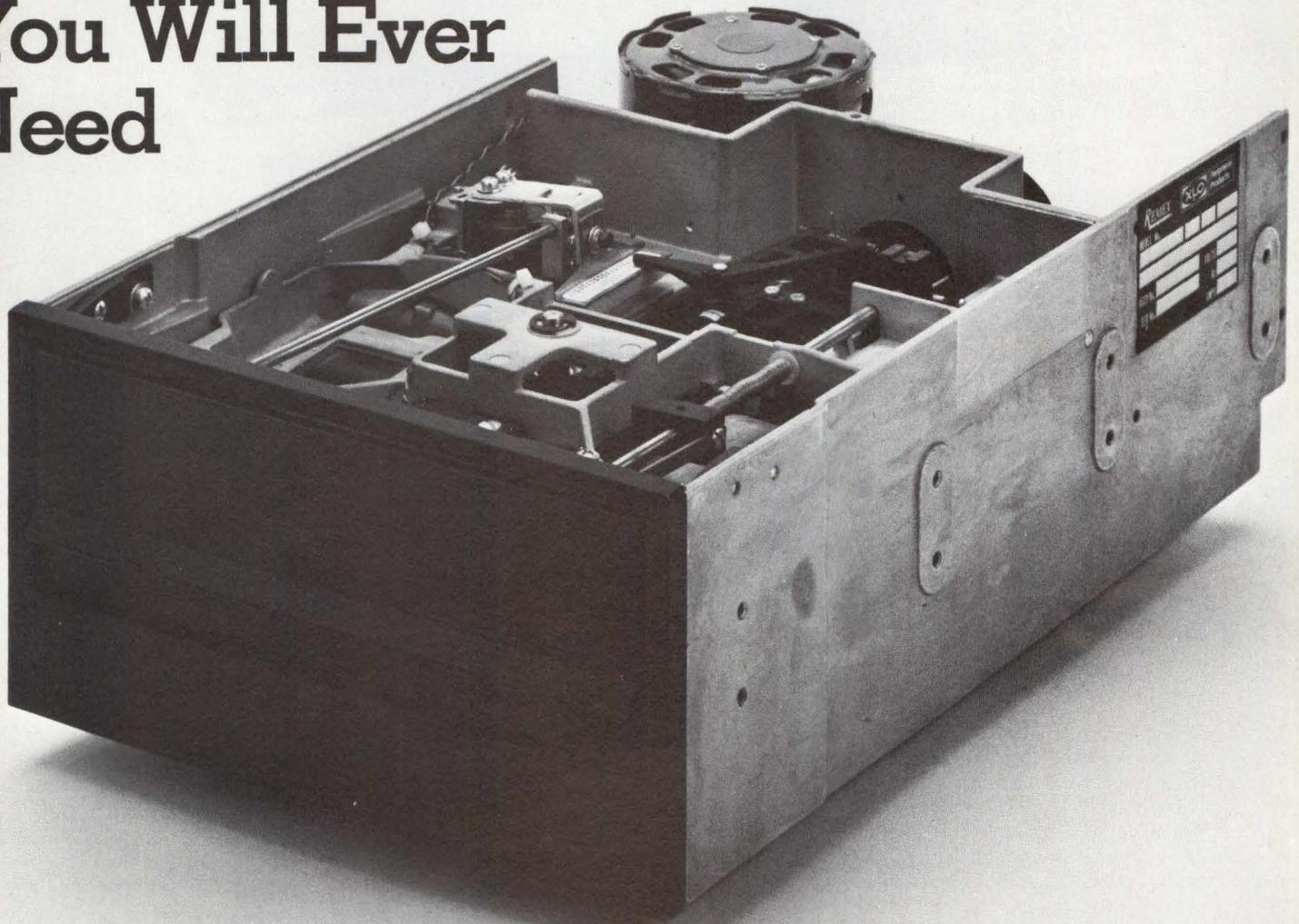
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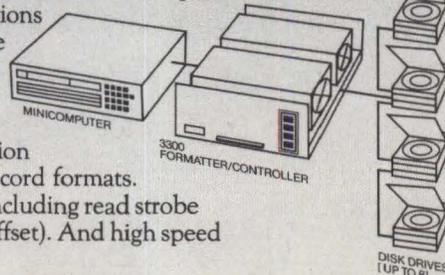


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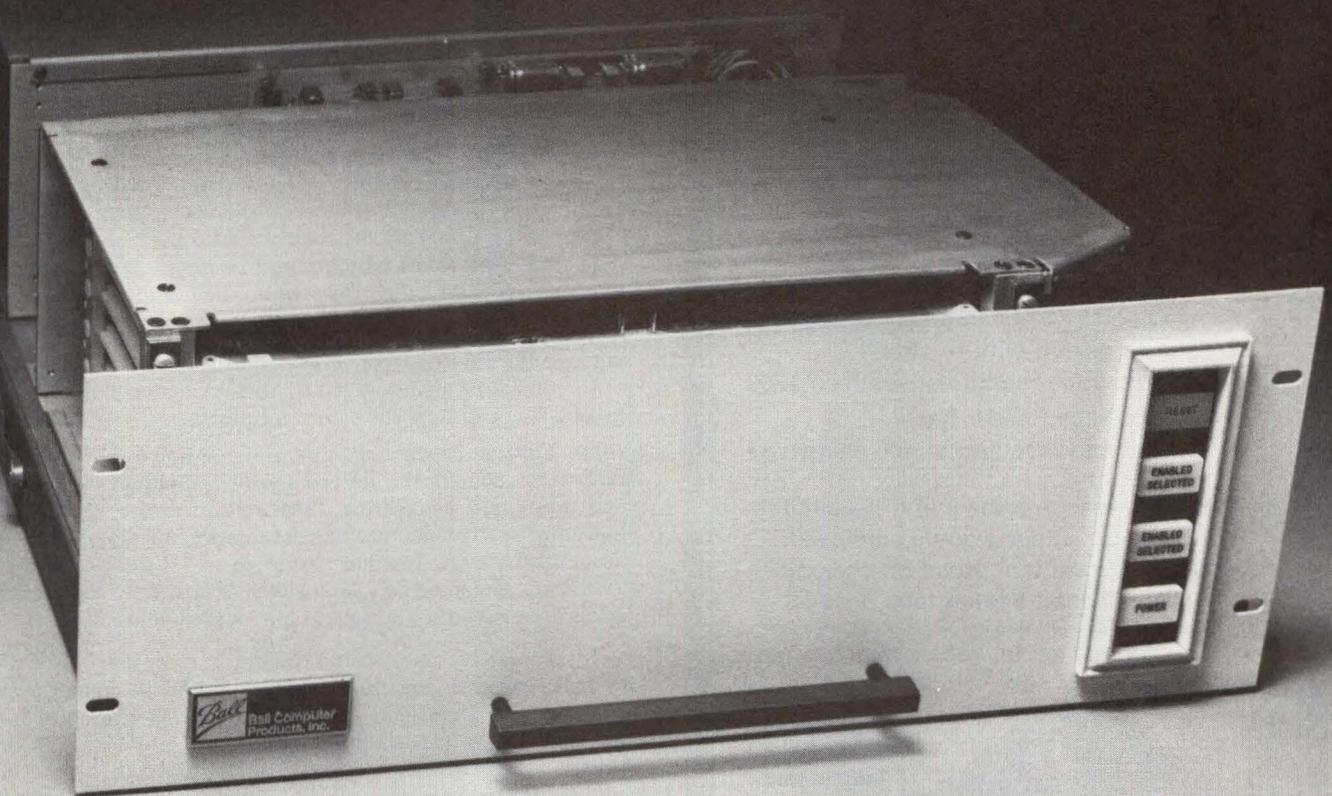


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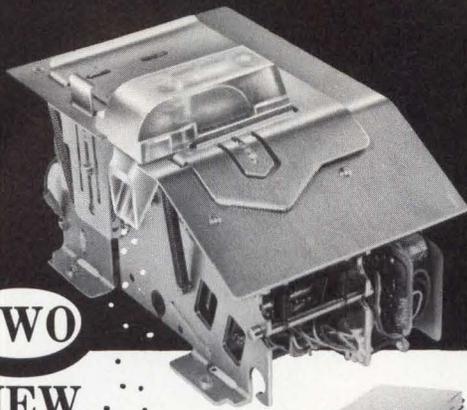
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computer networks coupled with the technological and economic advances of mini and microcomputer systems were cited as the major reasons for re-examining this area. Rapid evolution of these applications has rendered the 1971 distinctions between data processing and message switching applications as obsolete as the FCC's 1936 definitions of voice and record communication, established in an attempt to delineate between AT&T and Western Union business areas.

New rulings proposed by the FCC would eliminate the classification of an application as predominantly either communications or data processing when both functions were present. Data processing would be defined as using a computer for processing information, as well as where the semantic content or meaning of the original input data is changed or where the output data are a programmed response to input data. The FCC has also suggested at least three more specific types of data processing applications, including:

Arithmetic Processing—general commercial accounting, payroll, inventory control, banking, point-of-sale processing, financial and econometric modeling

Word Processing—interactive information retrieval systems, management information systems, text editing, translation, typesetting

Process Control—computer monitoring and control of a continuously occurring process, such as nuclear powered generating stations, electric power distribution grid, automatic machine tools, fire detection and control systems

Communications common carriers would be prohibited from providing such data processing services except by a totally separated and isolated subsidiary having different accounting, personnel, officers, and computer facilities.

Computer applications that would not be considered data processing, and which could be provided by a communications common carrier, would include:

Network Control and Routing—message and circuit switching, speed and code conversion, pulse format conversion, error control procedures, A-D and D-A conversions, signal processing, and time division multiplexing

Input/Output Processing—providing a network computer that will reconcile the differences of individual computers and terminals by editing, format conversion, and data buffering so that compatible data communications can be accomplished. A familiar example is Western Union's TWX/TELEX; conversion exclusivity of non-data processing applications would appear to be a valid conclusion

In the latter case, stored program computerized PBX systems could be concluded to be limited to communications common carriers. This would have a profound impact on the private telephone system (interconnect) industry. Also, the clear intention to separate data processing applications as the result of this inquiry will impact some of the plans of AT&T for its No. 4 Electronic Switching System. AT&T has been considering sharing a common No. 4 ESS to not only provide traditional voice switching services but also to provide data processing applications using its transaction terminal.

The FCC is soliciting comments on its proposed new rules by October 12, 1976 with reply comments targeted by November 11, 1976. A complete copy of this proposed inquiry can be obtained from the FCC in Washington, DC by requesting the proposal for Docket 20828. It is important that all parties interested in the outcome of this inquiry make their views known to the FCC.

The Contortionist.



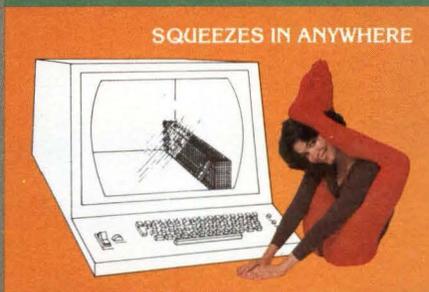
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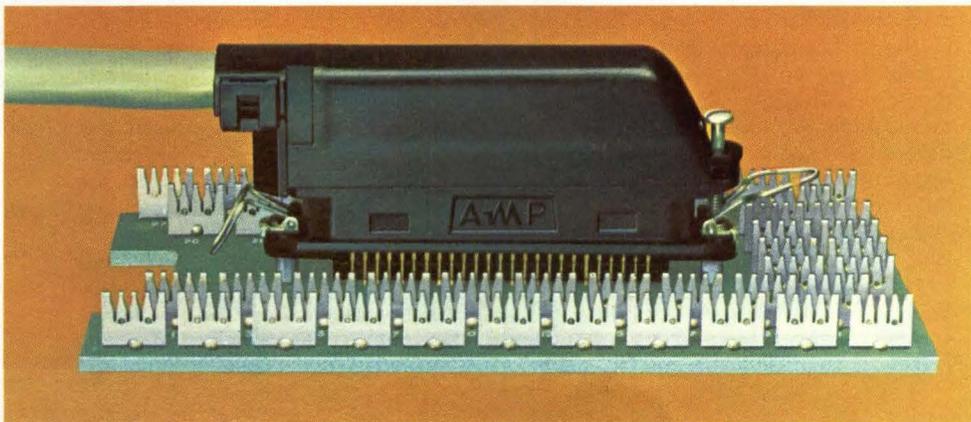
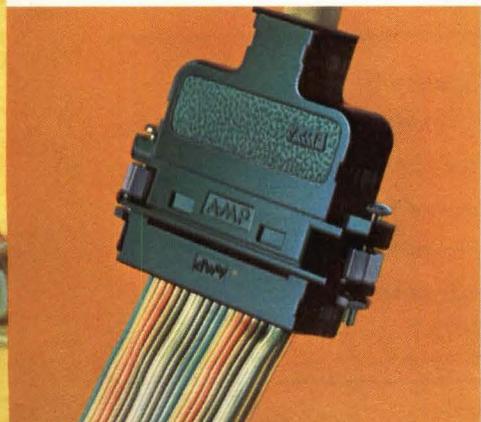
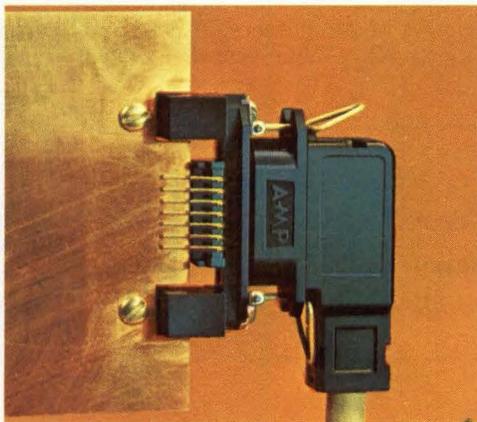
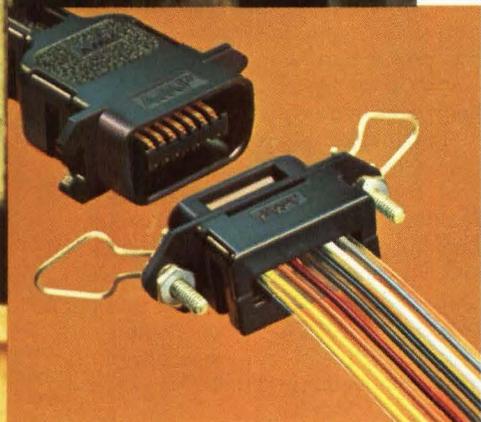
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Editor's Note: As another move in the continuing effort to provide our readers with key information in all areas of digital electronics, this month we are expanding the "Communication Channel" section. In addition to regular commentary by Mr Buckley, this section will include data communications information of particular value and interest to *Computer Design* readers.

Some months the content may be in the form of a conference summary—as it is this month. On other occasions it may discuss related technological advances or data communications industry news—or it may be a combination of any of these. In every case, however, the content will be chosen with our readers in mind.

International Council Shares Computer Communication Problems and Solutions

Sponsored by The International Council for Computer Communication and hosted by Trans-Canada Telephone System, the Third International Conference on Computer Communication (ICCC-76) was held in Toronto, Ontario from August 3 to 6. The aura was truly international with papers on "Advancement Through Resource Sharing" from diverse countries such as England, Australia, France, Japan, Germany, Norway, Sweden, Austria, Italy, and Switzerland, and with the Conference Inaugural address given by the Ambassador of Iran to Canada—Professor of Electrical Engineering at McGill University and Honorary Professor at Carleton University—Dr F. Reza. By far the preponderance of papers, however, were presented by speakers from companies in the U.S. and Canada.

FCC Chairman Discusses Policies and Predictions

Although not listed as the "keynote" address, the presentation with probably the most overall interest was given by Richard E. Wiley, Chairman of the U.S. Federal Communications Commission (FCC). Ostensibly, his theme was the role of computer communications in improving our standard of living—and a number of interesting and valid points along that line were offered. However, the discussion rapidly evolved to his central topic—current U.S. policies toward data communications, in particular the official FCC position concerning competition among manufacturers of related equipment. The

American Telephone and Telegraph Co and its lobby for passage of the Consumer Communications Reform Act of 1976 were never specifically mentioned, but there was little doubt that both were at the heart of the analysis.

According to Wiley, "future improvements in our standard of living depend upon our ability to produce, process, disseminate, and use information in a more efficient fashion" and gains in these areas depend upon developments in the merged technologies of computers and communications. He pointed out that 46% of

"... about 46% of our Gross National Product is devoted to ... information goods and services."

our Gross National Product—the oft-mentioned and mysterious GNP—constitutes production, processing, or distribution of information goods and services, with about half of that involving "market-type" information activities. His estimate is that more than half of our total wages are earned in areas of that information sector.

Since this sector revolves about the telecommunications industry, further development depends upon evolution of the industry—especially the area of computer communica-

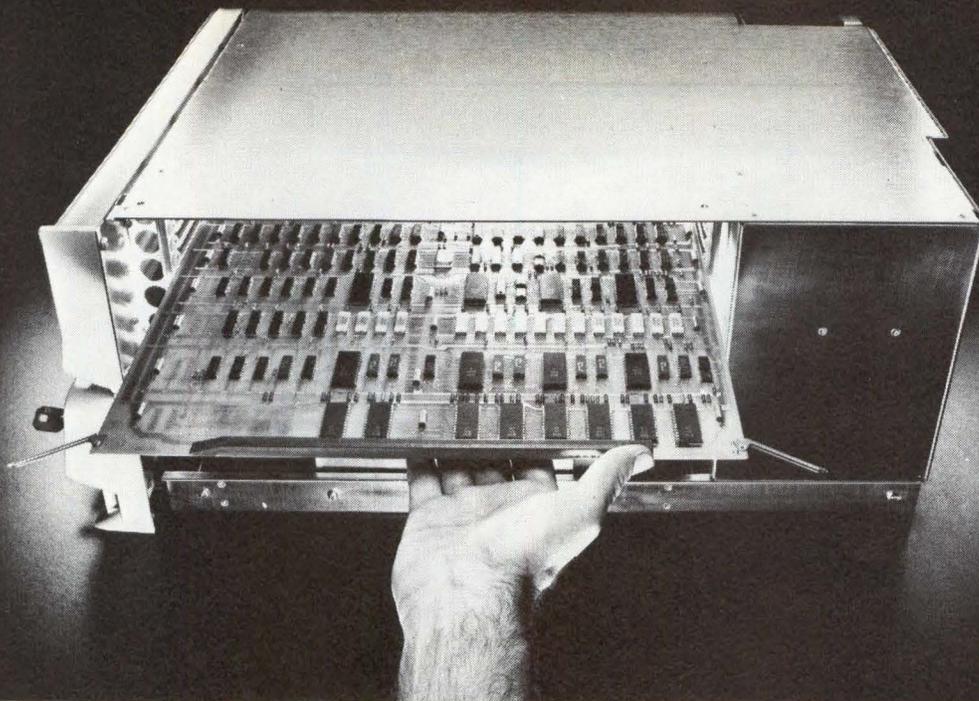
tions. Two general areas that are likely to benefit heavily from technological improvements are office automation and home computer centers because both necessitate close ties to the telephone network.

Although U.S. policies toward data communications apply to other specialized areas of common carrier communications, Wiley says they are of particular significance to computer communications. He characterized current FCC policies in a single word—freedom—in essence, to permit competition.

"If I had to characterize current FCC policies in a single word, I would choose the word freedom."

This competitive freedom "allows new terrestrial and satellite carriers to enter the data transmission market, . . . permits customers to connect their own properly certified terminal equipment directly to the lines of the established carriers, . . . authorizes entrepreneurs to lease basic transmission capacity from established carriers and to tailor that basic capacity to the specialized needs of their own customers, . . . lets otherwise unaffiliated users share private line services in order to take advantage of special rates or to gain network efficiencies, . . . sanctions subscribers to use the option of the international switched voice network for dataphone service, . . . and empowers established carriers to compete fully and fairly in the specialized data communications markets."

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These freedoms were provided through a series of basic FCC decisions, such as Carterfone, which in turn resulted from changes in electronic technology that occurred outside the control of the monopoly carriers and from dissatisfaction of specialized users with regular services offered by those carriers. (It is the subsequent "inevitable competition" that Wiley and the FCC believe are endangered by the Consumer Communications Reform Act, which—quoting from a letter from Wiley to the Chairman of the House Subcommittee on Communications¹—". . . will impede the development of the flexibility and options a national communications network can offer the American consumer.")

Although its policy is challenged by the legislation now in Congress, the FCC believes that "conscious flexibility" in data communications will permit economic and technical judgments of the marketplace to aid in deciding between packet and circuit switching, between satellite and terrestrial transmission, between general-purpose and specialized networks, and between different terminal devices.

Despite the admitted hazard of predicting the future in an area so intensely affected by changes in technology, Wiley ventured to outline

The effects of micro-processor and microcomputer developments "have put a severe strain on the definitions and rules that were laid down (by the FCC) in an era of centralized data processing and electromechanical switching."

the industry that he sees developing under current FCC policies. Foremost, he believes the massive local exchange and public message toll markets will continue to be supplied

on a monopoly basis—greatly stimulated by technological developments—but there will be extensive development of complex private, shared, and public networks for specialized applications. Possibly transmission, switching, multiplexing, network management, and other carrier supplied services will be unbundled, enabling users to form their own networks for those applications. Except for the

" . . . computer communications lies right at the very heart of mankind's next great advance in economic and social development."

possible supply of basic transmission capacity, specialized switching and other network services should be highly competitive—but that competition might not be extensive because of the costs involved.

Established carriers, as a result of their set market positions, will remain highly influential in most of the specialized markets, but they may find it advantageous to set up separate subsidiaries to compete in those markets. This would permit more speculative ventures, help prevent undesirable cross-subsidiaries, and minimize unnecessary extension of regulation.

Totally committed to the U.S./FCC policies, Wiley nevertheless recognizes that other countries, particularly those at different stages of economic and technological development and with different political and institutional interests, may choose different approaches. Development of increasingly important international computer communications networks

" . . . we must all intensify our efforts to coordinate international facilities to the fullest extent while respecting the policies and traditions of all countries concerned."

will necessitate full coordination of international facilities, while still respecting the policies and traditions of all concerned countries.

Another issue—currently under renewed study by the FCC—is the boundary between regulated common carrier activities and unregulated data processing. The investigation centers around regulations along the continuum from pure data processing to pure communications, and whether or not common carriers should be permitted to provide data processing services. Because of technological changes, a 1970 FCC decision on these "hybrid services" may no longer be realistic.

Large computers with relatively simple terminals are giving way to computer networks that include mini-computers, intelligent terminals, digital switches, and the application of microprocessors for multiplexing, error control, and signal processing, and in communications controllers and concentrators. Eliminating the "hybrid services" concept, the FCC proposes to define data processing as "the use of a computer for the purpose of processing information wherein: (a) the semantic content, or meaning, of input data is in any way transformed, or (b) where the out-

"I am entirely confident that there are adequate remedies available for dealing with any possible prospective adverse effects (of competition) long before they could occur."

put data constitute a programmed response to input data." The FCC hopes to set a regulatory boundary by defining data processing in positive terms rather than by exception as in the past.

Overall, Wiley stressed that the latitude must continue to exist which will permit contributions by everyone from the "largest corporation to the basement hobbyist." He believes that the "regulatory environment set up over the past 10 years in which basic telephone service is both protected and nurtured but which allows innovative contributions from all" should continue to exist but

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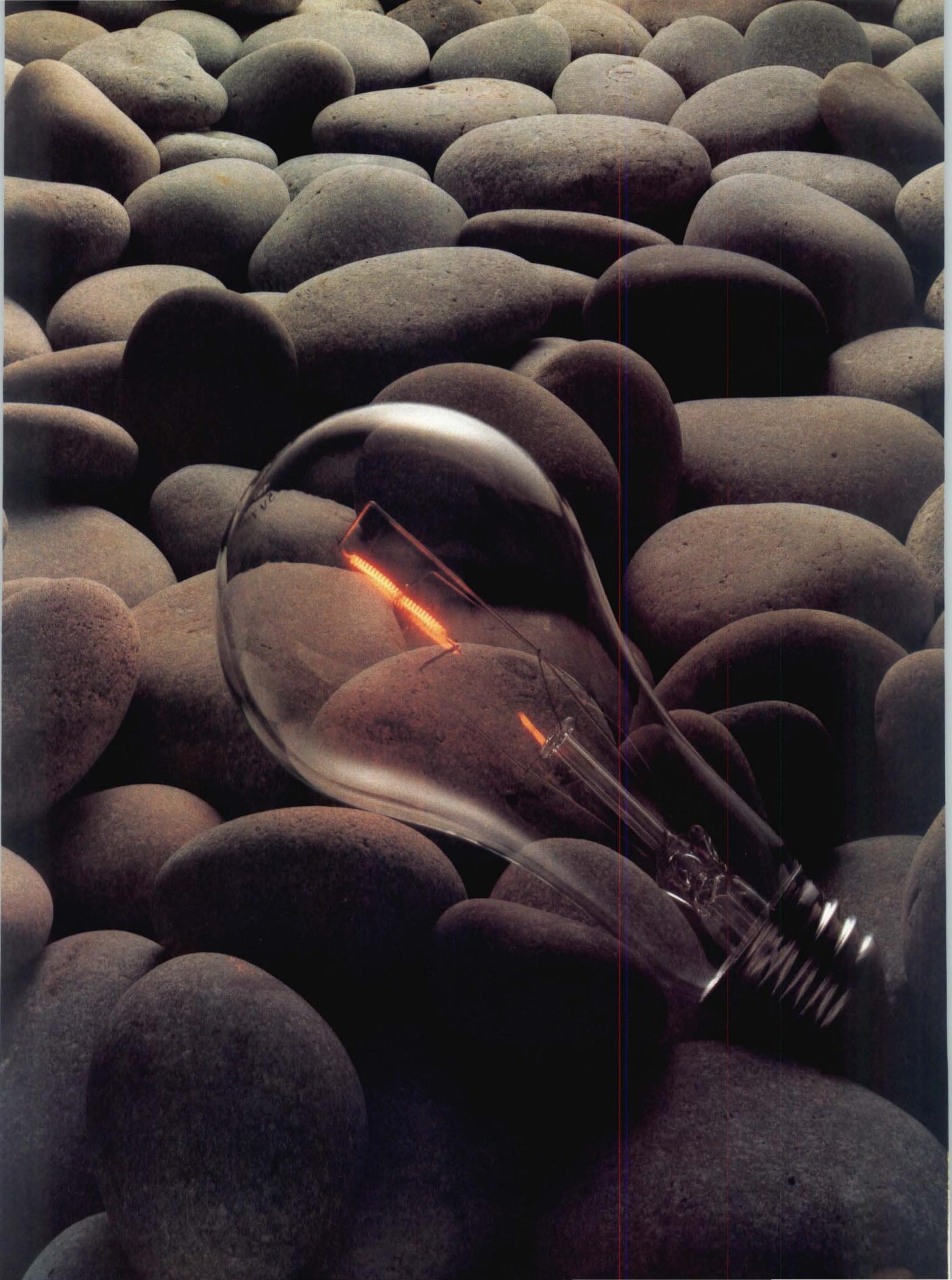


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must be refined. The end result will be an era in which our standard of living will be improved by the technological improvements provided by the "growing number of firms and individuals with ideas and products to satisfy these needs."

Specialized Switching Controversy Knows No National Boundaries

Much of the discussion involved in papers presented at ICC-76 on design of computer communication systems related to specialized switching—packet or circuit—and why a choice of one or the other was made in designing a network. (A technique combining the two² was not discussed.) In most cases packet switching was chosen.

France

Even though the initial HERMES project in France was oriented towards circuit switching, experimentation began in 1971 with packet switching techniques for development of a public service network.^{3,4,5} Based on results of ARPANET in the U.S., it was decided that packet switching offered at least three advantages: rapid implementation using standard computing hardware, economical adaptation to the "bursty" character of most computing communications, and possible use of switching node "intelligence" to overcome hardware diversity and incompatibility. Principal factors involved in making a decision included permanence of the service, accessibility, security, data transfer rates, transmission delays, and residual error rate.

Two radically different choices were considered for the basic service: exchange of postal-type messages and virtual circuits. The latter was finally chosen for both the basic service and the RCP's internal use. In the RCP network, a path is chosen at the establishment of the virtual circuit and is set up by updating information in each node traversed until the circuit is cleared.

Total control of resources has both advantages and consequences, but the speakers felt that the RCP network at the least provides a solid experimental base to support the choice of packet switching and virtual circuit service. It also serves in determining impact of the technique on applications and allows potential network operators to pinpoint problems.

Europe

The European Information Network presently includes 11 signatories: France, Germany, The Netherlands, Italy, Norway, Portugal, Sweden, Switzerland, the United Kingdom, Yugoslavia, and Eurotom. All signatories contribute equally to a common fund for development of a prototype network switching center. Reportedly,⁶ success to date has resulted from ability of the 11 parties to adapt and compromise their ideas. However, further problem areas—particularly in placing of contracts—still exist.

One of the study areas was the architectural designs and the network command languages they support. Interplay of one design involved a Pascal-based command language supported by a compiler, an intermediate language, and an interpreter.⁷ Resultant architecture is considered to be not overly complicated and its design should represent a manageable implementation effort.

Each of the initial centers—Eurotom, France, Italy, Switzerland, and the United Kingdom—involves a different major mainframe. Therefore standardization of areas such as network data representations, underlying services, and operating system variables is an absolute prerequisite to forming a workable network. Work to date indicates that there is a basis for future international standards.

Since the main function of the network is to provide an interconnection medium among the various centers in diverse countries, design objectives had to be clearly determined and carefully implemented—physically and politically.⁸ Software development was based on general principles and programs were written in a specially developed high level language called HELP 11. The software integration period was followed by a phase of intensive testing of both hardware and software. Even after installation and connection to the various computers at the centers, study and development will continue.

Each subscriber computer contains a transport station mechanism which shares access to the subnetwork between various users.⁹ These transport stations provide a more elaborate and secure switching service than the simple packet switching service offered by the subnetwork.

Another area of conflict exists in the priorities assigned by different centers. Although some are concerned primarily with transport station efficiency, others place stress on ease of implementation, speed of coding, measurement tools, or portability.

Japan

The Nippon Telegraph and Telephone Public Corp has been concerned with the need to accommodate non-packet mode terminals in a public packet switched network.¹⁰ This must be possible economically since most subscriber data terminals interfaced will be non-packet.

Such terminals accommodated are in either standard or delimiter class. A standard terminal has network standard transmission control procedure functions, while for the delimiter type the network defines sets of delimiters which trigger packet assembling and are not concerned with algorithms of the transmission control procedures.

A preliminary investigation shows that two sets of delimiters cover over 80% of existing online terminals in Japan. Although this class terminal does have disadvantages, both a wide range of transmission control procedures and computer data link control can be accommodated.

United States

A project at George Washington University, funded by the National Science Foundation (NSF) has been concerned with determining a method for avoiding the effects of interference in a multiclass packet switched network.¹¹ Messages in the classical store and forward packet switched network are composed of a group of packets—each independent, self-contained, and typically 1000 bits in size—and transmitted as such. Reassembly of the packet groups into the message at the destination point involves identification, classification, and other protocol functions. A design objective of any store and forward communication network is to evaluate the delivery delay of the packets and minimize it.

The NSF study resulted in a proposed method for reducing time delays of different class messages by a strategy in which the packet groups of different class messages are switched as a unit in a selective manner through a communication network. This reduces the amount of overhead associated with each multiclass transmission.

One of the many facets in a store and forward packet switching network is the steering or routing of messages. Typically there are multiple paths from a source node to a sink node with different immediate nodes and links to consider.

Proposed routing algorithms fit into three categories: fixed routing, centralized control; stochastic routing, distributed control; and content

guided routing, message control. An algorithm introduced for explicit path routing is a form of content guided routing.¹² It allows an originating node to choose a unique path from a set of one or more available paths to any destination. This algorithm has been found to be suitable for implementation in a network of non-homogeneous links and nodes because it requires only minimal processing and table storage in the intermediate nodes.

In brief, deterministic, end-to-end routing is provided by a simple table lookup mechanism which references precomputed tables. A field in the message header is updated at each node along the path, thereby allowing node tables of size KN, where K is the number of alternate paths available and N is the number of possible destinations.

Each node contains a set of pre-computed, static routing tables, one for every destination node in the network. In operation, the destination node address (DN) in the message header is used to select the explicit path routing table associated with that DN. The next node index (NNI) is then used to select the particular adjacent link/station to which the

message should be routed, along with an updated NNI value for use at that next node. The algorithm thus routes the message to and through the next node until it arrives at the destination node. There are multiple paths stored for each DN but only the one indicated by the NNI in the message header is selected. The user determines which path will be used through an initial setting, thus establishing the routing criteria on a message by message basis.

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Computers With Slot-Saving 32K Memory Boards and Terminal Printers Are Added to Line

Extending the Nova family upward by offering a slot-saving 32K-word memory board and memory protection, the Nova 3/D, a systems-oriented computer, provides 128K-word maximum memory capacity, easy configurability, and high level systems software. Announced by Data General Corp, Southboro, MA 01772, the 3/D uses the same 16-bit architecture as Nova 3 computers, with hardware stack and frame pointer, high speed direct memory access channel, and 16-level priority interrupt channel; and supports up to 128K words of MOS memory, with or without parity, core memory, or mixed memory.

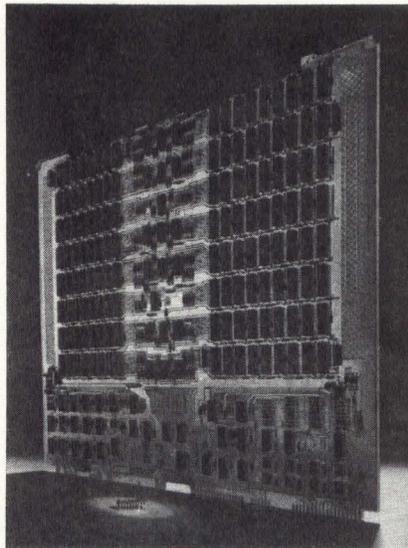
The 32K-word memory board is designed for use in all Nova 3 family computers. To provide easy maintenance to customers, the memory modules use a conventional 2-layer printed circuit board rather than a multilayer design. Circuit layout provides adequate power and ground networks for RAM chips and minimizes crosstalk between data, address, and clock signals. The 15" square board accommodates 144 memory chips, memory refresh control, and interfacing logic.

Memory cycle times are 700 ns for 32K, 16K, 8K, and 4K word semiconductor; 800 ns for 8K core, and 1 μ s for 16K core. Semiconductor memories use either Data General manufactured 4K RAMs or Texas Instruments parts as an alternate source.

Memory mapping and protection unit (MMPU) hardware performs logical-to-physical address translation, giving user programs access to 128K words of main memory through four address extension tables or maps: two program maps and two data channel maps. It also permits privileged instructions, I/O device protection, and main memory write and validity protection. This gives users the ability to run concurrent batch and multiterminal operations, when using the real-time disc operating system (RDOS). Each system program has full protected access to systems resources.

Also standard on the 3/D are programmers console, 16-bit I/O system, programmed data transfer, DMA automatic interrupt source identification, 61-device addressing capability,

16-level programmed priority interrupt, hardware stack architecture, external I/O bus connector, prewired peripheral connector, and electrically isolated system monitor bus. Options include battery backup, MOS memory parity, hardware multiply/



The 16-bit, 12-slot Nova 3/D from Data General uses 32K-word MOS memory modules with 700-ns cycle time to provide users with 128K-word memory capacity. Memory modules incorporate 144 4K RAM chips, memory refresh, and interfacing logic on conventional 2-layer PC boards, and minimize crosstalk between data, address, and clock signals through the circuit design

divide, high performance floating-point unit, real-time clock, and I/O expansion chassis.

The modular structure of the machine includes high density packaging of LSI and MSI circuitry, and a minimum of interconnections. Major subassemblies, such as CPU, memory modules, and major options, are on single boards to simplify troubleshooting and repair. The power supply also occupies a single PC board.

Available software includes RDOS, a diskette-based disc operating system, and a real-time operating system. Language processors are Extended FORTRAN IV and 5, Algol, single and multiuser Extended BASIC, and macroassemblers. A sensor-ac-

cess manager provides device handlers and subroutines to control I/O transfers between user programs and analog and digital sensor devices. A communications access manager supports synchronous and asynchronous communications subsystems.

Circle 140 on Inquiry Card

Terminal Printers

Interface compatible with all Nova and Eclipse computers, 6040 series models include KSR and RO, 30- and 60-char/s terminal printers. All provide full 132-column lines and are character compatible with Teletype™ and other ASCII devices. The Data General-manufactured units feature user-selectable view mode which moves the printing head so that the operator can read the last character printed; and a lead screw mechanism which drives the carriage to ensure precise horizontal and vertical head registration. A 40-character buffer and 60-char/s catch-up printing capability give the 6042 and 6043 printers true 30-char/s throughput capability; models 6040 and 6041 print at either 30 or 60 char/s.

Reliability and easy maintenance are provided by packaging the printer's components in five major groups: electronics, ribbon drive, printhead and carriage drive, keyboard and operator control panel, and paper feed. Side doors on the unit provide access to the interface, control circuits, and decoder—all on one PC board—and to the adjacent power supply. Reel drive and other components are accessible from the top of the unit.

Other design features consist of independent motor drives for paper, ribbon, and printhead which eliminates cumbersome linkages, clutches, or ganged drives, and keeps parts count to a minimum.

A 96-char upper/lower case English language character set is standard. Users can field-select upper/lower case, all upper case, or 128-char formats. Keyboard models can be used offline as typewriters. Form widths from 4 to 15" can be accommodated, and both left and right paperfeed tractors adjust, allowing the form to be placed anywhere on the carriage.

Circle 141 on Inquiry Card

Jack, The Giant Killer

In Peripheraland, there lived 5 terrible giants. The Tape Read Chain Gang some called them.

Anyone traveling through their forest with a bit of this or that wandered torturous paths. For it was vastly overgrown with componentry which boggled the mind and scratched the head. And the giants exacted much tribute from the unwary.

Many champions from the Valley had battled them. They always lost.

One day Jack arrived.

I am the giant killer, here to free you from the primitive bondage of the ogres for under 9 bucks, list.

You are small, cheap, and have a monolithic look, laughed the people. You will never function effectively in that tangled maze.

We'll see about that, said Jack. I have a secret. And he set off.

From behind a great clump of ICs sprang Input Multiplex, the first terrible giant.

Your NRZI or your life! he roared.

Let me go and I'll tell you a secret, said Jack.

Tell it at once, growled the giant.

Well, I not only handle phase, group and NRZI coding from 9-track but cartridges and cassettes as well, cried Jack, dancing about. And I can digitally select between two of these formats!

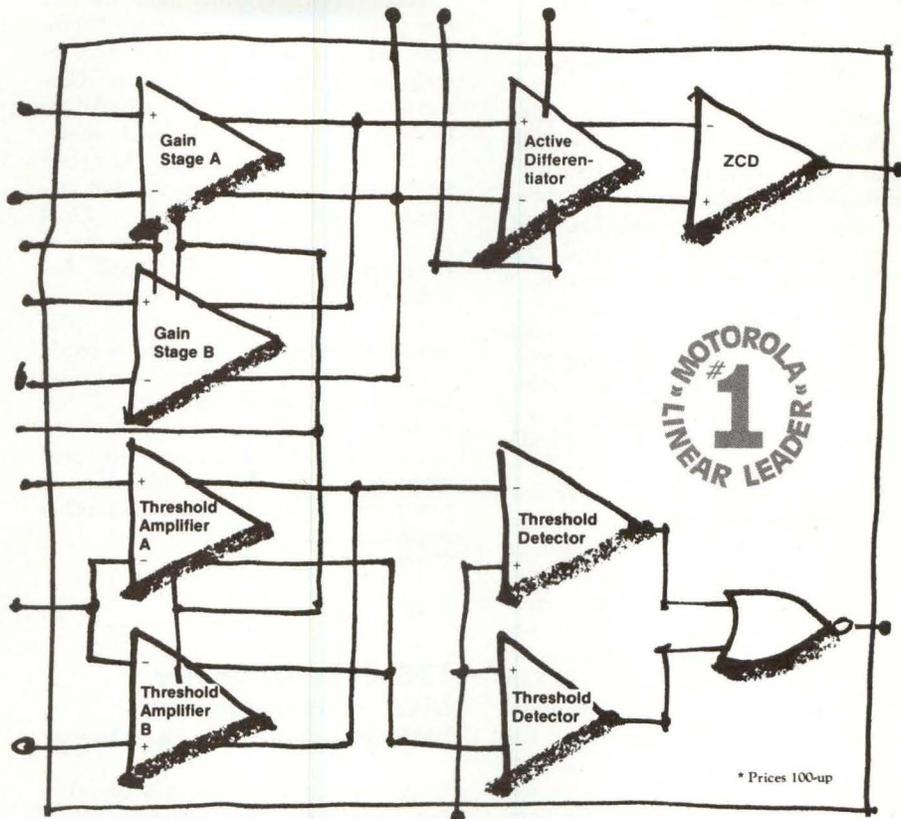
O, no! cried the giant and ran crashing off through the wood.

Soon Gaynstage, the second giant, confronted him.

Halt, he frothed.

Control yourself and I'll tell you my secret, said Jack.

Do so, grunted Gaynstage.



\$8.95* MC3468 Monolithic Read Amplifier Secret of Little Jack, Giant Killer, Who Clobbered The Tape Read Gang

My EGC (Electronic Gain Controlled) amplifier provides differential outputs for the active differentiator and a single output is available for threshold function.

AAAGH! screamed the giant. How awful! and fell backward into a wayside pool and drowned.

The third giant, Threshold Amplifier/Detector, leaped from the undergrowth. He shook Jack till his teeth rattled and he could hardly explain his secret.

Tell it! the giant bellowed.

M-M-My threshold amp gives an output signal wh-wh-whenver it exceeds the setting in p-p-pos or neg direction, replied Jack.

The bully turned red and choked on his own phase jitter.

Much the same happened with

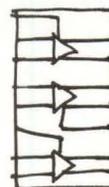
the fourth and fifth giants, Active differentiation and ZCD. Jack revealed his ensured linearity, optimum zero-crossing detection for excellent noise rejection and strict avoidance of timing distortion.

He laughed at the giants' horrorstruck faces as they took off.

When he returned the elated people cut down the forest and made him king, as he deserved.

Now it's no secret with a little jack you can go out and kill some giants of your own.

But you already concluded that.



MC3467, advance man and partner of Jack. Has 3 EGC preamps, diff inputs/outputs and 15 MHz BW. Operates near mag heads for less than 4 bucks.

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ISP Language Provides Tools for Analysis of Computer Hardware

A modeling technique that provides EDP specialists with a realistic means of comparing commercially available computer systems has been developed at Carnegie-Mellon University, Schenley Pk, Pittsburgh, PA 15213. The technique uses ISP, a special programming language, to standardize the description of hardware components and operating characteristics of computers. It may eventually enable new hardware designs to be generated automatically by computer.

Technical manuals and specifications furnished by computer manufacturers seldom provide enough information or data in comparable form to enable one machine's performance to be measured against another's on specific tasks. To overcome this difficulty, Dan Siewiorek and Sam Fuller, both associate professors of Computer Science and Electrical Engineering, worked to develop the modeling technique that enables different hardware designs to be compared through simulation, providing potential users with the ability to match their needs with available machine capabilities.

Formatted for use on a DEC PDP-10 computer, the simulation programming accepts an ISP description of a machine and causes the simulator to handle data in exactly the same manner as the described machine. This provides a detailed performance test in which processes are monitored and recorded step-by-step.

Using a simulator, rather than testing actual machines, permits application of standard benchmarks in the testing process, and allows hardware to be measured against a uniform scale. Sample problems can be tracked through every phase of each computation to precisely determine what task each design performs most efficiently.

Research was partially funded by the National Science Foundation, the Advanced Research Projects Agency of the Department of Defense, and the Army/Electronics Command; the Naval Research Laboratory, another funding agency, is currently using the system in their selection of computers by asking potential suppliers to provide an ISP description of their hardware.

Hardware description tools are just one phase of the comprehensive "Symbolic Manipulation of Computer Description" effort being done at Carnegie-Mellon. Since the simulation techniques furnish a detailed analysis of machine operations, they can be used to test designs without actually building hardware. Final phase of the project will consist of developing software that will enable much of the actual design process to be done by machine. The group has already developed a crude hardware generator that "works no better than a hand designer. . ." but believes that the process can eventually be fully automated to generate optimized designs based on a description of projected uses and other important criteria.

Circle 142 on Inquiry Card

13G-Byte Capacity Disc Subsystem Uses "Winchester" Technology

Using Winchester data module storage technology, the 33801 family of disc subsystems provide System/370 users with 400M bytes of directly accessible data on a single disc drive. According to Control Data Corp, Box O, Minneapolis, MN 55440, this is 20 to 25% more storage capacity than is offered by competitive products. In addition, from 800M to nearly 13G bytes of data storage require only a single 38302 controller. Savings in computer system operating costs can result because the logical arrangement of current 3330-11 data files need not be changed to take advantage of the greater storage capabilities.

Each drive unit in the series contains recording discs, read/write heads, and head arms in a sealed unit for protection of information. Data are transferred at nearly 1.2M bytes/s; average data access time is 25 ms within a logical volume. Drive options include units with 1.24M bytes of fixed head, zero-seek-time storage for performance sensitive applications that require faster data access.

Each disc storage unit consists of two drives; from one to four units can be configured in a single string. Four strings—32 drives with 12.8G-byte capacity—can be attached to the 38302 storage control unit.

Six models in the family are the A2 and A2F, each containing two drives and associated control logic to attach to the control unit; V2 and B2F, each with two drives and attaching to the A2/A2F; and models C2 and C2F, each with two drives plus alternate control logic to attach to a control unit. Alternate control logic is manually selected to provide backup in event of failure in the A2 or A2F units.

Disc subsystems can be used with IBM System/370 computers under the control of OS, DOS, OV/VS, and DOS/V operating systems and require no software modifications. Data formatted in 3330-11 logical volumes need not be converted to another mode for storage on these data module units. Since the 33801 units can be intermixed on the same controller with 33301, 33302, and 33401 disc products, the subsystems can serve as staging units for the 38500 mass storage unit.

Circle 143 on Inquiry Card

X-Y Matrix Keyboard Uses Strip Switches To Cut Costs in Half

A low profile keyboard that should cut costs for high volume keyboard users roughly in half is currently offered in 20- and 24-position standard versions, by Texas Instruments Inc, Control Products Div, Attleboro, MA 02703. Design is based on strips of disc switches in an X-Y matrix.

Key to the keyboard's low cost is the elimination of individually assembled switches as well as an arrangement of wire interconnections, which avoids the need for high cost circuit boards. Instead of individual snap-acting switches, the keyboard uses disc switches which are manufactured in strips, but which function independently. The design has only a few parts; it needs no circuit board, and it requires no soldering. In addition, integral keyboard connector leads eliminate the need for a separate connector; and the device is manufactured on a fully automated assembly line.

The carrying frame also functions as an electrical circuit element so that switches in any row (X-direction) are electrically common. Individual wires laid under each switch column form the Y-direction circuit elements. Another set of wires is

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For example, the effects of utility power variations, including brownout, are virtually eliminated since the Dependables continue supplying their specified outputs at full load over inputs of 92 to 138 VAC or 184 to 250 VAC. In fact, they'll operate for several minutes at inputs as low as 70 or 140 VAC. If AC fails completely, the supplies will hold up for 30 milliseconds, allowing orderly shutdown or transfer to optional battery back-up.

And logic designers plagued with an occasional "Perhaps" when switching all their "Falses" to "Trues," can relax with a power supply whose typical transient response of a 5-volt output to a 25% load step is on the order of 20 mv.

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Voltages and Currents	Similar to Single-Output Supplies

SINGLE OUTPUT SUPPLIES

MODEL	PM2496	PM2497	PM2498
Output Volts	Output Amps	Output Amps	Output Amps
2	100	200	400
3	60	100	200
5	50	100	200
5	—	150	300
12	25	60	120
15	25	50	100
18	22	45	90
21	18	38	76
24	16	33	66
28	13	27	54
SIZE (inches)	5 x 8 x 11	5 x 8 x 11	5 x 16 x 11



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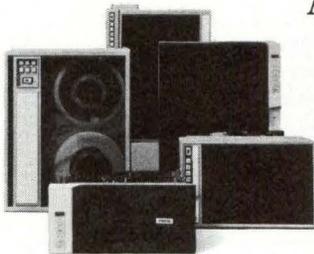
T1000. The Pertec superstar. Specifically developed to handle the great chunks of on-line data that systems will require tomorrow, as well as today. Because we recognize the futility of state-of-the-art CPUs, if the rest of your system can't keep up.

Expect cost-effective performance that just won't stop. T1000 whirls through heavy dp throughput at 75 to 125 ips—PE and NRZI read-after-write. Dual density for now, but we've also designed T1000 to handle GCR high density recording—why waste a powerful CPU on yesterday's technologies?

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With the T1000 now topping our tape line, it's hard to imagine anything an OEM could want, that Pertec can't deliver.

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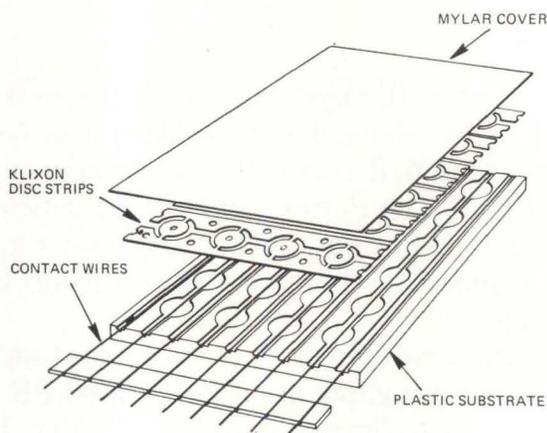
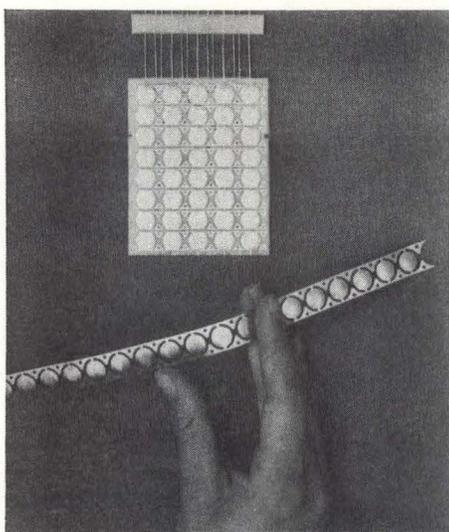
With over 60,000 tape drives already shipped, and still more capability to come, there's no question Pertec's committed to give you just what you need, *just when you're ready for it.* (Is it too corny to say "your wish is our command"?)

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CIRCLE 20 ON INQUIRY CARD



Based on X-Y matrix technology, Texas Instruments' low profile keyboard uses stamped strips of disc switches and a carrying frame which also functions as an electrical circuit element. Individual wires laid under each switch column form the Y-direction circuit element, another set of wires, located between switch columns, is electrically connected to the disc strips. Leads are arranged across the top of the keyboard, simplifying connections with motherboard circuitry

located between switch columns and is electrically connected to the disc strips. In this way all circuit elements emerge at the top of the keyboard, automatically forming an integral lead frame. Supporting board is a sheet of engineering-grade structured thermoplastic.

Since, in the keyboard design, the electrical and physical matrices coincide, and both are standardized in an X-Y format, users' electrical circuitry must accept this switching lay-

out. For maximum cost-effectiveness, the user also should plan on an X-Y arrangement in his interface circuitry.

The X-Y Matrix keyboard allows simplified assembly into a user's product; it comes readymade with a "lead frame," or wire umbilical, as an integral part. Leads of standard 0.020" cross-section wire are all arranged in a row at the top of the keyboard, simplifying connection to motherboard circuitry. Users can in-

sert wires directly into motherboard, and, where desired, solder along with other circuit components.

Designed to sell for \$0.04/switch position in 100,000-piece quantities, both 20- and 24-position standard versions are being offered with a 0.500 x 0.562" key spacing. Overall size is 2.400 x 2.950" for the 20-position model, 2.400 x 3.512" for the 24-position board. Minimum life is 500,000 operations.

Circle 144 on Inquiry Card

LED Alphanumeric Display Reduces Parts Count With Onboard Circuitry

A LED alphanumeric display that packs four 3.8-mm (0.15") high characters in each package, the HDSP-2000 is complete with onboard electronics. Offered in standard 12-pin DIPs, the devices contain onboard shift registers and externally programmable constant current drivers. Packages are mechanically and electrically end-stackable and TTL compatible.

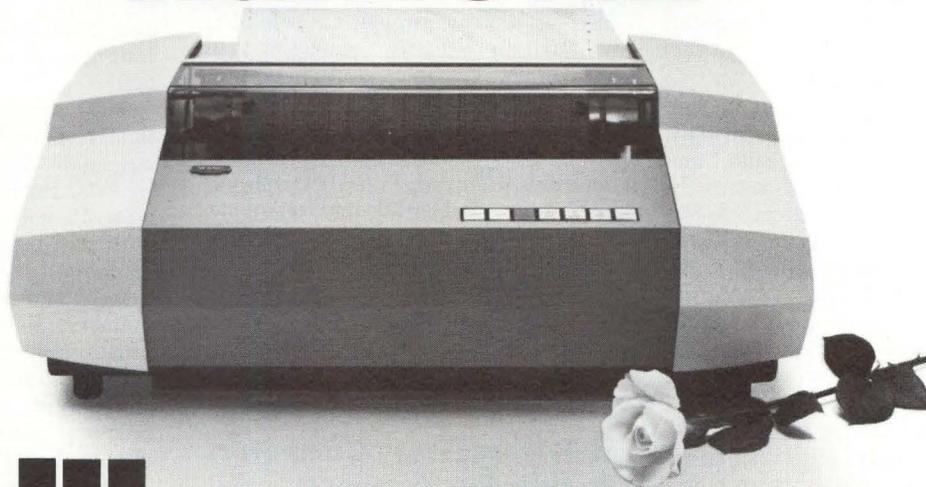
Traditionally single-digit LED dot matrix displays have been organized

in an X-Y addressable array, requiring 12 interconnect pins per digit, plus extensive row and column drive support electronics. The -2000 provides onboard storage of decoded row data plus constant current sinking row drivers for each of the 28 rows in the 4-character display. This approach allows the user to address each display package through just 11 active interconnections as opposed to the 176 interconnections and 36 components required to effect a similar function using conventional LED matrices.

Developed by Hewlett-Packard Co's Optoelectronics Div, 640 Page

Mill Rd, Palo Alto, CA 94304, the device consists of four LED matrices and two 14-bit serial-in/parallel-out shift registers. The LED matrix for each character is a 5 x 7 diode array organized with the anodes of each column tied in common and the cathodes of each row tied in common. Seven row-cathode commons of each character are tied to the constant current sinking outputs of seven successive stages of the shift registers; like columns of the four characters are tied together and brought to a single address pin. In this way, any diode in the four matrices may be addressed by shifting

Wang's new printer is getting called a lot of names...



like yours.

Call it what you will, Wang's new 120 Line Printer is an OEM natural.

Quiet...Fast...Versatile...Beautiful. The 120 gives you and your customers what you've always wanted from a line printer: Full Features. Reliability. Ease of operation. Crisp, legible printouts. Low price. Wang Quality.

The 120 boasts a wide array of features at a surprisingly low cost. 120 CPS; 7x9 dot matrix; fully-buffered 112 character line; upper and lower case 96 character set with full ASCII; a double-axis bearing plate for long life; a servo-driven head for quiet, reliable operation.

Wang's 120 comes in two models. The W-1 features 112 columns. The W-2 has a full 132 columns. Both are available with vertical format

control, mini-exerciser and RS232C.

Your customers will love the clean, crisp copies delivered by Wang's exclusive 9-pin head design. And the 120's expanded character-size capability lets them emphasize any portion of a printout with bold, eye-catching letters or numbers.

And if you're used to hearing your

customers moan about loading paper, just let them get their hands on the bottom-fed 120. Then stand back and listen to the sound of solid satisfaction.

To find out more about the printer that lives up to your name, fill out the coupon or call Wang OEM Sales at (617) 851-4111.

Please send me more information on Wang's 120 printer.

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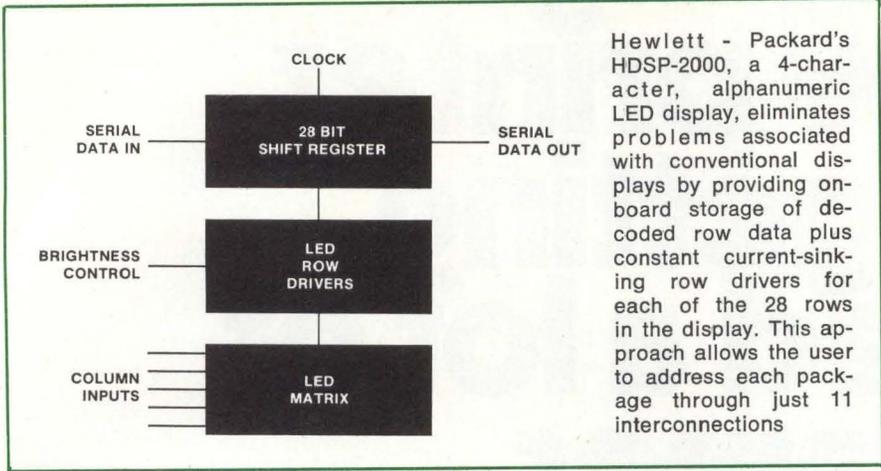
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CD10/119DP42



Hewlett - Packard's HDSP-2000, a 4-character, alphanumeric LED display, eliminates problems associated with conventional displays by providing on-board storage of decoded row data plus constant current-sinking row drivers for each of the 28 rows in the display. This approach allows the user to address each package through just 11 interconnections

data to the appropriate shift register location and applying a voltage to the appropriate column.

Since the device combines a significant amount of logic and display capability in a small package, on-board power dissipation is relatively high, making thermal design of the display mounting an important consideration. Full power operation at $T_A = 25^\circ\text{C}$ (with $V_{CC} = V_B = V_{COL} = 5.25\text{ V}$) is acceptable if the thermal resistance from pins to ambient, ϕ_{CA} , is not greater than $35^\circ\text{C}/\text{W}/\text{cluster}$, assuming that the display's mounting surface becomes an isothermal plane. If only one display is operated on this plane at 1.7 W, temperature rise above ambient becomes 42.5°C ; a second display doubles the temperature. Thus catastrophic levels are quickly reached, and an appropriate increment of heat dissipating capability must be added to the mounting plane for each display cluster added to the display string.

A practical display system using the device requires interfacing with a character generator and refresh memory. Refresh memory stores information to be displayed, coded in any of several standard data codes (a display font may be customized through use of a custom-coded ROM). The character generator receives data from the refresh memory and outputs seven display data bits corresponding to character and column select data input. These data are converted to serial format in a parallel-to-serial shift register for clocking to the array's shift register.

Each character is formed with a 5×7 dot matrix, capable of displaying the full ASCII code, lower

case as well as upper case letters, punctuation marks, mathematical and other symbols, and numerals. Each 4-character package measures 0.699×0.290 " high ($17.7 \times 7.25\text{ mm}$). The displays operate at temperatures from -20 to 70°C for use in hostile industrial environments. They are priced at \$47 for a 4-digit cluster (U.S. price) in quantities of 125 clusters.

Circle 145 on Inquiry Card

Multiprocessor Computers Double Performance, Improve Fault Tolerance

Medium-to-large scale B 6800 computers added to the company's '800' family are claimed to provide twice the performance of similar sized B 6700 systems now in use. According to Ray W. McDonald, Chairman of Burroughs Corp, Detroit, MI 48232, "the B 6800s represent a new level in the evolutionary development of Burroughs advanced multiprocessor architecture. . . ." Systems incorporate a faster CPU, with lookahead logic, which operates at 6.7 MHz; an I/O processor with larger buffers and increased channel capacity; a large high speed main memory subsystem; and a data communications subsystem that incorporates new network and message processing functions.

Three models in the series are the B 6807 and 6811, each with one central and one I/O processor; and the B 6821 with dual central and dual I/O processors. Systems can be configured to contain up to four central,

four I/O, and 16 data communications processors and 15,728,640 bytes of directly addressable memory. Central processor lookahead logic enables simultaneous fetch and execution of instructions. Fault tolerance is improved by having the CPU retry instructions, retry memory accesses by retaining addresses in the event of error conditions, and perform residue checks on all address calculations.

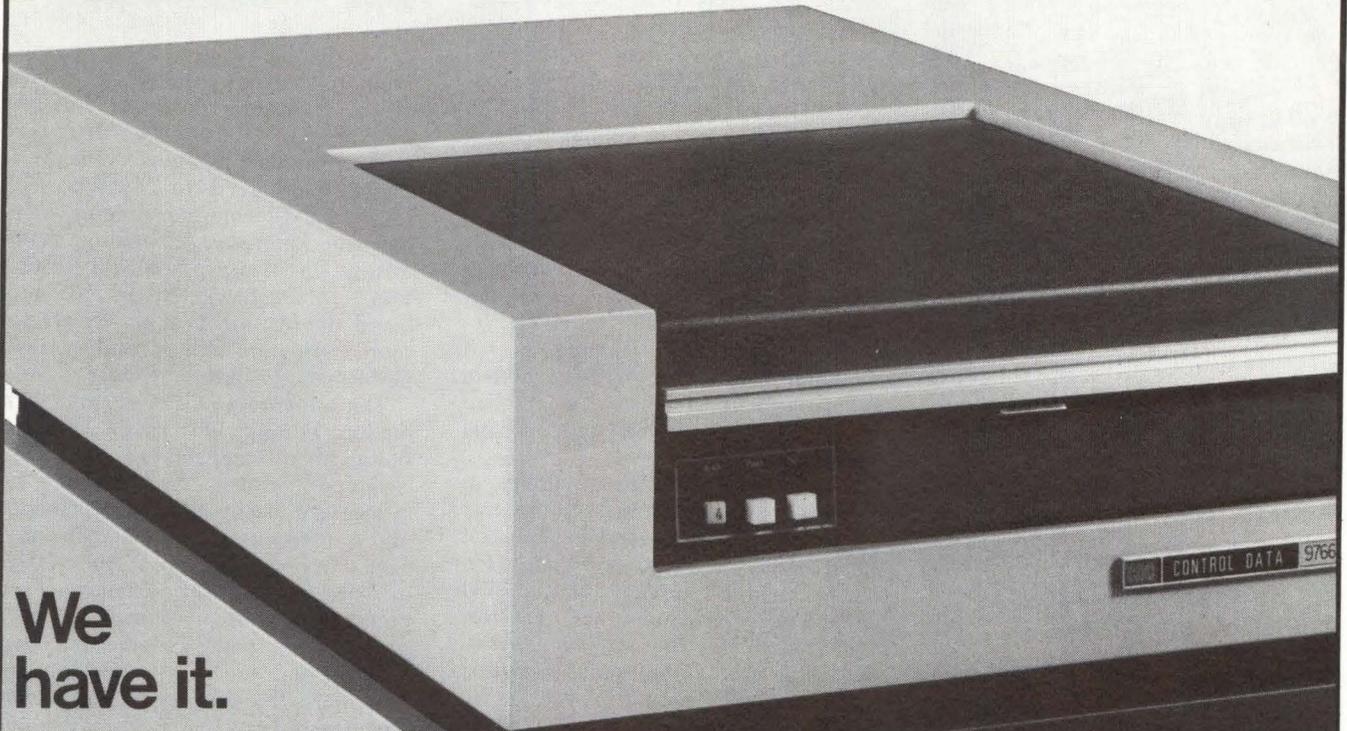
The series use self-powered, error-correcting, high density planar core memory that may be 2-way interleaved. Read access time is 325 ns for six bytes. Multiple central processor configurations have main memory that is associated with each CPU, plus memory that is global to all processors. Each CPU can have up to 3,145,728 bytes of main memory. Global™ memory has a capacity of up to 3,145,728 bytes. Optimized memory access logic enables the 6811 and 6821 CPUs to provide two and four times the throughput of the 6807.

I/O processors operate independently of the CPU and can sustain an aggregate data transfer rate of 2.2M bytes/s. Each processor has 20 channels; 12 with 512-byte buffers, eight with 256-byte buffers. I/O channels load data to and from peripheral devices and transfer data to and from memory simultaneously. The combination of expanded buffer sizes and simultaneous operation increases throughput by efficiently utilizing memory, making more cycles available to the CPU.

Effectiveness of the computer's distributed processing architecture is further extended by network and message processing functions that are incorporated in the data communications subsystem. Each subsystem has 393,216 bytes of memory and provides for network continuation audit, and recovery if the central system is not available.

The data communications processor (DCP) accumulates requests and messages from data communications devices and transfers them to disc files that are shared by and subsequently accessed by the main system. Broadband communications control enables the DCP to service multiple data links ranging from 19.2K to 1.3M bits/s. The control operates asynchronously with the DCP and communicates at the message level through binary synchronous or Burroughs Data Link Control Procedures. A new control provides high speed block transfers of messages between DCP memory and CPU memory independent of the DCP's operation. This further distribution of mes-

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12 MB	MMD	300	9730-12	Fixed, Sealed	Industry std. SMD I/O format and interface common to all models.
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48 MB	MMD	600	9730-48		
40 MB	SMD	200	9760	Removable	
80 MB	SMD	400	9762		
150 MB	SMD	200	9764		
300 MB	SMD	400	9766		

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sage handling increases throughput of the data communication subsystem.

Availability and maintainability are improved by a microprocessor-based maintenance processor and display. This processor uses regular system peripherals to run diagnostic routines, and has the ability to access and display status of the entire central system. A memory tester, incorporated in CPU logic, is also controlled by the processor. Maintenance diagnostics software can be system driven and run online, allowing maintenance confidence routines to be initiated by the user or by the system's master control program, and to run with user application programs. The CPU's built-in self-test logic allows the CPU to test itself during idle periods.

Circle 146 on Inquiry Card

Network Control System Incorporates Diagnostic/Restoral Functions

Monitoring, diagnostic, and restoral functions for high speed Fast-Poll multipoint modems are provided by the Multipoint Network Control System (MNCS) announced by Codex Corp., 15 Riverdale Ave, Newton, MA 02195. Operating through the use of a frequency division multiplexed secondary channel, the MNCS performs most functions without interrupting data on the high speed channel. All operations and controls are performed from the central site; no manual intervention is required at remote multipoint drop locations.

Composed of master control console, which provides the man-machine interface to the multipoint network, and remote card set, which installs on remote modems, the MNCS identi-

fies that portion of the network that is malfunctioning and allows network operation to be restored through alternate facilities. The console is capable of controlling up to eight separate multipoint lines, each of which can have up to 30 drops—for a total of 240 addressable locations. In addition, the system can be supplemented with digital patching modules which permit the console to be patched into an unlimited number of additional multipoint networks.

The unit provides three operating modes. Monitor mode allows EIA interface signals and modem indicators for all remote units to be determined successively or on a selective basis. A streaming search function identifies any remote modem whose inbound carrier has latched up and is interfering with normal system operation.

Test mode provides capability to perform five different system test functions: remote modem self-test check, outbound bit-error rate test, audio loopback on any unit, digital loopback on any unit, and poll test which simulates the dynamic operating modes of a multipoint network. Error performance is displayed on the front master console digital readout displays.

Configuration mode allows reconfiguration of the network from the central site using alternate facilities to maintain network operation despite failures. The MNCS can cause all modems on a selected line to fall back to lower operating speeds so that maximum utilization of degraded line facilities is possible.

Options to the MNCS include a dial backup autoanswer unit (DBAAU) which automatically switches a remote modem into a dial backup mode upon receipt of incoming dial calls; a modem substitution switch which switches a standby modem into op-

eration under MNCS control; and a node bypass switch which provides operation of MNCS functions at remote locations.

Circle 147 on Inquiry Card

Assembler/Editor Enables Interactive Editing With 4K Memory

An assembler/editor that enables users to perform interactive editing via a teleprinter keyboard, OMEGA 3/05 runs in 4K 16-bit words of core or semiconductor memory and is specially designed to function with LSI-3/05 Millicomputers. In developing the language, Computer Automation, Inc, Naked Mini Div, 18651 Von Karman, Irvine, CA 92713, combined the features of a conversational source program editor and a high performance, 2-pass assembler.

The software provides program generation, editing, and assembly capability in a compact, easy to use, Teletype™ driven environment. An in-memory source buffer manager allows the user to maintain and assemble programs without intermediate tapes. Either the new source program or the corresponding object program, or both, can be punched out for future use.

Reading free-form input, the assembler translates it and generates an object program. The editor provides interactive add, delete, and control functions to simplify the task of preparing and modifying programs. Source programs can be constructed in memory from pieces of existing programs or generated via a terminal keyboard and then assembled. Source program debugging is facilitated by automatic printing of easy to understand error codes after each erroneous statement.

Editing commands are entered via a TTY keyboard; listing and punching can be dynamically directed to the bit-serial TTY or to any device attached to the 3/05 via the distributed I/O system. Source input can be switched back and forth from the TTY keyboard to card reader, paper tape reader, or memory.

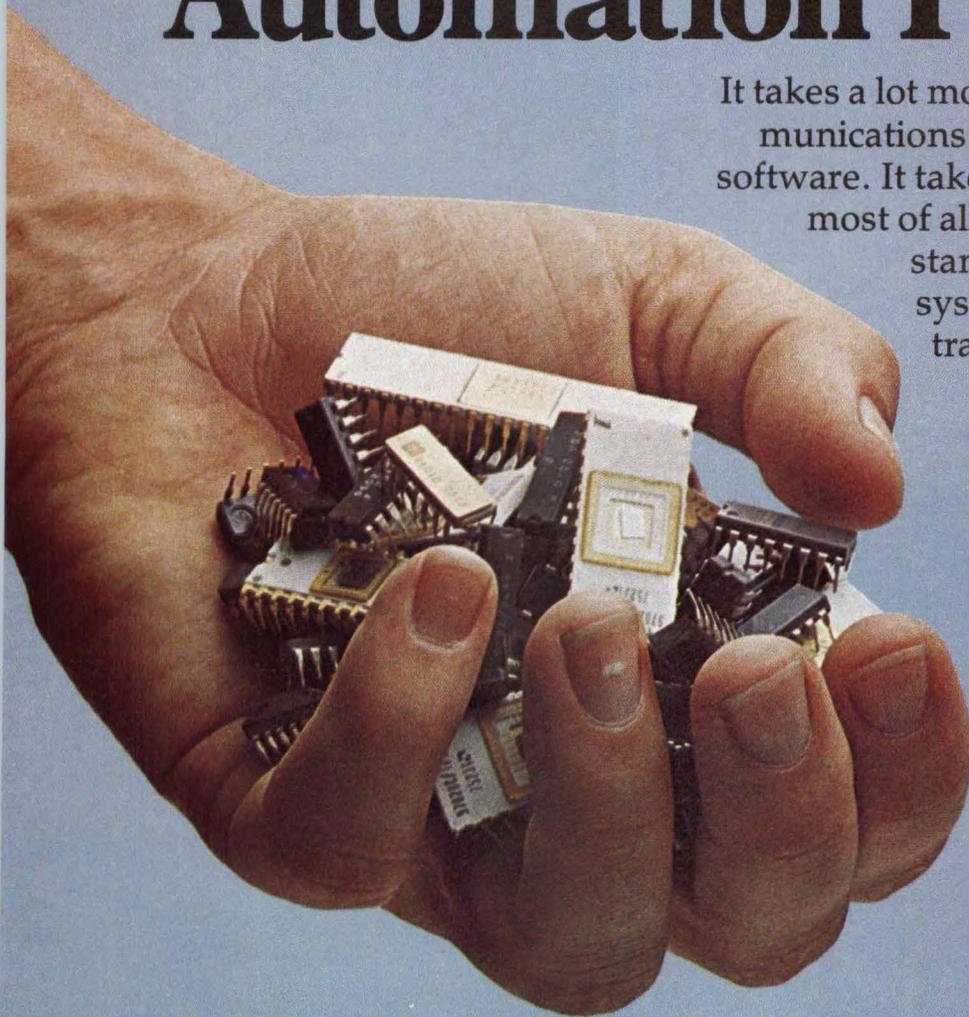
An extended version of the package is available to support the software with nonstandard peripherals. This package includes object code for the assembler nucleus and source code of assembler I/O routines. 8K memory is required. Both versions are supplied on paper tape with full documentation. Basic package is priced at \$140. □

Circle 148 on Inquiry Card



Supplementing Codex's family of LSI Fast-Poll 4800- to 9600-bit/s multipoint modems, the Multipoint Network Control System operates through a frequency division multiplexed secondary channel to provide monitoring, diagnostic, and restoral functions without interrupting data on the high speed channel

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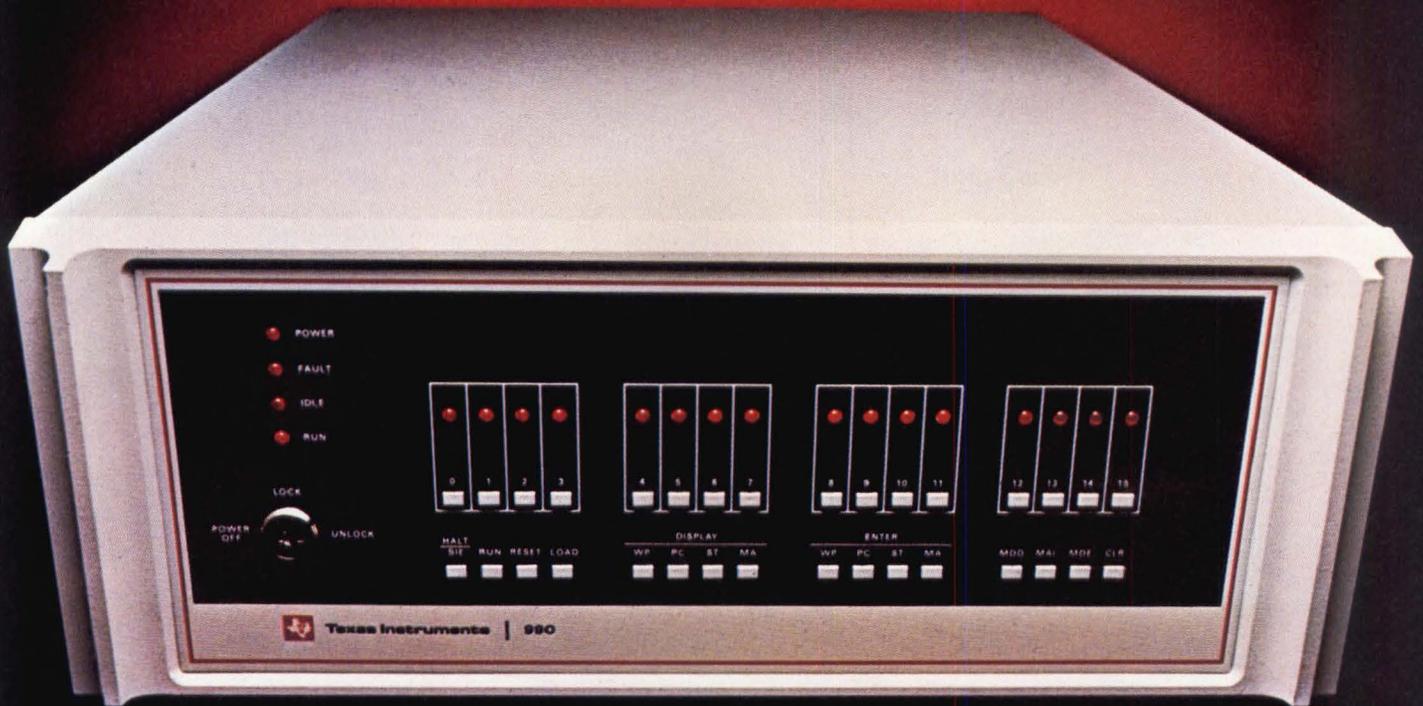
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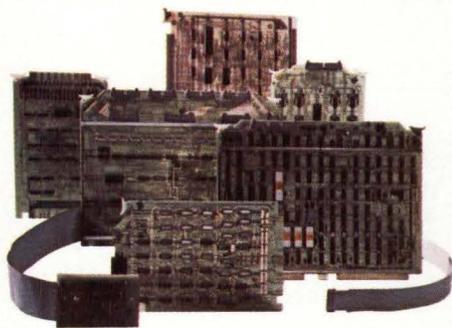
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Peripheral Interface Modules

interrupt structure. 16 registers arranged in a workspace concept. I/O that's directly programmable through the Communications Register Unit (CRU) and autonomously through a high-speed data bus. And bit, byte and word addressing of memory.

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In small or large configurations, the 990/10 design provides surprising flexibility for a small investment.

The CRU, with up to 4096 I/O lines, reduces interfacing costs by keeping controller complexity to a minimum. The TILINE* asynchronous high-



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speed data bus can support both high- and low-speed devices and takes advantage of design simplicity for simultaneous data transfer between peripherals, the CPU and memory.

With the 990/10, you get a powerful instruction set with an extended operating feature that allows hardware to take over operations that software would normally execute. An optional mapping feature provides memory protection and memory expansion to 1 million words. And, optional error-correcting memory corrects single-bit errors for increased system reliability.



DS 25/50 Disc Drives

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Model 979 Tape Drive

mands. We offer program development aids for creating and testing software, and communications software to support synchronous or asynchronous data transmission.

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1.

IBM-type ceramic heads with low pad force give 15,000 hours head life and extended media life.

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High reliability design makes possible 5000 hour MTBF with no recommended maintenance.

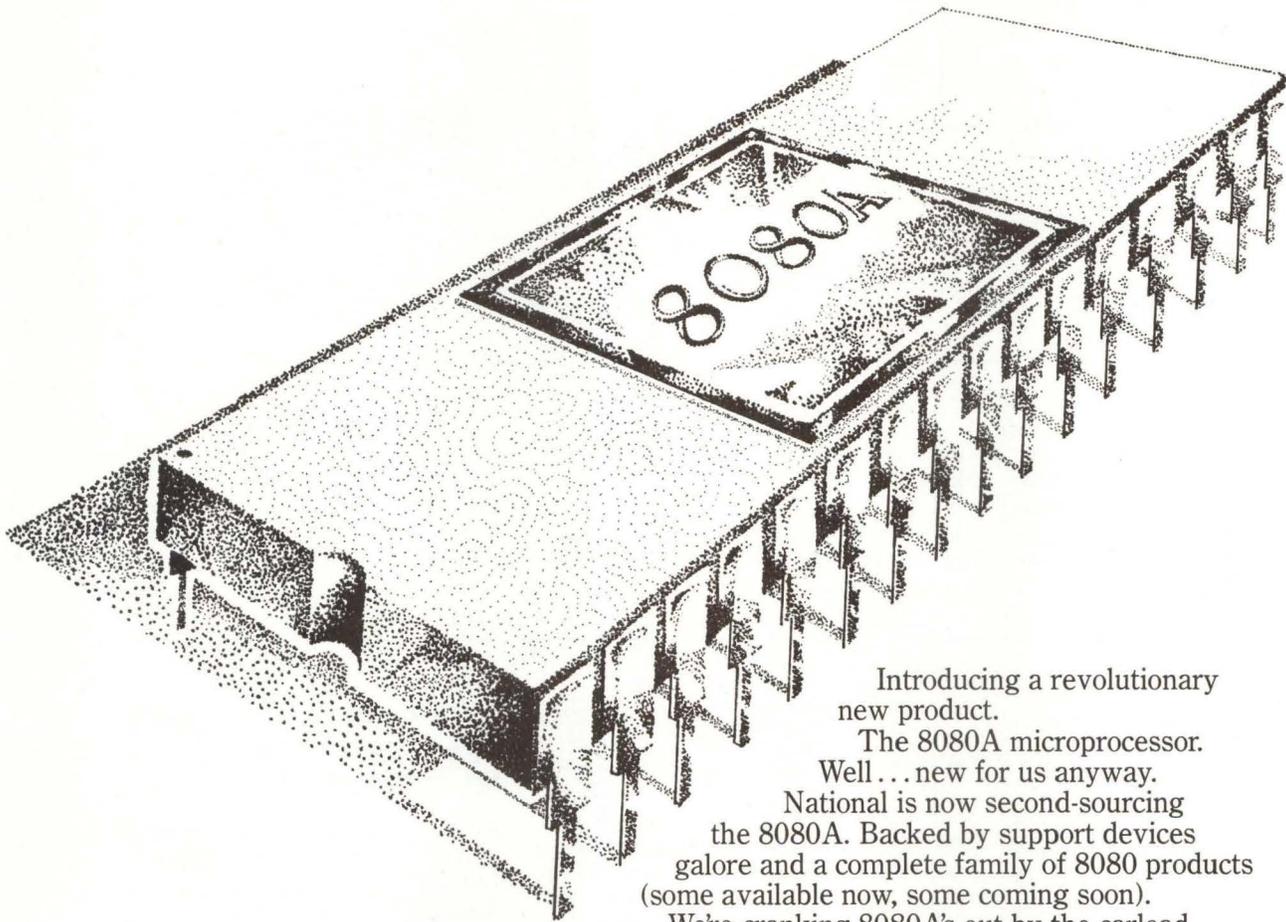
Die cast mainframe and carrier maintain precise tolerances.

1.

Fast access positioner and electronics facilitate 6 ms track to track seek with 164 ms average seek. Low friction uniball positioning assures data reliability of 1×10^{10} .

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The 8080A microprocessor. Well... new for us anyway.

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CD10

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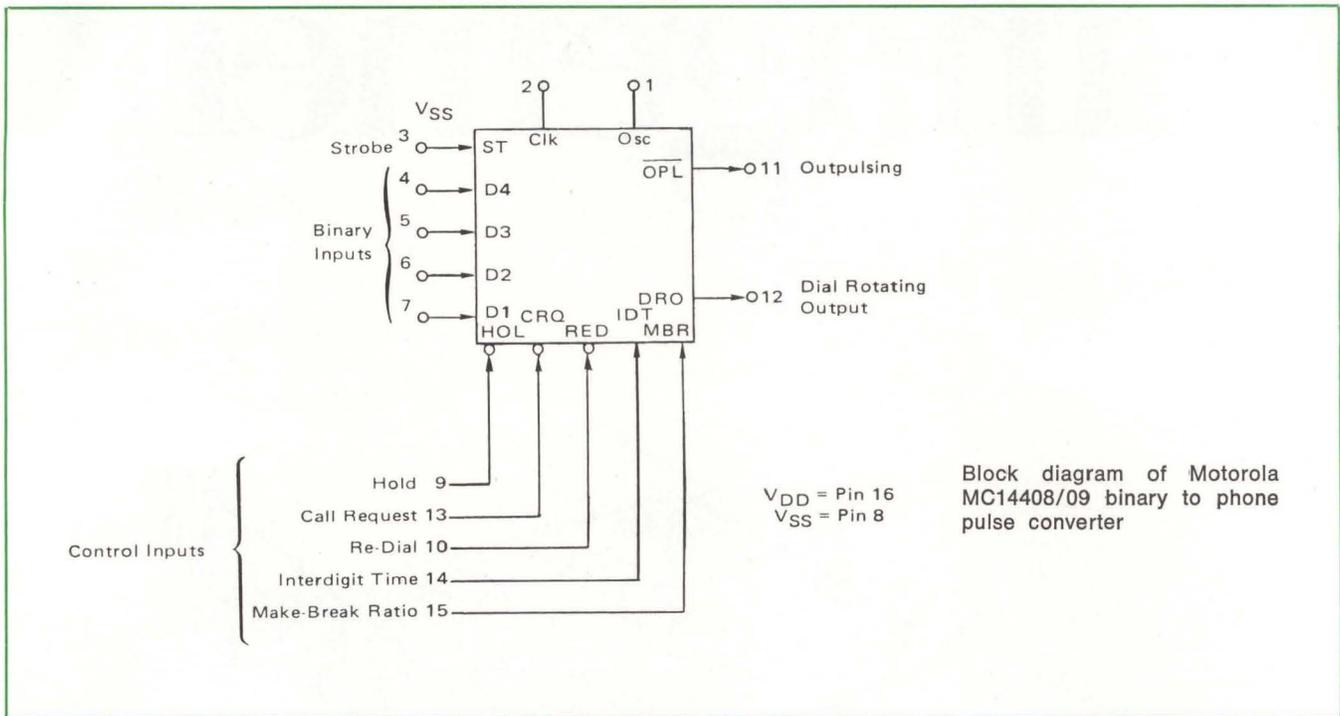
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 **National Semiconductor**



On-chip circuitry combined with an external capacitor and inductor provide the clock frequency. The phone system normally uses a 16-kHz clock frequency but the part will operate

over a frequency range of 4 to 80 kHz.

Both circuits, from Motorola Inc, Integrated Circuit Div, 3501 Ed Bluestein Blvd, Austin, TX 78721, operate

over a range of 3 to 6 V and are available in 16-pin DIL packages. Pricing in quantities of 100 to 999 is \$6.98 for plastic and \$9.08 for ceramic. Circle 351 on Inquiry Card

Small, Fast Settling, 8-Bit DACs Provide ±0.2% Nonlinearity

Quality performance usually found only in larger, more expensive modular units is claimed by the manufacturer for two versions of the DAC90. Both are monolithic 8-bit devices complete with internal reference and scaling resistors, and have 200-ns settling time to ±0.2% of full-scale range (FSR) for a 10- to 100-Ω load range. Nonlinearities are ±0.2% over the respective temperature ranges: -25 to 85°C for model BG, -55 to 125°C for SG.

Digital inputs are accepted in complementary binary format; devices may be connected for complementary straight binary or complementary offset binary operation. Adding an external inverter permits use in complementary 2's complement mode. Analog output will not vary by more than ±½ LSB over the specified tem-

perature ranges. Gain error of 5% and offset error of 1% of FSR are adjustable to zero with external trim pots.

Gain drift of the devices made by Burr-Brown Research Corp, International Airport Industrial Park, Tucson, AZ 85734, is ±50 ppm/°C; offset drifts are ±1 ppm of FSR/°C unipolar, ±50 ppm bipolar. Analog output ranges are ±1 and 0 to -2 mA; output impedances are 1.8 kΩ bipolar, 2 kΩ unipolar; compliance is -4 to 4 V; and internal reference is 7.6 V.

Power supply requirements are ±14.5 to ±15.5 V. Drain at the ±15-V rated supply is 7 mA. Sensitivity is ±0.02% of FSR/%V, at 15 V, ±0.002% at -15 V.

Prices of the 16-pin ceramic DIPs range from \$8.50 each for the BG and \$12.50 for the SG in 100 lots to \$13 and \$19, respectively, in lots of less than 25.

Circle 352 on Inquiry Card

Semi-Custom IIL Program Speeds Up Design Of Prototype Chips

SWAP (Stewart-Warner array programming), a concept in semi-custom LSI IIL that is claimed to permit 4-week delivery of first prototypes for tooling costs as low as \$1800, is based on the concept of a master chip with a standard pattern of circuits that have not been interconnected. An interconnection pattern for the master chip is designed and implemented according to each customer's requirements.

Stewart-Warner Microcircuits, 730 E Evelyn Ave, Sunnyvale, CA 94086 claims that IIL technology combined with implementation of the master chip technique offers distinct advantages in price and delivery. Gate costs as low as ½¢ each and the low tooling costs are said to give SWAP the following advantages over the conventional use of standard SSI/

Direct input and output of analog and digital signals to your computer.

RTP is a family of standard products that allows direct input and output of analog and digital signals to your general purpose digital computer.

The parameters of RTP design? Unprecedented reliability. Greatly reduced maintenance and ease of servicing. Less engineering design time for the system designer. Extending system life through non-obsolescence. Low cost.

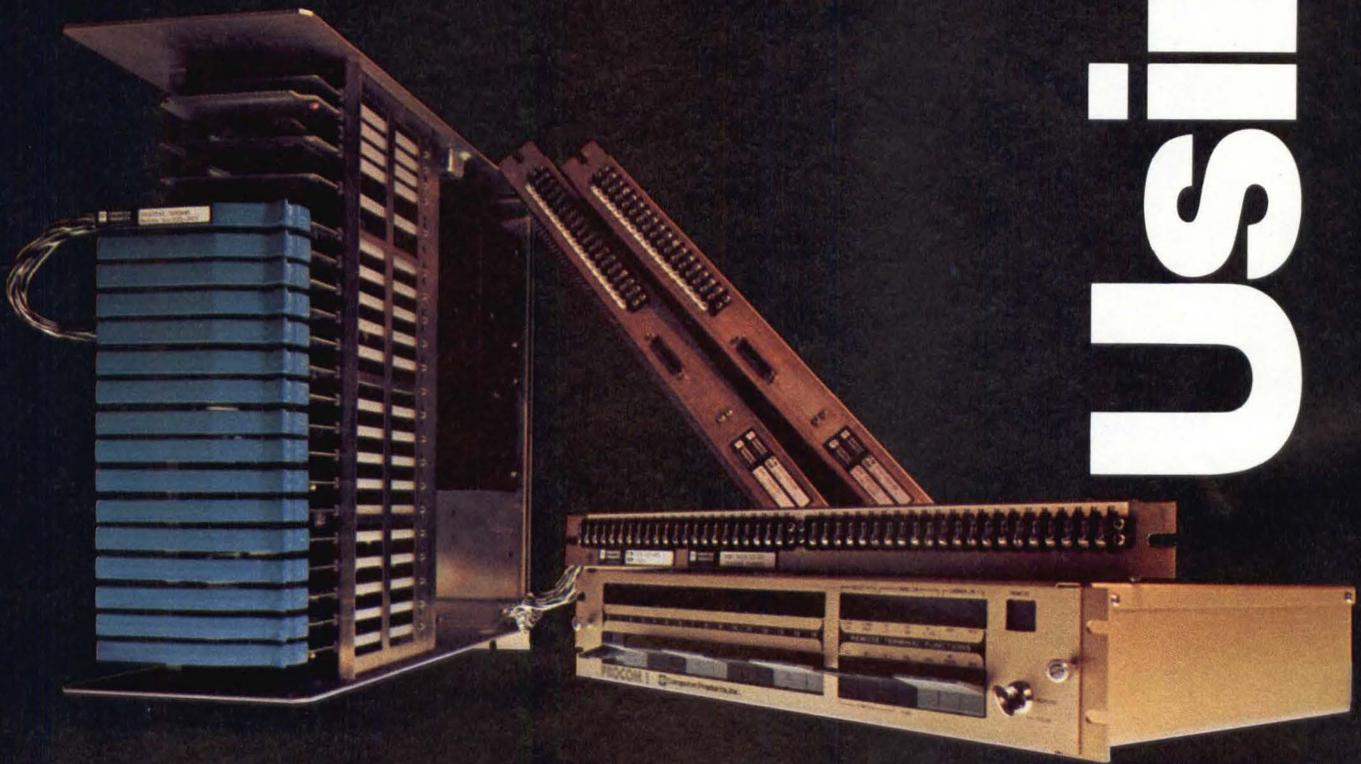
If you're involved in the design of a measurement and control system, we'd like to send you our

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g3

CIRCLE 26 ON INQUIRY CARD

UNRETOUCHED

MICROPHOTOS



Note rough jagged edges always present

Your IC lead frames look like this at 30X enlargement (unretouched). Because they are punched out of metal, the edges are rough, jagged and irregular. In contrast, the flat sides of the lead frame are smooth, even and perfectly plated.

Arrows indicate scars and abrasions made by rough edge of lead frame.



22X magnification, unretouched.

THEIRS

An ordinary edge-bearing socket contact after 5 insertions of DIP lead frame. Contact has been spread apart to show inside faces of contact. Notice how the contact has scars and abrasions from rough, irregular edge of IC lead frame. Electrical contact is degraded and resistance is increased. Reliability is obviously reduced.

Lead frame in place in an ordinary edge-bearing contact.



Arrows indicate contact surface still smooth, clean, free from abrasions.

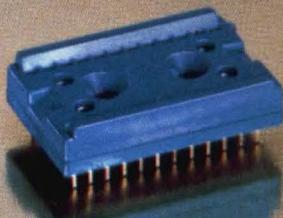
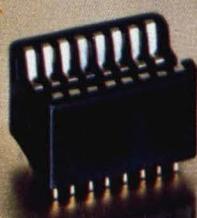


22X magnification, unretouched.

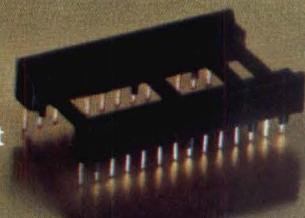
OURS

ROBINSON-NUGENT "side-wipe" socket contact after 5 insertions of DIP lead frame. Contact has been spread apart to show inside faces of contact. See how the RN contact—because it mates with the smooth, flat side of the IC lead frame—retains its surface integrity. This 100% greater lead frame contact results in continued high reliability.

Lead frame in place in RN "side-wipe" contact.



High reliability IC sockets ... we've got 'em all!



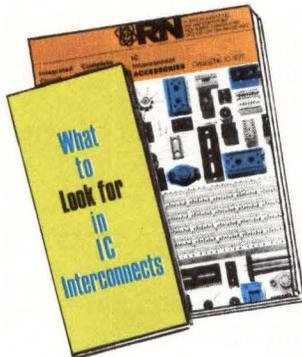
expose 'junk' socket problems

Secret of RN high reliability 'side-wipe' DIP sockets revealed by microphotos

Here's microscopic proof that high reliability Robinson-Nugent "side-wipe" DIP sockets make 100% greater contact than any edge-bearing socket on the market. This advance design provides constant low contact resistance, long term dependability—trouble-free IC interconnects. Yet RN high reliability DIP sockets cost no more than ordinary sockets!

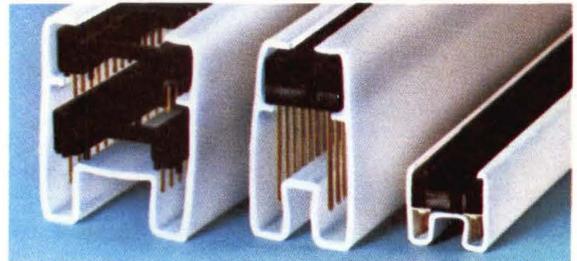


Get the high reliability that eliminates trouble. RN "side-wipe" DIP sockets make contact with the wide, flat sides of your IC leads. You get 100% greater surface contact for positive, trouble-free electrical connection.



WRITE TODAY

for catalog and informative book "What to Look for in IC Interconnects." Free from Robinson-Nugent—the people who make more kinds of high reliability IC sockets than anyone.

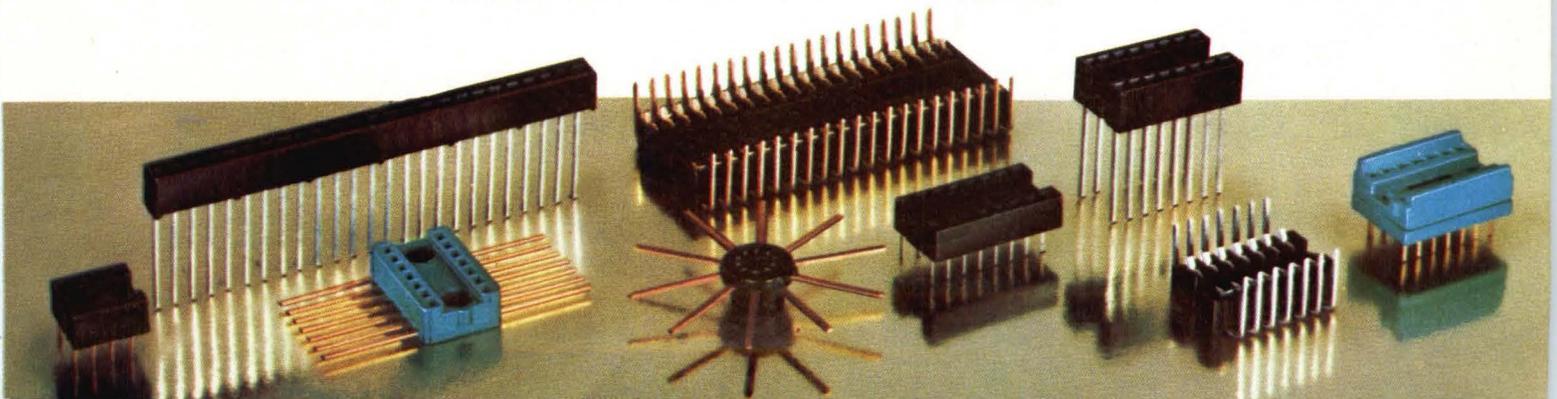


They're even packaged for high reliability. "Protecto-pak"® packaging delivers consistently perfect RN sockets to your production line—for automated or manual assembly.

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Call me, I'm interested. Circle 27.
Send product information. Circle 35.



MSI circuits: savings to the customer of 50% or more in direct IC costs; reduction in ICs required per system (one SWAP circuit replaces 5 to 100 standard devices); smaller physical size for less expensive PC boards and hardware, higher reliability, and smaller and less expensive system power supplies; reduced manufacturing costs per customer system with fewer IC insertions; simplified system checkout and repair; and reduced inventory control and procurement activity. IIL gates are in full compatibility with DTL, TTL, and CMOS ICs and discrete transistors.

Typical circuit functions that can be configured include logic gates, monostable and astable multivibrators, flip-flops, oscillators, and Schmitt triggers, with interface circuits available at each I/O pad. Two different versions of the chip are available: a 16-pin device with 208 gates and 14 interface circuits; and a 24-pin device with 408 gates and 22 interface circuits.

A custom design kit, a prerequisite for starting in this program, sells for \$25. It consists of a design manual (complete with vellum work sheets) and 15 sample devices.

Circle 353 on Inquiry Card

8-Bit Register Added To IC Filter Set

Completing a 3-part circuit set designed for digital filtering and signal processing applications up to 30 MHz, an 8-bit serial/parallel register is now available. The Am25LS22 includes a sign extend function for use with the 25LS14 multiplier and will be second-sourced by other manufacturers as the 54/74LS322.

The circuit is available from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086 in molded or hermetic DIP and specified for operation over commercial or military temperature ranges. All undergo 100% processing to the requirements of MIL-STD-883.

Prices in 100-piece lots range from \$4.60 each for a molded DIP rated from 0 to 70°C operation to \$9.20 for a hermetic DIP rated for -55 to 125°C. Dice are also available at \$4.25 for the commercial range and \$6.80 for the military.

Circle 354 on Inquiry Card

Multiplexers Combine Accuracy and High Speed in 16-Pin DIPs

MUX 202-M and 203, 8-channel single-ended multiplexers, are designed for use in multiple-output, time-shared A-D converters, transmitters, and receivers. Both are over-voltage protected on analog and digital inputs and are protected against channel interaction when the power is removed. For 16-channel applications, two of the 16-pin hermetic DIPs can be connected in less space than comparable 16-channel units.

Key specifications of the units from Hybrid Systems Corp, Crosby Dr, Bedford, MA 01730 are 0.01% accuracy, 0.01% crosstalk at 10 kHz, 0.5- μ s address time, TTL/CMOS compatibility, and ± 15 -V power requirements. The 202-M is fully processed to MIL-STD-883.

Circle 355 on Inquiry Card

Add-In Memories Meet LSI-11 Requirements

Two Mastermind™ 16-bit word semiconductor memory modules designed for complete compatibility with Digital Equipment Corp's LSI-11 computer have been announced by Memory Systems, Inc, 3341 W El Segundo Blvd, Hawthorne, CA 90250. Both are rated at 500-ns access time with 800-ns cycle time. Power required is 12 V at 0.5 A and 5 V at 2 A. Prices will start at \$875 for an 8K version (model 2000-8) and \$1450 for a 16K version (model 2000-16) in single quantities.

Circle 356 on Inquiry Card

Micropower Voltage Detector Circuits Have User-Settable Levels

ICL8211 and 8212, settable micropower voltage detector circuits, are capable of measuring between 2.0 and 30 V. Both devices maintain virtually constant power supply currents, typically 20 μ A, over the input voltage range during their off or "sensing" states.

Output of the 8211 in its on state is current limited to 7 mA, suitable for directly driving a LED lamp without a current limiting resistor. Output of the 8212 may vary, for applications demanding a variable output or higher current levels.

Both of the devices from Intersil, Inc, 10900 N Tantau Ave, Cupertino, CA 95014 can be connected to provide an output exhibiting an hysteresis effect, making them suitable for indicating transitory voltage excursions beyond pre-set limits, even after the input voltage has returned to an acceptable level.

Prices at 100 pieces for either device are \$1.50 for use from 0 to 70°C, packaged in an 8-pin miniDIP. Units are also available in TO-99 packages for use in commercial (0 to 70°C) or military (-55 to 125°C) ranges.

Circle 357 on Inquiry Card

Alternate Source Named for Mostek 4K RAM

Fairchild Camera and Instrument Corp and Mostek Corp jointly announced that Fairchild's MOS/CCD Products Div will be an alternate source for the Mostek MK 4027.

Fairchild has been supplying the 16-pin, 4096-bit dynamic RAM for the past year, and is now in high volume production for applications with access time requirements in the 200- to 350-ns range.

First shipments from Fairchild are scheduled for the fourth quarter of 1976.

Bipolar Producer Adds IIL Capability

Micro Components Corp, 99 Bald Hill Rd, Cranston, RI 02920, a custom producer of linear ICs, is now offering IIL circuitry as part of its regular product line. The IIL process offers the low powered advantages of CMOS with bipolar speed, and is said to provide other advantages including reduced costs, smaller equipment size, lower component count, and better inventory mix. Digital and linear circuit designs can be combined on the same chip. Many interface problems that previously existed with MOS designs are also resolved.

Because of IIL's extreme simplicity, up to 3500 gates or over 10,000 memory bits can be placed on one high yield chip. The speed-power can be as low as 0.13 pJ, at speeds nearly as fast as TTL. Power dissipation by the thousands of gates will be no more than that of existing 100-gate devices. In situations

Once you make up your mind not to be a follower, there's only one alternative.

You lead. It's that simple. As 3M did back in 1971 when we introduced the "Scotch" Brand 1/4" Data Cartridge. You know the changes it caused in the industry.

Then, in '73, we introduced the people-proof, jam-proof, wear-resistant DCD-3 Drive. It wasn't the first on the market, it was simply the best, with design features that confirmed 3M's engineering leadership. But if you're committed to this business, as we are, you're a slave to constant discontent.

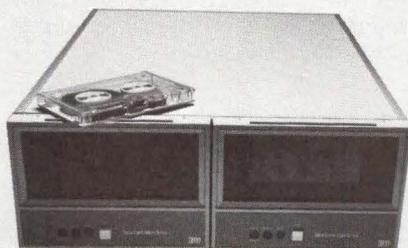
So now, we'd like to introduce you to our new DCS-3000 series, an ANSI-formatted system that allows one formatter to operate up to

8 drives. The media is our standard DC300A Cartridge with a total capacity of 23 million bits. Perhaps its greatest advantage is the ease with which you can integrate it into a system. Only one cable to the user's logic is required. And the complete set of status flags is available to indicate readiness to

perform a given function. There's an error check during both read and write operations, and an error flag to indicate errors. There's an automatic search (90 ips) to tape mark, and a variable-length erase function.

It adds up to this: now the system designer has a reasonably-priced peripheral that delivers both data reliability and data interchange capability. We're certain our competitors are going to be very interested in this new system. And if you are too, just write 3M Company Data Products, Dept. 129, Mincom Division, Bldg. 223-5E, 3M Center, St. Paul, Minnesota 55101.

**All our competitors
can do is follow us.**



DATA PRODUCTS **3M**
Mincom Division COMPANY
3M CENTER • SAINT PAUL, MINNESOTA 55101

where high speed is not a requirement, the chips will provide micro-watt power dissipation while supplying high current output drive capability.

Circle 358 on Inquiry Card

Analog IC Devices Meet Mil Specs

Five analog IC devices added to its high reliability product line by Signetics' Military Div, 811 E Arques Ave, Sunnyvale, CA 94086 are available over the full military temperature range and are processed in accordance with MIL-STD-883, classes A, B, and C. Two dual operational amplifiers, LM158 and SE532, are typically \$5.53 and \$5.60 each in 100-piece lots of class B rating. SE515 differential amplifier, DM7820 dual line receiver, and DM7830 dual differential line driver are \$14.63, \$22.68, and \$22.68, respectively, at the same rating.

Circle 359 on Inquiry Card

Support Center to Aid LSI Application

An LSI System Support Center located in West Palm Beach, Fla has been announced by Dr Steward S. Flaschen, ITT vice president and deputy general technical director. Its purpose is to assist ITT equipment and systems divisions in applying LSI circuits to their product lines. Headed by technical director Barry H. Soloway, the facility is intended "to provide increased capabilities for the design, selection, and testing of standard and custom LSI circuits." Although located at the site of the ITT Semiconductors plant, the center will operate as a separate entity, reporting to ITT World Headquarters in New York.

Generator Chip Offers Choice of 16 Baud Rates

A single baud rate generator, COM 5026, provides any one of 16 program or switch selectable output frequencies and is compatible with

dual baud rate generator COM 5016. It offers 16 asynchronous/synchronous baud rates, direct UART/USRT compatibility, a reprogrammable ROM for generating other frequencies, TTL and MOS compatibility, on-chip input pullup resistors, accuracy to within 0.01%, and a 50% duty cycle.

Produced by SMC Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11787, the chip is a silicon-gate n-channel MOS LSI device made by the Coplamos[®] process. With the addition of a crystal, it provides an output of any of 16 externally-selectable frequencies. The reprogrammable frequency-select ROM can be programmed to generate other frequencies from other crystal or external-input frequencies. Baud rate is externally selected by a 4-bit address. The 14-pin ceramic DIP device operates from 0 to 70°C and can be driven from a TTL level input or by an external crystal.

Circle 360 on Inquiry Card

IC Comparator Operates At Up to 100M Samples/s

High speed comparator SP750B features a maximum settling time of 2 ns and a propagation delay of 3.5 ns. Input and output levels are ECL-compatible.

Additional features of the device from Plessey Semiconductors, 1674 McGaw Ave, Irvine, CA 92714 that are said to reduce overall system hardware count and increase system reliability include an integral latch function that allows use in the hold mode, integral gating for decoding comparator outputs in a multilevel comparator chain, wired-or outputs for decoding for 4-bit lines, and precision switched current sources that can be summed for A-D conversions.

Used in a 4-bit parallel ADC, the comparator operates at rates up to 100M samples/s. In a complete A-D-A system, it operates at rates up to 30M samples/s with 8-bit accuracy.

Circle 361 on Inquiry Card

Power Drivers Added to Digital Interface Line

Twelve monolithic peripheral power drivers rated for continuous operation over the 0 to 85°C range have been added to its digital interface family by Sprague Electric Co, 555 Marshall St, North Adams, MA 01247.

Series UDN-3600 dual 2-input drivers are designed for loads such as incandescent lamps, LEDs, memories, heaters, and other noninductive loads of up to 600 mA at 80 V; series UDN-5700 dual and quad drivers with transient protected outputs are designed for use with inductive loads such as relays, solenoids, or stepping motors at up to 1.2 A (four drivers) or 600 mA (one driver) at 80 V.

All devices are available with AND, NAND, OR, or NOR digital logic inputs which are suitable for use with standard low level digital logic. Packaging is in 8- and 16-pin DIL plastic cases.

Circle 362 on Inquiry Card

Plastic DIP Op Amp Serves as Signal Processing Preamp

A pin-for-pin replacement for Raytheon's A739, the XR-4739 dual low noise operational amplifier IC is designed primarily for preamplifiers in signal processing equipment. It is available as a molded plastic 14-pin DIP, and operates over the 0 to 75°C commercial temperature range. The product from Exar Integrated Systems, Inc, 750 Palomar Ave, Sunnyvale, CA 94086 features S/N ratio of 76 dB (RIAA 10-mV ref), channel separation of 125 dB, unity gain bandwidth of 3 MHz, output short-circuit protection, and 0.1% distortion at 8.5-V rms output into a 2-kΩ load.

Circle 363 on Inquiry Card

8-Bit DAC Is Microprocessor Compatible

Compatible with any 8-bit microprocessor, the 7462 DAC operates on a single 5-V supply and provides 0- to 3-V analog output. The 8-bit device is available from Optical Electronics Inc, PO Box 11140, Tucson, AZ 85734 in a 16-pin DIP. Features include standard binary digital coding, 00000000 digital input code for 0 analog output, ±100-ppm maximum error, 100-ppm/°C maximum scale factor drift, 30-ppm/°C maximum linearity temperature drift, -55 to 100°C operating temperature range, and 30-ns maximum settling time to ½ LSB. □

Circle 364 on Inquiry Card

3M got there first. Again.

We put the features of our ¼" DC300A cartridge into a shirt-pocket size. Then we designed a drive—small in size, small in price, for applications where high data reliability must be combined with compact size.

The new DCD-1 system will fit in a 5 inch cube—the cartridge alone measures just 2.4 x 3.2 x .5 inches. Enough about size, let's talk performance.

The drive records *full width* across the entire tape, which virtually eliminates errors. It has an encoding method virtually independent of tape speed, and control logic that prevents the drive from accepting any command that might harm the cartridge.

The electronics are designed to give the system engineer the greatest application flexibility—

has byte oriented data input and output and 100,000 byte storage capacity. It's also designed to permit battery operation.

This new system will change the industry much like our ¼" cartridge. So it's time for our competitors to play follow the leader again—if they can. That's the story in a nutshell. Just send the coupon for more details.

**All our competitors
can do is follow us.**



Mail to: 3M Company
Data Products, Dept. 125
Mincom Division, Bldg. 223-5E
3M Center, St. Paul, Mn. 55101

I'm interested in receiving information on your DCD-1 Drive.

Name _____
Title _____
Firm _____
Address _____
City _____ State _____ Zip _____
Phone _____

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Mincom Division **3M**
COMPANY
3M CENTER • SAINT PAUL, MINNESOTA 55101

CIRCLE 29 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Computer Complex Automates and Protects Rapid Transit System

Rapid transit has always been a target for complaints by commuters and the delight of politicians who promise in election campaigns to remedy whatever their constituents claim is wrong at the moment. Mr and Ms Ordinary Citizen called their city council when they had to wait in the snow for a street car that was delayed by a frozen switch; Jesse James became very angry when the stagecoach from Dodge City was ambushed by Indians before he and Frank could attack it; and likely Julius Caesar was very unhappy when several slave rowers broke their oars and slowed down his galley while he was on his way to meet Cleopatra. Modes of transportation have changed—but riders are still just as displeased if their respective vehicles do not arrive on time.

Responsible agencies in many large cities are now seriously attempting to remedy the problems, and of

course automation and digital computers are playing key roles. Such corrective actions are usually slow-moving in cities that have existing systems because modifications can be costly, time-consuming, and difficult to carry out without interfering even more with transportation schedules. However, in cities where all new transit systems are being built, such as Sao Paulo, Brazil, computer-controlled configurations can be constructed with minimum hardship on commuters.

Sao Paulo Metro

Over six million of the present seven million inhabitants of the rapidly growing Sao Paulo metropolitan area depend on some form of surface transportation, necessitating a reliable and safe rapid transit system. The overall plan for this system includes two intersecting lines, one of which is already in operation.

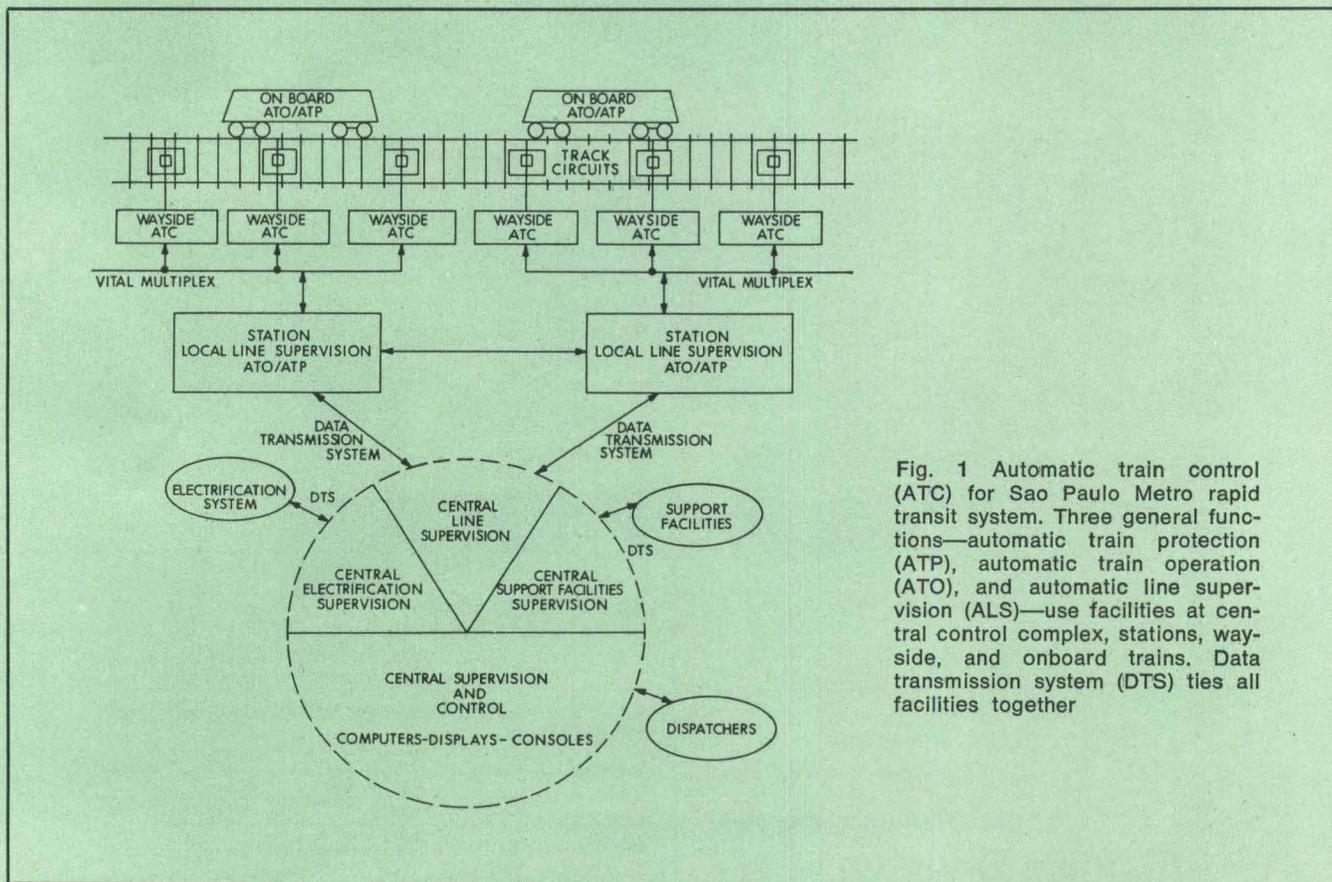
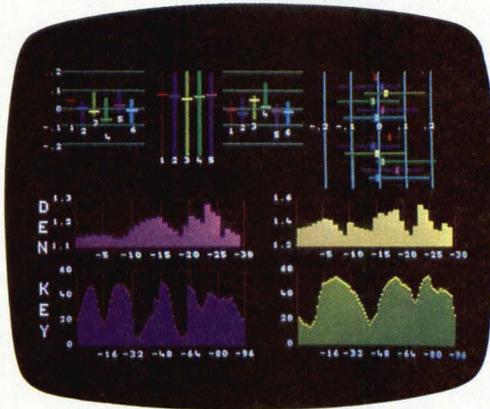


Fig. 1 Automatic train control (ATC) for Sao Paulo Metro rapid transit system. Three general functions—automatic train protection (ATP), automatic train operation (ATO), and automatic line supervision (ALS)—use facilities at central control complex, stations, wayside, and onboard trains. Data transmission system (DTS) ties all facilities together

What You Need Is What You Get.

Ramtek's new RM9000 modular graphics and imagery system gives you expandability, economy and flexibility.



Process Control: Color printing press.



Medical Imaging: Nuclear heart study.

Select The Performance You Need.

The RM9000's total modularity lets you select the exact performance you need to fill your particular application. You pay only for the performance you need. Nothing more. And that's like money in the bank.

Add On As You Have To.

As your needs change and grow, the RM9000's capability will grow right along with them. A comprehensive list of options such as expansion from black and white to grey scale or color—even a complete range of interactive peripherals and additional independent channels.

Microprocessor-Controlled Raster Scan.

The RM9000 is the first raster scan graphics and imagery system to be totally microprocessor

controlled. That means you can implement a higher-order user language to minimize programming costs without a sacrifice in system throughput.

Functional. Reliable. Maintainable.

High reliability is the direct result of intensive testing of components and systems prior to shipment. Solid state components and printed circuit construction are used exclusively. Result? No special preventive maintenance measures are required. In fact, the RM9000 can be pre-programmed with self-diagnostic capability.

You Need To Know More.

To fully appreciate the RM9000's capability, you need more details. Call or write Ramtek Corporation, 585 N. Mary Ave., Sunnyvale, CA 94086. (408) 735-8400.

ramtek
Our Experience Shows

Come visit us at the ISA Show, Booth Nos. 101, 103, and 105.

CIRCLE 30 ON INQUIRY CARD

If you can find any other logic board tester on the market that has all these features, we'll buy it for you.

Power-fail protection to safeguard software system.

Automatic loader provides one-step bootstrap procedure for system initialization.

Most complete service program available. One-year on-site warranty on entire system.

Simulator generated test program on diskette for convenience of program distribution.

LSI-II mini-computer with 16K words of memory and direct memory access.

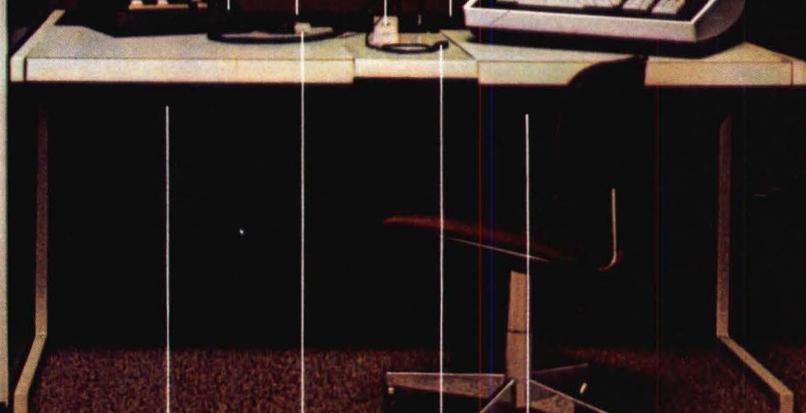
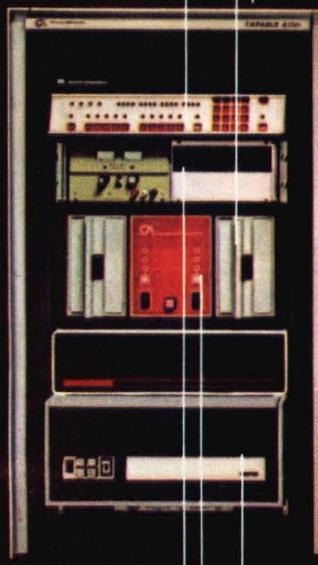
Console with built-in digital voltmeter for operator convenience.

Simulation capability can be added to test station or provided as stand-alone for fast, efficient test generation.

Both hardware (TAPS) and software (Simulator) modeling available for fault verification of the test program.

16K Core Memory, expandable to 64K.

Alphanumeric CRT for faster and quieter operation.



Wide range of UUT power supplies available.

Single or dual 256K byte floppy disk drive for low-cost mass storage.

Optional 5M byte dual moving head disk drive provides increased capacity for even the most complex boards.

Analog capability for testing hybrid boards.

UUT interface pins available in 3 types and expandable to 767 pins.

Guided Fault Isolation for fast troubleshooting by a low-skilled operator using a guided probe.

Added GFI capability using our new Clever Clip which can handle IC's up to 24 pins.

Our family of CAPABLE logic board testers are in a class by themselves. That's why we can make an offer like this and not worry for a minute that it'll be put to the test.

Because the only way to match our features is to custom-build or custom-order. And even then you can't match our pricing (starting under \$22,000).

To begin with, all CAPABLE testers have our own powerful, ComputerAutomation LSI-II 16-bit computer with 16K words of memory and direct memory access for quick execution of the test program.

Next, there's Guided Fault Isolation (GFI) with both a single point probe and our new Clever Clip™ which can handle IC's up to 24 pins. This not only makes testing faster, but also minimizes the chance for error because the operator has less to do. There's even a special readout that tells you if the clip isn't making proper contact with the pins.

Both our probe and Clever Clip have individually-programmed threshold settings, which allow them to adjust automatically as different logic levels are probed.

CAPABLE testers are available with three types of pin electronics—TTL, CMOS, and programmable. So we can tailor a test

system to your specific needs and minimize fixturing and adaptation costs when your needs change.

And since our entire system is modular, you can

add pin electronics up to 767 pins as your boards become larger and more complex. You can add additional memory as your test routines become larger. You can add new logic families. Or you can convert your CAPABLE into a complete analog test system. All as you need it.

Here's even more flexibility. An add-on simulation capability

with a unique offer attached: We'll buy it back at full price anytime your needs require that you upgrade to one of our larger simulators.

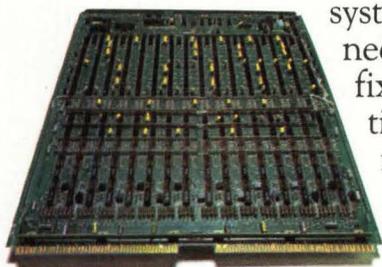
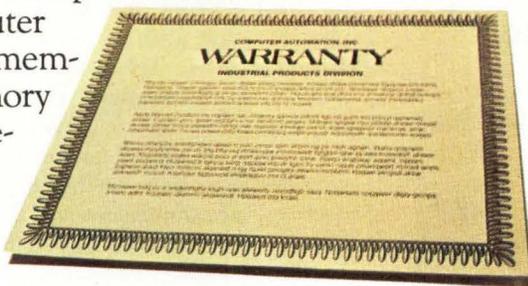
The list of CAPABLE features goes on: Automatic Test Generation (ATG). Fault Detect Verification (FDV). Analog testing capability. A ticket printer for producing hard copy failure reports. Even an alphanumeric CRT input/output terminal with standard office typewriter keyboard.

And CAPABLE testers carry the most complete support program available. Starting with a one-year, on-site warranty on the entire system—no exceptions. And including one week of technical training at start-up and on-going engineering assistance as you need it.

We're uniquely able to help you solve your testing problems because we've gone to school on our own testing problems. Our sister division produces over 35,000 boards a year, as the industry's second largest shipper of OEM mini-computers. And, using CAPABLE testers, they experience the industry's lowest percentage rate of field failure.

So before you buy a logic board tester, compare CAPABLE's features against the others. And if you find one (custom-builts don't count) that out-features and out-performs us for the same price, we'll buy it for you.

For details, write or call us. In the U.S.A., 18651 Von Karman, Irvine, CA 92713, Tel. (714) 833-8830 or in Europe, CAI Ltd., Hertford House, Denham Way, Maple Cross, Rickmansworth, WD3 2XD Hertfordshire, England, Tel. Rickmansworth 71211, Telex 922654.



ComputerAutomation
Industrial Products Division

This offer expires Oct. 31, 1976

CIRCLE 31 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

More than half a million passengers daily ride the 17-km (10.5-mi) North-South line and the total is expected to reach one million; by 1985, when the 27-km (17-mi) East-West line is fully operable, one and a half million more passengers will be riding that line every day. Trains of six cars now average 34 km/h (21 mph) but can operate at up to 100 km/h (62 mph).

In many ways similar to San Francisco's BART system, which is spread over 75 miles of double track, Sao Paulo's Metro, currently with only 10 miles of track, is approximately 60% as complex in terms of equipment. Where BART includes 34 stations along its route, Metro has 20 stations on less than one-seventh the length of BART's track. Therefore, the overall control and automation configuration for Metro must be highly sophisticated.

The complete automated control system (ATC) for Sao Paulo Metro, designed and supplied by Westinghouse Electric Corp, Pittsburgh, Pa, provides three general functions: train protection, train operation, and line supervision (Fig. 1). Present ATC components include a central control complex about midway along the North-South line, local units at each of the 20 stations and at the train yard and maintenance depot near the south end of the line, wayside equipment, car-mounted control packages, and the communications equipment that links the system together.

Communication between local terminals which monitor field devices and the central control computers is provided by a high speed digital data transmission system (DTS). Telemetry equipment monitors each of 10,000 points on the system at least once every two-thirds second and communicates with the computers over voice grade telephone lines (Fig. 2). Computers, consoles, displays, and loggers at the central control complex are interfaced to the online ATC via DTS. Signals are processed—both to and from the complex—by 30 modems. A 28-bit word (Fig. 3) was chosen to accommodate the significant amount of processing necessary at each terminal.

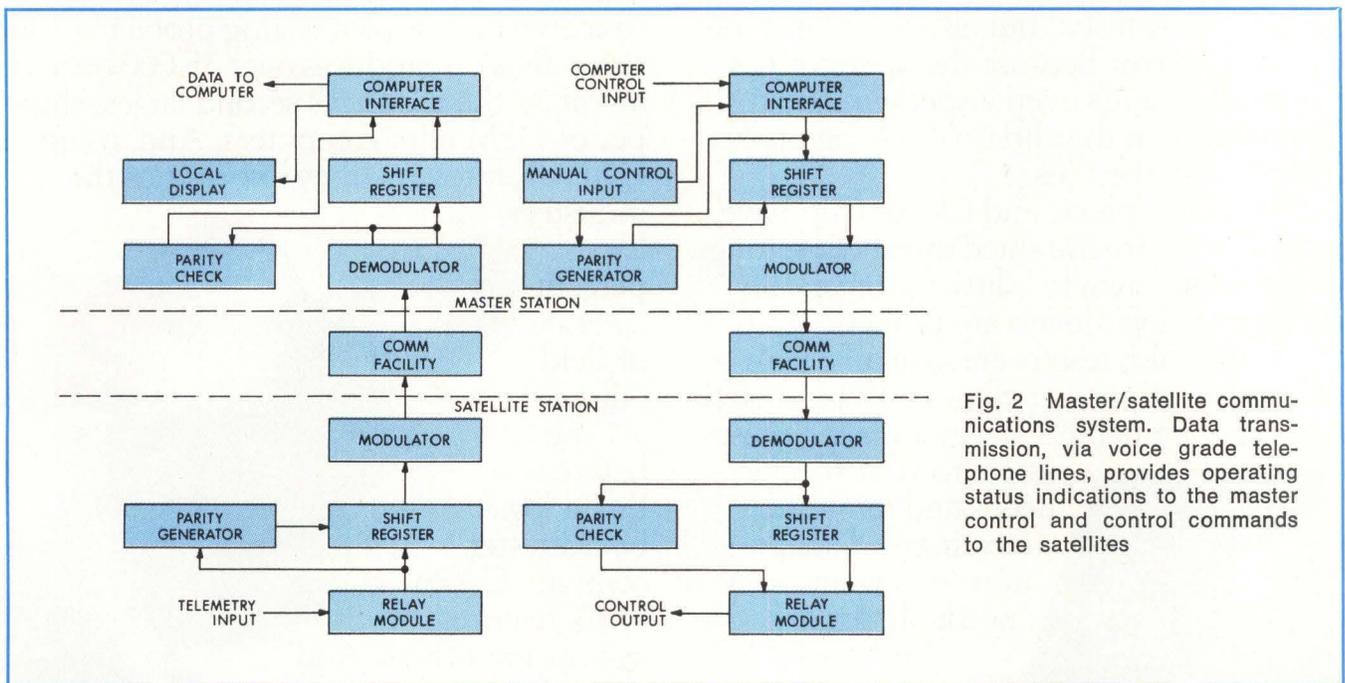


Fig. 2 Master/satellite communications system. Data transmission, via voice grade telephone lines, provides operating status indications to the master control and control commands to the satellites

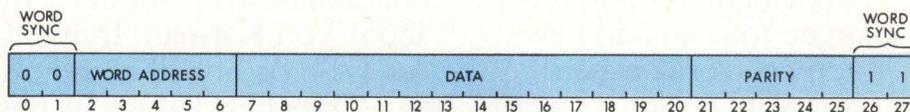


Fig. 3 Metro system data word format. 28-bit word covers data and address bit requirements, message security, and word synchronization

Power on or power off, reliable core holds the data. That's why system engineers are taking a new look at Ampex MCM, the Micro-computer Core Memory.

Sure, you can use semiconductor memory. Maybe smaller and cheaper at first glance. Then, the first time somebody plays with the power, you lose data. So you reload. That costs money. Or you design battery back-up. That also costs money.

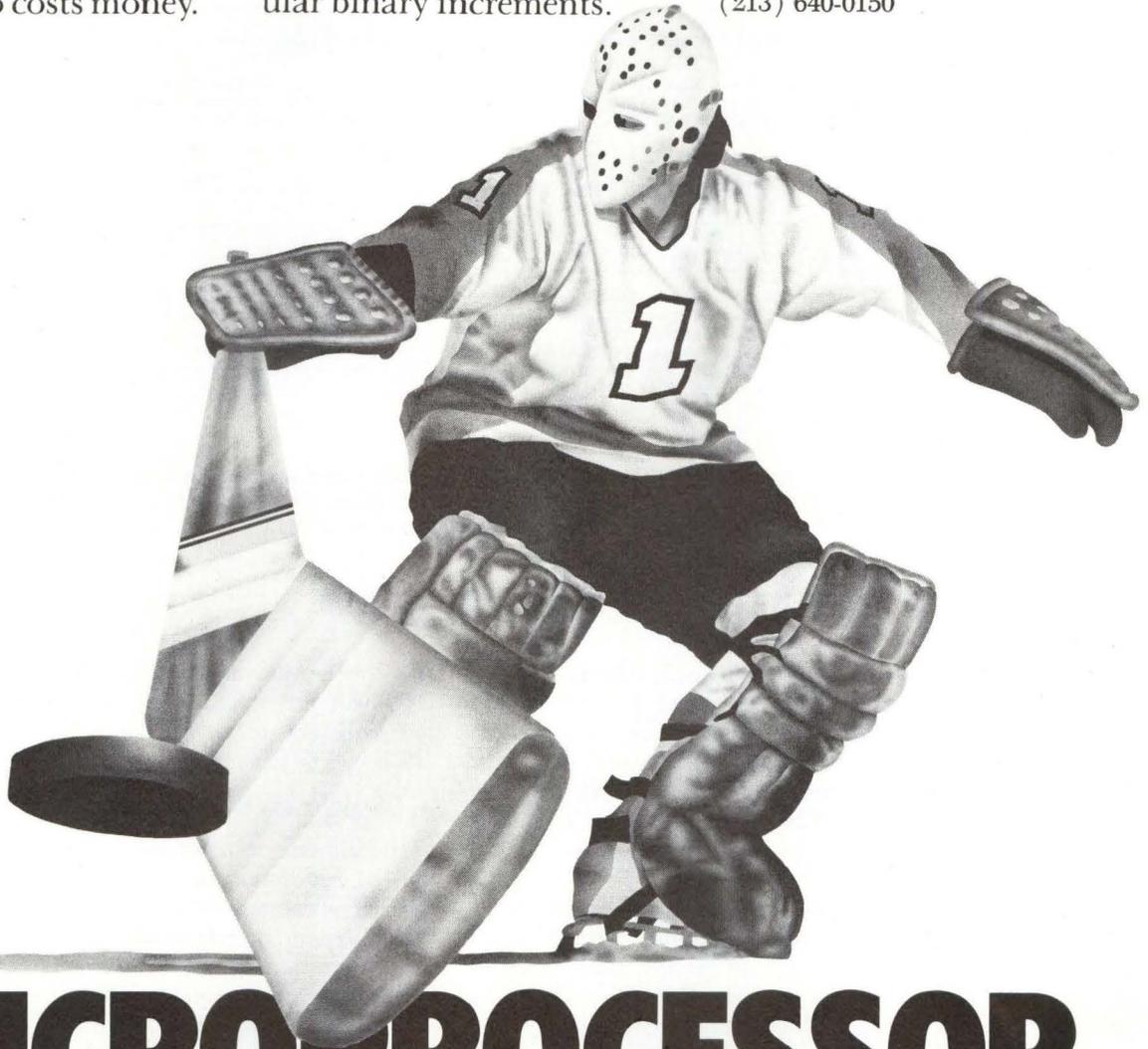
Matter of fact, *every* system provision for data preservation costs money. In the end, core costs less than semiconductor memory.

Get Ampex MCM. Ready to plug in and operate. No fussy assembly of components on boards. No support circuitry. Nothing but the steady reliability of core. Word lengths from 4 to 18 bits, storage capacity from 256 to 4096 words. In all popular binary increments.

Build Ampex MCM into your system, and you won't squander time and personnel bringing programs back up after the power goes down. Block the power play. Get Ampex MCM.

AMPEX

Ampex Memory Products Division
200 N. Nash St.
El Segundo, CA 90245
(213) 640-0150



MICROPROCESSOR CORE MEMORY BLOCKS POWER PLAY

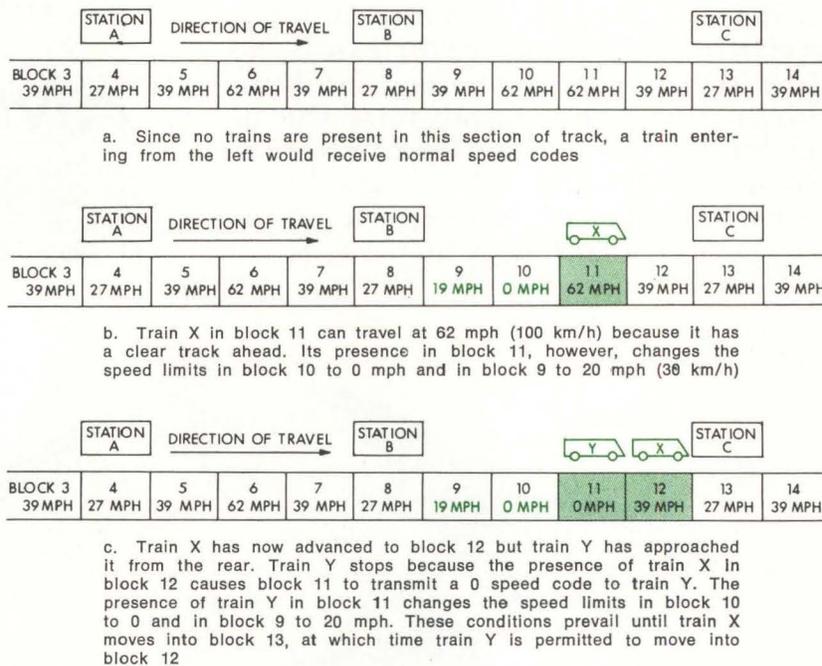


Fig. 4 Typical speed commands for Sao Paulo Metro system. Speeds shown are the maximum permitted in each 500-ft (152-m) block as determined by such factors as curves, grades, and distance from a station

Data transmitted by DTS are constantly checked for errors.¹ Any disagreement between parity bits will inhibit transfer of data to output circuits. Use of a 5-bit cyclic code detects all single and double bit errors, regardless of where they appear in the message, and all burst errors up to five bits. Burst errors of greater than five bits have a better than 96.9% chance of being detected.

To improve detection capability, a sync bit verification check is made during each decoding process. In addition, a carrier detection circuit in the modem receive circuitry acts effectively as a signal-to-noise (S/N) ratio detector. This will inhibit data transfer for S/N ratios below 12 dB.

A feature of the system is the use of an idle or status word, an internally generated message. A unique station address, part of the status word, is hardwired to each master and satellite DTS terminal. The status word is generated from the satellite terminal once during each scan of the remote input data, and from the master terminal whenever no other data are being transmitted from the computer. Each time the status word is received by a terminal the station address is logically compared with the local station address. A mismatch causes the DTS to inhibit further updating of its output registers and start a 5-s timer.

If the condition does not clear within five seconds, the DTS will enter a fail-safe mode which resets all output registers to a predetermined state and a local alarm will be generated.

Automatic Train Protection

Each station or multiple-station control zone is the hub of an automatic train protection (ATP) system that involves only the trains within that area. This safety system detects trains within its zone, maintains safe separation of trains, prevents trains from exceeding speed limits, and controls movement of trains through track intersections.

ATP moves trains according to speed profiles set up to prevent any accidents. Fixed block track circuits determine whether or not a block, usually 500 ft (152 m), of track is occupied. Signals sent to trains within the zone specify the speeds at which the trains may run, dependent upon the block each occupies (Fig. 3). Speed codes for the system are 0, 10, 30, 44, 62, 75, 87, and 100 km/h (0, 6, 19, 27, 39, 47, 54, and 62 mph).

Basically, as described in more detail in the caption to Fig. 4, the detected presence of a train in one block causes the computer to order speed adjustments in preceding blocks to be sure any following train

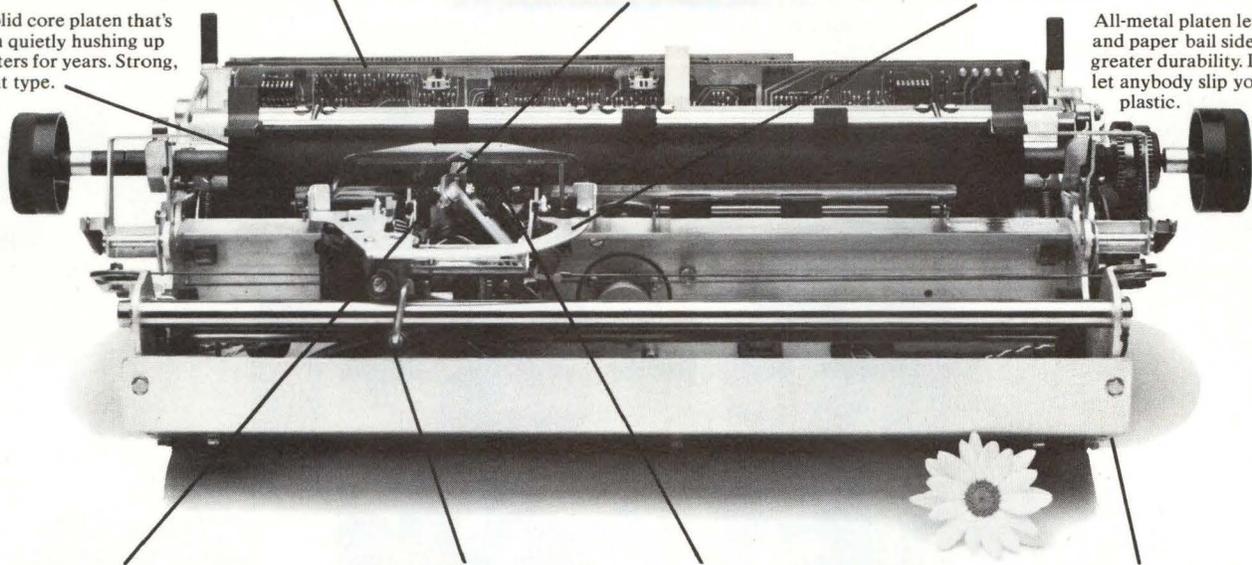
Solid-state electronics reduced to a few rugged "snap-in, snap-out" boards. Less to go wrong, more to go right.

A six-intensity hammer that knows the difference between a love pat and a punch. Each character, each punctuation mark gets just enough of a push to make the best impression.

Our fast ribbon lift makes sure only the ribbon lifts — not the whole cartridge. Greater speed, and a more natural typing rhythm and touch.

A solid core platen that's been quietly hushing up printers for years. Strong, silent type.

All-metal platen levers and paper bail sides for greater durability. Don't let anybody slip you plastic.



A positive printwheel latch to keep your daisy wheel properly positioned. No springs attached.

Carriage ball bearings for less friction, better vertical print registration, and fewer service problems. Best way to ride the rails.

Thirty-eight daisy wheel fonts to choose from including German, French, and Arabic Naskh. Good chance we speak your language, too.

Built to withstand the rigors of 100 characters per second. Currently delivers 30, 45, or (the industry's first) 55 cps.

Planned unobsolescence.

Call us old-fashioned.

Qume just believes continuity of product is everything. Savings in design, spares provisioning, training. So all Qume products are part of a continuing family. Not a designer-gone-berserk whim factory.

That's why the brand new 1976 Sprint Micro 3 pictured above is basically the same as the first Qume character printer we ever built. Each and every mechanical part is retrofittable, from the six-intensity hammer to the smooth-sailing carriage ball bearings.

So that any computer, terminal, or word processing system builder can buy Qume printers with the comforting knowledge that he'll face no printer-switching in midstream.

It's an interesting philosophy. (Made a big name for a small German car manufacturer a while back.)

And it's a sound philosophy we're committed to. Whether it's the industry's first true microprocessor-controlled character printer, our Sprint Micro 3. Or Qume's new WideTrack™ — 26 inches of bi-directional printing power.

All well and good, you might observe, but why buy Qume?

Because our unobsolescence philosophy is part of The Plan. A plan built on one simple rule: We don't compete with our customers. We don't make WP systems. We don't make terminals. We don't make computer systems. We have only one business — the printed word. And you get the best product we'll ever make.

Which leads us to believe, the only thing obsolete about Qume is its competition.

Qume®
the printed word

2323 Industrial Parkway West, Hayward, CA 94545 415/783-6100

25-bit words:

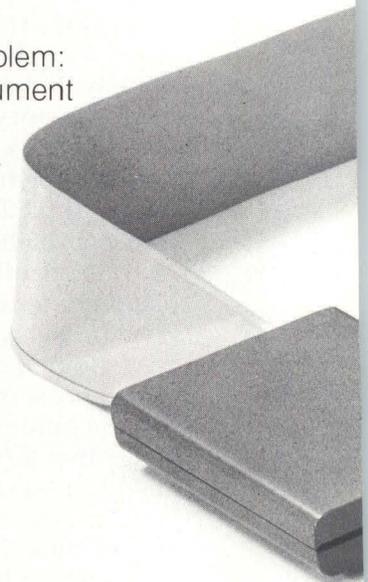
Biomation's 16+8+1 answer to μ Processor analysis.

The first microprocessor analyzer that really analyzes.

Biomation has developed a new instrument to solve a new problem: How to get inside the mind of your microprocessor. The instrument is our 168-D. The Mind Reader.

In the process, we've invented a new word. 25 bits long. Contains 16 bits of address, 8 bits of data, and one bit that tells you whether your machine is reading or writing. All in hex characters, just like your program listing.

The Mind Reader starts by capturing up to 256 of those 25-bit words at synchronous rates as fast as 10MHz. That's fast enough for anybody. You can dial in a hardware breakpoint and step your system through its program. Or you can monitor your system as it runs free. But that's just the beginning. Now watch:



First, the Big Picture

The Mind Reader takes a first macro-bite out of the territory you're investigating. 256 big words. In Memory Mode you can see the areas of memory where the action occurred. (You're writing into ROM, for heaven's sake!?)

Then zoom in!

The 168-D gives you a movable cursor that locks onto a location and stays with it through the analysis modes. Once you spot the action you've been looking for, stake it out with the cursor and switch to Page Mode. That gives you the address, data, and read/write information.

Now: A whole new perspective . . .

You've found the program, now switch to Sequential Mode and find out **how it got there**. Where were you coming from, and where did you go from there? Study all time relationships. A powerful new way to analyze the problem!

By switching to the List Mode you display the twenty words surrounding the cursor location you selected in the Page Mode. Address and data are presented in hex along with the R/W bit to let you compare the sequence to your program listing.

In summary: The 168-D lets you record with respect to time and analyze with respect to location.

It's the first microprocessor analyzer that really analyzes. You can put it to work today on **8080A** and **6800** problems. Personality modules for other μ P's are currently under development.

So if you're working with microprocessors and want to know whether your software or hardware is giving you problems, Biomation's 168-D Mind Reader will tell all: What happened . . . where . . . and when. You've got to get the data sheet.

Circle the number below. Better yet, call Biomation for a demo.

Biomation, 10411 Bubb Road, Cupertino, CA 95014, (408) 255-9500.

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DIGITAL CONTROL AND AUTOMATION SYSTEMS

stops before reaching the occupied block. Digital signals to the trains, sent along the rails, are coded by frequency-shift keying (FSK) of audio frequency signals.

Automatic Train Operation

Also a local control function, automatic train operation (ATO) operates the trains from start to stop within safety parameters provided by ATP. It opens and closes doors, accelerates and decelerates trains at the appropriate programmed rates, controls train speed according to schedule performance, controls train dwell time at the station, and reverses train direction at predetermined points (Figs. 5 and 6).

A 2-conductor, encapsulated, flat cable, with conductors crossing one another every foot, is laid along the third rail coverboard at each station. As a train approaches a station, an onboard antenna senses the crossovers. Then a stored computer program determines the distance to go and produces braking commands that bring the train to a smooth stop within 1 ft of the target.

FSK signals in the rails are detected and decoded into speed and other ATO commands. A permitted maximum speed is compared to the true vehicle speed as derived from the pulsed output of a tachometer driven by one axle of the train. If true speed exceeds permitted speed, the propulsion control is removed and brakes are automatically applied. Otherwise, a train is controlled within an accuracy of ± 2 mph.

Automatic Line Supervision

Some ATO functions such as dwell times, accelerating and decelerating rates, running speeds, station run-through, and routing are modified by automatic line supervision (ALS). This supervisory control system (Fig. 7) includes both local and central functions.

Local line supervision functions—all automatic—include train ID decoding, route request, route designation, passenger station sign control, and dwell control. All such functions are supervised at station-level controls.

Central line supervision, however, is based at the central control complex. Train schedules are stored in a computer which controls and supervises train routing, station dwell times, train performance adjustments, train dispatching, and corrective strategies. Train status monitor signals are compared to the stored schedules to determine performance adjustments that may be necessary.

Central Control Processing System

Three P-250 computers including Sigma 3 central processing units (CPUs), memory, and peripherals comprise the central control complex. Interfaces are provided for command consoles, control panels, and DTS.

Two of the computers, essentially identical, are used for control (A and B in Fig. 8); the third is used to simulate control procedures, for experimentation, and

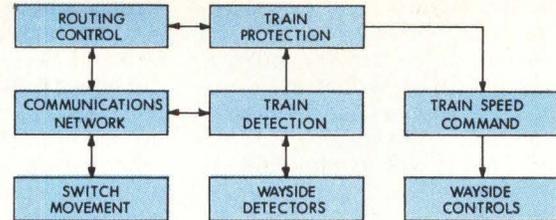


Fig. 5 Local zone system for automatic train control

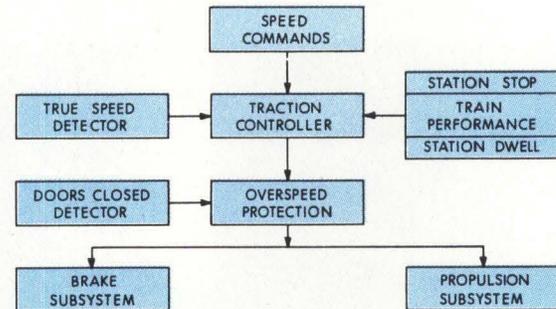


Fig. 6 Controls carried onboard trains for computer-automated operation

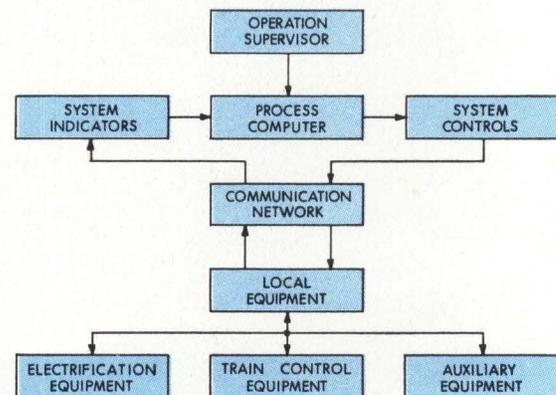


Fig. 7 Supervisory control system combining both local and central line supervision

for training. Control computers A and B interface directly with the online train system, and each alone can perform all supervision and control for the train system. Neither is a preferred computer, however. At any time one of these computers is controlling and

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CIRCLE 36 ON INQUIRY CARD

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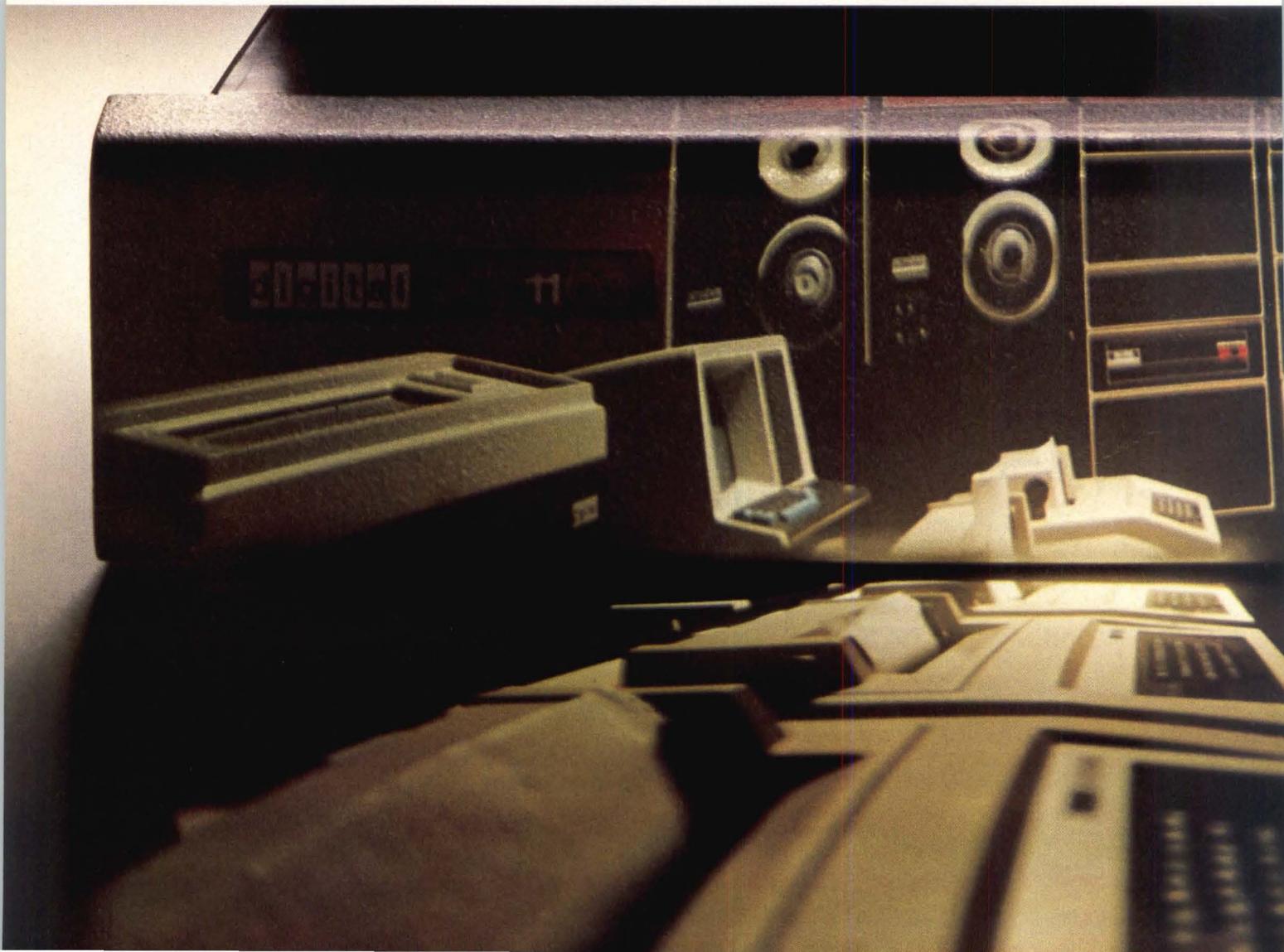
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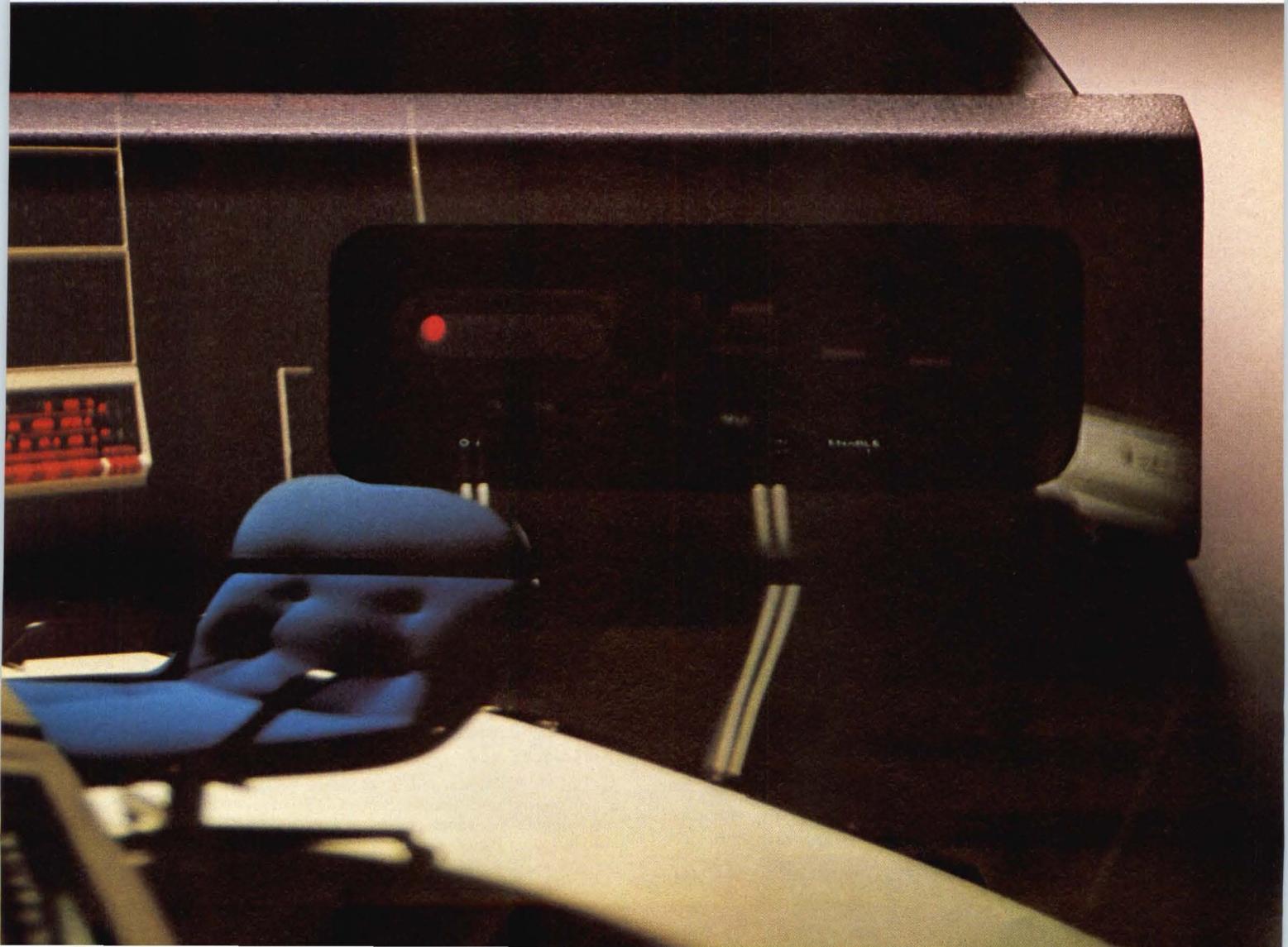
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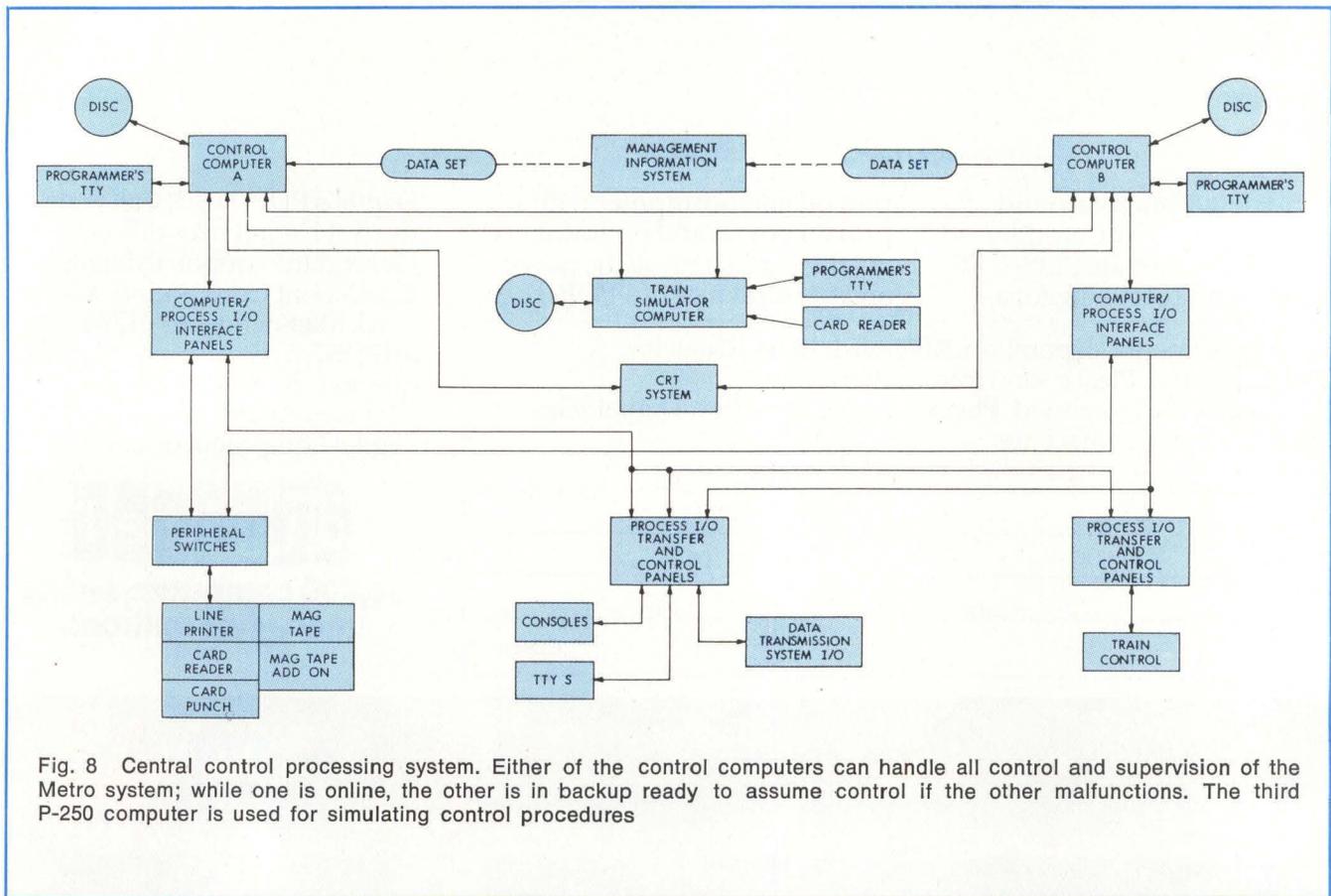


Fig. 8 Central control processing system. Either of the control computers can handle all control and supervision of the Metro system; while one is online, the other is in backup ready to assume control if the other malfunctions. The third P-250 computer is used for simulating control procedures

supervising while the other is in backup mode ready to assume those functions if a malfunction or failure should occur in the controlling computer.

In addition to the two control computers, each with 48K-word core memory, the system contains two 750K-word disc memories, two programmers' teletypewriter console units, 400-card/min. reader, 300-card/min. punch, 600-line/min. printer, and master/slave magnetic tape system (9-channel, 800-bits/in., NRZI, 60K-byte/s transfer rate). High speed data links between control computers and between control and simulator computers and low speed data links to the W-2500 management information system (MIS) computer, plus interface units, are included. Other components are a peripheral switch system capable of connecting peripheral devices to either of the control computers, five teleprinters, eight monochrome CRT monitors, and system interfaces. Communication transmission rate for the MIS computer is 600 baud. The simulation computer system contains CPU with 32K-word core memory, 375K-word disc memory, programmer's teletypewriter console unit, and 400-card/min. reader.

Guided by operating schedules, the control computer checks for correct train makeup, determines departure times from yards and stations, and routes trains. If the system is stable and all trains are running

normally (within $\pm 10\%$ of schedule), the computer merely supervises except for issuing nominal dwell times and making performance level checks.

As changes occur, however, the computer functions from a preprogrammed set of operations. For instance, if a train is late, and beyond the $\pm 10\%$ parameters, the computer will determine running time to the next station and then start adjustments in speed and dwell time to make up the lost seconds.

Higher level strategies supercede low level ones. If a severe disruption occurs, such as from a defective vehicle which cannot maintain proper speed, the computer executes higher level strategies beyond mere dwell adjustments. These strategies tend to spread trains out so that they do not bunch and cause safety problems. As an example, if the low level strategy of speeding up or slowing down trains cannot solve the problem, the computer may decide to change the overall schedule to match what the transit system is capable of performing at that time.

Reference

1. J. W. Brownson and T. C. Selis, "Digital Technology in an Urban Rapid Transit System," Westinghouse Electric Corp, unpublished paper
Circle 160 on Inquiry Card

Our statement on high density head-per-track disc technology:



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Interface System Permits
ASCII Communication Between
Controller and Central Computer

A microcomputer on a 6 x 6" PC board, added to one of the company's standard series 8080 process controllers allows that controller to communicate with a centrally located host computer via a 5-wire, bidirectional digital data highway and thereby be supervised by that computer. Alternately it can communicate with an intelligent terminal.

Basis of the 8000 computer interface system from Beckman Instruments, Inc, Process Instruments Div, 2500 Harbor Blvd, Fullerton, CA 92634 is an Intel 8080 microprocessor incorporated on a PC board which is placed in a slot in the controller. This provides a link between the central computer and analog functions of the control loop. Each loop has a dedicated controller which provides closed loop feedback control using analog proportional-integral-derivative (PID). Total backup control is provided in case of computer failure.

When the host computer is offline, data acquisition and control functions are automatically transferred down to the microcomputer/controller level without disrupting the process. The plant operator has access to each individual controller and can manually change controller settings on each loop through an interactive CRT terminal. An optional backup panel is available which enables the operator to access the individual control loops.

Data enters and leaves the host computer through standard RS-232 communications ports. One port can accommodate a minimum of 36 controllers. All communication on the data highway is in ASCII.

Reliability of data transfer between controllers and host computer is assured by 100% data verification. Using an echo check procedure, all data characters sent between the host computer and the controllers (and vice versa) are repeated.

Where series 8800 process controllers are now being used without computer control, interface cards can be added to the controllers with no additional hardwiring modifications when computerization becomes desirable. If not all of the loops in the process need to be under supervisory computer control, the customer can add computer interface cards only to those control loops that require the higher level of control. Other loops in the system remain under standard analog control.

An optional backup panel is available for systems where controllers are located away from the central control room. When the host computer is down, control is transferred to the backup panel which automatically scans each controller in sequence. If one of the controllers is outside deviation limits, an alarm alerts the operator who can address the control in question. Digital displays indicate the process variable setpoint, controller output,

and the amount of deviation. The operator can then correct the situation through the panel. All of the electronic controllers' features are retained. These include analog and digital circuits to give "totally" bumpless operation with any type of transfer, visual indication of all operating conditions, and setpoint indicators with easy-to-read color bands for deviation limits.

System Speeds Up LSI
Wafer-Probe Testing

Claims for the LSI-800 test system indicate that it speeds up wafer-probe testing by as much as 300 to 400% over conventional LSI device testers. Parallel pin electronic cards in the computer controlled, 10-MHz clock rate test system enable simultaneous parametric tests on all pins of the device under test. As an example, 2-station final test throughput of 8080-type microprocessors is said to be 4000 items/h compared to 900 items/h for other testers; one \$350,000 LSI-800 plus one \$20,000 wafer-probe tester matches four \$300,000 competitive test systems plus four wafer-probe testers.

Almost any test required for current LSI devices and microprocessors can be performed. In addition, the system can generate exotic test patterns including algorithmic patterns for RAM testing and true random patterns for LSI and microprocessor testing. A multidimensional software capability includes device characterization, production environment testing, and instant time-shared access to programs now in the company's central program library. The system is produced by Datatron, Inc, Test Systems Div, 1562 Reynolds Ave, Irvine, CA 92714.

Bin Sensing and Level Control
System Uses Air Sonar

Sonar-in-air is used in the detection loop of a non-contacting system that monitors the level of any material—liquid, granule, powder, metal, ore—in storage bins and automatically controls filling sequences. Developed by Wesmar Level Monitor Div, 905 Dexter Ave N, Seattle, WA 98109, the automated material handling and control system can be customized to a user's specific application since it is claimed to work with any filling technique and to be compatible with any level monitoring system. (For another system using sonar-in-air, see *Computer Design*, Sept 1976, pp 50-66.)

Sensors (one in each bin) are interrogated sequentially by an automatic scanner and the analog output information is fed to control system logic which initiates orders to fill bins if required. Filling sequences can be changed at any time and manual operation of the system can be maintained from a control console. Material inventory is shown on console meters. □

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CIRCLE 39 ON INQUIRY CARD



ISA-76

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ISA International Conference and Exhibit

To aid members of the scientific and industrial community meet the challenge of staying abreast of and implementing newly developed technology, the Instrument Society of America International Conference and Exhibit, under the direction of General Chairman Edward J. Byrne, Brown & Root, Inc, will examine "Productivity Through Instrumentation and Control." The technical program, coordinated by Program Chairman Robert F. Mahood, E. I. du Pont de Nemours & Co, Inc, includes technical paper sessions, workshops, clinics, and panels. In addition, several 2-day short courses are scheduled during Conference week to offer attendees an opportunity to update and increase their technical skills and knowledge.

Only sessions and courses of particular interest to *Computer Design* readers are outlined in the following pages. Information is necessarily limited to that available at press time.

Special Activities

Contributing a practical and valuable perspective to the Conference goals and today's technological philosophies, Donald C. Burnham, director-officer of Westinghouse Electric Corp, will deliver the Keynote Address on Monday at 10:30 am. On the social side, the ISA President's Reception, to be held Sunday from 4:30 to 6:00 p.m. in the Astroworld Hotels Ballroom, will provide an opportunity for attendees to meet ISA society officers.

The Honors and Awards Bicentennial Luncheon on Tuesday at 12:30 pm in the Astrophall will recognize those who have contributed significantly to the technology of instrumentation and to the Society. (Tickets are \$10 each.) Other social events include the Pulp & Paper Industry Division Luncheon at 12:30 pm Wednesday in the Astroworld Hotels (tickets \$8 each), and an authentic western style rodeo which will take place at Regal Ranch, Stafford, Texas. Beginning at 6:30 pm on Wednesday, the festivities include rodeo show, music, and barbeque. Busing from the Shamrock and Astroworld Hotels will be provided. (Tickets at \$15 each include busing.)

Registration and Exhibits

Fees for Conference and Exhibit registration are \$2 for ISA members, \$5 for nonmembers. Short courses carry a \$140 charge for members, \$170 for nonmembers. This includes course notes and text, coffee breaks, and admission to the Conference and Exhibits. Published technical papers and bound proceedings of the Conference will be on sale in the registration area of the Astrophall.

Registration hours are Sunday from 1 to 6 pm in the Astroworld Hotels Ballroom, and in the Astrophall on Monday from 9 am to 6:30 pm, Tuesday from 9 am to 7:30 pm, Wednesday from 8 am to 5:30 pm, and Thursday from 8 am to 4:30 pm. Exhibit hours are Monday 12 noon to 7 pm, Tuesday 10 am to 8 pm, Wednesday 9 am to 6 pm, and Thursday 9 am to 5 pm.

Short Courses

Monday and Tuesday

Industrial Computer Performance Measurement and Vendor-User Negotiations

Practical answers to problems of improving industrial computer performance are provided through specifying and testing key computer hardware, software, and application parameters.

Software Systems—Design and Management for Industrial Computer Programming

Introducing methods for designing and managing design of industrial automation systems and software for those systems, course covers concept and techniques and provides guidance in how and when to apply techniques.

Introduction to Computer Control

Internal computer design, computer hardware and software, and



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CIRCLE 40 ON INQUIRY CARD

unique application to industrial situations are outlined for those unfamiliar with computer equipment and programming. Discussions on economic justification, project management, and international standardization activity supplement overall understanding of the computer's role in process applications.

Wednesday and Thursday

CAMAC: Standard Modular Instrumentation and Digital Interface System

Introduction to the CAMAC modular interface standard for application in real-time data acquisition and control is provided through general description of system concepts and methods of implementing it in industrial control and laboratory automation.

Programmable Controllers

The subject of programmable controllers is developed through descriptions of the hardware, software, and applications.

Microcomputer Applications for Process Control

Course includes hardware demonstrations of typical microcomputers in addition to lectures on software and hardware considerations.

Technical Program Excerpts

Monday

Session 2 2:30-5:00 311

Architecture and Design of a Distributed Process Control System

Chairman: R. Dallimonti, Honeywell, Inc

"Analysis of Data Highway Loading by Simulation," R. J. Bibbero, Honeywell

"Design Considerations for Achieving Reliable Control Within Shared Microprocessor-Based Digital Controllers," P. W. Bur, Honeywell

"A Digital Communication System for Process Control Instrumentation," F. J. Romeu, Honeywell

"Operator Interface in Distributed Microprocessor Control System," C. R. Stewart, Honeywell

Session 3 2:30-5:00 208

Productivity Through Instrumentation in Chemical and Petroleum Plants

Chairman: F. G. Engstrom, The Foxboro Co

"Control Techniques in the Crude Oil Tower for Better Productivity," H. L. Wade, C. J. Ryskamp, and R. B. Britton, The Foxboro Co

"Reduce Distillation Cost Through Advanced Computer Control," D. L. Hoyle, The Foxboro Co, and R. B. Rice, Neches Butane Products Co

Session 5 2:30-5:00 307

New Digital Techniques in Process Control

Chairman: R. H. Ryan, The Foxboro Co

"CRT Process Operator's Interface, Past and Future," F. Kitchenska, The Foxboro Co

"The Use of Wide Band Coaxial Cable Data Systems in the Manufacturing Environment," A. I. Edwin, Interactive Systems
 "Local I/O, Remote I/O, or Distributed Computing for Computer Control Applications?" W. L. Avery, Digital Equipment
 "A Distributed Microprocessor-Based Control System Programmable by the Process Engineer," C. P. Pracht, Reliance Electric

Session 10 2:30-5:00 111

Panel: Nuclear Power Standards—The Need for a Managed Program

Chairman: H. Hubbard, Southern Service

Keynote Address: R. B. Minogue, U. S. Nuclear Regulatory Commission

Panelists: R. G. Hand, ISA Headquarters; J. E. Leary, Bechtel Power; J. V. Rocca, Pacific Gas & Electric; J. Russ, General Electric; E. C. Wenzinger, Nuclear Regulatory Commission; and W. J. Woollacott, ASME

Tuesday Morning

Session 11 10:00-12:30 401

Clinic: Microprocessor Applications to Control

Chairmen: J. Westwick, General Motors, and E. Lee, Pro-Log Corp

Fundamentals of using microprocessors in control systems will be presented using lectures and hands-on laboratory work. Lectures present theory in simple engineering terms and laboratory enables students to apply the theory and actually do design work.

Session 12 10:00-12:30 209

Control of Processes with Transport Delays

Chairman: J. F. Donoghue, Cleveland State University

"Digital Feedforward Control of a Sheet Process with a Product Nonlinearity," P. Vlahutin, Industrial Nucleonics

"Resolving Limit Conditions for Multivariable Controllers," J. B. Froisy, Celanese Chemical

Session 13 10:00-12:30 402

Pipeline Control & Instrumentation I

Chairman: R. J. Dunn, Exxon Pipeline Co

"Pipeline Control with Programmable Logic Controllers," W. F. Muma, Continental Pipe Line Co, and D. E. Henry, Struthers-Dunn

Session 15 10:00-12:30 307

Panel: Microcomputers for Instrumentation and Control

Chairman: H. P. Zinschlag, Monsanto Co

"Designing Microcomputers Into Your Products," R. G. Barnich, Process Computer Systems

"Microcomputers: A Potential Value for Process Control," A. D. Deramo, Westinghouse Electric

"Microcomputers and Process Control: Where's The Missing Link?" J. J. Katsaros, Fairchild Camera and Instrument

"Development of a Microprocessor-Based Clinical Analyzer Controller," J. E. Lewis and J. E. Davis, Barnes Hospital Laboratories

"Microcomputers for Remote Intelligent Monitoring and Control," R. M. Alden, General Automation

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"Manufacturer/User Interface for Microprocessor Based Systems,"
G. E. Kimble, Eagle Signal

Session 16 10:00-12:30 114

Clinic: Programmable Logic Controllers—Basics

Chairman: A. I. Schwartz, Westinghouse-Bettis

2-day clinic considers hows, whys, and wherefores of programmable controllers, including how they work, how to apply them, and hands-on use of equipment. Instructors are from Modicon.

Session 17 10:00-12:30 116

Clinic: How to Program Process Control Computers

Chairman: A. I. Schwartz, Westinghouse-Bettis

With the objective of providing hands-on experience in writing and testing digital computer programs for on-line control of real industrial processes, this clinic divides participants into 6-man teams to design and implement a control strategy involving interactive flow and level loops. Instructors are from Fisher Controls.

Tuesday Afternoon

Session 26 2:30-5:00 401

Clinic: Microprocessor Applications to Control

Chairmen: J. Westwick, General Motors, and E. Lee, Pro-Log Corp

(Continuation of Session 11)

Session 28 2:30-5:00 311

Microprocessor Based Control Systems

Chairman: S. C. Hu, Cleveland State University

"Interfacing a Microcomputer to a Minicomputer for Control Software Development," C. Baradello, R. Krutz, and W. J. Sauer, Carnegie-Mellon University

"Microprocessors—Characteristics and Roles in Process Control," S. C. Hu, Cleveland State University

"Position Control of Machine Tools Using a Microcomputer," W. J. Sauer and F. W. Paul, Carnegie-Mellon University

"A Multiprocessor Based Programmable Control," O. J. Struger and E. Dummermuth, Allen-Bradley

"Companding Data Conversion," D. J. Dooley, Precision Monolithics

Session 29 2:30-5:00 402

Pipeline Control & Instrumentation II

Chairman: R. J. Dunn, Exxon Pipeline Co

"Digital Computers for Gas Measuring Systems," R. D. Goodenough, Tennessee Gas Pipeline Co

Session 31 2:30-5:00 307

Digital Control Applications

Chairman: D. Whiteford, Rosemount, Inc

"The Economics of Flexibility—Packaged DDC Applied to Sulfur Recovery," J. M. Berra, Rosemount

"Crude Distillation Computer Control Experience," L. D. Van Horn and P. R. Latour, Biles & Associates

"Reliability Analysis and Backup for Process Computers," P. V. Bhat, Monsanto

"Computer Applications in Textiles," P. L. Grady and R. H. Ritchie, North Carolina State University

Session 32 2:30-5:00 114

Clinic: Programmable Logic Controllers—Basics

Chairman: A. I. Schwartz, Westinghouse-Bettis

(Continuation of Session 16)

Session 33 2:30-5:00 116

Clinic: How to Program Process Control Computers

Chairman: A. I. Schwartz, Westinghouse-Bettis

(Continuation of Session 17)

Session 38 2:30-5:00 403

Analog and Digital Control Techniques

Chairman: J. Gray, ACCO/Bristol

"A Microprocessor-Based Flow Monitoring System," C. W. McKay, University of Houston, and C. R. Gross, McKay Consulting Co
"The Great Analog/Digital Debate," J. J. Murray, Beckman Instruments

"Multiloop Process Controller Based on a Microprocessor," A. Uyetani, Tokyo Shibaura Electric

Session 40 2:30-5:00 107

Standards Implementation Application/Roundtable

Chairmen: R. Coel and M. Snyder, Fluor Engineers & Constructors Inc

"Metrication Conversion: Impact," H. F. Fabisch, Fluor Engineers & Constructors, and J. R. Coffey, Rosemount

"Intrinsic Safety Computer Program," Z. Zborovszky and G. A. Rinard, University of Denver, and L. Cotugno, Bureau of Mines
Roundtable: "The Whys and Wherefores of ISA Standards," W. B. Miller, Moore Products, and A. P. McCauley, SCM Corp

Wednesday Morning

Session 42 10:00-12:30 401

Clinic: Microprocessor Applications to Control

Chairmen: J. Westwick, General Motors, and E. Lee, Pro-Log Corp

(Continuation of Session 11)

Session 43 10:00-12:30 402

General Automatic Control

Chairman: G. L. Kramerich, Cleveland State University

"Computerized Control for Rubber Molding Presses," J. D. Ekland and J. R. Diehr, Federal-Mogul Corp

Session 44 10:00-12:30 206

Instrumentation in Natural Gas and Gasoline Plants

Chairman: E. H. Lochte, Fluor Engineers & Constructors, Inc

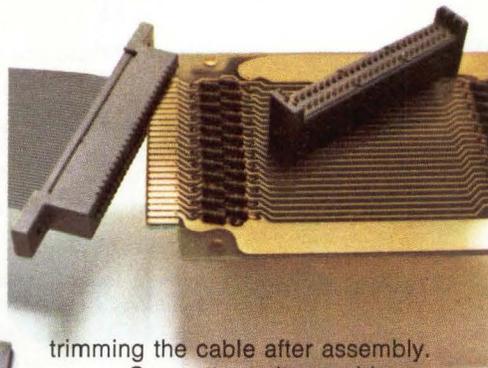
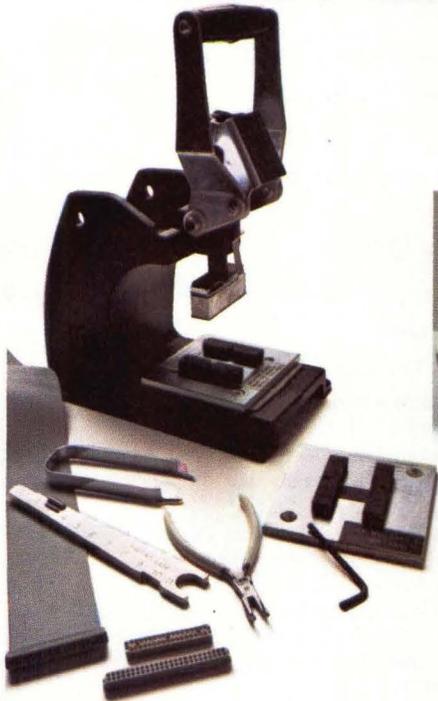
"Improve Efficiency and Productivity with Advanced Analog and Digital Controls," D. G. Langston and B. M. McCraw, Warren Petroleum Co

Session 46 10:00-12:30 307

Energy and Utility Conservation by Computer Control

Chairman: P. V. Bhat, Monsanto Co

Design with the complete flat cable/connector system.



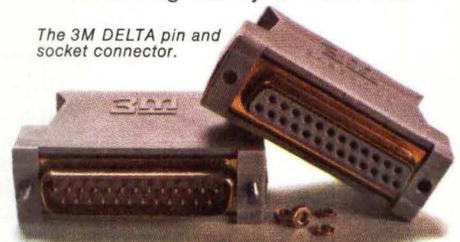
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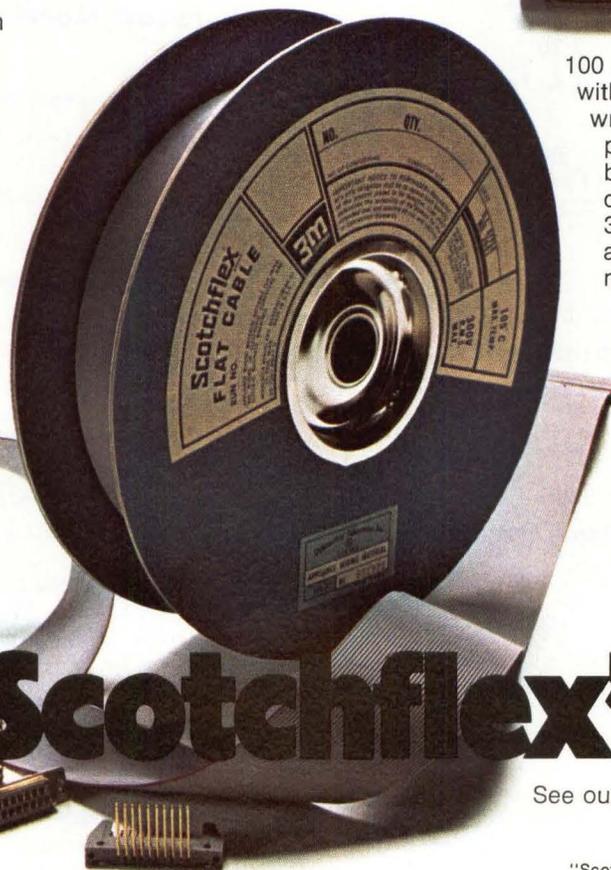
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"Industrial Power Demand Regulation by Computer Control," P. D. Madden, Union Carbide Corp

"Chiller Control Using On-Line Allocation for Energy Conservation," H. Zimmer, Fisher Controls

"Energy Savings Through Computer Utilization in a Plant's Central Refrigeration System," R. A. Stafford and D. M. Moore, Monsanto Textiles

"An Approach to Optimal On-Line Control of Industrial Utility Systems," C. G. Laspe and R. A. Krall, Jr, Honeywell

Session 47 10:00-12:30 114

Clinic: Programmable Logic Controllers—Advanced

Chairman: A. I. Schwartz, Westinghouse-Bettis
(Repeat of Session 16)

Session 48 10:00-12:30 116

Clinic: How to Program Process Control Computers

Chairman: A. I. Schwartz, Westinghouse-Bettis
(Repeat of Session 17)

Session 49 10:00-12:30 107

Clinic: Minicomputer Systems

Chairman: A. I. Schwartz, Westinghouse-Bettis

All-day clinic introduces minicomputer hardware and programming as well as giving insight into systems design and implementation, cost and justification considerations, industrial applications, and future trends. An actual operating system will provide an opportunity for hands-on experience. Instructors are from Hewlett-Packard.

Session 55 10:00-12:30 213

Control Valves—Noise/Digital Actuators

Chairman: M. L. Freeman, Ametek, Inc

"Digital Actuation and Interface of Rotary Control Valves," J. B. Hills and H. J. Fuller, Worcester Controls

"Digital Control Valve Actuators," E. G. Hofstetter, Jr, DeZurik

Wednesday Afternoon

Session 59 2:30-5:00 401

Clinic: Microprocessor Applications to Control

Chairmen: J. Westwick, General Motors, and E. Lee, Pro-Log Corp

(Repeat of Session 11)

Session 61 2:30-5:00 307

Digital Applications in the Paper Industry

Chairman: R. Genter, Fisher Controls Co

"A Computer Coordinated Control System for Batch Digitizers," O. K. Fadum, The Foxboro Co

"The Hidden Benefits from Better Process Control," P. R. Latour, Biles & Associates

"Bleach Plant Computer Control: Importance of Interface With Operator and the Process," W. A. Haverinen, Industrial Nucleonics Corp

Session 62 2:30-5:00 114

Clinic: Programmable Logic Controllers—Advanced

Chairman: A. I. Schwartz, Westinghouse-Bettis
(Continuation of Session 47)

Session 63 2:30-5:00 116

Clinic: How to Program Process Control Computers

Chairman: A. I. Schwartz, Westinghouse-Bettis
(Continuation of Session 48)

Session 64 2:30-5:00 107

Clinic: Minicomputer Systems

(Continuation of Session 49)

Session 68 2:30-5:00 210

Digital Applications

Chairman: E. Roland, Copeland & Roland, Inc

"Microprocessor Based Monitoring and Interlock System for Pneumatic Product Distribution," E. C. Croft, Foster Grant

"Parallel Interface Considerations for Process Control," C. A. Wiatrowski, University of Colorado, and B. K. Conant, Burr-Brown Research

"Process Safety and Reliability Through Process Control Computer/Programmable Controller Interconnection," J. C. Pfeiffer, ICI United States

"Refinery Supervisory Control by Using Process Control Oriented Software System," A. Uetani, Toshiba Electric, S. Ikenoue, Fuji Oil, and K. Ichida and T. Tohyama, Chiyoda Chemical Engineering and Construction

Thursday Morning

Session 71 10:00-12:30 401

Clinic: Microprocessor Applications to Control

Chairmen: J. Westwick, General Motors, and E. Lee, Pro-Log Corp

(Continuation of Session 59)

Session 74 10:00-12:30 107

Clinic: Minicomputer Systems

Chairman: A. I. Schwartz, Westinghouse-Bettis

(Repeat of Session 49)

Session 79 10:00-12:30 307

Development and Application of Uninterruptible Power Supplies to Process Industries

Chairman: D. R. Bratton, Solidstate Controls

"Refinery Applications of Uninterruptible Power Systems," E. G. Warren, Exxon

"Electric Utility Need for Uninterruptible Power Supplies," K. G. Allen, Jr and E. Floyd, Dallas Power & Light

"Comparison of Inverter Circuits for Use in Fixed Frequency Uninterruptible Power Supplies," D. R. Bratton and J. M. Powell, Solidstate Controls

"Uninterruptible Power Supplies for Operation and Control Computer Systems in an Electric Utility," K. R. Dawson, Jersey Central Power & Light

"Uninterruptible Power for the Trans Alaskan Pipeline," A. T. Aguilar, Fluor Engineers & Constructors

"Use of Uninterruptible Power Supplies in Chemical Plants," W. J. Johnson, Dow Chemical □

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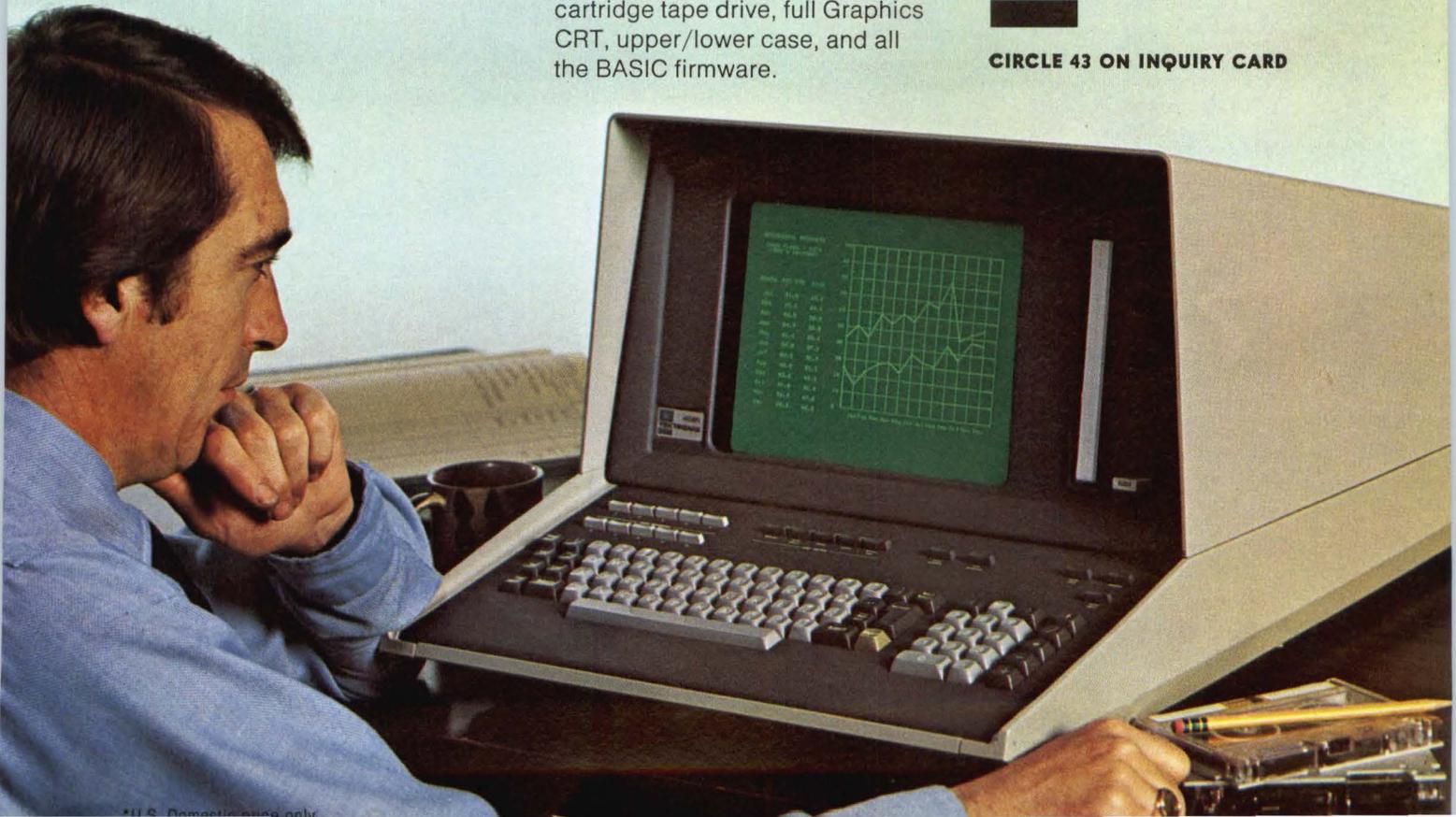
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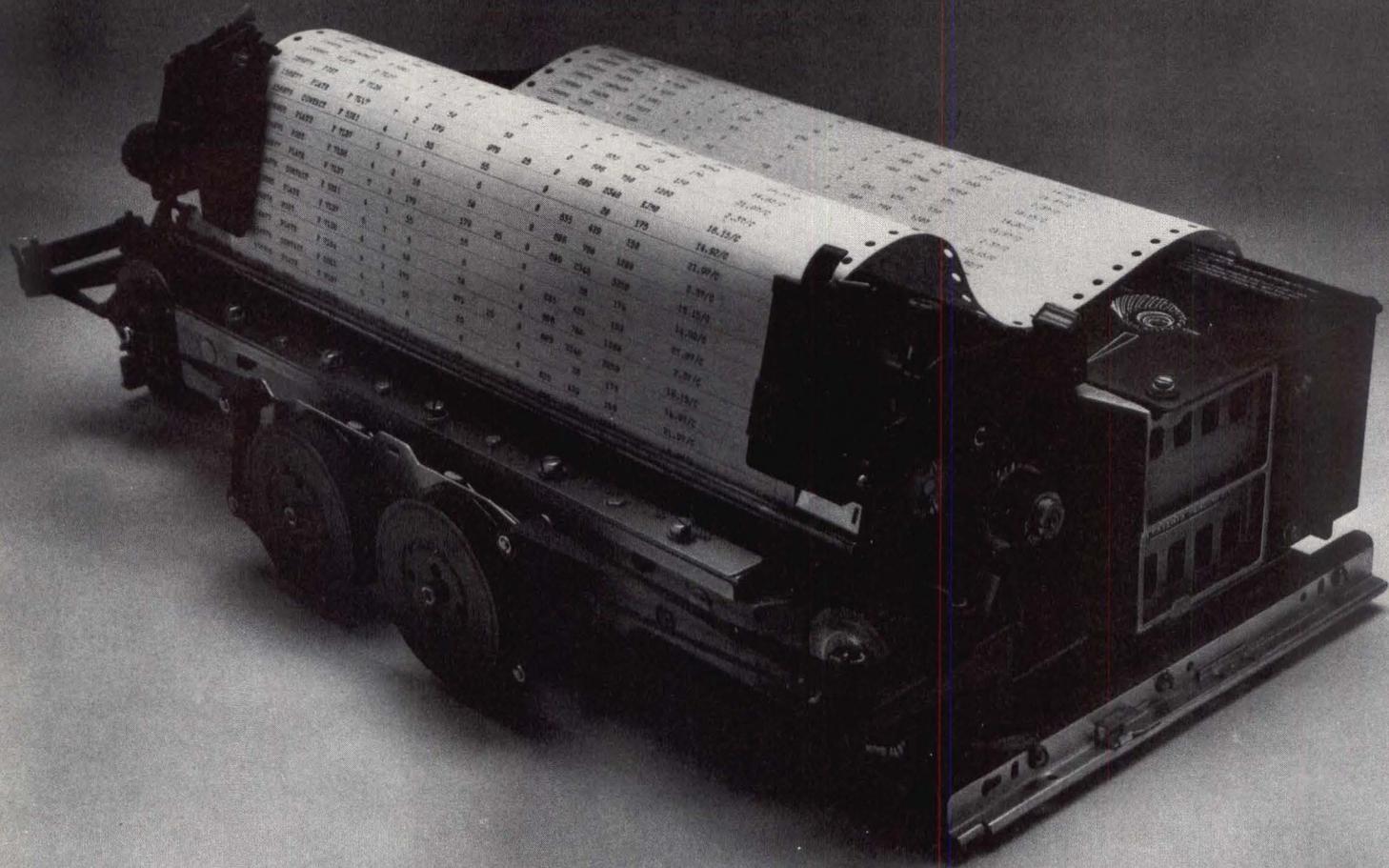
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Now well advanced in development, magnetic bubble systems offer advantages not found in other technologies, promising to fill the existing gap in the memory hierarchy and open up some entirely new applications

Magnetic Bubble Systems

Approach Practical Use

J. Egil Juliussen

**Texas Instruments, Incorporated
Dallas, Texas**

Memory systems based on magnetic bubble technology have a number of very significant potential applications, notably as microperipherals and in filling the prominent speed-cost and capacity-cost gaps in conventional memory hierarchies. Although numerous articles have been published about magnetic bubble memory devices and their operation,¹ very little seems to have been written about bubble memory systems, their advantages based on particular device characteristics, and their unusual system-level properties. System considerations depend, of course, on knowledge of the technology and of the devices, but also bring up such questions as how to establish an interface between a magnetic bubble memory (MBM) system and other equipment, what technologies compete with MBM systems, and what applications seem likely.

Magnetic bubble memories have advanced considerably since the concept was first reported at Bell Laboratories in the late 1960s. Today Bell is preparing to begin production of the devices (via Western Electric), while developments are known or surmised to be under way at many other organizations, including Texas Instruments, Rockwell International, IBM, Hewlett-Packard, Hitachi, Fujitsu, Plessey, and Philips. Over the next two years product announcements are expected and mass production seems certain to begin. In fact, in early 1976 Hitachi was to have started building bubble memories into office machines, point-of-sale terminals, and refreshed displays.²

Magnetic Bubble Memory Fundamentals

Bubble memories can be viewed as solid-state integrated analogs of rotating electromechanical memories,

such as discs, drums, and tape recorders. In both rotating and integrated versions, information is stored in the form of magnetized regions. These regions, in the integrated version, are cylindrical domains in a thin layer of magnetic material, with magnetization opposite to that of the surrounding area. Their presence or absence at specific locations corresponds to binary digits stored at those locations. These bits are made accessible by moving the domains within the solid layer to an access device, as opposed to physically moving the storage medium, as with disc or tape.

Storage material can be either a magnetic garnet grown epitaxially on a non-magnetic garnet substrate, or an amorphous metallic magnetic layer sputtered onto a substrate such as glass. Both types of material and techniques for processing them are similar to those used in the semiconductor industry; for example, single crystals of various materials are grown like silicon crystals. However, with fewer mask levels, and without stringent alignment requirements in processing, the bubble memory price per bit should be lower than that of silicon integrated memories.

Bubble Memory Operation

Four basic functions are required to operate a magnetic bubble memory—propagation, generation, detection, and annihilation. For block-organized chips, replication and transfer operations (Fig. 1) are also needed.

Bubble propagation is required for access to information on the chip. The most successful method of propagation has been to magnetize Permalloy patterns with an in-plane rotating field. Alternatives, such as use of current-carrying conductors or oscillating bias fields^{3,4} are not as highly developed. Permalloy patterns can be any of several shapes^{5,6,7} (Fig. 2).

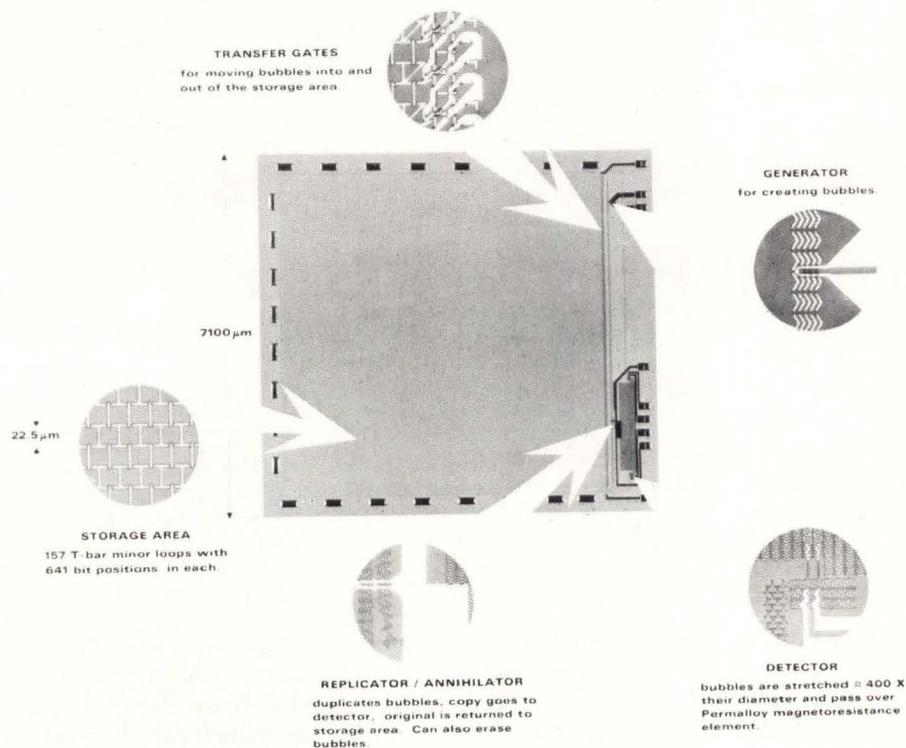


Fig. 1 Four functions. Every bubble memory chip requires these functions, as well as the storage array itself

Bubble generation is the process of writing information into the memory, most commonly with a nucleate generator. The latter consists of a hairpin-shaped conductor loop energized by a current pulse, which produces a bubble inside the end of the hairpin.

Detection of bubbles is required to read the memory content. This is generally done in a special section of the propagation circuit, where bubbles are stretched into wide strips that cause a distinct change in magnetoresistance of the Permalloy. The stretching is equivalent to preamplification, and assures a sense signal of several millivolts when the detector pattern and three bubbleless dummy patterns are interconnected as a bridge.

A bubble annihilator clears the memory data, and is commonly combined with a replicator. Replication of bubbles allows a nondestructive read operation, by duplicating information; one copy is read and discarded, while the original data remain in memory. Several methods of bubble replication are used. Like detectors, they stretch the bubble; however, they then cut it in two and send the pieces in different directions.^{8,9}

Bubble Chip Architectures

Many different ways have been developed to organize a bubble memory chip. The simplest organization is a single shift register. This is equivalent to a 1-track magnetic tape, and, like such a tape, has the drawback of long access time.

A better organization is the major/minor loop organization (Fig. 3). Multiple shift registers reduce the access time drastically from that of a serial organization, just as a fixed-head disc has much less access time than a tape; disc tracks are equivalent to minor loops. Therefore, first production runs of magnetic bubble chips will probably have a major/minor loop or single loop organization.

To access data, bubbles in the minor loop are first shifted to the position that is closest to the major loop. At this point, bubbles (or absence of bubbles) are transferred simultaneously from all minor loops to the major loop. Then they are shifted around the major loop, read, annihilated, or replicated, as required, and transferred back to the minor loops, regaining the same position previously occupied. There

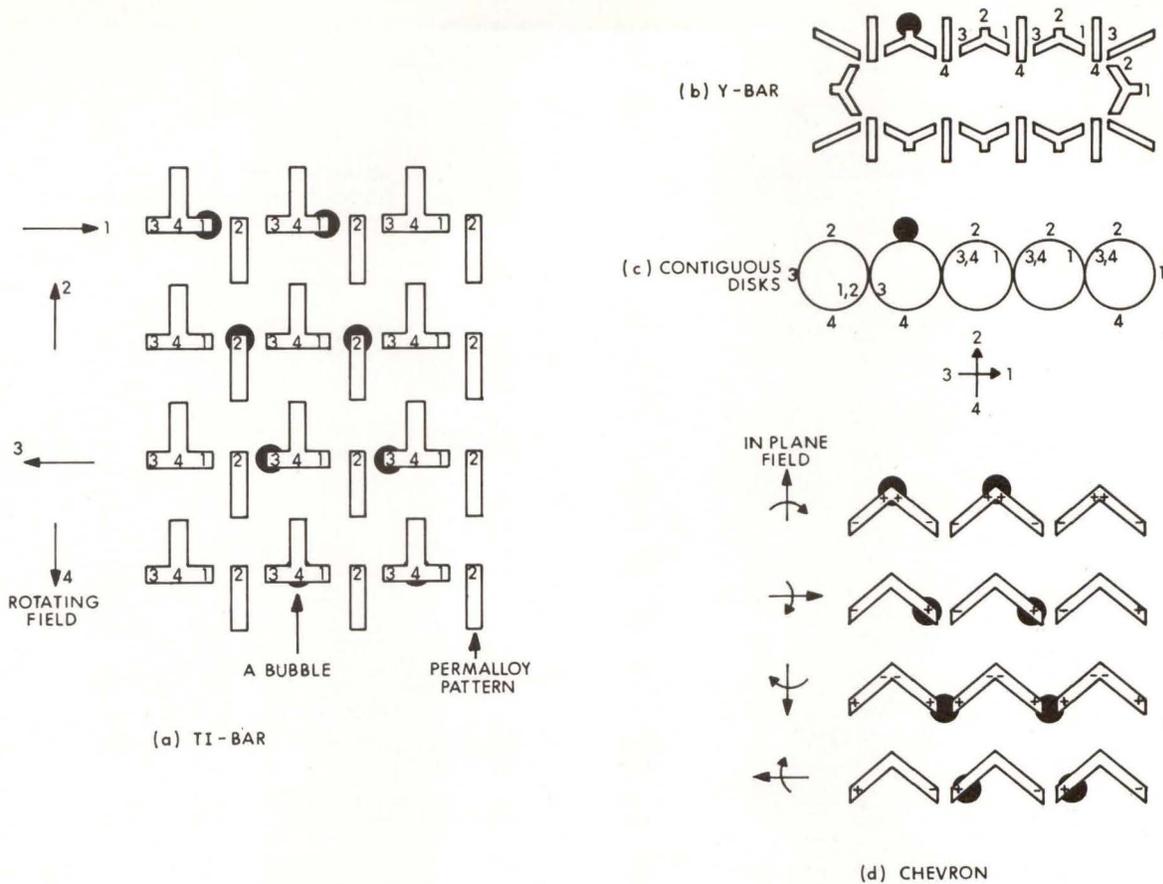


Fig. 2 Four propagation techniques. As external magnetic field rotates, bubbles move through the film medium controlled by field concentrations created by conductive patterns—(a) TI-bar, (b) Y-bar, (c) contiguous disc, or (d) chevrons. Field rotates clockwise for pattern d, and counterclockwise for the others, for left-to-right propagation

are many variations on the major/minor loop organization (Table 1).¹⁰

Recently an interesting bubble memory organization called the bubble ladder has been reported.^{11,12} The bubble ladder consists of storage loops that are linked together by binary switches in a chain fashion. If the binary switches are set in the bypass mode, each storage loop (or "chain-link") is an independent loop with circulating data. If all switches are set in the crossover mode, the whole ladder behaves as a large chained loop. The bubble ladder has many desirable characteristics for design of information files, but has the drawback of requiring a large number of control leads.

MBM Systems

Basic building block for bubble memories probably will be a single chip of about 100,000 bits in a dual-in-line package (DIP). Other building blocks are possible. For instance, Texas Instruments has experimented

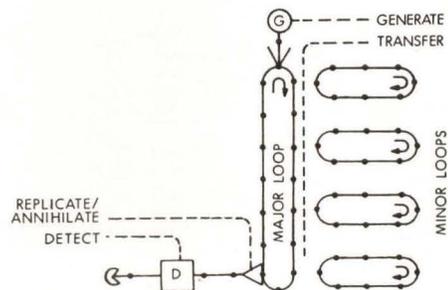
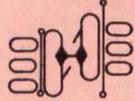
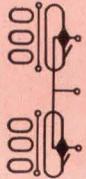
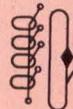
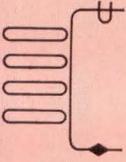
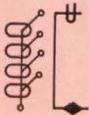
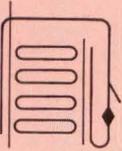
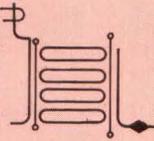
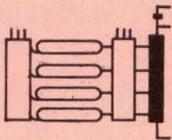


Fig. 3 Major/minor loops. Bubbles are stored in minor loops, transferred in parallel to major loop, from which they are read out. Storing new information follows reverse procedure

TABLE 1
Major/Minor Loop Organizations

Layout	Type	Access Time*	Return Time*	Advantages	Disadvantages
	Simple loop	$N/2$	—	Minimum leads No housekeeping	Long access time
	2-phase loop	$N/2$	—	Double data rate	2-phase detector
	Major-minor common transfer	$2\sqrt{N}$	$(R-1)\sqrt{N}$	Fast access Few leads	Low average data rate
	2-phase major- minor common transfer	$2\sqrt{N}$	$(R-1)\sqrt{N}$	Double data rate Few leads	2-phase detector Low average data rate
	Dual 1-phase major-minor tandem	$2\sqrt{N}$	$(R-1)\sqrt{N}$	Continuous data flow	2-pole detector output Housekeeping required
	Major-minor individual transfer	\sqrt{N}	$(R-1)\sqrt{N}$	Good access Bad loops ignored	Many leads

*Proportional average (N-bit chip)

Layout	Type	Access Time*	Return Time*	Advantages	Disadvantages
	Minor loops and common transfer/replicate	$2\sqrt{N}$	—	Fast access Data stays in homesite	Complex elements Reading problems
	Major-minor individual transfer/replicate	\sqrt{N}	—	Good access Data stays in homesite Continuous data flow	Many leads
	Minor loops and separate data return	$2\sqrt{N}$	$4\sqrt{N}$	Fast access Continuous data flow Simple elements	Data leaves homesite Long return time
	Minor loops and separate read/write ports	$2\sqrt{N}$	—	Fast access Data stays in homesite	Complex elements
	Minor loops and decoded input/output and guard-rail detector	$\log_2\sqrt{N}$	—	Fastest access	Decoders not proven

*Proportional average (N-bit chip)

with a module consisting of an array of 16 chips of 16,000 bits each.¹³

Both chip and system characteristics, as well as some qualitative features (Table 2), will affect system design. For example, because bubble memories have a shift register organization, and because one bit from each minor loop is transferred to the major loop

during memory accessing, a block organization is probable. However, a bubble chip is bit, byte, or word addressable, since the Permalloy pattern defines discrete storage locations.

Stop/start operation is a very advantageous feature. Stopping the shifting process completely, or restarting it from a standstill, takes only 10 to 20 μ s; thus after

TABLE 2

Bubble Memory Characteristics

Chip Characteristics

Storage density	1M bits/in. ²
Chip capacity	64K to 100K bits
Access time	1 to 4 ms
Transfer rate	100K bits/s
Packaging	10/16-pin DIP
Power dissipation	<1 W
Standby power	None
Temperature range	-25 to 75°C

System Characteristics

Transfer rate	0.1M to 1.5M bits/s
Packaging	PC board
Storage capacity	1M to 3M bits/board
Power dissipation	10 to 20 W
MTBF	10,000+ hours
Controller	Microprocessor-based

Qualitative Features

Serial access memory
Shift register organization
Block-oriented access
Bit addressable
Nonvolatile memory
Nondestructive read
Read-modify-write cycle
Stop/start operation
Lowers effective access time
Lowers power dissipation
Permits variable transfer rate
Minimizes buffer requirements
Modular storage capacities
Give low entry price
Bit price almost independent of storage size
Package pin-count independent of storage size
Few manufacturing steps
Manufacturing similar to IC production

each storage access the bubble chip can be stopped to conserve power. Similarly, during data transfer, stop/start operation can simulate variable transfer rates and can lower data buffering requirements. With proper usage, such as shifting separate modules independently and storing subprograms of a task in successive areas, effective access time can also be lowered.¹⁴ Additionally, stop/start operation simplifies hardware and software interfacing¹⁵ and lowers MBM controller complexity. If stop/start mode were possible in disc memories, each disc track could spin independently with nearly instantaneous stopping and starting. Bubble memories can also shift bidirectionally, but reverse motion is not likely to be used with current chip or system architectures.

Modularity is probably the most important characteristic of MBMs. This means that a low price per bit can be achieved for relatively small capacity—certainly not multimegabits. This is not true for rotating mass memories, whose bit-price depends heavily on storage size. Lowest current prices for flexible disc systems are almost \$3000, about \$9000 for a moving-head disc cartridge system. In contrast, an entry price of less than \$1000 is not unlikely for MBM (with fewer bits than a floppy disc of course).

A rarely noted feature of MBM is the package standardization which is possible. Its importance becomes apparent when one considers the undesirable effect of the various pin choices of 4K and 16K RAMs. Package standardization for MBM is easy because there are no address pins. With a given chip architecture an MBM chip can have the same number of pins independent of storage size.

However, absence of address pins does not mean an MBM cannot be addressed. On the contrary, addressing an MBM chip is quite simple. It requires two external counters, which are run at the rate of the bubble shifting. One counter selects the position in the minor loop to be read; the other counter is started when a block is transferred to the major loop and indicates when bubble replication, annihilation, detection, and

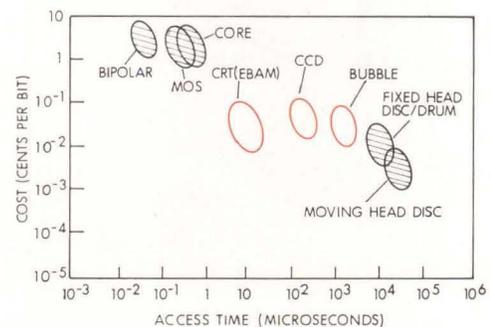


Fig. 4 Bubbles in access time gap. Chart relating cost per bit to access time shows how magnetic bubble systems fit between conventional solid-state and rotating magnetic mass memories

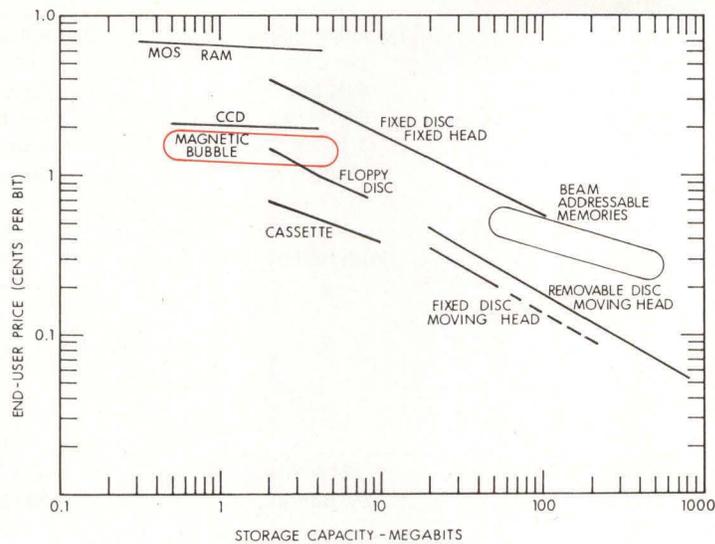


Fig. 5 Bubbles in capacity gap. When compared with other technologies in cost versus storage capacity, cost of magnetic bubble systems is seen to be almost independent of capacity, unlike rotating memories

generation take place. In an MBM controller these two counters are central to decision making. Either a state machine or a microprogrammed controller can be used. In either case the controller is less complex than is necessary for rotating mass memories.

Other advantages of MBM controllers include simpler software interfacing, flexible interrupt requirements, and less data buffering—all with reference to rotating mass memories. Furthermore, a controller can be implemented using only 100 to 150 standard TTL circuits, compared to 200 to 250 for a floppy disc interface. Both figures can be decreased, to 25 to 50 for MBM, if the controller is based on a microprocessor, and to as few as 10 if custom ICs are used. Such ICs have been developed for floppy disc controllers, and Bell Laboratories' 3-chip controller¹⁶ shows that the same is possible for MBM.

Competing Technologies

Magnetic bubble memories will have to compete with both established technologies, such as MOS RAM, fixed head discs, moving head disc cartridges, and floppy discs, and with emerging technologies such as charge-coupled devices (Table 3). To successfully enter the marketplace amidst such competition, MBM must have some combination of attractive features that other technologies cannot deliver. The most common measure is probably the access time versus cost per bit¹⁷. The chart (Fig. 4) shows the access and cost gap between random-access memories and rotating magnetic mass

storage into which charge-coupled devices (CCDs), MBMs, and electronic beam addressable memory (EBAM) fit.

However, a more important chart shows the relationship between cost per bit and storage capacity (Fig. 5). This chart shows that bit-prices of MOS RAM and CCD are almost independent of storage capacity. The same modularity will be an advantageous feature of MBM. Bit-price of rotating magnetic memories, on the other hand, is highly dependent on storage capacity, and falls rapidly with increasing size. As a result, for applications that require both primary and low capacity secondary storage, price per bit will be steep for rotating mass memory. Prime examples of such applications are those served by microprocessors. Therefore, at these low capacities, not exceeding 1M to 4M bits, both MBM and CCDs will be very cost-effective—particularly since entry price or bit-price at low storage capacities of rotating memories is not likely to change substantially. Meanwhile, the learning curve effect for CCD and MBM will lower the bit-price as production rates increase, so that MBM and CCD become competitive at higher and higher storage capacities.

MBMs and CCDs also have a packaging advantage over rotating mass memories. Both can have several megabits on a printed circuit that would fit in the CPU chassis.

Main advantages of magnetic bubbles over CCDs are nonvolatility, two to four times more bits per chip, and a possible reliability advantage arising from simpler processing and fewer chips for a given storage capacity. An MBM can stop dead in its tracks; CCDs have an idling speed about two orders of magni-

TABLE 3
Current Minicomputer Mass Memory Technologies

General Characteristics	MOS RAM	CCD	MBM
Access time	300 ns	100 μ s	1 to 3 ms
Transfer rate	2M bits/s per chip	1M to 5M bits/s per chip	100K bits/s per chip
Storage capacity (typ)	16K bits per chip	64K bits per chip	128K bits per chip
Read error rate	1 in 10^{10}	1 in 10^{10}	1 in 10^{12}
Reliability (MTBF in hours)	7000	7000+	10,000+
Removable media	No	No	No
Nonvolatile	With battery	With battery	Yes
Software interfacing capability (1 = easiest)	1	2	3
Hardware interfacing capability (1 = easiest)	1	2	3
System Example (Interfaced to Minicomputer)			
Usable bits	1M bits	2M bits	3M bits
Transfer rate	32M bits/s	2M bits/s	0.8M bits/s
Power (W)	60	30	30
Weight (lb)	4	4	8
Size (in.)	PC board in CPU	PC board in CPU	PC board in CPU
System price (typ)	\$7500	—	—
End User Price (cents/bit)	0.75	0.20 to 0.25	0.15 to 0.30

tude slower than normal data transfer speed. While this idling speed is for all practical purposes a stop, CCDs can not really stop completely, and MBMs can —an important advantage.

MBMs have some weaknesses compared to competing technologies. A low cost removable medium is not available for either MBMs or CCDs. Thus low cost, offline storage and data entry applications will remain

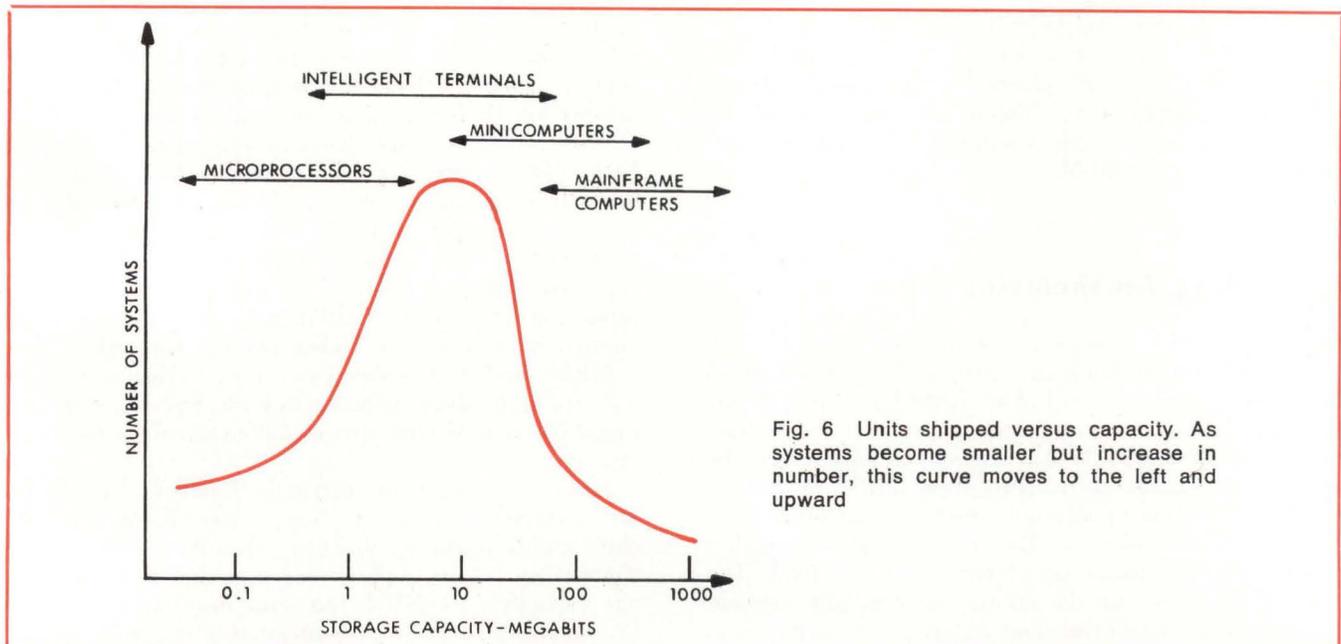


Fig. 6 Units shipped versus capacity. As systems become smaller but increase in number, this curve moves to the left and upward

Cassette	Floppy Disc	Moving Head Disc Cartridge	Fixed-Head Disc
40 s	300 ms	60 ms	8 ms
10K bits/s	250K bits/s	1.5M bits/s	4M bits/s
4M bits	3.1M bits	24M bits	4M bits
1 in 10 ⁷	1 in 10 ⁸	1 in 10 ¹⁰	1 in 10 ¹⁰
3000	4500	4500	10,000
Yes	Yes	Yes	Yes
Yes	Yes	Yes	Yes
4	5	6	5

3M bits	2M bits	20M bits	3.3M bits
10K bits/s	250K bits/s	1.5M bits/s	4M bits/s
25	75	150	350
8	25	60	100
5 x 5 x 5	5 x 14 x 10	18 x 23 x 7	19 x 19 x 12
\$2000	\$2900	\$9000	\$10,000
0.07	0.15	0.045	0.3

in the domain of rotating magnetic memories, specifically disc packs and floppy discs. The relatively low transfer rate of MBM may be a drawback in some applications, but can be overcome with parallel transfer from multiple bubble chips.

MBM is believed to have sufficient attractive features in relation to competing technologies to capture markets from established technologies, and also to have unique characteristics which will serve to create new markets.

MBM Applications

In the early 1970s when bubble technology first showed its potential, it was thought of primarily as filling the cost and access time gap between random-access and rotating magnetic memories. During this period many papers were written about bubble memories' place in the storage hierarchy and cost-performance ratios as compared to other technologies. Magnetic bubbles still have these characteristics, which will be utilized in the so-called fast auxiliary memory (FAM), one of MBM's first applications. (This and other application areas are outlined in Table 4.) This market consists primarily of mainframe computer peripherals and has traditionally been served by drums and either fixed- or moving-head discs. Both CCDs and EBAM will compete with bubbles for FAM applications.

TABLE 4
MBM Applications

Mainframe Peripheral
Fast auxiliary memory
Fixed-head disc replacement
Miniperipheral
Fixed-head disc replacement
Electronic disc
Floppy disc replacement
Operating system storage
Microperipheral
Intelligent terminals
POS, EFTS terminals
Word processors
Programmable calculators
Other microprocessor-based systems
Small Nonvolatile Storage
Measurement and test equipment
Telephone dialer
TV tuner storage
Military Applications
Fixed-head disc replacement
Tape recorder replacement

TABLE 5

Magnetic Bubble Memory Status

Company	Contribution
Bell Laboratories	Pioneering research and development Developed 0.46M-bit module Production being readied Product developments underway
Hewlett-Packard	Reported 32K-bit chip
IBM	Research on amorphous materials Research on contiguous disc Research on bubble lattice file
Rockwell International	Reported 64K-bit block access chip Demonstrated 100K-bit serial chips Demonstrated 0.8M-bit module Military contracts Pilot production being readied
Univac	Reported 16K-bit chip
Texas Instruments	Demonstrated 265K-bit module Demonstrated 100K-bit chips Military contracts—will deliver 100M-bit systems Pilot production being readied
Fujitsu	Reported 80K-bit chip
Hitachi	Announced a 32K-byte module 64K chip in pilot production 256K chip in development
Nippon Electric	Demonstrated 16K-bit chips Reported 100M-bit system
Plessey	Reported 8K-bit chips Reported 16K-bit chips
Philips	Published papers

A second and perhaps more important application area for magnetic bubbles is as microperipherals, offering an appropriate secondary storage for microcomputers at a reasonable price, just as the moving-head disc cartridge and a scaled-down magnetic tape drive filled a similar demand for early minicomputers and the Philips cassette, 3M cartridge, and floppy disc satisfied that for lower entry priced mass storage in more recent smaller and less expensive systems.

Today's explosion in the use of microprocessors will create a demand for still cheaper secondary memory, with 1M to 2M bits of magnetic bubbles on the same printed circuit board with the microprocessor, and primary read/write and read-only memory. In the majority of these applications, nonvolatility is very important. Below 2M bits, only two nonvolatile read/write memory technologies are currently feasible: magnetic bubbles and core. MBM will certainly have a large price advantage over core.

A bell-shaped curve (Fig. 6) shows how microprocessors, intelligent terminals, and minicomputers are using mass memories today. The peak represents the high yearly shipments of cassettes, cartridges, and floppy discs. With the availability of CCDs and MBMs

and the large shipments of microprocessors, the peak will become higher and will move to the left.

Bubble Memory Status

Magnetic bubble memories have developed rapidly. Most pioneering research and development took place during the period between 1969 and 1973; by the end of 1973, Bell Laboratories' and Texas Instruments' 16K-bit working chips were typical of the state-of-the-art.

During 1974 and 1975, bubble memory system prototypes were developed. A 460K-bit bubble memory module built at Bell Laboratories² is a typical example. Texas Instruments had a 256K-bit bubble memory module interfaced to a minicomputer¹³ in 1974, and has also operated a 100K-bit single chip.¹⁸ Rockwell International demonstrated a 0.8M-bit bubble memory module at several conferences during 1975.

By the end of 1976, several manufacturers should commence pilot production. Western Electric's production facility should have started¹⁶; Rockwell International expects to have commercial production underway¹⁹; while Texas Instruments will also have started

bubble memory pilot production.^{13,18} Volume production can be expected to begin 12 to 18 months later. Chips that will go into production have capacities of 64K to 100K bits and serial or major-minor loop organizations.

The time from bubble memory prototyping to volume production appears quite long. Although bubble memory production is similar to semiconductor production, it is nevertheless different enough to require separate production lines, at the cost of much time and large investments. However, once bubble memory production has started, improvements can rapidly be incorporated, such as larger, faster, and better chips.

Many companies are involved in bubble memory development, both in the U.S. and in Europe and Japan (Table 5). Worldwide, over \$20M is estimated to have been invested annually in MBM technology over the last few years.²⁰

Future Development

Although current bubble memory technology has impressive characteristics, there is room for large improvements. Key to lower bit-price of bubble memories is to pack more and more bits on a single chip. Today's packing density for MBM is about 1M bits/in.²

Using the TI-bar propagation method, a packing density increase of at least an order of magnitude seems possible by 1980, just by shrinking the bubble size. This means that a 1M-bit bubble chip is not unreasonable by that year.² Such a chip would have longer shift registers than current chips, and operate with both shift and transfer rates an order of magnitude higher than at present to keep the access time constant. Similarly, with smaller capacities, access time will improve to the submillisecond range. Using new technology, packing densities of well over 10M bits/in.² are possible in the 1980s. An example of such technology is contiguous disc propagation,⁷ which is currently being developed in several research laboratories. The contiguous disc propagation shown in Fig. 2 has the advantage of requiring fewer manufacturing tolerances than other propagation methods—which translates into higher packing densities.

The bubble lattice file^{2, 19, 20} packs bubbles much more closely than conventional bubble shift registers, storing information in two kinds of bubbles with different magnetizations. To fetch data from a bubble lattice, file groups of bubbles are moved by current pulses in conductors overlaid on the lattice. However, this technology is in an early research stage and production is unlikely to occur before 1980.

Conclusion

Magnetic bubbles are a rapidly emerging memory technology which will play an important role in the late 1970s. Bubble memories have many unique characteristics—nonvolatility, low entry price, low bit-price, small physical size, performance characteristics, and simple interfacing—which will fit a variety of applications—from mass memories for microprocessor systems to electronic discs for mainframe computers. Modularity allows magnetic bubbles to be scaled cor-

rectly for small nonvolatile memory applications, while the price/performance ratio fits fast auxiliary memories for large computers.

Both U. S. and foreign organizations are investing heavily in bubble memories. This sizeable investment makes the success of the technology in the marketplace probable.

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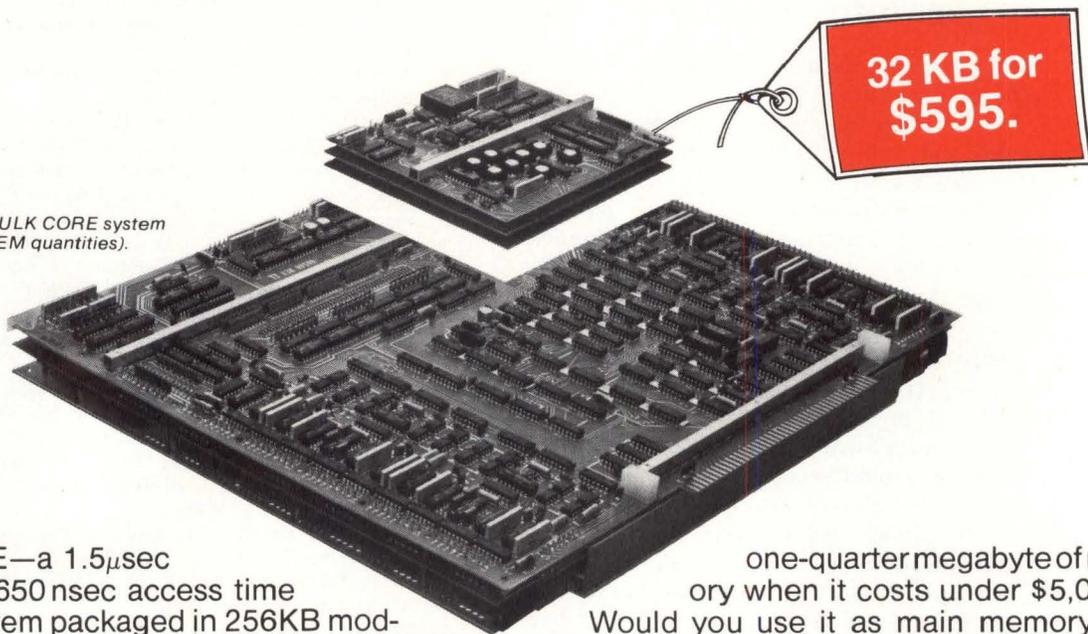


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Generating programs to solve design problems in micros, new to many engineers, need not be a headache, although some of the alternatives may seem puzzling at first sight

Software Support for Microprocessors Poses New Design Choices

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Emergence of microprocessors has required hardware design engineers to consider software more than at any other time in the past. One problem is how microprocessor software will be generated. Alternative methods, while not overwhelming, are numerous enough to require careful thought and planning. Failure to consider existing alternatives will burden the design engineer with tools that were supposed to make his job easier.

Software for the microprocessor can be generated using a time-share service, dedicated minicomputer, large computer system, manual methods, or a microcomputer built around a specific microprocessor. Each has advantages and disadvantages.

```
NAM TEST
ORG $1000
LDA A =%01010101
LDX #S200
REP STA A X
CPX #S27F
BEQ R2
COM A
INX
JMP REP
R2 RTS
END
```

Fig. 1 Assembly-language program. Most programmers prefer to write programs in a language such as this, if not in a higher level language such as FORTRAN. To translate these instructions into machine language requires an assembler, a program on the same machine that will run this program, or a cross-assembler on a different machine

Cross-Assemblers and Simulators

Instructions to be executed by a microprocessor are written by the designer in microprocessor assembly-level language (Fig. 1). Software converts the resulting instruction sequence or program into two forms: an assembly listing (Fig. 2), a documented form of the program; and an object program (Fig. 3), which is the binary code that is loaded into the microprocessor memory for execution. The assembly listing duplicates the programmer's written version of the program (right of Fig. 2) and also shows it in hexadecimal form, with program reference lines numbered in sequence, instruction addresses (also in sequence, taking into account differing instruction lengths), and real operand addresses replacing the symbolic addresses of the assembly language version. All of this is laid out in a format that is easy to read and correlate with the symbolic version. The object program is identical to the hexadecimal side of the assembly listing, except for the format; although shown in hexadecimal notation, it represents the undifferentiated string of bits that it actually is.

If the software that converts the programmer's listing into object code resides in a computer other than the selected microprocessor, it is called a cross-assembler. Cross-assemblers are usually written in FORTRAN to run on almost any computer. On the other hand, if conversion software resides in a computer

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00001				NAM	TEST
00002	1000			ORG	\$1000
00003	1000	86	55	LDA A	##%01010101
00004	1002	CE	0200	LDX	#\$200
00005	1005	A7	00	REP STA A	X
00006	1007	8C	027F	CPX	#\$27F
00007	100A	27	05	BEQ	R2
00008	100C	43		COM A	
00009	100D	08		INX	
00010	100E	7E	1005	JMP	REP
00011	1011	39		RTS	
00012				END	

Fig. 2 Assembly listing. Output of assembler is machine-language program in listing correlated with original assembly-language listing

S0060000	4844521B	
S1131000	8655CE0200A7008C027F270543087E1078	
S10510100	5399C	
S9030000	FC	

Fig. 3 Object program. Program is loaded into microprocessor memory in this form—a string of bits, shown here in hexadecimal notation with accessory information. Checksum is 1's complement of 8-bit sum of all bytes in record; it may come in handy as a means of locating an error in assembly or listing

using the selected microprocessor, it is called an assembler. Both forms produce identical outputs.

The program used for illustrative purposes is part of a software routine that tests a solid-state memory. During a complete test of the memory, patterns of alternate 1s and 0s are written into the memory cells and then are read from the memory.¹ One section of the routine loads the bit patterns, 01010101 and 10101010, into alternate memory locations. Following the program, as shown in Fig. 2, we see that

Line 1 gives the name of the program, which is required for this cross-assembler

Line 2, the ORG statement, defines the starting location in the microprocessor memory in which the program is stored. In this example, starting memory location is hexadecimal 1000 or decimal 4096

Line 3 contains the bit pattern or binary value, 01010101, loaded into microprocessor register A. In hexadecimal notation the value is 55_H

Line 4 loads memory location 200 into the microprocessor register X. This is the first location in which the bit pattern, 01010101, is to be stored

Line 5 stores the bit pattern in register A into the memory location specified by register X. In this example, when the program starts, register X contains the hexadecimal number 0200_H. Therefore, the bit pattern in register A is loaded into this memory location

Line 6 compares the contents of register X with a fixed number, the highest address of the memory to be tested
Line 7 tests to determine if the upper memory limit has been reached; if the result of the comparison is an indication of equality, the next statement executed (line 11) terminates the program. Otherwise line 8 is executed

Line 8 complements or inverts the binary pattern in register A; ie, it changes the bit pattern 01010101 into 10101010 (hexadecimal value AA) or vice versa in subsequent passes through the routine

Line 9 increments the contents of register X, initially loaded with 200_H, this instruction changes it to 201_H, and later to 202_H, 203_H, and so on

Line 10 repeats the routine by jumping to line 5. Where the first pass loaded hexadecimal 55 into location 200, the second loads AA into 201. All statements are executed until all memory locations have the required alternating pattern

Execution of this program can be simulated on a different computer. Simulator software provides complete information about memory status, accumulators, registers, program counter, stack pointer, and execution times for each instruction. Object program is stored in the simulated memory and the microprocessor status is printed each time an instruction is "executed."

Data outside of the colored block in Fig. 3 are information that the microcomputer or simulator program requires to load the object tape into its memory. Printed contents of memory location 1000-1011 (hexadecimal) after the object tape is loaded into simulated memory (Fig. 4) are identical to the object code produced by the assembler (Fig. 3). As the simulator program "executes" the program, it prints out step-by-step results (Fig. 5). It shows, for example, how register or accumulator A contains hexadecimal value

```

1000 86 55 CE 02 00 A7 00 8C 02 7F 27 05 43 08 7E 10
1010 05 39 00 00 00 00 00 00 00 00 00 00 00 00 00

```

MEMORY CONTENTS AFTER PROGRAM IS LOADED

MEMORY LOCATION

Fig. 4 Simulated representation. Object program can be printed out by simulator; each line is 16 consecutive bytes in hex notation, beginning at an address that is a multiple of 16. Last byte in program is in location 1011; all locations beyond contain 0s

(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	
1000	LDA	A	1001	1002	0000	55	00	000000	0000	000002
1002	LDX		1004	1005	0200	55	00	000000	0000	000005
1005	STA	A	0200	1007	0200	55	00	000000	0000	000011
1007	CPX		1009	100A	0200	55	00	000000	0000	000014
100A	BEQ		100B	100C	0200	55	00	000000	0000	000018
100C	COM	A	100C	100D	0200	AA	00	00N00C	0000	000020
100D	INX		100D	100E	0201	AA	00	00N00C	0000	000024
100E	JMP		1010	1005	0201	AA	00	00N00C	0000	000027
1005	STA	A	0201	1007	0201	AA	00	00N00C	0000	000033

Labels for Fig. 5:

- MEMORY LOCATION (points to column 1)
- INSTRUCTION BEING EXECUTED (points to column 2)
- MEMORY LOCATION OF OPERAND (points to column 3)
- LOCATION OF NEXT INSTRUCTION (points to column 4)
- CONTENTS OF INDEX REGISTER (points to column 5)
- CONTENTS OF ACCUMULATORS (points to column 6)
- CONTENTS OF CONDITION CODE REGISTER (points to column 7)
- STACK POINTER (points to column 8)
- CUMULATIVE EXECUTION TIME (points to column 10)

Fig. 5 Simulator output. Simulation prints out status of machine after each instruction is executed. Sequence resembles assembly listing of Fig. 2, but last instruction in this partial listing repeats the third line, with different operand and different word in accumulator. Full simulation would print out long sequence of lines like these, until compare instruction (CPX) discovers an equality and branch-on-equal instruction (BEQ) takes the program out of the loop. At this point a bit in the condition code register would indicate the condition for the branch; the register is not otherwise used in this routine, although other bits change from time to time. Stack pointer is not used at all here, although simulator prints its contents

55_H and then changes to AA_H. These numbers are stored, in binary, in memory locations 0200_H and 0201_H. After execution is continued for a further period of time, the contents of memory appear (Fig. 6) as alternate 55_H and AA_H patterns between memory locations 0200_H through 025B_H inclusive.

Support Software on a Time-Sharing System

As a means of writing, checking out, and generating programs with low capital investment, various national time-sharing systems support most microprocessor software. Primary cost is rental of a time-share terminal, which usually consists of a teletypewriter, modem, and paper tape reader/punch. Other costs are connect

```

0200 55 AA 55 AA
          •   •   •   •
0250 55 AA 55 AA 55 AA 55 AA 55 AA 55 AA 00 00 00 00
0260 00 00 00 00 00 00 00 00 00 00 00 00 00 00
          •   •   •   •

```

Fig. 6 Contents of memory after execution. This routine stores pattern of alternating 1s and 0s at all memory locations beginning at hexadecimal 0200. Simulator prints out this pattern when program has reached location 025B

charges, computer resource units (CRUs), character input/output (I/O), and program storage.

Connect charges are for the amount of time the user is connected to the computer. Typical costs are \$6 to \$9 per hour.

CRUs measure the amount of actual central processor unit (CPU) time the program uses when running the microprocessor software. Typical charges are \$0.10 to \$0.12 per unit, where a unit is $\frac{1}{10}$ second of CPU time. The user has no direct control over the number of CRUs, which directly depends upon the efficiency of the microprocessor cross-assembler program. Some cross-assembler programs are very inefficient, and require a great deal of central processor time—costing as much as \$25 to \$30 each time a program having 50 to 60 statements is assembled.

Character I/O is the number of characters transmitted and received by the time-sharing computer, at \$0.20 to \$0.30 per 1000 characters.

Program storage is the memory in the time-sharing system that is required to store a program. Typical charges are \$0.70 to \$0.80 per 2000 characters per month.

If a company is just beginning to use microprocessors, and anticipates small projects that do not require a large amount of software development, time-

sharing is probably a good choice. However, during the first weeks or months, costs will be high, until engineers learn the software (Fig. 7).

On lengthy projects that require 12 to 18 months for development, time-sharing costs may be a disadvantage. Cost on a time-sharing system can be controlled only with amount of usage. Decreased usage has to trade-off schedules with technical design of the project.

Dedicated Minicomputer Support System

Running cross-assembler and simulator software using a dedicated minicomputer approach is an expensive alternative. A minimum system would require a 16-bit CPU with 32K memory, a mass storage unit (moving head disc), and the usual stable of peripheral equipment: line printer, card reader, paper tape reader/punch, and I/O console. Beyond these hardware costs, cross-assembler and simulator software cost approximately \$1000 each and require FORTRAN capabilities on the minicomputer.^{2,3}

No matter what software vendors may say about software having been written in "standard" FORTRAN, the program will probably need modification to run on a

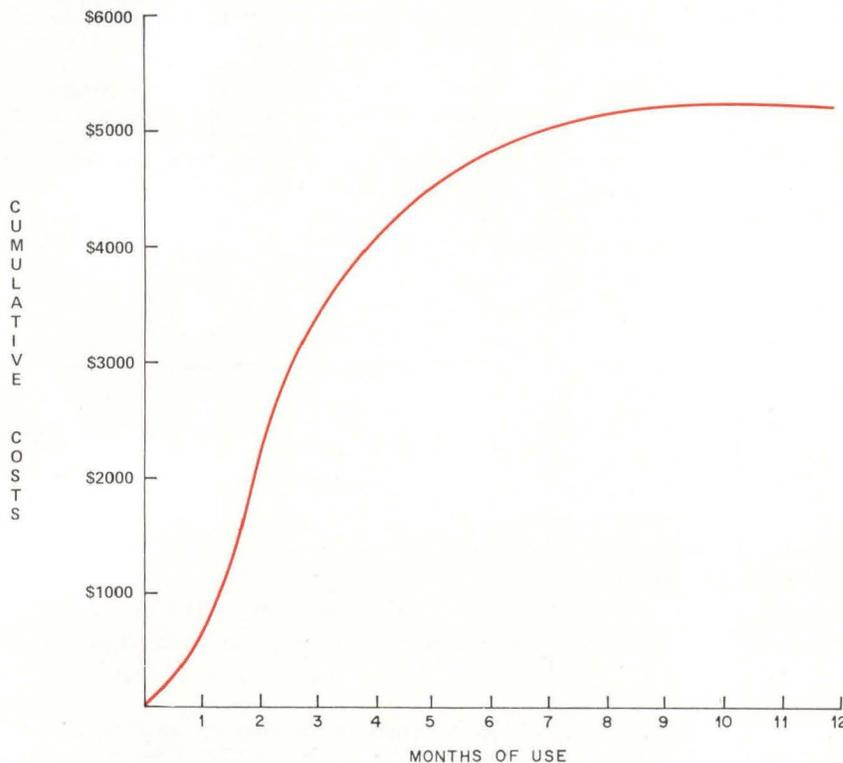


Fig. 7 Time-sharing costs. Although steep at first as users "learn the ropes," costs usually taper off toward end of first year. They may increase again when project enters test, debug, and documentation phases

particular machine. If the user is not an experienced FORTRAN programmer, he will find it difficult to install purchased software on the host machine in a reasonably short period of time, and may have to resort to time-sharing anyway.

If purchased support software is for a relatively new microprocessor and has not been used extensively, it will probably contain errors. The user should take care not to be the one to debug it for the vendor. These errors are extremely difficult to find; if not corrected they will make the software worthless to the design engineer.

If initial costs and problems are not too great, the dedicated minicomputer offers advantages of quick program turnaround, faster learning experience due to greater usage, and better control over the software product.

Large Computer System

Most medium-size companies have a computer on which they run inventory or payroll. Depending on its type and size, it could also serve part-time as an engineering tool. Purchased software could be installed and engineers could use it as a batch machine. Depending on the computer load, program turnaround time (time

period measured from program submission to availability of results) could be from 2 to 24 hours. This approach provides the advantage of using existing equipment, and requires only that the user purchase software and install it on the host computer. However, the user loses capability for interactive conversation, a desirable feature when using a simulator. Another disadvantage is that most large computers do not have paper tape output, requiring the engineer to manually generate object tapes.

Manual Generation of Object Code

Probably the least desirable alternative is to manually convert the assembly programs into machine code. This is feasible only for small programs having 60 to 100 statements.

Microcomputer Support System

The microcomputer offers the best alternative. Relatively low in cost (\$4000 to \$10,000), a microcomputer support system is usually built around the specific microprocessor; as a software development tool, therefore, it tests programs in a true execution mode rather than by simulation. Of two microcomputer configura-

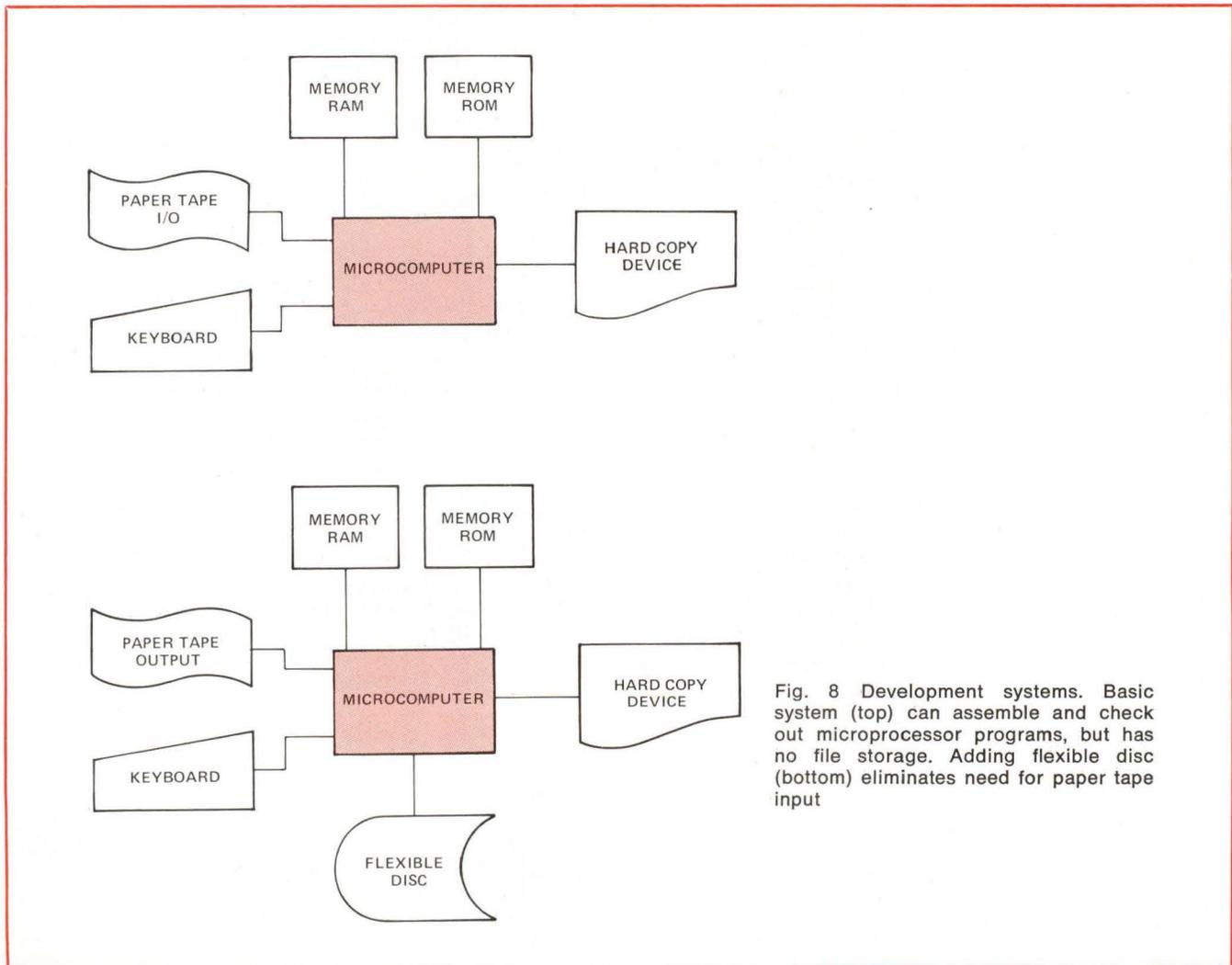


Fig. 8 Development systems. Basic system (top) can assemble and check out microprocessor programs, but has no file storage. Adding flexible disc (bottom) eliminates need for paper tape input

tions (Fig. 8), from an experienced point of view, the more complex is preferable, because it eliminates the cumbersome paper tape as a primary input device but can use paper tape output to program read-only memories. Usually a slow, low cost teletypewriter with paper tape punch and reader will serve this purpose, since the paper tape punch is not often used.

Disadvantages of this alternative are the slow I/O devices and the narrow usage of a particular microprocessor. As dynamic as the microprocessor market is now, selection of another microprocessor will require a similar, but not identical, software tool.

In Case of Purchase

Up to this point, five alternatives for microprocessor software development have been discussed. They all assume that the necessary supporting software, if any, is available—say on the time-sharing system or the computer that runs the cross-assembler. However, a sixth alternative remains—that of purchasing the necessary software and running it on an existing large or small system to produce the programs in a language appropriate to the microprocessor.

If this last alternative is chosen, results in the long run may be satisfactory, but difficulties may be encountered in the short run. The main problems with such portable software are statement ordering and variable initialization.

Every program of this nature uses a number of declarations, which must always be at the beginning of the program before any executable statement. Declaration statements define areas of storage, names of variables, and conditions that must be set up in the system to run the program properly. In some computers these statements must themselves be in a particular order; that order can be found in the computer's FORTRAN reference manual.

Among the initialization problems that occur are overlooking differences between data formats in a particular computer and formats assumed by the intended supporting software. For example, some 16-bit machines represent negative numbers in 2's-complement form, which means that the left-most bit in any word is a sign bit. Therefore, the largest positive integer that these machines can handle is a string of fifteen 1s (preceded by a 0 to indicate positiveness), represented in hexadecimal notation by 7FFF and in decimal by $2^{15} - 1$, or 32767. However, some cross-assemblers use values such as FFFF or 8000 (both in hexadecimal) in logical operations and to complement or mask bits in other variables. Users should check for the presence of this convention and modify the software accordingly, or run the risk of encountering elusive program bugs.

The American Standard Code for Information Interchange (ASCII) defines a basic set of 64 characters and an extended set of 128, the latter including both upper- and lower-case characters and certain control signals that are useful in data communications. Some cross-assemblers can work with the 64-character set, aided by certain conventions that make sure all characters are defined and recognizable; but some FORTRAN compilers work with only the older 48-character Hol-

lerith character set, and reject other variables—even if the assembler defines them. Again, the computer's FORTRAN reference manual contains a table of the character set recognized by the compiler; any characters not included in this set but required by the cross-assembler must be redefined.

Redefinition can be done in two ways: by specifying the unacceptable character in terms of its internal bit arrangement, listed in hexadecimal or octal form, or by a numerical equivalent (in decimal) of the internal arrangement. For example, the ASCII character set includes the symbols =, +, and !, which are equivalent to 3D, 2B, and 21 in hexadecimal. If the symbols are followed by a space (hexadecimal 20), as is often the case in an initialization statement defining a variable, the hexadecimal equivalents become 3D20, 2B20, and 2120. Decimal equivalents of these representations are 15648, 11040, and 8480. If specified in this way, the compiler accepts them and produces the appropriate bit configurations, which the assembler then recognizes in its own way.

Additional Good Practices

Installing the program may be easier if a macro flow-chart is drawn to help visualize various sections of the program. Understanding the flow of data may also be simplified if every subroutine is listed along with each subroutine that it calls and each that calls it. Because subroutines can sometimes be nested five or six levels deep—that is, call one another without passing control to the main program—the flow can become confusing.

Conclusion

Support software for microprocessors need not be a problem if the user is aware of alternatives in generating the software. Each solution described in this article has advantages and disadvantages to the potential user. Support software, such as cross-assembler and simulator, should be thought of as tools, just as are an oscilloscope or voltmeter, which help the engineer perform a job efficiently.

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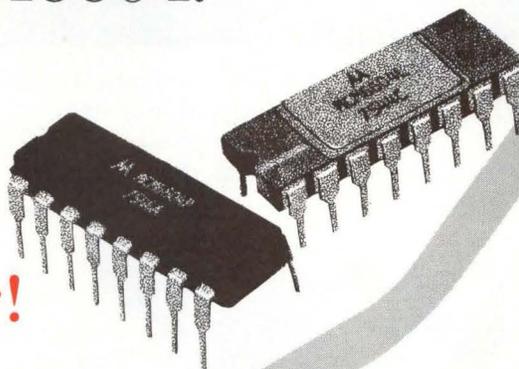
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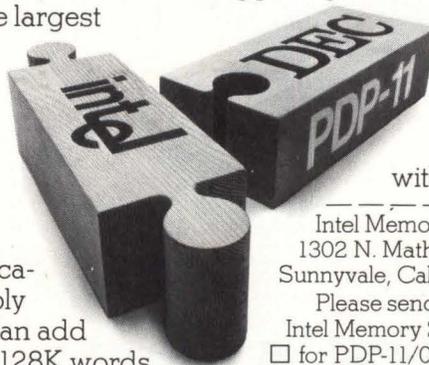
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Two methods of extending a computer's memory capacity are often called by each other's name, although they are quite different; each has its own advantages and disadvantages

Clearing Up the Confusion: Virtual vs Mapped Memory

Daniel J. Tanner

**Interdata Incorporated
Oceanport, New Jersey**

More than a few computer users, salesmen, and even analysts are confused by "memory mapping" and "virtual memory," as well as other black boxes attached to their computers. Their uncertainty lies in what each will and will not do, and how to describe the difference. Their dilemma is not surprising; more than one vendor represents mapped memory as virtual memory, and both schemes usually involve the concept of a map.

Yet this jargon need not be so perplexing. No present vendor of 16-bit minicomputers offers virtual memory (although some put that name on their mapped memories), while only one minicomputer vendor and a few mainframe vendors currently offer virtual memory in some of their systems. Interdata's Memory Access Controller (MAC) occupies a sort of intermediate position between virtual and mapped memory. In an operating system environment, its operation is completely transparent to most programs. It is similar to a peripheral device in that only the operating system modules directly responsible for its operation need be aware of its existence.

MAC allows an operating system to provide support to user programs in such a way that the program can be coded as if some subset of available memory, starting at address 0, were available to the program. The range of addresses thus referenced by the program is called the program address space. At load time, MAC can be used to map this program address space into available physical memory addresses so

that any program address, referenced during program execution, is translated (relocated) to the correct physical address before memory is accessed.

Stated simply, virtual memory often uses the total addressing capability of an architecture, or at least a large part of it implemented in the processor, to provide an address space that is larger than the physically attached memory; while mapped memory involves using the total physically attached memory, which is larger than the processor can directly address because of architecture (Fig. 1).

For example, one processor's architecture may have an instruction format that includes a 24-bit address. Such an address can point directly to over 16M words, bytes, or other minimum addressable unit. Single computers that physically attach such huge memories are not available; but virtual memory systems that large, together with a real memory of much smaller capacity—say a million words—are available.

Another processor's instruction format may provide for a 16-bit address, which can directly point to only 65,000-plus words; the processor, however, routinely attaches a 1M word main memory, accessing all parts with memory mapping.

Extra Hardware and Software

Both virtual memory and mapped memory require some legerdemain in both hardware and software. Most

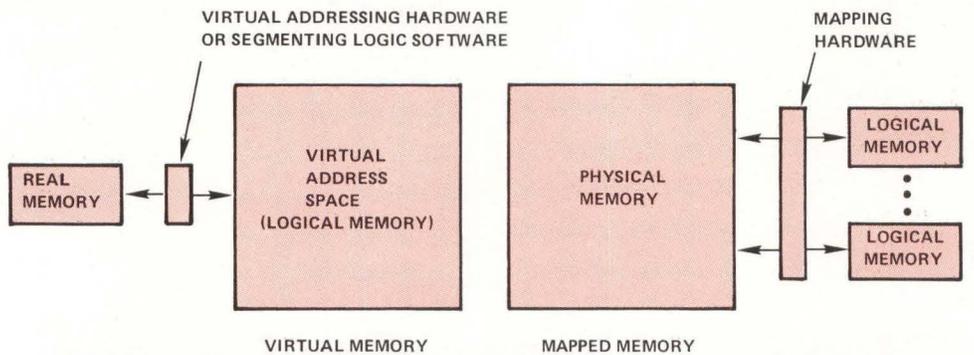


Fig. 1 Virtual vs mapped. Two widely used forms of extended memory often confused are actually inverses of each other. Virtual memory is larger than it looks, while mapped memory looks larger than it is. Both techniques make accessible large programs through limited facilities

virtual memory* requires hardware to translate an address supplied by the programmer into an address somewhere in real memory, and software to transfer desired data from secondary storage into real memory, where the translated address can point to it. The hardware is one or more registers that define which part of virtual memory is in real memory. Mapped memory requires, in addition to extra memory, a technique of dividing real memory into blocks and limiting all activity during a short period of time (ie, directing the activity of a particular task) to a single block.

The mapped system requires a program or any contiguous part of a program to be limited to one of these blocks, preceded by a firmware instruction that says, in effect, "Starting now, and continuing until the next instruction like this one, all references to memory addresses between 0 and 10,000 will actually point to locations between 50,000 and 60,000—the real addresses in this block now in use." The instruction would cause the first address of the current block to be stored in a mapping register and added to every user-supplied address.

In a multiprogramming mapped memory system, several blocks may be assigned to users; each user has access only to his own block while he is connected. Blocks are correlated with multiple mapping registers that translate addresses for various blocks. Before any user can go to work, he (or, usually, the operating system acting for him) must load his mapping register to define his block, much as a single user does.

Inside-Out Registers

Most virtual memory and mapped memory systems are alike in their use of registers. In a mapped memory, the registers define blocks; in virtual memory, they

define which part of virtual memory is in real memory (Fig. 2). The latter registers are called dynamic address translation (DAT) hardware by IBM. Although similar in concept, the registers' functional uses are inverses.

One important difference in system operation, however, is in the handling of the program status word (PSW), which describes the state of the machine at any given time. Substitution of one PSW for another is the mechanism by which the machine can interrupt one process, execute another, and return to the first at the point of interruption. The PSW always includes the current program counter. When a mapped memory is in use, the counter's capacity is the same as that of one page (because of the limits imposed by 16-bit architecture), so that some mechanisms other than the PSW must keep track of which page is in use at any moment. With a virtual memory, the program counter has a great many bits (because of the, usually, 32-bit architecture), all of which are part of the PSW. Therefore, the PSW need not be concerned with the program's actual location (real or virtual memory).

In some systems, each block in a mapped memory must be smaller than the addressable range available to the user, because it must also contain some overhead relating to its communication with the operating system and with input/output (I/O) devices; that is, the user's addressable range includes some addresses he cannot use because they are reserved for these overhead functions. Thus, while a system with 16-bit addresses theoretically can address up to 65,536 words, overhead requirements may preclude use of the most significant address bit.

*Virtual memory comes in demand paged or segmented form. Since only one mainframe vendor uses segmented virtual memory, and all others use demand paged, we refer here and elsewhere to the more common type.

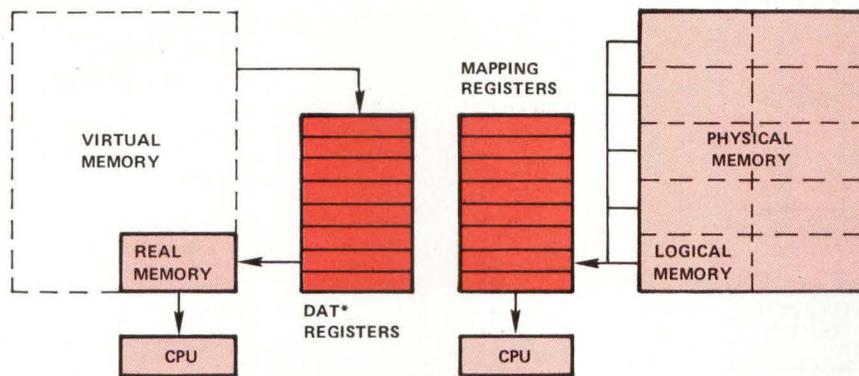


Fig. 2 Register inversion. Both virtual and mapped memory use registers—the former to show what part of a large data array is in small real memory, and the latter to define small blocks in a large real memory

*Dynamic Address Translation

One recourse is to ignore that bit, and make do with a 15-bit address and a 32,768-word space. Then if real memory capacity is 131,072 words, it can hold four of these 32K tasks. Each task is limited to that much space—and one of the four tasks is the system overhead. In this case there are four mapping registers, each with two bits to identify one of the four blocks (Fig. 3). The 15-bit user address plus the 2-bit mapping register constitute the 17 bits required to address any word in the 131K real memory. Three users can be on the system at one time; the fourth “user” is the operating system, for which 32K is probably more resident storage than it needs, since most of it is over-

laid as needed. Mapping restricts each of the three real users to his own 32K space, but each has use of the full space.

Another solution is to put part of the overhead in every page. In this case, the main operating system resides in its own page, with necessary overlays, leaving (in the example just given) three pages for users. The operating system, however, is more compact, occupying less memory, or doing more work in the same memory as before; while the users have 28K apiece. The other 4K in each user’s page is reserved for a particular function of the operating system that he uses—eg, device handler or FORTRAN run-time

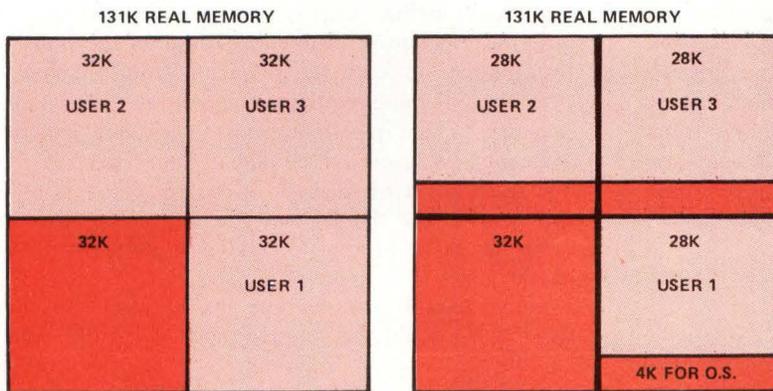


Fig. 3 Space restrictions. In a mapped memory at least one full page must be devoted to overhead (left) or part of every page as well (right)

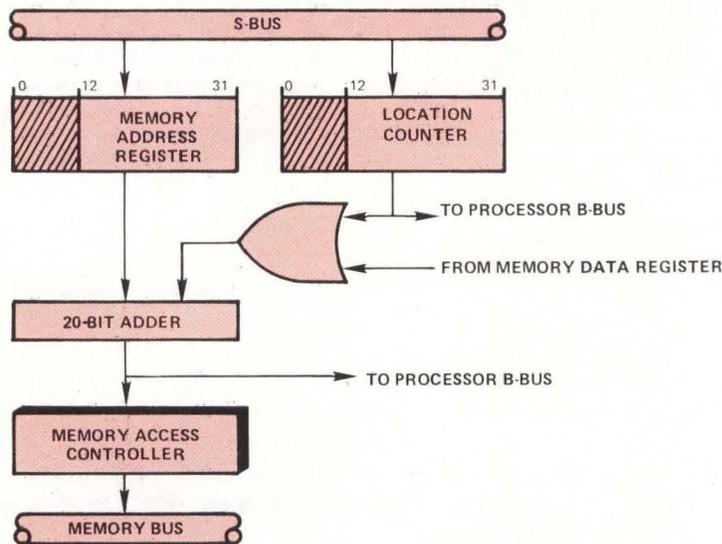


Fig. 4 Interdata's MAC. Memory relocation and protection is provided by the Memory Access Controller (MAC), a device that monitors all memory accesses. Under program control, it can (a) translate the address of a memory access from a 20-bit program address to a 20-bit physical address, (b) prevent write access to a block of memory, (c) reject instruction execution from a block of memory, or (d) detect an invalid memory access

library—and he does not have free access to it. The mechanism that keeps him out of this “overhead memory” is part of the hardware. These functions are copied as needed, and thus may be found more than once in the full 131K memory. Users who need several of these special functions simultaneously obtain them at the expense of their assigned memory space, which may shrink to 24K, 20K, and on down in 4K units.

Thus virtual memory lets addressable program space exceed real memory, while mapping lets real memory exceed addressable program space. Software and hardware for systems with either mapping or virtual memory usually make these benefits transparent to the user, by letting him write and run location-independent code. Operating systems may also provide dynamic allocation of memory.

Two Virtual Flavors

Virtual memory comes in two forms, segmented and demand-paged. Demand-paged virtual memory uses a mapping concept. It breaks up a program into “pages” of small equal size, and stores them on a fast disc or drum. It also logically divides physical memory into page-sized frames with hardware, and manages the pro-

cess of filling active physical memory with appropriate program pages on a demand basis.

Segmented virtual memory does not use a map. Rather, a program is divided into a root portion and a number of other segments. The root remains memory resident and calls other segments as needed. The compiler generates the root and its segments, but the user must be sure that the real memory, or the part that he is using, usually his partition, is at least as large as the largest segment. This puts the onus on the programmer to keep the segments from varying widely in size and thus requiring huge areas of seldom-used memory. That is, although he does not generate the segments, he is concerned about their sizes; if they are disparate, a lot of memory is wasted. This is especially true under the 80/20 rule, which says that in any program, 80% of the processing is performed by 20% of the code.

Quite possibly, under the 80/20 rule, the most active 20% could be tightly and efficiently generated by the segmenting compiler, but at run time would require only a fraction of the partition allocated, because some routines in the 80%, which is hardly ever used, were generated to be much larger. While no programmer has to segment his program this way, the segmenting compiler cannot discern infrequently

used routines. It is analogous to the engineer including in a design a special register used by only one or two instructions in a large repertoire, when, with a little care and planning, one of the general-purpose registers could be used.

The lone advantage of segmented virtual memory is that it costs less to manufacture than does a system with hardware for demand paging. This was especially true in the days of relatively high cost hardware and lost cost programmers. Demand-paged virtual memory does require a lot of hardware—a high performance direct-access device for paging, address translation hardware, and a hardware algorithm to determine which page to send back to the paging device when physical memory is full and a new page becomes active. This hardware algorithm is usually firmware in a read-only memory. Its design also affects how much time is spent swapping the 20% of code to and from the paging store; the 80/20 rule says this code should not be swapped at all, or swapped only very infrequently.

Demand Preference

Nevertheless, most manufacturers use demand paging in preference to segmentation, because advances in technology have reduced the cost of the extra hardware, while people-costs have risen dramatically. Clearly, demand-paging requires more engineering design effort than segmentation.

Mapped memory as opposed to virtual memory simply establishes a one-to-one correspondence between the program spaces of several small tasks or programs and the larger domain of the system's real memory. The tell-tale characteristic is that the size of mapped tasks must be small. Since mapping involves hardware, the expense is often avoided by making the hardware optional. It is not sold unless the memory for the system is to be larger than the largest task.

Trade-Offs of Mapping

Memory mapping, on minicomputers that use 16 address bits, brings up drawbacks that are not found in systems that use 20 or more address bits. For example, a 16-bit machine may have a 262K-word memory attached, and thus will require mapping to utilize all of it. It might have very small pages of 256 words, and require 1024 mapping registers to cover the whole memory; alternatively it could have substantially larger pages of 4096 words, and cover the memory with only 64 mapping registers.

This is the basic trade-off of mapped memory: the number of mapping registers against the page size. Smaller pages provide finer "granularity" in memory usage, which means that separate tasks and subtasks may conveniently fit in separate pages; but small pages require more mapping registers and more bits

in each register, both of which contribute to cost. In multi-user systems these pages would be divided among users in some way. If, to reduce cost, a hardware design specifies larger pages and fewer shorter mapping registers, the user may run out of pages without running out of space within pages. If he is willing to spend more money to have enough pages, he may discover that only his smallest subtasks fit conveniently in one page. Also to be considered, especially in systems constructed for real-time usage, is the time that must be spent loading and storing map registers as the processor's context is switched and the problem of reliably saving and restoring their contents in the event of, say, a power failure. Here, the engineer's contribution can become invaluable; many of today's 16-bit minicomputer systems suffer from serious inadequacies in these respects.

In another way the mapped-memory tradeoff affects computer utilization if the operating system requires some of the mapping registers for its own use. For example, it may use them in connection with its I/O controls or with a FORTRAN run-time library. If the pages are 4096 words each, every register taken over by the operating system shrinks the memory available to the user by that amount. Here, although smaller pages may mean less interference by the operating system, the size of tasks the user can handle is reduced, and costs are increased.

Mapped tasks do not necessarily have to equal the logical memory space permitted. The operating system may support roll-in/roll-out capability (also known as checkpointing), so that a task of, say, 28K words can run in less assigned memory by letting parts of it be overlaid by other parts. However, this creates problems for programmers and degrades task throughput.

Every Interdata minicomputer is capable of directly addressing its entire memory range. Mapping is not provided for 16-bit systems. Rather, the company's position is that if more than 65K bytes are required, the application is one of extended memory, and the advantages of a 32-bit computer are needed. A memory access and protection controller (Fig. 4), which provides memory protection and location independence is optional on a 7/32 and standard with the 8/32. It is required only for operation of the OS/32-MT operating system, and imposes no overhead on memory references.



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A Method of High Density Recording on Flexible Magnetic Discs

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To increase the amount of data stored on one flexible disc requires either more flux changes per inch of track or a better code; the latter is the obvious choice because the former is close to its physical upper limit

Ed Note: *Computer Design* readers will observe that this Tech Note is similar in many respects to another Note on double-density recording that appeared in the September issue of this magazine. Although the conclusions stated here are different from those of the previous author, both arguments are logical and well-presented. Therefore, the editors, who usually do not devote space to the same topic in consecutive months, thought both points of view were worthy of attention. Readers who design or use flexible disc drives or related equipment will want to consider both opinions carefully, and will be interested in a third view that will appear in a forthcoming issue.—WBR

During the last two years, the growth in use of flexible disc files (often called floppy discs) has been phenomenal. More and more applications are being found daily. Discs are useful in applications that require greater performance and reliability than tape cassettes or cartridges can provide, and that cost less per function than removable hard disc packs, such as keyed data entry, point-of-sale systems, remote batch terminals, microprogram loading, error logging, minicomputer program and data storage, and word processing.

In many of these applications, storage requirements are so extensive that they arouse interest in increasing the storage capacity of individual flexible discs. Increasing the linear density along the tracks on the disc surface is the easiest way to do this. To implement such a linear density change requires ei-

ther an increase in the number of flux changes per inch (fcpi) or a more efficient code. The latter is the obvious choice in a disc file that is already operating at densities as high as 6400 fcpi.

Most flexible disc files today use frequency modulation (FM) encoding, which writes data bits (D) at the center of the bit cells, and clock bits at the leading edge of the bit cells. Each clock bit and each binary 1 is represented by a flux change on the disc's magnetic surface, that appears at the output of the detector circuit as a rectangular pulse. Binary 0s are represented by no change in flux and no pulse at the detector. Clock frequency alone is f , corresponding to a stream of pulses from the detector separated by time T_1 when a series of 0s is read. When reading 1s, the frequency jumps to $2f$, and the pulse separation becomes $T/2$.

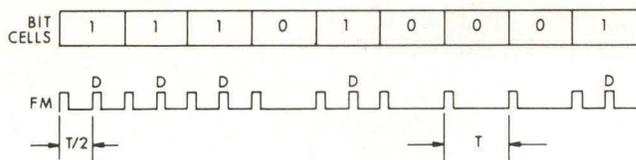


Fig. 1 FM encoding. In frequency modulation encoding of binary data, every bit cell has a clock pulse at its leading edge, and a 1 is stored in the form of a pulse at the center of the bit cell. Method imposes a penalty in the form of unneeded clock pulses

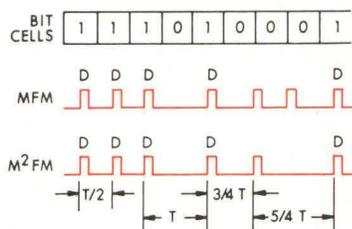


Fig. 2 More efficient codes. Modification of FM (top trace) eliminates clock pulse except between two cells containing 0s. Further modification (bottom trace) also eliminates clock pulse in second cell following a 1. Both codes eliminate unnecessary pulses, and permit recording on disc surface at higher density than ordinary FM

Modified Codes

In FM encoding a penalty is paid in clock bits (Fig. 1). Thus, if the code could be made more efficient by eliminating some of the clock bits, higher information densities could be achieved. One such technique, devised several years ago, is commonly called modified frequency modulation (MFM). This encoding scheme has been used successfully on high performance disc drives such as the IBM 3330 and 3340. Rules for MFM cause data bits (D) to be written at the center of the bit cells, as in FM, and clock bits to be written at the leading edge of the bit cells, but only when both the previous cell and the present cell store binary 0s. Since the sole function of clock bits is to synchronize the clock in the detector circuit in the ab-

sence of binary 1s in the data stream, they are not needed when 1s are present; leaving them out permits a reduction of the average spacing of data bits, thus increasing the apparent density of data stored on the disc without exceeding the physical limits for data and clock bits imposed by characteristics of the medium.

Additional modification of MFM enables more improvements in encoding efficiency through further optimization of the clock signals. This encoding scheme is commonly referred to as modified-modified frequency modulation (M²FM); it writes data bits (D) at the center of the bit cell, as before, and clock bits at the leading edge of a bit cell, but only if the previous bit cell contains neither a 1 nor a clock bit, and if the present bit cell also does not contain a 1.

In both modified forms of FM a given amount of data can be recorded in half the space (Fig. 2); the basic period between pulses is halved, corresponding to the doubling of the write oscillator frequency, but the number of flux changes per inch is the same as for basic FM. Thus the bit cell in MFM or M²FM is half the size of that for FM, and for a given track velocity the data transfer rate is doubled.

Disadvantages of Modified FM

Both MFM and M²FM can double the amount of data stored on a given length of track or a given area of disc, and double the rate at which it is transferred to or from the disc. However, both codes also have disadvantages.

Because the MFM or M²FM bit cell does not always contain a clock bit at its leading edge, encoding and decoding require more complex electronic circuitry. The most reliable method of separating MFM or M²FM encoded data is through use of a phase-locked oscillator (PLO) (Fig. 3). Once synchronized, the PLO tracks recorded information and generates separate "windows" for data bits and clock bits. Staying in synchronization with small, slow variations in disc speed, it averages quick variations caused by bit shift.

Bit shift is characteristic of all magnetic discs and tapes, including single-density flexible discs, but can be more serious with MFM and

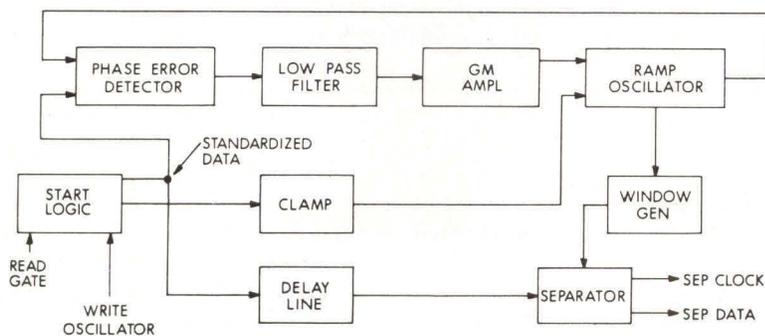


Fig. 3 Phase-locked oscillator. This circuit tracks recorded information and generates separate data and clock signals from it, even when, as with MFM and M²FM, some recorded clocks have been omitted

M²FM. It is a real or apparent tendency for a flux reversal to be read slightly before or after its nominal time. Because the number of flux changes per inch is the same with these high density codes as with FM, the amount of bit shift in absolute terms is the same; but because the bit cell is half the size, the system can tolerate only half as much bit shift without error. Therefore, to reduce the amount of bit shift, a write precompensation circuit is added to the controller logic for a floppy disc drive to compensate for known bit shift patterns.

Since most bit shift is predictable, on the basis of pulse superposition theory, the data pattern can be analyzed in a shift register (Fig. 4) during the write process, and data and clock bits can be written either early, on time, or late. If the pattern would cause a late bit shift, the bits are written early; if the bit shift was early, the bits are written late. Then, during the read process, the bits appear more nearly on time within the PLO window.

Thus the principal disadvantages of both high density codes are minimized, leaving only the problem of deciding which one to use in a particular system. In our opinion, the right code is M²FM. In both codes, minimum data bit separation is $T/2$; but minimum clock bit separation in MFM is also $T/2$, whereas in M²FM it is $(3/4)T$. Although both data and clock bit streams are in the same channel, they can be considered separately. Both streams are subject to bit shift, which is inversely proportional to bit separation, whereas the effectiveness of write precompensation is directly proportional to bit separation. Since MFM encoding has both a $T/2$ clock bit and $T/2$ data bit separation, bit shifts in both fields have nearly the same magnitude. Consequently, the system designer must theoretically use a symmetric PLO window.

In M²FM encoding, however, the minimum separation of clock bits is greater than that of data bits, so that the clock field has less bit shift than the data field. The system designer can take advantage of this difference by designing his PLO data separator with an asymmetric window that has a 60/40 ratio. This asymmetry gives greater system margin and reliability.

One factor that affects the ratio

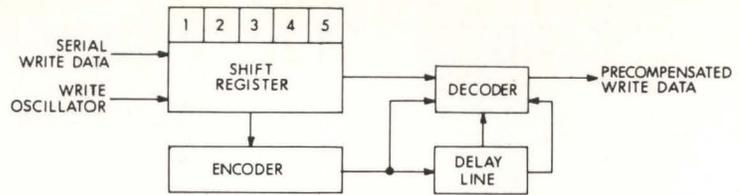


Fig. 4 Write precompensation. Data pass through shift register before being written; if data pattern implies that excessive bit shift would occur when it is read, it is written slightly early or late to compensate for timing error

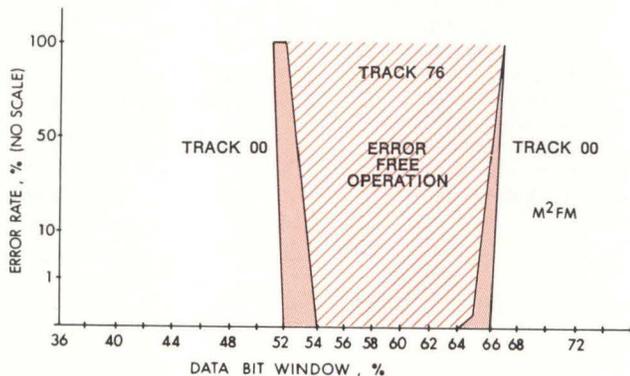
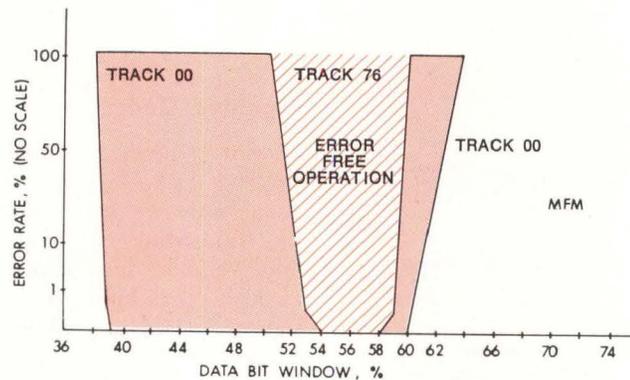


Fig. 5 Margin measurements. Data window for innermost track (crosshatched) is wider for M²FM than for MFM, and is more nearly equal to width of outermost track window, indicating substantially better reliability

of the two windows is the number of bit patterns that have to be checked to determine precompensation. MFM has four such patterns, while M²FM has only three; and one of the three requires much less precompensation (see Comparison of Write Precompensation). Measuring the effect of the window ratios in both encoding methods shows how much more tolerance is found in M²FM (Fig. 5).

These diagrams show the extent

to which the data window, as a percentage of the total bit period, could be varied without encountering errors. The extreme left and right edges of the tinted portion represent measurements of error rates at the disc's outermost track (Track 00). The innermost edges of the tinted portion show error rate measurements at the disc's innermost track (Track 76). The cross-hatched area represents error-free operation on

Comparison of Write Precompensation

	Bit Pattern	Amount of Correction
MFM	→ ← Bit to be written	
	X 0 1 1	225-250 ns late
	X 1 1 0	225-250 ns early
	1 0 0 0	225-250 ns late
M ² FM	→ ← Bit to be written	
	0 1 1 X	225-250 ns late
	1 1 0 X	225-250 ns early
	0 0 0 1	150-175 ns early

all tracks. In any given system the same read/write head serves both tracks as well as all intermediate ones, so the innermost track, which has the highest density, rules the system's performance.

For MFM the error-free windows are from 54 to 58% of the bit period; centered on 56%, the margin is only $\pm 2\%$. As pointed out previously, theory predicts the center of this window at 50%. The difference is due to a small maladjustment in the test setup, which doesn't affect the narrowness of the window or the spread between inner and outer tracks. On the other hand, for M²FM the window extends from 54 to 64%, so that the margin is $\pm 5\%$. The fact that the shaded portion of the M²FM diagram is only slightly wider than the crosshatched portion also shows that the error rate is more nearly the same for all tracks than it is in MFM.

Similar tests with the read/write head purposely misaligned relative to the track it was reading showed a much smaller error rate for a given misalignment, or a much larger tolerable misalignment for a given error rate, for M²FM than for MFM.

Summary

There are many approaches to increasing capacity of flexible disc drives. By far the simplest and most straightforward approach is to use more efficient encoding. Although a number of encoding schemes are available to the system designer, one that offers the greatest system margin and hence data handling reliability is most advantageous to him. We believe the M²FM encoding system satisfies this requirement, and our experience with flexible disc drive systems in the field supports our judgment. □

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New Error-Correcting Technique for Solid-State Memories Saves Hardware

Gary R. Basham

Commercial Memory Products Division
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Hawthorne, California

Innovation in the way check bits are generated reduces hardware, has less impact on throughput, yet offers same error-correcting and -detecting power of traditional codes

An error correction technique, which has been developed for use with semiconductor memory systems, corrects all single-bit errors, detects all double-bit errors, and detects some odd multiple-bit errors. In these respects it is like the classic Hamming error-correcting code, but it has an important difference in that it can be implemented with less hardware. Like all such codes, it exacts a penalty in the time required to process erroneous data; but again unlike the Hamming code, and as an improvement on certain variations of that code, it imposes the same delay on all bits of the word that is subject to correction, and thereby introduces no skew into parallel bit propagation.

Codes like this are increasingly important in semiconductor memories, in which density and intricacy of the chips create a statistical probability of error. In larger systems, hourly cost demands that down-

time be minimized; a small computer application may be process or batch control, where waste resulting from data errors can be harmful. Therefore, error correction can be valuable, provided that the value of the improved mean time between failures (MTBF) exceeds the circuit cost in dollars plus the value of the throughput time penalty.

The proposed design can improve MTBF five to 10 times, while lengthening access time about 20% and adding somewhat less than 30% to the dollar cost of memory. These figures are somewhat less than those for conventional codes.

As in the Hamming and related codes, the technique assigns a section of memory to a parity matrix in which check bits are stored for data sent to memory. Number of check bits required for each word of m bits is c , where $2^c \geq m + 1$. Thus, for a 64-bit word, $c = 7$; seven check bits can correct single-

bit errors. For double-bit error detection only one more check bit is needed. To allow errors in the check bits to be corrected, or detected, along with those in the data bits, the equation becomes $2^c \geq m + 1 + c$. Thus, for the 64-bit example, double-bit detection requires eight check bits. Economically, this is extremely important to computer designers considering error correction options, because obviously cost of error detection and correction is proportional to the logarithm of the data field size; the former increases much more slowly than the latter (Table 1).

Like most other parallel error correction circuits, the system comprises five main sections (see block diagram): generators for write and read check bits, a syndrome generator/decoder, a data corrector, and a check-bit memory. Data passing to or from main memory are the inputs to the two check-bit generators,

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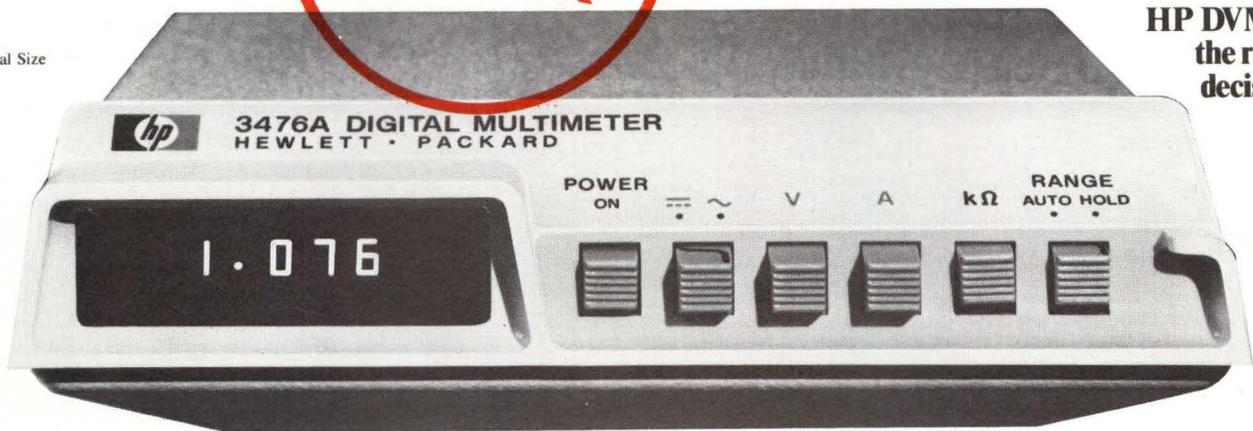
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TABLE 1
Cost of Error Correction

Data Bits	Check Bits	
	(Single Error Correction)	(Double Error Detection)
8	4	5
16	5	6
32	6	7
64	7	8
128	8	9

TABLE 2
Check Bit Parity Matrix

Check Bits	Data Bits															Parity	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14		15
C1	X	X	X		X		X		X		X		X		X		Odd
C2	X			X	X			X		X	X			X		X	Even
C3		X				X	X	X				X	X	X			Odd
C4			X	X	X	X	X	X							X	X	Even
C5									X	X	X	X	X	X	X	X	Odd
CD	X	X	X	X		X			X	X		X		X		X	Odd

which work from a parity matrix of various combinations of bits from the data field. Two sets of check bits are compared by the syndrome generator-detector; syndrome bits, when decoded, are the means of cor-

recting single-bit errors. Multiple-bit error signals are also derived from these syndrome bits.

Parity matrix (Table 2) generates an odd-parity sum for some bit combinations and an even-parity sum

for others; the sum in each case is one of the check bits. This odd-even mixture, which contrasts with the all-odd or sometimes all-even parities of most Hamming codes and their variants, detects catastrophic failures that manifest themselves as all 0s or all 1s—combinations that cannot occur in normal operation or as the result of failures that produce single or double errors. As the table shows, no two check bits are derived from the same set of data bits, and no two data bits contribute in the same way to all check bits. This is the characteristic that identifies each combination of parity errors.

Finally, check bit CD is generated from a selection of bits that make it equivalent to a parity sum of all bits, one of the relations in the classic Hamming code. Its value, in addition, is a parity sum of the other five check bits, and it is equivalent also to the parity sum of parities (not shown) of individual 8-bit bytes.

When check bits are stored alongside corresponding data bits in memory, they satisfy the requirement imposed by information theory that for single-error correction the minimum "Hamming distance" (minimum number of differing bits in any two error-free words) is 3. This is equivalent to each data bit's contribution to two parity sums. Since in fact each data bit contributes to three sums, the minimum Hamming distance is 4, permitting double-error detection as well as single-error correction.

During memory access, new check bits are generated from the fetched data. The new C1 through C5 check

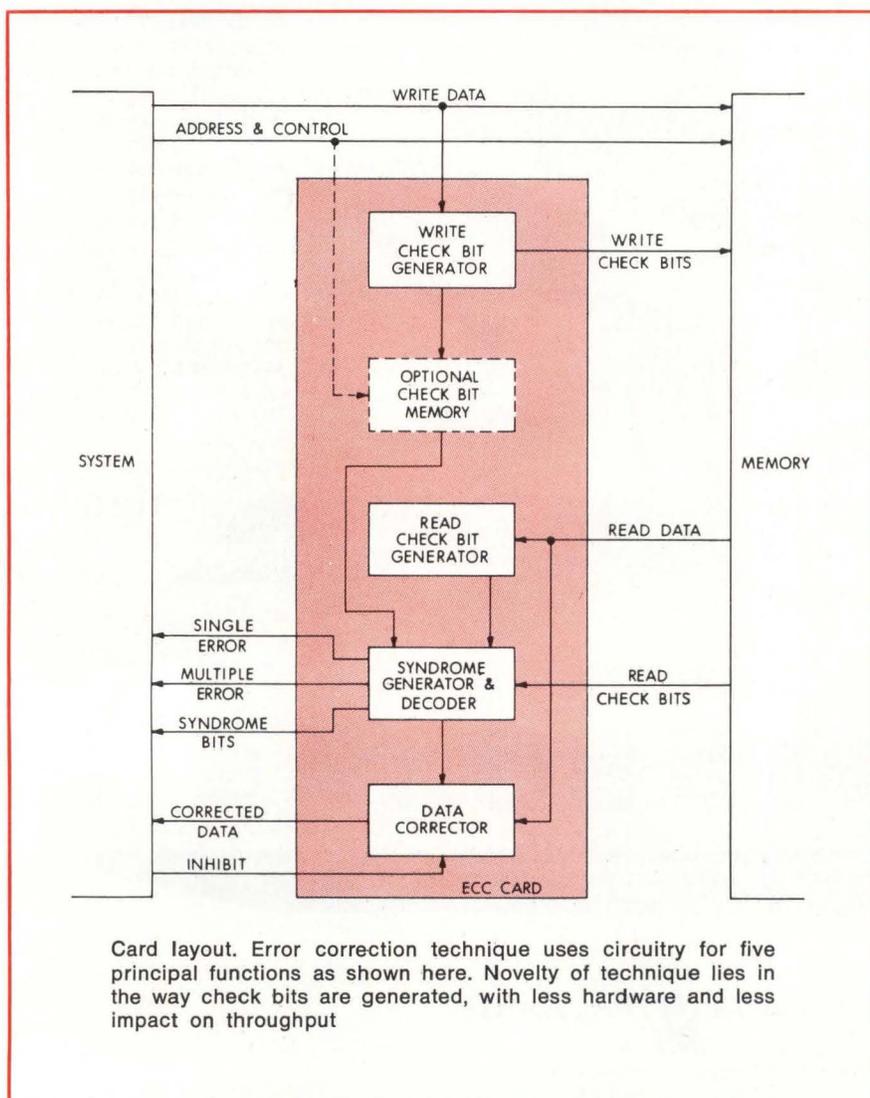


TABLE 3
Syndrome Bit Decoding

		S1-S2-S3							
S5	S4	000	100	010	110	001	101	011	111
0	0	CD	C1	C2	0	C3	1		
0	1	C4	2	3	4	5	6	7	
1	0	C5	8	9	10	11	12	13	
1	1	14	15						

bits are individually compared with the stored check bits that were fetched from memory. When fetched data or check bits contain an error, specific old and new check bits differ; the comparison produces five syndrome bits (Table 3). Each syndrome bit is 0 if the respective old and new check bits are equal, and 1 if they are different.

Of the five syndrome bits, three (S1, S2, and S3) represent bit posi-

tions in error within a byte. Syndromes S4 and S5 decode to give byte positions in error. For example, if the pattern for S1, S2, S3 were 1, 1, 0 and 0, 0 for S5, S4, the intersection in the decode table would identify data bit 0 as in error. Likewise, if S5, S4 were 0, 1 for the same pattern in S1, S2, S3, the intersection identifies data bit 4 as erroneous.

A sixth syndrome bit, SD, is the parity sum of three other parities: even parity on the stored check bits, plus two odd parities on the fetched data considered as two bytes. If the parity sum is odd, SD is 1; if even, SD is 0.

These six syndrome bits can detect single and multiple errors according to a simple rule: If SD = 1, in general, a single error has occurred; the other five syndrome bits, in conjunction with Table 3, identify the bit in error, and correcting it involves merely inverting the bit. However, occasionally the five syndrome bits will indicate a blank position in the table; if this happens, and SD = 1, an odd number

of errors is in the word, but the bits can be neither identified nor, therefore, corrected. Meanwhile, any combination of syndrome bits, regardless of what they indicate in the table, coming up when SD = 0, indicates an uncorrectable double or other even error.

This error correction system is implemented in the Micromemory 7703, a 32,768-word plug-compatible memory for the Nova 1200 computer. In addition to the ECC (error-correcting code), light emitting diodes (LEDs) on the card indicate the single- or multiple-bit error status. These same signals together with a manual switch form an error-stop feature; if any error occurs with the error-stop switch on, the memory halts while LEDs on the card indicate three high-order address bits and five syndrome bits. These identify the bit and row of the memory array, so that the defective memory chip can be readily located. A second switch on the card turns off the correction system manually—for example, if a diagnostic routine is to be run. □

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The Microprocessor Development System for the 8080, 2650, and 6800.

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And, it's universally accepted. It's so well accepted that design engineers call it a hardware development aid. It's so powerful, application programmers call it a complete software development system. And project managers? They know it as a great time and money saver and don't worry about what it's called.

Can the project manager be right?

The ability to interface with the different microprocessors of today and the new microprocessors of the future is the key benefit of Universal One. Universal One will never be obsolete and therefore provides the greatest *Return On Investment* of any microprocessor development system available today.

The universality of the system is based on Universal One's innovative multiple CPU architecture. One CPU, the Master CPU, is the controlling element of the system and executes all application *independent* functions; file management, text editing, system utilities, system I/O and software debugging.

The second CPU, the slave, which is controlled by the master, executes those functions that are application *dependent*; the microprocessor Assembler, in-circuit testing, user application programs, and user I/O. Additional microprocessor slaves are readily added by interfacing the new slave to the system bus and integrating it into the system software.

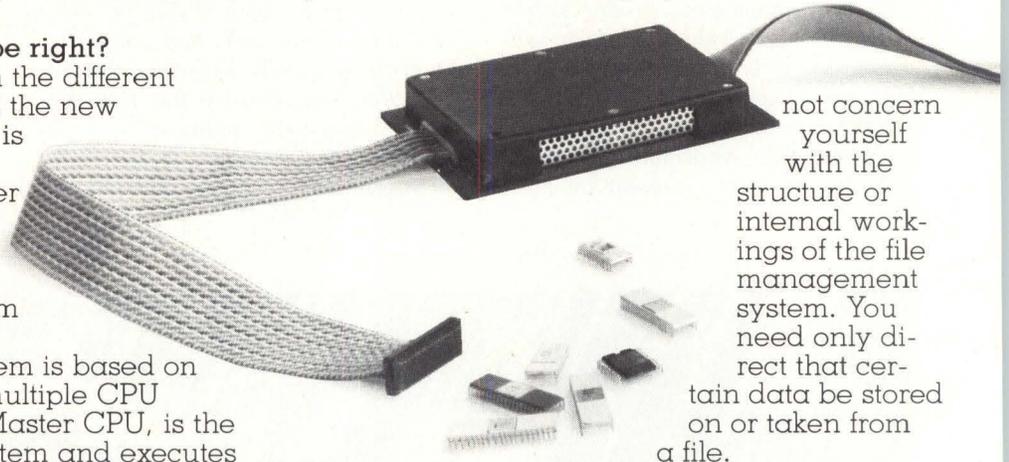
By meeting all the staff's needs, Universal One cuts costs. It's not necessary to have special test fixtures for design engineers and software development systems for programmers. Universal One saves on personnel training expenses since only one system interface need be learned.

Can the programmer be right?

Universal One's software capabilities rival those found on many powerful minicomputer systems. Universal Disk Operating System (UDOS) was developed specifically for and tailored to the multiple CPU architecture. The

operating system is executed by the Master CPU in its own totally protected Master memory to prevent disruptions by application programs.

UDOS is floppy disk file oriented. The system was designed specifically for the characteristics and peculiarities of a floppy disk and as such makes maximum use of its benefits. Many file management functions, normally required to be performed by the user, are performed automatically by UDOS. You need



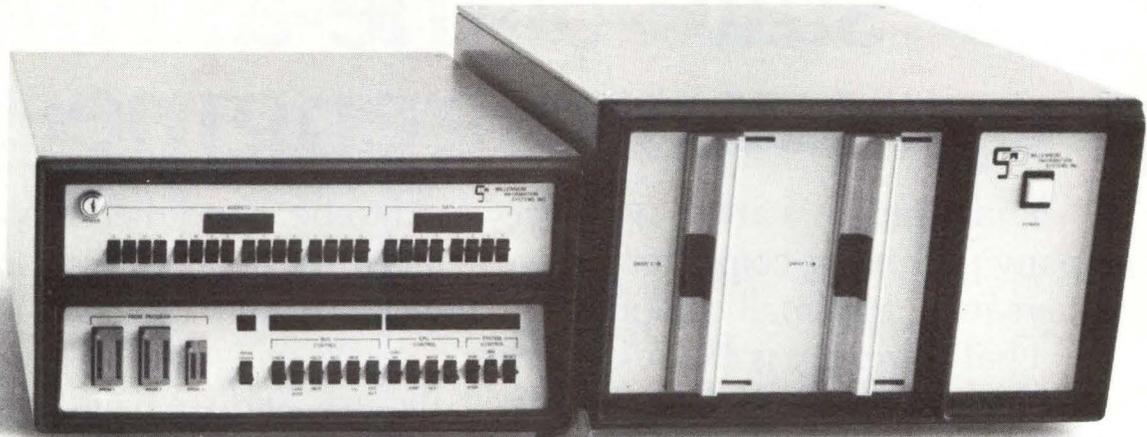
not concern yourself with the structure or internal workings of the file management system. You need only direct that certain data be stored on or taken from a file.

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Universal One contains a powerful text editor which is file oriented and has macro and iteration capabilities for combining commands.

Millennium provides comprehensive diagnostics which not only test the system's processors, memory & I/O but also check peripheral devices and interrupt logic.



Can the design engineer be right?

Universal One provides two modes of development system emulation for saving time during initial hardware debug and during hardware/software integration. In the first mode, Universal One emulates the prototype's microprocessor and its memory, while I/O functions are controlled by the user hardware. In the second mode, the prototype uses its own memory and I/O. Universal One's two-stage emulation eases the transition from initial test to full prototype implementation.

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Universal One's powerful operating system is easy to use so personnel get the most out of it whether they are inexperienced or advanced programmers. μ BASIC saves vast amounts of software development and maintenance time.

Last but not least, development system emulation simplifies hardware and software integration. Put it all together, it's the Universal One for 8080s, 2650s, *6800s, application programmers and design engineers.

* Available January, 1977

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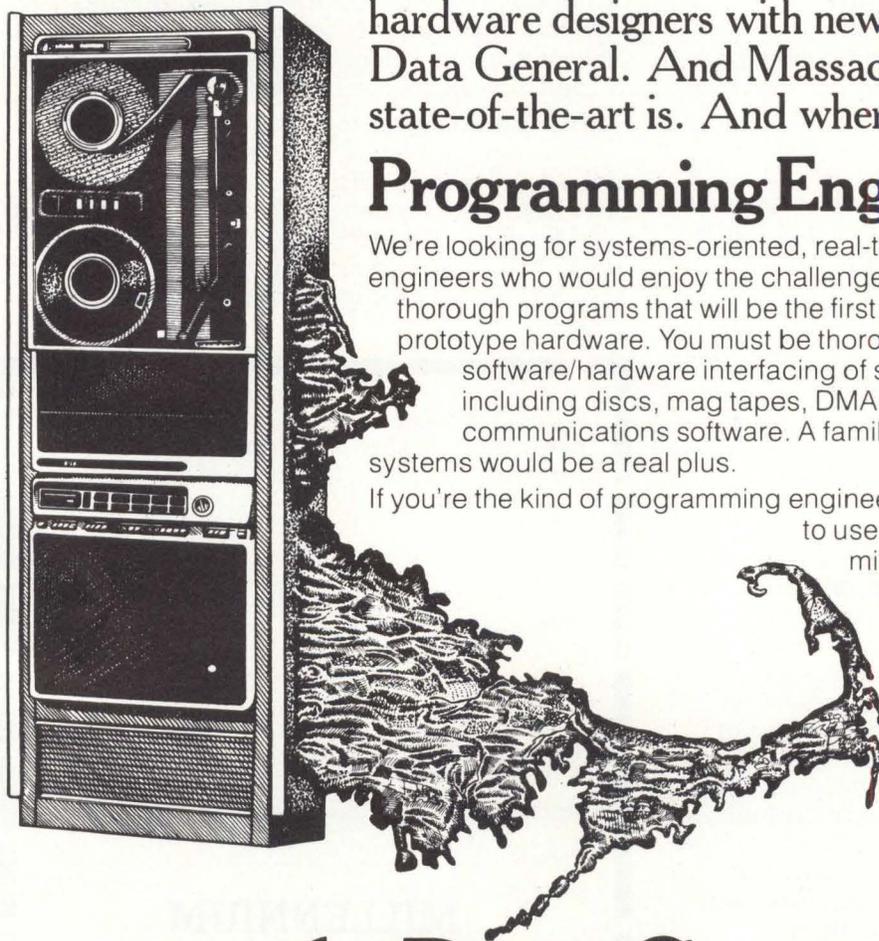
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Microcomputer Interfacing: A Software UART

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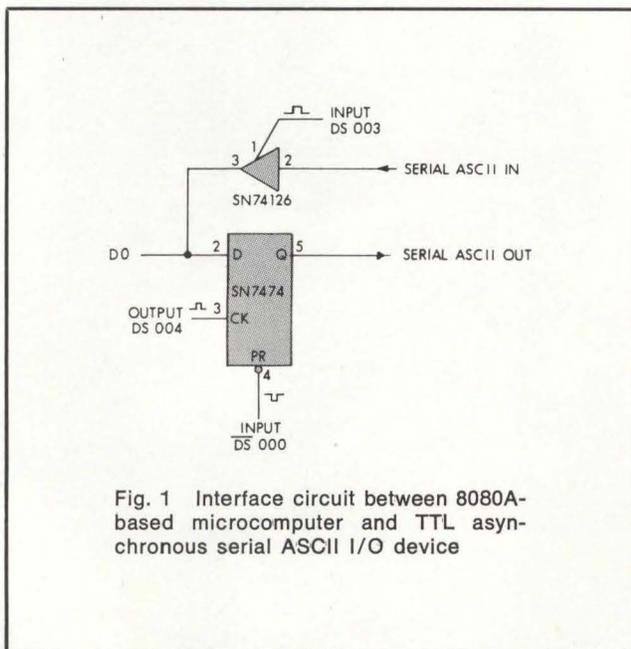


Fig. 1 Interface circuit between 8080A-based microcomputer and TTL asynchronous serial ASCII I/O device

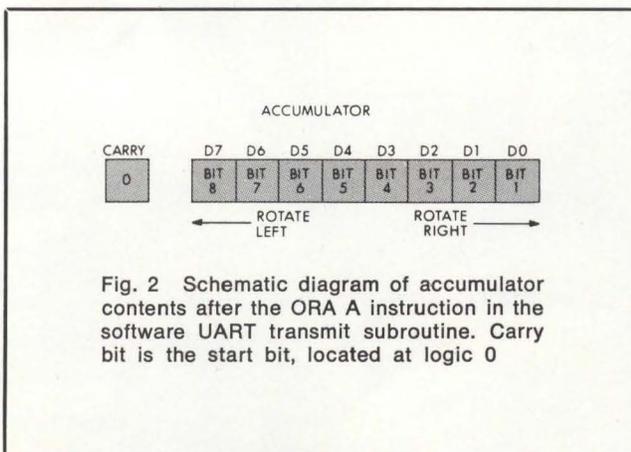


Fig. 2 Schematic diagram of accumulator contents after the ORA A instruction in the software UART transmit subroutine. Carry bit is the start bit, located at logic 0

This month, we return to the subject of the substitution of software for hardware, ie, the substitution of machine-level routines and subroutines for specific digital hardware devices that store, manipulate, transmit, or receive digital information (first discussed in *Computer Design*, July 1976, pp 120-121). The hardware device discussed here is the universal asynchronous receiver/transmitter (UART), a 40-pin integrated circuit (IC) chip that contains an independent 8-bit asynchronous receiver and independent 8-bit asynchronous transmitter. Data rates range from dc to 60K bits/s. Receiver and transmitter sections of the chip can be programmed for five, six, seven, or eight data bits, one or two stop bits, even or odd parity, and parity or no parity. The chip also contains a variety of flags. For further details, refer to manufacturer's literature or to Refs. 1 through 3.

An interface circuit for a simplified software UART is shown in Fig. 1. Owing to the nature of the specific application, there was no need for special flag bits or error checking. As a consequence, the interface circuit consists of a single 3-state input buffer gate (SN74126), a single output data latch (SN7474), two input device-select pulses, and one output device-select pulse. With appropriate modifications of the device-select pulses, this circuit can be employed with almost any microprocessor chip. In our case, an 8080A-based microcomputer operating at 750 kHz was used. In combination with operating software, this generates and detects asynchronous serial ASCII-coded 5-V TTL data. For teleprinter operation, additional hardware is required to convert 5-V logic levels to 20-mA current loop operation.⁴

The subroutine (see Microcomputer Transmit Subroutine) for the software UART occupies 20 to 25 successive program steps in memory once the appropriate PUSH, POP, and RET instructions have been included. Also required is a 9.09-ms time delay subroutine, which corresponds to an asynchronous serial ASCII data transmission rate of 110 baud, ie, teleprinter speed.

In the subroutine, register L is used as the bit counter for the 11-bit ASCII word, and is set initially to octal 013. Seven data bits plus the parity bit (bit 8) are assumed to be present in the accumulator. At LO = 146, the accumulator is ored with itself to clear the

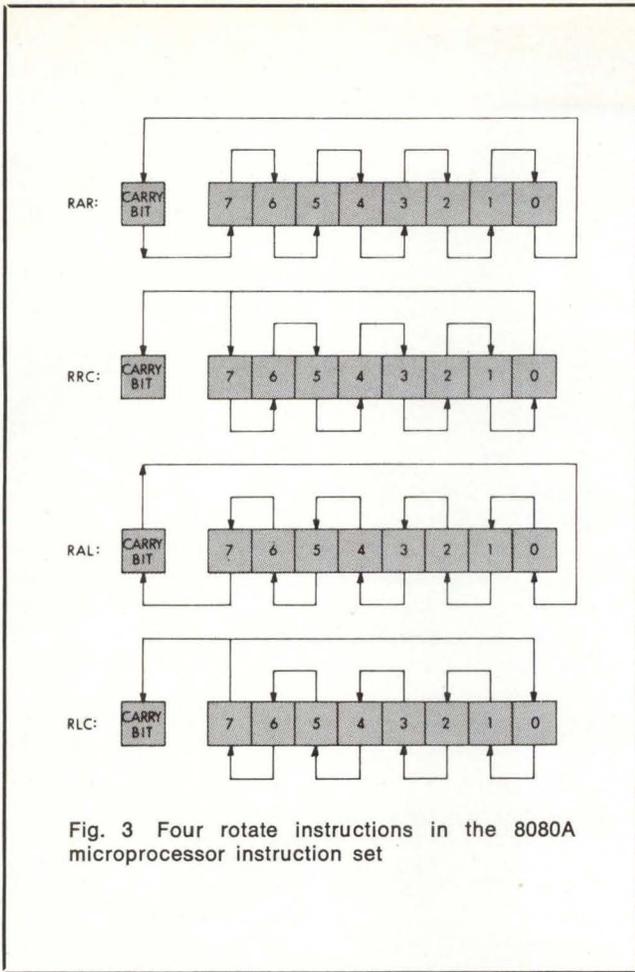


Fig. 3 Four rotate instructions in the 8080A microprocessor instruction set

carry bit, shown on the far left in Fig. 2. Least significant data bit in Fig. 2 is bit 1. At address LO = 147, a RAL instruction is performed to rotate the start bit to bit position D0 in the accumulator. Fig. 3 shows four different rotate instructions in the 8080A microprocessor instruction set.⁵ At LO = 150, the start bit is output to the SN7474 data latch (shown in Fig. 1). The program then goes into a 9.09-ms time delay subroutine, after which bit 1 is rotated into the D0 accumulator position and the carry bit is set to logic 1. Bit 1 is output to the data latch, ASCII word bit counter in register L is decremented, and program control is

returned to the time delay subroutine, which is called at LO = 152. The loop from LO = 152 to LO = 164 is executed a total of 11 times, after which register L becomes zero and the JNZ instruction at LO = 162 is ignored.

A software UART transmit subroutine possesses a flexibility equivalent to the original 40-pin UART chip. With appropriate modifications to the program or original accumulator data, five, six, seven, or eight data bits, one or two stop bits, even or odd parity, and parity or no parity can be transmitted. Modification of the time delay subroutine permits transmission at data rates from 60 to 9600 baud for a 750-kHz clock rate, and higher for 2- and 4-MHz 8080A clock rates.

Conversion from one data transmission rate to another is accomplished easily with the aid of appropriate software time delay subroutines, replacing RC (resistance-capacitance) time-constant circuits. An additional advantage that accrues from using software is the potential to perform code conversions. For example, 5-level Baudot keyboard send-receive machines are in widespread use and can still be obtained for under \$50. It is not too difficult to develop software that converts ASCII to Baudot and thus produce an inexpensive hard-copy terminal for the laboratory scientist or engineer, ham, or computer buff.

Since the software UART receive subroutine requires 50 instructions, it will not be repeated here.⁶ Basic programming concepts associated with the receive subroutine are illustrated in Fig. 4, which represents an 11-bit asynchronous serial ASCII word that is being detected by the 8080A-based microcomputer with the aid of the 3-state buffer gate shown in Fig. 1. The program repeatedly tests the "serial ASCII in" line in Fig. 1 for a logic 0 state, which corresponds to a start bit. Once that state is detected, the program goes into a 4.54-ms wait loop. Upon leaving the wait loop, the program again inputs logic 0 into bit position D0 in the accumulator, thus testing the validity of the start bit. The start bit is rotated to the carry bit, and the program then enters a 9.09-ms wait loop, after which it inputs bit 1 into position D0 in the accumulator. Register H is used as the SAVE register, which stores the growing ASCII data word. This register is rotated one position, and the 9.09-ms wait loop is again entered, after which bit 2 (a logic 0 in Fig. 4) is input into bit position D0 in the accumulator. Input of successive data and parity bits continues until the entire 8-bit data word is entered into the SAVE register. Two stop bits are also detected. With appropriate modifications, the program can detect parity or framing errors or an

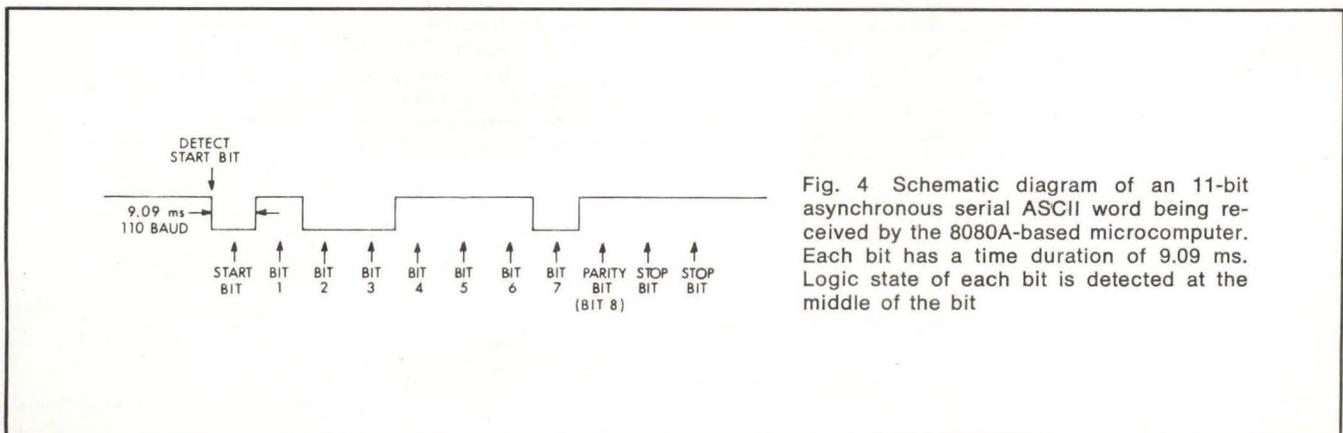


Fig. 4 Schematic diagram of an 11-bit asynchronous serial ASCII word being received by the 8080A-based microcomputer. Each bit has a time duration of 9.09 ms. Logic state of each bit is detected at the middle of the bit

Microcomputer Transmit Subroutine

LO Memory Address	Instruction Byte	Mnemonic	Description
•	•	•	
•	•	•	
			Accumulator contains 8-bit ASCII word. Bit 8 is the parity bit, which can be set for even or odd parity, or no parity
144	056	MVI L	Set ASCII word bit counter to 013
145	013	013	
146	267	ORA A	Set carry bit to logic 0
147	027	RAL	Rotate carry bit to D0 in accumulator
150	323	OUT	Output carry bit to SN7474 latch
151	004	004	
152	315	CALL	Call 9.09-ms time delay subroutine
153	<B2>	<B2>	LO address byte of time delay subroutine
154	<B3>	<B3>	HI address byte of time delay subroutine
155	037	RAR	Rotate bit in ASCII word to D0 in accumulator
156	067	STC	Set carry bit to logic 1
157	323	OUT	Output bit to SN7474 latch
160	004	004	
161	055	DCR L	Decrement bit counter by 1
162	302	JNZ	If bit counter has a value of zero, ignore this instruction. If all bits in the 11-bit ASCII word have not been transmitted, jump to address LO = 152
163	152	152	LO address byte
164	<B3>	<B3>	HI address byte
•			
•			
•			
•			At this point, the 8-bit ASCII word contained in the accumulator has been transmitted. Two stop bits have been added at the end of the eight bits and a single start bit, at logic 0, has been added at the beginning of the eight bits

overflow condition. With the aid of a second SN7474 latch, a data ready flag signal also can be generated from software.

The preceding software UART routines were used in a "smart" remote data entry station that was tied via a 20-mA current loop to a PDP-8/L minicomputer in a physical chemistry laboratory. The data entry station intercepted the 20-mA current loop tied to the minicomputer; the remote data entry station permitted students to load data into memory and transmit them as a block to the minicomputer, which analyzed them and provided a printout. With the aid of the 20-mA current loop operated in full-duplex mode, 10 or more remote data entry stations could be tied to the minicomputer.

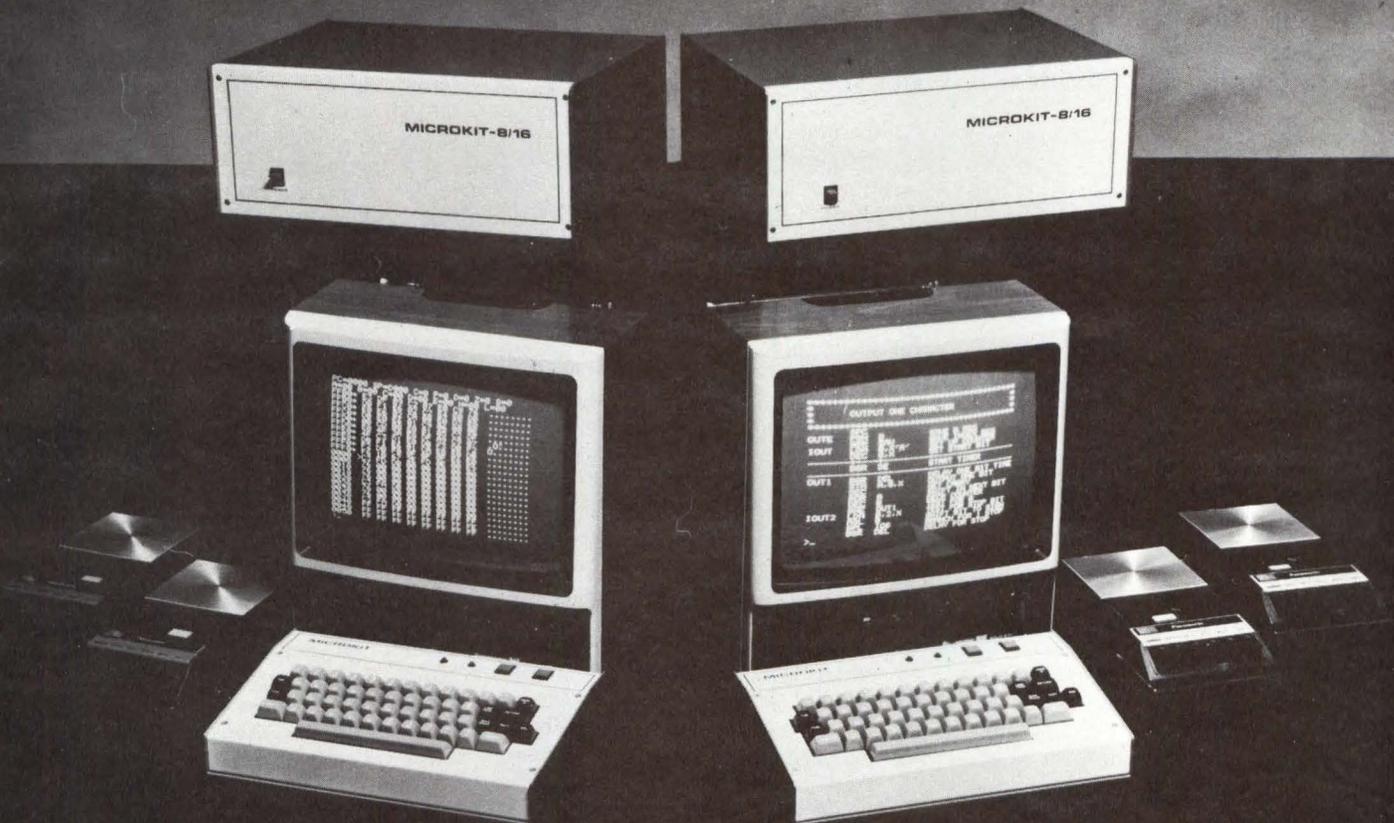
Software-hardware trade-offs that can be accomplished using microcomputers are important. Similar, and perhaps more comprehensive, routines have already been written for all of the popular microprocessor chips, such as the 16-bit PACE or 8-bit 6800. As microcomputers become faster and less expensive, it is more likely that all moderate speed digital functions will be executed via software.

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4. P. R. Rony, D. G. Larsen, and J. A. Titus, "Computer interfacing: Half duplex and full duplex current loops," *American Laboratory*, June 1975, p 78
5. *Bugbook III, Microcomputer Interfacing Experiments Using the Mark 80[®] Microcomputer, an 8080 System*, E & L Instrument, Inc, Derby, Conn, 1975
6. Copies of the transmit and receive subroutines and a description of the smart data entry station are available from Professor Paul Field, Dept of Chemistry, VPI & SU, Blacksburg, VA 24061

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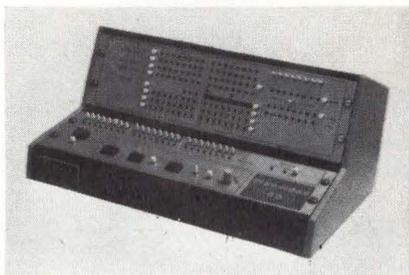
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Designed as a training computer to teach principles of microprocessors and programming, Picodidac 80 allows analysis and display of the CPU with registers, flags, program counter, and stack pointer, and permits visualization of elements such as memory, inputs, and outputs. This enables debugging of various instruction structures, addressing modes, and interrupts.

As a teaching computer, it starts with an introduction to information processing and proceeds to practical applications by means of sequential reasoning. Besides this didactic application, the computer can be used for other purposes simply by disconnecting its Promdidac memory board. Provisions have been made for peripheral interfaces.

Introduced by Laboratoires d'Electronique et d'Automatique du Nord, 236, rue Sadi Carnot, 59320 Haubourdin, France, the microcomputer contains an 8080 microprocessor CPU with clock, bus amplifier, RAM, and p/ROM, which are all pluggable boards. The console, providing LED binary displays and switches, is controlled by the program contained in the memory board.

The system has several working modes: "memory dialogue" shows writing and reading in RAM, and readings in p/ROM; "instruction for console" allows execution of each instruction programmed on the switches; and "instruction from memory" allows step-by-step or automatic execution of program instructions previously entered in RAM or p/ROM through switches or peripheral equipment. Therefore, 78 instructions of the microprocessor can be executed; if an incorrect instruction is programmed, the computer refuses it, signaling the error.

Circle 170 on Inquiry Card

Cross-Assemblers For Microprocessors Decrease Time and Cost

Cross-assemblers for one microprocessor that run on another's development system have been released by The Boston Systems Office, Inc, 400-1 Totten Pond Rd, Waltham, MA 02154. Written in assembly language, the assemblers require 8K bytes of memory and have full macro and conditional capabilities. According to the company, the assemblers offer increased savings in both time and cost, and require less space, compared to other manufacturer distributed cross-assemblers.

Requiring no temporary files, the 2-pass assemblers are made specifically for the host machine; they can simply be loaded and run without making changes. Also, naming of files is not restricted; once the cross-assembler is running, the user tells it whatever names have been chosen for the files. Offered on national time-sharing, assemblers are currently available for Intel 8080, 8008, 4040, 4004; Motorola M6800; MOS Technology 6500 series; Fairchild F-8; National Semiconductor PACE; Rockwell PPS/4, PPS/8; Texas Instruments 9900; TMS 1000 series; and all compatible devices. These assemblers are running on DECsystem 10 and 20, PDP-11, Novas, IBM 370, and other computers.

Circle 171 on Inquiry Card

40-Pin, Single Chip Microcontroller Adapts Easily to Applications

WD/40, a single chip microcontroller for dedicated computing and control applications, is a standalone 40-pin device requiring few or no support circuits. It contains its own register file, mask programmable control ROM, output PLA, internal oscillator, and power-up clear circuitry. The chip requires only a single power supply and is directly TTL compatible.

To ease writing and checking out of programs, an editor, assembler, and simulator are also available from Western Digital Corp, 3128 Red Hill Ave, PO Box 2180, Newport Beach, CA 92663. The chip comes in a 64-pin package with internal con-

trol ROM inputs and outputs available on the outside for direct connection to p/ROMs. A development board containing the 64-pin chip and p/ROMs is also available.

Capable of directly addressing up to 64 signals for input information, the chip also has two programmable interrupts and one wait input. Scanned output and 16 static outputs can drive an 8-digit numeric display.

Its instruction set is applications rather than computer oriented; instruction format is register-to-register rather than RAM-accumulator, making it easy to learn and apply. Multiple-digit arithmetic operations such as adds and subtracts are programmed at the instruction level, not by subroutine. A program ROM of 4K bits and one level of subroutine are provided. Internal register file storage (exclusive of output registers) is 128 bits (32 digits).

Using the customer's flowchart and the chip simulator, the company will write the necessary program and generate the custom mask. Cost of the programming mask is \$1500, which includes 10 chips for customer evaluation, plus the opportunity to change the mask two times. In quantities of 1K and up, the chip sells for \$8.95.

Circle 172 on Inquiry Card

Evaluator Eases Microprocessor System Development

The M68USE User System Evaluator (U.S.E.), compatible with the EXORCISER™, consists of an M6800 processor module, intercept module, and cable and buffer assembly, and permits externally constructed M6800 microprocessor systems to be connected to the EXORCISER. System evaluation can be accomplished through diagnostic and control features of the EXbug firmware and system analyzer. At the production level, the system can be employed to test finished M6800 microprocessor systems.

An EXORCISER/U.S.E. system from Motorola Semiconductor Products, Inc, PO Box 20294, Phoenix, AZ 85036 has a single, shared processor architecture; U.S.E. processor module therefore replaces the original MPU module in an EXORCISER. Interface between the EXORCISER and external system can be changed anytime; modular options of the EXORCISER, such as memory and I/O, can be incorporated into the external system during emulation, allowing comparative evaluation between the EXORCISER functions used for emulation and resultant functions developed

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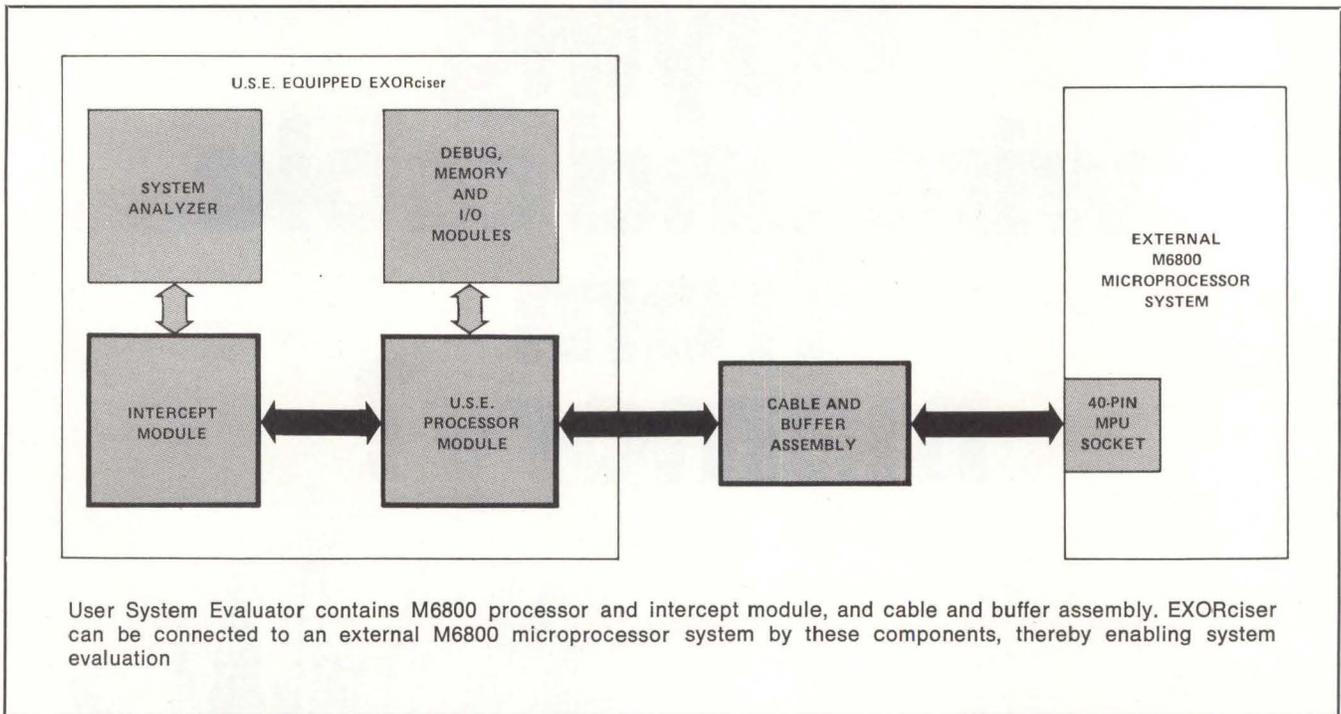
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in the external system. A prototype residing in-chassis can be tested and transferred, section by section, from the EXORciser to the external system.

Cable and buffer assembly connects the processor module to the

external system; the assembly terminates in a 40-pin, DIP connector that plugs into the external MPU socket. This is the I/O port through which EXORciser functions are extended to the external system and through

which the MPU inputs are monitored. An intercept module connects a system analyzer to the U.S.E. processor module; analyzer functions can be extended via the 40-pin I/O port. Circle 173 on Inquiry Card

Bus-Oriented Backplane Allows System Adaption To Many Applications

Key to the application flexibility of this microprocessing system is its printed circuit, bus-oriented backplane. Omnibyte Corp, 900 Jorie Blvd, Oak Brook, IL 60521 has designed individual $4\frac{1}{2} \times 6\frac{1}{2}$ " cards to uniformly interface with the backplane. I/O data are accessed from the front of the cards through mass-terminated ribbon cables and connectors, thus eliminating time-consuming, custom interconnections on the backplane. The bin is left unmodified for any configuration of memory and I/O interface boards. Both analog and digital I/O boards are accommodated in the same bin.

Viewed alternately as a micro-computer containing I/O electronics or as an intelligent I/O system that includes a microprocessor and its associated memory, the system is

housed in a rugged 16-slot card cage interconnected by the backplane which requires no custom wiring.



Versatile microprocessing system features bus-oriented backplane, with $4\frac{1}{2} \times 6\frac{1}{2}$ " cards designed for uniform interfacing. Six individual cards are crate controller (top left), CPU board (top right), 4K ROM/2K RAM (center left), PIA board (center right), ACIA board (bottom left), and Kluge card (bottom right). Omnibin and power supply are also available (top)

Fourteen of the 16 slots will accept any combination of RAM, ROM, or I/O cards, providing system configuration to individual needs. Two remaining slots contain the CPU and multifunction controller card.

The system is designed around the Motorola M6800, an 8-bit, n-channel microprocessor capable of addressing 64K bytes of memory with its 16-bit address bus. Each memory card contains a 4-bit address comparator to provide switch-selectable location of 4K blocks of memory. The controller card allocates one selectable 4K memory to the I/O modules. System modularity requires changing only the CPU card to accommodate a different processor.

Available memory and I/O cards include a 4K p/ROM/2K RAM card; an ACIA providing RS-232-C, 20-mA current loop, and TTL serial output; a parallel output card with eight bytes of programmable I/O and 16 control lines; a dual 12-bit DAC

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- 960 Upper Case Character Display
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- 32 Positive Action Switches
- 11 Selectable Baud Rates†
 (from 75 to 19,200)
- 1 RS232S Interface
- 1 20mA Current-loop
- 1 Hatchback Bonnet

†No official minimum requirements have yet been established.

NET WEIGHT: 25 lbs
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*DCA means Direct Cursor Addressing. And that's exactly what you'll find added to each and every ADM-3A Dumb Terminal from Lear Siegler. As a basic, standard ingredient.

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CIRCLE 55 ON INQUIRY CARD

card; and a "Kluge" card that interfaces to the backplane, leaving the rest of the card for solder or wirewrapped custom circuitry. Power supplies also are available.
 Circle 174 on Inquiry Card

Low Cost Analyzer Tests and Debugs μ Processor Hardware/Software

Designed to test and debug software and hardware of any microprocessor system, model 50 is an address and data bus monitor with hardware breakpoint capability for microprocessors. Tester is usable with all microprocessor families having accessible address and data buses up to 16 bits wide each.

In many respects, the analyzer is functionally equivalent to a 32-channel logic analyzer, but has additional features. Search modes locate and identify the first and last instruction in a program loop; a transfer mode steps forward or backward through programs without setting addresses. Tester can be used as a passive real-time monitor or as an interactive breakpoint generator. Other features include versatile delay modes and after halt stepping capabilities, dual clock provision, $N + 1/N - 1$ strobe, and status indicators.

Up to four units may be interconnected for wider display, complex triggering, or higher speed. Introduced by Systron-Donner Corp, Concord Instrument Div, 10 Systron Dr, Concord, CA 94518, the basic model operates at up to 4-MHz clock or instruction cycle rates and up to eight machine cycles per instruction.
 Circle 175 on Inquiry Card

Microprogramming Language Available Via Time-Sharing Network

A general-purpose microprogramming language called DAPL is now available on time-sharing. Testing and acceptance by various 4-bit slice manufacturers has been completed, and DAPL is now accessible via the nationwide toll-free network of Remote Computing Corp, 1 Wilshire Building,

Suite 1400, Los Angeles, CA 90017. Currently supporting the AMD2900 and Fairchild 9400, the product will soon cover the Motorola 10800 and MMI 6700.

DAPL allows the microprogrammer to select any of four levels to provide a convenient symbolic representation of microprograms. Macros and symbolic values are allowed at all levels. At level 0, microinstructions are formed by sequences of symbolic names, binary, octal, decimal, and hexadecimal numbers. At level 1 they are formed as a series of fields, with each field being sequentially assigned a value as in level 0. Additionally, label tables are allowed for mapping ROMs and PLAs. Level 2 extends the microinstruction field definition to include symbolic names and default values. Finally, level 3 allows microprograms to be expressed in register transfer notation.

Microprograms from 8192 words x 256 bits are allowed. Free form input with comments arbitrarily interspersed for documentation is featured, along with an interlist command that lists the generated microcode directly beneath the associated macroinstruction. A complete variable cross-reference listing with extensive error detection and debugging aids is available. Both hexadecimal or binary object file formats are offered.
 Circle 176 on Inquiry Card

Microprogram Controller Operates with Bit Slices and Arithmetic Devices

Designed to be used in conjunction with conventional bit slices, such as the AMD 2901, Intel 3002, and the company's 6701, and with TTL MSI arithmetic devices, such as the TI 74S181 ALU, the Schottky TTL microprogram controller can also be used as the central control in any nonarithmetic system built with TTL. Announced by Monolithic Memories, Inc, 1165 E Arques Ave, Sunnyvale, CA 94086, the 57110/67110's high speed, 30-ns propagation delay and flexibility allow it to be used in minicomputer emulation and for high speed controllers for discs, tapes, printers, and CRTs.

Controller consists of a microprogram sequencer capable of addressing 512-word pages of memory, and

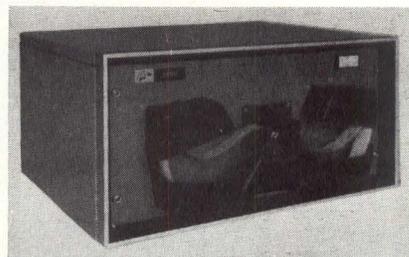
a loop counter used for repeating loops of microcode, both with subroutine capability; all branch logic required in a bit slice system including flag storage; and shifting logic connections to provide shifting options for bit slices. The controller addresses the system control memory holding the microcode.

Eight instructions allow classical program store addressing such as continue, conditional and unconditional jumps, subroutine jumps, and subroutine return. One special feature, a subroutine jump, allows any piece of existing code to be used as a subroutine, enabling easy modification of code. Branching system, based on controlling the least significant address bit of the address register directly from the branch condition logic, allows 2-way branching at each clock period and 4-way branching with the on-chip loop counter. Counter can be preloaded to any value up to 31 and decremented; any section of code can be repeated up to 32 times for iterative procedures such as multiplication, division, and square root.

Easy-to-use controller offers savings in system cost, PC board area, and power. It is packaged in a 40-pin DIP, uses a single 5-V power supply, and is available in both commercial and military temperature range versions. Product support will include a microassembler.
 Circle 177 on Inquiry Card

Low Cost Paper Tape System Offers Floppy Disc Performance

Total system design of the μ PAL 2650 is aimed at providing the user with the convenience and throughput of floppy disc storage at the cost of paper tape hardware. Software/hardware development system pres-



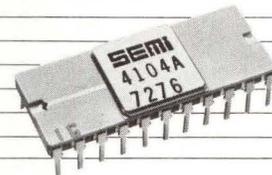
The μ PAL 2650 hardware/software development system containing a 2650 microprocessor, parallel I/O interface card, and 8K bytes of RAM furnishes floppy disc performance at the cost of paper tape hardware

MEMORY AT WORK

Retail Sales

The point of sale terminal is just one application where data integrity and ease of maintenance are vital. The SEMI 4104A static 4K RAM answers both problems perfectly. It is static; that means simpler, faster field maintenance. And just 15 mw will protect data. The 1K x 4 organization is ideal for small capacity systems, and the 200 nsec access (350 nsec cycle) time makes it fast enough for any 8080A class

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ently supports the 2650 microprocessor; in the future, Processor Applications Ltd, 2801 E Valley View Ave, West Covina, CA 91792 plans to include software to support other microprocessors.

Two factors that contribute to high performance are the coding efficiency of the microprocessor itself, which permits powerful monitors, text editors, assemblers, and other utility programs to reside in very small ROM memory spaces; and a software/hardware design that allows instant selection and application of these tools to development programs concurrently in RAM memory. Re-loading and punching of source tapes are therefore avoided.

Realistic program modules of up to 300 statements, including comments, can be assembled within 8K of memory. Software is structured so that cross-references between program modules are easily maintained.

Basic unit includes chassis, power supplies, high speed tape reader, CPU board, parallel I/O interface card, and 8K bytes of RAM. Software supplied includes the Monpal system monitor, the Fixit editor, and

the Micro assembler. Floppy disc-type performance is achieved when the last two are supplied in their optional ROM versions.

Monitor features logical assignment of physical devices, load and dump in binary or hexadecimal formats, memory and register examination, and breakpoint capability; p/ROM tapes may be prepared and verified in high- and low-"nibble," or full byte formats.

The character string editor's commands provide the user with complete control of text pointers and the ability to find, delete, change, or write any character string in the text buffer. Commands may be linked in any order to provide sophisticated page mode editing with a single command string.

With variable length symbols to reduce the need for comments, the assembler allows the use of externally defined symbols which streamline and simplify the use of segmented programming modules. Standard Signetics mnemonics and definitions (described in their assembler programming manual) are used. Circle 178 on Inquiry Card

Crash-Proof System Is Compatible With All Microprocessors

A dual-processor prototyping and development system for microprocessor applications, called TWIN (TestWare INstrument), offers a "crash-proof" development environment. Programs under development are completely separate from the operating system; errors made in the development process cannot alter system integrity or software already completed.

Operational functions are handled by one CPU (Signetics 2650 microprocessor) referred to as the "master." A second, or "slave," CPU is used for developing programs and interfacing prototype devices. Only the slave must match the user-selected microprocessor for "design-in" applications.

Software is available for using a 2650 microprocessor as the slave CPU, but the hardware architecture is independent of the microprocessor used as the slave. Signetics, 811 E Arques Ave, Sunnyvale, CA 94086 eventually expects to offer software for its

3000 bipolar series, and for other microprocessors.

Typical system consists of a development computer with dual p/ROM programmer, dual-drive floppy disc unit, operator console, and TWICE cable. TWICE (TestWare In-Circuit Emulator) supports the development, integration, and checkout of the user's software and hardware. A sophisticated cable arrangement emulates the user's hardware system in the development process. The microprocessor in the user's development prototype can be removed and the cable plugged directly into the same socket. Other end of the cable attaches to the TWIN system, enabling the TWIN slave CPU to function as the processor that the user will employ in the finished product.

System is provided with a full range of supporting software including a disc-based operating system, text editor, resident assembler, and extensive debugging and diagnostic capabilities. Ability to develop microprocessor programs is expanded by the dedicated CPU which stores and manipulates all associated user codes

and programs. The other CPU works strictly with the system resident operating commands and programs. Separation of company software from the user's developing system eliminates housekeeping required to distinguish user programs from internal operations.

The user can switch back and forth from independent software/hardware development modes to hardware/software in-circuit emulation modes. Programming language is symbolic assembler-type with syntax, typical of minicomputer languages. This language is generally accepted as easy to understand and work with. When software is fully debugged, the object code can be burned into a p/ROM using the TWIN system.

Two configurations are available: super—a fully configured microcomputer system, incorporates a CRT, printer, floppy disc unit, and the dual-CPU microcomputer; and basic—the same system without CRT or printer terminals. Basic units feature dual memory expandable from 16K to 64K bytes, 16-bit bus instruction, RS-232 and current-loop interfaces with a transmission rate of 110 to 1200 baud, TWICE cable, and all system software.

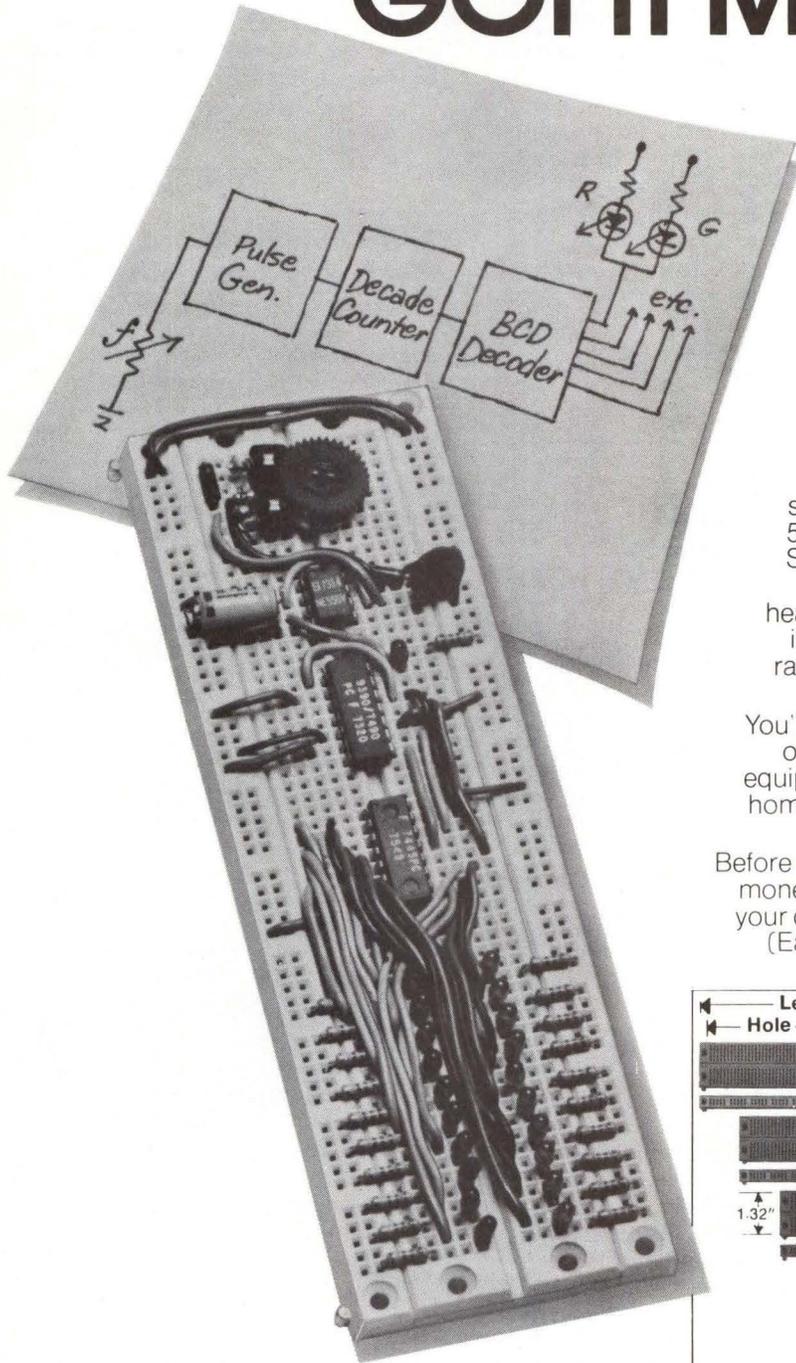
Circle 179 on Inquiry Card

Industrial Microcomputer Provides Alternative to Hardwired Systems

An industrial series for automatic test and instrumentation applications, Rigel II microcomputer series comprises a complete set of instrumentation modules centered around a microcomputer. Housed in a main-frame containing a standardized back-panel wiring bus and power supply, the modules interface directly with process control signals and provide a variety of control panel displays. No special computer interface circuits or panel designs are required.

Announced by Androtek Systems, a division of DMI, Inc, PO Box 29098, 5589 Westerville Rd, Columbus, OH 43229, the microcomputer module (model MC-1) contains an 8-bit parallel CPU with 45 instructions, seven registers including accumulator, and a 7-level subroutine return address stack. Memory has 256 words of RAM, plus sockets to accept up to fourteen 256-word p/ROM chips. Timing clock is a 24-bit binary counting clock with 5-ms resolution. Up to six lighted panel buttons are connected through the I/O

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	QT-59S	6.5"	6.2"	118	12.50
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	QT-47B	5.3"	5.0"	16	2.25
	QT-35S	4.1"	3.8"	70	8.50
	QT-35B	4.1"	3.8"	12	2.00
	QT-18S	2.4"	2.1"	36	4.75
	QT-12S	1.8"	1.5"	24	3.75
	QT-8S	1.4"	1.1"	16	3.25
	QT-7S	1.3"	1.0"	14	3.00

All QT units are .33" thick.

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Industrial microcomputer module is housed in a mainframe containing power supply. Various modules contained in the series are (left to right): micro-computer, memory, I/O, set point, display, A-D converter, frequency counter, and D-A converter

ports—one 8-line 24-V buffered input port, 10-mA load/line, and one 8-line 24-V buffered output port, 50-mA drive/line. Memory modules permit expansion of memory to a full 16K words in 4K-word blocks, by any combination of ROM and RAM modules.

Six standardized peripheral modules can interface digital signals with analog signals, which are accessed and controlled by the computer through the analog interfacing modules. I/O modules interface digital input and output signals for control of relays, switches, etc. Models 10-2 and 10-4 contain two input and two output ports, and four input and four output ports, respectively. Six lighted front panel buttons are connected through the I/O ports.

Setpoint modules provide panel inputs of numerical information. Front panel devices include one through four 5-digit thumbwheel switches including available polarity. Up to four 8-line I/O ports are optional.

Providing panel display of numerical information such as levels, counts, data, or conditions, digital display modules are continuous 7-segment gas discharge displays. The 0.5" high numerals are offered in 3½-, 4-, 5½-, and 6-digit configurations. Up to six lighted panel buttons are connected through the two input and two output ports (others available on request).

A-D converter module interfaces analog voltage signals for read-in of voltages, currents, etc. Six differential input channels each have zero and span control. Ranges are 20 V, 2 V, or 200 mV full scale; conversion time is 30 μ s.

Interfacing periodic time varying input signals, the frequency counter module has six differential input channels with threshold and hysteresis. Ranges are 1-s, 100-ms, 10-ms, and 1-ms gate times in frequency count mode; 100-kHz, 10-kHz, 1 kHz, and 100-Hz counting frequencies in period mode.

D-A converter modules output analog signals on up to six output channels with zero and span control for each. Range is from 0- to ± 5 -mA dc output signal with 10-V compliance; settling time is 10 μ s. Available accessories for the series include line isolation panels, mainframe interconnect kit, and rack-mounting conversion kit.

Circle 180 on Inquiry Card

Bipolar p/ROMs Offer Advantages Over MOS p/ROMs

Developed as an 8K/16K p/ROM board that is plug-compatible with Intel's Single Board Computer System (SBC 80/10), System Development Kit (SDK-80), and Intellec[®] Microcomputer Development System (MDS-800), board may contain up to 8K or 16K bytes of p/ROM/ROM depending on the p/ROM type used. Fusible link bipolar p/ROMs such as the 3604 may be used as well as light-erasable MOS p/ROMs such as 8704s and 8708s. Masked ROM equivalents of these p/ROMs may also be used.

Among several advantages over MOS p/ROMs, bipolar p/ROMs are faster, require only one 5-V power supply, and are lower in cost on a per bit basis. Switches and jumpers allow selection of p/ROM type and base address of the board. Switches are also used to alter the timing of acknowledge signals to correspond to the access time of each p/ROM type. A 3-terminal -5-V regulator is provided on the board so that the -10-V power supply in the MDS may optionally be used to provide -5 V for 8708 p/ROMs. All ICs on the board are socketed, and all edge connectors have gold fingers.

A reference manual with schematic and operation instructions is included. Board also is available from Micro-Tec, PO Box 337, Sunnyvale, CA 94088 with p/ROMs containing a self-

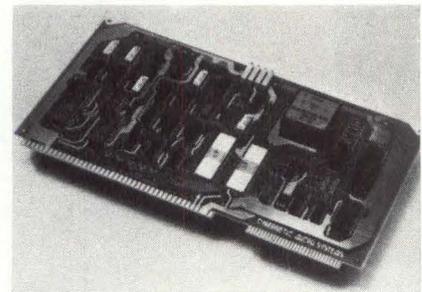
assembler for the Intel 8080 micro-processor and a line-oriented editor. Assembler, compatible with Intel's standard assembler, does not have a macro facility and allows only the operators plus, minus, multiply, and divide to be used in expressions. Editor allows assembler source lines to be inserted, replaced, or deleted.

Circle 181 on Inquiry Card

3-Way Single Board Controller Functions As System Console Device

Three functional modules are integrated on a single board in the peripheral controller—described as fully plug-compatible with Intel's SBC 80/10 (Single Board Computer) and Intellec[®] MDS (Microcomputer Development System). KDP/C (Keyboard-Display-Printer/Computing) board, measuring 6¾ x 12", handles an ASCII standard electronic keyboard, Victor Comptometer Corp printer, and onboard 4-function calculator. Board functions are controlled by the 8080 CPU of the host system.

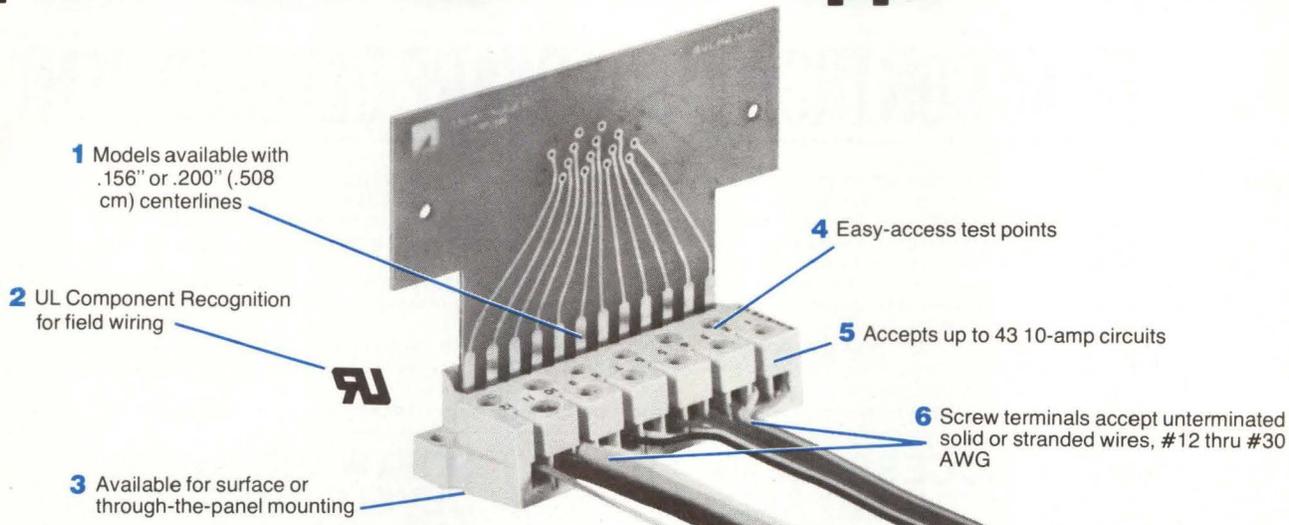
Introduced by Cybernetic Micro Systems, 2460 Embarcadero Way, Palo Alto, CA 94303, the onboard



KDP/C 3-way peripheral controller combines keyboard, display, printer, and calculator features on one 6¾ x 12" board

calculator performs four basic arithmetic functions to 12-digit accuracy. Display driver is compatible with a 7-segment, 12-digit plasma display. Additional calculator features include selectable stored constant multiplier/divisor; exchange; full floating input; floating intermediate; fixed selectable output decimal places (from 0 to 11), and a storage memory from

116 reasons why *only* Buchanan[®] PC Board Connectors provide **Lowest Total Applied Cost!**

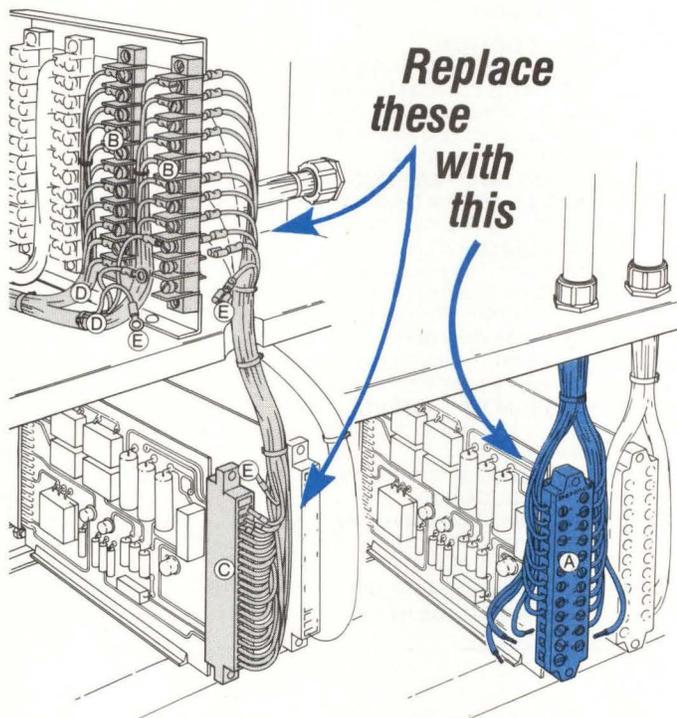


And here are 110 more—the 110 connections you eliminate!

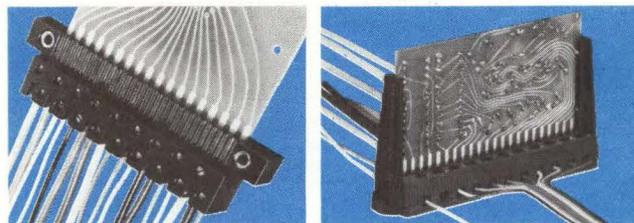
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 - Selecting the best-suited microprocessor
 - Developing software
 - Minimizing costs
 - Major pitfalls and how to avoid them
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 - Definitions of software, hardware and firmware
 - Basic software building blocks
 - 8080 program example: generating timing pulses
3. MICROCOMPUTER PROGRAMMING TECHNIQUES
 - Basic concepts
 - Decision making
 - Input/Output
 - Arithmetic
 - Data movement
4. SYSTEM ANALYSIS
 - Product definition guidelines
 - What to do in hardware, what to do in software
 - Example: A system for pattern recognition and analysis of analog waveforms
5. PROGRAM DESIGN
 - Computer languages: micro vs. machine vs. assembly vs. high level
 - Program design guidelines
6. PROGRAM IMPLEMENTATION
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 - Tradeoffs and case studies
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Two days

**Course 156 SOFTWARE/SYSTEM DEVELOPMENT: TOOLS
AND TECHNIQUES FOR MICROCOMPUTERS**
Two days

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which entries may be added or subtracted with 12-digit accuracy.

An ASCII keyboard interface allows the user to enter data into his system. Inputs are character-serial, bit-parallel, allowing the characters to be read using a simple input instruction and eliminating the need for a serial-to-parallel conversion scheme. Interface is compatible with any electronic keyboard having TTL-compatible data bits and strobe keyboard requirement, assuring maximum user flexibility.

When hard copies of any computation are required, the board interfaces directly with an IPM 130 dot-matrix printer, which prints at a rate of 110 char/s and a minimum of 90 lines of 34 characters each per minute. Printer's impact matrix mechanism offers multicopy printout; board contains a built-in standard 64-character ASCII, 5 x 7 dot-matrix font generator and all sensors and drivers for total printer control.

Circle 182 on Inquiry Card

Hobbyists Can Obtain High Performance, Low Cost Computer

The 400 system low cost, high performance hobby computer comprises a CPU, memory expansion board, I/O board, video graphics board, and floppy disc. Supported with extensive documentation and software, system can be obtained from Ohio Scientific Instruments, 11679 Hayden St, Hiram, OH 44234. Compatible prototyping board is provided for custom design; inexpensive wireless backplane board allows plug-in connection between all system boards.

Model 400 Super Board can be used as a powerful standalone computer or as a CPU in a large system. It will accept the 6502, 6512, or 6800 microprocessor, as well as 1024 words of RAM and 512 words of p/ROM. Featuring an ACIA terminal interface, it has provisions for 16 parallel I/O lines and full buffering for system expansion. Board itself is an 8 x 10" double-sided, solder-plated, plated through hole G-10 epoxy board. Complete with 60-page theory of operation and assembly manual, board costs \$29; it is also available with just micro-

processor, with full parts kit, or fully assembled and tested.

Memory expansion board (model 420) can be configured for 4K x 8 or 4K x 12 bits. It uses 2102 memories. Complete kit sells for \$119.

Model 430 I/O board is a complete analog and digital I/O subsystem which optimizes use of board space, buffers, decoders, and interconnections. High speed A-D input can be used over the full audio bandwidth. Two D-A converters and an unblank signal are provided for CRT graphics, X-Y plotters, and sound generation. Generalized serial communications system is designed for audio cassette, FSK, Baudot, or ASCII terminals.

Claimed to be the lowest cost television display, model 440 video graphics board requires no DMA—it uses its own on-board memory. Automatically refreshed picture requires no processor support. It operates in memory space yielding an effective baud rate of over 100K. Optional graphics with gray scale or color are available.

Each side of the 470 floppy disc stores a minimum of 256K bytes. With easy-to-use hardware and software, disc costs \$599.

Circle 183 on Inquiry Card

Microprocessor and Peripheral Circuits Expand Family Line

Addition of a microprocessor and four peripheral circuits to the TMS 9900 family will expand the applications spectrum of all 9900-series products. TMS 9980 is a MOS microprocessor packaged in a 40-pin DIP. As a 16-bit central processing unit, it executes the full 9900 instruction set including hardware multiply and divide. It features an 8-bit data bus and a 16-bit address bus, making it compatible with byte-oriented microprocessor memories. The flexible I/O system provides capability to do DMA, memory mapped I/O, or easy-to-use serial I/O port—the communications register unit (CRU). Six interrupts including a nonmaskable interrupt and reset will be available.

Oscillator and clock generator will be contained on-chip. Targeted to systems requiring smaller memory size

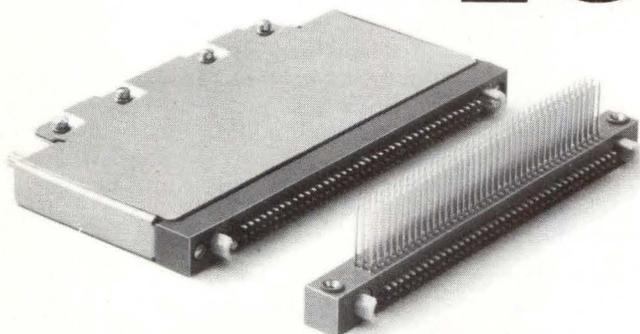
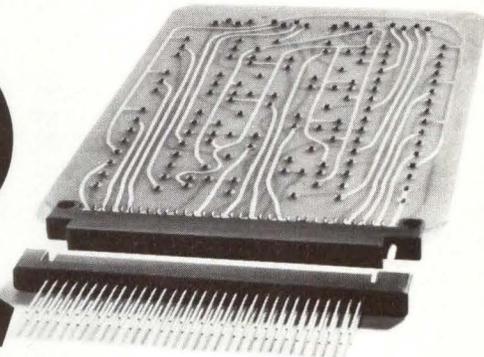
and less I/O, particularly where board space and chip count may be critical, the microprocessor also will compete head-on in the medium performance range with currently available 8-bit MPUs. The 4-phase clock generator and driver (9904) for the TMS 9900 is a low power Schottky design which provides driving by four MOS level clocks with a crystal-controlled input. Texas Instruments Inc, PO Box 5012, Dallas, TX 75222 has scheduled samples for the fourth quarter of 1976.

A programmable systems interface using n-MOS technology, 9901 can be used with 9900 or 9980 systems. It interfaces directly to the processor CRU port, and provides three functions—interrupt prioritization, I/O control, and interval timing. Under program control it can provide up to 15 individually maskable interrupt request lines, or up to 16 programmable I/O ports. With the device, one of the interrupt lines can be programmed as a wraparound interval timer with a resolution of 21 μ s to 699 ms. It is intended as a low cost general-purpose peripheral requiring a single TTL level clock and 5-V power supply; it will be available in a 40-pin DIP for sampling during the fourth quarter of 1976.

TMS 9902 is an n-MOS asynchronous communication controller (UART) which can take advantage of the CRU I/O port of the 9900 and 9980. Programmable features include data rates from 5 to 76,800 bits/s; character length from 5 to 8 bits; 1, 1.5, or 2 stop bits; and even or no parity. Also containing a wraparound interval timer with resolution from 64 to 16,384 μ s, it will be available for sampling in the fourth quarter in an 18-pin package, with a single TTL clock and 5-V power supply.

An n-MOS peripheral which performs synchronous communication control, 9903 also interfaces to the 9900 and 9980 via the CRU I/O port, allowing it to be packaged in a 20-pin 300-mil DIP. It requires a single 5-V power supply and TTL-level clock, and is programmable. Data rates can range from dc to 250K bits/s. Character length and sync register are programmable, and an interval timer is provided on-chip. It can handle various synchronous data transmission protocols including Bi-Sync and IBM's Synchronous Data Link Control (SDLC). Sample quantities will be available in the first quarter of 1977. Circle 184 on Inquiry Card

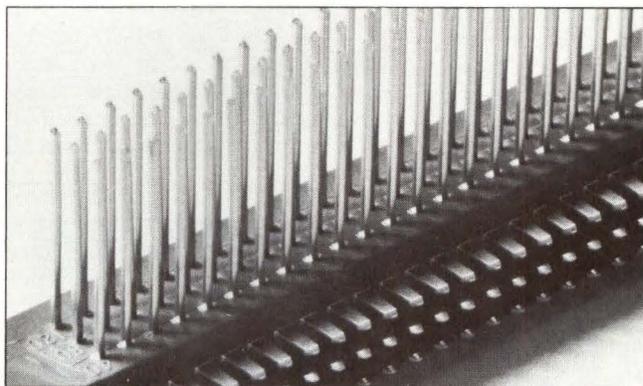
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Audio Response System Uses Are Economically and Technically Feasible

As a peripheral system for microcomputers, minicomputers, and large business mainframes, Votrax LVM-50 is a compact, solid-state multiplexed audio response system, providing multiline audio output and Touch Tone™ input handling capabilities. Features include variable word and message length for maximum flexibility; custom vocabulary consisting of words and phrases in the voice of the customer's choice; support of a wide range of audio response data sets, such as the company's Audio Response Modem, Bell 407A and 407B, and several commercially available 403 type units, plus full-feature support of the Bell Transaction™ Telephone, Automatic Call Distributor, and Call Directors.

Claimed by its manufacturer, Vocal Interface Div, Federal Screw Works, 500 Stephenson Highway, Suite 102, Troy, MI 48084, to offer large cost

and technical advantages, the system is simple to install and operate. Use of microprocessor technology in the system controller enables it to simulate operation of an asynchronous terminal (RS-232-C) on the host computer's communications port. All transactions between the controller and host computer are conducted using standard data formats without the need for elaborate support software or special interfacing hardware. Circle 185 on Inquiry Card

Microcomputer Card Optimizes Flexibility and Computing Power

The Am6800 microprocessor card is designed primarily for an Altair 8800 or IMSAI 8080 microcomputer. Enabling two microprocessors to be used in the same computer, the card allows a computer to be converted to an AMI or Motorola 6800 micro-

processor-based system, enables full use of software development, and increases total computing power. Card was developed by MRS, PO Box 1220, Hawthorne, CA 90250.

Requiring no modifications, the card is on one board and is pin compatible. It does not interfere with normal execution of 8080 programs. Features include 2-μs MPU cycle time, transfer time not exceeding one MPU cycle time, and alternate processing between 8080 and 6800 during one program. Card gains control via software command (one instruction); user can return control either by the front panel stop switch or through software (one instruction). Memories are fast or slow, static or dynamic. MPU status signals are brought out on unused bus lines (jumper option). At the same time, the 8080 processor card remains in the computer to handle all front panel controls. Current drain of the 6800 card is less than 1 A.

Available with socket for a 40-pin microprocessor, card has spare 14-pin IC etched holes for custom changes. All data and address lines are 3-state buffered. Cards are fully assembled and tested, with schematics included. □

Circle 186 on Inquiry Card

New... from Delta
USER PROGRAMMABLE DISPLAY TERMINAL

Introducing the **DELTA 4500**—The new display terminal with round-the-clock reliability that's ready to solve your problem now, at a price that's hard to beat.

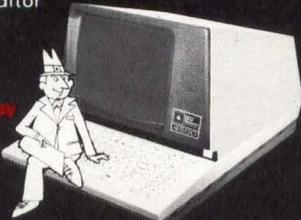
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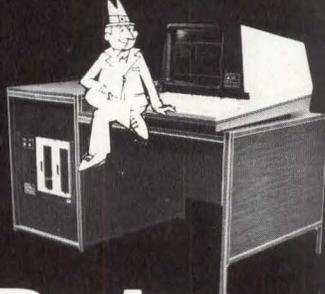
Introducing the **DELTA 4700**—the data storage and handling system that reduces computer time, lowers data processing costs, and simplifies data handling for text editing, data entry, and data storage and retrieval applications.

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- Up to 16 kilobytes of read/write memory (up to 64K option)
- Data manipulation, including Read/Write, Modify, Search and Copy.

The **DELTA 4700** System also:

- Is backed by nationwide customer service in over 150 locations
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- Is supplied with full documentation—hardware and software.

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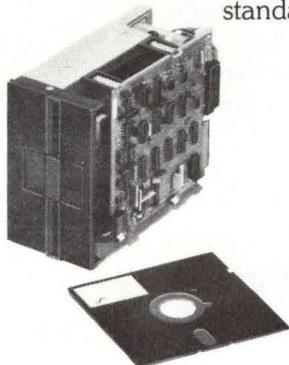
Go minifloppy.

This little half-pint is half the size, half the cost of a standard floppy but Shugart packs a lot of proven technology into that itty-bitty box (3.25" x 5.75" x 8.0").

The same proprietary glass bonded ferrite/ceramic read/write head and recording technology used in 40,000 standard-sized Shugart floppy drives give the SA400 minifloppy dependable data integrity— $1/10^8$ soft errors, $1/10^{11}$ hard errors. You'll be hard pressed to find that integrity in any cassette.

You won't get 110 K byte storage capacity at 125 K bit/second data transfer rates either.

Special minifloppy drive features include direct drive stepping motor actuator, DC servo-controlled spindle drive, and less power dissipation than any standard floppy.



The minidiskette media is just like the standard flexible disk, only smaller. Available in hard or soft sectored formats from several media sources, it shares the same oxide formulation, technology and technique of manufacture.

Protective jacket is just 5.25" square.

The Shugart minifloppy drive keeps data safe, too. Positive media interlock prevents minidiskette damage.

Our standard write protect circuitry prevents loss of recorded information.

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Whether you build word processing equipment or an entry level microprocessor system, an intelligent calculator or a hobby computer, the Shugart minifloppy drive can help you bridge the price/performance gap between cassette and standard flexible disk.

The gap is gone.

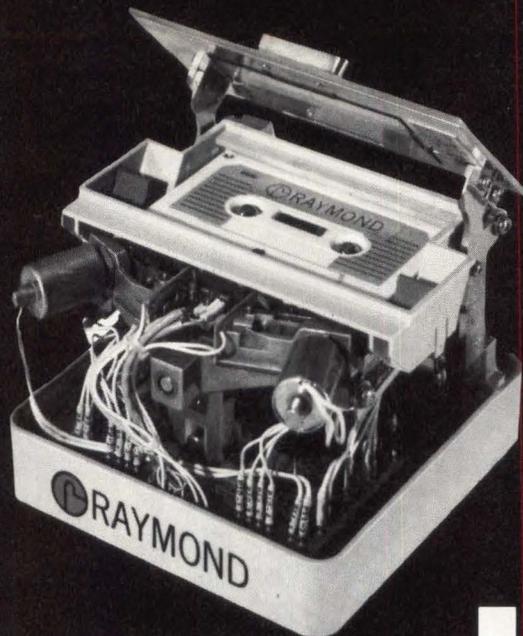
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The introduction of the first Raycorder in 1970 marked the end of the struggle to use basically audio-type cassette transports in digital systems. Designed solely for digital data, the Raycorder established new standards of accuracy and reliability.

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It continues to be the finest transport for standard Philips cassettes. Our free brochure tells the full story.

Size: 5.5" x 5.8" x 3.9"

Weight: Under 4 pounds

Data Transfer Rate: Up to 24,000 BPS

Data Capacity: 700K bytes

two sizes



Mini-Raycorder

With the advent of the micro-processor has come the need for even smaller tape transports—in test equipment, in desk-top calculators, in portable battery-operated terminals and in scores of other applications. Once again, Raymond is ready.

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Size: 3.0" x 3.0" x 1.8"

Weight: 16 ounces, including electronics

Data Transfer Rate: 2,400 BPS

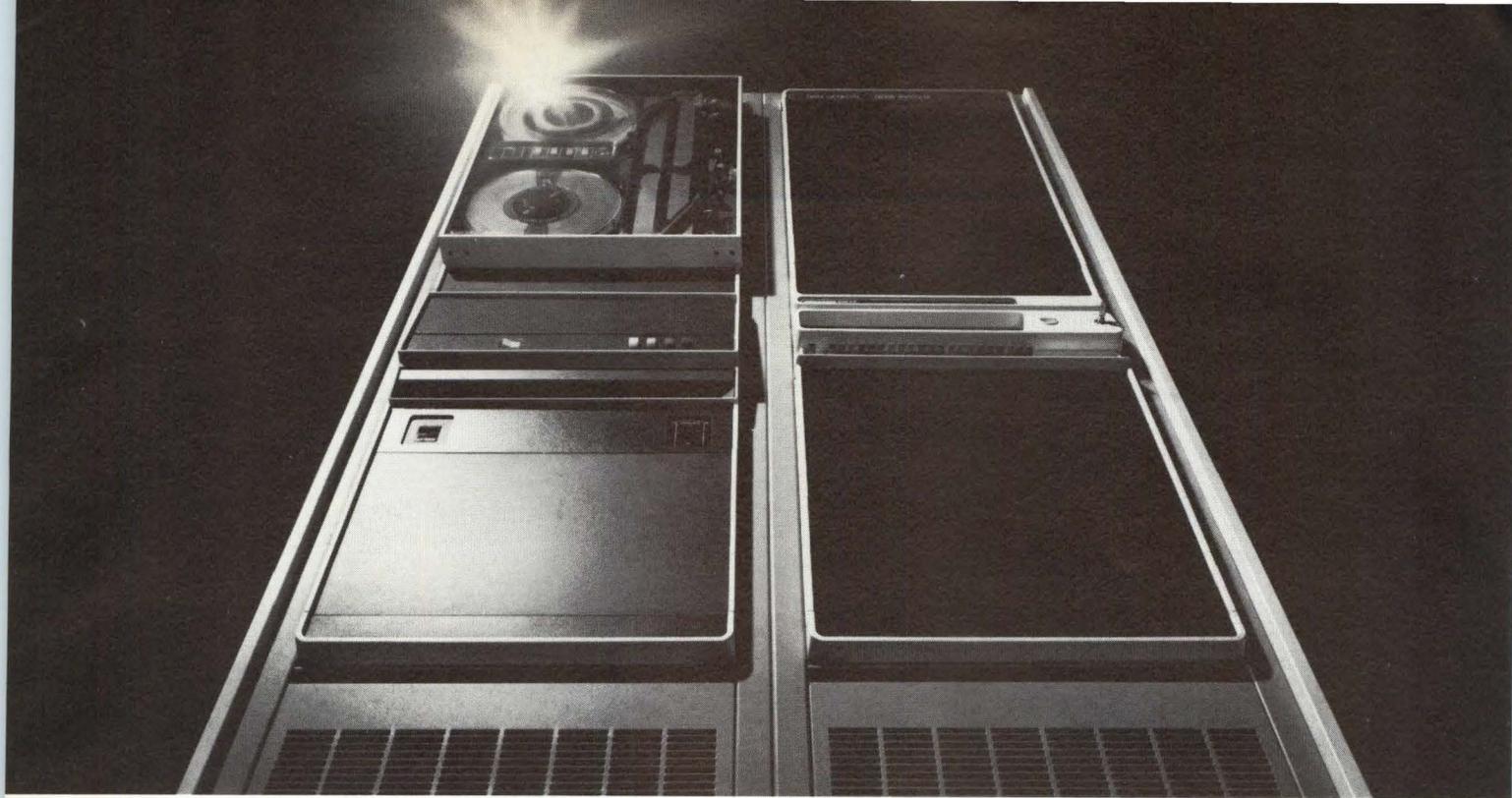
Data Capacity: (single-track) 128K bytes

Complete specifications are available for the asking. Contact "Bud" Gould.



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The single-board CPU design concept Data General pioneered. The same concept that led to our removeable single-board power supply module.

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And see what the NOVA line is up to now.

NOVA 3/D

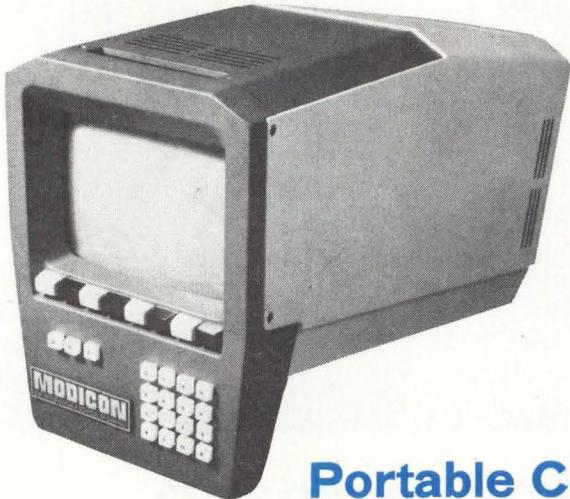
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CIRCLE 61 ON INQUIRY CARD

PRODUCT FEATURE



Portable CRT Panel Performs Online

Debugging and Editing of Programmable Controllers

Program editing of complete programmable controller (PC) circuits can be performed without disturbing the PC from performance of its existing program through use of the model P140 universal programming panel (UPP). Once all changes are made in a circuit, the PC program is automatically updated with those changes by pressing a single button. Claimed to be the first CRT programming panel designed for online use, this portable UPP is built to withstand shop floor use and is designed to be compatible with all current and future Modicon Corp programmable controllers.

Monitoring, editing, debugging, and programming can be conducted from a single location. The control engineer can check on the operation of machines or processes without leaving his office, or can carry the 40-lb UPP to a convenient location on the shop floor.

Operating Features

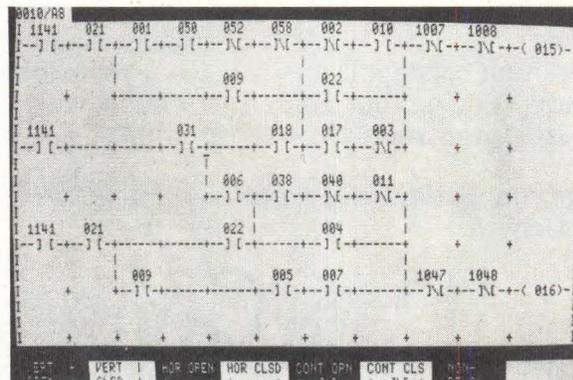
From one to seven lines of logic, each containing up to 10 contacts, can be displayed on the CRT screen, permitting control engineers to program circuits directly from their re-

lay ladder diagrams. Lines and contacts can be interconnected horizontally or vertically in any manner desired within the 7 x 10 screen matrix. The control engineer, therefore, sees his complete multiple-element circuit develop on the CRT screen as he programs it, and can copy relay programs from original relay ladder diagrams without modification.

Changes can be made at will on the multiple elements after a free format circuit is programmed. Contacts can be moved vertically or lines moved horizontally for flexi-

bility when editing or debugging such programs. In addition, the UPP can handle conventional 4-contact/line programming, using two independent portions of a split screen. Up to 14 logic lines can be displayed at one time with this concept.

Automatic cross-referencing of inputs and outputs is accomplished by calling up the next line of logic in which an input or output is used and displaying it on the screen. Alternately, numbers of all lines in which that input or output is used can be listed. The next line in the program can be called up auto-



Close-up of CRT screen. Designations in alternating black and white blocks across bottom of display serve as changeable labels for buttons of opposite colors positioned directly below on the face of the panel. When a button is pushed, its corresponding label on the CRT changes to indicate the function performed.

matically by pressing an increment button, and an erase function permits a line to be removed from the screen.

Values contained in registers within the controller can also be displayed. The control engineer can then watch data enter and leave registers, ensuring proper operation of the data transfer functions programmed into the controller. Depending on operator preference, numeric values of registers can be displayed in decimal, hexadecimal, or binary notation.

Unlabeled multiple-purpose buttons across the top of the panel just below the CRT screen (see UPP photo) are identified on the lower part of the screen in positions relative to the buttons (as shown on the close-up of the screen). These labels, alternating black and white opposite to the color of the respective button, change designations as necessary, in essence providing a large number of labels for only eight buttons. For example, when a button labeled "relay" on the screen is pushed, its label would automatically switch to "normally open series contact" or other meaningful designation.

In addition to the portable P140, a desk-top P145 version is available. This model includes an ASCII keyboard in addition to all features of the smaller model and can be used as a terminal when plugged into the company's 1084 PC.

Price and Delivery

Price for the P140 universal programming panel has not been firmly established, but it will be "competitive" with that of the company's P112 manual programming panel (\$4500). Production deliveries will begin in November. Modicon Corp, PO Box 83, Shawsheen Village Station, Andover, MA 01810. Tel: (617)475-4700.

For additional information circle 199 on inquiry card.

Microprocessor Software

Intel 8080/8008 • Intel 4040/4004 • Motorola 6800 • Fairchild F8 • Signetics 2650

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These programs, written in ANSI standard Fortran IV, have been installed on various computers from 16 bit minis to 60 bit maxis. (over a dozen different manufacturers) The assemblers are compatible with those available from the respective suppliers. Additionally, the Motorola, Fairchild, and Signetics assemblers have macro and conditional assembly facilities not provided by the manufacturers. The simulators enable users to set breakpoints, trace program flow, display and modify registers and memory, simulate I/O and interrupts, etc.

We provide many services that you don't usually get from the manufacturer including:

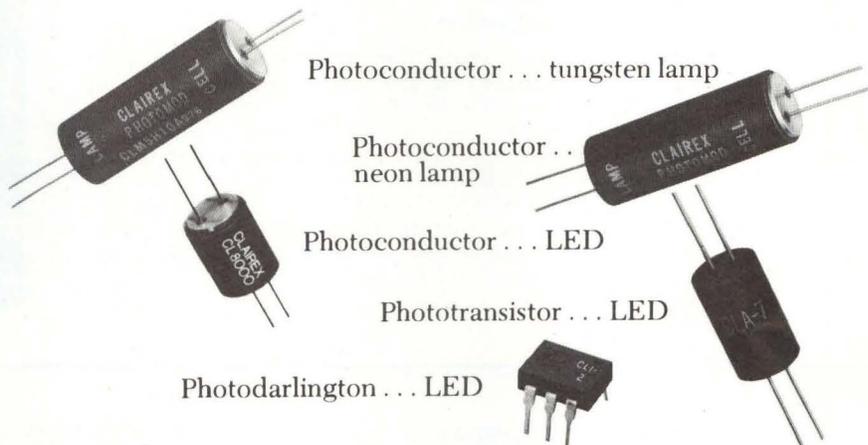
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- advice on what is necessary to modify Microtec's programs for customers' individual requirements

These programs are well commented, modular and fully documented. A manual and source listing accompany each program. The Assemblers are priced at \$800 and the Simulators are priced at \$650.

For more information contact **MICROTEC**
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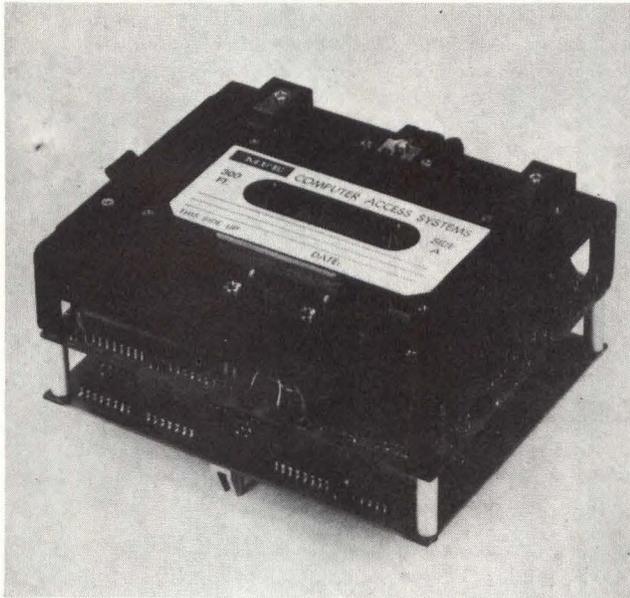
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CIRCLE 63 ON INQUIRY CARD

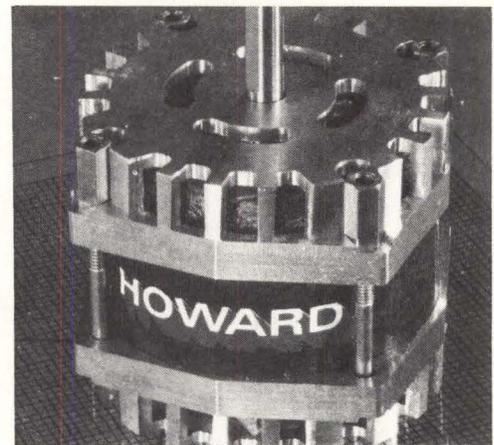


I/O Board for Cassette Transport Provides Mini and Microcomputer Parallel Interface

Over 75% of the circuitry as well as timing adjustment flexibility necessary for parallel interface to almost all mini and microcomputers are supplied in an 8-bit I/O board that plugs into and becomes part of the company's 250B digital cassette transport. Only supply line terminators have to be added by the customer in order to record data in an ANSI/ECMA compatible format. I/O consists of eight each input, output, and control lines and five interrupt lines. The parallel option includes four speed controls for R/W, search, low rewind/fast forward, and high rewind/fast forward; adjustable write oscillator for write clock generation; and biphasic level encoder/decoder circuits for recording at data rates up to 32K bits or 4K bytes/s. A 40-pin, 3M-type 3432 connector joins the board to the customer's interface. **MFE Corp.**, Keewaydin Dr, Salem, NH 03079. Circle 200 on Inquiry Card

Floppy Disc Drive Motor Matches Power Output in Shorter Configuration

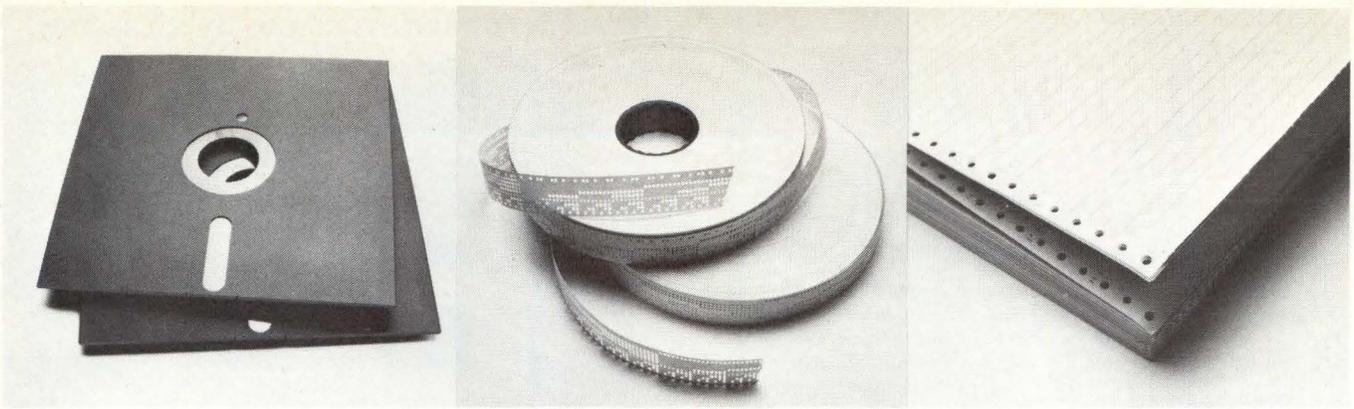
Although only 2 $\frac{3}{4}$ " high, nearly 17% shorter than motors of equal power, the FHP floppy disc drive motor delivers $\frac{1}{400}$ hp and is completely interchangeable with other motors used for the same purpose. Torque range of the reluctance synchronous motor is $\frac{1}{125}$ to $\frac{1}{40}$ hp. The company claims that a precision-machined end housing which maintains accurate concentricity of parts provides an air gap that is far better than that of conventional motors. Specs include 115/230-Vac, 50- to 60-Hz power requirements; 115-V, 0.35-A or 230-V, 0.18-A full load current; 115-V, 0.55-A or 230-V, 0.28-A lock rotor current; 1500 to 1800 rpm; and 90- to 127-V range. Ball bearings are used and thermal protection is a standard feature. **Howard Industries**, 1 N Dixie Highway, Milford, IL 60953. Circle 201 on Inquiry Card



Random-Access Alphanumeric Display Meets Microprocessor Application Requirements



Complete interface, drive, and refresh electronics on the 2.3 x 8.2 x 0.8" DE/200 random-access alphanumeric display peripheral offer universal compatibility with bus-oriented microcomputer systems. Each of 20 char positions in the 6.6" line is directly addressable. Display changes on the "Micro-Display" as ordered by the microprocessor are instantaneous, with no line shift effect. The 0.35 x 0.2" char, produced by fluorescent technology, are readable at up to 20 ft under ambient light conditions. Char design is 14-segment starburst; color is blue-green, filterable to blue, green, or yellow; and set is full upper case ASCII as well as char plus period and char plus comma. Signal connections consist of five address, three strobe, and eight data. There are six power connections for 5 Vdc at 1 A; 45 Vdc, 20 mA; and 8.5 Vac, 70 mA. **Digital Electronics Corp.**, 2126 Sixth St, Berkeley, CA 94710. Circle 202 on Inquiry Card



WE'LL READ, TYPE, RECORD, PRINT, PUNCH, SPOOL AND REPRODUCE FOR JUST ABOUT ANYBODY.

We believe everybody has the right to choose the best computer system to fit specific business needs.

That's why we make the best peripheral equipment for just about any configuration.

And that's why behind that claim we've put over 100 years of experience in precision engineering and gaining electronic capabilities to meet the demands of almost any system.

So, today, we have the equipment for whatever media is best for you.

PRINTERS

We have a whole group of matrix printers to pick from, in various speed ranges and all with superb accuracy and neatness.

For instance, there's our new 4540 matrix, with a revolutionary printing head, high speed printing, and economical cost.

PAPER TAPE

If paper tape meets your needs, we've got high quality readers, spoolers, or punches for your choosing.

Take our Facit 4020 Paper Tape Reader or Facit 4070 Tape Punch, for example. They're already seen with some of the best computers in the world.

FLEXIBLE DISKS

And, if you're looking for flexible disk drive, we can work together, too.

Our single floppy disks are expertly designed for easy installation, safe disk handling, and one of the fastest access times around.

Even better, our dual floppy disks give you all the same precision and accuracy, plus twice the data capacity of the single machine for only a fraction more investment.

And the special box-in-a-box construction, with its ability to reduce the problems created by heat and increase reliability, is something you won't find in any other flexible disk drive.

So, whatever Facit peripheral you choose for your needs, you've selected our choice piece. Because they're all made to work hard, work long, and require a minimum amount of maintenance.

In fact, we honestly feel that no other OEM manufacturer offers a better performance to price ratio. It's just part of the Facit belief that all our equipment should make work easier and more efficient for everybody.

If you'd like more information about our equal opportunities in peripheral equipment, send us the coupon below. We think you'll find Facit has the right idea about all your business needs.



4070 PUNCH

4231 DISK DRIVE

4554 PRINTER



CDN1076

66 Field Point Road Greenwich, Conn. 06830

Please tell me more about Facit's equal opportunities in peripheral equipment.

Name _____

Company _____

Address _____

City _____ State _____ Zip _____

PRODUCTS

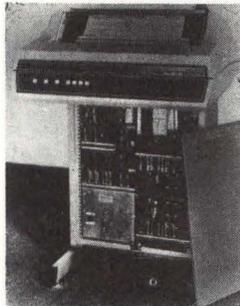
DISKETTE EQUIPPED MICROCOMPUTER

TD-1 TermiDisk is a communications-oriented microcomputer equipped with one to four std IBM-compatible diskette devices. Resident programs for file management and editing operate with full editing power on a single disc but can be field expanded to up to four diskettes and nearly 1M bytes of storage. Control of the system is achieved through keyboard or code control, allowing the same capability for remotely located terminals as is available to the local terminal. Communication with terminals and modems is through standardized serial ports equipped with RS-232 or current-loop interfaces. Two ports



are provided; each is capable of communication with 5-, 6-, 7-, or 8-bit data at rates of from 50 to 19,200 baud. **International Computer Products, Inc.**, 2925 Merrell Rd, Dallas, TX 75229. Circle 203 on Inquiry Card

COMMUNICATION CONTROLLER



Processor-based TermiNet™ 9600 communication controller is a factory programmed device with processor, solid-state memory system, power supply, and I/O interfaces. It can handle data transmission up to 9600 baud synchronous or asynchronous and is compatible with different communication protocols through emulation packages. Presently available are IBM 2780 or 3780, DCT-1000, and packages for use on Mark III time-sharing service. A self-test card evaluates controller logic, isolating faults

to a card and giving visual display of system status. Memory can be composed of EPROMs, RAMs, and jumper-programmable ROMs. Firmware control program in EPROM is executed by the processor. I/O interfaces are asynchronous, synchronous, and parallel. **General Electric Co., Data Communications Products Dept.**, Waynesboro, VA 22980.

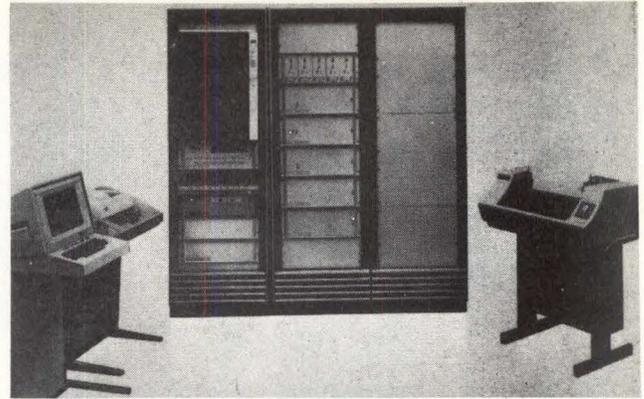
Circle 204 on Inquiry Card

PC BOARD TEST CLIP

Designed specifically for testing, debugging, and troubleshooting complex PC boards, the Sunnyclip makes a temporary electrical connection with a plated-through hole of a double-sided PC board without damaging plating. A split sleeve of brass is press-fitted into the device's pinch type grip body. A reverse tapered pin, attached to the grip, serves as an "expander" for the split sleeve. When the grip is squeezed together, the tapered pin is forced out of the split sleeve, allowing the sleeve to collapse. In collapsed mode, the pin will enter a #51 (0.067") plated-through hole with zero force. Once in position, the grip is released, and the tapered pin automatically returns the sleeve to its original expanded mode, producing a firm, broad area contact with the hole plating. **Sunny Day Designs**, PO Box 146, Ann Arbor, MI 48107.

Circle 205 on Inquiry Card

ANALOG INSTRUMENTATION INPUT SUBSYSTEM



The 7200 series system input subsystem is integrated from modular components, allowing users to choose any number and type of analog inputs. It is shipped pretested, ready for installation on Data General Nova and Eclipse, DEC PDP-8 or 11, or similar mini-computers. Analog input is accommodated with 8-channel multiplexer cards inserted into a 16-position chassis. Sixteen chassis give a total of 2016 channels; two channels in each chassis are reserved for calibration. Multiplexer cards handle input ranges from ± 5 mV to ± 10.24 V using J-FET, MOS-FET, and low thermal reed relay switches. Digitizing and control occur through the universal data acquisition and control module, which contains input multiplexer, gain switching amp, sample/hold circuits, ADC, and power supply. A third chassis provides subsystem control, reducing overhead requirements of the minicomputer. **Datum Inc., Data Systems Div.**, 1363 S State College Blvd, Anaheim, CA 92806.

Circle 206 on Inquiry Card

REEL-TO-REEL TAPE TRANSPORT

Low profile 7- or 9-track unit provides 120K-byte/s data transfer rate using Floating Shuttle™ buffering concept. Operating at 75 in./s with std 8½" reels of ½" magnetic tape, the model TDX/8 records at densities of 800 bits/in. NRZI, 1600 bits/in. PE, or dual density. Data transfer rate is 120K bytes/s at 1600 bits/in.; total storage capacity on 1200 ft of tape is >23M bytes. Low 12" vertical height is achieved by elimination of need for vacuum columns, and allows use of the transport in minicomputer and avionics systems. The shuttle method reduces parts count, provides improved MTBF, and lowers power consumption. Elimination of vacuum pumps reduces the noise level. **Qantex Div., North Atlantic Industries, Inc.**, Plainview, NY 11803.

Circle 207 on Inquiry Card

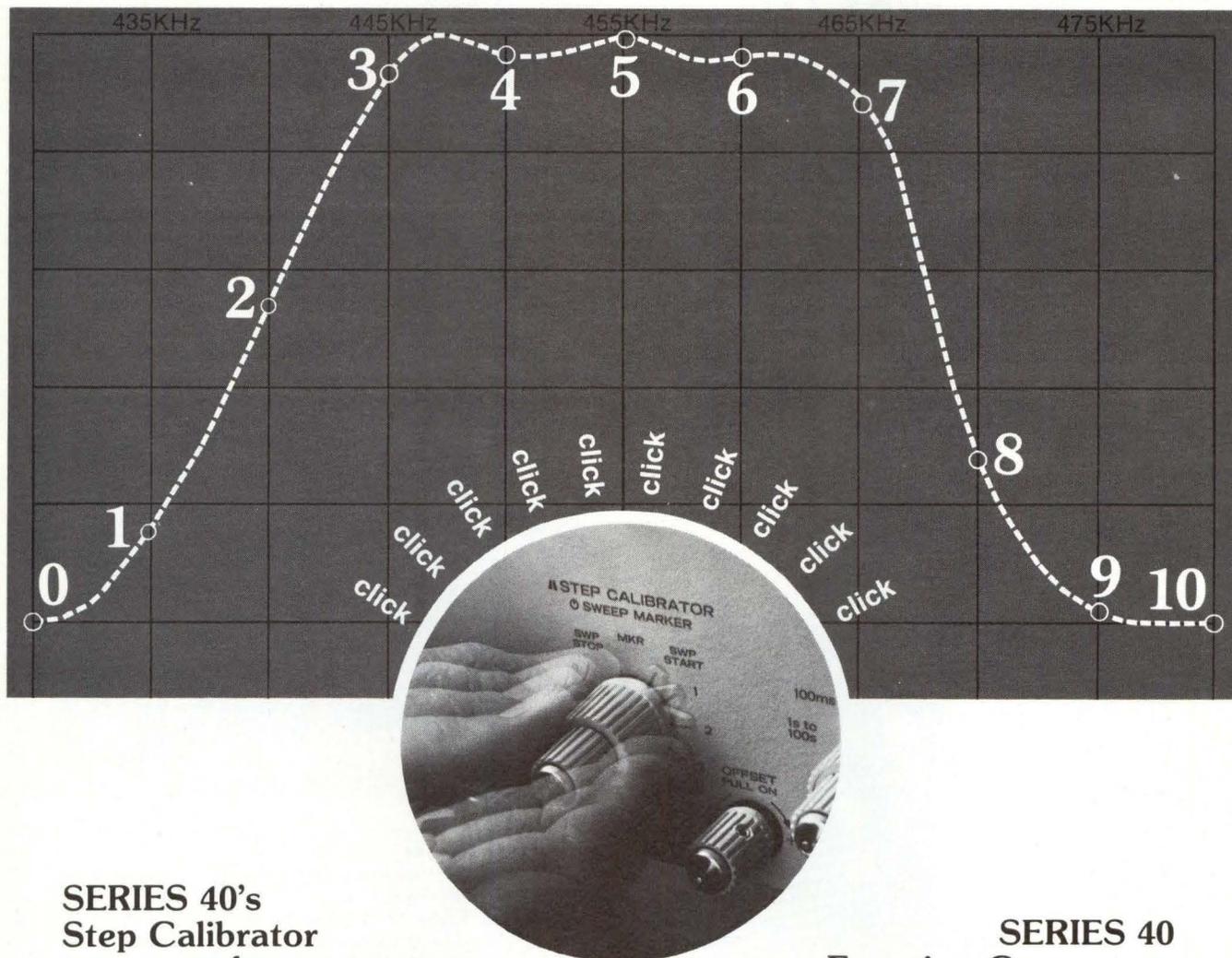
LIGHT PEN



LP-400 series offers sensitivity of 2 ft-L with response time of <300 ns to permit high speed, real-time graphic systems. All circuitry is contained in the pen's body and is TTL compatible, eliminating the need for extra boards in the customer's system. Patented touch-actuated switching provides fingertip control with no bounce, and lifetime immunity from corrosion and wear. The finder light beam insures accurate focusing of photodetector on a 0.130" acceptance circle. Spectral response is from 3600 to 9000 Å; radiant sensitivity is 2 ft-L with 200 ns, 0.02 spot; and background tolerance is 10^2 mW/cm² (direct sunlight). Duty cycle is 100 kHz; and power requirements are -15 V $\pm 5\%$, 30 mA and 5 V $\pm 5\%$, 175 mA. **Information Control Corp.**, 9610 Bellanca Ave, Los Angeles, CA 90045.

Circle 208 on Inquiry Card

How to get through a bandwidth in ten easy steps.



SERIES 40's Step Calibrator measures frequency response with the click of a switch.

Set SERIES 40's main dial *once*, and you'll get eleven precise frequencies in ten equal steps by simply clicking the Step Calibrator switch from zero to ten. With 1000:1 frequency change in the log mode, each step is equivalent to approximately one octave, which is particularly useful in audio testing. And unlike other function generators, SERIES 40 allows you to step up or down without having to cycle through the entire ten steps.

So — when you're testing frequency response, just set up the band edges and click through the ten steps, measuring amplitude at each step... it's that easy.

SERIES 40 Function Generators — New from INTERSTATE

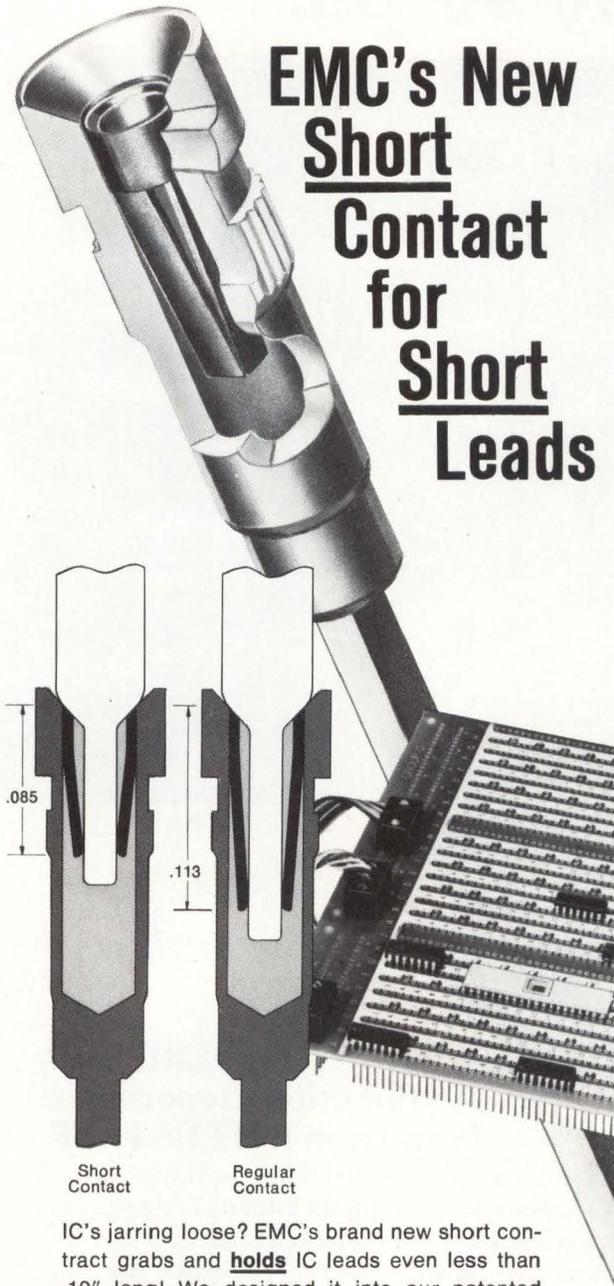
SERIES 40 gives you plenty of amplitude — 40 V peak-to-peak (open circuit) — and takes the guesswork out of pinpointing response with its continuously variable Frequency Marker. SERIES 40 also offers you INTERSTATE's exclusive direct-reading sweep limit control and full spectrum of function generator capabilities in five models from \$475 to \$695. For additional SERIES 40 specifications, call Product Marketing at (714) 549-8282, or write Interstate Electronics, Dept. 7000, Box 3117, Anaheim, CA 92803.



INTERSTATE
ELECTRONICS CORPORATION
Subsidiary of A-T-O Inc.

Short Story

EMC's New Short Contact for Short Leads



IC's jarring loose? EMC's brand new short contact grabs and **holds** IC leads even less than .10" long! We designed it into our patented Nurl-Loc® terminal to provide the precise insertion and withdrawal forces you need. And Nurl-Loc® gives you 5 times the gripping surface to prevent twist and spread the stress to eliminate warping. Short contacts are available now in EMC's Wire-Wrap® Panels . . . and in our full line of DIP and Transistor Sockets. Call Allan Klepper (401) 769-3800 for the longer story, or write Electronic Molding Corp., 96 Mill Street, Woonsocket, R.I. 02895.

Wire-Wrap® Gardner-Denver Co.



PRODUCTS

TOUCH INPUT SYSTEMS

Comprising a matrix of IR light beams projected directly above the working surface, the touch input system is activated by interrupting an X and a Y beam, using any stylus opaque to IR, such as a finger or a pencil. It produces the coordinates of the broken beams as binary X and Y data. Operation is completely digital, and requires no programmed tracking or A-D conversion. Systems are suitable for replacement of light pens or tablet input systems, and can be used with computer-generated displays, film projection, or other systems. Unit features audible feedback response, serial or parallel interface, and diagnostic test points. Electronics are 7400-series TTL, and photo-optics are TIL-31 and -81. Resolution is 0.250" min. Scanning rate is 150 char/s max. **Carroll Mfg Co**, 1212 Hagan St, Champaign, IL 61820. Circle 209 on Inquiry Card

DATA ACQUISITION SYSTEM

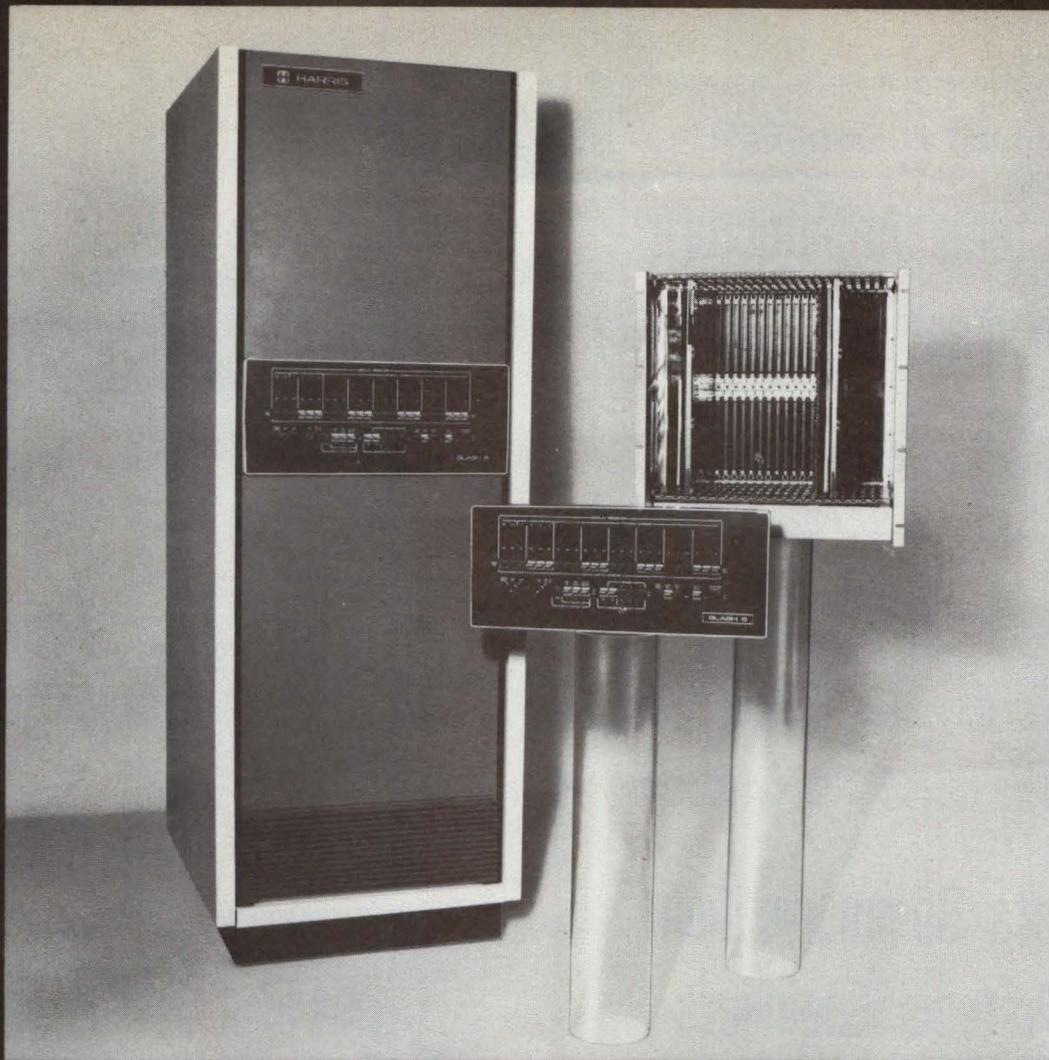


A microprocessor-based system designed for industrial process and test monitoring, scanning, alarming, and control, Digitem System 2000 is available in configurations ranging from small satellite to large scale versions having 2000 inputs or more. The system uses unique FXS signal conditioner and multiplexer designs to provide flexibility and reliability. Directly compatible with temperature sensors and std transducers, the device's output options include strip and line printers, CRT displays, punches, mag tape, and teleprinters. Features include phantom pushbutton operator's panel or CRT interactive operator's setup panel, analog and digital inputs, control or annunciator outputs, and choice of peripherals. **FX Systems Corp**, Mount Marion Rd, Saugerties, NY 12477.

Circle 210 on Inquiry Card

AUTOMATED REMITTANCE PROCESSING SYSTEM

ReaDoc Mark IV reads OCR documents or punched cards, audit trails checks and remittance documents, endorses checks, and encodes them in MICR symbols. Capturing, processing, and recording each remittance in a single transaction, the device reduces manual handling. No preprocessing or sorting is required. System can process multiple payments with a single check, and multiple checks for a single payment. A typ system consists of minicomputer with 64K byte memory, disc drive (5.8M- to 50M-byte capacity), magnetic tape drive, and from one to 32 terminals and/or CRT key entry stations. Each terminal is composed of CRT, keyboard, punched card or OCR reader, document transport, MICR encoding unit, check transport and endorser, audit trail units, and multiple microprocessors for control. **Ball Computer Products, Inc**, 860 E Arques Ave, Sunnyvale, CA 94086. Circle 211 on Inquiry Card



The Harris Slash 6. Supermini performance. At super minicost.

If you recognize optimum price/performance value when you see it, you should see our new SLASH 6. It outperforms most 32-bit minis, at a price that's better than many 16-bit minis.

The Harris Slash 6 costs only \$14,500*. You get 600 nanosecond cycle time; 48KB of MOS memory with error correction; hardware multiply, divide, and square root; 8 priority interrupts; and a turnkey control panel.

You get building-block architecture

that lets you expand your systems as your needs expand. And sophisticated real-time software that no other machines offer in this price/performance range.

The Harris Slash 6. The first truly low-cost/high performance computer for all of you who were waiting for optimum price performance value. Harris Computer Systems, 1200 Gateway Dr., Ft. Lauderdale, FL. 33309. Europe: Techmation N.V., Gebouw 105/106, Schiphol-Oost, The Netherlands.

HARRIS



COMMUNICATIONS AND
INFORMATION HANDLING

*Volume discounts available.

CIRCLE 67 ON INQUIRY CARD

147

Retail Point-of-Sale

Systems Architecture Development Engineers (2)

To define system requirements involving real-time POS micro/minicomputer systems.

Both positions involve the conceptual design, performance analysis and critical performance/cost trade-offs; one will emphasize the software system elements, the other the hardware elements.

An experience range of from 4-7 years in planning, design, analysis, and documentation of on-line, real-time systems mixed with some detail design work in both hardware and software development will meet the challenge of these 2 senior openings in our Advanced Development group along with your degree in engineering/computer science.

NCR's Point-of-Sale organization is expanding to meet the demands of the exploding POS market.

Data Communication Systems Engineers

To evaluate data communication module and equipment for applicability in Retail Point-of-Sale terminal systems. Will generate standards for data communication circuit handshaking and will propose future communication products. To provide support for data communication system analysis and proposals for future retail systems.

Candidates should bring a degree and a good understanding of Binary Synchronous (BSC), ANSI Asynchronous and SDLC Control procedures. Knowledge of Modems, Communication adapters, and Communication procedures essential and a knowledge of Common Carrier facilities desirable.

These 2 opportunities in our Retail System Architecture organization are highly visible positions and offer strong exposure and growth.

NCR's P.O.S. facility is located in a lovely, rural community in east central Ohio.

We invite you to respond as soon as practical.

Robert W. Donovan
Terminal Systems Division—Cambridge
NCR Corporation
Cambridge, Ohio 43725
614-439-0398

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An Equal Opportunity Employer

PRODUCTS

DATA INSERTION GENERATOR



Capable of inserting two separate 16-char lines into any std video signal, the DIG-602 accepts BCD information via a rear panel connector to display IRIC time data on one line. A second line may be written from front panel thumbwheel switches, thereby displaying 16 char of the full ASCII uc subset. Position of the titling can be moved anywhere in the video frame via front panel controls. Length of each line of char can vary from 15 to 95% of the raster width. Inserted char video level can be continuously adjusted from 100% white to pure black with a potentiometer. With selection of auto contrast feature, level of the char will automatically switch from black to white as the background gray-scale changes. **I.S.I. Group, Inc.**, 133 Jackson St NE, Albuquerque, NM 87108.

Circle 212 on Inquiry Card

PORTABLE TERMINALS

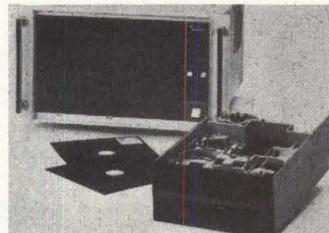


Providing a low cost method of testing communication systems and debugging programs, Execuport model 380 "Troubleshooter" functions as a std portable terminal and has an operator-switchable char set that allows printing of normal nonprint char such as device control codes and vertical and horizontal tabs. Std models operate on ASCII, but units can be supplied for use with other codes, such as APL, Baudot, IBM correspondence code, or RS-244A—the EIA code used in NC operations. Terminal receives and prints a continuous data stream at speeds up to 30 char/s. Operations normally performed upon receipt of a nonprint char, such as carriage return, are not executed; instead a special symbol is printed to provide a graphic record of the data stream. **Computer Transceiver Systems, Inc.**, E 66 Midland Ave, Paramus, NJ 07652.

Circle 213 on Inquiry Card

FLEXIBLE DISC SYSTEM

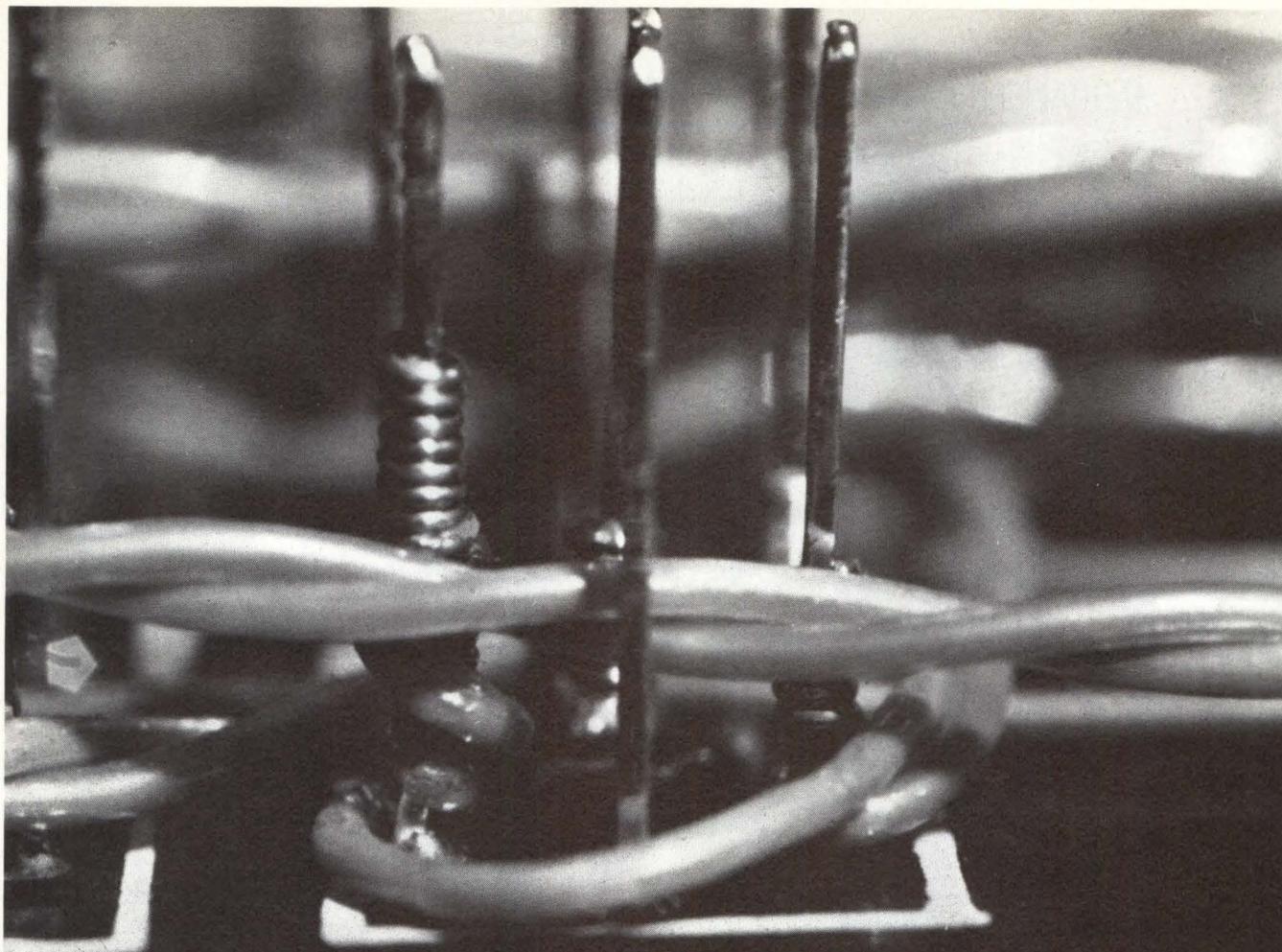
RFS 7500 incorporates from one to four flexible disc drives, formatter electronics, and power supply in a 19" rack-mountable chassis. Formatter is microprocessor-based, performing many functions within the system which normally require computer



time. Features include ability to implement IBM 3740 format or user-selectable variable sector size. In the latter, adjustment of a simple DIP switch on the formatter PC card allows the user to select a 1-, 2-, 4-, 8-, 16-, 26-, or 32-sector format. Use of soft sectoring technique similar to

IBM 3740 format permits users to increase data capacity by decreasing sectors without changing software. Variable length data block transfer saves computer time. **Remex, div of Ex-Cell-O Corp.**, 1733 Alton St, Santa Ana, CA 92705.

Circle 214 on Inquiry Card



KYNAR^{*} resin... the tough, reliable and economical insulation for computer wires.

Kynar insulated wire has been performing successfully in hundreds of computer installations for over 12 years because Kynar PVF-2 coated wire is resistant to shorts that result from cut-through abrasion.

Yes, Kynar is tough. It resists the abrasion and cut-through that can occur during wire-wrap machine application. Its excellent resistance to cold-flow protects against electrical failures when wires are bent tightly around sharp-cornered posts. Kynar cuts and

strips smoothly in automatic wiring machines. It is heat-resistant, lightweight, and has exceptionally high tensile and impact strength.

Kynar is readily available, and at a truly economical price. For a sample, complete specs and a list of wire fabricators, contact the Plastics Department, Pennwalt Corporation, Three Parkway, Philadelphia, PA 19102. (215) 587-7519.

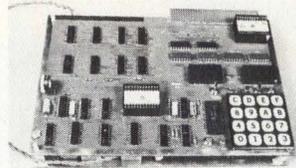
 **PENNWALT**
ENGINEERING PLASTICS

*Kynar is Pennwalt's registered trademark for its polyvinylidene resin.

PRODUCTS

1702A MANUAL EPROM PROGRAMMER

Features hex keypad, two digit hex address and two digit hex data display. Controls include load, clear, go! (step), key/copy, data in/data out, and counter up/down. Profile card includes high voltage pulse regulator, timing, 8 bit address and 8 bit data drivers/receivers. Two 6½" x 9" stacked cards with spacers. Allows programming in 20 minutes — copying in 5 minutes. Requires +5, -9, and +80 volts.



ASSEMBLED \$299.95
KIT \$189.95

NOW

The best of two worlds... use our 1702 EPROM programmer as a manual data/address entry programmer... or connect it to your processor.

IMSAI/ALTAIR computer interface (requires 3 output ports, +1 input port) and software \$49.95

Briefcase unit with power supplies and interface connectors (assembled and tested only) \$599.95

ANNOUNCING

Our NEW 16K Byte Pseudo-Static, IMSAI/ALTAIR compatible RAM. Single card slot. Uses less power than equivalent low power RAM. All memory chips socketed. Uses all prime, factory fresh ICs. High quality, two-sided, through-hole plated circuit board. Crystal controlled, totally invisible refresh system requires NO software management. Just plug it in and use like STATIC memory.

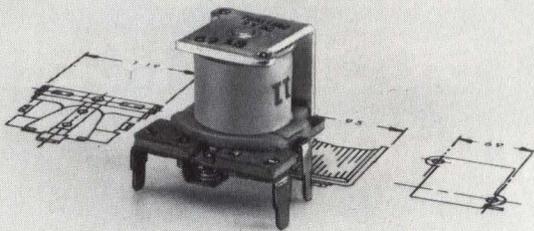
Complete kit \$349.95
Assembled, tested, and burned in \$549.95

ASSOCIATED ELECTRONICS

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CIRCLE 69 ON INQUIRY CARD

10 amps of switching in a 1" cube



Series 19 Relay. One of the most compact and reliable relays you'll ever use.

In just one cubic inch, the remarkable Series 19 relay combines the advantages of miniaturization with a capacity to handle heavy switching loads. Result: more performance in a smaller overall package. Yet the cost is low — less than \$2.00 each in 1000-piece quantities.

Contact arrangement is SPDT. Rating is 10 amps, 28 vdc or 115 v, 60 hz. Available coil voltages range from 3 to 24 vdc.

Consider the Series 19 relay for low level to 10 amp switching applications such as remote control, alarm systems and similar industrial and commercial uses.

Send for information now!

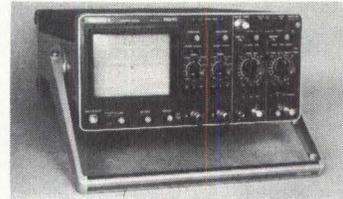
NORTH AMERICAN PHILIPS CONTROLS CORP.

Frederick, Md. 21701 • (301) 663-5141

CIRCLE 70 ON INQUIRY CARD

150-MHz PORTABLE OSCILLOSCOPE

PM3265E, a 150-MHz dual-trace oscilloscope, features on-screen display of both main and delayed timebase in the alternate mode, enabling both main timebase with intensified zone and delayed timebase expansion of both traces to be viewed simultaneously. Front panel trace separation controls allow easy alignment of the resulting 4-trace display.



The unit has 5-mV sensitivity to the full 150-MHz bandwidth and a max sweep speed of 2 ns/div. Cold switching techniques provide an efficient front panel controls layout which includes completely separate delayed

timebase control sections. Weighing 21 lb, the scope uses only 55 W. Use of a direct-conversion power supply allows operation from most voltage and frequencies from 90 to 270 V, ac or dc, without switching. **Philips Test & Measuring Instruments, Inc.**, 400 Crossways Park Dr, Woodbury, NY 11797.

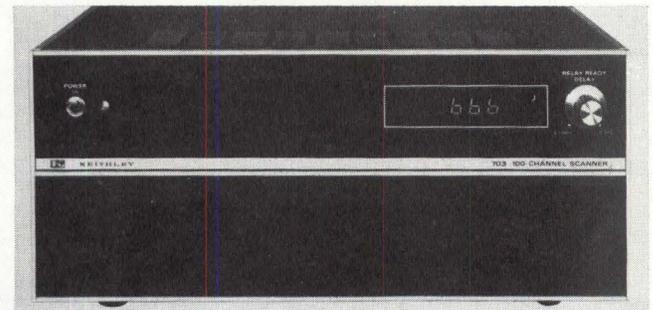
Circle 215 on Inquiry Card

SEMICONDUCTOR TESTING SYSTEM

Made up from modular components, the 203 permits automatic function and parameter tests to be programmed as desired so that problem- and memory-oriented tests are possible, and semiconductor memories can be tested under worst-case conditions. It operates with up to 16 multichannel clock-pulse generators and a time resolution of 1 ns at a max clock frequency of 20 MHz. Dc parameters such as short-circuit interruption, discharge, and loading currents can be measured. The system can also be used for multiplexing and/or testing stations operating in parallel. Core of the system is a microprogrammed CPU, which allows addresses and data to be generated independently of each other, permitting preprogrammed timing sets to be selected for each test cycle. **Siemens AG**, Postfach 3240, D-8520 Erlangen 2, Federal Republic of Germany.

Circle 216 on Inquiry Card

100-CHANNEL SCANNER



Model 703, a scanner mainframe that can switch up to 100 channels, is intended for use in the System 1, a calculator-controlled measuring system that provides instrument control, data acquisition, and reduction, and control of experiment or process. When used in the System 1, the scanner can be remotely controlled to select one or more of 100 channels; multiple active channels can be selected simultaneously. Remote control of channels can be accomplished in any order. Plug-in scanner cards provide highly isolated channel selection. Multiple scanner mainframes can be daisy-chained to expand to a total of 1000 channels. A 3-digit readout on the front panel displays the last switched channel and provides two error indicators. **Keithley Instruments, Inc.**, 28775 Aurora Rd, Cleveland, OH 44139.

Circle 217 on Inquiry Card

THE ONLY DISK DRIVES THAT DON'T NEED CLEAN AIR TO BREATHE.

Each Trident disk drive has its own enclosed air filtration system. No other removable-pack disk drives do.

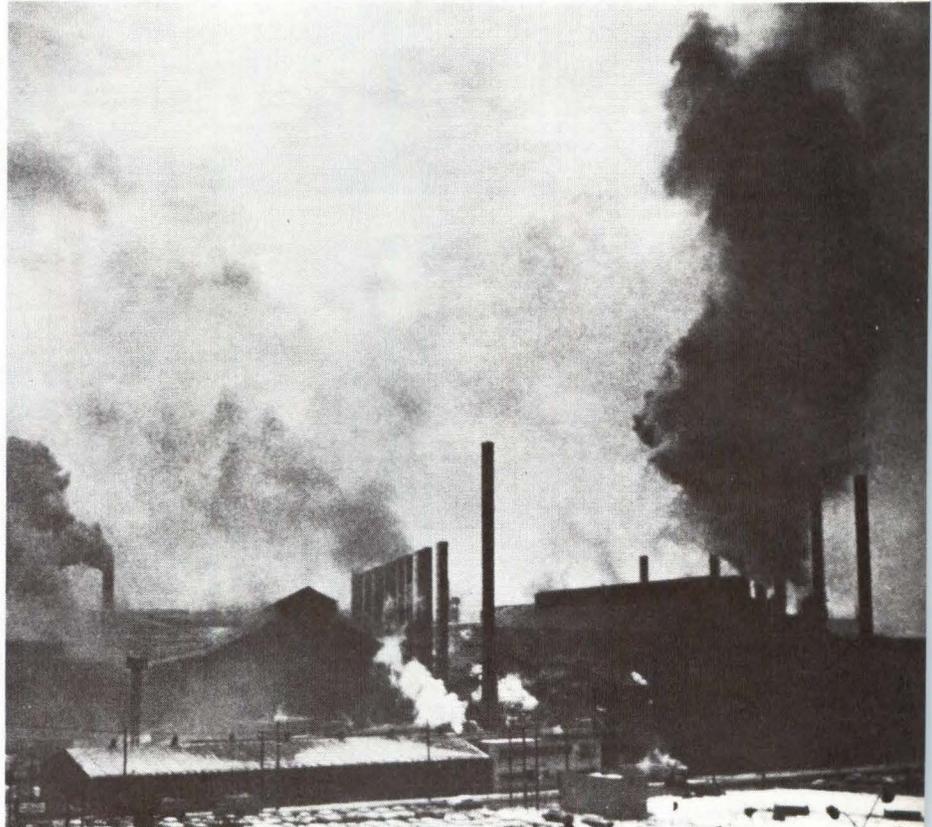
This means you can use a Trident just about anywhere. In a warehouse. Or a factory. Even in a smoke-filled room.

This kind of flexibility is just one reason Trident is the choice of growing businesses everywhere.

You find Tridents on the job in department stores—taking care of inventory control right at the point of sale.

Tridents are at the heart of the reservations systems for major hotel chains.

And Tridents are the continuing choice of the nation's leading OEMs.



NEW! LARGE CAPACITY TRIDENTS.

Now there are two new large capacity Trident disk drives—the T-200 and T-300.

They join the T-25, T-50 and T-80 to give you a wide range of capacities—all the way from 27 to 312 megabytes.

So now, as your needs grow, you have the capacity to meet those needs.

Each Trident model is functionally compatible with every other Trident model.

Each gives you track-following servo-technology. And each gives you one of the lowest cost-per-byte ratios in the industry.

A SOLUTION FOR YOUR PROBLEMS.

At CalComp we've been solving the data problems of growing businesses for years.

If your growing systems business needs

more flexibility, and if you want the experience and expertise that only CalComp can give you, call or write:

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CD-10-76, 2411 West La Palma Avenue,
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CALCOMP



The Right Time The Right Place The Right People



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Now that the nation's economy and the electronics revolution are accelerating again, next April is an ideal time to display electronics products and services directly to the key domestic and international audiences who will attend **Electro77**.

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(Attach Your Business Card Here)

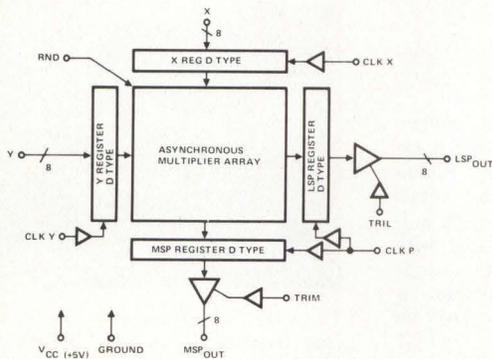
TWO FAST MULTIPLIERS For Signal Processing

• SINGLE CHIP

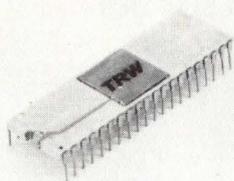
• BIPOLAR

• SINGLE 5V SUPPLY

8-BIT MULTIPLIER 130 Nanoseconds



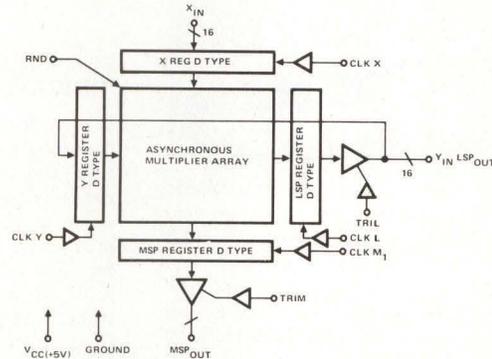
- Parallel 8 x 8 Bit
- Two's Complement
- Internally Latched
- TTL Compatible I/O
- 3-State Outputs
- Rounding Option
- Single Chip Bipolar Technology
- Asynchronous Multiply



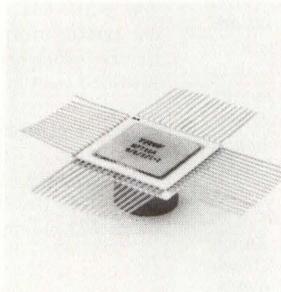
40-Pin DIP

**\$100⁰⁰
Each in
1-24
Quantities**

16-BIT MULTIPLIER 200 Nanoseconds



- Parallel 16 x 16 Bit Multiplier
- Two's Complement
- Internally Latched
- TTL Compatible I/O
- 3-State Outputs
- Rounding Option
- Single Chip Bipolar Technology
- Asynchronous Multiply



64-Pin Flat Pack
DIP available soon

**\$325⁰⁰
Each in
1-24
Quantities**

Coming next a 128-Bit Shift Register and a 64-Bit Parallel Correlator.

Delivery is 30 days or less. For detailed data, applications information and prices call (213) 536-1977. Or write: TRW Electronic Systems Division, One Space Park, E2/9043, Redondo Beach, California 90278.

LSI products from a company called

TRW

PRODUCTS

MICROPROCESSOR-CONTROLLED DATA TERMINAL



Printing at up to 45 char/s with a Diablo HyType II mechanism under program control, T-3000 terminal is supplied with EIA Standard RS-232-C, 25-pin interface connector and ASCII code. All logical circuitry, memory, microprocessor, power supply and keyboard are contained as a single desktop unit. The terminal is capable of self-diagnosing internal problems, and printing an error message to indicate if the error is internal or in the communications system. **Multiterm Corp.**, 2612 Artesia Blvd, Redondo Beach, CA 90278. Circle 218 on Inquiry Card

SERIAL INTERFACE FOR READER/PUNCH

Model 1560-S is a compact, self-contained desktop unit with integral electronics, power supply, and asynchronous serial interface. Designed for use between terminal device and its associated modem or data coupler, it can also be connected to the serial port of most mini and microprocessors. Punch operates at up to 60 char/s, perforating all varieties of commercial tape. Internal DIP switches allow reader data rates of 50, 75, 110, 134.5, 150, 300, 600, 1200, or 2400 baud, independent of punch rate. **Sweda International, OEM Products**, 34 Maple Ave, Pine Brook, NJ 07058. Circle 219 on Inquiry Card

HYBRID COMPUTER SYSTEM

A small scale, fully-integrated hybrid computer system, MiniHybrid includes Data-Pacer digital processor, with 16K-word core memory and 133K floppy disc capacity; parallel analog processor, hybrid communications interface with 60 analog/digital channels; and ASR-33 teletypewriter for digital I/O. An alphanumeric/graphic CRT terminal, X-Y plotter, and further digital, analog, and interface capability can be added. Both analog and digital software are provided. **Electronic Associates, Inc.**, West Long Branch, NJ 07764. Circle 220 on Inquiry Card

DOT MATRIX PRINTER

Double-head model 5703 has an output of 75 lines/min. at 132-char/line, and the single head 5701 prints at 50 lines/min. The 7 x 9 matrix printheads have been life tested to 150 million char. Buffer memory is composed of four 2 x 132-bit shift registers. The printers allow easy loading and unloading of paper, ribbon changes, and paper alignment and tension adjustment. Noise level is <65 dB. Std char set conforms to ASCII code. **Juki Machinery Corp of America**, 3186-G Airway Ave, Costa Mesa, CA 92626. Circle 221 on Inquiry Card

SUBMINIATURE INDICATOR LIGHTS

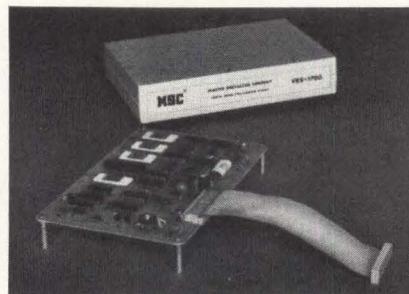
Lights use T-1 $\frac{3}{4}$ incandescent midjet flange base lamps, 1.35 to 28 V, which extend into the cap for full, uniform illumination. Caps are round, square, and rectangular, in $\frac{1}{2}$ -, $\frac{5}{8}$ -, $\frac{3}{4}$ -, $\frac{1}{2}$ x $\frac{3}{4}$ -, and $\frac{3}{4}$ x 1-inch sizes. Six colors are available with face and sides the same, or with opaque sides of a different color. Available for front mounting in $1\frac{15}{32}$ " holes and for front or back of panel insertion in $\frac{1}{2}$ " holes, assemblies are complete with mounting hardware. **Dialight, a North American Philips Co.**, 203 Harrison Pl, Brooklyn, NY 11237. Circle 222 on Inquiry Card

PAPER TAPE READER

ATR-400 reads photoelectrically at up to 400 or 480 char/s, 60-Hz synchronous, and 200 char/s asynchronous. It accommodates 5-, 6-, 7-, or 8-level tapes. Direct connection with TTL is possible. Optical reading system utilizes silicon solar cell photoelectric elements, and the light source is provided with an automatic luminance compensation circuit. Self-contained dc power source and compact construction reduce installation space. Rack mount is also available. **ASACA Corp of America**, 1289 Rand Rd, Des Plaines, IL 60016. Circle 223 on Inquiry Card

VOICE READOUT SYSTEM

The basic model 1700 consists of one circuit board and has a 1 to 16 word vocabulary; expansion to 32 words is possible with a second board. Each word is stored in a



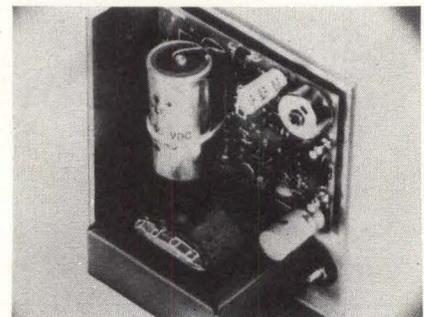
ROM; whole word storage results in a natural sounding voice. Storing each word in its own individual memory makes it easy to call up words in the sequence required. Std words includes digits 0 to 9, as well as plus, minus, times, divide, and equal. The unit accepts either binary address or 10 mutually exclusive switch closures for the first 10 numeric words. **Master Specialties Co.**, 1640 Monrovia Ave, Costa Mesa, CA 92627. Circle 224 on Inquiry Card

INTERACTIVE TERMINAL



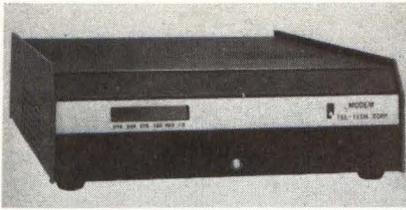
The CDC 751-10 microprocessor-based display terminal is an asynchronous remote terminal controlled by an Intel 8080 microprocessor. It displays 1920 char of data in a 24-line x 80-char format. Characters are formed in a 7 x 9 dot matrix pattern. Terminal displays a complement of 128 char, including 95 ASCII char and ASCII representation of 33 control codes. Character and control code keys are arranged in a typewriter-style layout on a detachable keyboard, which can be located up to 2 ft from the display. **Control Data Corp.**, PO Box O, Minneapolis, MN 55440. Circle 225 on Inquiry Card

DC POWER SUPPLIES



HAPS series models are offered with outputs of 150 Vdc at 0.150 A; 180 Vdc at 0.150 A; 200 Vdc at 0.125 A; and 250 Vdc at 0.1 A. Hermetically sealed IC regulators and integrated Darlington transistor driver stages provide reliability. Electrostatically shielded isolation type transformers used with a high frequency bypass capacitor filter circuit reduce feedthrough of high frequency transients better than 4:1. All models operate on universal inputs of 115/230 Vac ($\pm 10\%$), 47 to 440 Hz (derated 10% at 50 Hz). **Adtech Power, Inc.**, 1621 S Sinclair St, Anaheim, CA 92806. Circle 226 on Inquiry Card

LIMITED DISTANCE MODEM



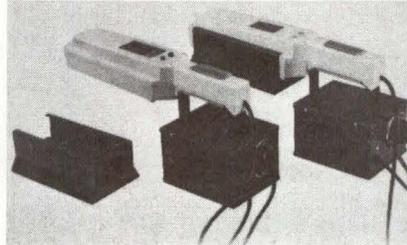
The LDM-7296 data set provides economical data transmission over limited distances on unconditioned, nonloaded wire pairs. Modem transmits and receives nonsynchronous serial data at rates from 0 to 9600 bits/s, and synchronous data at 1800, 2400, 3600, 4800, 7200, or 9600 bits/s. It operates simplex or half-duplex on a single pair, or full-duplex on two pairs. All circuitry is contained on a single PC card which may be integrated into terminal or other equipment. **Syntech Corp.**, 11810 Parklawn Dr, Rockville, MD 20852.
Circle 227 on Inquiry Card

UNIVERSAL PRODUCT CODE READ HEAD

Measuring grocery industry's UPC at the press of a button, automatic read head is designed as an accessory to the firm's UPC verifier. The V322-5 Check Mate increases accuracy from ± 5 to $\pm 3\%$. Head scans the code at a controlled speed and constant tilt angle, eliminating any variables asso-

ciated with hand-held code pen scanning. Output is fed directly into the UPC verifier, which translates lines and spaces into readable Arabic numeral display. It then indicates how much wider or narrower from perfect the bars of the 12 characters are. **Skan-A-Matic Corp.**, PO Box S, Elbridge, NY 13060.
Circle 228 on Inquiry Card

EPROM ERASING SYSTEM



UV lamps for erasing p/ROMs offer short wave capability which shortens erasure time to minutes. S-52T, featuring timer assembly and holding tray, will erase up to 16 chips in about 7 min. UVS-54T also includes timer assembly and holding tray, and provides complete erasure for up to 8 chips in about 14 min. Housed in rugged lightweight CYCOLAC[®] for portability, the units are available in 115- or 220-V versions. **Ultra-Violet Products, Inc.**, 5100 Walnut Grove Ave, San Gabriel, CA 91778.
Circle 229 on Inquiry Card

D-A CONVERTER

High performance, 15-bit, four quadrant multiplying converter, DAC-M features low feed-through capacitance. Unit is an encapsulated module that measures 2.625 x 3.125 x 0.42" and weighs 5 oz. All interfaces are DTL or TTL compatible. Designed for use in X-Y plotters, character generators, programmed pulse generators, and meter drive circuits, device meets MIL-STD-202D, making it suitable for military and aerospace applications. Converters are available in accuracy grades between ± 0.024 and $\pm 0.0031\%$. **ILC Data Device Corp.**, Airport International Plaza, Bohemia, NY 11716.
Circle 230 on Inquiry Card

LOW PROFILE 6-POLE RELAY

Lightweight, 6 Form C relay permits PC board spacing on 0.6" (1.54 cm) centers and accepts drive directly from logic ICs. The 6-pole T10 is available in coil voltages of 6, 12, 24, and 48 Vdc having permissive-make contacts rated 0.1 to 3 A at 28 Vdc or 120 Vac resistive, or bifurcated contacts rated low level to 1 A at 60 Vdc or 120 Vac resistive. This arrangement gives long operating life due to minimal contact bounce. Life expectancy is 50M operations min mechanical, 50K at full load. **Potter & Brumfield Div, AMF Inc.**, 200 Richard Creek Dr, Princeton, IN 47671.
Circle 231 on Inquiry Card

THE HOT NEW S-D MICROPROCESSOR ANALYZER

ONLY \$865 but Model 50 does more than a 32-channel logic analyzer costing 3 times as much.

First Universal Analyzer: Useable with all microprocessor families that have accessible bus structure.

Display: 16 bits of data and 16 bits of address.

Unique Search Modes: Identify the first and last instruction in a program loop, then step forward or backward through programs.

Passive or Interactive: Use as a passive real time monitor.

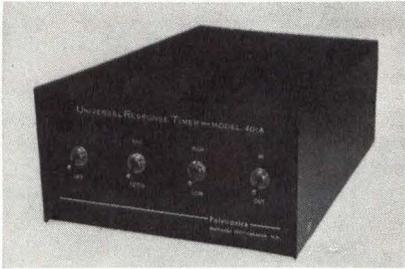
Find out more about the time-saving (to put it mildly) Model 50 features such as delay by loops, single step, dual clock, N-1/N+1 strobe, multiple unit capability, etc. Contact:

SYSTRON  DONNER

10 Systron Drive • Concord, CA 94518 • Phone (415) 676-5000

PRODUCTS

UNIVERSAL RESPONSE TIMER



A low cost system for computerizing reaction-response measurements, model 401A measures $3\frac{1}{4} \times 5\frac{5}{8} \times 10\frac{1}{4}$ " and requires approximately 10 W, 110 V, 60 Hz. Most common timesharing terminals with an RS-232 interface can be used to present stimuli; responses can be made with either switch closures or the terminal keyboard. Keyboard responses are limited to a single character. Complete external control of the timer is provided on the accessory jack. Timer can be operated without a computer, using a terminal to print out responses and times. **Polytronics**, Methodist Hill, Lebanon, NH 03766.

Circle 232 on Inquiry Card

FLAT RIBBON CABLES WITH CONNECTORS

Great Jumpers™ and Great Daisy Jumpers™ are fully assembled and pretested cables with connectors. Great Jumpers are available in widths of 20, 26, 34, 40, and 50 conductors. Connectors—card edge, PC board, and socket—are molded directly onto the vinyl ribbon cable with integral molded strain reliefs and complete line-by-line probeability. Flat vinyl cable is available in electric pink with solid or stranded #28 AWG conductors, and connectors on either or both ends. Great Daisy Jumpers are the daisy-chain version of Great Jumpers. **AP Products Inc.**, Box 110, 72 Corwin Dr, Painesville, OH 44077. Circle 233 on Inquiry Card

INCANDESCENT ALPHANUMERIC DISPLAY

A directly viewed 16-segment display with $\frac{5}{16}$ " char height, model 0-64 offers 9K ft-L of light output providing contrast ratios of up to 7 to 1, filtered, in 10K ft-cd of ambient light. Device comes in a miniature 0.312 D x 0.406 H x 0.375" W package. Drawing only 17 mA per segment, it can be ac or dc driven, and lends itself to most multiplexing circuits. Accessories for the 4-V device are a connector and decoder/driver. **Refac Electronics Corp.**, PO Box 809, Winsted, CT 06098. Circle 234 on Inquiry Card

PROGRAMMABLE CONTROLLER

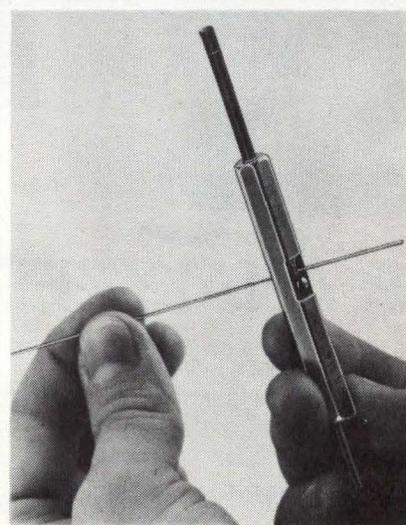
The 8500 allows direct interfacing of mini-computers, terminals, data acquisition equipment, and other nonstandard peripherals to IBM 360/370 computer systems. Unit can connect to the byte multiplexer, block multiplexer, or selector channel; connection of external equipment can be made through current loop, RS-232-C asynchronous and synchronous serial interfaces, or high speed parallel interfaces. Basic unit includes IBM channel adapter, 16-bit parallel processor, diskette drive, system control panel, and maintenance panel. **Austron Inc.**, 1915 Kramer Lane, Austin, TX 78758. Circle 235 on Inquiry Card

AUTOMATIC LOGIC TEST SYSTEM

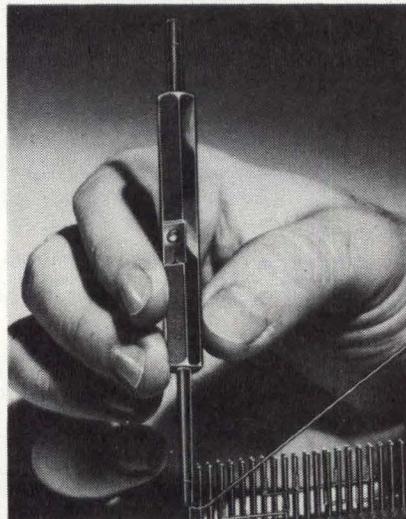
Suitable for testing high speed logic circuits such as Schottky TTL, as well as circuits demanding low capacitance such as CMOS, the MB2410 system features a test head adapter identical to that of the larger MB2420 and MB2460 systems with very short path lengths. Test programs are fully compatible with the other two systems, and programs generated using the company's FLASH logic simulation software on the larger systems can also be run on the MB2410. System runs from an internal 10-MHz crystal clock. **Membrain Ltd.**, Ferndown Industrial Estate, Wimborne, Dorset, BH21 7PG England. Circle 236 on Inquiry Card

IN WIRE-WRAPPING HAS THE LINE...

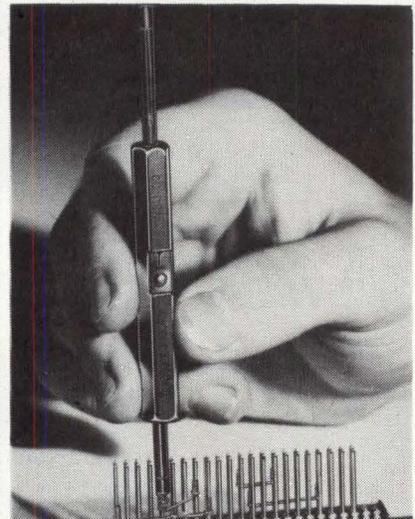
HOBBY-WRAP-30



STRIP



WRAP



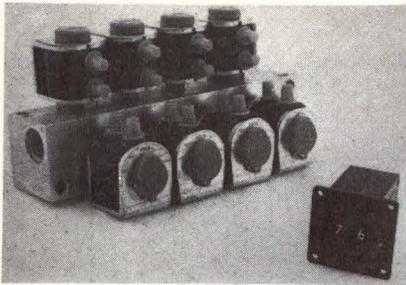
UNWRAP

OK MACHINE & TOOL CORPORATION

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TELEX: 125091 TELEX: 232395

REMOTE BCD VALVE

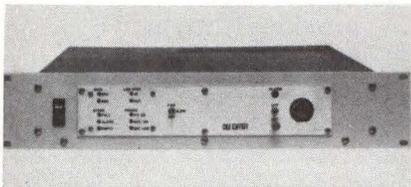


Valve remotely controls small flows of liquid or gas. BCD input command to the valve is generated by a 2-digit thumbwheel switch which allows the valve to be manually set to any of 100 discrete settings, ranging from bubble tight "00" to full flow "99". Each setting activates a combination of 120-Vac ASCO™ solenoid actuators which control flow through individual BCD weighted metering orifices. Measuring 11.4 x 11.4 x 26 cm (4½ x 4½ x 10¼"), it may be located in any position. **Digital Dynamics, Inc.**, 830 E Evelyn Ave, Suite A, Sunnyvale, CA 94086. Circle 237 on Inquiry Card

DIGITAL FACSIMILE SYSTEM

Capable of handling both ASCII and compressed digital facsimile signals over 3-kHz lines, system consists of the company's digital facsimile recorder and digitizer at the receive terminal and a digital scanner and digitizer at the transmit terminal. Available in 11- or 18-in. versions, it also may be interfaced with a computer, TTY keyboard, or floppy disc. Receive terminal receives ASCII signal at rates from 1200 to 9600 bits/s. **Alden Electronic and Impulse Recording Equipment Co, Inc.**, Alden Research Ctr, Westboro, MA 01581. Circle 238 on Inquiry Card

DATA BUFFER CONTROLLER

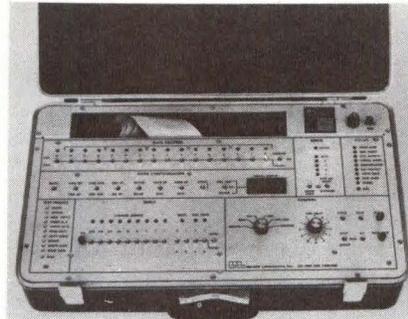


Microprocessor-controlled model 850-B provides temporary storage of up to 61K char of serial asynchronous data. The logic unit can be programmed to provide integral functions such as dual data buffering, selective calling or dial-up terminal operation, and speed or code conversion processing. A backup battery prevents data loss on power failure. Data connections are EIA RS-232-C or neutral loop operating full- or half-duplex, 5- or 8-level at 50 to 4800 baud. Indicators provide send and receive data status, store full/empty, ac power on, and aural alarm disabled. **Nu Data Corp.**, 32 Fairview Ave, Little Silver, NJ 07739. Circle 239 on Inquiry Card

LOW PROFILE DIP SOCKET

Designed for high density packaging, the ICL DIP socket has a 26% lower profile (only 0.15" high) to cut packaging space. Other features are 0.100" lead progression for max board density, high vibration resistance, and self-lock leads for high speed automatic production. Its R-N "side-wipe" single leaf contacts are reliable and it is available with from 8 to 40 leads. **Robinson-Nugent**, 800 E Eighth St, New Albany, IN 47150. Circle 240 on Inquiry Card

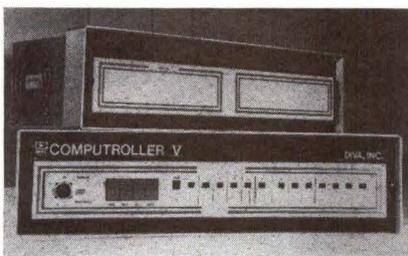
DISC EXERCISER



Performing a series of switch-selectable tests ranging from simple restore operations through complex data exercises on 2315-type disc drives such as Wangco, Pertec, and Diablo, the DX-1000 disc exerciser includes restore, seek, seek incrementing, decrement seek, increment or decrement up or down the disc, and random patterns of incrementing. Digital read-out of seek time in milliseconds, rpm in seconds, and sector count provides assurance that the disc drive is within specs. **Wilson Laboratories, Inc.**, 2536-D E Fender Ave, Fullerton, CA 92631. Circle 241 on Inquiry Card

INTELLIGENT DISC CONTROLLER

Computroller V uses a microprocessor and a ROM-resident emulator program to obtain software compatibility and transparency with respect to DEC PDP-11, Interdata, and Data General Nova and Eclipse minicomputer operating systems. Responding to code written for the vendor's own disc peripheral, it requires no special I/O driver. Other features include automatic ECC, data, and header, within controller; automatic retry algorithm; and 1.33M-byte/s max sustained burst rate. **Diva, Inc.**, 607 Industrial Way W, Eatontown, NJ 07724.



Circle 242 on Inquiry Card



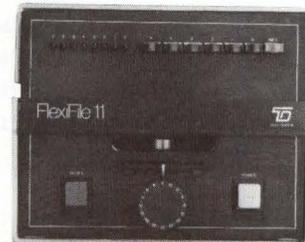
Introducing The FlexiFile Family From Tri-Data... FlexiFile 10



...requires

NO software modification in your present system. Tri Data provides an RS-232 coupler for data communications interface. So you can replace your data set or terminal. Connected between the terminal and modem, the FlexiFile 10 can serve as a recording device for both units. And you can replace high speed paper tape . . . 816 feet per single floppy disk.

FlexiFile 11



is user-defined. It's as easy as pushing the reset switch. 8 LED'S indicate each operating mode. 6 input switches let you determine the operating mode . . . using your own protocols, control words, and commands. The FlexiFile 11 is Microprocessor Controlled and floppy disk based. Our fully modular interfaces include an RS 232 coupler, and IEEE-488 Instrumentation Bus, and an 8' Bit Parallel Bus.

Complete program loading and on-line storage. Stand alone or rack mount options.



Tri-Data
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Mountain View, Ca.
94043
415-969-3700

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TWX: 910-379-6978

PRODUCTS

PRINTER FOR MICROPROCESSORS



For use with microprocessor development systems, printer operates at speeds which make it possible to reduce 3 h of TTY operation to <5 min. of output time. Std printer has 80 print columns and will print at speeds up to 2400 lines/min. A 132-col version is available which can print at speeds up to 1400 lines/min. Line-to-line spacing is 6/in.; column-to-column spacing is 10/in. Interface signals have been arranged to allow ease of interfacing with most microprocessor systems. **Houston Instrument**, One Houston Sq, Austin, TX 78753.

Circle 243 on Inquiry Card

REED RELAY

Redesigned type D Multireed[®] relays can be used in scanner/multiplexers of both 2-wire "flying capacitor" and 3-wire guarded types. Design meets the operating characteristics of typ data acquisition systems. Life of low distortion relay is considerably greater than that for dry reed relays, and about the same as that for mercury-wetted contact relays. Thermal and dynamic noise levels are lower than in the other two types. Relays are suitable for high density packaging on PC boards. **Thermosen, Inc.**, 375 Fairfield Ave, Stamford, CT 06904.

Circle 244 on Inquiry Card

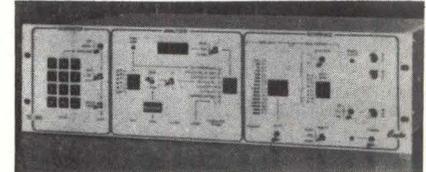
DATA LOGGER

The low power, multichannel analog input logger weighs 3 lb and measures 3.8 x 4.5 x 7.0". Model 221 features a true incremental method of recording data on std Philips cassettes. One to 16 channels of



analog information at a 0- to 10-V level may be multiplexed, converted to digital data, buffered, and clocked onto a cassette tape at rates up to 100 bits/s. Recording format is complementary NRZ and recording density is 615 bits/in. Unit is CMOS throughout, and requires only 85 mA when recording. **Memodyne Corp.**, 385 Elliot St, Newton Upper Falls, MA 02164.

COMMUNICATION TEST SET



TC-100 is a microprogrammed data communications test set for use in tech control systems or as a portable testing device. It can simulate and test all components of the network, including both hardware and software. Entire unit is contained in just 5 1/4" of rack panel space. Three functional units—generator, analyzer, and interface—together with keyboard entry, digital display, and clearly labeled controls, provide operator ease and convenience. **Cooke Engineering Div, Dynatech Laboratories, Inc.**, 900 Slaters Lane, Alexandria, VA 22314.

Circle 246 on Inquiry Card

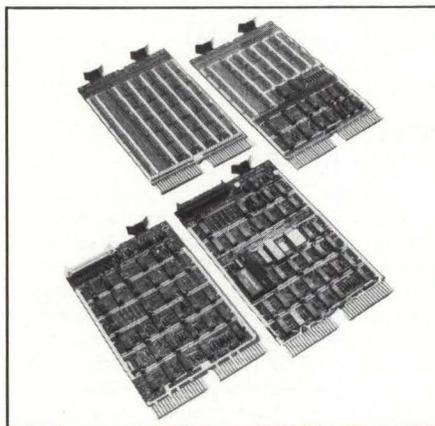
MDB SYSTEMS presents... The LSI-11 Connection

GP Logic Modules • Peripheral Controllers • Communications • Interfaces • Special Purpose Modules • Accessory Hardware

Plus: DEC's own LSI-11 Microprocessor Module. MDB Systems products always equal and usually exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are software and diagnostic transparent to the host computer. MDB products are competitively priced; delivery is usually within 14 days ARO or sooner.

Here are some MDB Systems connections to LSI-11 microprocessors:

- General Purpose Controllers:
 - Serial for TTY, displays, communications
 - Parallel for programmed I/O and DMA
 - Do-it-yourself dual and quad wirewrap for any



DIP design

- Device Controllers for most major manufacturer's
 - Printers
 - Card equipment
 - Paper tape equipment
 - Plotters
- Communications/Terminal Modules
 - Asynchronous Serial Line Interface
 - Synchronous Serial Line Interface

- MDB Backplane/Card Guide Assembly
 - MDB's is a *real* chassis, accepts eight quad modules
- Special Purpose Modules and Accessories
 - System monitoring unit provides front panel Switch addressing
 - Power on/off sequencing
 - Bus extenders/terminators
 - E-PROM and PROM modules
 - Bus connectors for backplane assemblies

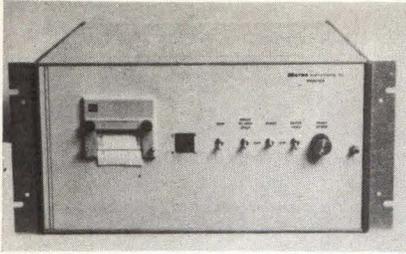
Check first with MDB Systems for your LSI-11 interface requirements.

MDB also supplies interface modules for DEC PCP-11, Data General NOVA, and Interdata minicomputers.

MDB
MDB SYSTEMS, INC.

1995 N. Batavia St., Orange, California 92665
714/998-6900 TWX: 910-593-1339

ANNUNCIATOR WITH PRINTED OUTPUT



The Metranunciator CRT display with remote scanning capability is now available with printer which outputs alarms sequentially. Plain language printout consists of time, legend, and condition: onset of alarm condition, acknowledgement, or clear of alarm. Complete unit is available with std ISA annunciation sequences (including first-out) and duplicate displays on slave CRTs. Inputs from contact closures (N.O. or N.C.) are wired to terminal blocks in the chassis. Cables bring signals to CRT and/or printer. **Metra Instruments, Inc.**, 1161 San Antonio Rd, Mountain View, CA 94043.
Circle 247 on Inquiry Card

HIGH SPEED TERMINAL

The LX1010 has print speed of 180 char/s and uses a microprocessor to provide compatible communication with all computer protocols, codes, and modes. Interactive terminal can communicate in ASCII, BCD, or Telex codes, at speeds from 75 to 4800 baud, both synchronously and asynchronously. This allows it to be used for ASCII time-sharing at 1200 baud; then changed for use as a 2741, with or without APL, or as a 3767 in SDLC protocol. **LogAbax, U. S. Div.**, 10889 Wilshire Blvd, Los Angeles, CA 90024.
Circle 248 on Inquiry Card

COUNTER/SEQUENCER



MTS-6400, incorporating an 8080-type microprocessor, allows users to arbitrarily set start/stop times for each of 64 channels. Channel and start/stop time data are displayed on three groups of 7-segment readouts. Each of 64 channels has individual output line for connection to an external device. Outputs will sink up to 150 mA at 30 Vdc—enough to drive relay loads. System time base may be programmed via the keyboard. Increments from 1 count/ms to 1 count/hr can be selected by the user. Time values may be up to six digits long. **Heurikon Corp.**, 700 W Badger Rd, Madison, WI 53713.
Circle 249 on Inquiry Card

64-BIT SHIFT REGISTER

The SR-64P module is used with indexing conveyors and rotary indexing tables to sense faulty or missing parts (or other inputs) at one location on the conveyor and then reject the part (or other output) at a preset location further down the conveyor. Inputs may be limit switches, 3-wire proximity and photoelectric sensors, or outputs from other logic modules. A "stage selector" allows selection of up to 64 stages in the indexing system between the input and output functions. Modules may be cascaded for additional stages. **Banner Engineering Corp.**, 9714 10th Ave N, Minneapolis, MN 55441.
Circle 250 on Inquiry Card

ALTERNATE ACTION PUSHBUTTON SWITCH

An illuminated dpdt switch that meets all MIL-S-22885/18-02 requirements, the J20145 is environmentally sealed and shock and vibration resistant. Temp range is -55 to 85°C. The switch maintains stable contact resistance throughout its lifetime, especially at min current as specified in the spec. It is rated at 28 Vdc or 115 Vac, 2 A resistive, 1.5 A inductive, and 0.5 A lamp load. Operating force is 2 ±1 lb with a max 0.160" plunger travel. **Control Switch, a Cutler-Hammer Co.**, 1420 Delmar Dr, Folcroft, PA 19032.
Circle 251 on Inquiry Card

DC-DC POWER SUPPLY MODULE

The P series is a single output 25-W low noise, isolated-regulated dc-dc converter module. Std input power levels of 12, 24, or 48 Vdc are available for output ratings of 5 Vdc, 5 A; 6 V, 4 A; 8 V, 3 A; 12 V, 2 A; or 15 V, 1.6 A. Regulation is ±0.2% max. Output setting accuracy is ±0.5% typ. Average voltage tempo is ±0.01%/°C; stability is ±0.05%/24 h. Sense leads also are provided. Self-contained module has four 4-40 flush mounting inserts to mount the 24-in.² bottom surface to a heat sink. **Stevens-Arnold, Inc.**, 7 Elkins St. South Boston, MA 02127.
Circle 252 on Inquiry Card

U/LC CHARACTER SET FOR DISPLAY TERMINAL

Available on TeleComputer II CRT display terminal, u/lc option enhances readability. Compatibility with teletypewriters and time-sharing systems is maintained by incorporation of convenient keyboard switch that permits user to select uc-only operations. A Teletype-compatible computer terminal that uses any size TV monitor for visual output and up to 10 different monitors at the same time, the portable, briefcase-packaged unit includes 5" CRT display, terminal, and acoustic coupler. **Digi-Log Systems, Inc.**, Babylon Rd, Horsham, PA 19044.
Circle 253 on Inquiry Card

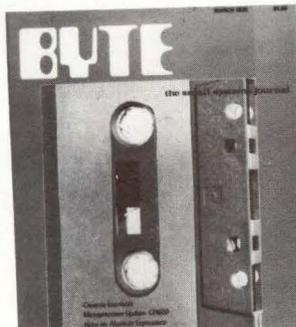
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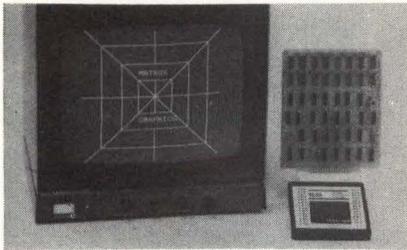
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PRODUCTS

GRAPHIC DISPLAY



MTX-256**2 displays 65,536 dots arranged in a 256 x 256 dot raster with each dot individually addressed in less than 3.4 μ s. System consists of two modules. Central timing unit module provides all TV sync signals and interface timing signals for any microprocessor and for image memory module; image memory is a 65,536-bit RAM, which stores one TV field (256 x 256) with one level of intensity (no external refresh required). Memory is continuously scanned to produce a video signal that drives any std monochrome or color TV monitor directly. **Matrox Electronic Systems**, PO Box 56, Ahuntsic Sta, Montreal, Quebec H3L 2S0 Canada. Circle 254 on Inquiry Card

ASYNCHRONOUS MULTIPLEXER BOARD

Eight asynchronous communication I/O channels, line printer controller, and real-time clock on a single PC board, the Multiplexer allows installation of up to 64 asynchronous channels in one Data General processor. Each channel is RS-232-C compatible and interfaces to local terminals or data set in half- or full-duplex operation. Eight different baud rates, from 110 to 9600, are jumper-selectable. Real-time clock operating under program control provides crystal-controlled interrupts of 1 kHz, 100 and 60 Hz. **STC Systems, Inc, OEM Products Group**, 9 Brook Ave, Maywood, NJ 07607. Circle 255 on Inquiry Card

ROTARY VISCOUS DAMPER

Simple in design and completely self-contained in a sealed, tamper-proof 2 1/4" dia 1 1/16" envelope, damper P/N 312554 provides vibration damping, speed control, deceleration, tensioning, and similar functions. It is self-lubricating, requires no maintenance, and combines proven reliability with long service life. Angular travel is a full 360 deg, bidirectional. Breakout torque is 3.0 in.-lb max. Torque at 50 rpm is 6.5 in.-lb max, and at 300 rpm, 8.5 in.-lb min. **Houdaille Hydraulics**, 537 E Delavan Ave, Buffalo, NY 14211. Circle 256 on Inquiry Card

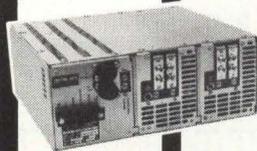
PERIPHERAL EQUIPMENT ADAPTER

Designed as an economic approach to increasing capabilities of existing CRT display units and keyboard printers, the adapter allows up to three terminal devices, with either EIA-voltage or 20-mA current loop electrical interface to be connected to a single EIA-compatible port, modem, or multiplexer channel. When the unit is not online with the computer, it automatically interconnects the terminals for offline preparation or transcribing of data. **United Data Services Co, Inc**, 3024 N 33rd Dr, 103, Phoenix, AZ 85017. Circle 257 on Inquiry Card

LED/PHOTODIODE FIBER OPTIC LINK

MDL100 series comprise simple flexible fiberoptic data links with high speed IR LED transmitters and pin photodiodes as receivers. LED and photodiodes are mounted in 3-terminal TO-5 headers. Devices are isolated from case ground for flexibility in design of driver and amplifier processing circuits. Modules are sealed into SMA or BNC connectors for direct coupling of multifiber cables with min insertion loss. -124 uses an L2 LED with D2 photodiode and operates from dc to 4 MHz in either analog or digital mode. **Meret Inc**, 1815-24th St, Santa Monica, CA 90404. Circle 258 on Inquiry Card

OEM DESIGNERS Get this FREE Design File on CDC's new modular switching power supplies

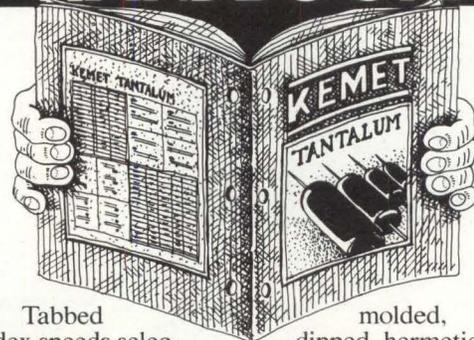


These compact, modular power supply switchers simplify design in 300-600 watt applications and keep costs down too. (They're priced at less than 90¢ per watt!) Benefits to the end user include **low EMI noise levels** (we are designed to meet VDE STD 0875) and **highly reliable operation** plus convenient maintenance and easy add-on capability up to 1200 watts in a single, 19 in. rack. Get specs, prices and feature details today from:

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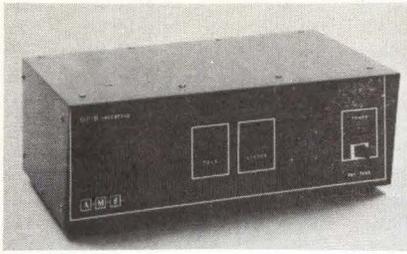
molded, dipped, hermetic. Axial or radial leads. Polar and non-polar. Chips, too. Send for your free copy. Components Department. Union Carbide Corporation, Box 5928, Greenville, SC 29606.



COMPONENTS DEPARTMENT

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ANALOG-DIGITAL INTERFACES



Two IEEE-488 GPIB (HPIB) interfaces are compatible with Tektronix 4051, H-P 9825 and 9803, and Wang 2200 systems. Model 704 combines eight analog inputs with seven BCD digits of input and output. Sampling rate, channel number, and self-scan operation are programmable. An internal clock provides 12 sampling rates from 1 to 4000/s. Input range is adjustable from ± 1 to ± 10 V full scale. Four output trigger pulses are also provided. Model 703 is a digital-only interface with 10 BCD inputs, 12 BCD outputs, and four triggers. Both have interrupt and serial polling capability. **AMS, Inc.**, PO Box 873, Lake Elmo, MN 55042.

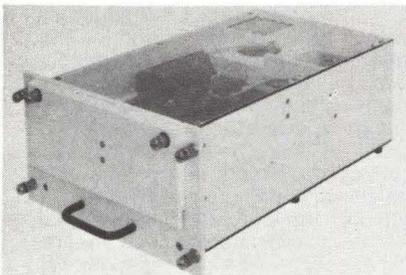
Circle 259 on Inquiry Card

PRIVATE LINE INTERFACE UNIT

Type L550A channel service unit provides interface facilities to the digital data system (DDS) network at the local loop level. Located at the subscriber's premises, the unit conditions the data terminal equipment signal for transmission over private line metallic circuits to the DDS central office. It provides level adjustment, equalization, and circuit protection, and is intended for use with equipment that supplies a bipolar, return-to-zero interface signal. **GTE Lenkurt Inc.**, Dept C720, 1105 County Rd, San Carlos, CA 94070.

Circle 260 on Inquiry Card

MILITARIZED FLEXIBLE DISC DRIVE



MIL-E-16400 compatible DD-400 provides 3M bits of online random-access storage on interchangeable floppy disc media. Each diskette provides 77 data tracks with 3200 bits/in. data packing, establishing media compatibility with the IBM 3740. Data can be transferred at a peak rate of 2.5×10^6 bits/s. Drive provides fully militarized and ruggedized memory unit with MTBF in excess of 5000 h. **Miltope Corp.**, 532 Broad Hollow Rd, Melville, NY 11746.

Circle 261 on Inquiry Card

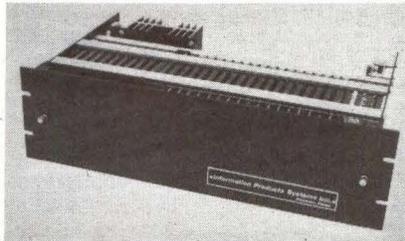
DIGITAL STEPPER

Motor provides resolutions of either 2000 steps (0.18 deg) or 4000 steps (0.09 deg) per revolution. Measuring 3.55" in diameter and 3.06" in length, NuSyn 2.75-250-1-8 handles up to 55 in.-lb of torque (880 in.-oz) at a speed of 4500 steps/s with significant torque remaining at higher speeds. Slew speeds range from 7K to 10K steps/s depending on the step angle selected. Resolution and accuracy provide true open loop operation. **Mesur-Matic Electronics Corp.**, 50 Grove St, Salem, MA 01970.

Circle 262 on Inquiry Card

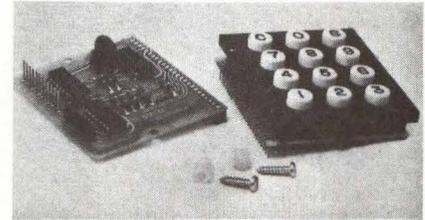
MAGNETIC TAPE FORMATTERS

Model 1700 series IBM and ANSI std formatters feature 90% low power Schottky to achieve less than 12.5-W power consumption in NRZI/PE dual-speed, dual-density units. NRZI consumes 5 W. Formatters provide for external control allowing synchronizing of an external event to the data



R/W operation, and provide a deep data deskew register for superior data recovery from marginal PE mag tape. Postamble detection circuits eliminate premature terminations when reading long PE data records. **Information Products Systems, Inc.**, 6565 Rookin, Houston, TX 77074.

KEYBOARD ADDER BOARD



Optional plug-on adder boards, containing BCD encoding or other signal processing circuitry, feature compact packaging to minimize behind the panel space. Keyboards are available with unlighted opaque keybuttons or with LEDs mounted in attractive transparent colored keybuttons for full illumination. They provide positive visual indication of function status or data acceptance. Easy to read keytop markings or decorative decals are color-coordinated to complement keyboard appearance. **Stacoswitch, Inc.**, 1139 Baker St, Costa Mesa, CA 92626.

Circle 264 on Inquiry Card

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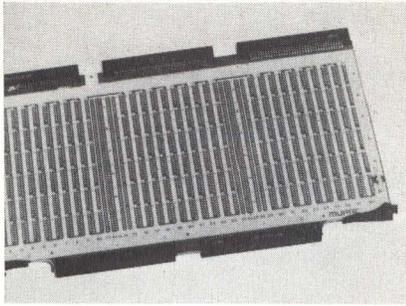


Computer Operations, Inc.

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(301) 459-2100 TELEX 89-8327

PRODUCTS

HIGH DENSITY WIREWRAP PANELS



Panels handle up to 200 ICs of any mix of 14/16/18/22/24/28/36/40/42-pin packages. High I/O provisions of up to 540 pins permit flexibility of subdividing logic requirements without sacrificing electrical or mechanical integrity. In addition, multiple voltage planes (V1, V2, and gnd) enable panels to be used for prototyping of microprocessors, RAMs, ROMs, and other MSI/LSI ICs. The 326 series panels may be mounted in conventional modular rack assemblies with multiple voltage connector power planes, or on planar frames with ribbon cable I/O provisions. **Mupac Corp.**, 646 Summer St, Brockton, MA 02402. Circle 265 on Inquiry Card

COMPUTER POWER CENTER

A mobile, flexible unit designed to allow computer systems to be quickly and easily installed, relocated, or reconfigured without high labor costs, the computer power center accepts raw building power, transforms it into the computers' voltage requirements, and distributes the power to the system's individual components and peripherals. Installation requires only that building power be connected to a junction box; the device's input cable is plugged into the box, and the computer is plugged into the center. **Computer Power Systems Corp.**, 3303 Harbor Blvd, Bldg H-5, Costa Mesa, CA 92626. Circle 266 on Inquiry Card

MICROPROCESSOR INTERFACE PRODUCTS

Interface and logic modules for DEC LSI-11 microprocessor include g-p 1710 GPIO and 11B DMA controller and WWB1 and 11WWB dual and quad wirewrap modules. I/O modules are LP11 line printer, CR11 card reader, and PC11 paper tape reader/punch controllers. Communications modules include DLV11 asynchronous and DUV11 synchronous serial line interfaces. Accessory hardware consists of BPA84 version of DEC's backplane card guide assembly, with double the capacity. **MDB Systems, Inc.**, 1995 N Batavia St, Orange, CA 92665. Circle 267 on Inquiry Card

PROGRAMMABLE GRAPHICS DISPLAY SYSTEM

Combining high speed display data processing and fast access MOS RAM refresh memories with the ability to perform automatic block transfers via DMA, the expandable GCT-3000 series meets both simple and complex display requirements. Based on the -3011 programmable graphic processor, the system features 256 x 256 to 1024 x 1024 resolution range; bit map type refresh, expandable from 1 to 16 bits/picture element; and refresh memory read-back. **Genisco Computers, a div of Genisco Technology Corp.**, 17805-D Sky Park Circle Dr, Irvine, CA 92714. Circle 268 on Inquiry Card

STONE DECODER MODULE

BDI 800 meets or exceeds telephone company requirements for dynamic range, twist, detection time, and talk-off sensitivity. It detects all 16 Touch Tone[®] codes and provides data storage and buffering. Outputs are available with the data strobe pulse and can be either BCD or 2-of-8 encoded. All outputs are TTL and MOS compatible and can be provided at positive or negative true logic levels. The single card module can be interfaced either by direct connection to telephone line or through any approved interface device. **BDI Electronics-Telecommunications**, PO Box 1416, Mountain View, CA 94042. Circle 269 on Inquiry Card

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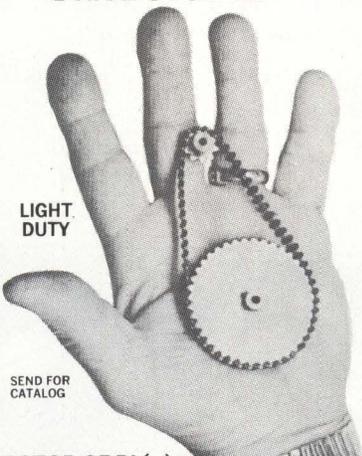
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THE AUTOMATED MULTIPHASIC HEALTH TESTING MARKET

The need for an advanced system to enable physicians to handle physical exams and clerical transactions on a semi-automated basis is potentially a billion dollar market. Presently, larger and more sophisticated multiphasic health testing centers are in limited use throughout the U.S., performing a relatively small number of annual physical examinations.

Frost & Sullivan has completed a 200-page report which analyzes and projects over the next ten years the market for automated multiphasic health testing systems and determines the potential for the use of an advanced system for physical examinations and clerical transactions (ASPECTS) in physicians' offices. Market forecasts are furnished for the equipment subsystems, supplies and accessories to be used in ASPECT. Various ASPECT configurations are proposed. Factors which will both stimulate and limit the growth of AMHT's and ASPECT are explored. Emphasized are: the prospect for increased annual physical examinations over the next 10-15 years, the ability to handle these increases, and the likely approaches. Responses to a questionnaire survey of physicians, multiphasic health testing operators and suppliers document the results.

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DIL-PACKAGED OSCILLATOR

Low profile crystal TTL 14-pin DIP oscillator measures 0.2 x 0.49 x 0.78". It drives fanout of 10 TTL at any fixed frequency from 4 to 20 MHz with frequency tolerance of $\pm 0.01\%$ from -25 to 75°C , output squarewave with logic 1 greater than or equal to 2.4 V, and logic 0 less than or equal to 0.4 V. **Connor-Winfield Corp.**, West Chicago, IL 60185.
Circle 270 on Inquiry Card

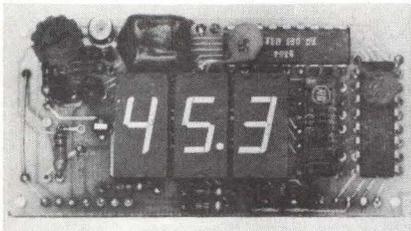
TABLETOP COMPUTER SYSTEM



A compact, disc-based table-top computer system which serves as a standalone replacement for time-share systems and as an independent terminal in networked installations, the 8510 includes DEC LSI-11 micro-computer, 20K words of high speed RAM, flexible disc drive system capable of storing over 256K bytes of data in IBM-compatible format, and both RS-232-C and 20-mA current loop interfaces. Baud rate is switch-selectable from 50 to 19,200. Software support includes disc operating system including Macro assembler, editor, linker, librarian, batch processor, plus BASIC language interpreter and FORTRAN IV compiler. **Terak Corp.**, Box 3078, Scottsdale, AZ 85257.

Circle 271 on Inquiry Card

DIGITAL PANEL METER

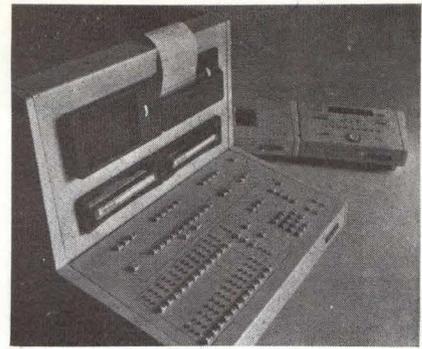


Designed to mount behind the panel by means of four standoff spacers, the model 325 is built on a single PC board (2.9 x 1.4"). LED display is bright orange, 0.4" high, with automatic polarity indication and external decimal point selection. Typ specs are 1000-M Ω impedance, $\pm 0.1\%$ accuracy and linearity, 7-pA typ input bias current, tempo of $\pm 0.005\%/^\circ\text{C}$, and power consumption of 550 mW. Four ranges are available—1, 10, 100, and 1000 Vdc with up to 1200-V overvoltage protection. **International Microtronics Corp.**, 4016 E Tennessee St, Tucson, AZ 85714.

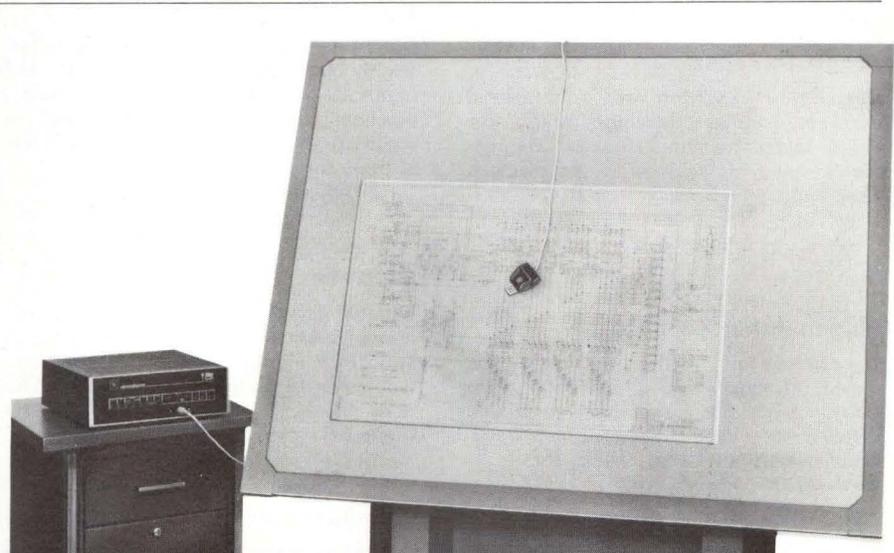
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SEMICONDUCTOR TEST SYSTEM

The J401 TTL IC test system offers test and data-gathering capabilities of large systems, yet permits a device engineer to master programming in about 30 min. System performs functional and dc-parametric testing to data-sheet specs. "Menu programming," an interactive procedure whereby the system continually prompts the operator for information via the CRT display, is used. Format for each test is set up automatically. System consists of communications console, operator's panel, test deck, test package, and power supply. **Teradyne, Inc.**, 183 Essex St, Boston, MA 02111.



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LITERATURE

Machine Tools

Brochure describes economic handbook, a concise compilation of facts and figures about the U.S. machine tool industry and its relationship to national economy and world trade. **National Machine Tool Builders' Association**, McLean, Va.

Circle 300 on Inquiry Card

Miniature Pushbutton/Toggle Switches

Engineering diagrams and dimensional drawings highlight brochure which discusses mechanical and electrical environmental specs of family of toggle switches. **Oak Industries Inc, Switch Div**, Crystal Lake, Ill.

Circle 301 on Inquiry Card

Plug-In Power Supplies

Descriptions of supplies with octal plug mounting/interconnection and options are furnished in full-color bulletin containing detailed specs and illustrated typ applications. **Acopian Corp**, Easton, Pa.

Circle 302 on Inquiry Card

Timing and Control Components

Product guide contains illustrations, condensed specs, and data on full line of motors, switches, relays, thermostats, indicators, and timers. **North American Philips Controls Corp**, Cheshire, Conn.

Circle 303 on Inquiry Card

Multifunction Voltensor

Containing circuit and outline drawings, data sheet discusses features, operation, applications, and specs of model 545, in addition to mounting kit specs and selection guide. **Calex Manufacturing Co, Inc**, Pleasant Hill, Calif.

Circle 304 on Inquiry Card

OCR Machines

As an aid to system planners, nontechnical sketchbook focuses on capabilities and economic applications of optical character recognition machines. **Context Corp**, Burlington, Mass.

Circle 305 on Inquiry Card

Latch Connectors

Through charts, drawings, and diagrams, specs of line of connectors for mass-termination of flat cable are supplied in catalog. **AMP Inc**, Harrisburg, Pa.

Circle 306 on Inquiry Card

Programmable Terminal System

Illustrated brochure covers components, hardware, software, and emulation packages of the PTS-100, as well as the PTS/1200 distributed processing system. **Raytheon Data Systems**, Norwood, Mass.

Circle 307 on Inquiry Card

Training Courses

Describing courses in both software (assembly and higher level languages) and hardware (computers and std peripherals), brochure also furnishes information on facilities and faculty. **Varian Data Machines**, Irvine, Calif.

Circle 308 on Inquiry Card

Switches

Catalog includes photos, line drawings, general information, and specs on over 300 switches, indicator lights, sockets, and custom products. **Chicago Switch, Inc**, Chicago, Ill.

Circle 309 on Inquiry Card

Wire Insulation

Guide presents properties, comparative characteristic charts, and electrical, thermal, mechanical, and fire performance data of Tefzel[®] fluoropolymers as wire insulation. **E. I. du Pont de Nemours & Co, Inc**, Wilmington, Del.

Circle 310 on Inquiry Card

Character Printers

Features, specs, and benefits of the microprocessor-powered WideTrack printer and Sprint Micro 3 family of printers are detailed in illustrated brochure. **Qume**, Hayward, Calif.

Circle 311 on Inquiry Card

Data Communications Modem

Reconditioned, 2400-bit/s modem 3300/24 is discussed in literature which includes description of benefits, applications, and technical and functional information. **International Communications Corp**, Miami, Fla.

Circle 312 on Inquiry Card

4K RAMs

Prepared to help designers select 16-, 18-, or 22-pin RAM devices, study features comparison of factors, with tables, diagrams, and drawings. **Texas Instruments Inc**, Dallas, Tex.

Circle 313 on Inquiry Card

Voltage Regulation

Theory, design, and operation booklet offers information on line voltage regulation problems, solutions, and applications, with comparison chart of specs. **Sola Electric, Div of Sola Basic Industries**, Elk Grove Village, Ill.

Circle 314 on Inquiry Card

I/O Cable

Information, specs, and qualifications of multipair miniature data transmission cable are outlined in data sheet. **Hitemp Wires Div, Addington Laboratories, Inc**, Covina, Calif.

Circle 315 on Inquiry Card

Tape Transports

Users manual contains detailed information for the design, preparation, and installation of an interface for both phase-encoded and nonreturn-to-zero synchronous digital magnetic tape transports. **Pertec Corp, Peripheral Equipment Div**, Chatsworth, Calif.

Circle 316 on Inquiry Card

IC Test System

Brochure details specs and applications of the J401 TTL IC test system and outlines features of its interactive programming technique. **Teradyne, Inc**, Boston, Mass.

Circle 317 on Inquiry Card

Electronic dc Motors

Featuring a quick selection reference of key specs, bulletin includes general information on miniature brushless motors and Hall generators. **Siemens Corp, Power Engineering Div**, Iselin, NJ.

Circle 318 on Inquiry Card

Used Computer Equipment

Use of the multiple listing service for buying and selling equipment is explained in 20-page booklet, and is compared with available alternatives. **Computer Multiple Listing Service**, Fairfax, Va.

Circle 319 on Inquiry Card

Stepper Motors

Electrical, dimensional, and speed/torque data, and typ applications are covered in product information sheet presenting series of 4-phase permanent magnet motors. **ECM Motor Co**, Schaumburg, Ill.

Circle 320 on Inquiry Card

Deflection Amplifier

Features, applications, and general and mechanical specs of the Mark I magnetic X and Y deflection amplifier are listed in data sheet. **CPS, Inc**, Sunnyvale, Calif.

Circle 321 on Inquiry Card

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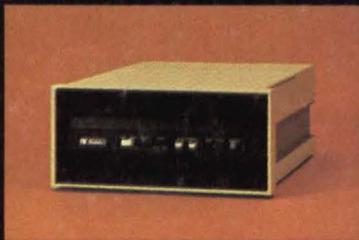
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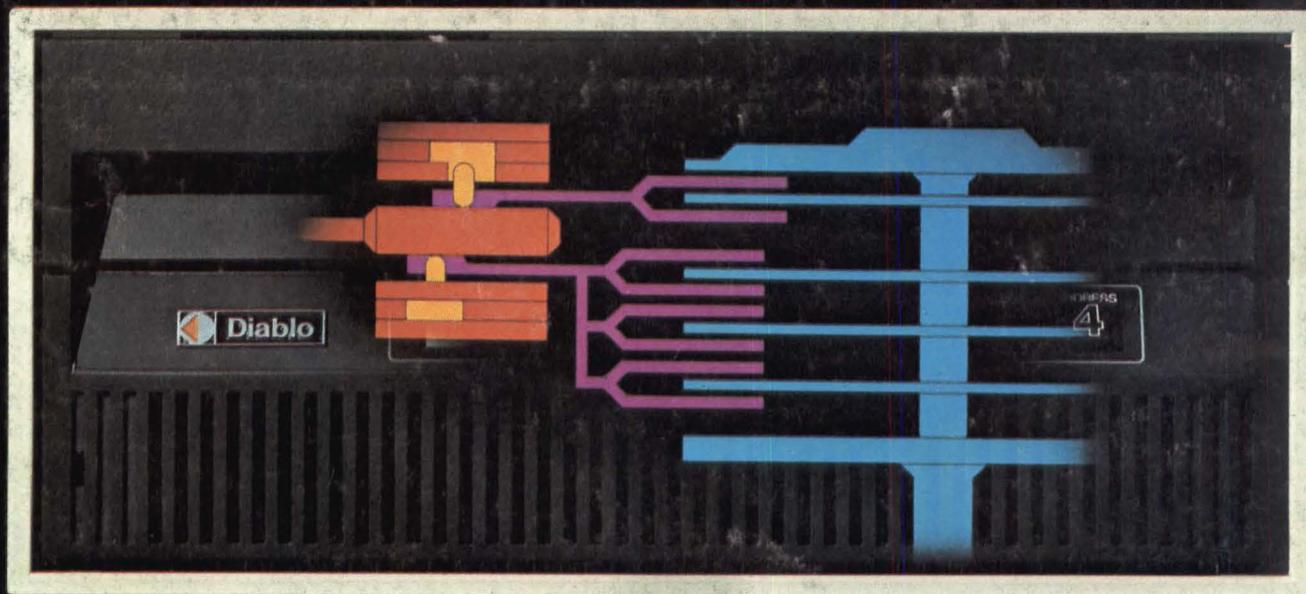
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