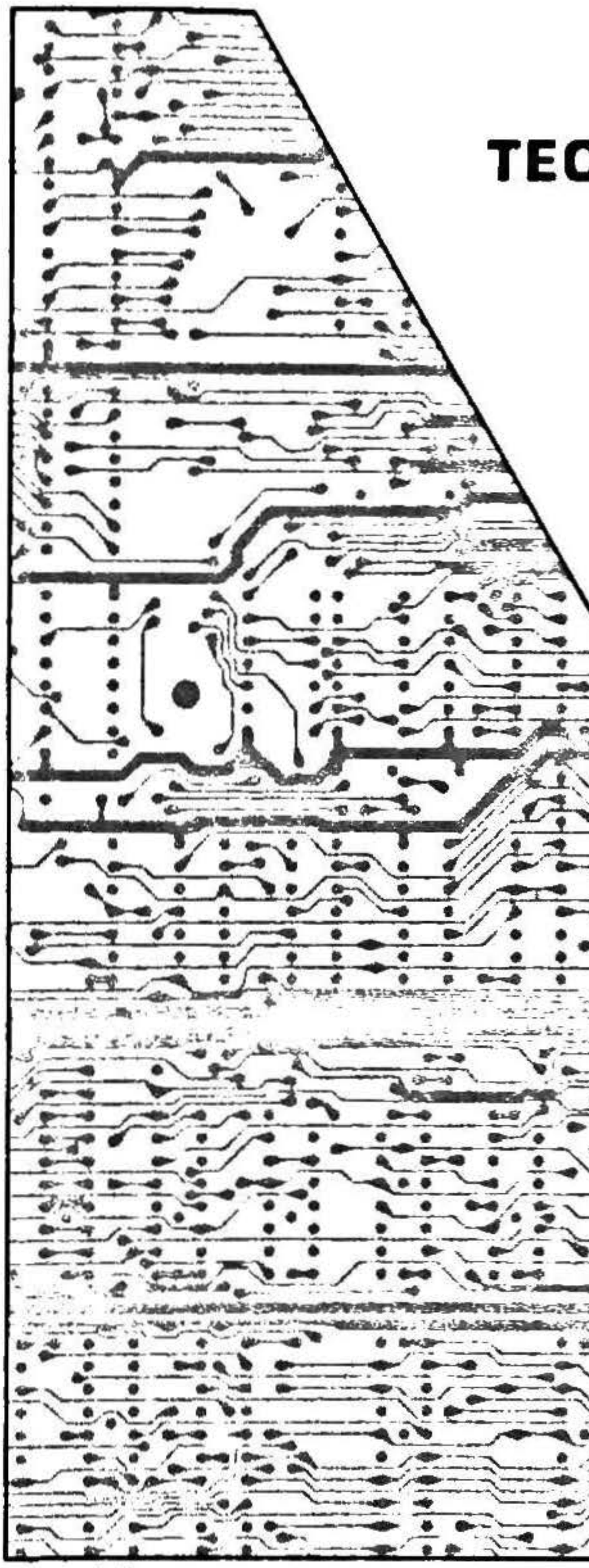
CompuPro™



DISK 1B™
TECHNICAL MANUAL
236A

8261-0101A

December 1986

DISK 1B

TECHNICAL MANUAL

HIGH – PERFORMANCE FLOPPY DISK CONTROLLER
FOR 8" AND 5.25" DRIVES

Preface

This manual describes the features and functions of the DISK 1B[tm] board. It also contains information on how to program the DISK 1B. This is a reference manual for programmers, hardware engineers, and anyone else who needs to understand how the DISK 1B functions in a CompuPro[tm] computer system. It is not a troubleshooting guide or a repair manual.

This manual begins with an overall description of the board and a detailed account of the switch settings. For those seeking more details on the DISK 1B, a functional description follows the switch setting section. Programming considerations, specifications, and schematics are also included.

For those who are interested in getting "up and running" in a hurry, please refer to the software installation guide provided with your operating system.

DISK 1B TECHNICAL MANUAL

Hayward, CA 94545

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Overall Description

The DISK 1B provides an interface between the IEEE 696/S-100 bus and up to four 8" or 5.25" floppy disk drives. Connectors on the DISK 1B supply all the signals necessary to control these drives. Designed for full electrical and mechanical compatibility with the IEEE 696/S-100 bus standard, this board boasts several innovative features including:

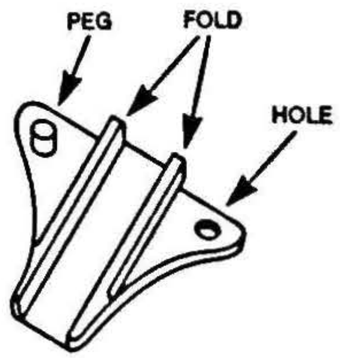
- 24-bit DMA data transfers with the ability to cross 64K boundaries.
- Priority arbitration for the on-board DMA circuitry that will allow up to 16 temporary bus masters to operate without conflict.
- I/O mapped control for uninterrupted memory space.
- An advanced, third generation Floppy Disk Controller (765A or 8272A).
- An advanced digital data separator for reliable data transfers that eliminates adjustments.
- Provision for running both 5.25" and 8" floppy drives at the same time.
- On-board boot EPROM with the capability of supporting many different processor and peripheral boot routines.
- Software selectable floppy data rates to allow support of many drives.

Installing the DISK 1B Board

Basic Installation

Step 1. Unpack the Board.

Along with the board, you will find two card extractors in the plastic bag.



CARD EXTRACTOR

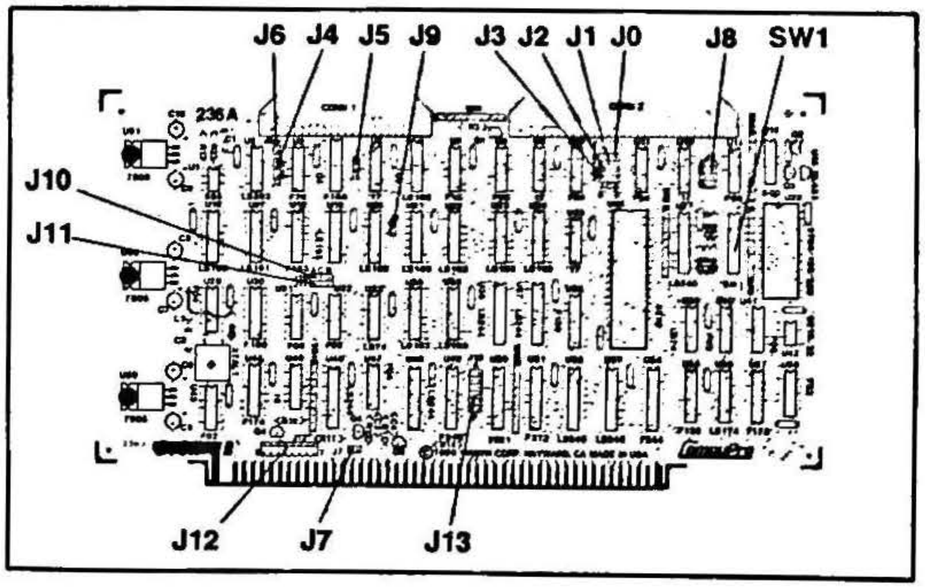
Step 2. Install the Card Extractors.

1. Hold the board so the component side is toward you. (See diagram below.)

2. Insert the peg on the card extractor into the hole in the right corner of the board. Fold the extractor over the board's edge until the extractor's hole snaps over the peg.

   NOTE: Make sure the long edge of the extractor is along the top edge of the board.

3. Repeat for left extractor.



Step 3. Check Switch and Jumper Settings

For standard switch settings for a CompuPro operating system check the operating system Installation Guide. Otherwise, refer to the **Switch Settings** and **Jumper Settings** sections in this manual. The locations of the switch and jumpers on the board are shown in the diagram on the preceding page.

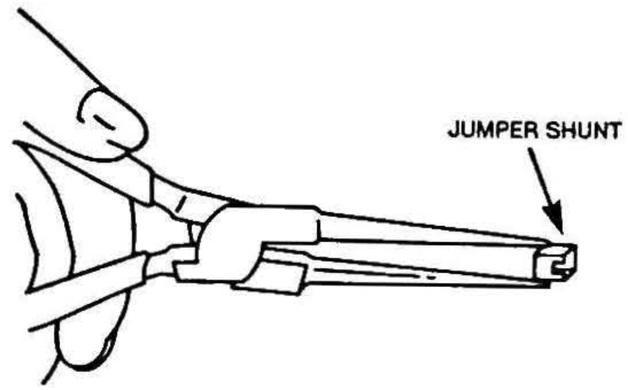
Step 4. How to Install Jumper Shunt Connectors

Jumper Shunts

A jumper shunt is a small plastic part used to connect two pins on the jumper connector. Jumper shunts should be installed notch side up.

IF: The board is not correctly jumpered.

THEN: Use a pair of needle nose pliers to gently remove, and carefully replace the jumper shunt in its proper location.



Step 5. Insert the DISK 1B into the S-100 Bus.

The power to the system must be off. Place the board into a slot towards the back of the enclosure. The edge connector is offset, so the board fits only one way. **Push down GENTLY until the board is firmly installed.**

Switch Settings

Switch Summary

The DISK 1B has a single 10-position dip-switch, SW1, which controls three functions:

- The block size and addressing of the on-board EPROM (positions 1-8).
- Whether the EPROM is used to boot the system after a system reset (position 9).
- The polarity of a software readable switch (position 10).

SW1 Position	Function
1	EPROM Address A14
2	EPROM Address A13
3	EPROM Address A12
4	EPROM Address A11
5	Block Size select MSB
6	EPROM Address A10
7	Block Size select LSB
8	EPROM Address A9
9	EPROM BOOT ENABLE (ON enables boot from EPROM).
10	READABLE SWITCH (ON reads 0)

Note that when a paddle is OFF, the corresponding address bit is high, and when a paddle is ON, the bit is low.

Switch Description

The on-board EPROM can be either a 2764 (8K by 8), 27128 (16K by 8), or 27256 (32K by 8) for total space from 8K bytes to 32K bytes. On power-up or reset, the main processor looks to this memory space for instructions, using the EPROM as a "boot EPROM." The block size of the EPROM that is visible to the processor can be 512, 1K, or 2K bytes. The total number of different routines available is equal to the EPROM size divided by the block size. For example, 16 different 512 byte routines are available using a 2764 EPROM, or 32 different 1K byte routines are available using a 27256 EPROM.

The address bits and corresponding switch positions are given in Table 2. The switch settings required for different block sizes are given in Table 3 for the different EPROMs allowed.

Table 2 - EPROM Addresses Selected by Switch SW1

SW1 Position	Address on EPROM
1	A14 (not used in 2764, 27128)
2	A13 (not used in 2764)
3	A12
4	A11
6	A10
8	A9

Table 3 - SW1 Settings for Different EPROMS and Block Sizes

Block Size	EPROM Size		
	2764	27128	27256
512	Pos 3,4,6,8 addr Pos 5,7 OFF Pos 1,2 not used	Pos 2-4,6,8 addr Pos 5,7 OFF Pos 1 not used	Pos 1-4,6,8 addr Pos 5,7 OFF
1K	Pos 3,4,6 addr Pos 5,8 OFF Pos 7 ON Pos 1,2 not used	Pos 2-4,6 addr Pos 5,8 OFF Pos 7 ON Pos 1 not used	Pos 1-4,6 addr Pos 5,8 OFF Pos 7 ON
2K	Pos 3,4 addr Pos 6,8 OFF Pos 5,7 ON Pos 1,2 not used	Pos 2-4 addr Pos 6,8 OFF Pos 5,7 ON Pos 1 not used	Pos 1-4 addr Pos 6,8 OFF Pos 5,7 ON

The boot EPROM on the DISK 1B contains software routines required to load the initial sectors of the disk operating system into memory for system startup ("boot up"). System RAM must be present from 0h to 7FFh for proper operation of the boot EPROM. The different routines in the EPROM allow different processor types (8086, 68K, etc.) to load the disk operating system from different devices (floppy disks, hard disks, etc.). As new processors and new boot devices are added by CompuPro, the version of the boot EPROM installed on the DISK 1B may need to be changed. Please refer to the Software Installation Guide for the system to determine the appropriate switch settings for the particular boot EPROM on the DISK 1B.

SW1 position 9 controls whether the boot EPROM is enabled after a system reset. The boot EPROM may be enabled by putting position 9 of SW1 in the ON position, and disabled by placing it in the OFF position.

Remember, the boot hardware on the DISK 1B board requires that memory respond to PHANTOM* at the host processor's reset address. If the memory residing at this address does not respond to PHANTOM* and the boot EPROM is enabled, a bus conflict will occur and possible damage could result.

SW1 position 10 can be read by the host CPU. When the host CPU reads this bit (bit 2 in relative I/O port 2), it will read a 0 when position 10 is ON, and a 1 when position 10 is OFF. This feature can be useful in systems to allow the software to determine what hardware is in the system. For example, in the CompuPro Concurrent DOS 8-16 Version 5.0 operating system, when this position is ON, the software expects a SYSTEM SUPPORT 1 in the system, and when this position is OFF, the software expects a SYSTEM SUPPORT 2. The installation guide for the operating system on a particular computer will explain the function of this switch when used with that operating system.

This completes the section on switches.

Jumper Settings

Jumper Summary

The DISK 1B has 13 jumpers that allow considerable flexibility. Jumpers J0-3 and J8 are the only ones on the board that have pins and tandem shunts installed. The remaining jumpers (J4-7, J9-13) are set with small traces on the board to the configuration that most users will want.

Table 4 - Summary of Jumpers

J	Position	Function
0	A-C	Select 5.25" for DRIVE 0
	B-C	Select 8" for DRIVE 0
1	A-C	Select 5.25" for DRIVE 1
	B-C	Select 8" for DRIVE 1
2	A-C	Select 5.25" for DRIVE 2
	B-C	Select 8" for DRIVE 2
3	A-C	Select 5.25" for DRIVE 3
	B-C	Select 8" for DRIVE 3 (pins and shunts are installed in J0-J3)
4	A-C	WD 92C32 or SMC 9236 Data Separator in U42
	B-C	9216B Data Separator in U42 (trace normally connects B-C on board)
5		Installed allows HDLD* (pin 4) on 5.25" cable to be driven. Removed floats HDLD* dis-asserted. (normally not connected)
6		Installed allows RWRITE* (pin 2) on 5.25" cable to be drive. Removed floats RWRITE* dis-asserted. (trace normally connects)
7		Installed allows PHANTOM* (pin 67) to be driven on the S-100 bus during accesses to boot EPROM. Removed disables PHANTOM* assertion. (trace normally connects)

Table 4 - Summary of Jumpers (Continued)

J	Position	Function
8	A	Installed returns READY to FDC on DRIVE SELECT 0
	B	Installed returns READY to FDC on DRIVE SELECT 1
	C	Installed returns READY to FDC on DRIVE SELECT 2
	D	Installed returns READY to FDC on DRIVE SELECT 3
		(pins and shunts are installed)
9		Installed places 3 wait states in DMA, boot EPROM, and I/O cycles to the DISK 1B (for up to 12.5 MHz bus speeds).
		Removed places 4 wait states in all of above.
		(trace normally connects on board)
10,11	A-C	Eliminates write precompensation on the drives
	B-C	Uses write precompensation on the drives
		(traces normally connect B-C)
12	0	Interrupt from FDC goes to VI0* (pin 4) on S-100
	1	Interrupt from FDC goes to VI1* (pin 5) on S-100
	2	Interrupt from FDC goes to VI2* (pin 6) on S-100
	3	Interrupt from FDC goes to VI3* (pin 7) on S-100
	4	Interrupt from FDC goes to VI4* (pin 8) on S-100
	5	Interrupt from FDC goes to VI5* (pin 9) on S-100
	6	Interrupt from FDC goes to VI6* (pin 10) on S-100
	7	Interrupt from FDC goes to VI7* (pin 11) on S-100
		(trace normally connects VI4*)

Table 4 - Summary of Jumpers (Continued)

J	Position	Function
13	A	I/O port address A2 (normally connected)
	B	I/O port address A3 (normally connected)
	C	I/O port address A4 (normally connected)
	D	I/O port address A5 (normally connected)
	E	I/O port address A6 (normally open)
	F	I/O port address A7 (normally open)
		(default I/O ports are C0h to C3h)

Note that when an address jumper is open, the corresponding address bit is high, and when an address jumper is connected, the bit is low.

Jumper Description

Jumpers J0 through J3 select which drives are 5.25" and which are 8". Each drive connected to the DISK 1B must be jumpered (on the drive) for a different drive select. J0 through J3 then must be set on the DISK 1B to correspond to which drives are 8" and which drives are 5.25". A shunt across A-C selects 5.25"; a shunt across B-C selects 8".

For example, if an 8" drive was jumpered as drive 0, and a 5.25" drive was jumpered as drive 2, J0 must be set to B-C, and J2 must be set to A-C. J0 through J3 have pins and shunts installed at the factory. These must be set to the configuration of the target system.

Jumper J4 selects different clock rates for the digital data separator in U42. If a shunt is placed across B-C, a 9216B from either SMC (Standard Microsystems Corp.) or WD (Western Digital) must be in U42. The 9216B is the standard performance part, and can be used with good quality drives that have low jitter in their read data stream. The higher performance WD 92C32 or SMC 9236 requires J4 to be set to A-C. Some drives with more jitter in their read data stream may require this higher performance part for reliable operation. J4 normally has no pins installed and has a trace across B-C. This can be cut and pins installed to change the setting.

Jumper J5 allows the DISK 1B to assert HDLD* (Head Load, pin 4) on the 34 pin 5.25" cable. With J5 removed (as shipped), the DISK 1B will never assert HDLD*. Most 5.25" drives automatically load the head when MTR ON* (Motor On, pin 16) and DRIVE SELECT* (DRS0-3*, pins 6, 10, 12, or 14) are asserted. Please refer to the drive specification for information on how a particular drive works. If a drive does need HDLD* to be asserted, J5 should then be installed. Setting bit D2 in relative port 0h low then asserts HDLD*. On reset, when J5 is installed, HDLD* is asserted.

Jumper J6 allows the DISK 1B to assert RWRITE* (Reduced Write, pin 2) on the 34 pin 5.25" cable. This jumper is normally connected with a trace on the solder side of the board. When writing certain types of diskettes on certain types of drives, asserting this line is necessary for error free writing. Most drives don't care about this line, and some drives use this line for different functions. The drive manual must be consulted on use of this signal. Setting bit D4 in relative port 0h low asserts RWRITE*. On reset, when J6 is installed, RWRITE* is asserted.

Jumper J7 allows PHANTOM* (pin 67) on the S-100 bus to be asserted when the host CPU is reading the boot EPROM. J7 is normally connected with a trace on the solder side of the board. If the standard boot EPROM on the DISK 1B is used, this jumper must be connected. If it is ever necessary to disconnect PHANTOM*, this jumper can be cut.

Jumper J8 is a four position jumper that allows READY to be asserted to the 765A or 8272A floppy disk controller (FDC) automatically whenever a particular drive is selected. This is necessary as some floppy drives do not assert READY in the manner that the floppy disk controller needs it. Install a jumper according to the following table depending on which drives need READY to be driven automatically. Jumpers should not be installed if a drive returns READY normally.

Table 5 - READY to FDC on DRIVE SELECT

J8	Function
A	Installed returns READY to FDC on DRIVE SELECT 0
B	Installed returns READY to FDC on DRIVE SELECT 1
C	Installed returns READY to FDC on DRIVE SELECT 2
D	Installed returns READY to FDC on DRIVE SELECT 3

Jumper J9 selects between three and four wait states inserted on DISK 1B DMA cycles, I/O cycles to the DISK 1B, and memory reads from the boot EPROM. In systems up to 12.5 MHz, 3 wait states are adequate for all the above type of cycles. Thus, J9 is connected by a small trace on the solder side of the board. If it is ever necessary to move to 4 wait states, cut the small trace connecting J9 on the solder side of the board.

Jumper J10 and J11 control whether write precompensation is used when writing the floppy disks. Both jumpers must be set the same way. Most drives accept 250 ns of write precompensation, and thus J10 and J11 are connected on the component side of the board across B-C. If it ever necessary to eliminate write precompensation for all the drives, the traces across B-C on J10 and J11 should be cut, and jumpers should be installed across A-C of J10 and J11.

Jumper J12 is an eight position jumper that selects which S-100 vectored interrupt (VI) is asserted when the floppy disk controller asserts an interrupt. Any VI from VI0* (position 0) to VI7* (position 7) can be asserted by placing a jumper across the proper position. As CompuPro systems use VI4* for the DISK 1B, there is a small trace on the solder side of the board connecting position 4. If it is necessary to use another interrupt for the DISK 1B, cut the small trace and install a jumper in the proper position.

Jumper J13 is a six position jumper that selects what base I/O port the DISK 1B's 4 I/O ports are located at. The DISK 1B uses 8 bit address decoding. An installed jumper selects a 0 for the address bit, and a removed jumper selects a 1. The following table shows which position of J13 (A-F) stands for which bit of address.

Table 6 - Jumper J13 I/O Port Addressing

J13	Address Bit
A	I/O port address A2 (normally connected)
B	I/O port address A3 (normally connected)
C	I/O port address A4 (normally connected)
D	I/O port address A5 (normally connected)
E	I/O port address A6 (normally open)
F	I/O port address A7 (normally open)

(default I/O ports are C0h to C3h)

As the standard CompuPro address for the DISK 1B is 0C0h-0C3h, traces on the component side of the board normally connect position A through D to select this address. If it is ever necessary to change this address, the small traces can be cut and jumpers installed.

This completes the section on jumpers.

Functional Description

Disk Interface Port Map

The DISK 1B interface uses a block of four port addresses for communication between it and the host processor. After boot, DISK 1B occupies no memory space of the host processor and performs all data transfers via DMA. The address of the first port is jumper settable to any I/O address which is a multiple of four. The ports will be referred to as relative ports 0 - 3. See the section on jumper settings for how to set the I/O port address.

Table 7 - I/O Port Overview

Relative Port	Function
0 Read	FDC Main Status Register
0 Write	Drive Select Register
1 Read	FDC Data Register
1 Write	FDC Data Register
2 Read	Drive Status Register
2 Write	DMA Address Register
3 Read	(not used)
3 Write	Motor Control Register

FDC Main Status Register (read only)

This is the main status register of the FDC chip. It may be read to obtain the status of the drives and the controller chip. Please refer to the 8272A/765A data sheet for a description of the bits in this register. See appendix 2 for information on obtaining the 8272A data sheet.

Drive Select Register (write only)

The Drive Select Register controls a number of different functions on the DISK 1B. Bit 7 allows the DISK 1B to force a hard reset to the FDC. Bits 6 and 5 allow the selection of four different floppy disk data rates. Bit 4 allows the DISK 1B to assert reduced write (RWRITE*, pin 2) to 5.25" drives. Bit 3 allows the assertion of TS (two-sided) to the FDC when using 5.25" drives. Finally, bit 2 allows the DISK 1B to assert head load (HDLD*, pin 4) to 5.25" drives. Bits 1 and 0 are not used and should be set 0. The bit positions and function are shown in the following table.

Table 8 - Drive Select Register Description (Port 0)

Bit	Function
0	not used
1	not used
2	5.25" HDLD* (assert HDLD* - 0, dis-assert HDLD* - 1)
3	Force Two Sided (Normal - 0, Force - 1)
4	5.25" RWRITE* (assert RWRITE* -0, dis-assert RWRITE* - 1)
5	5.25"/8" Data Rate Select (8" - 0, 5.25" - 1)
6	HI/LO data rate select (normal - 0, special - 1)
7	Floppy Disk Controller Reset (run - 0, reset - 1)

FDC Data Register (read/write)

The FDC Main Data Register is the main communication path between the host system and the FDC chip. All command and result status pass through this register.

Drive Status Register (read only)

The Drive Status Register allows software to poll a drive's READY* status, view the drive's INDEX* pulse, check the FDC interrupt status, and read the readable switch. The bit positions are shown in the following table.

Table 9 - Drive Status Register Description (Port 2)

Bit	Function
0	Drive Ready Status (READY - 1)
1	Drive Index Pulse (PULSE - 1)
2	Readable Switch SW1-10 (ON - 0, OFF - 1)
3-6	(not used)
7	FDC Interrupt Status (INTERRUPT ACTIVE - 1)

DMA Address Register (write only)

The DMA address register is actually a push-down stack of three 1-byte registers. To use this register to load an address, load a 3-byte DMA address most significant byte first.

Motor Register (write only)

The Motor Register allows: 1)software setting of the motor control lines for drives that respond to these lines and, 2)disabling of the boot EPROM. A system reset (not a floppy disk controller reset) is required to re-enable the boot EPROM. The Control Bits are described in the following table.

Table 10 - Motor Control Register Description (Port 3)

Bit	Function
0	Boot EPROM Disable (Disable - 0, System Reset to Re-enable)
1-3	(not used)
7	Floppy Motor Control (Motors ON - 1, Motors OFF - 0)

NOTE: Bit 7 controls both 8" floppy and 5.25" floppy motors.

Data Rate Select

Two bits are provided in the drive select register to choose the data rate for the floppy disk controller (FDC). In addition, The FDC senses whether the floppy disk inserted in the drive is formatted as double density (MFM encoded), or single density (FM encoded). The single density (FM) data rate is half the double density (MFM) data rate.

Four different double density (MFM) data rates are selectable with the two bits in the data select register. They are: 500K bits/sec for 8" drives and 5.25" IBM* AT style high-capacity drives; 250K bits/sec for 5.25" drives such as the Mitsubishi M4853; 300K bits/sec for IBM AT style high-capacity drives reading IBM PC style disks; and 150K bits/sec. If the floppy disk in the drive is single density (FM), the FDC will sense it and automatically cut the data rate in half.

Choose the rate depending on the drive type and disk format being used. The following table gives the data rate as a function of the drive select register bits 5 and 6.

Table 11 - Data Rate Select

Drive Select Register Bit 6	Bit 5	MFM Data Rate Chosen	FM Data Rate Chosen
0	0	500K bits/sec	250K bits/sec
0	1	250K bits/sec	125K bits/sec
1	0	300K bits/sec	150K bits/sec
1	1	150K bits/sec	75K bits/sec

Floppy Disk Controller Reset

In addition to being asserted when a system reset is driven (RESET, pin 75 on the S-100 bus), the floppy disk controller (FDC) reset pin is asserted when bit 7 in the drive select register is set high. The FDC can get into an illegal state that requires a hardware reset to the chip to clear. The DISK 1B provides such a reset under software control.

To assert reset to the FDC, set bit 7 of the drive select register high. To release reset, set this bit low. Make sure that an adequate width reset pulse (at least 7 microseconds) is given to the floppy disk controller. Also make sure to delay for about the same length of time after reset is released before sending new commands to the FDC.

Interrupts

The DISK 1B is capable of running in either a polled mode or an interrupt-driven mode that is particularly suited for multi-user environments. The DRIVE STATUS port (relative port 2) allows software to sample the interrupt output of the floppy disk controller on data bit 7. To run in an interrupt driven mode, the interrupt output of the floppy disk controller is driven onto one of the vectored interrupt lines (VI0* thru VI7*) of the S-100 bus. This is accomplished by installing a jumper shunt or #30 wrap wire across the posts (if installed) at jumper location J12, positions 0-7. Jumpers 0 thru 7 correspond directly to VI0* thru VI7*. All CompuPro software uses VI4* for the floppy disk interrupt.

Wait State Enable

The DISK 1B inserts wait states into the boot EPROM read as well as the I/O and DMA read and write cycles when fast processors are being used. In systems with system clock speeds up to 12.5 MHz, jumper J9 should be installed to select three wait states. J9 can be removed if four wait states are needed.

Arbiter and Priority Selection

The DISK 1B controller allows multiple DMA devices to be active on the S-100 bus at one time. As long as a DMA board (temporary bus master) conforms to the IEEE 696/S-100 specifications concerning DMA arbitration and prioritization, up to 16 different bus masters may gain use of the bus in order of their assigned priority. Remember, there should never be more than one temporary bus master at a given priority level.

The priority of the DISK 1B board is fixed at 0Fh, the highest possible value. Make sure that no other DMA device in the system is set to 0Fh.

Motor Control Enable

A bit is provided in the Motor Control Register to control the four designated motor control lines for the 8" floppy drives, and one motor control line for 5.25" minifloppies. Some drives may not respond to these lines. By controlling the contents of this bit, the drives may have their motors turned "ON" or "OFF". In addition, this register has an automatic timeout feature that turns all the motors "OFF" approximately 15 seconds after the last access to the controller. Any access of the board resets this timer and the 15 seconds starts again.

Boot EPROM

The boot EPROM contains the software routines required to load the initial sectors of the disk operating system into memory for system startup. A complete description of the functions and capabilities of the boot EPROM addressing as well as how to set SW1 to use it is given in the Switch Settings section of this manual.

On power-up, when SW1 position 9 is ON, the boot EPROM will appear as memory at the host CPU's reset address and, in fact, at all memory addresses. The DISK 1B will assert PHANTOM* and provide data to the host CPU on every memory read cycle. The DISK 1B will not assert PHANTOM* during memory write or I/O cycles from the host CPU. This is so the host CPU can write to system RAM and command the DISK 1B during boot up. The host CPU will continue to read from the boot EPROM until a "1" is written to the motor control register bit 7. This will turn the boot EPROM off until the system is reset, regardless of what is written to this bit after the "1" is.

DISK 1B Connector Pinouts

Table 12 - DISK 1B Connector Pinouts

DISK 1B CONN 2 Pin	8" Drive Signal	DISK 1B CONN 1 Pin	5.25" Drive Signal
2	Low Current		
4	Motor OFF 1		
6	Motor OFF 2		
8	Motor OFF 3		
10	Two Sided		
12	NC		
14	Side Select		
16	NC		
18	Head Load	2	Reduced Write
20	Index (8")	4	Head Load
22	READY	6	Drive Select 4
24	Motor OFF 4	8	Index (5")
26	Drive Select 1	10	Drive Select 1
28	Drive Select 2	12	Drive Select 2
30	Drive Select 3	14	Drive Select 3
32	Drive Select 4	16	Motor ON
34	Direction Select	18	Direction Select
36	Step	20	Step
38	Write Data	22	Write Data
40	Write Gate	24	Write Gate
42	Track 00	26	Track 00
44	Write Protect	28	Write Protect
46	Read Data	30	Read Data
48	NC	32	Side Select
50	NC	34	READY

All odd pins ground on both cables.

Programming Considerations

Minifloppy Drives

Several things must be considered when using minifloppy drives with the DISK 1B, and these are listed below.

- Most minifloppy drives use data rates that are different from that of 8" drives, therefore, the clock frequency of the FDC and other circuitry must be changed. This is accomplished by setting bits 5 and 6 in the Drive Select Register. After this is done, at least 5 microseconds must elapse before sending anything to the FDC to let it settle down, and then new specify instructions must be sent to the FDC. Since the clock to the FDC is now different, the specify values must be modified accordingly (refer to the FDC data sheet).

- Since almost all minifloppy drives have a Motor Control Line, there is a time lapse of about 0.5 second between turning the drive motor ON and when it comes up to speed. The motor must be up to speed before attempting to read or write to the drive. The MOTOR REGISTER will automatically time out and shut off the drives after approximately 15 seconds when there is no activity on the drive.

- Some minifloppies have a READY line and some do not. If the drive does, leave the corresponding jumper on J8 disconnected. If the drive does not generate READY, the corresponding position on J8 will need to be jumpered so that the READY line of the FDC is driven when the drive is selected. This will make the FDC think that the drive is ready whenever the drive is selected. Other means (such as polling) must be employed to see when the drive is really ready.

- Since minifloppy drives do not have a signal that tells the FDC that a floppy is single or double sided, this must be handled with external logic. This is accomplished by setting the Force Two Sided line (F2S) when a double sided floppy is used. The reason for this is that the FDC will not access the second side of a diskette when it thinks the diskette is single sided.

WARNING!

Not all floppy disk controllers generate true IBM compatible 3740 and System 34 formats even though they claim to. Therefore, it is strongly recommended that the DISK 1B not be used to copy data onto a diskette that has been formatted by another controller! The proper procedure is to format diskettes using the DISK 1B, and copy the contents of other diskettes onto the newly formatted diskettes.

If the other controller generates a true IBM type format, or the diskettes were formatted by IBM, they will not have to be formatted before using them with the DISK 1B.

Specifications for 8" Floppy Disk Drives

For the disk drives, the 50-pin cable connecting CONN 2 of the DISK 1B to 8" floppy drives is standard except that the stepper motors must be enabled at all times (not tied to drive select or head load). This causes the steppers to be powered at all times (they will get warm), and allows stepping without the lamp on the front of the drive being "ON" (so be careful). In addition, do not tie the head load signal to drive select since the 765A/8272A is always scanning the drives (this would result in a buzz). Use standard 50-pin ribbon cable to connect the drives to the controller, and terminate the last drive in the line as specified in the drive manual.

NOTE: Due to the steppers being enabled at all times, the disk power supply must be able to handle full load on the +24V line all the times and the drive enclosure must have adequate cooling.

Specifications for 5.25" Minifloppy Disk Drives

If the minifloppy drive has a head load line, install the appropriate jumper to bring the head load out to pin 4. Otherwise, jumper the minifloppy so the heads load on drive select. Set the drive select so READY is generated only when the drive is selected and a diskette is spinning in the drive. If possible, READY should go false when the drive door is opened.

Programming Example

Below is an example of code that might appear in the boot EPROM for the 8" and 5.25" floppy drives using an 8086 type processor. It is intended solely as an example and does not necessarily represent the best way to program the DISK 1B.

```
                        ;
                        ; PURPOSE: Simple test program for the DISK1B.  This program will read
                        ;          in the entire track 0 off of a 5 1/4" diskette.
                        ;
000A                    CPUSPD  EQU     10      ;Set to CPU speed
0014                    CPUFACTOR EQU   20      ;20 for 80286, 37 for 8086, 45 for 8088
                        ;
0002                    FDDRIVE EQU     2               ; physical drive number to test
                        ;
00C0                    FDPORT  EQU     0C0h            ; controller port for DISK 1A
0003                    FDON    EQU     3               ; disk motors and PROM on/off offset
00C3                    PHANOFF EQU     FDPORT + FDON
0000                    FDDRS   EQU     0               ; set floppy disk clock rate offset
0020                    FD5SL   EQU     20h             ; select 5-1/4 inch data rate (4 MHz)
0008                    FDF2S   EQU     8               ; force 2-sidedness for 5" floppies
0000                    FDCS    EQU     0               ; floppy disk status register offset
0001                    FDCD    EQU     1               ; data register offset
0008                    FDRSTS  EQU     8               ; read status command
0080                    FDC_EOC EQU     80h             ; end of cylinder error
0020                    FDC_SKE EQU     20H             ; seek end
0002                    INTS    EQU     2               ; command status register offset (when read)
0002                    FDMA    EQU     INTS            ; DMA address offset (when write)
                        ;
                        ; Some general useful equates
000A                    CR      EQU     0AH
000D                    LF      EQU     0DH
0024                    EOS     EQU     '$'

                                CSEG
                        ; External OS dependent routines
                        extrn   PRINT:near              ; Print message pointed to by "DX"
                        extrn   EXIT:near               ; Exit OS gracefully, no parameters
                        ;
                                ORG     0
                        ;
                        ENTER:
0000 BA2801     R               MOV  DX,offset TRYMSG   ; show trying to read message
0003 E80000     E               CALL    PRINT
0006 B0FE               ENTFT:  MOV     AL,0FEh         ; turn on disk motors and turn off PROM
0008 E6C3                       OUT     PHANOFF,AL      ; send command
000A B000                       MOV     AL,0            ; set no TS, use 8" data rate for all seeks
000C E6C0                       OUT     FDPORT+FDDRS,AL ; set it
000E B90500                     MOV     CX,5
0011 E8C500     00D9            CALL    FDCWAIT         ; delay for motors to come up to speed
```



```
                        ;
                        ; first, load specify command
0014 B503                       MOV     CH,length SPEC  ; length of specify command into counter
0016 B100                       MOV     CL,0            ; no status bytes returned
0018 BE5001     R               MOV     SI,offset SPEC  ; source index points to specify command
001B E87000     008E            CALL    EXEC            ; send command
001E B9F000                     MOV     CX,240          ; must delay for 240 MS after specify command

0021 E8B500     00D9            CALL    FDCWAIT         ;  for 8272a to stabilize
                        ; then recalibrate drive
0024 B502                       MOV     CH,length RECAL ; length of recalibrate drive head command
0026 B100                       MOV     CL,0            ; no status bytes for this command
0028 BE5301     R               MOV     SI,offset RECAL ; SI now points to recalibrate command
002B E86000     008E            CALL    EXEC            ; send command
002E E89200     00C3 RECLMT:    CALL    WAITINT         ; wait for interrupt complete bit
                        ;
                        ; verify successful completion of recalibrate command
                        ;
0031 B008                       MOV     AL,FDRSTS       ; read status command
0033 E6C1                       OUT     FDPORT+FDCD,AL  ; send it
                        ;
0035 B90200                     MOV     CX,2            ; get two status bytes
0038 E86600     00A1            CALL    GCMPS
003B 2C20                       SUB     AL,FDC_SKE      ; remove seek end bit
003D 740C       004B            JZ      ADDR            ; if seek end, no other errors -- done
003F A05E01     R               MOV     AL,TEMPBUF      ; get first status byte again
0042 2403                       AND     AL,00000011b    ; mask to drive select bits only
0044 3C02                       CMP     AL,FDDRIVE      ; see if this was desired drive
0046 75E6       002E            JNE     RECLMT          ; must have been ready line change for some
                        ;                               ; other drive, wait for something else to happen
0048 E9B5FF     0000            JMP     ENTER           ; else some real error, so start again
                        ;
                        ; execute read operation sequence
                        ; output beginning DMA address
004B 8CD8               ADDR:   MOV     AX,DS           ; get current data segment
004D B104                       MOV     CL,4            ; set up for 4 bit shift (*16)
004F D3C0                       ROL     AX,CL           ;
0051 8BD8                       MOV     BX,AX           ; save copy in BX for lower addres calculation
0053 240F                       AND     AL,0FH          ; mask off to high nybble only
0055 81E3F0FF                   AND     BX,0FFF0H       ; mask off high nybble from rest of address
0059 81C36401   R               ADD     BX,offset BUFFER ; add in local buffer offset
005D 1400                       ADC     AL,0            ; add any carry to high nybble
005F BAC200                     MOV     DX,FDPORT+FDMA  ; point to dma address port
0062 EE                         OUT     DX,AL           ; send high nybble
0063 8AC7                       MOV     AL,BH
0065 EE                         OUT     DX,AL           ; send middle byte
0066 8AC3                       MOV     AL,BL
0068 EE                         OUT     DX,AL           ; send low byte
```

```
                        ;
                        ; read all data on track 0 to get the cold boot secondary loader
0069 E85E00     00CA            CALL    FDCS            ; set up the 5 1/4" data rate
006C B509                       MOV     CH,length READ  ; length of read track command
006E B107                       MOV     CL,7            ; get max status bytes back
0070 BE5501   R                 MOV     SI,offset READ  ; point to read command
0073 E81800     008E            CALL    EXEC            ; send command
0076 8B07                       MOV     AX,[BX]         ; pick up first two status bytes
0078 25F8FF                     AND     AX,0FFF8h       ; strip the head and drive select bits
007B 2D4080                     SUB AX,(FDC_EOC*256)+40H ; remove End of Cylinder error and abnormal

                        ;                               ;  completion status
                        ; if "abnormal ending" caused by "end of cylinder" error, then read is valid
007E 7405       0085            JZ      READOK
0080 BA1101   R                 MOV  DX,offset ERRMSG
0083 EB03       0088            JMPS    PERROR          ; print error message and exit

0085 BA0001   R       READOK: MOV  DX,offset OKMSG    ; show read ok message
0088 E80000   E       PERROR: CALL    PRINT           ; at console
008B E90000   E               JMP     EXIT            ; and exit to OS
                        ;       should never return
                        ;
                        ;
                        ; send a command to the 8272a floppy disk controller
                        ;  SI => command block
                        ;  CH => number of bytes to output to controller
                        ;  CL => number of bytes to input to status buffer
                        ;
008E FC                 EXEC:   CLD                     ; clear direction for subsequent command load
008F 9CFA                       PUSHF ! CLI             ; disable ints during command send
0091 E82800     00BC    EXECLP: CALL    GETRQM          ; wait for request to service master
0094 AC                         LODSB                   ; otherwise, load command byte
0095 E6C1                       OUT     FDPORT+FDCD,AL  ; and send it
0097 FECD                       DEC     CH              ; count this byte as sent
0099 75F6       0091            JNZ     EXECLP          ; loop until all bytes sent
009B 9D                         POPF
009C E317       00B5            JCXZ    EXEC0           ; exit now if no status bytes
                        ;
009E E82200     00C3            CALL    WAITINT         ; wait for command to complete
                        ;
                        ; Get completion status byte(s) into TEMBUF buffer.
                        ;  Entry CX = Number of status byte to read in
                        ;  Exit AL = first status byte with drive select removed
                        ;       BX = pointer to status byte buffer
00A1 BB5E01   R       GOMPS:  MOV  BX,offset TEMPBUF  ; point to status buffer address
00A4 E81500     00BC  GOMPS2: CALL    GETRQM          ; wait for request to service master
00A7 EAC1                       IN      AL,FDPORT+FDCD  ; get a status byte
00A9 8807                       MOV     [BX],AL
```



```
00AB 43                         INC     BX              ; bump status buffer pointer
00AC E2F6       00A4            LOOP    GOMPS2          ; decrement status byte counter, loop until 0
00AE BB5E01   R                 MOV  BX,offset TEMPBUF
00B1 8A07                       MOV     AL,[BX]         ; get first returned status byte
00B3 24F8                       AND     AL,0F8H         ; remove drive/head select
00B5 50                 EXEC0:  PUSH    AX              ; save possible return status
00B6 B000                       MOV     AL,0            ; set data rate back maximum, no TS
00B8 E6C0                       OUT     FDPORT+FDDRS,AL ; (rate is always reset back to 8" value)
00BA 58                         POP     AX
00BB C3                         RET
                        ;
                        ; Wait for "Request to Service Master" bit to indicate FDC is ready
00BC EAC0               GETRQM: IN      AL,FDPORT+FDCS  ; get status of drive

00BE A880                       TEST    AL,80H          ; check if ready
00C0 74FA       00BC            JZ      GETRQM          ; loop if not
00C2 C3                         RET
                        ;
                        ; Wait for 8272a command to complete, in a multi-tasking environment
                        ;  this is where you would wait for an interrupt
00C3 EAC2               WAITINT:IN      AL,FDPORT+INTS  ; see if command execution completed
00C5 A880                       TEST    AL,80H          ; see if int bit set
00C7 74FA       00C3            JZ      WAITINT         ; loop if not
00C9 C3                         RET                     ; return when command is completed
                        ;
                        ; Set up the 5 1/4" data rate
00CA 5051               FDCS:   PUSH AX ! PUSH CX
00CC B028                       MOV     AL,FDCSL+FDF2S  ; set the 5 1/4" data rate (4 mhz) and
                                                        ;  force "two sided"
00CE E6C0                       OUT     FDPORT+FDDRS,AL ; send to special select register
00D0 B90300                     MOV     CX,3            ; allow the PLL to stabilize at the lower freq
00D3 E80300     00D9            CALL    FDCWAIT         ;  byte waiting 3 milliseconds
00D6 5958                       POP CX ! POP AX         ; recover incoming registers
00D8 C3                         RET
                        ;
00D9 B8F401             FDCWAIT:MOV     AX,(CPUSPD*1000)/CPUFACTOR ;1 millisecond delay factor
00DC 50                 FDCDLY: PUSH AX ! POP AX        ; stop prefetcher in cpu
00DE 48                         DEC     AX              ; bump internal loop counter
00DF 75FB       00DC            JNZ     FDCDLY          ; loop for 1 millisecond
00E1 E2F6       00D9            LOOP    FDCWAIT         ; loop until all specified milliseconds complete
00E3 C3                         RET
                        ;
                                DSEG
                                ORG     100H
```

```
                ;*****************************************
                ;*    FIXED STORAGE FOR DISK PARAMETERS    *
                ;*****************************************
0100 0A0D44697368 OKMSG   DB      CR,LF,'Disk read ok',CR,LF,EOS
     207265616420
     6F6B0A0D24
0111 0A0D4572726F ERRMSG  DB      CR,LF,'Error on disk read',CR,LF,EOS
     72206F6E2064
     69736B207265
     61640A0D24
0128 0A0D41747465 TRYMSG  DB      CR,LF,'Attempting read on floppy drive ',FDDRIVE+'0','..'
     6D7074696E67
     207265616420
     6F6E20666C6F
     707079206472
     697665520322E
     2E
014D 0A0D24               DB      CR,LF,EOS


                ;
                ;*****************************************
                ;*    FIXED STORAGE FOR DISK PARAMETERS    *
                ;*****************************************
                ; 5 1/4" floppy --
                ; floppy disk specification command
0150 03DF1E     SPEC    DB      3,0DFh,1Eh      ;3 ms step rate
                ; home to track 0, drive 0
0153 0702       RECAL   DB      7,FDDRIVE
                ;
                ; read sector command for 8272 controller (MFM)
                ; head select, drive select
                ; cylinder 0
                ; head 0
                ; starting sector
                ; "N" parameter (1024 byte sectors)
                ; number of sectors (NSS1024) = 5K bytes
                ; gap length (GPL)
                ; data length (DTL)
0155 460200000103 READ    DB      46h,FDDRIVE,0,0,1,3,5,35h,0FFh
     0535FF
                ;
015E 000000000000 TEMPBUF DB      0,0,0,0,0,0     ;
                ;
0164            BUFFER  RB      1024 * 5        ;Enough room for 1 5 1/4" track
1564 00                 DB      0               ;Force complete hex generation

                        END
```


Appendix A

Specifications

Timing	Meets all IEEE 696/S-100 specifications. Runs in systems exceeding 10 MHz.
Floppy Disk Controller .	Third generation NEC 765A or INTEL 8272A. Innovative clock design allows four popular floppy disk data rates.
Data Separator	Digital Data Separator 9216B or 9232.
DMA Type	Cycle stealing (releases CPU after transfer), 24-bit address, crosses 64K boundaries.
DMA Arbitration	Meets all IEEE 696/S-100 specifications.
Arbitration Priority . .	Highest priority (0Fh).
Port Addressing	Four port locations required, jumper-selectable to any four port boundary in the lower 256 port (8 bit) space.
Boot EPROM	Asserts PHANTOM* line for operation, may contain 64 boot routines of 512 bytes each, 32 routines of 1K each, or 16 routines of 2K each.
Interrupt	Drives any one of eight vectored interrupt lines (VI0-VI7).
Wait States	Automatically inserted.
Current Consumption . .	Typical 1500 mA at +8V (+5V in regulated systems). Maximum 2100 mA. No ±16V (±12V in regulated systems) current.

SPECIFICATIONS (Continued)

Disk Format and Interface

Drive Interface	Direct connection to Qume Trak 842, Mitsubishi M2896 8" drives and M4853 5.25" drives.
Drive Requirements . . .	Supports up to four drives, single-sided or double-sided, single-density or double-density, 8" or 5.25".
Media Format	Supports IBM 3740/System 34 soft sectored formats, along with many other popular formats when using Concurrent DOS 8-16.
Encoding	FM or MFM-precompensated.
Sector Size	Single-density: 128 byte. Double-density: 256, 512 and 1024 byte.
Tracks	Supports drives with up to 256 tracks.
Data Transfer Rate . . .	500K, 300K, 250K, 150K, 125K, 75K bits/second, software selectable.

Appendix B

Manufacturers Reference

Detailed information about the 8272A FDC can be found in the *1986 Microsystems Components Handbook* (order no. 230843) from Intel. The data sheet can be found in Volume 2 of that two volume set. It can be obtained from Intel by contacting:

INTEL Literature Sales
P.O. Box 58130
Santa Clara, CA. 95052-8130

or call: (800)548-4725 for Intel Literature Sales, or,
(800)538-1876 for other inquiries.

Appendix C

Disk Drive Jumper Settings

Mitsubishi M4853 5.25" Half-height Drive

INSTALL HS, MM (DS 0, 1, 2 or 3 as appropriate)

Leave terminator resistor pack installed on the last drive of the cable.

Qume Trak 842 8" Full-height Drive

INSTALL C, 2S, DL, (DS0, 1, 2, or 3 as appropriate)

REMOVE T40, GND, DS, D, DC, Y, HA

Cut HL and X, all others intact. Leave terminator resistor pack installed on the last drive of the cable.

Mitshubishi M2896 8" Half-height Drive

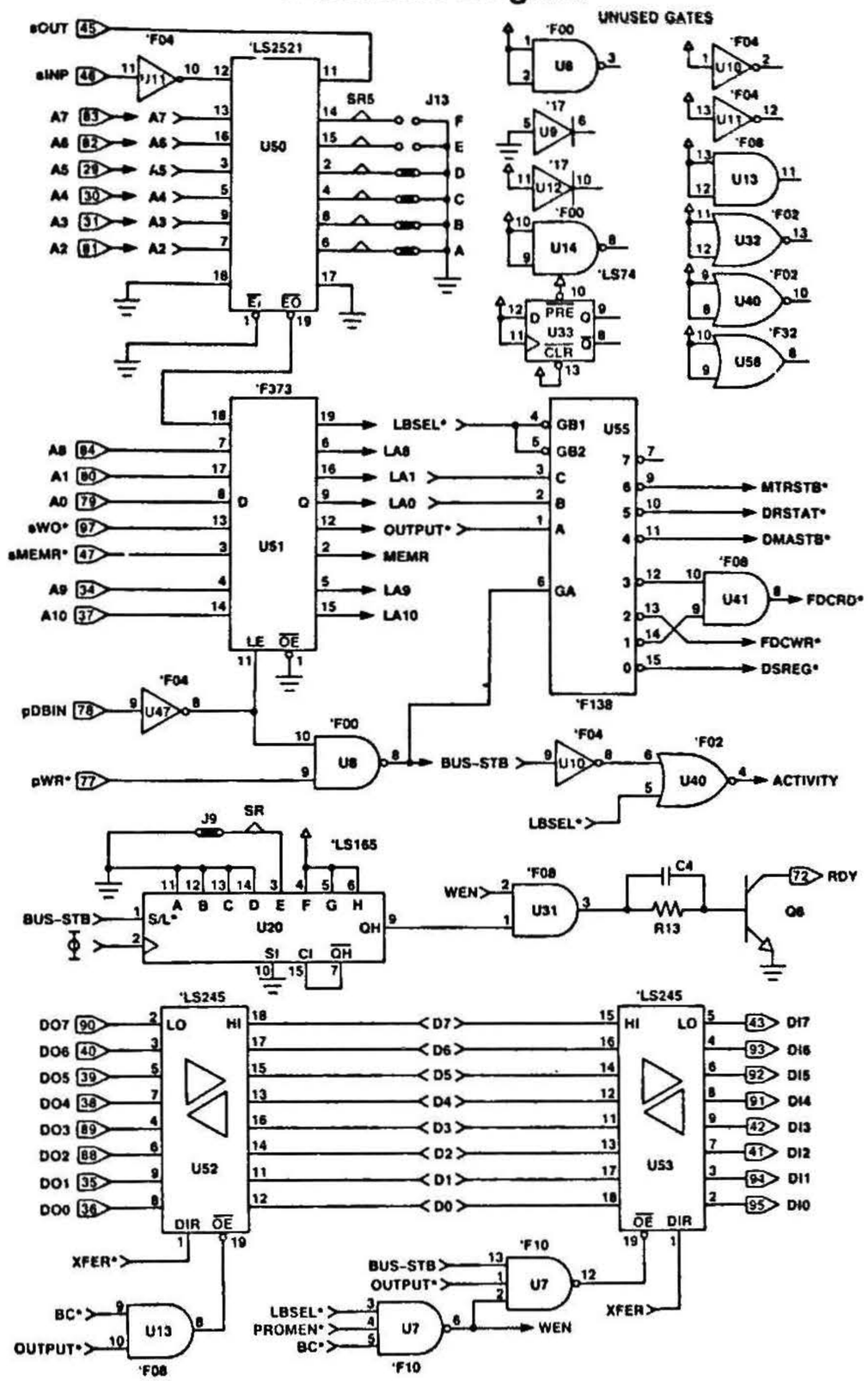
INSTALL JFG, SI, PS, 2S, M2, S2, C, I, R, IR, RFa, A, B, RS, HY, HUD, WP, Z, (DS0, 1, 2, or 3 as appropriate)

REMOVE All OTHERS

Leave terminator resistor pack installed on the last drive of the cable.

Appendix D

Schematic Diagram



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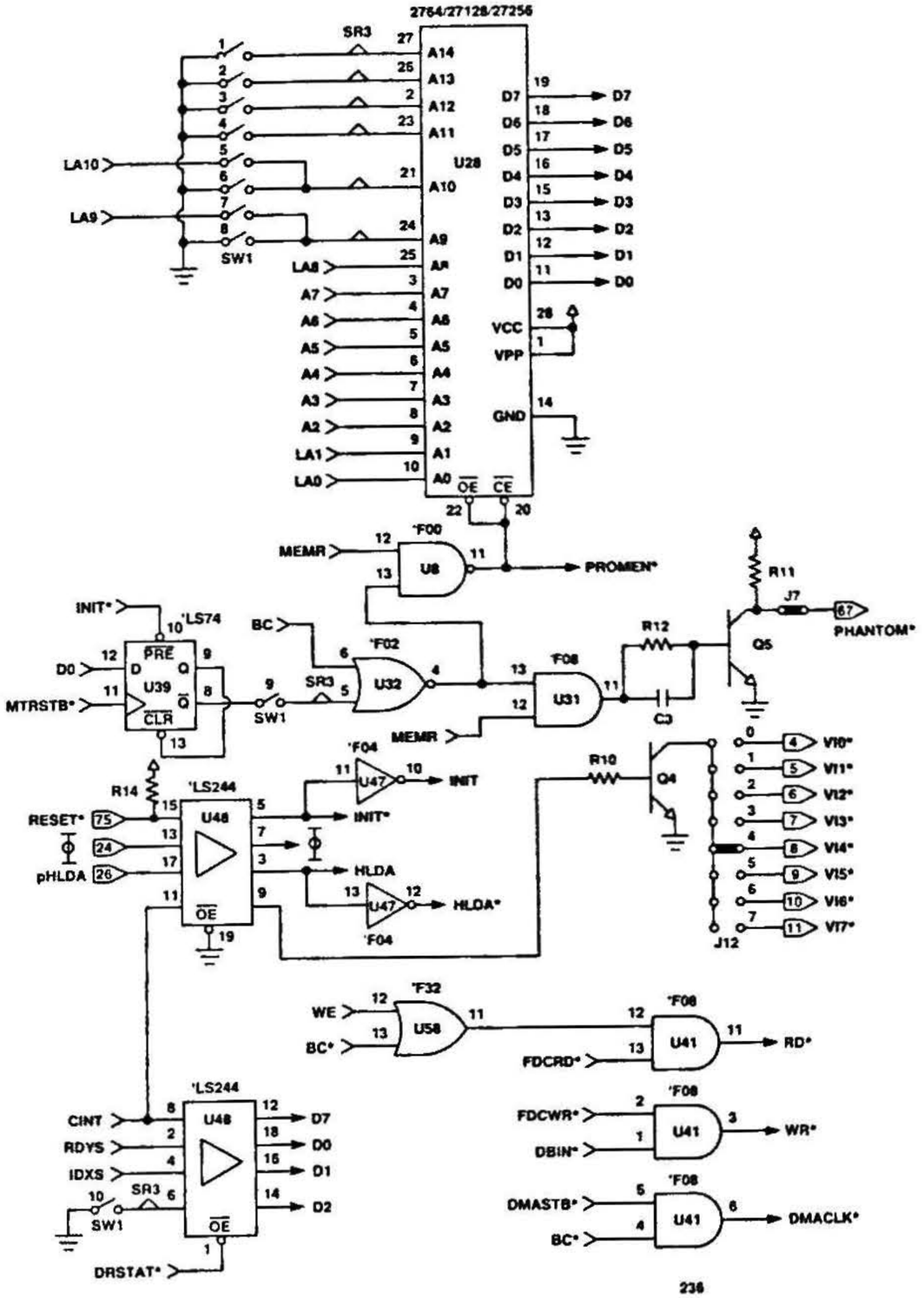

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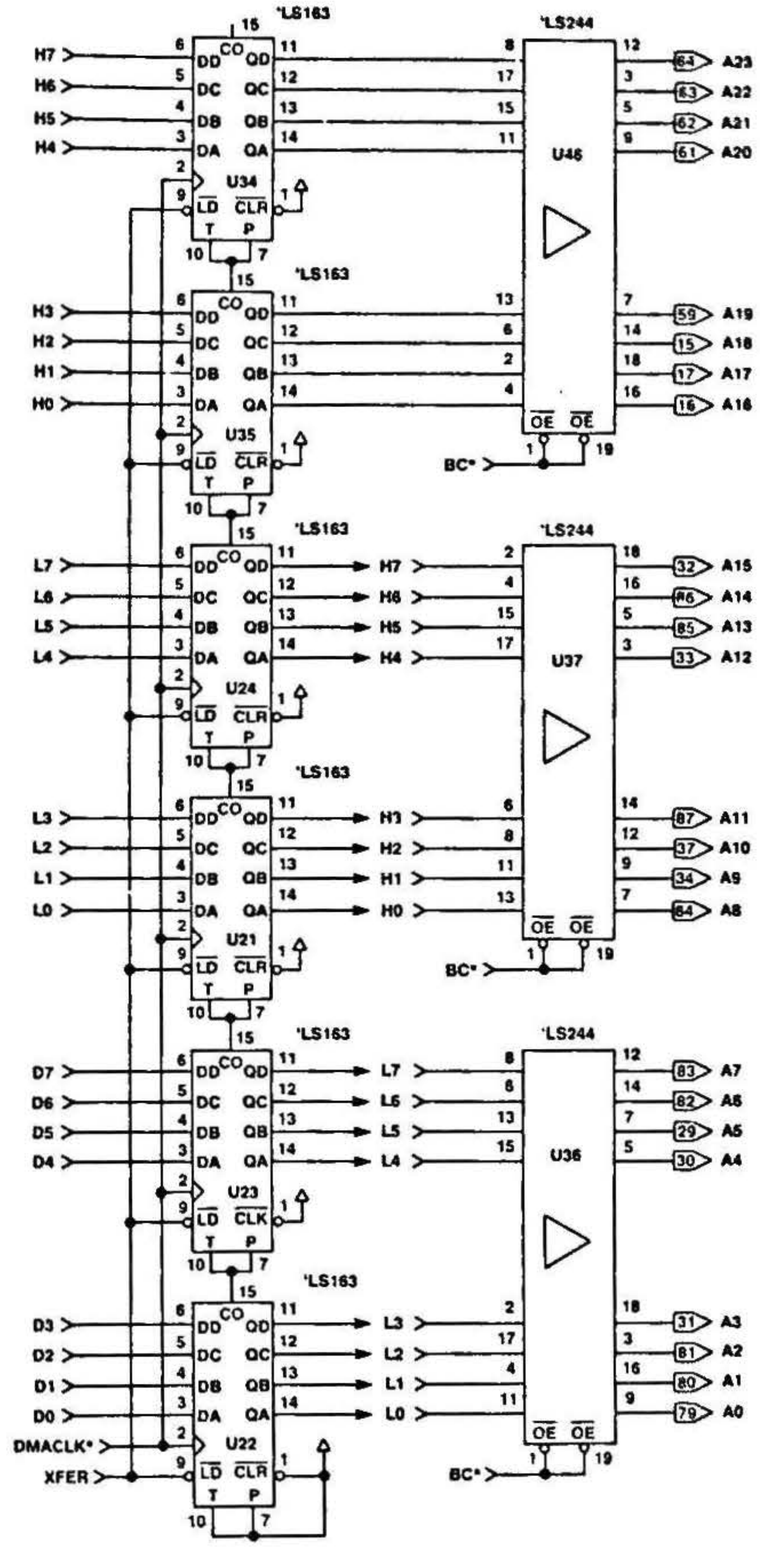

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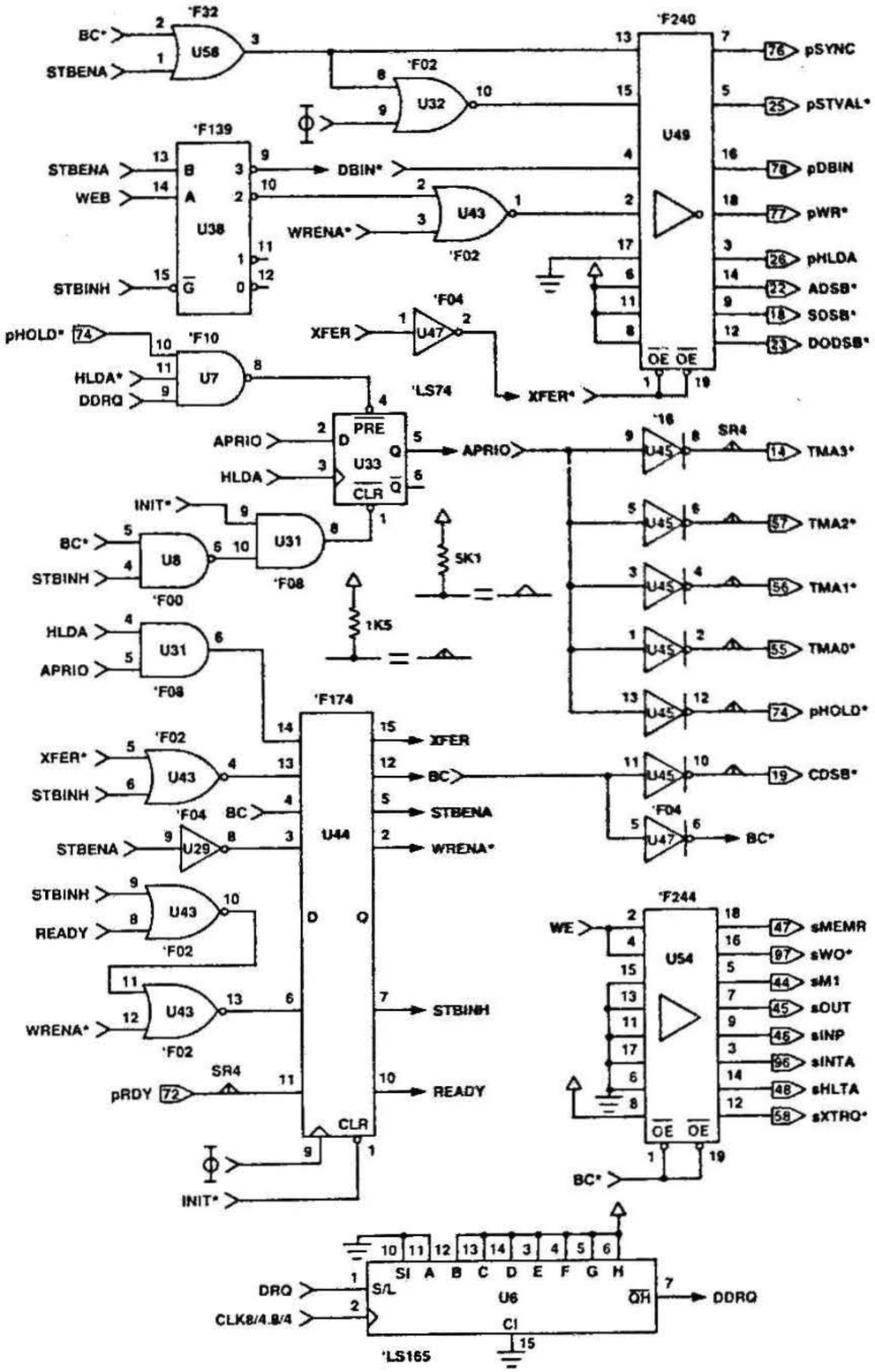

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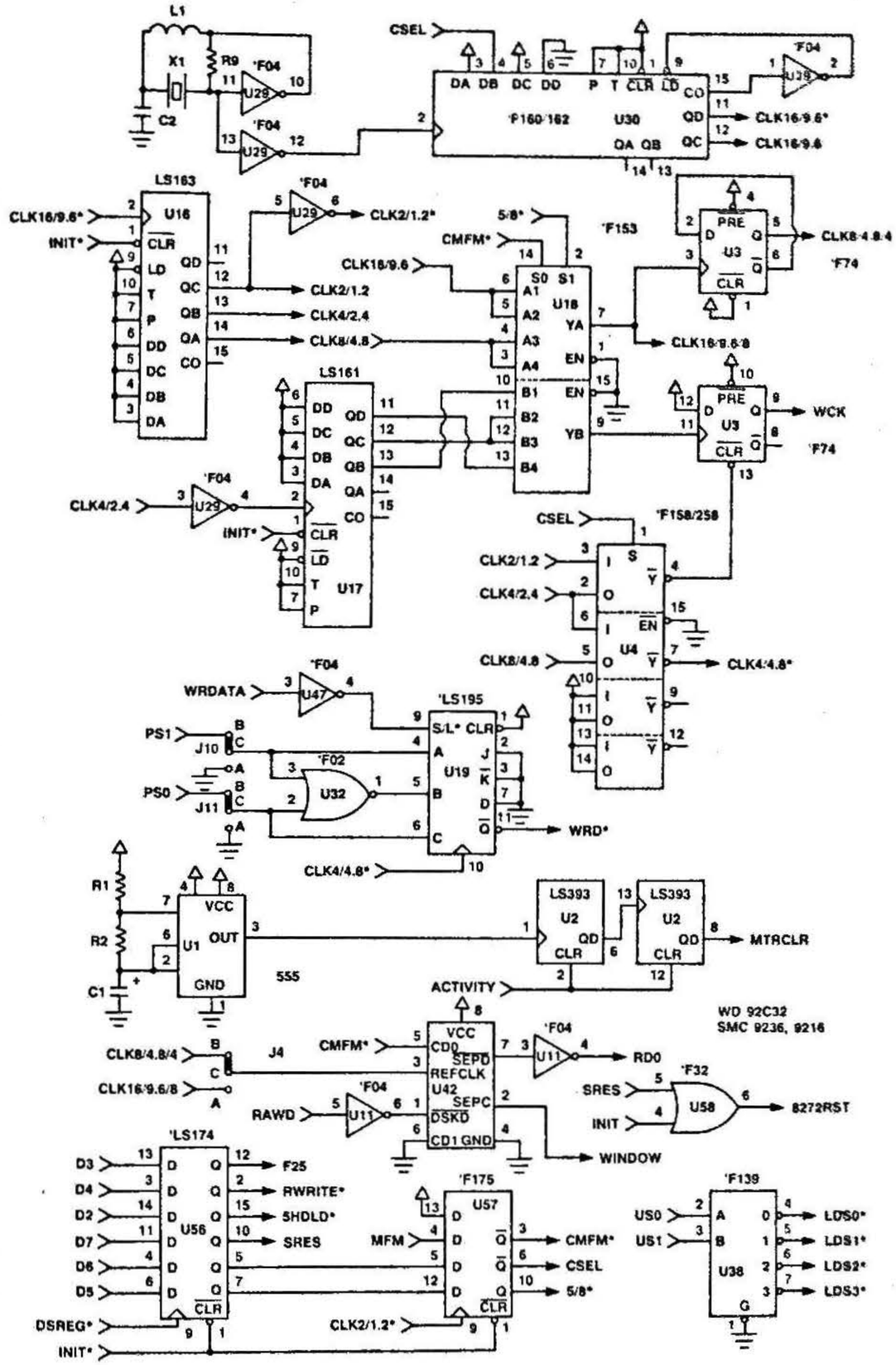

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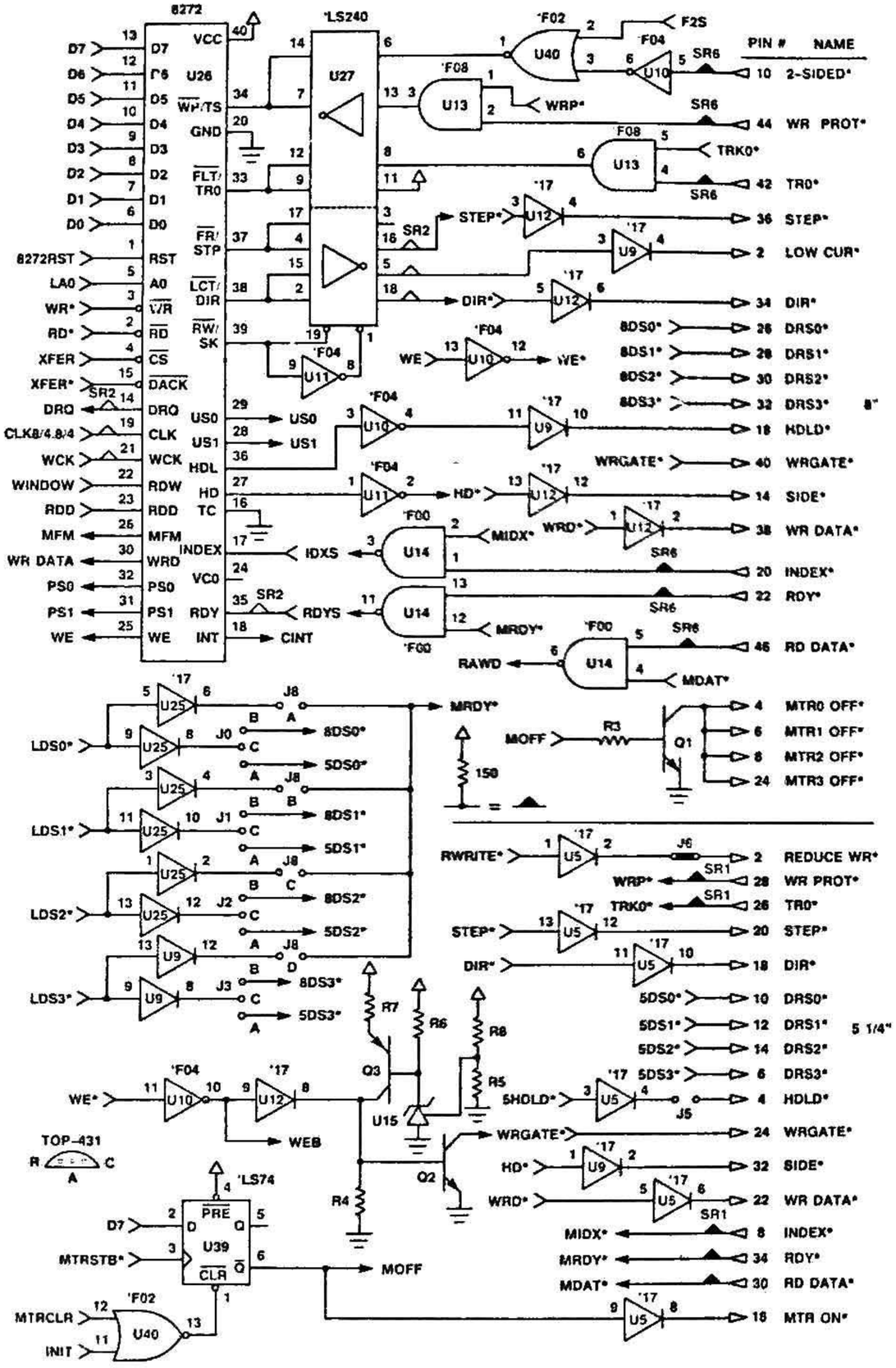

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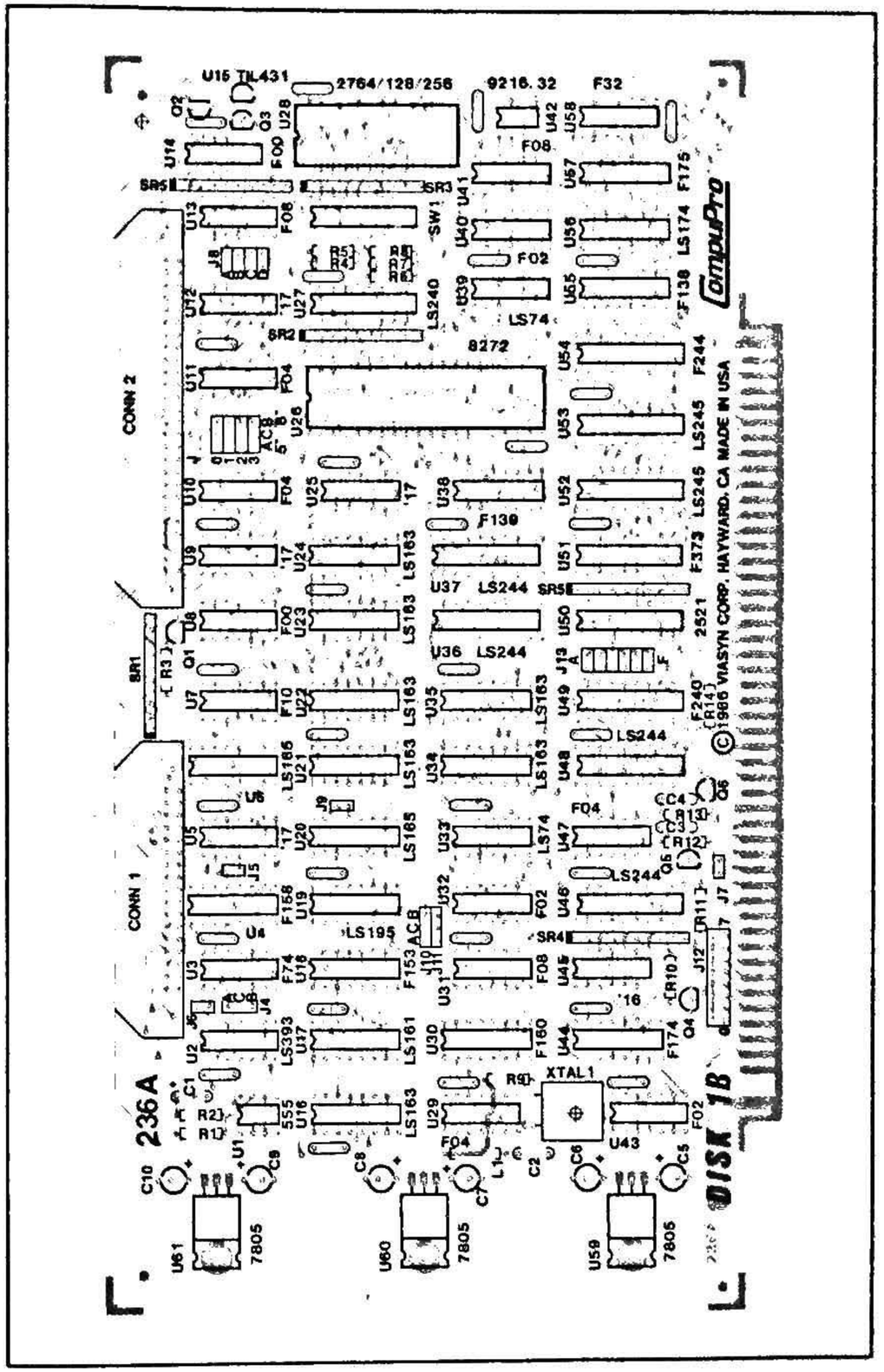
Appendix E

Component Layout



LIMITED WARRANTY

Viasyn Corporation warrants this computer product to be in good working order for a period of 180 days from the date of shipment from the factory, or 90 days from the date of retail sale of the product to the original end user, whichever comes first. Should this product fail to be in good working order at any time during this warranty period, VIASYN will, at its option, repair or replace the item at no additional charge except as set forth below. Repair parts and replacement products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of VIASYN. This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse or unauthorized modification of the product. To obtain service under this warranty the item must be returned to VIASYN as described below.

If you need assistance, or suspect an equipment failure, always contact your Viasyn Reseller first. If you are not satisfied by the actions taken by your Viasyn Reseller, please call VIASYN at (415) 786-0909 to obtain a Return Material Authorization (RMA) number, or write to VIASYN at 26538 Danti Court, Hayward, CA, 94545-3999, Att: RMA. Be sure to include a copy of the original bill of sale to establish a purchase date. If the product is delivered by mail or common carrier, you agree to insure the product or assume the risk of loss or damage in transit, to prepay shipping charges to VIASYN and to use the original shipping container or equivalent. Be sure to mark the RMA number on the outside of the shipping container or delivery may be refused. Contact your Viasyn Reseller or write to VIASYN at the above address for further information.

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If this product is out of warranty, please call or write the VIASYN RMA department to obtain a quotation for factory service. If this product was sold as a system by VIASYN, it may eligible and you may elect to purchase on site/depot maintenance from UNISYS. Contact your Viasyn Reseller, or VIASYN for details.

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In no event shall VIASYN or its service contractor be liable for any incidental, indirect, special or consequential damages, including but not limited to loss of use, revenue or profit, even if VIASYN or its service contractor has been advised, knew or should have known of the possibility of such damages, or damages caused by VIASYN's customer's failure to perform its obligations under this agreement; or claims, demands or actions against VIASYN's customer by any other party.

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