77715775

CONTROL DATA CORPORATION

CONTROL DATA®
WREN™ DISK DRIVE
MODEL 9415-5

THEORY OF OPERATION
DIAGRAMS
MAINTENANCE (NON-SEALED AREA)
PARTS DATA (NON-SEALED AREA)

MAGNETIC PERIPHERALS, INC.
a Control Data Company

Volume 2F

HARDWARE MAINTENANCE MANUAL

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REVISION RECORD

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Address all comments concerning this publication to the distributor or use the enclosed user comment sheet located in the back of this publication.

PREFACE

This Manual provides the information needed to maintain and troubleshoot the CDC Model 9415-5 WREN™ Disk Drive (BJ7D5-A). It is intended to serve customer engineers who require information about the WREN Disk Drive maintenance.

The total content of the Manual is comprised of four sections, each having a unique publication number, and is contained in one volume. The manual's publication number (77715775) along with the unit series code number, should be used when making reference to the WREN-5 Disk Drive Hardware Maintenance Manual.

The following table identifies the content of this manual.

SECTION NUMBER	TITLE	PUBLICATION NO.
*4	Theory of Operations	77715776
5	Diagrams	77715777
6	Maintenance	77715778
7	Parts Data	77715779

* Sections 1, 2 and 3 are provided in the WREN Disk Drive Installation/ Operation Manual P/N 77715771.

TABLE OF CONTENTS

4.1 INTRODUCTION

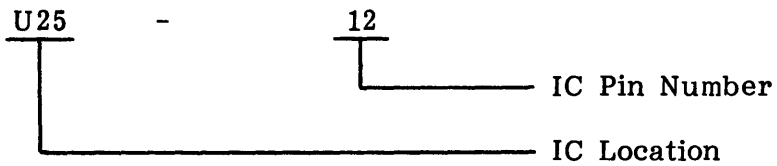
The theory of operation for the WREN Disk Drive will be in two parts: the mechanical and the electrical descriptions. The theory describes typical operations and does not list variations or unusual conditions resulting from unique system hardware or software environments.

The general block diagram of the WREN is shown in Figure 4-1. As the theory proceeds various block diagrams will be used to aid in the interpretation of the systems.

Diagrams used in this section are simplified for instructional purposes and may not agree with those in later sections. Where conflicts arise, the logic diagrams of Section 5 of this manual take precedence.

Logic signal names may be followed by the symbol "+L" or "-L". Active high (+4 Volts for TTL or -0.8 Volts ECL) have "+L" while active low (+0.8 Volts for TTL or -1.7 Volts for ECL) have "-L". ECL signals may also indicate active high with "-P" and active low with "-N" suffix.

Integrated circuit pin will be identified by IC location and pin number. For example "U25-12" is pin 12 of IC U25. The IC locations appear on each device in the logic diagrams.



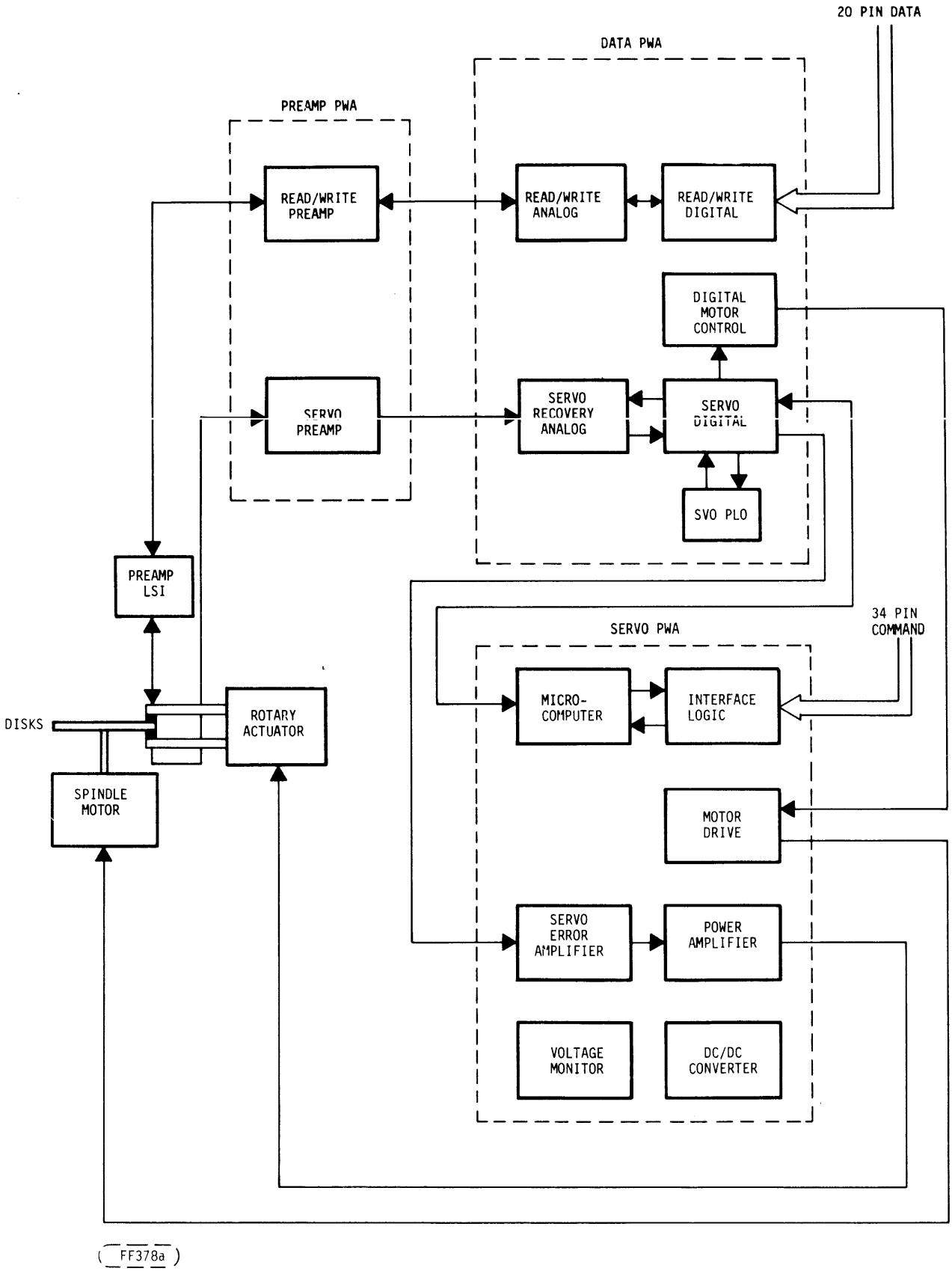


FIGURE 4-1. WREN-5 GENERAL BLOCK DIAGRAM

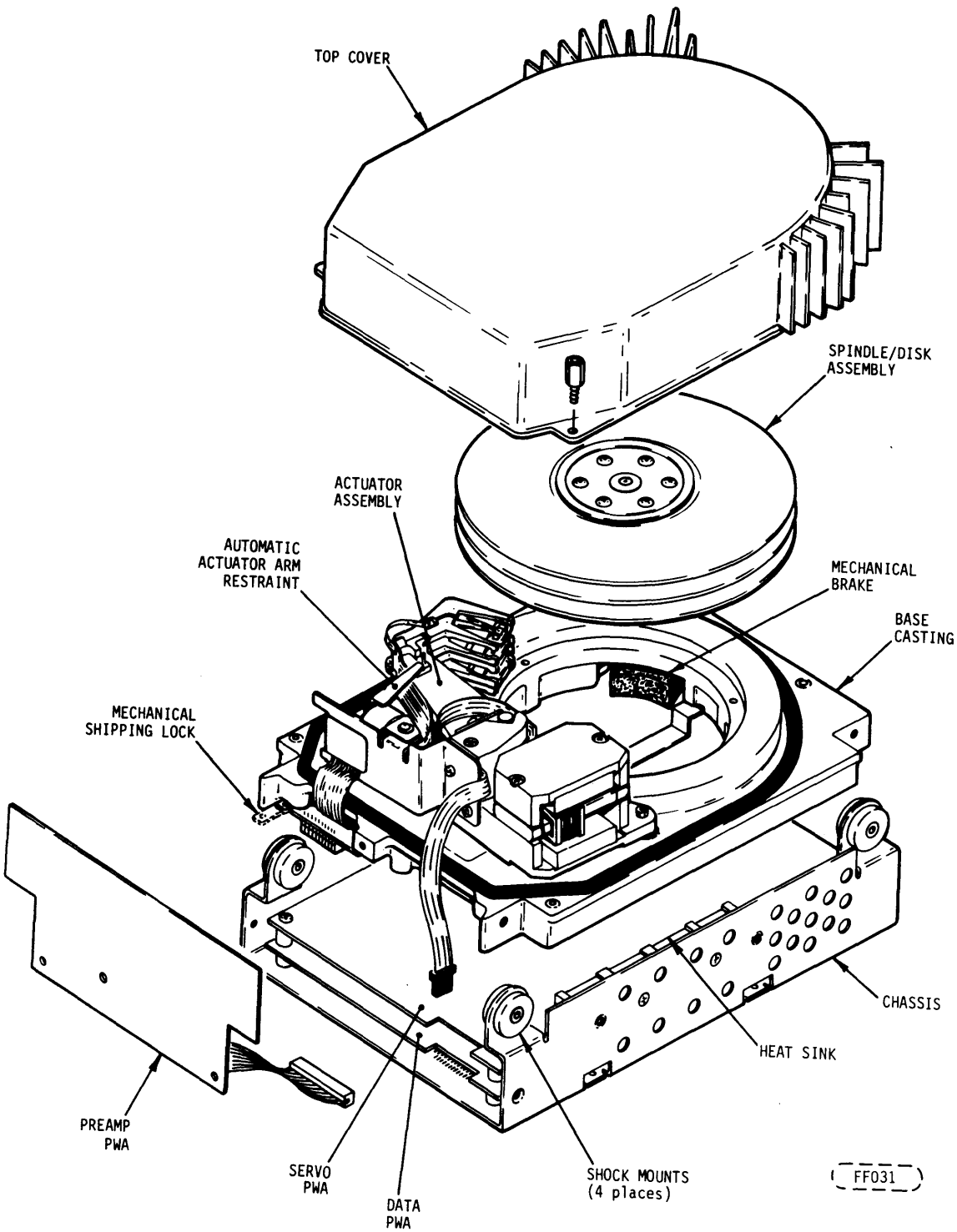


FIGURE 4-2. WREN MAJOR ASSEMBLIES

4.2 ASSEMBLIES

Figure 4-2 illustrates the physical placement of the major assemblies of the WREN Disk Drive. The following paragraphs describe the operation of these assemblies.

4.2.1 MECHANICAL ASSEMBLIES

There are just two major subassemblies which make up a WREN disk drive (Figure 4-2). The base assembly contains the media, filtration system and spindle motor. The base is built and tested as a unit and then mated with the actuator assembly. The actuator assembly contains the bobbin, coil, magnets, rotary arm and heads. After the actuator is mated to the base the information needed to position the heads is written on the bottom surface of the bottom disk. This operation is called servo track writing (STW) and will be explained in detail later. After STW the stop is installed and adjusted. The stop keeps the servo head over the servo data and will be adjusted only in connection with STW. The cover assembly is then installed with three screws. These operations are performed in special clean rooms to keep the media contamination free. For this reason the top cover of a WREN should not be removed. The assemblies and components described in the following paragraphs are in an environmentally sealed area and shall be serviced at factory level depot ONLY. See Maintenance Section 6 for the items of General Maintenance.

4.2.1.1 ACTUATOR ASSEMBLY

The WREN actuator is a rotary voice coil positioner. The voice coil can be thought of as a motor that moves through only a small angle. The motor stator consists of two permanent magnets, one upper and one lower, and a core bar (Figure 4-3). The motor rotor is a coil on a bobbin which fits around the stator core. By controlling the magnitude and direction of the rotor current the rotor can be positioned any where in its range. The bobbin is attached to the rotary arm which provides the head mounting.

These are two bearings mounted in a bore thru the area. A shaft runs thru these bearings. This shaft is held in two V shape grooves on the housing which holds the magnets. The housing is later mounted to the base deck. Connection is made to the bobbin thru a three conductor flex cable.

The heads are mounted by screwing them into six slots at the end of the actuator arm. Each head has a short flex cable on it which must be soldered to a flex cable on the actuator arm.

The flex cable on the actuator arm has an SSI115 integrated circuit on it. The signals to and from the five data heads pass thru this circuit. The signal from the servo head passes directly to the connector which passes all signals to the Preamp PWA.

Removal and replacement of the actuator is a depot level maintenance procedure ONLY.

4.2.1.2 BASE ASSEMBLY

The base assembly consists of the base casting, spindle assembly, head actuator assy and two filtration systems as shown in Figure 4-4.

The base casting is the frame of the drive and all assemblies mount to it. The base casting also divides the drive into sealed and unsealed compartments. The area above the base casting and under the cover is sealed and provides a clean environment. The heads in the WREN fly at only 15 to 18 microinches therefore the air in the sealed compartment must be kept very clean.

The spindle to which the disks are attached is an integral part of the spindle motor. The disks are the recording media for the drive. The recording surface of each disk is coated with a layer of magnetic iron oxide and related binders. The WREN also has a lubricant over the oxide, this reduces the friction when the heads are landing. The drive can have up to three disks, each separated by a spacer. The whole assembly is held together by a clamp plate which bolts to the top of the spindle hub. The assembly then is bolted to the base casting with the spindle shaft protruding through the base.

The spindle motor is a two phase brushless DC motor. The motor rotor mounted on the opposite end from the spindle which serves as a braking surface and has fan blades which provides some air flow to cool the electronics. A grounding spring rests on the center of the rotor and bolts to the base casting, this provides a path for any static electricity generated by the head-disk interface to flow to the ground.

The arm restraint solenoid holds the arm and heads over the landing zone next to the spindle when power is not applied. The shipping lock reinforces the holding action to assure heads will not move during any shocks that may occur during shipping.

A brake on the bottom of the drive presses against the rotor of the spindle motor anytime power is not applied to the drive. This brake stops the spindle quickly to protect the surface of the disk in the landing zone.

The first of the filtration is an absolute filter. It is bolted over a hole in the base casting and provides clean air to equalize the pressure between the sealed compartment and the outside world. The second system is a recirculating filter. It removes any foreign material that may be present in the sealed compartment. Air is pulled out of this filter by the low pressure created near the spindle. Air then can circulate thru open areas in the spindle and flow out across all the disks. Some of the air will flow through this filter whenever the disk is spun. Over the life of the drive all the air in the sealed compartment will be cleaned many times.

Any servicing of the spindle assembly, spindle motor and filters is a depot level procedure ONLY. ENCROACHMENT OF THE SEALED AREA VOIDS THE UNIT WARRANTY.

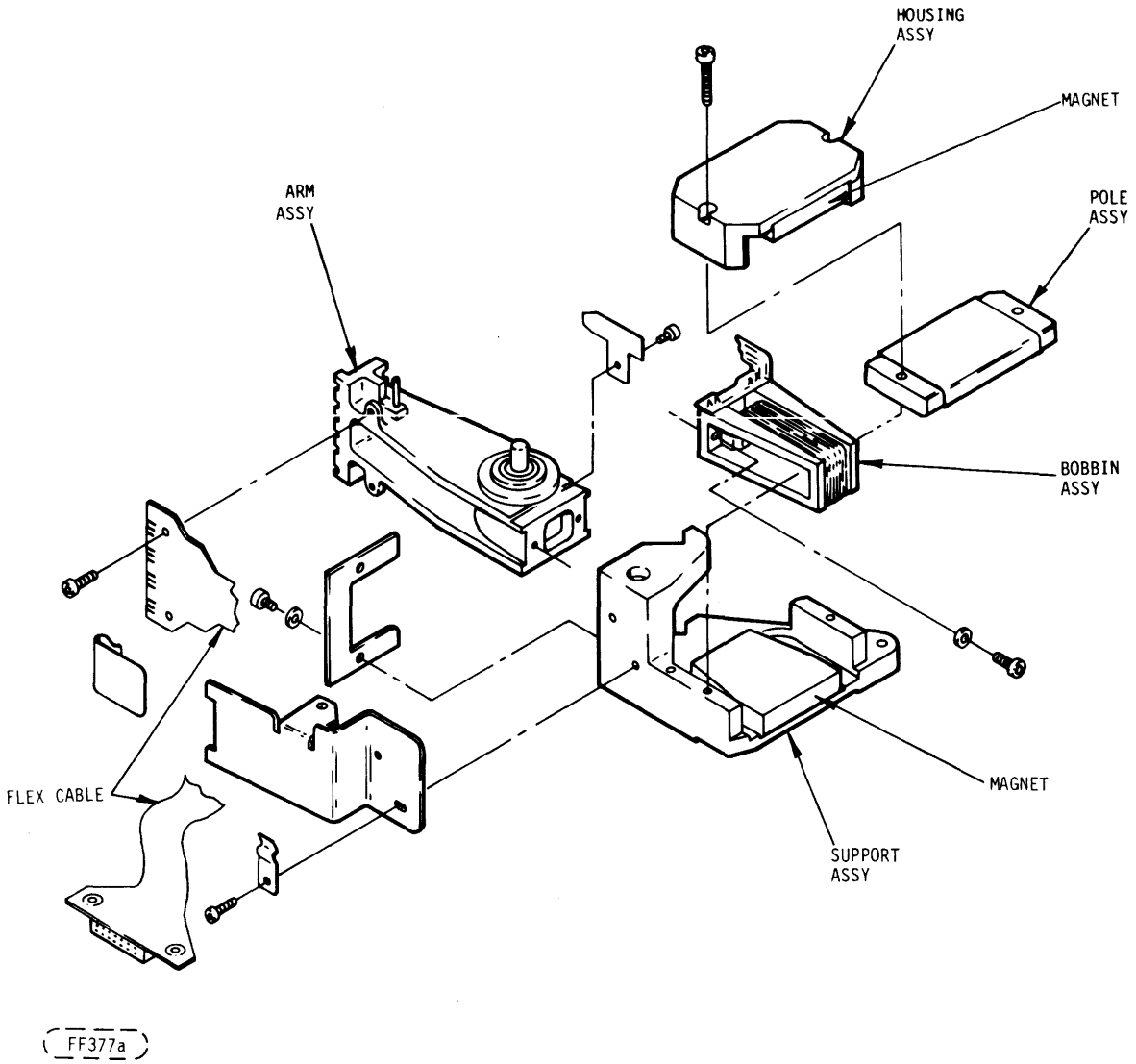


FIGURE 4-3. WREN ACTUATOR ASSEMBLY

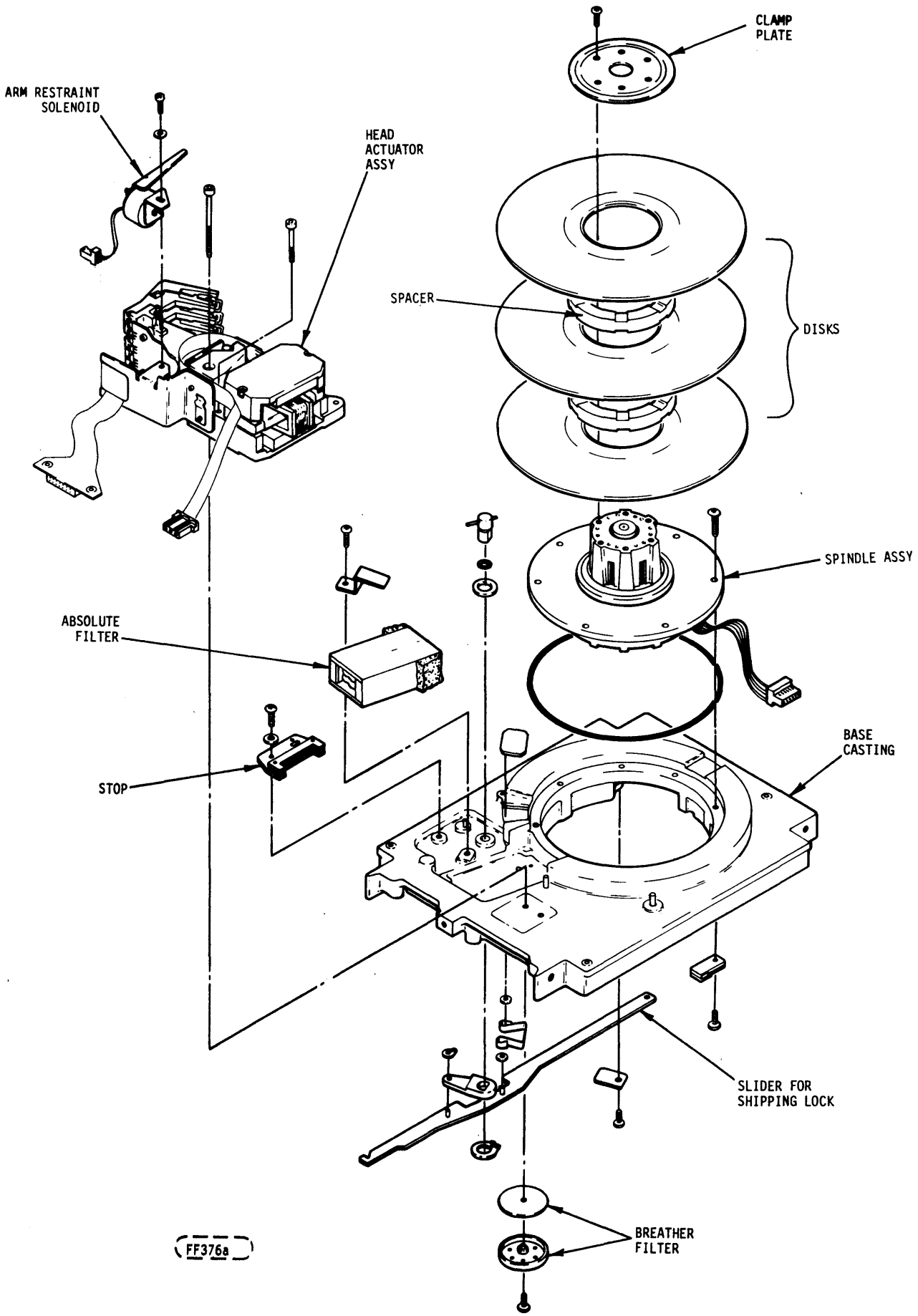


FIGURE 4-4. WREN BASE ASSEMBLY

4.3 FUNCTIONAL DESCRIPTION

4.3.1 GENERAL

This description is organized into the following major headings:

- Overall Drive Control System
- Head Positioning System
- Read/Write System
- Auxiliary Systems

4.3.2 OVERALL DRIVE CONTROL SYSTEM

The WREN is under the control (excluding any control exerted by the controller via the interface lines) of the Microcomputer on the Main PWA. The Microcomputer system is described in the following paragraph 4.3.2.1. Any further details of the Microcomputer Theory must be taken from vendor publications for the various chips in the Microcomputer System.

4.3.2.1 MICROCOMPUTER OVERVIEW

Figure 4-5 shows a simplified block diagram of the microcomputer. The microcomputer is an 8749 with two kilobytes of internal program memory. It also uses an 8243 port expander to increase the number of output signals. The microcomputer has no control of the read/write section with the exception of the write current magnitude.

When a step is received from the command cable interface, it is synchronized with the microcomputer clock and applied to the Test 1 input of the 8749. This causes a counter to be incremented with each step pulse. The interface direction line is latched with the step pulse and applied to one of the Bus Port inputs. These two lines have all the information needed to cause a seek operation.

When a seek is in progress, track-crossing pulses are generated in the servo LSI logic; these are applied to the 8749's Interrupt input. This input remains active until the Interrupt is serviced and a track-pulse reset is sent to the servo LSI on a Port 2 line. In this manner, the microcomputer keeps track of all incoming step pulses and track crossings that occur. The address latch enable (ALE) signal is sent to the spindle motor control as a clock for the speed regulator. During a seek, a seven-bit velocity command is output on Port 1 and goes to a D/A converter in the servo amplifier. The eighth bit on Port 1 is active for a high velocity command, and inactive for a low velocity command. A line from the port expander, titled "VCLO" (Velocity Command Low) is active for a low velocity command, and inactive for a high velocity command. The FINE signal puts the servo system into either the fine or coarse mode of operation. This signal is used in conjunction with the forward/odd lines. Forward refers to a seek from a lower to a higher numbered cylinder. In the coarse mode, this line is active during a forward seek and inactive during a reverse seek. When the drive switches to the fine mode this line is active when the target track is even and inactive when the target track is odd.

The Power On Reset signal originates from the port expander. During start-up, Power-On Reset is active for approximately 6 seconds. This enables the current regulator in the spindle motor control. When it is inactive, it enables the speed regulator. It is also used to provide appropriate resets to sequential logic contained in the drive electronics. During start-up, motor speed is monitored on the Bus Port from the Motor Speed line. The phase lock oscillator (PLO) lock line is continuously monitored. Also during start-up, the servo is disabled via the Servo Disable line.

When the servo PLO is locked and the spindle motor is up to speed, head loading can commence. This is accomplished by the microcomputer issuing a velocity command, detecting guard band, performing an RTZ, and switching back to fine mode on cylinder zero. The data zone latch is set by Index. Index code is written only in the data zone. This enables the microcomputer to distinguish between the data zone and the start zone.

There is a guard band latch external to the microcomputer that will disable the servo if guard band is encountered after the initial head load. During the head loading, this latch is disabled while setting on Track "0" or while performing a seek to Track "0". This is true because Track "0" is in the guard band. This disable is activated by the guard band latch clear line from the port expander.

There is one other input to the Bus Port, called Test Seek. This input can be grounded with a jumper shunt and causes the drive to go into a continuous test seek following head load and the calibrate operation.

With the completion of head load, the microcomputer puts the drive through an automatic calibration procedure. During the calibrate sequence, a test seek is performed and timed by the mcrocomputer. When the microcomputer detects that the test seek is too slow, a short pulse is output on the Velocity adjust line. This pulse causes the automatic gain control (AGC) amplifier gain to decrease one step. This sequence is then repeated until the test seek is performed in the required time. The drive then returns to cylinder zero and sets the ready line. The ready line serves to indicate that the drive is on cylinder and ready to read or write. It will be false whenever the heads are outside the data zone. The SEEK COMP line issues a pulse at the end of a seek to set the seek complete latch.

A servo will be disabled and the ready line made false at any time that loss of servo PLO lock is detected. A timing diagram for the step-pulse synchronizer is shown in Figure 4-6.

4.3.2.2 MICROCOMPUTER FIRMWARE ROUTINES

The flow charts that follow illustrate the manner in which the microcomputer controls servo operation in the WREN. Figure 4-7 shows a chart of the primary modules that make up the WREN firmware. On power up, the program starts and always returns to the Main Idle module. During start-up, the program exits the Main Idle module and goes to the System Initialize module. Following System Initialize, it then goes to the Head Load module. Upon completion of Head Load, the program branches back to the Main Idle loop.

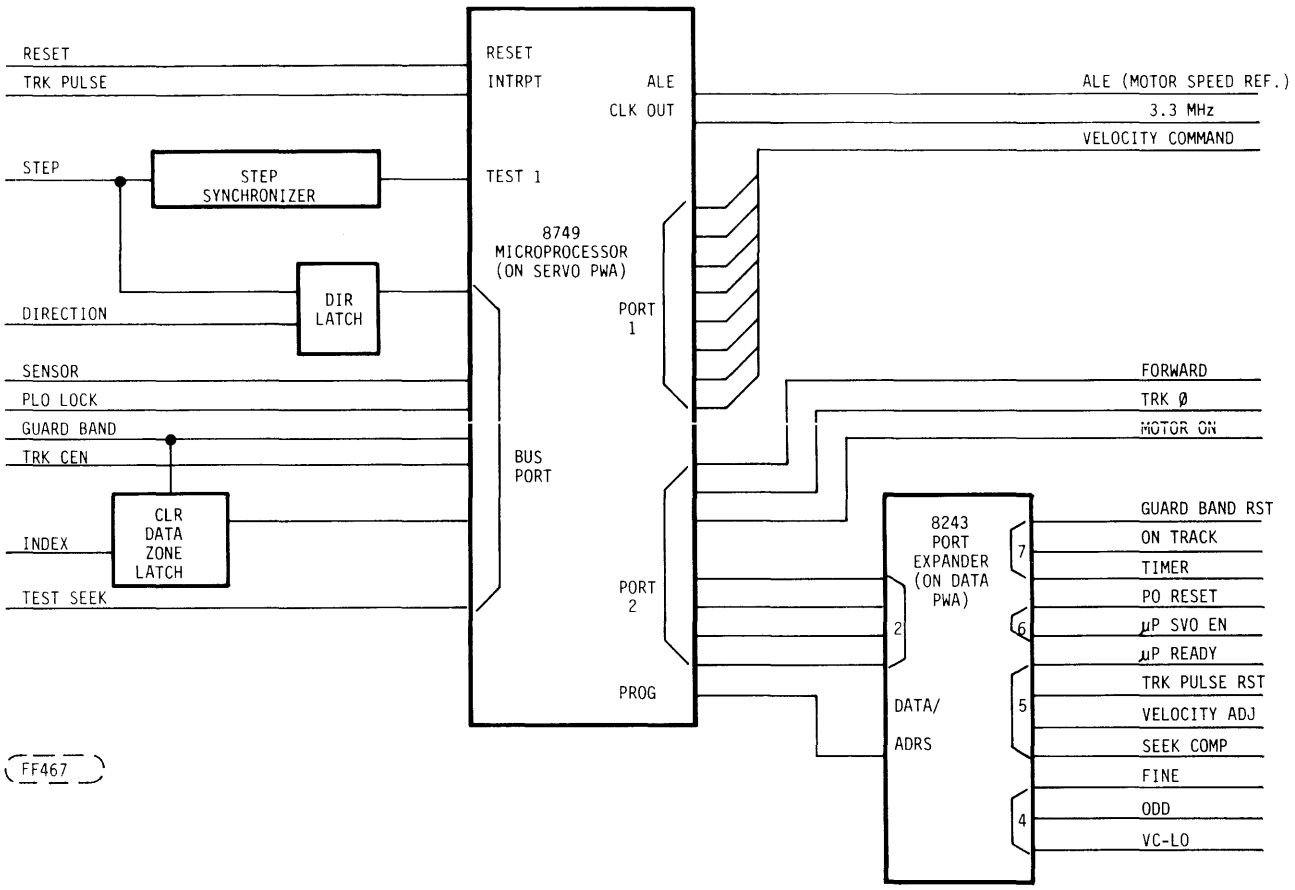


FIGURE 4-5. WREN MICROCOMPUTER BLOCK DIAGRAM

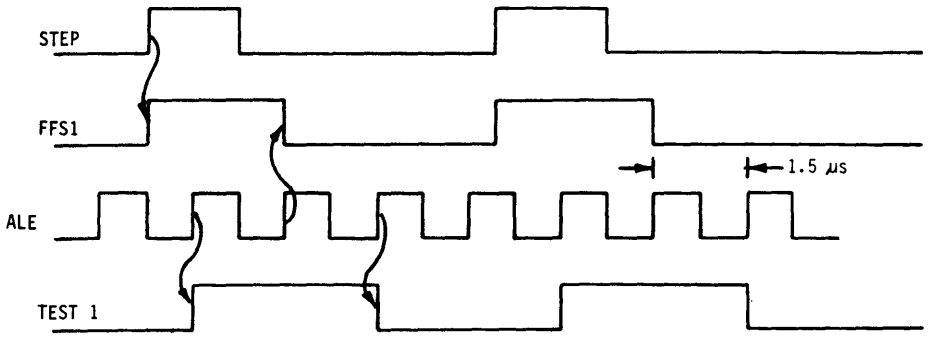


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FIGURE 4-6. WREN MICROCOMPUTER STEP PULSE SYNCHRONIZER

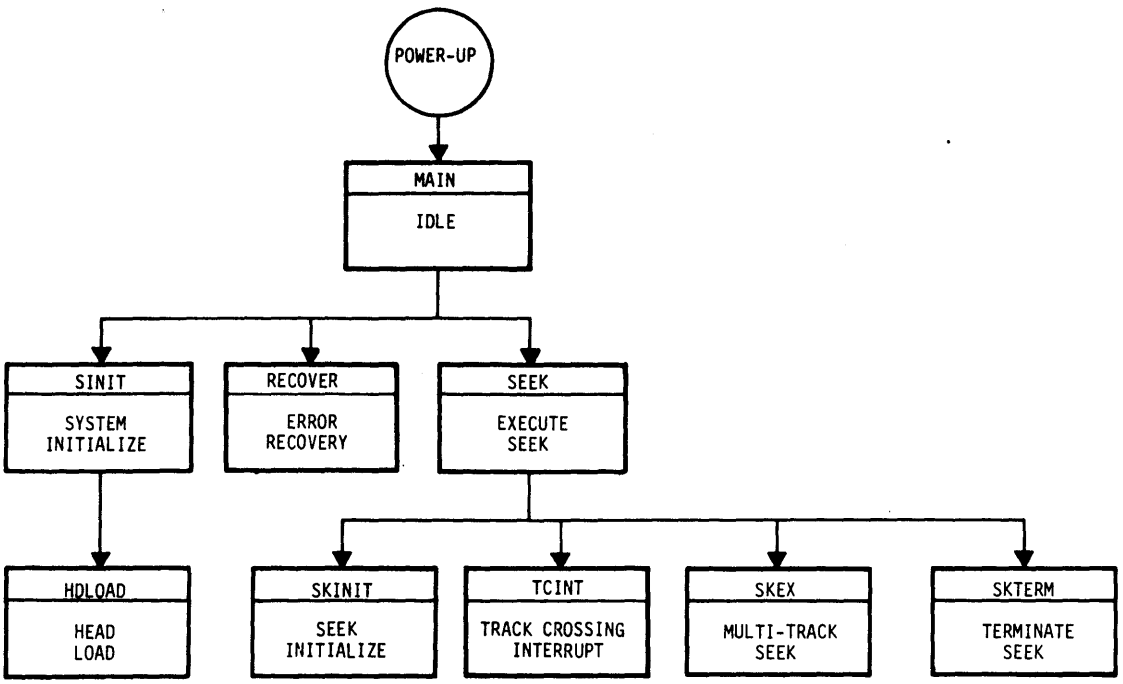

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FIGURE 4-7. FIRMWARE MODULE CHART

(A) Main Idle Loop Module

Assuming a normal power-up sequence has been completed, the program goes to the Main Idle loop (Figure 4-8). Upon receipt of a Step pulse, the program will branch to the Seek module. From the Seek module, it proceeds to the Seek Initialize module. From the Seek Initialize module, it branches to a seek execution module. At the conclusion of a seek, it will go to the Terminate module. Upon completion of the Seek Terminate, it will return to the Main Idle Loop.

In the Main Idle Loop the processor checks for three possible status fault conditions (1) incorrect motor speed, (2) loss of servo PLO lock and (3) servo system disabled (an internal flag). If a Status Fault condition is present, the program will go into one of several recovery routines. Normally it is during this time that the servo is disabled and the heads would be reloaded. In the event of a servo disable, the microcomputer will automatically attempt to reload heads to cylinder zero. If there are six unsuccessful attempts, a trap state is entered. Operator intervention is the only way out of a trap state. Cycling power will restart the program and a new System Initialize sequence will be attempted.

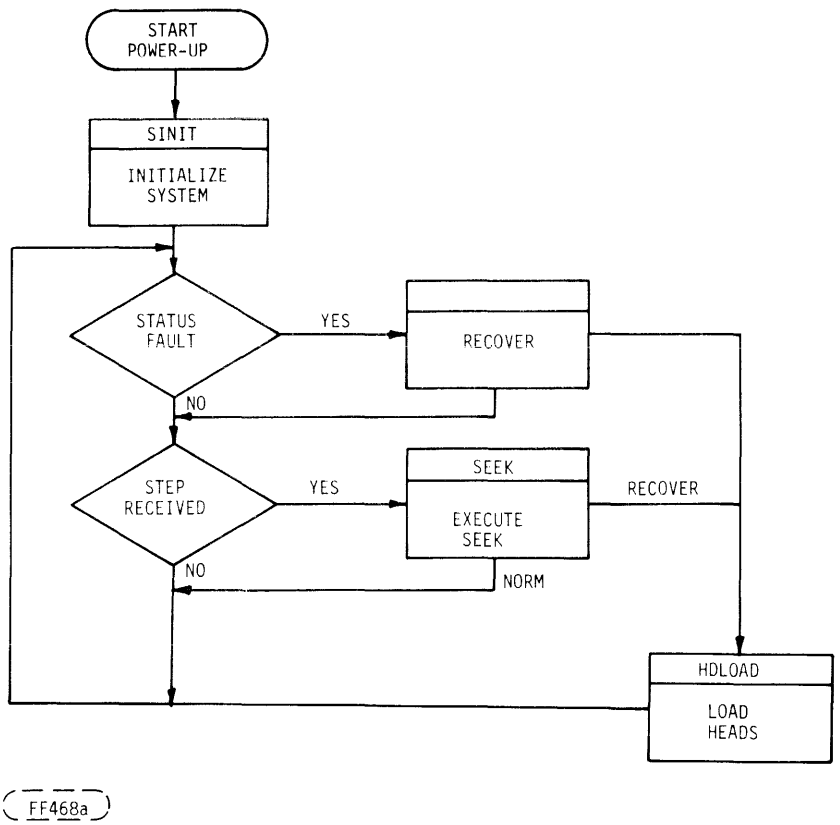

FIGURE 4-8. MAIN IDLE MODULE

(B) System Initialize Module

The System Initialize module (Figure 4-9) starts with processor self-tests, then issues a System Reset for 4 seconds to bring the motor up to speed. A speed check is made, then the program branches to the Head Load routine. Following the Head Load, a velocity test is performed. This test will be attempted repeatedly, incrementing the velocity each time the test fails, until the test passes. There is then a check to see if the seek test pin has been grounded, and if so, the seek test continues. If not, errors are checked and the module returns to the Main Idle loop.

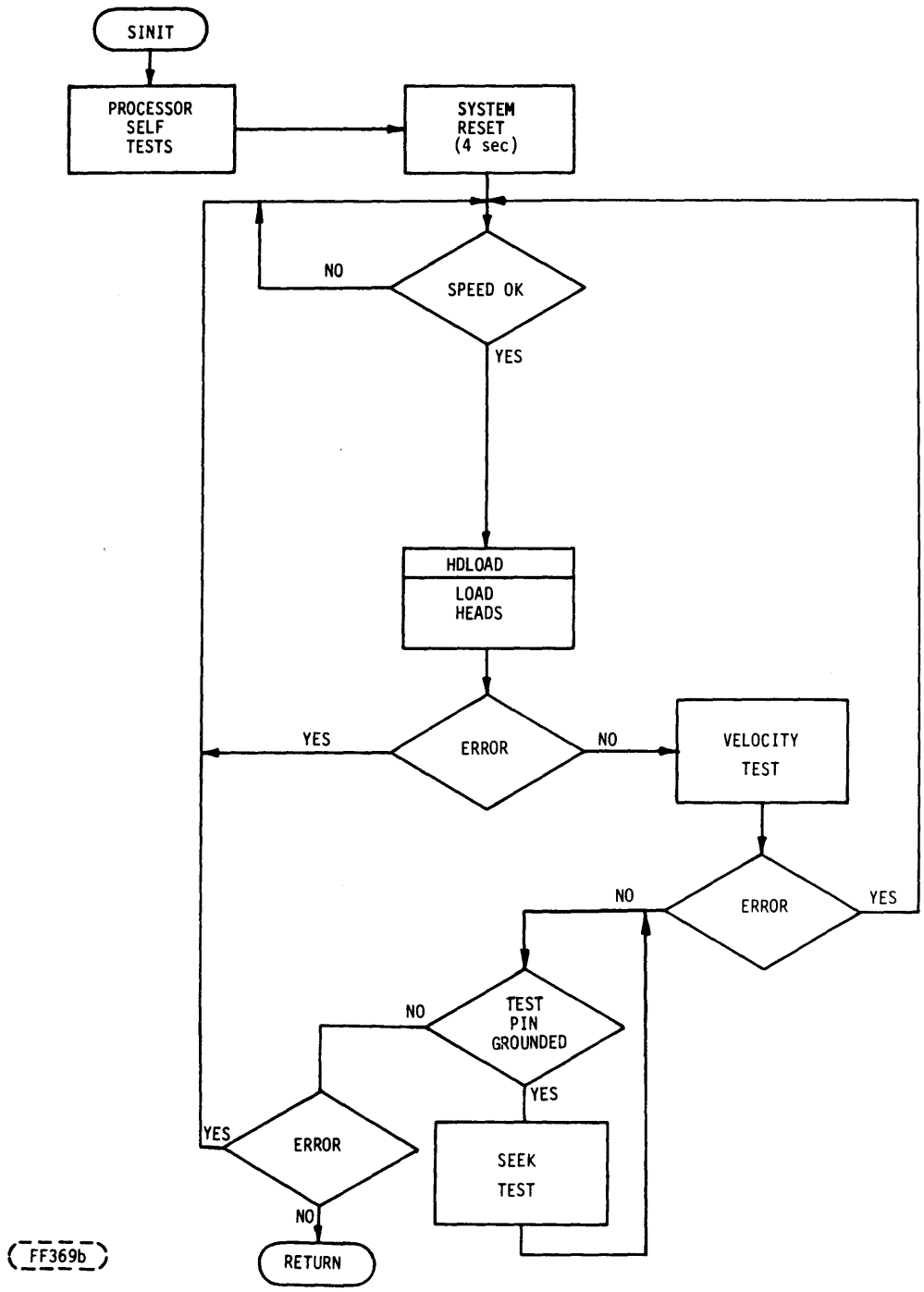

FIGURE 4-9. SYSTEM INITIALIZE

(C) Head Load Module

In the Head Load routine (Figure 4-10) the presence of a guard band dibit signal pattern is checked. In the start zone, there should be no guard band. Next the data zone is checked. If the head load is occurring during a power-up, the data zone flip-flop may be in an ambiguous state. In this case the data zone check is skipped.

The next step is to move the arm out of the start zone across the disk and to position it on Track 0.

The head load velocity command is issued, the reverse and coarse load are enabled, the guard band detector is disabled and the positioner movement begins. After guard band is detected, the sequence continues looking for the exit of guard band. After exiting guard band, the first track-crossing pulse detected sets the Odd and Fine mode. The guard band latch is now enabled.

If during the start of a head load, the guard band is detected in the start zone, the servo will be enabled and set in Forward. This is an attempt to drive the arm back into the start zone. It should be noted that during a head load sequence at this point, if data zone is detected the same form of recovery results.

After the arm is commanded to move a timer will be started in anticipation of detecting guard band. If this timer times out, the servo is disabled. Once in guard band, a similar time-out test occurs which if failed also results in disabling the servo. Following exit of guard band, if a track crossing is not detected within an appropriate time-out, the servo will also be disabled.

The Disable Servo Routine (DISSVO) is described in Figure 4-18, sheet 4-23.

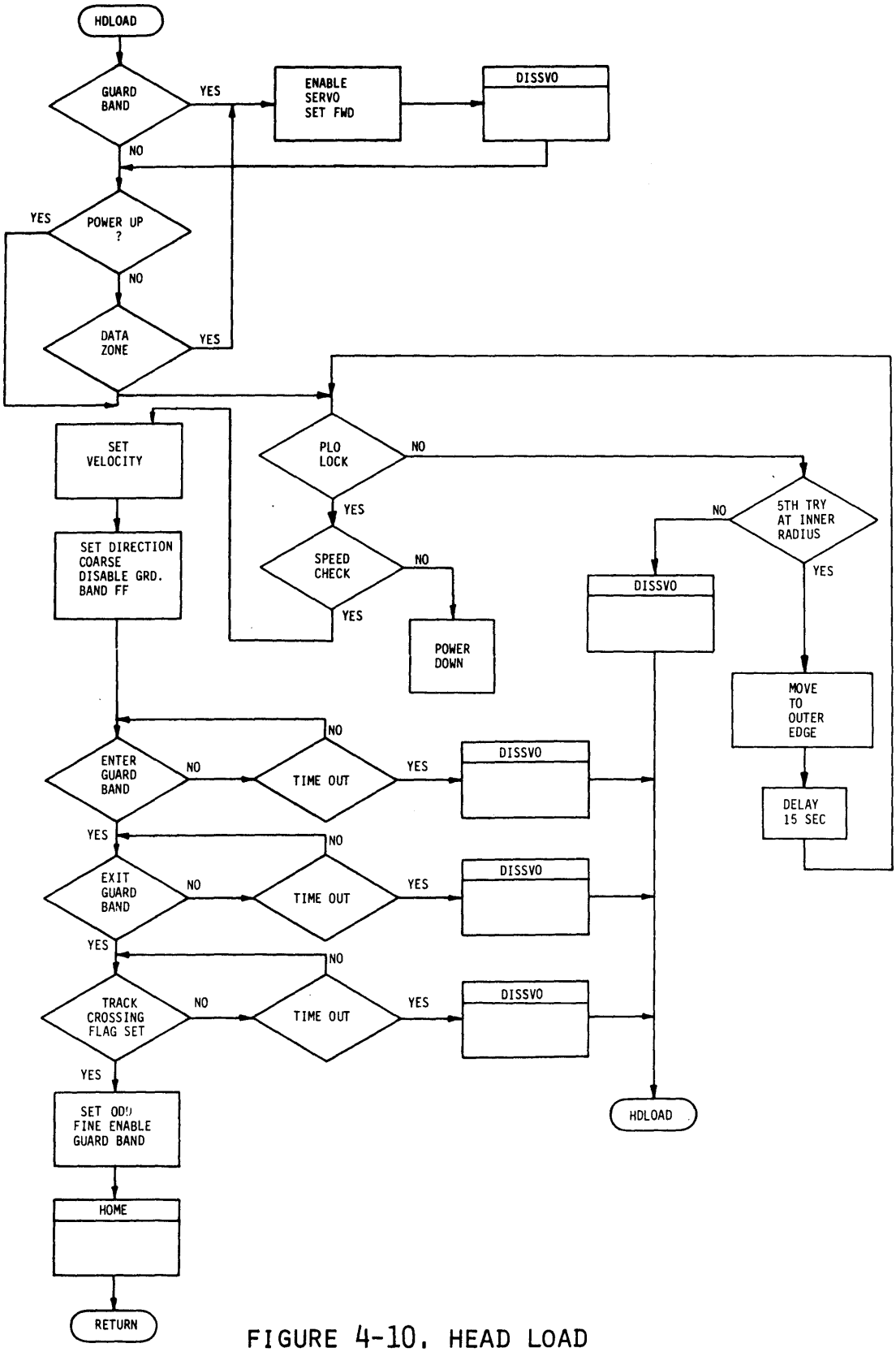

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FIGURE 4-10. HEAD LOAD

(E) Execute Seek

When a Step pulse is received from the command interface, a branch is made from the Main Idle loop into the Seek module (Figure 4-12). First a Seek Initialize routine is carried out. This will be covered in a later paragraph. Next the seek length is calculated based on a number of Step pulses that have been received to this point. A test is performed to determine if the seek length has exceeded the limit of the data zone. If this occurs, an automatic RTZ is performed by branching to the Home or RTZ module. If the step limit has not been exceeded, a branch is made to Seek Execution module. On return from the seek module, the program will continue into the Seek Terminate module, and finally a return to the idle mode.

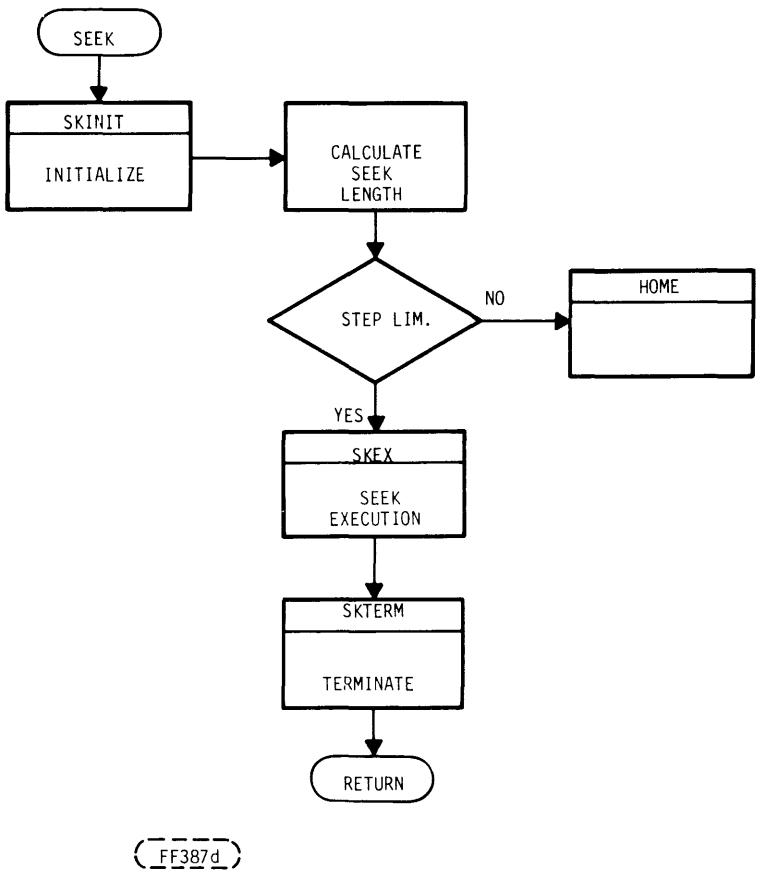

FIGURE 4-12. EXECUTE SEEK

(F) Seek Initialize Module

In the Seek Initialize module (Figure 4-13), the direction input is read and stored. Next all initial conditions are saved and the step limit, or a number of steps acceptable without exiting the data zone, is calculated. There is then a return to the seek module. Once a seek has started, when a cylinder is crossed, a track crossing interrupt will be received (Figure 4-15). When servicing the interrupt, the current address counter is updated. Next the track-crossing flag will be set, the interrupt logic will be cleared and there is a return to the sending module.

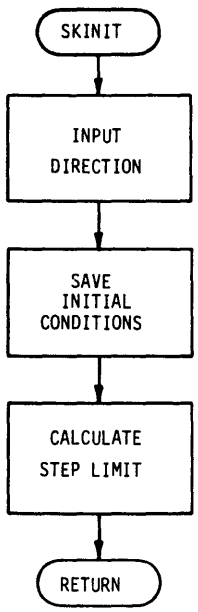

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FIGURE 4-13. SEEK INITIALIZE

(G) Multi Track Seek Module

The Seek Execution module (Figure 4-12) first sets the direction and coarse mode, then a large loop is entered. While the seek is taking place, the status is monitored. If an error occurs, the servo is disabled. The step count is also monitored. A step limit has already been established at this point, and if it is exceeded, a return is made to the main seek module. Each time the step count is determined, the number of steps left can be calculated. This value will determine the velocity to send. This loop is exited when only one step is left in the seek, at which time it must be determined if this was a one-track seek to begin with or not. If it was, nothing is done to the velocity at this point, but if this was a multi-track seek, an intermediate velocity is sent out. Then when track center is observed, the one-track seek velocity is sent. In either case, the last track-crossing interrupt is expected. If it does not come soon enough (or if track center does not come for a multi-track seek) the Disable-Servo routine is called and a return made to the main seek module. If the last track-crossing interrupt is detected, the new track address is calculated, fine mode is set, and return is made to the main seek module.

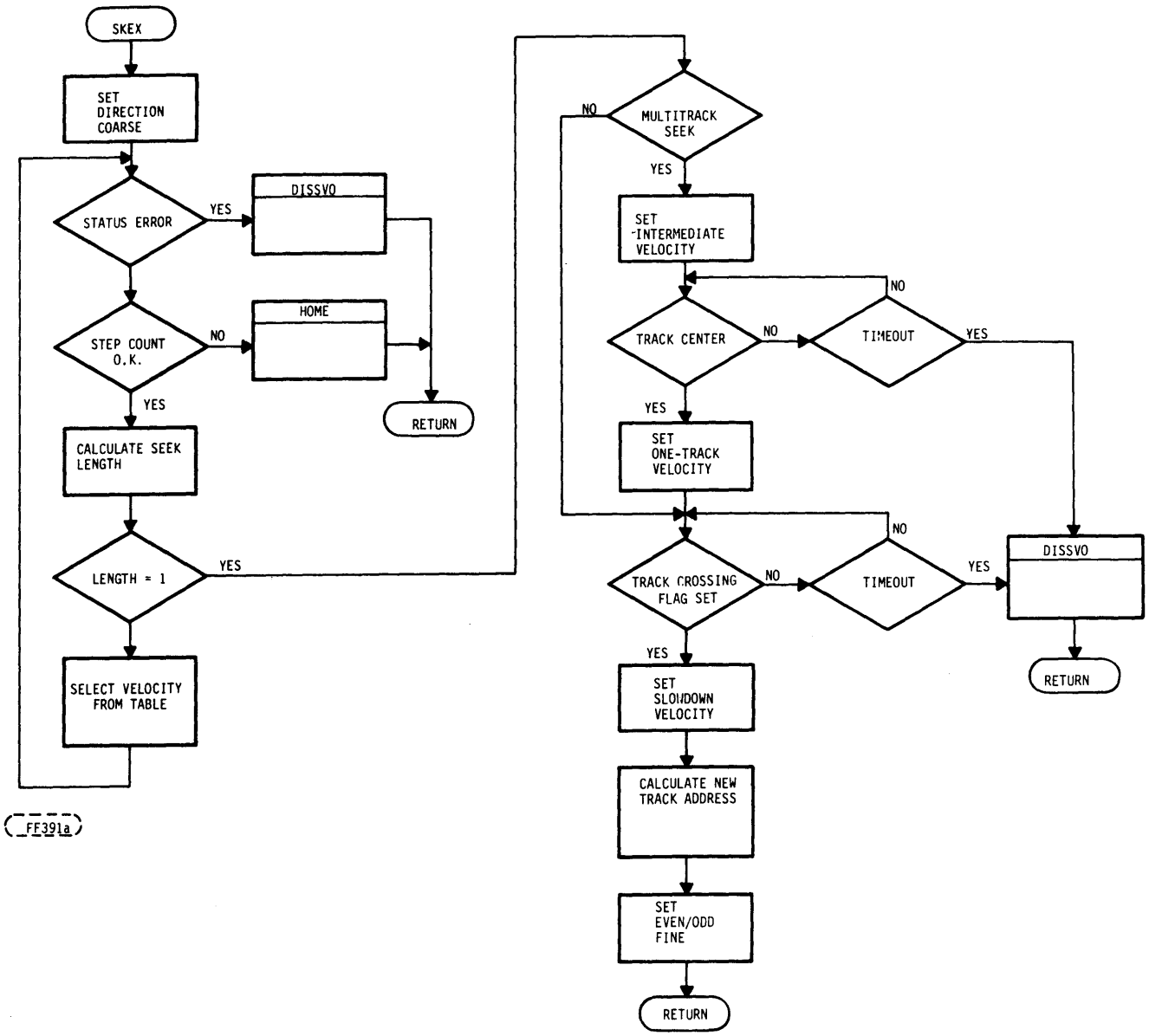

FIGURE 4-14. MULTI-TRACK SEEK

(H) Track Crossing Interrupt Module

The Track Crossing Interrupt updates the counter that records which track the head is on. It also sets a track crossing flag so that the multiseek module knows when a track is crossed.

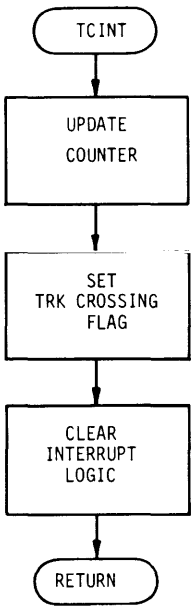

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FIGURE 4-15. TRACK CROSSING INTERRUPT

(I) Seek Terminate Module

The Seek Terminate module is used to complete a seek. The system is in Fine mode upon entering this module. First an eight-bit word is output on Port 1. This word sets the write current level used if a write command is received for this cylinder address. Then a track-center signal is detected which starts a settling timeout. This lasts approximately three microseconds. Lastly, firmware counters are reset.

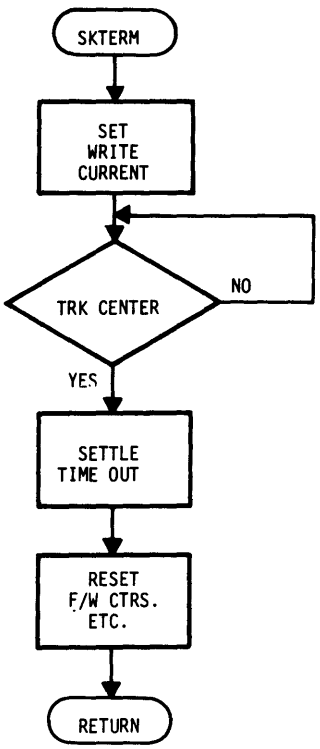

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FIGURE 4-16. SEEK TERMINATE

(J) Error Recovery Module

The Recover module (Figure 4-17) first checks the PLO lock, if the PLO is unlocked, filter runout is checked. If not, a check for servo error is made. Filter runout is checked on error. Next guard band is checked, if guard band is found, the guard band filter runout is checked. If guard band is not found, control is turned back to the calling module. This completes the fast recover module. If filter runout is not all right, Disable servo is called first.

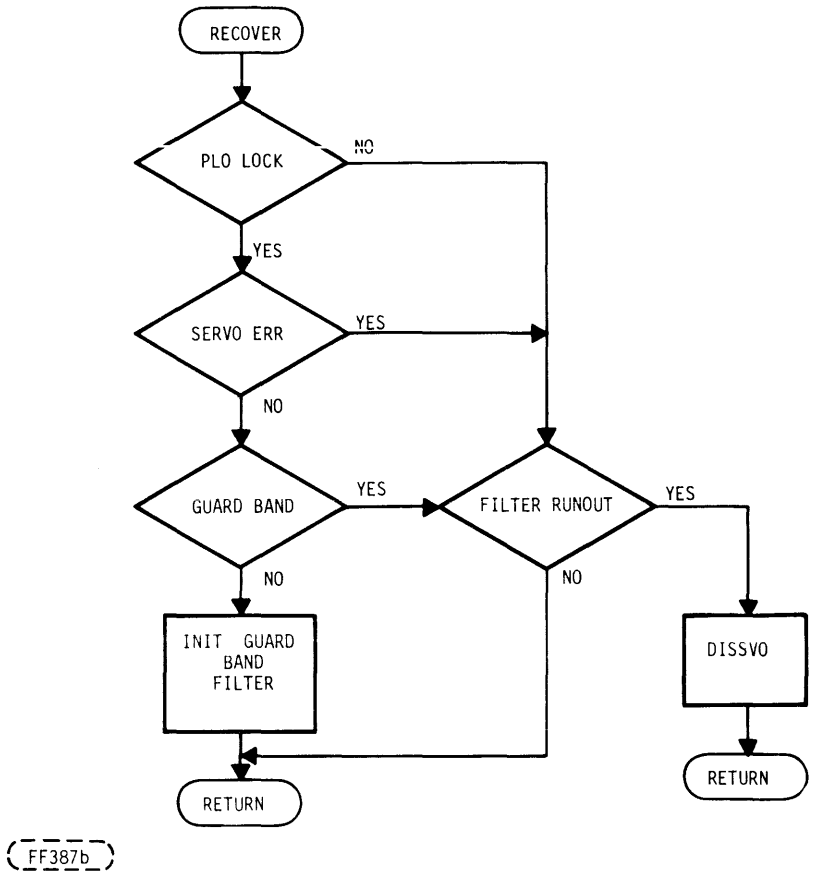


FIGURE 4-17. RECOVER

(K) Disable Servo Module

In the Disable Servo Routine (Figure 4-18) the following lines are set inactive:

- Guard band latch
- Ready

The track-crossing interrupt and step counter are also disabled. Then a re-entry counter is incremented and tested to see if this is the sixth pass. If it is, the processor stops and will do nothing until the drive is powered down and up again. If not, control is returned to the calling module.

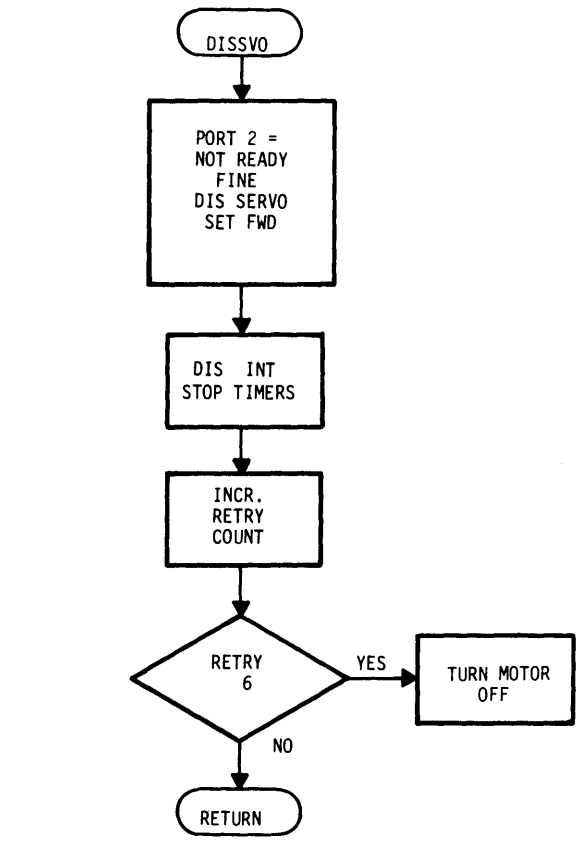


FIGURE 4-18. DISABLE SERVO

4.3.3 HEAD POSITIONING SYSTEM

4.3.3.1 GENERAL

The data heads are positioned on the disk by a closed loop servo system (Figure 4-19). Mounted on the same actuator as the data head is a servo head which reads the specially formatted information on the servo surface (lower surface of the bottom disk). This information is decoded and amplified for the error signal needed to keep the actuator on track. The microcomputer provides a command signal to move from track to track.

The servo system contains a position loop, a velocity loop and a current loop. Figure 4-19 is a simplified block diagram of the servo system. The current loop is analog while the velocity and position loops are a combination of digital and analog circuitry. The compensation loops are not shown for simplicity. The positioning servo system utilizes velocity information that is obtained by differentiation of position signals.

The positioning operation begins when the system controller sends a step and direction command. The microcomputer then initiates and controls the seek. There are times when the microcomputer initiates a seek without a system controller command. Initial head-load and recovery from faults are two of these times.

The microcomputer counts the number of tracks to be traversed and searches a velocity profile table for the correct velocity command code. The microcomputer outputs a digital number representing the initial velocity taken from the velocity profile table. A digital-to-analog converter generates an analog voltage which is amplified and applied to the actuator voice coil. The microcomputer also switches the servo circuit into the velocity mode. This begins the move to the destination track and causes information on the servo surface to be decoded into a velocity feedback signal. Each time the center of a track is crossed, the servo circuitry detects it and informs the microcomputer. The target track distance is then recalculated. As the heads approach the target track the microcomputer reduces the velocity. When the heads are within less than one-half track of their destination the microcomputer switches the servo to the fine mode.

In the fine mode the information on the servo surface is decoded into positional feedback. The microcomputer also decides if the target track is odd or even and sets a line to tell the servo circuit which track to center on.

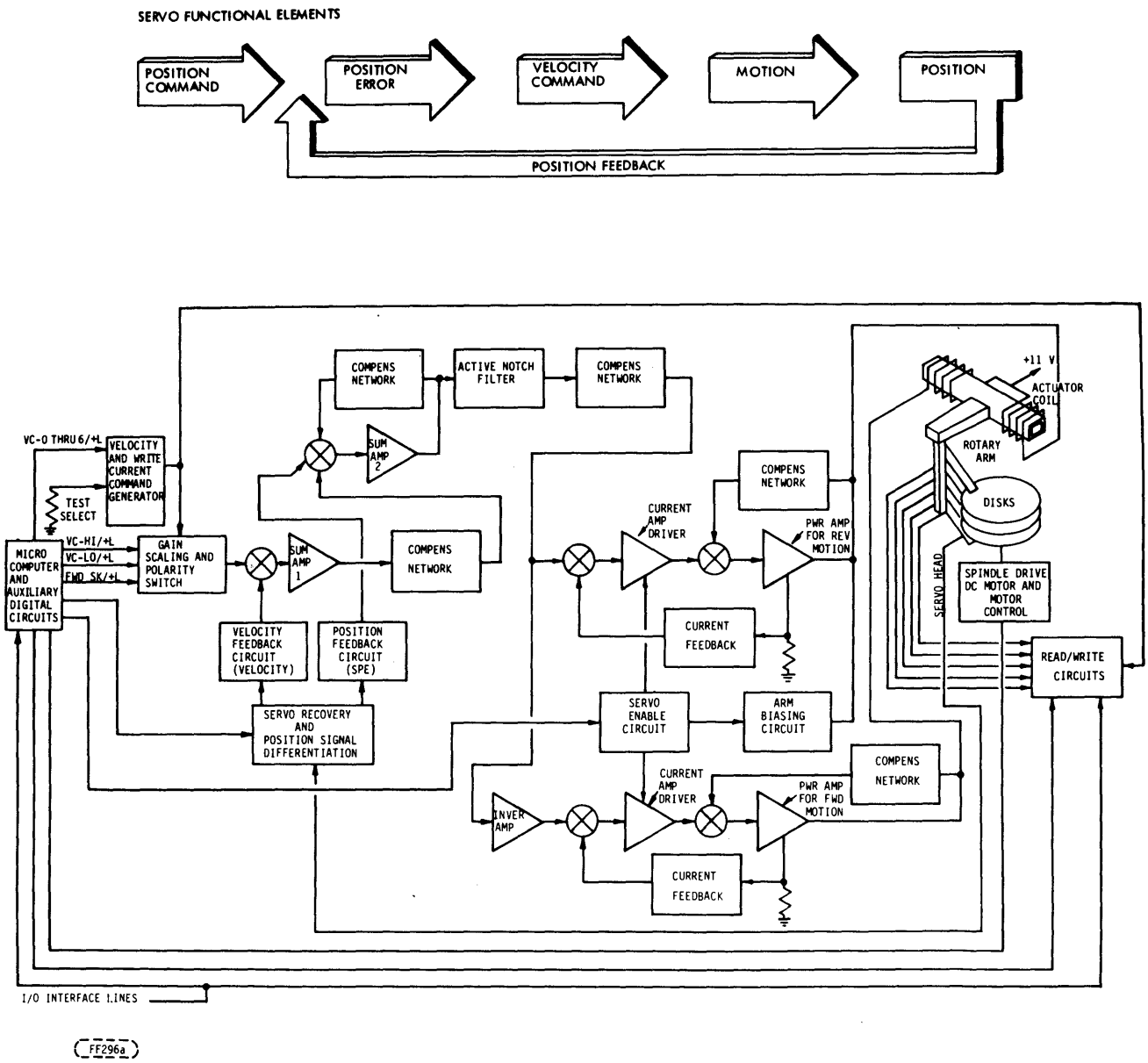


FIGURE 4-19. GENERAL BLOCK DIAGRAM

4.3.3.2 SERVO SURFACE FORMAT

The servo surface is divided into four zones as shown in Figure 4-20. The data zone defines the read/write area on the other surfaces (track 00 to 696). The guard bands have coded information to tell the drive when the heads are outside the data zone. The WREN uses a landing zone because the heads are over media at all times. Flying and landing the heads in this zone prevents damage to customer data when cycling power. The landing zone also has data to enable the servo timing circuits to synchronize during start-up. Special data on track -79 is used during manufacturing to set the mechanical stop.

The servo format used in the WREN is composed of a five-dibit pattern. There are 2688 servo fields per track. The individual dibits within the servo field are called:

- Sync
- Code
- Even
- Odd
- Quadrature

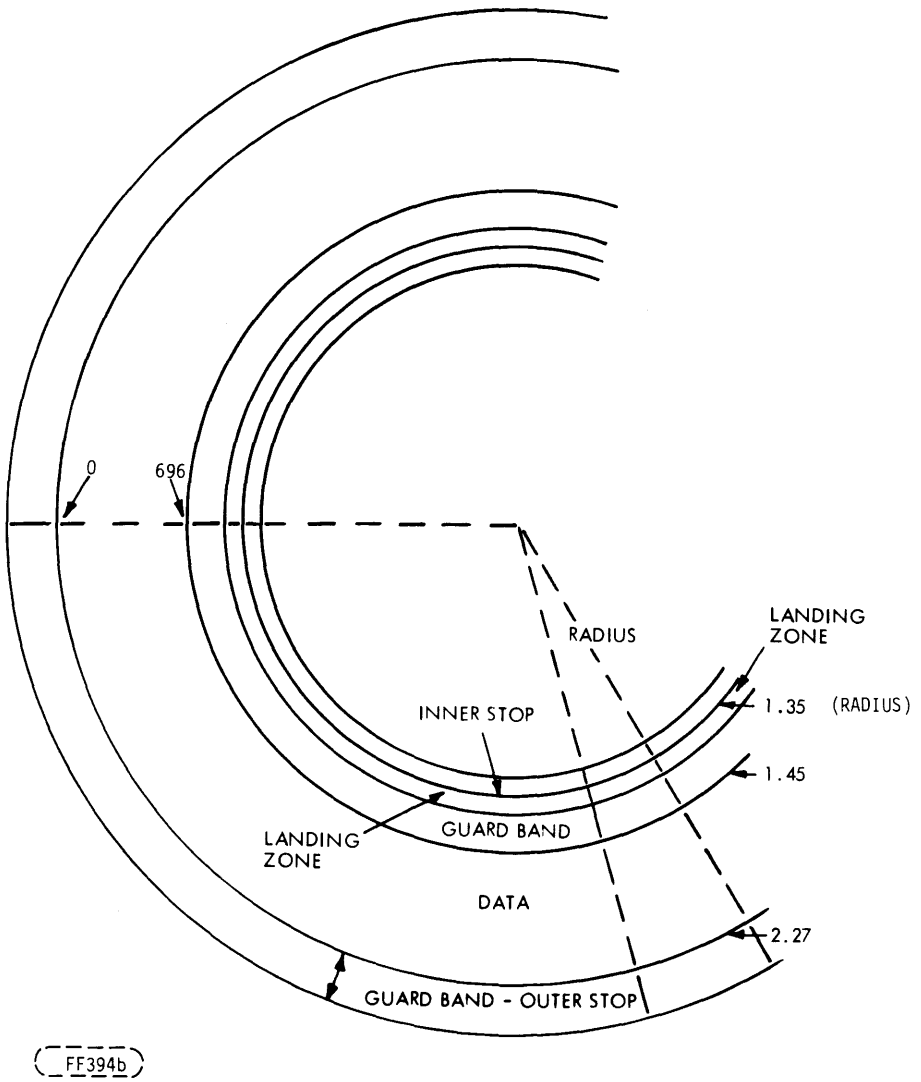
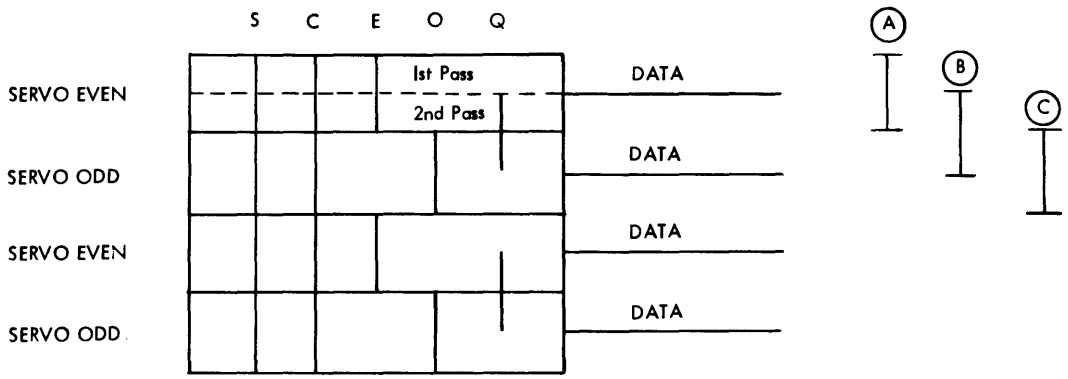


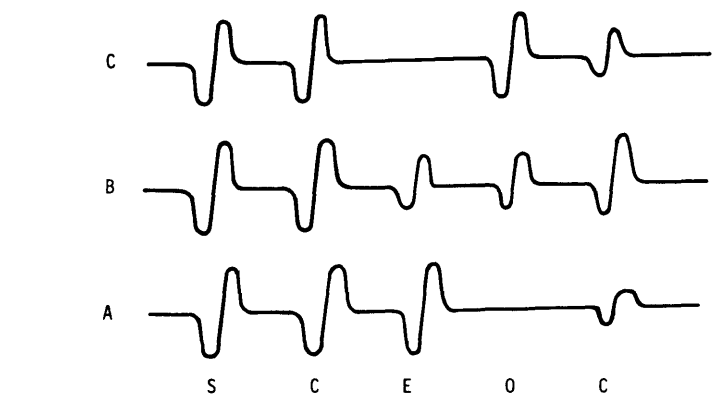
FIGURE 4-20. WREN SERVO TRACK LOCATIONS

The sync bits are used to lock the PLO which then provides the basic timing to decode the rest of the dibits. The code bit is used to mark the index and to differentiate the data zone from the guard band. The even, odd and quadrature bits are used to derive the position and velocity feedback signals.

Servo tracks come in two varieties, even and odd. All tracks have sync bit. The code bit is present in the guard band, but only in every other field. The code bit is also present for four fields at the beginning of each data track to mark the index. Only even tracks have even bits and only odd tracks have odd bits. The quadrature bit is written half on the outside of the even track and half on the inside of the odd track as shown in Figure 4-21.



G297a



FF393a

FIGURE 4-21. DIBIT PATTERNS

Data tracks on the other surfaces are offset one-half track from servo tracks, this means that when the servo head is halfway between an odd and even track the data head is on track center. Dibit pattern B in Figure 4-21 shows what the servo information will look like when the data head is on track center. Note that the odd and even bits are of equal amplitude and the quadrature bit is a maximum amplitude. The servo circuits find the center of data tracks by subtracting the peak values of the odd dibits from the peak values of even dibits (see Figure 4-22). When this value is zero the data heads are centered. If the peak values of the quadrature dibit are also zero the track is odd. On the other hand if the quadrature dibit are at their maximum value the track is even.

When the servo is in the velocity mode the absolute value of the slope of the position signal is used as the velocity feedback. However, this slope has a discontinuity between tracks due to a change in sign. Therefore, when the position signal is over a set threshold the absolute value of the quadrature slope is used as the velocity feedback.

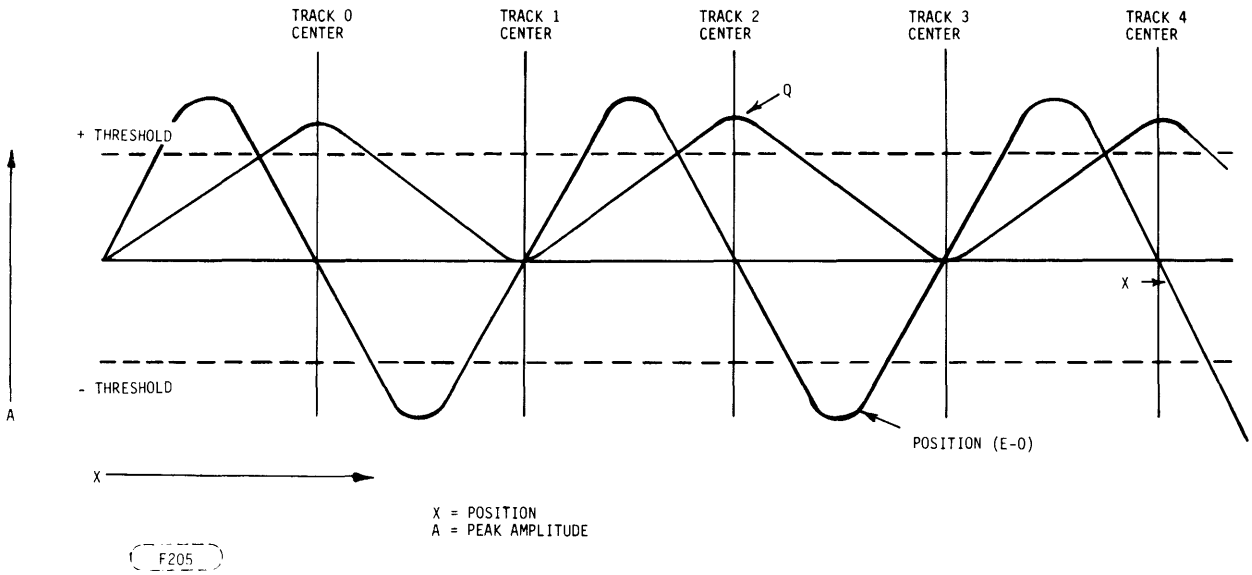


FIGURE 4-22. DERIVED POSITION AND QUADRATURE SIGNALS

4.3.3.3 DETAILED POSITIONING SYSTEM DESCRIPTION

A block diagram of the WREN Servo System is shown in Figure 4-19. Two signals derived by the Servo Analog Data Recovery circuits are position and velocity signals. A block diagram of the analog circuits used to provide these signals is shown in Figure 4-23. These signals are used by the closed loop servo system to control the seeking and positioning of the heads. The analog circuits are controlled by the digital LSI circuit, which provides the proper gating signals, and by the microcomputer.

A detailed description of the functions of the circuits shown in Figure 4-23 is as follows:

The signal from the servo disk is amplified by a low noise preamp (M116) and filtered. This preamp is located on the Preamp PWA. The output is sent to the Data PWA where it is again amplified (733) and filtered and applied to the Servo Analog LSI chip. The Analog LSI chip contains an automatic gain control (AGC) amp which is the controlling element in an AGC loop contained within the chip. Also in the chip is a high speed comparator with a threshold set at 50% of the peak dibit level which outputs a pulse when any dibits amplitude exceed 50% of the peak AGC level. The input signal from the 733 amp is applied to the AGC amp in the analog LSI. It is then amplified again and coupled to a buffer amp. The buffer amp drives a gated AGC current pump detector. The detector is gated such that only the sync dibit is used for AGC. The combined action of the AGC system is to produce a constant amplitude sync dibit at the output of the buffer amp. The AGC reference voltage controls the peak amplitude of the output of the buffer. This voltage is supplied externally to the LSI chip by a D/A converter circuit. The reference voltage is set up during a calibration cycle when power is applied to the drive.

The internal buffer output is also applied to three gated peak detectors which peak detect the three position dibits, even, odd and quad. The even and odd peak detectors are applied to different amps with a gain of 4.5. The output of the difference amp is filtered by a two-pole active filter. This signal is E-O (even-odd) and is inverted to produce O-E (odd-even). These signals are shown in Figure 4-24. During seeks no position feedback is used and the position switching circuit grounds the SPE signal (servo position error). During track following mode (FINE) the position switching circuit selects either the E-O or O-E signal depending upon which polarity track (even or odd) is to be followed.

The velocity signal is developed from the position signal by taking the derivative of the E-O and O-E signals. These two velocity signals re (Ve-o and Vo-e) are applied to the velocity switches. These signals are of opposite polarity and the proper one is selected depending upon the position of the head over an even or odd track. The position of the head is determined by the servo digital LSI which detects the presence or absence of a Q dibit pulse. This signal is outputted by the LSI as $Q>50$ and $Q<50$. These two signals control what velocity feedback signal is used. As the head moves between tracks, the E-O and O-E signals become non-linear and their velocity signals are not accurate. To overcome this a quadrature dibit is written on the servo surface which is offset by 1/2 track from the even and odd dibits. This dibit is peak detected by the Q peak detector and amplified and filtered to generate the Qp signal.

This is inverted and becomes -Qp. Qp and -Qp are also differentiated to produce two other velocity signals V_Q and $-V_Q$. One of these signals is selected by comparing the amplitudes of the E-O and O-E signals. If either of these go too positive and enter their nonlinear region the velocity feedback signal is switched to the V_Q or $-V_Q$ signal. The output from the velocity switches is buffered by an ampliffer (LM308A) and this output is applied to the servo error amp as the velocity feedback.

The gain of the position and velocity feedback signals is controlled by the amplitude of dibits that are peak detected. The amplitude of the dibits is set by the AGC system which is referenced to an external voltage (AGC REF VOLTAGE). By changing the reference voltage the amount of feedback to the servo loop may be changed. This fact is used to adjust the velocity feedback signal to the exact amount required independent of component tolerances, etc. This is done upon power up sequence under control of the microcomputer circuits. The microcomputer does test seeks during which it measures the velocity of the arm. If the velocity is incorrect it will increment the auto velocity adjust counter which changes the AGC REF VOLTAGE. Another test seek is performed and the process repeats until the correct velocity is achieved. This adjusts for errors associated with normal component tolerances.

Also located in the Servo Analog LSI are several comparator circuits. One of these is the Track Center Comparators which tells the microcomputer circuit that the head has reached the center of the track. This is used in the settle routine and also will indicate if the head has gone off track for some reason. Another comparitor simply senses if the E-O signal is positive (E-O> O). This signal is used by the servo digital LSI in the track crossing generator circuit.

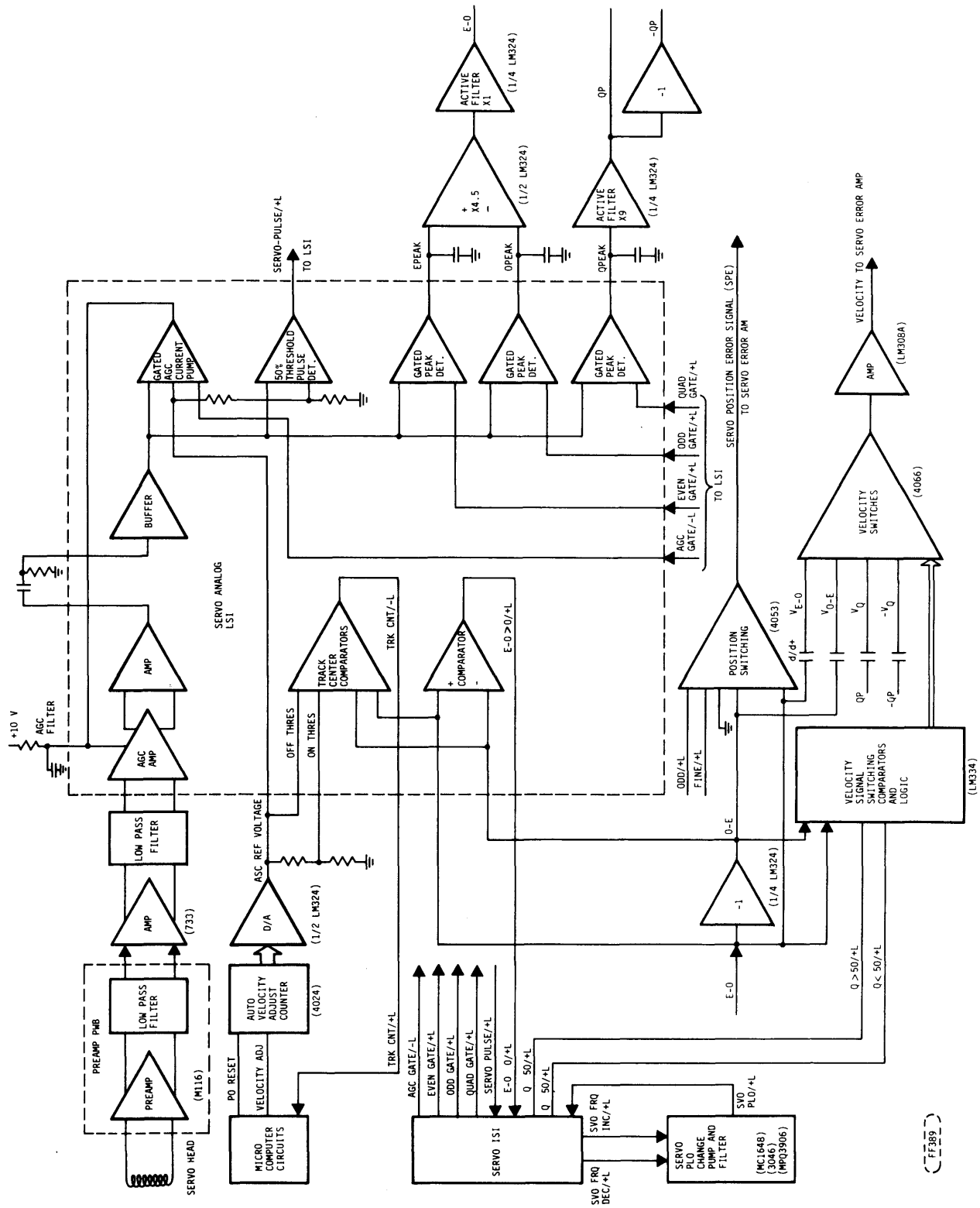


FIGURE 4-23. WREN SERVO ANALOG DATA RECOVERY CIRCUITS

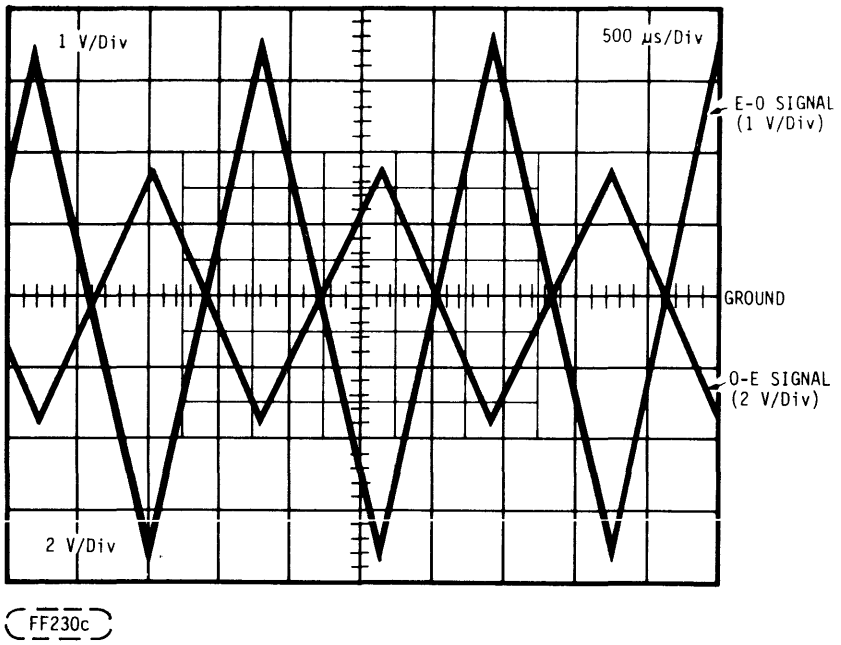


FIGURE 4-24. E-O AND O-E SIGNALS

In addition to the position and velocity signals, the analog circuits of the servo system provides the following functional groups. (See Figure 4-19.)

- Velocity and write current command generator
- Actuator drive circuits:
  1. Gain scaling and polarity switch
  2. Summing amplifiers
  3. Power amplifier
- Servo system velocity feedback circuit
- Servo system position feedback and offset generating circuit
- Active notch filter and compensation networks
- Servo enable and rotary arm biasing circuit.

The velocity and write current command generator is located on the Servo PWA. The microcomputer outputs a seven bit digital command by proper activation of the VC-0/+L through VC-6/+L lines to the digital to analog converter (DAC) (U25). The DAC output is connected to current to voltage converter U21-1. Scaling of the DAC output is accomplished at the factory by selecting the value of the test select resistor R70. The two velocity ranges are chosen by the microcomputer by activating the VC-LO/+L or VC-HI/+L lines. The gain scaling of the amplifier U-34 is provided thru analog switches U29-14 and U29-4. The Microprocessor controls the direction of the seek by determing the inverting or noninverting configuration of the polarity switching amplifier U21-7. When this line is set "HIGH" the actuator drive circuits provide "REVERSE" motion of the rotary arm (from lower numbered tracks towards higher numbered tracks). When the seek is complete, R148 and R149 are disconnected from U21-7 and U34 output is grounded. This allows write current levels to be set at U22-1 without affecting the servo system. Summing amplifier U20 in the seek mode subtracts the velocity feedback signal from the velocity command signal to generate the velocity error signal.

The velocity error signal drives the power amplifier through amplifier U14 and active notch filter U10-7. During the seek mode the line FINE/+L is "LOW" and position feedback signal is removed. When the rotary arm is positioned on track (FINE/+L is "HIGH"), the position signal will be active.

The power amplifier drives the head actuator coil. Q2 emitter resistor R21 feeds back a voltage proportional to the current in the actuator coil for "FORWARD" motion. The feedback voltage is summed with the actuator drive signal at pin 13 of U10. Q1 emitter resistor R20 feeds back a voltage proportional to the current in the actuator coil for "REVERSE" motion. The feedback voltage is summed with the actuator drive signal at pin 9 of U10.

The compensation networks (R14, C6 and R9, C7) control the gain and band width of the output stages of the Power Amp in order to insure high frequency stability. The compensation networks (R32, R33, C13 and R93, C30) control the band width of the current loop. The U14 compensation feedback network (R105, R103, C43) together with the active 2.4 kHz notch filter provides high frequency compensation in the velocity loops and attenuates frequencies that may cause mechanical resonances.

The U14 compensation feedback network (104, R103, C11) provides low frequency compensation for the position loop.

The network (R132, R133, C58) provides low frequency compensation in the velocity loop. The noise in velocity feedback is attenuated by compensation networks (R139, R130, C57 and R131 and C56).

Servo disable and actuator retract are controlled by DISABLE/+L line and provided by CR8, CR9, Q5, U7 (6,7,8) and Q8. The actuator retract procedure energizes the reverse winding with a controlled current to pull the arm into the landing zone. The DISABLE/+L line can be activated by both the microcomputer (UP SERVO EN/-L) and the voltage fault monitor. Voltage fault monitor set the DISABLE/+L line "HIGH" anytime when either one of the external power supplies (+12 V or +5 V) or internally generated -5 V is lost. In this case RESET/-L line is set "LOW". That resets the microcomputer. Anytime the DISABLE/+L line is active, WRT INHIBIT/+L is also set "HIGH" and disables the write function.

4.3.4 READ/WRITE SYSTEM

4.3.4.1 GENERAL

To maximize the amount of data stored on the disk, the frequency of the flux reversals must be carefully controlled. Several recording methods are available and each has its advantages and disadvantages. The WREN-5 uses the MFM technique.

The time required to define one bit of information is called a cell. Each cell is nominally 200 ns in width. The data transfer rate is therefore, nominally 5.0 mega data bits/sec.

MFM defines a 1 by writing a flux transition at mid cell time. It defines a 0 by writing a flux transition at the end of cell time except when the cell is followed by a 1 in which case no flux transition is written in that cell.

The advantages and disadvantages of MFM recording are listed below:

- Fewer flux reversals are needed to represent a given binary number because there are no compulsory flux reversals at cell boundaries, achieving higher recording densities of data without increasing the number of flux reversals per inch. The number of flux reversals varies from a maximum of one reversal per bit (all "1's" or all "0's") to a minimum of one reversal for every two bits (alternating "1's" and "0's").

- Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency achieved because of fewer flux reversals required for a given binary number.

- Transition polarities have no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic which includes a PLO and high quality recording media.

4.3.4.2 WRITE CIRCUITS

The magnitude of the write current is changed as a function of the cylinder address. The microcomputer uses the same digital to analog converter (D/A) that was used for the velocity command. The D/A is set to zero for the inner tracks where the write current is minimum. It is set to 83 for the outer tracks which need the maximum write current. The output of the D/A should vary from zero to about 2.85 volts. The write current is therefore increased about every eight tracks.

Figure 4-25 is a block diagram of the Pre-Amp PWA. When the write gate is enabled the write data is clocked into the write data flip-flop. This converts the data to differential data by the use of both inverted and non-inverted outputs. The write data circuit provides equal current to both polarities of the write data. The data is then sent on to the preamp. The WRITE SELECT/-L signal is a low TTL level signal to enable the write of the head preamp. The write enable circuit controls the following:

1. The write data circuit which was explained above.

2. The write select circuit which puts the preamp in the write mode. When write select is inactive the preamp will be in the read mode.

   The write current level circuit which controls the magnitude of the write current is disabled by the unsafe signal. This circuit sets the minimum current and adds an adjusted current with the aid of the write current control (as explained above). The signal labeled write current sinks current of amplitude almost equal to the write current through one side of the head coils.

The unsafe latch is set by an unsafe signal generated by the head preamp. It disables the write current and sets the unsafe latch. The unsafe latch holds the write select, write current, and write enable circuits disabled until they are reset by the controller or the digital circuits.

4.3.4.3 READ CIRCUITS

When the disk drive is not writing the signal from the Read/Write heads is amplified by the head preamp located at the head flex cable close to the head. By being near the heads the signal to noise ratio is improved. The signal is amplified (39 times nominal) and sent through the flex cable in a differential mode outside the sealed unit.

This signal is received by the pre-amp PWA as RD-DATA-N and RD-DATA-P. The amplitude of this signal is in the millivolt range. A three pole linear phase low pass filter reduces the high frequency noise of the signal. The signal is amplified and processed by a pulse-slimming network. The pulse-slimmer improves the signal resolution and conditions it for signal detection and recovery. The enhances signal is amplified and applied differentially as RD-ANALOG-N and RD-ANALOG-P to the data PWA.

The read circuitry of the read/write analog PWA (see Figure 4-26) converts the preamplified analog read data to digital MFM data. The data is first attenuated by a FET for gain control. The signal is then amplified and sent through a five pole linear phase filter to improve the signal to noise ratio. The signal is differentiated to convert the signal peaks to zero-crossings by an active differentiator for good common mode rejection.

At this point the data is split into three parallel paths. In the AGC circuit path the signal is peak detected and filtered at this point. The peaks are averaged by a current amplifier and a capacitor. Controlling the attenuator with this voltage gives the circuit automatic gain control. The two remaining data paths are the high resolution and low resolution channels. In the high resolution path no further filtering is added. The signal is buffered and sent through a delay line.

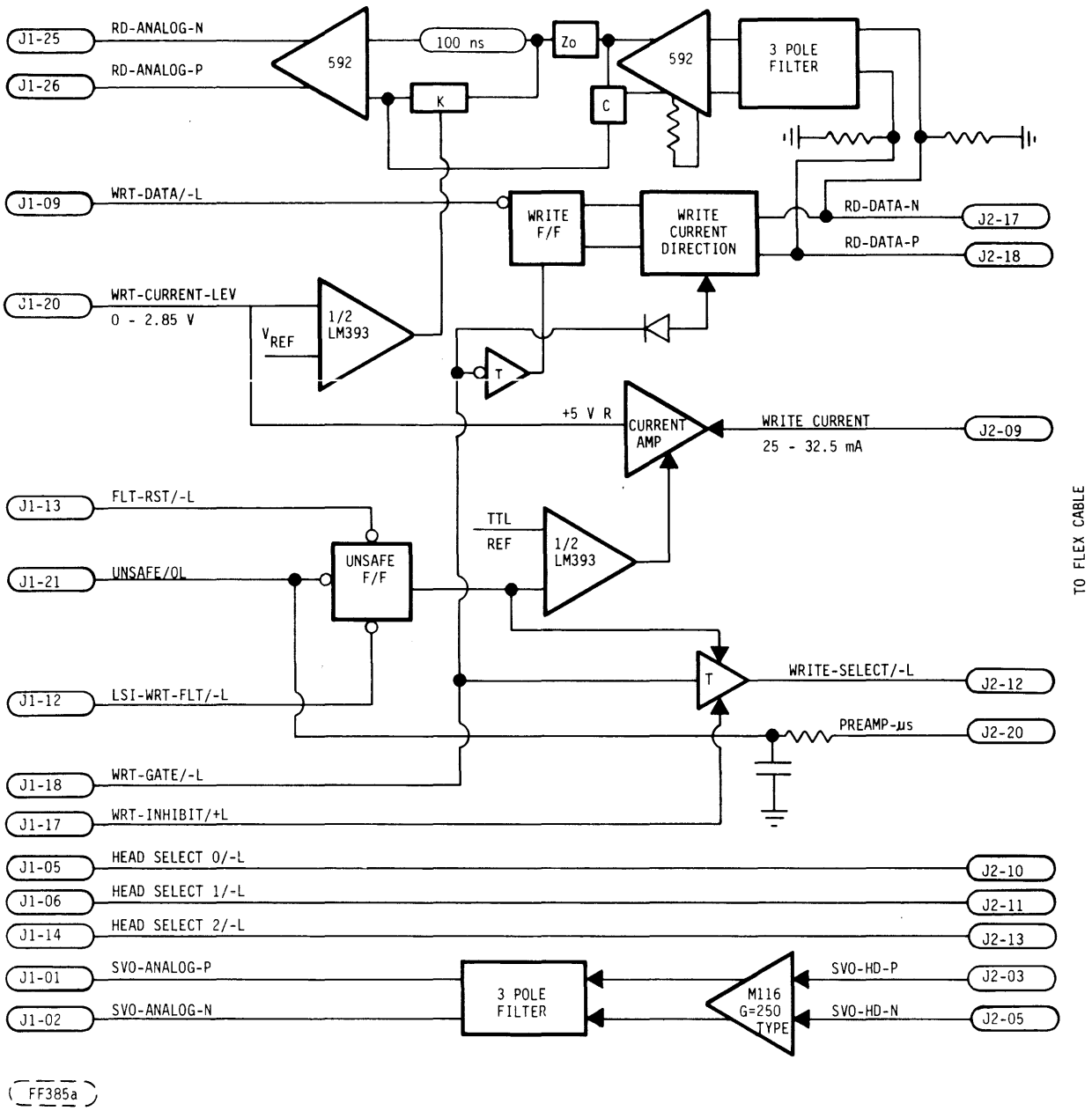


FIGURE 4-25. PRE-AMP BLOCK DIAGRAM

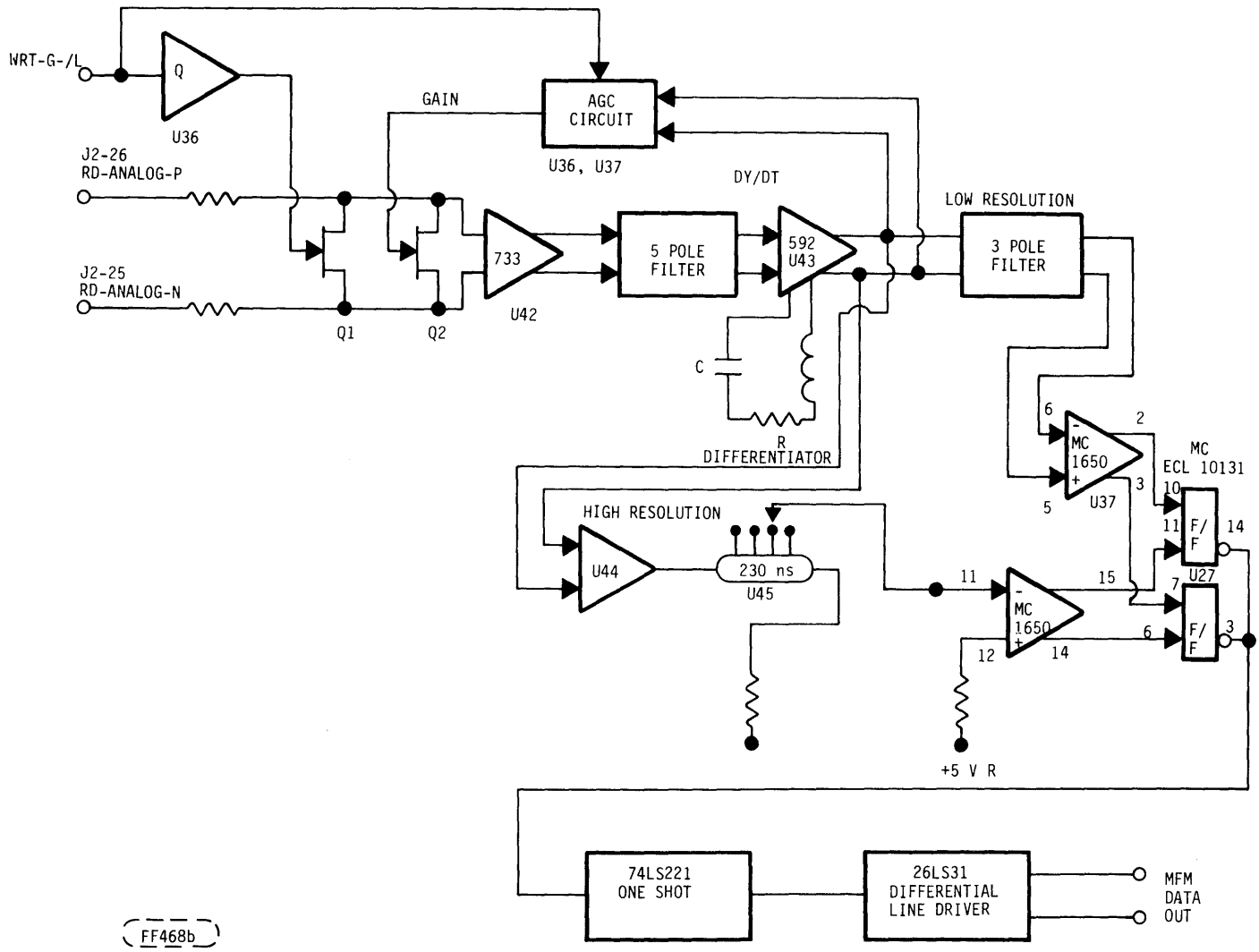


FIGURE 4-26. DATA PWA READ ANALOG FUNCTION

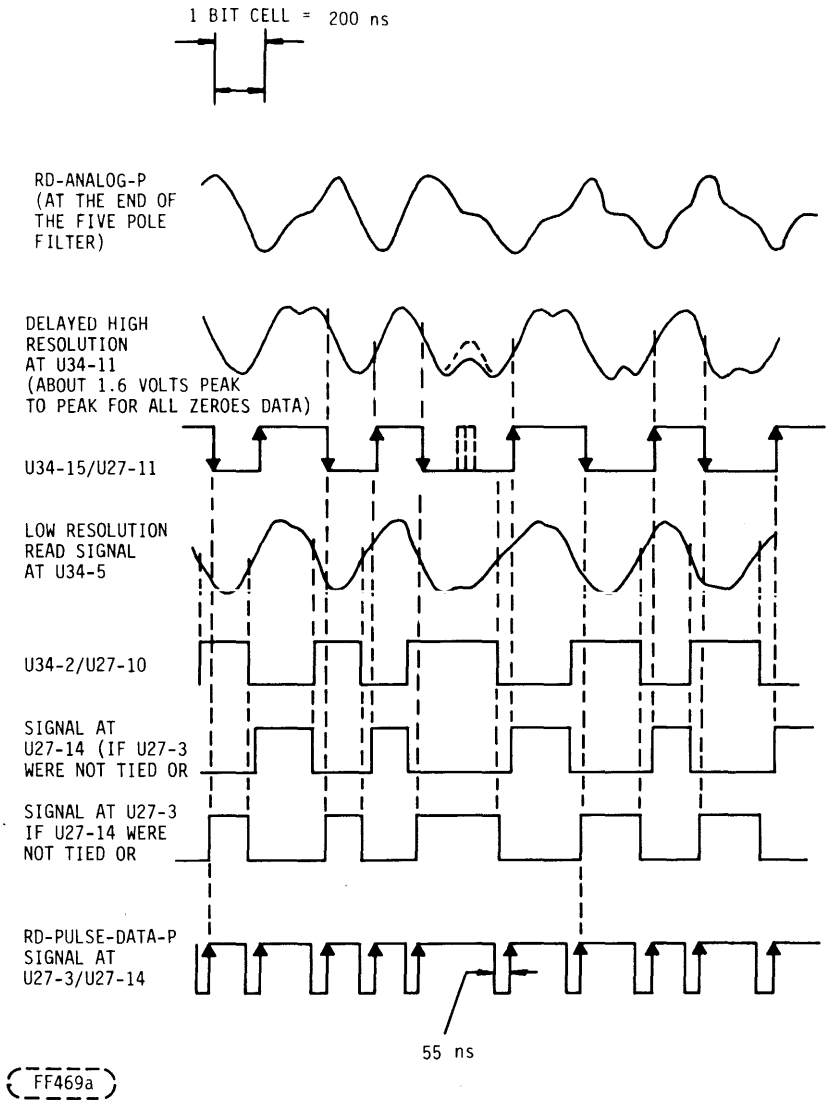


FIGURE 4-27. READ ANALOG TIMING DIAGRAM

The low resolution path adds a low pass filter to reject high frequency components (mostly third harmonics). This reduces the possibility of extraneous zero-crossing when the data frequency is low. This also induces a phase lag so that the signal now matches the delayed high resolution signal.

Both path signals are now converted to digital type signals by sending them through differential comparators. The signals are then sent to a pair of flip-flops which resolve the differences. The high resolution data clocks both flip-flops and the low resolution data enables them. Therefore the low resolution data acts as a qualifier and eliminates false transitions without changing true ones. The outputs of the flip-flops are wires-"OR"ed to produce a pulse for each flux transition. This data is used to trigger a 74LS221 one shot which generates 25 ns pulses. This signal is amplified by a 26LS31 to generate the balanced differential READ signals which are outputted on the interface. The timing diagram (see Figure 4-27), shows the waveform relationships. FET Q2 is turned on during the write mode to clamp the signal and reduce the write to read switch time.

4.3.4.4 HEAD PREAMP CHIP AT THE FLEX CABLE

The read/write preamp performs the following four functions:

1. The preamp selects the correct head.
2. The preamp diverts the write current to the selected head.
3. The preamp creates an unsafe signal for the following conditions:
   a. Shorted heads.
   b. Open heads.
   c. Write current in the read mode.
   d. No write data in the write mode.
4. The preamp amplifies the read data from the selected head.

The head select encoding is shown in Figure 4-28 and a block diagram of the head preamp in Figure 4-25. Note that the disk surfaces are numbered from the bottom up. It should also be noted that the preamp operates on +5 and -5 Volts. When the preamp is in the read mode the data is presented on the READ-DATA-N and READ-DATA-P lines. If the WRITE SELECT line is taken to low TTL level the preamp is switched to the write mode. The proper value of write current must then be sinked from the write current (WC) line. If an unsafe condition is present the preamp will bring the unsafe line from TTL high to TTL low. This will cause the digital circuitry to set the fault latch. The preamp will perform read or write operations on the head selected at the time, therefore, the head selection must be made before read or write is enabled.

INTERFACE LEVEL						
HD-SEL-2 J3-06	HD-SEL-1 J3-04	HD-SEL-0 J3-32	Head Location	Media Selected	Head Preamp SSI 115	Head Number
0	0	0	Top Head	Bottom Media	22,23	0
0	0	1	Bottom Head	Middle Media	20,21	1
0	1	0	Top Head	Middle Media	18,19	2
0	1	1	Bottom Head	Top Media	16,17	3
1	0	0	Top Head	Top Media	14,15	4

Note - A "1" corresponds to 0 to 0.4 Volts and a "0" to 2.4 to 5.25 Volts at the interface.
During read, invalid head select input codes (5, 6 and 7) have the effect of not selecting any heads. An unsafe is produced when writing to an invalid head or if there are no data transitions during a write.

FIGURE 4-28. WREN HEAD-SELECT ENCODING

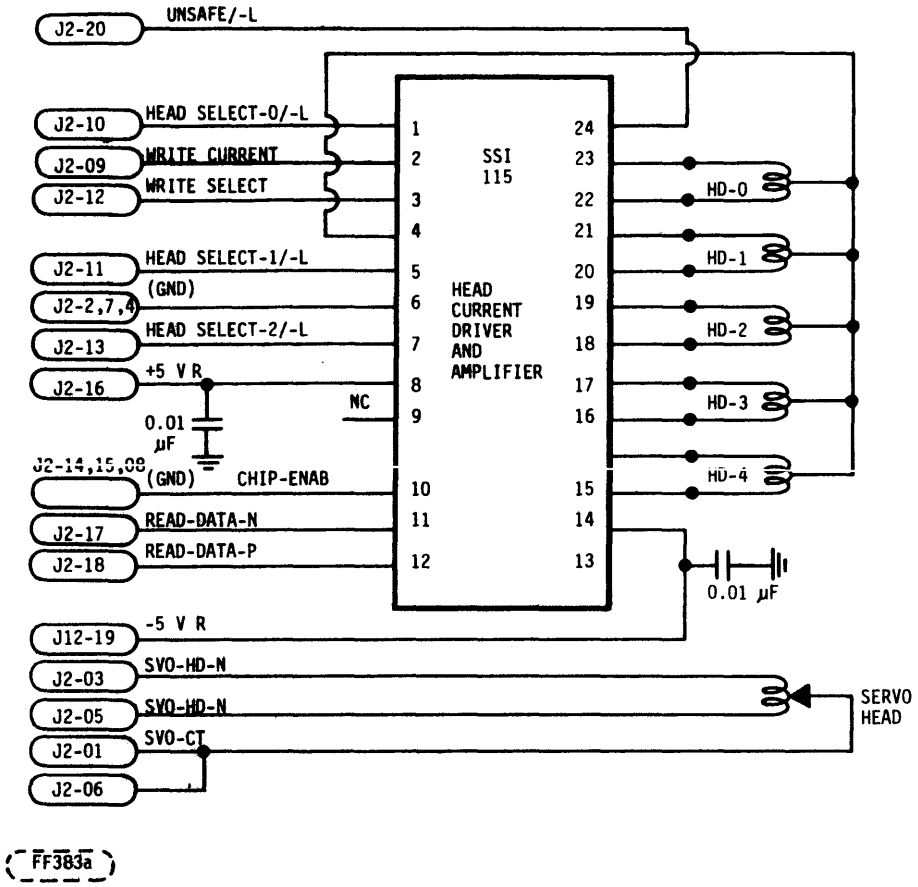


FIGURE 4-29. HEAD PREAMP AND DRIVER (AT THE FLEX CABLE)

4.3.5 AUXILIARY SYSTEMS

4.3.5.1 WREN POWER SUPPLY CIRCUITS

The WREN requires only two external voltages, +12 volts and +5 volts but some circuits in the WREN require a negative voltage. This negative voltage is provided by a DC-DC converter circuit. In addition to this converter, voltage regulators provide +10 volts and +5 volts for critical read/write and servo circuits. Figure 4-30 is a block diagram of the power supply circuits internal to the WREN.

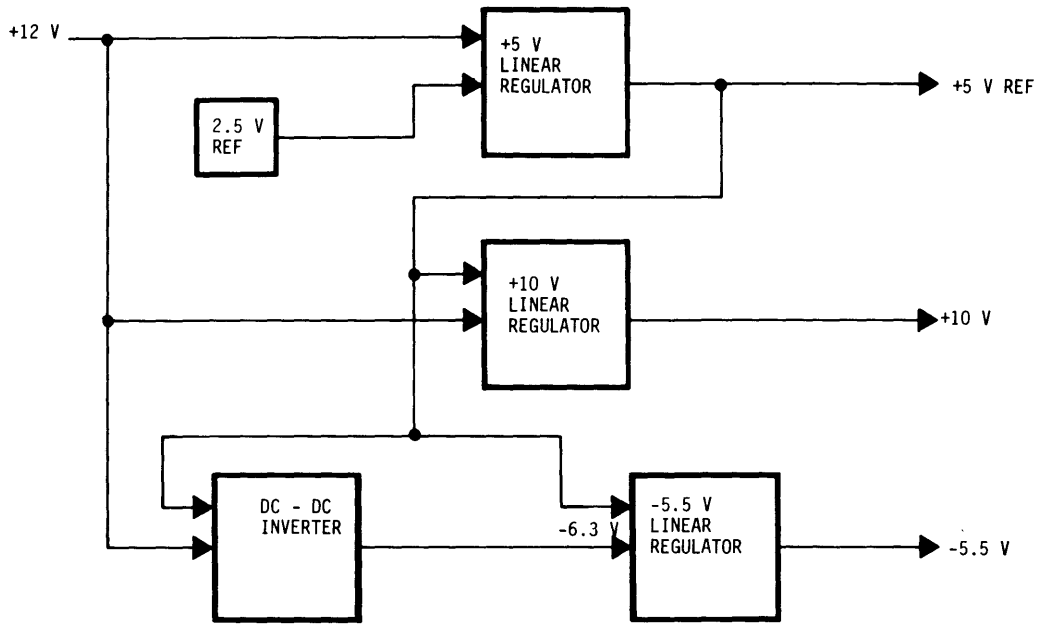


FIGURE 4-30. WREN POWER SUPPLY CIRCUITS

Figure 4-31 shows the schematic of the DC-DC inverter and linear regulator. Two comparators (LM393) control the operation of the switcher. If the output voltage at point C is too low then the bottom comparator will turn off and allow the switch transistor (3762) to apply +12 volts to point A of the 100 μH coil. This causes the current through the coil to increase linearly. This current is sensed by a 0.51 ohm resistor and when the current reaches ≈1 amp the upper comparator will turn on which turns off the switch transistor. The voltage at point A will then go negative until the catch diode (1N5818) turns on. This clamps the voltage across the inductor to ≈-6.7 volts and the current in the inductor decreases linearly to zero. This current charges the 39 μF output capacitor which increases the output voltage. This increase in output voltage causes the lower comparator to switch on which will inhibit the switch transistor from turning on. The load current will discharge the 39 μF capacitor until the lower comparator switches states and starts the cycle over. Figure 4-35 gives typical waveforms for a load current of 200 ma. The output of C is well regulated but has high ripple (ie ≈ 200 mV). This voltage is then regulated by a linear regulator to remove ripple and decrease output impedance. The output of the linear regulator is -5.525 volts. This output is referenced to the +5 V R voltage and is sensed by an op-amp (LM324) which drives a NPN pass transistor (MPQ2222) via a PNP current source (MPQ3762). The use of a NPN pass transistor allows the regulator to function to very low voltage across the pass transistor (typ ≈ 0.3 volts).

+5 volt and +10 volt Regulators

Figure 4-33 is a schematic of the +5 volt and +10 volt regulators. The +5 volt regulator is a conventional series pass design referenced to a 2.5 volt reference (MC 1403). The output (+5 V R) is used as the reference for all other regulators. The 10 volt regulator is similar to the -5.525 volt design except the transistors are of opposite polarity (ie NPN vs PNP). This allows

the regulator to keep a 10 volt output even if the +12 volt input reduces to ≈10.4 volts. Two pass transistors are used with current balancing resistors (4.7 ohm) to insure adequate power dissipation.

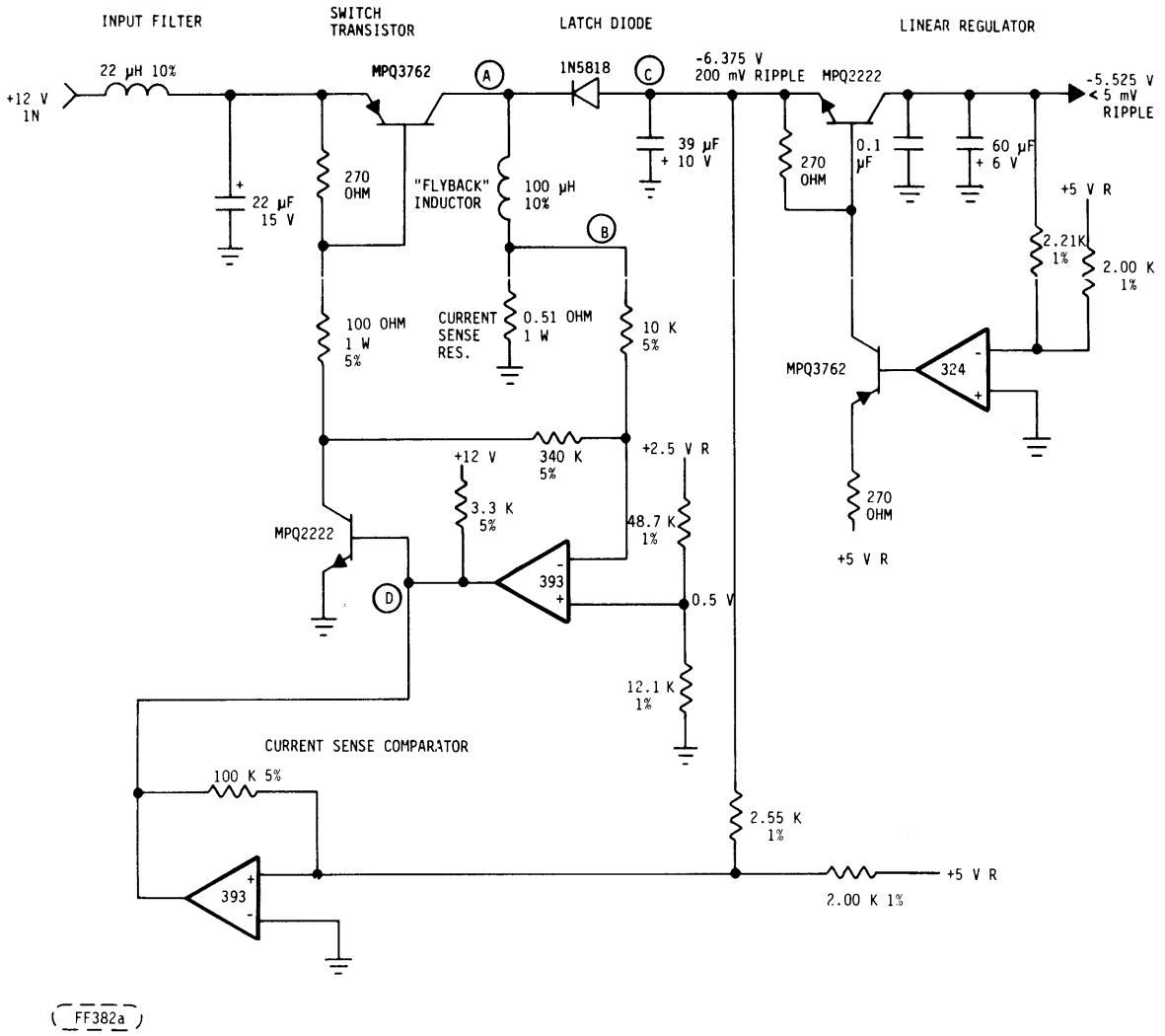


FIGURE 4-31. WREN DC-DC CONVERTER

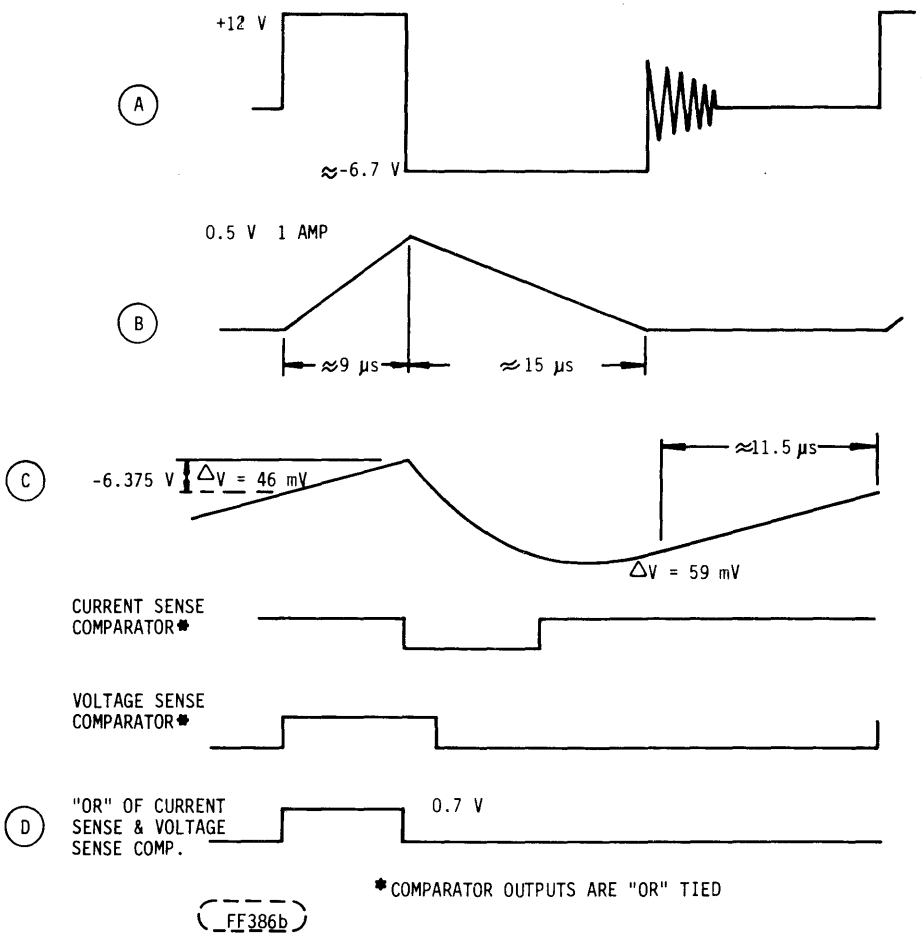


FIGURE 4-32. DC-DC CONVERTER WAVEFORMS

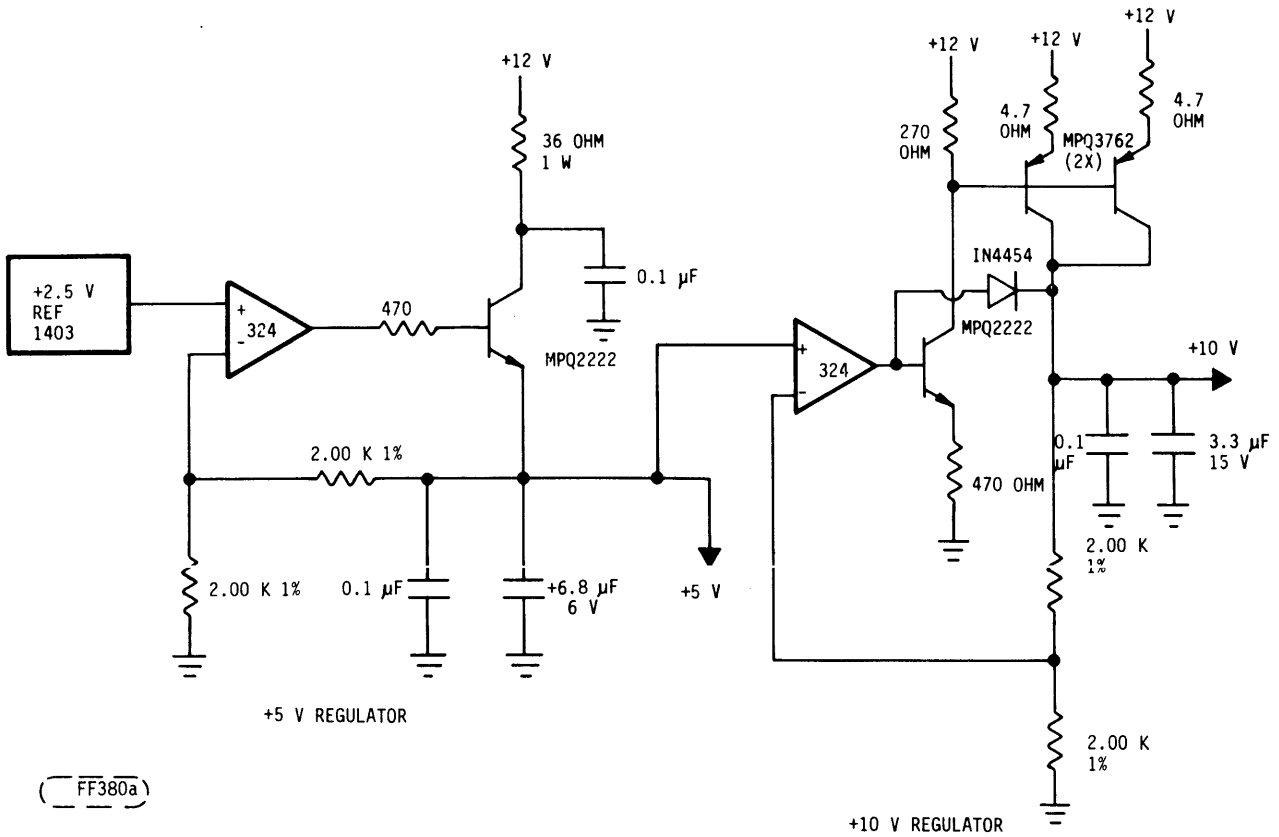


FIGURE 4-33. +5 AND +10 VOLT REGULATORS

4.3.5.2 VOLTAGE MONITORING

The WREN monitors the internal and external power supplies. This is done to assure data on the disk is not destroyed when power is shut off or interrupted. The circuits for doing this are on the SERVO-PWA. These circuits monitor the +5 and +12 volt external sources and the +10 and -5.5 volt supplies internal to the drive. These circuits also provide a delay of approximately 0.3 seconds after the +5 volt supply is turned on to allow the logic and microprocessor to be reset.

The outputs of the voltage monitoring circuits are used to directly inhibit any write current and to signal the microprocessor of voltage loss.

4.3.5.3 SPINDLE MOTOR CONTROL

A two phase brushless DC motorized spindle is driven by a current controlled power amplifier and commutation is regulated once per phase by a sensor device inside the spindle motor. The motor current is set by the amplitude of a filtered pulse width modulated signal generated by the speed control circuits located in the servo-motor control LSI. (See Figure 4-34.)

The motor control logic in the servo LSI chip uses the clock signal derived from the microprocessor clock as a reference to determine the motor speed error. The servo LSI generates an output width proportional to the amount that the motor speed is under the desired speed. The duty cycle of this signal is divided into 8 steps between 0% (minimum error) and 100% (maximum error). The 100% duty cycle is used while starting.

The back EMF derived from the stored energy in the disks and spindle is used to hold the actuator solenoid in an unlocked position while moving the head actuator into the landing zone after external power is removed.

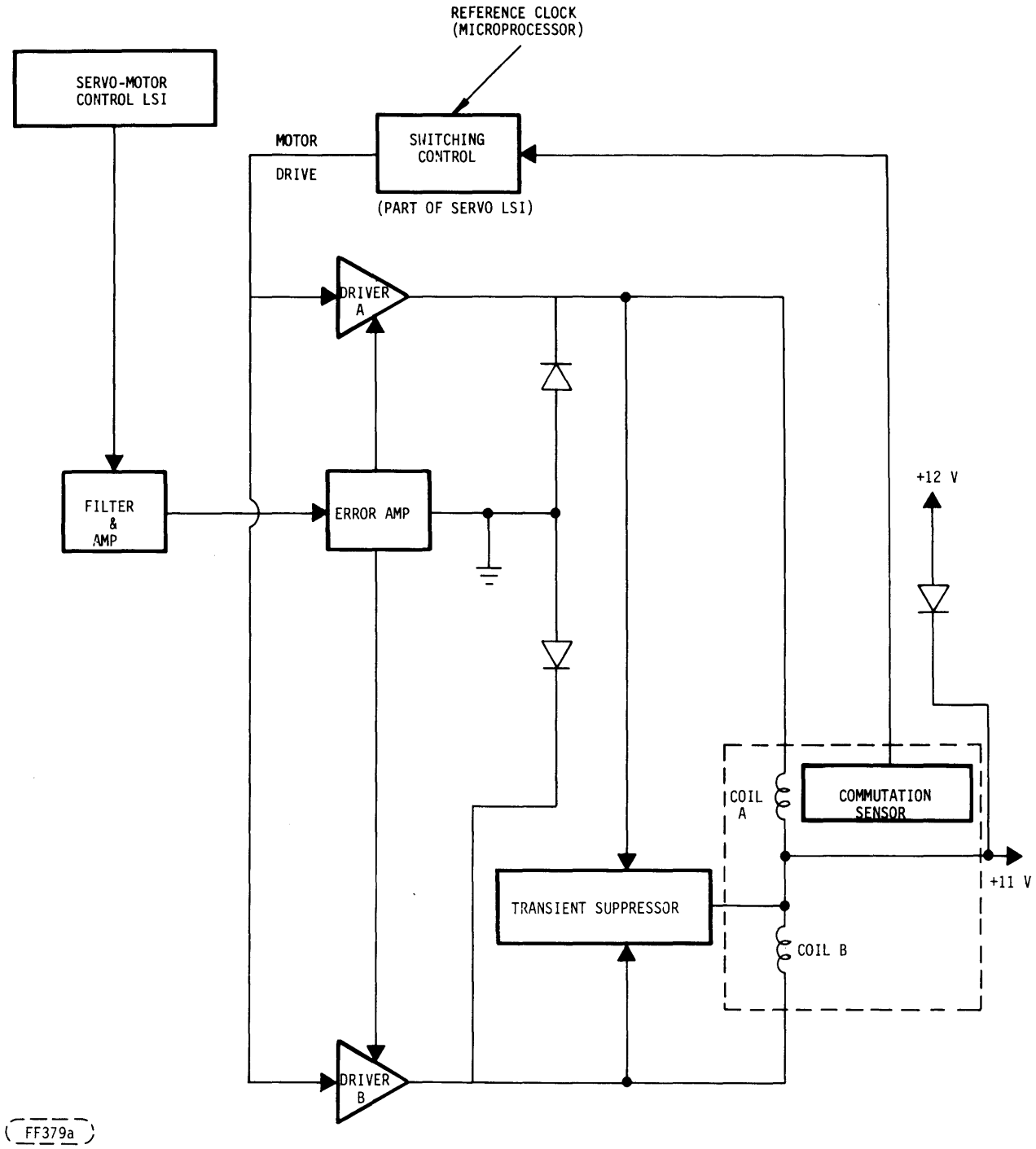


FIGURE 4-34. MOTORIZED SPINDLE DRIVE

5.1 INTRODUCTION

This section contains the interconnect diagrams, an example of logic symbology, an explanation of the use of zone signs for signal tracing, schematics, and printed wire assemblies of the printed circuit boards used in the WREN I-5 disk drives.

5.2 INTERCONNECT DIAGRAMS

The interconnect diagram (Figure 5-1) details the cabling between the Servo PWA, Data PWA, Preamp PWA and the Flex Circuit.

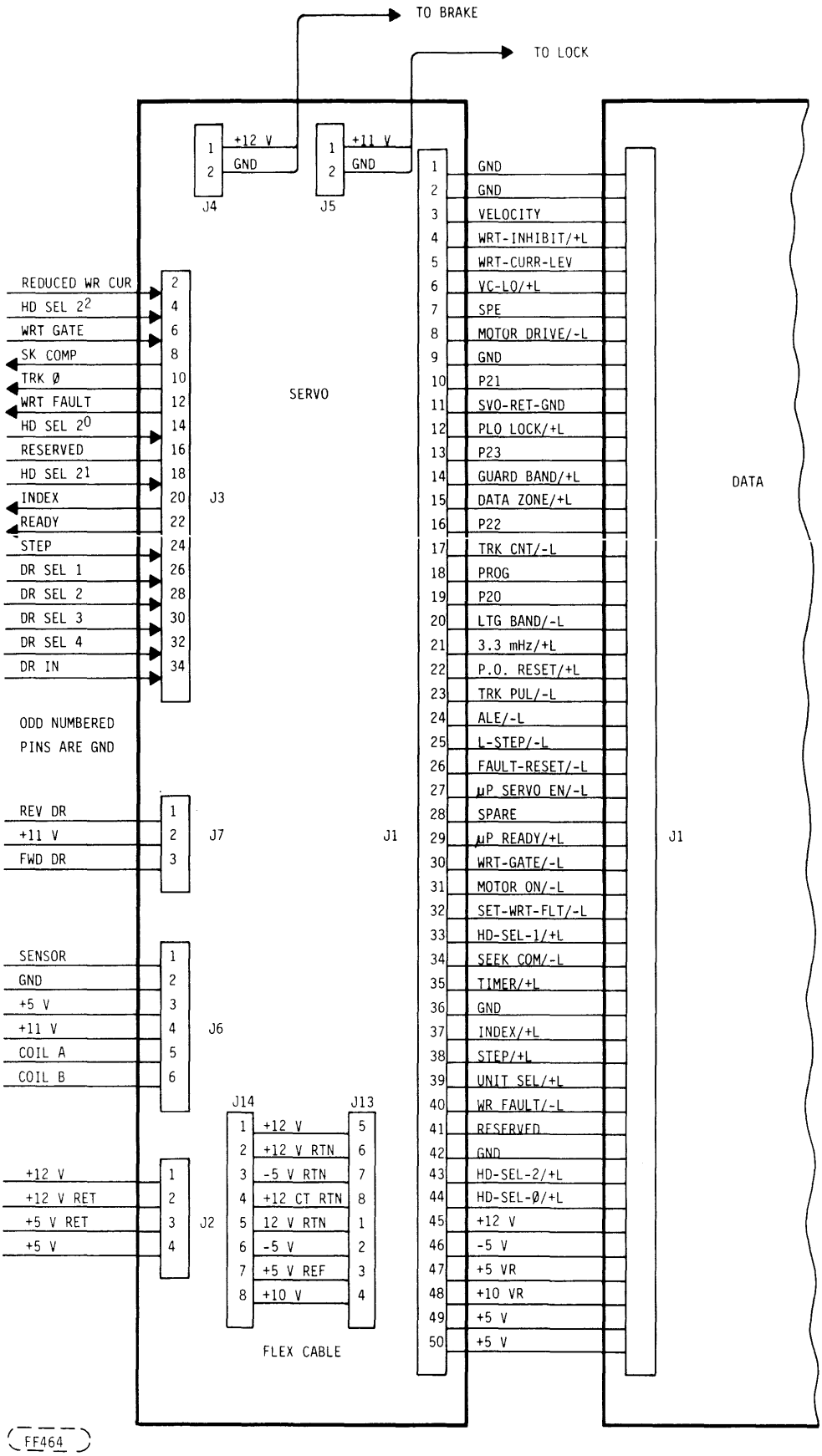


FIGURE 5-1. WREN I-5 INTERCONNECT DIAGRAM (SHEET 1 OF 2)

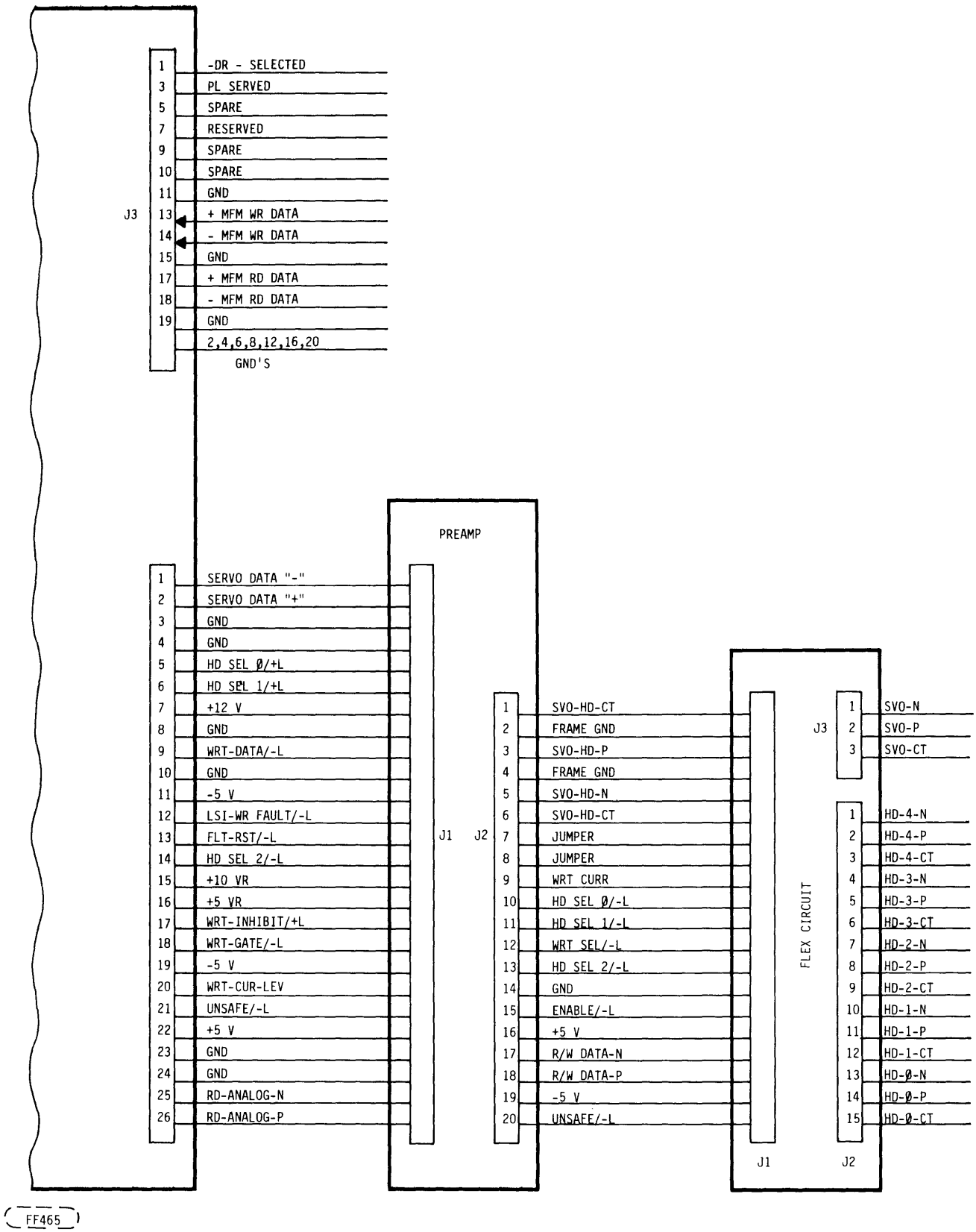


FIGURE 5-1. WREN I-5 INTERCONNECT DIAGRAM (SHEET 2 OF 2)

5.3 CIRCUIT BOARD DOCUMENTATION

Each of the following boards (Table 5-1) consists of schematics and a printed wire assembly. Each schematic has a sheet number which is used to facilitate point-to-point signal tracing from schematic to schematic. The use of cross reference numbers for signal tracing is explained in paragraph 5.3.1. Refer to Figure 4-2 for location of the circuit board assemblies in the WREN I-5 Disk Drive.

TABLE 5-1. WREN CIRCUIT BOARDS

CKT PWA IDENT	FIGURE NUMBER	TITLE
77734850	5-5	SERVO PWA
77734800	5-6	DATA PWA
77734700	5-7	R/W PREAMP PWA
77712180	5-8	R/W - S FLEX PWA

5.3.1 POINT-TO-POINT CONNECTIONS BETWEEN SCHEMATICS

Logic signals can be traced by using the sheet and zone references. An example, is shown using Figures 5-2 and 5-3 which are portions of sheets from the SERVO-5 schematics. The signal, SERVO ERROR, is shown in Figure 5-2 as going to sheet 5-D8 (Zone D8). Referring to Figure 5-3, SERVO ERROR is shown coming onto sheet 5 in Zone D8. It shows that it came from sheet 3-A1 (Zone A1).

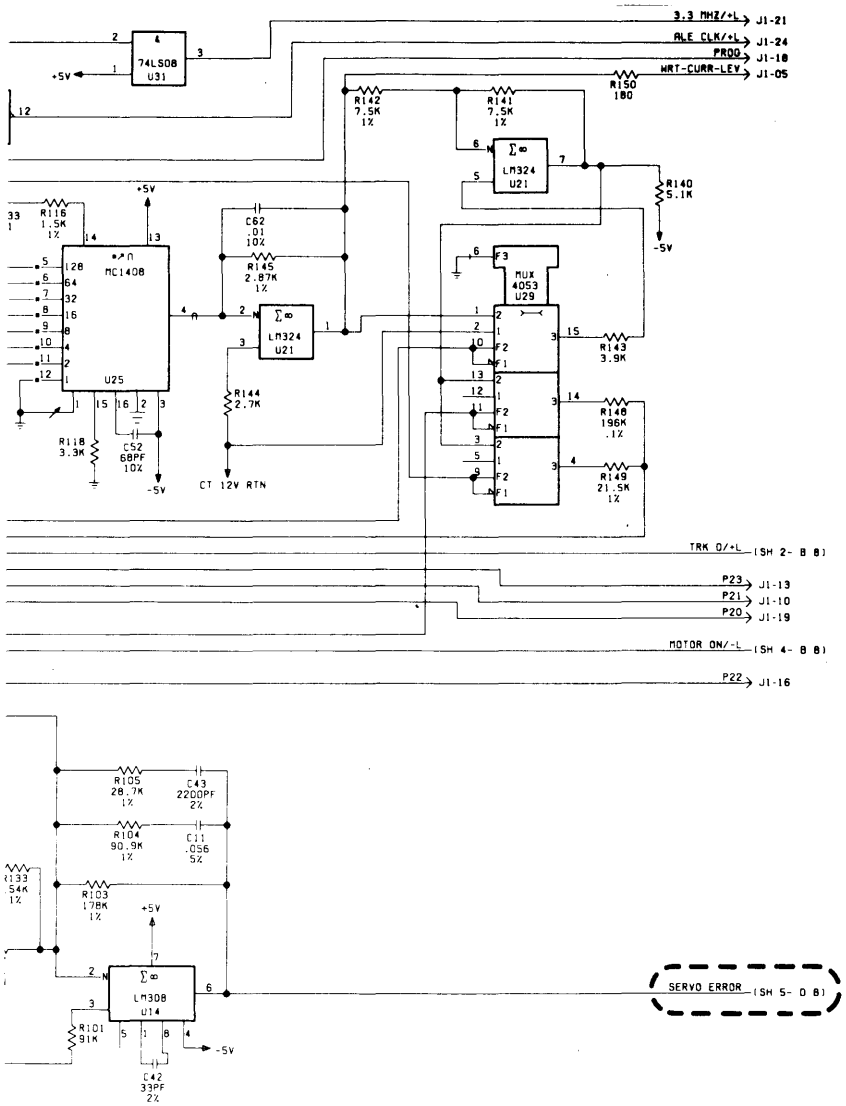


FIGURE 5-2. SERVO SCHEMATIC
(SHEET 3)

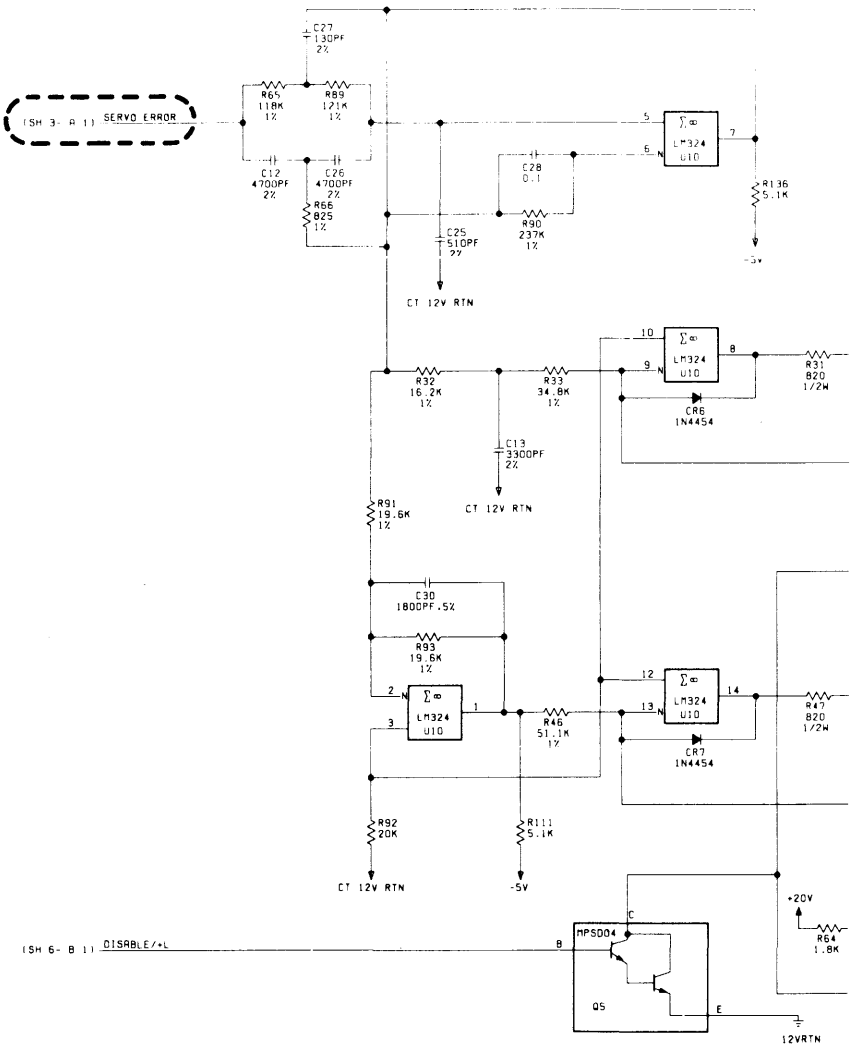


FIGURE 5-3. SERVO SCHEMATIC
(SHEET 5)

5.4 LOGIC SYMBOLOGY

Examples of logic symbology are shown in Table 5-2. Refer to an Integrated Circuit Manufacturer's Handbook for specific Large Scale Integrated Circuit specifications and descriptions.

5.4.1 IC PACKAGE LAYOUT

The pin locations for typical Integrated Circuit (IC) packages are shown below.

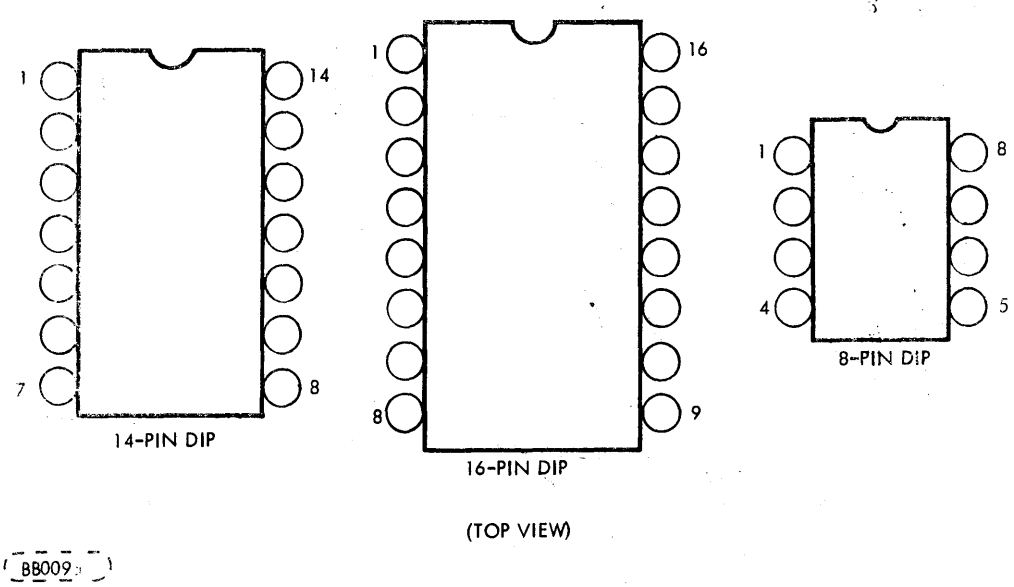
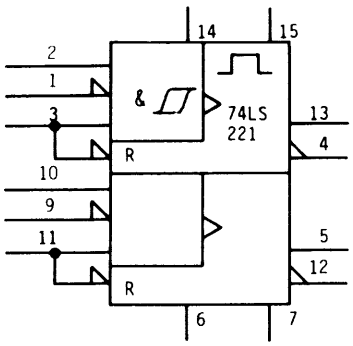


FIGURE 5-4. IC PACKAGE LAYOUT

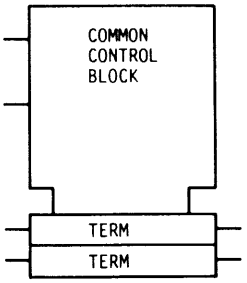
TABLE 5-2. LOGIC SYMBOLOGY EXAMPLES



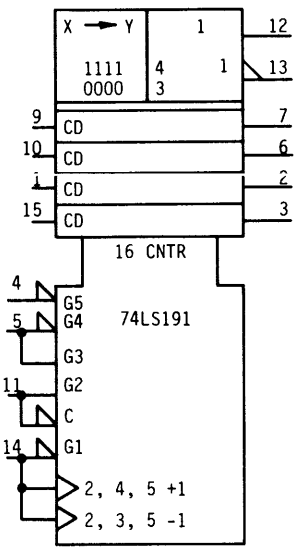
THE 74LS221 IS A DUAL MONOSTABLE MULTIVIBRATOR WITH SCHMITT TRIGGER INPUTS. THE TWO SECTIONS ARE INDEPENDENT EXCEPT FOR A COMMON POWER SOURCE.

TRIGGERING OCCURS AT A PARTICULAR INPUT VOLTAGE LEVEL AND IS NOT DIRECTLY RELATED TO TRANSITION TIME OF THE INPUT SIGNAL. HYSTERESIS INPUT ALLOWS JITTER FREE TRIGGERING.

PIN 2 (10) GENERATES A TRIGGER ON ITS POSITIVE GOING SLOPE OR INHIBITS THE TRIGGER WHEN LOW. PIN 1 (9) GENERATES A TRIGGER ON ITS NEGATIVE GOING SLOPE OR INHIBITS THE TRIGGER WHEN HIGH. PIN 3 (11) ENABLES THE TRIGGER WHEN HIGH OR INHIBITS THE TRIGGER AND RESETS THE MONOSTABLE WHEN LOW. PINS 13 (5) AND 4 (12) ARE RESPECTIVELY THE POSITIVE AND NEGATIVE GOING PULSE OUTPUTS. EXTERNAL R-C COMPONENTS CONNECTED TO PINS 14 AND 15 (6 AND 7) DETERMINE THE DURATION OF THE OUTPUT PULSE.



INPUTS TO THE COMMON CONTROL BLOCK AFFECT EVERY TERM IN THE ARRAY. INPUTS TO EACH TERM AFFECT ONLY THAT TERM.



THE 74LS191 IS A SYNCHRONOUS UP/DOWN COUNTER. EACH STAGE HAS AN INPUT AND AN OUTPUT PIN AS FOLLOWS:

INPUT	STAGE	OUTPUT
9	D	7
10	C	6
1	B	2
15	A	3

WHEN OPERATED AS A COUNTER, STAGE A IS THE LEAST SIGNIFICANT BIT.

PIN 4 WHEN LOW (G5) "SELECTS" THE IC AND ENABLES IT TO RESPOND TO OTHER CONTROL SIGNALS.

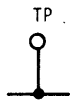
PIN 11 WHEN LOW (C) ENABLES PARALLEL INPUT. ALL FOUR STAGES ASSUME THE STATE OF THE INPUT PINS. WHEN PIN 11 IS HIGH (G2) DATA INPUTS ARE DISABLED AND THE COUNTER IS ENABLED.

PIN 5 WHEN LOW (G4) PERMITS THE COUNTER TO INCREMENT. PIN 5 WHEN HIGH (G3) PERMITS THE COUNTER TO DECREMENT.

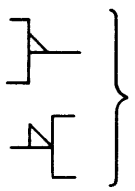
PIN 14 (G1) IS THE "CLOCK" INPUT. WHEN THE COUNTER IS ENABLED, A LOW TO HIGH TRANSITION OF PIN 14 CAUSES THE COUNTER TO CHANGE STATE.

PIN 13 IS THE "RIPPLE CLOCK OUT" TO PERMIT COUNTERS TO BE CASCADED.

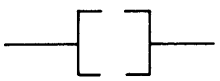
PIN 12 INDICATES MAX/MIN WHICH ANTICIPATES THE "RIPPLE CLOCK".



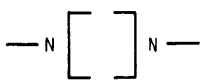
TEST POINT



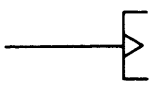
LOGIC POLARITY INDICATOR- "LO" ACTIVE STATE.



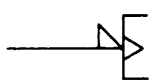
IMPLIED SIGN INDICATOR- ABSENCE OF AN N SIGN INDICATOR IMPLIES A NON-INVERTING SIGNAL RELATIVE TO OTHER IMPLIED SIGN SIGNAL LINES. EFFECT IS THE SAME AS THE USE OF P SIGN INDICATOR INTERNALLY.



SIGN INDICATOR-USED TO INDICATE INVERSION RELATIVE TO IMPLIED SIGN SIGNAL LINES.



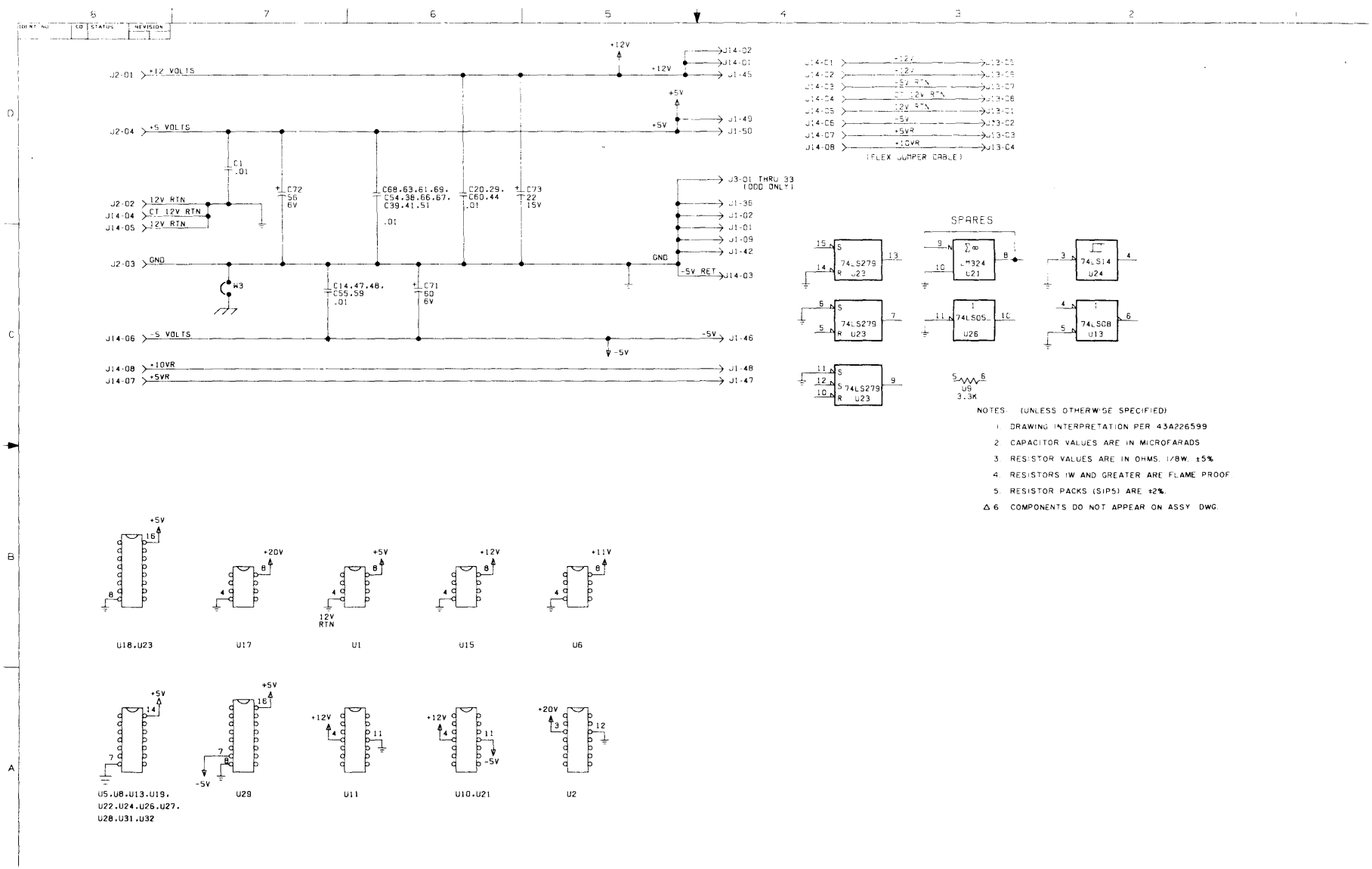
DYNAMIC INPUT ACTIVE DURING THE TRANSITION FROM LOW TO HIGH STATE



DYNAMIC INPUT ACTIVE DURING THE TRANSITION FROM HIGH TO LOW STATE

X/Y	BINARY LEVEL CONVERTER
I	"OR" GATE
&	"AND" GATE
	SCHMITT TRIGGER - CIRCUIT WITH PULSE SHAPING CAPABILITIES
Σ∞	SUMMING AMPLIFIER
X → Y	CODER-INPUT CODE X CONVERTED TO OUTPUT CODE Y

FF235



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. DRAWING INTERPRETATION PER 43A226599
2. CAPACITOR VALUES ARE IN MICROFARADS
3. RESISTOR VALUES ARE IN OHMS, 1/8W, ±5%
4. RESISTORS 1W AND GREATER ARE FLAME PROOF
5. RESISTOR PACKS (SIP5) ARE ±2%.
Δ 6. COMPONENTS DO NOT APPEAR ON ASSY DWG.

FIGURE 5-5. SERVO SCHEMATIC (SHEET 1 OF 9)

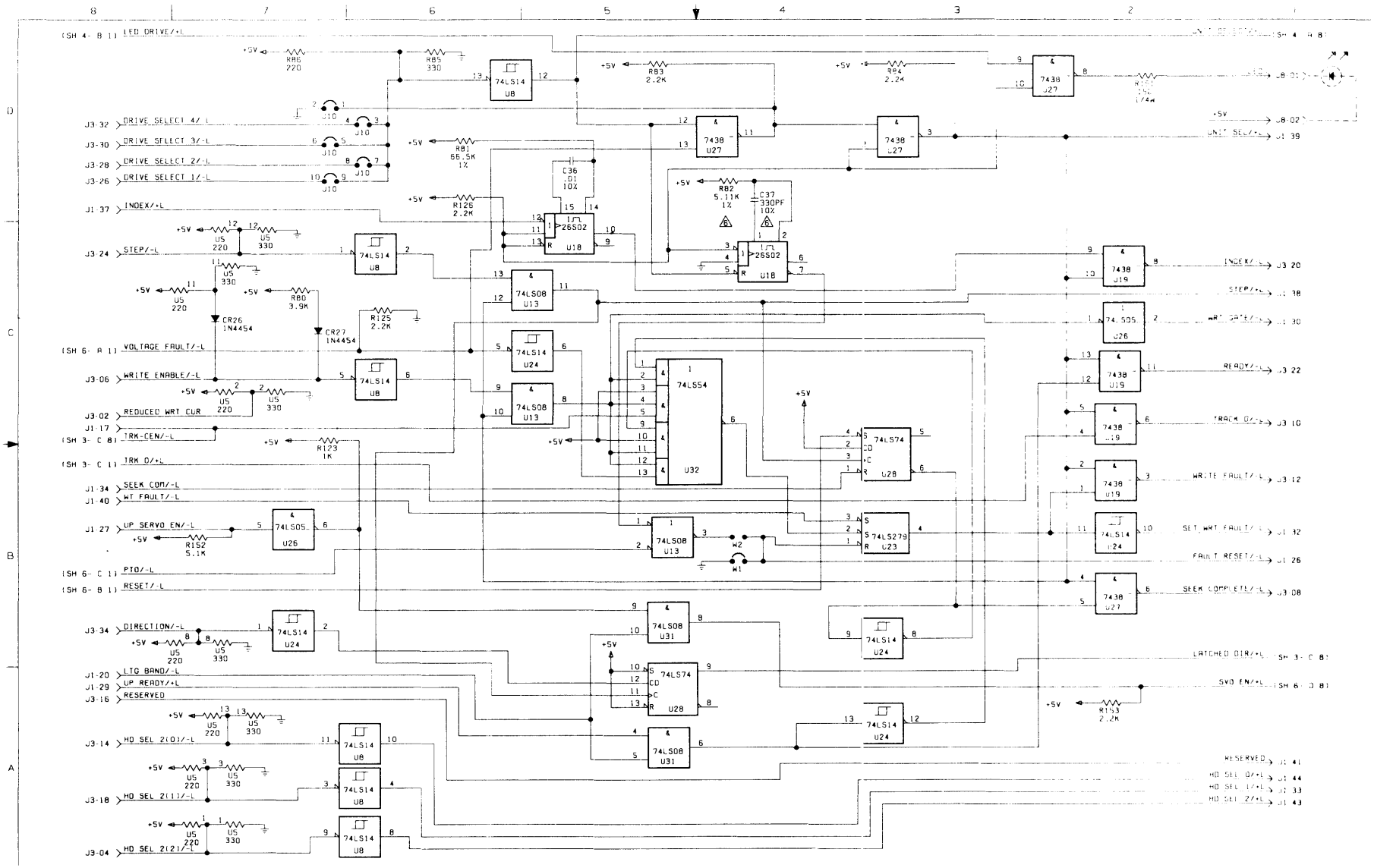


FIGURE 5-5. SERVO SCHEMATIC (SHEET 2 OF 9)

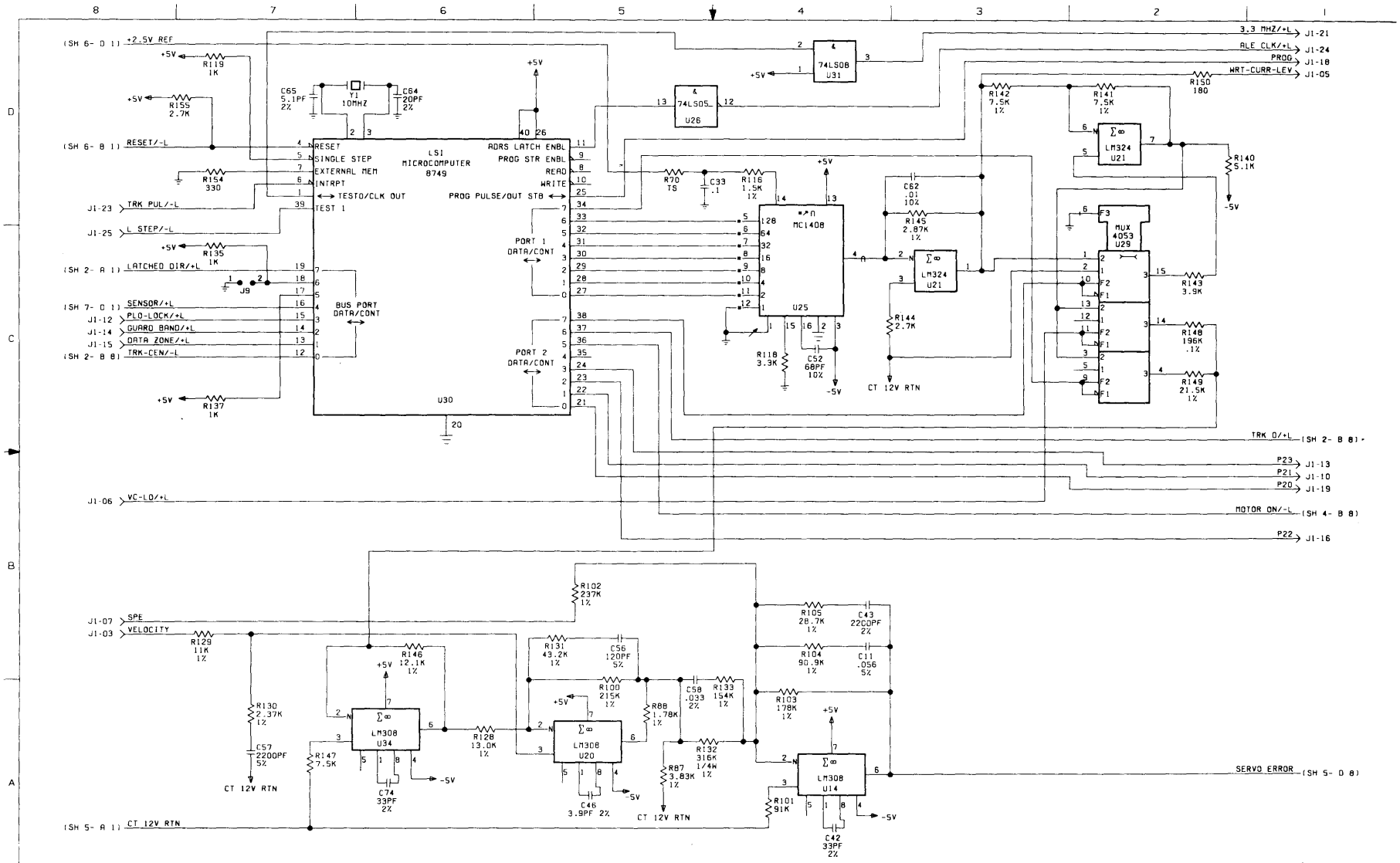


FIGURE 5-5. SERVO SCHEMATIC (SHEET 3 OF 9)

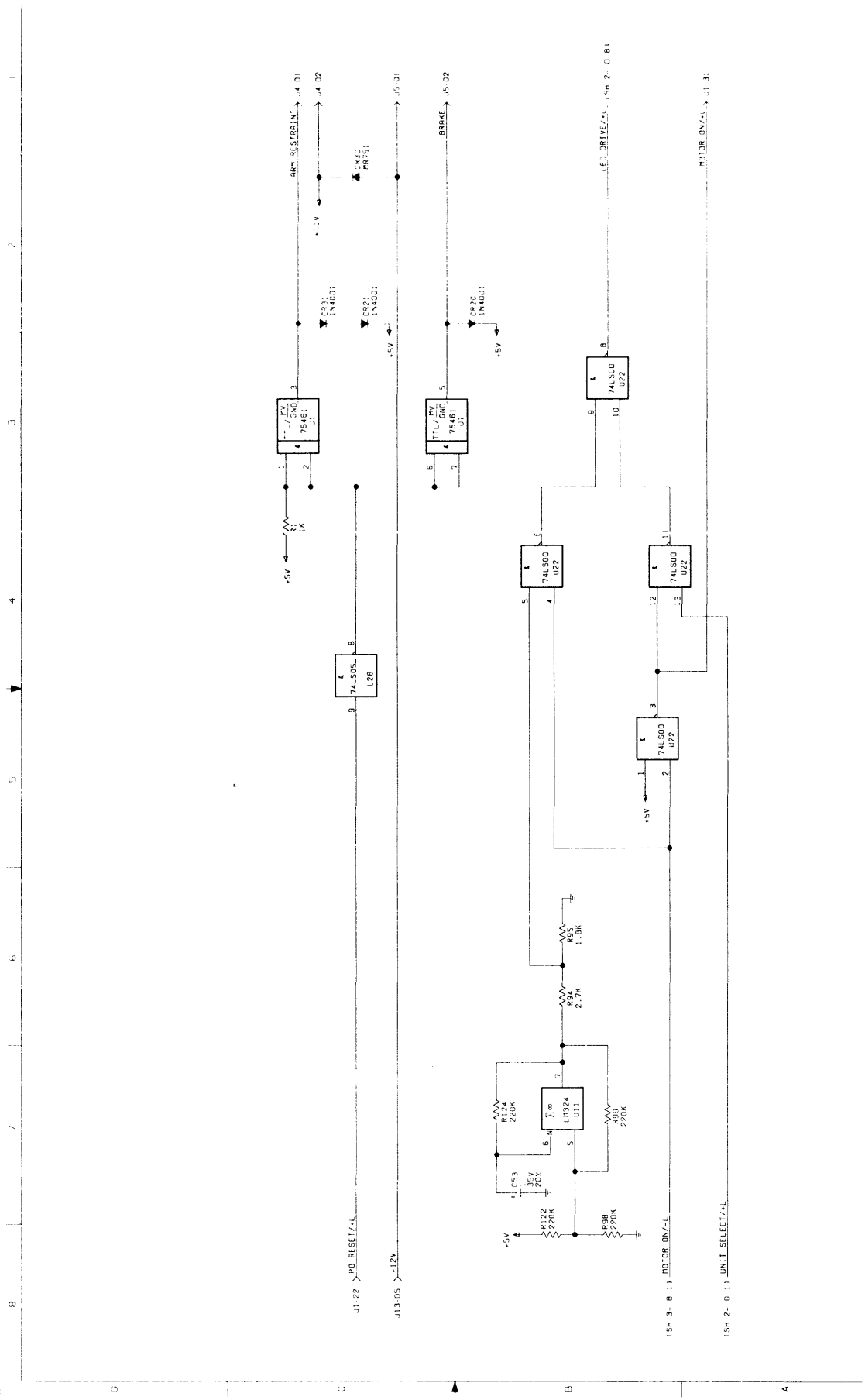


FIGURE 5-5. SERVO SCHEMATIC (SHEET 4 OF 9)

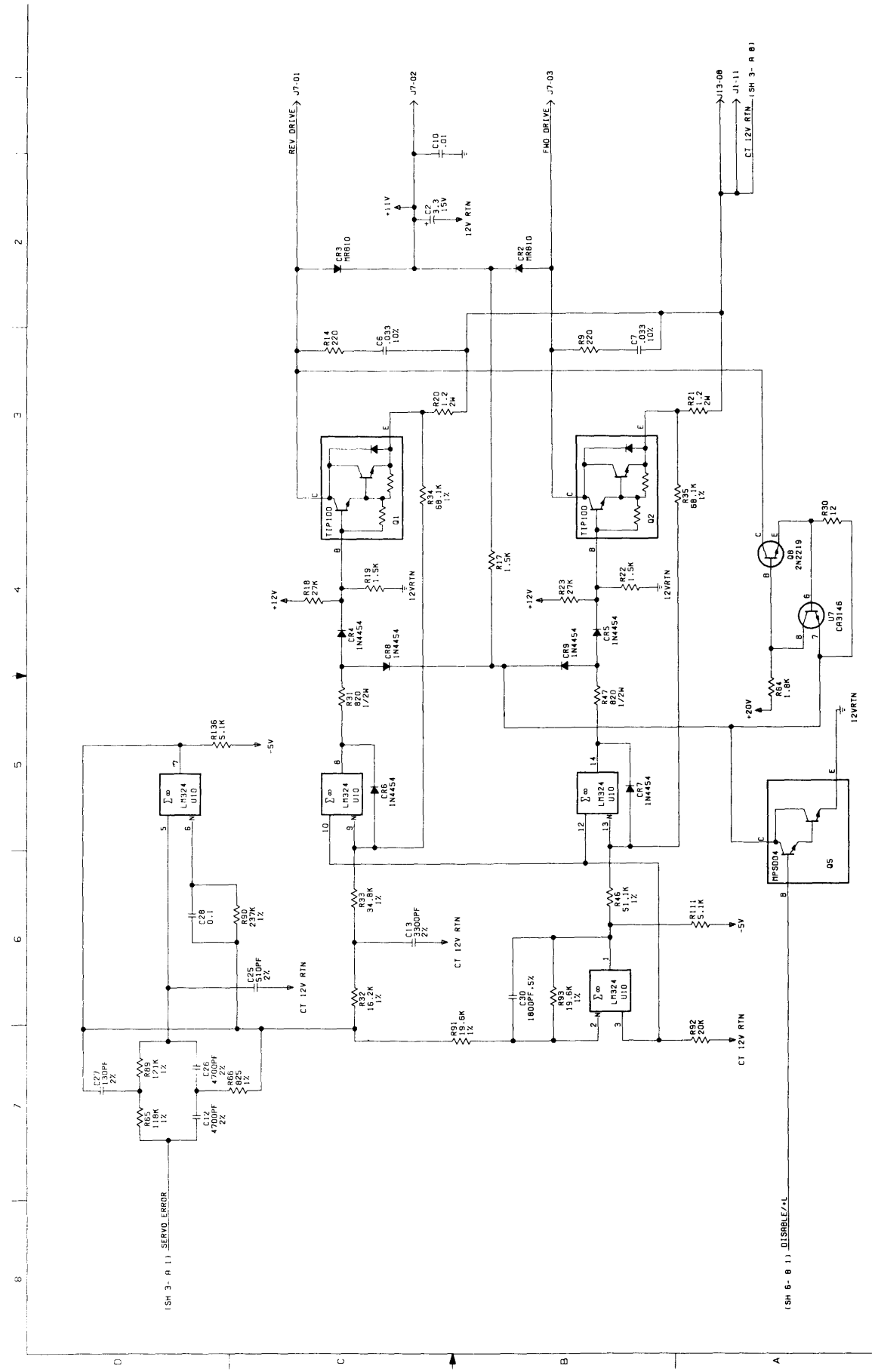


FIGURE 5-5. SERVO SCHEMATIC (SHEET 5 OF 9)

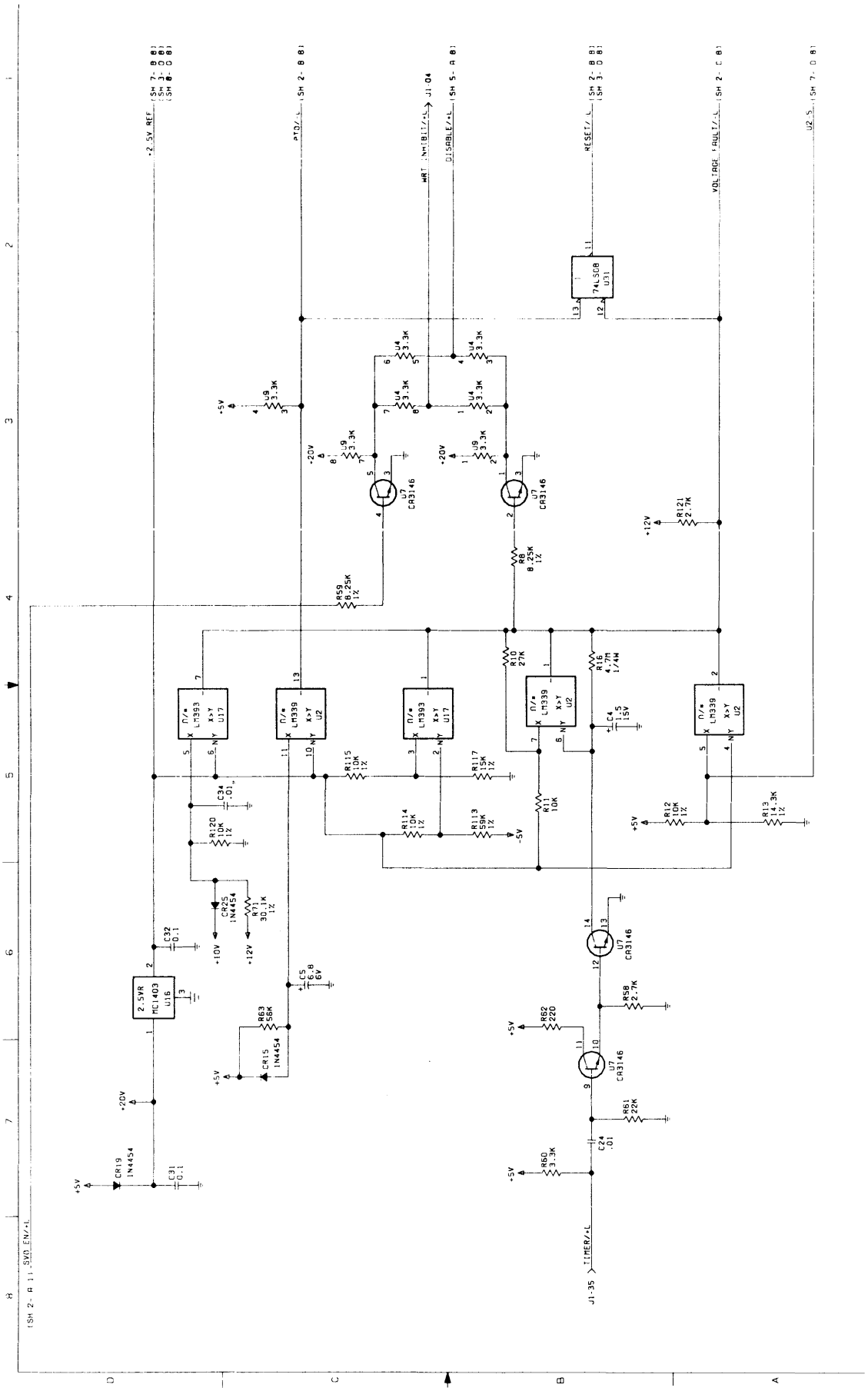


FIGURE 5-5. SERVO SCHEMATIC (SHEET 6 OF 9)

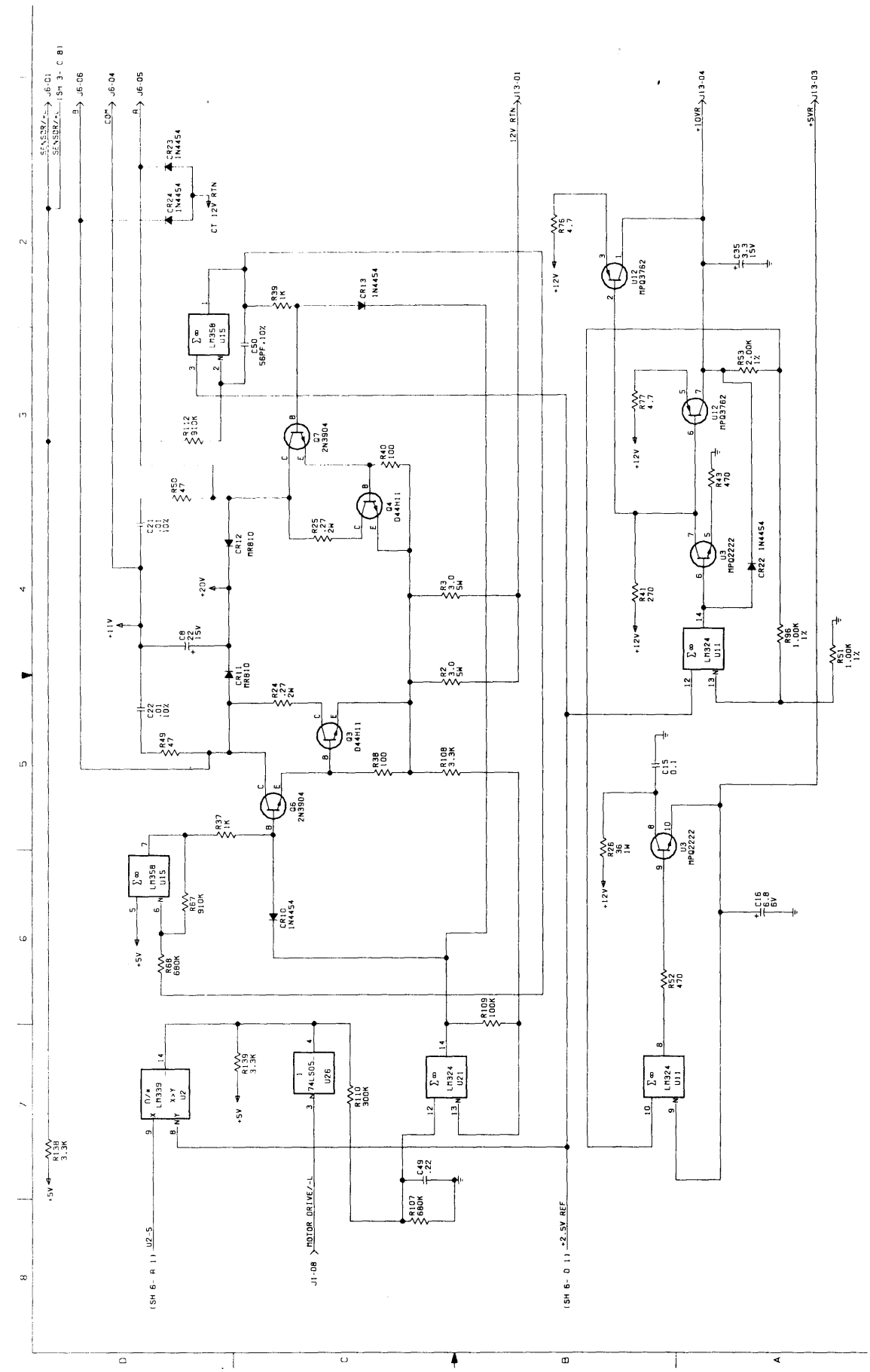


FIGURE 5-5. SERVO SCHEMATIC (SHEET 7 OF 9)

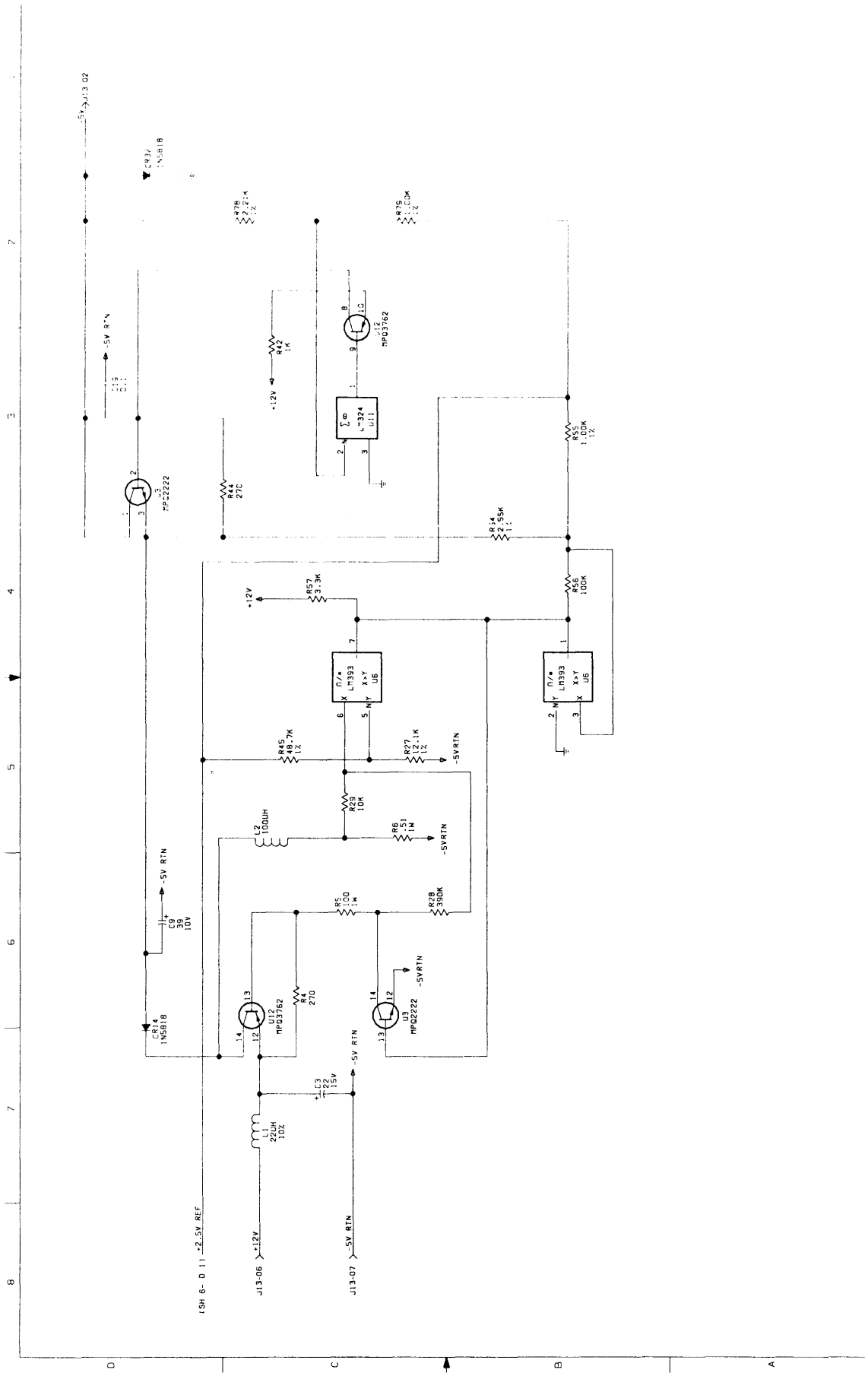


FIGURE 5-5. SERVO SCHEMATIC (SHEET 8 OF 9)

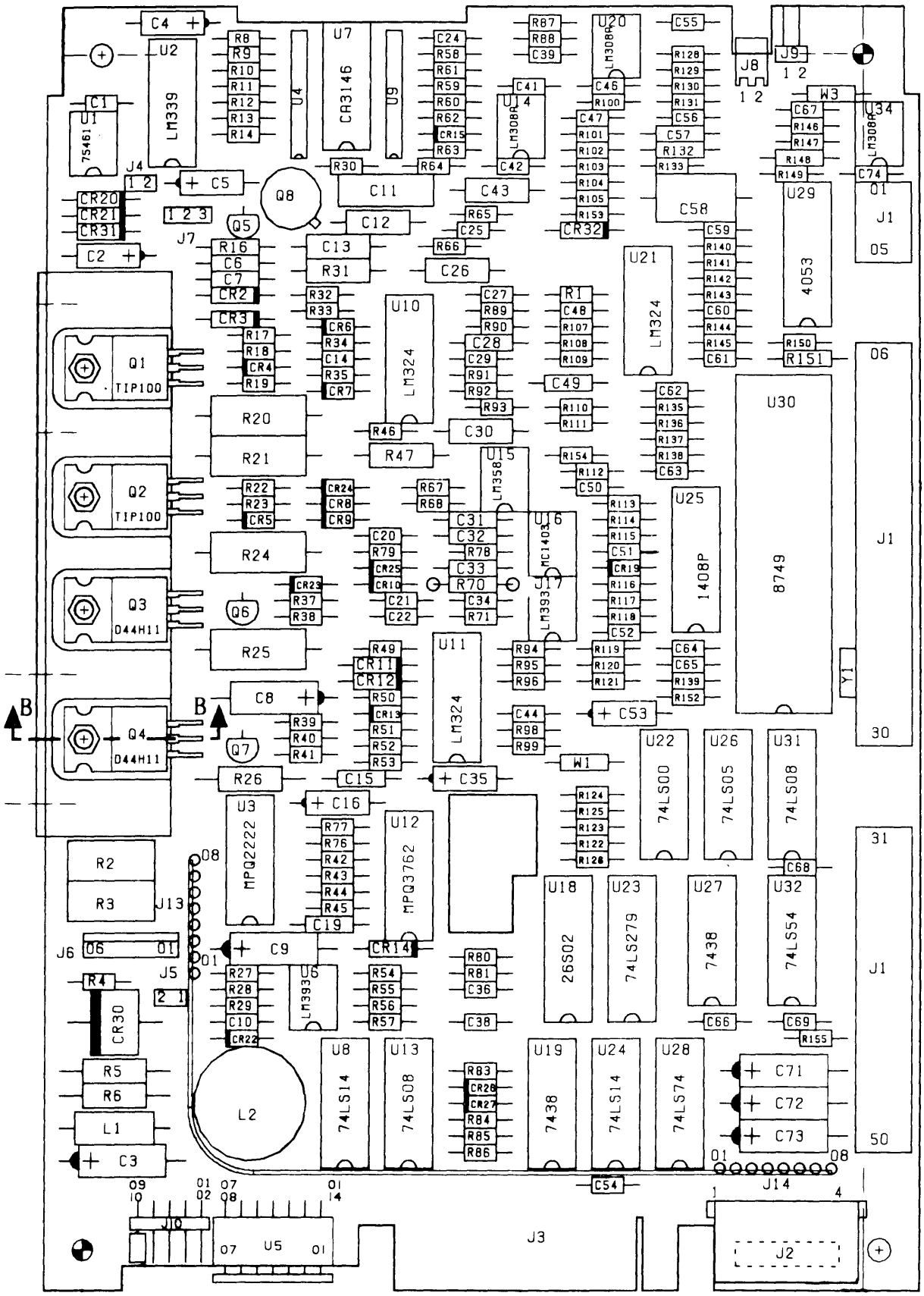


FIGURE 5-5. SERVO PWA (SHEET 9 OF 9)

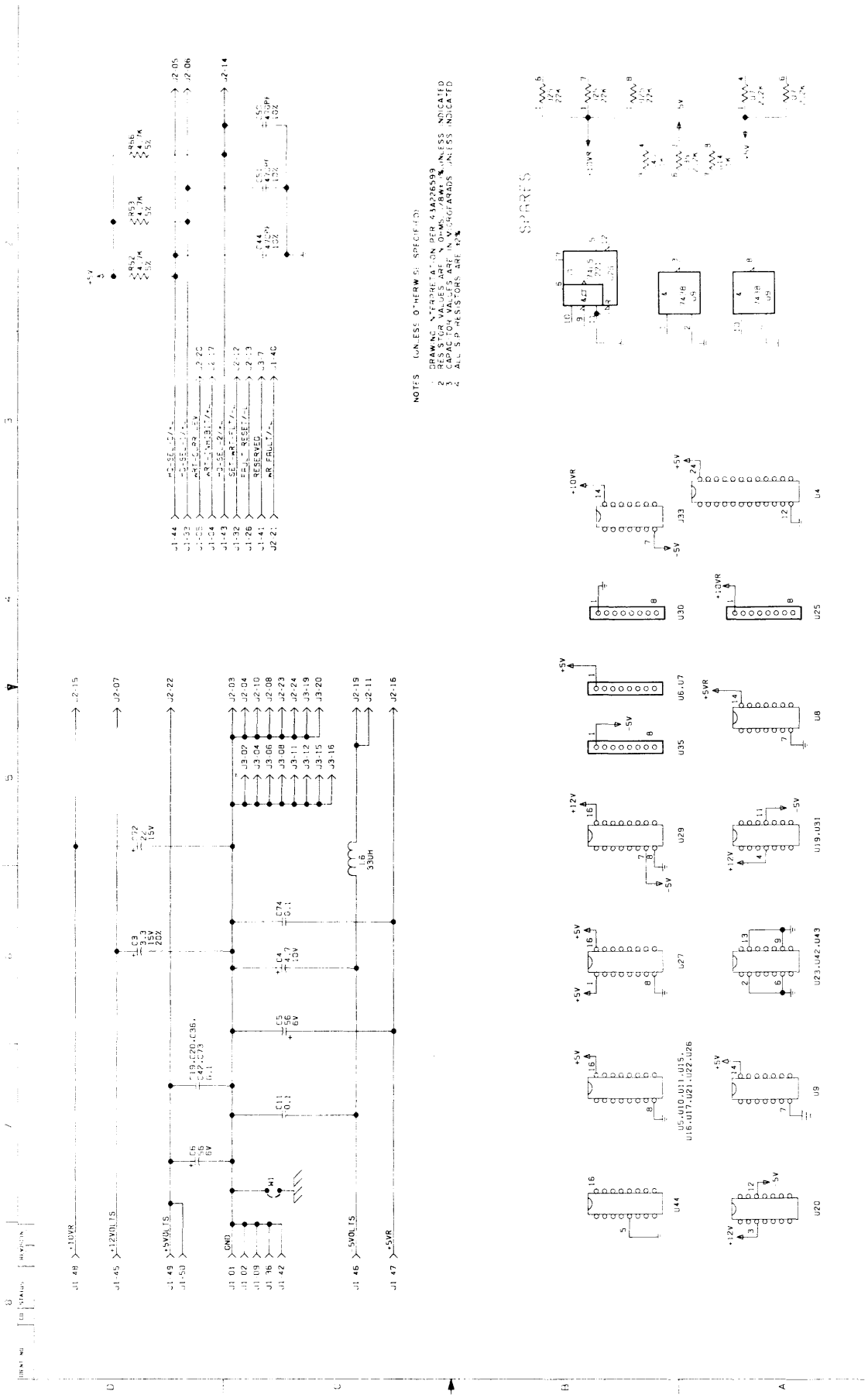


FIGURE 5-6. DATA SCHEMATIC (SHEET 1 OF 6)

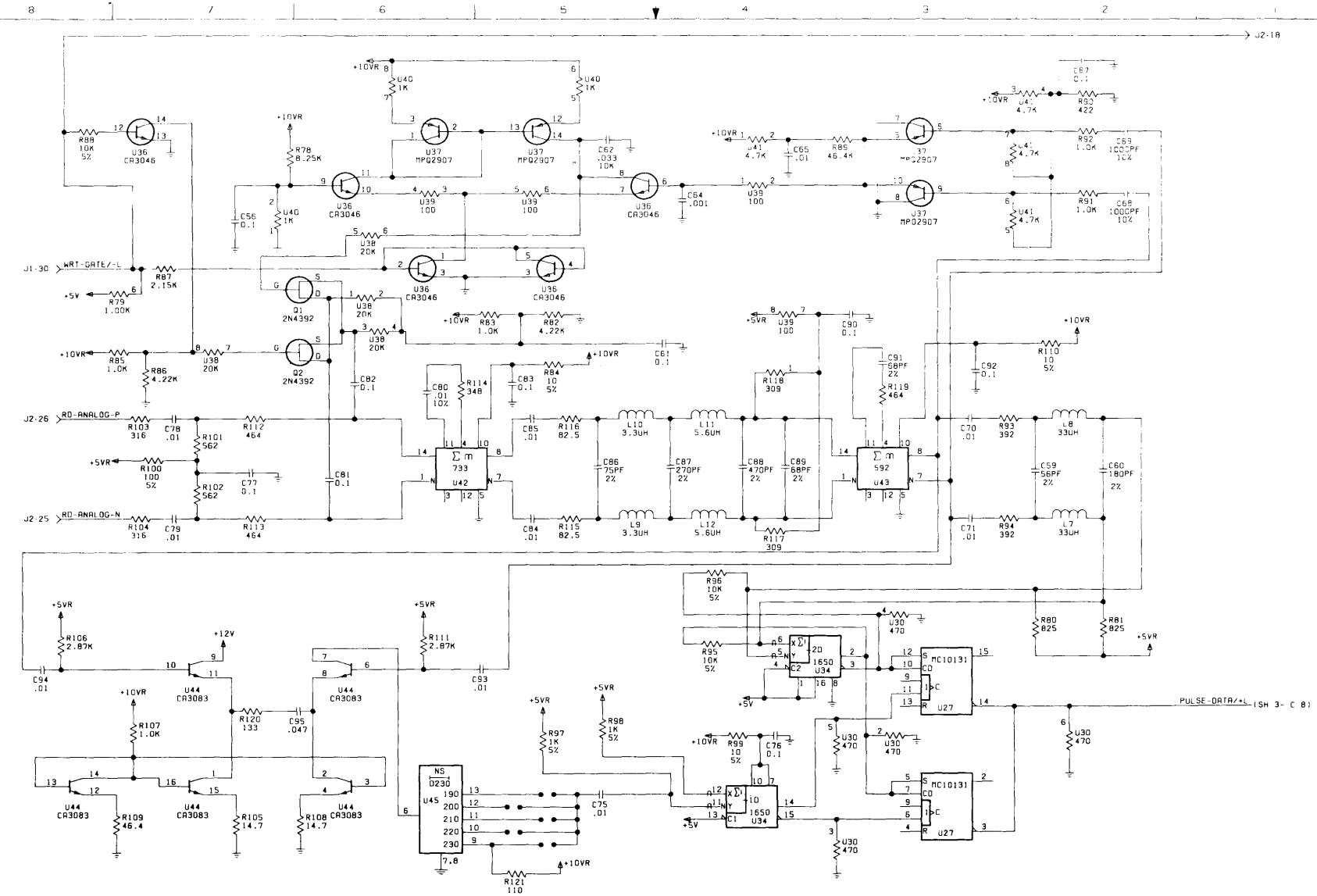


FIGURE 5-6. DATA SCHEMATIC (SHEET 2 OF 6)

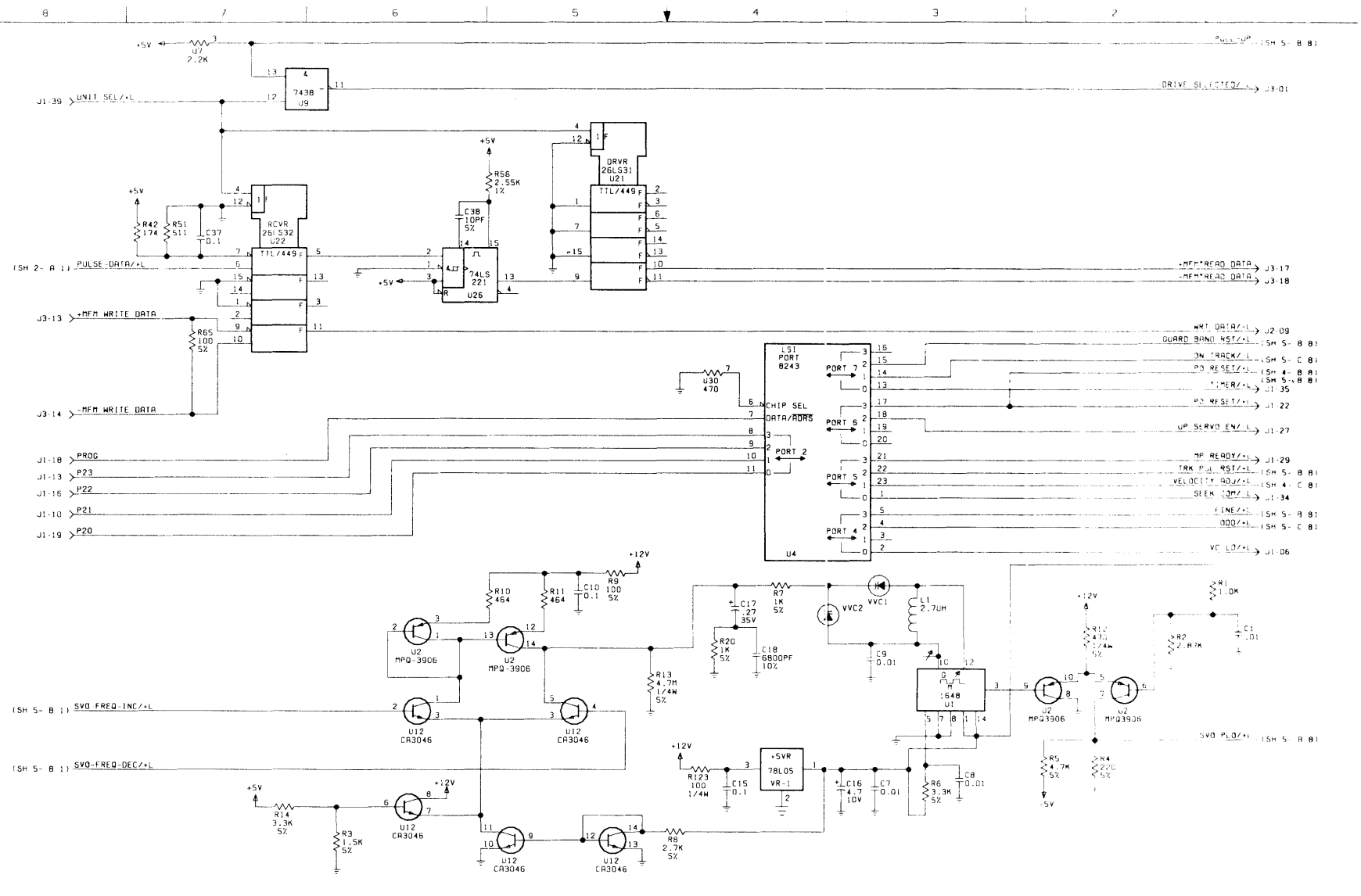


FIGURE 5-6. DATA SCHEMATIC (SHEET 3 OF 6)

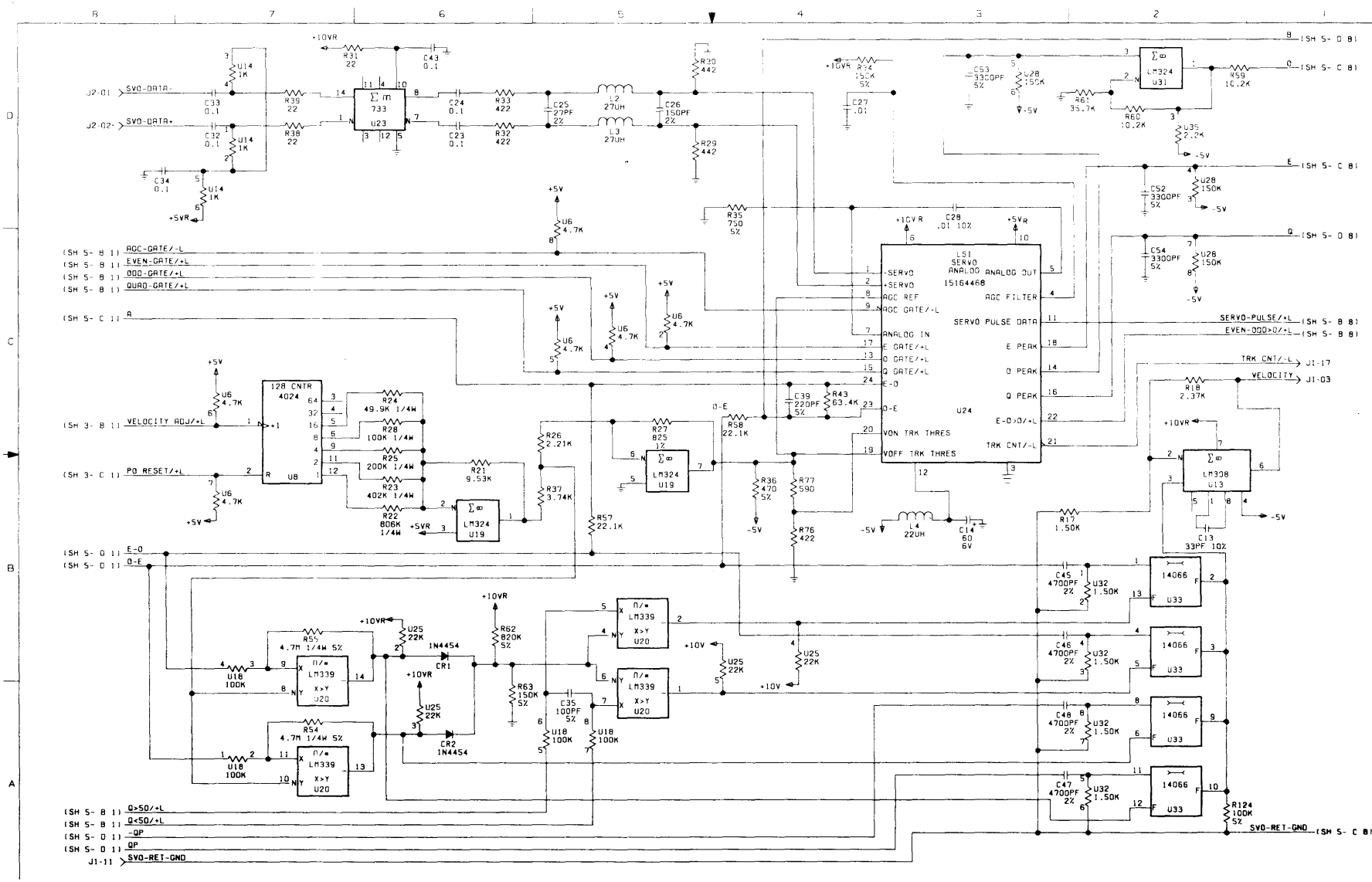


FIGURE 5-6. DATA SCHEMATIC (SHEET 4 OF 6)

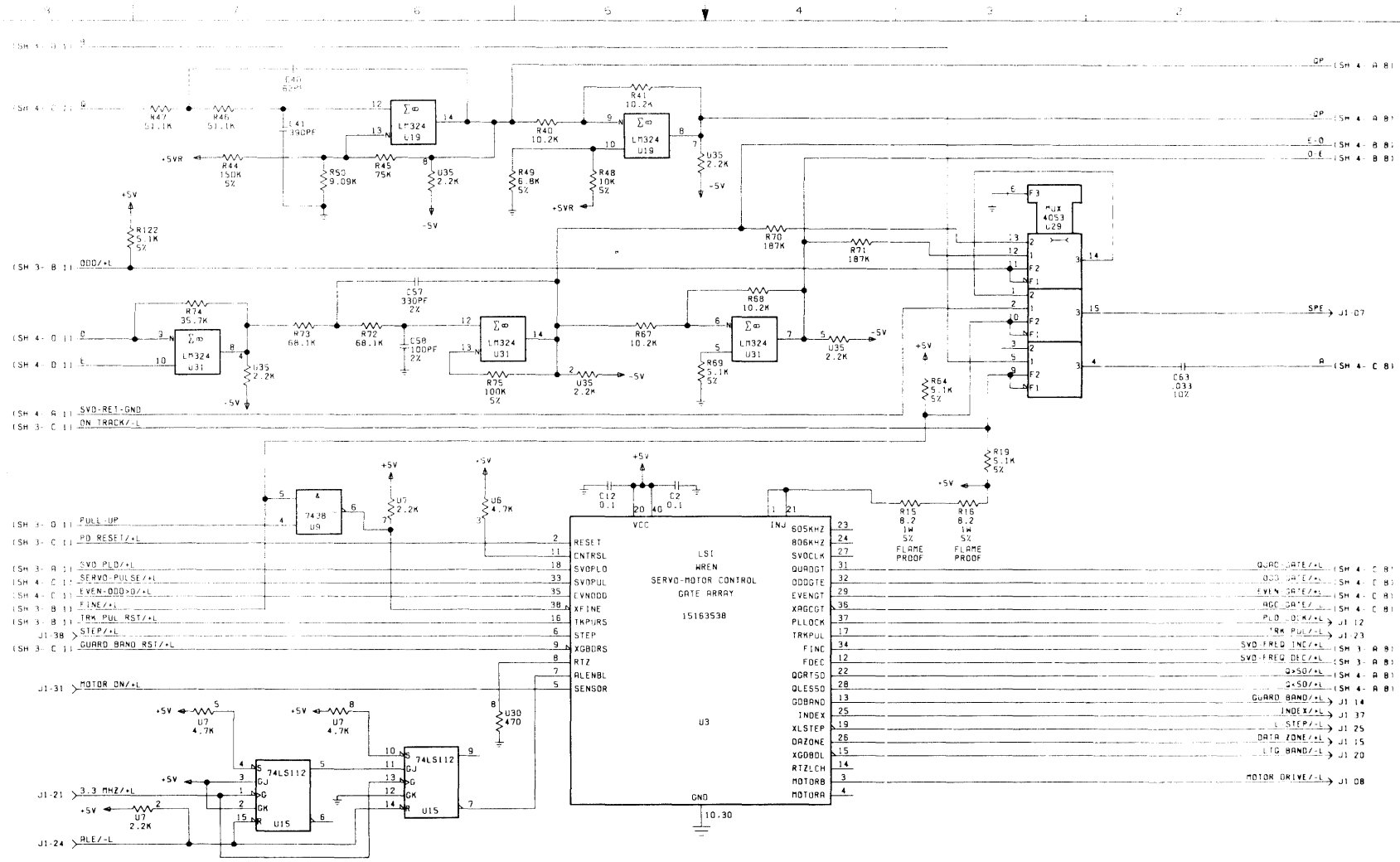


FIGURE 5-6. DATA SCHEMATIC (SHEET 5 OF 6)

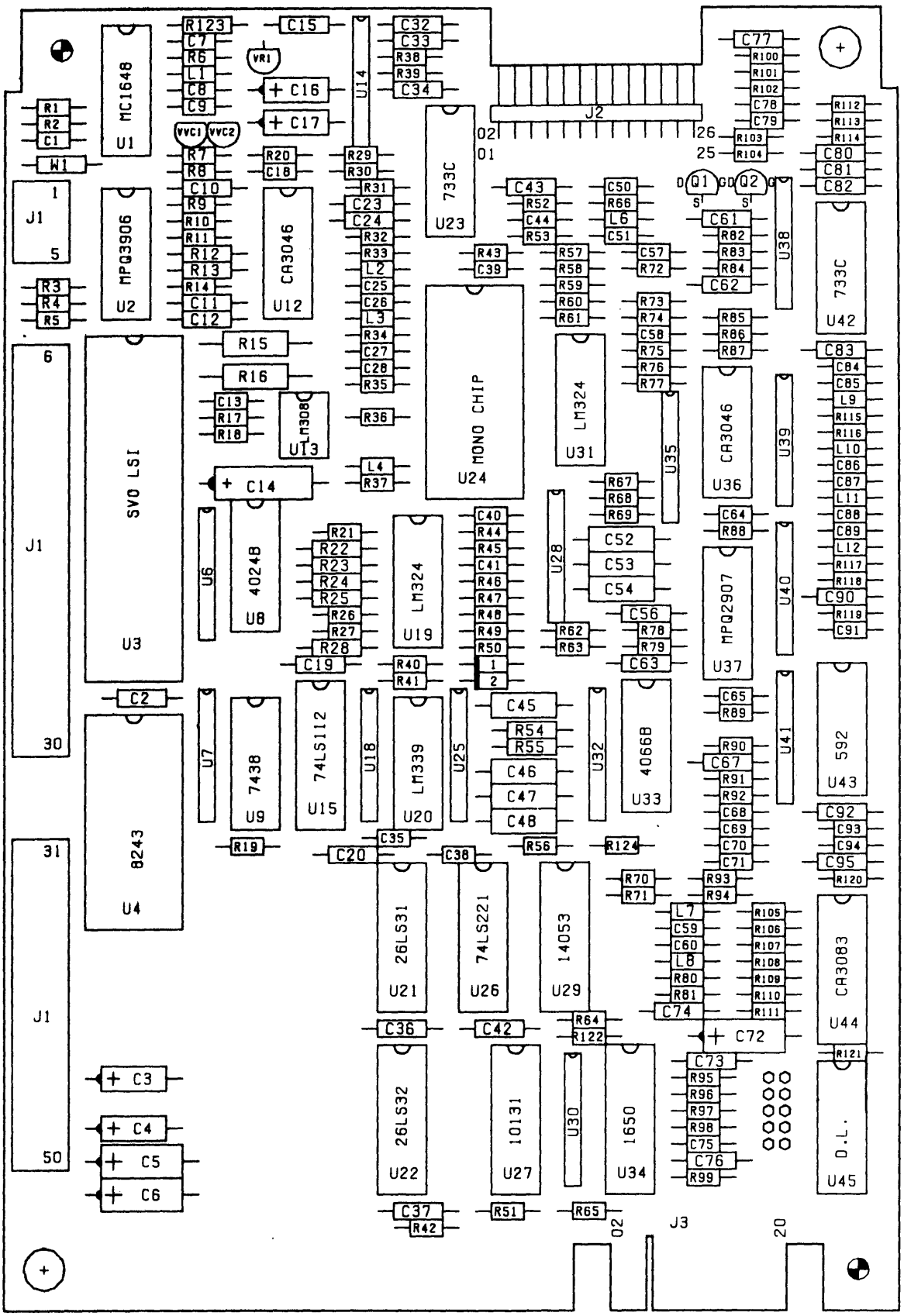


FIGURE 5-6. DATA PWA (SHEET 6 OF 6)

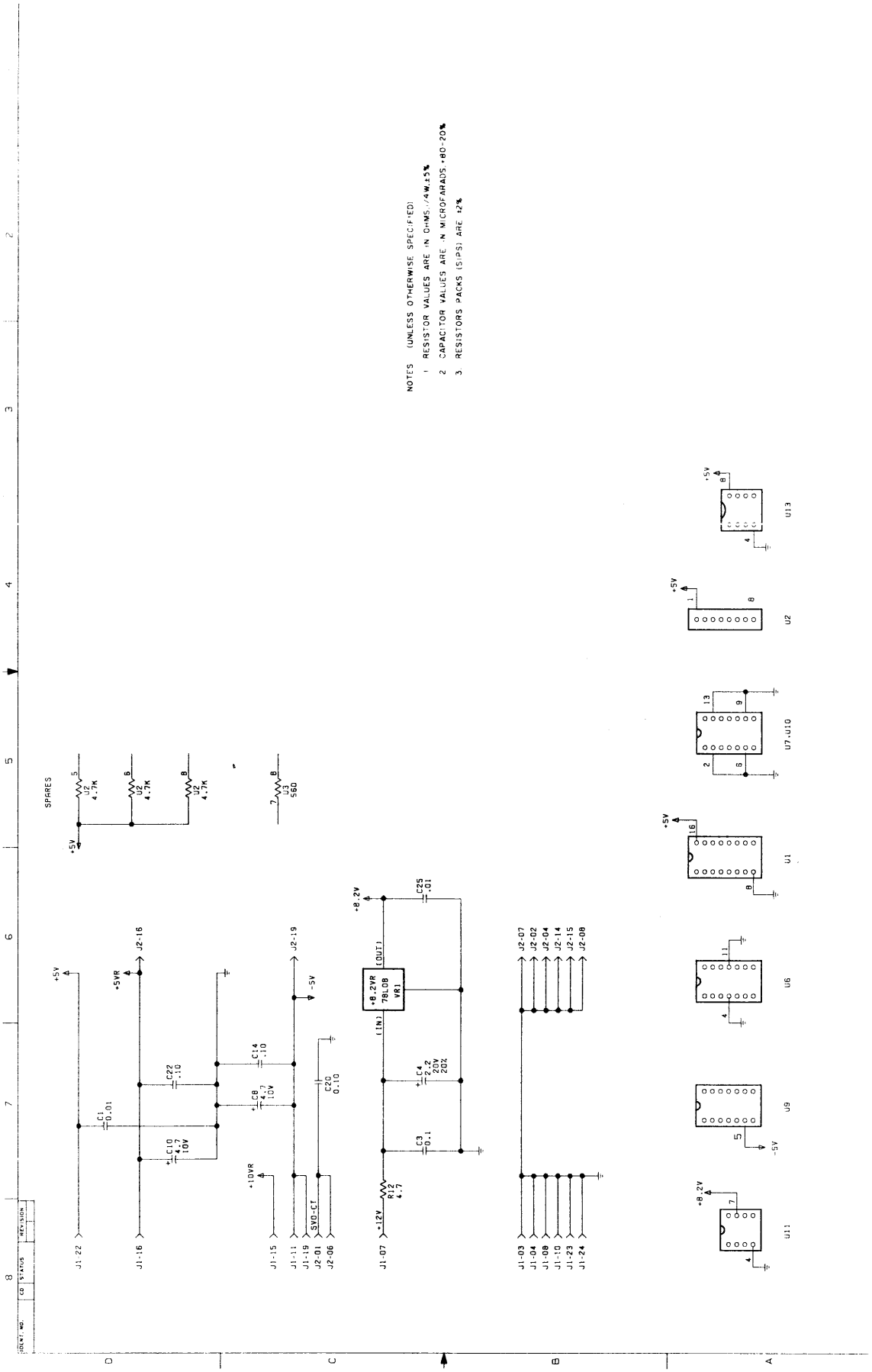


FIGURE 5-7. R/W PREAMP SCHEMATIC (SHEET 1 OF 3)

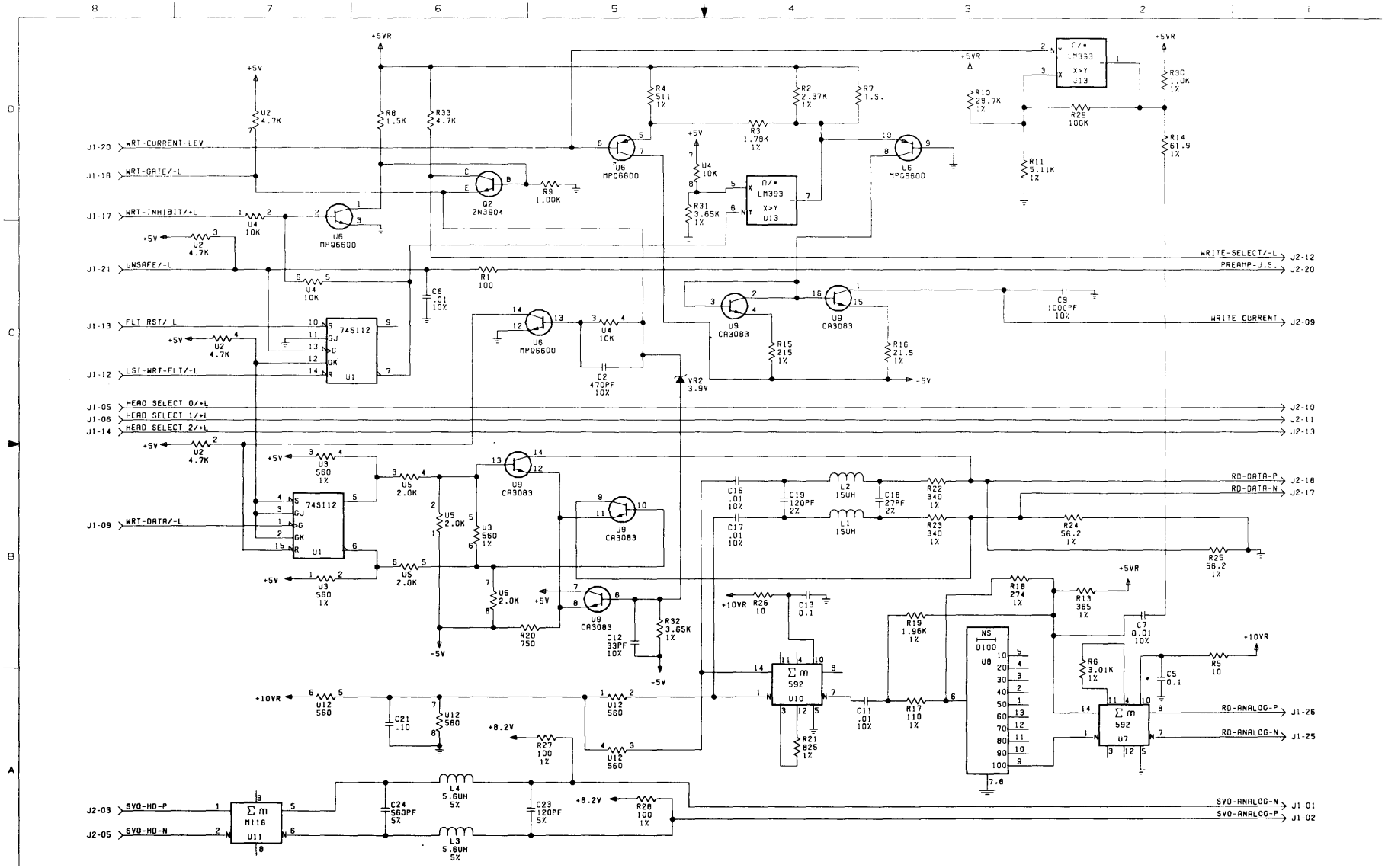


FIGURE 5-7. R/W PREAMP SCHEMATIC (SHEET 2 OF 3)

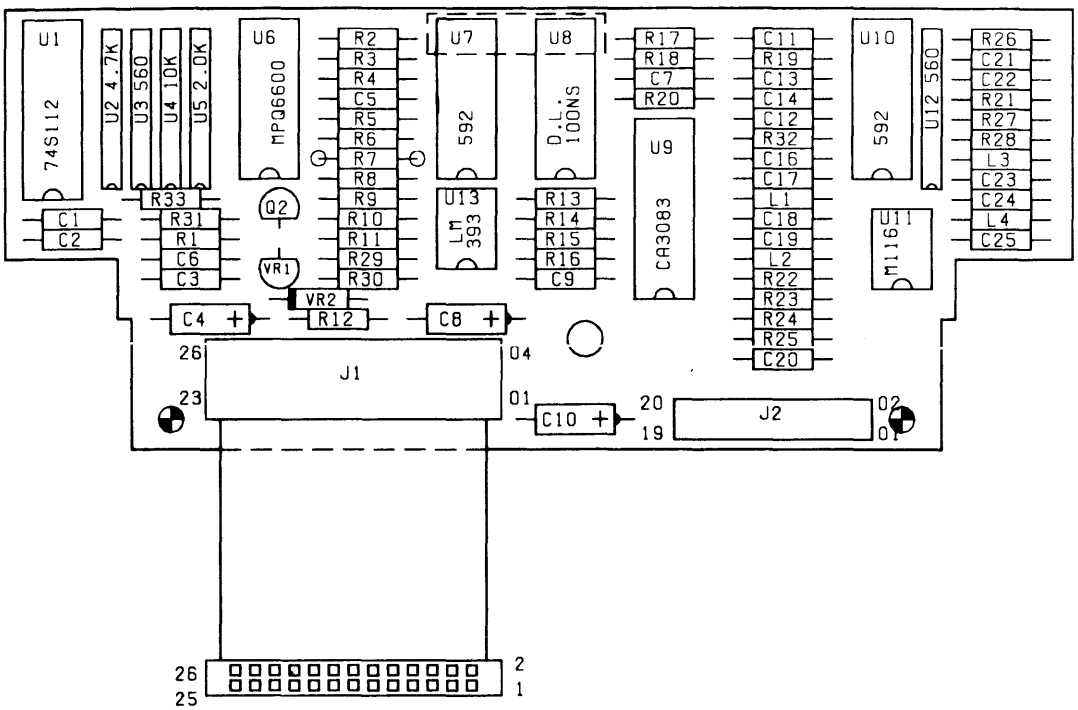
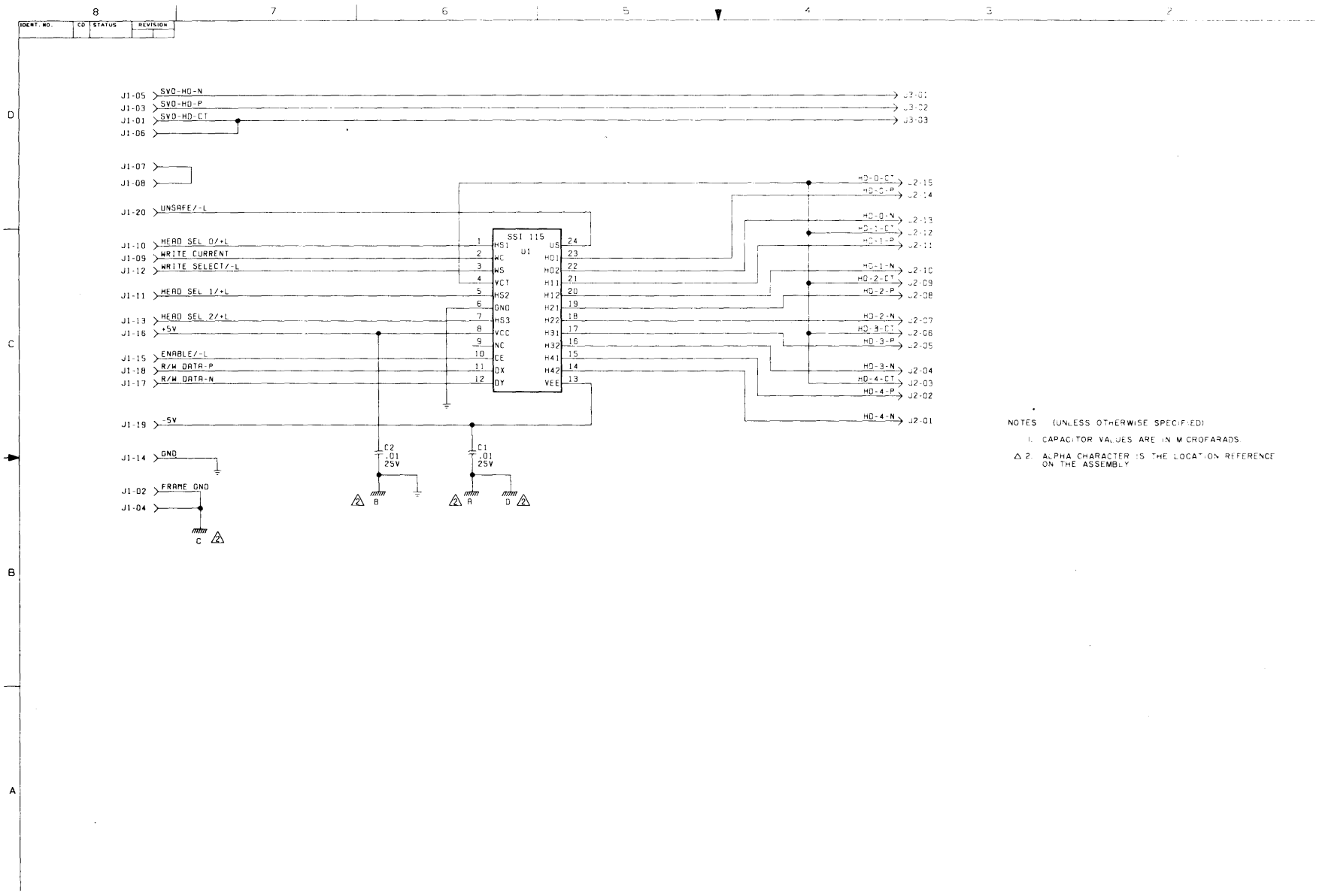


FIGURE 5-7. R/W PREAMP PWA (SHEET 3 OF 3)



NOTES (UNLESS OTHERWISE SPECIFIED)

1. CAPACITOR VALUES ARE IN MICROFARADS.

△2. ALPHA CHARACTER IS THE LOCATION REFERENCE ON THE ASSEMBLY.

FIGURE 5-8. R/W-S FLEX SCHEMATIC (SHEET 1 OF 2)

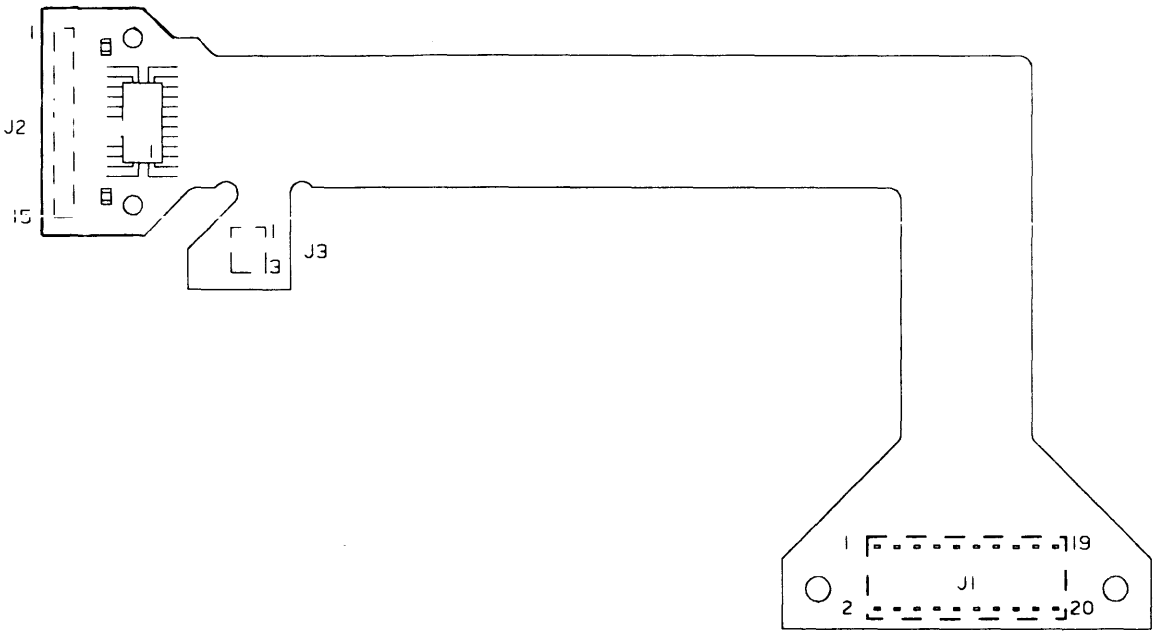


FIGURE 5-8. R/W-S FLEX PWA (SHEET 2 OF 2)

6.1 INTRODUCTION

This section contains the instructions required to maintain the CDC Model 9415-5 WREN Disk Drive. The information presented is provided for corrective maintenance as no preventative maintenance is required. All maintenance should be performed by qualified and trained service personnel.

The maintenance procedures detailed below should be performed only after power to the WREN drive has been turned off, the shipping lock engaged, the DC power, interface, and data-signal cable connectors removed. The drive should then be placed with the chassis on a sponge rubber or foam mat on a flat surface.

The maintenance procedures provided in this section assume that the proper test equipment is available to troubleshoot and replace selected malfunctioning parts. Parts replacement is performed OUTSIDE THE SEALED AREA OF THE DRIVE, ONLY. ENCROACHMENT OF THE SEALED AREA VOIDS THE UNIT WARRANTY.

6.2 SAFETY AND SPECIAL MAINTENANCE PRECAUTIONS

- Avoid overtightening hardware (screws, nuts, etc.) when replacing assemblies and components. All screws and nuts are of the low carbon variety.
- Do not connect or disconnect cables without first removing all power from the drive.

CAUTION

The circuit assemblies contained in this equipment can be degraded or destroyed by ELECTRO-STATIC DISCHARGE (ESD).

Static electrical charges can accumulate quickly on personnel, clothing, and synthetic materials. When brought in close proximity to or, in contact with delicate components, ELECTRO-STATIC DISCHARGE OR FIELDS can cause damage to these parts. This damage may result in degraded reliability or immediate failure of the affected component or assembly.

To insure optimum/reliable equipment operation, it is required that technical support personnel discharge themselves by periodically touching the chassis ground prior to and during the handling of ESD susceptable assemblies. This procedure is very important when handling Printed Circuit Boards.

Printed Circuit Boards should be handled or transported in electrically conductive plastic bags to insure optimum protection against potential ESD damage.

6.3 MAINTENANCE TOOLS

Additional tools other than those normally used by computer and data processing service personnel are required. These tools (Table 6-1) are used to maintain that part of the 9415 WREN Disk Drive external to the sealed area.

TABLE 6-1. SPECIAL TOOLS

PART NUMBER	DESCRIPTION
TBD	TORX TX-15
TBD	TORX TX-09

6.4 MAINTENANCE PROCEDURE

6.4.1 INDEX AND SCHEDULE

The WREN-5 is designed such that preventative maintenance at the user site is not required. Special testing is not required to confirm repairs other than the test that is used to isolate the fault.

6.4.2 REMOVAL AND REPLACEMENT PROCEDURE LIST

Table 6-2 lists the removal and replacement procedures provided in this section. The procedures are for the removal and replacement of recommended spare assemblies and components for the WREN.

TABLE 6-2. LIST OF REMOVAL AND REPLACEMENT PROCEDURES

Paragraph No.	Removal and Replacement Procedure
6.4.2.1	LED/Mount
6.4.2.2	PWA, R/W Preamp
6.4.2.3	PWA, Servo-5
6.4.2.4	PWA, Data-5
6.4.2.5	Ground Spring
6.4.2.6	Brake Mechanism

6.4.2.1 LED/MOUNT REMOVAL AND REPLACEMENT

1. Remove power from WREN disk drive.
2. Engage shipping lock.
3. Disconnect DC power, interface, and data - signal cables.
4. Place the WREN on a sponge rubber or foam pad on a flat surface with the chassis down.
5. Remove front panel by removing the two mounting screws.
6. Remove the section of the LED mount by prying it up with a small flat blade screwdriver.
7. Slide the LED out the front of the front panel.
8. Remove LED from mount section.

Replace LED by reversing the procedure.

NOTE
The shorter lead of the LED is nearest to the outside edge of the front panel.

6.4.2.2 R/W PREAMP PWA REMOVAL AND REPLACEMENT

1. Follow instructions 1-5 in paragraph 6.4.2.1.
2. Remove mounting screw in middle of the R/W Preamp.
3. Carefully pull the R/W Preamp away from the drive. This disengages the connection from the R/W Preamp to the servo PWA.

4. Disconnect the cable coupling the R/W Preamp and the Data PWA at the Data PWA.

The R/W Preamp is installed by reversing these instructions. When tightening the screw that holds the PWA in place be sure that the two black wires which run under the top cover in that area are not pinched between the flex cable connector and the base deck.

6.4.2.3 SERVO-5 PWA REMOVAL AND REPLACEMENT

1. Follow instructions 1-4 in paragraph 6.4.2.2.
2. Loosen but do not remove the two chassis mounting screws nearest the square end of the cover.
3. Remove the two chassis mounting screws from the rounded end of the cover.

CAUTION

Be sure to support the drive so it does not fall on to the PWA boards.

4. Lift the sealed area of the drive carefully and disconnect the four connections coming from the sealed area.
5. Continue supporting sealed area while removing the two remaining chassis mounting screws (these were loosened in instruction number 2).
6. Place the sealed area on its cover (upside down) on the sponge rubber or foam pad.
7. Remove the 4 screws holding the PWA assembly. Two are located on the bottom and two on the side of the chassis.
8. Remove the 4 screws holding the PWA assembly together.
9. Separate the two PWA boards, being careful not to lose the five spacers (these spacers are on the connector between the boards).

The Servo-5 PWA is installed by reversing these instructions.

6.4.2.4 DATA-5 PWA REMOVAL AND REPLACEMENT

1. Follow instructions 1-9 in paragraph 6.4.2.3.
2. Remove the five spacers, being careful not to lose them.

The Data PWA is installed by reversing these instructions.

6.4.2.5 GROUND SPRING REMOVAL AND REPLACEMENT

1. Follow instructions 1-6 in paragraph 6.4.2.3.
2. Remove the two screws holding the ground spring down.
3. Remove ground spring.

Install ground spring by reversing the instructions.

NOTE

Center the ground spring over the center of the motor as much as possible.

6.4.2.6 BRAKE MECHANISM REMOVAL AND REPLACEMENT

1. Follow instruction 1 in paragraph 6.4.2.5.
2. Remove screw and washer in the center of the brake.

Replacement of Brake Mechanism.

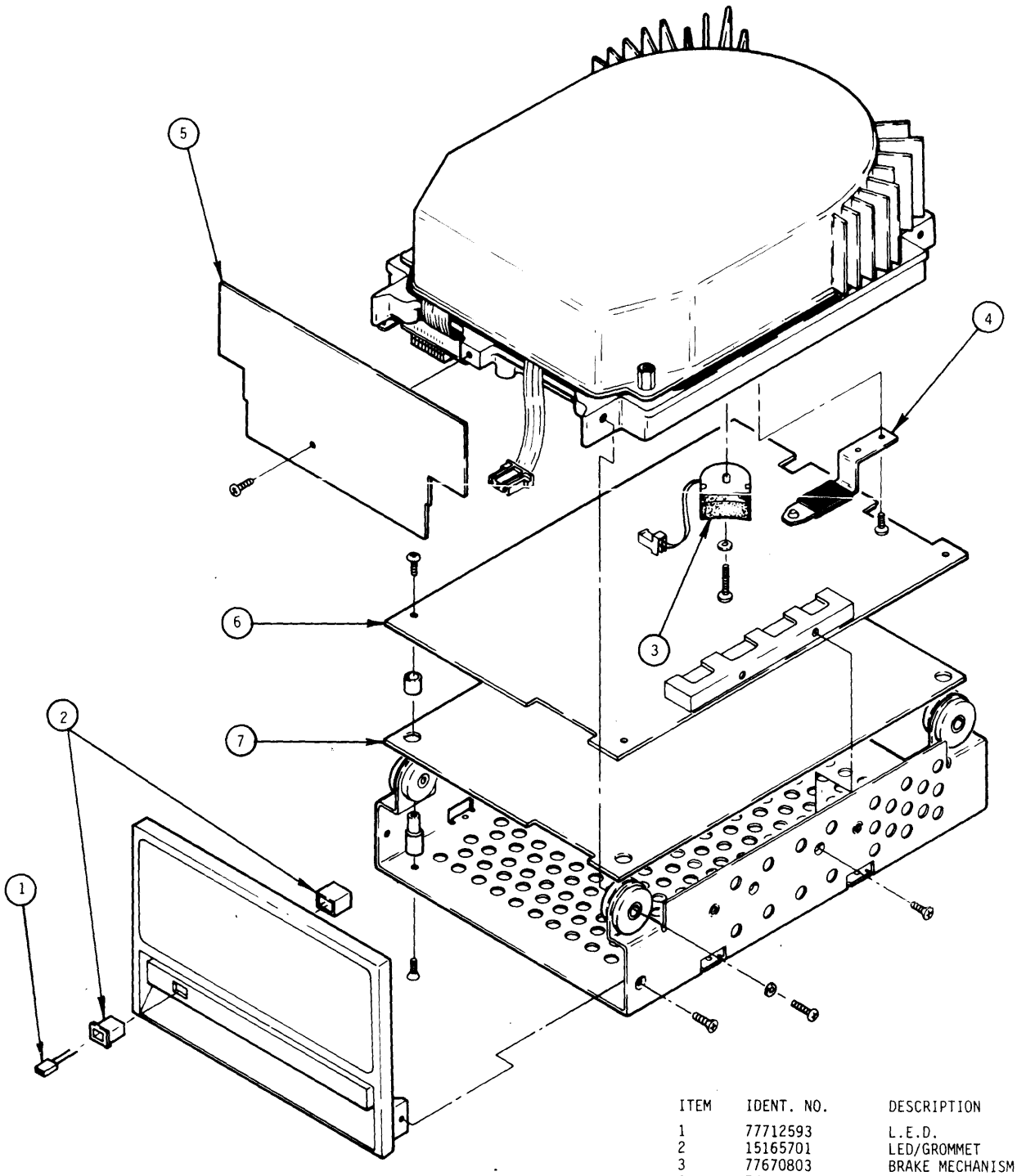
3. Install brake with hinged side away from the ground spring.
4. Install screw and bellville washer, but do not tighten at this time.
5. Insert 0.010 inch shim between brake and motor.
6. Push brake into the motor and tighten screw.
7. Remove shim.
8. Hold brake shoe against brake mechanism and rotate motor counter clockwise. This is a check to make sure brake doesn't hinder operation.
9. Reverse operations in instruction number 1 to finish replacement.

7.1 INTRODUCTION

This section provides the information to order the recommended replaceable parts for the WREN Disk Drive.

7.2 ORDERING PARTS

When ordering replacement parts for the WREN Disk Drive, include the equipment identification number to insure positive identification of parts.



ITEM	IDENT. NO.	DESCRIPTION
1	77712593	L.E.D.
2	15165701	LED/GROMMET
3	77670803	BRAKE MECHANISM
4	77730331	GND SPRING
5	*	R/W PREAMP PWA
6	*	SERVO PWA
7	*	DATA PWA

*REFER TO TABLE 5-1 FOR PRINTED CIRCUIT BOARD IDENTIFICATION NO.

FIGURE 7-1. WREN-5 RECOMMENDED SPARES

USER COMMENTS

	TECHNICAL PUBLICATIONS FILE REFERENCE

Date _____

FROM:

Name _____

Address _____

City _____

State _____ Zip Code _____

Area Code _____ Phone _____

NOTE:

This form is not intended to be used as an order blank. Control Data Corporation welcomes your evalaution of this publication. Please indicate any errors, suggested additions or deletions, or general comments below.

Business-related questions are to be directed to your Local Sales Office.

Equipment Identification _____ Part Number _____ Serial No. _____

Document : (Title/Number/Revision) _____

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