83324220

CONTROL DATA CORPORATION

CDC® STORAGE MODULE DRIVE

BJ501

BJ5D7

BJ701

BJ7B1

GENERAL DESCRIPTION

OPERATION

THEORY OF OPERATION

DISCRETE COMPONENT CIRCUITS

HARDWARE REFERENCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A (4-1-81)	Manual released.
B (11-17-82)	Manual updated with technical and editorial changes.
C (07-12-83)	Manual updated with technical and editorial changes.

REVISION LETTERS I, O, Q AND X ARE NOT USED.

Address comments concerning this manual to:

Control Data Corporation
Small Disk Division
Customer Documentation Dept.
7725 Washington Avenue So.
Edina, Mn 55435

or use Comment Sheet in the back of this manual.

LIST OF EFFECTIVE PAGES

Sheet 1 of 3

New features, as well as changes, deletions, and additions to information in this manual are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV	PAGE	REV
Cover	-	1-11	A
Blank	-	1-12	A
Title P	-	1-13	A
ii	C	Blank	-
iii	B	S-2 Div	-
iv	B	Blank	-
v	A	2-1	A
Blank	-	2-2	A
vii	B	2-3	A
viii	B	2-4	A
ix	C	2-5	C
x	C	2-6	C
xi	A	2-7	C
xii	A	2-8	C
xiii	B	S-3 Div	-
xiv	A	Blank	-
xv	A	3-1	A
Blank	-	3-2	A
xvii	A	3-3	A
xviii	A	3-4	B
xix	A	3-5	A
Blank	-	3-6	A
S-1 Div	-	3-7	A
Blank	-	3-8	A
1-1	A	3-9	A
1-2	A	3-10	A
1-3	A	3-11	A
1-4	A	3-12	A
1-5	A	3-13	A
1-6	A	3-14	A
1-7	A	3-15	A
1-8	A	3-16	A
1-9	A	3-17	A
1-10	A	3-18	A

LIST OF EFFECTIVE PAGES (Contd)

Sheet 2 of 3

PAGE	REV	PAGE	REV
3-19	A	3-60	A
3-20	A	3-61	A
3-21	A	3-62	A
3-22	A	3-63	A
3-23	A	3-64	A
3-24	A	3-65	A
3-25	B	3-66	A
3-26	A	3-67	A
3-27	B	3-68	A
3-28	A	3-69	A
3-29	A	3-70	A
3-30	A	3-71	A
3-31	A	3-72	A
3-32	A	3-73	A
3-33	B	3-74	A
3-34	A	3-75	A
3-35	A	3-76	A
3-36	A	3-77	A
3-37	A	3-78	A
3-38	A	3-79	A
3-39	A	3-80	A
3-40	A	3-81	A
3-41	A	3-82	A
3-42	A	3-83	A
3-43	A	3-84	A
3-44	A	3-85	A
3-45	A	3-86	A
3-46	A	3-87	A
3-47	A	3-88	A
3-48	A	3-89	A
3-49	A	3-90	A
3-50	A	3-91	A
3-51	A	3-92	A
3-52	A	3-93	A
3-53	A	3-94	A
3-54	A	3-95	A
3-55	A	3-96	A
3-56	A	3-97	A
3-57	A	3-98	A
3-58	A	3-99	A
3-59	A	3-100	A

LIST OF EFFECTIVE PAGES (Contd)

Sheet 3 of 3

PAGE	REV	PAGE	REV
3-101	A	4-6	A
3-102	A	4-7	A
3-103	A	4-8	A
3-104	A	4-9	A
3-105	A	4-10	A
3-106	A	4-11	A
3-107	A	4-12	A
3-108	A	4-13	A
3-109	A	4-14	A
3-110	A	4-15	A
3-111	A	4-16	A
3-112	A	4-17	A
3-113	A	4-18	A
3-114	A	4-19	A
3-115	A	4-20	A
3-116	A	4-21	A
3-117	A	4-22	A
3-118	A	4-23	A
3-119	A	4-24	A
3-120	A	4-25	A
3-121	A	4-26	A
3-122	A	4-27	A
3-123	A	4-28	A
Blank	-	4-29	A
S-4 Div	-	4-30	A
Blank	-	4-31	A
4-1	A	4-32	A
4-2	A	Cmt Sht	-
4-3	A	Rtn Env	-
4-4	A	Blank	-
4-5	A	Cover	-

PREFACE

This manual contains reference information applicable to the BJ501 and BJ701 storage module drives (SMD's).

The manual has been prepared for customer engineers and other technical personnel directly involved with maintaining the storage module drive (SMD).

Reference information is provided in four sections in this manual. Section numbers and a brief description of their contents are listed below.

Section 1 - General Description. Describes equipment functions, specifications, and equipment number identification.

Section 2 - Operation. Describes and illustrates the location and use of all controls and indicators, power on sequencing, and disk pack installation and removal.

Section 3 - Theory of Operation. Describes basic logic and mechanical functions.

Section 4 - Description of discrete component circuits and their functions. For ease of using the logic diagrams, transistors and their associated components are frequently condensed into an equivalent logic symbol. This section, arranged in alphabetical order of the circuit type designator (AAA-ZZZ) explains these functions and illustrates the actual discrete elements.

The following manuals apply to the BJ501 and BJ701 SMD/s and are available from Control Data Literature Distribution Services, 308 North Dale Street, St. Paul, MN 55103:

Publication No.	Title
83311300	BJ701 Maintenance
83311100	BJ501 Maintenance
83324220	BJ501/BJ5D7, BJ701/BJ7B1 Reference

Publication No.	Title
83322440	CDC Microcircuits, Vol. 1 (Functional Description of Integrated Circuits)
83324440	CDC Microcircuits, Vol. 2 (Functional Description of Integrated Circuits)
83323770	A Guide for the Disk Drive Operator.

WARNING

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. All 60 Hz units S/C 48 and below, and all 50 Hz units have not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of the FCC Rules which are designed to provide reasonable protection against such interference when operated in a commercial environment. All 60 Hz units S/C 49 and above have been tested and found to comply with the above regulations. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

CONTENTS

FIGURES

TABLES

ABBREVIATIONS

AC	Alternating Current
ADRS	Address
AGC	Automatic Gain Control
AM	Address Mark
AMP	Amplifier, Ampere
BCD	Binary Coded Decimal
C	Celsius
CAR	Cylinder Address Register
CDC	Control Data Corporation
CKT	Circuit
CLR	Clear
CM	Centimeter
COMP	Compensation
CONTd	Continued
CYL	Cylinder
D	Duty
D/A	Digital to Analog
DB	Decibels
DC	Direct Current
DIFF	Difference
DLYD	Delayed
DTL	Diode Transister Logic
ECL	Emitter Coupled Logic
ECO	Engineering Change Order
EMER	Emergency
EMF	Electromotive Force
EOT	End of Travel
F	Fahrenheit
FCO	Field Change Order
FET	Field Effect Transister
FF	Flip Flop
FLT	Fault
FREQ	Frequency
FT	Foot
FWD	Forward
GEN	Generator
GND	Ground
HEX	Hexadecimal
HYST	Hysteresis
I/O	Input-Output

ABBREVIATIONS (Contd)

INTLK	Interlock
IPS	Inches per Second
KHz	Kilo Hertz
KM	Kilometer
LD	Load
LOC	Location
M	Meter
MA	Milliamp
MAG	Magnitude
MAX	Maximum
MB	Mega Byte
MFM	Modified Frequency Modulation
MHz	Megahertz
MM	Millimeter
MS	Millisecond
MUX	Multiplex
MV	Millivolt
NEG	Negative
NOM	Nominal
NORM	Normal
NRZ	Non Return To Zero
OP	Operation
PLL	Phase Lock Loop
PLO	Phase Lock Oscillator
PNL	Panel
POS	Positive
PWR	Power
R	Resister
RC	Resistance-capacitance
RCVR	Receiver
RD	Read
RDY	Ready
REF	Reference
REG	Register
REV	Reverse
RLY	Relay
RPM	Revolutions Per Minute
RPS	Rotational Position Sensing
RTZ	Return to Zero
SEC	Seconds
SEL	Select
SMD	Storage Module Drive
SW	Switch
t	Time
TTL	Transistor Transistor Logic

ABBREVIATIONS (Contd)

V	Volt
VCC	Collector Supply Voltage (DC)
VCO	Voltage Controlled Oscillator
VDC	Volts Direct Current
W.R.	Write, Read
XDUCER	Transducer

SECTION 1

GENERAL DESCRIPTION

GENERAL DESCRIPTION 1

INTRODUCTION

The BJ501/5D7 and BJ701/7B1 Storage Module Drives (SMDs) are high speed, random access digital data storage devices that connect to a central processor through a controller. The major difference between the drives is their storage capacity. The total data storage capacity of the BJ501/5D7 drives is 40 megabytes, and BJ701/7B1 drives is 80 megabytes. The only exceptions are the BJ7B1G and H which unlike other BJ7B1s, are 40 MB units. All the equipment specifications for each drive are listed in table 1-1.

The remainder of this section provides a general description of the drives and is divided into the following areas:

- Data Storage Medium - Describes the disk pack which is the medium used to store the data.
- Drive Functional Description - Explains the basic function of the drive.
- Drive Physical Description - Provides a basic description of the drives physical characteristics.
- Equipment Configuration - Describes the various drive configurations and how to identify them.

TABLE 1-1. DRIVE SPECIFICATIONS

Specification	Value
PHYSICAL SPECIFICATIONS	
Refer to maintenance manual.	
ENVIRONMENT	
Temperature	
Operating	15.5°C (60°F) to 32°C (90°F)
Gradient	6.6°C (12°F) per hour
Transit (packed)	-34°C (-30°F) to +66°C (+150°F)
Relative Humidity (no condensation)	
Operating	20% to 80%
Transit (packed)	5% to 95%
Altitude	
Operating	-305 m (-1000 ft) to 3050 m (+10,000 ft)
Transit (packed)	-305 m (-1000 ft) to 4600 m (+15,000 ft)
POWER SPECIFICATIONS	
Refer to maintenance manual.	

Table Continued on Next Page

TABLE 1-1. DRIVE SPECIFICATIONS (Contd)

Specification	Value
DATA RECORDING SPECIFICATIONS	
Disk Pack	
Packs/Drive	1
Recording Surfaces/ Disk Pack	5
Usable Tracks/ Recording Surface	40 MB - 412, 80 MB - 823
Tracks/Cylinder	5
Tracks/Inch	BJ501/507 - 205, BJ701/7B1 - 384
Track Spacing	0.066 mm (0.0052 in) nominal
Rotational Speed	3600 r/min
Disk Pack	BJ501/507 - CDC 9876 or equivalent BJ701/7B1 - CDC 9877 or equivalent
Disk Surface Diameter (nominal)	356 mm (14 in)
Disks/Disk Pack	5 (top and bottom disks are for protection only)
Coating	Magnetic oxide
Seek Timing	
Access Mechanism	Voice coil driven by servo loop
822 Track Seek	55 ms (maximum)
1-Track Seek	BJ501/507 - 7ms (maximum), BJ701/7B1 - 6ms (maximum)
Average Seek	30 ms

Table Continued on Next Page

TABLE 1-1. DRIVE SPECIFICATIONS (Contd)

Specification	Value
Latency Time	
Average	8.33 ms (at 3600 r/min)
Maximum	17.2 ms (at 3492 r/min)
Recording	
Mode	Modified Frequency Modulation (MFM)
Bit Density (nominal)	
outer track	1590 bits per cm (4038 bits per in)
inner track	2377 bits per cm (6038 bits per in)
Rate	9.677 MHz (nominal), 1 209 600 characters/second
Heads	
Recording	5
Servo (positioning)	1
Read/Write Width	0.051 mm (0.002 in) nominal
Data Capacity	
Nominal	BJ501/507 - 40 MB, *BJ701/7B1 - 80 MB
Bits/Track	161 281 (unsectored)
Bits/Cylinder	806 400 (unsectored)
Bits/Pack	40 MB 325 785 600 (unsectored) 80 MB 651 571 200 (unsectored)
Bits/Byte	8
Bytes/Track	20 160
Tracks/Cylinder	5

Table Continued on Next Page

TABLE 1-1. DRIVE SPECIFICATIONS (Contd)

Specification	Value
Controllers per Drive	1
Drives per Controller	16 (maximum)
Interface Cables	
Maximum Total System Length	30 m (100 ft)
Type	Control: Twisted pair Signal: Twinax
Connectors	3 per drive
Pin Assignments	Refer to Maintenance Manual
Signal Functions	Refer to Section 3 of this manual

* Exceptions are the BJ7B1 G and H which have data capacities of 40 MB.

DATA STORAGE MEDIUM

The data storage medium for the drive is a disk pack, consisting of five 14 - inch disks, center mounted on a hub (see figure 1-1). The disk pack is portable and interchangeable between equivalent drives. The packs are not interchangeable, however, between the 40 and 80 megabyte drives.

The disk pack has a total of six usable surfaces, each coated with a layer of magnetic oxide and related binders and adhesives. One of these surfaces, referred to as the servo surface, contains information prerecorded at the factory. This surface is used by the drive to generate position information and various timing signals. The remaining five surfaces can be used by the system for data storage and are referred to as data surfaces.

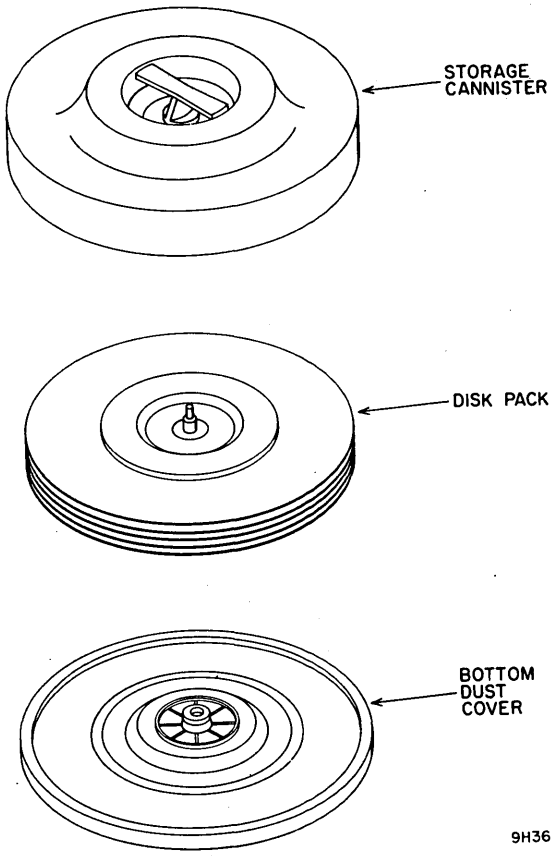


Figure 1-1. Disk Pack

DRIVE FUNCTIONAL DESCRIPTION

The drive contains all the circuits and mechanical devices necessary to record data on and recover it from the disk pack (see figure 1-2). The necessary power for this is provided by the drives power supply, which receives its input power from the site main power source.

All functions performed by the drive are done under direction of the controller. The controller communicates with the drive via the interface which consists of a number of I/O lines carrying the necessary signals to and from the drive.

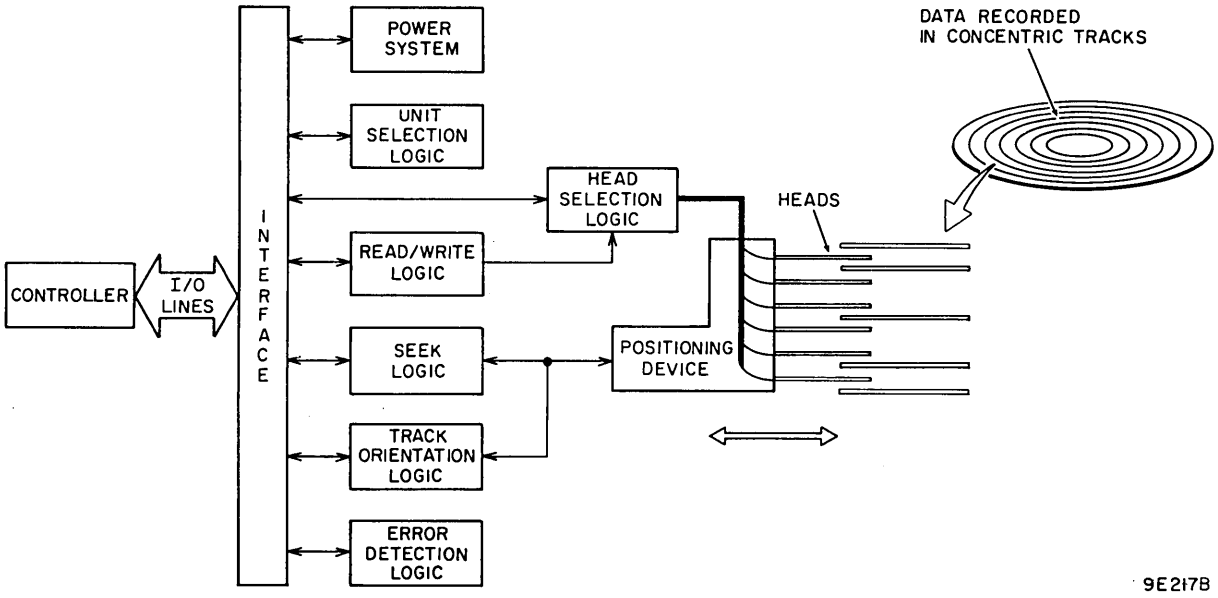


Figure 1-2. Drive Functional Blocks

Some interface lines, including those that carry commands to the drive, are not enabled unless the drive is selected by the controller. Unit selection allows the controller, which can be connected to more than one drive, to initiate and direct an operation on a specific unit.

All operations performed by the drive are related to data storage and recovery (normally referred to as writing and reading). The actual reading and writing is performed by electromagnetic devices called heads that are positioned over the recording surfaces of the rotating disk pack. There is a separate head for each surface in the pack and the heads are positioned in such a way that data is written in concentric tracks around the disk surfaces (see figure 1-2).

Before any read or write operation can be performed the controller must instruct the drive to position the heads over the desired track (called seeking) and also to use the head located over the surface (head selection) where the operation is to be performed.

After selecting a head and arriving at the data track, the controller still must locate that portion of the track on which the data is to be written or read. This is called track orientation and is done by using the Index and Sector signals generated by the drive. The Index signal indicates the logical beginning of each track and the Sector signals are used by the controller to determine the position of the head on the track with respect to index.

When the desired location is reached the controller commands the drive to actually read or write the data. During a read operation the drive recovers data from the pack, and transmits it to the controller. During a write operation, the drive receives data from the controller, processes it and writes it on the disk pack.

The drive is also capable of recognizing certain errors that may occur during its operation. When an error is detected, it is indicated either by a signal to the controller or by a maintenance indicator on the drive itself.

DRIVE PHYSICAL DESCRIPTION

GENERAL

The basic configuration includes one SMD mounted on the top of the cabinet. An additional SMD or controller can be drawer mounted in the lower part of the cabinet. The drawer mounted unit slides out for convenient access (refer to figure 1-3).

Figure 1-3 shows the SMD cabinet with and without a drawer mounted SMD (refer to controller manual for details concerning the drawer mounted controller).

Figure 1-4 illustrates the basic storage module drive removed form the cabinet. The following paragraphs give brief descriptions of the major assemblies. Detailed information on the construction and functions of the assemblies is provided in Section 3 of this manual.

TOP COVER ASSEMBLY

The top cover assembly protects the other drive assemblies during operation. The drive cover for pack loading is opened by means of a latch under the cover. An electrical switch senses that the cover is opened, disables the spindle motor power, and commands retract if the heads are loaded.

SPINDLE ASSEMBLY

The spindle assembly mounts and rotates the disk pack. Its associated drive motor runs continuously whenever a pack is installed, the pack cover is closed, and the START switch is on.

ACTUATOR ASSEMBLY

The actuator assembly mounts the read/write heads for processing data. The actuator contains a voice coil positioner controlled by a closed-loop, continuous-feedback servo system.

SHROUD

The shroud surrounds the disk pack. The shroud protects the pack, aids in directing air from the blower to the pack, and prevents the operator from damaging the read/write heads with the pack.

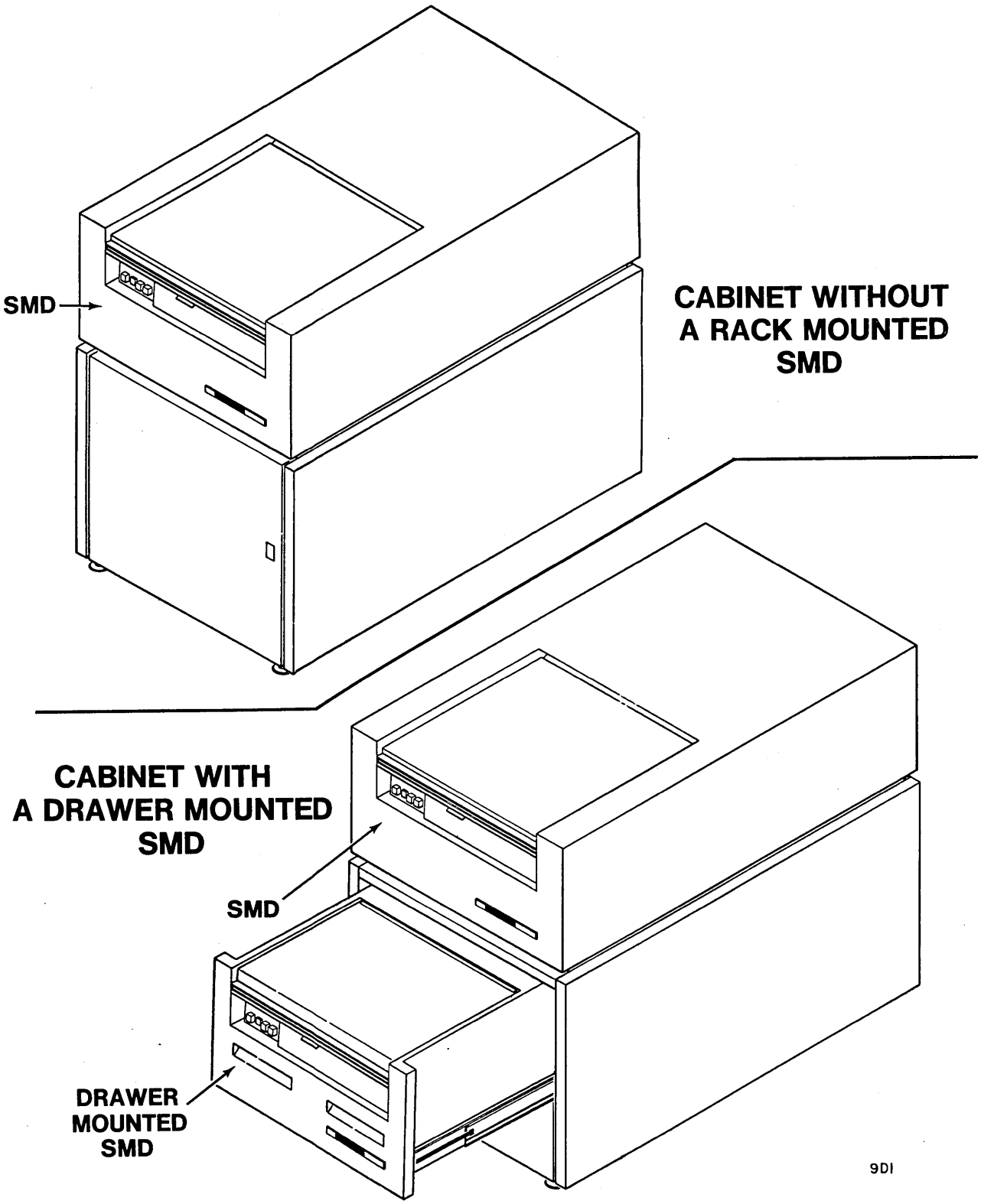


Figure 1-3. SMD Cabinet

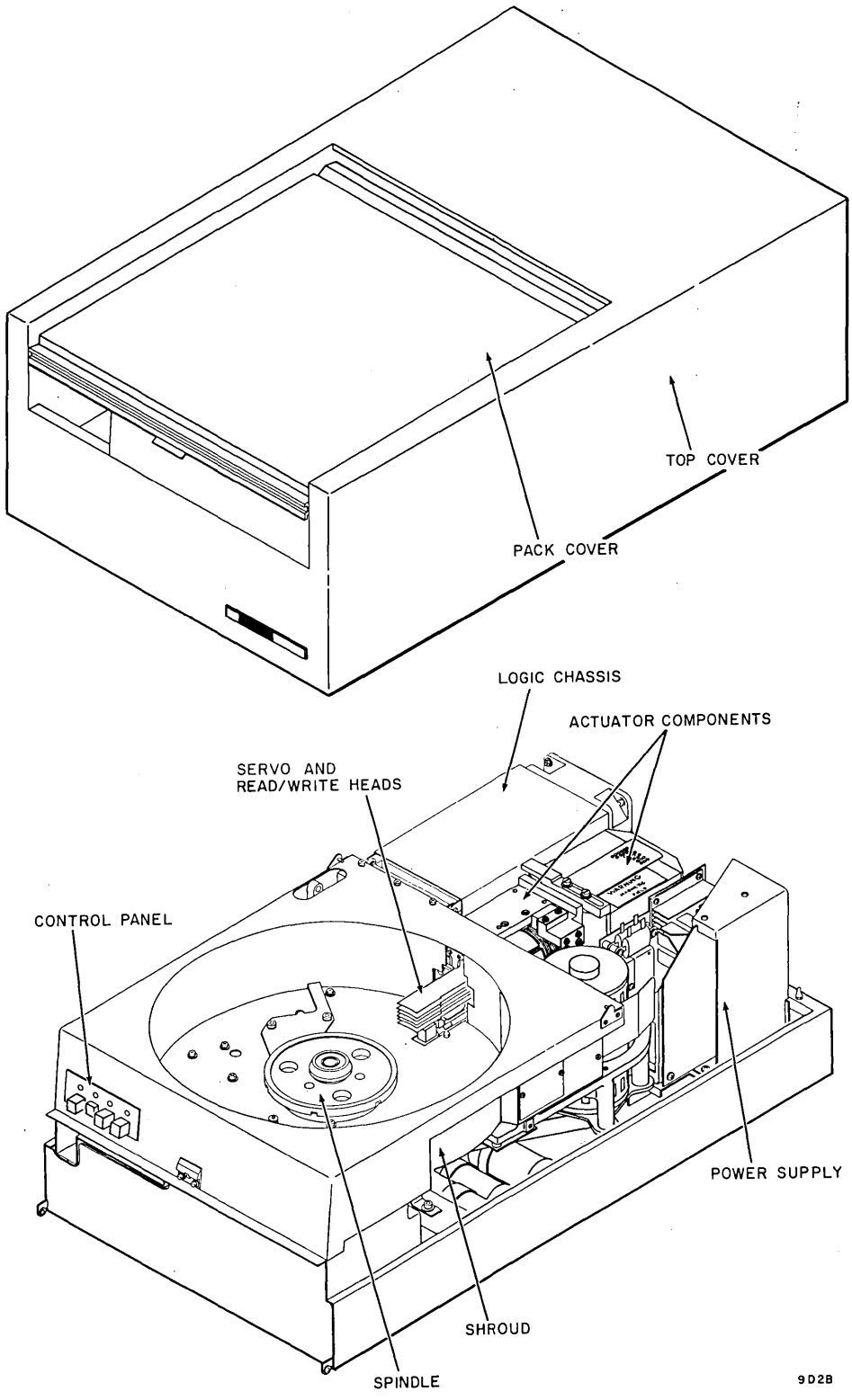


Figure 1-4. Assembly Locations

LOGIC CHASSIS

The logic chassis serves as the mounting point for the main complement of the logic cards. The chassis is mounted on the deck assembly. The backpanel terminals provide ready access to all signals entering and leaving each card. In addition, the cards have test points for monitoring critical signals within the cards.

POWER SUPPLY

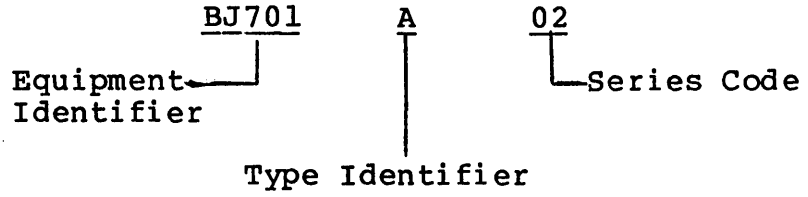
The power supply distributes the dc power required by the drive. Incoming power is filtered by a line filter and applied to main ac power circuit breaker and a secondary ac power circuit breaker for the power supply.

EQUIPMENT CONFIGURATION

An equipment number is assigned to each drive to identify its configuration. This provides a systematic method of identifying, accounting, and controlling changes that affect drive logic and mechanical components.

The equipment configuration is identified by a nameplate attached to the frame at the back of the drive.

The equipment Identification Number will be similar to the following:



The Equipment Identifier indicates the basic function of the unit. Refer to the equipment configuration listing in the preface.

The Type Identifier indicates a non-interchangeable difference in equipments that affects the interface. The term "Mod" is sometimes used interchangeably with "Type Identifier".

The Series Code changes with each non-interchangeable change within the equipment. Drives with different series codes are fully interchangeable at the system level; however, not all of their electrical or mechanical components may be interchangeable. Series codes are changed by Engineering Change Order (ECO) only at the factory.

Other changes are accomplished by Field Change Order (FCO). These changes may be installed either at the factory or by field personnel. FCO changes are indicated by an entry on the FCO Log that accompanies each machine. It is important that this log be kept current by the person installing each FCO.

Manuals accompanying unit shipments from the manufacturer match the configuration of those units. Subsequent manual changes are controlled by the Revision Record sheet behind the title page of every manual. This sheet identifies the Series Code and FCO effectivity of manual changes. If maintenance will be perfomred using a manual other than the manual supplied with each drive, verify that the manual and drive configurations match.

SECTION 2

OPERATION

OPERATION 2

INTRODUCTION

This section provides instructions and related information for operating the drive.

CONTROLS AND INDICATORS

The drive has a control panel located on the front of the machine, and power switches and a running time meter located at the rear. Figure 2-1 illustrates the controls and indicators, and Table 2-1 provides functional descriptions.

OPERATING INSTRUCTIONS

POWER APPLICATION

1. Set AC POWER circuit breaker to ON. Leave AC breaker on at all times, especially if the pack is stored in the drive to maintain cleanliness of shroud and pack.

2. Set POWER SUPPLY circuit breaker to ON.

3. Install a disk pack (refer to Disk Pack Installation procedure).

4. Press operator panel START switch.

5. Spindle motor energizes. Head loading sequence begins when spindle is up to speed.

CAUTION

If abnormal heads load is observed, correct problem and inspect pack and heads before using drive.

6. Head loading sequence is complete when heads are positioned to track 0. Drive is now ready to receive a Read, Write, or Seek command from the control unit. READY indicator is on.

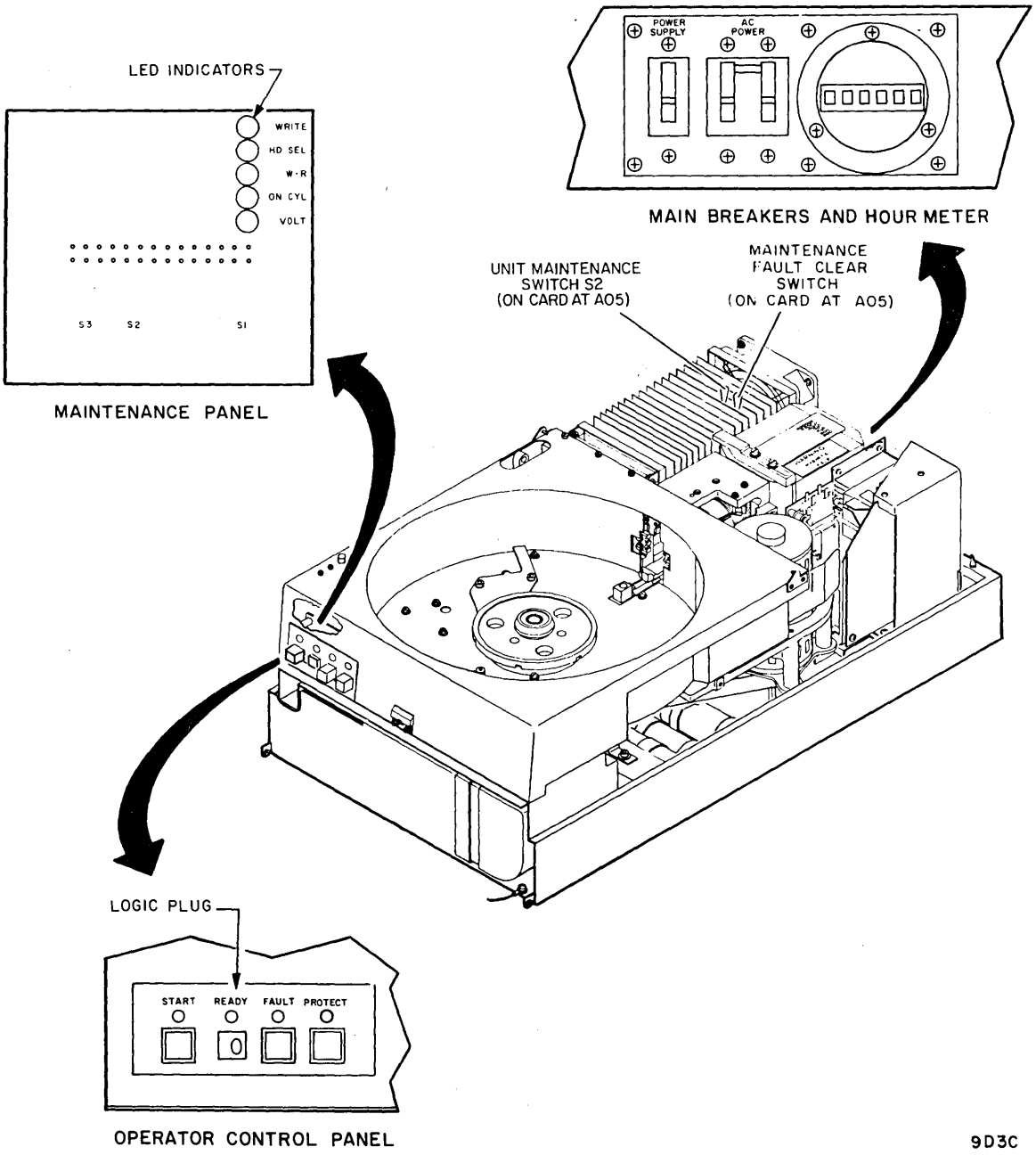


Figure 2-1. Controls and Indicators

TABLE 2-1. CONTROLS AND INDICATORS

Control or Indicator	Function
OPERATOR PANEL	
START switch	Energizes (when pressed to light) spindle drive motor and begins First Seek sequence provided the following conditions are met: 1. Disk Pack is in place and canister removed. 2. Pack cover is closed. 3. Circuit breakers are on. Causes a power off sequence (when pressed to extinguish start indicator).
START indicator	Lights when switch is on.
LOGIC PLUG	Completes circuitry to permit selection of the unit through a binary code. CAUTION Unit select logic plug should not be changed or removed unless unit is shut off with heads unloaded.
READY indicator	Lights when the unit is up to speed, the heads are loaded, and no fault condition exists.
FAULT switch	Clears the fault circuitry and extinguishes the FAULT indicator. (Does not clear Maintenance Fault register.)

Table Continued on Next Page

TABLE 2-1. CONTROLS AND INDICATORS (Contd)

Control or Indicator	Function
	OPERATOR PANEL
UNIT MAINTENANCE switch	Prevents drive from activating Unit Select signal, thus preventing drive from being selected. This switch should not be used during normal on line operation.
FAULT indicator	Lights in response to one or more of the following conditions: 1. Read and write are selected at the same time. 2. No ac write current when Write Gate is present. 3. More than one head is selected. 4. Read or Write is selected while off cylinder. 5. Low voltage condition sensed for ±5 V, ±20 V, ±42 V. 6. Loss of dibit signal for 350 ms with heads loaded.
PROTECT switch	Enables or disables write driver.
PROTECT switch	When lighted, indicates that the drive is write protected.
	REAR PANEL
AC POWER circuit breaker	Controls application of ac power.
POWER SUPPLY circuit breaker	Controls application of dc power to the logic chassis.
Elapsed Time Meter	Active when ac power and dc power are applied by circuit breakers. Records accumulated ac power-on time.

Table Continued on Next Page

TABLE 2-1. CONTROLS AND INDICATORS (Contd)

Control or Indicator	Function
MAINTENANCE PANEL (BACK OF OP PNL)	
WRITE FAULT indicator	Write was attempted and no ac write current and/or dc current was sensed.
HEAD SELECT FAULT indicator	More than one head selected.
W.R. FAULT indicator	Read and write were selected at the same time.
ON CYLINDER FAULT indicator	Read or write was selected while off cylinder.
VOLTAGE FAULT indicator	Low voltage condition existed for ±5 V, ±20 V, ±42 V.

DISK PACK SPECIAL PRECAUTIONS

The following describes precautions that must be observed when handling, storing, and using the disk pack. Failure to observe these precautions can result in damage to the pack and loss of data. If any doubt exists about the packs functional condition, return the pack to the vendor enclosing a description of the known or suspected problem.

Problem Detection

Should improper disk pack operation be indicated by any of the following conditions, immediately power down the drive and remove the pack.

CAUTION

If any media problems are suspected, do not use the media on another drive until full assurance is made that no damage or contamination has ocurred to the media.

Also, do not use the drive with another media until full assurance is made that no damage or contamination has ocurred to the drive heads or to the shroud area.

1. A sudden increase in error rates related to one or more heads.

2. An unusual noise such as pinging or scratching.

3. A burning oder.

4. Contamination of the pack from dust, smoke, oil or the like is suspected.

Handling Precautions

Observe the following precautions when using and handling the disk pack.

1. Do not mark on disk packs. Residue may be released that could cause airborne contamination.

2. Do not attach any label to the disk pack itself. Labels will not remain attached when the pack is spinning and catastrophic head crashes may result. All labels should be placed on the pack canister if required.

3. Use extreme care not to drop the pack or strike it against another object (even if the pack is in the canister).

4. Never remove the pack from its protective canister except in a computer room environment free of dust, smoke, and other contaminants.

5. Never attempt to clean the disk pack. Cleaning can be done only by the vendor. Attempts to clean the pack can result in serious change to the pack and/or drive and is done at the risk of the user.

Storage Precautions

Observe the following precautions when storing disk packes.

1. Store disk packs in machine-room atmosphere (60°F to 90°F, 10% to 80% relative humidity).

2. If disk pack must be stored in different environment, allow two hours for adjustment to computer environment before use.

3. Never store disk pack in direct sunlight or in dirty environment.

4. Store disk packs flat, not on edge. They may be stacked with similar packs when stored.

5. Always be sure that both top and bottom plastic canister covers are on disk pack and locked together whenever it is not actually installed in a drive.

DISK PACK INSTALLATION

Make certain that the disk drive on which the disk pack is to be installed has been maintained according to the Preventive Maintenance section.

1. Raise pack access cover. (AC POWER circuit breaker must be ON.)

2. Lift disk pack by plastic canister handle.

3. Disengage bottom dust cover from disk pack by turning canister handle counterclockwise. Set cover aside in an uncontaminated area.

CAUTION

Avoid abusive contact between the disk pack and the spindle. The read/write heads are sometimes manually positioned during maintenance procedures. Make certain that the heads are fully retracted.

4. Place disk pack onto spindle.

NOTE

A spindle lock mechanism is actuated when the disk pack canister cover is on the spindle. The mechanism holds the spindle stationary while loading or unloading a disk pack.

5. Twist canister handle clockwise to lock disk pack in place.

NOTE

A clink may be heard as the spindle lock mechanism engages.

6. Lift canister clear of disk pack, place bottom dust cover on canister, and set aside in an uncontaminated area.

7. Close pack access cover immediately to prevent entry of dust and contamination of disk surfaces.

DISK PACK REMOVAL

WARNING

Do not open pack access cover while disks are spinning or attempt to slow disks by hand.

1. Press operator panel START switch to extinguish the START indicator.

2. Check that disk pack rotation has stopped. (Stopping time is approximately 1.5 minutes without brake and 20 seconds with brake.)

3. Raise front cover.

CAUTION

The read/write heads are sometimes manually positioned during maintenance procedures. Make certain that the heads are fully retracted.

4. Place plastic canister over mounted disk pack so that post protruding from center of disk pack is received into canister handle.

5. Twist canister handle counterclockwise until disk pack is free of spindle.

CAUTION

Avoid abusive contact between the disk pack and the spindle assembly.

6. Lift canister and disk pack clear of spindle.

7. Close front cover.

8. Place bottom dust cover in position on disk pack and lock it.

SECTION 3

THEORY OF OPERATION

INTRODUCTION

The theory of operation section describes drive functions and the hardware used in performing them. It is divided into the following major areas (refer to figure 3-1):

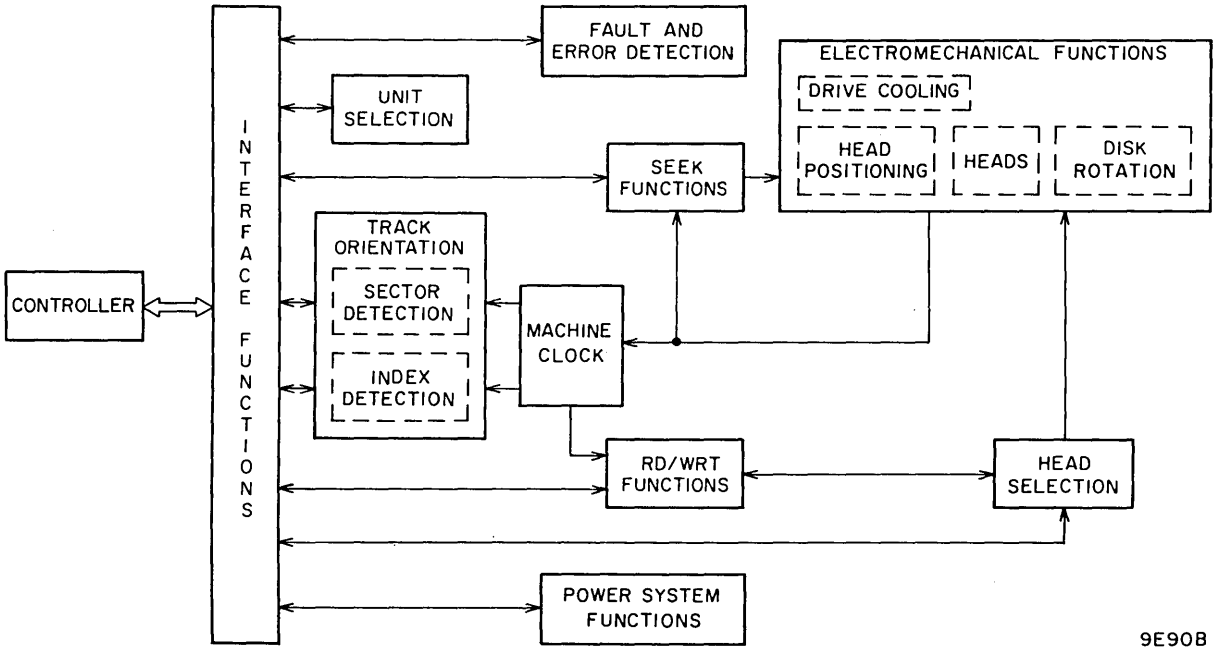


Figure 3-1. Drive Functional Block Diagram

- Power System Functions - Describes how the drive provides the voltages necessary for drive operation.

- Electromechanical Functions - Provides a physical and functional description of the mechanical and electromechanical systems (disk pack rotation, head positioning, and air flow).

- Interface Functions - Describes the signal lines connecting the drive and controller. It also describes the I/O signals carried by these lines and how they are processed by the drive logic.

- Unit Selection - Explains how the controller logically selects the drive so the drive will respond to controller commands.

- Seek Functions - Explains how the servo logic controls the movements of the head positioning mechanism in positioning the heads over the disk pack.

- Machine Clock Functions - Explains how this circuit uses signals derived from the disk pack to generate timing pulses for the index, sector and read/write circuits.

- Head Operation and Selection - Explains the head selection process.

- Track Orientation - Describes how the drive detects the index pattern which is used to indicate the logical beginning of each track and also explains how the drive derives the sector pulses, which are used to determine the angular position of the read/write heads with respect to Index.

- Read/Write Functions - Describes how the drive processes the data that it reads from and writes on the disk pack.

- Fault Detection - Describes the conditions that the drive interprets as faults.

The descriptions in this section are limited to drive operations only. In addition, they explain typcial operations and do not list variations or unusual conditions resulting from unique system hardware or software environments.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in the hardware maintenance manual should take precedence over those in this manual if there is a conflict between the two.

POWER SYSTEM FUNCTIONS

GENERAL

The major element in the drives power system is the power supply. The power supply receives its input from the site ac power source and uses it to produce the ac and dc voltages necessary for drive operation.

The drive motor is started and heads load function initiated during the power on sequence. The power off sequence unloads the heads and stops the drive motor. The drives LOCAL/REMOTE Switch permits these sequences to be initiated either at the drive (local) or the controller (remote).

The remainder of this discussion provides further description of the power system and is divided into the following areas:

- Power Distribution - Describes how the power is distributed to the drive circuitry.
- Power On Sequence - Describes how power is applied to the drive motor and the heads load sequence initiated.
- Power Off Sequence - Describes how the heads are unloaded and the drive motor stopped.
- Emergency Retract and Data Protection - Explains sequence performed when conditions exist requiring the heads be unloaded immediately.

POWER DISTRIBUTION

Power distribution consists of routing power to the various elements in the power supply and rest of the drive so that the power on sequence can be performed. The distribution is controlled by circuit breakers located on the control panel. These circuit breakers also provide overload protection. The power distribution circuits are shown on figure 3-2 and basic operation is explained in the following.

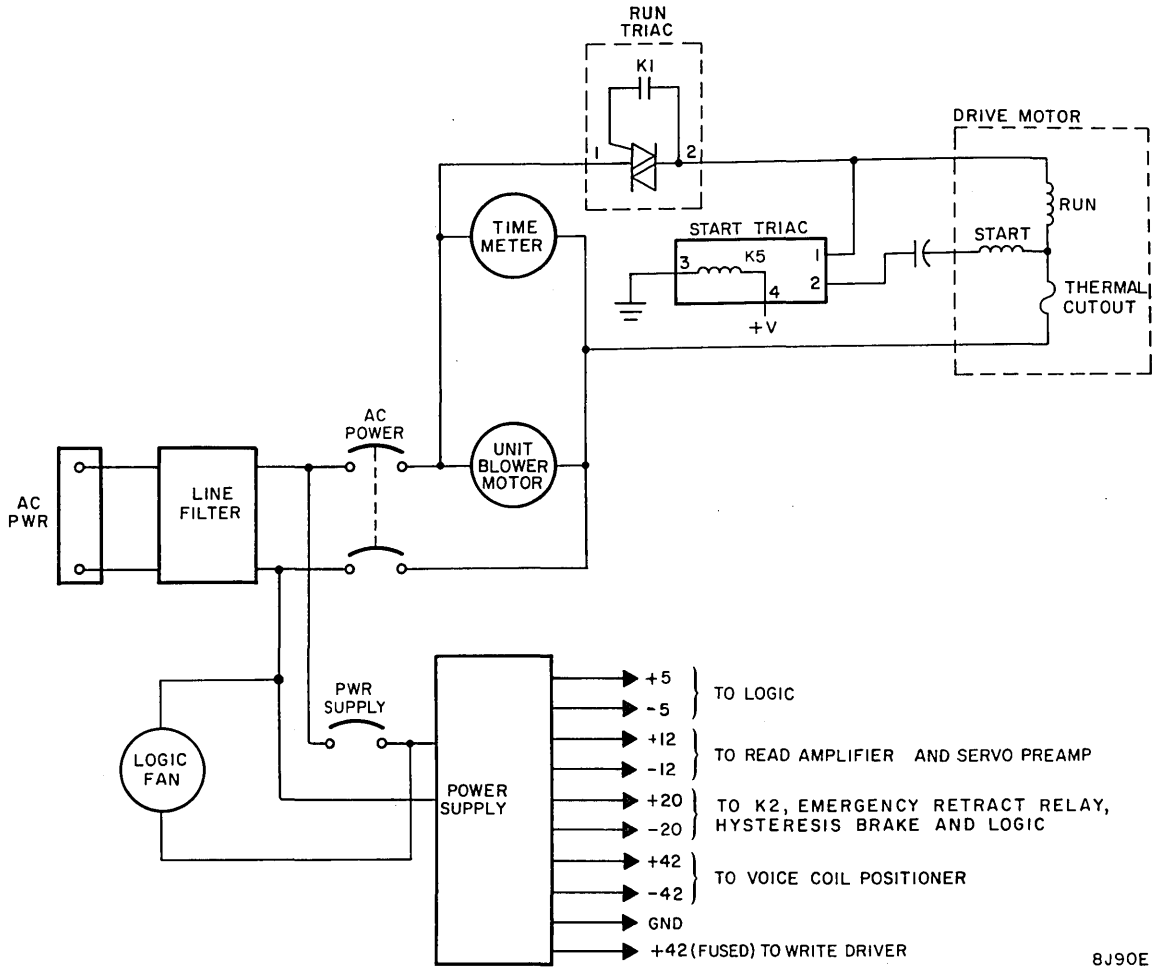


Figure 3-2. Power Distribution

Site main ac power is input to the power supply via the AC POWER circuit breaker. When this breaker is closed, it applies power to the HOUR meter and blower motor. It also provides the input to the drive motor control triacs; however, the motor does not start until the power on sequence.

Closing the POWER SUPPLY circuit breaker applies power to the logic fan and dc power supply. The dc power supply converts the ac input into the dc voltages necessary for drive operation.

Power On Sequence

The power on sequence starts the drive motor and initiates loading of the heads. Figure 3-3 shows the circuits involved in this sequence and figures 3-4, 3-5, and 3-6 are flow charts of the operation.

The power on sequence begins when the operator presses the START switch. If all circuit breakers and interlocks are closed, pressing this switch deenergizes the hysteresis brake and energizes the Start and Run triacs. This causes the drive motor to start. The drive belt transfers drive motor motion to the spindle, thereby, causing the disk pack to rotate.

When pack speed reaches about 2800 r/min, the Up To Speed signal goes active and energizes the emergency retract relay (K2). Energizing this relay connects the voice coil to the power amplifier. This puts the voice coil under control of the servo system, thus allowing the heads load sequence to begin whenever the 25 second heads load delay (triggered when the START switch is pressed) times out. Details of the heads load sequence are given in the First Seek discussion.

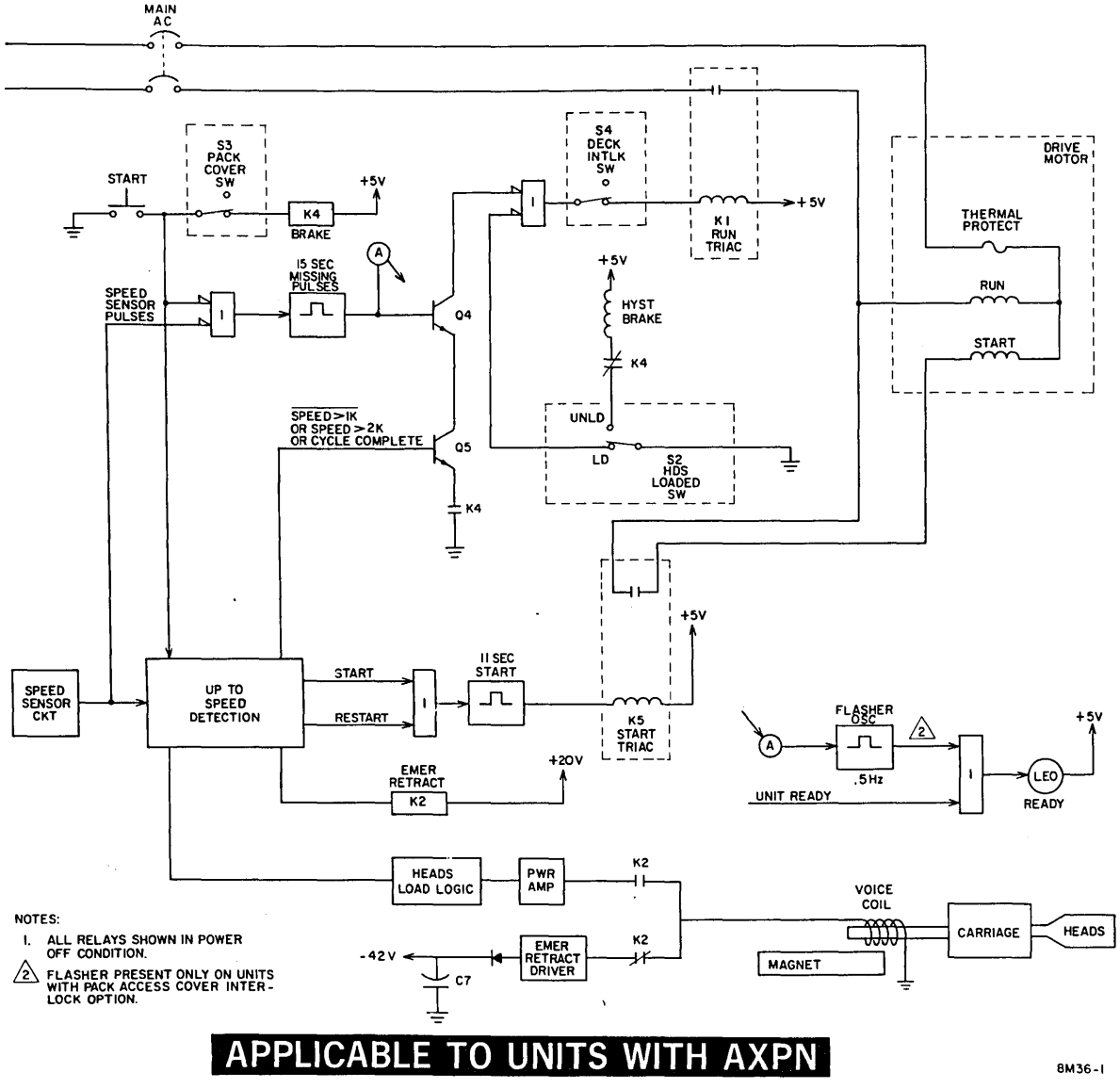


Figure 3-3. Power On Sequence Circuits (Sheet 1 of 3)

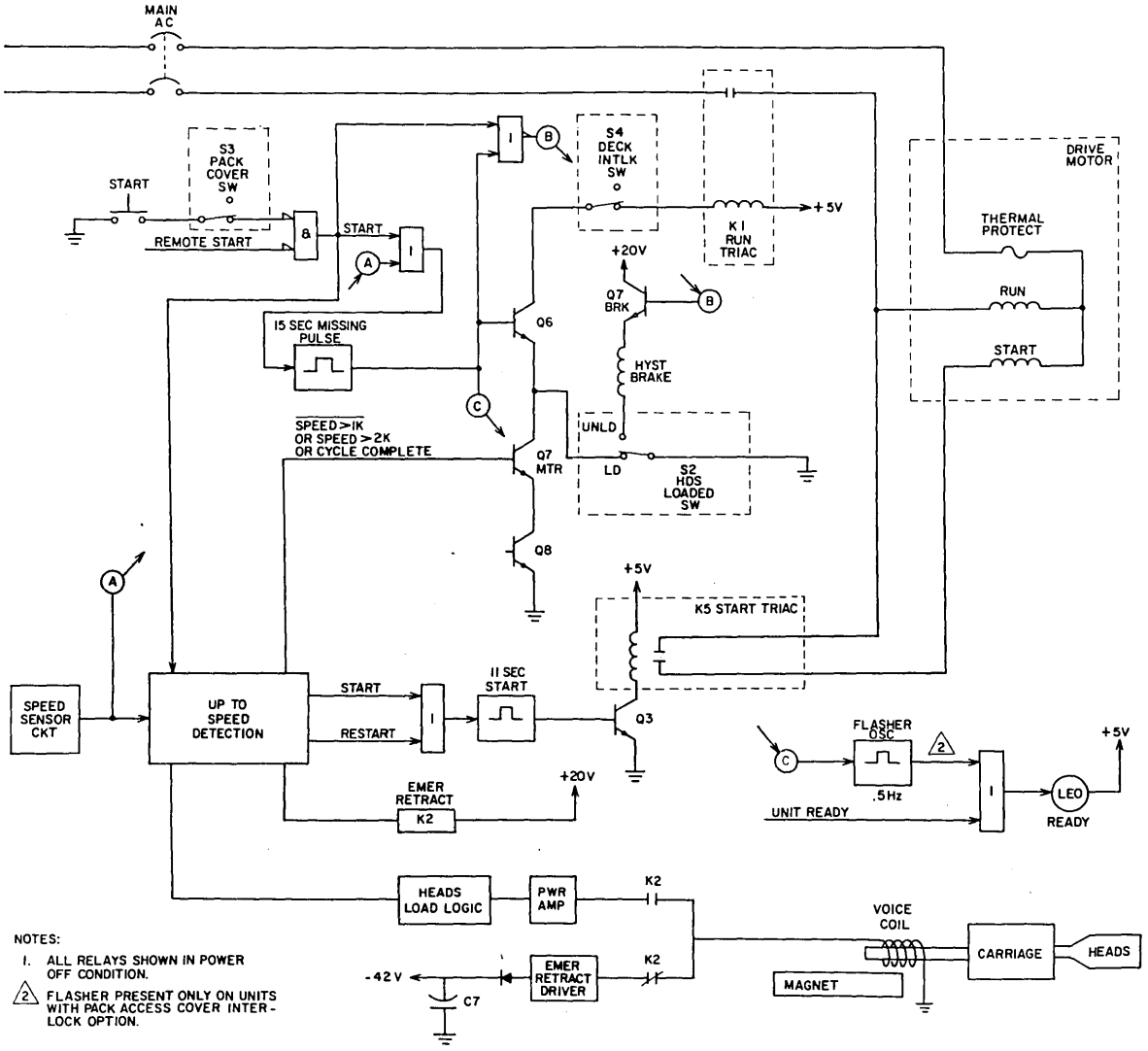


Figure 3-3. Power On Sequence Circuits (Sheet 2 of 3)

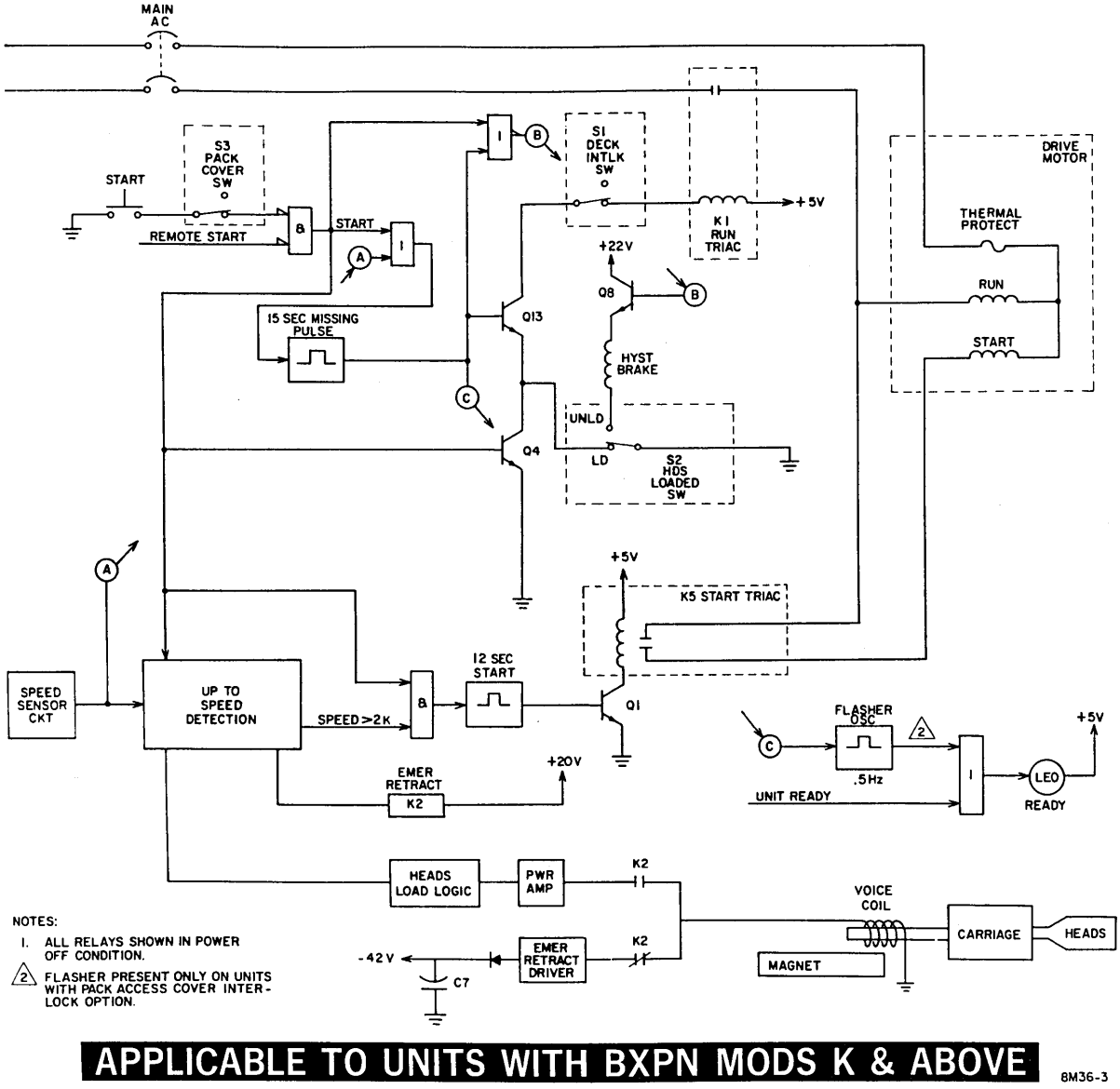


Figure 3-3. Power On Sequence Circuits (Sheet 3 of 3)

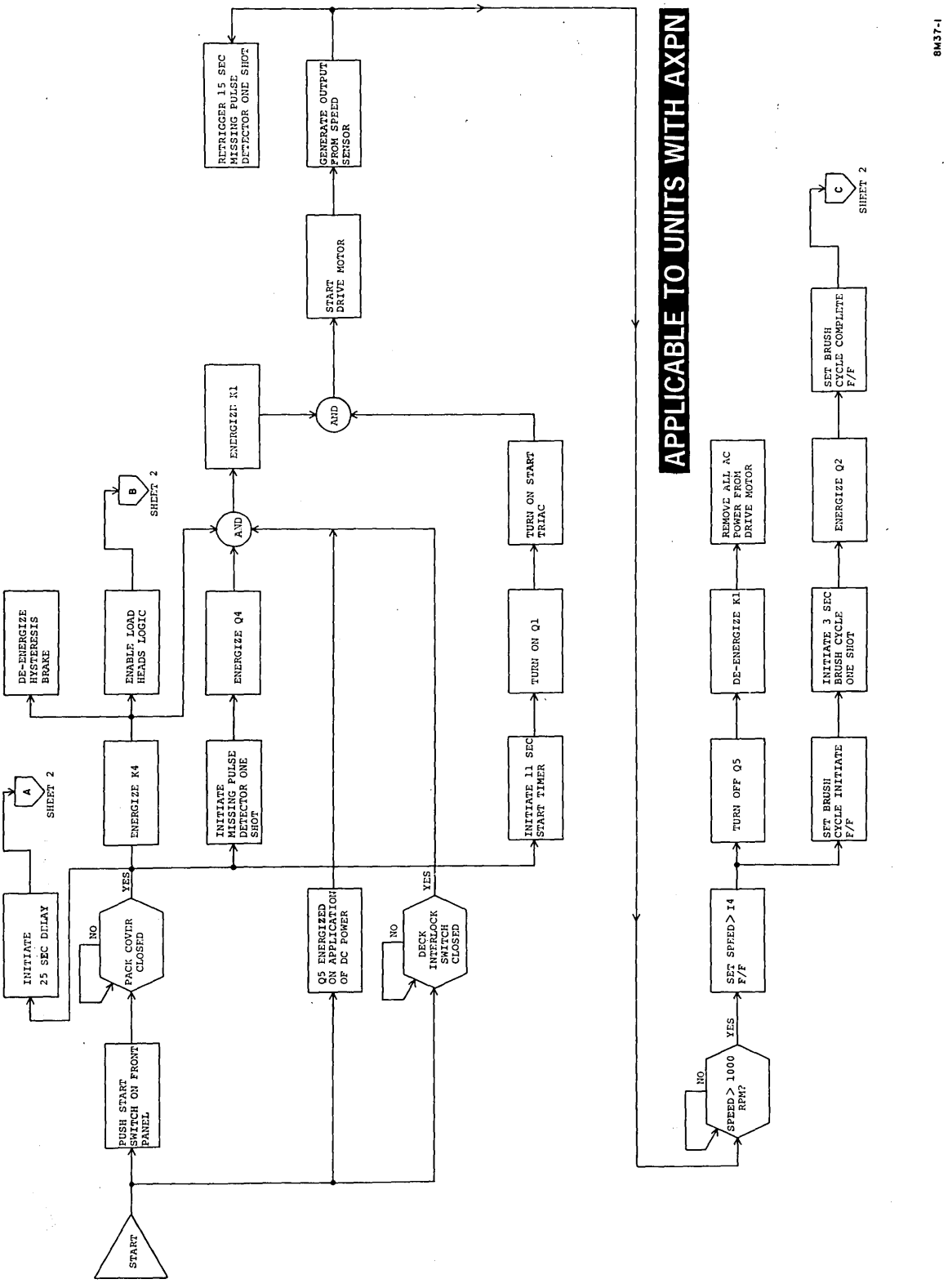


Figure 3-4. AXPN Power On Sequence Flow Chart (Sheet 1 of 2)

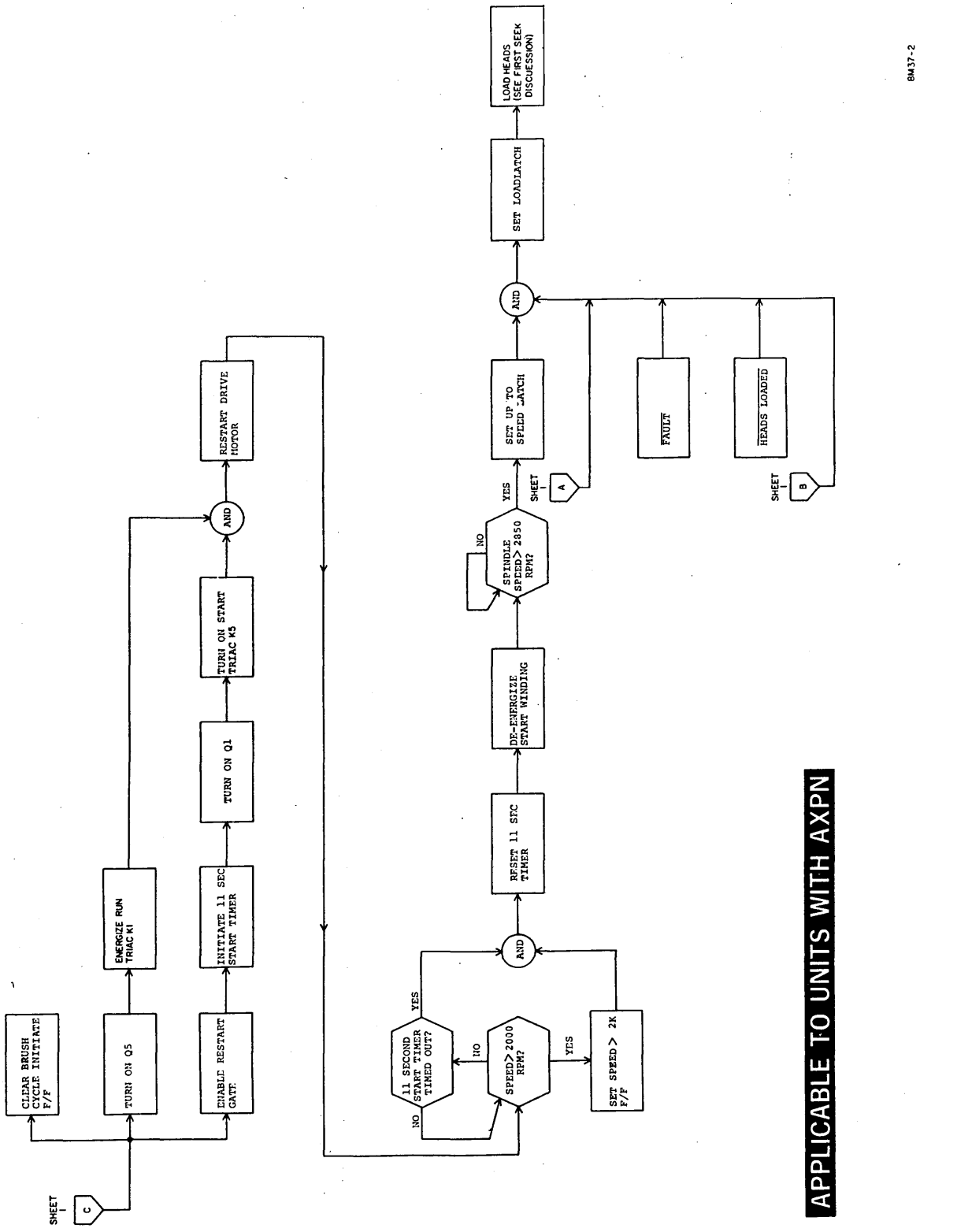


Figure 3-4. AXPN Power On Sequence Flow Chart (Sheet 2 of 2)

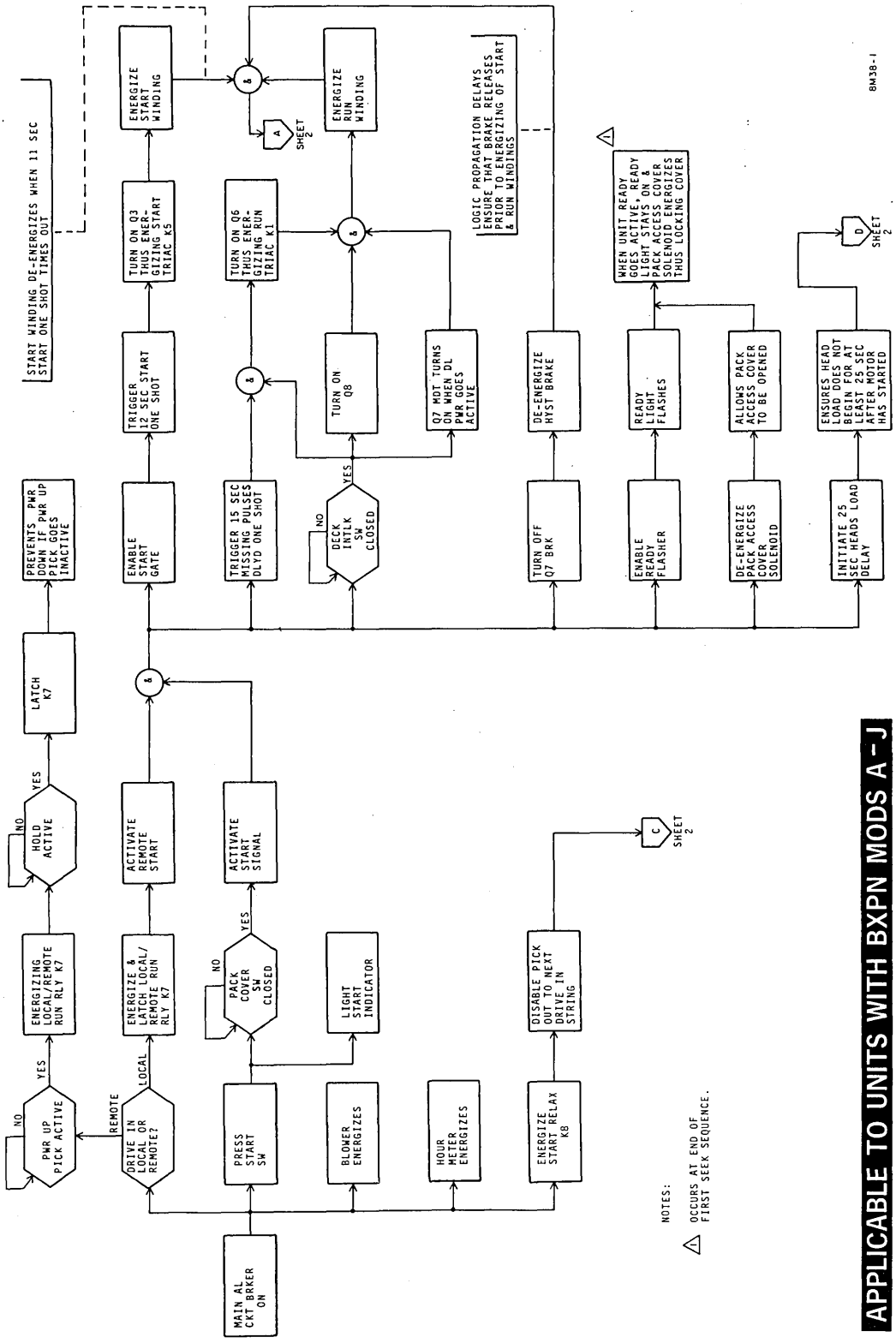


Figure 3-5. BXPN A-J Power On Sequence Flow Chart (Sheet 1 of 3)

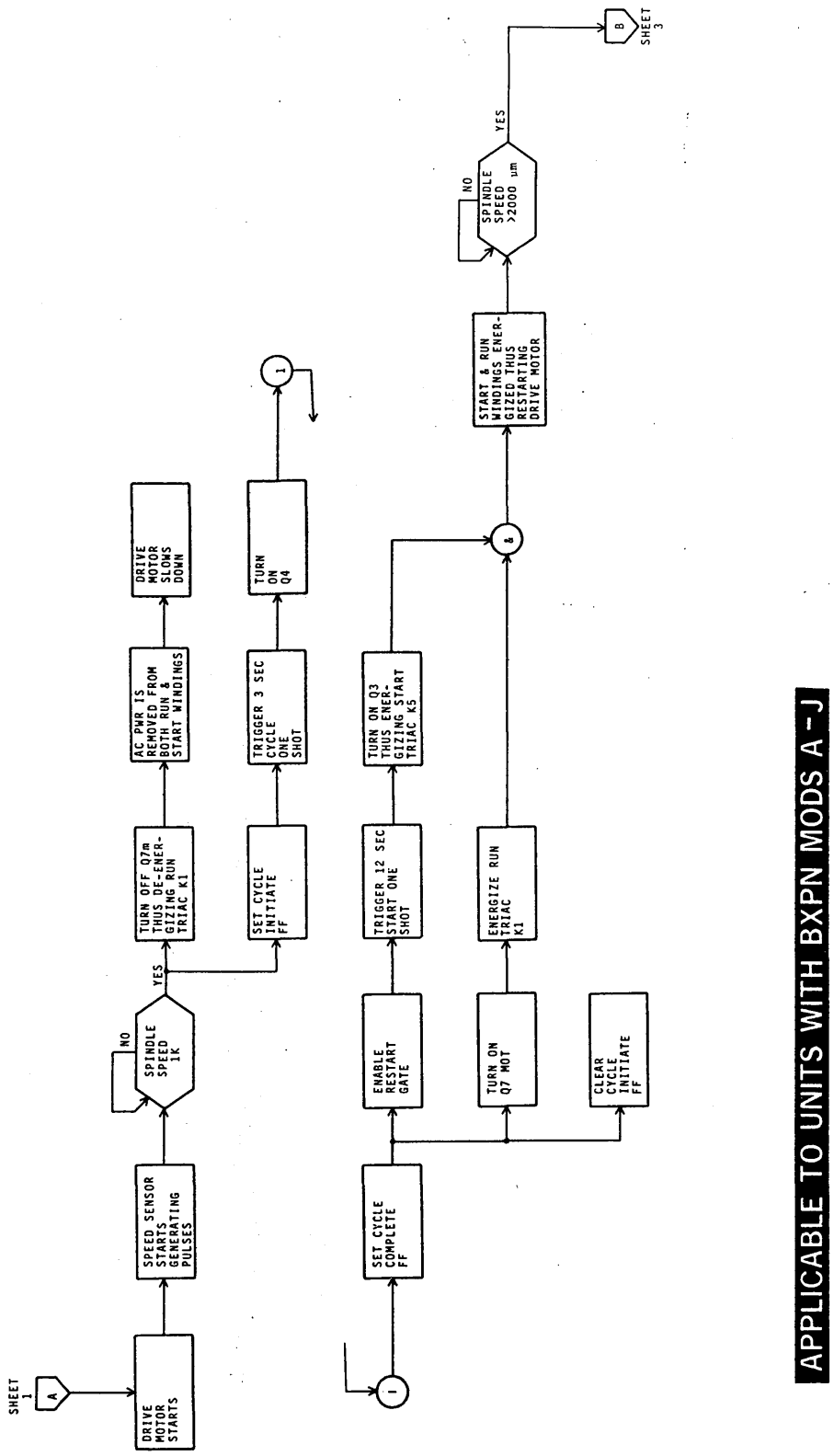


Figure 3-5. BXPN A-J Power On Sequence Flow Chart (Sheet 2 of 3)

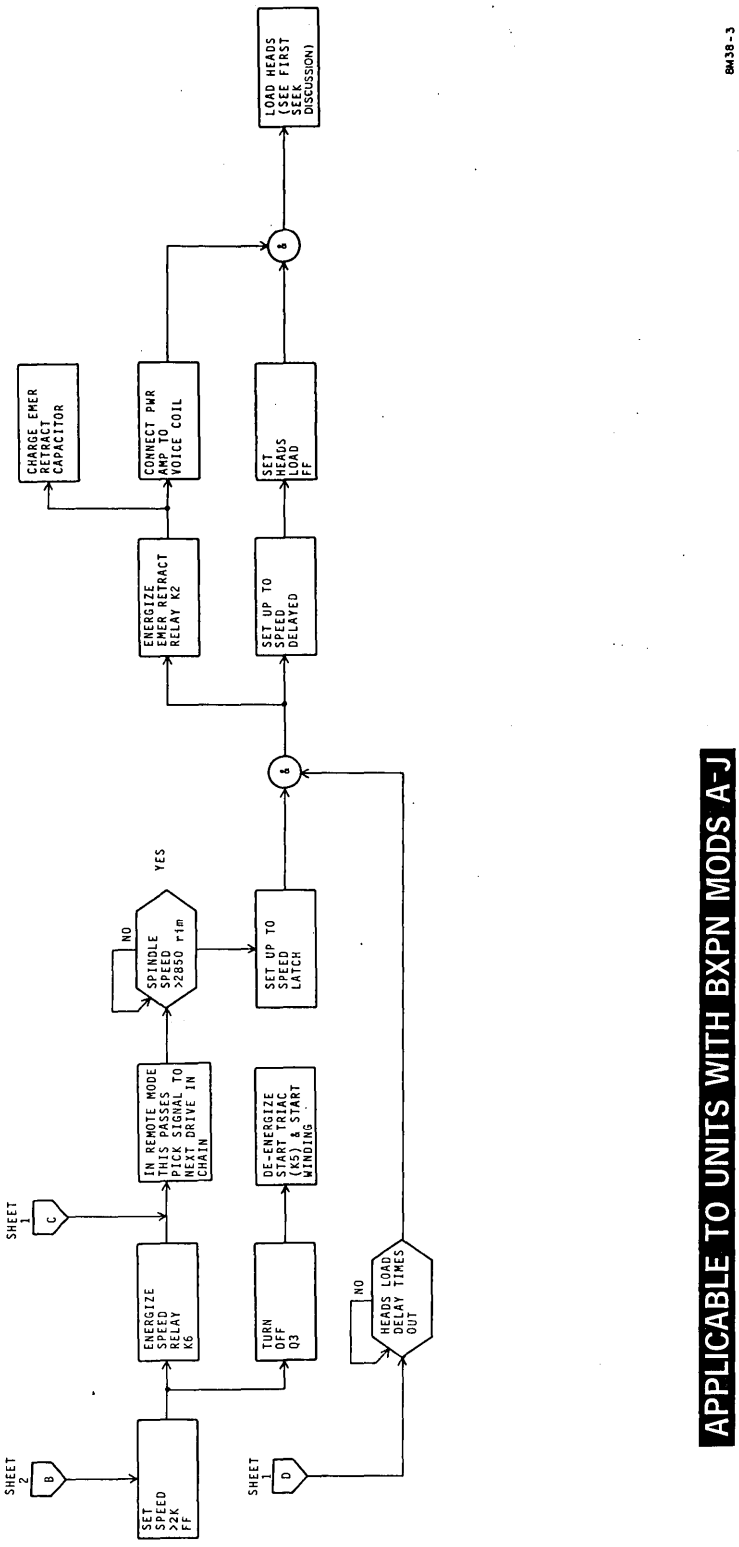


Figure 3-5. BXPN A-J Power On Sequence Flow Chart
(Sheet 3 of 3)

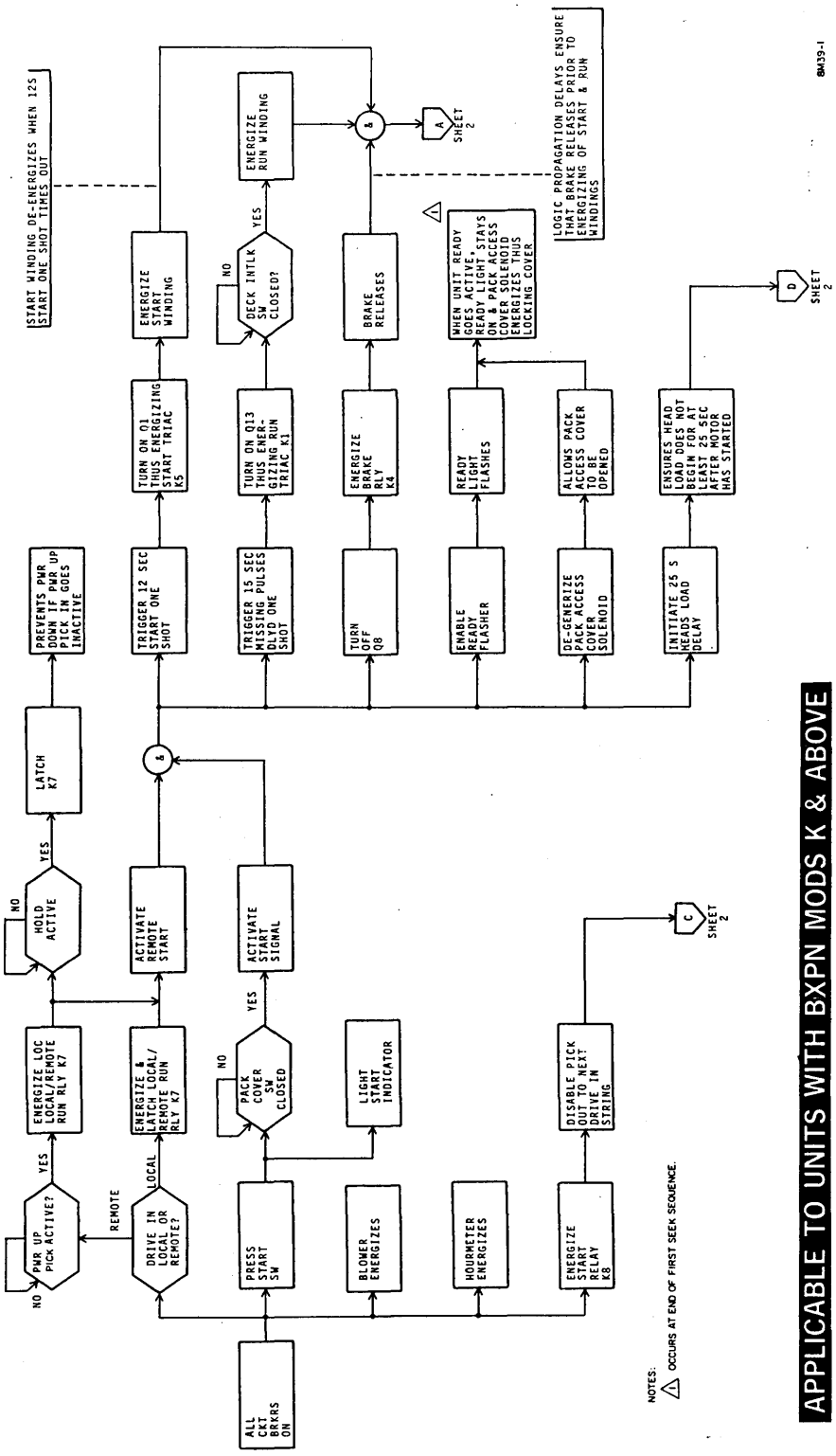


Figure 3-6. BXPN K & Above Power On Sequence Flow Chart (Sheet 1 of 2)

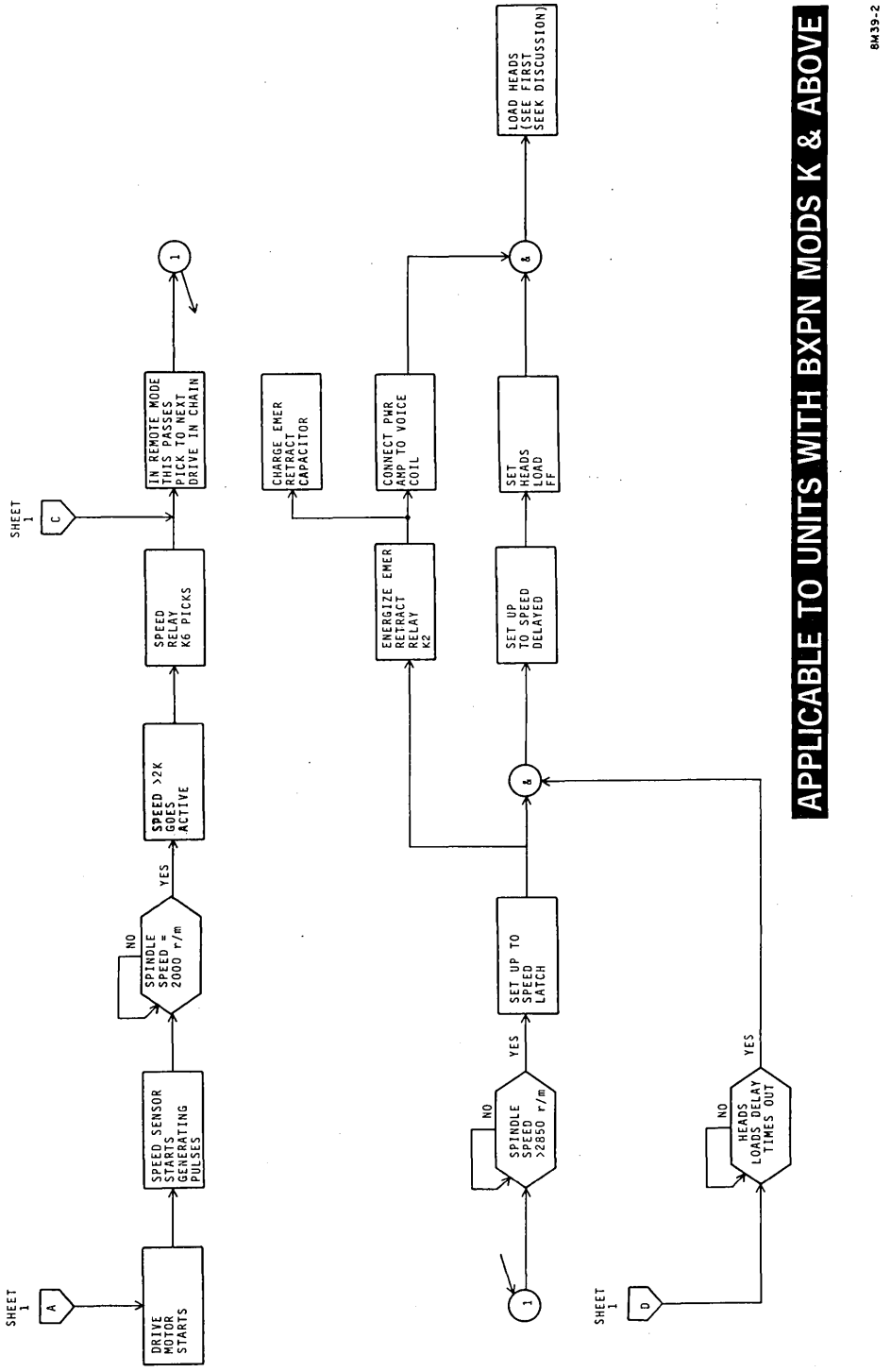


Figure 3-6. BXPN K & Above Power On Sequence Flow Chart (Sheet 2 of 2)

Power Off Sequence

The power off sequence unloads the heads and stops the drive motor. Figure 3-3 shows the circuits involved in this sequence and figure 3-7 is a flow chart of the operation.

The power off sequence begins when the START switch is pressed. This enables the RTZ logic (see RTZ Seek discussion) and cause the heads to move in the reverse direction.

When the heads unloaded switch indicates the heads are unloaded, the following events occur:

- The RTZ logic is disabled
- The run triac (K1) is deenergized to remove power from the drive motor run winding.
- The hysteresis brake is energized and applies a braking action to the drive motor.

Removing power from the run winding and energizing the brake cause the drive motor and therefore the disk pack to slow down. When pack speed is less than 2800 r/min the Emergency Retract relay (K2) deenergizes. This disconnects the voice coil from the power amplifier and connects it to the emergency retract circuit. The emergency retract circuit input pulls the heads back to the fully retracted position.

The drive motor continues to slow down and comes to a complete stop within 30 seconds of the start of the sequence. This leaves the drive in a standby condition with the blowers on and dc power active.

EMERGENCY RETRACT AND DATA PROTECTION

General

The heads are retracted under emergency conditions to prevent damage to them if the disk speed is reduced. The sequence is initiated when relay K2 is deenergized thus connecting the voice coil to the emergency retract circuit. The emergency retract circuit applies -42 volts to the voice coil causing the carriage to retract at approximately 16 inches per second. When the heads are retracted the heads loaded switch transfers and disables the emergency retract circuit.

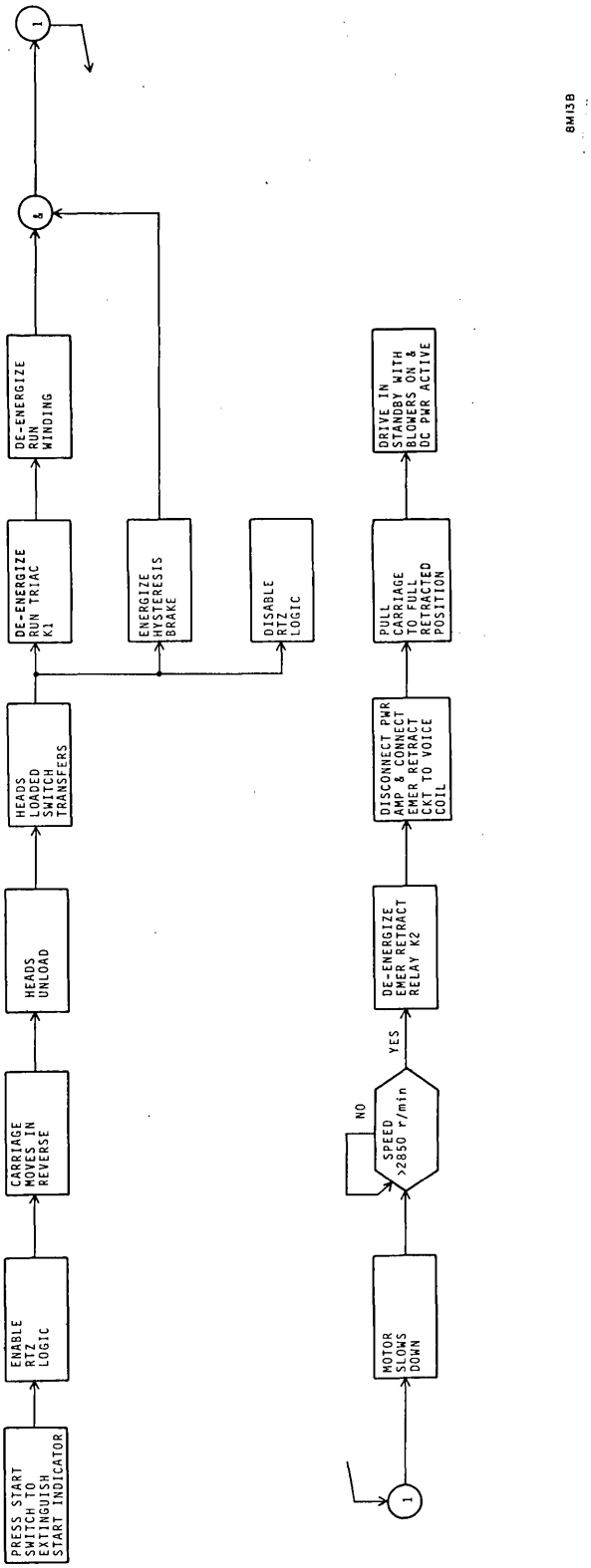


Figure 3-7. Power Off Sequence Flow Chart

The following conditions cause an emergency retract to occur:

- Loss of ac power
- Loss of spindle motor speed
- Loss of dc power
- Opening the pack cover interlock

The following paragraphs describe each of these conditions.

Loss of AC Power

Loss of site power results in:

1. The dc power supply outputs dropping to zero.
2. De-energizing all relays and disabling the logic
3. Transferring the contacts of K2 to provide a path from the emergency retract circuit to the voice coil. This circuit pulls the carriage back to its retracted stop.

Loss of ac power at the AC POWER circuit breaker or within the unit results in the loss of spindle speed (see below).

Loss of Spindle Speed

If the spindle motor speed drops below 2800 r/min, the speed detection circuit in the logic detects the speed loss and opens relay K2. This connects the voice coil to the emergency retract circuit.

Loss of DC Power

Fault circuitry in the logic detects the loss of dc voltage outputs from the power supply. Relay K2 is then opened either by the logic or directly by the loss of +20 V, thus connecting the emergency retract circuit to the voice coil. If the +12 V power is lost, servo dibits will not be detected and after approximately 350 ms the heads are unloaded. A Fault indication will appear on the control panel.

Pack Cover Interlock

Opening the pack cover interlock has the same effect as pressing the START switch (refer to Power Off sequence discussion).

ELECTROMECHANICAL FUNCTIONS

GENERAL

Certain drive functions are a result of the electromechanical devices working under the control of logical circuitry. These functions include disk pack rotation, head positioning, and drive cooling and ventilation.

Disk pack rotation is performed by the disk pack rotation mechanism, which is controlled by the power system. The purpose of disk pack rotation is to create a cushion of air on the disk surfaces. The cushion of air allows the heads (which read and write the data) to move over the disk surfaces without actually contacting them.

The heads are positioned over specific data tracks on the disk surface by the head positioning mechanism. The mechanism is controlled by the servo circuits (refer to discussion of Seek Operations) and the power system.

Drive cooling and ventilation is provided by the air flow system. The main element in this system is the blower motor which receives its power from the power system.

Figure 3-8 is a block diagram showing each of the previously discussed mechanisms. A more detailed physical and functional description of each is provided in the following discussions.

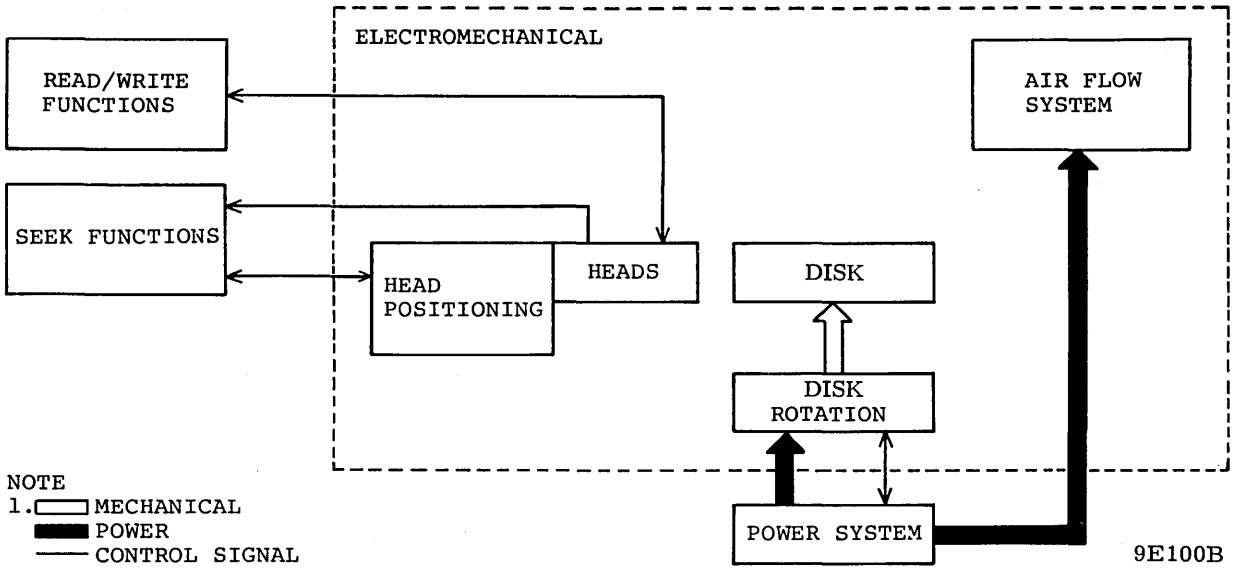


Figure 3-8. Electromechanical Functions - Diagram Block

DISK PACK ROTATION

General

The disk pack must be rotating fast enough to allow the heads to fly before any drive operation can be performed. The following mechanisms work in conjunction with the power system to control disk pack rotation (refer to figure 3-9):

- Drive Motor - Provides rotating motion for the spindle and disk pack.
- Spindle - Provides rotating mounting surface for disk pack.

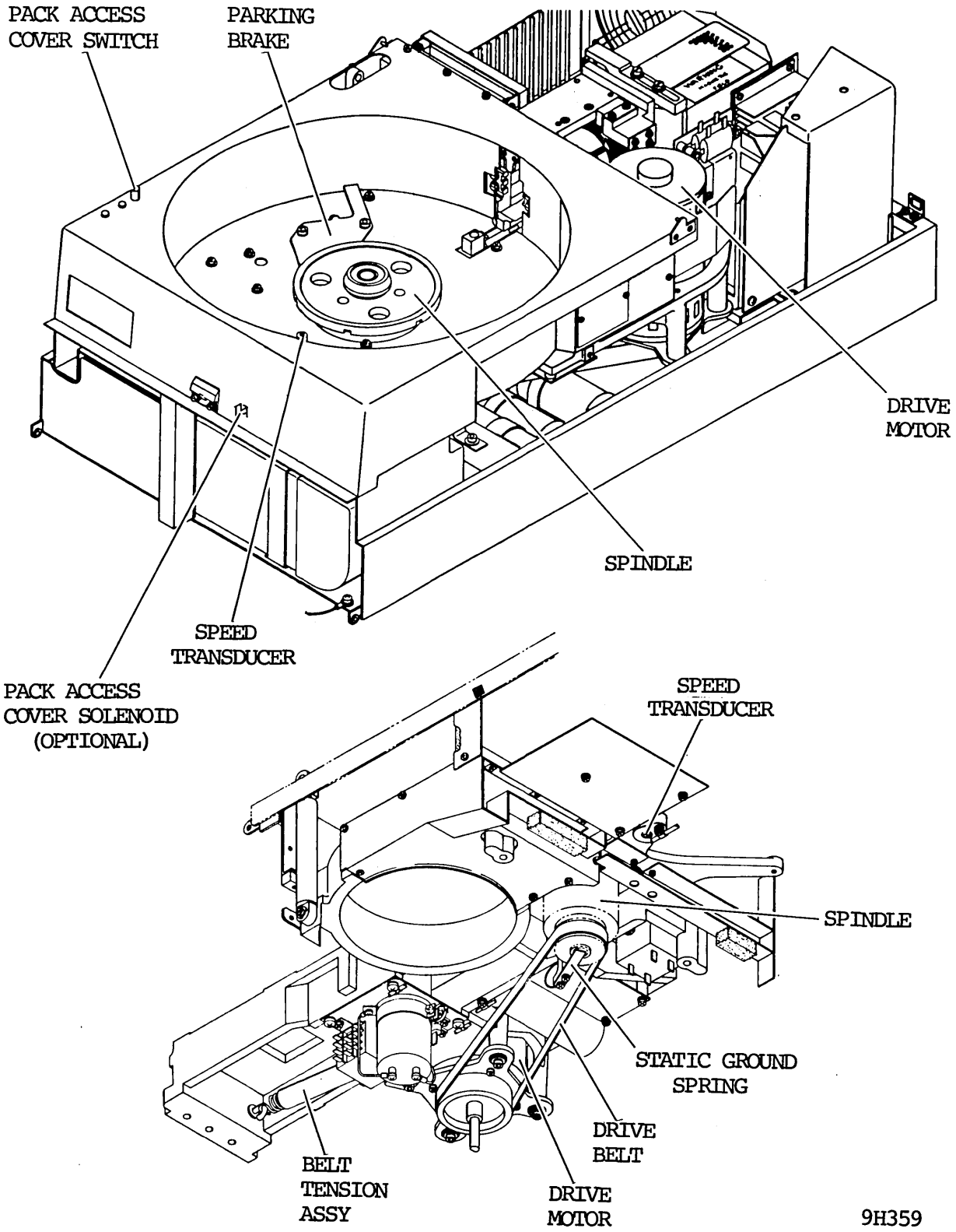


Figure 3-9. Disk Pack Rotation Mechanisms

- Parking Brake - Holds spindle while pack is being installed.
- Speed Transducer - Generates pulses that are used to determine speed of spindle.
- Pack Access Cover Switch - Ensures that pack access cover is closed before disk pack rotation begins.
- Pack Access Cover Solenoid - (Optional) Prevents pack access cover from being opened while pack is rotating.

These mechanisms are further described in the following paragraphs.

Drive Motor

The drive motor provides the rotational energy required to rotate the spindle and disk pack. The motor is mounted on the under side of the deck casting.

Motion is transferred from motor to spindle via the drive belt. This belt connects the pulley on the shaft of the drive motor to the pulley on the lower end of the spindle.

The spring in the belt tension assembly maintains enough tension on the plate to keep the drive belt tight. The spring tension is adjustable so tension on the belt can be adjusted to provide the best coupling between drive motor and spindle pulleys.

The motor starts during the power on sequence when power is applied to its start and run windings (refer to Power On Sequence discussion). The start winding helps the run winding start the motor in motion and get it up to speed. After nine seconds the start winding is no longer needed, and is disabled by the logic. The motor continues to accelerate, using only its run winding, until it reaches its maximum speed (approximately 3600 r/min). This speed is maintained until power is removed from the motors run winding.

The temperature of the drive motor is monitored by its internal thermal switch. If the motor overheats, this switch opens (pops up) resulting in loss of power to the drive motor. The motor slows down causing an emergency retract and power off sequence. The drive motor cannot be restarted until it cools off and the thermal switch is reset.

Hystersis Brake Assembly

The hysteresis brake decelerates the drive motor during a Power Off sequence (refer to Power Off sequence paragraph). The brake is energized whenever relay K4 is de-energized and the heads are unloaded. The brake mounts directly on the motor shaft, below the motor pulley. The brake consists of two concentric permeable bodies assembled with a uniform gap separating the outer diameter of one from the inner diameter of the other. These adjacent surfaces contain a series of pole faces. A permanent magnet, in the shape of a cup, fits in the gap to separate the cylinders. This cup is connected to the motor shaft by two setscrews. As long as spindle motor power is applied, brake power is not available and the cup is driven at the speed of the motor. When spindle motor power is removed and the heads unload, braking power is applied. A flux field is created between the inner and outer cylinder pole faces as braking voltage (+20 V) is applied to the inner cylinder. The flux field sets up what is in effect magnetic friction between the inner cylinder and the cup, causing the cup (and motor shaft) to decelerate. Brake deceleration in turn causes spindle motor deceleration.

Spindle

The spindle provides the means of mounting the disk pack within the drive and also of rotating the pack when the drive motor is energized.

When the pack is mounted, its lower guard disk rests on the pack mounting plate. This plate connects to a shaft which in turn connects to the pulley on the lower end of the spindle. When the drive motor starts, it transfers motion to this pulley via the drive belt and causes the pack mounting plate and disk pack to rotate.

The disk pack must be secured to the mounting plate with enough force so the two of themn will rotate together. This force is provided by the lockshaft, which is a spring loaded shaft located within the spindle. When the pack is installed, the mounting screw on the bottom of the pack is threaded into the internal threads in the upper end of the lockshaft. As the pack is tightened down against the mounting plate, the springs holding the lockshaft exert a downward force on the pack. When this force is sufficient, a release mechanism (in the handle of the disk pack storage cannister) releases the cannister from the pack. The pack is now installed and will rotate whenever the drive motor is energized.

The ground spring bleeds off any static electricity accumulating on the spindle.

Spindle Lock-Brake

The spindle-lock brake holds the spindle stationary whenever a disk pack is installed or removed. It is actuated by the disk pack storage cannister which contacts the spindle brake lock arm. This causes the brake tooth to move up and engage a slot in the bottom of the spindle thus preventing the spindle from rotating. When the cannister is removed, the arm is released, the brake tooth disengages, and the spindle is free to turn.

Speed Transducer

The speed transducer is a device that generates signals used to determine if spindle speed is sufficient to allow the heads to fly. The transducer is mounted beneath the spindle and consists of a small coil and core assembly. The transducer acts as a magnetic pick up, generating a pulse each time it senses a magnetic flux change. Since there are two magnetic slugs embedded in the bottom plate assembly of the disk pack (at 180 intervals), two pulses are generated for each revoltuion of the pack.

The speed logic monitors these signals and uses them to determine if spindle speed is at least 3000 r/min. When this speed is reached, the Speed Pulse Interval Detector can no longer time out and the Up To Speed signal is generated. It is this signal which allows the Emergency Retract Relay to pick and the heads to load. As long as the drive remains up to speed, the Emergency Retract Relay remains picked allowing the power amplifier to control the carriage position.

Pack Access Cover Switch

The pack access cover switch must be closed for the drive motor to start. The switch is in series with the START switch, and therefore only allows the Start signal through when the pack access cover is closed.

HEAD POSITIONING

GENERAL

Data is read from and written on the disk by the heads. However, the drive must position the heads over a specific track on the disk pack before a read or write operation can be performed. Head positioning is performed by the actuator, under control of the signals received from the servo circuits (refer to discussion on Seek Functions).

The actuator is mounted at the rear of the deck assembly in a position so that the heads (when extended) are driven into the pack area within the shroud and out over the disk pack. The actuator (see figure 3-10) is made up of the rail bracket, carriage and coil, and magnet assemblies.

ACTUATOR PHYSICAL DESCRIPTION

The carriage is the moveable portion of the assembly. It has the heads mounted on the front portion and the coil is attached to the rear. The carriage bearings ride on the upper and lower rails. The upper rail is attached to the rail bracket which is in turn attached to the deck casting. The lower rail is attached directly to the deck casting. In order to achieve accurate positioning, a precise alignment exists between the rails, rail bracket and deck castings.

Two cam towers, mounted on the front of the rail bracket, support the heads when they are in their retracted position. As the carriage moves forward during the heads load sequence, the heads ride down the ramps on the cam towers and are loaded onto the disk surface.

In addition to the upper rail and cam towers, the rail bracket also provides mounting for the upper stop block, heads loaded switch, and the flex lead assembly. The upper stop block, in conjunction with the lower stop block which is mounted on the deck, provide an absolute stop to prevent the carriage from being driven too far forward. The heads loaded switch provides a signal to the logic to indicate when the heads are loaded. The switch opens when the heads are extended (loaded). The flex lead assembly provides a means of applying voice coil drive power to the moving voice coil. The flex lead assembly consists of two flat flexible conductors and their associated insulating strips.

The magnet assembly provides a cutout area which allows the coil to move in and out of the magnet in response to the servo signals. The magnet also houses the velocity transducer. The transducer consists of a coil and a core. The transducer coil extends through the center of the magnet assembly and remains in a fixed position. The coil is attached to the rear of the carriage, inside the voice coil, and moves with the carriage. The velocity transducer provides an output signal which has amplitude and polarity directly proportional to the rate and direction of the carriage movement.

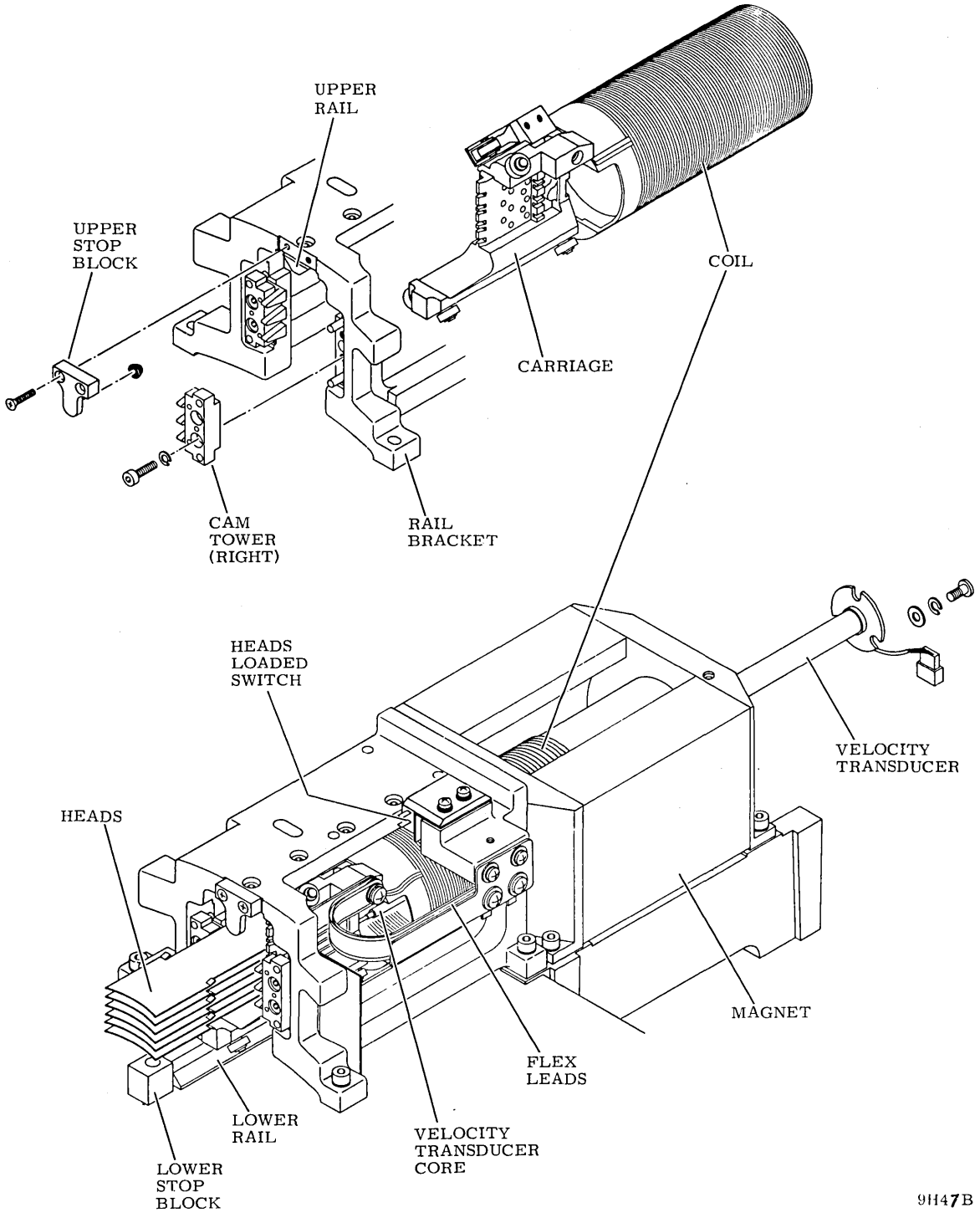


Figure 3-10. Actuator Components

ACTUATOR FUNCTIONAL DESCRIPTION

The movement of the carriage and voice coil (and therefore the heads) is controlled by the positioning signals from the servo logic. The positioning signals are derived in the seek logic and processed by the power amplifier. The output of the power amplifier is a current signal which is applied to the voice coil through the flex lead assembly.

The current from the power amplifier causes a magnetic field around the voice coil which reacts with the permanent magnetic field around the magnet. This reaction either draws the voice coil into the magnetic field or forces it away, depending on the polarity of the current through the voice coil. The acceleration of the voice coil is dependent on the amplitude of the voice coil current.

HEAD DESCRIPTION

General

The heads are electromagnetic devices that record data on and read it from the disk pack. They are mounted in the end of a supporting arm; the head and arm together are called a head-arm assembly. The head-arm assemblies attach to the carriage.

The drive has 6 heads, one for each disk surface. There are two types of heads (1) read/write and (2) servo. There are 5 read/write heads which are used to record data on and read it from the data surface. There is one servo head which is used to read position information from the servo surface. This information is used by the drives servo circuits.

The following describes the physical characteristics of the head-arm assemblies and also how they function during head load and unload sequences. Further information concerning the heads is found in the discussions on head positioning, read/write, and seek functions.

Head-Arm Assemblies

Each head-arm assembly consists of a rigid arm, heads load spring, gimbal spring, and the head (refer to figure 3-11).

The rigid arm is mounted on the carriage and causes carriage motion to be transmitted to the head. However, the arm does not provide the action necessary for the head to load, unload and follow the disk surface. This action is provided by the head load and gimbal springs.

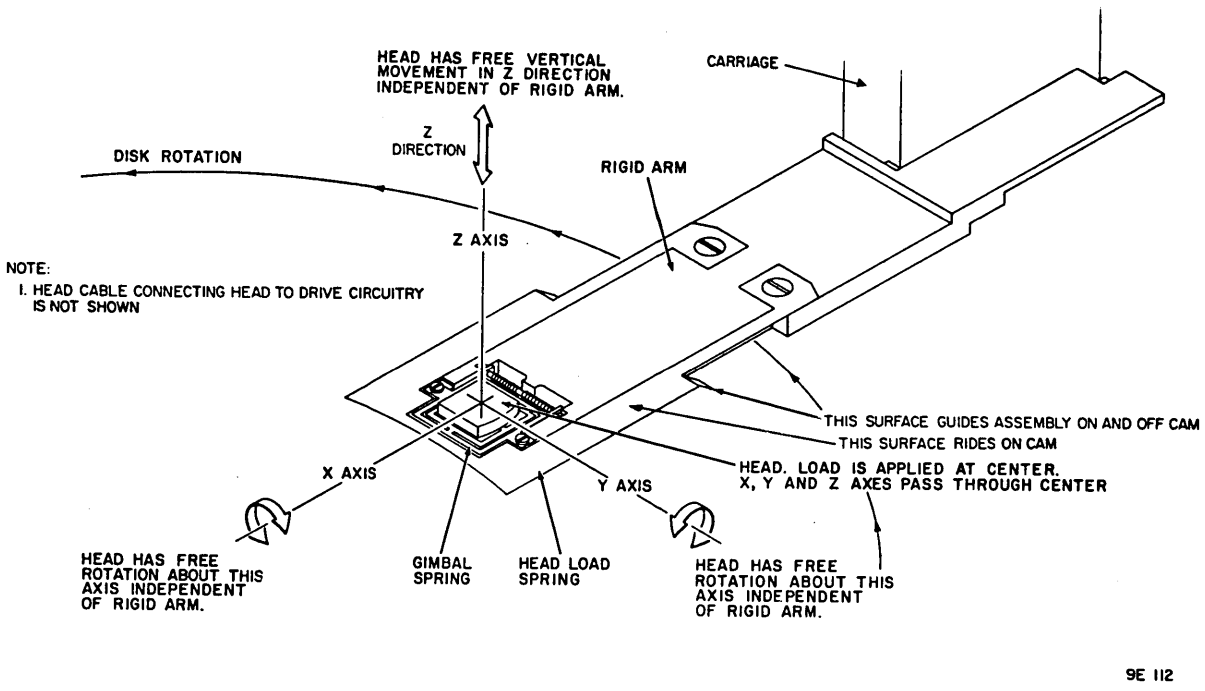


Figure 3-11. Head-Arm Assembly

The head load spring attaches to the rigid arm and is the mounting point for the gimbal spring. The head in turn attaches to the gimbal spring.

During head loading and unloading, the head load springs ride on the cam tower ramps and keep the heads from contacting one another. When the heads are loaded, the head load and gimbal springs work together and allow the heads to move independently of the rigid arms in the direction shown in figure 3-9. Such motion is necessary because when the heads are over the disk surfaces they do not contact the disk but actually fly on a cushion of air created by the spinning of the disk pack.

Information is sent to and from the heads via the head-arm cables. One end of each cable connects to a head and the other end has a plug which connects to the head select/read amplifier card.

Head Loading

The heads must be loaded before the heads can be positioned to a data track for the recording and reading of data. Loading the heads consists of moving them forward from their retracted (unloaded) positions until they are over the disk surfaces. All heads are loaded simultaneously.

The load sequence is initiated during the power up sequence when the disk pack has reached 2800 r/min. At this speed the spinning disk creates a sufficient cushion of air to allow the heads to fly.

When the pack is up to speed and the load logic is enabled, the heads move forward with the head load springs riding on the cam tower ramps. As the heads move out over the disk surfaces, the head springs ride off the surfaces of the cam tower ramps (refer to figure 3-12).

The load springs, while riding off the ramps, unflex and force the heads toward the air cushions on the spinning disk surfaces. When the cushions of air are encountered, they resist any further approach by the heads. However, the head load springs continue to force the heads down until the opposing air and spring pressures are equal.

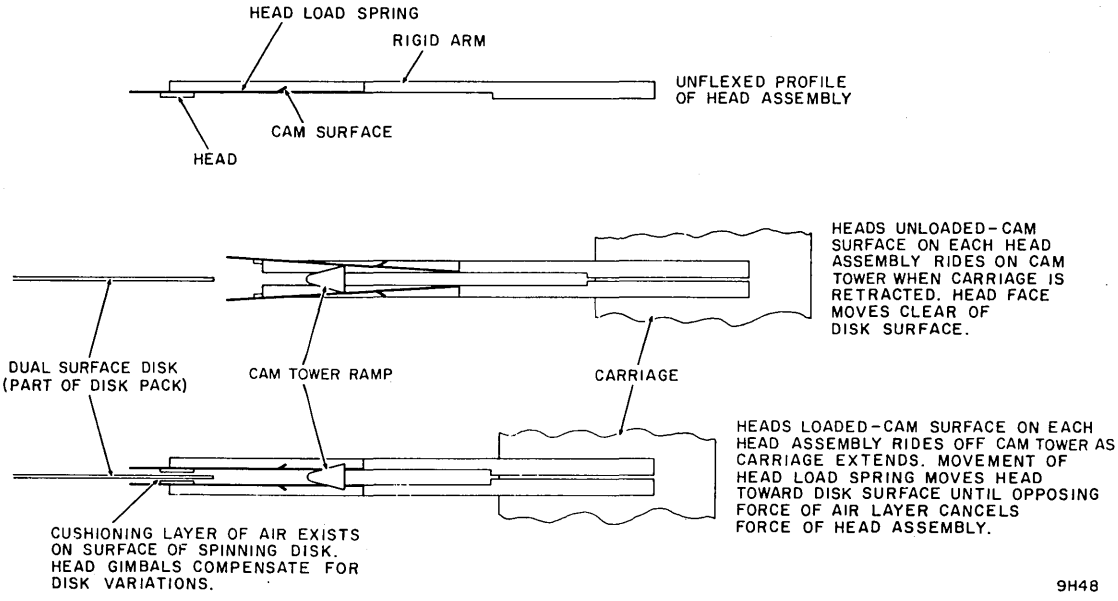


Figure 3-12. Head Loading

The air cushion pressure varies directly with disk speed and if the disk pack is rotating at the proper speed, the air and spring pressures should be equal when the heads are flying at the correct height above the disks.

If the disk pack drops below this speed, air cushion pressure decreases and the head load springs force the heads closer to the disks. Sufficient loss of speed causes the heads to stop flying and contact the disk surfaces. This is called head crash and can cause damage to both the head and disk surfaces.

Because insufficient disk speed causes head crash, loading occurs only after the disk pack is up to speed. For the same reason, the heads unload automatically if disk pack speed drops below a safe operating level (refer to discussion on emergency retract).

Head Unloading

The heads must be unloaded whenever the pack is stopped or if it is spinning too slowly to fly the heads. Unloading consists of retracting the heads until they are no longer over the disk surfaces.

The unload sequence is initiated either during a normal power off sequence, or during an emergency retract function. In both cases current is applied to the voice coil that causes the carriage to move back towards the retracted stop.

As the carriage retracts, the head load springs encounter the cam tower ramps and the heads are pulled away from the disk surfaces. The carriage continues to move back until it is fully retracted.

AIR FLOW SYSTEM

The air flow system provides cooling for the electronic components in the drive and a supply of clean air into the pack area to ensure cleanliness. The air flow system includes the blower assembly, primary filter, and absolute filter.

Air is initially drawn in through the primary filter which removes most of the particles from the air. The primary filter is located in the front of the case assembly on all mounting configurations except the acoustic. The primary filter in the acoustic cabinet is located in the front of the cabinet base, facing the floor.

On all drives, the air is drawn into the machine by the blower assembly. The blower motor provides the force to pull the air in and then push it through the machine. A port in the rear of the blower housing vents air into the read/write cards on the back of the shroud and through the logic chassis.

The other outlet from the blower housing vents air through the absolute filter, which removes all particles which might cause damage to the heads or disks. The air is then blown into the pack area, across the turning disks, and out through the heads and actuator mechanism. Since the air is forces into the pack area, a positive pressure is created which prevents contaminated air from entering around the pack access cover. Air coming out of the pack area through the actuator also vents across the power amplifier and power supply.

INTERFACE

GENERAL

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals and read/write data transmitted and received by the drive.

The interface consists of the I/O cables and the logic required to process the signals sent between drive and controller.

The following describes both the I/O cables and I/O signal processing.

I/O CABLES

All signal lines between drive and controller are contained in two I/O cables. These are referred to as the A and B cables.

The A cable contains lines connected in twisted pairs, which carry commands and control information to the drive and status information to the controller.

The B cable contains lines which are either shielded or connected as twisted pairs. These lines carry read/write data, clock and status information between drive and controller.

Figure 3-13 shows all lines (except those not used) in the A and B cables. The functions of each of these lines is explained in tables 3-1 and 3-2.

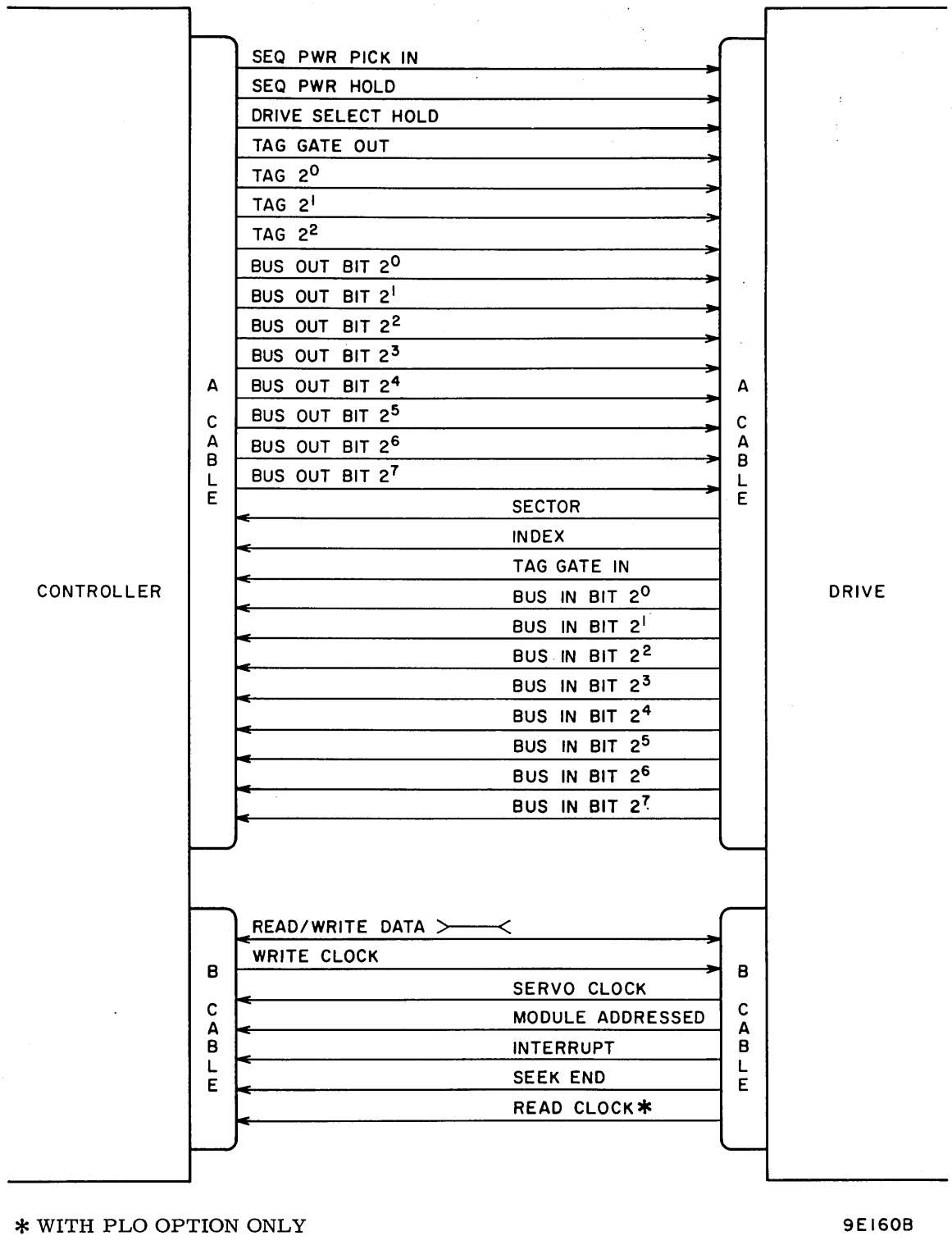


Figure 3-13. Interface Lines

TABLE 3-1. CONTROLLER TO DRIVE SIGNAL LINE FUNCTIONS

Signal Line	Signal Function
Sequence Power Pick	Used for power sequencing. A ground on this line powers up drive if LOCAL/REMOTE switch is in REMOTE, and START switch is on (refer to discussion on Power System).
Sequence Power Hold	Used for power sequencing. This line must be grounded at controller for drive to complete and hold remote power up sequence (refer to discussion on Power System).
Drive Select Hold	Allows signal information to be received by drive. Signal must be active to select or control drive. Essentially an open cable detector.
Tag Gate Out	Enables drives tag bus decode thus gating the tag bus commands to the drive logic (refer to discussion in I/O Signal Processing).
Tag Bus 0-2	Carry information which is decoded by drives tag bus decode and used in conjunction with Bus Out Lines to produce desired function (refer to table 3-3 and to discussion on I/O Signal Processing)
Bus Out Bits	Carry information which is used in conjunction with Tag Bus lines to produce specific drive functions (refer to table 3-3 and to discussion on I/O Signal Processing)
Write Clock	Used by drive write circuits this signal is synchronized to NRZ data sent from controller. This signal is actually Servo clock retransmitted to the drive by the controller and is transmitted continuously.
Read/Write Data	Carries Write data to drive during write operations and Read data to controller during read operations (refer to discussions on Read/Write functions).

TABLE 3-2. DRIVE TO CONTROLLER SIGNAL LINE FUNCTIONS

Signal	Function
Sector	Derived from servo surface of disk pack, this signal can occur any number of times per revolution of disk pack. Number of sector pulses occurring per revolution depends on setting of switches on card in position A06 in logic chassis (refer to discussion on Sector Detection).
Index	Occurs once per revolution of disk pack and its leading edge is considered leading edge of sector zero. This pulse is typically 2.5 µs in width (refer to discussion on Index).
Tag Gate In	Goes active about 300 ns after the drive has received Select Hold and Tag Gate Out; by this time Bus In is stable and can be sampled by controller. It should be noted that during read/write operations Bus In is dynamic and Tag Gate In indicates compliance with the command.
Bus In Bits	Carry status information concerning operation being performed (refer to table 3-3).
Servo Clock	Derived from disk pack servo surface, this signal has a nominal frequency of 9.67 Mhz but varies as disk pack rotational speed varies (refer to discussion on Machine Clock).
Module Addressed	Goes active when drive receives Tag 000 accompanied by logical address (on Bus Out Bits 4-7) that match logical address as indicated by drive Logical address Plug (refer to discussion on Unit Selection).
Interrupt	Goes active when drives rotational position sensing is activated and the drive is over a specified sector (refer to discussion on rotational position sensing).

Table Continued on Next Page

TABLE 3-2. DRIVE TO CONTROLLER SIGNAL LINE FUNCTIONS (Contd)

Signal	Function
Seek End	Indicates a seek operation has been completed. It is an indication of On Cylinder or seek error; therefore, the seek may or may not have been successful (refer to discussion on Seek Functions).
Read Clock	Derived from NRZ read data in those units with Read PLO option (refer to discussions on Read/Write Functions).

I/O SIGNAL PROCESSING

General

I/O signals from the controller initiate and control all drive operations except power on (refer to discussion on Power System). The I/O signals are sent to receivers in the drive and are routed from the receivers to the appropriate drive logic. The drive in turn sends information back to the controller via the transmitters. Figure 3-14 shows all I/O signals and how they are routed to and from the drive logic.

There are two basic types of I/O signals: (1) tag/bus out/bus in and (2) discrete. The two types differ in that the tag/bus out/bus in signals work in conjunction to perform a variety of functions while generally the discrete signals work independently each performing a specific function. Both types are described in the following.

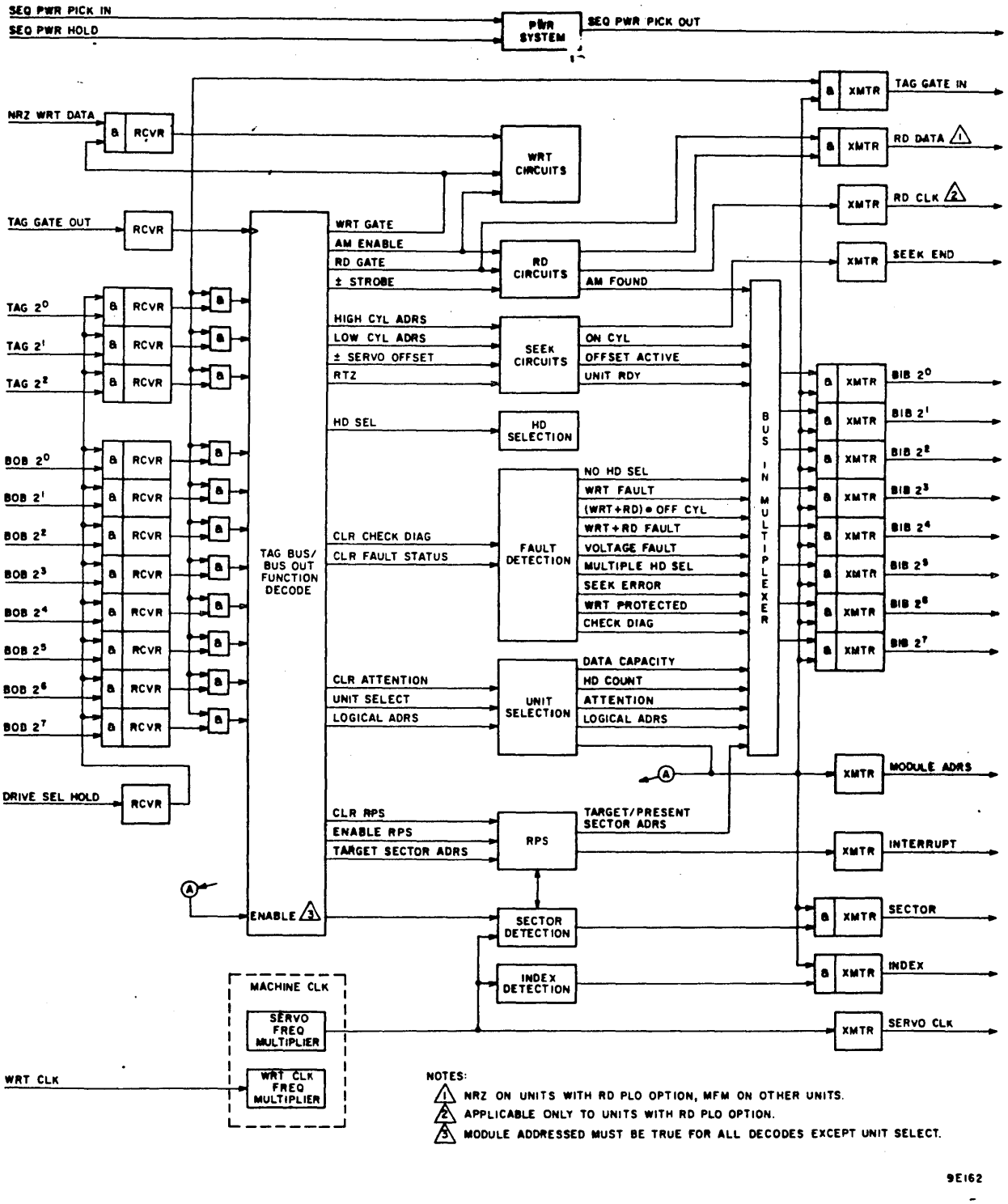


Figure 3-14. I/O Signal Processing Logic

Tag/Bus Signals

All commands are sent to the drive via the tag and bus out signal lines. The tag lines define the basic operation to be performed and the bus out lines modify or further define the basic operation. Whenever the drive receives a tag/bus out command it responds by sending status information back to the controller via the bus in lines.

Table 3-3 explains all the tag/bus out commands recognized by the drive and also describes the drives bus in responses to them. Figure 3-15 is a flow chart of the basic tag/bus out command sequence.

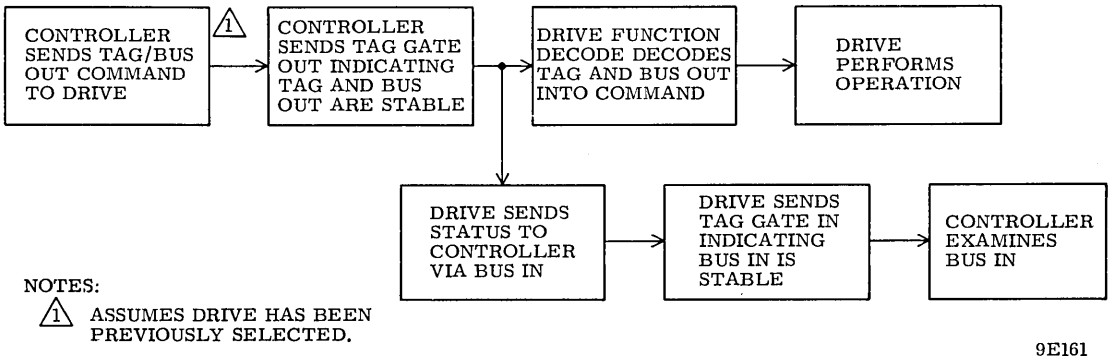


Figure 3-15. Tag/Bus Out Command Sequence Flow Chart

TABLE 3-3. TAG FUNCTIONS

Tag	Function
000 Unit Select	1. Used in conjunction with Bus Out bits 4-7 to initiate drive selection. Once selected, the drive replies with Module Addressed and status on Bus In (refer to discussion on Unit Selection for more information). 2. Bus Out is defined as follows: BOB 0-3 Not Used 4 Logical Address Bit 2^3 5 Logical Address Bit 2^2 6 Logical Address Bit 2^1 7 Logical Address Bit 2^0 3. Bus In is defined as follows: BIB 0 Device ID: If logical one it indicates 80 MB drive. If logical zero it indicates 40 MB drive. BIB 1 Device ID: Always false to indicate that this unit has 5 data heads. BIB 2 Not Used BIB 3 Attention: When true it indicates that heads were unloaded and disk pack slowed down (possible pack change). This bit is cleared by Tag 010, BOB 1 (Clear Attention). BIB 4-7 Logical Address: Reflect contents of Bus Out bits 4-7.
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
001 Error Recovery	1. Initiate data error recovery operations. Specific operation is determined by bus out bits accompanying tag. 2. Bus Out is defined as follows: BOB 0* Early Strobe: Conditions MFM to NRZ converter circuits to strobe data at earlier than optimum time (refer to discussion on Read PLO/Data Separator). BOB 1* Late Strobe: Same as early strobe except that data is strobed at later than optimum time. BOB 2 Positive Offset: Causes drive to move heads slightly off the on cylinder position in a direction towards the spindle. BOB 3 Negative Offset: Same as positive offset except heads are moved away from spindle. BOB 4- Not Used 7 These conditions are disabled by any of the following commands: RTZ (Tag 010, BOB 0), Low Cylinder (Tag 110), Clear Error Recovery (Tag 010, BOB 4), or another Tag 001 with the associated bit (0, 1, 2, or 3) false. 3. Bus In is the same as for Tag 000.

Table Continued on Next Page

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
010 Diagnostic	1. Causes drive to perform various diagnostic functions, the specific functions performed depends on the contents of bus out. 2. Bus Out is defined as follows: BOB 0 Return to Zero Seek (RTZ): Causes drive to perform seek to cylinder 000. It also clears the Seek Error FF, resets the head register and disables the Early/Late strobe and servo offset conditions. BOB 1 Clear Attention: Clears the drives Attention FF. BOB 2 Clear Check Diagnostic: Provided fault condition no longer exists, this clears drives Fault FF and the Check Diagnostic bit. However, fault register FFs and indicators are not cleared (refer to discussion on Fault and Error Conditions). BOB 3 Clear Fault Status: Provided fault no longer exists, this clears drive's Fault latch, Fault register FFs and maintenance indicators (refer to discussion of Fault and Error Conditions). BOB 4 Clear Error Recovery: Disables error recovery conditions initiated by Error Recovery Tag (001). BOB 5 Clear RPS: Disables rotational position sensing (refer to discussion on rotational position sensing). BOB 6, 7 Not Used
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
010	3. Bus in is defined as follows: BIB 0 No Head Select: Indicates drive has been commanded to select a head address greater than 4 (maximum head address). Bit is cleared by selecting a valid head count (address less than 4). BIB 1 Write Fault: Indicates an absence of write current when a write operation is being performed. Detection of this fault prevents drive from writing data. BIB 2 Write or Read and Off Cylinder: Indicates that a write or read operation has been attempted while the heads are not on cylinder. Detection of this fault prevents drive from writing data. BIB 3 Write and Read: Indicates that a write and a read operation were commanded at the same time. Detection of this fault prevents drive from writing data. BIB 4 Voltage Fault: Indicates 5 V, 20 V, or 46 V are below normal. This fault prevents drive from writing. BIB 5 Head Select Fault: Indicates more than one head selected at same time. This fault prevents drive from writing. BIB 6 Seek Error: Indicates one of the following errors occurred during seek operation. • Drive unable to complete seek within 500 ms.
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	• Carriage moved to position outside recording field (forward or reverse EOT detected). • Drive was commanded to seek to cylinder address greater than 822 (410 on 40 MB units). Seek error condition is cleared only by Return to Zero Seek command (Tag 010, BIB 0). BIB 7 Write Protect: Indicated drive's write circuits are disabled. This signal goes true under any of the following conditions: • WRITE PROTECT switch on drive operator panel is depressed and indicator is lighted. • Head alignment is being performed. • Fault condition exists that inhibits writer. Write protect condition is disabled when WRITE PROTECT switch on drive operator panel is pressed to extinguish indicator. If a write operation is commanded during a write protect condition the Check Diagnostic bit goes true.
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
011 Head Select	1. Initiates selection of head indicated by address on bus out (refer to discussion on Head Selection). 2. Bus out is defined as follows: BOB 0-4 Not Used 5 Head Address 2^2 6 Head Address 2^1 7 Head Address 2^0 3. Bus in bits are defined the same as for Tag 010.
High Cylinder 100	1. Sends high cylinder address bits (2^8 and 2^9) to the drive via bus out. These bits must always precede the low cylinder address bits sent via Tag 110. 2. Bus out is defined as follows: BOB 0-5 Not Used 6 Cylinder Address Bit 2^9 (used only on 80 MB units) 7 Cylinder Address Bit 2^8
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	3. Bus in contains Target register bits 2^0 through 2^7. This information is loaded into Target register during a Tag 101 and is defined as follows: BIB 0 Enable RPS 1 Target Sector Bit 2^6 2 Target Sector Bit 2^5 3 Target Sector Bit 2^4 4 Target Sector Bit 2^3 5 Target Sector Bit 2^2 6 Target Sector Bit 2^1 7 Target Sector Bit 2^0
Target Register 101	1. Used to initiate rotational position sensing (RPS) and also to read contents of drive's Present Sector register. The specific function performed depends on the contents of bus out (refer to discussion on Rotational Position Sensing). 2. Bus out is defined as follows:
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	BOB 0 Enable RPS: When true it causes drive to store, in its Target register, the sector address contained on Bus Out bits 1-7 and also enables RPS so drive will raise its Interrupt line each time it reaches this sector. When false, it causes drive to store, in its Target register, the address of sector it is in when command is received. RPS is not enabled when the bit is false. BOB 1 Target Sector Bit 2^6 BOB 2 Target Sector Bit 2^5 BOB 3 Target Sector Bit 2^4 BOB 4 Target Sector Bit 2^3 BOB 5 Target Sector Bit 2^2 BOB 6 Target Sector Bit 2^1 BOB 7 Target Sector Bit 2^0 3. When BOB 0 is true, bus in reflects what was sent on bus out (target sector). When BOB 0 is false, bus in displays sector drive was in when command was received (present sector). Bit assignments in both cases are as follows: BIB / With BOB 0 True / With BOB 0 False 0 / Enable RPS / Store Present Sector
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	1 Target Sector 2^6 Present Sector 2^6 2 Target Sector 2^5 Present Sector 2^5 3 Target Sector 2^4 Present Sector 2^4 4 Target Sector 2^3 Present Sector 2^3 5 Target Sector 2^2 Present Sector 2^2 6 Target Sector 2^1 Present Sector 2^1 7 Target Sector 2^0 Present Sector 2^0
Low Cylinder 110	1. Sends lower seven bits of new cylinder address to drive and initiates seek operation. This tag must be preceded by a high cylinder tag (100) if there is a change in the high cylinder address (bits 2^8 and 2^9). 2. Bus Out is defined as follows: BOB 0 Cylinder Address 2^7 1 Cylinder Address 2^6 2 Cylinder Address 2^5 3 Cylinder Address 2^4 4 Cylinder Address 2^3 5 Cylinder Address 2^2
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	6 Cylinder Address 2^1 7 Cylinder Address 2^0 3. Bus in is defined the same as for Tag 111.
Control 111	1. Initiates various functions depending on the contents of bus out. 2. Bus out is defined as follows. BOB 0 Transfer Sector Count: Causes drive to enable RPS and transfer present sector count to Target register (refer to discussion on RPS). BOB 1 Write Gate: Causes drive to start writing data on disk (refer to discussion on Write Circuits). BOB 2 Not Used BOB 3 Read Gate: Causes drive to read data from disk and send it to controller (refer to discussion on Read Circuits). BOB 4 Address Mark Enable: Causes drive to either read or write address marks. When this bit is true, along with BOB 1 (Write Gate) the drive creates an address mark and write fault detection is inhibited. When this bit is true along with BOB 3 (Read Gate) the drive searches for and address mark and when it is found sets BIB 4 (refer to discussions on Read/Write Functions).

Table Continued on Next Page

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	BOB 5-7 Not Used 3. Bus in is defined as follows: BIB 0 Address Mark Found: Goes true when drive detects an address mark during a read operation. BIB 1 Not Used BIB 2 On Cylinder: Indicates heads are positioned and drive is ready to read, write or perform another seek operation. BIB 3 Unit Ready: Indicates drive is up to speed, heads are loaded, and no fault condition exists. BIB 4, 5 Not Used BIB 6 Offset Active: Indicated drive servo is in offset mode. BIB 7 Check Diagnostics: Indicates one of the following conditions exists: ● Seek Error latch set ● Fault latch set ● No Head Selected fault ● Write Gate true during write protect condition. Further information status can be obtained via a Tag 010 (Diagnostic).
*Applicable only to units with Read PLO option.	

Discrete Signal

In addition to the tag/bus out/bus in signals, there are various discrete signal lines going between drive and controller. These lines carry clock, status, control and read/write data signals. The function of each of the discrete lines is explained in table 3-2.

UNIT SELECTION

The drive must be selected before it will respond to any commands from or transmit certain I/O signals to the controller. This is the case because Tag/Bus Out decode and certain transmitters are not enabled until the drives Module Selected signal is active (this is shown on figure 3-14.

The unit select sequence is initiated by a Select tag (000) accompanied by an address on Bus Out bits 2^4 through 2^7. Because the tag and Bus Out receivers are enabled by the Drive Select Hold signal, it is necessary that this signal be active when the Unit Select Tag and logical address are sent.

When the drive recognizes the Unit Select tag, it compares its own logical address to the address sent by the controller. The drives logical address is determined by the logical address plug which fits into the operator control panel. Depending on the plug used, this address can be any number from 0 to 15. If no plug is used the number is 15.

If the address sent by the controller is the same as that of the drive, the drive enables its Module Addressed signal. This signal is sent to the controller and is also used by the drive to enable certain transmitters and to enable Tag/Bus Out function decode to decode other commands.

Figure 3-16 shows the logic involved in unit selection and table 3-4 briefly describes the major elements shown in this figure.

SEEK FUNCTIONS

GENERAL

Seek operations are those drive functions that cause a repositioning of the read/write heads. The heads are attached to the actuator which, in turn, is moved by a voice coil positioner. The mechanical elements involved are described in the discussions on electromachanical functions.

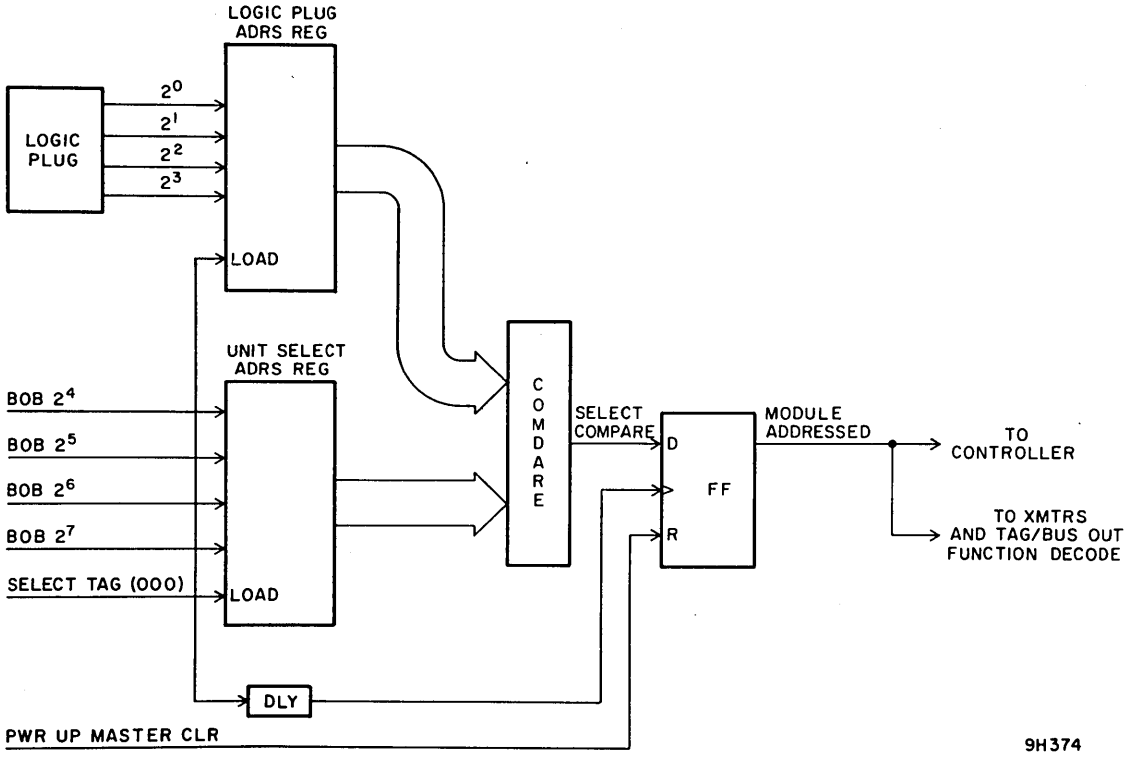


Figure 3-16. Unit Select Logic

The discussion on Seek operations is divided into the following areas:

- Servo Circuit Operation - Describes the servo circuit, which controls the voice coil positioner.
- Basic Seek Operation - Provides a general description of how the drive functions during a seek operation.
- Types of Seeks - Describes the different types of seeks performed by the drive.
- End of Travel Detection - Describes what happens when the drive positions the heads beyond the normal area of travel.

TABLE 3-4. UNIT SELECT CIRCUIT FUNCTIONS

Element	Function
Compare Circuits	Compares address sent from controller with that of drive logical address plug and provides active output when they are the same.
Logic Plug	Fits into drive operator control panel and determines logical address of drive.
Logic Plug Address Register	Loads address of logic plug when Unit Select Tag is received and applies it to input of compare circuit.
Unit Select Address Register	Loads address sent by controller when Unit Select tag is received and applies it to input of compare circuits.
Module Addressed FF	Setting this FF enables Module Addressed signal to controller indicating drive is selected. Enables tag and bus out function decode so drive can respond to further commands, and also enables Bus In and various other transmitters to controller.

The following discussions on seek functions are applicable to all drives covered by this manual. However because the number of usable tracks differs between the 40 and 80 MB drives, some specifications relating to track numbering and seek length are different. When differences exist, the 40 MB specifications are given first and the 80 MB follows in parenthesis.

SERVO CIRCUIT OPERATION

The servo circuit is a closed loop servo-mechanism used to position the read/write heads. Figure 3-17 is a simplified schematic of the servo circuit. Functions of the major elements of the system are explained in Table 3-5.

A servo loop sums all of the error voltages imposed on it. The loop always attempts to maintain itself at a null. If not nulled, the loop will adjust the correctable device (in this case, the voice coil positioner) to achieve this null. Signals applied to the loop are called error voltage. Two major error voltages are used:

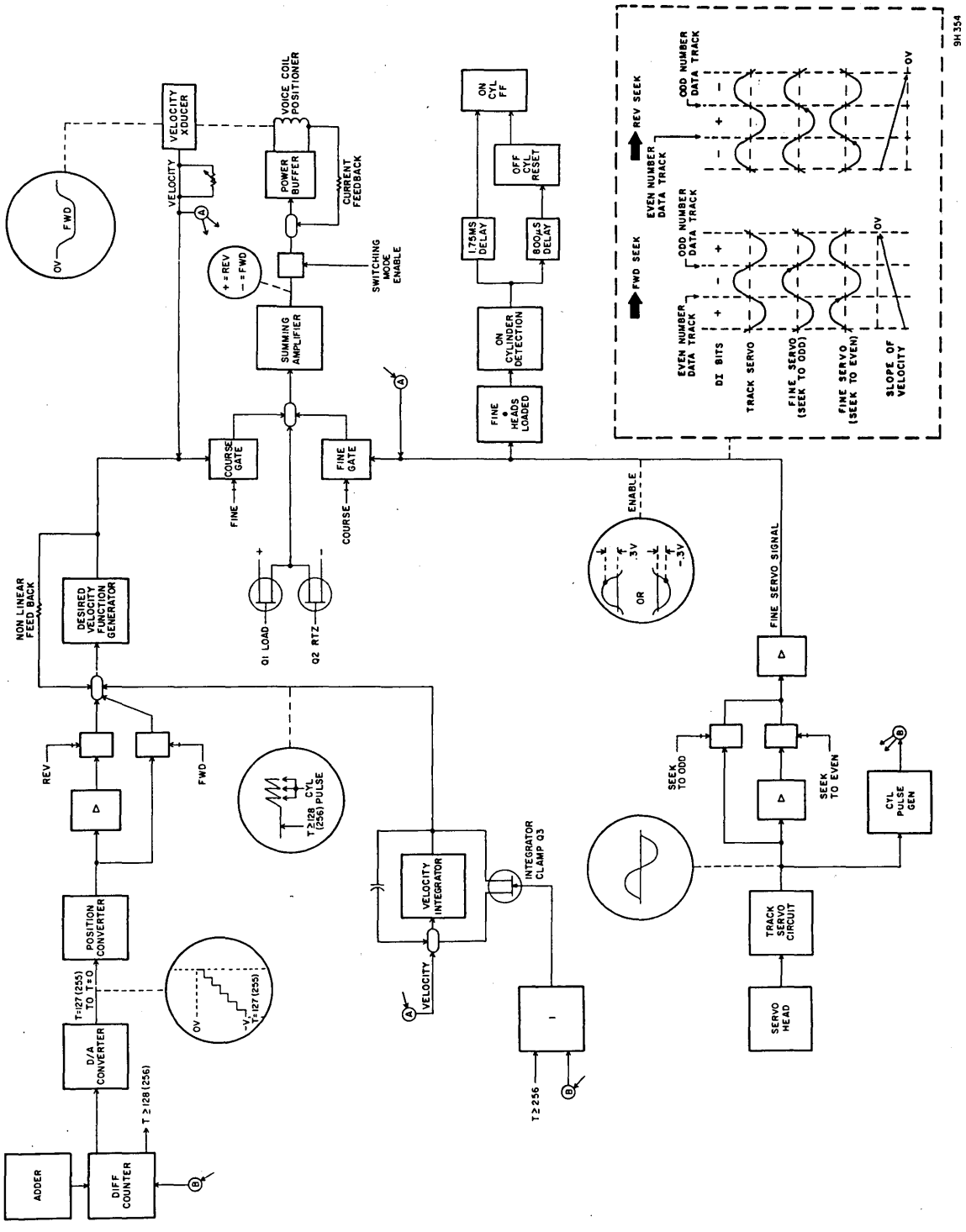


Figure 3-17. Servo Circuit

1. A position error: this is the departure of the positioner from the desired position.

2. A feedback signal to modify (or oppose) the position error to cause a smooth motion of the positioner.

The position error signal is provided by the coarse position voltage generator and the fine position voltage amplifier and their allied elements. The amplitude of the signal is proportional to the distance from the present position to the desired position. The major feedback signal is the output of the velocity transducer. The amplitude of this signal is proportional to the velocity of the positioner while the polarity indicates the direction of motion, forward or reverse.

TABLE 3-5. SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Cylinder Address Register	Holds the present cylinder address. It is updated to the new cylinder address when a seek is initiated.
Cylinder Address Adder	Combines the present cylinder address with the new cylinder address complement to arrive at the difference.
Difference Counter	Holds the number of tracks yet to be crossed before reaching the desired track or cylinder. Counter value is zero when on cylinder.
Digital-to-Analog Converter	Monitors the seven lowest order bits of difference counter to provide an analog indication of Position Error during the last 128(256) tracks (except last track) of all Seek operations.

Table Continued on Next Page

TABLE 3-5. SERVO CIRCUIT FUNCTIONS (Contd)

Circuit Element	Function
Position Converter	Provides coarse position error signal, the amplitude of which is proportional to the number of tracks to go. Amplitude is clamped at negative saturation while tracks remaining are equal to, or greater than 128(256). Amplitude decreases in discrete steps (controlled by D/A converter) as the last 128(256) tracks of a seek are crossed. Signal is inverted for reverse seeks.
Desired Velocity Function Generator	Processes position error signal at gain levels that vary as position error decreases. The resulting output is the analog representation of the desired velocity curve to achieve maximum control to deceleration. The parallel non-linear feedback circuit maintains tight loop control by increasing gain as the position error signal approaches zero. This gain control prevents loss of control during the critical deceleration portion of the seek and is essential to minimize overshoot and settle out problems. It also minimizes drift about null.
Summing Amplifier	Generates a control signal to drive the power amplifier. When position error exceeds Velocity Amplifier signal, control signal causes power amplifier to accelerate carriage. When velocity signal exceeds Position Error, carriage decelerates.
Switching Mode Control	Decelerates carriage from tracks equal 128(256) to tracks equal 7 by supplying pulses of maximum reverse current to the voice coil to follow position error deceleration curve.
Load Gate	Provides a constant positive input to the summing amplifier forward head motion during the load sequence.

Table Continued on Next Page

TABLE 3-5. SERVO CIRCUIT FUNCTIONS (Contd)

Circuit Element	Function
RTZ GATE	Provides a constant negative input to the summing amplifier to cause reverse head motion during an RTZ operation.
Power Amplifier	Responds to summing amplifier derived control signal to drive carriage mounted voice coil positioner. Current feedback is used to stabilize the gain of the power amplifier.
Velocity Amplifier	Amplifies signal of carriage mounted linear velocity transducer to provide an indication of velocity to the servo circuit. Also receives a negative feedback from positioner which acts to cancel current coupling that occurs from the velocity transducer location within the magnetic field created when current is applied to the voice coil positioner. The associated amplifier disable forces amplifier gain to zero during a Power Off sequence (unload heads). This is required so that coupling between the positioner field and the velocity transducer does not cause oscillation during movement to the retraction position.
Velocity Integrator	Provides an integrated representation of velocity between each of the last 256 track pulses of a seek. Integrator is clamped off to gain of zero at all other times. Integrator output is a sawtooth waveform applied to input of desired velocity function generator between each track pulse to fill in or smooth out the stepped signal of the D/A converter (received via the position converter).
Table Continued on Next Page	

TABLE 3-5. SERVO CIRCUIT FUNCTIONS (Contd)

Circuit Element	Function
Fine Servo and Fine Latch	Fine servo monitors integrated velocity. When difference counter is 1 (T=1) and integrated velocity exceeds 1.4 V, it indicates that there is one-half track to go. Fine latch sets to enable fine gate and disable coarse gate. This switches Position Error input to summing amplifier from desired velocity (coarse gate) to fine position (fine gate). Fine also has the following effects: a. Turns on integrator clamp to switch off velocity integrator b. Enables on cylinder detection. During load or RTZ sequences, both outputs of Fine latch are high. This disables both the fine and coarse gates so that motion is under control of load gate or RTZ gate.
Slope FF	Used to select proper track servo signal phase for use as fine position analog signal (signal controlling servo loop as last track is approached and carriage is stopped). If CAR bit 0 is not set, the seek destination is an even numbered track and the track servo signal will not be inverted for use in stopping the carriage. If CAR bit 0 is set, an odd track is identified and track servo is inverted. Register bit content is placed in Slope FF which performs actual gating.
On Cylinder Detector	Monitors fine position signal when $T \leq 1$. When signal is less than about 0.3 V (0.98 V), heads are close enough to track centerline to be assumed to be on cylinder. After 1.75 ms delay, On Cylinder is returned to controller and to drive logic. If heads overshoot at end of seek so that voltage exceeds 0.5 V(1.61 V), delay is reinitiated. Delay permits carriage to settle out before controller may attempt any read/write operations.

The loop applies its position and feedback signals to one point, the summing amplifier. If the summation of these signals is not equal to zero, the summing amplifier outputs a signal proportional to the amplitude of the error voltage (which signifies the amount of displacement from the desired position) and the phase of the error voltage (which indicates the direction of displacement).

The error output from the summing amplifier is applied to the power amplifier which supplies the current for the voice coil positioner. The voice coil positioner supports and moves the read/write heads. The voice coil is located within a powerful magnet and whenever a current passes through the voice coil windings, the interaction of the induced emf and the magnet's flux field cause the positioner to move. The acceleration of the motion is proportional to the polarity and amplitude of the voice coil current.

TRACK SERVO CIRCUIT

General

The track servo circuit provides head positioning information. The signals generated by this circuit:

1. Generates dibit signals that are used by the end of travel detection, Index, and servo frequency multiplier circuits.

2. Generate a track servo signal that indicates the displacement of the heads from their nominal track centerline.

3. Generate cylinder pulses during seeks to indicate each cylinder crossing.

Information for this circuit is derived from the track servo head (figure 3-18). This is physically similar to the read/write heads, except that it does not write. The head reads information from the servo track surface of the disk pack. This information is known as dibits; dibit is a shortened term for dipole bit. Dibits are prerecorded on the servo surface during manufacture of the disk pack. Do not confuse the servo surface with the other five disk pack recording surfaces.

Dibits are the result of the manner in which flux reversals are recorded on the servo tracks. One type of track, known as the Even track, contains negative dibits. The other track, the Odd track, contains positive dibits.

There are 412(823) dibit tracks on the servo surface. At the outer edge of the surface is a band of 24 positive dibit tracks. This area is the Reverse End of Travel (EOT) or outer guard band. In addition, there are 412(823) servo tracks alternately recorded with negative and positive dibits. Finally, toward the inner edge of the pack, there are 36 tracks containing only negative dibits. This is the Forward EOT or inner guard band.

When the read/write heads are located at the centerline of a data track, the track servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent dibit signals. The amplitude of each dibit component is proportional to the read coil overlap of the recorded servo tracks. With the head centered, the amplitudes of the two types of dibits are equal. As the head moves away from its centered position, the amplitude of one dibit component increases while the other decreases. This error voltage is the track servo signal.

The basic elements of the track servo circuit are illustrated in figure 3-19 while Table 3-6 explains their functions.

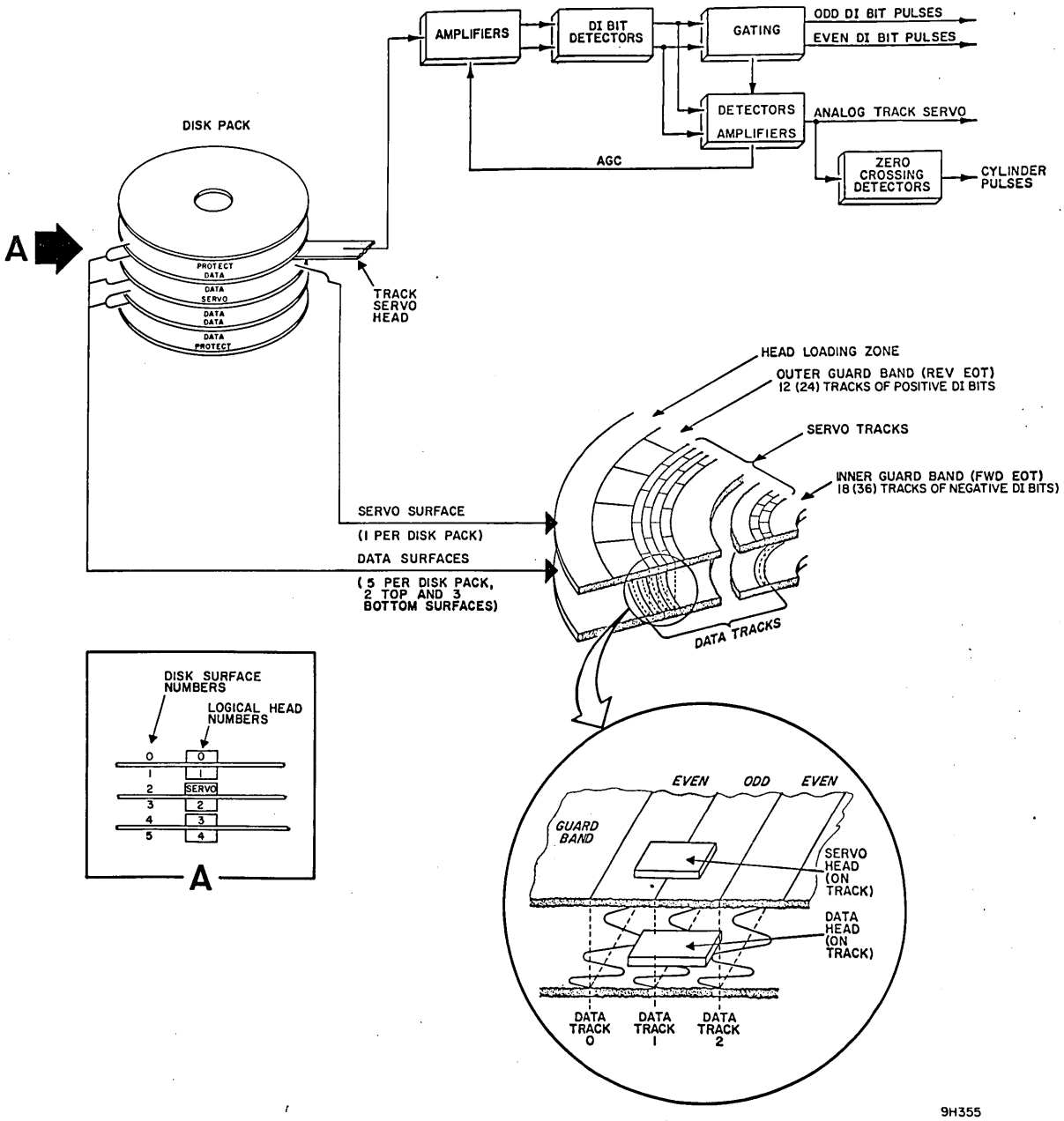


Figure 3-18. Track Servo Disk Layout

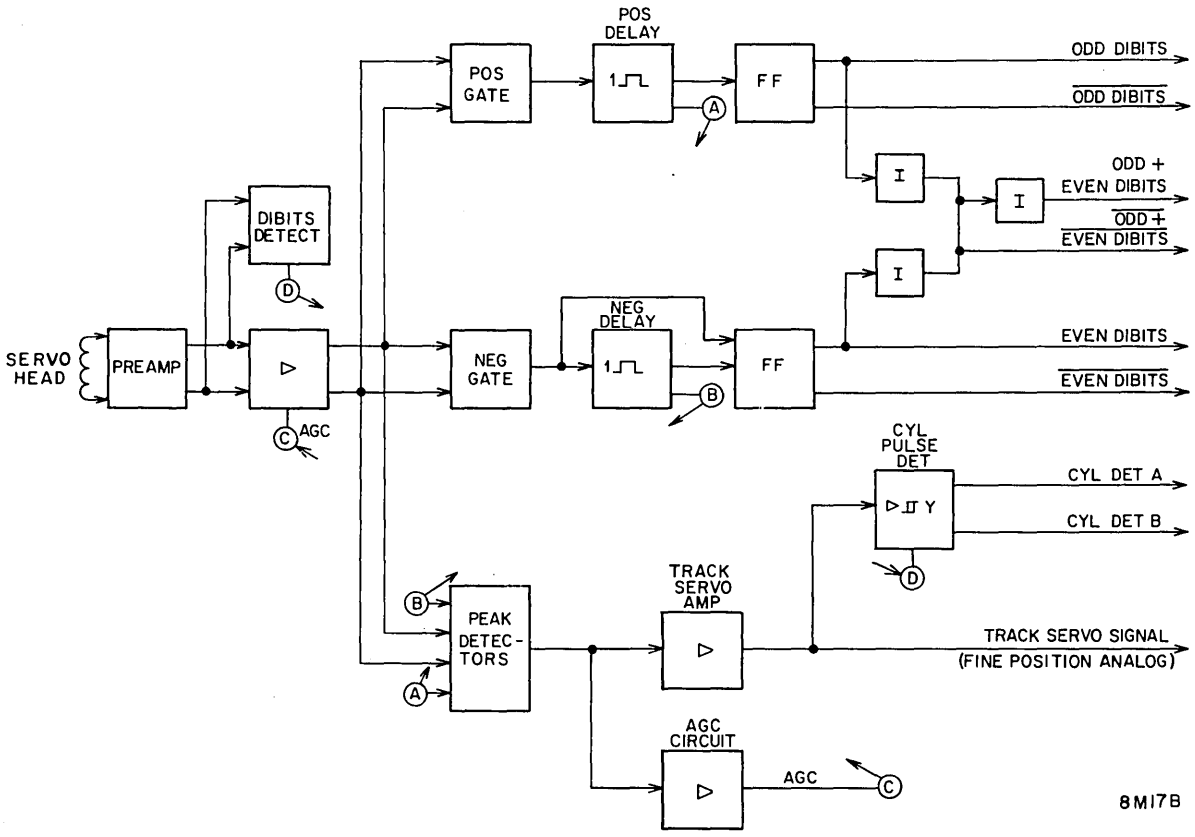


Figure 3-19. Track Servo Circuit

TABLE 3-6. TRACK SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Track Servo Head	Reads dibit information from the disk servo tracks. This head cannot write.
Track Servo Preamplifier	Amplifies the signal read by the track servo head.
Positive and Negative Gates	Separate dibit waveforms into positive and negative components. Positive gate triggers during first half-cycle of positive dibits (read from odd dibit track) and second half-cycle of negative dibits (read from even dibit track). Negative gate triggers in the reverse condition.
Positive and Negative Delays	Function as synchronizing gates to control dibit pulses generation. Positive delay fires at the leading edge of positive gate. If negative gate output is available before positive delay times out, it indicates that positive dibit has been sensed. This fires the odd dibit one-shot. (Although the positive delay fires during negative dibits, a negative gate is not available immediately thereafter; the odd dibit one-shot is not enabled.) The negative delay functions in the reverse condition. These delays inhibit inputs to peak detectors so that they react only to the positive peaks of their respective dibits.
Even Dibits and Odd Dibits One-Shots	Provide 890 ±20 ns pulses indicating dibits. Frequency of each one-shot is 403 kHz.

Table Continued on Next Page

TABLE 3-6. TRACK SERVO CIRCUIT FUNCTIONS (Contd)

Circuit Element	Function
Peak Detectors	Provide peak detection of dibit signals. Outputs are proportional to dibit amplitudes: the greater the amplitude, the more negative the output. When head is centered between dibit tracks, outputs of + and - integrators are equal. As head moves from centered position, output from one integrator increases negatively while output from the other integrator becomes less negative. The difference between these two outputs is proportional to servo head displacement from centered (on cylinder) position.
AGC Circuit	AGC voltage is proportional to sum of dibit signals. As signal strength increases, voltage goes less negative to reduce circuit gain.
Heads Loaded Detection	Provides positive signal when dibit amplitude is sufficient to indicate that heads are loaded over dibit tracks. Prior to this high output, positive/negative gates are inhibited to indicate no servo tracks detected. If dibits are not available within 350 ms after start of Load sequence (or if lost for 350 ms at any other time), no servo tracks FF sets. This initiates an RTZ sequence to unload heads and sets fault FF.
Track Servo Amplifier	Provides signal proportional to sum of + and - peak detectors. Output is null when head is centered between dibit tracks (on cylinder); negative when over odd track or outer guard band; positive when over even track or inner guard band.

Table Continued on Next Page

TABLE 3-6. TRACK SERVO CIRCUIT FUNCTIONS (Contd)

Circuit Element	Function
Cylinder Pulse	Provides cylinder pulses to difference counter and other logic elements as track servo signal approaches null. One pulse is generated per track crossed (even/odd transition or odd/even transition).
Velocity Integrator	Provides ramp signal proportional to distance travelled (velocity integrated with time). Output is positive-going during forward seek; negative-going during reverse seek. Output is pulled back to zero to reinitiate integrator function by each cylinder pulse, or during certain conditions of RTZ or Load sequences.
End of Travel (EOT) Detection	Monitors integrated velocity to enable EOT circuit. When velocity integrator output exceeds about 1.4 V, heads have moved a distance of approximately two tracks without sensing any cylinder pulses.
Reverse EOT FF	Indicates that heads are positioned over outer guard band. Refer to First Seek and RTZs discussions for further details.
Forward EOT FF	Indicates that heads are positioned over inner guard band. This is an error condition.

Dibit Gating

After being differentially amplified, the servo signal is applied to gates that separate the dibit signals by sensing the positive and negative flux reversals (figure 3-20). A positive dibit consists of a positive-going waveform immediately followed by a negative-going waveform. This component triggers the Odd Dibits FF. On the other hand, a negative dibit consists of a negative-going waveform followed immediately by a positive-going waveform. This component triggers the Even Dibits FF.

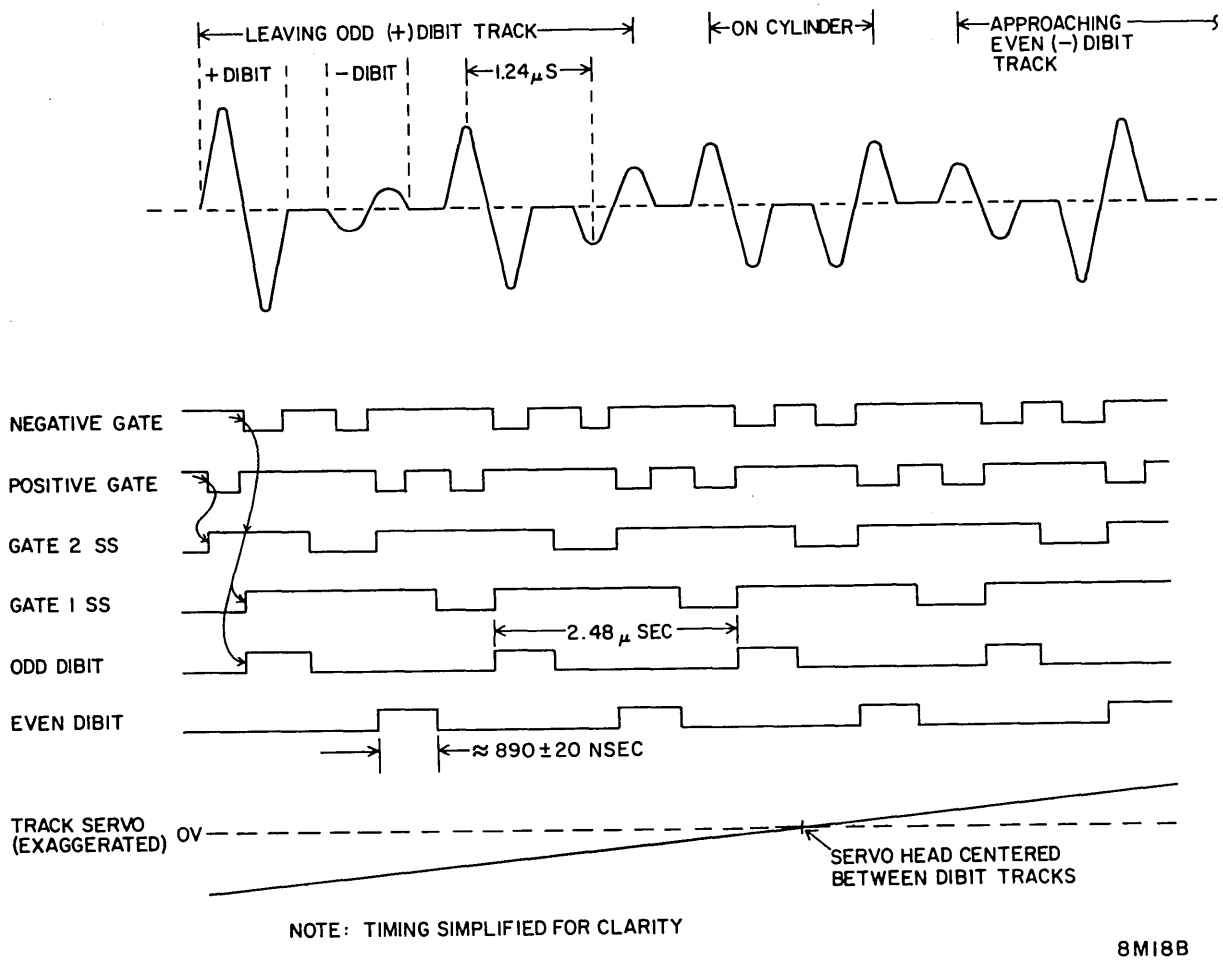


Figure 3-20. Track Servo Circuit - Signals and Timing

Track Servo Signal Generation

The track servo signal indicates the displacement of the servo head from the on-track position. When the head is centered between dibit tracks, this signal is at a null. It swings in the positive direction when the amplitude of the even (negative) dibits being sensed exceeds the amplitude of the odd (positive) dibits, and vice-versa. Amplitude is maximum when the head is centered over one dibit track, that is, the head is at its maximum distance from the centerline of the data track.

The servo signal is generated by the peak detectors that monitor their respective dibits. If the positive dibit amplitude exceeds the negative dibit amplitude, the output of the + dibits peak detector is greater than that of the - dibits peak detector. The outputs of these two detectors are applied to a summing amplifier whose output represents the distance between the two detector outputs. This output is the track servo signal. This signal is at its maximum negative value when the servo head is positioned over the outer guard band or over one of the odd dibit tracks. It is at its maximum positive value when the servo head is positioned over the inner guard band or over one of the even dibit tracks.

The track servo signal is applied to the servo circuit and to the cylinder detect circuit. In the servo circuit, it is used to generate the fine position analog signal that controls movement during the last one-half track of a seek or during a Load sequence. The cylinder detect circuit generates cylinder pulses as the track servo signal approaches a null.

Circuit gain control is achieved by applying the outputs from the peak detectors to a second summing amplifier. Its output is negative in proportion to signal strength: the stronger the signal, the less negative the agc voltage. This signal is applied to the agc amplifier to control the resistance of a FET within the amplifier. The FET is connected across the differential inputs to the amplifier. The less negative the agc, the less the resistance; therefore; more of the signal is shunted by the FET to reduce circuit gain.

Cylinder Pulse Generation

As the servo head crosses the interface of the even/odd dibit tracks (figure 3-21), the servo signal decreases toward null. The two detected cylinder pulses are ORed to a Schmitt trigger. The hysteresis designed into the trigger causes it to be up only while the servo signal is between 0 V and 0.4 V. This provides a 40 µs (10 µs) cylinder pulse. Each cylinder pulse decrements the difference counter and switches the velocity integrator to ground.

It is possible that the last cylinder pulse may not be generated when the seek is completed, causing the difference counter to hang up at 001. The On Cylinder signal provides a pulse to decrease the difference counter to 000. With the difference counter at 000 (T=0) and On Cylinder available, the Seek Complete FF sets.

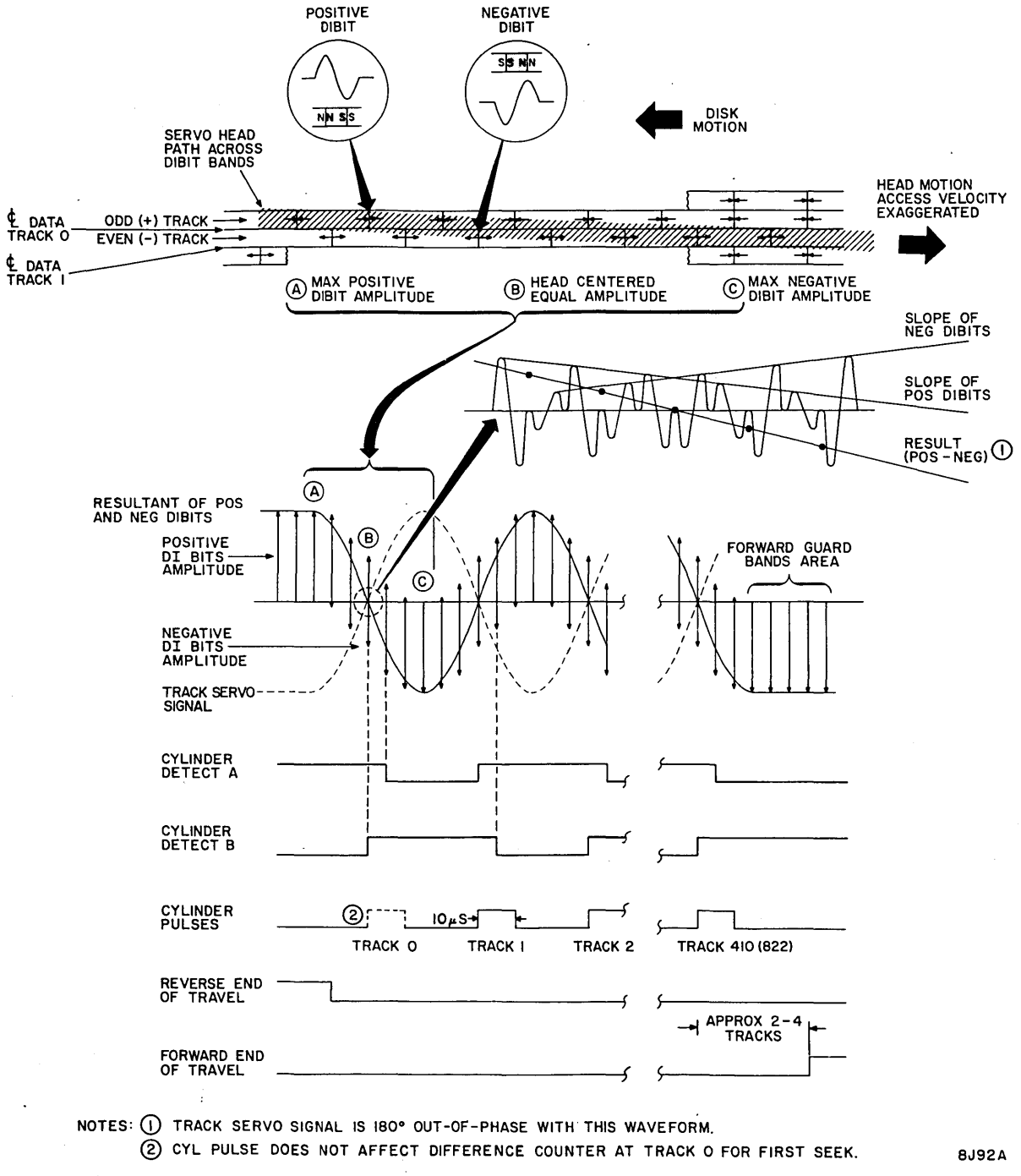


Figure 3-21. Cylinder Pulse Generation - Signals and Timing

The track servo circuit remains active following completion of a seek. If the servo head drifts off of its centered position, the track servo signal will no longer be at null. The signal, functioning as the fine position analog signal within the servo circuit, will act as a position error signal to drive the positioner back into position.

BASIC SEEK OPERATION

General

Seek operations are initiated by a series of control signals from the controller or by internally-generated signals within the drive during power up conditions. Most long seeks may be divided into four phases (see figure 3-22).

1. Accelerate Phase: the voice coil receives full current to move the positioner from the current cylinder towards the new cylinder.

2. Coast Phase: velocity is at its maximium and the positioner velocity is constant.

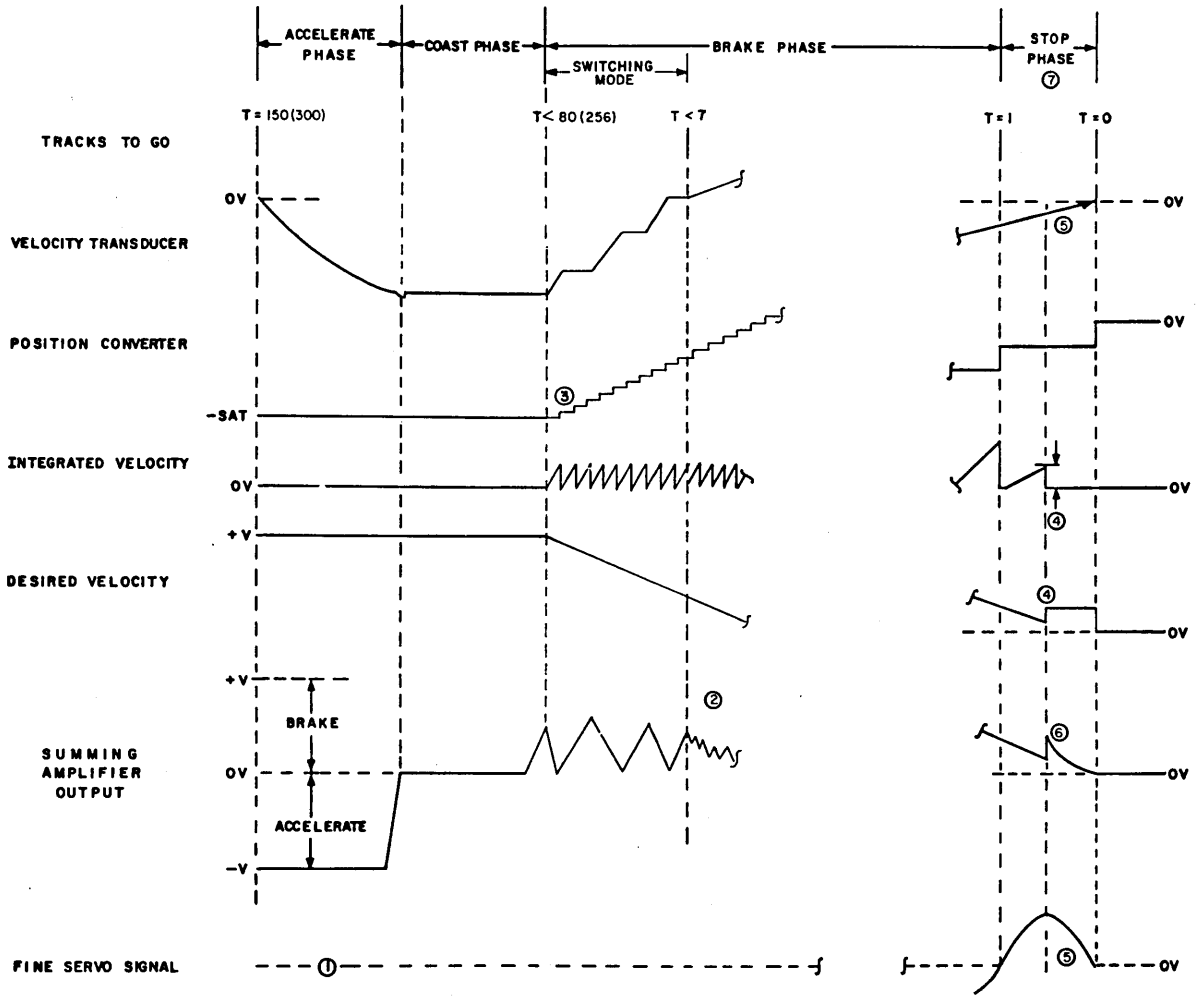
3. Deceleration Phase: the positioner is approaching the desired cylinder. Its velocity must be reduced by braking action to prevent overshoot.

4. Stop Phase: the positioner is almost at the desired cylinder. It must be stopped at the precise centerline of the new data cylinder. The logic is in Fine mode to stop and hold the positioner at the new cylinder.

Refer to the various seek descriptions for detailed information on the exact seek sequencing.

Acceleration Phase

This phase is controlled largely by the coarse position error signal. The controller sends the desired address to the cylinder address register and adder. The adder combines the new address with the present address to obtain the difference. The difference is gated into the difference counter, which decrements until tracks-to-go equals zero.



NOTES:

① SIGNAL HAS NO EFFECT UNTIL FINE LATCH SETS.

② GAIN CHANGE CAUSED BY ADDITION OF INTEGRATED VELOCITY SIGNAL TO POSITION CONVERTER SIGNAL.

⑤ OUTPUT DECREASES WITH EACH CYLINDER PULSE.

④ FINE LATCH SETS WHEN $T \leq 1$ AND INTEGRATED VELOCITY > 1.4V. DESIRED VELOCITY HAS NO FURTHER EFFECT.

⑤ COMBINATION OF THESE TWO SIGNALS CONTROLS OUTPUT FROM SUMMING AMPLIFIER.

⑥ GAIN CHANGE CAUSED BY SWITCH FROM COARSE TO FINE CONTROL. ALTHOUGH CONTINUOUS BRAKING ACTION IS ILLUSTRATED, OUTPUT MAY BE NEGATIVE (ACCELERATE) IF FINE SERVO SIGNAL EXCEEDS VELOCITY SIGNAL.

⑦ SCALE CHANGED AT T=1 FOR CLARITY.

8. DRAWING NOT TO SCALE FOR TIMING OR RELATIVE SIGNAL AMPLITUDE. IT IS SIMPLIFIED TO ILLUSTRATE SIGNAL FUNCTIONS.

8J91D

Figure 3-22. Servo Circuit Signals

The outputs of the difference counter are applied to the D/A converter. The value of these bits indicates the position error (or tracks-to-go) from 0 to 128(256), that is, the amplitude of the D/A converter output is directly proportional to the number of tracks remaining in the seek. If the remaining seek length is greater than 128(256), the D/A converter output is clamped at its maximum saturated value to cause the maximum error signal.

The input to the summing amplifier is now a large signal. Since there is no velocity yet, the current through the voice coil is maximum, causing maximum acceleration.

As the positioner accelerates, a velocity signal is generated by the velocity transducer. This signal opposes the position error signal. Its amplitude, however, is less. Acceleration continues.

Coast Phase

Eventually, the amplitude of the position error signal and the velocity feedback signal are equal. The net error signal in the loop drops to zero. The summing amplifier output follows, so current is cut off. Velocity is constant. Friction losses tend to slow the positioner but, as it does, the velocity signal decreases. This allows the position error signal to call for more current.

Deceleration Phase

Braking action starts as the positioner approaches its selected cylinder.

The track servo circuit (refer to Track Servo Circuit description) has been generating cylinder pulses as each cylinder is passed. These pulses are used to decrement the difference counter.

When T<256, the servo loop changes to the switching mode to maintain speed along desired velocity curve. This curve is the analog version of the number of tracks-to-go.

The velocity curve is generated by the desired velocity function generator. Its output is compared with velocity to achieve maximum deceleration under all conditions without overshoot. The deceleration curve permitting the best control is obtained by taking the square root of the position signal and comparing it with velocity. The position signal is the sum of the following:

1. The position error signal from the position converter. Its output, which is now unclamped, is a signal whose amplitude is proportional to the number of tracks-to-go.

2. Integrated velocity from the velocity integrator. Integrating a velocity signal provides a signal proportional to distance. This signal is a sawtooth waveform: it is pulled back to zero by each cylinder pulse and increases in proportion to velocity and time (distance). The combination of the stepping-down output from the position converter with the ramp integrated velocity signal results in a smooth curve of constantly-decreasing magnitude.

3. The square root function provided by the non-linear feedback around the desired velocity function generator.

When the desired velocity signal becomes less than the Velocity signal, current is applied to the voice coil in the maximum reverse direction until the velocity of the carriage slows down below the instantaneous desired velocity value. The current to the voice coil is then turned off and the carriage coasts under its own inertia while the difference counter continues to count down (decreasing the desired velocity signal). If the carriage velocity becomes too high for the existing desired velocity signal, a maximum reverse current is again applied until the velocity slows down below the instantaneous desired velocity value.

At $T \leq 7$ the switching mode logic is disabled and the total summing amplifier output is used to decelerate the carriage to keep the Velocity signal/Position Error signal difference to zero.

Stop Phase

Stop Phase begins when the difference counter indicates that there is one track-to-go. When T=1, the velocity integrator signal is pulled back to zero by the cylinder pulse. Its output, indicating distance, increases. When its amplitude indicates approximately one-half track remains, Fine Enable sets the fine gate. Desired velocity is disabled since the coarse gate is opened by Fine being set.

The last half-track of motion is controlled by the fine position analog signal from the track servo circuit. Fine position and velocity are applied to the summing amplifier through the fine gate. The summing of these two signals controls the braking current.

At the start of the seek, the slope FF is set if the seek is to an odd-numbered cylinder. The slope signal controls the phase of the track servo signal applied to the fine position amplifier. This adjustment is required since track servo signal phasing is a function of the servo head position: the signal is positive when over negative dibits and negative when over positive dibits. Therefore, on forward seeks, the signal decreases when approaching a data track with an odd number and increases when approaching a data track with an even number. The opposite is true during a reverse seek.

Phasing of the track servo signal is selected so that the fine position opposes the velocity signal during the last half-track of the seek. Both signals are decreasing. If either is greater, the summing amplifier makes minor braking current adjustments. When the heads are on cylinder, both signals are zero and current is zero.

When the fine position signal is less than about 0.3 V (0.98 V) the positioner is, for all practical purposes, positioned over the data track. This initiates the On Cylinder delay. After 1.75 ms, On Cylinder is returned to the controller.

The fine servo remains active even though On Cylinder is up. This is the track following or position error operation. Since the positioner is not mechanically locked in place, it can drift off cylinder. As long as it is precisely positioned, the dibits read from the adjacent dibit tracks are equal and opposite. Should the carriage move, one dibit signal will increase in amplitude. This results in a slight track servo signal which is translated into the fine position signal. The summing amplifier, in turn, senses this off-null condition and drives the positioner back on cylinder.

If the positioner goes off cylinder sufficiently to cause a fine position signal greater than 0.5 V (1.61 V) for more than 800 µs, the On Cylinder signal is lost.

The loop also permits positioner offset if the program requires it for error recovery. A Servo Offset Negative code provides a negative bias input to the fine position amplifier. This is now an error signal to the summing amplifier to cause a forward motion. This motion stops when the bias voltage and track servo voltage cancel. Servo Offset Positive causes reverse offset.

Short Seeks

The preceding explanation assumed that the seeks were long enough for the positioner to attain maximum velocity. Accelerating to maximum velocity of about 70 ips requires 60 (200) tracks. During short seeks, gating is identical although relative phasing of the error signals will vary.

During seeks less than 128 (256) tracks, certain signals are available immediately: integrated velocity, non-linear feedback to the desired velocity function generator, and a position converter output not clamped at its maximum value. These signals generate a position error voltage to accelerate the positioner. Because the amplitude of the desired velocity signal is less, however, the voice coil current is not as great as during long seeks.

The net effect of these differences is that system gain is reduced. Acceleration is reduced accordingly to permit minimum total seek time while not permitting over acceleration that would cause overshoot. The primary function remains unchanged: acceleration occurs when the position error signal exceeds the velocity signal; braking occurs when the velocity signal exceeds the position error signal.

TYPES OF SEEKS

General

The drive performs 3 basic types of seeks:

- First Seek - Initiated by pressing the START switch, it causes the heads to load and position themselves at cylinder 000.
- Direct (Forward/Reverse) Seek - Performed when the controller commands the drive to move the heads from one location to another.
- Return to Zero Seek - Initiated by the controller it causes the drive to position the heads at cylinder 000.

First Seek (Load)

This function involves the activities that a unit must perform before it can effectively respond to a Read, Write, or Seek command from the controller. This function consists mainly of power supply relay sequencing and status checking by the units logic. As a result, no actual selection of the unit is required and very little drive/controller signal exchange occurs.

Successful progression of the function assumes that all circuit breakers are on, disk pack is installed on spindle of unit, and the interlock is closed. Successful completion of a load is signified by the occurence of an On Cylinder and the lighting of the READY indicator.

Initiation of the function occurs when the operator panel START switch is pressed. See figures 3-23 and 3-24 for the first seek flow chart and timing diagram. The START switch enables relay K4. This releases the hysteresis brake and starts the spindle motor through relay K1.

When the disk pack speed reaches approximately 2800 r/min, voice coil relay K2 is energized to connect the power amplifier to the voice coil. The speed sensing circuitry also enables the up to speed logic at approximately 2800 r/min, providing an Up To Speed signal to the Load latch. The Load latch activates circuitry to produce an average forward 7 ips access that mechanically loads the heads. The carriage continues forward with the servo head searching for the prerecorded positive dibit signals on the track servo surface. When the reverse EOT area (all odd, positive, dibits) is sensed, the Load latch is cleared, the Reverse EOT FF is set, and the Fine gate and latch are enabled. The carriage now moves under control of the Fine Position analog signal. When even dibits are detected (approaching track 000) the Fine Servo signal decelerates the carriage.

The drive sends On Cylinder to the controller 1.75 ms after the Fine Position signal is less than 0.3 V (0.98 V). The carriage stops when the Fine Position signal is 0 V. The Servo Ready latch is then set, and the READY indicator is turned on. The drive is now ready to perform a Read, Write, or Seek operation.

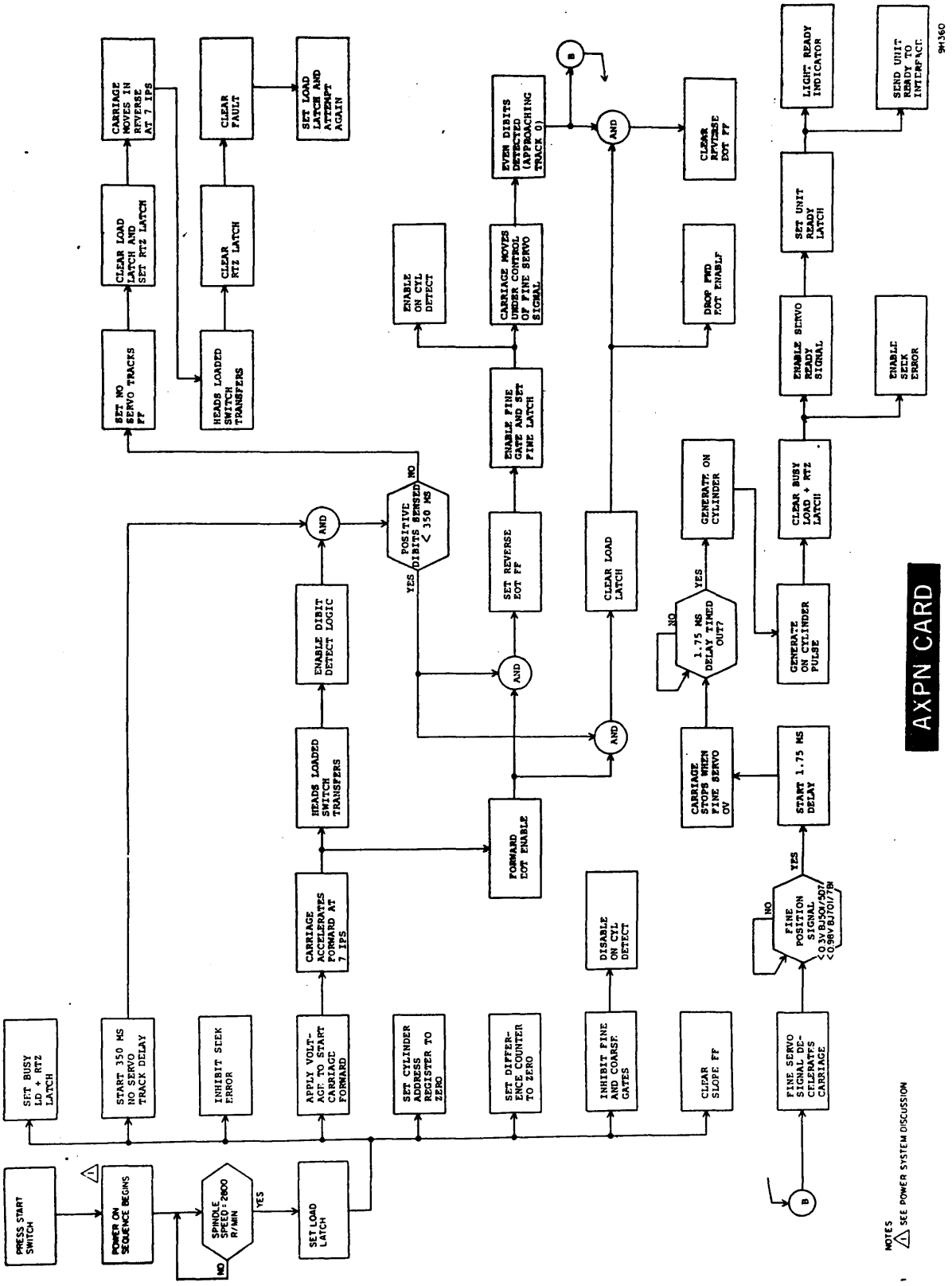
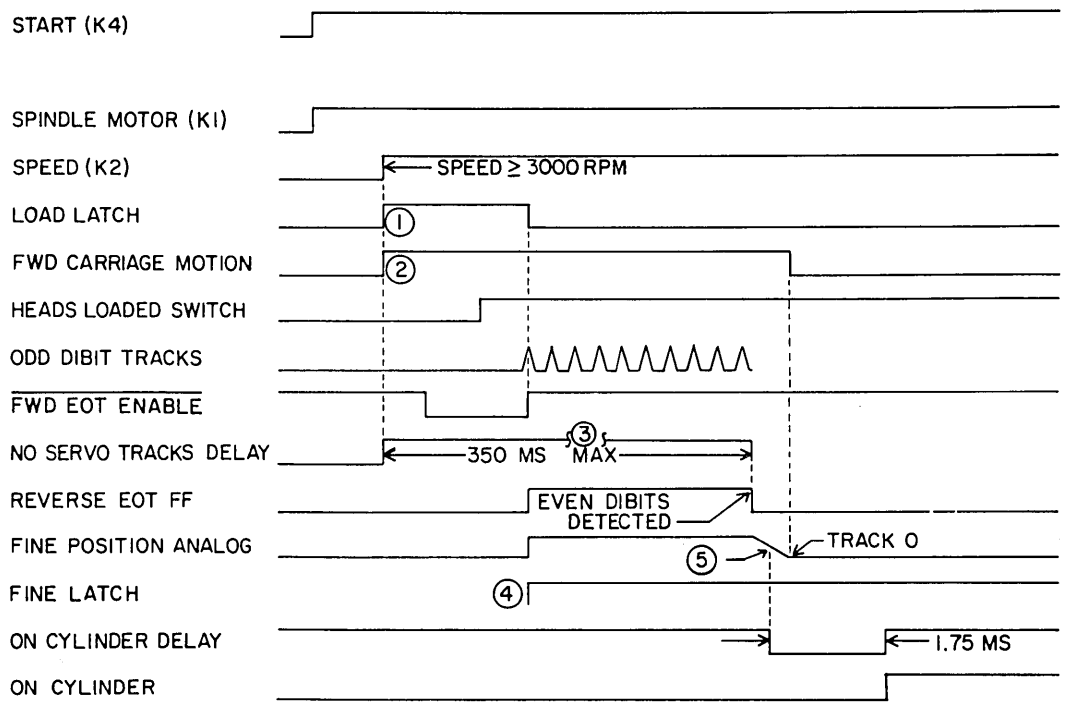


Figure 3-23. First Seek Flow Chart



NOTES:

1. LOAD LATCH CAUSES LOAD GATE TO APPLY A FORWARD SEEK VOLTAGE TO VOICE COIL SUMMING AMP. FINE GATE IS INHIBITED. CYLINDER ADDRESS REGISTER AND DIFFERENCE COUNTER ARE SET TO ZERO.
2. MOTION TO 18 mm (7 in) PER SECOND PROVIDED BY LOAD GATE UNTIL ODD DIBITS SET REVERSE EOT FF. MOTION CONTROL THEN PROVIDED BY FINE POSITION SIGNAL.
3. DIBITS MUST BE DETECTED WITHIN 350 MS OR FAULT IS SET. HEADS UNLOAD.
4. FINE LATCH IS JAMMED AT START OF LOAD UNTIL LOAD FF CLEARS, KEEPING COARSE OR FINE GATE DISABLED. WHEN LOAD FF CLEARS, T ≤ 1, AND FINE ENABLE IS HIGH, THE FINE LATCH WILL BE SET.
5. ON CYLINDER DELAY STARTS WHEN FINE POSITION SIGNAL <0.3 V (BJ501/507) OR 0.98 V (BJ701/781)

8J93C

Figure 3-24. First Seek Timing

If, for any reason, the dibit signals are not detected by the servo head within 350 ms after the Load latch is set, the RTZ latch is set and the carriage is retracted to the heads unloaded position. The FAULT indicator is then turned on. When the FAULT switch is pushed, the Fault latch is cleared and the carriage will attempt another seek to track 000. Once again if the dibit signals are not detected within 350 ms, the carriage will be retracted to the heads unloaded position and the FAULT indicator turned on.

Direct (Forward/Reverse) Seek

The Direct Seek function involves those operations that must be performed to move the read/write heads from their current track or cylinder location to the one specified by the controller. Refer to figures 3-25 and 3-26. Assume that the drive is at track 10 and awaiting further instructions. Assume also that the controller wishes to do a read or write operation at track 320. When the controller determines that the drive is ready, it sends the new cylinder address along with Tag 1. Raising Tag 1 places the old address and compliment of the new address in the adder. After the compare has been made, the difference counter is loaded with the number of tracks to go. When the controller drops Tag 1, the new cylinder address is loaded into the CAR, the seek direction is sent to the servo, and a Start Seek pulse is generated. (Refer to the servo circuit discussion for general seek functions).

The Forward Seek signal from the cylinder address adder gates the output of the position converter (Position Error signal) into the desired velocity function generator. (A Reverse Seek would have gated an inverted Position Error signal.) Since the seek length is greater than 128 (256) tracks, the position converter output is clamped at a fixed voltage. Start Seek clears the Fine latch, so the output of the desired velocity function generator is gated through the coarse gate to the summing amplifier. Since the carriage is stationary, no Velocity signal exists to balance the Position Error, and forward motion of the carriage begins.

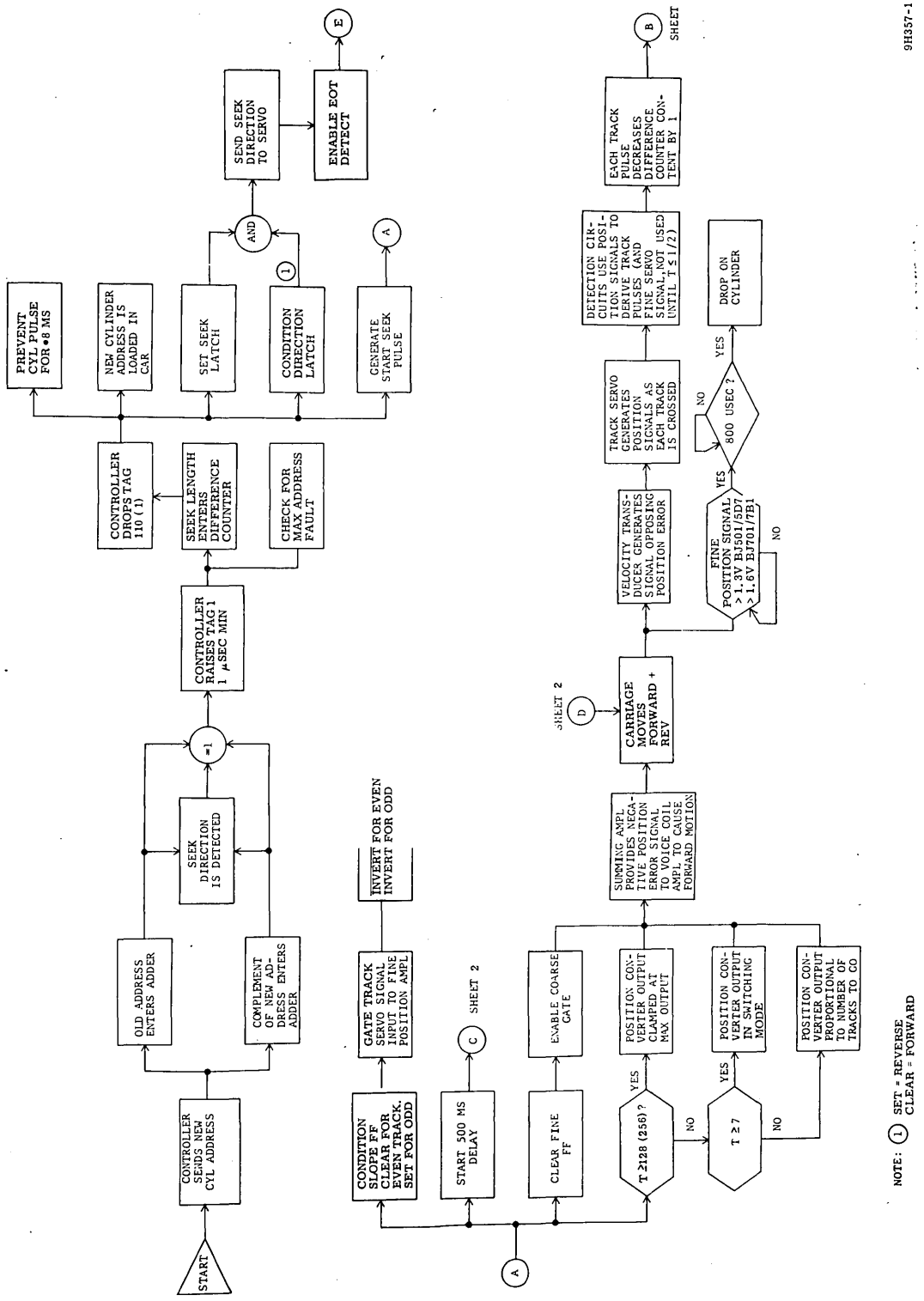


Figure 3-25. Direct Seek Flow Chart (Sheet 1 of 2)

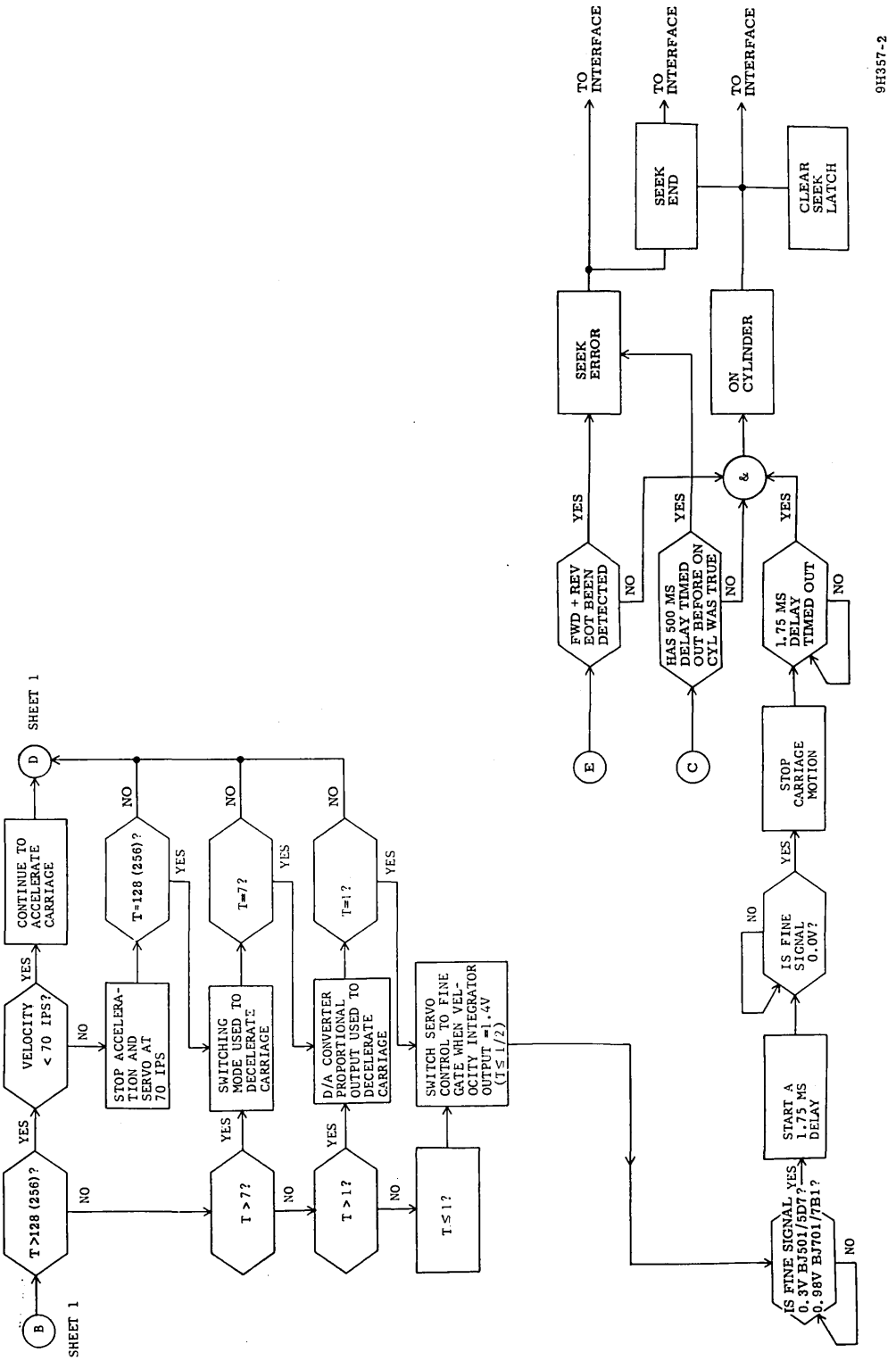
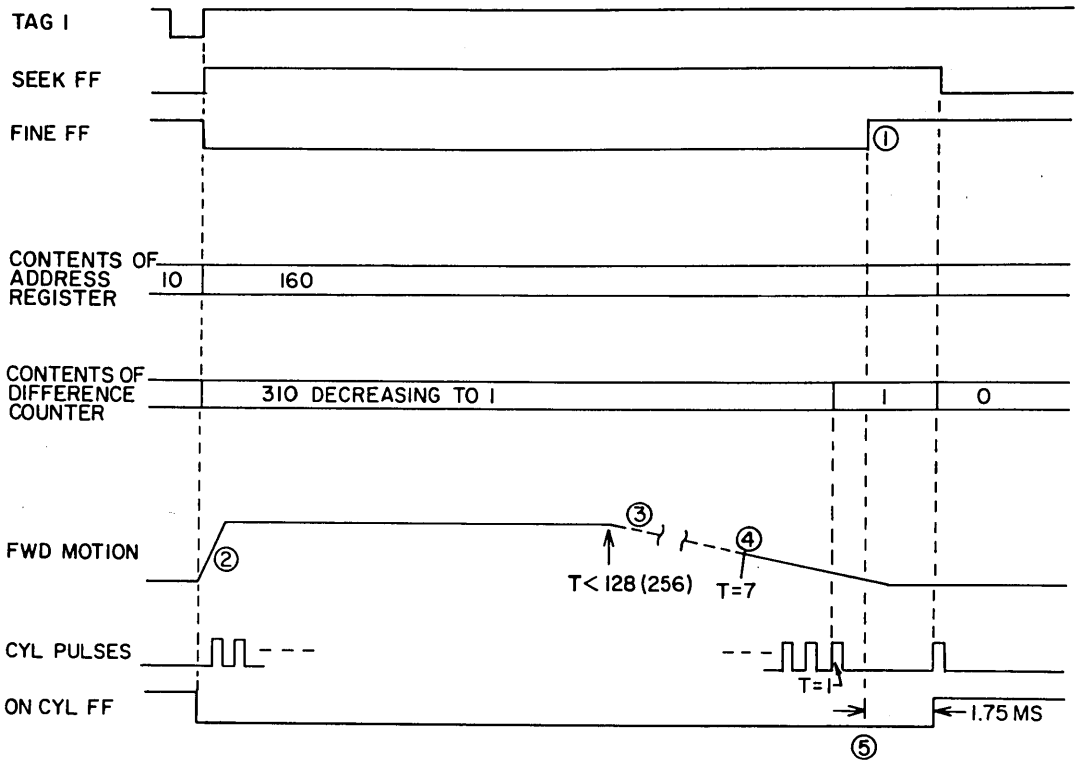


Figure 3-25. Direct Seek Flow Chart (Sheet 2 of 2)



NOTES:
① FINE FF SETS WHEN VELOCITY INTEGRATOR OUTPUT ≤ 1.4V AND T ≤ I.
② APPROXIMATELY 60 (200)(MIN) TRACKS REQUIRED TO ACCELERATE TO 180mm (70in) PER SEC.
③ SWITCHING MODE DECELERATES CARRIAGE FROM T = 128 (256) TO T=7
④ UNSWITCHED POSITION ERROR SIGNAL DECELERATES CARRIAGE DURING T ≤ 7 THROUGH T ≤ I.
⑤ ON CYLINDER DELAY STARTS WHEN FINE POSITION SIGNAL< 0.3V (BJ501/5D7) OR 0.98V(BJ701/7B1)
⑥ TIMES ARE NOT TO SCALE.

9H358

Figure 3-26. Direct Seek Timing

With the Position Error signal clamped at maximum, the power amplifier output (and voice coil positioner current) will be maximum and the carriage will continue to accelerate. As the carriage moves forward, outputs from the track servo head are processed to derive a cylinder pulse as each cylinder is crossed. Each pulse decreases the content of the difference counter by one. When acceleration has increased to the point where the Velocity Amplifier signal and the Position Error signal cancel each other, the Summing Amplifier Control signal drops off. During this phase, the carriage coasts, with the power amplifier providing only enough output voltage to compensate for the back emf of the moving voice coil positioner.

When the tracks remaining in the Seek are approximately 128(256), the position converter voltage clamp is disabled, and for the remainder of the Seek (except for the last track), the servo position error is derived from the D/A converter. As each track is crossed, the D/A converter output steps down by a precise and linear amount. So that the Position Error provided at the desired velocity function generator input is not stepped, the integrator on between each cylinder pulse. The resulting integrator sawtooth output is added to the D/A converter output and fills-in the area between the leading edges of each step.

As the Position Error signal begins to decrease, the servo system is changed to the switching mode. When the Position Error signal becomes less than the Velocity signal, current is applied to the voice coil in the maximum reverse direction until the velocity of the carriage slows down below the instantaneous position error value. The current to the voice coil is then turned off and the carriage coasts under its own inertia while the difference counter continues to count down (decreasing the Position Error signal). If the carriage velocity becomes too high for existing Position Error signal, a maximum reverse current is again applied until the velocity slows down below the instantaneous position error value.

At T=7, the switching mode logic is disabled and the total summing amplifier output is used to decelerate the carriage to keep the Velocity signal/Position Error signal difference to zero.

When the counter indicates one track to go the desired destination, the Integrated Velocity signal is reset by the regular cylinder pulse. The Integrated Velocity, which indicates distance, brings up Fine Enable when about one-half track of travel remains. This sets the Fine latch which, in turn, enables the Fine gate and disables the Coarse gate.

Desired velocity no longer has a effect; the position error is supplied by the Fine Servo signal. This signal is the track servo signal from the track servo circuit. The amplitude of the signal is proportional to the distance between current head position and the desired cylinder.

Since the desired destination is track 320, bit 0 of the Address register is "0". This causes the Slope FF to be cleared. As a result, the track servo signal is inverted to form the Fine Servo signal. In all seeks, the Fine Servo signal is phased to be opposite to the velocity signal. As the carriage approaches track 320, the Fine Servo signal approaches 0 V. The summing amplifier responds to this decrease in amplitude by decelerating the carriage so that the sum of the Velocity signal always just cancels the Fine Servo signal. At track 320, both Velocity and Position Error equal zero, and all motion stops with the servo circuit at null. Only a Position Error will cause additional motion. When the Fine Servo signal is less than 0.3 V(0.98 V), a delay of 1.75 ms starts. The On Cylinder signal occurs when the delay times out.

Certain conditions indicate that the seek was not completed successfully. This is a Seek Error. These conditions are:

1. On Cylinder not generated within 500 ms from the start of the seek.

2. Forward EOT sensed. The carriage returns to cylinder 411(822) and remains there.

3. Reverse EOT sensed. The carrige returns to cylinder 000 and remains there.

4. If the carriage drifts off cylinder enough for the fine position signal to be greater than about 1.61 volt for more than 800 µs, the Seek Error FF sets. In addition, if the drive is reading or writing, the Fault FF also sets. Write gate is disabled. The unit will not accept any commands until the error is cleared manually.

5. Command seek to track greater than 411 for 40 MB drives or 822 for 80 MB drive.

All of these conditions require an RTZ command to clear the error. RTZ clears Seek Error and returns the drive to cylinder 000.

Reverse seeks function in an identical manner, except that all phases and polarities are reversed. Total seek times for forward or reverse seeks are identical for seeks of equivalent lengths.

Return To Zero Seek (RTZ)

The RTZ function allows a controller to return the heads to track 000 when a Seek Error occurs. See figures 3-27 and 3-28 for the RTZ seek flow chart and timing diagram.

The RTZ pulse sets the RTZ latch and clears the Seek Error FF. This enables the RTZ gate, resulting in a bias voltage that forces an average 180 mm (7 in) per second reverse motion of the carriage. When the carriage passes cylinder 000, no more even dibits are detected. This is the Reverse EOT area. The lack of even dibits inhibits cylinder pulses, allowing the velocity integrator in the track servo circuit to reach a negative output in excess of 1.4 V. This, along with odd dibits, sets the Reverse EOT FF. The integrator is reset, but reverse motion continues unimpeded.

After an additional reverse motion of about two to four tracks, the velocity integrator output again exceeds 1.4 V. The RTZ latch is cleared while the Load latch sets.

The Load latch activates circuitry to produce an average forward 180 mm (7 in) per second access. The carriage continues forward with the servo head searching for the prerecorded positive dibit signals on the track servo surface. When the reverse EOT area (all odd, or positive, dibits) is sensed, the Load latch is cleared, the Reverse EOT FF is set, and the Fine gate and latch are enabled. The carriage now moves under control of the Fine Position analog signal. When even dibits are detected (approaching track 000), the Fine Servo signal decelerates the carriage.

The drive sends On Cylinder to the controller 1.75 ms after the Fine Position signal is less than 0.3 V(0.98 V). The carriage stops when the Fine Position signal is 0 V. The sequence must be completed within 500 ms after RTZ seek initiation, or else the Seek Error FF is set.

The RTZ seek function is also used during normal power off sequencing. If the START switch is pressed by the operator, the control interlock opens. This raises the Unload Heads signal in the drive logic. The RTZ latch sets to initiate a 180 mm (7 in) per second reverse seek.

This time, however, the EOT Enable circuit is disabled so that the velocity integrator signal has no effect. In turn, the Load latch is disabled. Reverse motion continues until the heads unload.

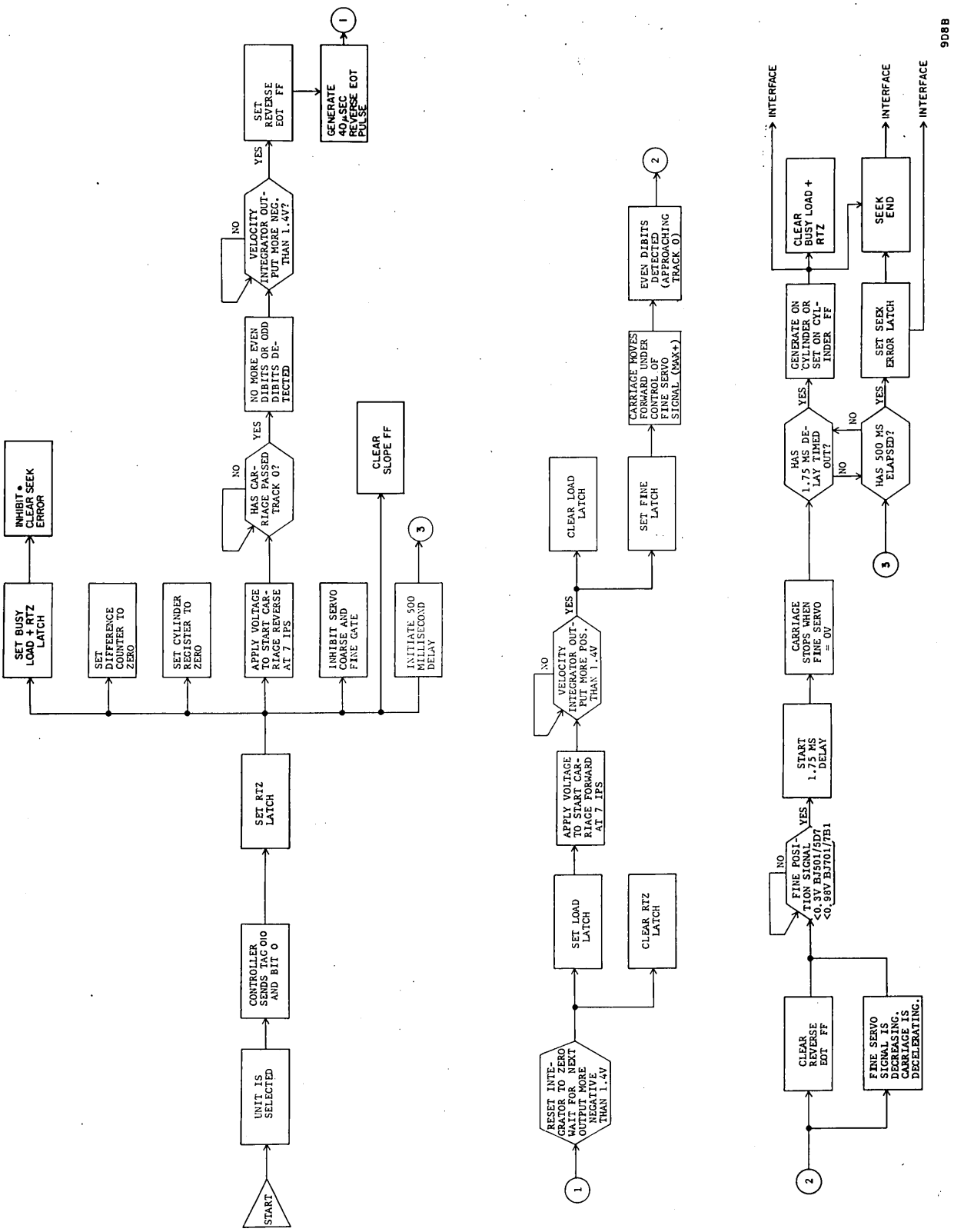
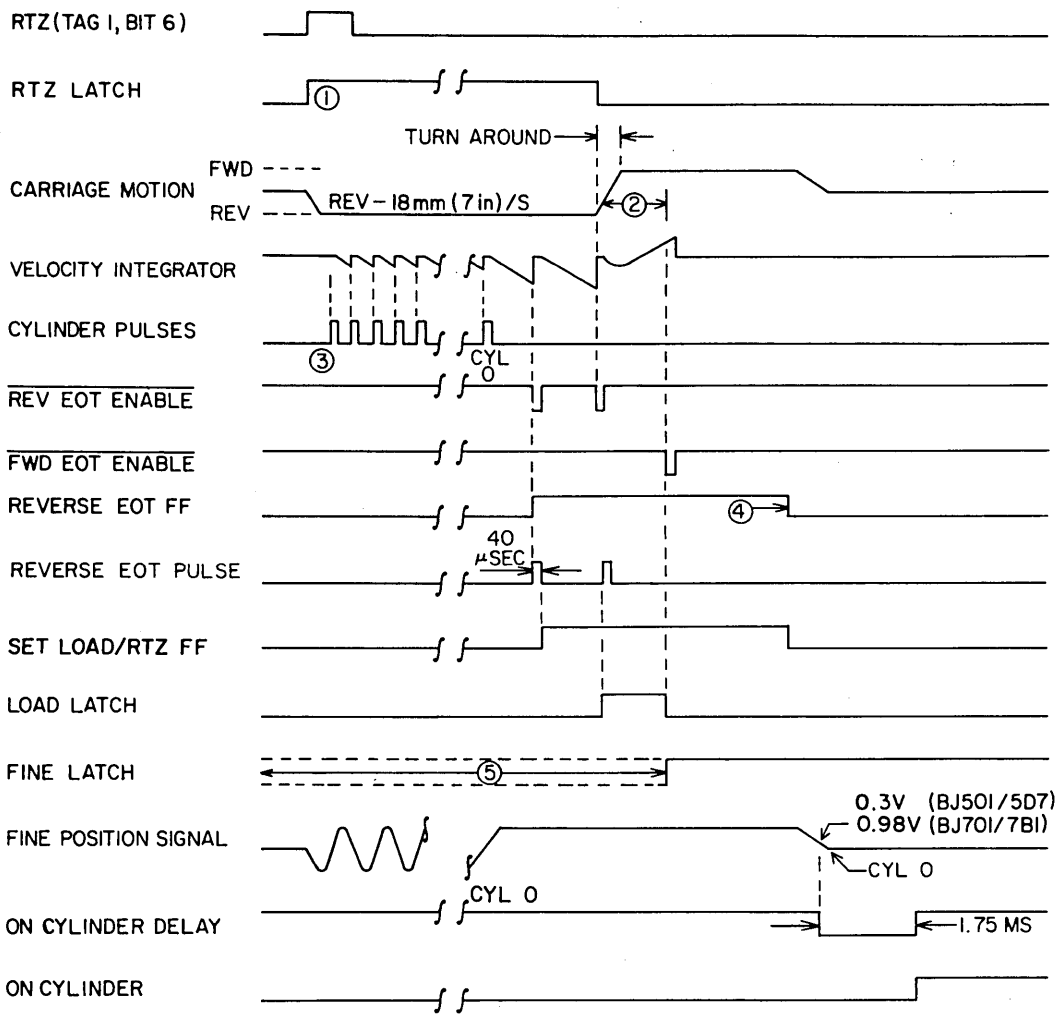


Figure 3-27. Return to Zero Seek Flow Chart



NOTES:

① RTZ LATCH CAUSES RTZ GATE TO APPLY NEG VOLTAGE (SEEK REV) TO VOICE COIL SUMMING AMPL. COARSE AND FINE GATES INHIBITED. CYLINDER REGISTER SET TO ZERO AND DIFFERENCE COUNTER SET TO ZERO.

② FWD MOTION TO 18 mm (7in) PER SECOND PROVIDED BY LOAD GATE, IT PROVIDES + (SEEK FWD) TO SUMMING AMPL. WHEN LOAD LATCH CLEARS, MOTION CONTROL PROVIDED BY FINE SERVO SIGNAL.

③ CYLINDER PULSES RESTART VELOCITY INTEGRATOR. THEY DO NOT AFFECT DIFFERENCE COUNTER.

④ REVERSE EOT FF CLEARED BY FIRST EVEN DI BITS. (APPROACHING TRACK 0).

⑤ BOTH OUTPUTS ARE HIGH WITH EITHER RTZ OR LOAD LATCH SET. THIS DISABLES COARSE AND FINE GATES. FF THEN SET BY T ≤ 1 AND FINE ENABLE.

8J97A

Figure 3-28. Return to Zero Seek Timing Diagram

The RTZs function transfers automatically to the heads unloaded condition if dibits are lost for more than 350 ms.

End Of Travel Detection

The end of travel circuit determines when the heads are positioned outside of the normal data cylinders. This function is used during Load and RTZ sequences and to indicate an error condition during a seek.

Forward EOT indicates that the heads are within the inner guard band. Assume that the controller has commanded a forward seek and the positioner proceeds past cylinder 411 (822). Sequencing is as follows:

1. As the heads move forward, the velocity integrator output produces a signal proportional to velocity (the input to the integrator) and time (provided by the integrator capacitor). The input, which is a positive-going ramp during forward seeks, represents distance travelled. It is pulled back to ground by cylinder pulses. As long as cylinder pulses are generated, the output cannot reach an effective value.

2. After track 411(822) is passed, no more odd dibit tracks are detected, resulting in no more cylinder pulses to reset the velocity integrator. When the output exceeds approximately 1.4 V (2 tracks), Forward EOT Enable comes up. This signal, in conjunction with the even dibits picked off of the inner guard band, sets the Forward EOT FF.

   With the Forward EOT FF set:

   a. Seek Error FF sets to return Seek Error to the controller.

   b. Seek FF (set at the start of the seek) is cleared.

   c. The difference counter is set to 000 (T=0).

   d. Fine Enable is raised within the servo circuit.

   e. Because of c and d the Fine Gate, in the servo circuit, is enabled.

   f. The Slope FF is cleared to indicate a seek to an even-numbered cylinder.

4. The track servo, functioning as the fine position analog signal in the servo circuit, is gated to the servo summing amplifier via the Fine Gate. The signal is at a maximum amplitude because only even dibits are being sensed. This error voltage causes the positioner to drive in reverse until the servo signal drops to zero; the heads are then positioned at cylinder 411(822).

5. An RTZ command is required to clear the Seek Error status.

Reverse EOT indicates that the heads are positioned over the outer guard band. If this condition occurs during regular reverse seeks, the Reverse EOT FF sets. This initiates an automatic Load sequence to return the actuator to cylinder 000.

MACHINE CLOCK

GENERAL

The machine clock circuits generate the clock signals necessary for drive operation. These circuits are divided into two areas (1) Servo Clock Multiplier and (2) Write Clock Multiplier. These are both explained in the following discussions.

SERVO CLOCK MULTIPLIER

The servo clock multiplier circuits (refer to figure 3-29) generates clock pulses used by the sector detection, Index detection and the Read PLO circuits. It also generates the 9.67 MHz Servo Clock signal that is sent to the controller.

The main element in the servo clock multiplier circuit is the phase lock loop. This loop consists of a phase and frequency detector, error amplifier, voltage controlled oscillator and a divide by 12 circuit. The function of the loop is to adjust itself until its output is identical in phase and frequency to its input.

The input to the loop consists of the dibit signals from the track servo circuit (refer to discussion on Position Feedback Generation). The nominal frequency of these signals is 806 kHz; however, their actual frequency is a function of and varies directly with disk pack speed. This means that the output of the loop will also vary with disk pack speed.

The phase and frequency detection circuit makes the comparison between the input dibits and the output of the loop.

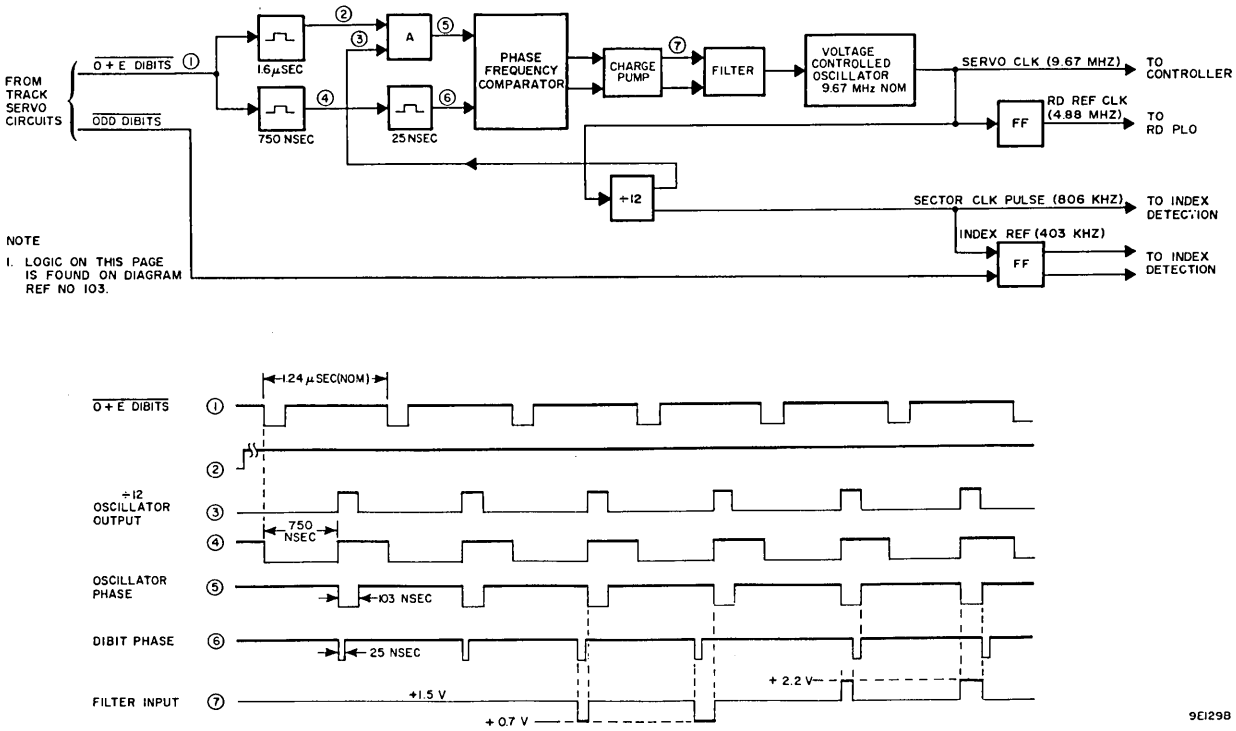


Figure 3-29. Servo Clock Multiplier

The input dibits are applied via two retriggerable multi-vibrators. One of these multi-vibrators provides a 750 ns (approximate) output pulse which is then fed through a pulse forming circuit to provide a 25 ns input pulse for the phase and frequency detector. These pulses vary at the dibit frequency. The other multi-vibrator has a 1.6 μs output which is used to enable the feedback pulses from the loop output to the input of the phase and frequency detector. The 1.6 μs pulse is longer than the period of the nominal dibit frequency (806 kHz); therefore, the feedback pulses are continuously gated as long as dibits are present.

The outputs from the detector are fixed amplitude pulses which are a function of the time (or phase) difference between the positive going edges of the two inputs (refer to figure 3-29).

These outputs are applied to the error amplifier which integrates them and generates a voltage proportional to the phase difference between them. This voltage is used as a control voltage for the Voltage controlled oscillator.

The control voltage causes the VCO frequency to vary in the direction necessary to eliminate the phase or frequency difference between the input and output of the loop. The VCO output is then divided by 12, by the divide by 12 circuit, and fed back to the loop input.

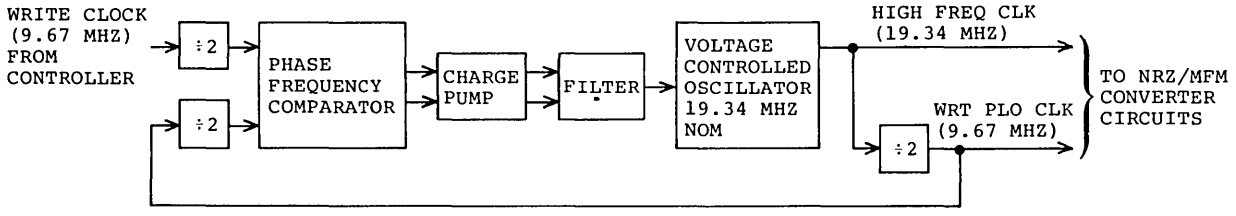
When the VCO output is 9.67 MHz, the feedback provided by the divide by 12 circuit will be 806 KHz and the loop will be synchronized.

Both the 9.67 MHz and 806 kHz signals are divided by two thus producing 4.84 MHz and 403 kHz signals. All four of these frequencies are used by the drive as shown on figure 3-29.

WRITE CLOCK FREQUENCY MULTIPLIER

The write clock frequency multiplier circuit (refer to figure 3-30) generates the 19.34 MHz and 9.67 kHz signals used during write operations.

This circuit consists mainly of a phase lock loop and operates essentially the same as the servo clock multiplier. However, the input to the write clock multiplier is the 9.67 MHz Write Clock signals from the controller. The phase lock loop synchronizes to these signals and provides the 19.34 MHz and 9.67 MHz outputs. These outputs are used by the NRZ and MFM converter and Write Compensation circuits during write operations.



NOTE
1. LOGIC ON THIS PAGE IS FOUND ON DIAGRAM REF. NUMBER 104.

9E130

Figure 3-30. Write Clock Multiplier

HEAD OPERATION AND SELECTION

GENERAL

Information is recorded on and read from the disk by the read/write heads (refer to figure 3-31). The drive has 5 read/write heads, one for each data recording surface in the disk pack. For this reason, before a read or write can be performed, the controller must command the drive to select the head located over the disk surface where the data is to be read or written.

The following discusses how the heads read and write the data and also how the desired head is selected.

HEAD FUNCTIONAL DESCRIPTION

Data is written by passing a current through a read/write coil within the selected head. This generates a flux field across the gap in the head (figure 3-32). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a North pole and a South pole. The writing process orients the poles to permanently store the direction of the flux field as

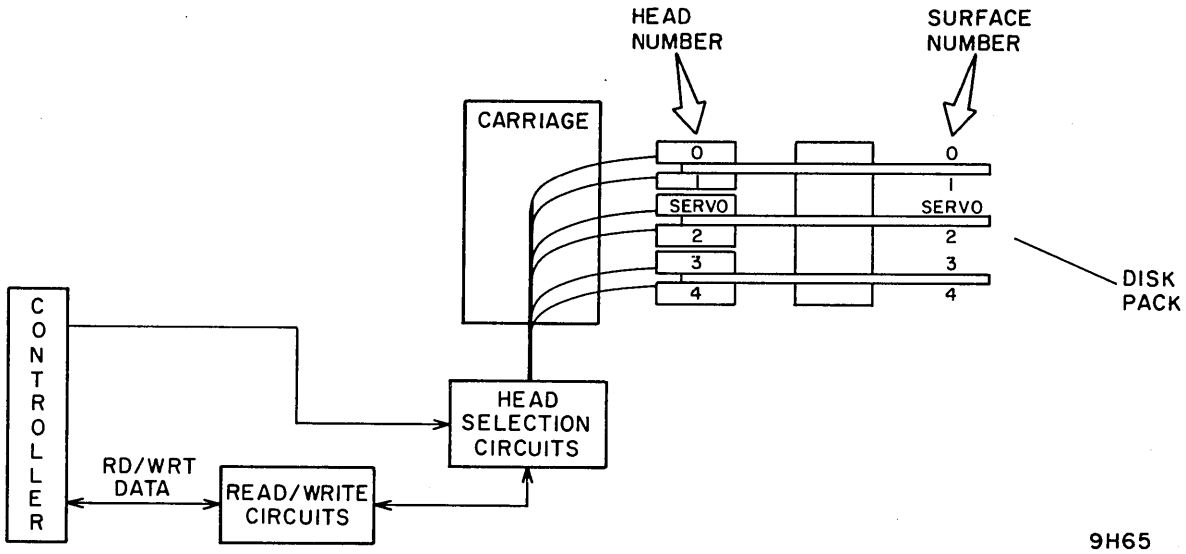
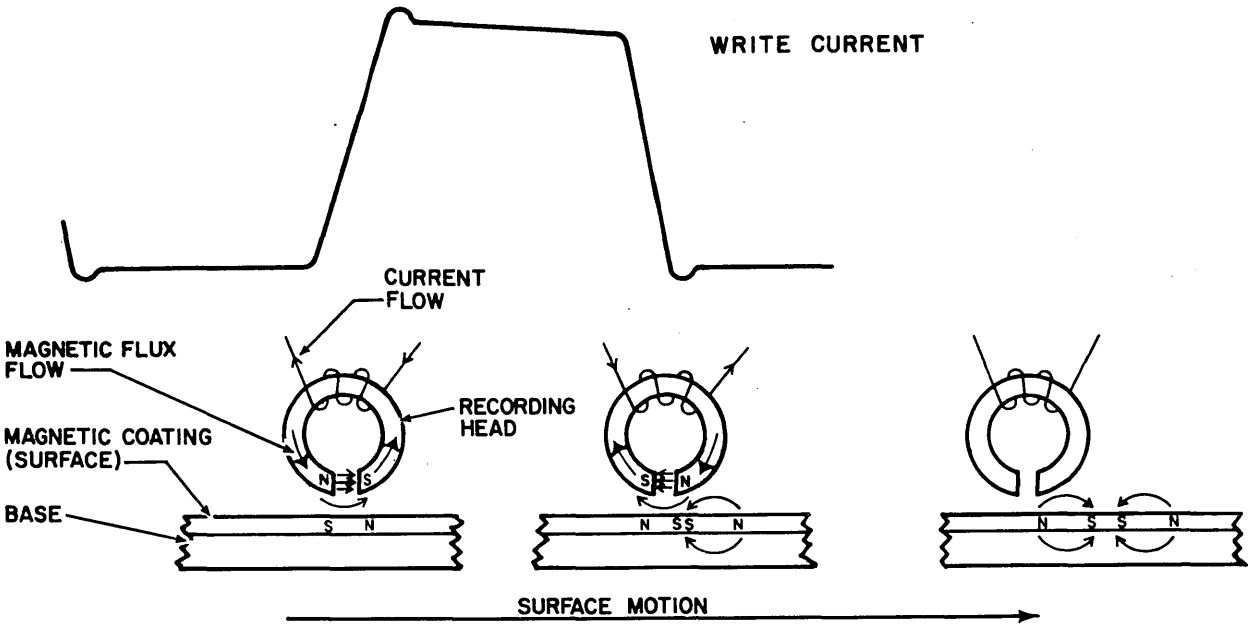


Figure 3-31. Read/Write Heads



NOTE: RELATIVE HEAD TO SURFACE MOTION, RECORDING (WRITE OPERATION) 7S17A

Figure 3-32. Writing Data

the oxide passes beneath the head. The direction of the flux field is a function of Write current polarity while its amplitude depends on the amount of current: the greater the current, the more oxide particles that are affected.

Information (data) is written by reversing the current through the head. This change in current polarity switches the direction of the flux field across the gap. The flux change defines a data bit.

Erasing old data is accomplished by writing over any data which may already be on the disk. The write current is zoned in four current zones to ensure proper saturation level for best head resolution (refer to discussion on Write Current Control). The write current is maximum on the outer tracks and progressively decreased for inner tracks.

During a read operation, disk motion beneath the head causes the stored flux to induce a voltage in the head windings (refer to figure 3-33). This voltage is analyzed by the read circuit to define the data recorded on the disk. Each flux reversal (caused by a current polarity change while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

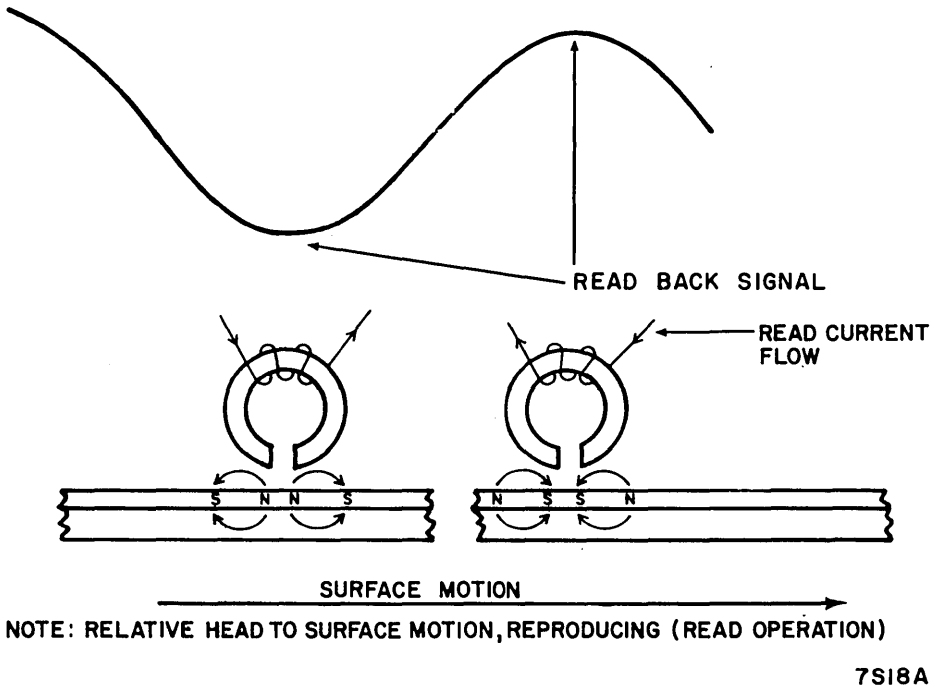


Figure 3-33. Reading Data

HEAD SELECTION

A head must be selected before a read or write operation can be performed. Head selection starts when the controller sends the drive a Head Select tag and a head address. The head address is sent on Bus Out bits 5 through 7).

The Head Select tag gates the address into the Head Address register. This address is then decoded to a Head Enable signal (0 through 4 depending on Bus Out bits 5 through 7). This signal then enables the head current drive associated with the addressed head and allows the head to conduct as shown on figure 3-34.

If more than one head is selected, a fault is indicated (refer to discussion of Fault and Error Conditions).

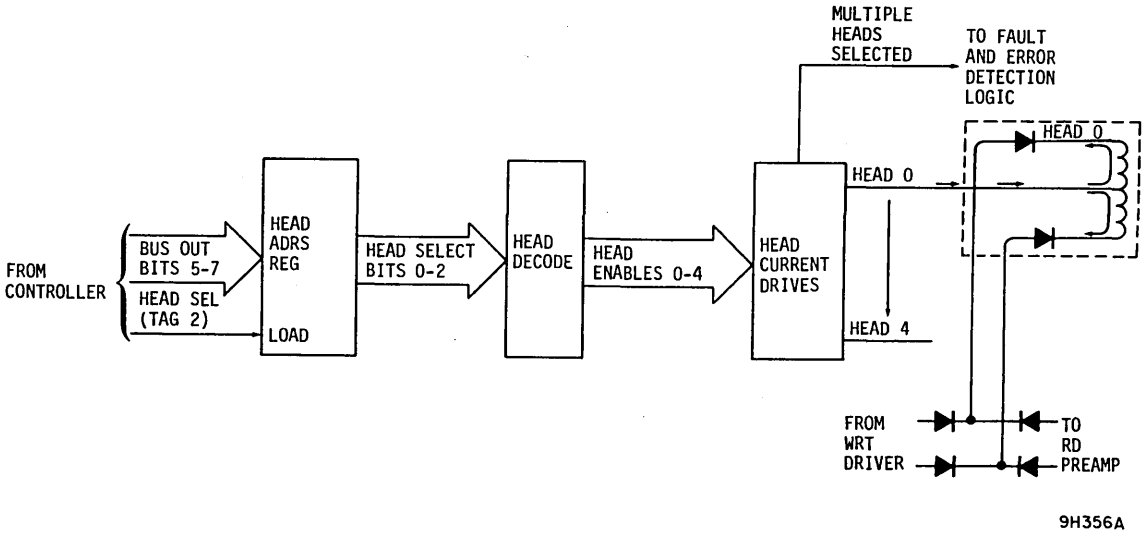


Figure 3-34. Head Select Circuits

TRACK ORIENTATION

GENERAL

After finding the proper cylinder and selecting a head, the controller still may not read or write data until it determines the head is over that part of the data track where the data is to be read or written.

The controller accomplishes this by using the Index and Sector signals which are generated by the drive. How the drive generates these signals is explained in the following.

INDEX DETECTION

Each track on the servo disk contains a pattern of missing dibits referred to as the Index pattern (refer to discussion on Servo Zone). When the drives Index Detection circuits (refer to figure 3-35) detect this pattern, they generate a 2.5 µs Index signal. The Index signal indicates, both to the drive and controller, the logical beginning of a track.

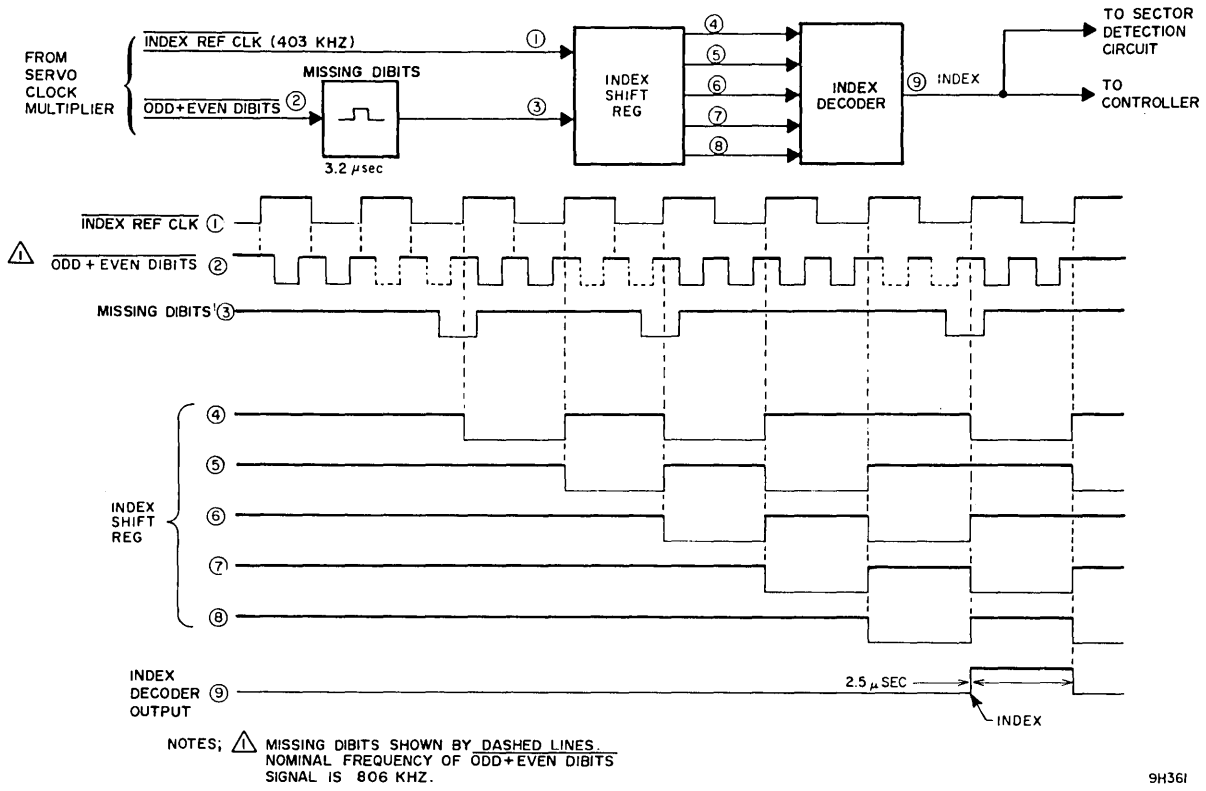


Figure 3-35. Index Detection - Logic and Timing

The Odd Or Even Dibits signal provides the data necessary to actually detect the missing dibit pattern. This signal is derived from the dibits detected from the disk and has a nominal frequency of 806 KHz (refer to discussion on Odd/Even Dibits Clock Generation). Because this signal is derived from the dibits, whenever a dibit is missing an Odd Or Even Dibits pulse is also missing.

Detection of missing dibits is done by the Missing Dibits one shot. This one shot is triggered by the Odd or Even Dibits signals and will not time out as long as dibits are present. However, if two or more consecutive dibits are missed the one shot times out. The output of the Missing Dibits one shot provides the data input for the first stage of the Index Shift register.

The Index Shift register loads the output of the Missing Dibits one shot into its first stage (and also performs its shift) each time a 403 KHz Index Reference Clock pulse occurs. When the one shot is in a triggered state (indicating dibits were present) a one is loaded into the register. However, when the one shot is timed out (indicating two or more dibits were missing) a zero loads into the register.

The contents of the Index shift register are continuously compared to the index pattern by the Index decoder and when the shift register contains the pattern indicating Index has occurred, the Index Decoder generates an Index signal. The missing dibit pattern associated with index and the pattern contained in the shift register when index has occurred are shown on figure 3-35.

In summary, the Index detection circuit contains three main elements:

- Missing Dibits one shot - Detects the missing dibits in the Index pattern.
- Index Shift register - Accumulates the dibit pattern so that it can be compared with the pattern occurring during Index.
- Index Decoder - Compares the contents of the Index Shift register with the Index pattern and generates an output signal when Index is detected.

These elements work in conjunction with the two input signals (Odd Or Even Dibits and 403 kHz Index Reference Clock) to produce the Index signal. The Index signal is sent to the controller and is also used to reset the drives sector detection circuitry.

SECTOR DETECTION

General

The sector circuits generate signals which are used by the system to determine the angular position of the heads with respect to Index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disk pack. The Sector pulses logically divide the disk into areas called sectors.

The following describes how the sector pulses are generated and also describes rotational position sensing (RPS).

Sector Pulse Generation.

The Sector pulses are generated by the Sector Bit counter which causes a pulse to be generated each time it indicates its maximum value of 4095 (refer to figure 3-36).

One counter is incremented by the 806 kHz clock pulses. These clock pulses are derived from the servo track dibit signals (refer to discussion on track servo circuit) and exactly 13,440 clock pulses occur during each revolution of the disk pack.

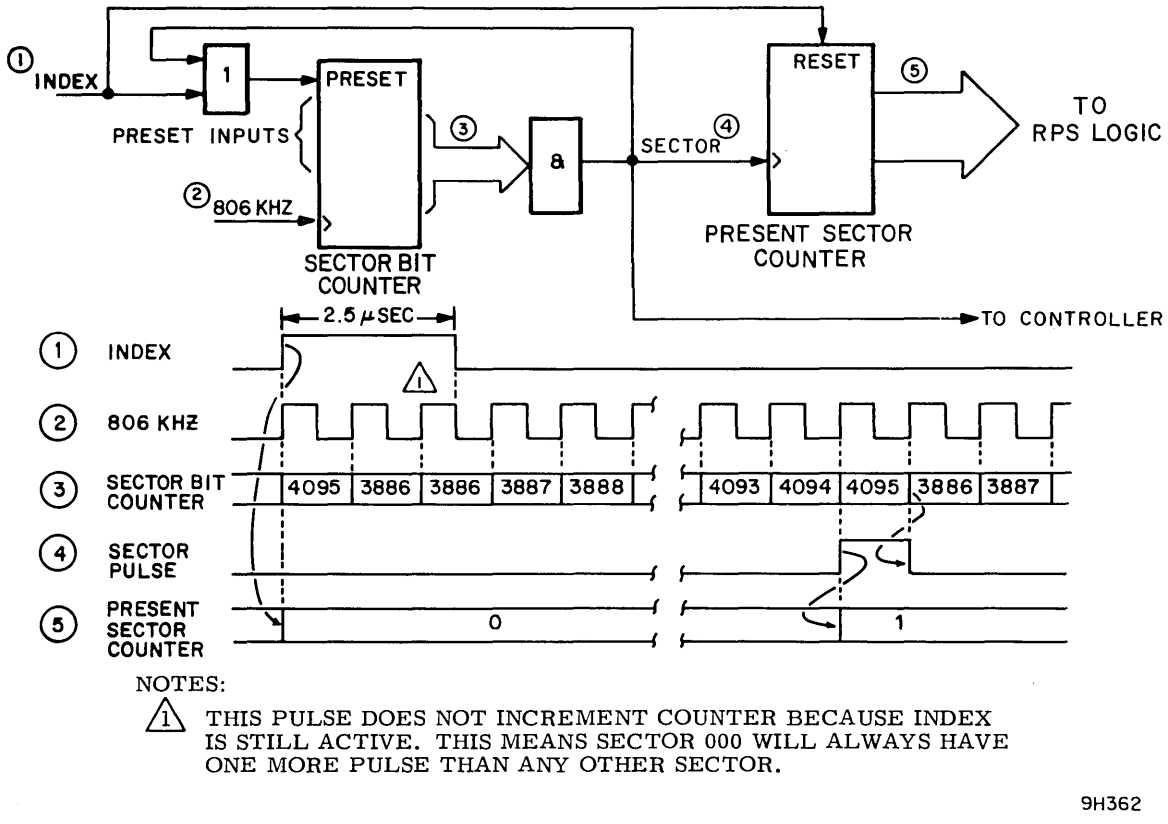


Figure 3-36. Sector Detection - Logic and Timing

The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution. This is done by presetting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors, the counter would have to count 210 clock pulses in each sector (13,440 divided by 64) and the counter would be preset to 3886. In this case the counter starts at 3886 and increments each clock time until it reaches the maximum count of 4095. Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (210) presets the counter back to 3886 (thus disabling the Sector pulse) and the counter begins the next sector. The 3886 is obtained by subtracting 210 from 4096 which is the total number of clock pulses the counter is capable of counting (0 through 4095 = 4096).

The sector length is varied by changing the value of the preset inputs to the counter. This is done by rewiring the sector plug located on the logic chassis backpanel. Refer to section 1 of the maintenance manual for details regarding the rewiring of the sector plug.

The Sector pulses are sent to the controller and are also used to increment the Present Sector counter.

The Present Sector counter counts the Sector pulses (starting at Index) and therefore always indicates the number of the sector the heads are currently over. This count is used by the rotational position sensing circuits.

Rotational Position Sensing (RPS)

The RPS operation consists of the drive raising its Interrupt line to the controller each time it reaches a specific sector. The sector is specified by the controller at the start of the operation. The Interrupt line is raised each time the sector is detected (even if the drive is deselected) unless the RPS is disabled. The purpose of the function is to free the system for other operations while the drive searches for the sector.

RPS is enabled by a Tag 101 (Target Register) with Bus Out bit 0 true. This command causes the drive to set the RPS Enabled latch and enable the contents of Bus Out bits 1 through 7 to the Target mux (refer to figure 3-37). Bus Out bits 1 through 7 contain the number of the target sector at which the drive will raise the Interrupt line.

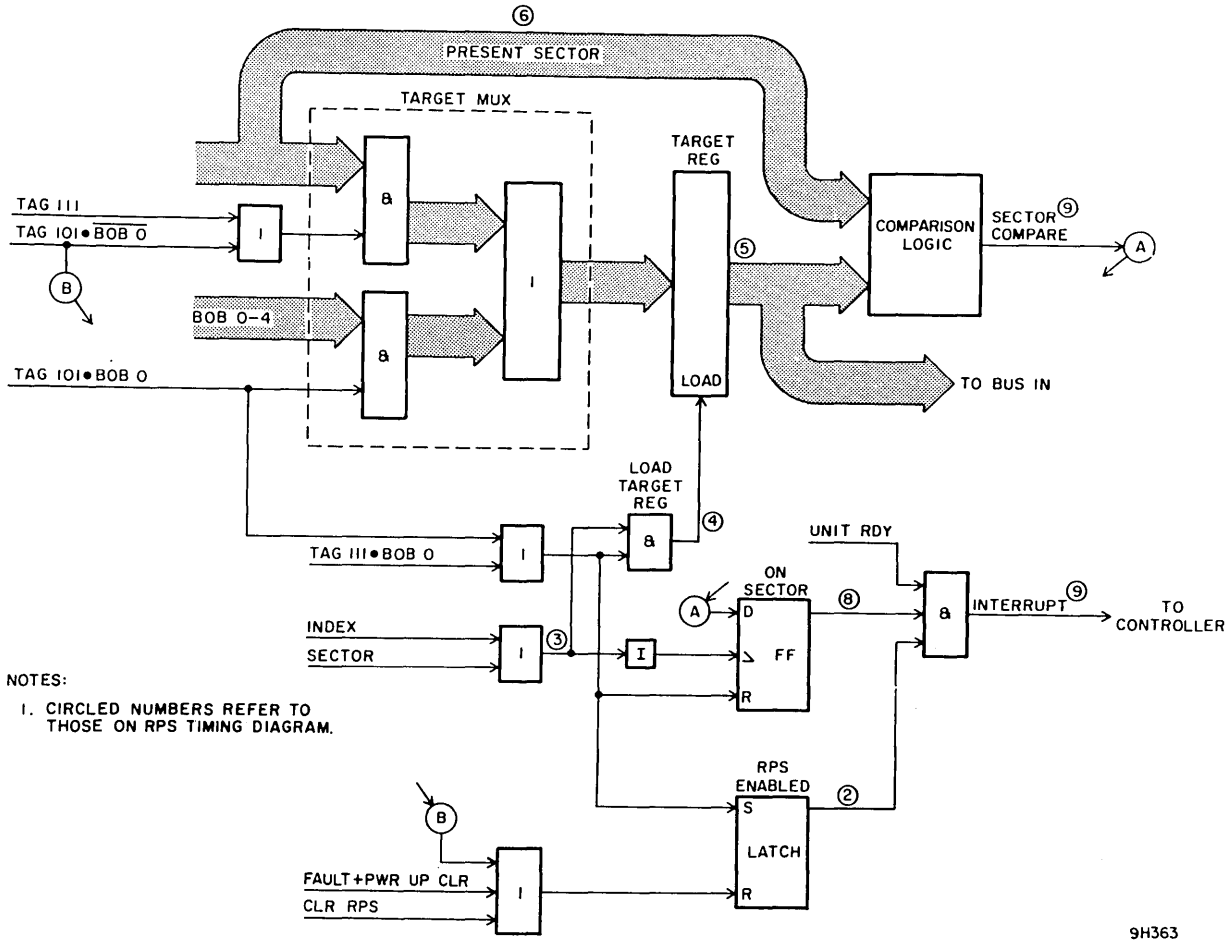


Figure 3-37. RPS Logic

The Target register is loaded with the target sector at the next Sector or Index pulse following the receipt of the Target register command (refer to figure 3-38).

As the disk rotates, the Sector pulses continue to increment the present sector count and this count is compared with the contents of the Target register. When the two are equal, the drive has reached the target sector and the Sector Compare signal goes true. This sets the Enable Interrupt FF which, in turn, enables the Interrupt signal to the controller. The Interrupt signal remains active until the end of the target sector. The drive raises the Interrupt line each revolution (even if the drive is deselected until the RPS is disabled via a Clear RPS command (Tag 010 and Bus Out bit 5).

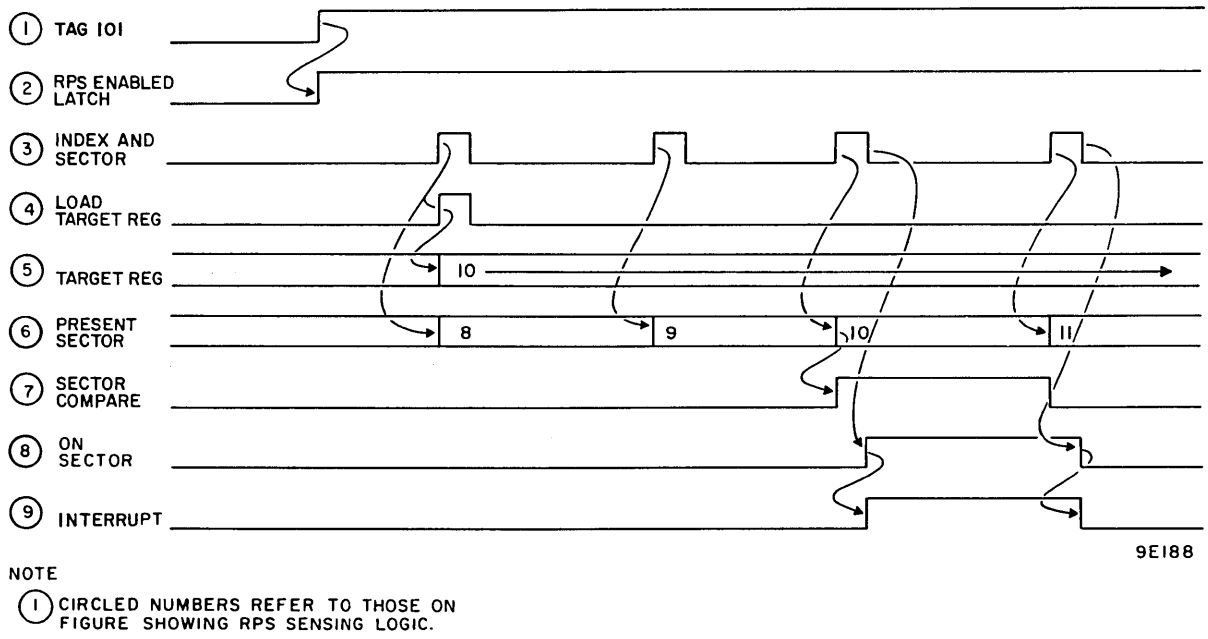


Figure 3-38. Rotational Position Sensing Timing

The RPS circuits are also used to store the number of the sector where a read or write command is received. This function is initiated when the drive receives a Control tag (111) with Bus Out bit 0 true. This causes the drive to load the Target register with the present sector count which remains in the Target register until a Control tag (with Bus Out bit 0 true) loads another number into it. The controller can retrieve the sector number via a Target Register tag with Bus Out bit 0 false.

READ/WRITE FUNCTIONS

GENERAL

When the drive is on cylinder, has a head selected, and has located the proper place on the data track, it is ready to perform a read or write operation. The controller initiates a read or write operation by sending the drive a Control tag (111) and the proper bus out bits (refer to discussion on interface functions).

During a read operation, the drive recovers data from the disk and transfers it to the controller. During a write operation, the drive receives data from the controller and records it on the disk.

Figure 3-39 is a block diagram of the read/write circuits. The remainder of this discussion describes the read/write circuits and is divided into the following areas.

WRITE OPERATIONS

General

Write circuit operation is initiated by a Control tag (111) with BOB 1 active true. This allows the drive to start processing serial NRZ data received from the controller. The write data is received via the bidirectional Read/Write data line and is first sent to the NRZ to MFM converter/write compensation circuits. These circuits convert the data to MFM and also compensate it for problems caused by variations in data frequency. The compensated data is then processed by the write drive circuits and written on the disk.

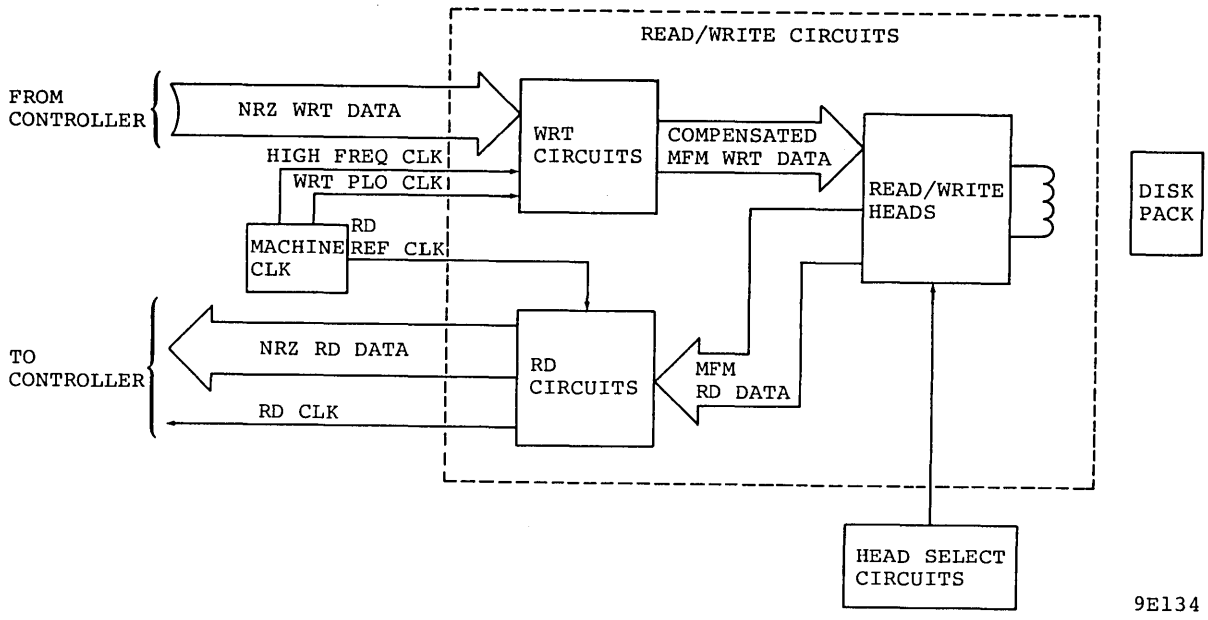


Figure 3-39. Read/Write Circuits Block Diagram

Figure 3-40 shows the write circuits and table 3-7 briefly explains their function.

The following paragraphs describe MFM recording, which is the technique used for recording data on the disk, and also explains how the drive circuits function during a read or write operation.

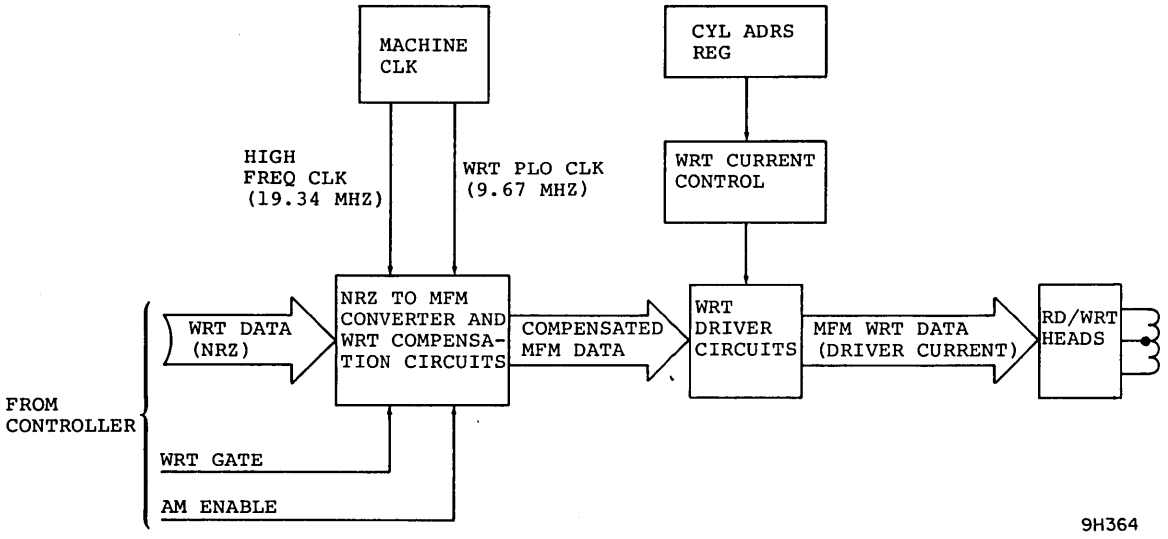


Figure 3-40. Write Cricuits Block Diagram

Principles Of MFM Recording

In order to define the binary dibits stored on the pack, the frequency of the flux reversals must be carefully controlled. Several recording methods are available; each has its advantages and disadvantages. This unit uses the Modified Frequency Modulation technique.

TABLE 3-7. WRITE CIRCUIT FUNCTIONS

Circuit	Function
NRZ to MFM Converter and write Compensation Circuits	Converts the NRZ data from the controller to MFM data and also compensates the data for problems caused by variations in the write data frequency.
Write Driver Circuits	Uses the MFM data to produce the current necessary to record data on the disk.
Write Current Control	Reduces the write current amplitude as the heads move from the outer tracks to inner tracks. This assures that the correct amount of current will be used as the circumference of the cylinders decrease.

The length of time required to define one bit of information is the cell. Each cell is nominally 103 ns in width. The data transfer rate is, therefore, nominally 9.677 MHz.

MFM defines a "1" by writing a pulse at the half-cell time (figure 3-41). A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is Clock; however, Clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell.

The rules for MFM recording may be summarized as follows:

- There is a flux transition for each "1" bit at the time of the "1".
- There is a flux transition between each pair of "0" bits.
- There is no flux transition between the bits of a "10" or "01" combination.

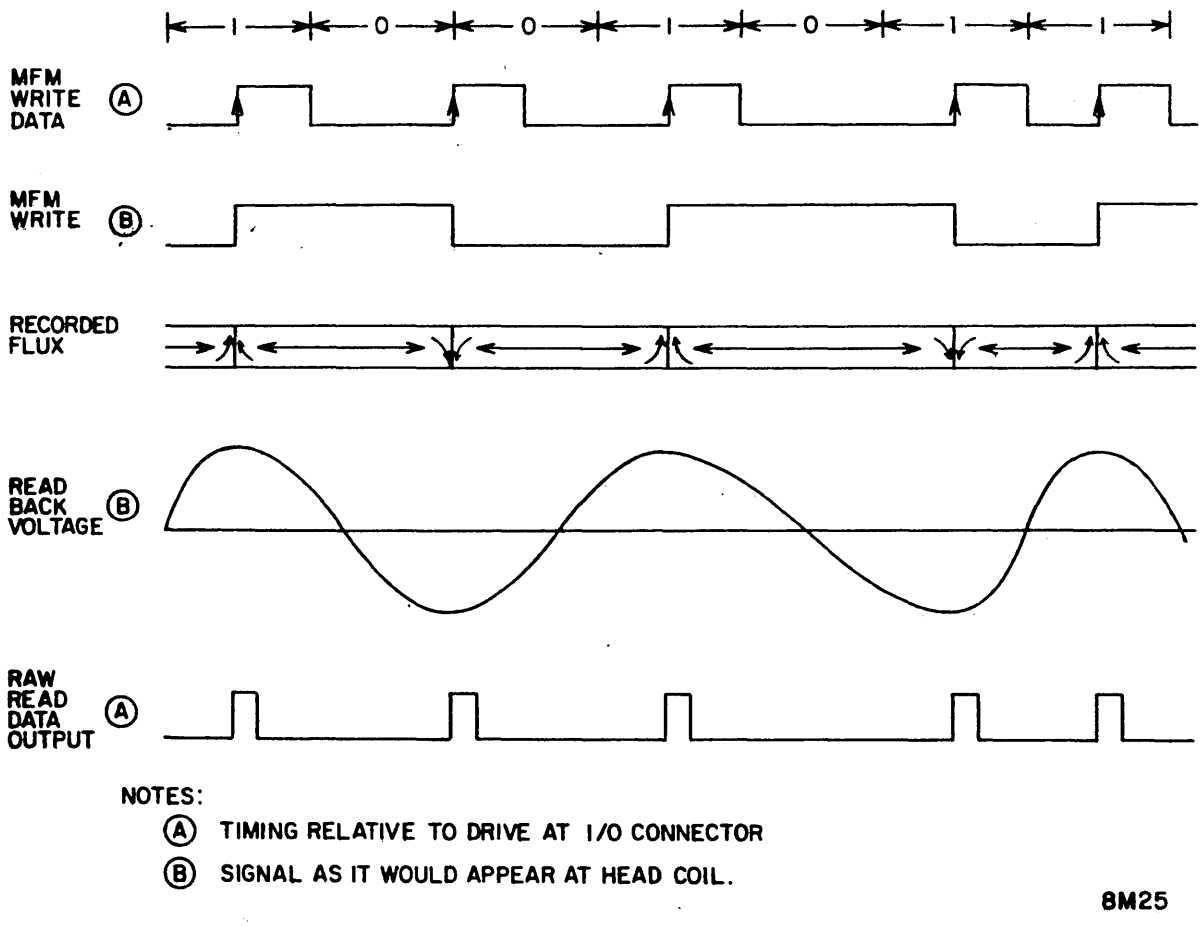


Figure 3-41. MFM Recording - Waveforms and Timing

NRZ To MFM Converter/Write Compensation Circuits

The NRZ to MFM converter/write compensation circuits convert the NRZ data into MFM data and also shift the output MFM pulses to compensate for problems caused by variations in data frequency. Figures 3-42 and 3-43 show simplified logic and timing for these circuits.

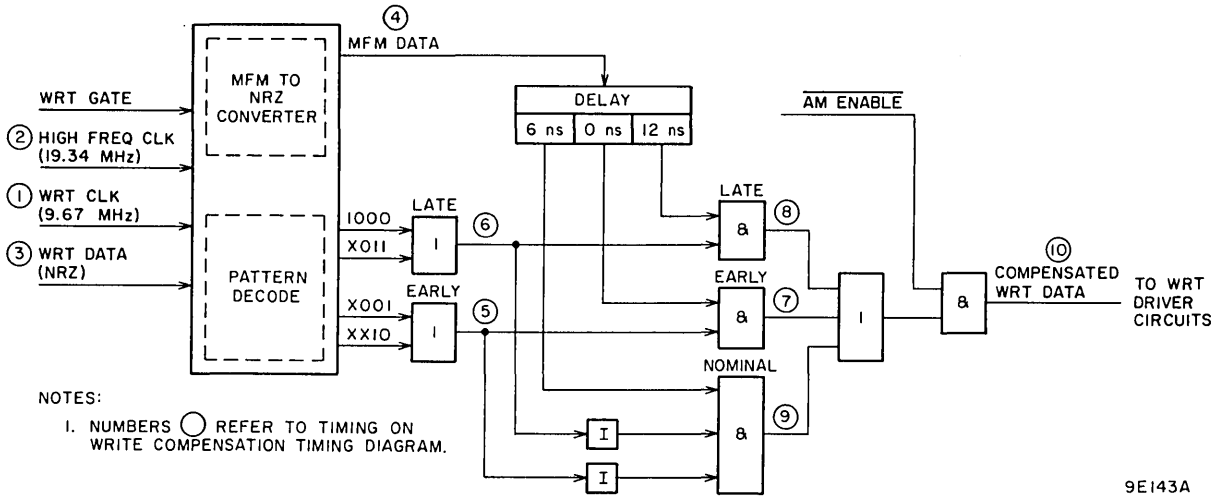


Figure 3-42. Write Compensation NRZ to MFM Converter Circuits

The 9.67 MHz and 19.34 MHz signals from the servo frequency multiplier circuit provide basic timing signals for these circuits. The NRZ data from the controller provides the data input.

The NRZ to MFM converter converts the NRZ data into MFM data and applies it to a delay line in the write compensation circuits. This delay line has three outputs which are combined with the outputs of the pattern decode logic (at the Early, Late, and Nominal gates) to produce compensated write data.

The pattern decode logic analyzes the NRZ data and determines if its frequency is constant, increasing or decreasing. This is necessary because if the frequency is increasing or decreasing, problems can occur during subsequent read operations. These problems are eliminated by compensating the data before writing it on the disk.

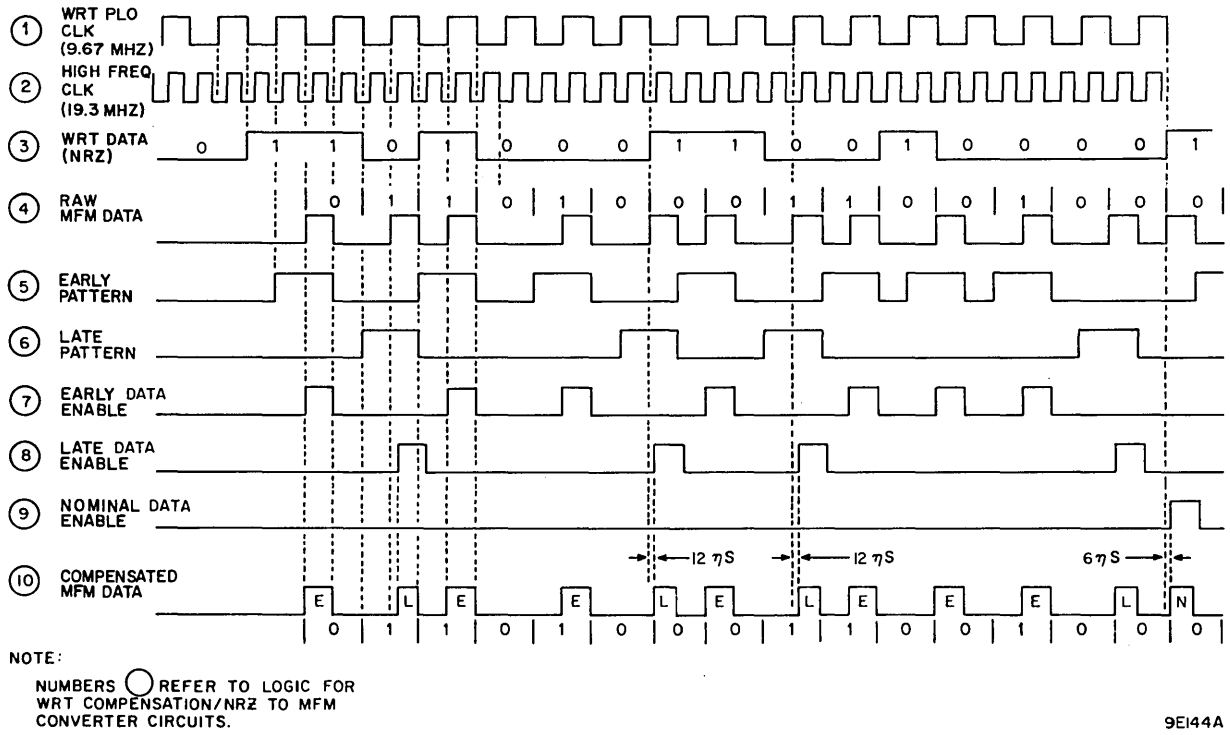


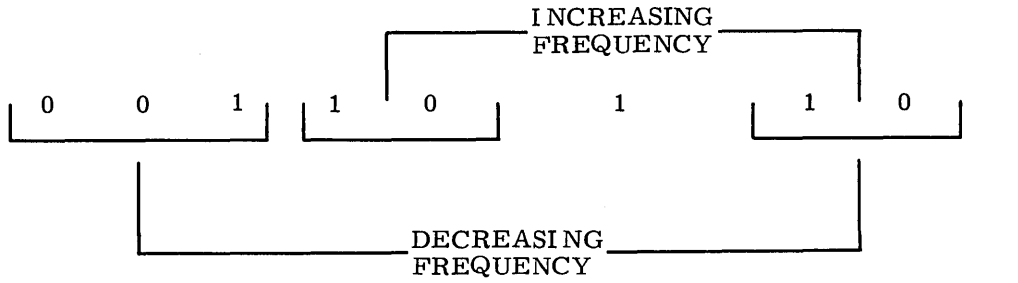
Figure 3-43. Write Compensation Timing

The data frequency is constant whenever all ones or all zeros are being recorded because all pulses are separated by one cell (103 ns). However, a 011 pattern represents a frequency increase since there is a delay of about 1.5 cell between the 01 and only 1.0 cell between the 11. On the other hand a 10 pattern represents a frequency decrease since a pulse is not written at all in the second cell. A 001 pattern is also a frequency decrease since there is a 1.0 cell interval between the first two bits and 1.5 cell between the last two.

The previous examples examined only two or three bits without regard to the preceding or subsequent data pattern. The actual combinations are somewhat more complex. The drive logic examines and defines the following patterns:

Pattern	Frequency Change
011	Increasing
1000	Increasing
10	Decreasing
001	Decreasing

Any data pattern will have considerable overlapping of the data pattern frequency changes. Consider the overlap of these eight bits:



9E251

The outputs from the pattern decode logic enable either the Early, Late or Nominal gate (depending on the input frequency) to provide compensated Write data as follows:

- If frequency is constant, there will be no peak shift. In this case the data is defined as nominal and is delayed 6 ns.
- If frequency is decreasing, the apparent readback peak would occur later than nominal. To compensate for this, the data is not delayed and is therefore 6 ns earlier than the nominal data.
- If frequency is increasing, the apparent readback peak would occur earlier than nominal. Therefore, this data is delayed 12 ns which is 6 ns later than nominal.

After being write compensated the data is transmitted to the write driver circuits.

Write Driver Circuit

The compensated write data is sent to the read/write chassis and applied to a differential receiver in the write driver circuits (refer to figure 3-44). The output of the receiver then serves as a clock for the Write Toggle FF. This flip flop toggles only when the Write Enable signal is active. The output of this flip flop provide the input to the Write Driver which in turn generates the current for the read/write heads. The magnitude of the current applied to the heads is controlled by the write current control circuits.

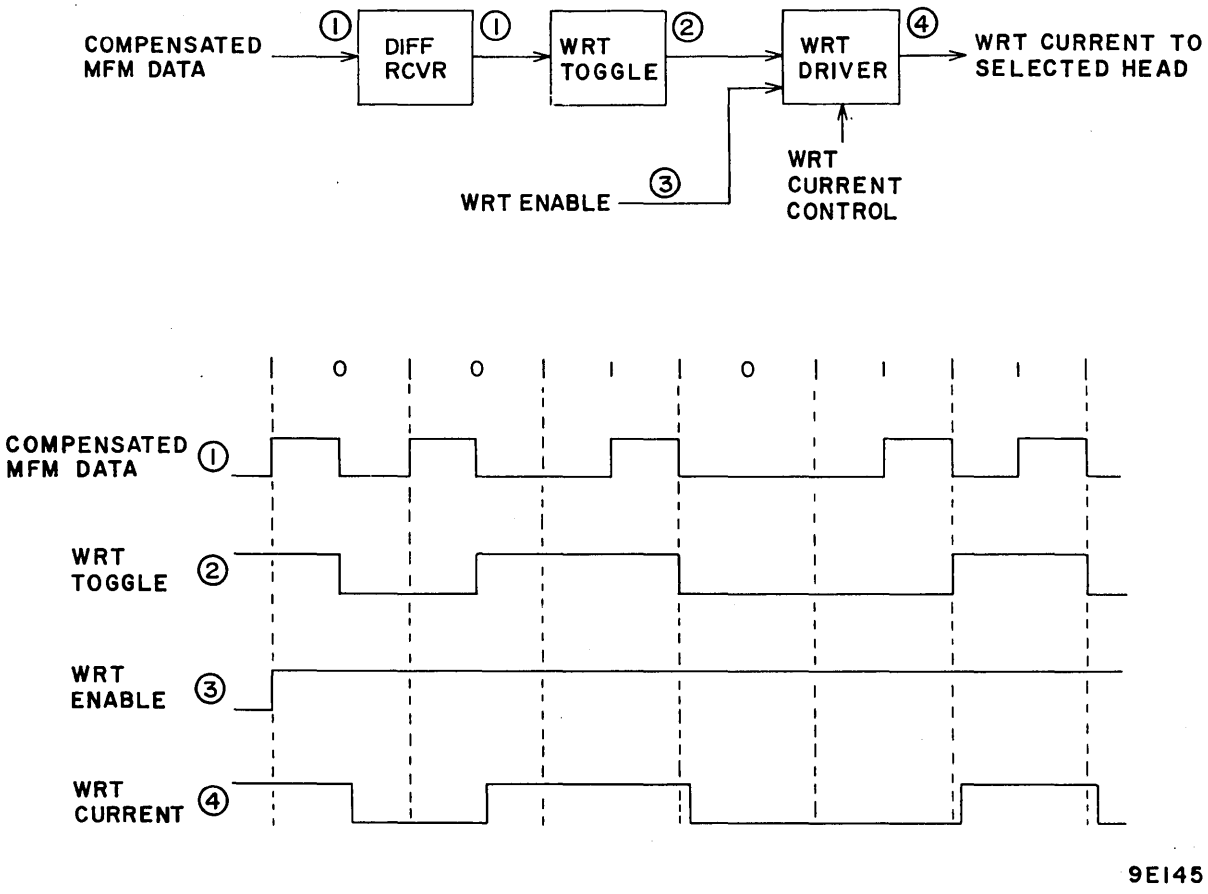


Figure 3-44. Write Driver Circuits and Timing

Write Current Control

The magnitude of the write current sent to the heads is controlled as a function of cylinder address. This is referred to as write current zoning. There are seven write current zones (A through G). Write current is reduced at each zone boundary from outer to inner tracks. Table 3-8 defines the cylinders in each write current zone.

Table 3-8. WRITE CURRENT ZONES

Zone	40 MB	80 MB
A	000-063	000-127
B	064-127	128-255
C	128-191	256-383
D	192-255	384-511
E	256-319	512-639
F	320-383	640-767
G	384-410	768-822

Writing Address Marks

The address mark is an area that contains neither MFM "1's" or "0's". The drive starts writing an Address Mark when it receives Tag 111 and Bus Out bits 1 and 4 from the controller. This activates the Address Mark Enable signal which prevents compensated write data from going to the write driver circuits. The write driver continues to generate current for the write coil but without data no current reversals occur. The effect is to erase all information from the disk. The drive stops writing the address mark when the controller drops Tag 111 or Bus Out bits 1 or 4.

Write Data Protection

General

Write data protection consists of disabling the write driver circuit whenever there is a danger of writing faulty data on the disk pack. It is initiated if the drive detects the Write Protect signal active, Fault latch set, or a low voltage condition. All of these are described in the following.

Write Protect

The Write Protect signal goes active if any of the following occurs.

- Controller commands a write while the heads are in an offset position.
- WRITE PROTECT switch on drive operator panel has been depressed to light the indicator. In this case, depressing the switch to extinguish the indicator causes the Write Protect signal to go inactive.
- Head alignment is being performed.
- Low dc voltage condition is detected or the disk pack speed slows down below 2800 r/min. Both of these conditions will also cause an emergency retract of the heads.

Fault

The Fault latch sets as a result of a number of drive malfunctions. The conditions causing the Fault latch to set are described in the discussions on fault and error conditions.

Loss of Voltage

If power is lost or drops below a certain level, an emergency retract is performed. However, in this case it is possible that the other signals used to disable the write driver (Write Protect and Fault) will not function properly and the drive will continue to write while the heads are being retracted. This could alter or destroy data already on the pack. The loss of voltage protection circuit consists of a capacitive discharge network that ensures the write circuits are disabled until the heads are unloaded.

READ OPERATIONS

General

Read operations are initiated by a Control tag (111) with Bus Out bit 3 true. This enables the analog data detection circuits, which sense the data written on the disk and generate analog read data signals.

The analog data goes to the read analog to digital converter which changes it into digital MFM data.

In units with the Read PLO/Data Separator option, the read PLO and data separator change the MFM data to NRZ and also generate a 9.67 MHz Read Clock signal. Both data and clock are then sent to the controller. In units without this option, the digital MFM data is sent directly to the controller.

The read circuits also detect the address mark area and send an Address Mark Found signal to the controller.

Figure 3-45 shows the main elements in the read circuits and table 3-8 briefly describes each of these elements. The following paragraphs further describe the read circuits.

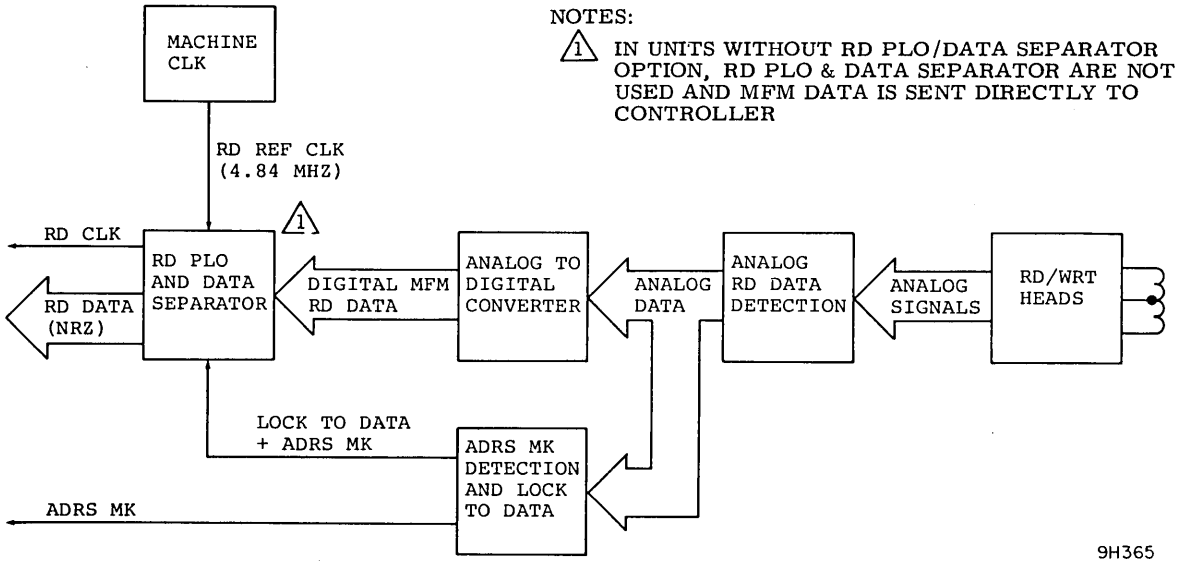


Figure 3-45. Read Circuits Block Diagram

TABLE 3-9. READ CIRCUIT FUNCTIONS

Circuit	Function
Analog Read Data Detection Circuits	Processes the analog signals sensed by the read/write heads so they can be used by the digital to analog converter.
Digital to Analog Converter	Changes the analog MFM data into digital MFM data. This data is sent to the read PLO and data separator.
Address Mark Detection	Detects the Address Mark and transmits an Address Mark Found signal to the controller.

Analog Read Data Detection Circuits

The analog read data detection circuits (refer to figure 3-46) processes the analog MFM data detected from the disk so it can be used by the analog to digital converter circuits.

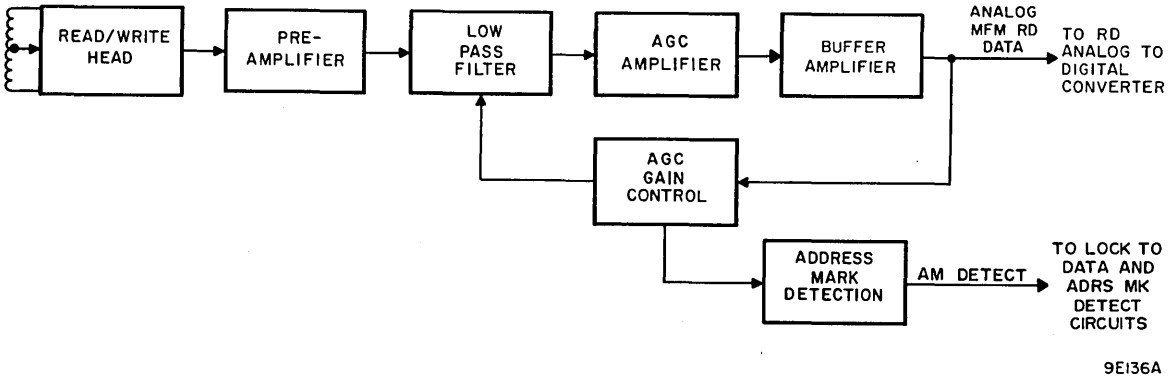


Figure 3-46. Analog Read Data Detection Circuits

The Read Pre-amplifier provides preliminary amplification of the analog voltage induced in the read coil. This voltage is induced in the coil by the magnetic flux stored in the disk oxide during write operations (refer to discussion on Basic Read/Write Principles). The frequency of the analog voltage is proportional to the frequency of the magnetic field flux transitions sensed by the read coil.

The low pass filter on the output of the Read Pre-amplifier attenuates the high frequency noise on the read data signals and provides a linear phase response over the range of read data frequencies. The output of the filter is applied to the AGC amplifier. This circuit generates an output signal amplitude that remains within certain limits regardless of the amplitude of the input signal. The AGC Gain Control circuit provides the control voltage for the AGC amplifier and also provides inputs to the Address Mark detection circuits.

The Buffer amplifier processes the AGC amplifier output to provide the proper input for the analog to digital converter circuit.

Read Analog To Digital Converter

The read analog to digital converter circuits (refer to figure 3-47) receive analog MFM read data from the analog read data detection circuit and convert it to digital MFM data.

The analog to digital converter circuit consists of high and low resolution channels and the Data Latch FF. The high and low resolution channels detect the analog data by means of zero cross detectors consisting of Schmidt triggers. The zero cross detectors convert the analog data to digital pulses which are then applied to the Data Latch FF. The FF uses the outputs of both channels to produce a digital MFM data output. The low resolution channel provides the D input to the FF and the high resolution channel provides the clock. This produces an output from the Data Latch FF which retains the timing of the high resolution channel.

Both channels are necessary because of certain high frequency components present in the analog read data signals. These components can cause extraneous zero crossings which are detected by the zero cross detectors. However, the low pass filter in the low resolution channel attenuates the high freqeuncy components thus eliminating any possible extraneous outputs from the channels zero crossing detector.

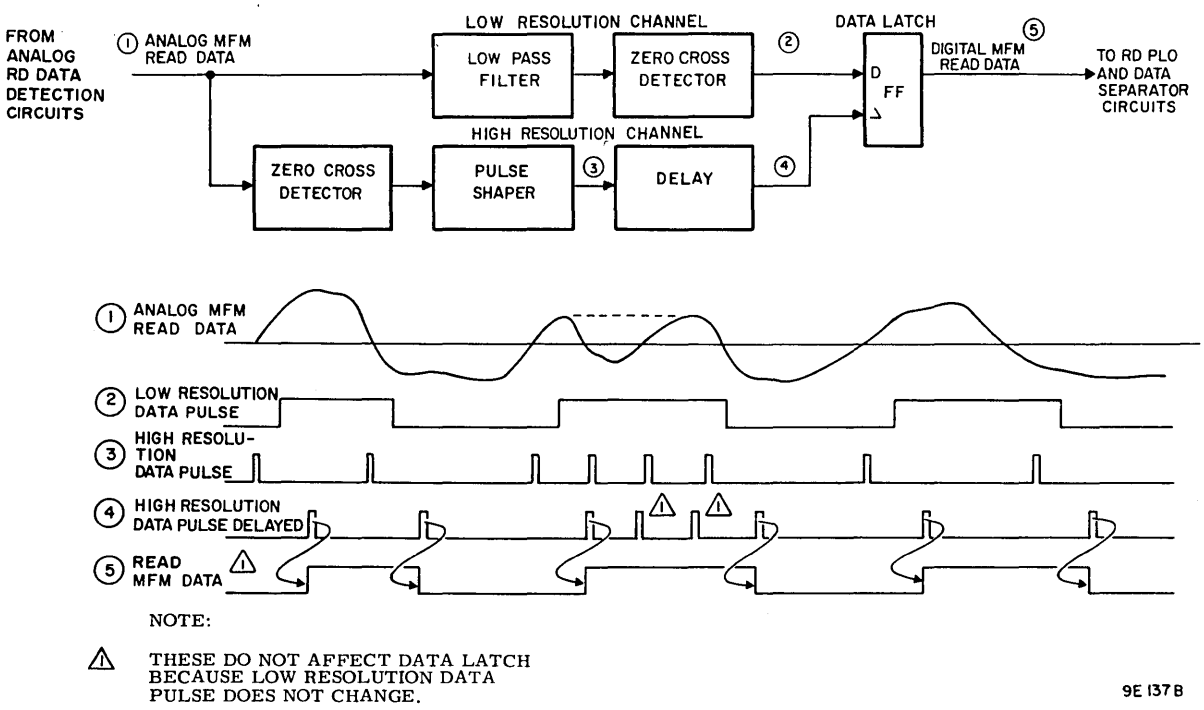


Figure 3-47. Read Analog To Digital Converter Logic and Timing

The high resolution channel still detects the crossings and generates clock inputs to the FF, but without the D input provided by the low resolution channel the extraneous clock pulses are ignored.

If the drive has the Read PLO/Data Separator option, the digital MFM read data is sent to the PLO and data separator which use it to generate the NRZ data and Read clock. However, if the drive does not have this option the data is sent directly to the controller.

Lock To Data And Address Mark Detection Circuits

These circuits generate (refer to figure 3-48) the Lock to Data signal and also detect the address mark area. The Lock to Data signal is used to synchronize the read PLO and data separator circuits on these units with this option (other units do not use the signal). Finding the address mark area sets Bus In bit 0 to the controller.

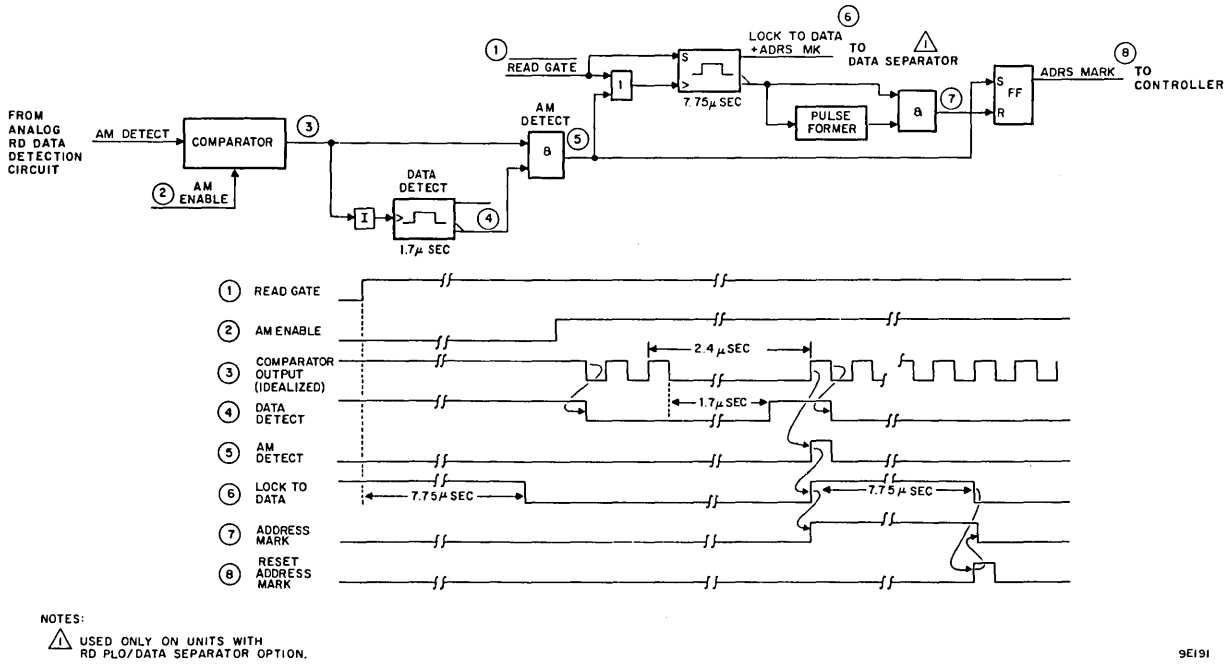


Figure 3-48. Lock to Data/Address Mark Detection Logic and Timing

The Lock to Data signal is active whenever the Lock to Data one shot is in the set state. This one shot is triggered (to the set state) when either the Read Gate signal (Tag 111, Bus Out bit 3) goes inactive or the address mark is detected.

When the Read Gate signal goes inactive it triggers the one shot and also causes it to be held in the set state. When the Read Gate signal goes active again, it removes the set conditions from the one shot and allows it to time out after 7.75 μs. Therefore, a 7.75 μs lock to data period occurs at the beginning of every read operation.

Detecting the address mark also triggers a 7.75 μs pulse from the one shot. The address mark consists of an area about 2.4 μs in length that contains neither MFM ones or zeros.

The address mark detection circuit is enabled only during read operations (Tag 3 and Bus bit 3 active). The controller activates the circuit by raising Bus Out bit 4 (Address Mark Enable).

The Address Mark Enable signal causes the comparator to start generating output pulses that trigger and retrigger the Data Detect one shot. The comparator generates the output pulses only when there are input data pulses. Therefore, during the address mark area the comparator stops generating pulses and the one shot times out 1.7 µs after the last data pulse was detected. The first data pulse following the address mark area enables the Address Mark Detect gate. This triggers the Lock to Data one shot which causes a 7.75 µs Lock to Data period and also a 7.75 µs Address Mark signal.

Read PLO And Data Separator (Applicable Only To Units With RD PLO/Data Separator Option)

General

This circuit has two functions: (1) to convert the MFM data from the analog to digital converter into NRZ data and (2) to generate a Read Clock signal which is locked to the frequency of the read data (9.67 MHz nominal). Both the NRZ data and the Read Clock signal are transmitted to the controller.

The read PLO and data separator circuits consist of four main parts (refer to figure 3-49):

- Input Control - Controls whether MFM data or 4.84 MHz clock pulses will furnish the input to the circuit.
- Data Strobe Delay - Delays the pulses to provide the proper input to the VCO. These circuits also provide error recovery capability.
- Phase Lock Loop - Synchronizes the circuit outputs to the phase and frequency of the inputs.
- Data Separator - Converts the MFM data to NRZ data and generates the Read clock. This circuit is actually a part of the phase lock loop.

The remainder of this discussion further describes the read PLO and data separator circuits.

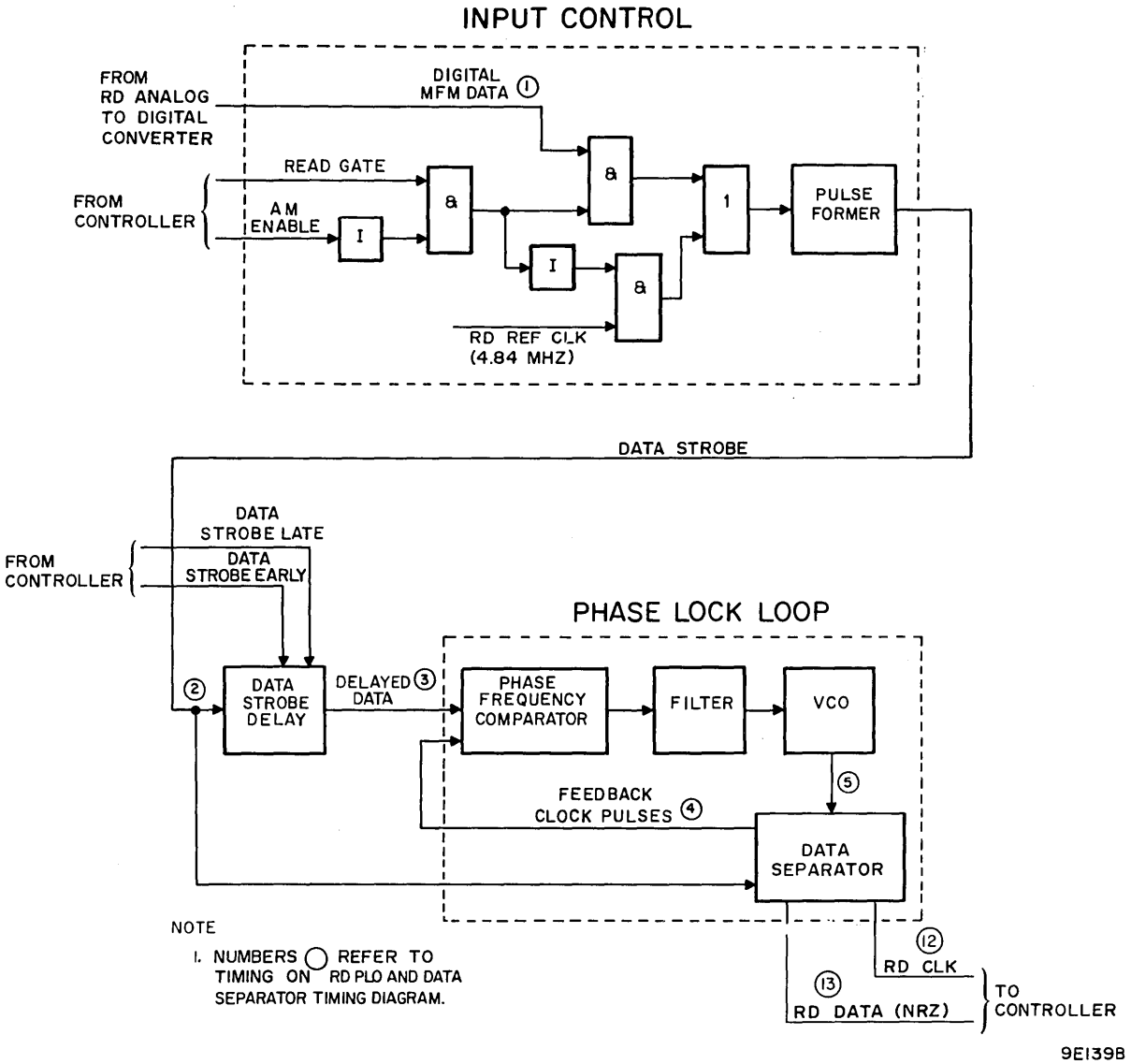


Figure 3-49. Read PLO and Data Separator Circuits

Input Control

The input control circuit (refer to figure 3-49) selects the input that will be used by the read PLO and data separator circuits. This input will always be either MFM data from the read analog to digital converter or 4.84 MHz clock pulses from the servo frequency multiplier circuit.

The 4.84 MHz clock signal is used only when the drive is not reading MFM data, such as before Read Gate is raised. It also uses the 4.84 MHz clock whenever the Address Mark Enable signal is active because this indicates the drive is expecting the address mark which contains no MFM data. The drive uses the clock signal as a substitute for the read data for two reasons: (1) the signal is derived from the track servo dibits and therefore, its frequency (like that of the read data) varies directly with disk pack speed and (2) after being processed by the pulse forming circuits, it has about the same nominal frequency as the read data (9.67 MHz). This results in it being easier for the phase lock loop to synchronize to the proper frequency when switching from one of the signals to the other.

Once selected the signal is applied to a pulse forming network which generates a 20 ns pulse for each transition of the input. These pulses are then applied to the data strobe delay circuits and also furnish the data input to the data separator.

Data Strobe Delay

The purpose of the data strobe delay circuit (refer to figure 3-49) is to delay the data pulses sufficiently to provide the proper timing relationship at the input to the phase lock loop. The output of the data strobe delay circuit is delayed by a time determined by the state of the Data Strobe Early and Data Strobe Late signals. These signals facilitate the recovery of marginal data and are enabled by the Error Recovery tag (001).

The output of this circuit is the Delayed Data signals which are sent to the input of the phase lock loop.

Phase Lock Loop

The phase lock loop (refer to figure 3-49) synchronizes the read PLO/data separator circuit outputs (NRZ data and Read Clock) to the input (either MFM data or 4.84 MHz clock). The loop accomplishes this by comparing and following two signals: (1) the Delayed Data signals which have a constant phase and frequency relationship to the input MFM data or 4.84 MHz Clock (whichever is used) and (2) the Feedback Clock Pulse signals which have a constant phase and frequency relationship to the output NRZ data and Read Clock signals. The loop inputs are applied to the phase/frequency comparator.

The phase/frequency comparator generates output pulses which are a function of the phase and frequency between the positive going edges of the inputs. The filter circuit uses the comparator outputs to generate a control voltage for the voltage controlled oscillator (VCO).

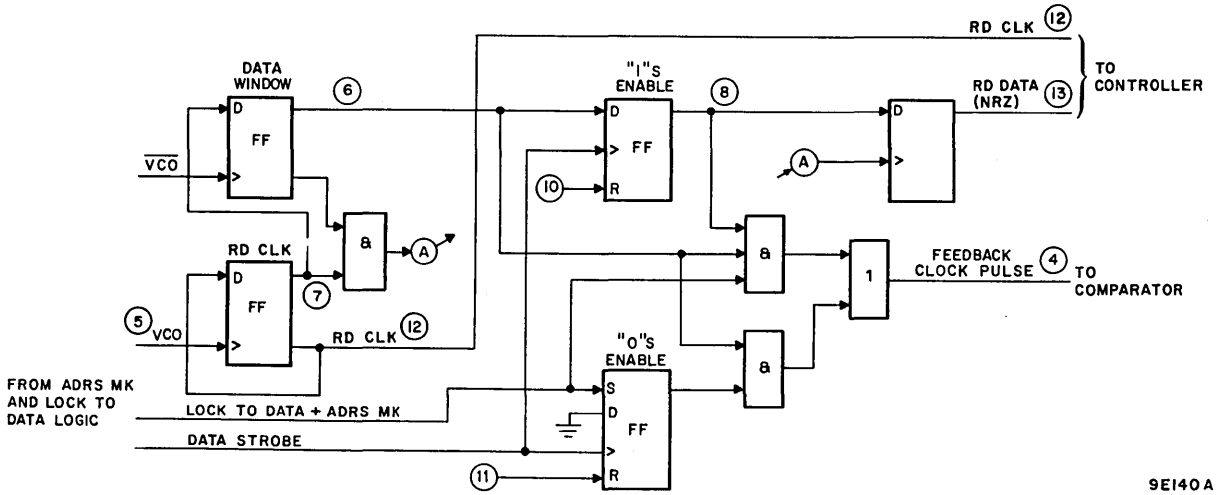
This control voltage causes the frequency of the VCO to vary in the direction necessary to eliminate the phase and frequency differences between the two signals that were input to the comparator.

The output frequency of the VCO is actually twice that of the input so for an input of 9.67 MHz it has an output of 19.34 MHz. However, the data separator divides this by two before generating the Feedback Clock Pulse signals thereby providing a feedback to the comparator that satisfies the loop.

Data Separator

This circuit determines if the data pulses represent a one or zero and then converts the data to NRZ. It also generates the Feedback Clock Pulses to the comparator and the 9.67 MHz Read Clock that is sent to the controller. Figures 3-50 and 3-51 show simplified logic and timing for the data separator circuit.

The VCO outputs provide the proper timing relationships for the data separator by controlling the Data Window and Read Clock FFs. The Read Clock FF generates the 9.67 MHz Read Clock signal and also provides timing signals to the data separator logic. The Data Window FF generates the Data window which is used to determine whether the input data pulses represent ones or zeros. The actual decoding of the data is done by the "1's" Enable and "0's" Enable FFs.



NOTE

1. NUMBERS ◯ REFER TO TIMING ON RD PLO AND DATA SEPARATOR TIMING DIAGRAM.

Figure 3-50. Data Separator Logic

If a data pulse represents a one it occurs during the data window and sets the "1's" Enable FF. Setting this FF generates a Feedback Clock pulse and causes the Data Buffer FF to generate a NRZ one.

If the data pulse represents a zero the "1's" Enable FF is not set and the Data Buffer FF generates a NRZ zero. In this case the "0's" Enable FF which is set by every data pulse generates the Feedback Clock Pulse signal.

Before accurate detection of data can begin, the proper phase relationship must be established between the data (representing ones and zeros) and the VCO output pulses. This is done during a 7.75 µs lock to data period which is initiated by the Lock to Data signal. This signal is a 7.75 µs pulse that occurs when the Read Gate signal goes true or when the address mark is detected. The Lock to Data signal holds the "0's" Enable FF set and disables the output of the "1's" Enable FF. Therefore, if the circuit is to synchronize properly the pulse must occur during a period when the drive is reading only zeros.

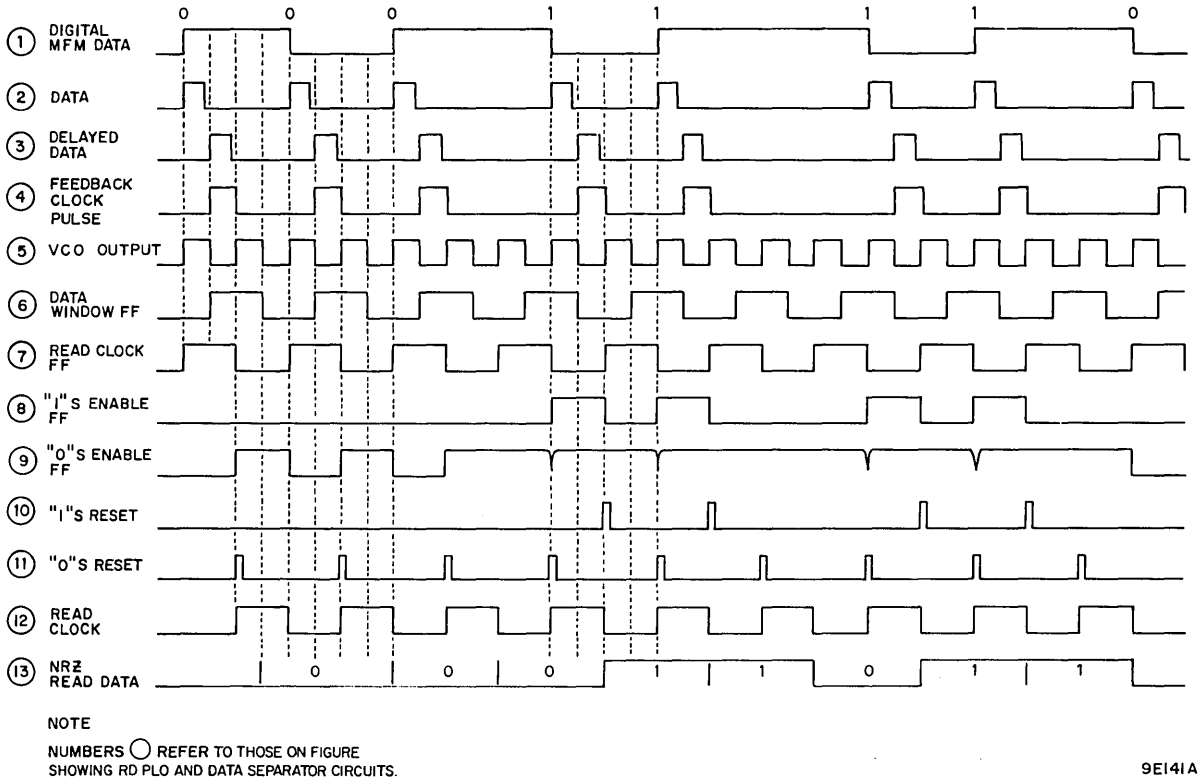


Figure 3-51. RD PLO and Data Separator Timing

FAULT AND ERROR CONDITIONS

GENERAL

The following describes those conditions which are interpreted by the drive as errors. All of these conditions either light an indicator at the drive and/or send a signal to the controller indicating an error has occurred.

These errors are divided into two categories: (1) those indicated by Fault Latch and register (2) those not indicated by Fault Latch and register. Both are explained in the following (refer to figure 3-52).

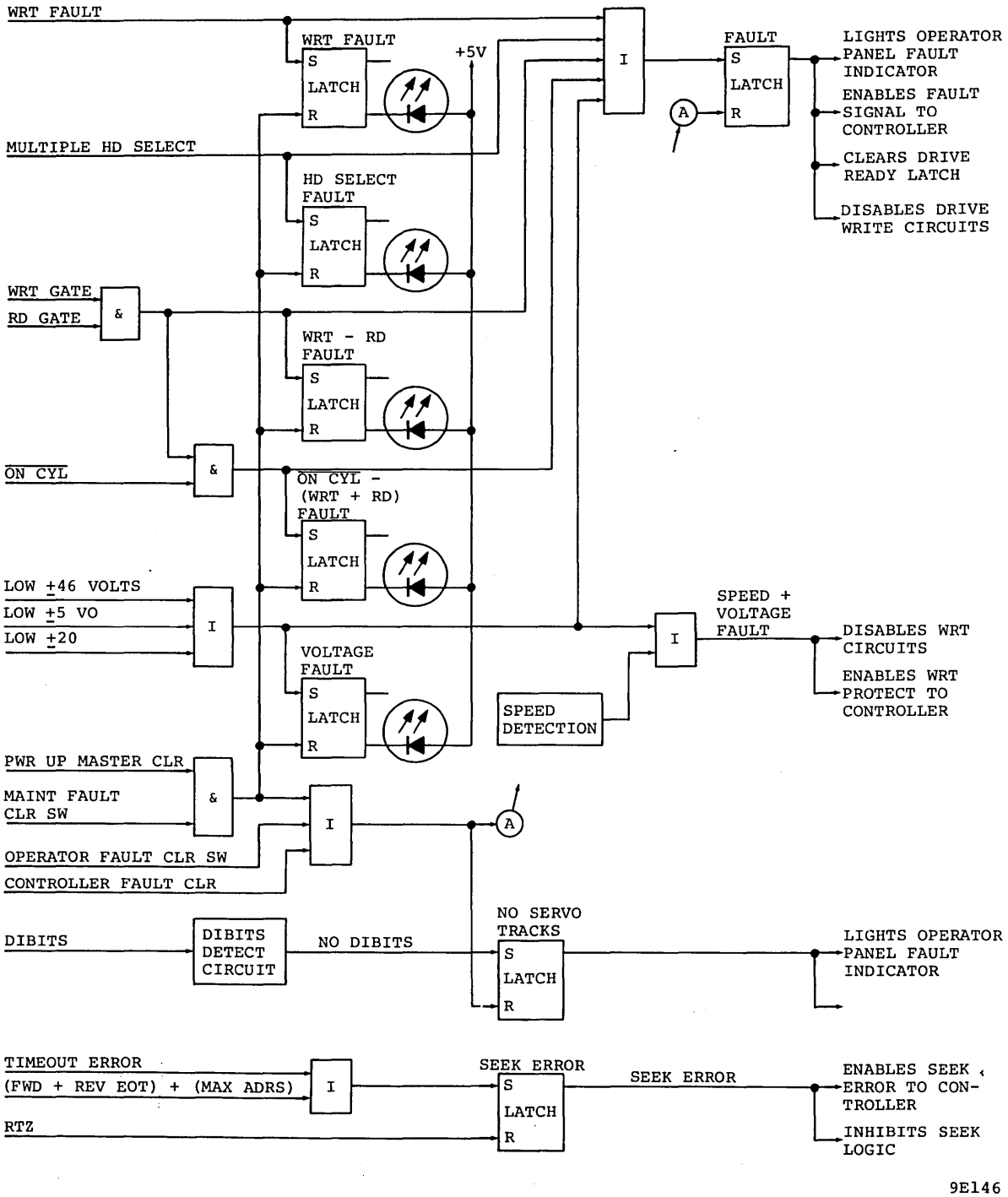


Figure 3-52. Fault and Error Detection Logic

ERRORS INDICATED BY FAULT LATCH AND REGISTER

General

Certain errors set the drives Fault latch and also set the fault register latches associated with the error condition.

Setting the Fault Latch does five things: (1) enables the fault line to the controller (2) lights the FAULT indicator on the drives operator control panel (3) clears the drives Unit Ready signal (4) inhibits the drives write and load circuitry and (5) causes the Check Diagnostic bit (bit 7), of the Low Cylinder (110) and Control (111) Tag bus in status bytes (refer to discussion on I/O Signal Processing), to be true. Also, for drives of S/C 18 & ABV, the Write Protect bit (BIB 7) of the Diagnostic Tag bus (010) goes true. These events prevent further drive operations from being performed until the error is corrected and the Fault latch is cleared.

Providing the error condition or conditions no longer exist, the Fault latch is cleared by any of the following:

- FAULT switch on operator panel.
- Controller Fault Clear signal from the controller.
- Maintenance Fault Clear switch on Fault card.
- Powering down the unit.

Whenever an error occurs that sets the Fault latch, it also sets a latch in the fault register. These latches provide a means of storing the error indication so it can be referred to later for maintenance purposes. They also cause a corresponding bit to be true in the Error Recovery (001) and Diagnostic (010) bus in status bytes (refer to discussion on I/O Signal Processing). The fault register latches are cleared only by powering down the drive or by the Maintenance Fault Clear switch on the fault card.

The following describes each of the conditions causing the Fault latch and fault register latches to be set.

Write Fault

A write fault is indicated if any of the following conditions exist.

- Low output from write driver indicating it may not be operating properly.

- Low current input to write driver.
- Low +22 volts to write driver.
- No write data transitions when Write Gate is active.

More Than One Head Selected

This fault is generated whenever more than one head is selected. The outputs of the head select circuits are monitored by summing and voltage comparator circuits. If more than one head is selected, the circuit generates a Multiple Select Fault.

Read And Write

This fault is generated whenever the drive receives a Read gate and Write gate simultaneously from the controller.

(Read Or Write) And Off Cylinder

This fault is generated if the drive is in an Off Cylinder condition and it receives a Read or Write gate from the controller.

Voltage Fault

This fault is generated whenever the ±46, ±5 or ±20 voltages are below satisfactory operating levels.

ERRORS NOT INDICATED BY FAULT LATCH OR REGISTER

General

The following errors are detected by the drive but are not stored in the fault register and do not set the Fault latch. However, they do cause the drive to give other error indications and this is explained in the following paragraphs.

Low Speed Or Voltage

The Speed or Voltage Fault signal goes true when the drive detects either a low voltage condition or that drive spindle speed is below 2700 r/min. When either of these are detected, the drive write circuits are disabled and the Write Protect signal is sent to the controller. These also result in an emergency retract of the heads (refer to discussion on Emergency Retract).

No Servo Tracks Fault

If dibits are not detected within 350 ms after the load seek sequence begins, the No Servo Tracks latch is set. This lights the FAULT indicator on the drive operator control panel and also enables the Return to Zero (RTZS) logic. Enabling the RTZS logic causes the heads to unload. Another load cannot be started until the No Servo Tracks latch is cleared. The No Servo Tracks latch is cleared in the same manner as the Fault latch.

Seek Error

The Seek Error latch is set by any of the following error conditions:

- On Cylinder was not obtained within 500 ms from the start of the seek.
- Forward or reverse end of travel (EOT) sensed.
- Drive is commanded to seek to a cylinder address greater than 410 (822).

Setting the Seek Error latch enables the Seek Error line to the controller, inhibits the drive from performing another seek until the Seek Error latch is cleared, and also causes the Check Diagnostic bit (7), of the low cylinder (110) and control (111) tag bus in status bytes, to be true. The latch is cleared by a Return to Zero Seek command.

SECTION 4

DISCRETE COMPONENT CIRCUITS

INTRODUCTION

This section contains descriptions of all the discrete component circuits found in the drive and/or the FA727 controller. These circuits are arranged in alphabetical order (AAA-ZZZ) according to the circuit designator.

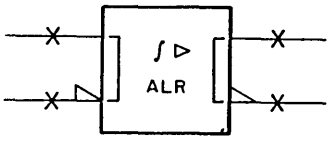
Amplifier and Filter - ALR

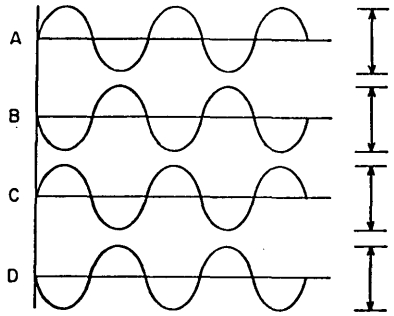
The ALR circuit is a differential amplifier and a 2 pole linear phase filter followed by a differential buffer amplifier. The amplifier stage has a gain of approximately 2.

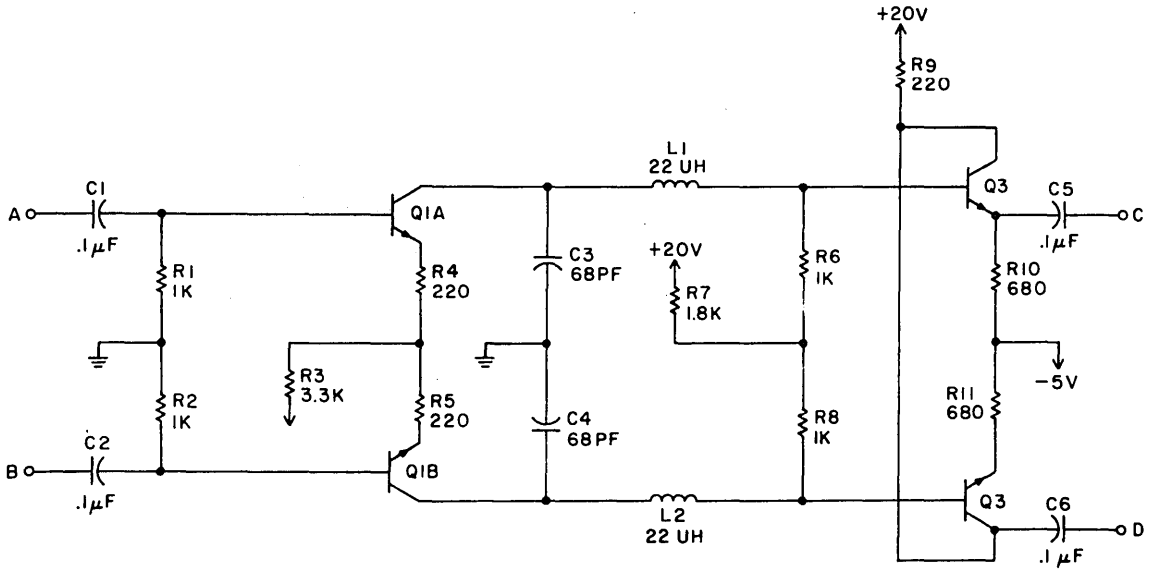
Q1A and B form the differential amp with R6 and R8 being the load resistors and also impedance matching resistors for the filter. The inductors L1 and L2 and capacitors C3 and C4 make up the rest of the filter. The upper break design frequence (-3 db point) of the filter is 3.13 MHz.

The input coupling capacitors C1 and 2 in conjunction with bias resistors R1 and 2 give the circuit a low frequency cutoff (-3 db point) of less than 2 kHz.

The output is a differential emitter follower buffer consisting of Q3 and 4 and R10 and 11, that is used to reduce the output impedance.





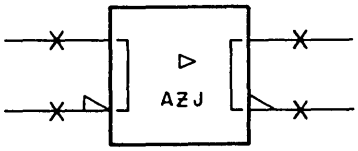


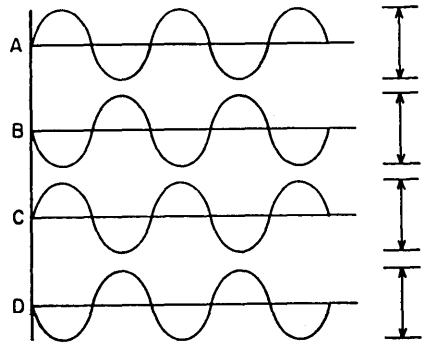
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

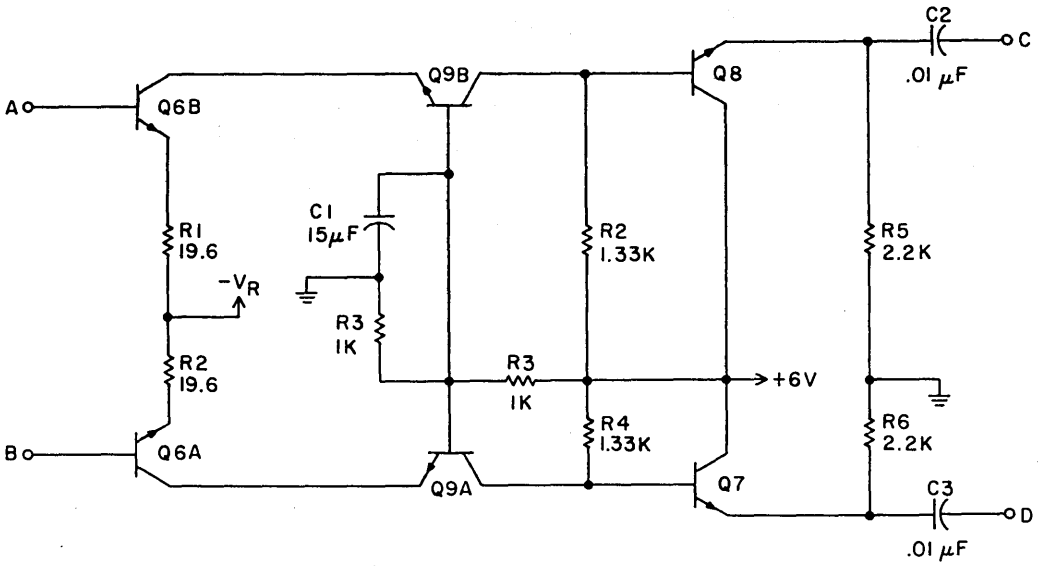
Differential Amplifier - AZJ

The preamplifier is a cascade type with a matched pair of transistors (Q6A and Q6B) used as a common emitter front end followed by another matched pain of transistors (Q9A and Q9B) used as a common base second stage, this effectively reduces the emitter collector capacitance of the common emitter front end.

The final stage of the front end is a emitter follower (Q7 and Q8) used as a buffer between the preamp and filter section. Resistors R1 and R2 in the emitter circuit give the front end a input impedance of just under the 500 ohms. The constant current source for the preamp supplies approximately 2.5 ma.





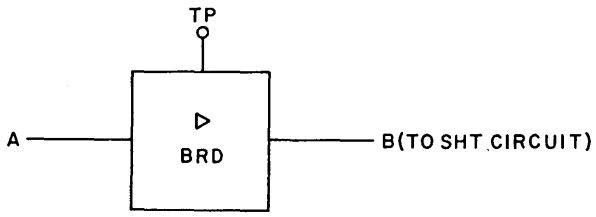


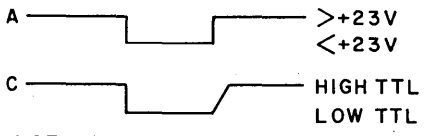
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

LEVEL TRANSLATOR (COMPARATOR SECTION) - BRD

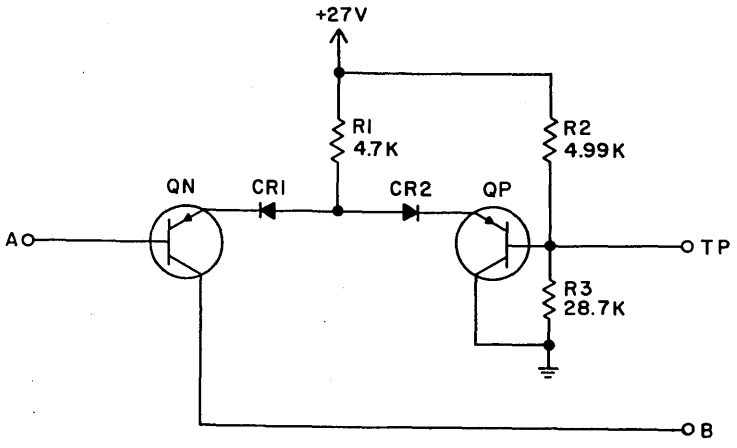
The BRD circuit is a differential voltage comparator which operates in conjunction with the SHT circuit to translate input signal levels of below +23 V to a low TTL output and input signal levels of above +23 V to a high TTL output.

The BRD circuit functions in conjunction with the SHT circuit to indicate whether or not the write current is below a minimum value. (See SHT circuit description.) A voltage reference of +23 V is applied to the base of transistor QP. With normal write current, the base of QN is below +23 V. Under these conditions transistor QN is on and transistor QP is off, and the resistor in the collector circuit of QN provides a forward bias voltage to the SHT circuit. If the write current is below the acceptable minimum, the voltage at the base of QN goes above +23 V. Then QN turns off and QP turns on, and the resistor in the collector circuit of QN does not develop sufficient forward bias for the SHT circuit.





NOTE: A IS INPUT TO BRD CIRCUIT
C IS OUTPUT OF SHT CIRCUIT



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

Amplifier and Filter - BZJ

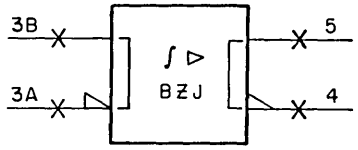
The BZJ circuit is a differential amplifier and a 4 pole low pass Butterworth filter followed by a differential buffer amplifier. The amplifier stage has a gain of approximately 7.5.

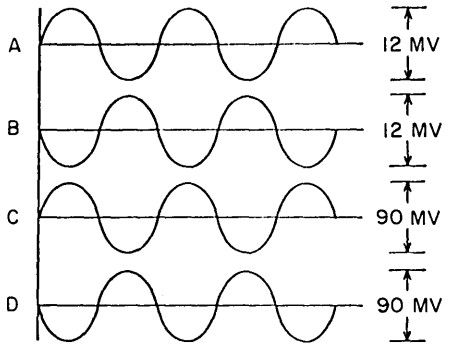
Q3A and B form the differential amplifier with R5 and R6 being the load resistors and also impedance matching resistors for the filter. The inductors L1, L2, L3, and L4 and capacitors C1, C2, C3 and C4 make up the rest of the filter. The upper break frequency (-3db point) of the filter is approximately 6.8 MHz.

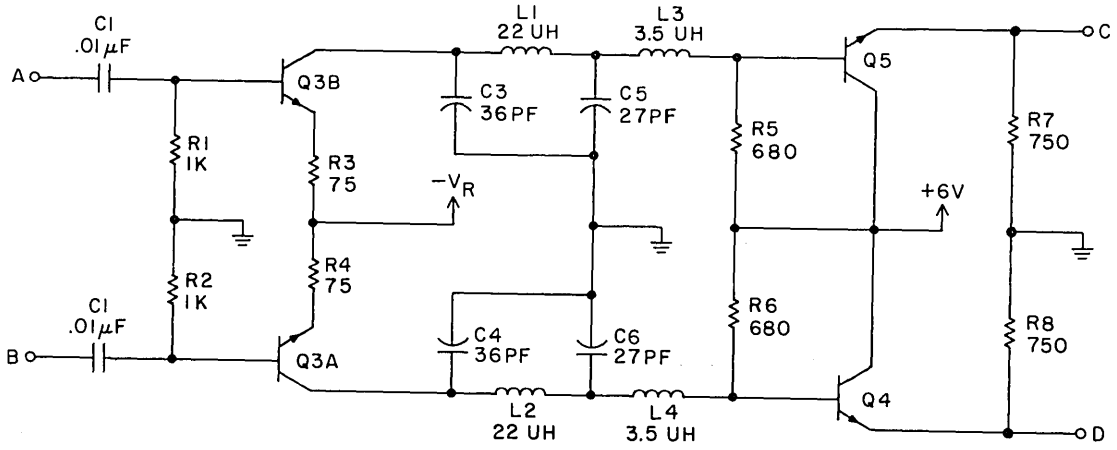
The input capacitors C1 and C2 in conjunction with resistors R1 and R2 give the circuit a low frequency cutoff (-3 db point) of less than 20 kHz.

The output is a differential buffer consisting of Q4, Q5, R7, and R8 that is used to reduce the output impedance and give more drive.

The constant current source for the differential amp supplies approximately 4.75 ma.



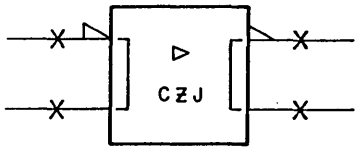


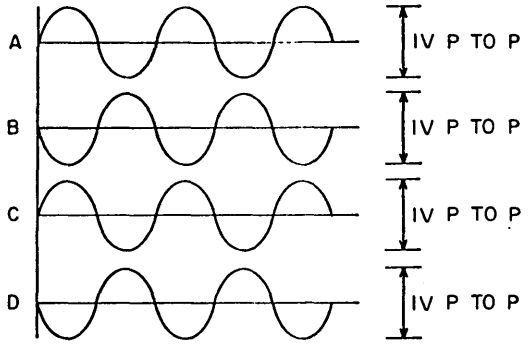


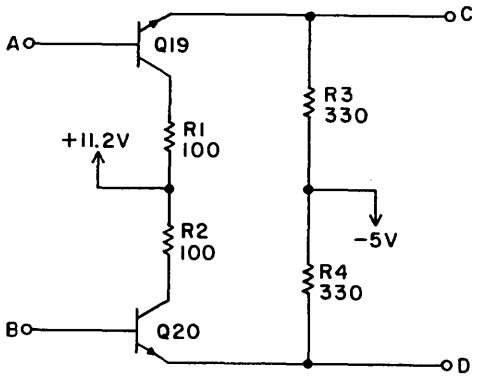
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

BUFFER AMPLIFIER - CZJ

The CZJ circuit is a buffer amplifier designed to increase the output signal driving capability of a differentially amplified signal. Q19 and Q20 are emitter followers that present comparatively high input impedance and low output impedance.





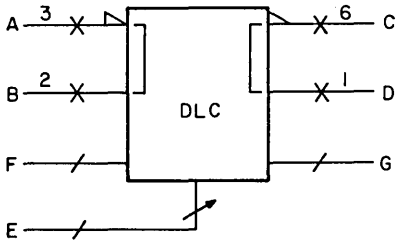


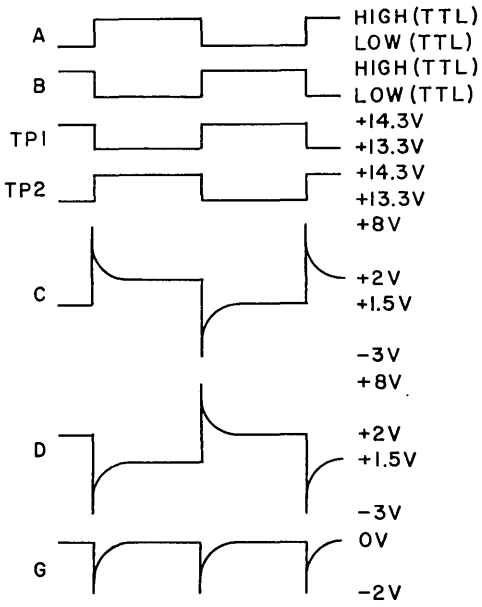
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

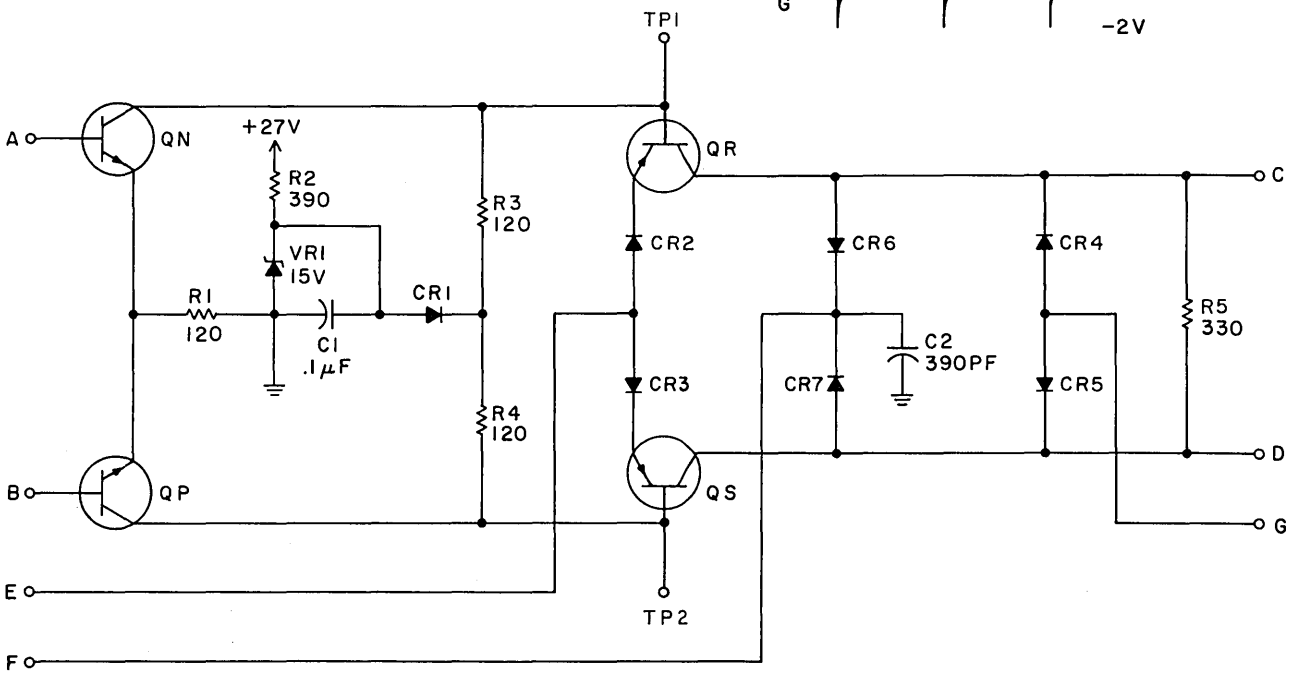
WRITE DRIVER -DLC

The DLC circuit is a differential current switch which converts voltage input signals to current for driving a differential recording head.

TTL level signals are applied to inputs A and B. Transistors QN and QP drive the bases of transistors QR and QS to control current to the head. The current source is connected to input E and supplied to the emitters of transistors QR and QS through diodes CR2 and CR3. Differentiated current is available to the head at outputs C and D. Diodes CR6 and CR7 provide a path to ground for write current when input F is grounded by a write protect circuit. Diodes CR4 and CR5 rectify the echo pulses from the head and apply them to a write voltage fault circuit through output G.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

Rectifier - DZJ

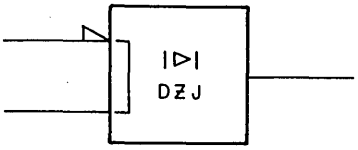
The DZJ circuit is a full wave rectifier with a differential input and single ended output.

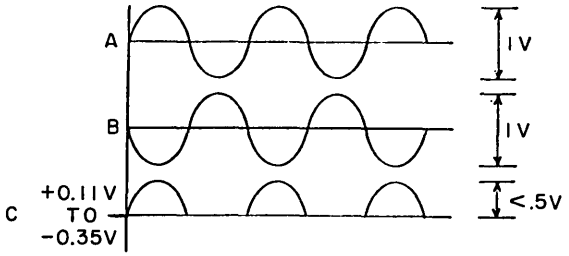
The rectifier consists of a matched pair of transistors (Q1A and B) used as a differential pair. Q1A and Q1B conduct during the positive half input cycle and back biased during the negative half input cycle. Q2 is used as a constant current source supplying about 4.5 ma.

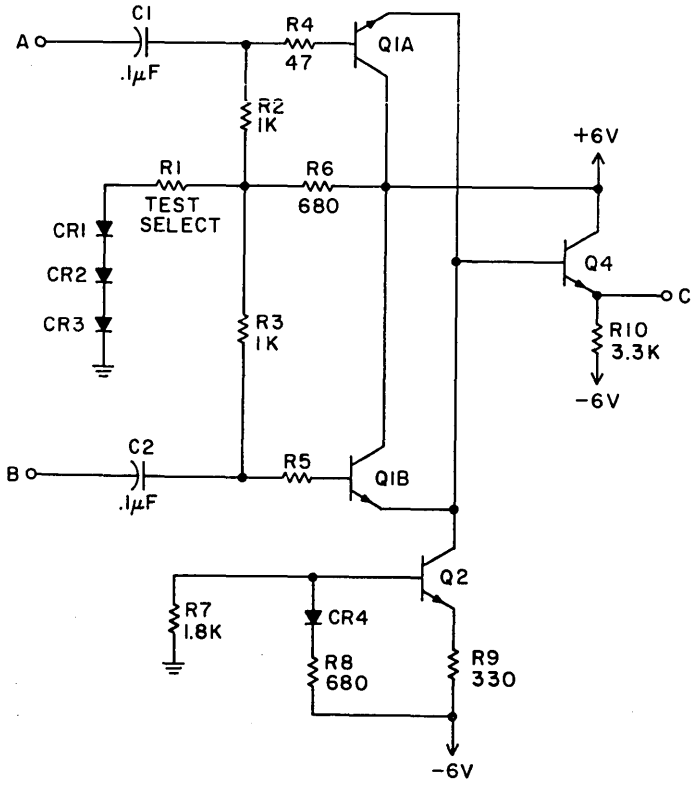
Diodes CR1, 2, and 3 along with test select R1 and R2 form an adjustable bias network. This adjusts the DC base line at output C from about -0.35v to +0.11v and is set so that the output of the AGC amplifier is 2v p-p.

The output buffer amplifier is Q4 and presents a comparatively high input impedance and a low output impedance.

The input frequence response is greater than 2 kHz.







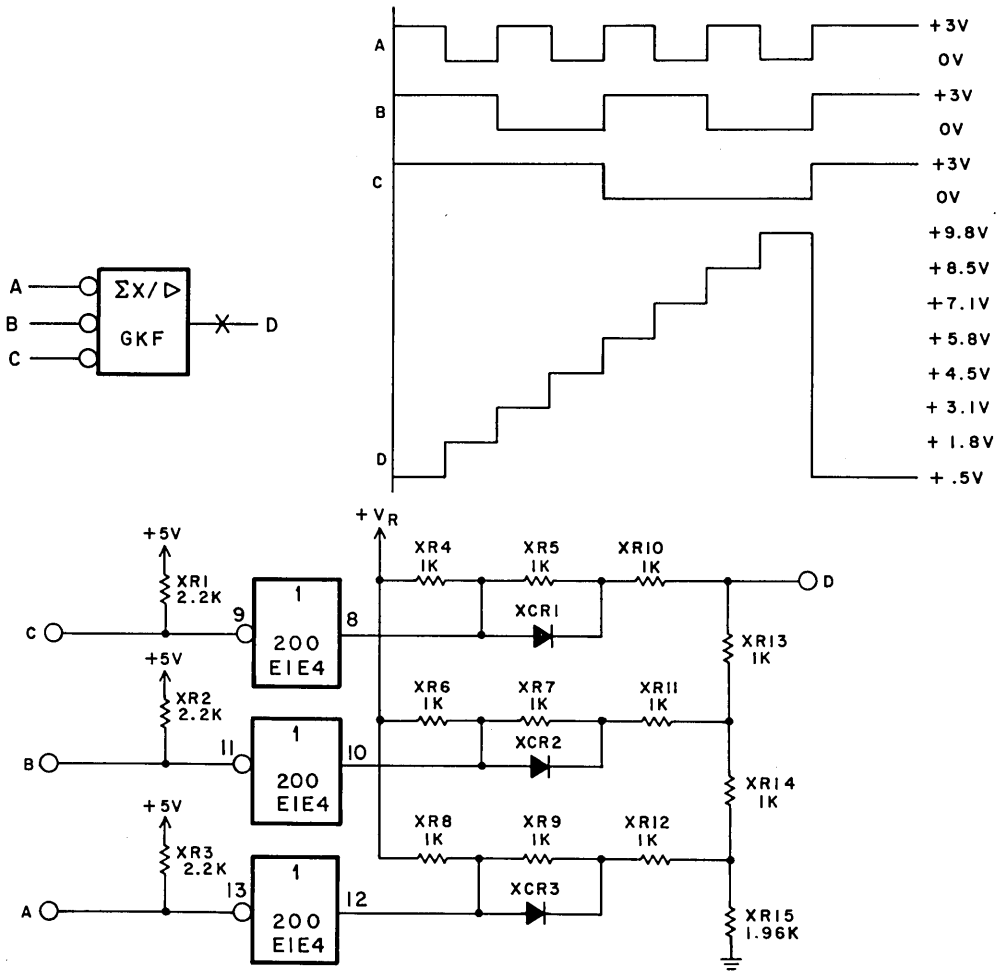
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

DIGITAL TO ANALOG CONVERTER - GKF

The GKF circuit converts three digital input signals to an analog output whose level depends upon the logical combination at the inputs.

The element 200 is an open collector IC. When pin 9 of element 200 is +3 volts or a "1", its output (pin 8) is 0 volts. When pin 9 is 0 volts or a "0", its output (pin 8) is open and the resistor divider (XR4, XR10, XR13, etc.) to V_r determine the voltage at an identical manner but have less influence on the voltage at point D because of their entry connection in the resistor network.

When V_r is +12 volts the output at D corresponding with the various combinations of logic input is as shown in the waveform diagram.



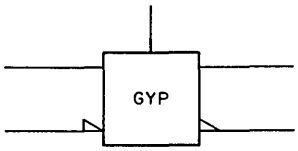
NOTE:
VOLTAGE AND COMPONENENT VALUES ARE FOR REFERENCE ONLY. 7J14

Voltage Controlled Oscillator - GYP

General

This circuit is used as part of a phase lock loop (refer to Figure 1). When Frequency Out is not equal to Frequency In, the comparator generates a voltage that causes the GUE circuit output (Frequency Out) to vary in the direction necessary to eliminate the difference. When the two frequencies are the same, the loop is said to be locked. The GUE circuit is made up of five main parts (refer to Figure 2).

- Level Shifter
- Current Pump
- Filter
- Buffer and Level Shifter
- Voltage Controlled Oscillator



The following explains each of these parts.

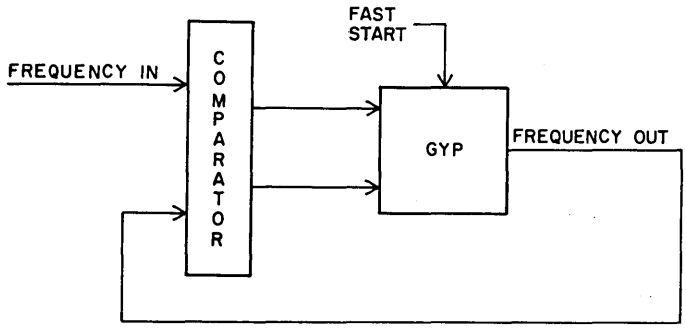


Figure 1

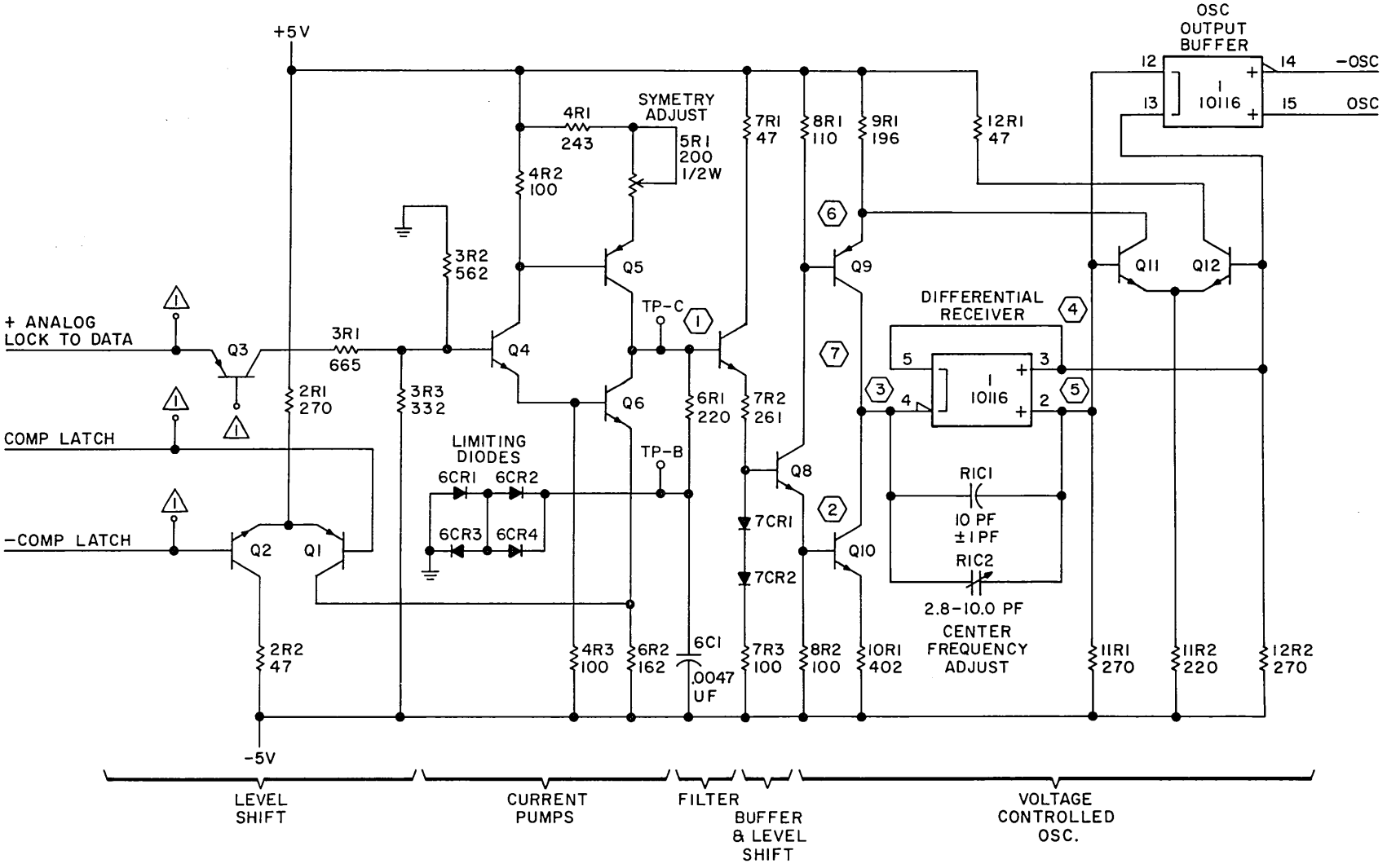
Level Shifter

Transistors Q1 and Q2 shift the ECL voltage levels, received from the comparator latch, to the levels required to control the current pumps. Current flows through either transistor Q1 or Q2 depending upon which has the more negative base. When the base of transistor Q1 is more negative, it conducts and provides the current to turn off transistor Q6. When the base of transistor Q2 is more negative, transistor Q1 turns off and transistor Q2 conducts, causing current flow through resistor 2R2 to the -5 volt supply. Turning off transistor Q1 allows transistor Q6 to turn on.

Current Pump

Transistors Q5 and Q6 form the current pump circuit. The conduction of transistor Q6 is determined by the voltage drop of resistor 6R2 compared to the base voltage of transistor Q6 (which is the drop across resistor 4R3). If transistor Q1 (see level shift circuits) is turned off, the voltage drop across resistor 6R2 is less than the transistor Q6 base voltage and transistor Q6 will have a constant collector current. However, if transistor Q1 is turned on, more current flows through resistor 6R2 causing a larger voltage drop. This causes the emitter of transistor Q6 to be more positive than its base thus turning it off. Transistor Q5 conducts regardless of the state of transistor Q6.

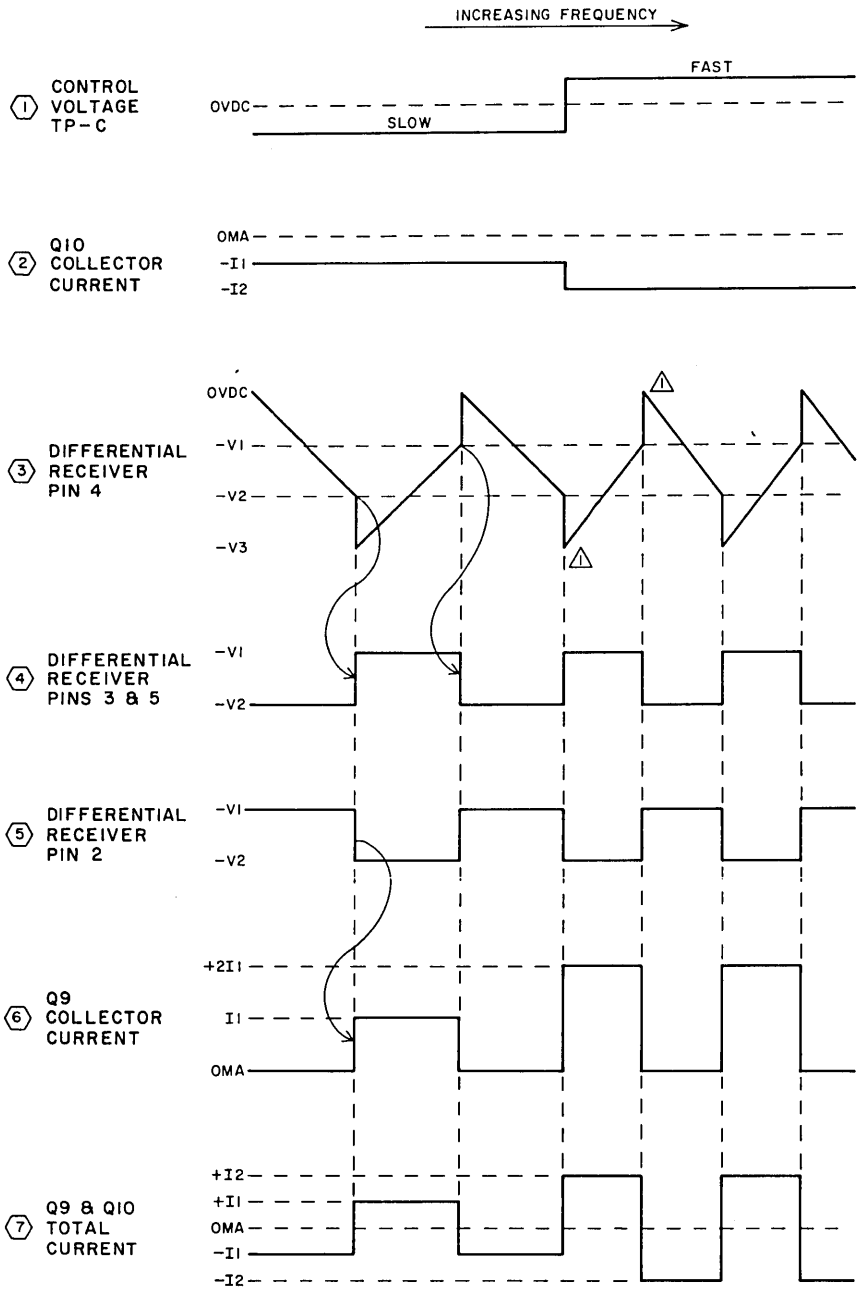
The gain of the current pumps is controlled by the Analog Lock to Data signal. Transistor Q3 converts the ECL Levels of this signal to a current which controls the bias of emitter follower transistor Q4. An ECL "0" on the emitter of transister Q3 leaves it turned off. This decreases the conduction of transistor Q4 and the gain of the current pumps. An ECL "1" on the emitter of transistor Q3 causes it to saturate, thus increasing the conduction of transistor Q4 and the gain of the current pump, changing the conduction of transistor Q4 controls the gain of the current pump by changing the voltage drops across resistors 4R2 and 4R3. These resistors determine the base voltages (and gain) of the current pump and since resistor 4R2 equals resistor 4R3 these base voltages will always be equal.



NOTES:

1. TERMINATED TO PROVIDE PROPER VOLTAGES AT THESE POINTS.
2. CIRCUIT VALUES ARE FOR REFERENCE ONLY. ACTUAL VALUES MAY VARY.
3. NUMBERS ⬡ REFER TO TIMING ON FIGURE 3.

Figure 2



NOTES:

1. POSITIVE FEEDBACK FROM PIN 2 PUSHES CAPACITORS PAST REFERENCE VOLTAGES THUS PRODUCING FASTER SWITCHING.
2. NUMBERS ⬡ REFER TO SCHEMATIC ON FIGURE 2.

Figure 3

The symetry of the output current waveform is adjusted by varying resistor 5R1 which controls the base emitter bias of transistor Q5. Resistor 5R1 is normally adjusted so that when the input to the level shifter (from the comparator) has a duty cycle of 50%, the conduction of transistor Q5 is one half that of transistor Q6. This produces a square wave output current to the filter circuit.

Filter

The filter consists of resistor 6R1, capacitor 6C1 and limiting diodes 6CR1 through 6CR4. The output from the current pump flows through resistor 6R1 producing a square wave voltage. This voltage is integrated by capacitor 6C1 thus creating an average dc level. The resultant voltage (square wave plus average) acts as a control voltage and determines the instantaneous frequency of the voltage controlled oscillator (VCO). The average dc level defines the average VCO frequency. Changes in the duty cycle of the current-pump. Square-wave output immediately affects the voltage across resistor 6R1 and gradually changes the average dc level.

The nominal VCO frequency is obtained when the control voltage is 0 volts. The limiting diodes (6CR1 through 6CR4) limit the average voltage change to ±1.2 volts or a VCO frequency change of about ±20%.

Buffer and Level Shifter

The buffer circuit consists of emitter follower transistor Q7, which presents a high impedance to the filter and a low impedance to the oscillator circuit. Resistor 7R1 limits current in the collector of transistor Q7.

Resistors 7R2 and 7R3 form a voltage divider and level shifter circuit that obtains the proper VCO frequency to control voltage function. Diodes 7CR1 and 7CR2 compensate for the base emitter drops of transistors Q8, Q9 and Q10 in the oscillator.

Voltage Controlled Oscillator

The VCO output frequency varies as a function of the buffered control voltage received via Q7. This voltage is applied to the base of emitter follower transistor Q8. The current through transistor Q8 and resistors 8R1 and 8R2 define equal base voltages on transistors Q9 and Q10; therefore, their output currents will vary in direct proportion to one another as a result of a change in control voltage.

Transistor Q9 is switched on and off by transistor Q11; however, transistor Q10 is controlled only by the voltage drop across resistor 8R2. When transistor Q9 is off, transistor Q10 discharges capacitors R1C1 and R1C2 as shown in Figure 3. The voltage on the capacitors is sensed by input pin 4 of the differential receiver which compares it to input pins 3 and 5 (which have ECL "1" and "0" levels). When the capacitor voltage discharges to reference level -V2 the differential receiver switches; (see timing on Figure 3). This causes transistor Q11 to decrease its conduction to a level which allows transistor Q9 to turn on.

When transistor Q9 is on, it provides twice the current of transistor Q10. One half of this current supplies transistor Q10 and the other half charges the capacitors. Transistor Q9 charges the capacitors at the same rate as transistor Q10 discharged them. When they charge to level -V1 (see Figure 2), the differential receiver switches again, this time increasing the conduction of transistor Q11 to a level that causes transistor Q0 to turn off.

Output pin 2 of the differential receiver provides positive feedback through capacitors R1C1 and R1C2 to ensure clean fast switching.

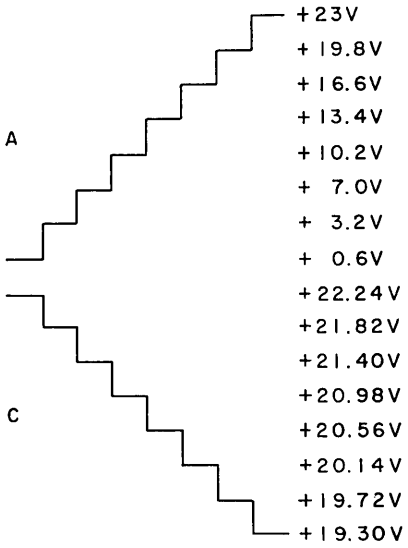
As shown on Figure 3, the output frequency of the oscillator varies directly with the control voltage. The center frequency of the oscillator is changed by adjusting R1C2.

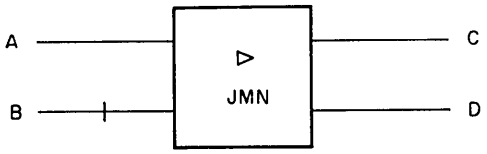
The oscillator output buffer prevents external loading from affecting the oscillator.

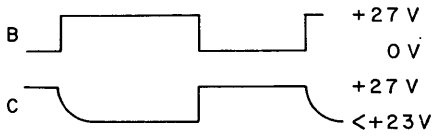
VOLTAGE CONTROLLED CURRENT SOURCE - JMN

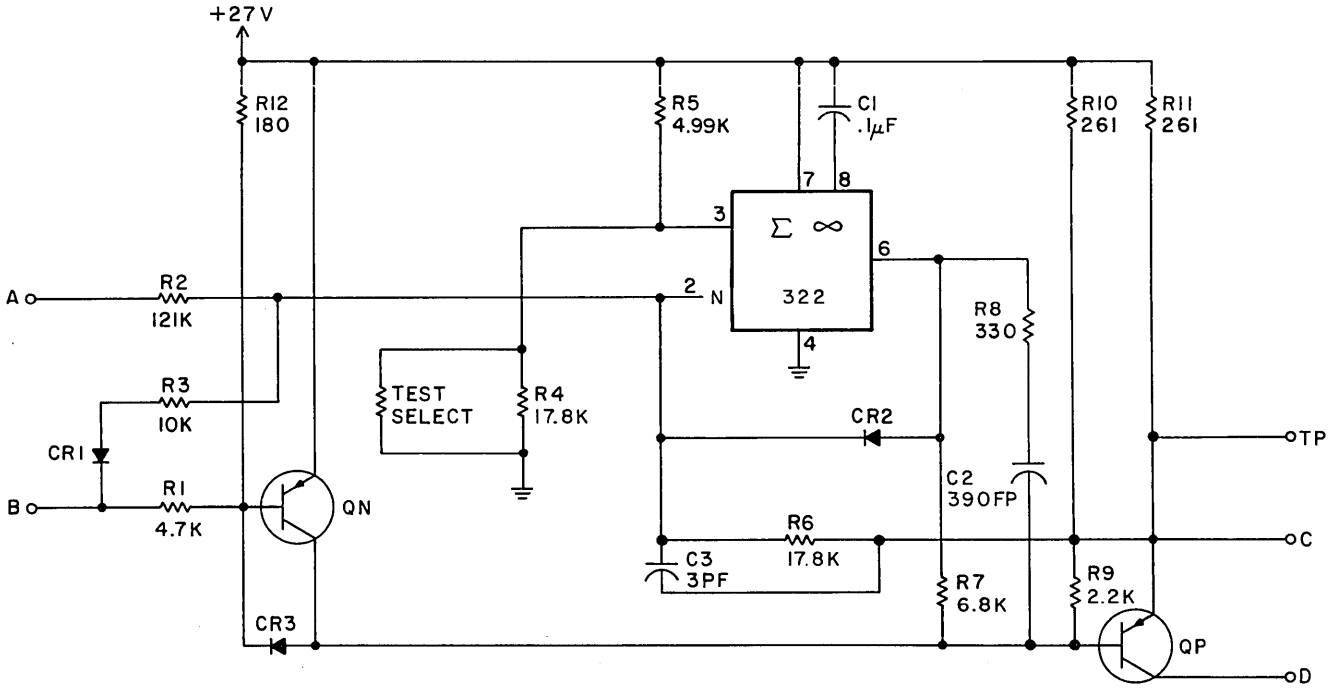
The JMN circuit accepts an analog input voltage and converts it to a voltage controlled current for the write driver.

The JMN circuit receives the analog output of a digital to analog converter. The 322 operational amplifier in the JMN circuit inverts the analog input at A and translates the voltage level to drive the base of current source transistor QP. Write current output is supplied at output D. Current sensing is provided at output C so that other circuitry can test for proper current level output. Control from a write current protect circuit is applied to input B. Current is supplied at output D when input B is +27V. Current source transistor QP is shut off when input B goes to ground.





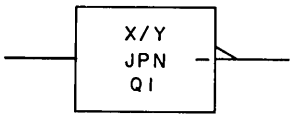


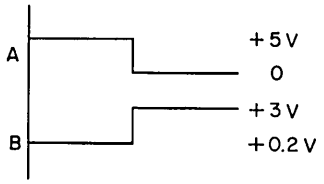


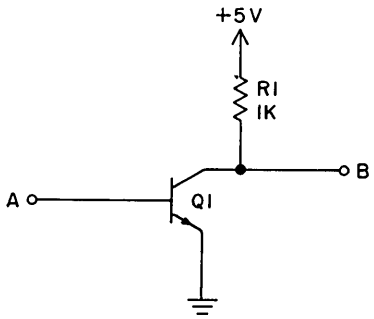
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

Current Preamp - JPN

The JPN circuit is used for expanding the fan out capabilities of TTL circuits following this circuit. In a typical circuit the JPN is driven by a open collector output TTL circuit. When input A is driven low, Q1 shuts off and output B goes to +5V. With a high at input A, Q1 turns on, driving output B to about +0.2 volts.

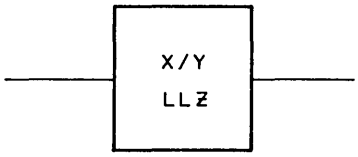


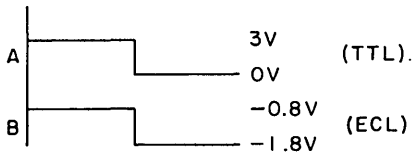


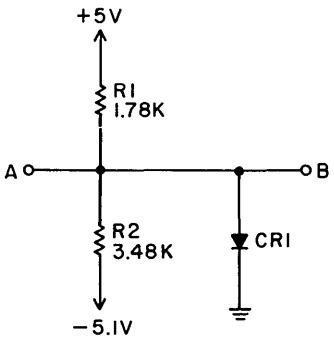


PASSIVE TRANSLATOR (TTL TO ECL) - LLZ

R3 and R2 form a resistor divider that changes normal (and worst case) TTL levels into normal (and worst case) ECL levels. A "1" TTL will translate into a "1" ECL. R1 serves as a pullup in case there is no input and causes a "1" to be outputted. CR1 is a germanium clamp to limit the output voltage to +0.2 in case an input voltage of +5 or greater is applied.





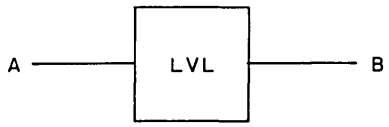


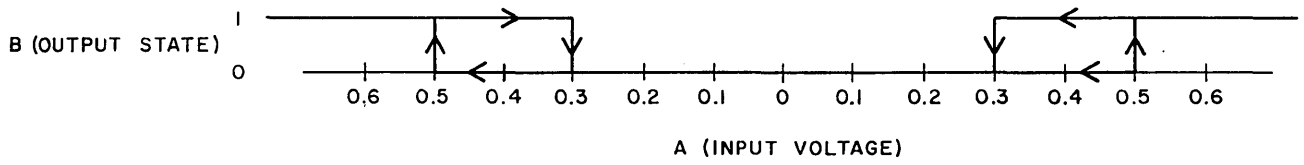
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

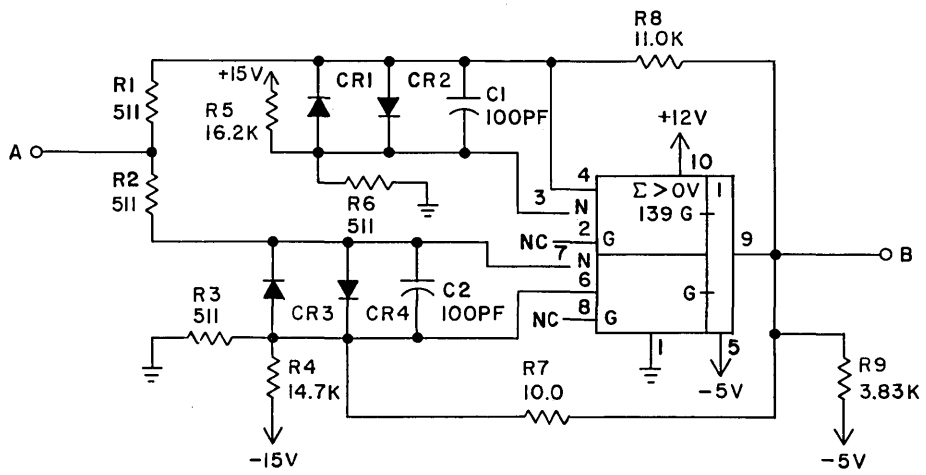
ANALOG TO DIGITAL CONVERTER - LVL

The LVL circuit is an analog to digital converter. The state of the digital output voltage at B is dependent upon the value of the input voltage at A.

The LVL circuit is used to convert the fine servo signal to a digital level. The digital output signal of the LVL circuit inhibits the On Cylinder signal. When the value of the signal at input A goes from greater than ±0.5 V toward 0 V, output B goes to a logical 0 as the input signal crosses ±0.3 V. As the signal at input A goes from 0 V toward greater than ±0.5 V, output B goes to a logical 1 as the input signal crosses ±0.5 V.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

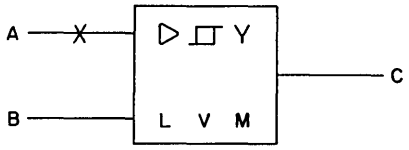
VOLTAGE COMPARATOR - LVM

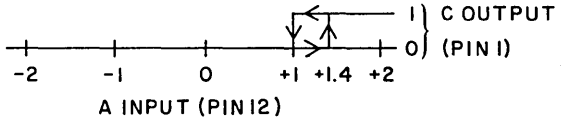
The LVM circuit compares a voltage at input A against a reference voltage and produces a bilevel digital signal at output C.

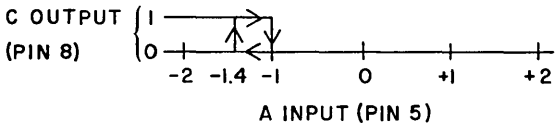
The following discussion describes an LVM circuit using one half of a 310 integrated circuit and using a positive reference voltage. The LVM can also be used with a negative reference voltage having the output as shown in the waveform diagrams.

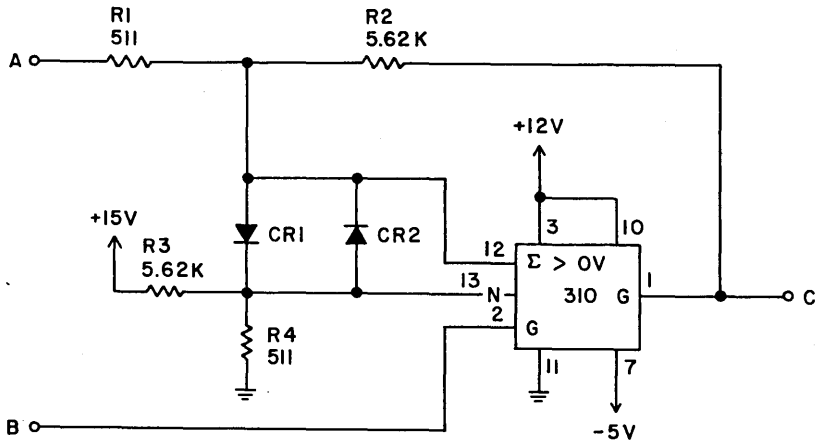
A reference voltage is established at pin 13. When input A goes in a positive direction to +1.4 V, output C goes to a TTL level "1". When input A goes in a negative direction to +1.0 V, output C goes to a TTL level "0".

Input B is used to enable or disable the LVM circuit. When input B is a "1", it enables the circuit. When input B is a "0", it disables the circuit and forces a constant "0" output at C.









NOTES: 1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
2. LVM CIRCUIT USING POSITIVE REFERENCE VOLTAGE.

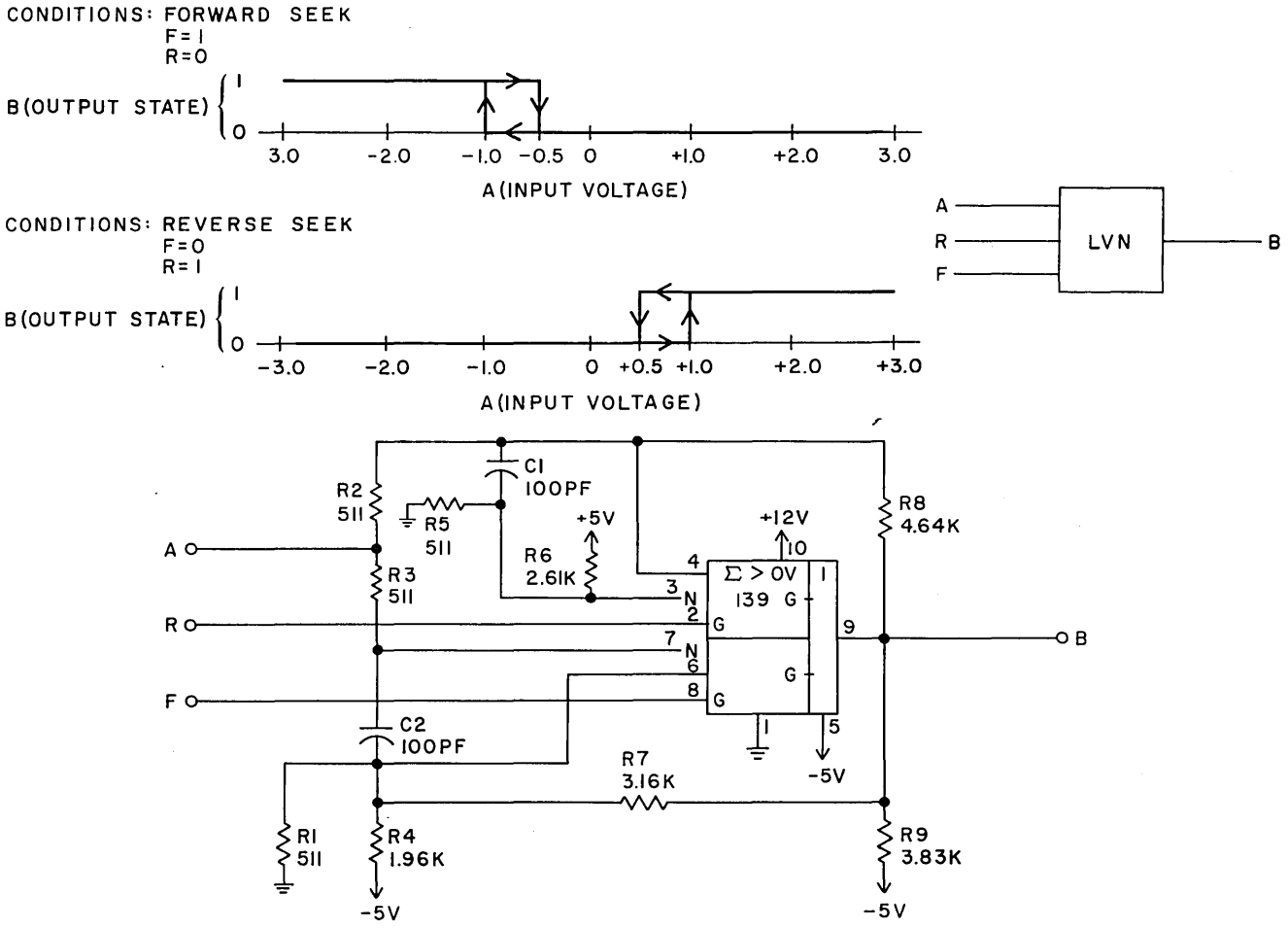
ANALOG TO DIGITAL CONVERTER - LVN

The LVN circuit is an analog to digital converter. The state of the digital output voltage at B is dependent upon the value of the input voltage at A and the logical states of R and F.

The LVN circuit is used to convert the coarse command error signal (summing amplifier output) to a digital level. The digital signal output of the LVN circuit enables the power amplifier of the drive to operate in the switching mode, thereby reducing transistor power dissipation during the coarse positioning mode. Two enable controls, reverse (R) and forward (F), are used to gate the proper circuitry.

The analog voltage at input A is representative of the carriage drive signal. This voltage varies between a nominal plus and minus 2.9 volts. During a forward full seek, input A changes polarity from +2.9 V to -2.9 V when the pre-programmed circuits determine that carriage acceleration is required. Also during the forward seek, forward enable (F) is a logical 1. The result of these two conditions is that output B goes to a logical 1. When B is at a logical 1 the power amplifier is turned on. When carriage acceleration is determined to be sufficient, A goes from -2.9 V toward +2.9 V. Then B goes to a logical 0, and the power amplifier is turned off. During deceleration output B switches alternately from logical 0 to logical 1 to switch the power amplifier on and off as required.

LVN circuit functions during a reverse seek are complementary to a forward seek, except that a logical 1 at B still turns on the power amplifier and a logical 0 at B turns it off.

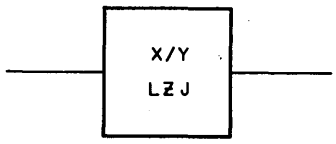


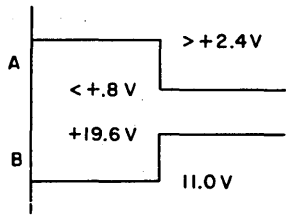
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

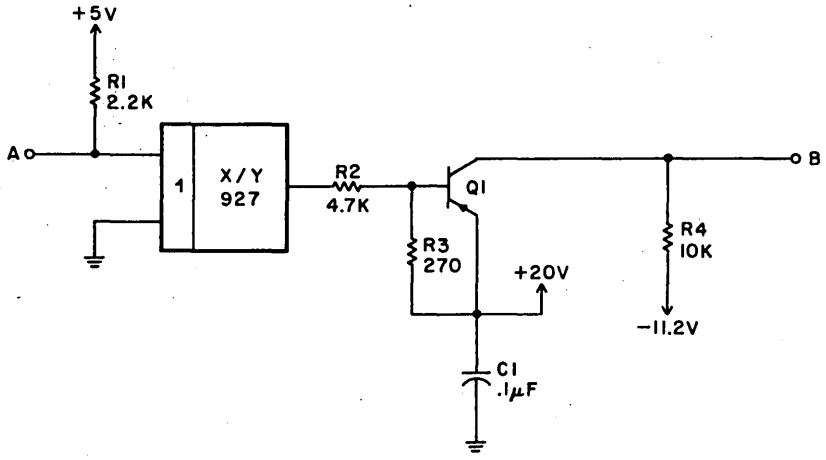
Level Translator/Read Enable - LZJ

The read enable circuit is enabled when the input is low (TTL level), thus causing the output to go to almost +20v and enabling the read matrix. A low on the input of the 927 turns on its output transistor and current flows from +20v thru the emitter base junction of Q1, thru R2 and the output transistor collector to emitter of the 927. This puts the collector of Q1 at just below +20v.

A high on the input of the 927 turns the open collector output transistor off and prevents current from flowing from emitter to base of Q1, thus turning off Q1. With Q1 off the pull down resistor (R4) takes the output to approximately -11v. This back biases the head select diode matrix to a negative level sufficient to prevent write spikes from causing damage by entering the read preamp.



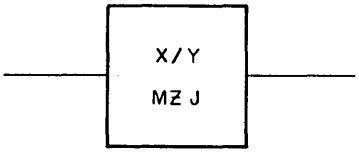


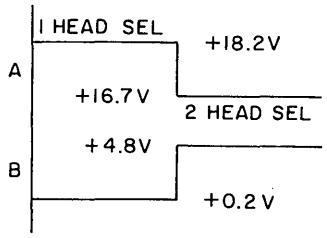


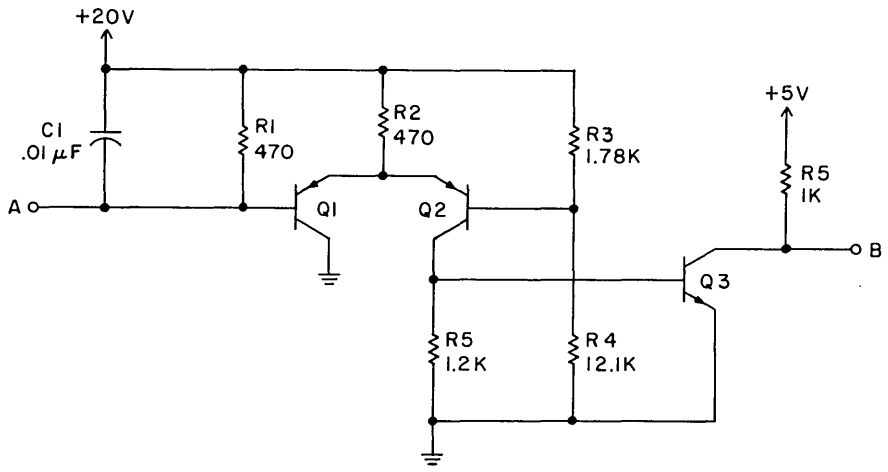
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

Level Translator - MZJ

The multiple select fault circuitry uses a differential voltage comparitor to sense if two or more heads are selected. A voltage reference of +17.4v is established at the base of Q2 with no head selected. With one head selected the voltage at the base of Q1 will be 18.2v, thus Q2 and Q3 will conduct keeping the output of Q3 low (TTL level) indicating no fault. If two or more heads are selected at the same time the base voltage at Q1 will be 16.7v or greater causing Q1 to conduct and Q2 and Q3 to turn off. The output will then go high a (TTL level) indicating a fault.

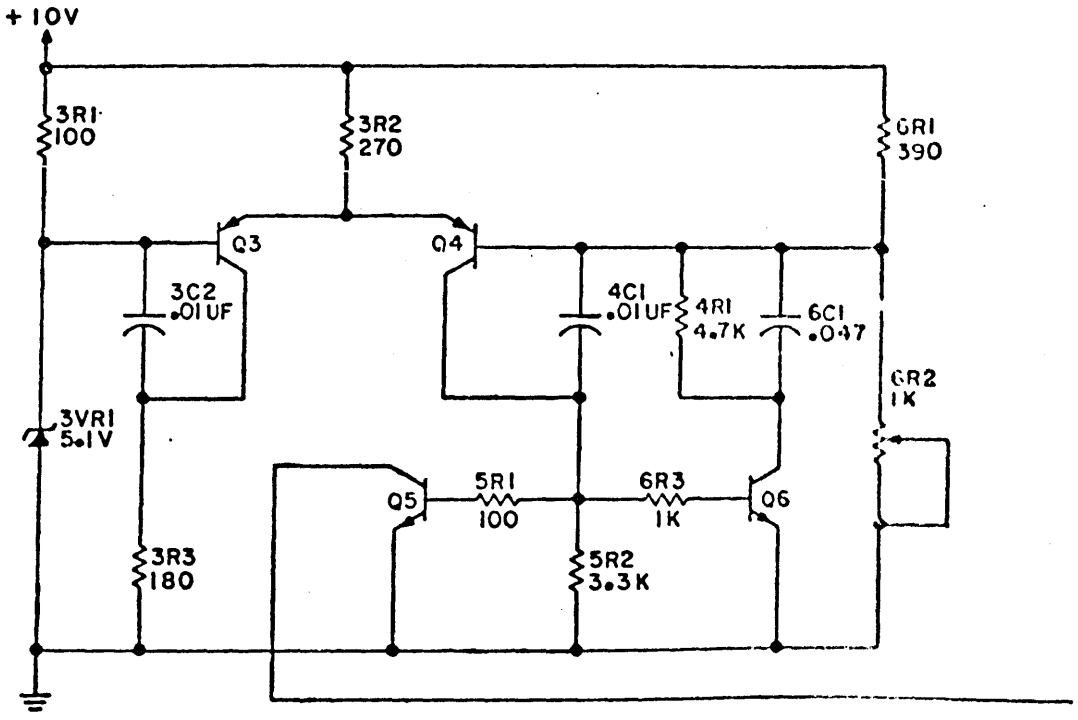






NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

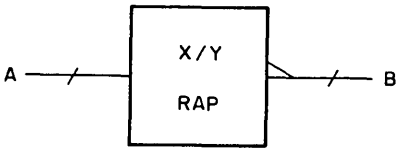
Circuit description to be supplied at a later date.

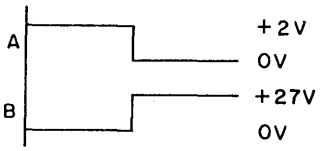


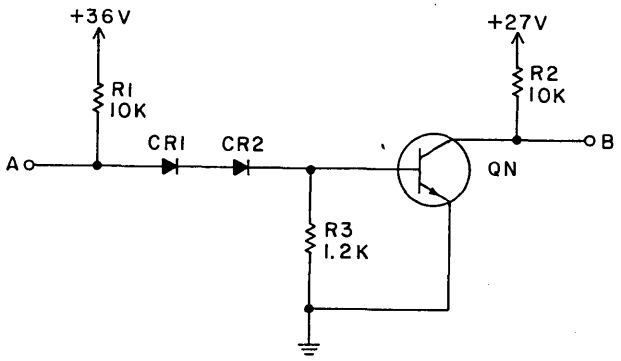
WRITE PROTECT CLAMP - RAP

The RAP circuit acts as a clamp, changing its output impedance path from high to low when the input is switched high.

When the input at A is low (TTL) Q1 is turned off, and the impedance from B to ground is high. When A is switched high (TTL) Q1 is turned on, providing a low impedance path between output B and ground for the write current.





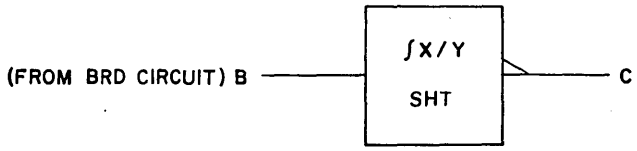


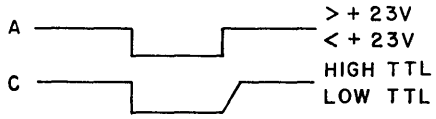
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

LEVEL TRANSLATOR (OUTPUT SECTION) - SHT

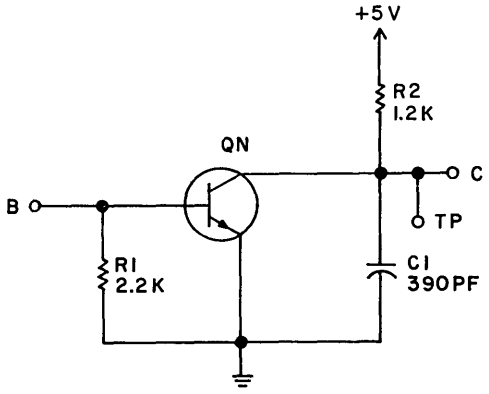
The SHT circuit provides a TTL compatible output for the comparator section of a level translator.

The SHT circuit functions in conjunction with the BRD circuit to indicate whether or not the write current is below a minimum value. (See BRD circuit description.) The output of the BRD circuit provides bias for transistor QN to turn it on or off. When the write current falls below +23V, QN is turned on to provide a low level TTL output. When the write current is above +23V, QN is turned off to provide a high level TTL output.





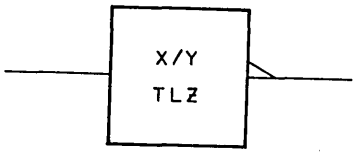
NOTE: A IS INPUT TO BRD CIRCUIT
C IS OUTPUT OF SHT CIRCUIT

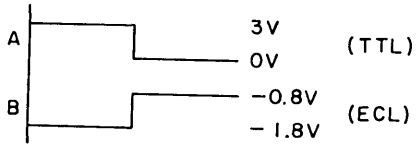


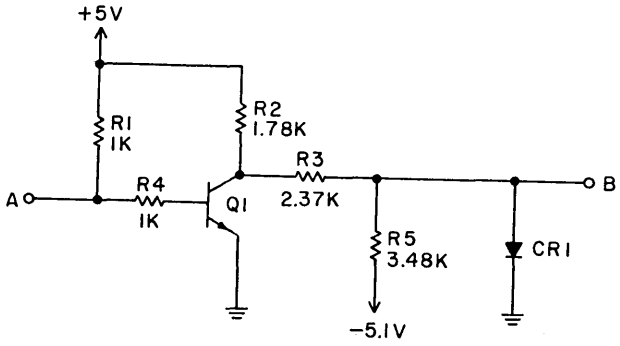
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

INVERTING TRANSLATOR (TTL TO ECL) - TLZ

The first part, consisting of R_1, R_4 and Q_1 form a simple transistor inverter to turn TTL "1's" into TTL "0's". The second part, R_2, R_3, R_5, and CR_1, form a LLZ passive translator which produces ECL levels from TTL inputs.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

DELAY - UB-

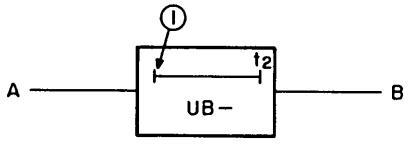
The capacitor delay circuits delay a "1" input at A for a specified period of time before providing a "1" output at B. Delay time for a "0" pulse is negligible.

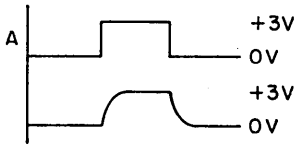
Assume a "0", ground, enters at A. If the capacitor is discharged, it remains discharged and the output remains "0". If the capacitor is charged when the "0" signal appears, the capacitor discharges almost instantaneously, and the "0" appears with no noticeable delay.

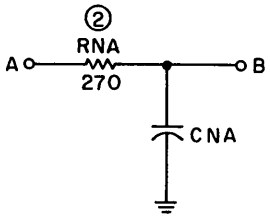
If a "1", +3 volts, enters A while the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage before a "1" can appear at B. The required charge time is the delay time of the circuit. The charge time is dependent on the capacitor value, the resistance between the source voltage and the capacitor, and the minimum voltage required to produce a "1" output.

Delay times for capacitive delays used are as follows:

Delay Type	Time	CNA	RNA
UBR	40 NS	2200 PF	None
UBS	25 NS	680 PF	None







NOTES:

① COMPONENT VALUES VARY.

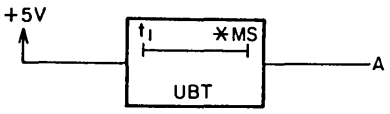
② USED ON UBR AND UBS ONLY.

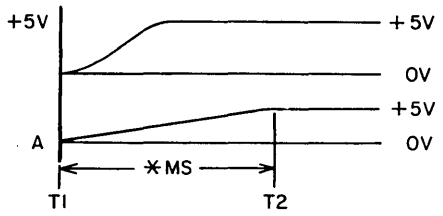
3 VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

DELAY - UBT

The UBT delay circuit delays application +5 volts to a standard TTL gate during a power up sequence.

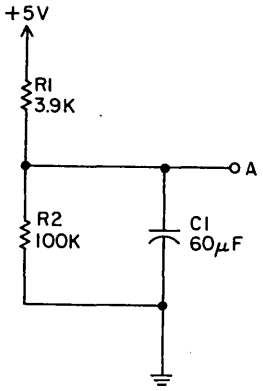
Applying +5v (T1) slowly raises output A to +5 volts as C1 is charging. As the voltage across C1 approaches 5 volts, output A raises to 5 volts after a specific delay time determined by the values of R1, R2, and C1.





* TYPICAL DELAY TIMES

R1	R2	C1	DELAY TIME
3.9K	100K	60μF	80 MS
6.8K	10K	60μF	30 MS



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

DELAY - UC-

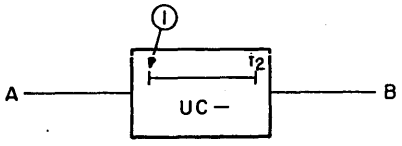
The UC-delay circuit is used to delay open-collector integrated circuits. The circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v and a capacitor connected to ground.

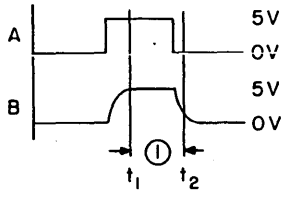
Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

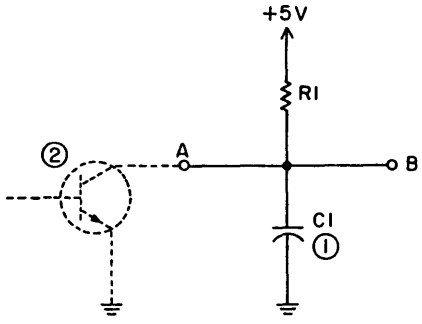
If a "1" (+3.0v) enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.

Characteristics of the UC-circuits are as follows:

Circuit Type	Capacitance	Resistance	Delay
UCM	5600PF	1.2K	1.5US
UCP	5600PF	560	0.8US
UCR	5600PF	1K	1.3US
UCS	3.3UF	2.2K	1MS
UCV	270PF	2.61K	175NS
UCY	200PF	10K	200NS





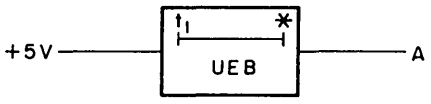


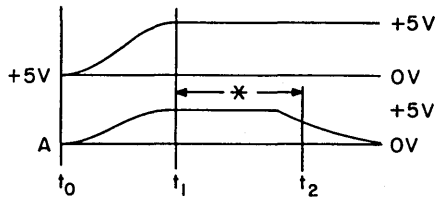
NOTES:
① DELAY TIME DEPENDENT ON CIRCUIT TYPE.
② OPEN COLLECTOR TRANSISTOR IN PRECEDING STAGE.

DELAY - UEB

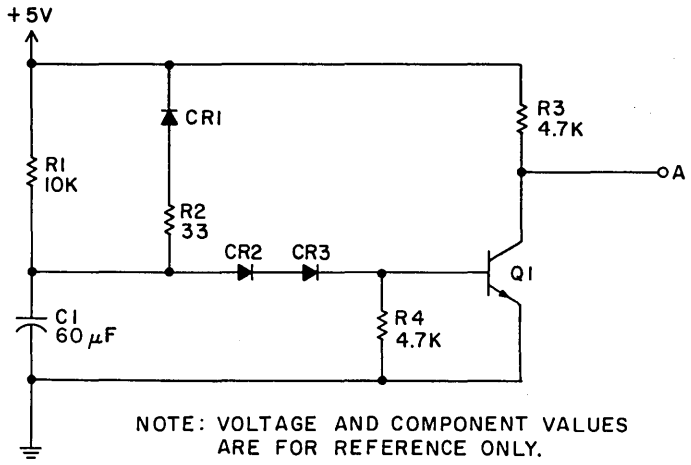
The UEB circuit delays application of ground to a standard TTL gate during a power-up sequence.

During power off phase (T_0), capacitor C1 is discharged by R4, CR2, and CR3. Applying +5v power (T_1) raises output A to +5v as power comes up. At this time (T_1) Q1 is off and C1 is charging. As the voltage across C1 approaches 5 volts, Q1 turns (T_2) on reducing output A to about 0 volts.





* DELAY TIME VARIES WITH COMPONENT VALUES, SEE LOGIC DIAGRAMS FOR SPECIFIC DELAY TIME.



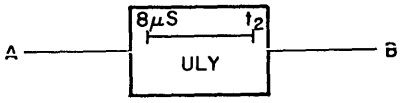
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

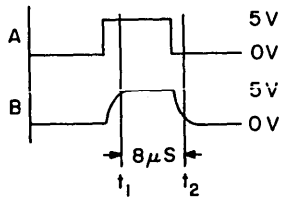
DELAY - ULY

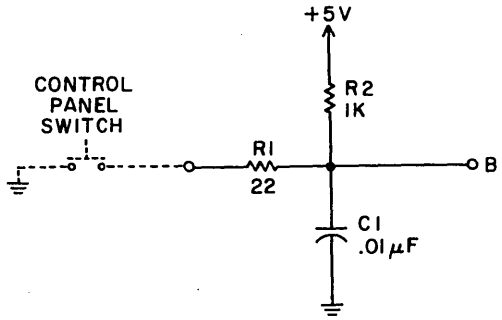
The ULY-delay circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v, a capacitor connected to ground, and a series input resistor.

Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

If an open circuit ("1") enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.





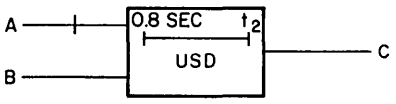


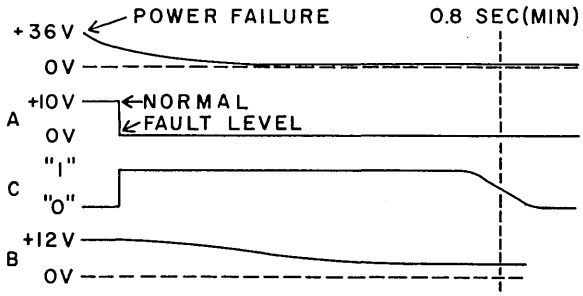
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

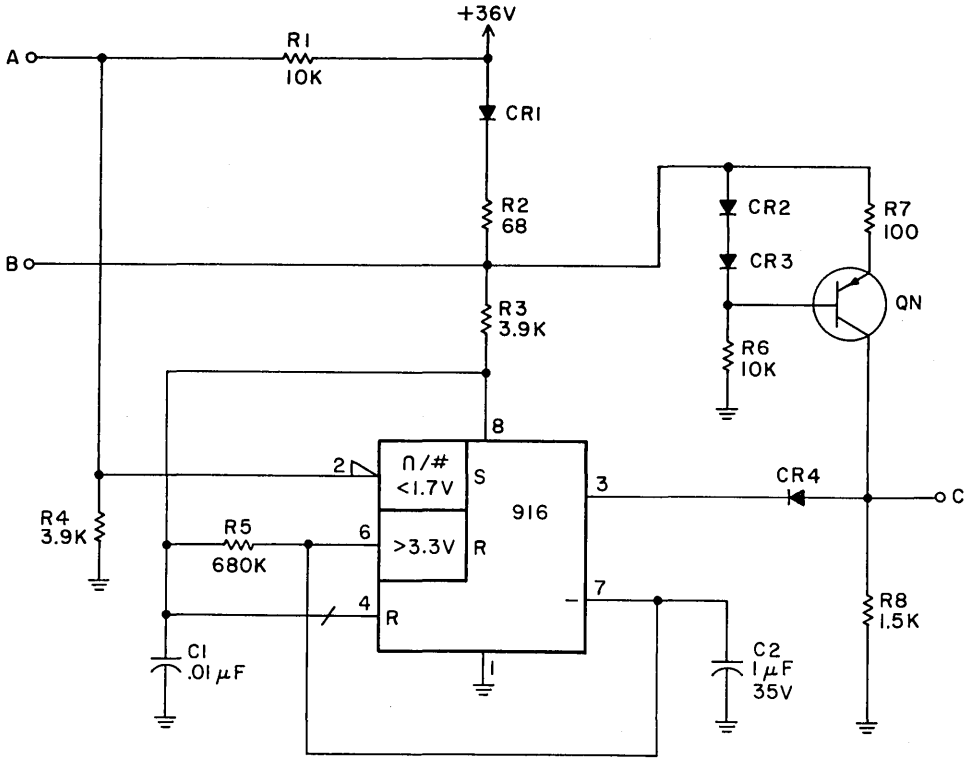
DELAY - USD

The USD circuit maintains a TTL high level output for 0.8 sec during the time that the power supply voltage is dropping.

The USD circuit functions as the delay portion of a write fault clamp circuit which prevents write current from reaching the head during a +36 V supply voltage fault condition. The switching action of transistor QN is initiated by the fault trigger at input A. QN is turned on when input A goes to 0 V, causing output C to go high. Resistor R5 and capacitor C2 provide the time-out constant to keep output C high for 0.8 sec. Stored energy is supplied at input B to maintain QN in the on state for the 0.8 sec duration. The high output at C is used to switch on a write clamp circuit.





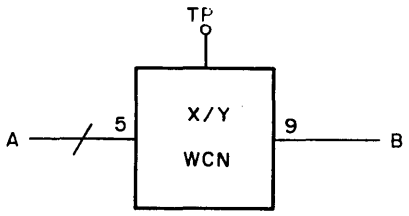


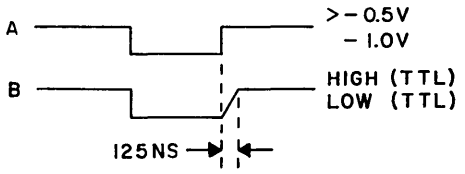
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

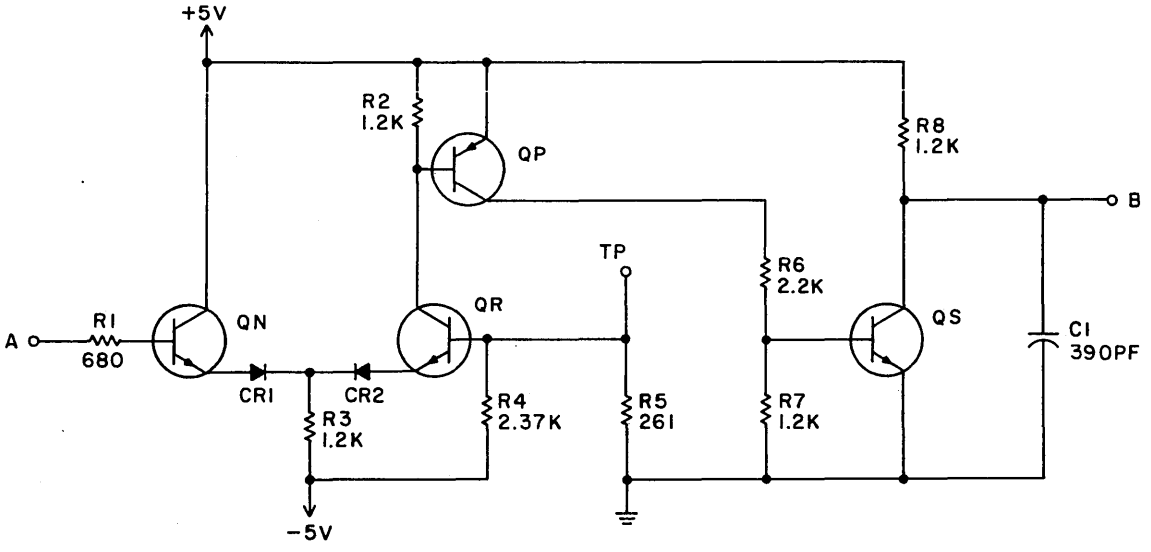
LEVEL TRANSLATOR - WCN

The WCN circuit translates input signal levels of below -0.5 V to a low TTL level output and input signal levels of above -0.5 V to a high TTL level output.

The WCN circuit has a differential voltage comparator circuit to indicate whether the write driver is on or off. A voltage reference of -0.5 V is applied to the base of transistor QR. When the write driver is off, the voltage at the base of transistor QN is -1 V, turning off QN. Therefore, transistor QR is turned on and its collector voltage goes low, turning on transistor QP. Transistor QS is then forward biased providing a low TTL output. If the write driver is on, the voltage to the base of QN goes above -0.5 V (less negative) and QN is turned on. As a result QR, QP, and QS are turned off, providing a high TTL output. Capacitor C1 delays the low to high transition by 125 ns.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

COMMENT SHEET

MANUAL TITLE:

PUBLICATION NO.: **REVISION:**

NAME: _____

COMPANY: _____

STREET ADDRESS: _____

CITY: _____ **STATE:** _____ **ZIP CODE:** _____

This form is not intended to be used as an order blank. Control Data Corporation welcomes your evaluation of this manual. Please indicate any errors, suggested additions or deletions, or general comments below (please include page number references).

☐ Please Reply ☐ No Reply Necessary

CUT ALONG LINE

PRINTED IN U.S.A.

KØR-0502D

NO POSTAGE STAMP NECESSARY IF MAILED IN U.S.A.

FOLD ON DOTTED LINES AND TAPE. POSTAL REGULATIONS PROHIBIT THE USE OF STAPLES.

FOLD

FOLD

FIRST CLASS
PERMIT NO. 8241

MINNEAPOLIS, MINN.

BUSINESS REPLY MAIL

NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

POSTAGE WILL BE PAID BY

CONTROL DATA CORPORATION
TWIN CITIES DISK DIVISION
CUSTOMER DOCUMENTATION DEPARTMENT
5950 CLEARWATER DRIVE
MINNETONKA, MN. 55343

CUT ALONG LINE

FOLD

FOLD

CORPORATE HEADQUARTERS, P.O. BOX 0, MINNEAPOLIS, MINN. 55440
SALES OFFICES AND SERVICE CENTERS IN MAJOR CITIES THROUGHOUT THE WORLD

LITHO IN U.S.A.

CONTROL DATA CORPORATION