CONTROL DATA
CORPORATION

CONTROL DATA®
3234 MASS STORAGE CONTROLLERS

HARDWARE REFERENCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
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B	Manual revised; incorporates Engineering Change Order 32840 which incorporates Field Change
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PREFACE

This publication contains reference information for CONTROL DATA® 3234-A/B/C/D/E Mass Storage Controllers which may be used with the CONTROL DATA® 3000 Computer Data Channels. The user of this manual should be familiar with the Control Data 3000 Series Data Channel I/O specifications and operating characteristics.

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GENERAL DESCRIPTION 1

INTRODUCTION

The 3234 Mass Storage Controller interfaces 3000 computer system data channels and one or more of the peripheral storage devices listed in Table 1-1. The controller, data channel, and one or more storage devices comprise a mass storage subsystem. The controller synchronizes data transfer and controls the programmed selection of operating modes between the data channel and storage devices (refer to Figure 1-1). This manual provides descriptive, programming, and operating information for the mass storage subsystem.

The following are the peripheral storage devices.

- Special Option 60076 (adapter)† - The special adapter chassis (housed in the controller cabinet) interfaces the controller logic to the strip file.
- Disk File - Either the 813 or 814 Disk File unit and cabinet in which the disks and associated electronics are housed
- Disk Drive - Either the 853 or 854 Disk Storage Drive units, their associated disk pack, and the cabinet in which the pack and associated drive unit logic are housed
- Disk Pack - The 850 Disk Pack assembly consisting of 10 recording disks mounted on a common vertical axis. Each disk is approximately 14 inches in diameter. The packs are portable and interchangeable among various disk drive units.
- Strip File†† - The 2321 Data Cell Storage unit and the cabinet in which the cells, subcells, strips, associated logic, and electronics are housed
- Data Cell† - The strip file storage assembly. Each cell consists of 20 sub-cells each containing 10 recording strips. The cells are portable and interchangeable between the various strip file units. A full complement of 10 cells (either data or ballast) is required to complete the array necessary for strip operations.†
- Ballast Cell† - A dummy cell used to maintain the proper balance of the array when less than a full complement of data cells is used

Figure 1-2 shows a disk pack and a data cell in their protective containers.

† Applies to 3234-A/B/C models only

†† Throughout the manual the IBM 2321 Data Cell will be referred to as the strip file.

TABLE 1-1. CONTROLLER APPLICATIONS

Applicable Storage Devices and/or Error Recovery Capability				
Controller Model	813/814 Disk File	853/854 Disk Storage Drive	2321 Strip File Sp Opt 60076 Data Cell	Error Recovery Capability
3234-A	Yes	Yes	Yes	No
3234-B	Yes	Yes	Yes	No
3234-C	Yes	Yes	Yes	No
3234-D	Yes	Yes	No	Yes
3234-E	Yes	Yes	No	Yes

FUNCTIONAL DESCRIPTION

The controller, in conjunction with the applicable peripherals (singly or in any combination), operates as a mass storage subsystem having medium access time, nonvolatile, mass storage facilities. The subsystem provides large volume data storage with random access and interchangeable storage pack and data cell capabilities.

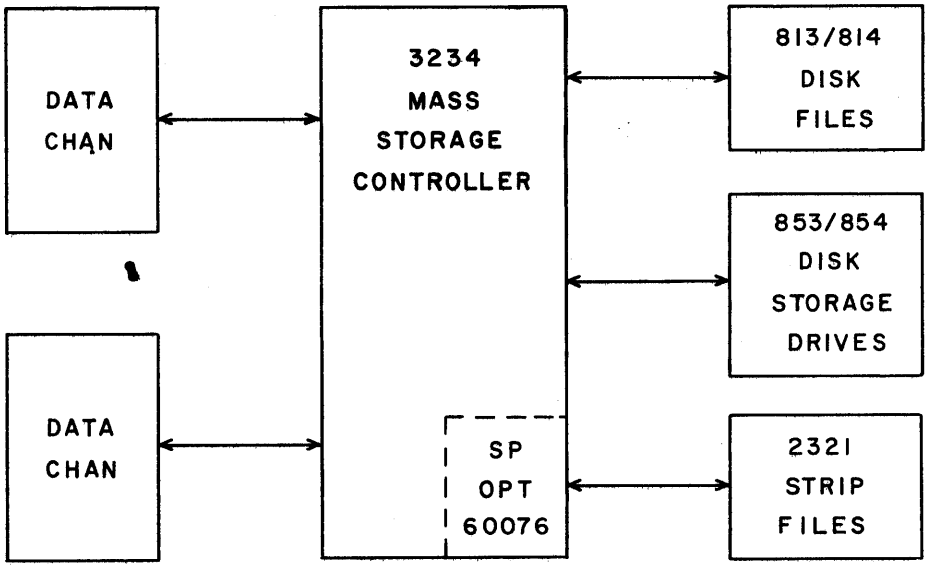

Figure 1-1. Typical Configuration

SUBSYSTEM CONFIGURATION

The mass storage subsystem has expandable capabilities. The minimum subsystem consists of a single data channel, a controller, and one of the storage devices. The subsystem can be expanded with the addition of a second data channel and additional storage devices. When two data channels are connected in the subsystem they operate on a time-shared basis.

The maximum subsystem consists of two data channels, a controller, and up to eight peripheral storage devices.† To incorporate strip file units into the subsystem for the applicable controller models, the adapter chassis (special option 60076) must be added to the controller. The adapter can accommodate up to four strip file units.

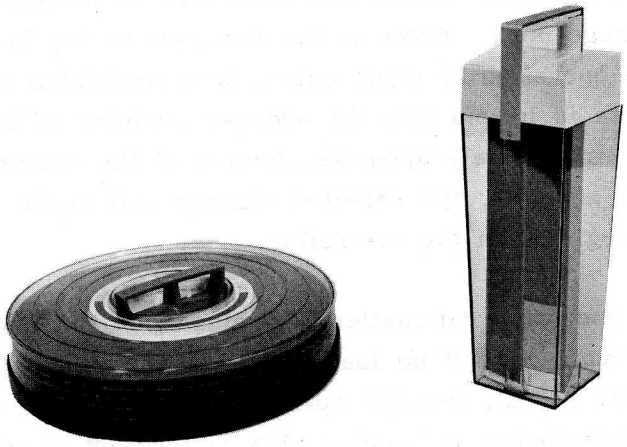

Figure 1-2. Disk Pack and Data Cell

The types of storage units used in the subsystem may be intermixed in any combination or may be all of one type. No provision is made for more than one adapter in the controller. Therefore, no more than four strip files may be connected to the controller.

The subsystem operates under program control from the computer. A 12-bit connect code selects the equipment (controller) and the unit (peripheral storage device). The 12-bit function codes provide for selecting operating modes, interrupts, and loading and unloading address information.

†The 814 Disk File is considered as two storage units.

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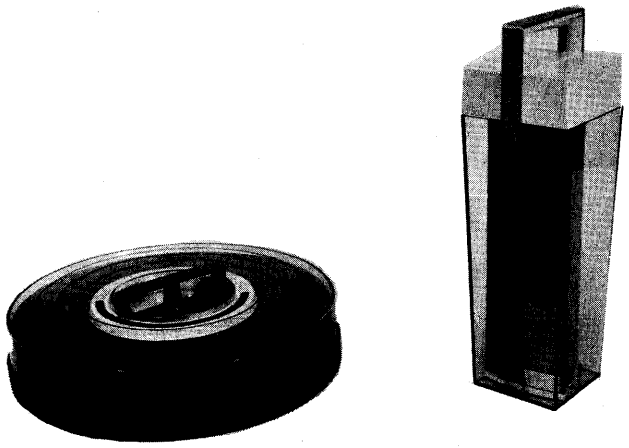

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CONTROLLER

The standard 3000 series signals are exchanged between the controller and the data channels. The controller translates the connect code and the function codes issued by the computer to control peripheral operation. The controller buffers data between the peripherals and the data channels. It accepts data from the data channels in a parallel format, disassembles it, and transmits the data serially to the appropriate storage unit. In a similar manner, the controller accepts serial data from the selected storage unit, assembles it into 12-bit bytes, and transfers it in parallel to the appropriate data channel.

The computer controls the subsystem operations through the 12-bit function codes and a 24-bit address word. Issuing a function code specifying the mode of operation prepares the controller and selected peripheral unit for an I/O operation. The issuance of a load address function code causes the controller to prepare for a seek operation† within the selected storage unit. Prior to the issuance of the load address code, the computer must do a write operation to issue output data containing address information to the controller. The data is loaded into the address register of the controller and the seek operation starts immediately upon termination of the output operation. If the address loaded is a legal address, the selected storage unit seeks the position specified by the contents of the register in the controller.

A sector verify operation automatically begins upon initiation of the I/O at the location specified by the address. If no load address operation is performed prior to receipt of a read or write signal, the I/O operation begins at the address presently held in the address register (cylinder and sector plus 1; location at which the previous operation ended)†† except when a unit is at the last legal address. In the latter case, a new seek must be initiated or an address error is generated. The 3234-D/E models contain error recovery procedures. A variety of functions are available for error identification and correction, depending on the type of error present.

---

†An operation in which the R/W heads are physically positioned to the addressed cylinder

††When an I/O operation is in progress (or ends) the controller automatically updates the address registers at the end of each sector except when an address error is detected, or when the abnormal EOP interrupt is selected and an abnormal condition occurs.

PERIPHERAL STORAGE DEVICES

The peripheral storage devices use a ferrous oxide coating as the magnetic recording medium.

The disk file and drive use the cylinder concept of recording to minimize positioner movement (Figure 1-3). The data is read or written consecutively from sector to sector within a track and from a track on one side of a disk to the same track on the opposite side of the same disk, then to the same track on the next sequential surface of the next disk, and so on. This method uses internal switching of the R/W heads to minimize positioner movement, which results in the data being recorded in a cylindrical drum-type pattern.

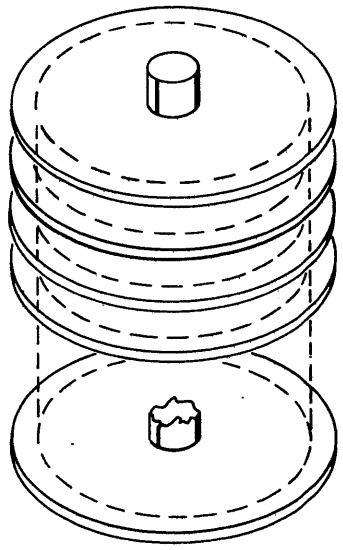


Figure 1-3. Cylinder Concept of Data Recording

DISK FILES

The 813 and 814 Disk Files are contained in similar cabinets (Figure 1-4). Each cabinet contains two drive spindles. A stack of 18 disks can be mounted on each half of the spindle (Figure 1-5). The 18 disks provide a total of 32 recording surfaces (the top and bottom surfaces are not used for recording). Each stack is subdivided into two groups. The spindles rotate (nonsynchronously) at approximately 1180 revolutions per minute less induction slip.

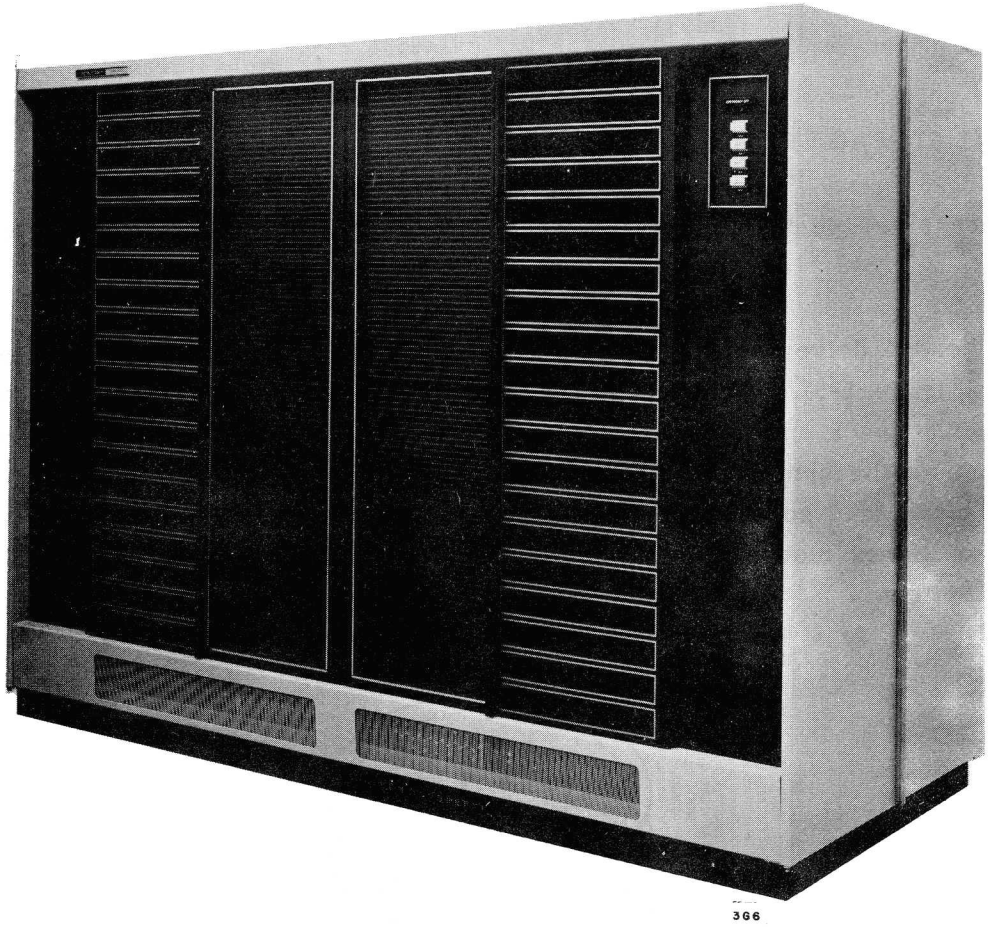
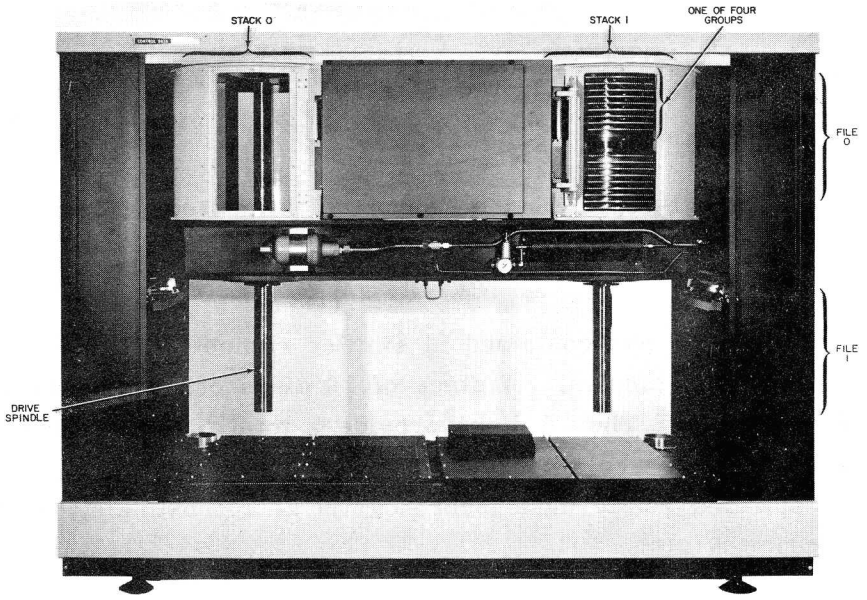


Figure 1-4. 813/814 Cabinet



2358

Figure 1-5. Disk File Physical Layout

Each disk is approximately 26 inches in diameter; each stack is approximately 18 inches high.

The 813 contains two stacks of disks mounted on the upper half of the spindles. A single hydraulically positioned access assembly serves the two stacks with two separate horizontally opposed groups of R/W head arms. Mounted on the end of each head arm are two head pads, each containing four R/W heads. There are four R/W heads for each of the 32 recording surfaces in a stack. The accesses (which move simultaneously in opposite directions) can be positioned to any of 64 positions to provide a total of 128 recording cylinders (64 per stack).

The 814 contains four stacks mounted on the two spindles with two independent hydraulically positioned access assemblies serving the four stacks. Each half (upper disks and positioner, or lower disks and positioner) of the 814 Disk File is considered an independent unit and is addressed, accessed, and operated on independently. Thus, access and operation to either half of an 814 Disk File is identical to the access and operation in an 813 Disk File.

DISK STORAGE DRIVES

The disk storage drives (Figure 1-6) are random access storage devices. The access mechanism consists of ten arms mounted in pairs on a movable carriage. Each pair of arms is positioned between two disks. A single R/W head is mounted on the extremity of each arm. On an initial seek (performed by loading a disk pack, closing the cover, and pressing the START switch), the carriage moves horizontally from an initially retracted position (to facilitate disk pack insertion and removal) to the first track near the edge of the disk. The unit then moves the heads to the innermost track and then withdraws the heads back to track 000. During the latter process, the heads are loaded (put in a recording attitude near the surface of disks).

The 853 and 854 Disk Storage Drives are contained in similar cabinets. The 853 has provisions for positioning to 100 cylinders; the 854 for positioning to 203 cylinders. Both types utilize the standard 851 Disk Pack; however, because track spacing is different in the two types of devices, a pack recorded on one type (for example, 853) cannot be read on the other type (for example, 854). The packs rotate at approximately 2400 revolutions per minute.

STRIP FILE†

The strip file (Figure 1-7) is a direct access storage device. The unit is capable of retrieving and restoring individual magnetic storage strips from an array of cells. The data is written and read from the strips which are approximately 13 inches long, 2-1/4 inches wide, and 0.005 inch thick. Each strip is coated on one side with an iron oxide recording medium and on the other side with an antistatic carbon coating.

Each file contains 2000 strips set in an array consisting of 10 removable cells and arranged in a vertical cylinder (Figure 1-8). Each cell is subdivided into 20 subcells with 10 recording strips per subcell. During operation, the array is hydraulically positioned (in the direction of least travel) to any of the 200 subcells. A mechanical linkage then selects the addressed strip, pulls it from its storage location, and places it on a small drum. The drum rotates the strip past a R/W head bar assembly. The assembly contains 20 R/W heads and can be positioned to any of five locations to provide access to the 100 recording tracks on the strip. When use of the strip is completed, it is restored to its original storage location in the subcell.

† Applies to 3234-A/B/C models only

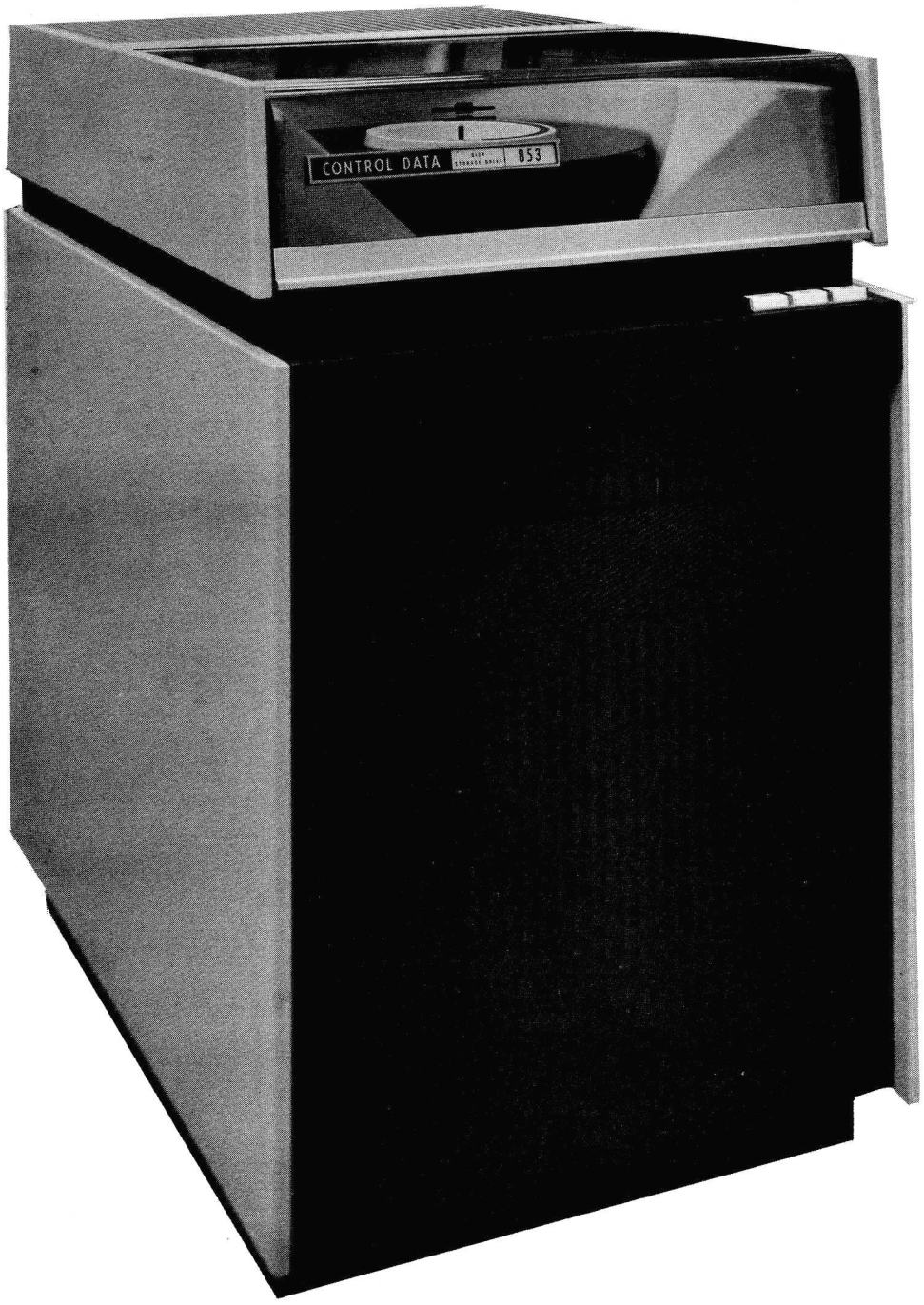


Figure 1-6. 853 Disk Storage Drive

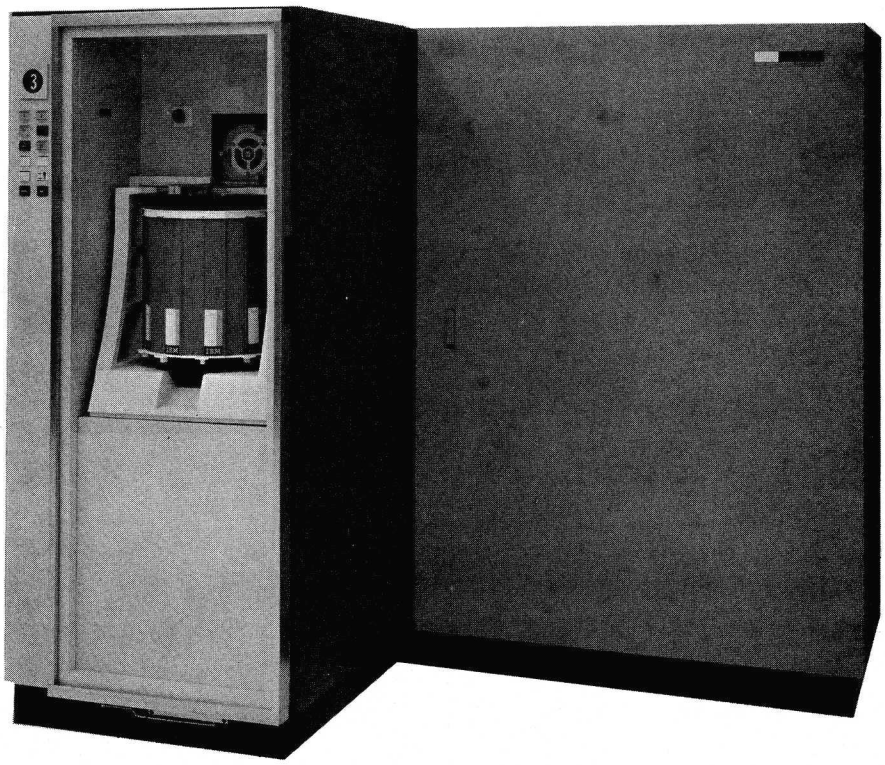


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Figure 1-7. Strip File

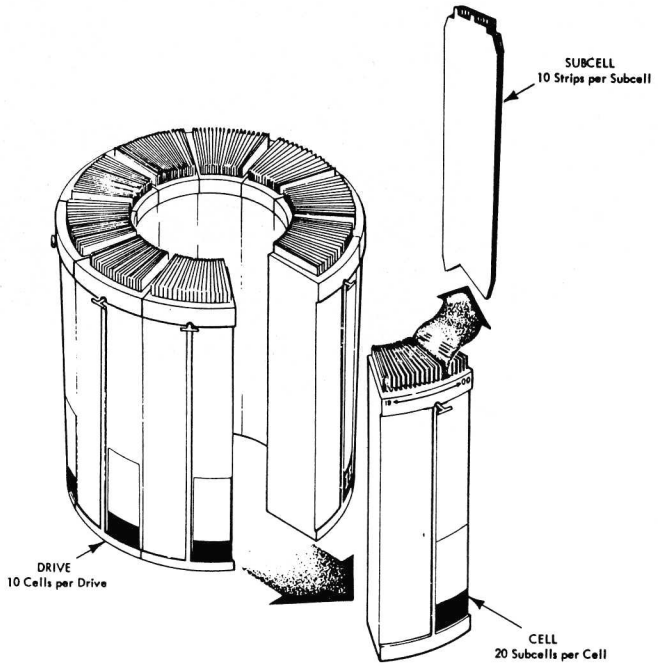


Figure 1-8. Array Subdivisions

DATA FORMAT

The basic data word consists of a 12-bit byte. Multiple bytes are recorded in each sector with multiple sectors recorded in each of the storage mediums. Physical arrangement of the tracks and cylinders in the storage devices varies dependent upon the device. Table 1-2 indicates the sector, track, and cylinder formats for the various storage devices.

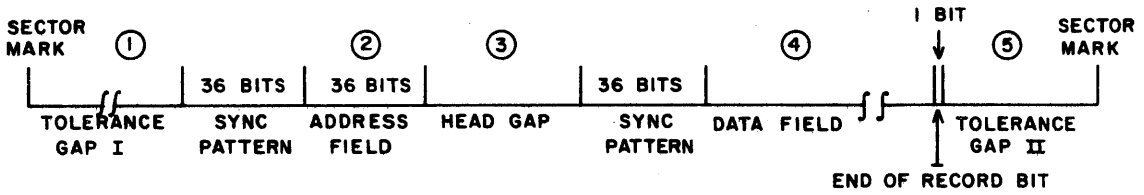
TABLE 1-2. UNIT STORAGE FORMAT AND CAPACITY

Unit / Division	813	814	853	854	2321 ††
Byte	12 bits per byte (all units)				
Sector	128 bytes (1536 bits)	128 bytes (1536 bits)	128 bytes (1536 bits)	128 bytes (1536 bits)	1380 bytes (16,560 bits)
Track	32 sectors (49,152 bits)	32 sectors (49,152 bits)	16 sectors (24,576 bits)	16 sectors (24,576 bits)	1 sector (16,560 bits)
Cylinder	128 tracks (6,291,456 bits)	128 tracks (6,291,456 bits)	10 tracks (245,760 bits)	10 tracks (245,760 bits)	20 tracks (331,200 bits)
Access	128 cylinders (805,306,568 bits)	128 cylinders (805,306,568 bits)	NA †	NA	NA
Strip ††	NA	NA	NA	NA	5 cylinders (1,656,000 bits)
Subcell ††	NA	NA	NA	NA	10 strips
Cell ††	NA	NA	NA	NA	20 subcells (331,200,000 bits)
Unit Total Capacity	1 access (805,306,568 bits)	2 accesses (1,610,612,936 bits)	100 cylinders (24,576,000 bits)	200 cylinders (49,152,000 bits)	10 cells (3,312,000,000 bits)

† Not applicable
†† Applies to 3234-A/B/C models only

SECTOR FORMAT

Figure 1-9 shows the basic sector format used in the peripheral storage devices. While only the data field in each sector can be changed by the program, the entire format is shown to aid in understanding the make-up of each sector in the track. Figure 1-10 shows disk, track, and sector organization for a disk pack (the disk file is similar).



(1)	Tolerance gap I	Disk file Disk drive	60 bits	Provides initial head switching time
		Strip file†	360 bits	
(2)	Address field	Upper portion Lower portion Checkword	12 bits each	Write lockout and defective track bits; sector address information and checkword
(3)	Head gap	Disk file Disk drive	60 bits	R/W head, erase gap
		Strip file†	360 bits	
(4)	Data field	Disk file Disk drive	128 bytes + 1 (1536 bits)	12-bit checkword
		Strip file†	1380 bytes + 6 (16,560 bits)	12-bit checkwords
(5)	Tolerance gap II	Disk file Disk drive	95 bits	Motor speed variation and R/W, erase gap
		Strip file†	830 bits	

Figure 1-9. Sector Format

† Applies to 3234-A/B/C models only

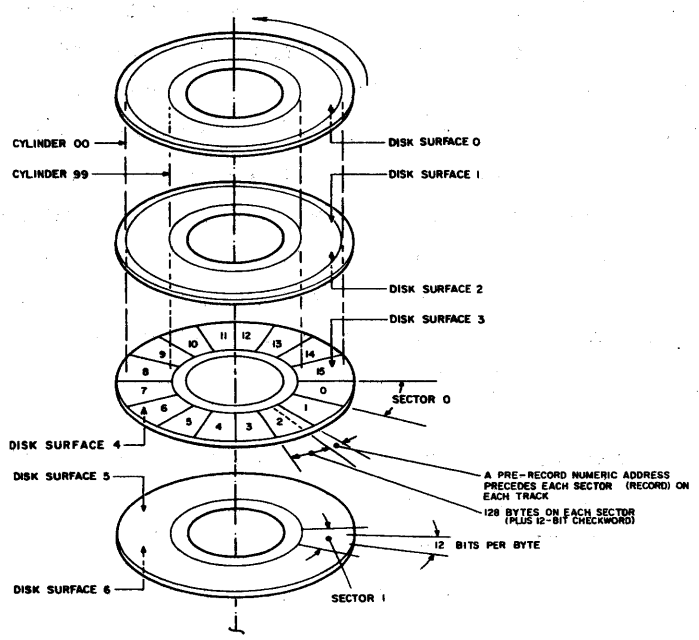


Figure 1-10. Disk Pack Storage Arrangement

CHECKWORD

Address and data transfers are checked for accuracy by generation of a 12-bit redundant checkword in the controller. During operations the controller generates and verifies checkwords to determine the correctness of addresses and data transferred between the controller and the various peripheral storage devices.

As data (or addresses) is read or written, each bit is also fed into the cyclic encoder. As the data (or addresses) enters the encoder, it is shifted through the encoder and half adder stages (A, B, C, D, and E, Figure 1-11) continuously until the last bit of data or address is entered. The remainder is a cyclic code generated from the address or data being transferred. The checkword is obtained by dividing the address or data (which is taken as a code polynomial) by the polynomial $X^{12} + X^{11} + X^3 + X^2 + X + 1$ (Figure 1-11).

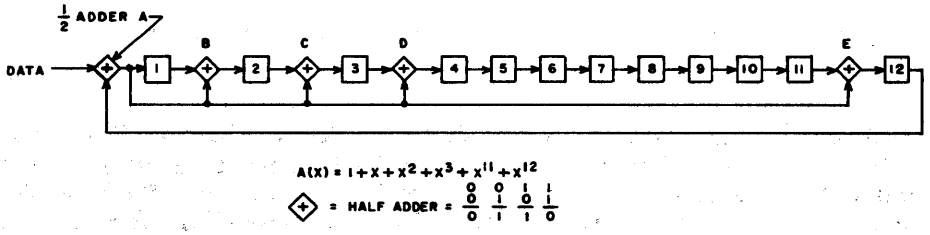


Figure 1-11. Block Diagram: Cyclic Encoder

The checkword is the 12-bit code left in the cyclic encoder after the last bit of address or data has entered the encoder. This is then written immediately following the address when the address is originally written or at the end of the sector for each write function (six checkwords are written per sector in the strip file). During subsequent address verification or read operations the address or data being read is again fed into the encoder, and if the original data was written and read correctly, the two checkwords cancel each other. The encoder is then in a clear state. (If any stage of the encoder is set upon completion of the operation, an error has occurred in either the original writing on the storage unit or during the subsequent read operation, and a checkword error indication is generated.)

The theory behind the operation of the cyclic encoder (cyclic code) involves a mathematical formula.† The error detection capability of the cyclic encoder falls within the following limits, where a burst equals the number of bits between any two bits in error.

1. If a burst is 12 bits or less, all errors are detected.
2. If a burst is 13 bits, an undetected error occurs approximately every 2^{-11} (one out of every 2048 errors is undetected).
3. If a burst is 14 bits or greater, an undetected error occurs approximately every 2^{-12} (one out of every 4096 errors is undetected).

DATA TRANSFER

Data is addressed and written in a storage unit in discrete blocks (sectors); however, the data channel can read or record as little as one byte or as many bytes as necessary to reach the end of file or end of cell (in the case of the strip file). When reading or writing, the operation must commence at the start of a sector. When writing, if less than a full sector is written, the remainder of the sector is automatically filled with zeros. The nominal data transfer rate is:

Disk file	98,000 bytes per second
Disk drive	100,000 bytes per second
Strip file (3234-A/B/C)	36,000 bytes per second

† For a general description of cyclic code theory refer to "Error Correcting Codes" by W. Wesley Peterson, MIT Press. For a detailed description of the type of cyclic encoder used in this controller refer to "A Study of Methods of Error Detection During Transmission of Binary Information" by Carl Superko, Control Data Corporation.

Timing diagrams which indicate the relationship between the data signals and the reply signals during buffered operations are shown under Programming Considerations.

ACCESS TIME

Access time is equal to the cylinder-positioning time plus the rotational-latency time. The following maximum positioning times were achieved as an average over several maximum positioner moves. Maximum access time is the sum of maximum positioning time plus maximum latency time. Average access time is the sum of average positioning time plus average latency time.

DISK FILE

Maximum access time	162.9 milliseconds
Average access time	95.7 milliseconds
Maximum positioning time (major move)	100.0 milliseconds
Maximum positioning time (minor move)	25.0 milliseconds
Average positioning time (1/3 of maximum move)	70.0 milliseconds
Maximum latency	51.4 ± 1.5 milliseconds
Average latency	25.7 milliseconds

DISK STORAGE DRIVE

Maximum access time	190.0 milliseconds
Average access time	107.5 milliseconds
Maximum positioning time	165.0 milliseconds
Average positioning time (1/3 of maximum move)	95.0 milliseconds
Cylinder to cylinder positioning time	30.0 milliseconds
Maximum latency	25 ± 0.5 milliseconds
Average latency	12.5 milliseconds

STRIP FILE †

Access time is defined as the interval from the issuance of a seek command from the controller to the 2321 until the generation of a strip ready signal in the 2321. This includes time to restore a previously addressed strip (if required). Average access times under varying conditions are as follows:

Move head bar (can be overlapped with other motions)	95.00 milliseconds
Select head R/W element	0.10 milliseconds
Maximum latency	50 ± 0.65 milliseconds
Restore strip	200.00 milliseconds

† Applies to 3234-A/B/C models only

Strip Seek Time Without Restore	Number of Subcells Moved	Strip Seek Time With Restore
175 milliseconds	0	375 milliseconds
250 milliseconds	1	450 milliseconds
350 milliseconds	50	550 milliseconds
400 milliseconds	100	600 milliseconds

1738 COMPATABILITY

Certain design and operating compatibility exists between the 1738 Disk Drive Subsystem and the 3234 Mass Storage Subsystem. For a complete explanation, refer to Disk Storage Drives under Programming Considerations.

CODES

Table 2-1 lists all codes applicable to the controller and the associated subsystem. A complete explanation of each code follows the table.

TABLE 2-1. CONNECT, FUNCTION, AND STATUS CODES

Connect	
Connect Code	N0DU †
Function	
Release and disconnect	0000
Restore	0001
+ 1 cylinder seek ††	0002
- 1 cylinder seek ††	0003
Clear	0005
Load address	0010
Return address	0011
Read disk address ††	0013
Select interrupt on ready and not busy	0020
Release interrupt on ready and not busy	0021
Select interrupt on end of operation	0022
Release interrupt on end of operation	0023

† N = equipment number of controller
D = device type (1 = Disk Drive; 2 = Disk File; 3 = Strip File)
U = unit number of storage device

†† 3234-D/E only

TABLE 2-1. CONNECT, FUNCTION, AND STATUS CODES (Cont'd)

Function		
Select interrupt on abnormal end of operation		0024
Release interrupt on abnormal end of operation		0025
Select interrupt on opposite channel release		0026
Release interrupt on opposite channel release		0027
Select interrupt on end of seek		0030
Release interrupt on end of seek		0031
Disk file status†		0032
Clear disk file status†		0033
Disable sector verify†		0034
Write address normal†		0035
Write address defective†		0036
Write address lockout†		0037
Read		0040
Write		0041
Search compare		0042
Masked search compare		0043
Checkword verify		0044
Read checkword		0045
Magnitude search (record $\leq$ buffer)		0050
Magnitude search (record $\geq$ buffer)		0051
Equality search (record = buffer)		0052
Buffer mode		0053
End of record mode		0054
Margin selection†		04XX
Status		
Ready	0	XXX1
Busy	1	XXX2
Abnormal/unavailable	2	XXX4
On sector	3, $\overline{2}$	XX10
Address error	3, 2	XX14

† 3234-D/E only

TABLE 2-1. CONNECT, FUNCTION, AND STATUS CODES (Cont'd)

Status		
No compare	4, $\overline{2}$	XX20
Lost data	4, 2	XX24
End of record	5, $\overline{2}$	XX40
Checkword error	5, 2	XX44
Write lockout on read (normal)	6, $\overline{2}$	X1X0
Write lockout on write (abnormal)	6, 2	X1X4
Positioner ready	7	X2XX
End of operation interrupt	8	X4XX
Abnormal end of operation interrupt	9	1XXX
Seek interrupt	10	2XXX
Reserved	11, $\overline{2}$	4XX0
Defective track	11, 2	4XX4

CONNECT CODE (NODU)

The 12-bit connect code (Figure 2-1) designates the equipment (controller), the peripheral device type (disk drive, disk file, strip file), and the unit with which the computer is to communicate.

Reservation capability is set up on a data channel basis. Once the data channel is connected to the controller and unit, the controller and unit are reserved until specifically released by that channel via a master clear, channel clear, or release and disconnect function code.

Upon receipt of the connect code by the controller, a reply or reject is returned to the data channel. If the desired controller, device, and unit are available, a reply is returned immediately. If the controller is unable to accept and perform the connect, a reject is returned. Upon receipt of a reject, the computer must request a status response and interrogate the status bits in order to determine whether the reject was a result of the controller being reserved, the storage type being nonexistent, or the unit being unavailable. Refer to explanation of status response bits unavailable (XXX4) and reserved (4XXX).

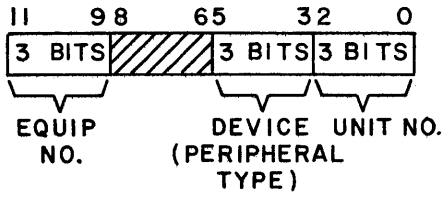


Figure 2-1. Connect Code Format

BITS 0 THROUGH 2

Bits 0 through 2 designate the logic unit number (0 through 7) with which the program communicates. The number designated is variable from 0 through 7 by means of the unit designation jumper wires located on the maintenance control panel (Figure 3-1).

BITS 3 THROUGH 5

Bits 3 through 5 designate the type of peripheral device with which the program is to communicate. All other device codes are illegal and cause a reject to be issued.

XX1X	Disk drive
XX2X	Disk file
XX3X	Strip file

BITS 6 THROUGH 8

Unused

BITS 9 THROUGH 11

Bits 9 through 11 designate the equipment with which the program desires to communicate. The number designating the equipment (controller) is variable from 0 through 7 by means of the rotary equipment number switch located in the controller cabinet.

FUNCTION CODES

The function codes consist of control and address codes which affect the reservation of the controller and the positioning of the R/W heads. The interrupt codes set and remove interrupt selections. The error recovery codes (3234-D/E) allow flexibility and control in the determination and correction of various error conditions. The I/O codes define the input and output operations and the mode select codes are used to set parameters of the search-compare operation.

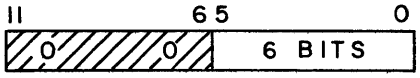


Figure 2-2. Function Code Format

A reject is issued upon receipt of a function code whenever the controller is busy with an operation other than a seek.

A reply is issued upon receipt of an unassigned function code, but the code does not produce action in the controller.

CONTROL AND ADDRESS CODES

The control codes provide the computer with a means of releasing the subsystem, removing all reserves, I/O selections, and interrupt signals, deselecting the data channel, and restoring the recording strip (in the case of the strip file), thus reducing the address time on future references to new strips. The address codes are used to address the selected storage unit or to return the current address. In either case the address is loaded into or taken from the controller address register. The address format varies for each type of storage unit. (Refer to addressing for complete address and format information.)

RELEASE AND DISCONNECT (0000)

This code logically releases the subsystem from the data channel. It causes all reserves to be removed, clears all interrupt signals, removes all I/O code selections, clears the read parity and write check error conditions, and drops the status response lines.

RESTORE (0001)

Dependent upon the type of device selected, the restore code causes the following:

Disk Drive	Initiates a seek to position (cylinder) zero of the disk pack
Disk File	Causes the positioners to move out of the recording area
Strip File†	Causes the file to restore the recording strip to its proper subcell location. If no strip is presently loaded, the code is ignored (no-op). Use of the restore code, in conjunction with the strip file, reduces strip wear as well as access time of possible future requests to a different strip.

+1 CYLINDER SEEK (0002)††

The +1 cylinder seek function code initiates a forward one-cylinder seek. A seek forward and a difference count of 1 is sent to the disk unit without computing the difference or restoring to zero. The automatic restore is cleared. This function does not affect the contents of the address register in the controller, the cylinder, head, and sector register in the drive. Interrupts resulting from this operation are the same as a seek operation, except for the seek interrupt. It is generated if the last operation was a seek but it is not generated if the last operation was a read or write.

-1 CYLINDER SEEK (0003)††

The -1 cylinder seek function code is identical to the 0002 function code, except that a seek is initiated in the reverse direction.

CLEAR (0005)

The clear code clears all major components in the subsystem, but does not affect the connect, reserved, or unit select status of the subsystem.

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† Applies to 3234-A/B/C models only

†† Applies to 3234-D/E models only

LOAD ADDRESS (0010)

The load address code causes the next output data to be loaded into the 24-bit controller address register. The data is continuously loaded into the address register (in the format indicated under addressing) until the output operation terminates. On completion, a seek operation is automatically initiated in the selected storage unit. All subsequent load address functions to the same storage unit are rejected until the seek is completed (or it is determined that the seek will be incomplete).

RETURN ADDRESS (0011)

The return address code, in conjunction with an input operation, causes the controller to return the content of the 24-bit address register to the data channel. The address is continuously returned (in the format indicated under addressing) until the input operation terminates.

READ DISK ADDRESS (0013)†

The read disk address function code causes a 36-bit input buffer to return the address read from the disk unit. The address read is that specified by the address register. An end of operation interrupt is generated after the third 12-bit byte of data. An end of record is sent on the fourth byte, if requested.

INTERRUPT CODES

The interrupt codes establish and remove the interrupt selections that determine which conditions send an interrupt signal to the data channel.

A manual master clear or channel clear removes all interrupt selections (except the interrupt on opposite channel release for the channel that is reserved).

An interrupt signal may be dropped by a manual master clear, channel clear, or any function code including reselecting the same selection.

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† Applies to 3234-D/E models only

SELECT INTERRUPT ON READY AND NOT BUSY (0020)

The select interrupt on ready and not busy code activates the interrupt line the next time the subsystem becomes ready and not busy (at the end of the next operation).

RELEASE INTERRUPT ON READY AND NOT BUSY (0021)

The release interrupt on ready and not busy code removes the associated interrupt selection set up by the 0020 code. No interrupt notification of ready and not busy is sent until the condition is reselected.

SELECT INTERRUPT ON END OF OPERATION (0022)

The select interrupt on end of operation code causes the interrupt line to be activated and the associated status bit to be set on completion of the next operation whether the end of operation is normal or abnormal.

The following conditions cause an interrupt on end of operation.

1. At the end of the sector in which a read or write operation ended
2. When the channel goes inactive at the end of a return address operation
3. After a seek command is sent to the storage unit on a load address operation

RELEASE INTERRUPT ON END OF OPERATION (0023)

The release interrupt on end of operation code removes the associated interrupt selection set up by the 0022 code. No interrupt indication of end of operation is sent until the condition is reselected.

SELECT INTERRUPT ON ABNORMAL END OF OPERATION (0024)

The select interrupt on abnormal end of operation code causes the interrupt line to be activated and the associated status bit to be set on the stopping of an operation because of any abnormal condition within the controller or selected storage unit.

The following conditions are considered abnormal.

1. Detection of an address error
2. Any attempt to write at a location which is in a write lockout state
3. Occurrence of a checkword error (indication of an error in the data read from the selected storage unit)
4. Occurrence of a lost data error (data missed due to channel failure to maintain a fast enough transfer rate)
5. Any attempt to perform an operation on a defective track
6. Dropping ready during any operation

RELEASE INTERRUPT ON ABNORMAL END OF OPERATION (0025)

The release interrupt on abnormal end of operation code removes the associated interrupt selection set up by the 0024 code. No interrupt indication of abnormal end of operation is sent until the condition is reselected.

SELECT INTERRUPT ON OPPOSITE CHANNEL RELEASE (0026)

The select interrupt on opposite channel release code causes an interrupt signal to be sent whenever the opposite data channel (the channel presently maintaining a reserved state of the controller) releases its reservation of the controller and storage units. If only one data channel is connected to the controller, this code is not applicable and should not be used.

NOTE

The interrupt is conditioned upon the dropping of the reserve. Therefore, a master clear causes the interrupt only if the data channel executing the master clear has the subsystem reserved.

RELEASE INTERRUPT ON OPPOSITE CHANNEL RELEASE (0027)

The release interrupt on opposite channel release code removes the associated interrupt selection set up by the 0026 code. No interrupt indication of a release by the opposite channel is sent until the condition is reselected.

SELECT INTERRUPT ON END OF SEEK (0030)

The select interrupt on end of seek code causes the interrupt line to be activated and the associated status bit set at the end of the seek operation (in any storage unit) regardless of whether the seek was complete or incomplete.

RELEASE INTERRUPT ON END OF SEEK (0031)

The release interrupt on end of seek code removes the associated interrupt selection set up by the 0030 code. No interrupt indication of an end of seek operation is sent until the condition is reselected.

ERROR RECOVERY CODES †

Error recovery codes provide for positive error identification and recovery techniques. They allow, when needed, sampling of conditions in the disk file, disabling sector verify, or writing of address headers without certain restrictions. The margin selection function allows movement of the positioner in small increments to circumvent track defects, if necessary. It also provides for varying the read strobe to adjust for fluctuations in read timing.

DISK FILE STATUS (0032)†

The disk file status function brings up the read status select line to enable the file fault status onto the control bus. The controller then switches the channel status lines to receive the file status. The function is accepted by the controller and a reply generated whether the controller is ready or not, provided there is no transmission parity error. A reject is generated if the controller is busy. This function is cleared by a 0033, 0000, 0005 function, or a master clear.

The file status can be displayed on the maintenance panel by setting the REGISTER SELECT switch to FILE STATUS. The following are the status bit assignments.

† Applies to 3234-D/E models only

Bit 0	Voltage error
Bit 1	Logic error
Bit 2	Write error
Bit 3	Head select X error
Bit 4	Head select Y error
Bit 5	Read/write error
Bit 6 through Bit 11	Unused

CLEAR DISK FILE STATUS (0033)†

The clear disk file status function code clears the disk file status function selection. The reply and reject conditions are the same as for the 0032 function code.

DISABLE SECTOR VERIFY (0034)†

The disable sector verify function code suppresses the need to verify the address before a read, write, or search operation. This function must precede the 004X functions and clears on the next end of operation. Multisector operation is possible. The defective sector and write lockout status is suppressed during this operation.

Selection of this function requires that the correct address of the pack or disk must have been specified in the last seek operation. A read disk address function (0013) should precede this function to ensure that the head is properly positioned.

WRITE ADDRESS NORMAL (0035)†

The write address normal function, when followed by a load address operation, writes a new header in the sector specified by the address register. The load address operation initiates the write header operation. No seek interrupt occurs on a programmed write header. An end of operation is generated if previously selected. A read disk address function (0013) should precede this function to ensure that the read/write head is properly positioned.

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† Applies to 3234-D/E models only

WRITE ADDRESS DEFECTIVE (0036)†

The write address defective function code is identical to the 0035 function except that the defective sector bit is added in the header.

WRITE ADDRESS LOCKOUT (0037)†

The write address lockout function code is identical to the 0035 function code except that the write lockout bit is added in the header.

MARGIN SELECTION (04XX)†

The margin selection function code sends eight bits to the disk which add small increments in cylinder movement or allow small variations in the read strobe time, depending on the bit assignments (Figure 2-3). A reply is sent to the channel if the controller is ready and not busy, and if no transmission parity error exists. A reject is generated if the controller is busy or not ready, with one exception (the clear fault function (0600) is accepted if the controller (or unit) is not ready).

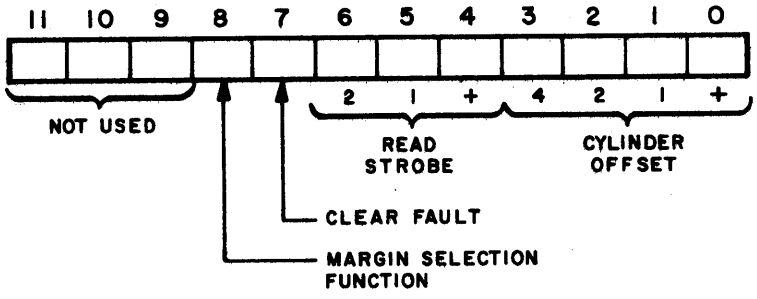

Figure 2-3. Margin Selection

† Applies to 3234-D/E models only

CYLINDER OFFSET

The cylinder offset portion of the function moves the positioner off cylinder in increments of 0.00075 inch in the 813 Disk File. The disk file drops on cylinder for a minimum of 10 milliseconds. The maximum time is less than one cylinder move. The busy status goes up during the function and drops when the on cylinder comes up. Only read operations are allowed off cylinder. A write operation in any offset position other than zero generates a fault and drops ready. No interrupts are generated during this operation.

Function	Offset (inch)
0400	-.00000
0401	+.00000
0402	-.00075
0403	+.00075
0404	-.00150
0405	+.00150
0406	-.00225
0407	+.00225
0410	-.00300
0411	+.00300
0412	-.00375
0413	+.00375
0414	-.00450
0415	+.00450
0416	-.00525
0417	+.00525

READ STROBE

The read strobe portion of the function varies the read strobe in increments of 15 nanoseconds in the 813/814 Disk Files. No busy status or interrupts are generated other than the normal reply or reject signals.

Function	Offset (nanoseconds)
0400	-00
0420	+00
0440	-15
0460	+15
0500	-30
0520	+30
0540	-45
0560	+45

CLEAR FAULT (0600)

The clear fault bit, when set, clears all fault status conditions in the disk file except a solid fault condition.

The following are examples of margin selection functions.

0407 - Select offset +.00225, and clear read strobe
0527 - Select offset +.00225, and select read strobe +30 nanoseconds
0537 - Select offset +.00525, and select read strobe +30 nanoseconds
0417 - Select offset +.00525, and clear read strobe
0400 - Clear offset and clear read strobe
0600 - Clear fault, clear offset, and clear read strobe

INPUT/OUTPUT CODES

The following codes define the conditions for the various data handling operations which cause the transfer of data between the data channel and/or the controller and the selected peripheral storage device. With the exception of the checkword verify, the codes all require initiation of an input or output operation in order to activate the subsystem. Refer to Programming Considerations for timing diagrams of buffered I/O operations.

READ (0040)

The read mode, in conjunction with an input operation, causes the controller to initiate a read operation from the selected storage unit at the address specified by the contents of the controller address register. The operation continues until halted by one of the conditions listed under interrupt on end of operation. When operating in EOR mode, an EOR signal is transmitted to the data channel on detection of a record mark at the end of a data block if the data channel tries to read past the end of record.

WRITE (0041)

The write mode, in conjunction with an output operation, causes the controller to initiate a write operation to the selected storage unit at the address specified by the contents of the controller address register. The operation continues until halted by one of the conditions listed under the interrupt on end of operation. If an output operation terminates before the end of the current data block, the remainder of the block is automatically filled with zeros. The checkword is always written at the end of the block. When operating in EOR mode, an EOR mark is recorded at the end of the last block written.

SEARCH COMPARE (0042)

The search compare mode, in conjunction with an output operation, causes the controller to initiate a read operation from the selected storage unit at the address specified by the contents of the controller address register.

The output operation transmits data to the controller which is compared by bytes on a bit-by-bit basis with the data read from the storage unit. The compare is performed according to the previous settings of the mode select functions.

Upon occurrence of a miscompare (unsuccessful comparison), the no compare status bit is set.

MASKED SEARCH COMPARE (0043)

The masked search compare mode, in conjunction with an output operation, causes the controller to initiate a read operation from the selected storage unit at the address specified by the contents of the controller address register.

The output operation transmits data to the controller which is compared by bytes on a bit-by-bit basis with the data read from the storage unit. If a byte in the output data contains all 1's (7777_8), however, no comparison is made on the associated byte read. The compare operation is performed according to the previous settings of the mode select function.

Upon occurrence of a miscompare (unsuccessful comparison), the no compare status bit is set.

CHECKWORD VERIFY (0044)

The checkword verify code is the only operating mode that does not require a buffer. On receipt of this function code by the controller, the data within the current cylinder (or strip in the strip file) is read and checked for an illegal checkword. Operation commences at the present address position of the read/write heads and continues to the end of that cylinder (or strip in the strip file).

NOTE

When operating in EOR mode, only one record is verified; if no record mark is present, the rest of the file/cell is verified.

READ CHECKWORD (0045)

The read checkword operation, in conjunction with an input operation, causes the controller to initiate a read operation from the selected storage unit at the address specified by the contents of the controller address register. This operation is identical to the 0040 read function except that all checkword(s) read are returned to the data channel along with the data.

There is one checkword per data block in the disk file and disk drive units. There are six checkwords per data block in the strip file (refer to Checkword Location).

The operation continues until halted by one of the conditions listed under Select Interrupt on End of Operation.

The following codes select and specify the conditions under which the 0042 and 0043 search compare functions operate, and determine and identify the conditions under which an end of operation occurs.

MAGNITUDE SEARCH (RECORD $\leq$ BUFFER) (0050)

The magnitude search code modifies the search compare operation so the comparison is satisfied if the data read (searched) is equal to or less than the output data.

The search is unsuccessful (no compare status bit sets) when the first (high order) unmasked output data bit is a 0 and the record bit is a 1.

MAGNITUDE SEARCH (RECORD ≥ BUFFER) (0051)

The magnitude search code modifies the search compare operation so the comparison is satisfied if the data read (searched) is equal to or greater than the output data.

The search is unsuccessful (no compare status bit sets) when the first (high order) unmasked output data bit is a 1 and the record bit is a 0.

EQUALITY SEARCH (RECORD = BUFFER) (0052)

The equality search code modifies the search compare operation so the comparison is satisfied only if the data read (searched) is equal to the output data. Any master clear operation automatically selects this mode of operation.

The search is unsuccessful (no compare status bit sets) when the first unmasked output data bit is different from the record bit read.

BUFFER MODE (0053)

The buffer mode code prepares the controller for a subsequent I/O operation wherein the end of operation is defined as the word count of the I/O operation. (Refer to Buffer Restrictions under Programming Considerations.)

END OF RECORD MODE (0054)

The end of record mode code prepares the controller for a subsequent I/O operation wherein the end of operation is defined as the limit of the record as follows:

Write - a record mark is recorded at the end of the block in which the output operation ended. The original output operation may be from less than a single block to an entire file (cell) in length.

Read - an end of record signal is sent to the data channel each time the record mark is detected if the data channel tries to read past the end of record.

Any master clear automatically selects this mode of operation.

STATUS CODES

The computer determines the state of the controller and storage units by the use of a 12-bit status response available to the data channel. The computer initiates a copy status instruction and samples the status response on the lines from the controller. The computer may sample a status response anytime it is connected, or after a connect attempt is rejected if the controller and/or peripheral units are under control or reservation by a different data channel. The status response may be a combination of any of the available response bits.

The status response bits (Table 2-1) indicate the state of the controller and storage unit to which the data channel is connected or last attempted to connect. A 1 in the bit position indicates the condition is present (or has occurred); a 0 indicates the condition is not present (or has not occurred). An interrupt must previously have been selected or the associated interrupt status bit will be a 0 even though a condition that would normally set the interrupt has occurred (that is, a copy status does not indicate that an abnormal end of operation has occurred unless the abnormal end of operation interrupt is selected). If the abnormal end of operation interrupt is selected, the operation ends, the interrupt error status bits are set, and the interrupt is sent to the data channel immediately upon occurrence of the error condition. However, if the abnormal end of operation interrupt is not selected, the error status bits are set immediately upon occurrence of the error condition even though the operation may not end until the buffer is completed.

READY (XXX1) - BIT 0

The presence of bit 0 indicates that the unit last connected is in an operable condition and ready for use. A storage unit is considered ready when it is available and ready to operate. The unit becomes not ready for the following conditions.

DISK FILE AND DISK DRIVE UNITS

1. Disk pack not loaded (applicable to disk drive unit only)
2. R/W heads not landed
3. Disk motor not up to speed
4. File or disk drive unsafe condition from selected unit (refer to Unsafe Conditions)
5. No such unit
6. Wrong unit type designation

STRIP FILE

1. ENABLE/DISABLE (running time meter) switch in the disable position
2. Unit is in customer engineering mode (off-line)
3. Manual intervention
4. File unsafe condition (refer to Unsafe Conditions)
5. No such unit
6. Wrong unit type designation

No such unit and wrong unit type designation conditions cause a reject or connect on all unit types.

Any 1X, 4X, or 5X function code is rejected when the controller is not ready; other function codes are accepted even though the controller is not ready. If a unit becomes not ready during an operation, the operation ceases immediately and (if selected) the abnormal end of operation interrupt is sent to the data channel.

BUSY (XXX2) - BIT 1

The presence of bit 1 indicates that the controller and/or peripheral unit specified by the connect code are currently performing an operation and are unable to initiate any new action at this time. The bit becomes a 0 at the end of operation.

The busy status normally follows the channel busy signal. However, the busy status remains until the checkword has been written or read, the address register updated, and in the case of the strip file, until the adapter busy signal drops. (This is the end of operation on a read or write function and if selected, the end of operation interrupt occurs at this time.) Any abnormal condition which causes an end of operation to occur causes the busy status to drop.

In the case of a checkword search even though no buffer is initiated, the subsystem is busy until the search is finished.

A storage unit is busy following a seek initiation until the seek is completed; however, the controller is available for operation to a different unit as soon as the positioner ready signal drops.

ABNORMAL/UNAVAILABLE (XXX4) - BIT 2

When the system is connected and reserved, the presence of bit 2 indicates that an abnormal condition exists in the controller or storage unit and assigns a different meaning to the status bits XX1X through X1XX and 4XXX.

If a connect attempt is rejected, the presence of bit 2 indicates that the storage unit requested by the connect code was unavailable.

When a unit is unavailable it is considered to be permanently unavailable (manual intervention is necessary to remove the cause of unavailability).

ON SECTOR (XX10) - BITS 3,$\overline{2}$

DISK FILE AND DISK STORAGE DRIVE UNITS

The on sector status bit comes up one sector prior to the addressed sector with or after the positioner ready status. This allows the computer a one-sector time slot in which to initiate an operation on the addressed sector. If no operation is initiated within the one-sector time slot (1 millesecond), the on sector status bit drops and comes up again one revolution later.

STRIP FILE†

When operating with the strip file unit there is only one sector per track; therefore, the on sector status bit comes up at the index (8 milliseconds before the sector starts) and stays up until the unit is operated on.

Refer to Programming Considerations for timing diagrams showing the relationship between the on sector and positioner ready signals.

ADDRESS ERROR (XX14) - BITS 3,2

The presence of the address error code indicates that an address error has been detected due to one of the following conditions.

† Applies to 3234-A/B/C models only

1. The address register contains an illegal address.
2. The content of the address register does not compare with the address being read from the storage unit.
3. The controller has been requested to operate beyond the storage unit address limits.
4. The seek operation initiated by the load address was incomplete.
5. A defective track bit is present.†
6. A checkword error occurs during address verification.
7. A seek error occurs from the disk unit.

If an error occurs during an operation, the operation ends immediately, and if selected, an abnormal end of operation interrupt is transmitted. A new load address function should be performed before any new I/O is attempted.

For the 3234-D/E models, additional bits further define the address error status as follows. Other bit combinations are possible.

(0255) Address error with checkword error - This results from a read error which causes a header checkword error.

(4355) Address error with checkword error, defective sector, and write-lockout detected. This condition is the same as 0255 except that the incorrect sync bit causes other bits to be detected.

(4205) Defective sector status - The defective sector bit without address error indicates the header was tagged defective by the computer or the maintenance panel.

NO COMPARE (XX20) - BITS 4,$\overline{2}$

The presence of the no compare status code indicates that a miscomparison was detected during the preceding search compare operation.

LOST DATA (XX24) - BITS 4,2

The presence of lost data status code indicates that data has been lost because of the data channel (computer) delay. Specifically, in the case of an output operation, no data was ready when the storage unit was ready to write, or in the case of an input operation, the data channel had not yet accepted the last byte read when the storage unit had another byte ready.

† Applies to 3234-A/B/C models only

Upon detection of lost data, operation ends immediately if the abnormal EOP interrupt is selected and the associated status bits set. If the abnormal end of operation interrupt is not selected, operation continues in a normal manner; however, the lost data status bit sets.

END OF RECORD (XX40) - BITS 5,$\overline{2}$

The presence of the end of record bit indicates that an end of record bit has been detected at the end of the last sector when operating in end of record mode. If the subsystem is not operating in the end of record mode, this bit is a 0 even though an end of record bit is present at the end of a sector.

CHECKWORD ERROR (XX44) - BITS 5,2

The presence of the checkword error status code indicates that an incorrect checkword has been detected during a read, search compare, or checkword verify operation.

WRITE LOCKOUT ON READ (X1X0) - BITS 6,$\overline{2}$

On an input (read) operation it is permissible to operate in a write protected area and other than setting this status bit, operation proceeds in a normal manner.

WRITE LOCKOUT ON WRITE (X1X4) - BITS 6,2

For an output (write) operation the write lockout on write is an abnormal condition, and if the abnormal end of operation interrupt is selected, operation ends immediately upon initiation of the operation. The abnormal end of operation interrupt sets.

If the abnormal end of operation interrupt is not selected, the output data is accepted by the controller; however, the data accepted is ignored and no data is written on the selected storage unit.

POSITIONER READY (X2XX) - BIT 7

The presence of bit 7 indicates that a positioner ready signal has been received from the selected storage unit. In the disk file and disk drive units this signal comes up as soon as the positioner is settled on the cylinder. The positioner ready must come up before on sector can come up.

The positioner ready status stays up until a new load address operation is initiated. If selected, an end of operation interrupt sets when the positioner ready is dropped. When the positioner ready comes back up, a ready not busy interrupt sets if selected.

Refer to Programming Considerations for timing diagrams showing the relationship between the on sector and positioner ready signals.

END OF OPERATION INTERRUPT (X4XX) - BIT 8†

The presence of bit 8 indicates the interrupt was caused by an end of operation.

ABNORMAL END OF OPERATION INTERRUPT (1XXX) - BIT 9 †

The presence of bit 9 indicates the interrupt was caused by an abnormal end of operation.

SEEK INTERRUPT (2XXX) - BIT 10

The presence of bit 10 indicates the interrupt was caused by the end of a seek operation (in any storage unit) regardless of whether the seek was complete or incomplete.

RESERVED (4XXX) - BITS 11,$\overline{2}$

The presence of the reserved status code indicates that the last connect attempted to the subsystem was rejected because the subsystem was reserved by the opposite data channel.

†For an explanation of end of operation and an abnormal end of operation, refer to interrupt codes 0022 and 0024.

DEFECTIVE TRACK (4XX4) - BITS 11,2 †

The presence of the defective track status code indicates a defective track bit has been detected at the address referenced by the content of the controller address register. Once a track is marked defective any I/O operation attempted on that track hangs up and an address error occurs (refer to abnormal EOP interrupt). (The defective track bit is written manually into the header via the maintenance panel.)

PROGRAMMING CONSIDERATIONS

The following information concerns problems that may arise in programming mass storage subsystems. Most of the procedures are common to all computers and storage devices; those that are unique to a particular computer or unit are designated.

CONNECT

Device type codes other than XX1X, XX2X, and XX3X are illegal and cause the connect to be rejected. The unavailable and not ready status bits set.

SIMULTANEOUS CONNECT

If the two data channels attached to the same controller simultaneously attempt to connect to the controller, neither channel is given preference. The controller connects to the data channel recognized first.

Initiation of the operation need not take place immediately after the connect is made; once the connect is made, the channel has the controller and subsystem reserved until specifically released by that channel.

MODE RESTRICTIONS

Operations which are inconsistent with the mode selected cause the computer to hang up (that is, initiation of an output (write) when read mode is selected).

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† Applies to 3234-A/B/C models. On the 3234-D/E models, no address error is generated. Individual sectors can be labeled defective by software.

MASTER CLEAR, RELEASE, AND DISCONNECT

A manual or program (channel) master clear, clear function, or restore function cause the address register to be cleared to zero. A release and disconnect has no effect on the content of the address register. The master clear, clear function, and release and disconnect remove all interrupt selections except the interrupt on opposite channel release. A master clear automatically selects end of record and magnitude search (record = buffer) mode.

STRIP FILE†

If the strip file is busy when a master clear is initiated, the master clear may cause the file to go inoperative and require manual intervention to remove the inoperative condition.

DISK UNIT

Any master clear to a unit which is busy with a write operation causes the operation to cease immediately; however, the previously recorded data and checkword in the remainder of the sector are unaltered (and now useless). Therefore, a subsequent read operation causes a checkword error to be generated from the inconsistent data recorded in the sector.

Any master clear to a disk unit busy with a read operation causes operation to cease immediately, but has no other effect on the present or subsequent operations.

RESTORE (STRIP FILE)†

When the equipment is disconnected (strip file released), the strip is automatically restored if the same strip is not readdressed (unit reconnected) within 16 revolutions of the drum (approximately 800 milliseconds).

INTERRUPTS

An interrupt signal may be dropped by any master clear, clear function, release and disconnect function, or by any new function code including reselecting the same interrupt selection.

† Applies to 3234-A/B/C models only

Only the interrupt on opposite channel release interrupt selection remains when a release and disconnect is performed. All other interrupt selections are removed whenever a master clear, clear function, or release and disconnect are performed.

NOTE

The interrupt on opposite channel release can be cleared by a master clear or clear function only when the opposite channel is not reserved (that is, the channel B release interrupt selection can be cleared only if channel B is not reserved.)

Any interrupt selection may be removed by its associated release interrupt code.

A data channel which has the subsystem reserved receives all interrupts selected. The channel not in control (reservation) of the subsystem can be interrupted only by a previously selected interrupt on opposite channel release. All other interrupts from the controller to the data channel not in control are inhibited even though the interrupt is selected.

ABNORMAL EOP INTERRUPT

The abnormal end of operation interrupt should always be used when performing any I/O operations (4X codes) other than the load and return address functions. If the interrupt is not used and either an address error or not ready condition occurs, the channel hangs up in a busy condition. With the interrupt selected, an interrupt lockout override is sent back to the data channel to allow the program (via a clear channel instruction) to recover from the hung condition.

SEEK/SECTOR VERIFICATION

When any I/O code (4X) operation is initiated an automatic seek is performed to the address specified by the content of the controller address register. (Normally no positioner or strip loading movement takes place since this seek operation would have been performed subsequent to the last load address operation.) A header verification takes place at the sector following the one in which the last operation ended unless the new I/O is initiated in a different unit than the one last referenced.† In the latter case, if the positioner is not in the proper cylinder, both a seek and header verify sequence are automatically initiated.

†When any I/O is in progress (or ends), the controller automatically updates the address registers at the end of each sector except when an address error is detected or the abnormal EOP interrupt is selected and an abnormal condition occurs.

OVERLAP SEEK

Overlap seek capability is incorporated within the units and can be performed on any storage unit in the subsystem as follows:

1. Select unit, select seek interrupt, and initiate a seek operation (by performing a load address function).
2. Repeat step 1 for other desired storage units.
3. On detection of an interrupt,† search the selected storage units for an on sector status bit to determine which unit is ready for operation.
4. Initiate and perform I/O operation.
5. Continue from step 3.

The on sector status is returned from a storage unit in which a seek operation (load address operation) is completed (positioner ready) until a read/write (or master clear) is performed on that unit. Therefore, if several overlapped seeks are initiated, but with no read/write operations, a seek interrupt is generated each time the seek interrupt is selected until all previously addressed units have had a read/write (or master clear) operation performed on them.

NOTE

The seek interrupt is generated from a line common to all units where an interrupt can be generated by a unit in which a seek was initiated even though the controller is no longer connected to that particular storage device.

SEEK INTERRUPTS

The on sector status is returned from a storage unit after a seek operation has been completed. The on sector status line remains active until a read, write, or new seek is performed on that unit, or if a drive release, controller release, or channel clear is issued. If more than one unit is given a seek, the unit which completes its seek first will generate a seek interrupt (this unit can be determined by selecting each unit and checking on sector status). This interrupt can be cleared by issuing any function. However, even though another unit sends back an on sector signal, another interrupt will not occur. Another seek interrupt can occur only if an operation is performed. The end of operation enables the next on sector to set the seek interrupt if it is selected.

† An alternate method is to omit the interrupt and immediately (on completion of seek initiations) commence a continuous search of the on sector status bits.

Any function sent to the controller clears an interrupt, and if the controller is in the condition of expecting a seek interrupt (that is, seek interrupt selected and one or more units with seeks in progress), a function issued during this period could occur at the same time as an on sector signal from a unit. If this occurred, the seek interrupt could be cleared before the computer had time to respond, and since the interrupt cannot occur again until an operation is performed, the result is a lost interrupt. It should also be noted that if more than one unit has a seek in progress and the computer receives a seek interrupt from one unit and performs an operation on it, the possibility exists of a lost interrupt at the time the end of operation occurs. A possible solution is to deselect the seek interrupt before the operation is performed, and reselect after the operation is complete.

On a seek operation the busy status remains up until the seek is completed, but the controller accepts a new connect or function as soon as the controller has sent the seek pulse to the unit. If the end of operation interrupt is set, the interrupt is generated when the controller is ready to accept a new connect or function.

1X AND 4X FUNCTION CODES

When preparing the subsystem for operation via the issuance of the various function codes, the 1X (address) or 4X (I/O codes) must be issued last or they will be cleared out by the next function code issued. With the exception of the checkword verify code, 0044, the 1X and 4X function codes are designed to be followed by a buffered operation.

RECORDS

Records consist of full sectors only. If an output from the data channel consists of less than a full sector when operating in end of record mode, the remainder of the sector is automatically filled with zeros and the record mark is written at the end of the sector. It is possible to count and locate record marks in the various storage units by performing a checkword verify in end of record mode, and then performing a return address. The sector address returned is one greater than the address in which the record mark was detected. The difference between the starting and ending addresses is one greater than the number of sectors in the record.

SYSTEM ERRORS AND PERFORMANCE

The controller recognizes the following error conditions.

1. Transmission parity error
2. Lost data
3. Write lockout
4. Checkword error
5. Address error
6. Defective sector

With the exception of the transmission parity error, the presence of the errors may be detected through the use of interrupts and/or a status response.

Other internal error conditions (refer to Unsafe Conditions) from the selected storage unit cause the subsystem to go to the not ready state. (The not ready condition may be detected via the status response.)

TRANSMISSION PARITY ERROR

The transmission (XMSN) parity circuits examine each byte transmitted to the controller from the data channel, generate a new parity bit for that byte, and compare the parity bit generated with the parity bit accompanying the byte. If the bits do not agree, the PARITY ERROR indicator lights.

Transmission of the error indication to the data channel is dependent upon the code or data causing the error.

XMSN PARITY ERROR ON CONNECT

If the error is detected on a connect code, the controller does not connect; if connected, it disconnects (including its status lines). The transmission PARITY ERROR indicator lights, but no reply, reject, or transmission parity error signals are sent to the data channel.

XMSN PARITY ERROR ON FUNCTION

If an error occurs on the function code, the transmission parity error signal is sent to the data channel and the error indicator lights; however, the function code is ignored by the controller (no reply or reject is sent).

XMSN PARITY ERROR ON DATA TRANSFER

If an error is detected on a data byte received from the data channel, the XMSN parity error signal is sent and the error indicator lights. The controller returns a reply and uses the data in the normal manner.

LOST DATA

A lost data error occurs when the data channel does not transmit or receive data at the fixed rate required by the subsystem. This condition can occur when the data channel serving the mass storage subsystem must compete with several other devices for access to the computer storage. Specifically, an error occurs when the computer does not have data ready to be written when the storage unit is ready to write (output operation), or the computer has not yet accepted the data read when the storage unit has another byte ready (input operation).

WRITE LOCKOUT

To prevent accidental destruction of data, each sector address is equipped with a write lockout bit. Setting the bit to a 1 prevents any computer operation from writing in that sector. The smallest segment of storage area that can be locked out is a track (3234-A/B/C). The smallest segment of storage area that can be locked out in the 3234-D/E is a sector.

Attempting to write in a sector or track that has the write lockout bit set generates an abnormal condition (write lockout error). The write operation is then performed in a normal manner except that no writing or erasing takes place (the write and erase enable are disabled by the lockout). If selected, the abnormal end of operation interrupt is set and operation ends immediately.

Reading from a sector/track that has the write lockout bit set is accomplished in a normal manner (this is not considered an abnormal condition) even though the write lockout status bit sets. No abnormal end of operation interrupt is generated even though it is selected (refer to WRITE LOCKOUT switch under Switches and Indicators).

CHECKWORD ERROR

During write operations, a cyclic encoder in the controller generates a 12-bit check character referred to as a checkword. This checkword is written at the end of each sector (in the disk files and disk drive units); six checkwords are written per sector (track) in the strip file.

During a read/search operation a new checkword is generated from the data read and compared against the checkword previously written. If the two do not agree, an error has occurred in writing, reading, or transferring of data between the controller and selected storage unit, and a checkword error is generated.

On detection of a checkword error, the associated status bit sets, and if selected, an abnormal end of operation interrupt is generated. If the abnormal end of operation interrupt is not selected, the checkword error status bit sets; however, operation continues in a normal manner.

NOTE

If a checkword error is detected in an address header, an address error is generated and operation ceases immediately (refer to address error).

ADDRESS ERROR

An address operation consists of two main phases.

1. A seek operation wherein, upon completion of an output operation following a load address function, the R/W heads are positioned to the addressed cylinder.
2. A header verification sequence wherein, upon initiation of an operation, an automatic seek operation takes place, and the address header is read and verified for the addressed sector.

An address error can occur in either the previously initiated seek operation or during the header verification sequence. Therefore, since initiation of an operation (and header verification) may occur anytime and is semi-unrelated to any preceding seek operation, an address error can occur at two distinct and mutually independent times (upon detection of a seek error or upon detection of a header verification error).

SEEK ERROR

An address error occurs during a seek operation if either of the following conditions is detected.

1. The controller address register contains an illegal address. (The controller is being requested to operate beyond the address limitations of the selected storage unit.) (Applicable to all models, indicated by status 0215)

2. The seek operation initiated by the preceding load address function and buffer is incomplete as indicated by a seek error signal for the selected unit. (Applicable to all models, indicated by status 0015)

HEADER VERIFICATION ERROR

An address error occurs during a header verification sequence if any of the following conditions are detected.

1. The content of the controller address register does not compare with the address being read from the selected storage unit (on all 3234 models, indicated by status 0215).
2. A checkword error is detected in the address being read (on the 3234-A/B/C models, indicated by status 0215; on the 3234-D/E models, indicated by status 0255).
3. An address in which the defective sector bit is being read (on the 3234-A/B/C models, indicated by status 4215; on the 3234-D/E models, indicated by status 4205).
4. An address in which the incorrect sync bit has been detected, causing the checkword error, defective sector, and write lockout bits to be detected (on the 3234-A/B/C models, indicated by status 4315; on the 3234-D/E models, indicated by status 4355).

On detection of an address error the associated status bit sets, and if selected, the abnormal end of operation interrupt is generated on initiation of an operation. (If the abnormal end of operation interrupt is not selected, the channel hangs up on initiation of the operation.)

DEFECTIVE SECTOR

In order to prevent reading or writing in a sector which contains a defective (faulty) recording medium, a defective sector bit is normally written in each faulty sector. The sector is defective when this bit is a 0.

On detection of a defective sector, the associated status and address error bits set (except for the 3234-D/E models in which no address error occurs), and if selected, the abnormal end of operation interrupt is generated upon initiation of an operation (refer to DEFECTIVE SECTOR switch under Switches and Indicators). In the 3234-D/E models, individual sectors may be labeled defective by software.

ADDRESSING

After transmitting the connect code, the computer may transmit a load address function code. If the operation is to start or continue at the address location presently held in the controller address register, the select and I/O operating mode codes are set up on completion of the connect. The address currently held in the register is the one in which the next I/O operation takes place. This address is automatically incremented after each sector is written or read from the selected storage unit with the following exceptions.

1. The equipment becomes not ready during an operation.
2. The abnormal end of operation interrupt is selected and any abnormal condition occurs.
3. An address error occurs.

This process takes place throughout the entire file, pack, or cell from the starting address up to and including the last available address. If the I/O operation attempts to cause incrementation to continue beyond the last available address, an address error occurs, and if selected, the abnormal end of operation interrupt is generated. Once the last available address has been utilized, the address register must be reset. This may be done by loading a specific address (via the load address function) or by executing a master clear or a clear function instruction. In the latter two cases, the register is set to zero. However, if a new address is necessary for the next operation, the load address code must be sent to the controller.

LOAD ADDRESS

On initiation of an output operation following receipt of the load address function code, the controller commences loading 12-bit bytes from the data channel. These bytes form a 24-bit address word which is automatically loaded into the address register by the controller. The first byte of the address is loaded into the upper portion of the register; the second byte is loaded into the lower portion of the register. The output from

the computer may consist of several words. The controller continues to load the bytes into the address register as previously described until the end of the operation. Thus, the last two bytes transferred comprise the address remaining in the address register.

NOTE

The 3000 series computers disassemble words upper byte first.

ADDRESS FORMAT

The address format structure varies within the various peripheral types (refer to Figures 2-4, 2-5, and 2-6). The byte address specifies (in the case of the disk file and disk drive units) the cylinder, track, and sector within the cylinder at which the next operation takes place.

From a programming viewpoint the lower address portion may be considered to specify the addresses of all sectors in a single cylinder/strip. In the disk file and disk drive, the lower order bits of the lower address specify one of the sectors in a track; the upper order bits of the lower address specify one of the tracks in the cylinder.

During multiple-recorded transfers (operations of more than one sector in length), the address is automatically augmented to select the next sequential sector location. This process takes place throughout the entire file, pack, or cell up to and including (but not beyond) the last address (operation is not end-around within a file, pack, or data cell).

DISK FILE

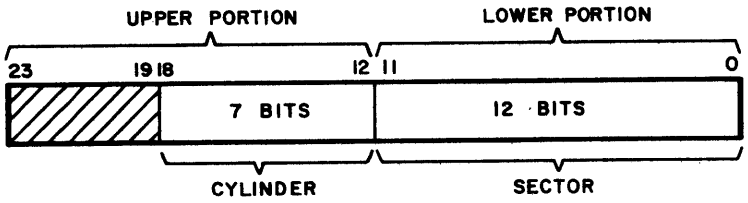


Figure 2-4. Disk File Address Format

Bits 0 through 11 specify one of 4096_{10} sectors in a cylinder (addresses 0 through 7777_8). Bits 0 through 4 specify one of 32_{10} sectors per track (addresses 0 through 37_8); bits 5 through 11 specify one of 128_{10} tracks per cylinder (addresses 0 through 177_8).

Bits 12 through 18 specify one of 128_{10} cylinders per access (unit) (addresses 0 through 177_8). Addresses above 177_8 are illegal and cause an address error to be generated.

DISK STORAGE DRIVE

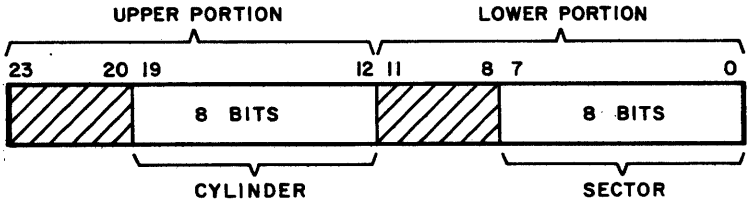


Figure 2-5. Disk Storage Drive Address Format

Bits 0 through 7 specify one of 160_{10} sectors per cylinder (addresses 0 through 237_8). Addresses above 237_8 are illegal and cause an address error to be generated. Bits 0 through 3 specify one of 16_{10} sectors per track (addresses 0 through 17_8). Bits 4 through 7 specify one of 10_{10} tracks per cylinder (addresses 0 through 11_8).

Bits 12 through 19 specify one of 100_{10} cylinders (addresses 0 through 143_8) in the 853 Disk Storage Drive units or one of 203_{10} cylinders (addresses 0 through 312_8) in the 854 Disk Storage Drive units. Addresses above 143_8 in the 853 or above 312_8 in the 854 are illegal and cause an address error to be generated.

STRIP FILE†

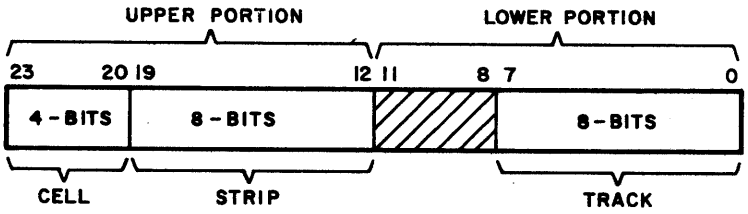


Figure 2-6. Strip File Address Format

Bits 0 through 7 specify one of 100_{10} tracks (sectors) per strip (addresses 0 through 143_8). Addresses above 143_8 are illegal and cause an address error to be generated.

Bits 12 through 19 specify one of 200_{10} strips per cell (addresses 0 through 307_8). Addresses above 307_8 are illegal and cause an address error to be generated.

† Applies to 3234-A/B/C models only

Bits 20 through 23 specify one of 10 cells per array (unit), (addresses 0 through 11_8). Addresses above 11_8 are illegal and cause an address error to be generated.

The strip file addresses for track/cylinder (lower portion) and subcell/strip (upper portion) are continuous binary addresses. Table 2-2 indicates decimal to octal conversion of the addresses used by the strip file.

TABLE 2-2. STRIP FILE ADDRESS CONVERSION CHARTS

TRACK (head selections) — LOWER ADDRESSES

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Cylinder (head position)	0	0	1	2	3	4	5	6	7	10	11	12	13	14	15	16	17	20	21	22	23
	1	24	25	26	27	30	31	32	33	34	35	36	37	40	41	42	43	44	45	46	47
	2	50	51	52	53	54	55	56	57	60	61	62	63	64	65	66	67	70	71	72	73
	3	74	75	76	77	100	101	102	103	104	105	106	107	110	111	112	113	114	115	116	117
	4	120	121	122	123	124	125	126	127	130	131	132	133	134	135	136	137	140	141	142	143

SUBCELL — UPPER ADDRESSES

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Strip	0	0	12	24	36	50	62	74	106	120	132	144	156	170	202	214	226	240	252	264	276
	1	1	13	25	37	51	63	75	107	121	133	145	157	171	203	215	227	241	253	265	277
	2	2	14	26	40	52	64	76	110	122	134	146	160	172	204	216	230	242	254	266	300
	3	3	15	27	41	53	65	77	111	123	135	147	161	173	205	217	231	243	255	267	301
	4	4	16	30	42	54	66	100	112	124	136	150	162	174	206	220	232	244	256	270	302
	5	5	17	31	43	55	67	101	113	125	137	151	163	175	207	221	233	245	257	271	303
	6	6	20	32	44	56	70	102	114	126	140	152	164	176	210	222	234	246	260	272	304
	7	7	21	33	45	57	71	103	115	127	141	153	165	177	211	223	235	247	261	273	305
	8	10	22	34	46	60	72	104	116	130	142	154	166	200	212	224	236	250	262	274	306
	9	11	23	35	47	61	73	105	117	131	143	155	167	201	213	225	237	251	263	275	307

STRIP FILE †

The following considerations apply only to the strip file.

CHECKWORD LOCATION

Six checkwords are written in each sector (track) in the strip file. These checkwords are located in the following byte-positions within each track.

106	874
362	1130
618	1386 (last byte of the track)

RESTORE

The unit select must be dropped (either by releasing, clearing, or disconnecting) or a restore function performed in order to prevent excessive strip wear. If a select is dropped for more than 0.8 microsecond, an automatic restore is initiated in the file.

TEST CELL

A special customer engineering test cell is provided to aid in strip file maintenance procedures. It becomes program responsibility to prevent damage (writing) of the information within this cell when the test cell is in the array.

CELL REPLACEMENT

Individual cells can be installed in any of the 10 positions of the array. When installing a cell, care must be taken to ascertain that it is in the proper position. The cell accessed by the previous operation is under the access station and not at the replacement station (Figure 2-7).

DISK STORAGE DRIVES

The following considerations apply only to the disk drive units.

Compatibility exists between the 1738 disk drive subsystem and the 3234 mass storage subsystem. However, the compatibility is limited to those features necessary for data recoverability. To accomplish this, all record gaps are of the same size, the address

† Applies to 3234-A/B/C models only

headers are recognizable by both subsystems, and the data areas contain the same number of bits. Both subsystems use a 12-bit cyclic code (checkword) for error detection.

The following differences exist in the two subsystems.

1. Data transfer:

   3234 12-bit byte

   1738 16-bit byte

   Computer formatting is necessary for conversion of word size between the two systems.

2. The 3234 subsystem utilizes a write lockout bit in the address header (refer to write lockout); this bit is not used or recognized by the 1738 subsystem.
3. The 3234 subsystem has an EOR mode available; the 1738 subsystem does not use or recognize the EOR bit.

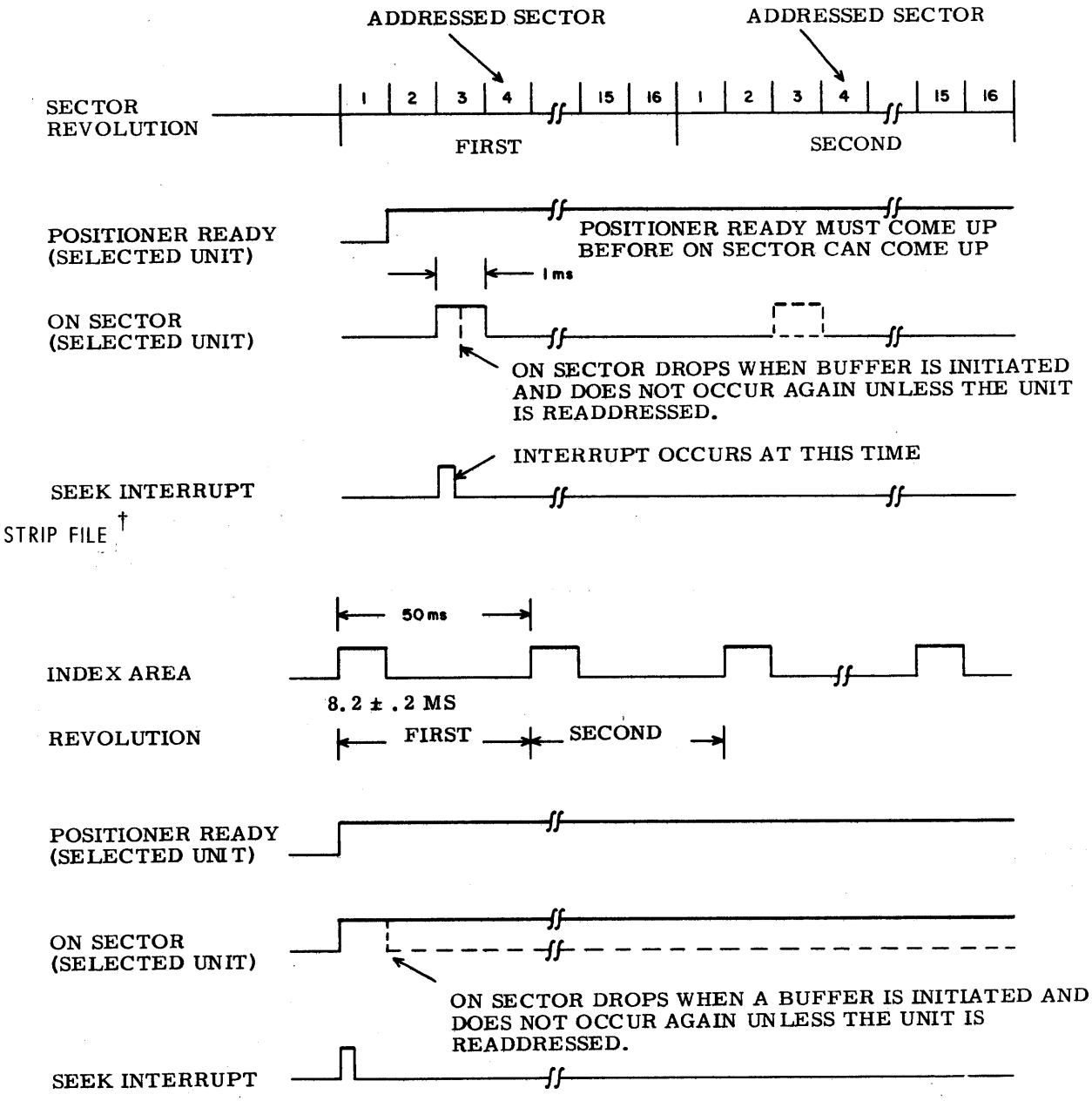
UNSAFE CONDITIONS

The presence of an unsafe condition indicates the selected storage unit has one or more of the following fault conditions and causes the controller to become not ready.

1. More than one R/W head selected
2. Both the read and write controls set
3. Erase and write driver on (strip file only)
4. Both write drives on (strip file only)
5. Read or write on and not ready set
6. Read and erase drivers both on
7. Write driver on and erase driver off (disk file and disk drive only)

SECTOR TIMING

DISK FILE AND DISK DRIVE UNITS

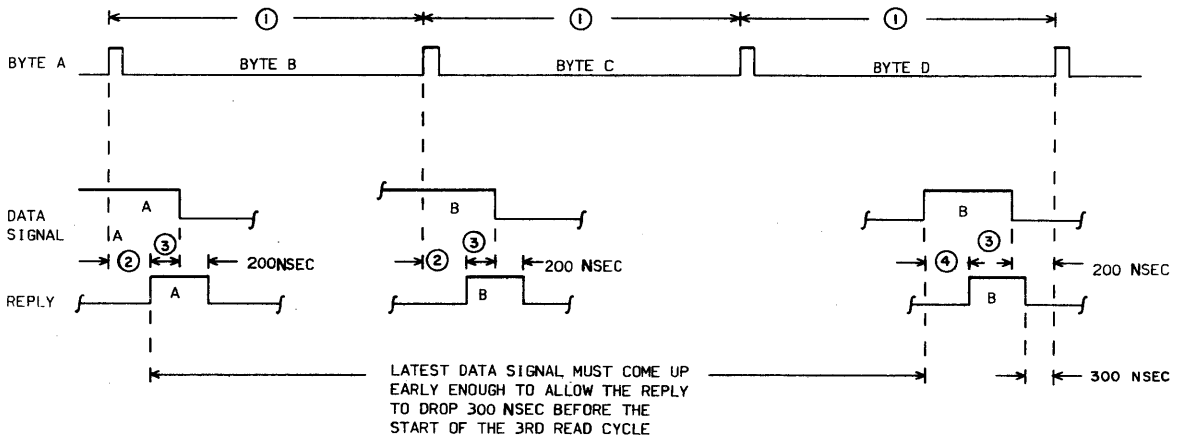


STRIP FILE †

† Applies to 3234-A/B/C only

BUFFER TIMING

INPUT



ALL TIMES ARE MEASURED AT THE CONTROLLER INTERFACE

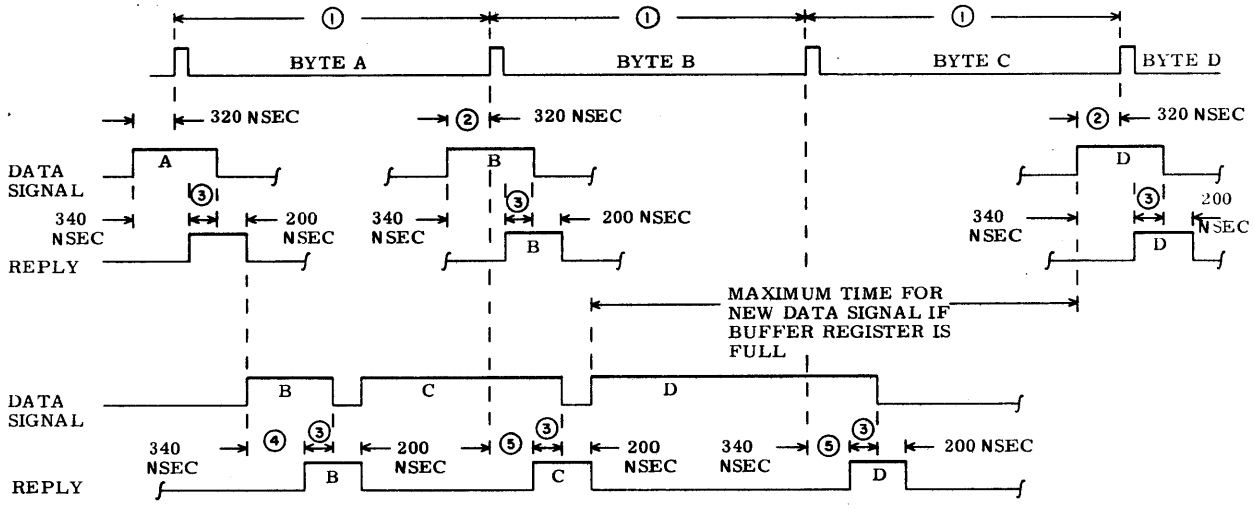
① DISK FILE 10.2 μSEC
DISK DRIVE 9.6 μSEC
STRIP FILE 27.4 μSEC

② LATEST REPLY, 700 NSEC IF BUFFER REGISTER IS EMPTY

③ CABLE DELAY AND TURN AROUND TIME

④ EARLIEST REPLY, 340 NSEC IF BUFFER REGISTER IS FULL

OUTPUT



ALL TIMES ARE MEASURED AT THE CONTROLLER INTERFACE

① DISK FILE 10.2 μSEC
DISK DRIVE 9.6 μSEC
STRIP FILE 27.4 μSEC

② IF BUFFER REGISTER IS EMPTY DATA SIGNAL MUST COME UP 320 NSEC BEFORE ITS ASSOCIATED WRITE CYCLE

③ CABLE DELAY AND TURN AROUND TIME

④ EARLIEST REPLY TO A DATA SIGNAL, 340 NSEC IF BUFFER REGISTER IS EMPTY.

⑤ LATEST REPLY TO A DATA SIGNAL, 500 NSEC FROM START OF NEXT WRITE CYCLE IF BUFFER REGISTER IS FULL

MANUAL OPERATIONS

Operation of the mass storage subsystem is under program control from the computer through the use of the connect and function codes. Initial manual starting procedures include turning power onto the equipment, selecting the various switch settings, and loading a disk pack or data cell into the associated unit (if none are presently loaded). Disk packs, disk files, and data cells must have headers recorded before they can be used for programmed operation.

POWER SEQUENCE

The following procedure brings the subsystem up from a deadstart (no power applied to the storage units or controller).

1. Turn on the unit circuit breaker and then turn on the main power circuit breaker† in the controller.

   The disk drive units and strip file automatically enter a power-on sequence. Each disk drive unit requires approximately 30 seconds to come up to speed and land the R/W heads. In a multiple unit system, each succeeding disk drive motor is automatically sequenced. The sequencing overlaps and a full complement of drive units should be up to speed in approximately 1 minute. The last disk drive (or controller if no disk drives are in the subsystem) initiates the power-on sequence in the strip files. A strip file requires approximately 10 to 15 seconds to become ready and sequence the next unit; however, the power-on sequencing does not overlap and each file begins only upon completion of the previous file becoming ready. As soon as the disk drive and strip file units become operable (R/W heads landed) and the READY indicator (located in the unit designation indicator in the disk drives) lights, operation for both the disk drives and strip files may begin; however, a 15-minute warmup period is recommended when commencing from a cold start.

2. Normally the disk file and associated hydraulic unit should have all switches in the proper position and only step 7 should be necessary to activate the units.

NOTE

Pressing the normal STOP switch requires a 20-second delay before shutdown. Pressing EMERGENCY OFF shuts down the system instantly.

† On 3234-A/C/D models, CB1 is located on the front of the power panel. On 3234-B/E models, S1 is located on top of the power distribution box.

CAUTION

Except in emergencies the blowers should remain on at all times to prevent dirt accumulation on the disk surfaces.

If the units must be started from a completely shutdown position, the following steps should be performed.

1. Open front doors on the disk file and hydraulic unit plus the right side door on the disk file.
2. Place all front panel circuit breakers of both units to the ON position.
3. Set both positioner switches to the NORMAL position.
4. Set all manual/automatic switches to the AUTOMATIC position.
5. Set FILE OPERATION switch to the AUTOMATIC position.
6. Set main circuit breaker (located below power distribution panel) to the ON position.
7. Press START and observe START indicator light. The following indicators light temporarily: LOW FILE TEMP, STACK RPM 0, STACK RPM 1, and dc voltages.

   The disk file requires approximately 3 minutes to come up to operating speed; the hydraulic unit requires approximately 15 minutes (on water-cooled unit).

LOADING AND UNLOADING PROCEDURES

The storage medium of the disk file units cannot be changed. Use the following procedures to load or change the storage medium in the disk storage drive and strip file units.

DISK STORAGE DRIVE

1. If the unit is operating, turn power off by pressing the START switch located on the front of the disk drive unit. Wait for the spindle to stop rotating.
2. Lift the disk drive unit cover upward as far as possible to provide maximum loading clearance.
3. Load or unload the pack as follows:

For loading, place the pack on the spindle and turn the cover handle clockwise to a full stop position. The pack should now be tight on the spindle and the protective cover lift off easily.

For unloading, engage the protective cover over the disk pack and rotate the cover three times in a counterclockwise direction. The pack releases from the spindle and can be lifted from the drive unit.

4. Close the disk drive unit cover and press the START switch on the front of the drive unit. This causes the unit to perform an initial seek operation which positions and loads the R/W heads and brings the unit to the ready state. (Operation cannot commence until this step is performed.)

STRIP FILE†

To facilitate a cell replacement, five operating aids are provided (Figures 2-7 and 2-8).

1. An entry door which permits access to the cell array. An interlock in the door molding prevents any machine motion while the door is open.
2. The cell location indicator which identifies (by number) the cell located in the replacement position. It also identifies the cell presently positioned at the access station.
3. SPINDLE RELEASE lever which allows the operator to manually rotate the array to any position.
4. The cell locking lever which prevents unit operation if any position is lacking a cell (normal or ballast).
5. Cell elevating door which raises the cell to facilitate cell replacement.

To remove or change a cell, use the following procedure.

1. Open the entry door (DRIVE READY indicator should go out).††
2. Open (pull out) the spindle release lever and rotate the array to place the desired cell at the replacement position.
3. Press the cell locking lever.
4. Lift the cell elevating door (the cell lifts upward about an inch).

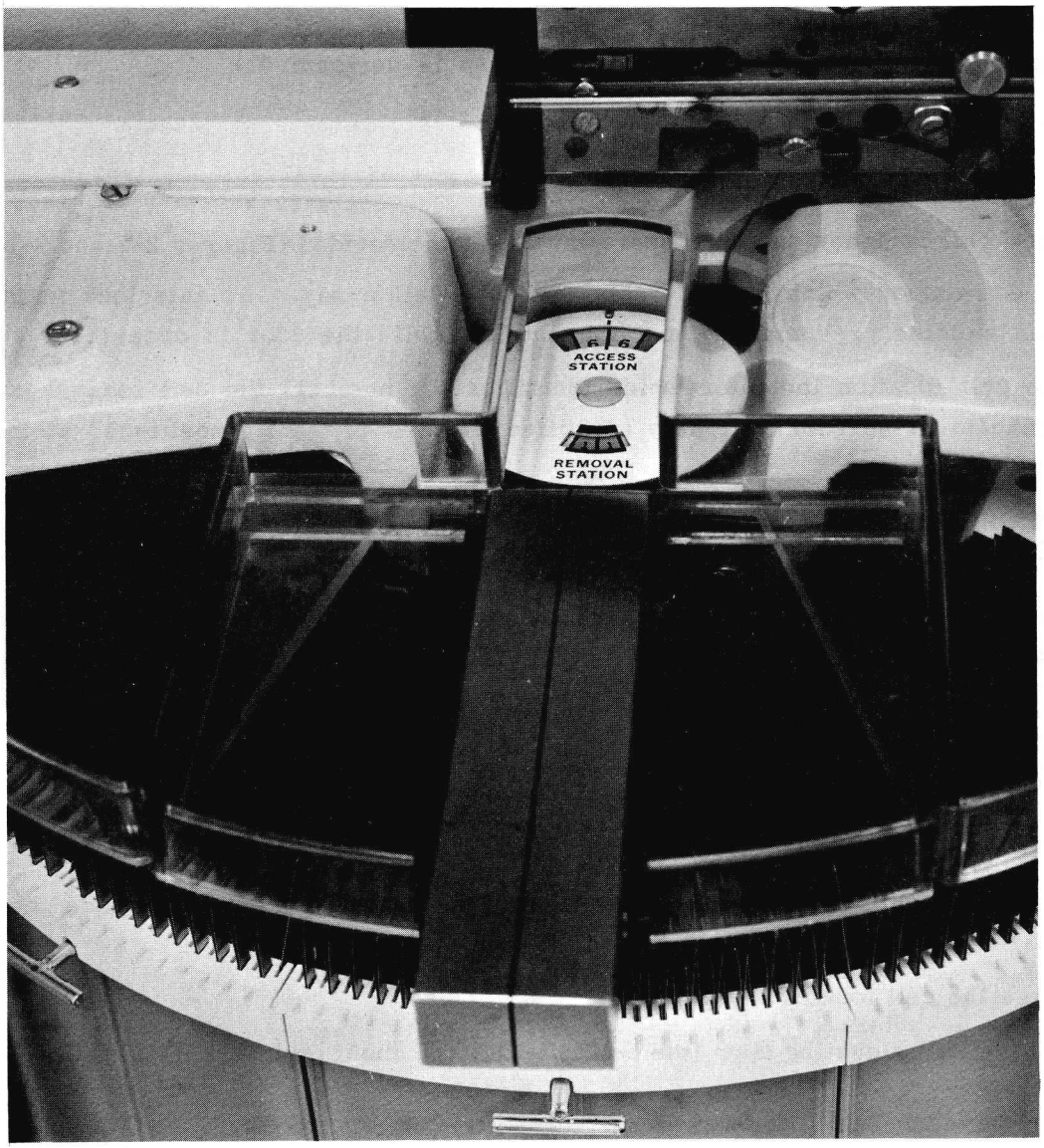
† Applies to 3234-A/B/C only
†† Door cannot be opened if the unit is selected.

5. Place a cell cover over the top of the cell and rotate the cover locking lever counterclockwise. The cell is now engaged by the cover and may be lifted from the unit and placed in protective plastic container (Figure 2-9).

To load the unit, reverse the events previously listed starting with step 4.

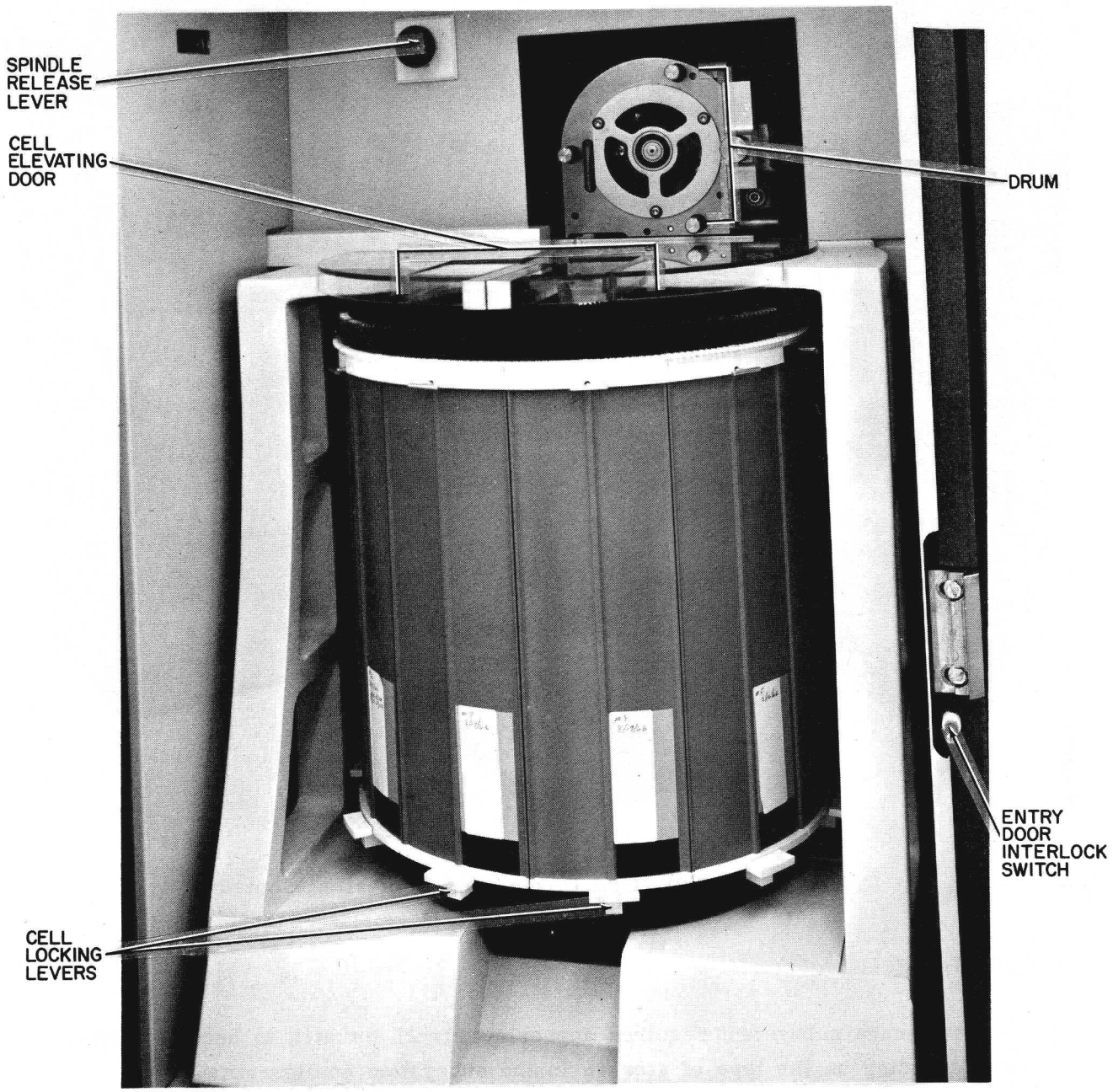
When loading is completed and the entry door is closed, the indicator light pattern should be:

AC-ON	DRIVE OP
DC-ON	DRIVE READY



2167

Figure 2-7. Cell Indicator and Elevating Door



2129

Figure 2-8. Cell Array

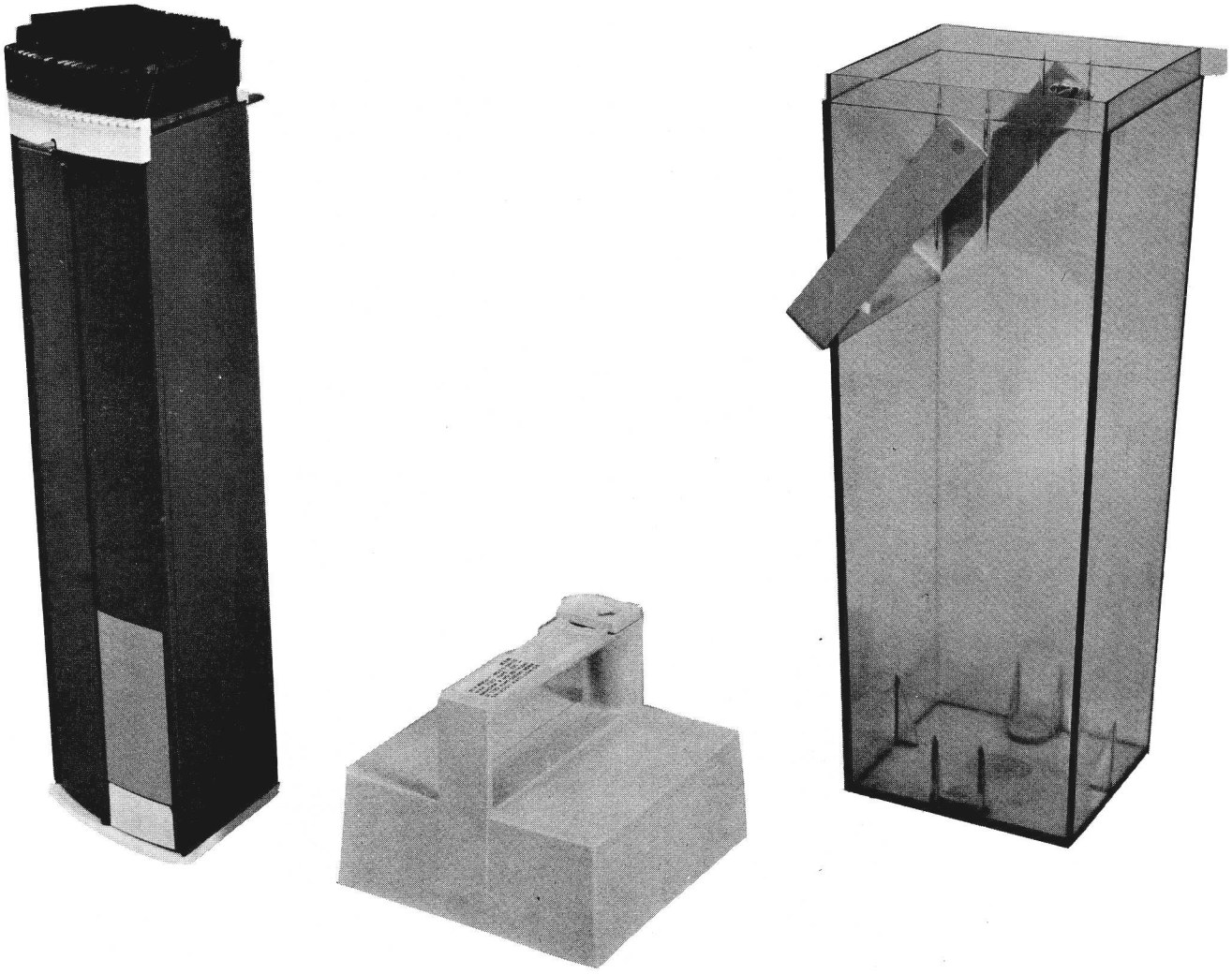


Figure 2-9. Cell, Cell Cover, and Protective Container

READY STATE

The mass storage subsystem requires approximately 15 minutes to become operative (ready) depending on the type of storage in the subsystem configuration.

The controller is always ready when power is available; however, subsystem readiness (indicated by the ready status bit) depends upon the state of the selected storage unit.

DISK FILE

The disk file units are ready only when all of the following conditions are present.

1. Power is available to the disk and hydraulic units.
2. The hydraulic and air systems are opening.
3. Hydraulic temperature ($100^{o}F$) and pressure (1150 pounds per square inch) are up to normal.
4. The disks are spinning and up to speed (1180 revolutions per minute).
5. The positioner is in the landing area and the R/W heads are landed and in an operating position.

The disks require approximately 5 minutes to come up to speed; the hydraulic unit requires approximately 15 minutes to come up to the proper operating temperature.

DISK STORAGE DRIVE

The disk drive units are ready only when all of the following conditions are present.

1. A pack is loaded.
2. The cover is closed.
3. The disks are spinning and up to speed (2400 rpm).
4. An initial seek has been performed to position the R/W head (refer to Loading and Unloading Procedures).

The disk drive requires approximately 30 seconds to bring the disks up to speed and perform the initial seek operation.

STRIP FILE †

Strip file units are ready only when all the following conditions are present.

1. A full complement of data cells or ballast (dummy) cells is in the array.
2. The cell locking lever is engaged.
3. The array door and cell elevating door are closed.
4. The spindle release knob is disengaged.
5. The drive is operative (power-on and all proper settings, etc.).
6. A strip ready condition exists (the drum is selected and the array stationary).

† Applies to 3234-A/B/C only

The strip file requires approximately 10 to 15 seconds to perform a power-on sequence and become ready; however, a 15-minute warmup period is recommended when commencing from a cold start. In a multiple unit system, each succeeding strip file is automatically sequenced; however, sequencing does not overlap and each file commences only upon completion of the previous file becoming ready.

PROCEDURES FOR WRITING ADDRESS HEADERS

Address headers are normally written from the maintenance panel. In order to write the header, defective track, and write lockout bits, the following procedure should be followed.

NOTE

Do not use the REPEAT mode switch when writing headers. Ensure that the REPEAT switch is OFF.

1. Turn the maintenance panel keyswitch ON.
2. Patch the desired PHYSICAL UNITS jumper wire into LOGICAL UNIT 0.
3. Set the DEVICE SELECT switch to the desired device type.
4. Select the desired ending mode by pressing the appropriate switch/indicator (TRACK, CYL, etc.).
5. Enter the starting addresses into the upper and lower portions of the address register. (Select the appropriate portion of the address register via the REGISTER SELECT switch and enter the starting address by pressing the appropriate register indicator/pushbutton switches.)
6. If there is no good or usable data in the sectors where new headers are to be written, the HEADER and DATA switches must be set to the WRITE position. If there is useful data in the sectors and only headers are to be written, the HEADER switch must be set to the WRITE position and the DATA switch to the READ position.
7. If write lockout and/or defective track bits are to be written, these switches should be set to ON.
8. Press the SEEK ADRS. switch.

Step 8 initiates the operation which ends when the address of the last sector of the selected storage area has been written or an abnormal condition occurs. Any abnormal condition is displayed in the status register.

NOTE

When in read data mode, the data read is not displayed in the data register.

On completion of the operation, select READ HEADERS and READ DATA and read (verify) the area just written. Error conditions are displayed in the status register. When complete, return all switches to their normal positions.

PROCEDURES FOR WRITING DATA

Data can be written from the maintenance panel. The procedure is to read headers and write data. To accomplish this, the following procedures should be followed.

1. Turn the maintenance panel keyswitch ON.
2. Patch the desired PHYSICAL UNITS jumper wire into LOGICAL UNIT 0.
3. Set the DEVICE SELECT switch to the desired device type.
4. Select the desired storage mode by pressing the appropriate switch/indicator (TRACK, CYL, etc.).
5. Enter the data to be written into the data register. Select the appropriate data register via the REGISTER SELECT switch and enter the data by pressing the appropriate register indicator/pushbutton switches.
6. Set the HEADER switch to READ and the DATA switch to WRITE.
7. The WRITE LOCKOUT and/or DEFECTIVE TRACK switches should be OFF.
8. Press the SEEK ADRS. switch.

Step 8 initiates the operation which ends when the last sector of the selected storage area has been written or an abnormal condition occurs. Any abnormal condition is displayed in the status register.

On completion of the operation, select READ HEADERS and READ DATA and read (verify) the area just written. Error conditions are displayed in the status register.

NOTE

When in read data mode, the data read is not displayed in the data register.

When complete, return all switches to their normal positions.

SAMPLE PROGRAM ROUTINES

To aid in understanding the 3234 Mass Storage subsystem, two sample programs (A and B) are included. Each program is preceded by a short explanation of the program and an associated flow chart (Figures 2-10 and 2-11). Both routines are written in 3200 COMPASS language.

PROGRAM SEQUENCE

Basic Programming Sequence

	SEQUENCE	COMMENT
1.	Connect	Connect code selects controller and peripheral unit (if available).
	Select response	If the connect operation is successful, a reply is returned; if not (controller or peripheral unit unavailable), a reject is returned. Return to connect after determining the cause of the reject.
2.	Select interrupts	Any desired interrupt conditions should be selected at this point.
3.	Load address	If a new address location (other than the one presently held in the controller address register) is desired, it should be sent prior to the execution of an operating mode selection.
4.	Select operating modes	Function code selects the desired modes of operation.
5.	Set up R/W	Function code selects a read or write function.
6.	Initiate operation	Receipt of a read or write signal initiates operation within the selected unit. Completion of the operation may be detected through the end of operation interrupt or dropping of the busy status bit.

PROGRAM A

This routine assumes the controller to be on channel 3 as equipment 5 with an 853 Disk Storage Drive as unit 0 and an 813 Disk File as unit 1. The routine utilizes the overlap seek feature by initiating positioner movement in first the disk drive, and then initiating positioner movement in the disk file. The routine then loops, searching for a successful positioner ready status on either unit. As soon as a positioner ready status is located, that unit is readdressed and one sector of data is written. The unit is readdressed again and a compare is performed to determine whether the data was correctly written. (If the data is incorrectly written, the write and compare operations are performed again.)

Upon completion of a successful compare, a similar operation is performed on the other unit. After both units have been written on and successful compares made, the program stops.

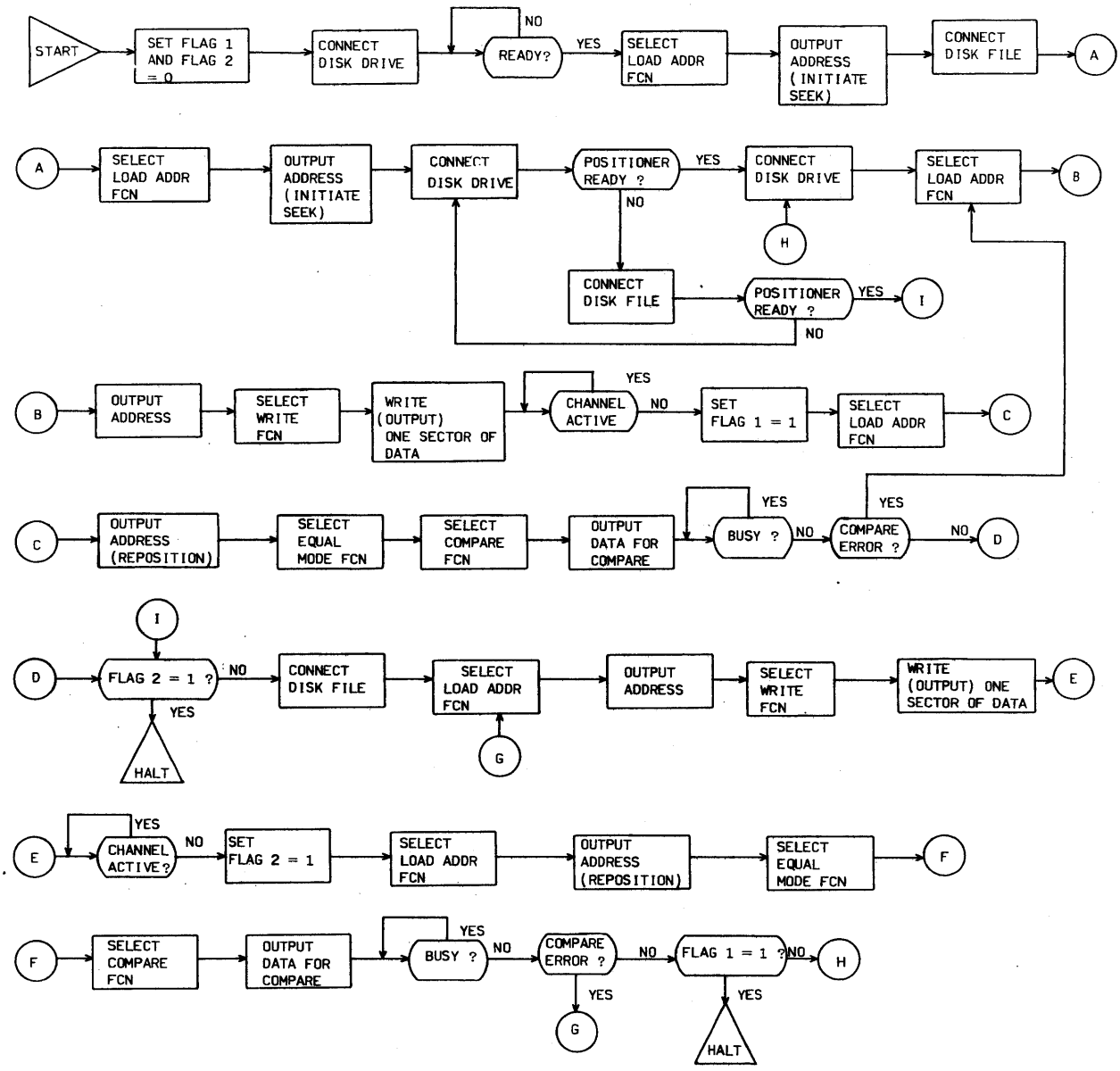


Figure 2-10. Flow Chart, Program A

```
AA      ENA     0
        STA     FLAG 1
        STA     FLAG 2
A       CON     5010B, 3        Connect disk drive zero on
        UJP     A               equipment 5, channel 3
        EXS     1, 3            Check for ready status
        UJP     *+2
        UJP     *-2
B       SEL     10B, 3          Load address function
        UJP     B
C       OUTW    3, ADDRESS 1, ADDRESS 1+1   Output disk drive address
        UJP     *-2
D       CON     5021B, 3        Connect disk file one on
        UJP     D               equipment 5, channel 3
        SEL     10B, 3          Load address
        UJP     *-1
        OUTW    3, ADDRESS 2, ADDRESS 3+1   Output disk file address
        UJP     *-2
DD      CON     5010B, 3        Reconnect disk drive
        UJP     *-1
        EXS     200B, 0         Check for the first unit
        UJP     E               that will have positioner ready
        CON     5021B, 3        Reconnect disk file
        UJP     *-1
        EXS     200B, 3         Check positioner ready
        UJP     F
DDD     UJP     DD
E       CON     5010B, 3
        UJP     *-1
ERR     SEL     10B, 3          Load address
        UJP     *-1             Reset the address register
        OUTW    3, ADDRESS 1, ADDRESS 1+1   for the disk drive
        UJP     *-2
        SEL     41B, 3          Select write function
        UJP     *-1
        OUTW    3, DATA, DATA +64   Write one sector of data
        UJP     *-2
        PAUS    40B             Wait channel inactive
        UJP     *-1
```

```
        ENA     1
        STA     FLAG 1
        SEL     10B, 3          Reposition the disk drive
        UJP     *-1
        OUTW    3, ADDRESS 1, ADDRESS 1+1
        UJP     *-2
        SEL     52B, 3          Select equal mode
        UJP     *-1
        SEL     42B, 3          Select compare function
        UJP     *-1
        OUTW    3, DATA, DATA +64   Output data for compare
        UJP     *-2
        EXS     2, 3            Wait not busy
        UJP     *-1
        EXS     20B, 3          Compare error
        UJP     ERR             Must rewrite data
F       LDA     FLAG 2          Has disk file been written on?
        AZJ,NE  H               (If yes, flag 2=1)
        CON     5021B, 3
        UJP     *-1
ERR 1   SEL     10B, 3
        UJP     *-1             Reposition the disk file
        OUTW    3, ADDRESS 2, ADDRESS 2+1
        UJP     *-2
        SEL     41B, 3
        UJP     *-1
        OUTW    3, DATA 1, DATA 1+64    Write one sector
        UJP     *-2                     of data
        ENA     1
        STA     FLAG 2
        PAUS    40B             Wait channel inactive
        UJP     *-1
        SEL     10B, 3          Reposition the disk file
        UJP     *-1
        OUTW    3, ADDRESS 2, ADDRESS 2+1
        UJP     *-2
        SEL     52B, 3          Select equal mode
        UJP     *-1
        SEL     42B, 3          Select compare function
```

```
            UJP     *-1
            OUTW    3, DATA 1, DATA 1+64    Output data for compare
            UJP     *-2
            EXS     2, 3                    Wait not busy
            UJP     *-1
            EXS     20B, 3                  Compare error
            UJP     ERR 1                   Must rewrite data
            LDA     FLAG 1                  Has disk pack been written on?
            AZJ,EQ  E                       (If yes, flag 1=1)
H           HLT     *                       End
ADDRESS 1   OCT     01400220                Disk drive address
ADDRESS 2   OCT     01200776                Disk file address
```

PROGRAM B

This routine assumes the 3234-A/B/C controller (equipped with Special Option 60076)† to be on channel 3 as equipment 1 with a strip file as unit 2. Two tests are performed which calculate the time (in milliseconds) to perform the following:

1. The time required to pick one strip
2. The time for the drum (which rotates the selected strip past the R/W heads) to make one revolution

The routine loops 10 times during the first test (operation) and then types out the maximum, average, and minimum time required to perform the operation; a similar looping and typeout is then performed for the second test (operation). The process time and typeout subroutines are not actually included in this program sample.

†Special option 60076 is the adapter for the 2321 Data Cell (strip file). Applies to 3234-A/B/C models only.

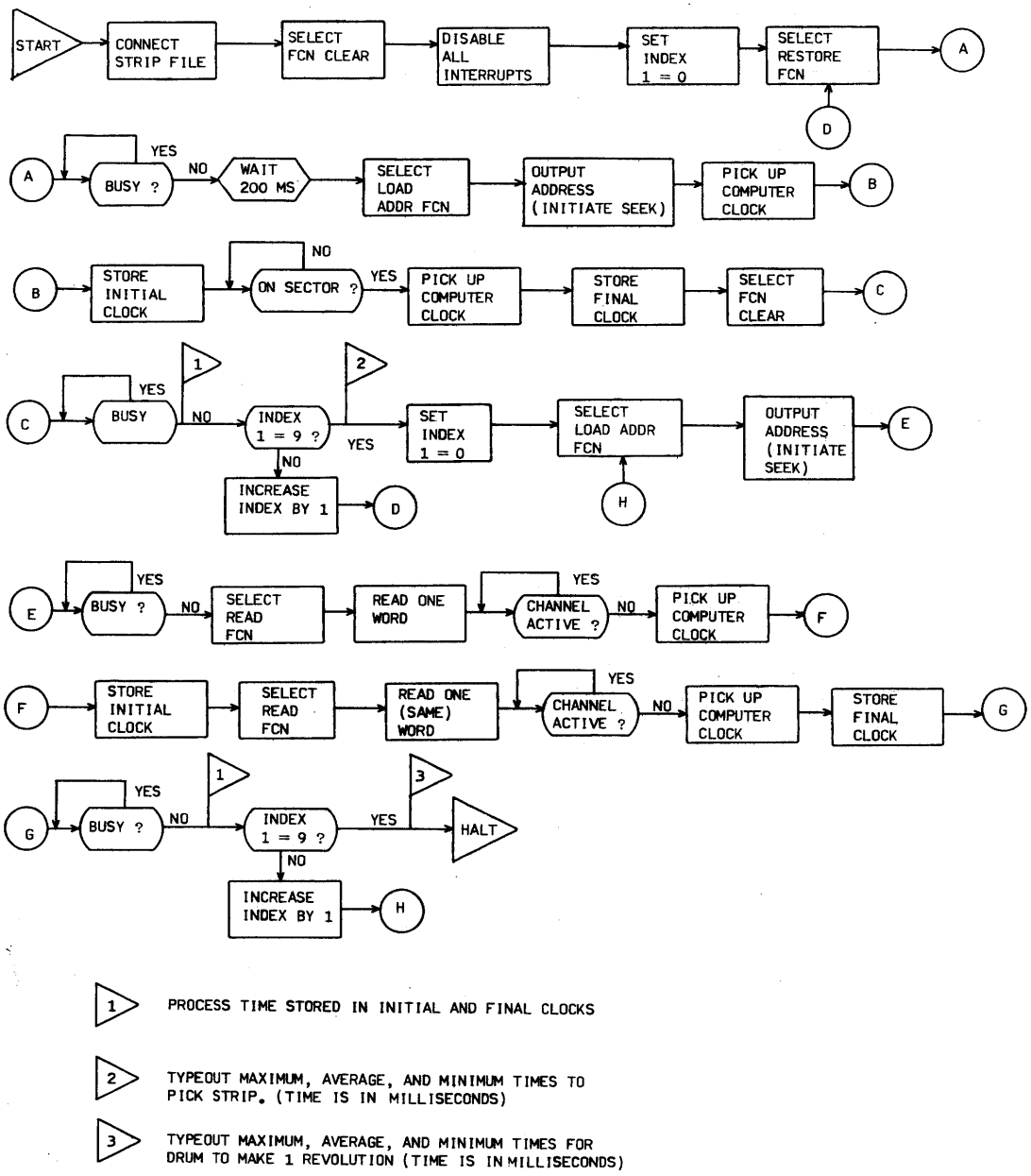


Figure 2-11. Flow Chart, Program B

CON	1002B, 3	Connect to unit 2, Equipment 1, Channel 3
UJP	*-1	
SEL	5, 3	Function clear to knockdown on sector status
UJP	*-1	
DINT		Disable interrupts
ENI	0, 1	Counter to repeat 10 times

```
A       SEL     1, 3                        Restore strip
        UJP     *-1
        EXS     1, 3                        Wait controller not busy
        UJP     *-1
        TMA     22B
        INA     200
        STA     STOR                        Wait 200 milliseconds to make
        LDQ     STOR                        sure restore is complete
        TMA     22B
        AQJ,LT  *-2
        SEL     10B, 3                      Select load address
        UJP     *-1
        OUTW    3, ADDRESS, ADDRESS+1       Output address (initiate seek)
        UJP     *-2
        TMA     22B                         Pick up clock as soon as output
                                            initiated
        STA     CLOCK I                     Store initial clock
        EXS     10B, 3                      Wait on sector status
        UJP     *+2
        UJP     *-2
        TMA     22B                         On sector-store final clock
        STA     CLOCK F
        SEL     5, 3                        Function clear to knockdown
        UJP     *-1                         on sector status
        EXS     1, 3                        Wait controller not busy
        UJP     *-1
```

Process time stored in CLOCK I and CLOCK F.

```
        ISI     9, 1                        Repeat 10 times
        UJP     A
```

Typeout maximum, average, and minimum times to pick one strip.

```
        ENI     0,1
B       SEL     10B, 3                      Select load address
        UJP     *-1
        OUTW    3, ADDRESS, ADDRESS+1       Output address (initiate seek)
        UJP     *-2
```

```
        EXS     1, 3                    Wait controller not busy
        UJP     *-1
        SEL     40B, 3                  Select read function
        UJP     *-1
        INPW    3, BUFFER, BUFFER+1     Read one word
        UJP     *-2
        PAUS    10B                     Wait channel inactive
        UJP     *-1
        TMA     22B                     Channel inactive - store initial
                                        clock
        STA     CLOCK I
        SEL     40B, 3                  Select read function
        UJP     *-1
        INPW    3, BUFFER, BUFFER+1     Read one word
        UJP     *-2
        PAUS    10B                     Wait channel inactive
        UJP     *-1
        TMA     22B                     Channel inactive - store final
                                        clock
        STA     CLOCK F
        EXS     1, 3                    Wait controller not busy
        UJP     *-1
```

Process time stored in CLOCK I and CLOCK F

```
        ISI     9, 1                    Repeat 10 times
        UJP     B
        HLT     *                       End
```

Typeout maximum, average, and minimum times for one drum revolution in milliseconds.

```
ADDRESS OCT     10330044                Address cell=2, strip=33,
                                        track (sector)=44
STOR    OCT     0
CLOCK I OCT     0
CLOCK F OCT     0
BUFFR   BSS     500B                    Read buffer
```

MAINTENANCE PANEL

The maintenance panel (Figure 3-1) is controlled by means of a locking keyswitch; however, the following items on the panel are active at all times (regardless of whether the panel keyswitch is in the ON or OFF position).

1. The eight LOGICAL UNITS and PHYSICAL UNITS designation jumpers
2. The two equipment number switches (CONTROL A and CONTROL B) and their associated CONNECTED, RESERVED, and PARITY ERROR indicators
3. The REGISTER SELECT switch
4. The register indicator/switches

NOTE

The maintenance panel switch/indicators (TRACK, CYL/STRIP, etc.) light up when pressed even when the keyswitch is in the OFF position. The switch function is active only when the keyswitch is in the ON position.

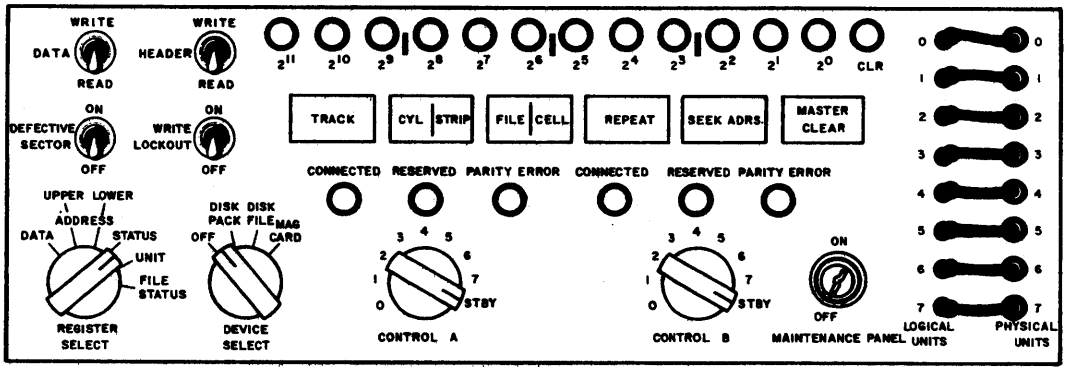


Figure 3-1. Maintenance Panel

The purpose and method of use for the various switches and indicators on the maintenance panel is explained in the following paragraphs. While the panel is designed primarily as a maintenance aid, it is necessary to activate the panel (turn the keyswitch ON) in order to write address headers or to enter defective track or write lockout bits in the address headers.

NOTE

When the keyswitch is ON and an ending mode switch (TRACK, CYL etc.) is selected, all programmed and/or manual master clears from the computer are inhibited. This prevents the possibility of the computer clearing the registers just before a seek is initiated from the panel.

MAINTENANCE PANEL

For normal programmed operation, the MAINTENANCE PANEL (keyswitch) switch must be OFF. When the switch is in the ON position, all switches and indicators on the panel are active and override any program settings in the controller. The switch is used to activate other switches of the panel.

CONTROL A AND CONTROL B

CONTROL A and CONTROL B are two sets of switches and indicators which provide individual control for each data channel physically connected to the controller. Each set consists of a rotary switch which permits varying the equipment (controller) designation from 0 through 7 and STBY, and a CONNECTED, RESERVED, and PARITY ERROR indicator which lights when the associated condition exists in the controller.

LOGICAL/PHYSICAL UNITS

These jumper wires provide for varying the LOGICAL/PHYSICAL UNITS (unit designation jumpers) designation relationship. The units of the subsystem are permanently wired in at the controller; however, their logical designation may be varied by plugging the appropriate PHYSICAL UNITS jumper into the desired LOGICAL UNITS jack. If strip files are included, they must be physical units 0 through 3. (If less than four strip files are in the subsystem, the higher order numbered units should be removed first.)

NOTE

All panel operations are through LOGICAL UNIT 0; therefore, when operating from the panel, the PHYSICAL UNIT to be operated on must be plugged into LOGICAL UNIT 0.

DEVICE SELECT

For normal programmed operation, this switch must be OFF. This rotary switch selects the device type (disk drive, disk file, or strip file) from the maintenance panel. When the keyswitch is ON, this switch instantly overrides any previous (present) programmed selection.

REGISTER SELECT

This rotary switch provides the capability for displaying and entering information via the register indicator/switches to or from the register selected. For the 3234-B/C/D/E models only, the UNIT position indicates which physical unit is connected. For the 3234-D/E models only, the FILE STATUS position causes the file status to be displayed.

REGISTER INDICATORS/SWITCHES

Thirteen indicator/switches (CLR and bits 0 through 11) provide for displaying and/or entering information to and from the register indicated by the setting of the REGISTER SELECT switch. The CLR switch clears only the selected register.

DEFECTIVE SECTOR

For normal programmed operations, this switch should be OFF. This toggle switch is used to write a defective track bit in each sector of the address headers (refer to Procedures for Writing Address Headers).

DATA (WRITE)

For normal programmed operations, this switch should be in the READ position. This toggle switch provides for writing data from the panel via the register indicator/switches. The same data (byte) is written in the entire storage area specified by the mode selection (for example, TRACK, CYL, etc.).

DATA (READ)

Provides for reading data from the selected storage area. The data read is not displayed in the data register when operating from the panel; however, a checkword error and other errors are sensed, and are displayed in the status register.

HEADER

For normal programmed operations, this switch should be in the READ position. This toggle switch provides for writing or reading address headers in the storage area selected during a control panel operation by the setting of the ending mode switches (refer to Procedures for Writing Address Headers).

WRITE LOCKOUT

The WLO bit recorded in the address header prevents the computer from writing in a sector except when the WRITE LOCKOUT switch is off and the maintenance panel key-switch is on. This combination allows the computer to override the WLO without re-writing the address header. This is the only time the keyswitch should be on when under program control. All other switches (DEVICE SELECT, TRACK, CYL/STRIP, and FILE/CELL) must be off. Data is not protected during panel operations.

Six indicator/pushbutton switches provide for selecting the ending point of an operating mode (storage area), repeating the selected operation, seeking, and master clearing from the panel. For normal programmed operations, these switch/indicators should be off. The following are the various switch/indicators and their functions.

TRACK

The TRACK switch/indicator selects the track mode in which the entire track designated by the content of the address register is operated upon.

NOTE

Operation ceases at the end of the selected mode (that is, the track or cylinder operated on is read/written only once). (Refer to REPEAT switch.)

CYL/STRIP

This switch/indicator selects cylinder (or strip in the strip file) mode wherein the remainder of the cylinder (strip) designated by the content of the address register is operated upon, starting at the address held in the address register. (The STRIP portion applies to the 3234-A/B/C only.)

NOTE

While it is possible to operate on an entire file, pack, or cell, the entire array cannot be operated on without individually selecting each of the ten cells. When using this switch, the REPEAT switch should be off since a file (cell) is not repeated automatically.

FILE/CELL

This switch/indicator selects file (or cell in the strip file) mode wherein the remainder of the file (cell) designated by the content of the address register is operated on, starting at the address held in the address register. (The CELL portion applies to the 3234-A/B/C only.)

REPEAT

The REPEAT switch/indicator is used for troubleshooting in a particular mode. When on, this switch causes the selected mode of operation to be continuously repeated; that is, when in track mode, the same track is continuously read or written. The repeat operation halts at the end of the selected storage area when the switch is off.

When in file/cell mode, this switch should be off. A file/cell is not repeated.

NOTE

The previous switch must be used for maintenance purposes only. When this switch is used, the controller does not stop for any abnormal conditions unless it is unable to continue.

SEEK ADRS.

This switch/indicator initiates a seek operation on the selected unit to the address indicated by the content of the address register. On completion of the seek, the selected I/O operation commences. (On the 3234-D/E models, when the indicator is lighted, it indicates that the MODE switch on the switch panel is not in the NORMAL position.)

MASTER CLEAR

This switch/indicator causes a master clear in the controller and selected disk drive or disk file. Master clear is not used by the strip file. If a master clear is performed while a write operation is in progress, operation ceases immediately. That sector now contains two portions of useless information and generates a checkword error if a read operation is attempted. (A no-op is generated in the strip file.)

CARD SWITCHES

The card switches (Figure 3-2)† are used in conjunction with the maintenance panel.

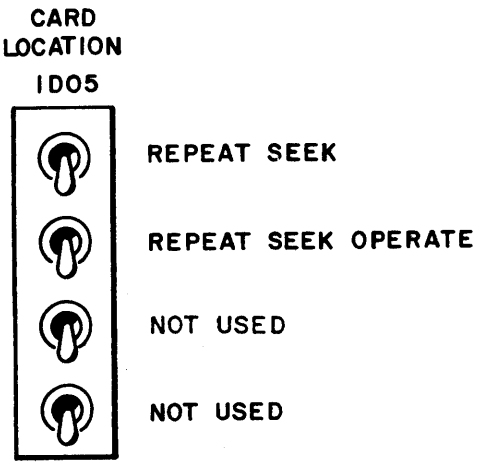


Figure 3-2. Card Switches

REPEAT SEEK

This switch is for maintenance purposes only and causes the disk unit to seek alternately between cylinder zero and the selected cylinder under the following conditions.

1. It is on (up position).
2. Track or cylinder mode is selected.
3. The SEEK ADRS. switch is pressed.

REPEAT SEEK OPERATE

This switch is for maintenance purposes only and causes the disk unit to seek alternately between cylinder zero and the selected cylinder and perform an operation under the following conditions.

1. It is on (up position).
2. The repeat seek switch is on.

† Applies to 3234-A/B/C models only

3. Track or cylinder mode is selected.

4. The SEEK ADRS. switch is pressed.

The controller stops for an error condition and the REPEAT switch does not override an error.

SWITCH PANEL

The switch panel (Figure 3-3)† is an extension of the maintenance panel and is used in conjunction with it.

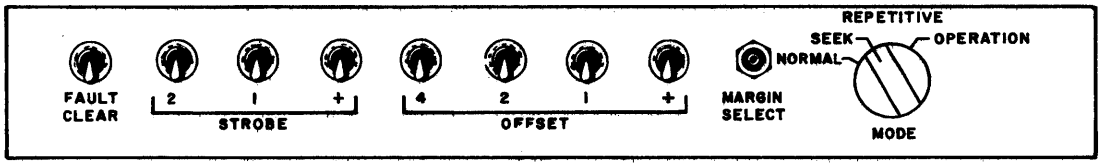


Figure 3-3. Switch Panel

MODE

The MODE switch is used for maintenance purposes. When in any position other than NORMAL, the SEEK ADRS. indicator on the maintenance panel lights. The positions are described as follows:

NORMAL: Inactive position

REPETITIVE SEEK: Causes the disk unit to seek alternately between cylinder zero and the selected cylinder when track or cylinder is selected and the SEEK ADRS. switch is pressed

REPETITIVE OPERATION: Causes the disk unit to seek alternately between cylinder zero and the selected cylinder, and to perform an operation when the track or cylinder mode is selected and the SEEK ADRS. switch is pressed

MARGIN SELECT

When pressed, the MARGIN SELECT switch transmits to the file positioner the values selected on the OFFSET and STROBE switches.

† Applies to 3234-D/E models only

OFFSET AND STROBE

The OFFSET and STROBE toggle switches are used to simulate the margin selection function offset and strobe values. The switches are set to the desired value and the MARGIN SELECT switch is pushed to pass the information to the file.

FAULT CLEAR

The FAULT CLEAR toggle switch, when up, clears fault status conditions in the file when the MARGIN SELECT switch is pressed.

COMMENT SHEET

MANUAL TITLE Control Data® 3234 Mass Storage Controllers

Hardware Reference Manual

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