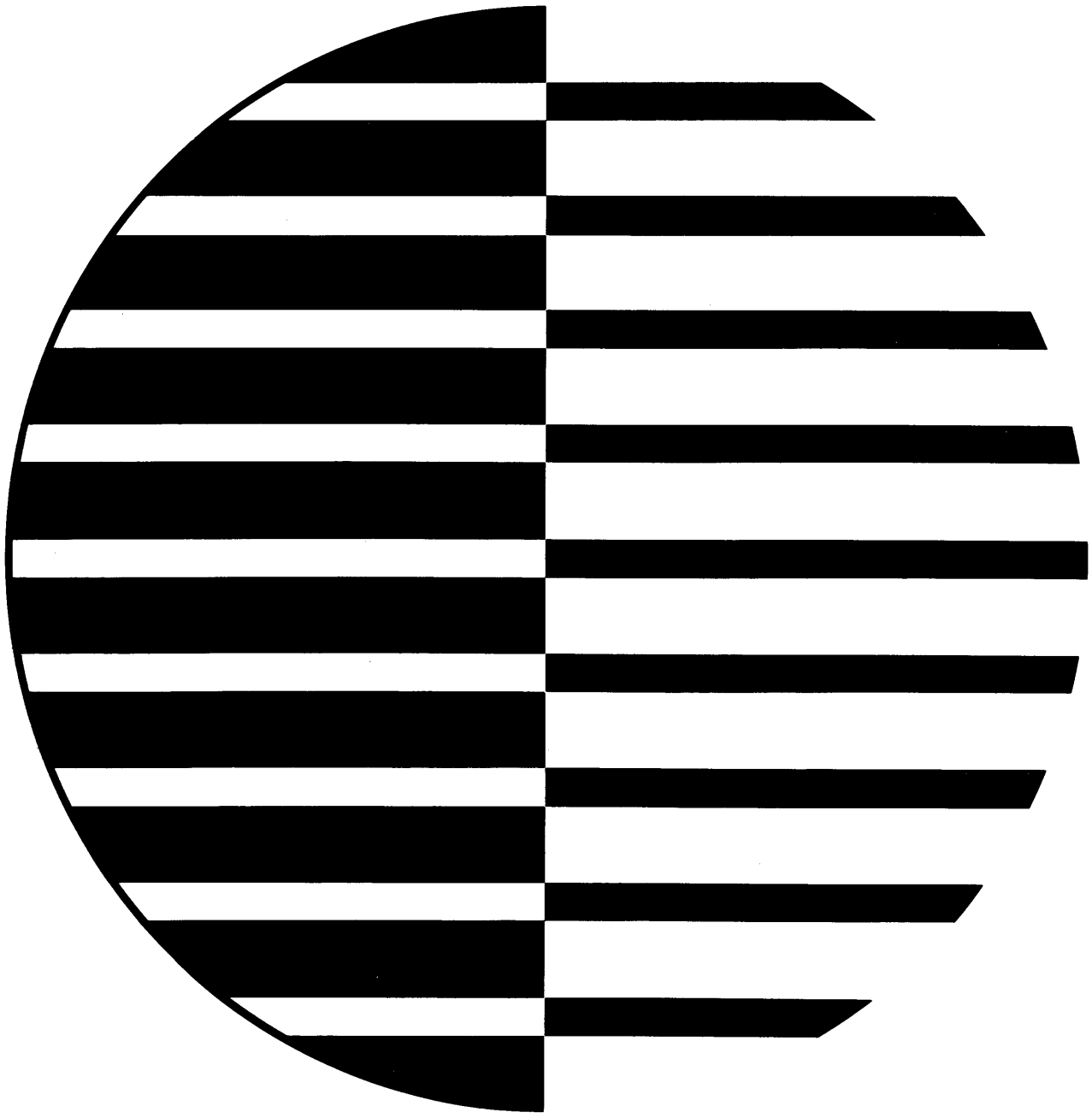
CONTROL DATA®
6400/6500/6600 COMPUTER SYSTEMS
Input/Output Specifications



RECORD of REVISIONS

REVISION	NOTES
A	Clarification of Text, pages v and 19 revised.
B	Change Order 11521 updated figures, changed cable specs and removed appendix A. This
(9-24-65)	manual obsoletes all previous editions.
C (11-9-65)	Publications Change Order CA11922, miscellaneous corrections on page 1-1.
D	Publications Change Order 14530 deleted obsolete information and incorporated new information.
(9-1-66)	Section 4 was deleted and I/O specifications for 6602/12 Console, 6603 Disk File, 6681 Data
	Channel Converter, and 6682/83 Satellite Coupler were added. Title was changed from 6000
	Series Computer System I/O Specifications to 6400/6600 Computer System I/O Specifications.
	This printing obsoletes all previous editions.
E	Publications Change Order 17433. No Product Designation affected. The following pages were
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CONTENTS

FIGURES

TABLES

1610

A CONTROL DATA 6000 SERIES COMPUTER SYSTEM

6602/6612 Display Console (foreground) - includes a keyboard for manual input and operator control and two 10-inch display tubes for display of problem status and operator directives.

Main Frame (center) - contains 10 Peripheral and Control Processors, Central Processor, Central Memory, some I/O synchronizers. The main frame in this photo is that of the 6600 Computer System; main frame for the 6400 System varies in physical appearance, depending on options included in the system.

6603 Disk file (right rear) - supplementary mass storage device; holds 500 million bits of information.

626 Magnetic Tape Transport (left rear) - 1-inch magnetic tape units for supplementary storage; binary data handled at 800 bpi.

607 Magnetic Tape Transport (left front) - 1/2-inch magnetic tape units for supplementary storage; binary or BCD data handled at 200, 556, or 800 bpi.

405 Card Reader (right front) - reads binary or BCD cards at 1200 cards per minute rate.

6681 Data Channel Converter (not shown) - permits 6400/6500/6600 computers to use 3000 Series peripheral equipment.

6682/83 Satellite Coupler (not shown) - permits direct connection between any two standard 6400/6500/6600 Data Channels.

1. INTRODUCTION

This specification describes the CONTROL DATA® 6400/6500/6600 Computer System Input/Output (I/O) characteristics and the I/O signals. Its purpose is to describe a uniform set of operating characteristics, consistent with accepted engineering practices and moderate hardware requirements, which will apply to all equipments. This information will aid in successful connection and communication between the computer and Data Channel equipment.

The 6400/6500/6600 Computer System includes 10 separate Peripheral and Control Processors, any one of which can exchange data with external equipment connected to 12 separate but identical Data Channels. Each external equipment communicates with a Data Channel via a synchronizer. Two types of cable signal transfers may be used with 6400/6500/6600 synchronizers. These are one-shot pulse transmission and static d-c level transmission.

The one-shot pulse is used for all signal transfers between a Data Channel and synchronizer.

A synchronizer changes the one-shot pulse signals used by the Data Channel into the signals required by the particular external equipment and vice versa.

The static d-c levels are used for signal transfers between synchronizer and external equipment only (e. g., 626 Tape Transport); however, one-shot pulse signal transfers may also be used here (e. g., 6602/12 Console, 6603 Disk File).

An installation may include both types of signal transfer between synchronizer and external device and both may be used on a common Data Channel.

2. CHANNEL CHARACTERISTICS

Each channel* handles 12-bit words at varying rates up to a maximum of one word every μsec, the equivalent of a one megacycle (mc) transfer rate. All channels may be in operation at the same time. Pulse communication is used on all the data and control lines of a channel, and all lines are synchronized to the Peripheral Processor* clock system. Each channel has a 12-bit bidirectional register plus several bidirectional control designators which define the status of the register and the channel.

A Channel Active designator (flag) is set from an internal source to reserve a channel for communication between a processor* and synchronizer. A Channel Inactive signal from an internal or external source clears the Channel Active flag to terminate communication.

A Channel Full flag is set at the same time a word is entered in the channel register from an internal or external source. An internal or external Channel Empty signal clears the Full flag, which in turn statically clears the channel register.

The pulses on the data and control lines are one-shot, non-repeated type transmissions, and all synchronizers must provide for storing the information. Other control includes two clock signals and one Master Clear signal for external devices. Clock signals are 10 mc (100 nsec period) and 1 mc (1 μsec period).

Channel data and control lines are grouped into two cables, input and output (Figure 2-1). The output cable carries processor signals to synchronizers; the input cable carries synchronizer signals to the processor and also carries the two processor clock signals to

* All references to channel mean Data Channel; processor refers to Peripheral Processor.

the synchronizers. All devices on a channel connect to the data and control lines in a series-parallel scheme. Each synchronizer samples the lines and unconditionally relays all signals to the next in-line synchronizer* (which may be the processor). Each synchronizer times the signal relay on the 10 mc clock signal from the processor so all synchronizers and the processor are synchronous and time-displaced from each other one or more clock periods. The scheme provides for orderly, high-speed data exchange.

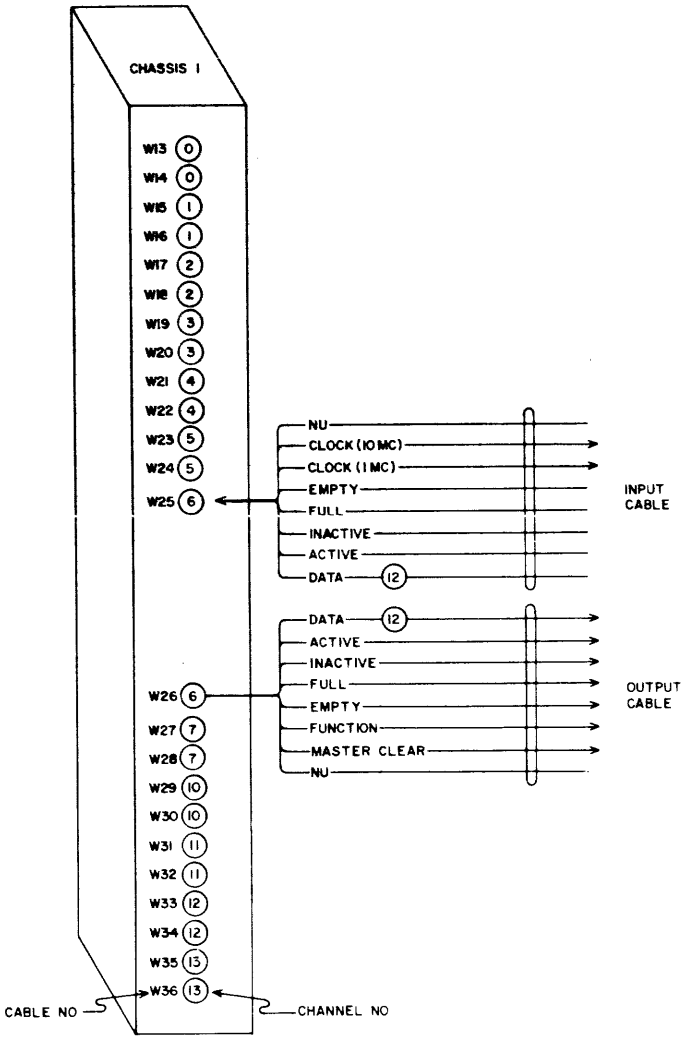


Figure 2-1. Data Channel Signals

*This is not true in the 6681 in which function codes are not relayed when the 6681 is selected.

DATA CHANNEL SIGNAL SPECIFICATIONS

The data channel cable signals are shown in Table 2-1. Separate output and input cables are used for each data channel.

TABLE 2-1. DATA CHANNEL COAXIAL CABLE LINES

INPUT CABLE	COLOR CODE	OUTPUT CABLE
Data 2^0	90	Data 2^0
Data 2^1	91	Data 2^1
Data 2^2	92	Data 2^2
Data 2^3	93	Data 2^3
Data 2^4	94	Data 2^4
Data 2^5	95	Data 2^5
Data 2^6	96	Data 2^6
Data 2^7	97	Data 2^7
Data 2^8	98	Data 2^8
Data 2^9	99	Data 2^9
Data 2^{10}	900	Data 2^{10}
Data 2^{11}	901	Data 2^{11}
Active	902	Active
Inactive	903	Inactive
Full	904	Full
Empty	905	Empty
Clock (10 mc)	906	Function
Clock (1 mc)	907	Master Clear
Not used	908	Not used

Each cable line originates and terminates at taper pins plugged directly into printed circuit module connectors.

TRANSMITTER-RECEIVER CIRCUITS

Typical data channel transmitter-receiver circuits and line voltage waveform are shown in Figure 2-2.

Binary one voltage is measured at the circuit terminals of the sending device as shown below. No voltage is impressed on the line for binary zero.

Binary one	1.4v ± 0.1v
Pulse width	35 nsec ± 10 per cent
Pulse amplitude	1.4v peak at 19 ma into 73 ohm coaxial cable terminated in its approximate characteristic impedance
Rise time	5 nsec
Fall time	5 nsec

Input circuits in the external equipment synchronizer must terminate the line in its characteristic impedance to minimize standing waves.

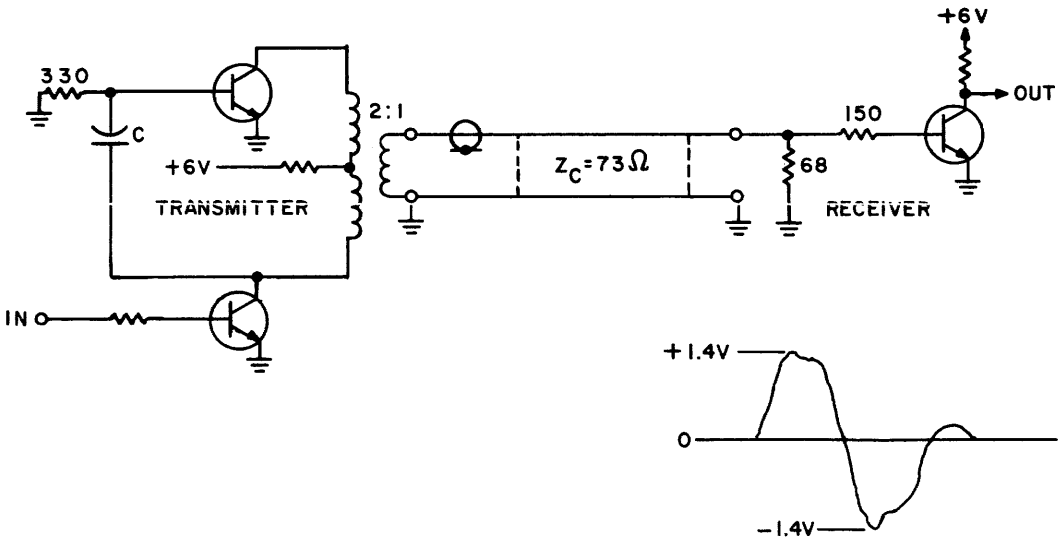


Figure 2-2. Transmitter-receiver Circuits and Line Voltage Waveform

SIGNAL TIMING

All lines connecting the processor and external equipment synchronizers are synchronized to the data channel clock signals. Signal delay on the lines and through synchronizer hardware must be taken into account to keep the data exchange synchronous. Coaxial cable delay is calculated at 1.5 nsec per foot.

The processor fills (and sends out on the line) or empties the Data Channel register at one μsec intervals or multiples thereof. In a processor data output case, if the data is sent at processor time Y, then a synchronizer can sample the lines (Y + 1.5x) nsec later, where x = length of output cable in feet.

The acknowledging synchronizer Empty signal (or Inactive signal) should arrive at the processor end of the input cable at an integral multiple of processor time Y (+0, -10 nsec) to avoid generating a runt pulse in the processor channel control. In a similar fashion, data input and Full signals from a synchronizer must arrive at the processor at an integral multiple of processor time Y (+0, -10 nsec). The clock signals available externally provide a time reference point relative to the processor and can be used for signal clocking in the synchronizer.

The 10 mc clock pulses lead data pulses by 25 nsec when a processor output word is on the lines. Processor data is identified by an accompanying Full pulse, function codes by a function pulse. Refer to Figure 2-3.

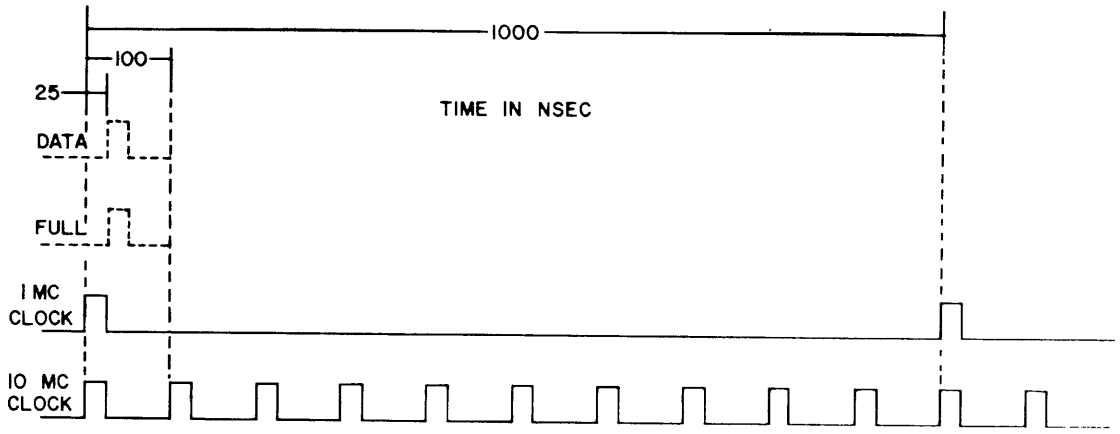


Figure 2-3. Clock Timing Sequence

Computation of cable time and signal delay time through internal hardware allows a synchronizer to place the signals on the lines for relay to the next in-line synchronizer at the same time relative to the processor, but later by an integral multiple of clock (10 mc) periods. Thus each synchronizer appears as the processor to the one next in line.

Depending on external requirements, the 10 mc clock pulses can be used to generate a multiple phase clock for incremental gating signals. The 1 mc clock pulses are synchronous with the 10 mc clock and are an alternate clocking signal for gating or other purposes.

The Master Clear line is pulsed at 4096 μsec periods as long as the DEAD START switch on the computer dead start panel is in ON position. The 1 μsec duration Master Clear establishes initial operating conditions.

SIGNAL RELAY

The signal relay is an integral part of each synchronizer. The relay is necessary in all synchronizers on a channel except in the one at the end of the line. Signal timing through the relay is at a 10 mc rate. Each synchronizer appears as the processor to the next in-line synchronizer except for a time lag of 100 nsec for each synchronizer between it and the data channel. Each synchronizer samples and stores all output signal lines in addition to sending them on to the next in-line synchronizer.

Each synchronizer also transfers all input signal lines on to the next in-line synchronizer. In addition, the device must provide for entering its signals on the same lines. The network feeding the processor (or next-in-line synchronizer) is thus an OR combination of a synchronizer and the one feeding it.

COAXIAL CABLE SPECIFICATIONS

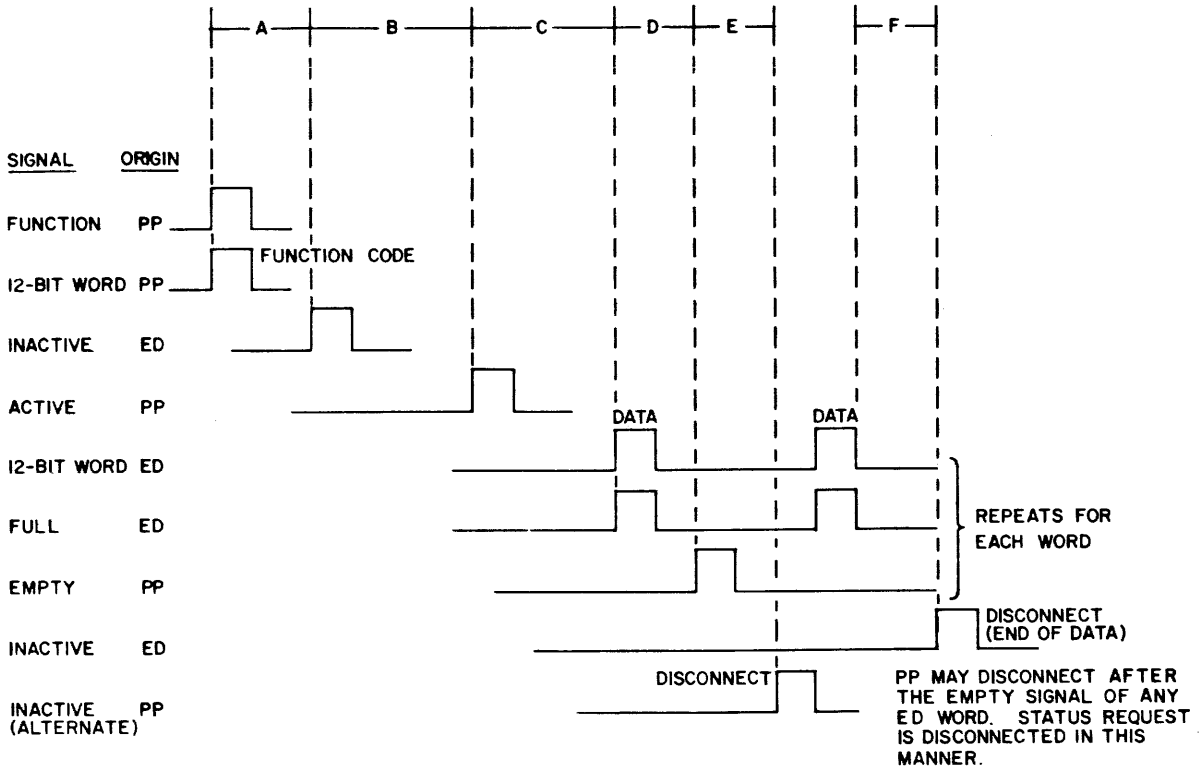
A 75-foot cable is used to connect each channel with external synchronizers. A 10-foot cable is used to connect each channel with internal synchronizers. The cable has 19 coaxial conductors, and each conductor and each shield is terminated with a taper pin. Specifications for this cable are listed below:

Cable (sheathed, coaxial)	Control Data Spec. No. 24567000
Length	10 or 75 feet
Number of coaxial conductors	19
Connectors	Taper Pins (30 AWG wire)
Impedance	70-73 ohms @ 1 mc
Line capacity	21.5 pf/foot maximum
Voltage rating	30 volt maximum

DATA INPUT SEQUENCE

An external device sends data to the processor by way of the synchronizer in the following manner (Figure 2-4):

1. The processor places a function word in the channel register and sets the Full flag and the Channel Active flag. Coincidently, it sends the word and a function signal to all synchronizers. The function signal tells all synchronizers to sample the word and identifies the word as a function code rather than a data word. The code selects a synchronizer and a mode of operation. Non-selected synchronizers clear, leaving only the selected one turned on.
2. The synchronizer sends an Inactive signal to the processor indicating acceptance of the function code. The signal drops the Channel Active flag which in turn drops the Full flag and clears the channel register.
3. The processor sets the Channel Active flag and sends an Active signal to the synchronizer which signals the device to start sending data.
4. The device reads a word and then sends the word to the channel register with a Full signal which sets the Channel Full flag.
5. The processor stores the word, drops the Full flag, and returns an Empty signal indicating acceptance of the word. The device clears its data register and prepares to send the next word.
6. Steps 4 and 5 repeat for each word transferred.
7. At the end of the transfer, the synchronizer clears its Active condition and sends an Inactive signal to the processor to indicate end of data. The signal clears the Channel Active flag to disconnect the synchronizer and the processor from the channel.
8. As an alternative, the processor may choose to disconnect from the channel before the device has sent all of its data. The processor does this by dropping the Active flag and sending an Inactive signal to the synchronizer which immediately clears its Active condition and sends no more data, although the device may continue to the end of its record or cycle (e. g., a magnetic tape unit would continue to end-of-record and stop in the record gap).



PP = Peripheral and Control Processor; ED = External Device

A. Time is a function of ED - PP recognizes inactive 1 μsec after function or at an integral multiple thereafter

B. Time is a function of PP - Minimum time 100 nsec, actual time is a function of the PP program.

C. Time is a function of ED

D. Time is a function of PP - Minimum time 100 nsec, maximum time an integral multiple of 100 nsec intervals thereafter

E. Time is a function of PP - Minimum time 3 μsec, maximum time an integral multiple of 1 μsec intervals thereafter

F. Time is a function of ED

Figure 2-4. Data Input Sequence, Data Channel

STATUS REQUEST

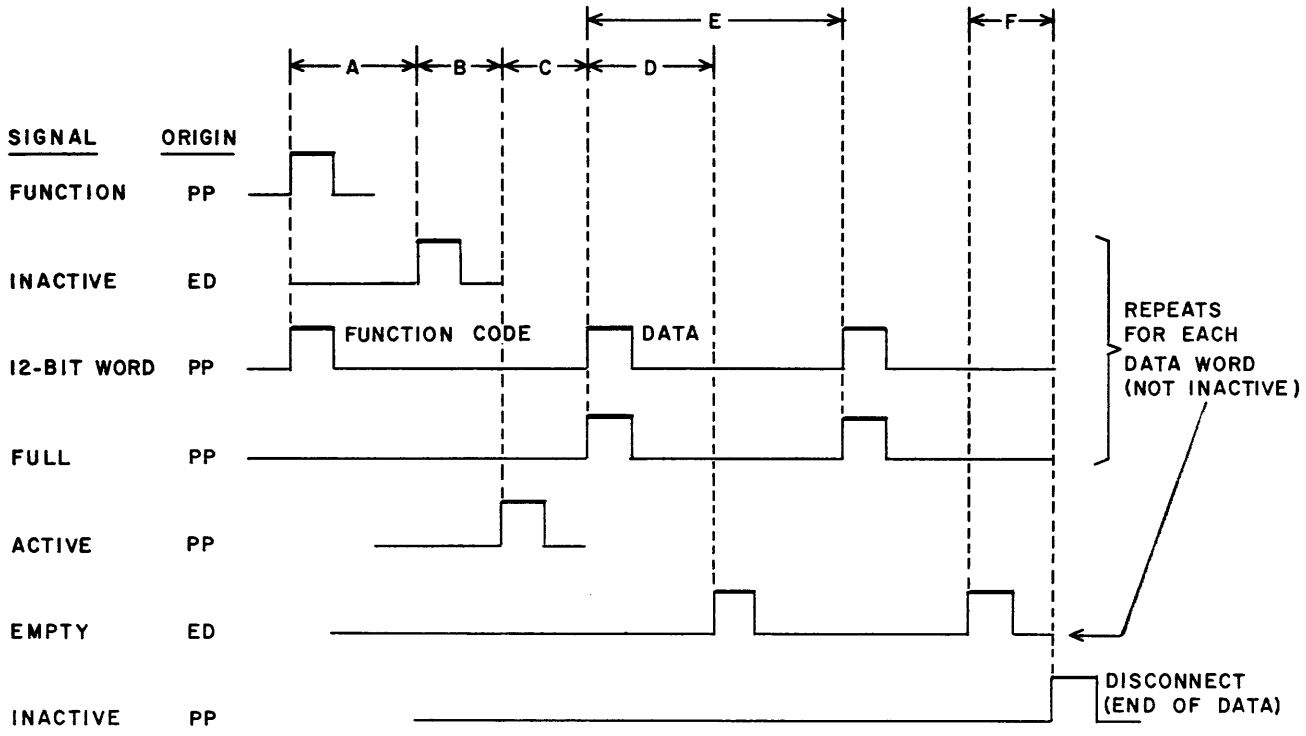
A Status Request is a special one word data input transfer in which an external device indicates a ready or error condition to a processor (Figure 2-4).

1. The processor places a function word in the channel register and sets the Full flag and the Channel Active flag. Coincidently, it sends the word and a Function signal to all synchronizers. The Function signal tells all synchronizers to sample the word and defines the word as a Function code rather than a data word. The code selects a synchronizer and places it in Status mode. Non-selected synchronizers clear, leaving only the selected one turned on.
2. The synchronizer sends an Inactive signal to the processor indicating acceptance of the Status function code. The signal drops the Channel Active flag which in turn drops the Full flag and clears the channel register.
3. The processor sets the Channel Active flag and sends an Active signal to the synchronizer which signals the device to send the Status word.
4. The synchronizer sends the status word to the channel register with a Full signal which sets the Channel Full flag.
5. The processor stores the word, drops the Full flag, and returns an Empty signal indicating acceptance of the word.
6. The processor drops the Channel Active flag to disconnect the channel and sends an Inactive signal to the synchronizer to disconnect it.

DATA OUTPUT SEQUENCE

The processor sends data to an external device in the following manner (Figure 2-5):

1. The processor places a function word in the channel register and sets the Full flag and the Channel Active flag. Coincidently, it sends the word and a Function signal to all devices. The Function signal tells all synchronizers to sample the word and identifies the word as a function code rather than a data word. The code selects a synchronizer and a mode of operation. Non-selected synchronizers clear, leaving only the selected one turned on.
2. The synchronizer sends an Inactive signal to the processor, indicating acceptance of the function code. The signal drops the Channel Active flag which in turn drops the Full flag and clears the channel register.
3. The processor sets the Channel Active flag and sends an Active signal to the synchronizer which signals the device that data flow is starting.
4. The processor places a data word in the channel register and sets the Full flag. Coincidently, it sends the word and a Full signal to the synchronizer.
5. The synchronizer accepts the word and sends an Empty signal to the processor where it clears the channel register and drops the Full flag.
6. Steps 4 and 5 repeat for each processor word.
7. After the last word is transferred and acknowledged by the Synchronizer Empty signal, the processor drops the Channel Active flag and sends an Inactive signal to the synchronizer to turn it off.



PP = Peripheral and Control Processor; ED = External Device

A. Time is a function of ED - PP recognizes inactive 1 μsec after function or at an integral multiple thereafter

B. Time is a function of PP - Minimum time 100 nsec, actual time is a function of the PP program.

C. Time is a function of PP - Minimum time 2 μsec or 4 μsec depending on instruction

D. Time is a function of ED

E. Time is a function of ED - Minimum PP time is 1 μsec

F. Time is a function of PP - Minimum time 2 μsec after empty from ED

Figure 2-5. Data Output Sequence, Data Channel

3. SYNCHRONIZER-EQUIPMENT CONNECTIONS

TYPICAL CONNECTION

6400/6500/6600 synchronizers are connected to an associated Data Channel as shown in the typical configuration of Figure 3-1.

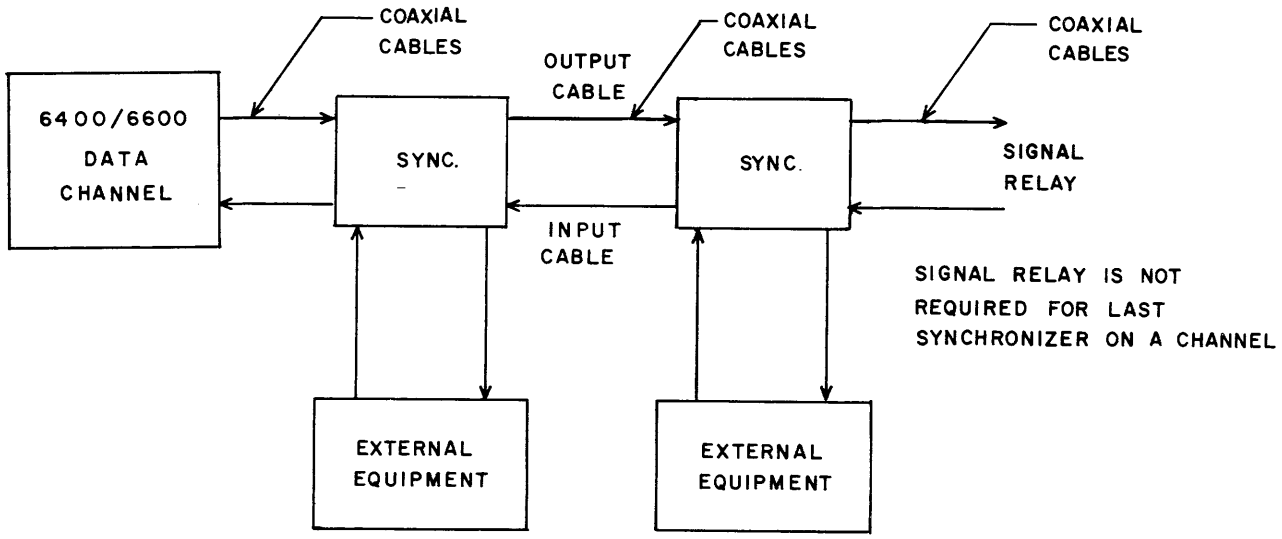


Figure 3-1. Typical Synchronizer - Equipment Connections

Several synchronizers may be connected to a common Data Channel, provided none have identical Select function codes.

SPECIAL CONNECTIONS

There are two special equipments which have a modified configuration. These are the 6681 Data Channel Converter and the 6682/83 Satellite Coupler (see Figures 3-2 and 3-3).

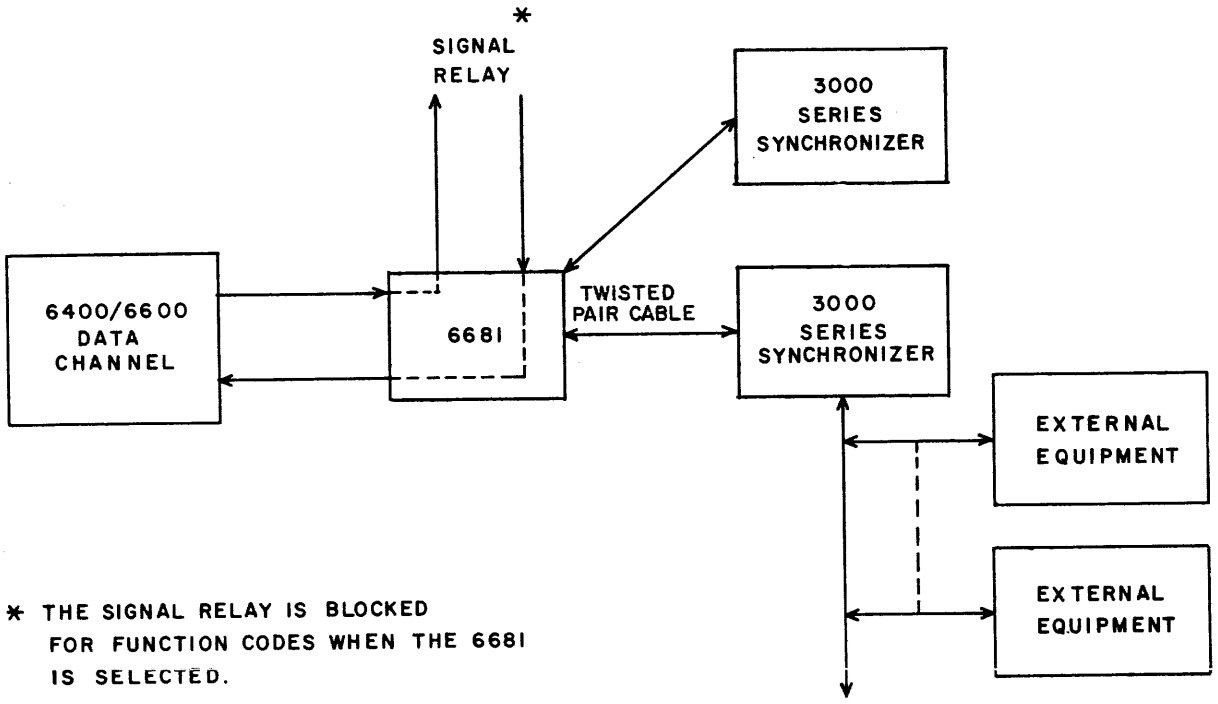


Figure 3-2. Typical 6681 Configuration

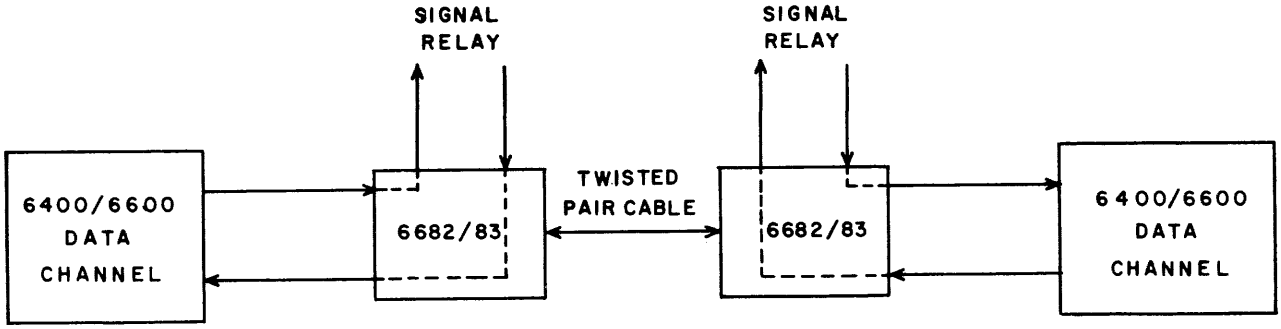


Figure 3-3. Typical 6682/83 Configuration

The 6681 may be selected by a Select function code or by performing a Master Clear. The 6682/83 and all other synchronizers may be selected by a Select function code only.

CABLE SIGNALS

Signal transfers between synchronizer and data channel is via coaxial cable as described in Section 2. Signal transfer between synchronizer and an external device is via coaxial or twisted pair cable, for one-shot pulse and static d-c transmission respectively.

The following tables list the synchronizer to equipment cables and their associated line signal names.

TABLE 3-1. 6602/12 CONSOLE SYNCHRONIZER CABLES

CABLE A	COLOR CODE	CABLE B
X BIT 0	90	KEYBOARD BIT 0
X BIT 1	91	KEYBOARD BIT 1
X BIT 2	92	KEYBOARD BIT 2
X BIT 3	93	KEYBOARD BIT 3
X BIT 4	94	KEYBOARD BIT 4
X BIT 5	95	KEYBOARD BIT 5
X BIT 6	96	KEY DOWN
X BIT 7	97	KEY UP
X BIT 8	98	UNBLANK LEFT
Y BIT 0	99	UNBLANK RIGHT
Y BIT 1	900	SMALL SIZE
Y BIT 2	901	MEDIUM SIZE
Y BIT 3	902	NOT USED
Y BIT 4	903	VERT. PUSH (ANALOG)
Y BIT 5	904	VERT. PULL (ANALOG)
Y BIT 6	905	HORIZ. PUSH (ANALOG)
Y BIT 7	906	HORIZ. PULL (ANALOG)
Y BIT 8	907	NOT USED
FOCUS/ASTIGMATISM	908	NOT USED

TABLE 3-2. 6603 DISK SYNCHRONIZER CABLES

CABLE A	COLOR CODE	CABLE B
WRITE DATA BIT 0	90	READ DATA BIT 0
WRITE DATA BIT 1	91	READ DATA BIT 1
WRITE DATA BIT 2	92	READ DATA BIT 2
WRITE DATA BIT 3	93	READ DATA BIT 3
WRITE DATA BIT 4	94	READ DATA BIT 4
WRITE DATA BIT 5	95	READ DATA BIT 5
WRITE DATA BIT 6	96	READ DATA BIT 6
WRITE DATA BIT 7	97	READ DATA BIT 7
WRITE DATA BIT 8	98	READ DATA BIT 8
WRITE DATA BIT 9	99	READ DATA BIT 9
WRITE DATA BIT 10	900	READ DATA BIT 10
WRITE DATA BIT 11	901	READ DATA BIT 11
POSITION CONTROL	902	REV. MARK
GROUP CONTROL	903	CLOCK
WRITE CONTROL	904	NOT USED
CLOCK	905	NOT USED
NOT USED	906	NOT USED
NOT USED	907	NOT USED
NOT USED	908	NOT USED

TABLE 3-3. 6681 DATA CHANNEL CONVERTER CABLES

CABLE A	PINS	CABLE B
DATA BIT 0	A1-2	STATUS BIT 0
DATA BIT 1	A3-4	STATUS BIT 1
DATA BIT 2	A5-6	STATUS BIT 2
DATA BIT 3	A7-8	STATUS BIT 3
DATA BIT 4	A9-10	STATUS BIT 4
DATA BIT 5	B1-2	STATUS BIT 5
DATA BIT 6	B3-4	STATUS BIT 6
DATA BIT 7	B5-6	STATUS BIT 7
DATA BIT 8	B7-8	STATUS BIT 8
DATA BIT 9	B9-10	STATUS BIT 9
DATA BIT 10	C1-2	STATUS BIT 10
DATA BIT 11	C3-4	STATUS BIT 11
PARITY BIT	C5-6	COMPUTER RUNNING
CHANNEL BUSY	C7-8	NEGATE BCD
NOT USED	C9-10	NOT USED
READ	D1-2	INTERRUPT LINE 0
WRITE	D3-4	INTERRUPT LINE 1
CONNECT	D5-6	INTERRUPT LINE 2
FUNCTION	D7-8	INTERRUPT LINE 3
DATA SIGNAL	D9-10	INTERRUPT LINE 4
REPLY	E1-2	INTERRUPT LINE 5
REJECT	E3-4	INTERRUPT LINE 6
END OF RECORD	E5-6	INTERRUPT LINE 7
PARITY ERROR	E7-8	NOT USED
NOT USED	E9-10	NOT USED
WORD MARK	F1-2	NOT USED
MASTER CLEAR	F3-4	NOT USED
NOT USED	F5-6	NOT USED
NOT USED	F7-8	NOT USED
TERMINATION POWER *	F9-10	TERMINATION POWER*

*Does not connect to lines in the cable.

TABLE 3-4. 6682/83 SATELLITE COUPLER CABLE

6682 TO 6682 CABLE	PINS
DATA BIT 0	A1-2
DATA BIT 1	A3-4
DATA BIT 2	A5-6
DATA BIT 3	A7-8
DATA BIT 4	A9-10
DATA BIT 5	B1-2
DATA BIT 6	B3-4
DATA BIT 7	B5-6
DATA BIT 8	B7-8
DATA BIT 9	B9-10
DATA BIT 10	C1-2
DATA BIT 11	C3-4
OUTPUT CHANNEL REQUEST TRANSMITTER	C5-6
OUTPUT CHANNEL REQUEST RECEIVER	C7-8
INPUT CHANNEL REQUEST TRANSMITTER	C9-10
INPUT CHANNEL REQUEST RECEIVER	D1-2
OUTPUT READY TRANSMITTER	D3-4
OUTPUT READY RECEIVER	D5-6
INPUT REQUEST TRANSMITTER	D7-8
INPUT REQUEST RECEIVER	D9-10
NOT USED	E1-2
NOT USED	E1-2
NOT USED	E3-4
NOT USED	E5-6
NOT USED	E7-8
NOT USED	E9-10
NOT USED	F1-2
NOT USED	F3-4
NOT USED	F5-6
NOT USED	F7-8
TERMINATION POWER*	F9-10

*Does not connect to lines in the cable.

TWISTED PAIR TRANSMITTER-RECEIVER CIRCUITS

Special twisted pair drivers are used to interface 3000 Series Logic and Cordwood Logic for external signal transfer. Typical transmitter and receiver circuits for these are shown in Figures 3-4 and 3-5. A Cordwood to 3000 transmitter can be used to drive a Cordwood from 3000 receiver. Both a transmitter and receiver may be placed on the same card and connect to common pins; in this fashion it is possible to have bi-directional signals on a single twisted pair line.

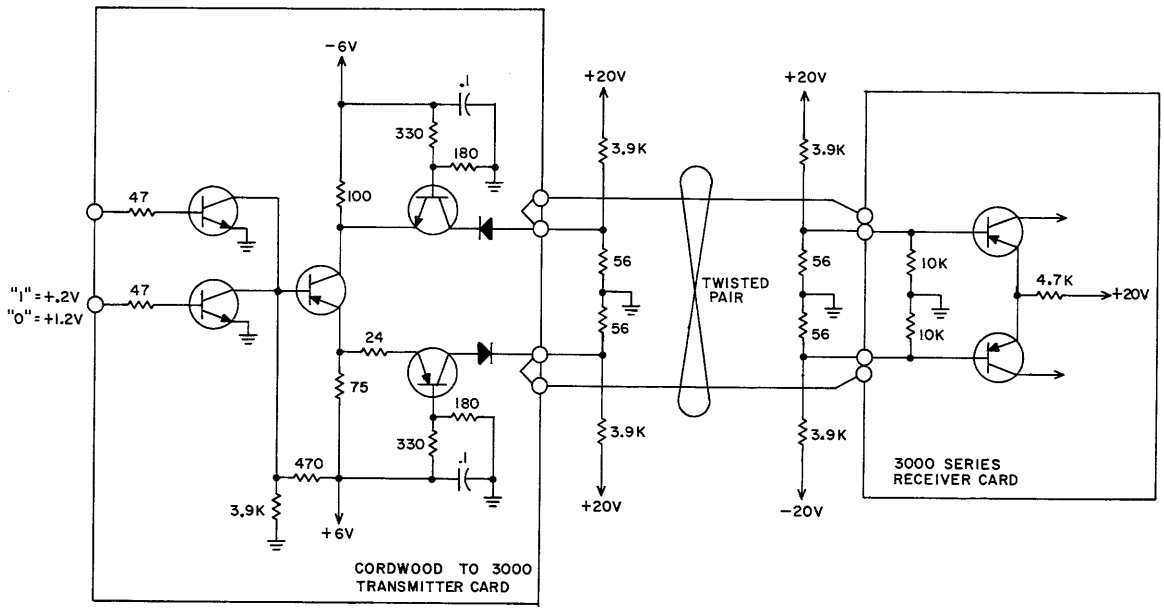


Figure 3-4. Typical Transmitter Circuit

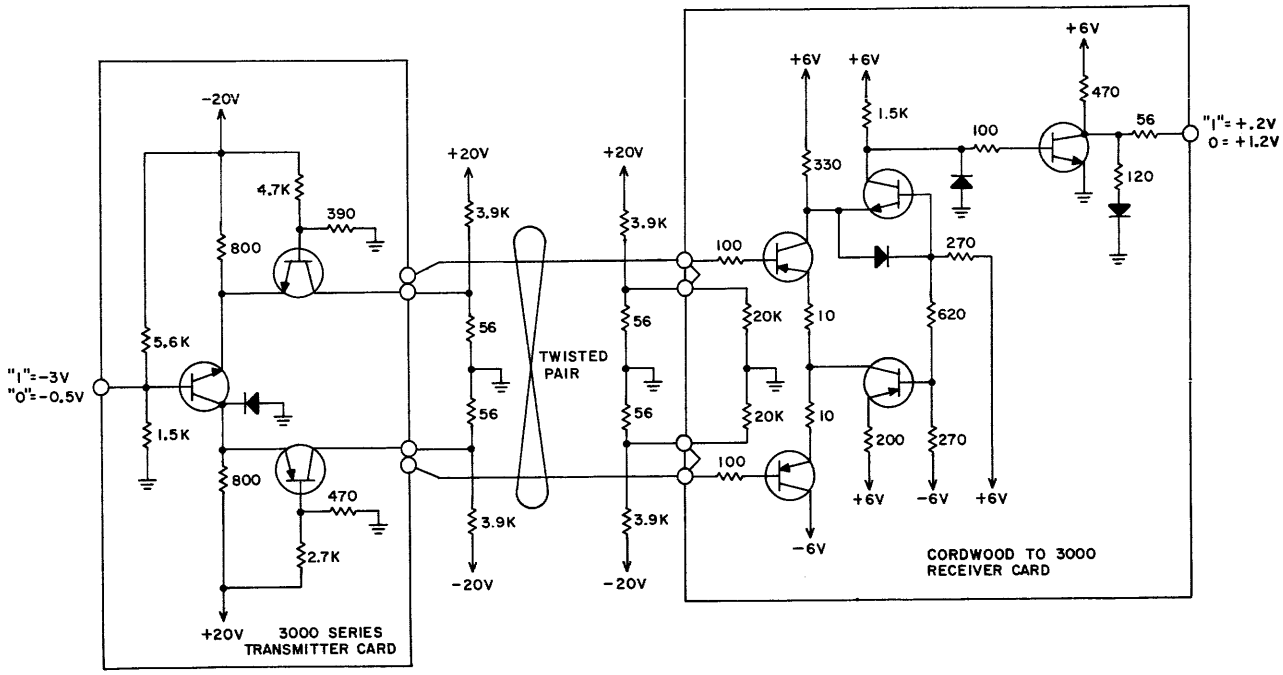


Figure 3-5. Typical Receiver Circuit

COMMENT SHEET

MANUAL TITLE CONTROL DATA 6400/6500/6600 COMPUTER SYSTEM

Input/Output Specifications

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