89638100

CONTROL DATA CORPORATION

CONTROL DATA®
CARTRIDGE DISK DRIVE CONTROLLER
FA716-A

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
MAINTENANCE AIDS
PARTS DATA
WIRE LIST

HARDWARE MAINTENANCE MANUAL

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PREFACE

This manual supplies customer engineering information for the CONTROL DATA® FA716-A Cartridge Disk Drive Controller. The controller is used with the AB107/AB108 Computer to control the 9425 or 9427 Cartridge Disk Drive. The user of this equipment should be familiar with the computer and cartridge disk drive equipment and software.

The following CONTROL DATA® publications may be useful as references:

Publication	Pub. No.
1733 Cartridge Disk Drive Controller Reference Manual	89638000
1784 Computer Reference Manual	89633400
AB107/AB108 Computer Customer Engineering Manual	89633300
I/O Specification Manual	89673100
856-2 CDD, CE Manuals	70618100 70618200
856-4 CDD, CE Manuals	70621000 70621100
System 17 Installation Manual	88996000

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SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

This section contains the functional and operational description of the CONTROL DATA® FA716-A Cartridge Disk Drive Controller.

The FA716-A Cartridge Disk Drive Controller contains the logic that interprets AB107/AB108 Central Processing Unit (CPU) function codes, controls the Cartridge Disk Drive (CDD) operations, assembles and disassembles 16-bit words between the CPU and the CDD, and provides the CDD status information to the CPU. The communication between the controller and the CPU is via the A/Q channel and the Direct Storage Access (DSA) channel. Each FA716-A may control as many as four CDD's in daisy chain configuration.

The controller logic is mounted on five 50-PAK Printed Wiring Boards. The boards may be mounted in the AB107/AB108 Computer Enclosure and power for them is supplied by the AB107/AB108 power supply.

FUNCTIONS

Interrupts

The controller may generate an interrupt due to three different conditions which may occur in the controller.

Data Interrupt

Data Interrupt will be generated when both the Data Interrupt Request flag and the Data Status are **Active.**

End of Operation (EOP) Interrupt

EOP Interrupt will be generated when both the EOP Interrupt Request flag and the EOP status are active.

Alarm Interrupt

Alarm Interrupt will be generated when both the Alarm Interrupt Request flag and the Alarm status are active.

Protect

When the Protect jumper plug is out, those I/O instructions not having the Protect bit set, will cause a Protect Violation and the command will be rejected. Director Status request is not rejected, if protect violation occurs.

INTERFACE

A single cable connects the controller with the first CDD, while each CDD has two identical interconnection plugs to enable chain interconnection. Figure 1-1 shows a typical CDD controller configuration. The interconnecting cable between the FA716-A and the first CDD is a 24 AWG copper wire twisted pairs cable having a length of 20 feet. The cable is plugged into the AB107/AB108 chassis. The standard cable between each adjacent CDD's is 10 feet long with connector CDC P/N 94351001 at both ends. Total length of daisy chain may not exceed 50 feet. The cables required for operation of the controller and the CDD are listed in Section 7 (Parts Data).

TERMINATOR

Each CDD requires a terminator (CDC P/N 46338700) when connected in a single configuration. The terminator must be placed on the last CDD unit in the daisy chain.

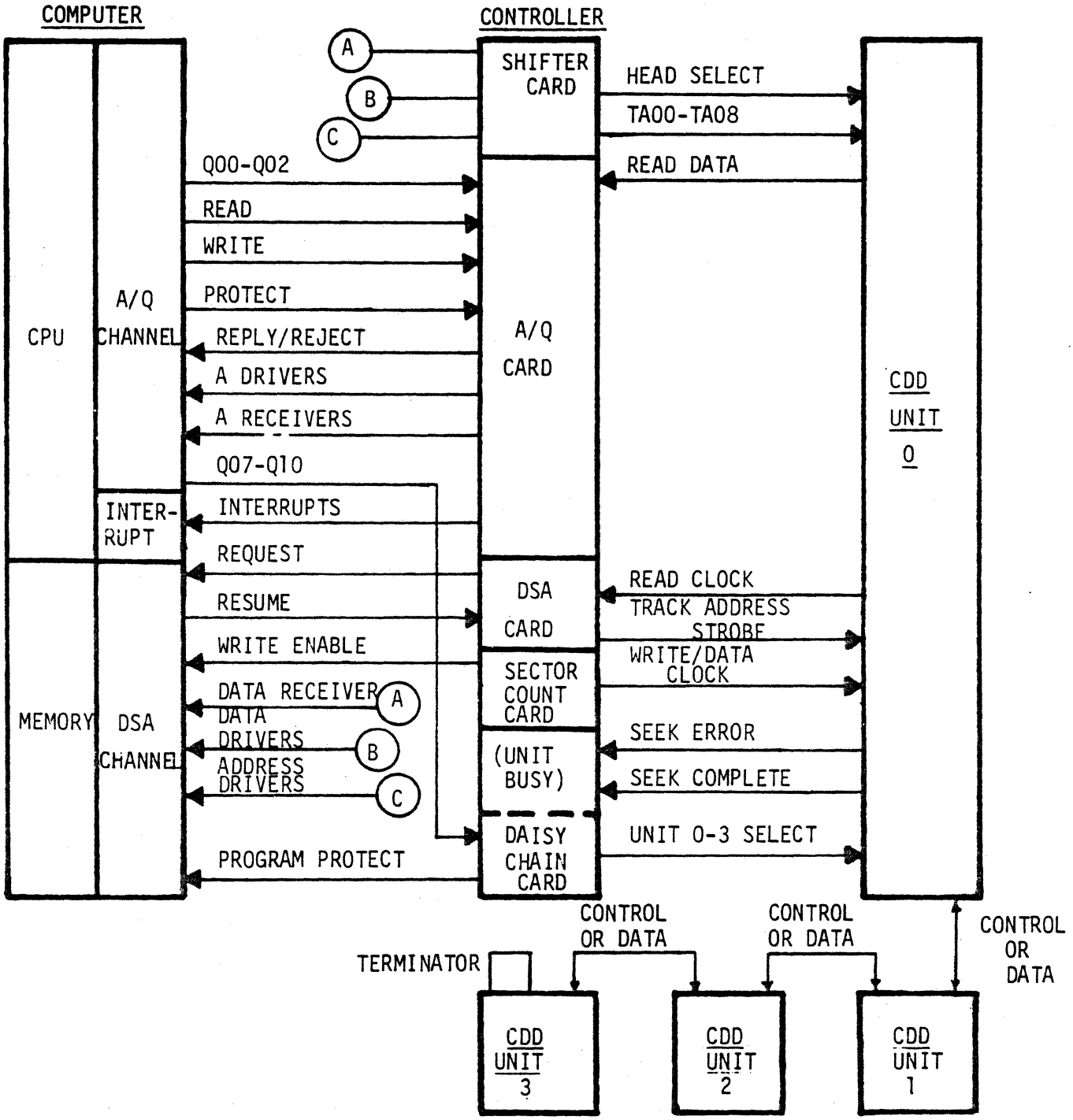


Figure 1-1. Typical System Configuration and Interface Signals

INTERFACE SIGNALS

Output Signals

The output lines carry the following signals:

1. Track Address Strobe (TA Strobe)

   This signal gates positioning information into the CDD. The positioning information is contained on the TA bit lines and is equal to the desired track address. The controller must receive an On Cylinder signal before sending a TA Strobe.

2. Track Address Bits (TA Bits 00 - 08)

   These signals are carried by nine lines and transmit the desired track address.

3. Return to Zero Seek (RTZS)

   This signal initiates positioning motion to cylinder 000 on the leading edge of the RTZS pulse (typically 1 μsec). The RTZS pulse may be repeated with the following limitations:

   a. An RTZS pulse may be sent whenever On Cylinder is present from the CDD, or

   b. An RTZS pulse may be sent without On Cylinder present if at least 300 msec has elapsed since the last RTZS pulse or TA Strobe pulse.

4. Head Select

   Two lines carry the signal that selects one of the four recording heads. The signals are the binary address of the desired head and must be held constant during a read or write operation.

TABLE 1-1. HEAD SELECTION

SIGNAL		
(DISK)	(SURFACE)	SELECTION
0	0	Cartridge top head
0	1	Cartridge bottom head
1	0	Fixed disk top head
1	1	Fixed disk bottom head

5. Write Data/Clock

One line carries the double frequency clock and data information signals to the CDD.

6. Write Gate

This signal enables write current.

7. Erase Gate

This signal enables the erase driver to pass current through the head erase coil.

8. Read Gate

This signal enables read data and clock information.

9. Unit Select

Four lines (one per unit) are used to select the desired unit. The signals or the lines must remain "on" during all communications with the unit except for monitoring of the seek complete or seek error signal. The first unit in the daisy chain is always "0", the second is "1", the third is "2" and the fourth is "3".

10. Terminator Power

+5 Vdc 630 mA (Typical) terminator power for the CDD transmission system is supplied by the AB107/AB108 via the controller.

Input Signals

1. On Cylinder

This signal indicates that the heads have reached the desired cylinder and are ready to read, write or seek. On Cylinder will also be sent when a Seek Error has occurred.

2. Read Data

Data read is separated into data pulses and clock pulses. This line carries data pulses.

3. Read Clock

Read clock signals are carried on this line.

4. Index Pulse

This signal is the index pulse from the selected unit which appears once every revolution, at the beginning of Sector Zero.

5. Sector Count

This signal is the sector pulse from the selected unit which appears at the beginning of each of the 29 sectors.

6. Fault

This signal indicates that the CDD has one or more of these fault conditions:

a. Multiple head selection
b. Read and write gate enabled at same time
c. Read and erase gate enabled at same time
d. Erase current and no write gate
e. Write current and no erase gate
f. Read, write or erase gates and no On Cylinder
g. Low voltage present (below specified values)

7. Unit Ready

This signal indicates that the CDD is operational, i.e. cartridge in, disks up to speed, and heads loaded.

8. Seek Complete or Seek Error

Four lines carry signals to indicate that the corresponding unit has completed a seek (Seek Complete) or is unable to complete a seek (Seek Error). This is a signal transmitted with or without the unit being selected. The Seek Complete is a static "1" which is cleared by a selected read gate or another seek command.

The Seek Error signal indicates that the heads have moved to an illegal address or that a seek was not completed within 200 msec. When a seek error occurs the CDD will reposition the heads to cylinder zero. When the heads reach cylinder zero On Cylinder will be indicated along with seek error (typically 125 ±55 nsec after the leading edge of seek error). An RTZS command sent to the unit indicating a seek error will clear the seek error condition, return the heads to cylinder zero, and enable an On Cylinder signal to be sent to the controller.

A Seek Error will cause the Seek Complete or Seek Error line to become a static "1", which can be cleared only by a Return to Zero Seek Command.

9. Terminator Monitor

This line (Slot 16, P2A05) is monitored by each unit to sense loss of controller power. This line is terminated by + 5Vdc through 100 ohms at each end. In the event of controller power loss, Unit Select is disabled. The unit will not respond to any commands until power is restored.

UNIT NUMBER

The Unit Number is defined as the position of the CDD in the daisy chain. This is accomplished by shifting the Unit Select lines between CDD's, each CDD in turn using the first line, as shown in Figure 1 - 2.

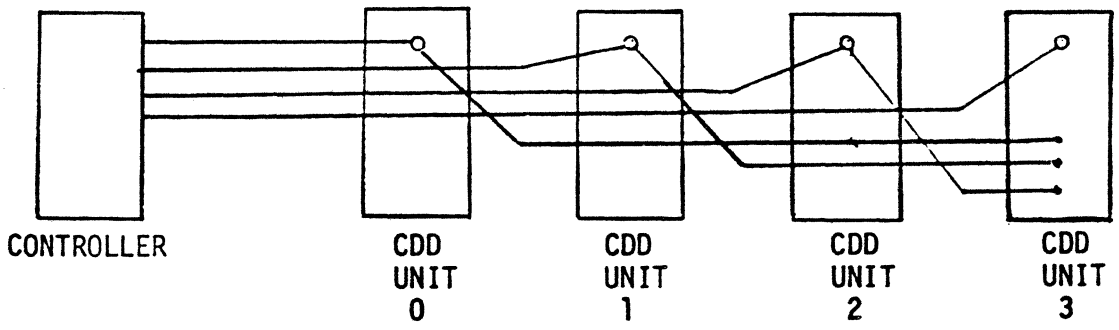


Figure 1-2. Unit Number Select Connection

SECTION 2

OPERATION AND PROGRAMMING

OPERATION AND PROGRAMMING

For operation and programming information refer to 1784 Computer Reference Manual, Publication Number 89633400, and the CDD Controller Reference Manual, Publication Number 89638000.

SECTION 3

INSTALLATION AND CHECKOUT

For complete installation and checkout information on this and other components of the System 17 consult:

Publication No. 88996000
Control Data System 17 - Installation Manual

INSTALLATION

Unpacking

1. Carefully remove wrapping from the 50-PAK controller cards. Check for physical damage to each card and record damage on the packing list. Check that part numbers agree with parts list.

2. Remove wrapping from cables and check for physical damage. Record damage on packing list. Check that part numbers agree with packing list.

Physical Limitations

Care must be taken to prevent damage to the controller cards. The cards must not be flexed, bent or dropped.

Power Requirements

The controller cards require +5 vdc derived from the power supply of the computer.

Cabling and Connectors

An external interconnecting cable is available for use with the controllers for connection between the computer and the disk drive. The external cable (part no. 89700400) is 25 feet long.

The internal cable (part no. 89700200) used between the back of the computer and the connector pins on the back plabe, is 15.5 inches long.

The interrupt cable (part no. 89724702) is 13.8 inches in length.

The last Cartridge Disk Drive must be equipped with a terminator (CDC part no. 46338700).

The total length of all interconnecting cables (including daisy chain cables) must not exceed 50 feet.

The wire lists for pin assignments will be found in Section 8.

Cooling Requirements

The controller cards are cooled by the forced air system of the computer. No further cooling is required.

Environmental Considerations

The environmental considerations necessary for operation (or storage) of the controller cards are listed in the Detailed Specifications of Table 1-1.

Preparation and Installation

To install the controller perform the following:

1. Inspect the enclosure, card slot, PW board slides and connector pins, for physical damage.
2. Place the Equipment Number, Protect and Scanner jumpers in the proper positions on each card. Refer to CDD controller reference manual 89638000.
3. Place the interrupt cable in the applicable position on the back plane. Refer to Table 3-1 and the 1784 Computer System Reference Manual 89633400.
4. Install controller internal cable between location 16, P2, on back plane and the output connector at the output location provided.
5. Install the external cable between the connector panel and CDD Unit 0.
6. Carefully install the controller cards in the assigned card slots. The card must slide in smoothly. The slots must be selected as shown in Table 3-2.

CAUTION

Do not install controller cards
in computer with power on.

CHECKOUT

1. Refer to the CPU/computer reference manual, publication number 89633400 and the CDD reference manual, publication number 89638000, for operation of the controller.
2. Determine that proper voltages are supplied to the controller card by measuring +5 vdc between test points 1 and 63 on the card.
3. Perform diagnostics check as described in the System Maintenance Monitor (SMM17) Manual, Publication Number 60182000.

TABLE 3-1. INTERRUPT CABLE INSTALLATION

The Interrupt cable will be installed between slot 19, connector/pin P2B18 and any of the following positions selected as required:

Line	Slot	Connector/Pin
1	25	P1B10
2		A07
3		B07
4		A05
6		A06
7	25	B06
8	26	B05
9		A10
10		B10
11		A07
12		B07
13		A05
14		A06
15	26	P1B05

TABLE 3-2. CARD LOCATIONS

PW Board	Location (slot)
Disk Daisy Chain	15
Disk DSA	16*
Disk Selector Count	17
Disk Shifter	18
Disk A/Q	19

* Internal cable will be connected to back plane at location 16,P2.

SECTION 4

THEORY OF OPERATION

SCOPE

Section 4 contains a functional description of the FA 716-A Cartridge Disc Controller operations. A general block diagram is provided in Figure 4-3 and detailed timing charts are available at the end of this section. Section 5 contains detailed logic diagrams for all the PWB's of this controller and a description of functional units. A general overview of the dynamic processes during certain functions in the controller are provided in Section 4. The diagrams and text in Section 5 focus on details which had to be omitted from the overview, but are essential to diagnostic and maintenance operations.

FUNCTIONAL DESCRIPTION

General Overview

The Cartridge Disc Controller is interfaced to the A/Q Channel and the Direct Storage Access (DSA) of the 1784 Computer. Operations are initiated from the A/Q Channel and are monitored by Status and Interrupt requests. The DSA interface is used exclusively for the transfer of data and addresses to or from the memory of the computer on a cycle stealing basis. Once an operation has been initiated through the A/Q Channel it may run to completion without further program action. The controller accepts data from the cartridge disc drive (CDD) in serial form and assembles it into 16 bit words which are transferred to the computer memory. Conversely, the 16 bit words accepted from the DSA are serialized by the controller before transmission to the CDD.

Basically the Cartridge Disc Drive is capable of two operations - Read or Write. Other functions can be considered as derivatives of these basic functions. The Compare function reads data from the disc and compares it with data input from the memory of the computer.

The Checkword Check Operation reads data and compares the checkword previously recorded on the disc with the checkword generated during the read operation. The Write Address function, as the name imples, writes addresses on the 29 Sectors of the track specified by the contents of the Cylinder Address Register in the controller.

Equipment Selection

Several equipments may share the input/output interface of the computer. For this reason jumper plugs are used on the PWB to select a discrete equipment number between 0 to 15 ($0\text{-}F_{16}$) for the disc controller. During the output of a command sequence, the same equipment number is carried in bits 07 through 10 of the Q Register. Only the controller where the equipment number set into the jumper plugs matches the bits coming from the Q Register, will respond to the computer with a Reply. The controller in turn can have up to four Cartridge Disc Drives. These individual CDD units are selected through bits 9 and 10 coming from the A Register of the computer.

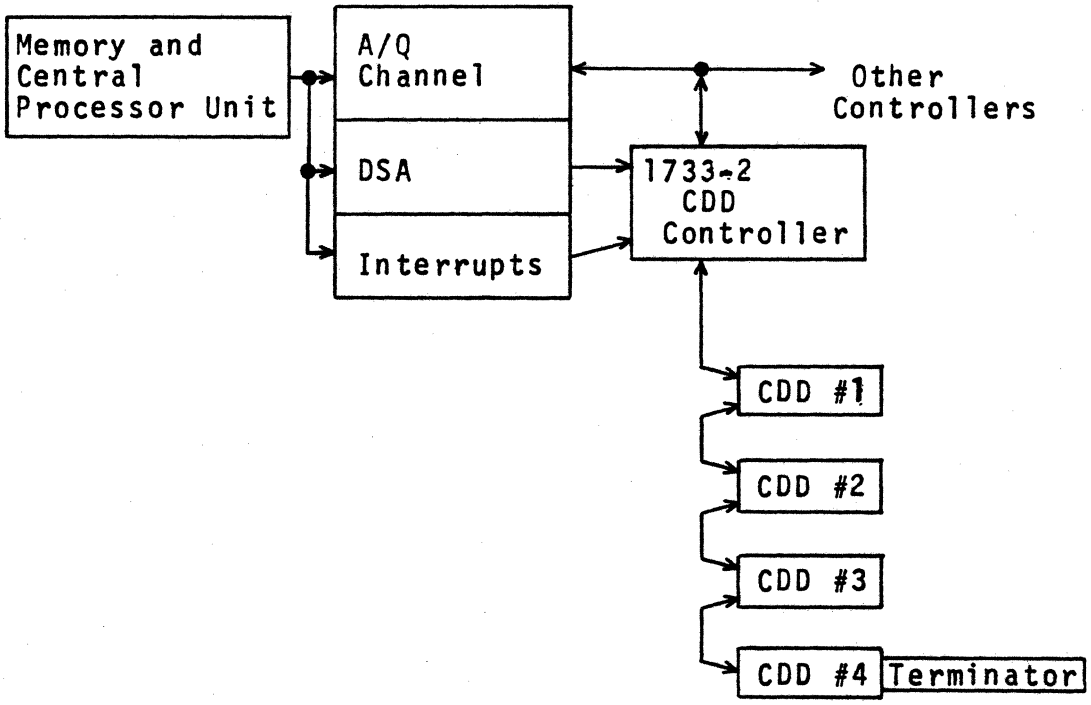


Figure 4-1. I/O Block Diagram

Operation Initiation

All operations in the controller are initiated by an INP or an OTP command in the computer program. At the time that an INP or OTP instruction are executed, the A/Q Channel transmits the Equipment Number (Bits 7 - 10 of the Q Register), the W=0 condition and either the A/Q Read or A/Q Write signal (OTP = A/Q Read; INP = A/Q Write).

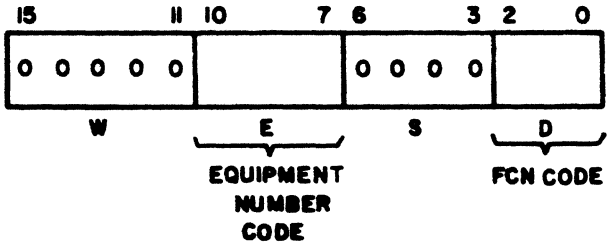


Figure 4-2. Q Register Format

TABLE 4-1. FUNCTION CODES

Value set in Q (Bits 02-00)	OTP Output from A	INP Input to A
000	Load Buffer	Clear Controller
001	Director Function	Director Status
010	Load Address	Cylinder Address Status
011	Write	Current Word Address Status
100	Read	Checkword Status
101	Compare	Drive Cylinder Status
110	Checkword Check	Illegal
111	Write Address	Illegal

Bits 0 through 2 of the Q Register define the contents of the A Register. Bits 7 through 10 of the Q Register must match the equipment number setting on the PWB of the controller. The W Portion of the Q Register must be zero. The Function Codes are described in this section.

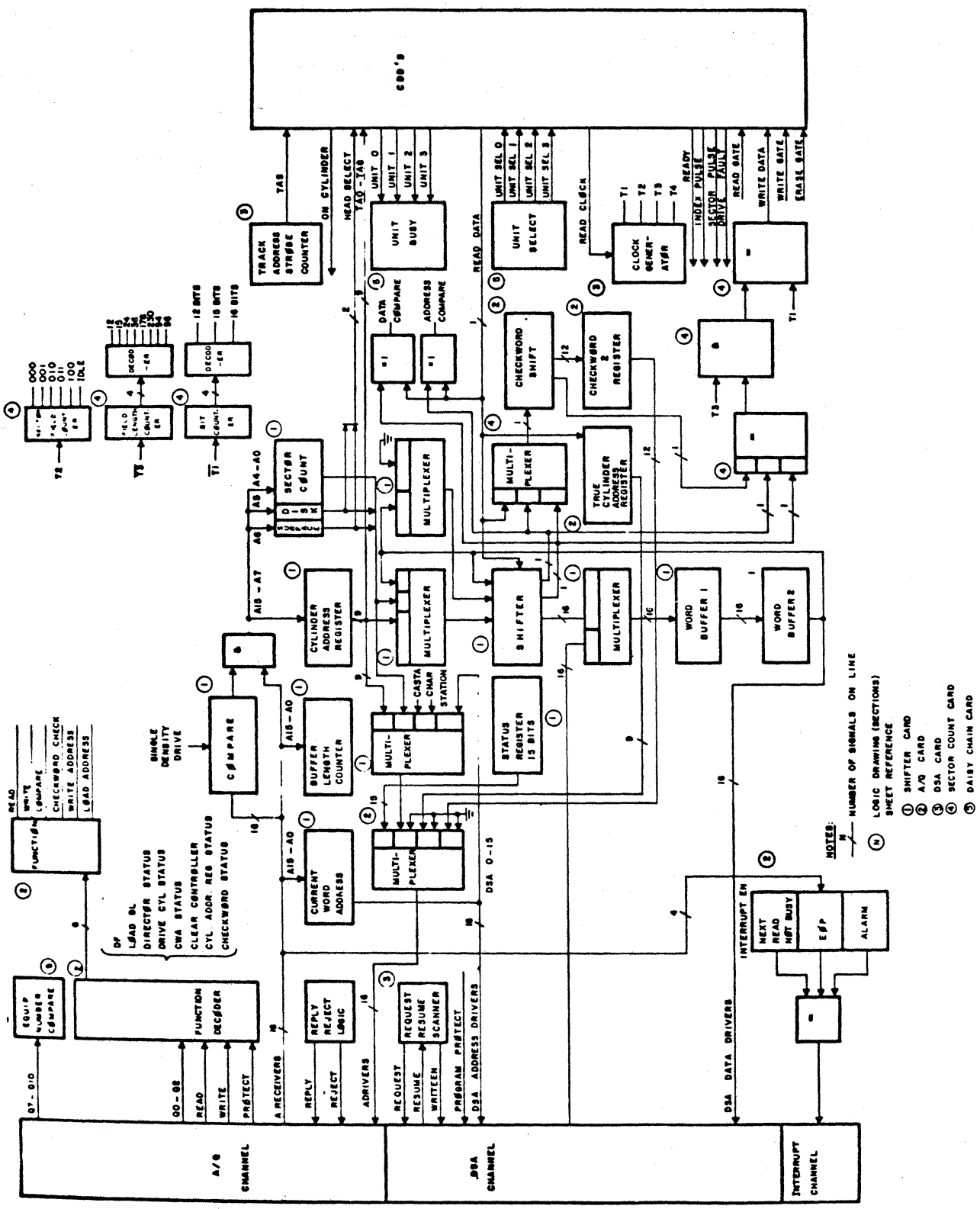


Figure 4-3. CDD Controller Block Diagram

Record Addressing

Addressing of the records is under program control. Records within the file are accessed by a 16-bit File Address Word sent to the drive via the AQ channel. The address word is divided into four parts, the sector, disk, surface and cylinder. Bits 0 through 4 designate one of the 29 sectors within a track. Bit 5 designates either a fixed (bit 5 = 1) disk, or the removable (bit 5 = 0) cartridge disk, and bit 6 specifies one of two surfaces in a cylinder (bit 6 = 0 specifies "top" surface; bit 6 = 1 specifies "bottom" surface). Bit 7 through 15 designates one of 406 cylinders within a disk. The File Address Word format is shown in Figure 4-4.

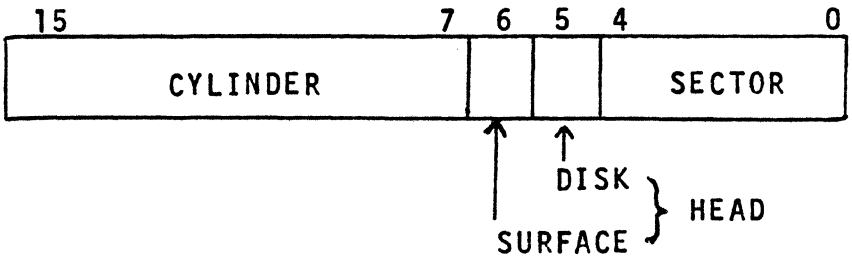


Figure 4-4. File Address Word

The file, disk, cylinder, track, and sector are defined as follows:

File - The file is defined as the entire recording surface available in the CDD unit.

Disk - The disk is defined as the entire recording surface on both sides of one disk; either the cartridge disk or the fixed disk.

Cylinder - The cylinder is defined as the recording surface on both surfaces of the cartridge and fixed disk at a given position of the head positioner.

Track - The track is defined as the recording surface under one read/write head at a given cylinder position.

Sector - The sector is defined as one data record and is the smallest addressable section of the file. The sector is 1/29th of a track and contains 1536 data bits or 96 sixteen-bit data words.

The sector includes head gaps and sync patterns in order to synchro-

nize the data between a drive and the controller.

Sector Format

The total sector length is 2155 bits of which 1536 bits are data. Bit assignments are as indicated in Figure 4-5.

The head gap is required to allow the current to stabilize after turning on the read/write heads. The sync patterns are written as all zeros except for the least significant bit which is a 1 denoting the end of the pattern. the sync pattern enables the controller to recognize the start of serial data bits from the drive. The 24-bit Address Format is shown in Figure 4-6. The controller generates and writes a checkword at the end of each address written and also at the end of each data record. The checkword is used during a Read to verify the accuracy of the data previously written. If the checkword does not agree with that which was written, a Checkword Error status bit will be set.

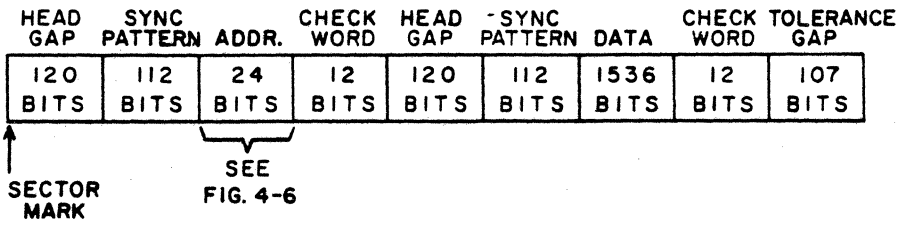


Figure 4-5. Sector Format

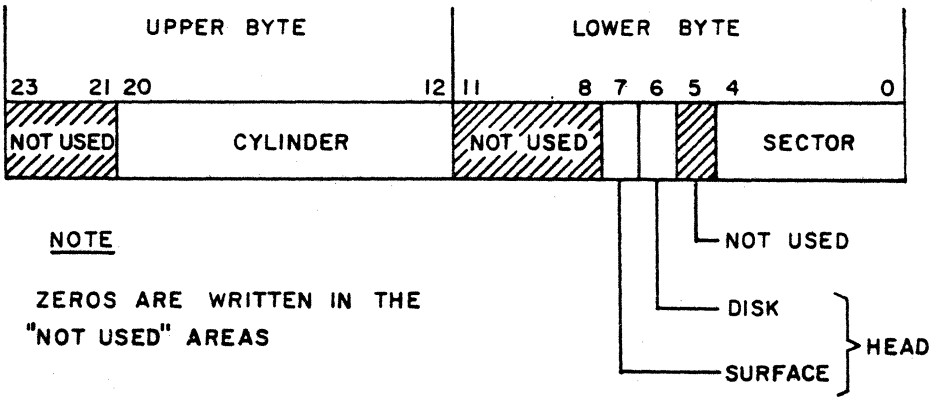


Figure 4-6. Address Format on CDD

Disk Organization

Refer to Figure 4-7 for view of disk organization.

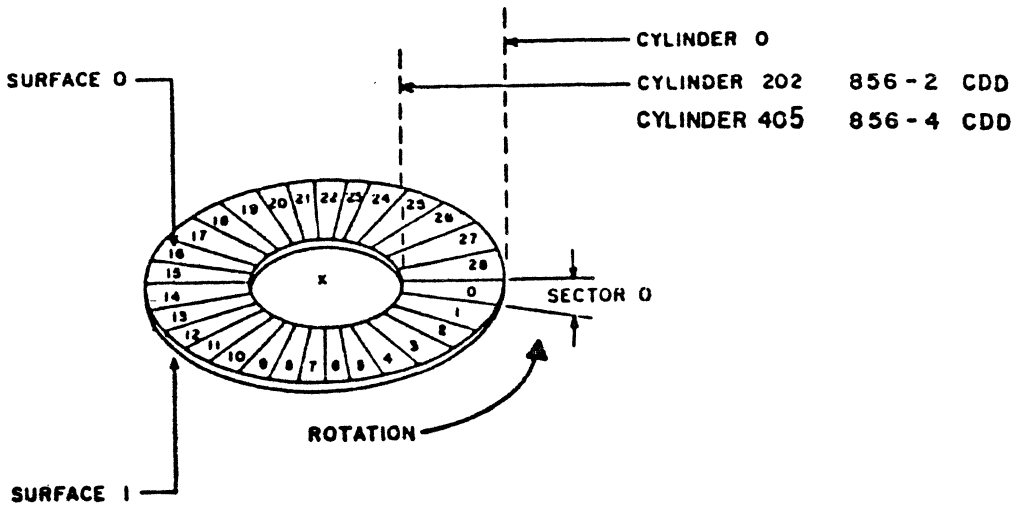


Figure 4-7. Disk Organization

SPECIFICATIONS

Storage Characteristics

Data Format:	16 bits per word	
	96 words per sector	
	29 sectors per track	
	2 tracks per cylinder	
856-2 CDD	203 cylinders per disk	
856-4 CDD	406 cylinders per disk	
	1 (or 2) disks per drive	
	Up to 4 drives	
Data Capacity:	1,536 bits per sector	(96 words per sector)
	44,544 bits per track	(2,784 words per track)
	89,088 bits per cylinder	(5,568 words per cylinder)
856-2 CDD	18,084,864 bits per disk	(1,130,304 words per disk)
856-4 CDD	36,347,904 bits per disk	(2,271,744 words per disk)
856-2 CDD	36,169,728 bits per drive (max)	(2,260,608 words per drive)
856-4 CDD	72,695,808 bits per drive (max)	(4,543,488 words per drive)

Access Time

Head Positioning time	35 msec (ave); 70 msec (max)
Cylinder-to-cylinder positioning time	7 msec
Latency time	25.0 msec (one disk revolution)
Access time (positioning plus latency time)	47.5 msec (ave); 95.0 (max)

Transfer Rate

Bit rate	0.4 usec per bit (2.5 Mega bits/ sec)
Word rate	6.4 usec per 16-bit word (156K words/ sec)

Checkword

The checkword is a cyclic code generated from the data or address by the controller. The checkword is the remainder which is obtained by dividing the data or the address (which is taken as a code polynomial) by the polynomial:

$$(X^{12} + X^{11} + X^3 + X^2 + X + 1)$$

Example:

1 0 1 ..... 1 1 0 1	Binary data or address record
$X^n + 0 + X^{n-2} \ldots X^3 + X^2 + 0 + 1$	Polynomial representation (where X is a dummy variable)
Record Polynomial	
$X^{12} + X^{11} + X^3 + X^2 + X + 1 =$	Quotient Polynomial + Remainder Polynomial = Coefficient of Checkword

These polynomials are treated according to the theorems of ordinary algebra with one exception, addition is done in modulus two.

$$1X^a + 1X^a = 0X^a + 0X^a = 0X^a$$

$$1X^a + 0X^a = 1X^a, \quad 0X^a + 1X^a = 1X^a$$

The generation of the checkword is represented by the diagram in Figure 4-8.

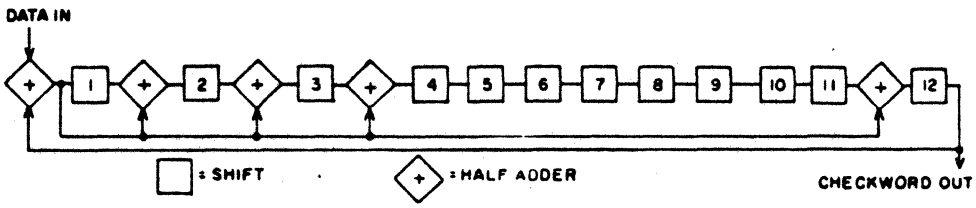


Figure 4-8. Checkword Generation

OUTPUT FROM A OPERATION

An Output from A operation is indicated by an Equipment Number match and the A/Q Write signal. The Function Code (bits Q00-Q02) specifies the operation to be performed as shown in Table 4-2.

TABLE 4-2. OUTPUT FROM A OPERATION

Function Code			Operation
Q02	Q01	Q00	
0	0	0	Load Buffer Length
0	0	1	Director Function
0	1	0	Load Address
0	1	1	Write
1	0	0	Read
1	0	1	Compare
1	1	0	Checkword Check
1	1	1	Write Address

Depending on the particular Function Code and on the state of the controller and selected drive, the operation is either executed or rejected.

In either case, 400 nanoseconds after the receipt of A/Q Write signal the A/Q Reply or Reject is transmitted.

The operation performed and the Reply and Reject conditions are as follows:

Load Buffer Length (000)

The Load Buffer Length transmits to the controller the binary value which represents the number of words to be transferred on the succeeding data transfer operation. During the execution of the OTP instruction this binary value is transmitted to the controller via the A register. If the selected drive is Ready, On Cylinder, Not Busy, and the Protect conditions are satisfied (i.e., either the selected drive is not protected or the selected drive is protected and the A/Q Protect signal is active), the controller loads the value from A into the Buffer Length Counter. On the subsequent Read, Write or Compare operation, the counter is decremented by one after each word is transmitted via the DSA. When the counter registers zero, the operation with the DSA is terminated.

Director Function (001)

The Director Function is used to select (or deselect) one of four possible disk drives and to select or clear interrupt enables. If the controller is not busy and the protect conditions are satisfied (i.e. either the

presently selected drive is Not Protected or the presently selected drive is Protected and the A/Q Protect signal is active) the controller will select the appropriate drive and establish the required interrupt conditions, as specified by the contents of the A register described in Figure 4-9.

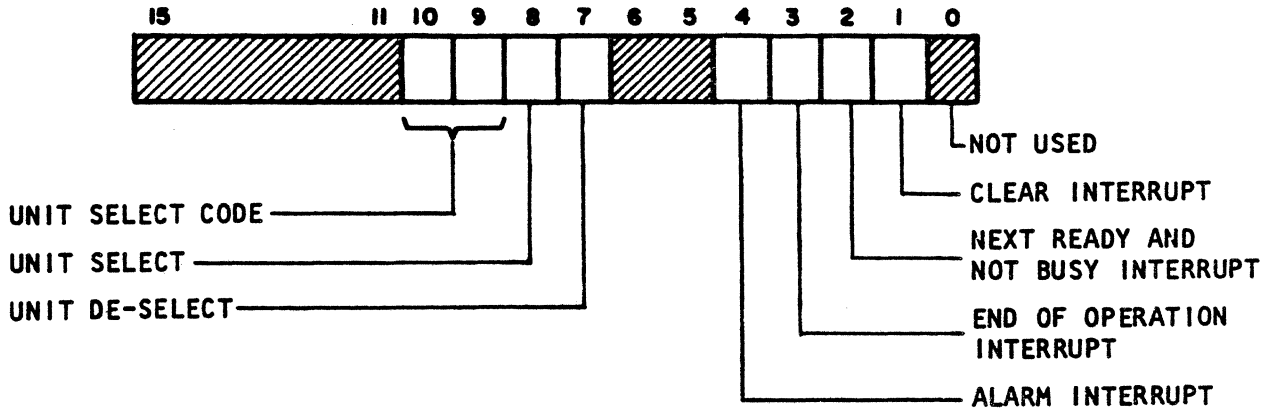


Figure 4-9. Selectable Interrupt Conditions and Unit Selection

A0 - Not Used

A1 = 1- Clear Interrupt - This bit causes all the interrupt selections to be cleared. This bit is sub-ordinate to the interrupt request

bits A02 through A04.

A2 = 1- Next Ready and Not Busy Interrupt Request - The selection of this request causes the interrupt line to become active when the controller becomes Ready and Not Busy. Note that any of the drives may be busy while seeking.

A3 = 1- End of Operation Interrupt Request - The selection of this request causes the interrupt to become active when the End of Operation Status bit is set.

A4 = 1- Alarm Interrupt Request - The selection of this request causes the interrupt line to become active when the alarm status bit is set.

A5 and A6 - Not Used

A7 = 1- Unit De-select. This bit releases the selected drive unit. It is used by a protected program to allow system control to pass to an unprotected program. The protected status is cleared by this bit. The drive remains selected.

A8 = 1- Unit Select. This bit allows the program to change the drive unit selection. The drive unit selected is determined by bits A9, A10.

A9 = 1- Unit Select Code. Least significant bit of 2 bit code.

A10 = 1-Unit Select Code. Most significant bit of 2 bit code.

Unit Select

Upon detection of a valid Director Function if A08 = 1 the controller causes the setting of the appropriate stage of the Unit Select register as specified by bits A09 and A10. If A07 = 1 the controller clear the previous unit selection. If both A07 and A08 are equal to one, the Clear takes precedence.

Director Function will be accepted if no Write, Read, Compare, Checkword Check or Write Address is in process on any unit and Protect conditions satisfied for the selected unit. If any unit is positioning, the Director Function will be accepted.

Load Address (010)

The Load Address function initiates a Seek to the File Address specified by the contents of the A register described in Table 4-3.

TABLE 4-3. LOAD ADDRESS FUNCTION

Code	Operation
A00-04	Sector Number ($0-28_{10}$)
A05	Disk Selection (Cartridge or Fixed)
A06	Surface Selection ("Top" or "Bottom")
A07-15	Cylinder Address ($0-405_{10}$ for 9427) ($0-202_{10}$ for 9425)

The Load Address function will be executed if neither the controller nor the selected unit is busy, the selected unit is Ready, On Cylinder and the Protect conditions are satisfied.

The controller checks the cylinder address and sector count to insure that the addresses are within the bounds of the selected drive. If the addresses are in order, the controller loads the contents of the A register into the Cylinder Address and Sector Count Register and Disk & Surface selection FF. In addition

the Track Address Strobe and the contents of the Cylinder Address Register are transmitted to the selected drive. Upon receipt of the strobe, the drive initiates the Seek to the required cylinder.

When the Seek is completed, the EOP status will be set if the controller is Not Busy. If the selected drive is unable to complete the seek, the Drive Seek Error status will be set.

If the cylinder address or sector count are not within the required limits, the Address Error status is set and the load of the Cylinder Address and Sector Count Register is inhibited.

Note that the A/Q Reply signal is transmitted to the channel in all cases (i.e., even if an Address Error is detected), 400 nanoseconds after the A/Q Write is detected. After transmitting the Reply, the controller is available for subsequent instructions.

The Buffer Length determines the updating of the address in the controller during the execution of a particular function such as Read or Write. The Sector is incremented after 96 words. At the end of the 29th sector the

Surface selection changes since the Cylinder consists of the upper and lower surface of either the cartridge or fixed disc. When the second track of the cylinder is filled, the head is moved to the next cylinder. The disc selection only changes with the Load Address function. As a practical example this means that a large buffer which started in the cartridge disc would not automatically be continued on the fixed disc, or vice versa.

Write (011)

The Write function transfers to the disk the number of words specified by the preceding Load Buffer Length. The starting location on the disk is that specified by the preceding Load Address function. If the transfer extends beyond a full track the heads will automatically be moved to the next cylinder. The transfer is continued until either the Buffer Length Register indicates zero, or the Cylinder Address Register is incremented beyond the last allowable address (at which point an Address Error will be indicated).

The Write function will be accepted if the controller and selected unit are not busy, the unit is Ready and On Cylinder and the protect conditions are satisfied. Upon receipt of the Write function the Write FF is set, the A/Q Reply transmitted and the Controller Busy FF set. Thereafter, the operation proceeds as in the Read function (See Read section) until the required sector is found and the SFC advanced to the 010 state.

At the beginning of the 010 field the FLC is reset to zero. At count 120 the Write Gate is set, thereby causing the Sync area composed of the Write Clock ("1" pulse every T_1) and a Data bit stream of zeros ("0" pulse every T_3) to be written on the disk. In addition, at count 120 the Need FF is set and the first two words of data to be written on the disk are read from memory via the DSA. At count 232, a "1" bit (the Sync Bit) is written on the disk and the SFC is advanced to 011, the data area.

If during the Write operation the Bit Counter indicates that a new word is required by the Shifter, but the Buffer 2 is empty, the Lost Data status is set. The operation is terminated after the end of the sector in which the Lost Data condition was detected.

Upon termination of the Write operation the contents of the various status words will be as described for a Read operation.

Read (100)

The Read function transfers to the memory the number of words specified by the preceding Load Buffer Length function. The starting location on the disk is that specified by the preceding Load Address function. If the transfer extends beyond a full track, the heads will automatically be switched to the second surface of the same (Cartridge or Fixed) disk. If the heads already reside on the second surface, they will automatically be moved to the next cylinder. The transfer is continued until either the Buffer Length Register indicates zero, or the Cylinder Address Register is incremented beyond the last allowable address (at

which point an Address Error will be indicated).

The Read function will be accepted if the controller and selected unit are Not Busy, the unit is Ready and On Cylinder and Protect conditions are satisfied. Upon receipt of the Read function, the Read FF is set, and A/Q Reply transmitted and the Controller Busy FF is set. Upon detection of the next Sector Mark, the Sector Field Counter (SFC) is set to field 000_2. In the middle of the Sync pattern the Read Gate is activated and the "one" at bit 112 is searched for. When the "one" bit is detected the SFC is advanced to 001_2 and the upper 12 bits of the File Address are loaded into the shifter. (See Figure 4-10). The address bits shifted from bit 11 of the shifter are compared bit by bit with the address read from the disk.

If all pairs of bits match, the lower 12 bits of the File Address are loaded into the shifter and similarly compared with the address read from the disk. If a mismatch is detected in either the upper or lower 12 bits, the Address

No Compare FF is set, the SFC is set to an unused state (Idle), and the operation halts until the next Sector Mark is detected. The File Address is again compared with the address read from the disk. This comparison is repeated until a sector is found in which all 24 bits of the File Address match. At this point the SFC is advanced to 010_2 and the processing of the sector continues.

In the middle of the Sync pattern (count 176 from beginning) in the 010 field the search is begun for the "one" bit. Upon detection of the one bit the SFC is advanced to 011_2 and the reading of the data is started.

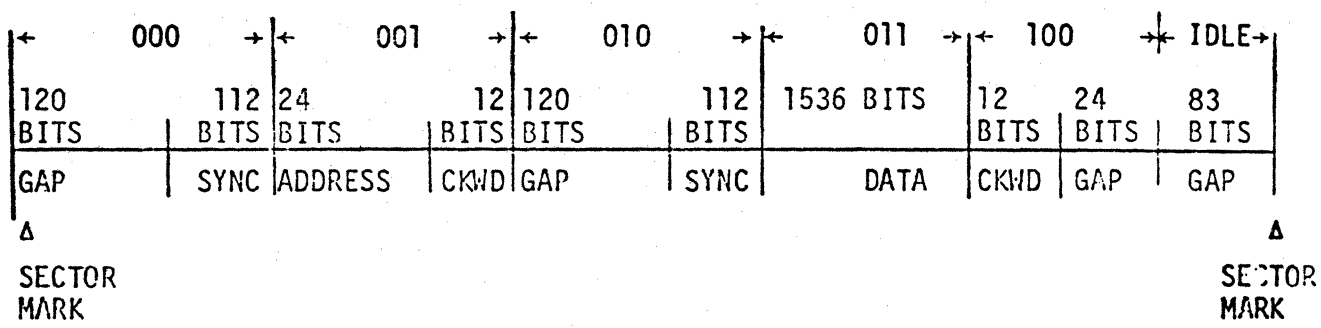


Figure 4-10. Sector Fields

At the beginning of the 011 (data) field, the Field Length Counter (FLC) and the Bit Counter are reset to zero. Thereafter the Bit Counter is incremented by one for every serial data bit transferred from the disk to the Shifter. The FLC is incremented once for every group of sixteen bits (i.e., for every word).

When the Bit Counter indicates that a 16 bit word has been assembled in the Shifter, the word is transferred to Buffer 1. If Buffer 2 is empty, the word is immediately transferred to Buffer 2 and the Need FF is set. The setting of the Need FF enables the Scanner to be captured, the Storage Request signal to be activated and the storage address to be transferred from the Current Word Address Register to the DSA. Upon receipt of the Storage Resume signal, the data is transferred from Buffer 2 to the memory location as specified by the Current Word Address.

If Buffer 2 already contains a word, the new word will remain in Buffer 1 until Buffer 2 is emptied. During the time that this word remains in either buffer, serial data is continually read from the disk to the Shifter.

The serial to parallel assembly and transfer to the DSA continues until the FLC is incremented to 96_{10}, indicating the end of the Data Field (011) of this sector. At the end of the data field, the SFC is advanced to 100 and the contents of the checkword circuit are loaded into the Checkword Status Register. Thus, the contents of the register indicate the actual checkword that was computed from the serial data read from this sector. After the Checkword Status Register is loaded the 12 bit data checkword is read serially from the disk, and inserted into the Checkword circuit. After the entire 12 bits are inserted, the Checkword circuit is inspected for a non-zero content which indicates a Checkword Error. If a Checkword Error occurs the entire Read operation is terminated regardless of the contents of the Buffer Length Register. If no Checkword

Error is indicated the SFC is set to the Idle state and the next sector is awaited. Upon detection of the next Sector Mark, the SFC is set to 000_2 and the processing (Address Comparison, Data Read, Checkword Check) of this sector is started.

Thereafter, each sector is processed in turn until the Buffer Length Counter is finally decremented to zero. At this point data transfer to the memory is halted, but the data is continued to be read from the disk until the end of the current sector. At the end of the current sector, the Checkword is checked and the File Address (Cylinder Address Register, Surface Selection FF and Sector Counter) is incremented to indicate the address of the sector following the last (partial or complete) sector read.

If during the Read operation the Bit Counter indicates that a new word has been assembled, but Buffer 1 is still full, the Lost Data status is set. The operation is terminated after the end of the sector in which the Lost Data condition was detected.

Upon termination (normal or abnormal) of the Read operation the Director Status will indicate End of Operation (EOP), Ready, On Cylinder and possibly other status. The Current Word Address status will indicate one more than the last memory location written into. The True Cylinder Address status will indicate the Cylinder Address that was transferred serially from the disk during the last sector that was read.

Compare (101)

The Compare function causes the disk controller to compare data read via the DSA from the memory with data read from the disk. The number of words to be compared is specified by a preceding Load Buffer Length function. The starting location on the disk is specified by the preceding Load Address function. As in the Read and Write functions, the heads will automatically be advanced until the number of words specified by the Buffer Length have been compared.

With respect to the transfer of serial data from the disk, the Compare function operates identically with the Read function. With respect to the transfer of parallel data from the memory the Compare function operates identically with the Write function The actual data processing is done serially with a bit-by-bit comparison between the data read from the disk and the data read from the memory and converted to serial form by the Shifter. Upon detection of the first mismatch, the Compare Error status is set. However, the comparison operation continues to the end of the buffer specified.

Checkword Check (110)

The Checkword Check function reads the data and checks the checkword of the entire track (29 sectors) as specified by the preceding Load Address function. No data is transferred between the DSA and the CDD controller.

At the beginning of the 011 field the contents of Buffer 2 are loaded into the Shifter, and the FLC and the Bit Counter are reset to zero. Thereafter the Bit Counter is incremented by one for every serial data bit transferred from the Shifter to the disk. The FLC is incremented by one for every group of sixteen bits (word) tranferred.

When the contents of Buffer 2 are transferred to the Shifter, the contents of Buffer 1 are transferred to Buffer 2 and the Need FF is set to initiate a DSA request for the third word. Thereafter, a Request is generated for every word transferred from Buffer 1 to Buffer 2 until the FLC indicates that 94_{10} words have been transferred. At this point the Inhibit Need FF is set and no further DSA requests are made for this sector.

As the serial data is transferred to the disk, it is also inserted into the Checkword circuit. After the last two words of the sector are written, the FLC indicates 96_{10} and the contents of the Checkword circuit are loaded into the Checkword register. The contents of this

register is the actual Checkword that was computed from the serial data written in this sector. Also at count 96_{10}, the SFC is advanced to the 100_2 state and the 12 bit Checkword is transferred from the Checkword circuit to the disk. At count 15 the Write Gate is reset. At count 36 the SFC is set to the Od;e Idle state to await the next Sector Mark.

Each sector is similarly processed until the Buffer Length Counter is finally decremented to zero. At this point the controller ceases requests for DSA Data but continues writing zero data on the disk until the end of the current sector. At the end of this sector the File Address is incremented to indicate the address of the sector following the last (partial or complete) sector written.

With respect to the transfer of data from the disk, the Checkword Check function is identical with the Read function. However, no data is transferred from the Shifter to the Word Buffers. If a Checkword Error is detected the operation is terminated with the File Address indicating the sector following the one in

which the error was detected.

Write Address (111)

The Write Address function causes the addresses to be written on the 29 sectors of the track specified by the contents of the Cylinder Address Register.

The Write Address function will be executed if the controller and previously selected unit are Not Busy and the selected unit is Ready, On Cylinder, and Protect conditions are satisfied.

Upon detections of the Write Address (WA) function, the WA FF is set and the A/Q Reply is transmitted to the channel, and the Controller Busy is set. When the Index Mark is next detected by the controller, the writing of the address field in the first sector is begun.

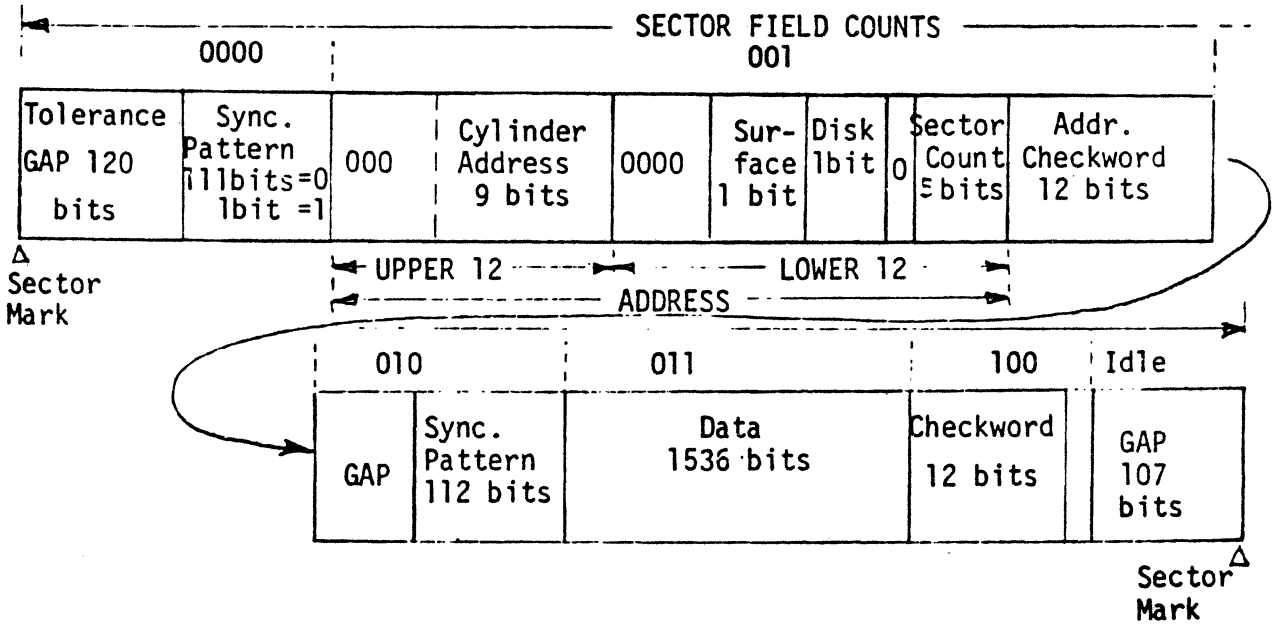


Figure 4-11. Sector Fields

Each sector is divided into fields as shown in Figure 4-11. The Sector Field Counter indicates which field is being operated on at the given time. The Write Address function Write fields 000 and 001 of each sector. The Tolerance Gap is created by counting 120 bits (with the Field Length Counter) after the Index Mark. The Sync Pattern is then written with the first 111 bits equal to zero and the 112th bit equal to one. At the beginning of the 001 field, the contents of the Cylinder Address Register are loaded into the 16-bit Shifter in the format shown in Figure 4-12.

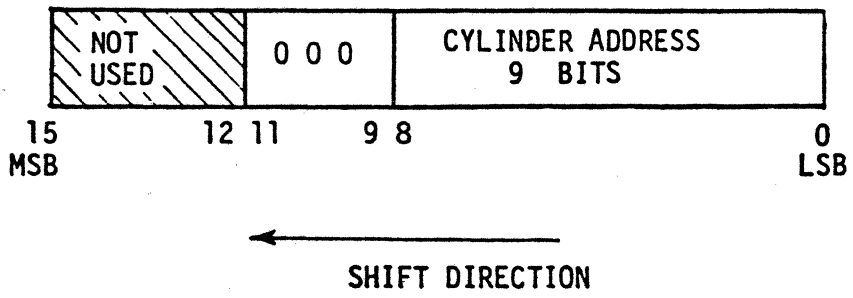


Figure 4-12. Upper 12 Address Bits

The contents of the Shifter bit 11 are written in serial form on the disk. After the upper 12 bits of the address are written, the contents of the Sector Count Register and Surface and Disk selection FF's are loaded into the shifter in the Format shown in Figure 4-13.

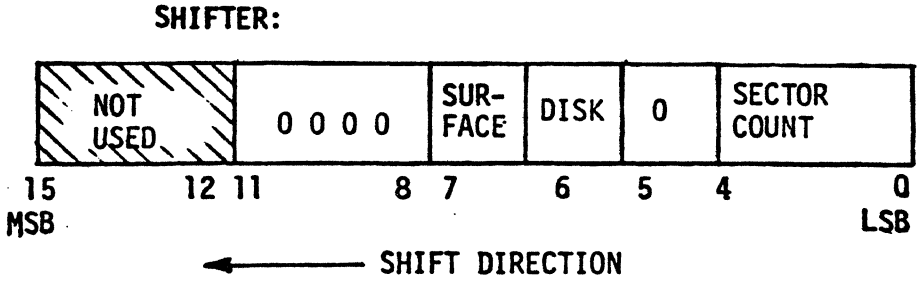


Figure 4-13. Lower 12 Address Bits

Thereupon, the lower 12 bits of the address are shifted to the disk from the Shifter bit 11.

As the Address bits are transferred to the disk the Address Checkword is computed in the Checkword Register. After the last bit of the address is written the 12 bits of the Checkword are transferred serially to the disk.

At the completion of field 001 the contents of the Sector Count Register are incremented by one. Thereupon, the operation awaits the beginning of the next sector (i.e., the next Sector Mark). The operation is repeated in the second and all succeeding sectors until the Sector Count is advanced to 29_{10}. At that point the operation is halted, the Controller Busy status is cleared and the EOP is set.

Autoload

The depression of the remote AUTOLOAD switch on the programmer's console causes the CDD controller to transfer one complete track of data from cylinder zero, surface zero, disk zero (i.e., Cartridge or Fixed depending on the state of the Head 0 Selection jumper) of unit zero, to the computer memory starting at location zero. Upon receipt of the Remote Autoload signal, the controller selects unit 0, issues an RTZS, and clears to zero the Cylinder Address Register, Sector Count Register, Surface and Disk Selection FF's and CWA Register. When the RTZS is completed, the drive returns the On Cylinder signal.

Thereafter, upon detection of the Index Mark, the controller initiates a Read operation starting at sector zero. The Read continues until all 29 sectors have been transferred, at which point the Autoload is terminated.

INPUT TO A OPERATION

An Input to A operation is indicated by an Equipment Number match and the A/Q Read signal. The Function Code (bits Q0-Q2) specifies the operation to be performed as shown in Table 4-4.

TABLE 4-4. INPUT TO A OPERATION

Function Code			Operation
Q02	Q01	Q00	
0	0	0	Clear Controller
0	0	1	Director Status
0	1	0	Cylinder Address Status
0	1	1	Current Word Address Status
1	0	0	Checkword Status
1	0	1	Drive Cylinder Status
1	1	0	Illegal
1	1	1	Illegal

If the operation specified is not illegal, it is executed immediately. That is, in the case of the status reads, the appropriate status is transmitted to the A register. In the case of the Clear Controller, a Return to Zero Seek (RTZS) is transmitted to the selected unit and the controller is set to an idle state (except for the A/Q Interface control logic). 400 nanoseconds after the receipt of the A/Q Read signal, the A/Q Reply signal is transmitted to the channel. When the A/Q Read goes inactive, the controller drops the A/Q Reply and ends the operation by either closing the gates to the A register or terminating the Clear signal.

If an illegal Function Code had been specified the controller takes no action other then transmitting the A/Q Reject signal instead of the A/Q Reply.

Description of Input to A Functions

A Read signal from the computer AQ channel defines the contents of A as an Input. The significance of the contents of A varies with the value in bits 00-02 of the Q register.

Clear Controller (000)

This function will clear the controller unconditionally and will generate a Return to Zero Seek (RTZS) to the selected drive. This function must be used with discretion since a Clear Controller signal will stop any current operation. RTZS signal is issued, Busy is not set. Unit Select is not cleared. If the controller is not busy at the end of the RTZS, End of Operation will be set.

Director Status (001)

This function is used to monitor the controller's operating status. The status information is loaded into the A register as shown in Figure 4-14.

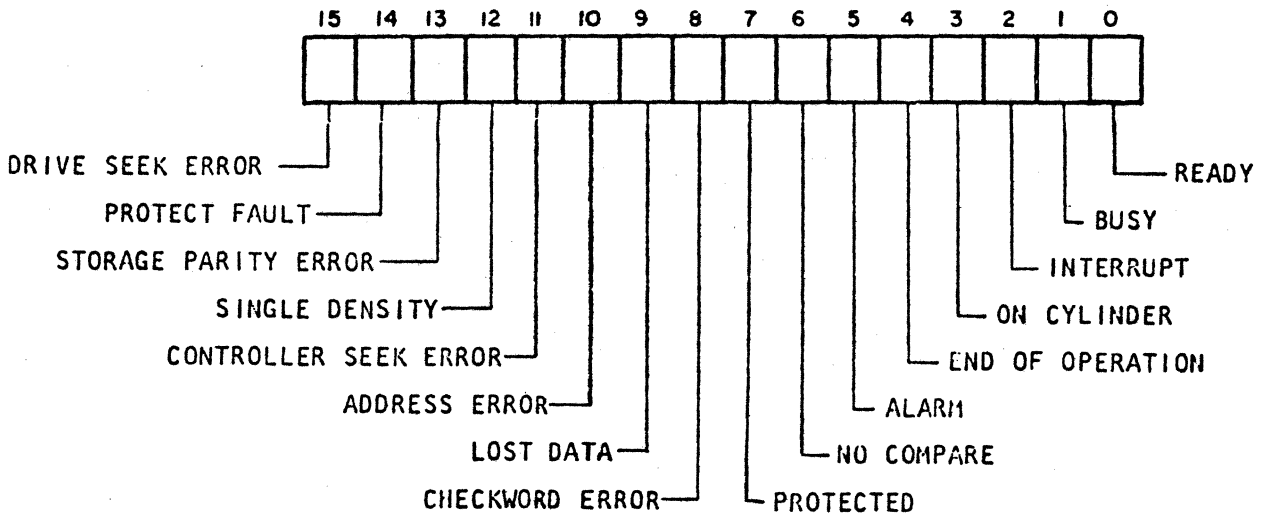


Figure 4-14. Director Status Format

The controller will accept this function at any time. The acceptance of this function causes no changes in the status of the controller.

The controller status is indicated by the presence of a one or zero bit in each of the A register bit positions. The conditions associated with each bit position is given above.

Ready (A0=1) - This bit indicates that the selected drive is available and ready to operate. The drive becomes Not Ready for the following reasons:

a. Disk Pack not in drive unit.
b. Disk drive motor not up to operating speed.
c. Read/Write heads not in operating position.
d. A fault condition develops in the selected drive.

This status condition will be affected by the operating program only if it selects a device physically not in the system or a device which is Not Ready.

Normally, the absence of this status bit indicates that manual (operator) intervention is required at the selected drive unit.

Busy (A1=1) - This bit indicates that the controller is presently involved in an operation.

This bit is set by the acceptance of a Write, Read, Compare, Checkword Check, or Write

Address function.

This bit will be cleared when the controller has completed its operation or an abnormal condition is detected which aborts the operation. Once initiated, the computer cannot clear the Busy condition except by a Clear Controller instruction.

Interrupt (A2=1) - This bit indicates that the selected interrupt condition has occurred. The bit will be cleared by the acceptance of any Output from A function.

On Cylinder (A3=1) - This bit will be set when the drive positioner of the selected unit is On Cylinder. It will be cleared if the drive unit is presently positioning or if a Seek Error is detected and the heads have not yet returned to cylinder zero.

End of Operation (A4=1) - This bit will be set whenever the controller portion of an operation is complete, or if any of the four units completes a seek and 30-50 Nsec after Busy status deactivates.

This bit will be cleared by an Output from A function.

Alarm (A5=1) - This bit indicates that one of the following abnormal conditions has occurred:

a. Not Ready and Busy (Alarm set immediately).

b. Checkword Error (Alarm sets at EOP).

c. Lost Data (Alarm sets at EOP).

d. Controller Seek Error (Alarm sets immediately).

e. Address Error (Alarm sets immediately).

f. Drive Seek Error (Alarm sets immediately).

g. Storage Parity Error (Alarm sets at EOP).

h. Protect Fault (Alarm sets at EOP).

Certain fault conditions in the Cartridge Disk Drive described in Section 1 of this manual will generate a DISK FAULT signal. The Alarm interrupt will be triggered. No status bits are available to sense these faults originating in the CDD. If the software tests of the available status bits do not indicate an abnormal condition, the CDD must be investigated. An illuminated FAULT switch on the CDD will

give a general indication. Additional LED indicators on the PWB inside the cabinet can be consulted for specific faults.

This bit will be cleared by any Output from A function. The Not Ready condition can be changed by manual intervention.

No Compare (A6=1) - This bit indicates that the data received from computer storage does not compare with data read from the file storage during a compare operation. This bit is cleared by any Output from A function.

Protected (A7=1) - This bit is present when the selected unit's PROTECT switch is on. (Allows only programs from the protected area of computer storage to have access to the drive.)

Checkword Error (A8=1) - This status bit indicates that the controller logic has detected an incorrect checkword in data read from file storage during a Read, Compare, or Checkword Check operation. This bit is cleared by any Output from A function.

Lost Data (A9=1) - This bit indicates that the computer's DSA bus has not been able to keep up to the file data transfer rate during a Write, Read, or Compare operation. This bit is cleared by any Output from A function.

Address Error (A10=1) - This bit indicates that the controller has detected a file address which is beyond the limits of the file storage capacity received from the computer or that the controller has advanced the file address beyond the limits of the file storage capacity. This bit is cleared by any Output from A function, accepted by controller.

The contents of the Cylinder Address register are not altered if the error is detected during a Load Address instruction. If the error is detected during a Read, Write or Compare operation, the heads will be advanced one track beyond the limit (that is, track 405 of the 856-4 CDD or track 203 of the 856-2 CDD). Note, if the last sector in the last cylinder is addressed during a Read, Write or Compare operation, an Address Error will be indicated

after the last sector has been read, written or compared.

Controller Seek Error (A11=1) - This bit indicates that the controller has been unable to obtain the file address selected during a Write, Read, Compare or Checkword Check operation. This error usually indicates a positioning error, dirty heads, or defective cartridge disk. The positioning error can be corrected by doing a status check of the drive cylinder, comparing this with the contents of the Cylinder Address register (to determine if, indeed, a positioning error has occurred). This bit will be cleared by any Output from A function accepted by the controller.

Single Density (A12=1) - When "one" this bit indicates that the selected drive is type 856-2. When zero the selected drive is type 856-4.

Storage Parity Error (A13=1) - This bit indicates that the controller has received a Parity Error signal from the DSA bus during a Controller-DSA transfer. The operation will end at the end of the sector being operated on. This bit will be cleared by any Output from A function.

Protect Fault (A14=1) - This bit indicates that an unprotected Read instruction initiated an operation to write in a protected computer storage area. The operation will end at the end of the sector being operated on. The protected computer storage area is not changed. This bit will be cleared by any Output from A function.

Drive Seek Error (A15=1) - This bit indicates that the drive unit has detected that the cylinder positioner has moved beyond the legal limits of the file storage area (below zero cylinder position 0 or above cylinder position 202 or 405) during a Write, Read or Compare function. This bit will be cleared by any Output from A function accepted by the controller.

Cylinder Address Status (010)

This function is used to monitor the file address, which is the address of the sector, track, and cylinder of selected unit being operated in when the controller is Busy. When the controller is Not Busy, it represents the address of the sector last processed plus one. See Figure 4-15. The address information is loaded into the A register and is arranged in the same format used by the computer to transfer the file address to the controller. This function will be accepted at any time by the controller.

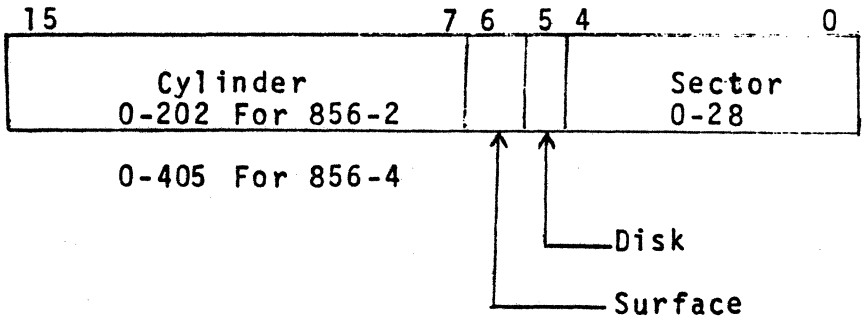


Figure 4-15. Cylinder Address Status Format

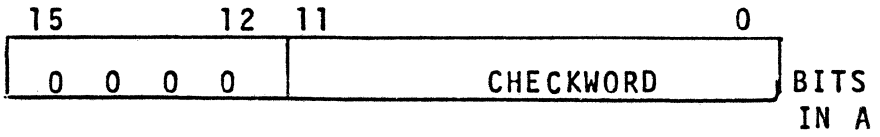
Current Word Address Status (011)

This function is used to monitor the Current Word Address (CWA) register. The contents of the CWA register are loaded into the A register. This provides the computer with information as to the area in storage being transferred, or the location of the area already transferred in a previous DSA operation, such as Read, Write or Compare. This function will be accepted unconditionally at any time by the controller.

Checkword Status (100)

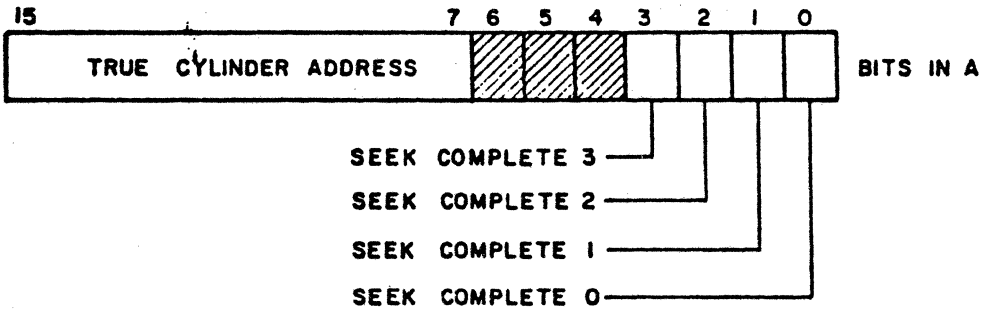
The Checkword Status is used to monitor the contents of the Checkword 2 register This register holds the Data Checkword on the last sector operated on.

The Checkword Status function will be accepted unconditionally at any time by the controller.



Drive Cylinder Status (101)

The Drive Cylinder Status is used to monitor the true cylinder address Read from the disk on the previous Read, Write, or Compare operation. This status word contains the cylinder address in bits 7 through 15. Bits 4 - 6 are unused. Bits 0-3, Seek Complete or Seek Error.



Four bits contain signals to indicate after EOP status is true, that the corresponding unit has completed a seek (Seek Complete) or is unable to complete a seek (Seek Error). These bits are available without the unit being selected. The Seek Complete is cleared by a new Load Address, Write, Read, Compare or Checkword Check Command issued to the particular unit. If a Seek Error occurred, bit

15 in the Director Status word is set if corresponding unit is selected, it must be cleared by Clear Controller (i.e., RTZS to selected unit).

Protect

The interaction between the computer and the peripheral controller can become somewhat complex when either or both are in a protected condition. For this reason Table 4-5 should be consulted.

The first column deals with a 1784 computer in which the Protect Switch is in the "off" position. In the second and third column the 1784 computer is assumed to have the Protect Switch in the "on" position. The 1733-2 Controller can be either protected (jumper plug removed on the Daisy Chain PWB) or unprotected.

Of particular interest is the condition where the 1733-2 is trying to read data from the CDD and writing into a protected memory area of the 1784. This generates a protect fault in the 1784 which is transmitted to the 1733-2 to

set the Alarm interrupt. The 1784 will not generate an internal interrupt under this condition.

The Write Protect feature of the CDD can be considered another Protect feature in the system. When the switch on the CDD is activated, it prevents the writing of data. There is no status indication in the controller to indicate that Write Protect has been activated. Should the controller execute a Write function it will run to completion in a normal manner. A Compare function must be used to detect that the data formerly recorded on the disk has not been altered.

TABLE 4-5

CONTROL DATA SYSTEM 17 CR PROTECT SCHEME

		1784 Protect Switch Set 1733-2 Controller		
		1784 Protected	Protected	Protected
	Protected Output	Reply	Reply	Reply
	Protected Input	Reply	Reply	Reply
A/Q I/O	Protected Output	Reply	Reply	Reject
	Protected Input	Reply	Reply	Reply
DSA I/O	WRITE-PROT.BUFFER Protected Out	Write	Write	Write
	WRITE-PROT.BUFFER Protected Out	Write	Write	Reject
	READ-PROT.BUFFER Protected Out	Read	Read	Read
	READ-PROT.BUFFER Protected Out	Read	Protect Fault *	Reject
	WRITE-UNPROT.BUFFER Protect Out	Write	Write	Write
	WRITE-UNPROT.BUFFER Protect Out	Write	Write	Write
	READ-UNPROT.BUFFER Protect Out	Read	Read	Read
	READ-UNPROT.BUFFER Protect Out	Read	Read	Reject

* Does not generate interrupt in 1784.

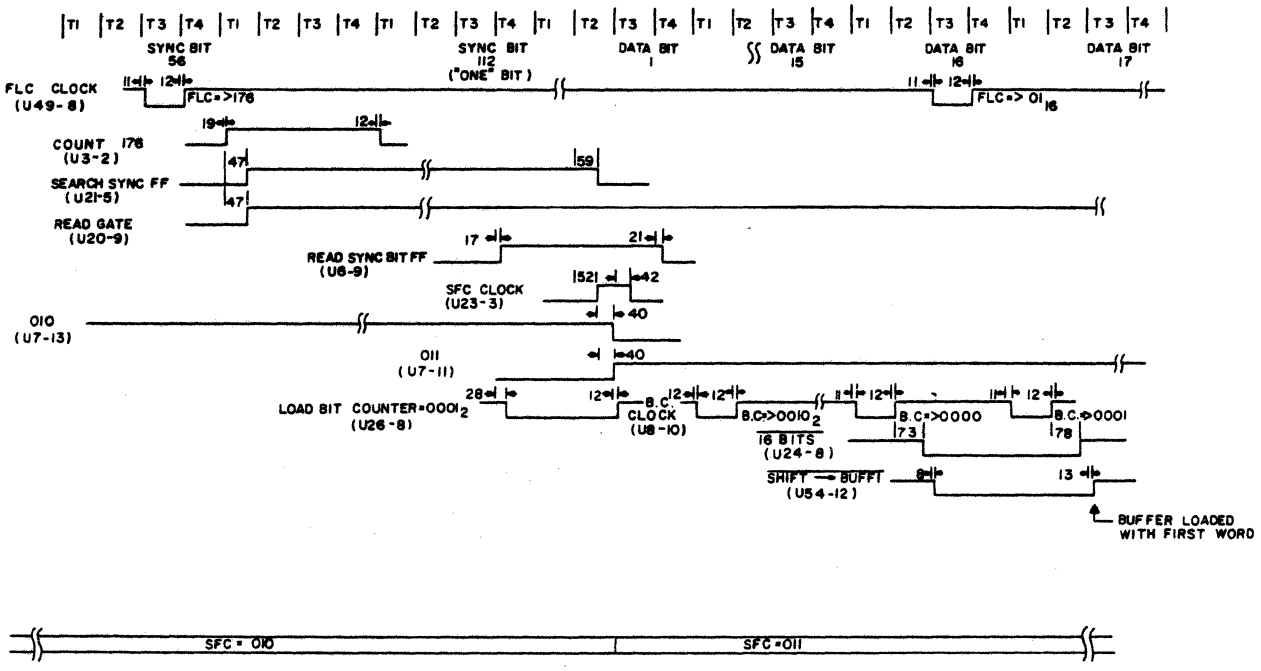


Figure 4-16 (a). Read and Checkword Timing

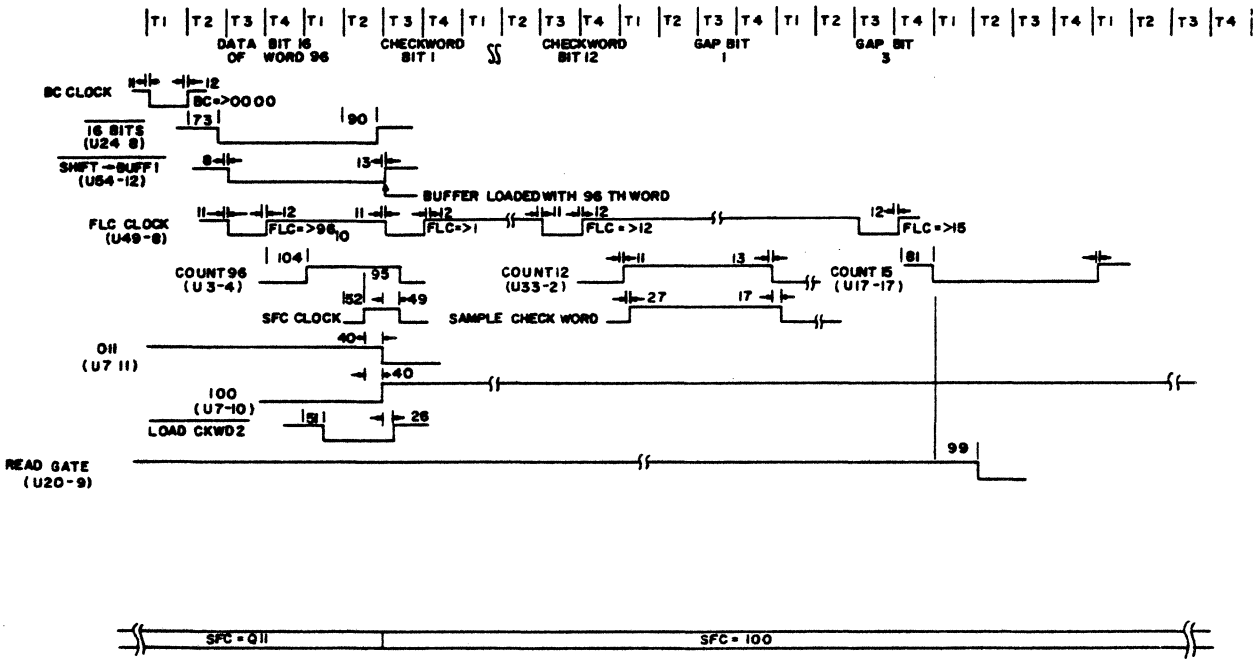


Figure 4-16 (b). Read and Checkword Timing

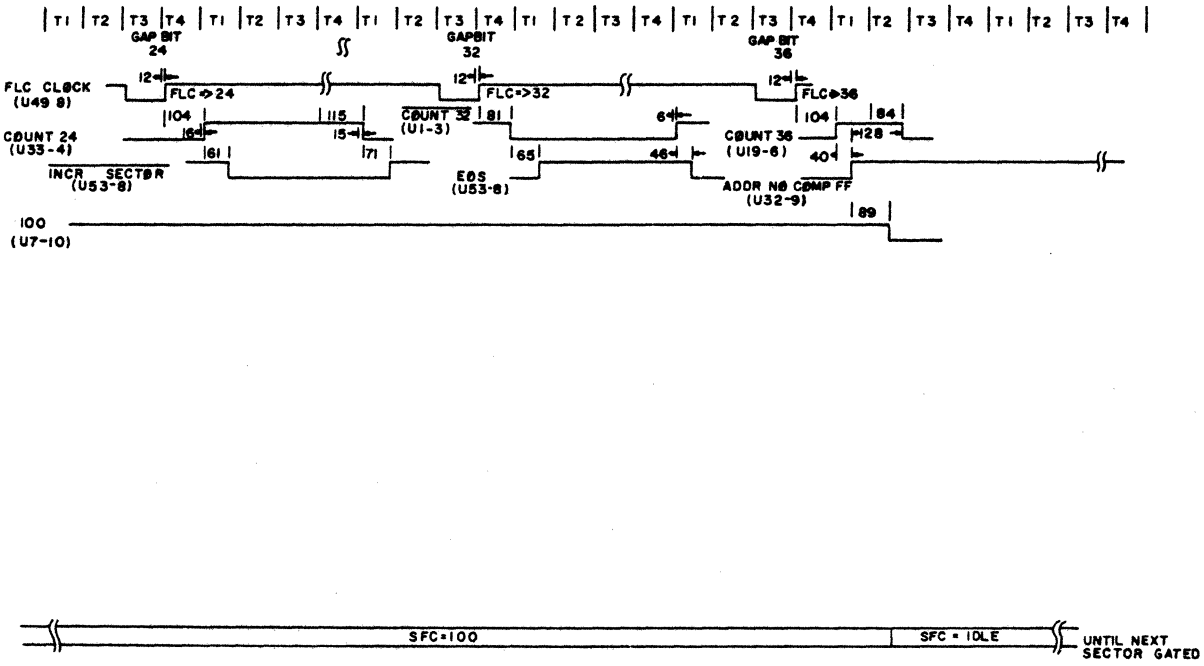


Figure 4-16 (c). Read and Checkword Timing

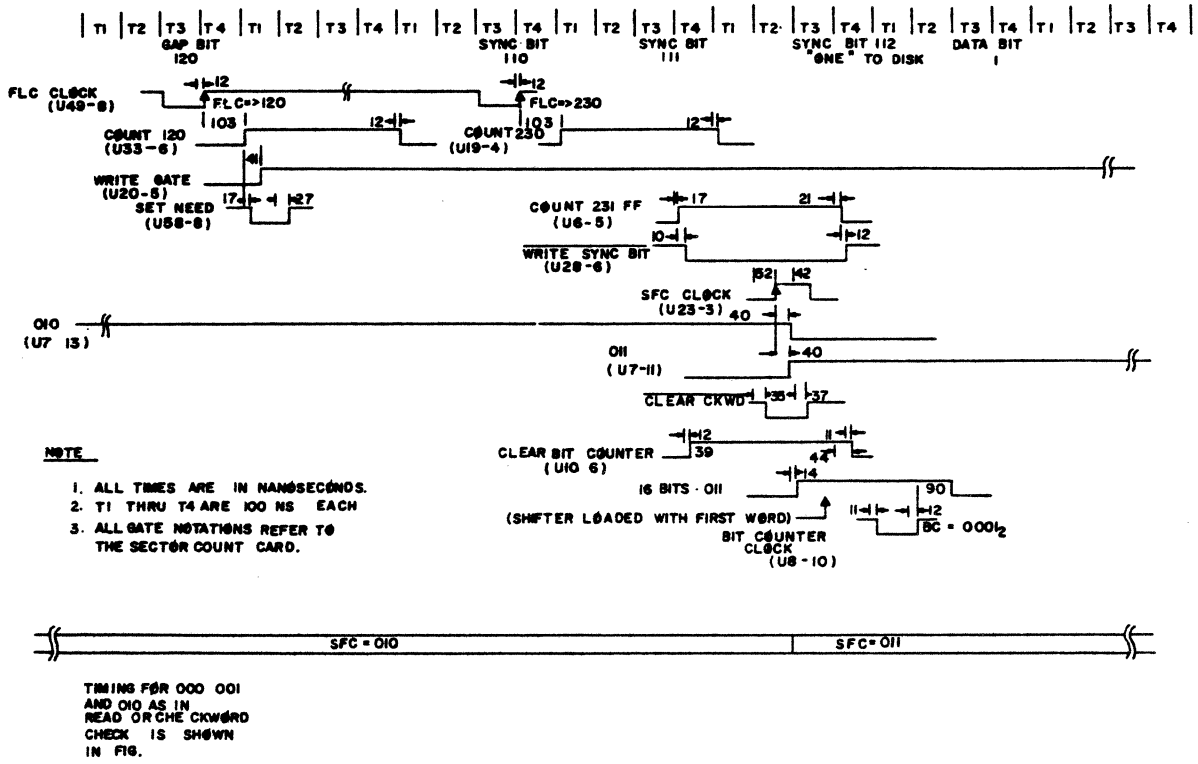


Figure 4-17 (a). Write Timing

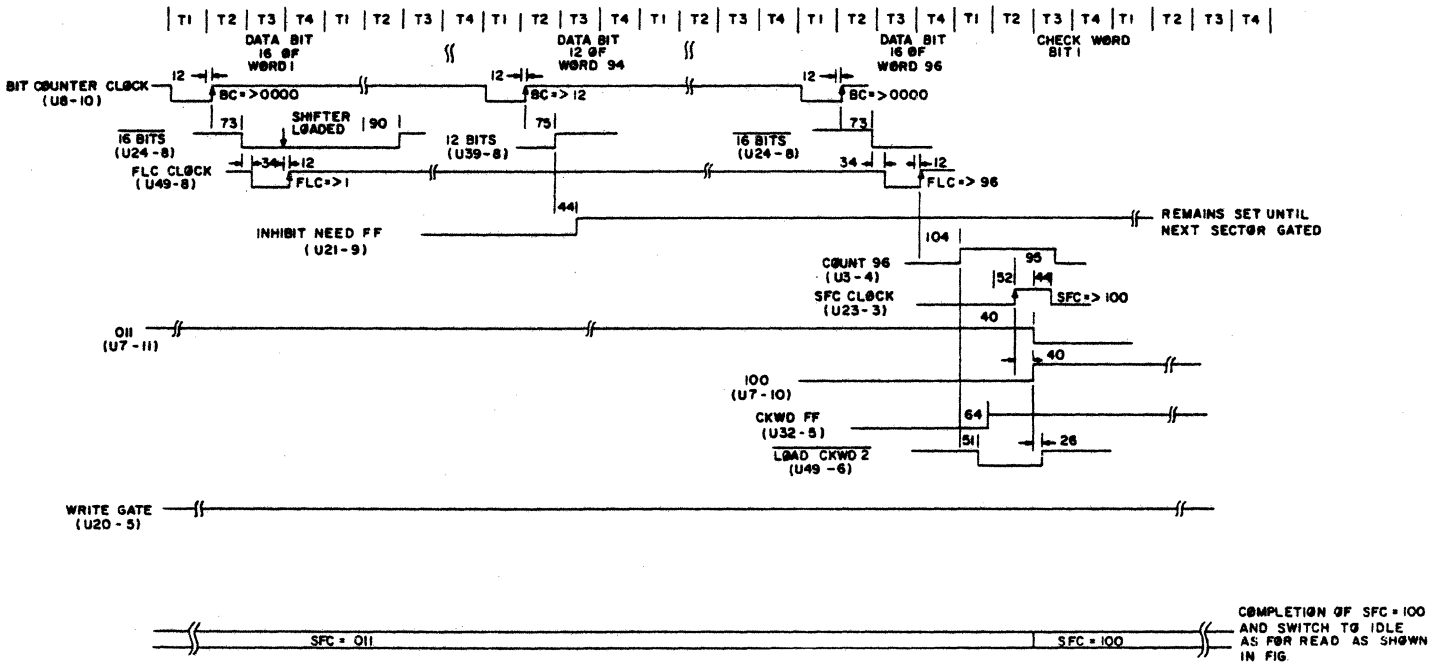


Figure 4-17 (b). Write Timing

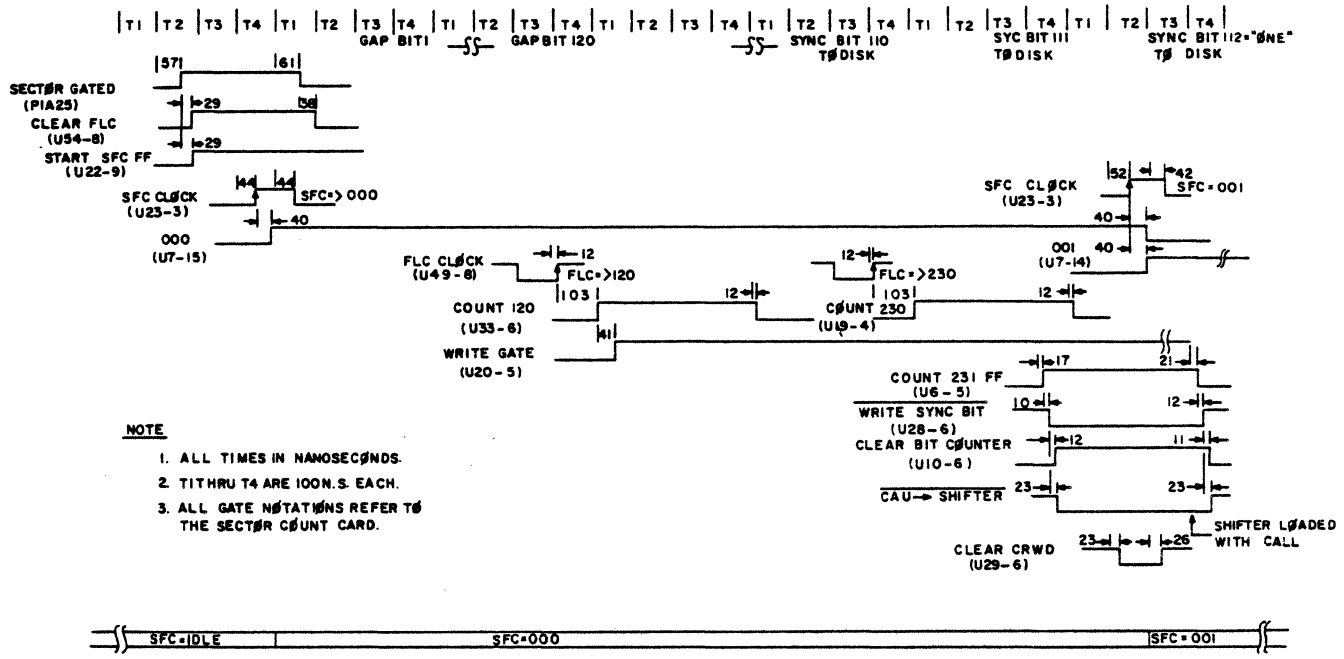


Figure 4-18 (a). Write Address Timing

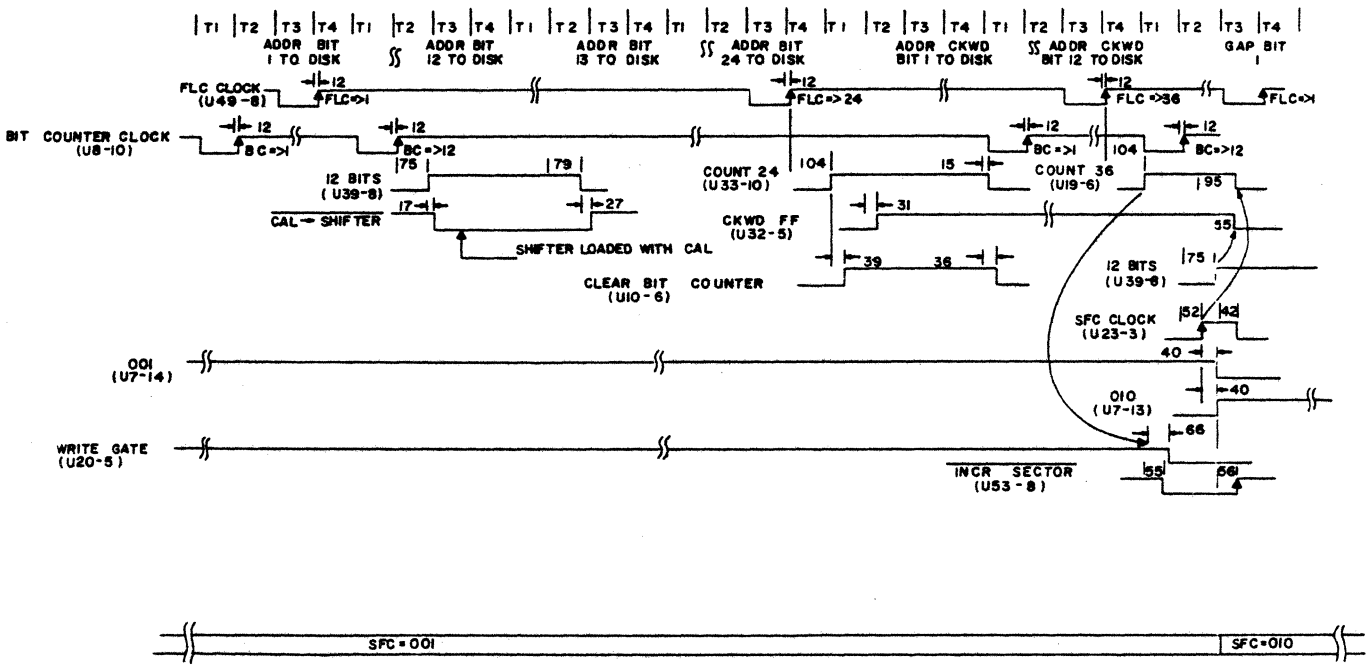


Figure 4-18 (b). Wrtte Address Timing

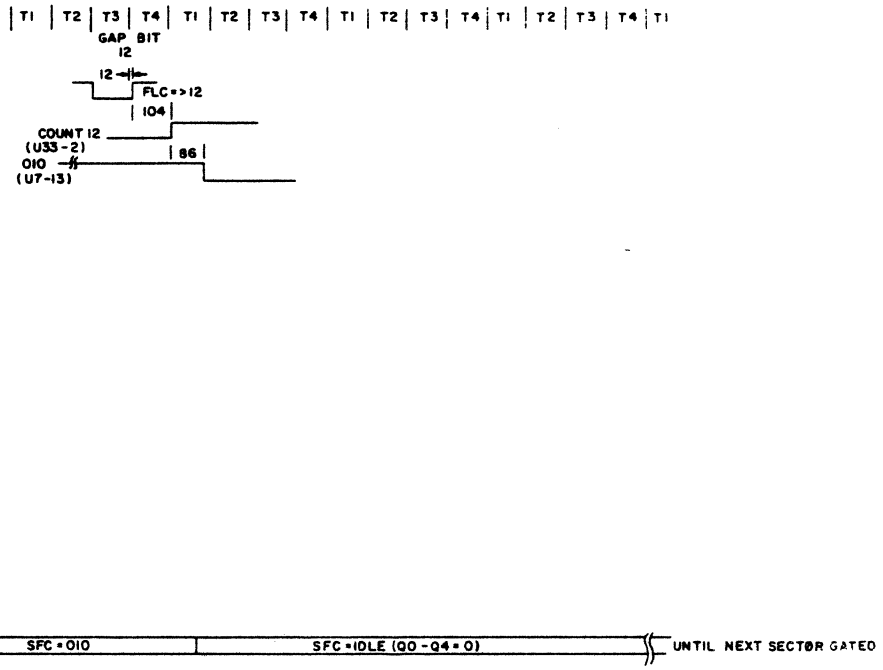


Figure 4-18 (c). Write Address Timing

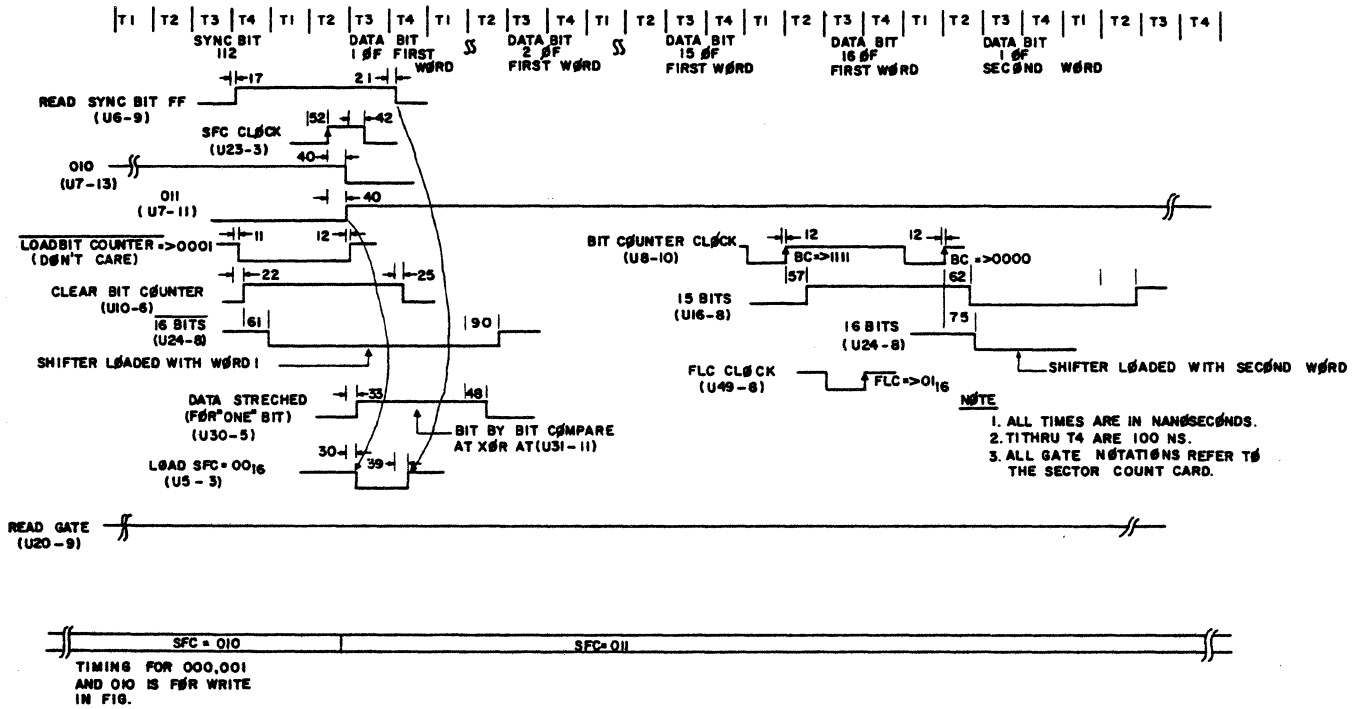


Figure 4-19 (a). Compare Timing

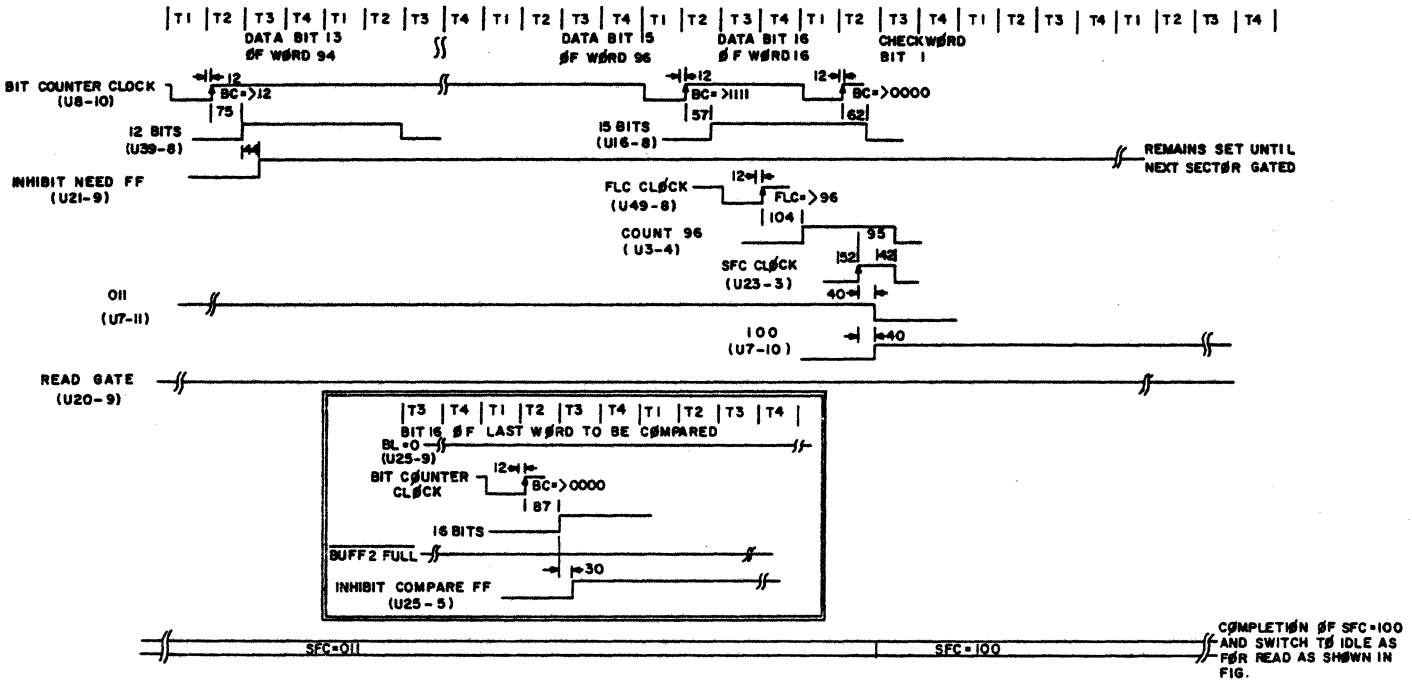
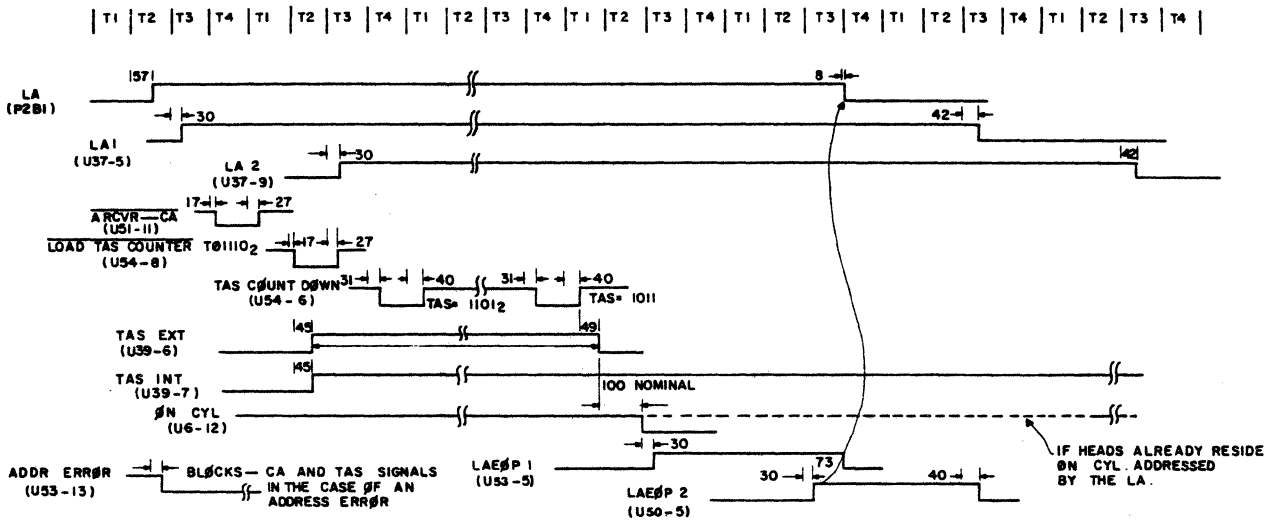


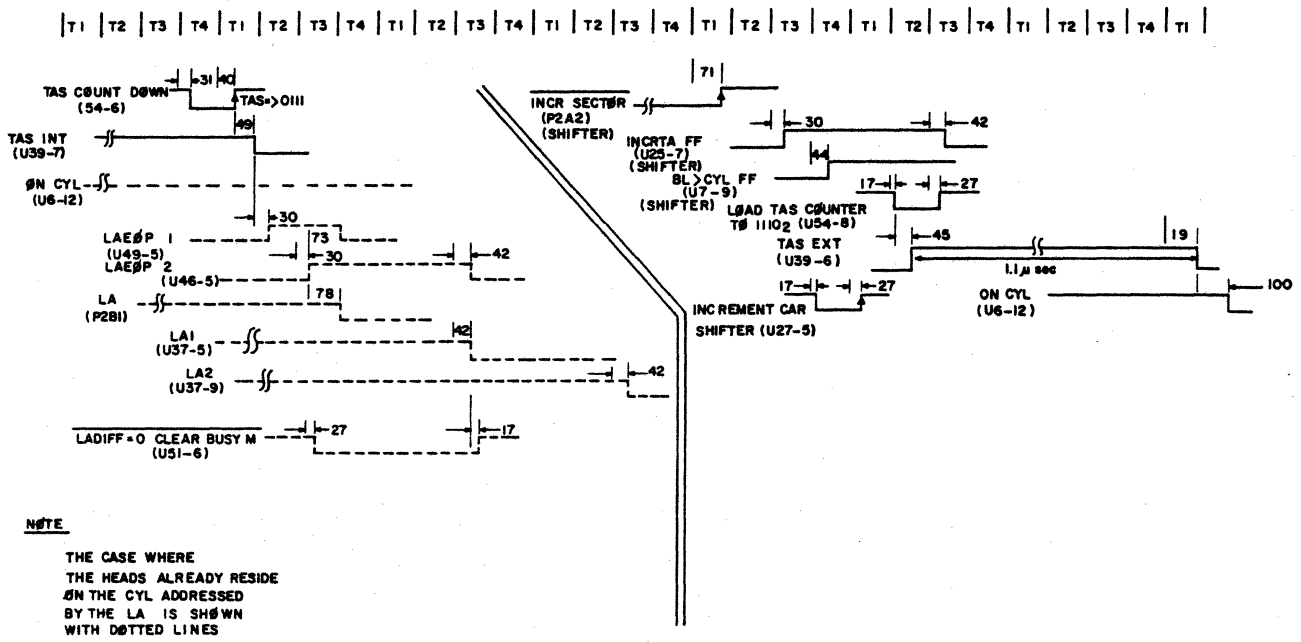
Figure 4-19 (b). Compare Timing



NØTE

1. ALL TIMES ARE IN NANØSECØNDS EXCEPT WHERE NØTED.
2. T1 THRU T4 ARE 100 NS. EACH
3. ALL GATE NOTATIONS REFER TØ THE DSA CARD

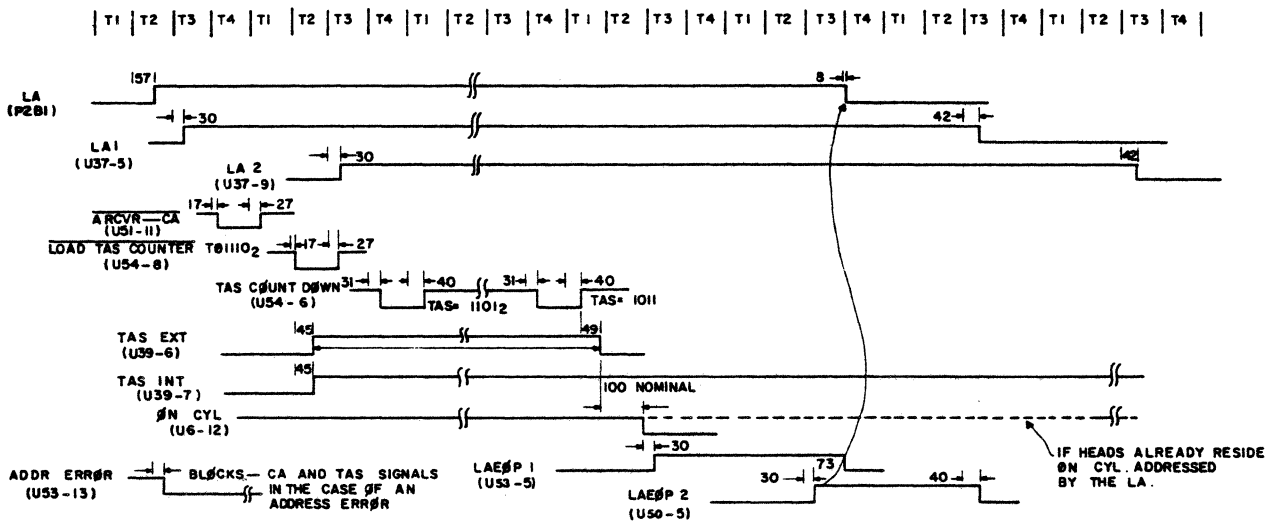
Figure 4-20 (a). Load Address Timing



NØTE

THE CASE WHERE THE HEADS ALREADY RESIDE ØN THE CYL ADDRESSED BY THE LA IS SHØWN WITH DØTTED LINES

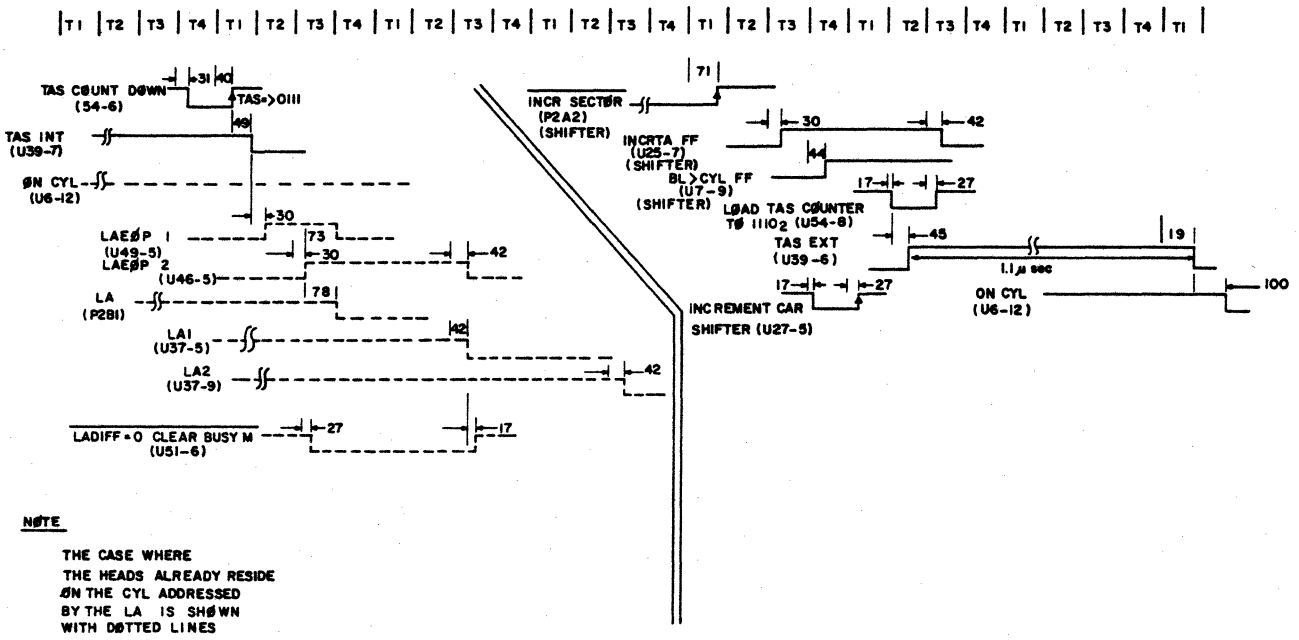
Figure 4-20 (b). Load Address Timing



NØTE

1. ALL TIMES ARE IN NANØSECØNDS EXCEPT WHERE NØTED.
2. T1 THRU T4 ARE 100 NS. EACH
3. ALL GATE NOTATIONS REFER TØ THE DSA CARD

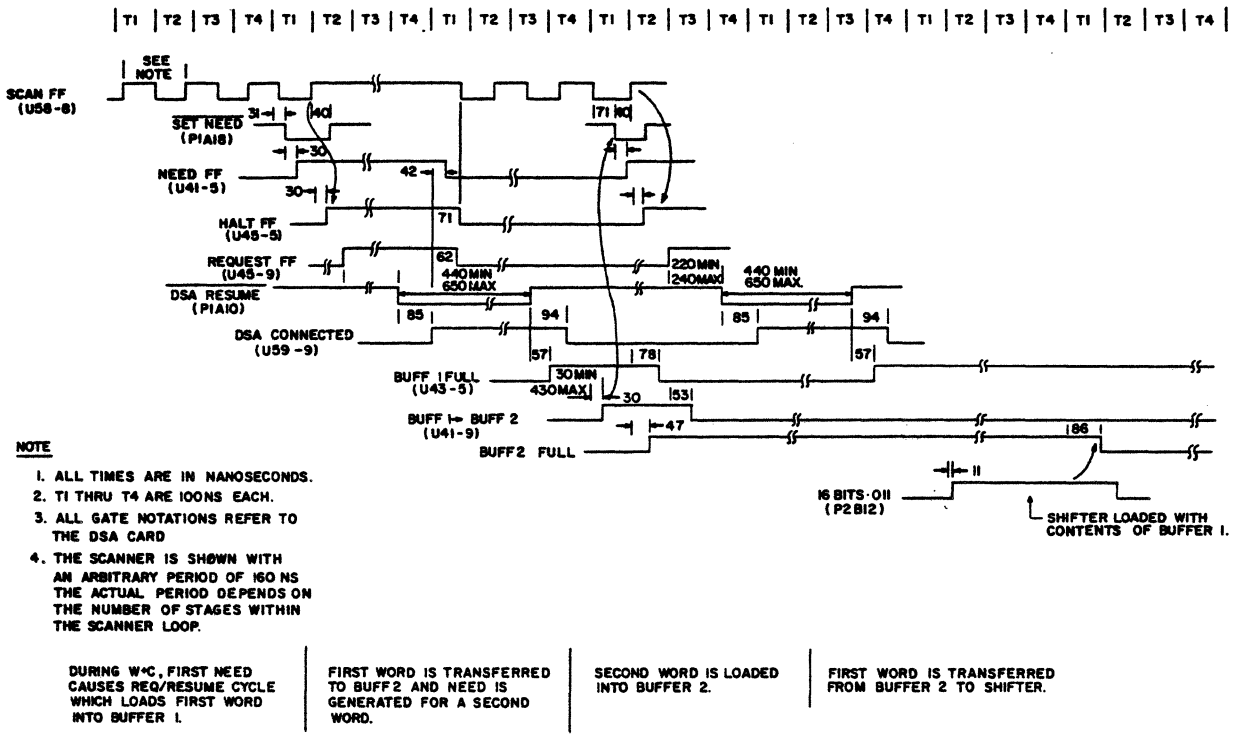
Figure 4-20 (a). Load Address Timing



NØTE

THE CASE WHERE THE HEADS ALREADY RESIDE ØN THE CYL ADDRESSED BY THE LA IS SHØWN WITH DØTTED LINES

Figure 4-20 (b). Load Address Timing

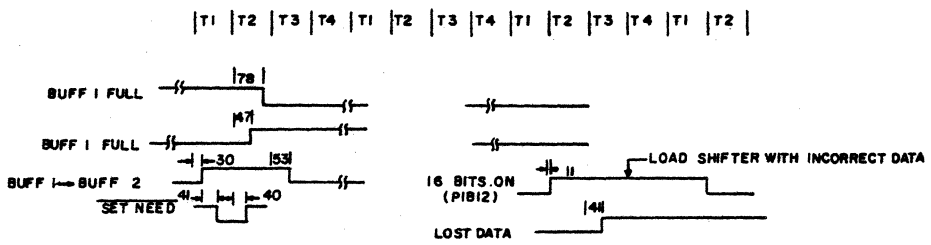


NOTE

1. ALL TIMES ARE IN NANOSECONDS.
2. T1 THRU T4 ARE 100NS EACH.
3. ALL GATE NOTATIONS REFER TO THE DSA CARD
4. THE SCANNER IS SHOWN WITH AN ARBITRARY PERIOD OF 160 NS THE ACTUAL PERIOD DEPENDS ON THE NUMBER OF STAGES WITHIN THE SCANNER LOOP.

DURING W*C, FIRST NEED CAUSES REQ/RESUME CYCLE WHICH LOADS FIRST WORD INTO BUFFER 1.	FIRST WORD IS TRANSFERRED TO BUFF2 AND NEED IS GENERATED FOR A SECOND WORD.	SECOND WORD IS LOADED INTO BUFFER 2.	FIRST WORD IS TRANSFERRED FROM BUFFER 2 TO SHIFTER.

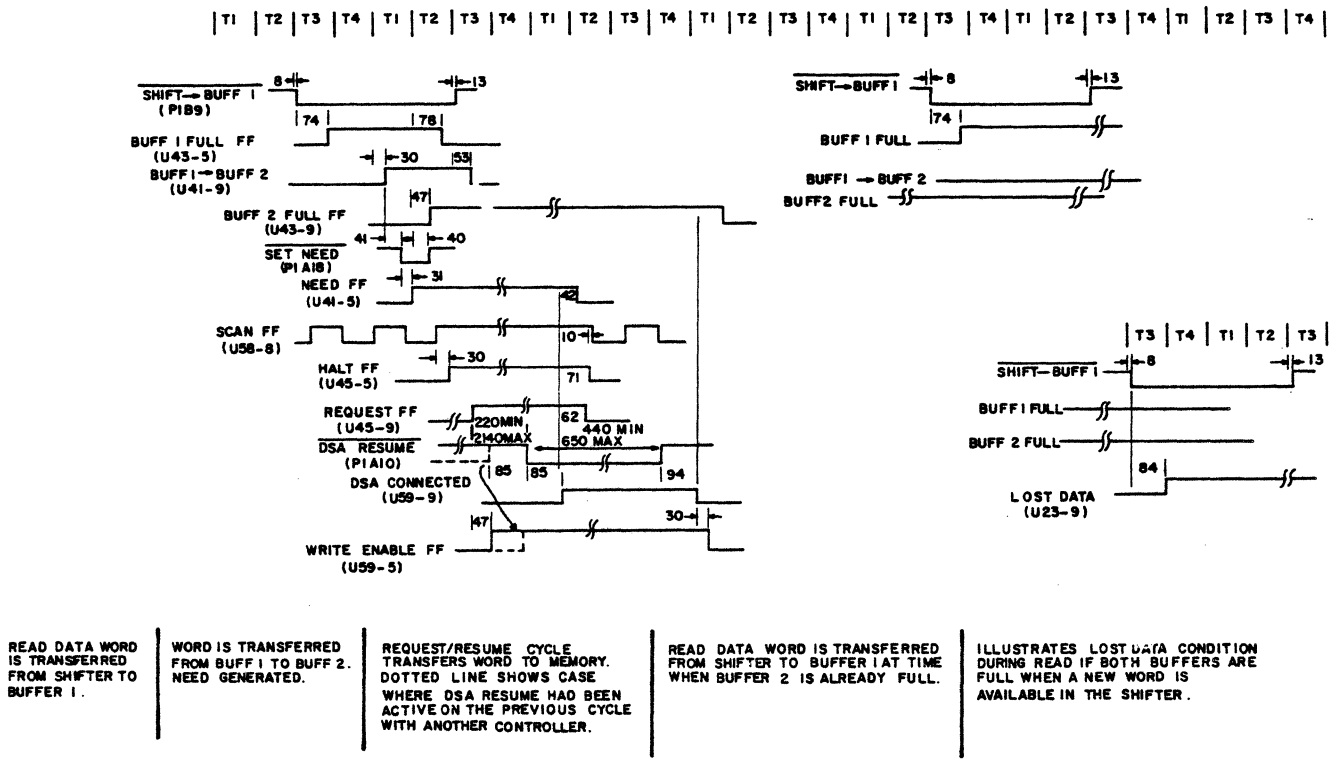
Figure 4-22 (a). Request Resume and Double Buffer Control - Write and Compare



SECOND WORD IS TRANSFERRED FROM BUFFER 1 TO BUFFER 2. NEED IS GENERATED FOR A THIRD WORD.

LOST DATA CONDITION DURING W+C IF BOTH BUFFERS ARE EMPTY WHEN DATA IS REQUIRED FOR SHIFTER.

Figure 4-22 (b). Request Resume and Double Buffer Control - Write and Compare



READ DATA WORD IS TRANSFERRED FROM SHIFTER TO BUFFER 1.	WORD IS TRANSFERRED FROM BUFF 1 TO BUFF 2. NEED GENERATED.	REQUEST/RESUME CYCLE TRANSFERS WORD TO MEMORY. DOTTED LINE SHOWS CASE WHERE DSA RESUME HAD BEEN ACTIVE ON THE PREVIOUS CYCLE WITH ANOTHER CONTROLLER.	READ DATA WORD IS TRANSFERRED FROM SHIFTER TO BUFFER 1 AT TIME WHEN BUFFER 2 IS ALREADY FULL.	ILLUSTRATES LOST DATA CONDITION DURING READ IF BOTH BUFFERS ARE FULL WHEN A NEW WORD IS AVAILABLE IN THE SHIFTER.

Figure 4-23. Request Resume & Double Buffer Control - Read

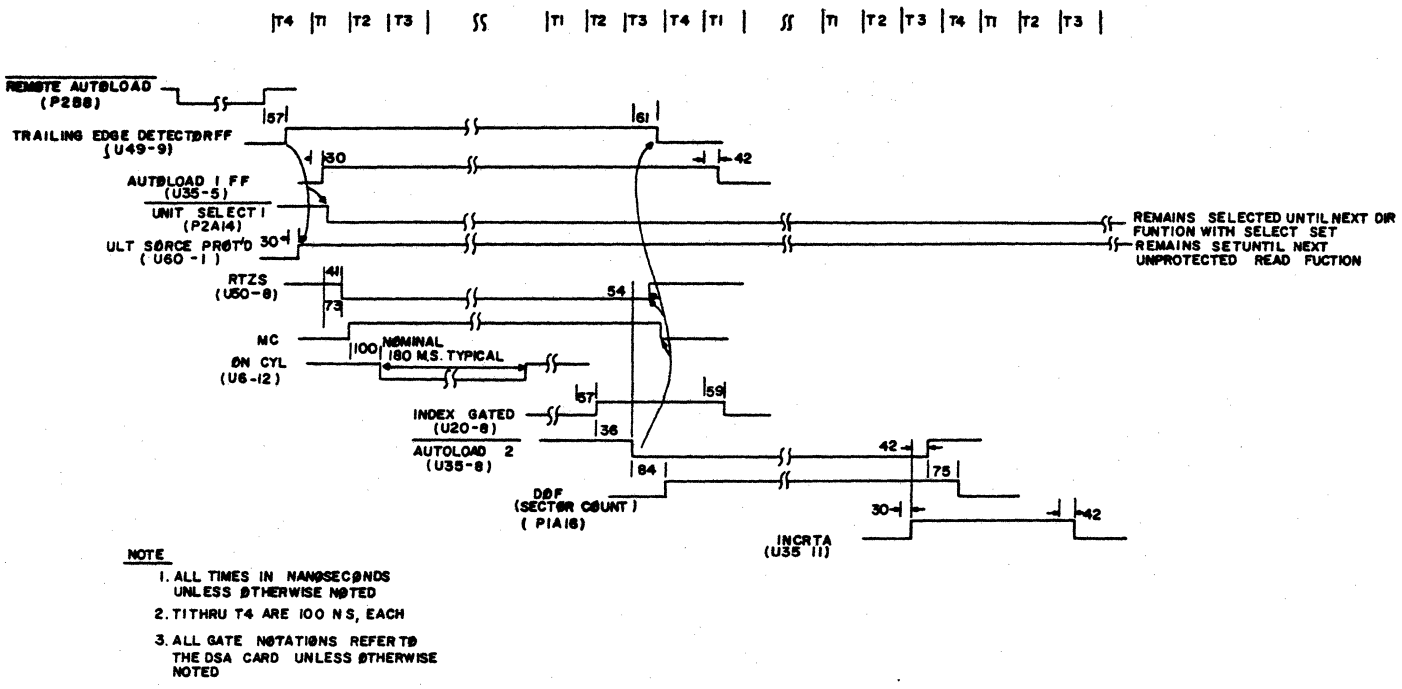


Figure 4-24. Autoload Timing

SECTION 5

LOGIC DIAGRAMS

KEY TO LOGIC SYMBOLS

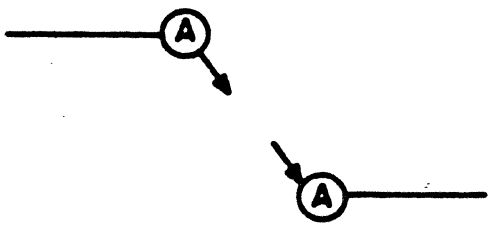
Publication 89723700 (Key to Logic Symbols) or equivalent, lists the symbols used in the logic diagrams in this manual and gives a short description of the functions they represent. The symbols conform generally to Control Data usage (Microcircuit Handbook, publication number 15006100), using the polarity logic convention.

The following paragraphs describe the signal flow conventions used.

SIGNAL FLOW

Input signals are drawn coming from the left or above; output signals are drawn going to the right or down.

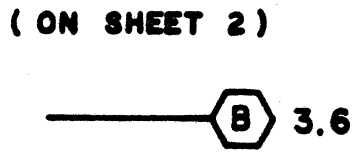
The signal lines are sometimes interrupted to allow logical grouping of components. At each such interruption one of the following indicators is used:

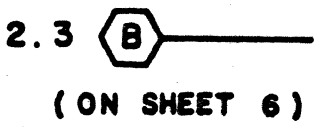


On-Sheet Continuation Reference Symbols

These symbols when used with the logic symbols in the following diagrams indicate that a connection exists between two points on a sheet. The arrows attached to each circle point from signal origin to signal destination. The letters, C, H, I, O and P are not used inside the circles, since they bear special significance on logic diagrams.

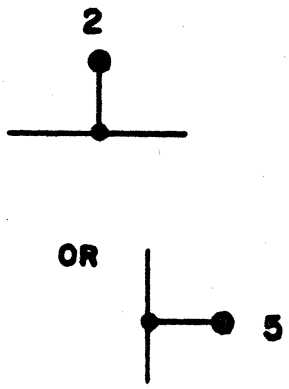
Off-Sheet Continuation Reference Symbols





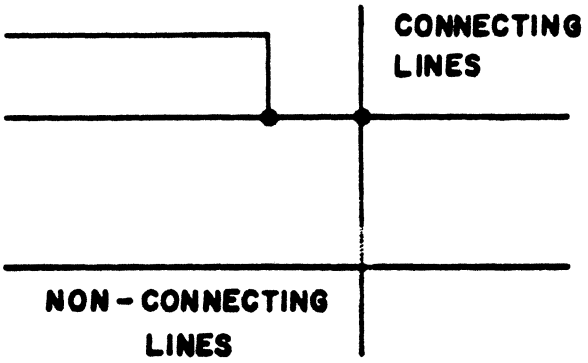
These symbols when used with the logic symbols in the following diagrams indicate that a common signal point exists between two sheets in a series of related drawings. These symbols point from output to direction of input as shown in the illustration. The letters C, H, I, O and P are not used in the hexagons, since they bear special significance on logic diagrams. The number(s) next to each hexagon indicate the sheet(s) that the signal is continued from or on. For instance, the numbers 3.6 refer to sheets 3 and 6, while 2.3 refers to sheets 2 and 3. It should be noted that the referenced sheet number(s) is always placed opposite the line extending from the hexagon.

Test Points



The test point symbol on the logic diagram shows the connection of a test point on the printed wiring board (PWB). The number adjacent to the symbol refers to the test point position on the PWB at the edge opposite the connectors. Only test point one is labeled on the edge of the PWB.

Connecting and Non-Connecting Lines

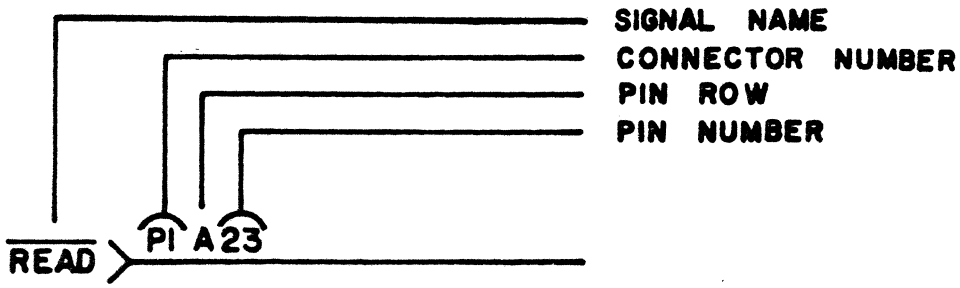


Lines connected to a common point or at a junction point are shown in the upper part of this illustration. No more than four lines are connected to a common point in the diagrams.

Lines crossing but not connected are shown in the lower part of this illustration.

Connectors

Connectors are represented on the logic diagram by the symbol for a female connector, for both input and output signals. The name of the signal is placed in the open end of the connector symbol (shown below), using the full name of the signal or the common abbreviation applicable to logic diagrams. The connector number, pin row and pin number are located above the line extending from the connector symbol.



SHIFTER PW BOARD (DWG NO. 89615800, SHEETS 1 THROUGH 8)

The Shifter card is divided into the following functional parts:

1. Shifter
2. Word Buffers and DSA Data Interface
3. DSA Address
4. Buffer Length
5. Cylinder Address
6. Status Selection

Shifter (DWG NO. 89615800, SHEET 5)

The sixteen bit synchronous shifter is used for all serial to parallel and parallel to serial conversion. The serial input is at the J-K pins of the 159 at U6. The parallel inputs are 1C0 pins of U6, U22, U5 and U21. The shifter is loaded (both serially and parallelly) on the rising edge of the SHIFTER CLOCK signal at the 2→ inputs of the 159's.

The parallel inputs to SHIFTER bits 0-11 come from the output of the 170 multiplexers at U51, 37, 36, 50 and 38 and the 189 at U35. The multiplexer outputs depend on the state of the SMPX0 and SMPX1 signals as follows: (See Sector D4 on drawing)

SMPX1	SMPX0	Multiplexer Outputs
LOW	LOW	MPX Bits 0-11 = zero (not used)
LOW	HIGH	MPX Bits 0-8 = (CYLINDER ADDRESS UPPER) CAU 12-20; MPX Bits 9-11 = zero
HIGH	LOW	MPX Bits 0-4 = (CYLINDER ADDRESS LOWER) CAL 0-4; MPX Bit 5 = zero MPX Bits 6-7 = CAL 6-7; MPX Bit 9-11 = zero
HIGH	HIGH	MPX Bits 0-11 = Buff 2; Bits 0-11

The parallel inputs to SHIFTER bits 12-15 come from bits 12-15 of BUFFER 2 (SHEET 4). The parallel load takes place on the rising edge of the SHIFTER CLOCK when the $\overline{\text{SHIFT LOAD}}$ signal is active.

The outputs of the SHIFTER go to the word buffers. In addition bits S11 and S15 go to the data and address compare logic on Sector Count card.

The shifter is set to all zeros by the $\overline{\text{CLEAR SHIFTER}}$ signal.

Word Buffers and DSA Data Interface (SHEET 4)

The two 16 bit word buffers, BUFFER 1 and BUFFER 2, are composed of the four-bit 168 latches at U1, U2, U18 and U17. BUFFER 1 is loaded from the output of the 189 multiplexer at U3, 4, 19 and 20. The multiplexer outputs depend on the state of the W+C signal as follows:

W+C	Multiplexer Outputs
LOW	MPX Bits 0-15 = Shifter Bits 0-15
HIGH	MPX Bits 0-15 = DSA Data Bits 0-15

BUFF 1 will be loaded when either the $\overline{\text{DSA} \rightarrow \text{BUFFER 1}}$ or the $\overline{\text{SHIFTER} \rightarrow \text{BUFFER 1}}$ signals are active.

BUFFER 2 is loaded from BUFFER 1 when the $\overline{\text{BUFF 1} \rightarrow \text{BUFF 2}}$ signal is active. The output of BUFFER 2 goes both to the shifter input multiplexers and to the sixteen 204 DSA DATA drivers at U34, 48, 33 and 47. The drivers are enabled when the $\overline{\text{WRITE ENABLE}}$ signal is active. Since the 204's are inverting drivers, the data to the DSA is active low.

DSA Address (SHEET 2)

The Current Word Address (CWA) counter consists of the four, four-bit 500 counters at U29, 30, 55 and 56. During a Read, Write or Compare instruction the CWA is loaded with the contents of A0-A15 when the $\overline{\text{ARCVR}\rightarrow\text{CWA}}$ signal is active. The contents of the CWA are incremented by one on the trailing edge of the $\overline{\text{CWA COUNT}}$

signal. The outputs of the CWA go to both the status selection multiplexers at U42, 43, 44 and 57 (SHEET 3) and to the inverters at U58, 31, 32 (SHEET 2) in the DSA Address interface. The DSA ADDRESS drivers (204 at U60, 59, 45 and 46) are enabled when the $\overline{\text{REQUEST}}$ signal is active. Because the 204's are inverting and there are inverters at the output of the CWA, the DSA ADDRESS will be active high.

The CWA is cleared to zeros by the master clear signal.

Buffer Length (SHEET 3)

The Buffer Length counter consists of the four, four-bit 500 counters at U13, 14, 28 and 41. During a Load Buffer instruction the contents of A0-A15 are loaded into the Buffer Length counter by the $\overline{\text{BL LOAD}}$ signal. The contents of the BL counter are decremented by one on the leading edge of both the $\overline{\text{SET NEED}}$ and $\overline{\text{ARCVR} \rightarrow \text{CWA}}$ signals. The counter is decremented by the $\overline{\text{ARCVR} \rightarrow \text{CWA}}$ signal once during each Read, Write or Compare operation. This decrementing presets the counter to one less than the total word count such that the $\overline{\text{BL BORROW}}$ signal becomes active when the last word is transferred. (The $\overline{\text{BL BORROW}}$ signal sets the BL = 0 on the card).

The BL counter is cleared by the master clear signal.

Cylinder Address (SHEET 6)

The nine-bit Current Cylinder Address (CAU20 - CAU12) is contained in the two 500 counters at U26 and 27 and in the 175 FF at U16-5. The five-bit Sector Count (CAL4 - CAL0) is contained in the 500 4-bit counter at U-39 (on Sheet 7) and the 175 at U25-5. The Disk (CAL6) and Surface (CAL7) select bits are contained in the 175 FF's at U16-9 and U7-5, respectively.

During a LOAD Address (LA) instruction the $\overline{\text{ARCVR} \rightarrow \text{CA}}$ signal causes the load of A15-A7 into the cylinder address register, A6 to the surface select bit, A5 to the disk select bit and A4-A0 to the sector counter.

At the initiation of a seek operation by the LA instruction, the contents of the cylinder address register (via the $\overline{CA20}$ - $\overline{CA12}$ signals) are transferred to the disk file. During a R+W+C+WA operation the contents of the cylinder address, the sector count, and the head and surface bits are transferred to the shifter for the parallel to serial conversion for the address compare or address write.

The sector count is incremented by one at the end of each sector on the trailing edge of the $\overline{INCR\ SECTOR}$ signal. When the sector count is incremented to 29_{10} (ID_{16}) the INCRTA (increment track address) FF at U25-9 is set on the leading edge of the next T3. The output of the INCRTA FF causes the surface SELECT BIT FF (CAL7) to be toggled on the next T2. If the CAL7 is set, the INCRTA causes the cylinder address register to be incremented by one at the leading edge of T4. The output of the cylinder address register is compared by the 524 magnitude comparator at U10, 11 and 12 (SHEET 6). The SET ADDRESS ERROR signal becomes active if CA20 CA12 is greater than the limit for the selected unit according to the state of the SELD UNIT TPI 100 signal.

The BL > CYL FF at U7-9 (SHEET 7) is set at the leading edge of T3 after setting of INCRTA FF if the CAL7 is already set. The output of the BL > CYL is used to initiate a TRACK ADDRESS Strobe to the disk file. The sector counter is cleared by the setting of INCRTA and on the following T3 INCRTA is reset.

The cylinder address register, sector counter and disk and surface select bits may be reset by the MASTER CLEAR signal.

Status Selection (SHEET 3)

The CACWA0 - CACWA15 signals will be equal to the contents of either the Current Word Address or that of the Cylinder Address Register, Sector Counter and Disk and Surface selection bits, depending on the state of the $\overline{CARST}$ signal, as follows:

$\overline{CARST}$	CACWA15 - CACWA0
LOW	CA20-CA12, CAL7, CAL6, CAL4-CAL0
HIGH	CWA15-CWA0

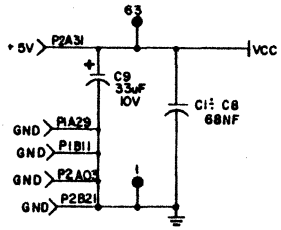
ØFF – SHEET REFERENCE

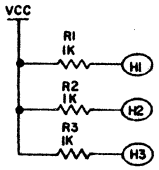
OFF SHEET REFERENCE LETTER	SIGNALS	SHEET LØCATIØN					
		2	3	4	5	6	7
A	A0	D-4	D-4				C-4
B	A1	D-4	D-4				C-4
C	INØR CAV					D-4	▼D-2
D	A 2	D-4	D-4				C-4
E	A 3	D-4	D-4				C-4
F	A 4	C-3	C-4				B-3
G	ARCVR=CA					C-4	B-4
J	A5	C-3	C-4				B-3
K	A6	C-3	C-4				B-4
L	A7	C-3	C-4			D-4	
M	A8	B-4	B-4			D-4	
N	A9	B-4	B-4			D-4	
P	A10	B-4	C-4			D-4	
Q						▼B-2	B-3
R	A11	B-4	C-4			C-3	
S	A12	B-3	A-4			C-3	
T	A13	B-3	A-4			C-3	
U	A14	B-3	B-4			C-3	
V	A15	B-3	B-4			C-2	
Z	MC			A-3		C-2	B-1
AA	CWA 0	▼D-3	D-2				
AB	CWA 1	▼D-3	D-2				
AC	CWA2	▼D-3	D-2				
AD	CWA 3	▼D-3	D-2				
AE	ARCVRCWA	C-4	D-4				
AF	MC	A-4	A-4			C-4	D-2
AG	CWA 4	▼C-2	C-2				
AH	CWA 5	▼C-2	C-2				
AJ	CWA6	▼C-3	C-2				
AK	CWA7	▼D-3	C-2				
AL	CWA8	▼B-3	B-2				
AM	CWA 9	▼B-2	B-2				
AN	CWA 10	▼B-3	B-2				
AP	CWA 11	▼B-2	B-2				
AQ				C-4	▼C-3		
AR	CWA 12	▼A-2	A-2				
AS	CWA13	▼A-2	A-2				
AT	CWA14	▼A-3	A-2				
AU	CWA15	▼A-3	A-2				
AV				D-4	▼A-3		
AW				C-4	▼C-3		
AX				D-4	▼A-3		
AY				D-4	▼A-3		
AZ				D-4	▼A-3		
BA	CAL0		D-2		A-4		▼C-3
BB	CAL 1		D-2		A-4		▼D-3

CØNTINUED ØN SHEET 8

SHEET REVISION STATUS							
1	2	3	4	5	6	7	8
04	05	05	05	04	06	06	03
A	A	A	A	A	A	A	A

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
03	CK 429	REDRAWN PER CDC STANDARDS				
04	CK 619	DRAWING ERRORS ON: SH4: P2B29 SH5: U35-14 SH7: U25-5; U7-13	Ryan	29-4-74		
05	CK 1024	DWG. ERRORS CORRECTED TAGS ADDED CORRECT REV 03	Ryan	oct, 74		
06	CK 983	SH6 A-3: U15-3/U11-11 REPLACES H4/U11-11 FOR 406 MAX TRACK CAPACITY	ML	8 3 75		
		SH7 A-4: VCC AND GND CONNECTIONS MOVED TO SHEET 1				
		FITS ASSY 89912100 REV 04				
A	CK 1154	RELEASED CLASS A USES PWB 89615700 REV 07	ML	4-5-75	HM	





NOTES:
1. ALL RESISTØRS ARE 1/4 WATT, 5%.
2. ▼– DENØTES SIGNAL ØRIGIN

AY 89912100
AW 89615700
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING
MATERIAL
FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA

FIRST USED ON FA 716-A

DWN	Neomi P.	11.12.73
CHKD		
ENGR		7.1.74
MFG		15 May 74
APPR		May 15

TITLE DETAILED LOGIC DIAGRAM
DISK SHIFTER

CODE IDENT C

DRAWING NO 89615800

SCALE

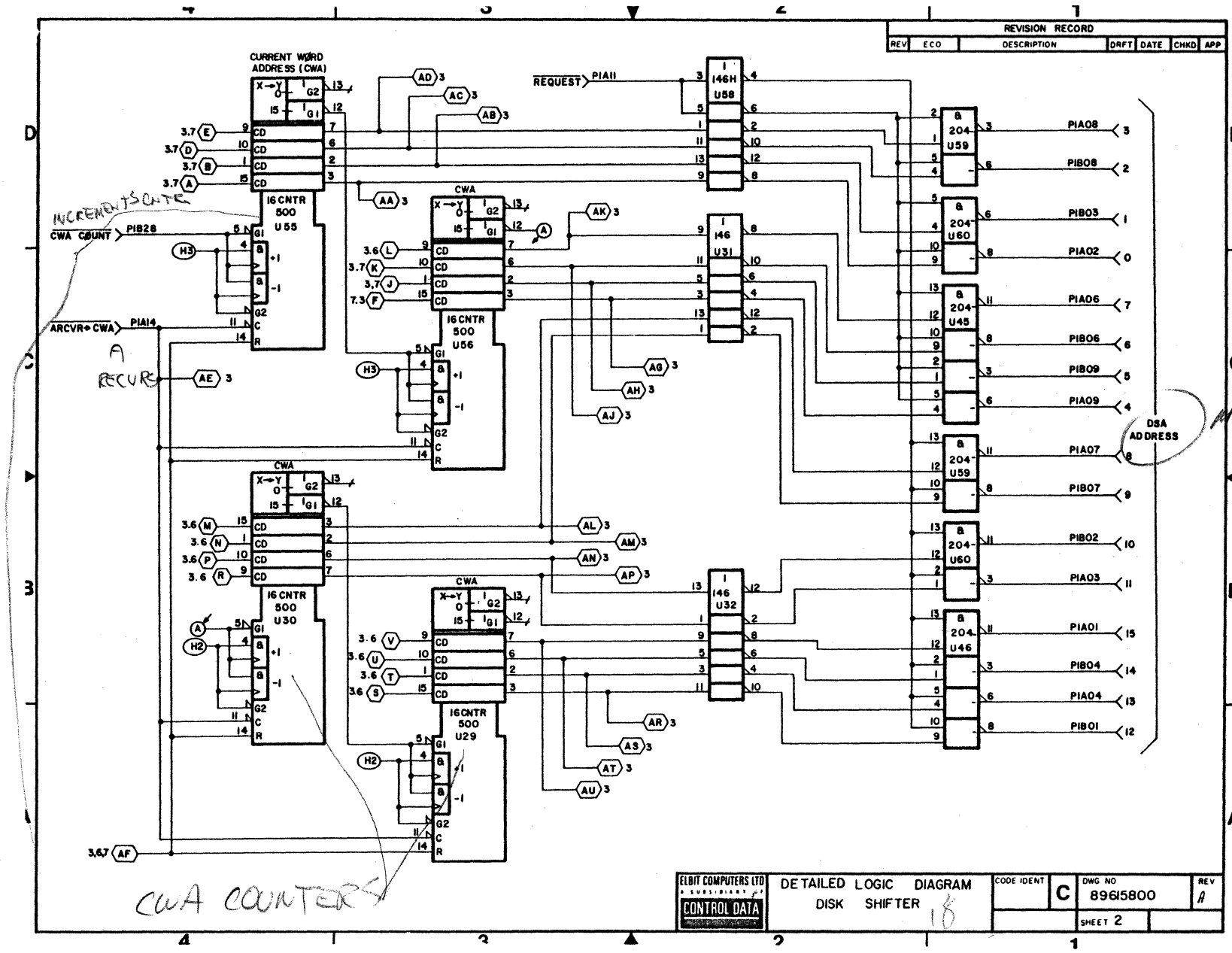
SHEET 1 OF 8

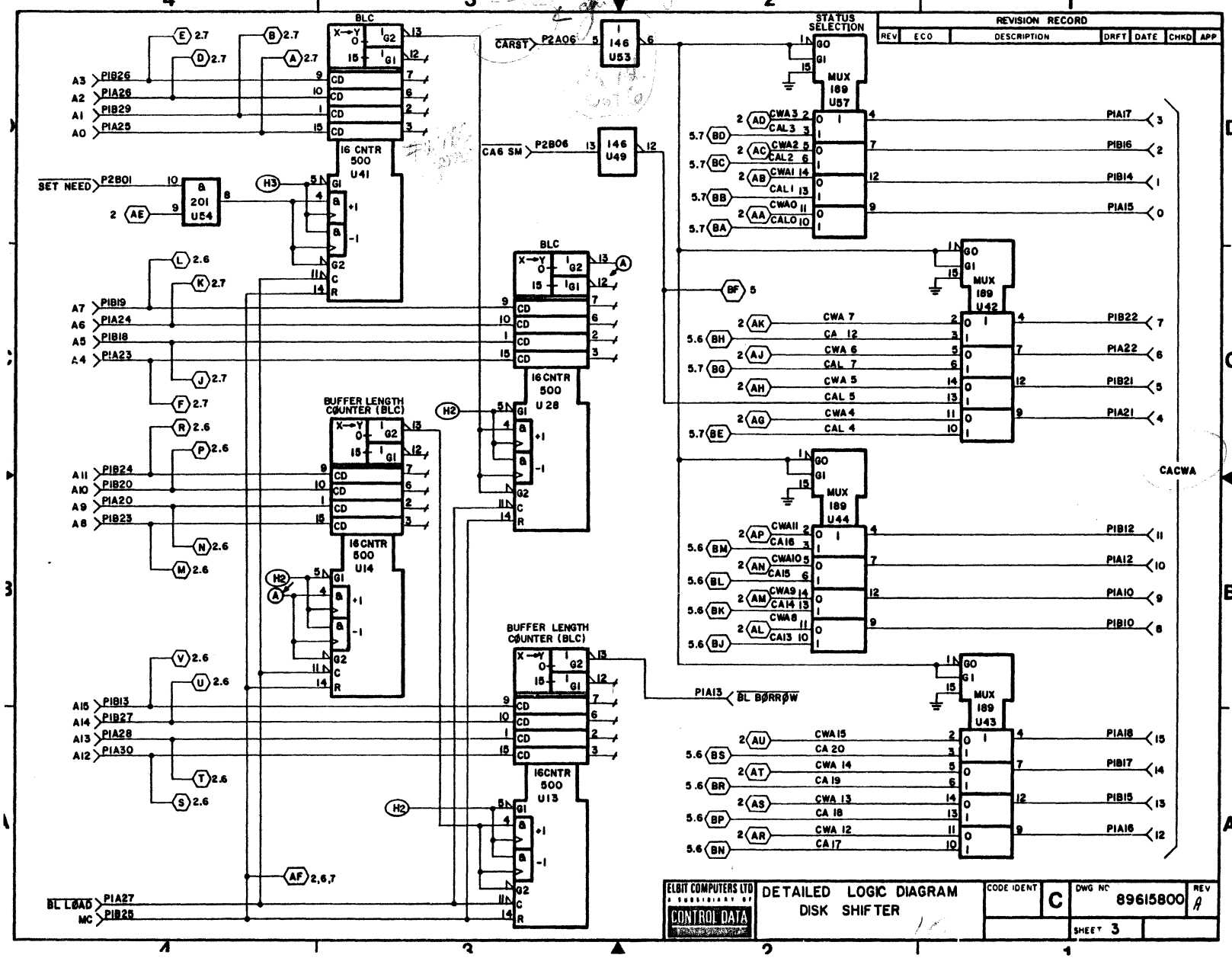
REVISION RECORD						
NO.	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

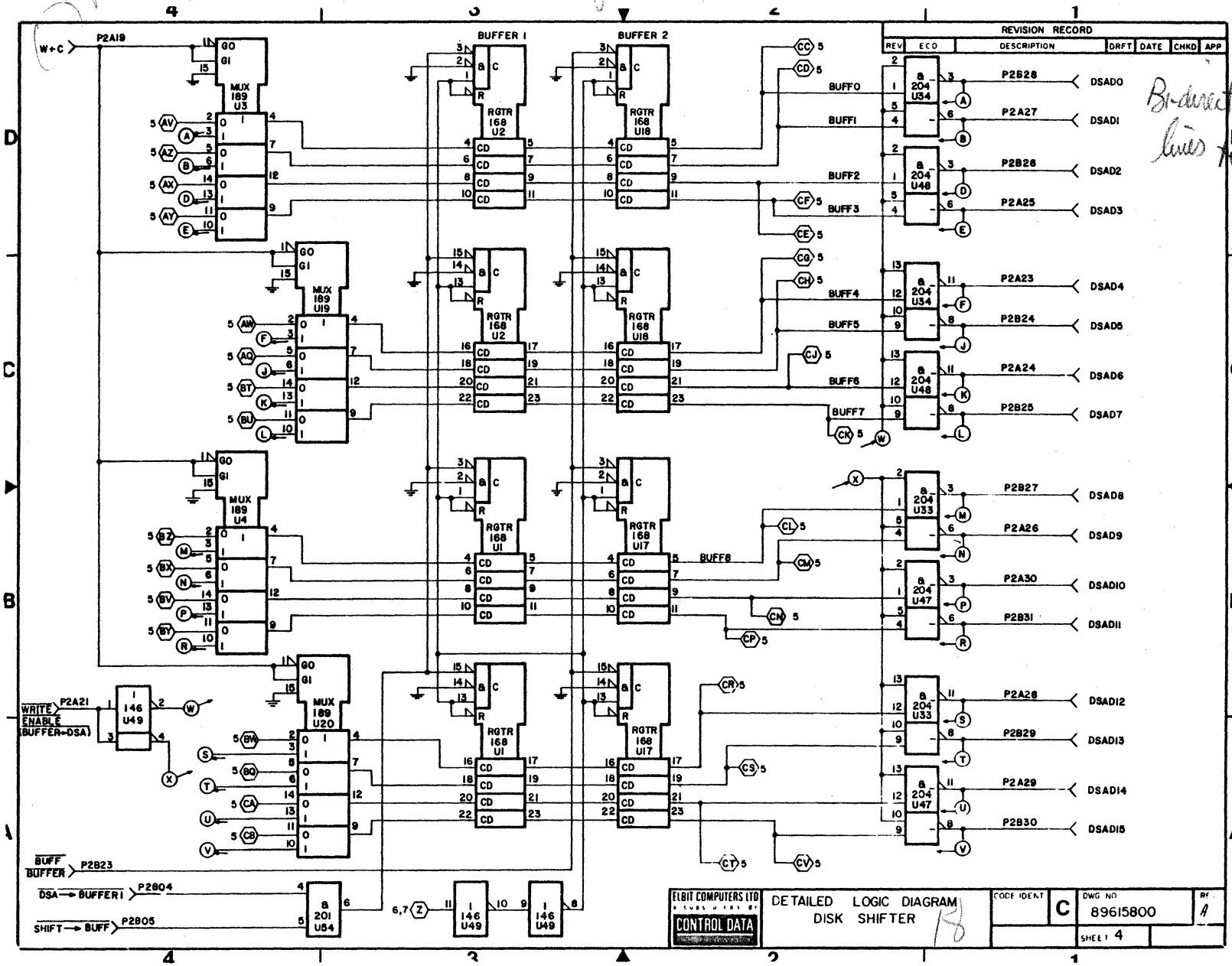
ØFF-SHEET REFERENCE
CØNTINUED FRØM SHEET 1

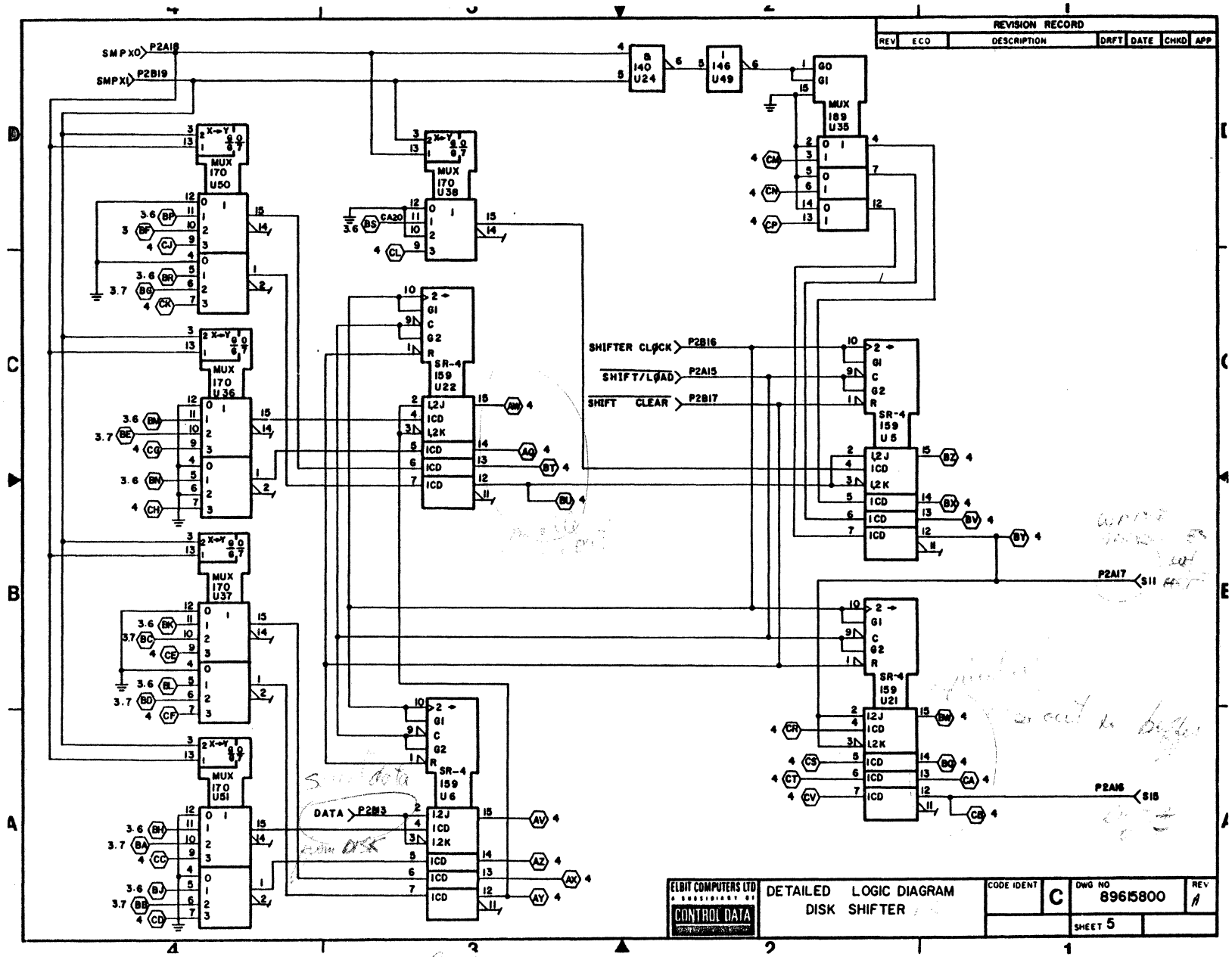
ØFF SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION					
		2	3	4	5	6	7
BC	CAL 2		D-2		B-4		▼D-3
BD	CAL 3		D-2		B-4		▼C-3
BE	CAL 4		C-2		C-4		▼B-3
BF	CAL 5		▼C-2		D-4		
BG	CAL 7		C-2		C-4		▼A-2
BH	CA 12		C-2		A-4	▼D-3	
BJ	CA 13		B-2		A-4	▼D-3	
BK	CA 14		B-2		B-4	▼D-3	
BL	CA 15		B-2		B-4	▼D-2	
BM	CA 16		B-2		C-4	▼C-2	
BN	CA 17		A-2		C-4	▼C-2	
BP	CA 18		A-2		D-4	▼C-2	
BQ				A-4	▼A-1		
BR	CA 19		A-2		C-4	▼C-2	
BS	CA 20		A-2		D-3	▼C-1	
BT				C-4	▼C-3		
BU				C-4	▼B-3		
BV				B-4	▼B-1		
BW				A-4	▼A-1		
BX				B-4	▼B-1		
BY	611			B-4	▼B-1		
BZ				B-4	▼C-1		
CA				A-4	▼A-1		
CB	515			A-4	▼A-1		
CC	BUFF 0			▼D-2	A-4		
CD	BUFF 1			▼D-2	A-4		
CE	BUFF 2			▼D-2	B-4		
CF	BUFF 3			▼D-2	A-4		
CG	BUFF 4			▼C-2	C-4		
CH	BUFF 5			▼C-2	B-4		
CJ	BUFF 6			▼C-2	D-4		
CK	BUFF 7			▼C-2	C-4		
CL	BUFF 8			▼B-2	C-3		
CM				▼B-2	D-2		
CN				▼B-2	D-2		
CP				▼B-2	D-2		
CR				▼A-2	B-2		
CS				▼A-2	A-2		
CT				▼A-2	A-2		
CV				▼A-2	A-2		

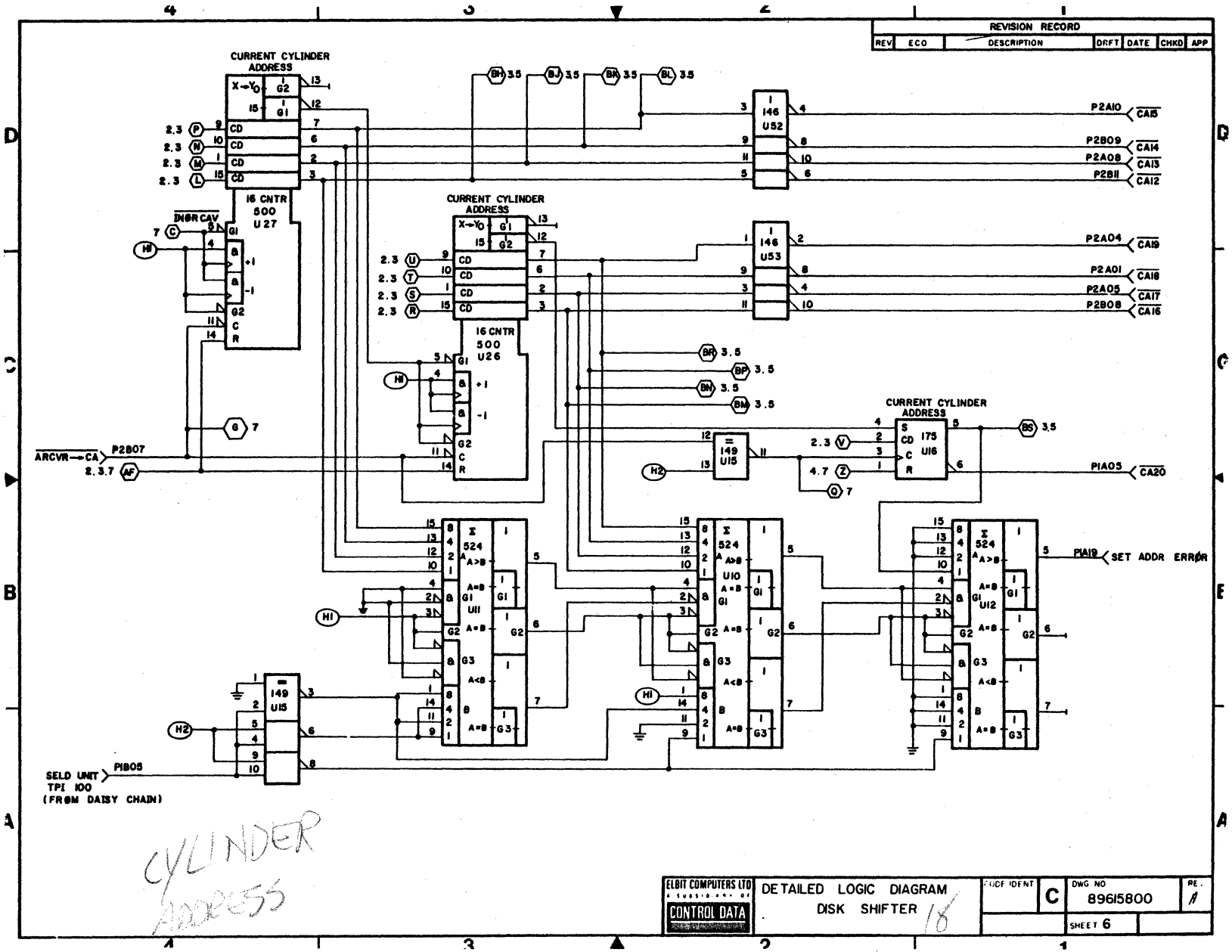
ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM DISK SHIFTER	CODE IDENT C	DWG NO 89615800	REV A
			SHEET 8	


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
CURRENT WORD ADDRESS (CWA)
CWA COUNT PIB28
ARCVR→CWA PIA14
REQUEST PIA11
INCREMENTS CNTR
A RECURS
16 CNTR 500 U55
16 CNTR 500 U56
16 CNTR 500 U30
16 CNTR 500 U29
146H U58
146 U31
146 U32
204 U59
204 U60
204 U45
204 U59
204 U60
204 U46
PIA08 PIB08 PIB03 PIA02 PIA06 PIB06 PIB09 PIA09 PIA07 PIB07 PIB02 PIA03 PIA01 PIB04 PIA04 PIB01
DSA ADDRESS
mem. address we all accessing
CWA COUNTERS
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK SHIFTER 16
CODE IDENT C
DWG NO 89615800
REV A
SHEET 2

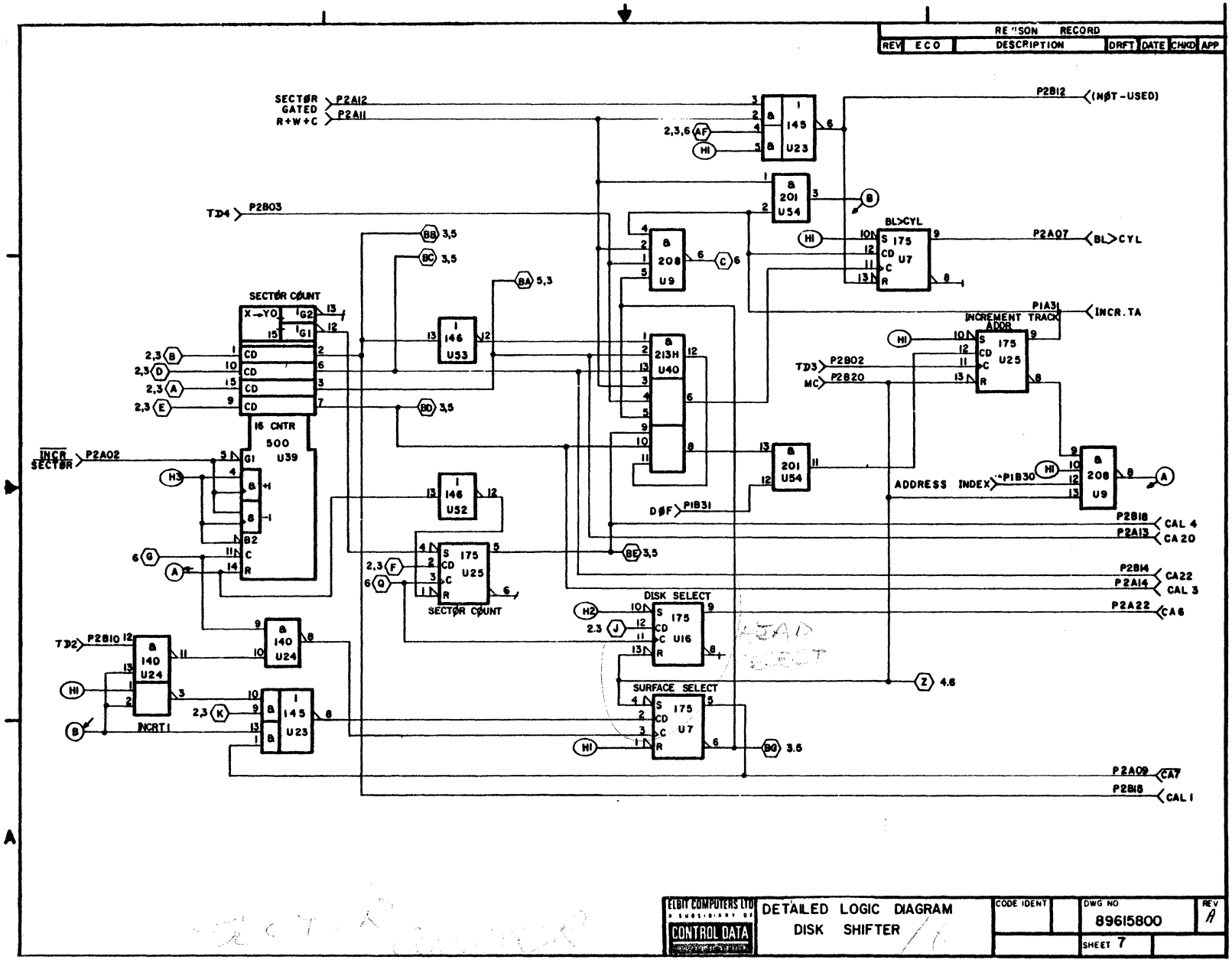

BLC
16 CNTR 500 U41
BLC
16CNTR 500 U28
BUFFER LENGTH COUNTER (BLC)
16CNTR 500 U14
BUFFER LENGTH COUNTER (BLC)
16CNTR 500 U13
STATUS SELECTION
MUX 189 U57
MUX 189 U42
MUX 189 U44
MUX 189 U43
CARST P2A06
CA6 SM P2B06
SET NEED P2B01
BL LOAD P1A27
MC P1B25
BL BORROW P1A13
CACWA
REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK SHIFTER
CODE IDENT C
DWG NO 89615800
REV A
SHEET 3


BUFFER 1
BUFFER 2
REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
W+C
P2A19
MUX 189 U3
MUX 189 U19
MUX 189 U4
MUX 189 U20
RGTR 168 U2
RGTR 168 U18
RGTR 168 U1
RGTR 168 U17
BUFF0
BUFF1
BUFF2
BUFF3
BUFF4
BUFF5
BUFF6
BUFF7
BUFF8
P2B28
P2A27
P2B26
P2A25
P2A23
P2B24
P2A24
P2B25
P2B27
P2A26
P2A30
P2B31
P2A28
P2B29
P2A29
P2B30
DSADO
DSADI
DSAD2
DSAD3
DSAD4
DSAD5
DSAD6
DSAD7
DSAD8
DSAD9
DSADIO
DSADII
DSADI2
DSADI3
DSADI4
DSADI5
WRITE ENABLE (BUFFER→DSA)
P2A21
BUFF BUFFER
P2B23
DSA→BUFFER I
P2B04
SHIFT→BUFF
P2B05
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK SHIFTER
CODE IDENT
C
DWG NO
89615800
REV
A
SHEET 4


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SMPXO P2A18
SMPXI P2B19
SHIFTER CLOCK P2B16
SHIFT/LOAD P2A15
SHIFT CLEAR P2B17
DATA P2B13
P2A17
P2A16
MUX 170 U50
MUX 170 U36
MUX 170 U37
MUX 170 U51
MUX 170 U38
MUX 189 U35
SR-4 159 U22
SR-4 159 U5
SR-4 159 U21
SR-4 159 U6
U24
U49
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK SHIFTER
CODE IDENT C
DWG NO 89615800
REV A
SHEET 5



CYLINDER ADDRESS


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SECTOR GATED R+W+C
P2A12
P2A11
P2B12
(NOT-USED)
TD4
P2B03
SECTOR COUNT
16 CNTR
500
U39
INCR SECTOR
P2A02
SECTOR COUNT
DISK SELECT
SURFACE SELECT
BL>CYL
P2A07
INCREMENT TRACK ADDR
P1A31
INCR.TA
TD3
P2B02
MC
P2B20
ADDRESS INDEX
P1B30
D0F
P1B31
P2B18
CAL 4
P2A13
CA 20
P2B14
CA22
P2A14
CAL 3
P2A22
CA6
P2A09
CA7
P2B15
CAL 1
TD2
P2B10
INCRT I
4.6
3.5
5,3
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK SHIFTER
CODE IDENT
DWG NO
89615800
REV
A
SHEET 7

"Pages 5-16 to 5-24 are unassigned."

A/Q PW BOARD (DWG NO. 89616100, Sheets 1-8).

The A/Q card is divided into the following functional parts:

1. Reply/Reject Logic
2. Function Register, Decode and Encode
3. Interrupt and Error Logic
4. Checkword
5. True Cylinder Address
6. Status Interface
7. CDD Interface

Reply/Reject Logic (SHEET 2)

The computer places the Equipment Number (in Q7 - Q10) a minimum of 100ns prior to activating the $\overline{\text{A/Q READ}}$ or $\overline{\text{A/Q WRITE}}$ signal. If the contents of Q7 - Q10 match the setting of the Equipment Number Switches the EQUIPMENT NUMBER MATCH signal will be active. The reset to the INSTRUCTION FF (U40 - 9) will go high when A/Q (R+W), EQUIPMENT NO. MATCH and $\overline{\text{A/QW=0}}$ are active and the FF will be set on the following $\overline{\text{TI}}$.

The REPLY ENABLE FF (U68) will be set 800ns later and the $\overline{\text{A/Q REPLY}}$ or $\overline{\text{A/Q REJECT}}$ will be transmitted, depending on the condition of the controller and the particular function code. Reply conditions for output function (A/Q WRITE) are DISK READY . $\overline{\text{BUSY RR}}$. POKM . DISK ON CYLINDER (at U3-6 on SHEET 7) or CTRLR BUSY . POKM . DF (= DF Gated at U21-8 on SHEET 3). The presence of either of these conditions will cause the generation of the $\overline{\text{AØAF+MC}}$ (Any Output from A Function or Master Clear) at U42-8 (SHEET 6). The reply condition for input functions (A/Q READ) is simply $\overline{\text{ILLEGAL FUNCT}}$ inactive. On T3 the REPLY CONDITION (U54-8) will be captured in the REPLY CONDITION FF (U70). If none of these Reply Conditions are active the REPLY CONDITION FF is not set and when the REPLY ENABLE FF sets, the $\overline{\text{A/Q REJECT}}$ signal is transmitted.

In response to the $\overline{\text{A/Q REPLY}}$ (or REJECT) signal the computer de-activates the $\overline{\text{A/Q WRITE}}$ or $\overline{\text{READ}}$ which causes the REPLY ENABLE FF to reset and on the next T1 the EQST FF resets. The resetting of $\overline{\text{EQST}}$ generates INITQ (U9 - 11) which enables the setting of the CTRLR BUSY FF (DSA Card).

Function Register, Decode and Encode

The inputs to the Function Decoder (167 at U61 on SHEET 3) are Q00 - Q02 (function code) and the output of the A/Q READ FF (U52 - 11, SHEET 2). When the $\overline{\text{EQST}}$ goes active at the enable input of the 167, the decode is allowed.

Depending on whether the function is immediately executable or requires an extended duration, the outputs of the Function Decode are either used directly or captured in the Function Register.

The Function Register consists of the four stages of the 520 latch at U59 (SHEET 3) and the two FF's at U37. If the REPLY CONDITION signal is active, the Function Register is loaded with the appropriate outputs of the FUNCTION DECODE on the leading edge of the T2 following the setting of the INSTRUCTION FF (U40, SHEET 2). At the same time, the BLOCK LOAD FF (U54-8 on SHEET 2) is set to prevent changing the contents of the Function Register on subsequent T2 pulses.

The outputs of the Function Register are used directly as well as being encoded into the following signals:

W + C
R + W + C
R + C + CC.ADR
R + W + C + CC.ADR

Where R=READ* + AUTOLOAD 2

WA·ADR
DOF-LA-AUTOLOAD=READ*+W+C+WA+CC
DOF-LA=R+W+C+ADDRESS
DOF=R+W+C+LA+ADDRESS

*READ does not include AUTOLOAD

On SHEET 3 the ADDRESS FF (U40-5) is set by the $\overline{\text{ADDRESS INDEX}}$ signal to indicate that either a WA or a CC instruction is in process and the Index Mark has been detected.

The Function Register and ADDRESS FF are cleared at the end of an operation (both normal and abnormal) by the $\overline{\text{RESET CTRLR BUSY} \cdot \text{SET EØP}}$ signal (SHEET 2) or the MASTER CLEAR. The LA FF (U37 on SHEET 3) is cleared at the end of the controller portion of a Load Address Operation by the $\overline{\text{CLEAR LA}}$ signal (SHEET 3) from U9-6.

Interrupt and Error Logic (SHEET 4)

The Interrupt Enable Register consists of three stages of the 520 three-bit latch at U4. The latches are loaded at the leading edge of DF gated. The data loaded depends on the state of A01 - A04 and the previous state of the latches as follows:

(a) When any of A02, A03 or A04 are high, the latches corresponding to the highs are set unconditionally.

(b) When A1 is high and any of A02, A03 or A04 are low, the stage corresponding to the lows will be reset.

(c) When A1 is low and any of the A02, A03 or A04 are low, the stage corresponding to the lows will remain in the state that existed before the DF Gated signal.

These conditions are expressed logically by:

$$D' = Ai + A1 \cdot D$$

where

D = State of latch after DF Gated

D = State of latch before DF Gated

Ai= A02, A03 or A04

The Interrupt Enable Register is cleared by the MASTER CLEAR signal.

On Sheet4, READY.$\overline{\text{BUSY}}$ 1 FF (U20) will be set at T1 when the disk is ready, on cylinder and the controller is not busy. The READY.$\overline{\text{BUSY}}$ 2 FF U20 will be set at the following T2. The Q output of READY·$\overline{\text{BUSY}}$ 1 is ANDed with the $\overline{Q}$ output of READY·$\overline{\text{BUSY}}$ 2 by the 141 at U2 along with the output of the NEXT READY NOT BUSY ENABLE. The resulting 100ns pulse at the output U2 - 12 sets the INTERRUPT FF which, in turn, causes the generation of the $\overline{\text{A/Q INTERRUPT}}$ signal.

Similarly, the INTERRUPT FF (U1-8 and 11) will be set to indicate the end of an operation if either of the $\overline{\text{EØPM} \cdot \overline{\text{CTRLR BUSY}}}$ or $\overline{\text{RESET CTRLR BUSY SET EØP}}$ signals at U58-8 is active and the EØP Enable (on Disk DSA) is set.

The INTERRUPT FF (U1) will also be set by the 100ns pulse resulting from the ANDing of the Q output of ALARM 1 (U5-9), the $\overline{Q}$ of ALARM 2 (U5-6) and ALARM ENABLE at U2-8. ALARM 1 FF is set by the output of the ERROR FF. The ERROR FF will be set by any one of the following:

(a) CONTROLLER BUSY · DISK NOT READY

(b) CONTROLLER SEEK ERROR

(c) ADDRESS ERROR

(d) DRIVE SEEK ERROR

(e) EØS · (STORAGE PARITY ERROR + PROTECT FAULT)

(f) EØS · (CHECKWORD ERROR + LOST DATA)

The ERROR FF is reset by the setting of the ALARM 2 FF or by the MASTER CLEAR signal.

The Q output of ALARM 1 is ANDed with the $\overline{Q}$ output of ALARM 2 at U6 - 3 (SHEET 4) to result in the signal, $\overline{\text{SET ALARM}}$. This 100ns signal both sets the ALARM FF and generates the $\overline{\text{RESET CTRLR BUSY-SET EØP}}$ signal on Disk. The ALARM FF is reset by $\overline{\text{AØAF+MC}}$.

The DISK SEEK ERROR, and CONTROLLER SEEK ERROR FF's (U63, U6 on SHEET 6) are set when the corresponding "set" signal becomes active. The PROTECT FAULT and STORAGE PARITY ERROR FF's are set when the corresponding error signal and the DSA connected signal are active at the trailing edge of the $\overline{\text{CWA COUNT}}\cdot(\overline{\text{RESUME}})$ signal. These four error FF's are cleared by $\overline{\text{AØAF+MC}}$.

Checkword (SHEET 5)

The twelve bit Check Word Shifter consists of the four stages of the 520 at U11, the two 159 Synchronous Shift Registers at U13 and U14 and the 175 at CHECKWORD 2 (U8-5). Serial data enters the Checkword via the INPUT CKWD signal. The CKWD SHIFT signal (from Sector Count card) causes the shift of Checkword. The inputs to bit zero, one, two, three and eleven are from the outputs of the 149 Exclusive OR's at U10 and U17. The Exclusive OR's perform a modulo two addition (half-add with carry discarded). The serial input to the Checkword is blocked by the $\overline{\text{W CKWD}}$ (Write Checkword) signal when the Checkword is being written onto the disk.

At the output of the Checkword Shifter is combinational logic to check that the contents of the Checkword are all zeros. During Read, Write or Checkword Check operations the DATA CKWD ERROR FF (at U8-9) will be set if the Checkword is not zero at the T2 when the SAMPLE CHECKWORD signal is present.

The DATA CKWD ERROR FF will be reset by $\overline{\text{A}\emptyset\text{AF+MC}}$. The signal $\overline{\text{ADDR. CKWD = 0}}$ will be active if the Ckwd is zero after reading the Address Checkword during a Read, Write, Compare or Checkword Check operation.

The 12 bit CHECKWORD 2 register consists of the 4 stages of the 500 at U28 and the 8 stages of the 168 at U30. When the $\overline{\text{LOAD CKWD 2}}$ signal is active, the contents of the Checkword are loaded into the Checkword 2 register. The Checkword 2 register is cleared by the MASTER CLEAR signal.

True Cylinder Address (SHEET 8)

The 9 bit True Cylinder Address (TCA) Shift register consists of the two 159 Shift registers at U15 and U16 and the FF at U68-5. The TRUE CYLINDER ENABLE FF (U54) is set during Read, Write, Compare and Checkword Check operation when the $\overline{\text{CAU} \rightarrow \text{SHIFT}}$ signal is active. The output of the TRUE CYLINDER ENABLE FF enables the shifting of the TCA register at T4. The serial input to the TCA shifter is from the READ DATA signal. The TCA register is cleared by the MASTER CLEAR signal.

Status Interface (SHEET 6,7)

The 170 multiplexers at U30, 31, 32, 45, 46, 47, 48 and 49 allow the selection of one out of four groups of 16 bits for input to the A register. The selection depends on the state of the four status functions (from the Function Decode) as follows:

S_1	S_0	Multiplexer Outputs
LOW	LOW	Bits 0-11 = Ckwd 0-11; Bits 12-15 = 0
LOW	HIGH	Director Status: Bit 0 = READY Bit 1 = CTRLR . Bit 2 = INTERRUPT FF Bit 3 = DISK ON CYL.

S_1	S_0	Multiplexer Outputs
		Bit 4 = EØP
		Bit 5 = ALARM FF
		Bit 6 = DATA NO COMPARE
		Bit 7 = SELECTED UNIT PROTECTED
		Bit 8 = DATA CKWD ERROR
		Bit 9 = LOST DATA
		Bit 10 =ADDRESS ERROR
		Bit 11 =CONTROLLER SEEK ERROR
		Bit 12 =SELECTED UNIT TP1 100 (Single Density)
		Bit 13 =STORAGE PARITY ERROR
		Bit 14 =PROTECT FAULT
		Bit 15 =DRIVE SEEK ERROR
HIGH	LOW	Bits 0-15 = Current Word Address 0-15
HIGH	HIGH	Bits 0-3 = SCØSE0-3 (Seek Complete or Seek Error)
		Bits 4-6 = 0
		Bits 7-15 = TCA 7-15 (True Cylinder Address)

The output of the multiplexers are transmitted to the A/Q channels A register via the 204 drivers. The drivers are enabled when A/Q READ and EQST are active. Since the drivers are inverting the data to the A register is active low.

CDD Interface (SHEET 4)

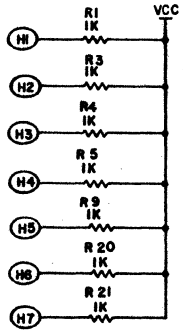
Four signals from the Cartridge Disk Drive (CDD) are received by the four stages of the 902 at U56. Disk Ready, Disk Fault, Set Drive Seek Error and Read Data are used on the A/Q card. In addition READ DATA is transmitted to the Sector Count card.

ØFF SHEET REFERENCE

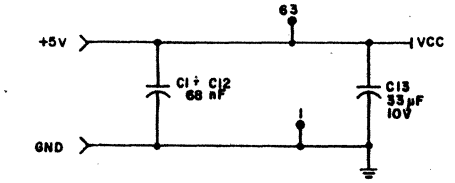
ØFF SHEET REFERENCE LETTER	SIGNALS	SHEET LØCATIØN						
		2	3	4	5	6	7	8
A	TCA7						D-2	B-1▼
B	TCA8					A-3		B-1▼
D	TCA9					A-3		B-1▼
E	TCA10					B-3		B-1▼
F	$\overline{MC}$	A-3▼		B-3	B-1			A-2
G						B-1▼	D-2	
J	READ DATA			C-4▼				B-2
K	TCA11					B-3		C-1▼
L	TCA12					C-3		C-1▼
M	TCA13					C-3		C-1▼
N	TCA14					D-3		C-1▼
Q	TCA15					D-3		B-1▼
R	MC	A-4▼			C-1			B-3
S		A-3▼	B-3					
T	R*C*CC*ADDR		B-1▼		C-4			C-4
U	CKWD 3				D-1▼		B-3	
V	CKWD 2				D-1▼		B-3	
W	A/Q READ	B-3▼	C-4			B-2		
X	CKWD 0				D-1▼		A-2	
Y	EQST	D-2▼				C-2		
Z	CKWD1				D-1▼		A-2	
AA			B-3▼			D-3	D-2	
AB			B-3▼			D-3	D-3	
AC	CKWD 10				A-1▼	B-3		
AE	CKWD 11				A-1▼	B-3		
AF	CKWD ERROR			A-3	A-3▼	A-3		
AG	CKWD 8				B-1▼	A-2		
AJ	CKWD 9				B-1▼	A-3		
AK	CKWD 6				B-1▼		D-3	
AL	CKWD 7				B-1▼		D-2	
AM	CKWD 4				B-1▼		C-3	
AN	ALARM			B-1▼				
AQ	$\overline{A/Q}$AF*MC	A-3▼		B-2	A-4	B-3		
AR	DISK ON CYL			C-4			B-3	
AS	READY			B-3▼			A-3	
AT	CKWD 5				B-1▼		C-3	
AU	INIT	B-3					B-3▼	
AV	T4	B-2						C-3
AW	ADDR ERROR			A-4		B-3		
AH	LOST DATA			A-4		A-3		
AY	CNTLR BUSY		A-4	C-4			B-3▼	
AP				C-1▼			B-3	
BA	$\overline{MCI}$	D-2▼					A-4	
BB				A-3		C-3▼		
BD	$\overline{SET\ DRIVE\ SEEK\ ERR}$			A-4▼		A-3		
BE	$\overline{DRIVE\ SEEK\ ERR}$			A-4		B-3▼		
BF		B-3	B-4▼					

SHEET REVISION STATUS								REVISION RECORD						
1	2	3	4	5	6	7	8	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
								12	CK1028	REDRAWN TO CDC STANDARD				
A	A	A	A	A	A	A	A	1	CK1169	RELEASED CLASS A FUNCT. DESC & SIGNALS ADDED				

		2	3	4	5	6	7	8
BG		B-3	B-4▼					
BH		C-3▼	C-4					
BJ		D-2▼	C-4					
BK	T1	B-2▼		B-3				
BL	T2	D-2▼		C-3	A-4			
BM	DF GATED	A-3	A-3▼					
BN	POKM		A-4				B-3	
BP		A-1▼	B-3					
BQ	R*W*C	A-1	C-1▼					
BR				A-3		B-3▼		
BS	DF GATED	A-3▼		D-3				
BT		A-4		C-4				
BU	R*C*CC		D-1▼		B-4			
BV	CTRLR BUSY			B-4			B-4	
AX		B-1▼					A-4	



NØTES:
1. ALL RESISTØRS ARE .25W ± 5 %
2. ▼–DENØTES SIGNAL ØRIGIN



AY 89778600
AW 89616001
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA

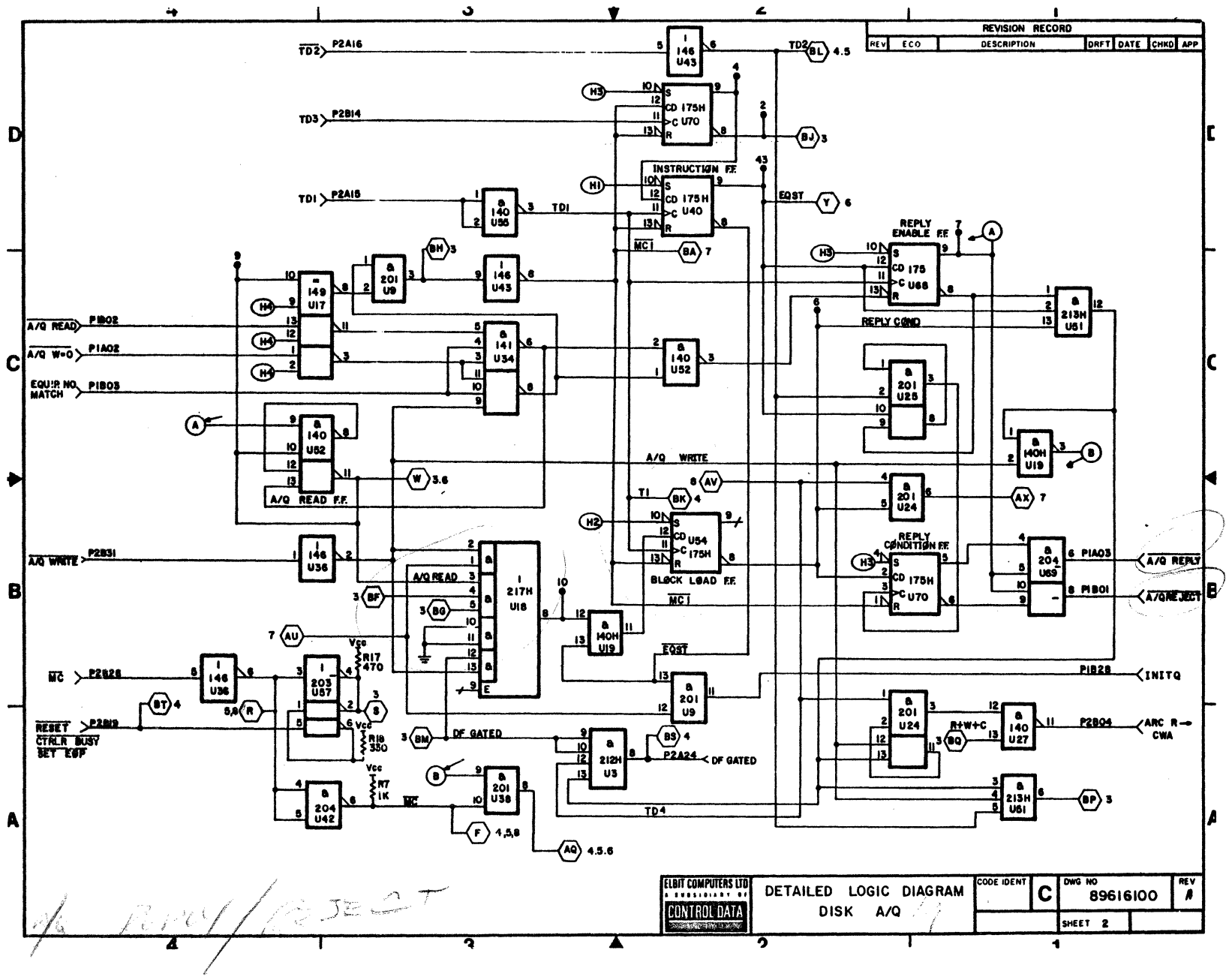
FIRST USED ON FA 716-A

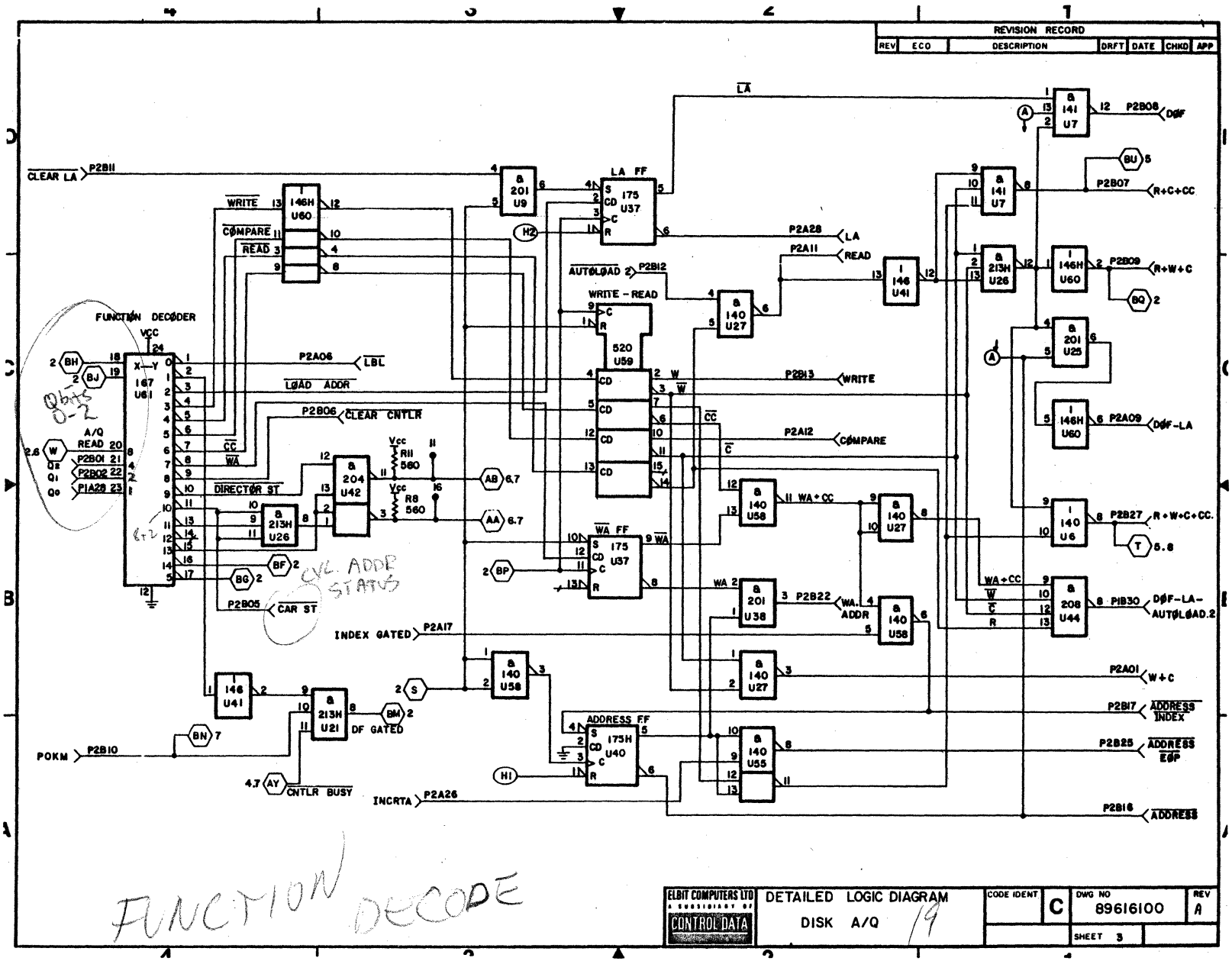
DWN	MIZRACHI. N	10.74
CHKD	M. Hanan	Oct 74
ENGR		
MFG	Wolf	
APPR		
Q.A.		

TITLE
DETAILED LOGIC DIAGRAM
DISK A/Q 19

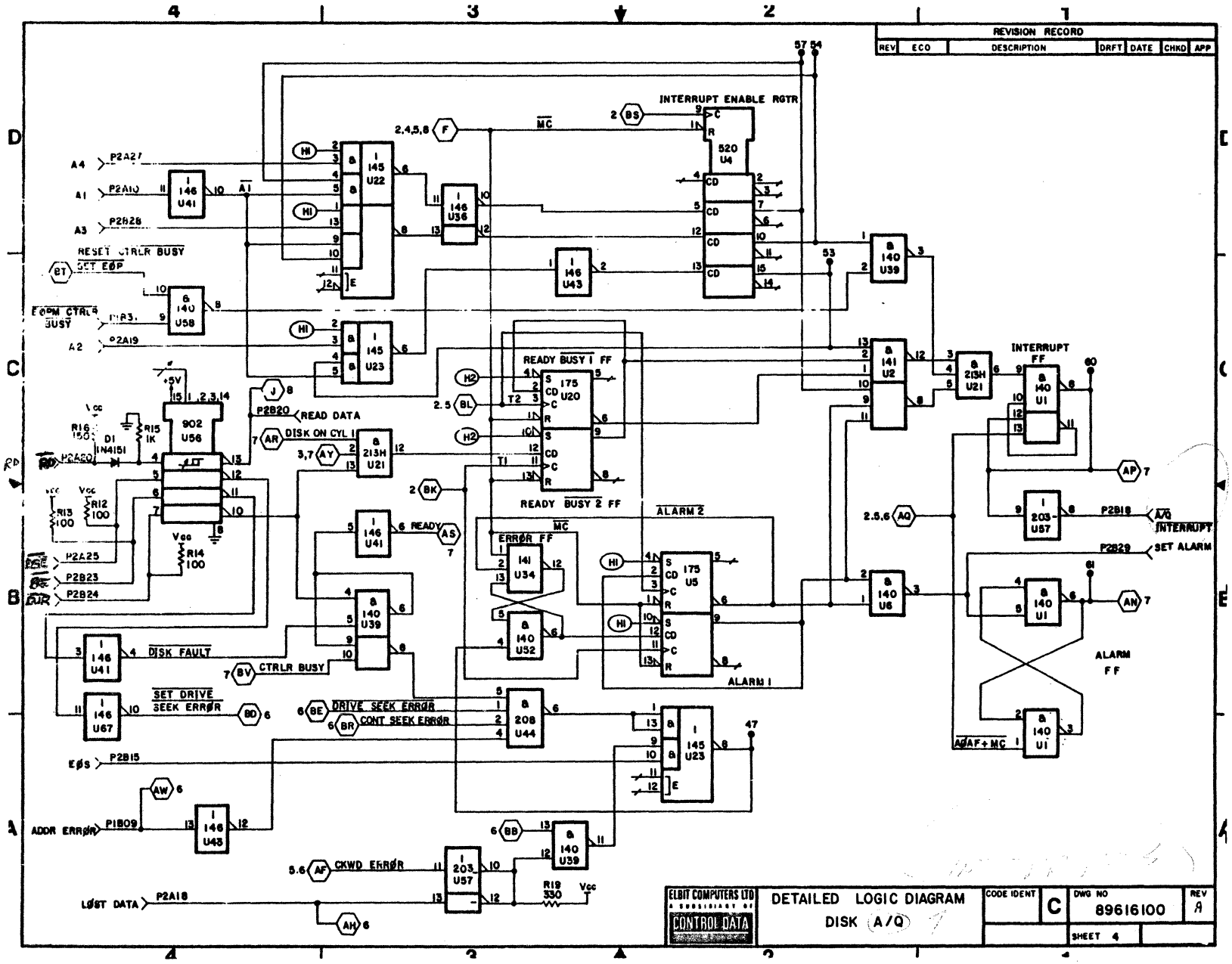
CODE IDENT	DRAWING NO
C	89616100

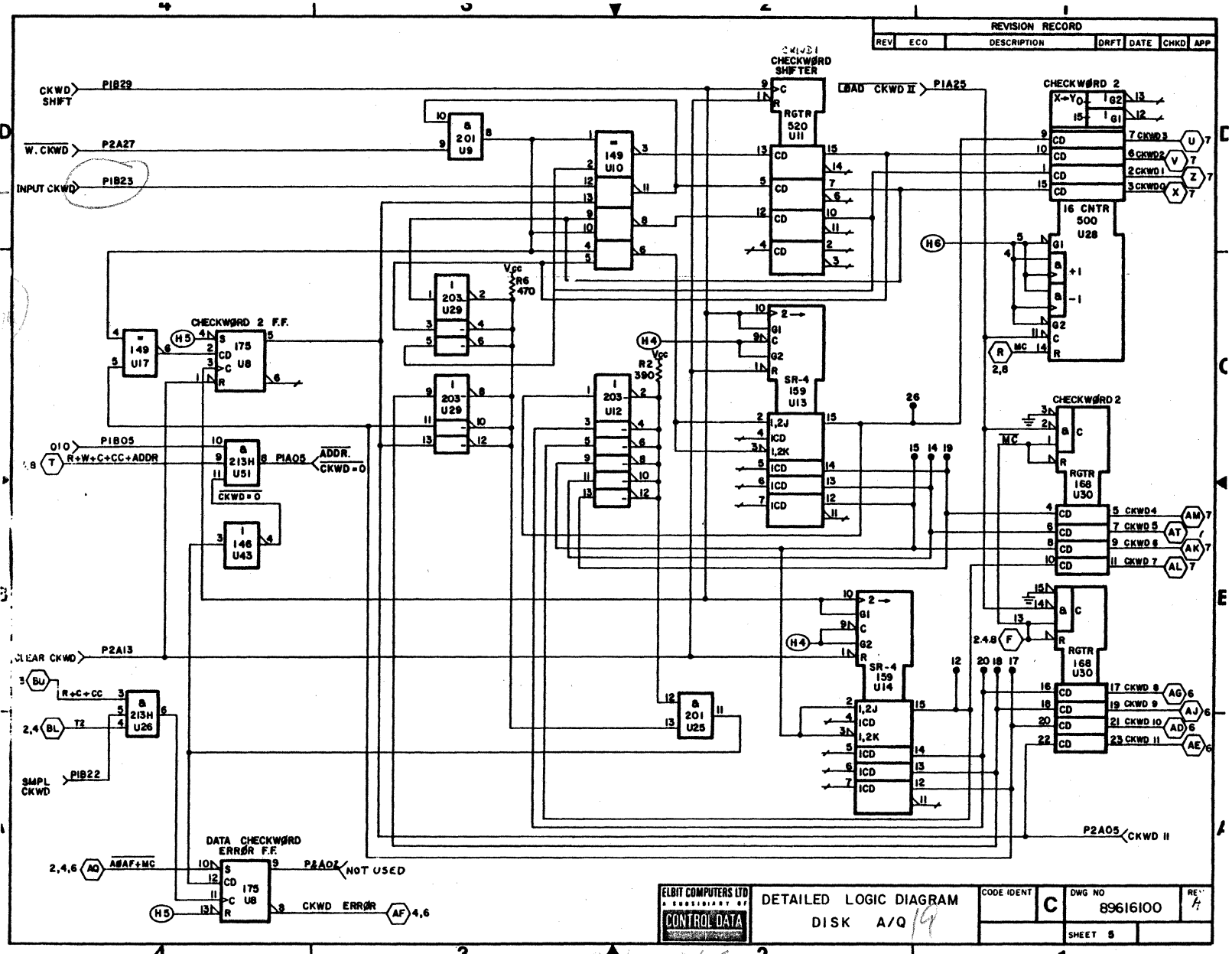
SCALE
SHEET 1 OF 8


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
TD2 P2A16
TD3 P2B14
TDI P2A15
A/Q READ P1B02
A/Q W=0 P1A02
EQUIP NO MATCH P1B03
A/Q WRITE P2B31
MC P2B26
RESET P2B19
CTRLR BUSY SET EOP
INSTRUCTION F.F.
REPLY ENABLE F.F.
REPLY COND
A/Q WRITE
A/Q READ F.F.
BLOCK LOAD F.F.
REPLY CONDITION F.F.
DF GATED
P2A24 DF GATED
R+W+C
P1B28 INITQ
P2B04 ARC R CWA
A/Q REPLY
A/Q REJECT
P1A03
P1B01
TD4
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK A/Q
CODE IDENT C
DWG NO 89616100
REV A
SHEET 2



FUNCTION DECODE

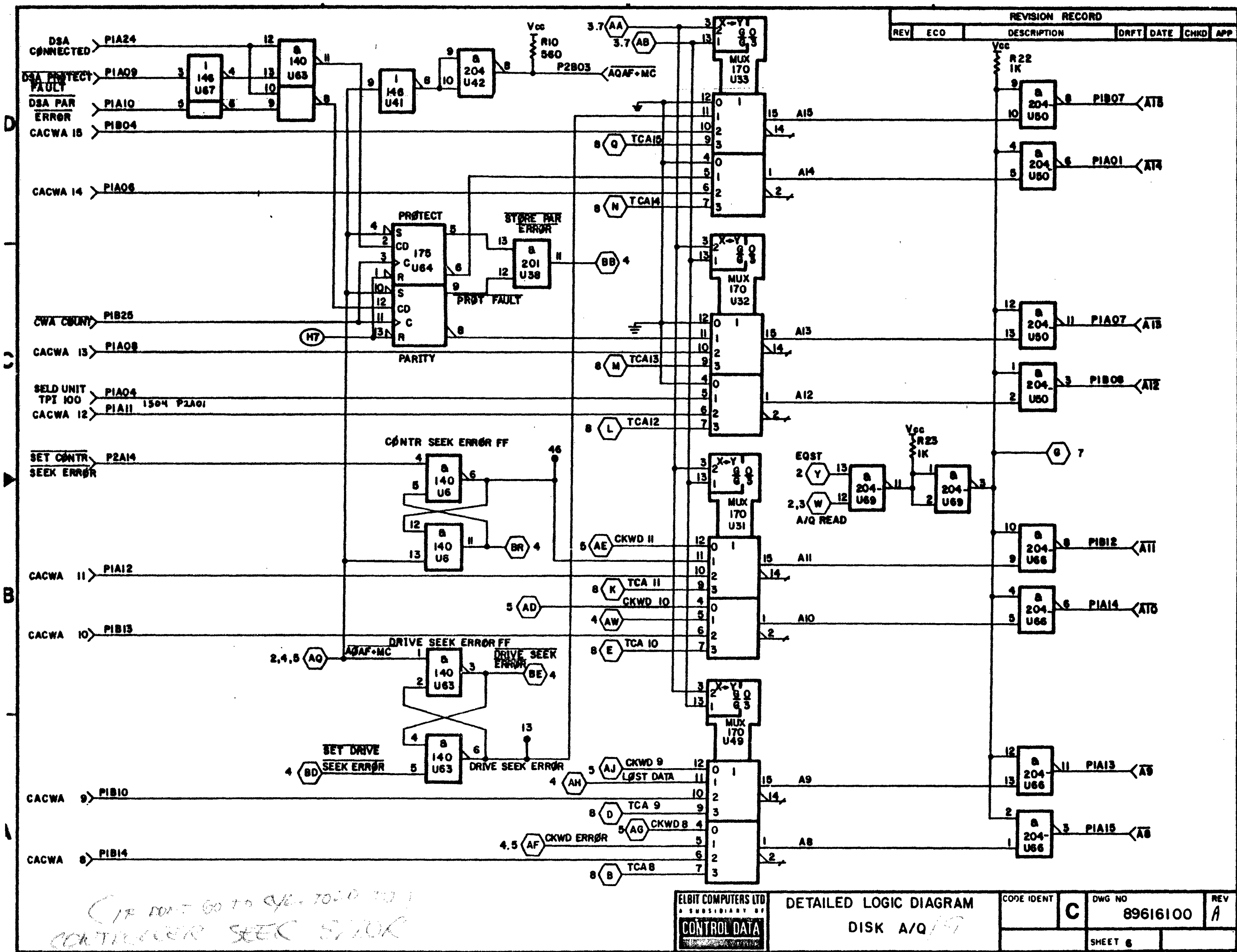

REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
INTERRUPT ENABLE RGTR
520 U4
READY BUSY 1 FF
READY BUSY 2 FF
ERROR FF
ALARM 2
ALARM 1
INTERRUPT FF
ALARM FF
READ DATA
DISK ON CYL 1
READY
DISK FAULT
CTRLR BUSY
SET DRIVE SEEK ERROR
DRIVE SEEK ERROR
CONT SEEK ERROR
ADDR ERROR
CKWD ERROR
LOST DATA
RESET CTRLR BUSY
SET EOP
INTERRUPT
SET ALARM
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK A/Q
CODE IDENT C
DWG NO 89616100
REV A
SHEET 4



data into checkword shifter (from checkword)

CHECKWORD check

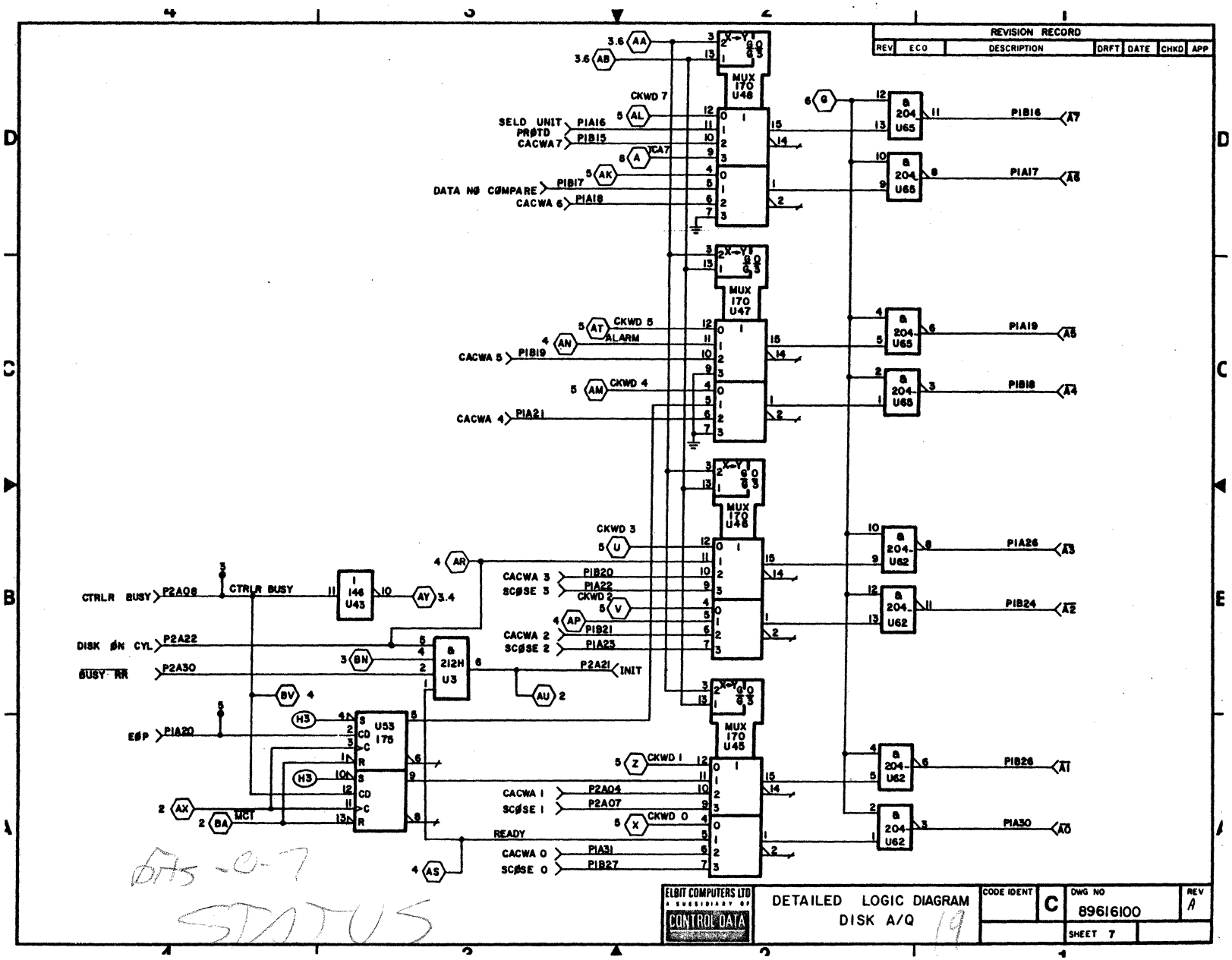
89638100 A

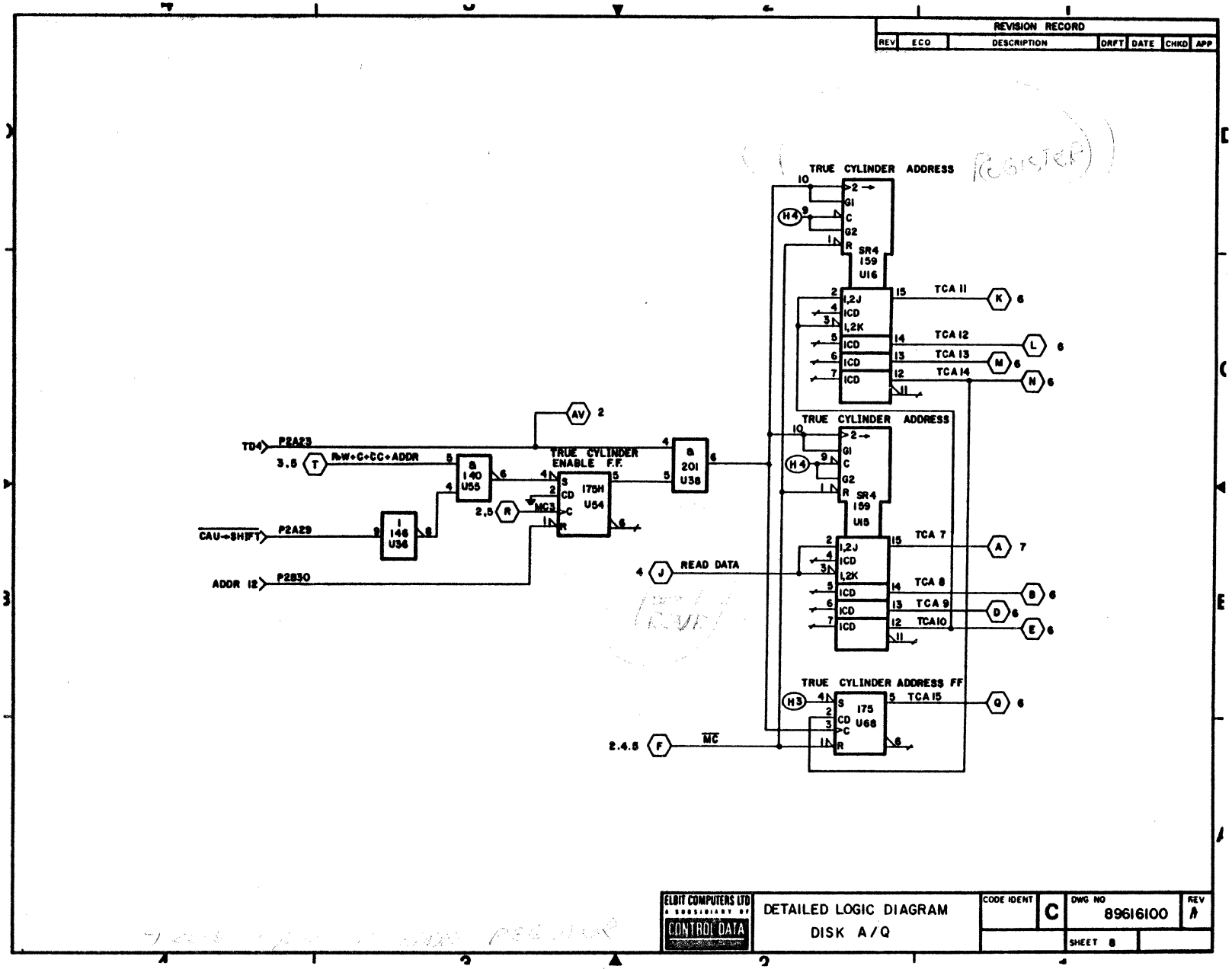


(IF DON'T GO TO CYC. 7050 TO 1
CONTROLLER SEEK ERROR
DRIVE SEEK ERROR
(OUT OF CYC.)

STATUS 8-15

5-37


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
MUX 170 U48
MUX 170 U47
MUX 170 U46
MUX 170 U45
CKWD 7
SELD UNIT PRØTD
CACWA 7
DATA NØ COMPARE
CACWA 6
CKWD 5 ALARM
CACWA 5
CKWD 4
CACWA 4
CKWD 3
CACWA 3
SCØSE 3
CKWD 2
CACWA 2
SCØSE 2
CKWD 1
CACWA 1
SCØSE 1
CKWD 0
CACWA 0
SCØSE 0
READY
CTRLR BUSY
DISK ØN CYL
BUSY RR
EØP
MCT
INIT
PIB16
PIA17
PIA19
PIB18
PIA26
PIB24
PIB26
PIA30
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK A/Q
CODE IDENT C
DWG NO 89616100
REV A
SHEET 7


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
TRUE CYLINDER ADDRESS
SR4 159 U16
TCA 11
TCA 12
TCA 13
TCA 14
TRUE CYLINDER ADDRESS
SR4 159 U15
TCA 7
TCA 8
TCA 9
TCA10
TRUE CYLINDER ADDRESS FF
175 U68
TCA 15
TRUE CYLINDER ENABLE F.F.
175H U54
8 140 U55
1 146 U36
8 201 U38
TD4 P2A23
R+W+C+CC+ADDR
CAU→SHIFT P2A29
ADDR 12 P2B30
READ DATA
MC
MC3
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK A/Q
CODE IDENT C
DWG NO 89616100
REV A
SHEET 8

OFF SHEET REFERENCE

OFF SHEET REFERENCE LETTER	SHEET LOCATION 2	3	4	5	6	7	8
A			C-4				B-2
B	C-4		C-3			C-2	
E	D-3	C-4	B-2	A-4			
F	C-4		B-3				
J	B-4	D-2	D-3				
L	A-2		D-3				
M	B-1		A-1	A-4	D-4		
N	D-2	C-4					
P	C-2	D-4					
Q	C-3	D-4					
S	B-2	C-2					
T	A-1	A-3					
W	C-3	C-3					
V	B-4		B-3			B-2	
Z	A-3	C-1					
AA				D-1		C-2	
AB				D-2		C-2	
AC				D-1		B-2	
AD				D-2		B-2	
AH				B-2		C-4	
AJ				B-2	B-2		
AK				C-2		B-4	
AL				B-2	A-2		
AM				C-2		C-4	
AN				C-2		C-4	
AP				B-2	A-2		
AQ				B-2		B-4	
AT					B-4		B-1
AW					A-4		B-1
AV					B-4		B-1
AX					A-2		B-1
AY					A-4		B-1
BA			B-4			C-2	
BB					A-2		B-2
BC					B-2		B-2
BD					B-2		B-2
BE						B-4	B-2
BG					C-4	C-4	
BH					C-4	C-4	
BJ		C-3				C-3	
BL		B-3				C-2	
BM		C-3				C-2	
BP		D-3	B-3			D-1	
BQ			B-1			C-4	
BS			A-4	A-3		C-4	
BT	C-3				C-4		
BU			A-4		D-2		
BW			A-4		D-2		

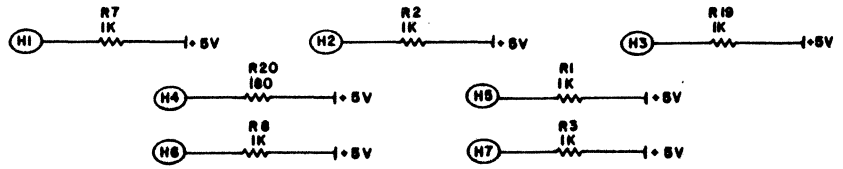
SHEET REVISION STATUS

1	2	3	4	5	6	7	8
08	08	06	01	06	06	08	06

REVISION RECORD

REV	ECO	DESCRIPTION	DRAFT	DATE	CHKD	APP
04	CK 448	REDRAWN TO SHEET CDC STD				
05	CK 427	LOGIC CHANGES FOR 89616800 REV 05				
06	CK 454	LOGIC FOR 89616801 REV 02.				
07	CK 589	LOGIC FOR 89778600 REV 01				
06	CK 649	DRAWING ERRORS SEE THE REVISION RECORD ON EACH SHEET USE ECO'S 454 AND 649 TO DRAW LOGIC REV 06		April 22, 74		
08	CK 712	CK 649 CHANGED TO REV 06		May 20, 74		
08	CK 1034	SH2, C-2, C-3: CONNECTION P2B14(T3)/U51-11 REPLACES U41-G/U51-11. USE ECO'S 712 AND 1034 FOR LOGIC REV 08.				

	2	3	4	5	6	7	8
CB	B-2			C-2			C-4
CD		D-1		A-1			C-4
CE			B-4		D-2		
CF			B-4		C-2		
CG			B-4		A-2		
CH			A-4		B-2		
CK			C-1			B-2	
CW	B-4	D-3					
DA			C-4				B-2
DB	B-2		B-3	B-2			B-2
DC					C-4		B-2
DD		D-2					C-3
DE	B-2	D-2					
DF	D-3				C-4		
DG		C-1		A-4			
DH					B-3	B-3	
DI		C-3				C-3	



NOTE: ALL RESISTORS ARE 0.25 WATT 5%

AY 89778600
AW 89616001
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

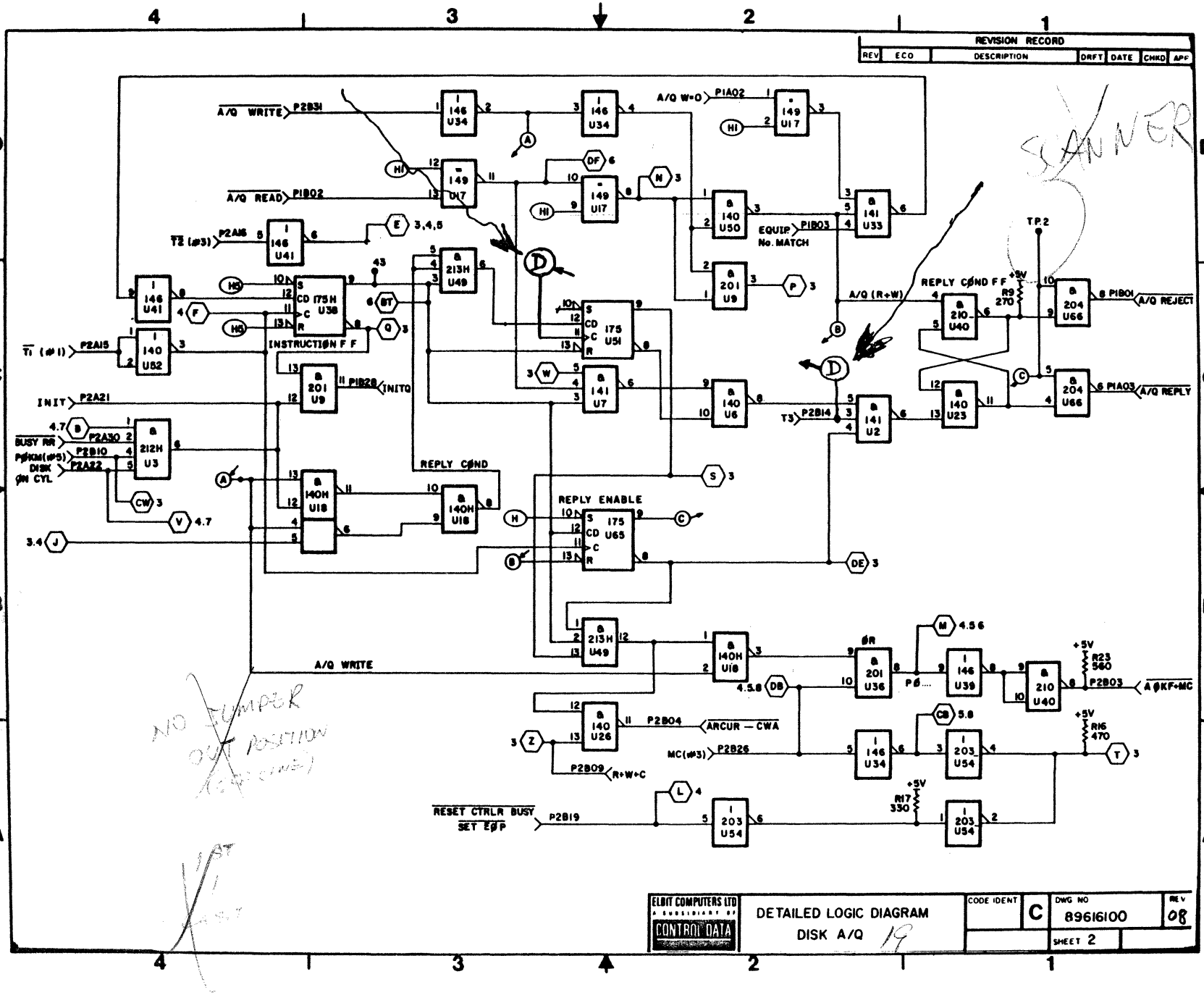
ELBIT COMPUTERS LTD
A SUBSIDIARY OF ELBIT

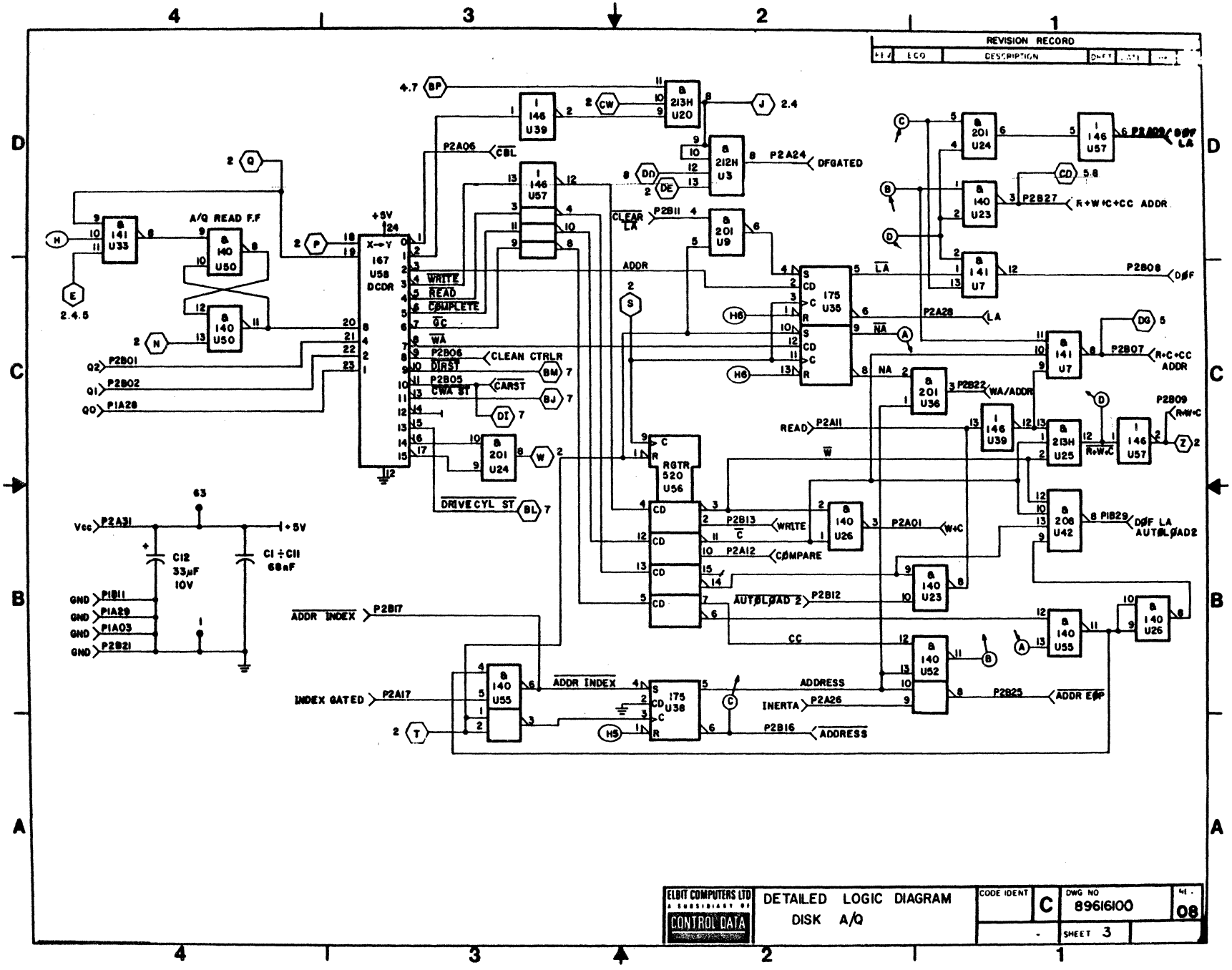
DWN	MIZRACHI N.	JAN. 8, 74
CHKD	DAVID A.	JAN. 8, 74
ENGR	AVIV G.	JAN. 8, 74
MFG		
APPR		

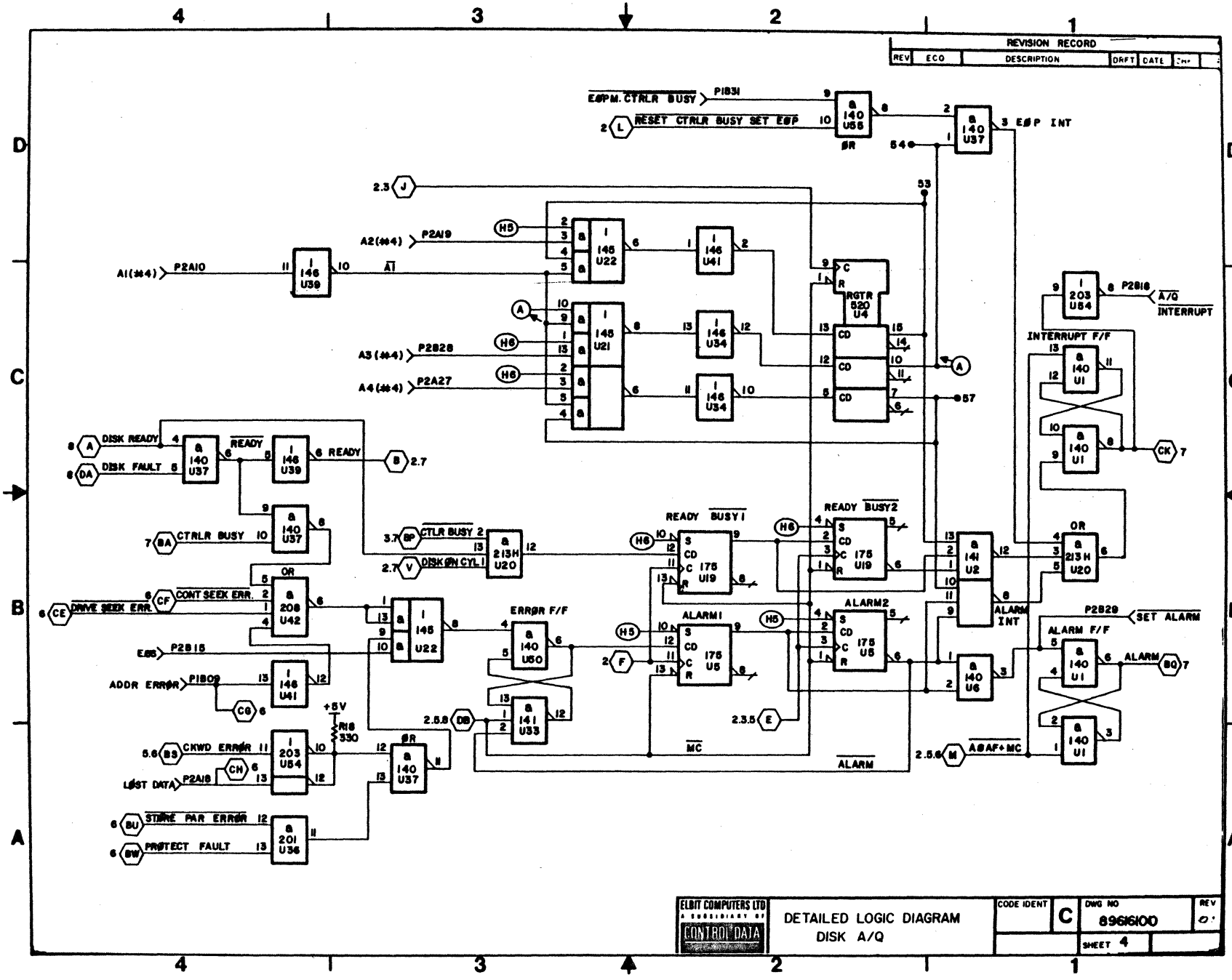
FIRST USED ON FA716-A

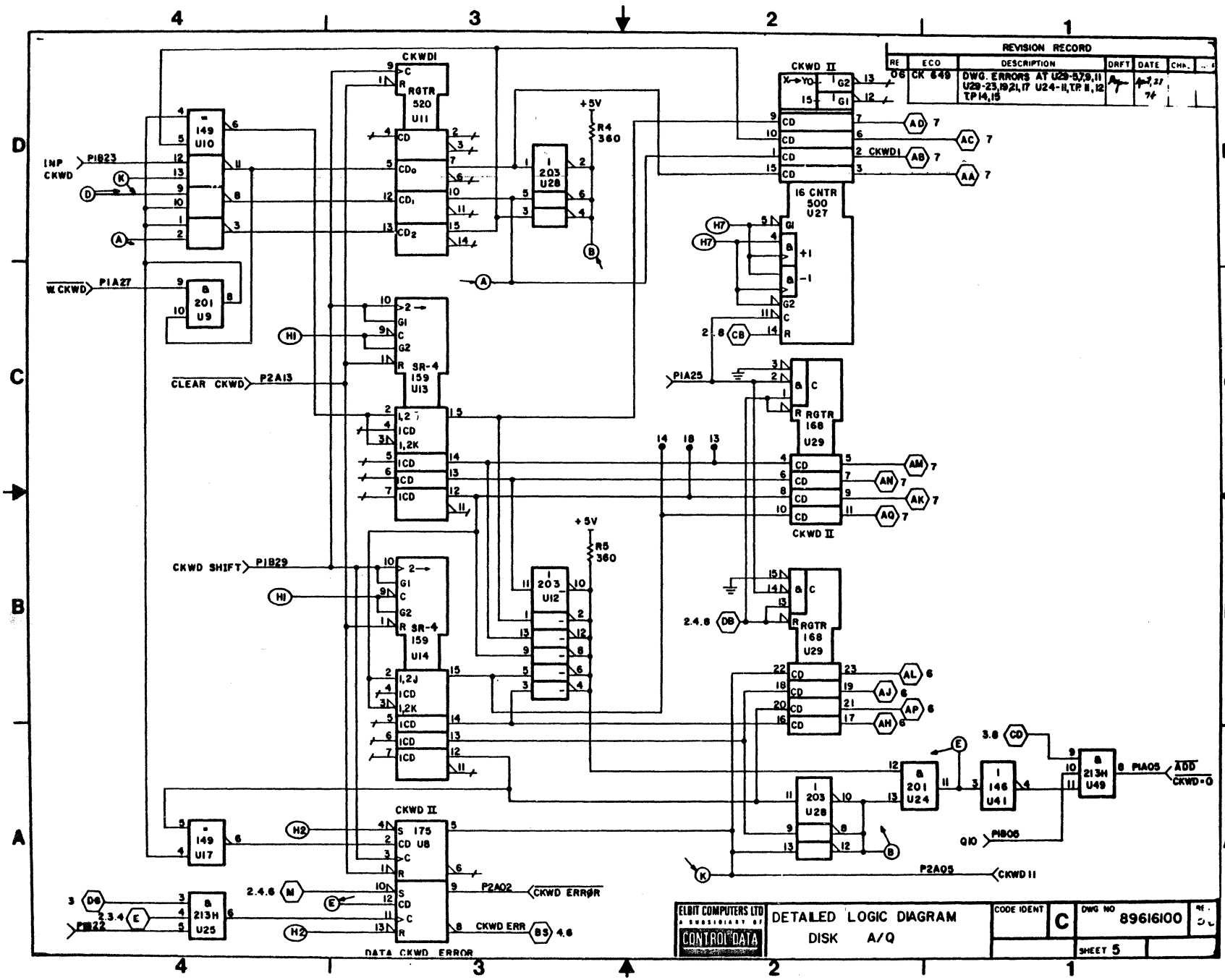
TITLE
DETAILED LOGIC DIAGRAM
DISK A/Q

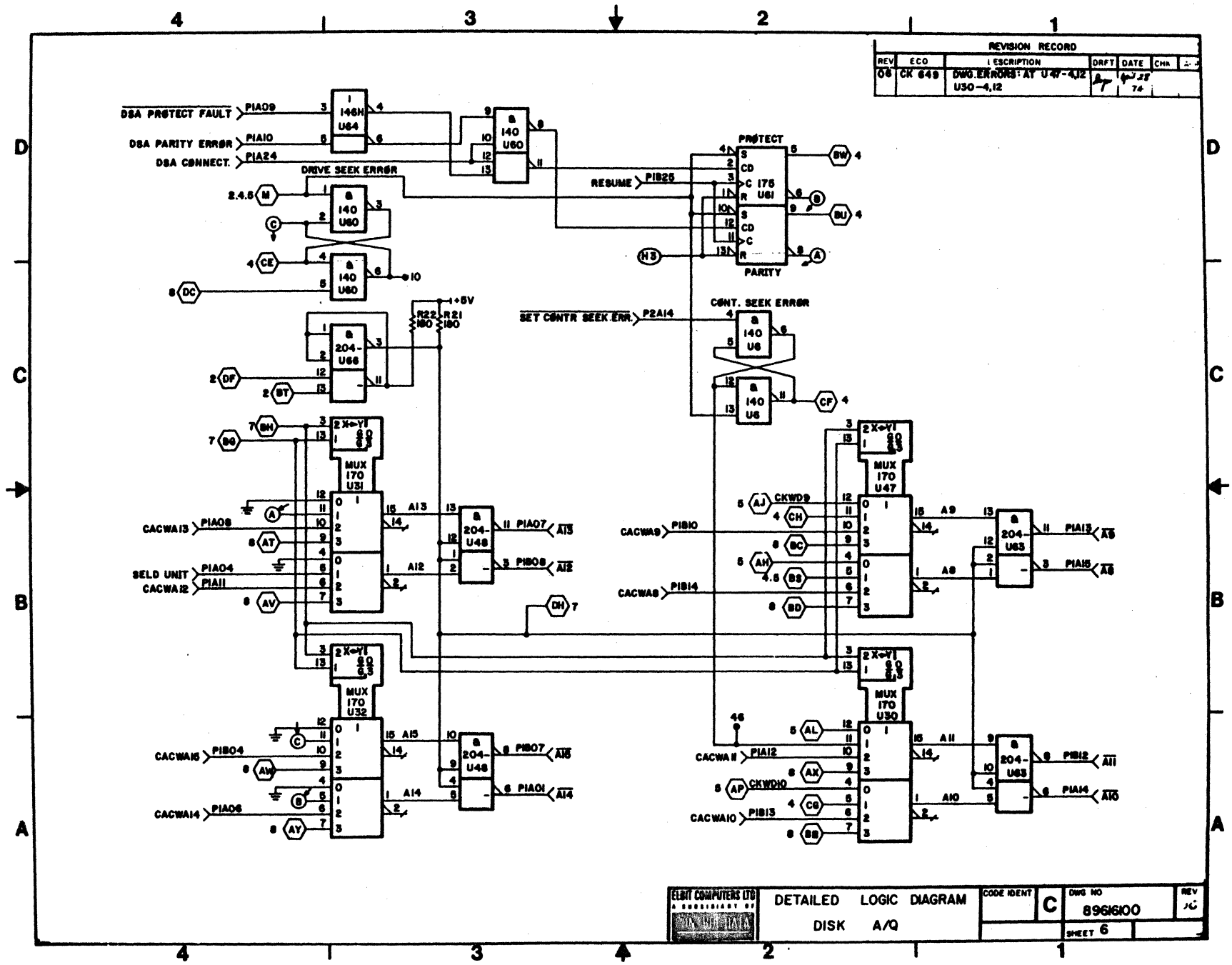
CODE IDENT: C
DRAWING NO: 89616100
SCALE
SHEET 1 OF 8

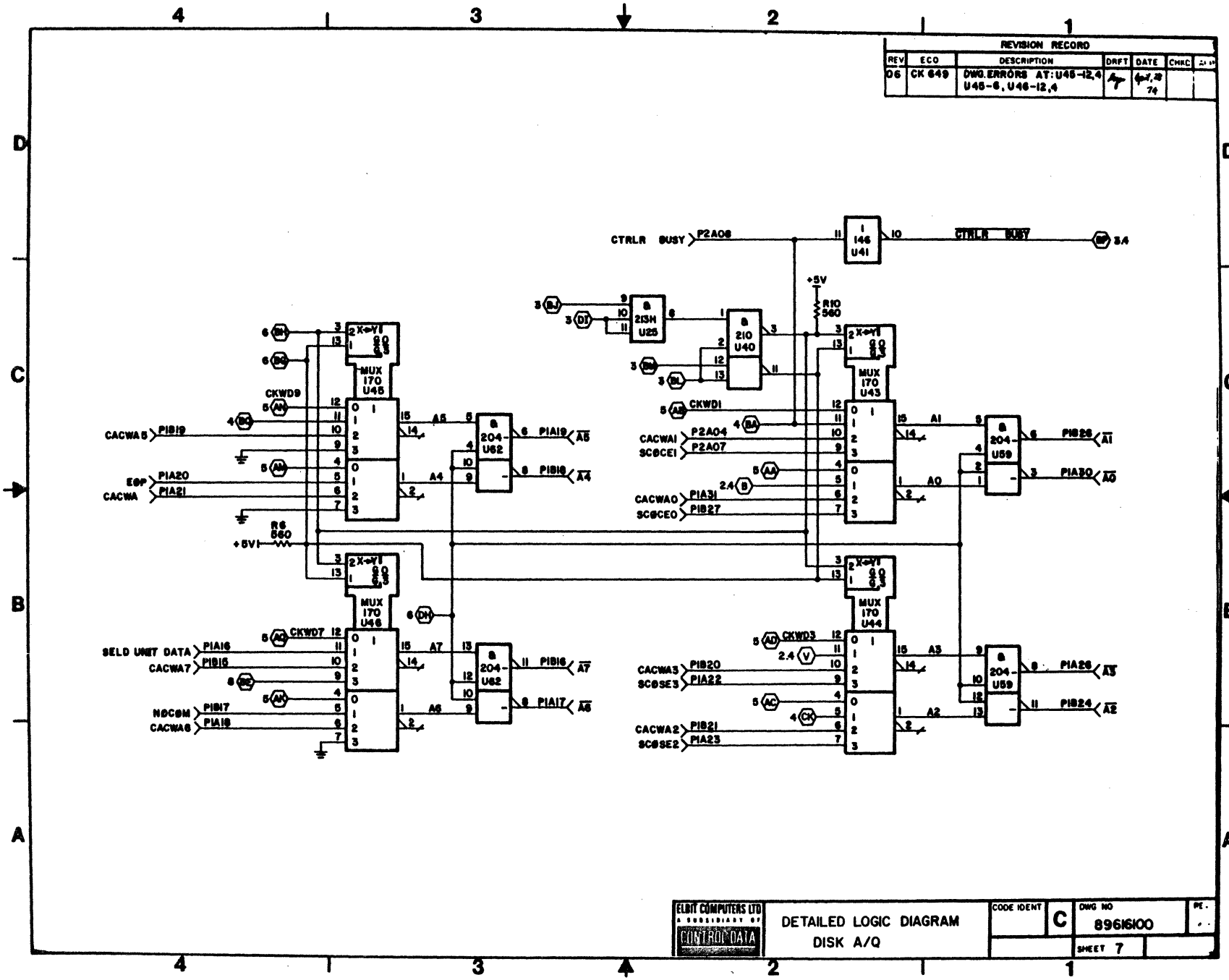

REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A/Q WRITE P2B31
A/Q READ P1B02
A/Q W=0 P1A02
A/Q (R+W)
EQUIP No. MATCH P1B03
REPLY COND F F
A/Q REJECT P1B01
A/Q REPLY P1A03
INSTRUCTION F F
INIT P2A21
INITQ P1B28
REPLY COND
REPLY ENABLE
T3 P2B14
BUSY RR P2A30
P2B10
DISK ON CYL P2A22
RESET CTRLR BUSY
SET EØP P2B19
MC(#3) P2B26
R+W+C P2B09
ARCUR — CWA P2B04
A ØKF+MC P2B03
TP.2
SCANNER
NO JUMPER OUT POSITION
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK A/Q
CODE IDENT C
DWG NO 89616100
REV 08
SHEET 2

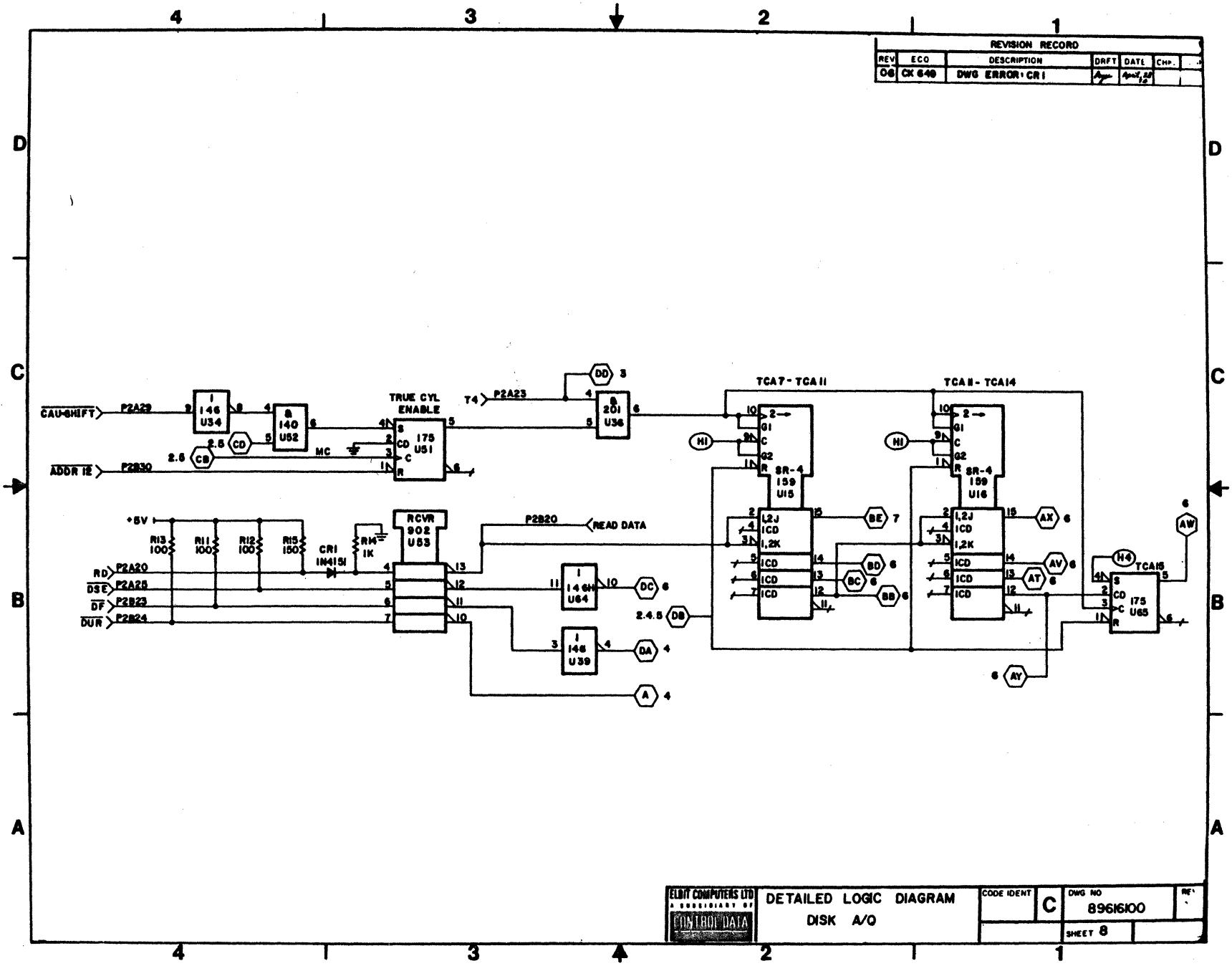

REVISION RECORD
ECO
DESCRIPTION
A/Q READ F.F
+5V
WRITE
READ
COMPLETE
WA
CLEAN CTRLR
CARST
DRIVE CYL ST
ADDR
CLEAR LA
DFGATED
READ
WRITE
COMPARE
ADDR INDEX
INDEX GATED
INERTA
ADDRESS
CC
RGTR 520 U56
DCDR
C12 33µF 10V
C1 ÷ C11 68nF
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK A/Q
CODE IDENT
C
DWG NO
89616100
SHEET 3
08


REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
E&PM. CTRLR BUSY
RESET CTRLR BUSY SET E&P
E&P INT
A1(##4)
P2A10
A2(##4)
P2A19
A3(##4)
P2B28
A4(##4)
P2A27
DISK READY
DISK FAULT
READY
CTRLR BUSY
CONT SEEK ERR.
DRIVE SEEK ERR.
P2B15
ADDR ERR&R
CKWD ERR&R
LOST DATA
STORE PAR ERR&R
PROTECT FAULT
CTLR BUSY 2
DISK ON CYL !
ERR&R F/F
READY BUSY1
READY BUSY2
ALARM1
ALARM2
ALARM INT
INTERRUPT F/F
A/Q INTERRUPT
ALARM F/F
SET ALARM
ALARM
A&AF+MC
OR
+5V
R18 330
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK A/Q
CODE IDENT
C
DWG NO
89616100
REV
SHEET 4


REVISION RECORD
RE | ECO | DESCRIPTION | DRFT | DATE | CHK
06 | CK 649 | DWG. ERRORS AT U29-5,7,9,11 U29-23,19,21,17 U24-11, TP 11, 12 TP 14, 15
CKWDI
RGTR 520 U11
149 U10
INP CKWD
P1B23
W CKWD
P1A27
201 U9
SR-4 159 U13
CLEAR CKWD
P2A13
SR-4 159 U14
CKWD SHIFT
P1B29
149 U17
213H U25
P1B22
CKWD II
S 175 CD U8
DATA CKWD ERROR
CKWD ERROR
P2A02
CKWD ERR
203 U28
R4 360
203 U12
R5 360
16 CNTR 500 U27
RGTR 168 U29
CKWD II
201 U24
146 U41
213H U49
P1A05
ADD
CKWD=0
P1B06
Q10
P2A05
CKWD II
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK A/Q
CODE IDENT C
DWG NO 89616100
SHEET 5


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHK
08 CK 649 DWG.ERRORS: AT U47-4,12 U30-4,12
DSA PROTECT FAULT PIA09
DSA PARITY ERROR PIA10
DSA CONNECT. PIA24
DRIVE SEEK ERROR
RESUME PIB25
PROTECT
PARITY
CONT. SEEK ERROR
SET CONTR SEEK ERR. P2A14
+5V
R22 180 R21 180
MUX 170 U31
MUX 170 U47
MUX 170 U32
MUX 170 U30
CACWA13 PIA08
SELD UNIT PIA04
CACWA12 PIA11
CACWA9 PIB10
CACWA8 PIB14
CACWA15 PIB04
CACWA14 PIA06
CACWA11 PIA12
CACWA10 PIB13
CKWD9
CKWD10
DIAGRAM
DISK A/Q
CODE IDENT C
DWG NO 8966100
SHEET 6


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD
06 CK 649 DWG. ERRORS AT: U45-12,4 U45-6, U46-12,4
CTRLR BUSY P2A08
MUX 170 U45
MUX 170 U46
MUX 170 U43
MUX 170 U44
CACWA5 PIB19
EOP PIA20
CACWA PIA21
SELD UNIT DATA PIA16
CACWA7 PIB15
NOCOM PIB17
CACWA6 PIA19
CACWAI P2A04
SCOCEI P2A07
CACWAO PIA31
SCOCEO PIB27
CACWA3 PIB20
SCOSE3 PIA22
CACWA2 PIB21
SCOSE2 PIA23
+5V
R6 560
R10 560
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK A/Q
CODE IDENT C
DWG NO 89616100
SHEET 7


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHK.
08 CK 648 DWG ERROR: CR1
CAU-SHIFT P2A29
ADDR 12 P2B30
TRUE CYL ENABLE
T4 P2A23
TCA7 - TCA11
TCA11 - TCA14
HI
MC
+5V
R13 100
R11 100
R12 100
R15 150
CR1 IN4151
RM 1K
RCVR 902 U53
RD P2A20
DSE P2A28
DF P2B23
DUR P2B24
P2B20 READ DATA
2.4.5 DB
TCA15
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK A/Q
CODE IDENT C
DWG NO 89616100
SHEET 8

DSA PW BOARD (Logic Diagram 89617300, Sheets 1-8).

The DSA Card is divided into the following functional parts:

1. Scanner
2. Request/Resume
3. Double Buffer Control
4. Clock Generation
5. Load Address and Track Address Strobe
6. Controller Busy/EOP
7. Autoload
8. CDD Interface
9. Controller Seek Error Detection
10. Sector and Index Gated Generation
11. Master Clear

Scanner (SHEET 2)

The SCAN FF U63-11 and 8 represents one stage of the distributed scanner. The appropriate jumper is inserted to indicate the controller's position relative to the other controllers attached to the DSA.

The stages of the scanner are attached such that the setting and resetting of one causes the setting and resetting of the next, except for the first to middle stage connection. In this case, the setting of the first causes the resetting of the middle. The resetting of the first, causes the setting of the middle. This setup results in a Scan pulse being transmitted from one stage to the next. The jumpers determine from which direction a given stage will receive the pulse and to which direction it will transmit the pulse.

When the controller wishes to send or receive data, the NEED FF is set. Upon the next setting of the SCAN FF, the HALT FF is set to prevent the resetting of the SCAN FF. The REQUEST FF is set on the next transition of the scanner pulse. When the RESUME is received from the DSA Channel, the HALT FF is reset and the scanner oscillation is allowed to continue.

Request/Resume (SHEET 2)

For each word of Read or Write Data to be transmitted, the controller sets the NEED FF via the $\overline{\text{SET NEED}}$ signal. After the scanner is Halted and captured, the REQUEST FF is set. The setting of the REQUEST FF generates the $\overline{\text{DSA REQUEST}}$ signal to the computer, and in the case of a Read instruction, if the RESUME from the previous memory cycle is inactive, also sets the WRITE ENABLE FF.

The WRITE ENABLE FF causes the generation of the $\overline{\text{DSA WRITE ENABLE}}$ signal to the computer. Upon receipt of the $\overline{\text{DSA RESUME}}$ signal, the DSA CONNECTED FF is set and the NEED FF is reset. The DSA CONNECTED FF is reset by the trailing edge of the RESUME signal. The WRITE ENABLE FF is Reset by the resetting of DSA CONNECTED.

The $\overline{\text{DSA PROG. PROT.}}$ signal is active during a write to the computer when the ULT. SOURCE PROT'd (Ultimate Source Protected) FF on the disk daisy chain has been previously set.

Double Buffer Control (SHEET 3)

During Write or Compare instruction, the BUFF 1 FULL FF is set by the trailing edge of the $\overline{\text{DSA}\rightarrow\text{BUFF 1}}$ signal. If the BUFF 2 FULL FF is not set, the BUFF 1 → BUFF 2 will be set at the next T1. The output of this FF allows the transfer of data from BUFFER 1 to BUFFER 2 on Disk, Shifter. The setting of BUFF 1 → BUFF 2 allows the resetting of BUFF 1 FULL and the setting of BUFF 2 FULL at T2. At the T3 the BUFF 1 → BUFF 2 FF is reset.

The BUFF 2 FULL FF (SHEET 3) is reset when the data is transferred from the BUFFER 2 to the shifter when the signal 16 BITS .011 (from Disk Sector Count) becomes active.

During a Read instruction the BUFF 1 FULL FF is set when data is transferred from the shifter to the BUFFER 1 by the $\overline{\text{SHIFT} \rightarrow \text{BUFF 1}}$ signal. The BUFF 1 → BUFF 2 FF is set and cleared as in Write and Compare operations. The BUFF 2 FULL FF is set by the BUFF 1 → BUFF 2 signal and cleared after data is transferred to the DSA at the trailing edge of the $\overline{\text{DSA CONNECTED}}$ signal.

During Write or Compare operations the LOST DATA FF will be set if BUFF 2 FULL is not set at the time that the 16 BITS .011 signal becomes active and neither $\overline{\text{BL = 0}}$ nor $\overline{\text{INHIBIT NEED}}$ is active. During a Read operation the LOST DATA FF will be set if the BUFF 1 FULL FF is set at the time that the $\overline{\text{SHIFTER} \rightarrow \text{BUFF 1}}$ signal becomes active. In all cases the LOST DATA FF is reset by the $\overline{\text{AØAF+MC}}$ signal

The $\overline{\text{DSA PRIORITY}}$ signal is active in the 011 field if during a Read, both BUFF 1 FULL and BUFF 2 FULL are set or, during a Write or Compare, both BUFF 1 FULL and BUFF 2 FULL are reset.

The signals SMPXS1 and SMPXS0 are used on Disk, Shifter, to control the multiplexer at the parallel input to the shifter. These signals depend on the states of the $\overline{\text{CAL} \rightarrow \text{SHIFTER}}$ and $\overline{\text{CAU} \rightarrow \text{SHIFTER}}$ (from Disk, Sector Count) and the output of the 140H at U12-8 (on SHEET 4).

Clock Generation (SHEET 4)

The Clock Generation logic produces a four phase clock, 100 ns per phase. When writing to the disk (i.e. Read Gate is not active) the 20 MHz oscillator is the source of the clock. The 20 MHz signal is divided in half by the JØHN0 FF. The output from the JØHN0 FF is fed to the clock input of JØHN1 and JØHN2. These two FF's are connected such that the output of JOHN1 is a square wave with a 400 ns period; the output of JOHN2 is the same square wave, 100 ns out of phase with the first. The combinational logic then selects the proper portions of the two square waves to produce the required clock pulses. The 242H's are in parallel for drive purposes.

During Read operations (i.e. $\overline{\text{READ GATE}}$ active) the source of the clock is the VCO output (nominally 10 MHz) synchronized with the READ CLOCK This signal is fed to the clock inputs of JØHN1 and JØHN2, which results in the required clock pulses.

Load Address and Track Address Strobe (SHEET 4)

The FF LA1 is set at the leading edge of T_3 after the LA signal (from A/Q card) becomes active. LA2 is set 400 ns later at the next T_3. The signal $\overline{\text{ARCVR} \rightarrow \text{CA}}$ will thus be active at the T_4, after the T_3 on which LA1 was set if $\overline{\text{ADDR. ERROR}}$ is not active. At T_2, the Track Address Strobe Counter (TAS Counter) will be loaded with the count 1110_2 and the INHIBIT COUNTER FF will be reset. Thereafter the TAS counter will be decremented by one at the trailing edge of each T_4. When the count equals 1001_2 the INHIBIT COUNTER FF is set and the decrementing of the TAS counter is blocked. Thus, the signal TAS INT is active from count 1110 to count 0111, (i.e., for 1.9 µsec). The signal TAS EXT.is active from count 1110 to count 1011, (i.e., for 1.1 µsec).

The signal LAEØP (sheet 5) is generated to indicate the end of the controller's portion of a seek operation initiated by an LA instruction. The FF LAEØP1 (SHEET 7) is set in the normal case when the signal ON CYL. drops after the Disk File receives the new track address. In the case where the new track

address equals the old track address, the ON CYL does not drop and the LAEØP1 FF will be set by the trailing edge of the TAS INT. signal. In both cases the FF LAEØP2 will be set at the leading edge of the following T_3. The setting of LAEØP2 causes the reset of LAEØP1. The $\overline{\text{LA DIFF = 0 CLEAR BUSY M}}$ is active when the LAEØP2 FF is set and the ON CYL signal has remained active.

Controller Busy/EOP (SHEET 5)

The CTRLR BUSY FF is set at the first T_1 after the initiation of Read (not including Autoload), Write, Compare, Check Word Check and Write Address instructions. The FF remains set until the operation ends (normally or abnormally). The normal end to Read, Write and Compare operation is at SECTOR GATED•BL= 0. The end of WA and CC operations is indicated by the $\overline{\text{ADDRESS EØP}}$ signal becoming active. Abnormal terminations are indicated by the $\overline{\text{SET ALARM}}$ signal. The same conditions that reset the CTRLR BUSY FF set the CTRLR EØP FF. The output of the CTRLR EØP FF is ORed with the $\overline{\text{EØPM·NOT CTRLR BUSY}}$ signal to yield the EØP STATUS signal. The end of the controller portion of an LA instruction is indicated by the LAEØP signal. $\overline{\text{CLEAR LA}}$ causes the resetting of LA FF on the A/Q card. An abnormal end to a seek operation causes the resetting of the appropriate UNIT BUSY FF on the Daisy Chain card, via the $\overline{\text{RESET CTRLR BUSY}}$ signal.

Autoload (SHEET 5)

The depression of the Remote Autoload signal causes the generation of the $\overline{\text{REMOTE AUTOLOAD}}$ pulse. The trailing edge of this pulse causes the Trailing Edge Detector (TED) FF (SHEET 5) to set. At the next T_1 the AUTOLOAD 1 FF will set. At the detection of the INDEX GATED and ON CYL signals AUTOLOAD 2 will set. Between the setting of AUTOLOAD 1 and AUTOLOAD 2 and START AUTOLOAD signal (U54-8 on SHEET 5) will cause the generation of MASTER CLEAR to the

controller and a RTZS (U19-5 on Sheet 8) to the drive. The setting of AUTOLOAD 2 (SHEET 5) clears the TRAILING EDGE DETECTOR FF. AUTOLOAD 1 is cleared at the next T_1. The AUTOLOAD 2 FF remains until the end of the track being read is indicated by the INCRTA signal.

CDD Interface (SHEET 6,7)

Sixteen signals are transmitted from the controller to the disk driver via the 180 transmitter. Four signals are received from the disk drives by the 902 receivers. In addition, the remaining signals in the CDD/Controller interface are passed via 12 pins on connector P2, with no connection to the DSA board itself. Finally, the presence of controller power is indicated by the Terminator Monitor signal which is simply connected to +5V via a 100Ω resistor on the board.

Controller Seek Error Detection (SHEET 7)

The Controller indicates a seek error if, during Read, Write, Compare or Checkword Check operations, three revolutions of the disk occur without an EØS (End of Sector) signal being detected. The first INDEX GATED sets the REV 1 FF. The second INDEX GATED clears the REV 1 FF which sets the REV 2 FF. The third INDEX GATED sets the REV 1 FF again. The presence of REV 1 and REV 1 and REV 2 set and the INDEX GATED signal cause the generation of the $\overline{\text{SET CONT SEEK ERROR}}$ signal. The presence of the EØS signal inhibits the counting by resetting the REV 1 and REV 2 FF's.

Sector and Index Gated Generation (SHEET 7)

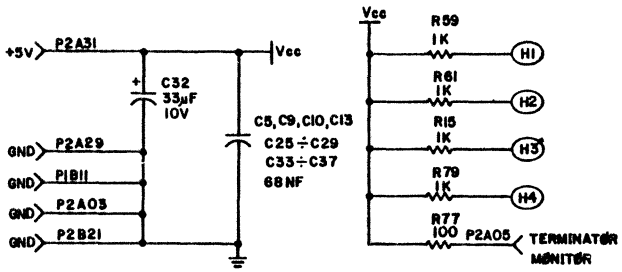
A three hundred nanosecond pulse is generated upon the detection of both the Index Mark and each of the Sector Marks. The SECTOR MARK 1 FF sets at the first T_2 after the sector and ON CYL signals become active. The SECTOR MARK FF sets at the next T_1. Between the setting of SECTOR MARK 1 and 2 the SECTOR GATED signal is active. The INDEX GATED signal is generated in an identical manner.

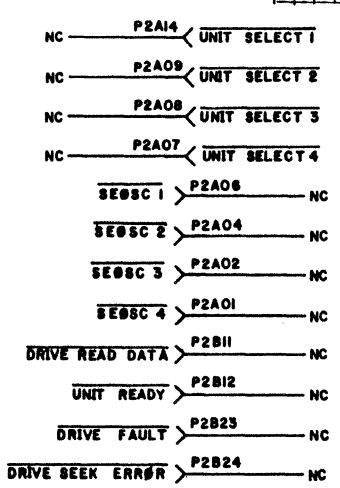
Master Clear

The Master Clear signal is generated by the presence of any of the $\overline{\text{CLEAR CTRLR}}$, $\overline{\text{AQMC}}$, or $\overline{\text{START AUTOLOAD}}$ signals. The $\overline{\text{CLEAR CTRLR}}$ and $\overline{\text{START AUTOLOAD}}$ also cause the generation of the $\overline{\text{RTZS}}$ signal.

ØFFSHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SIGNALS	SHEET LØCATIØN						
		2	3	4	5	6	7	8
A	READ	B-4	C-4					
B		A-2	D-3					
D	DSA CØNNECTED	B-2▼	C-4					
E	MC	A-3	C-4	B-4	B-1▼		C-3	
F	TD2		C-4▼	C-2			B-3	
G	BL=0		D-4		D-4			
J	TD3		D-3	C-3▼				
K	TD1		C-2	B-3▼				
L	ØØAF+MC		C-1		C-3		D-3	
M				D-4		A-1▼		
N	LA			B-4	D-3		A-2	
Q	INCRTA			A-4	B-3			
R	READ GATE					A-4		B-4
S	READ CLOCK			D-2			B-3▼	
T	MC			A-2	B-1▼			
U	TAS INT			B-1▼			A-3	
V	SECTØR GATED				D-4		C-1▼	
W	LAEØP				D-3		B-1▼	
X	ØNCYL				C-3		C-3▼	
Y	INØEX GATED				C-3		D-1▼	
Z	RTZS 2				B-1▼	B-4		
AA	A/Q MC			D-4	A-1▼		B-3	C-4
AB	TASTRØREEXT			A-2▼		B-4		
AC	DSA CØNNECTED	B-1	D-3					
AD	TD1			B-3▼	B-3		B-3	
AE				D-4▼			B-3	C-4
AF	TD3		C-3	C-3▼			A-2	
AG				C-4				D-1▼
AJ				C-1▼				C-4
AK		A-3	C-4					
AL			C-4		C-3			





NØTES:

1. ALL RESISTØRS ARE 0.25 WATT 5%
2. SYMBØL NC MEANS "NØT CØNNECTED TØ PRINTED CIRCUIT".
3. ▼ - DENØTES SIGNAL ØRIGIN.

SHEET REVISION STATUS

1	2	3	4	5	6	7	8
03	03	03	03	03	03	03	
04	04	04	04	04	04	04	
05	05	04	05	05	05	04	
06	06	06					06
07							
08	08	08					
09							
10	10	10		10			
11	10	11	11	11	04	11	11
A	A	A	A	A	A	A	A
B	A	B	B	B	B	B	A
C	C	C	B	C	B	B	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
03	CK432	REDRAWN PER CDC STD	DAYAN	8 JAN 74		
04	CK 149	LOGIC CHANGES FOR PWB REV. 05	Ayer	3-8-74		
05	CK 513	CONNECTION U26-10 TO U52-2 ADDED. U2 WAS TYPE 213H	Ayer	3-8-74		
06	CK 580	REVISED: GATE ADDED U58. U8 REPLACED BY NEW LOGIC. NEW SHEET 8 ADDED	Ayer	March 14, 74		
07	——	NOT USED				
08	CK 680	SH 3, C-2: PIA17 (T2) REPLACES U18-2 AT U14-6 TO IMPROVE SET ØF "LØST DATA" FF SH 4, D-4: ADME REPLACES MC AT U55-1, U6-8, U8-7 SH. 8, C-4: ADME REPLACES ME AT U8-A6; U8-A6; U26-8, U14-8 FITS ASSY 89964000 REV. 05	Ayer	13/74		
09		NOT USED				
10	CK 994	DWG ERRORS CORRECTED SHEETS 1,2,3,5 CORRECTS LOGIC REV. 09	Ayer	Oct, 74		
11	CK 971	CORRECTS REV. 08 RECORD SH. 5, B-1: GATE U48-8 ADDED. U48-8 REPLACES U44-11 AT UG5-10. FITS ASSY 89864000 REV. 01	Ayer	Dec, 23 74		
A	CK 1114	RELEASED CLASS A USES PWB 89838000 REV. 01	M.L.	4.5.75	M.M.	
B	CK 1407	SH. 5, A-D, U62-11 WAS SHIFT—SHIFT SH. 4, B-B U20-12 WAS TD1 SH. 4, B-B, U20-13 WAS TD1 SH. 8, B-C, U24-1 WAS ØØAF+MC SH. 8, E-D, U24-9 WAS SYNCH BUSY SH. 8, 4-B, U58-13 TA STROBE EXT U58-10 WAS ——+TS SH. 7, B-C U58-10 BAR	MONY	11.11.75		
C	CK 1432	SH 2: U46-1 WAS CONNECTED TO (E), ADDED (AK), ZONE A-3. SH 3: GATES U42-1,2,3 ADDED. U46-12 WAS CONNECTED TO (E). ADDED (AK), ZONE C-4. SH 5: ADDED (AL), ZONE C-3.	Ione	Dec 76		

AW 89781000
AY 89983500
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF ELBIT DATA

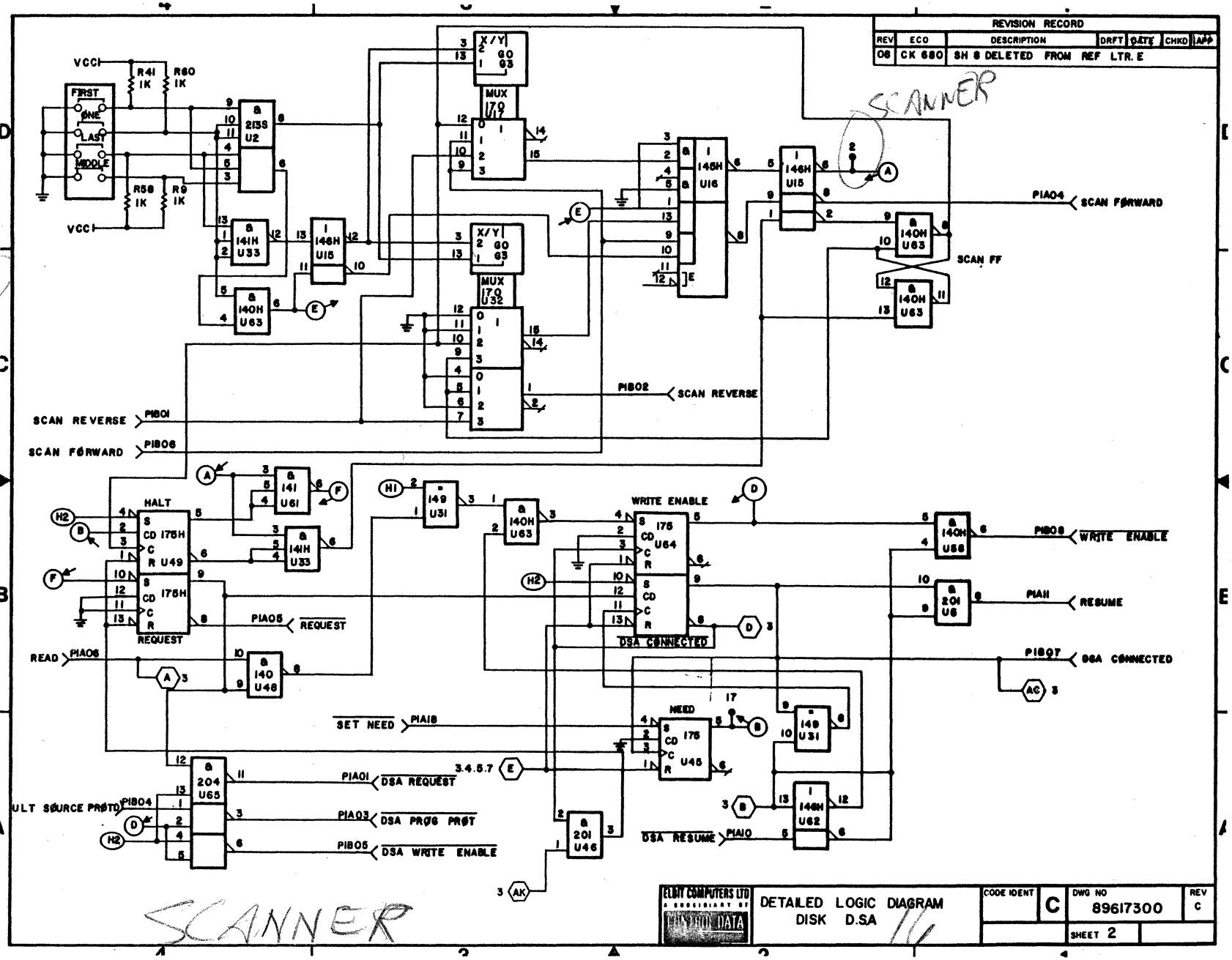
DWN	IONA	10.10.73
CHKD	[illegible]	7.1.74
ENGR	[illegible]	7.1.74
MFG	[illegible]	16 JAN 74
APPR	HAIM I.	4/4/74
Q.A.	[illegible]	

FIRST USED ON: FA 716-A

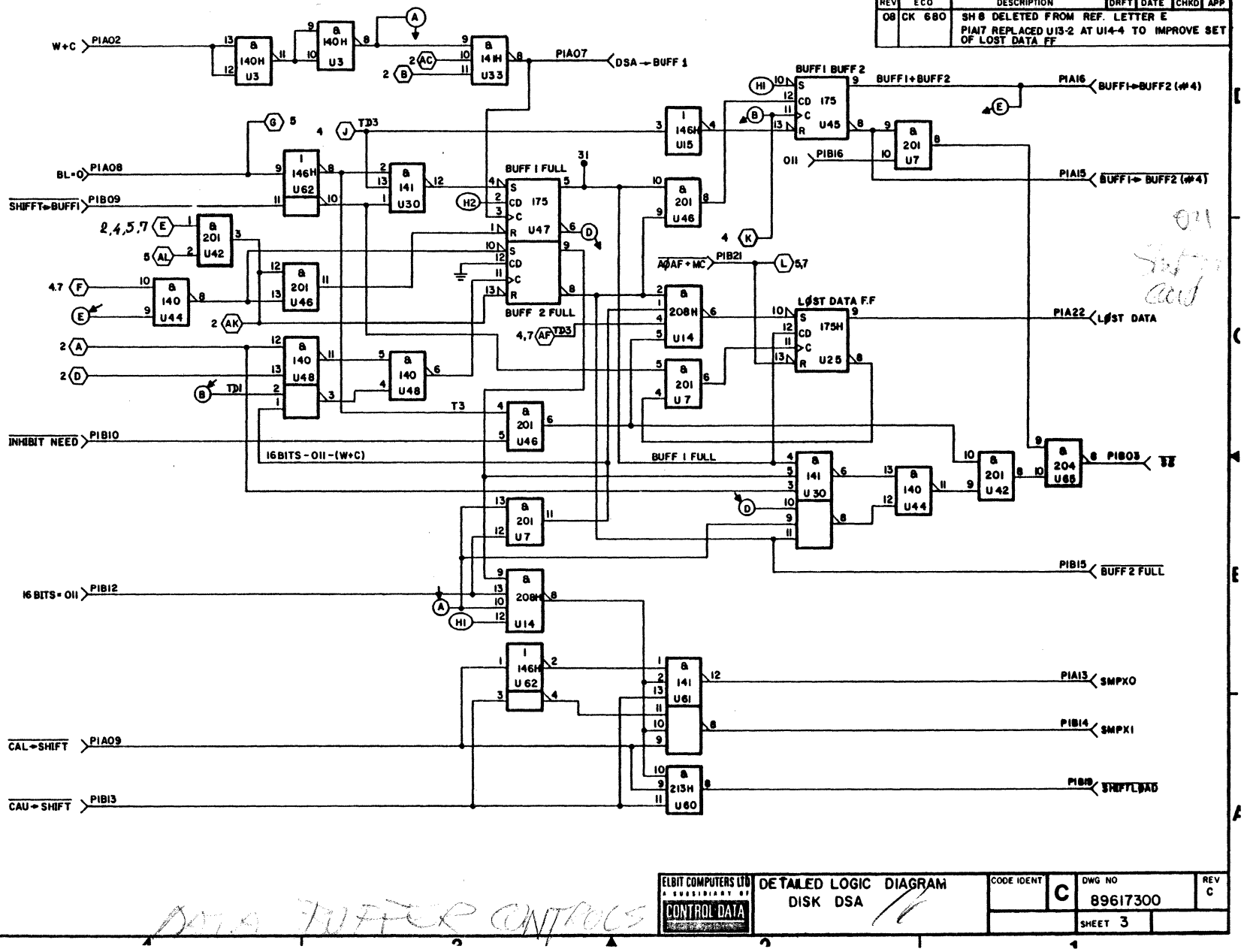
TITLE: DETAILED LOGIC DIAGRAM
DISK DSA

CODE IDENT: C
DRAWING NO: 89617300
SCALE:
SHEET 1 OF 8

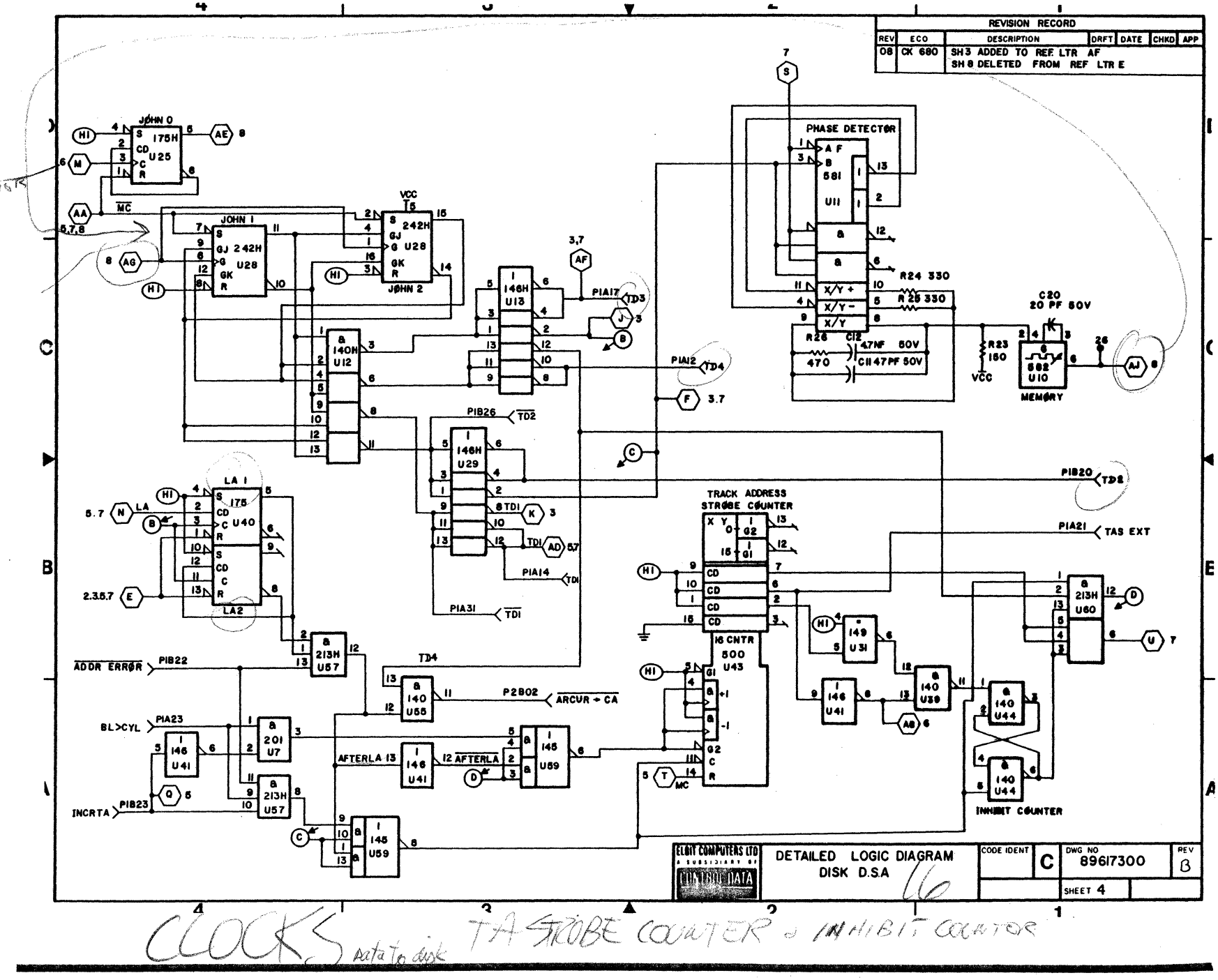
NO JUMPER OUT POSITION (OFF LINE)



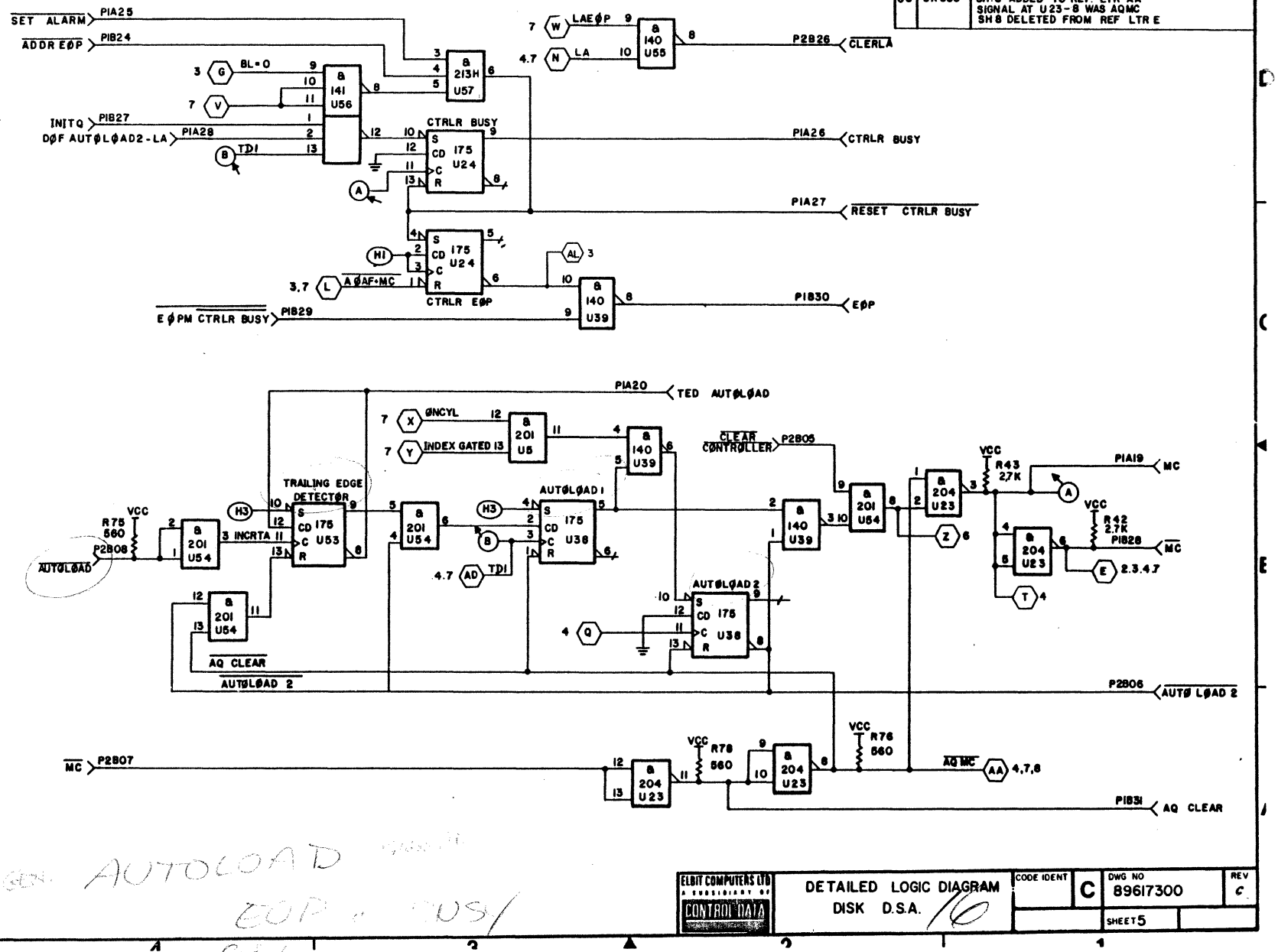
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
08	CK 680	SH 8 DELETED FROM REF. LETTER E PIA17 REPLACED U13-2 AT U14-4 TO IMPROVE SET OF LOST DATA FF				



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM DISK DSA	CODE IDENT C	DWG NO 89617300	REV C
			SHEET 3	


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
08 | CK 660 | SH3 ADDED TO REF LTR AF
SH 8 DELETED FROM REF LTR E
20 MHZ. OSCILLATOR
JOHN 0
JOHN 1
JOHN 2
PHASE DETECTOR
MEMORY
R24 330
R25 330
R26 470
C12 .47NF 50V
C11 47PF 50V
C20 20 PF 50V
R23 150
VCC
PIB26 TD2
PIA17 TD3
PIA12 TD4
PIB20 TD2
PIA21 TAS EXT
PIA14 TDI
PIA31 TDI
TRACK ADDRESS STROBE COUNTER
16 CNTR 500 U43
INHIBIT COUNTER
ADDR ERROR PIB22
BL>CYL PIA23
INCRTA PIB23
AFTERLA 13
12 AFTERLA
P2B02 ARCUR ÷ CA
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK D.S.A
CODE IDENT C
DWG NO 89617300
REV B
SHEET 4
CLOCKS
data to disk
TA STROBE COUNTER
INHIBIT COUNTER

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
08	CK680	SH.8 ADDED TO REF. LTR AA SIGNAL AT U23-8 WAS AQMC SH8 DELETED FROM REF LTR E				

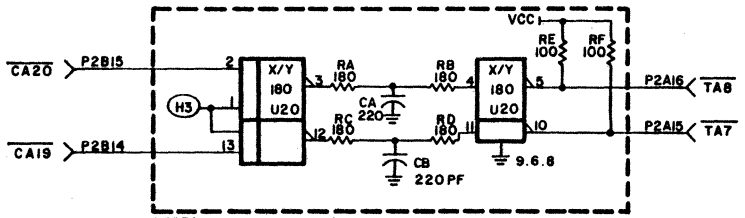


AUTOLOAD

EOP + BUSY

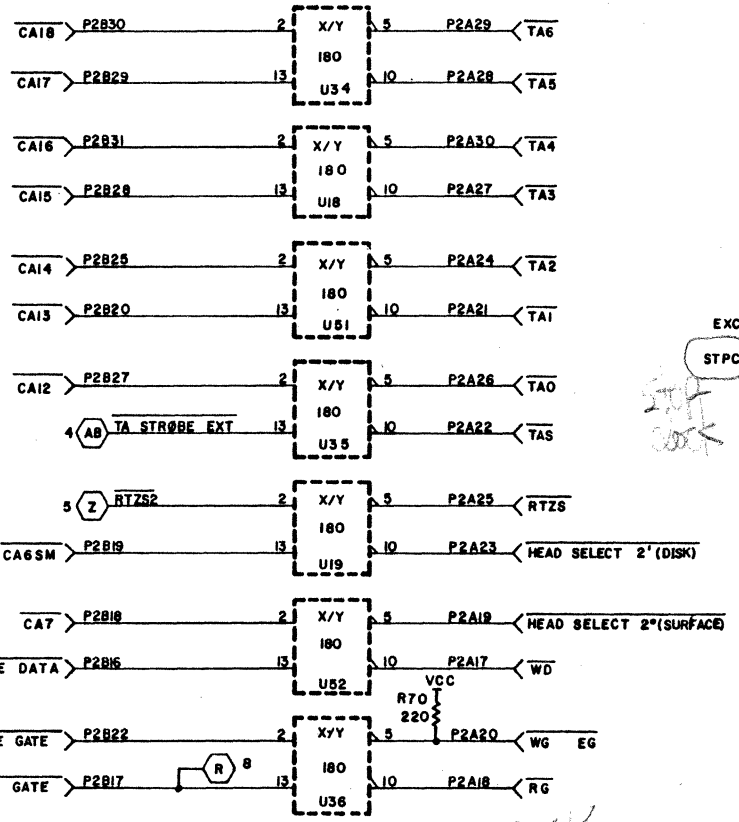
ELBIT COMPUTERS LTD / CONTROL DATA	DETAILED LOGIC DIAGRAM DISK D.S.A. 10	CODE IDENT C	DWG NO 89617300 REV C
			SHEET 5

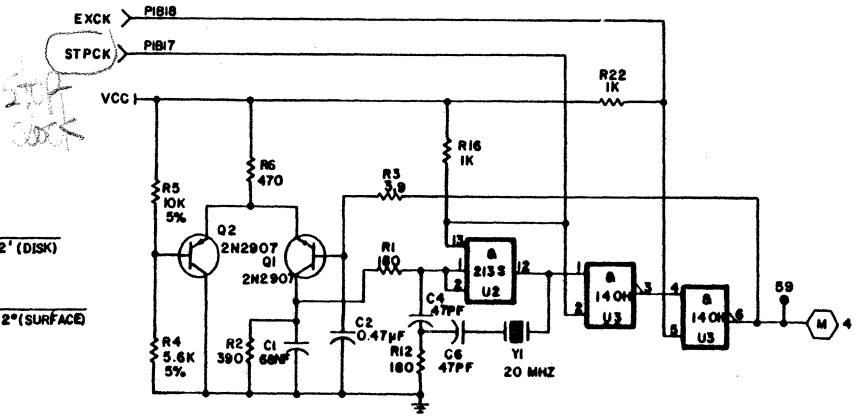
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



NOTE: EACH DOTTED LINE BOX BELOW CONTAINS A CIRCUIT SIMILAR TO ABOVE. CONSULT TABLE ON THE RIGHT FOR LIST OF RESISTORS AND CADACITORS.

IC NO	RESISTORS						CAPACITORS	
	R A	R B	R C	R D	R E	R F	C A	C B
U 20	R 36	R 35	R 13	R 14	R 38	R 37	C 18	C 8
U 34	R 45	R 44	R 29	R 30	R 62	R 47	C 21	C 15
U 18	R 28	R 27	R 8	R 7	R 63	R 46	C 14	C 3
U 51	R 67	R 68	R 51	R 50	R 66	R 69	C 30	C 22
U 35	R 49	R 48	R 34	R 33	R 64	R 52	C 23	C 16
U 19	R 32	R 31	R 10	R 11	R 65	R 80	C 17	C 7
U 52	R 73	R 72	R 56	R 57	R 71	R 74	C 31	C 24
U 36	R 55	R 54	R 39	R 40	R 70	R 53	C 25	C 19

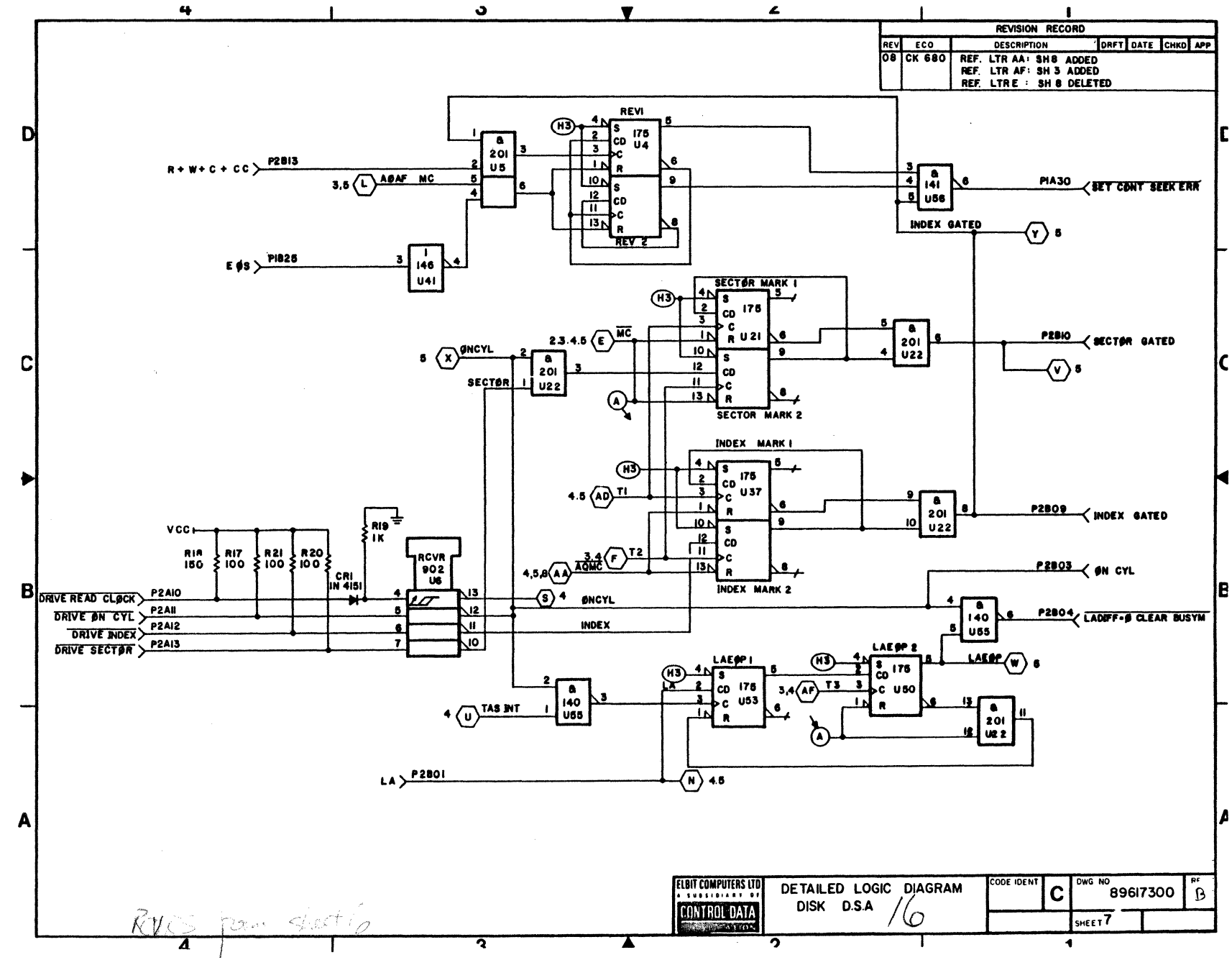




XMITTERS to DISK

GENERATE - CYL. ADDR (+2 STROBE) RTZS R/W Gate OSCILLATOR FOR CLOCKS

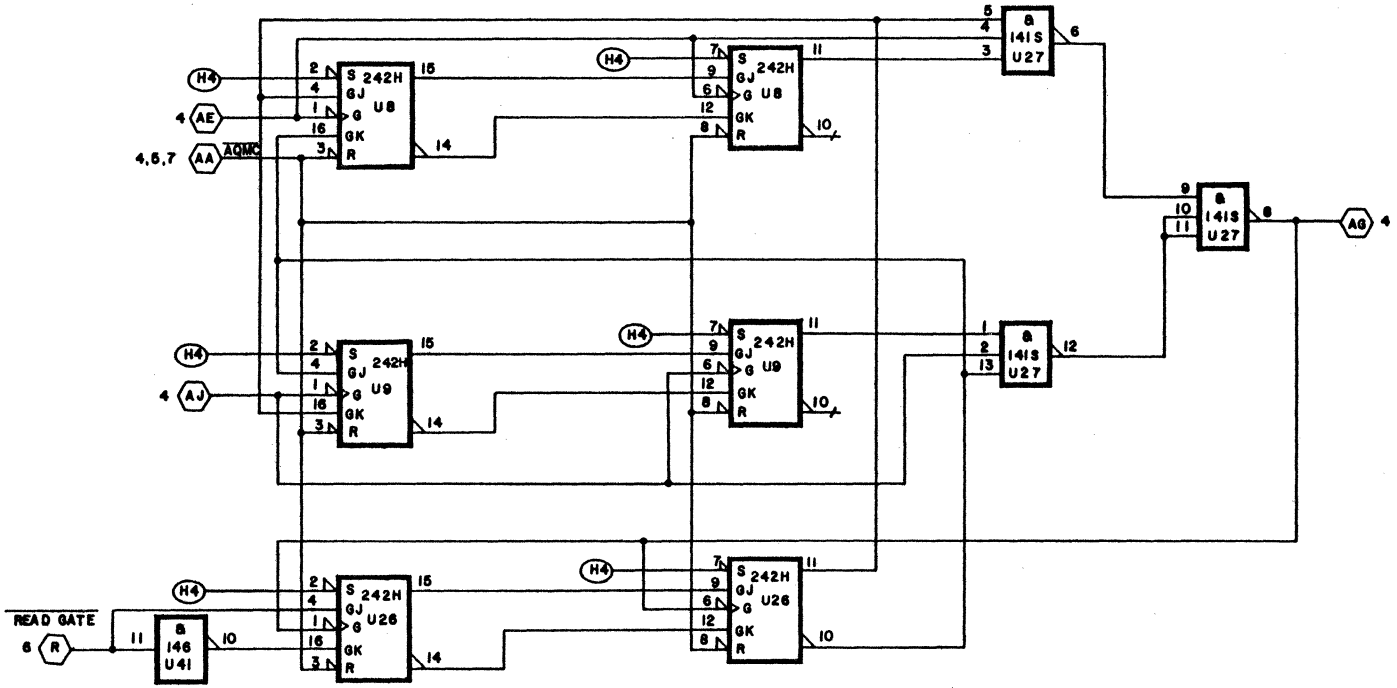
ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM DISK DSA	CODE IDENT C	DWG NO 89617300	REV B
			SHEET 6	



RVCS from sheet 6
SECTOR MARKS

5-62/5-63

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
08	CK 680	U23-8(AQMC) REPLACED U23-6(MC) AT U8-3 TO FIT TIMING DIAGRAM				



CLOCKS

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM DISK DSA	CODE IDENT	C	DWG NO 89617300	REV A
				SHEET 8	

89638100 C

"Pages 5-64 to 5-70 are unassigned."

SECTOR COUNT PW BOARD (Logic Diagram 89618200, Sheets 1-5).

Each of the 29 sectors on a track is divided into five distinct fields as shown in the Figure 5-7 below.

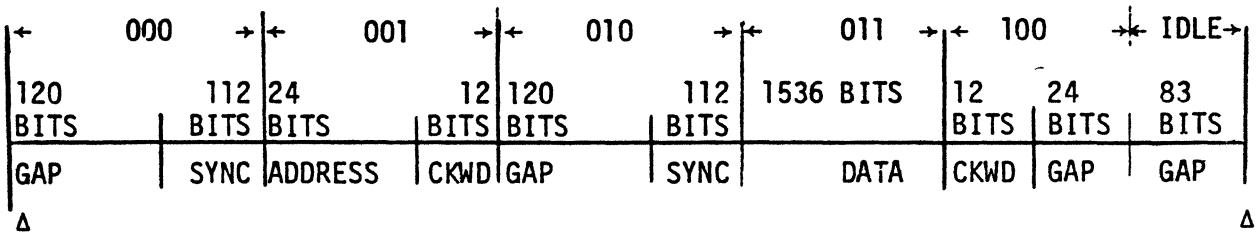


Figure 5-7. Track Fields (WA R+W+C+CC)

The fields are numbered 000_2 through 100_2 and are counted by the Sector Field Counter (SFC) at U7 (SHEET 3). Within each field the number of bits are counted by the Field Length Counter (FLC) at U18 and U2. Within the data field the Bit Counter at U9 counts bits and gives an indication for every group of 16 bits (words). The FLC then counts words by being incremented once for each group of 16 bits indicated by the Bit Counter.

Sector Field Counter (SFC) (SHEET 3)

Before an operation is initiated the SFC is held in the Idle state (Q00 thru Q04= zero) by the inactive DØF signal at U14. When an operation is initiated the DØF becomes active at U22-12. At the leading edge of the next Sector Gates (SG) signal the Start SFC FF at U22-9 is set. At the T4 of the same SG signal the Shifter (at U7), receives a Clock pulse and a "one" is entered into the first stage of the Shifter. This "one" represents the "000" state.

At the following T3, the START SFC FF is cleared. Thereafter, the initial "one" is shifted right at the leading edge of T_2 at the end of each field. Each stage of the Shifter thus represents one of the counts 000_2 thru 100_2.

When the processing of a particular sector is completed, the Shifter is set to all zeros (the "Idle" state) by the appropriate input at U14.

Field Length Counter (FLC) (SHEET 3)

At the beginning of each sector, the FLC is cleared to 00_{16} by the $\overline{\text{SECTOR GATED}}$ signal at U54-11. The FLC is also cleared at the beginning of each field within the sector by the $\overline{\text{INCR SFC}}$ signal at U54-9. The $\overline{\text{INCR SFC}}$ signal is active during the T_2 on which the SFC is incremented.

Thereafter, the FLC is incremented by one at the trailing edge of each T_3 except in the 011 field. In the 011 field the FLC is incremented at the trailing edge of T_3 when the signal $\overline{\text{16 BITS COMPARE + 15 BITS COMPARE}}$ (U43-8) is active.

The outputs of the FLC are decoded into various signals by the 167 one-of-sixteen decoder and the 203H at U3, U19 and U33.

Read, Compare and Checkword Check (SHEET 4)

SFC=000: FLC counts from zero to 232_{10}. At count 153_{10} (midway through the Sync area) the SEARCH SYNC (U21-5) and READ GATE (U20-9 SHEET 2) FF's are set. At count 232 the READ SYNC bit is detected and indicated by the setting of the READ SYNC BIT 1 FF (U6-9) at a T_4. The setting of the READ SYNC BIT 1 FF causes the SFC to advance to 001_2, the FLC and Bit Counter to be cleared to zero, the CLEAR CKWD to be active and the SEARCH SYNC FF to be reset. In addition the load of the upper order 12 bits of the address to the Shifter is enabled by the $\overline{\text{CAU→SHIFT}}$ signal (U11-11).

SFC=001: The FLC counts from zero to 36_{10}. The Bit Counter counts from zero. When the Bit Counter advances to a count of 1100, the signal $\overline{\text{12 BITS}}$ (U39-8 on SHEET 3) enables the load of the low order 12 bits of the address to the Shifter via the CAL → SHIFT signal (U58-12 on SHEET 2).

Each of the 24 Address bits loaded into the Shifter is compared with the corresponding bit read from the disk. The DATA STRETCHED FF (U30-5 SHEET 2) is set at T3 when a "one" bit is read from the disk. At the following T_1 the state of the DATA STRETCHED FF is compared with the state of the Shifter bit 11 (S_{11}) by the "Exclusive OR" at U31-8. If S_{11} does not equal DATA STRETCHED, the FF ADDRESS NO COMPARE U32-9 is set. The setting of the ADDRESS NO COMPARE FF clears the FLC and forces the SFC to the Idle state. Nothing further occurs until the next SECTOR GATED. If each pair of Address bits is equal, the controller continues to process this sector.

At FLC Count 24, the Bit Counter is cleared and at T_2, the CHECKWORD FF (U32-5) is set.

From Counts 25 through 36 the Checkword from the disk is passed through the Checkword logic (on A/Q card). If there is a Checkword Error, the signal $\overline{\text{ADDR CKWD=0}}$ will be inactive at U26-13 (SHEET 3). This causes the FLC to be cleared and the SFC to be set to the Idle state until the next Sector Gated.

If there is no Checkword Error, the FLC count 36 will cause the Read Gate to reset and the SFC to advance to 010.

SFC=010: The FLC counts from zero to 232_{10}. At count 176_{10} the SEARCH SYNC and READ GATE FF's are set. At count 232 the Read Sync Bit is detected and the READ SYNC BIT 1 FF (SHEET 4) is set. The setting of the READ SYNC BIT 1 FF causes the SFC to be advanced to 011, the FLC to be cleared, SEARCH SYNC FF to be reset, the $\overline{\text{CLEAR CKWD}}$ to be active and the Bit Counter to be loaded with the count 0001_2, or in the case of a Compare operation to be cleared to 0000_2.

SFC=011: Serial data is received on the READ DATA signal and transmitted to the Shifter via the DATA signal (U29-8 on SHEET 4). The Bit Counter is incremented once for every bit. In Read or Write operations when sixteen bits have been transferred, the signal $\overline{\text{16 BITS}}$ allows the FLC to be incremented. In compare operations the signal "15 BITS" allows the increment. Thereafter the FLC is incremented once for every group of 16 bits. The signal $\overline{\text{SHIFT} \rightarrow \text{BUFF 1}}$ causes the transfer of the word from the Shifter to the Buffer 1.

In the case of a Compare operation, data read from the disk is compared with data received from the DSA. The comparison is executed bit by bit by the "exclusive or" at U31 on SHEET 2). If a mismatch is detected between S_{15} and DATA STRETCHED the DATA NO COMPARE STATUS FF (U30-9) is set. The processing of the sector continues. If no mismatch is found, the comparison operation continues until either the data field is completed or the INHIBIT COMPARISON FF is set. The INHIBIT COMPARISON FF (U25-5 on SHEET 5) is set by the leading edge of 16 BITS ·011 when the Buffer Length is zero and the $\overline{\text{BUFFER 2 FULL}}$ signal is inactive; that is, immediately after the last word to be compared is completed. The INHIBIT COMPARISON FF is reset after the comparison operation is completed when the R+W+C signal drops and 16 bits is present.

At FLC Count 96 the SFC is incremented to 100 and the FLC and Bit Counter are cleared to zero. In addition the $\overline{\text{LOAD CKWD 2}}$ signal is generated to cause the transfer of the checkword from the checkword logic to the Checkword 2 register (A/Q card).

SFC=100: When the FLC count 15 becomes active, the Read Gate is reset. At count 12 the Sample Checkword signal is generated. At Count 24 the $\overline{\text{INCR SECTOR}}$ signal is activated. The trailing edge of this signal causes the increment of the File Address (Sector Counter and Cylinder Address Register). At Count 32 the EØS pulse is generated. At Count 36 the ADDR. NO COMPARE FF is set, thus forcing the SFC to the Idle state until the next sector is encountered.

Write

The Write operation is exactly the same as the Read until count 120 in 010. At the point the WRITE GATE FF (U20-6, Sheet 2) is set. The setting of the WRITE GATE enables the writing of the Write Clock pulses (at T_1) via the signal $\overline{\text{WRITE DATA}}$ U55-8 on SHEET 4.

At the T_4 after the FLC count 230 becomes active, the FF COUNT 231 is set, thereby generating the $\overline{\text{WRITE SYNC BIT}}$ signal at U28-6 on SHEET 2. The $\overline{\text{WRITE SYNC BIT}}$ causes the SFC to be advanced to 011, the FLC and Bit Counter to be cleared, the $\overline{\text{CLEAR CKWD}}$ to be active and a "one" to be written as bit 232.

SFC=011: Within the 011 field the Write operates similarly to the Read except that the signal 16 BITS .011 (U40-6 on SHEET 3) is used to enable the transfer of each word from Buffer 2 to the Shifter. In addition serial write data is received from the Shifter via signal S15 and transferred to the disk via $\overline{\text{WRITE DATA}}$.

At Count 96,the CKWD FF (SHEET 2) is set to allow the serial transfer of the Checkword (via CKWD 11) to the disk.

SFC 100: The Write operation is completed similarly to the Read. The Write Gate is reset at the completion of the operation by the COUNT 15 ·100 signal at U26-6 on SHEET 2.

Write Address

SFC = 000: The Write Gate is set at count 120. The setting of the Write Gate causes the writing of the Write Clock pulses (at T_1) via the $\overline{\text{WRITE DATA}}$ signal.

At Count 230 ·T4, the WRITE SYNC BIT signal is generated and at Count 232 the Sync bit is written.

SFC=001: The Shifter is loaded with the address as in the Read and Write operation. The address is transferred from the Shifter bit 11 by the S11 signal and transmitted to the disk via the $\overline{\text{WRITE DATA}}$ signal.

At Count 24 the CKWD FF is set and the Checkword is transferred serially from the Checkword logic via the Signal CKWD 11 and written on the disk via $\overline{\text{WRITE DATA}}$. The signal $\overline{\text{WD CKWD}}$ is active during the write of the Checkword.

At Count 36 the SFC is advanced to 010, the FLC is cleared, the WRITE GATE is reset and the signal $\overline{\text{INCR·SECTOR}}$ is generated.

The SFC is forced to the Idle state at Count 12 ·010 by the signal at U60-6 (SHEET 3). The SFC remains idle until the next SECTOR GATED signal, at which point the address of the next sector is written.

Need Generation (SHEET 5)

The 100 ns $\overline{\text{SET NEED}}$ signal is active once for each word transferred. During Write and Compare operation the $\overline{\text{SET NEED}}$ is generated for the first time at Count 120 in 010. Thereafter, $\overline{\text{SET NEED}}$ is generated whenever BUFF 1 → BUFF 2is active and neither the BL=0 NOT INHIBIT NEED FF is active.

During Read operations, the $\overline{\text{SET NEED}}$ is generated whenever BUFF 1 → BUFF 2 is active and the BL = 0 FF is not set.

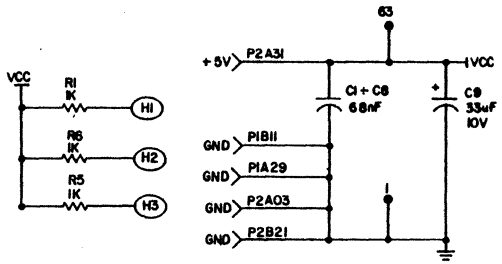
CWA Count (SHEET 5)

The Current Word Address register (on Shifter card) is decremented by the trailing edge of the $\overline{\text{CWA COUNT}}$ signal (U59-6). The $\overline{\text{CWA COUNT}}$ is generated by the RESUME signal.

ØFF SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SIGNALS	SHEET LØCATIØN 2	3	4	5
A		▼A-3		A-4	
B		▼C-2		B-3	
D			▼A-4	A-3	
E	WRITE SYNCHBIT	▼C-1	C-3	A-3	
F		C-4	C-1		
G	SI5	B-2		C-4	
J		▼A-3		B-3	
K	SII	B-2		B-4	
L		A-3	▼D-3	B-3	
M		▼A-1	A-3		
N		▼C-2		B-4	
P		▼C-1		B-4	
Q		B-3		▼C-2	
R		C-1	C-4	▼C-2	
S		C-2		▼D-2	
T			A-4	▼C-3	
U		▼B-3		C-4	
V	READ DATA	B-3		C-3	
W	TD2	C-1		C-4	C-1
Z		▼D-3	A-3		
Y		C-3	C-4	▼C-3	C-1
AA			▼B-1	D-2	
AB	WRITE	D-4		D-3	
AC		C-4	▼D-3	D-3	
AD		▼D-2		D-2	
AE			A-3		C-2
AF	TD4	D-2	D-4	C-4	
AG		▼A-4	C-4		
AK	COMPARE	A-4	A-4	C-4	D-1
AL		▼C-3			B-2
AM	ADDRESS	D-3			B-2
AN		C-4	▼C-1		
AP	W+C	B-4			A-3
AQ		D-3	▼D-1		B-4
AR	TD3	B-3	A-2	A-3	
AS	R+W+C	D-3			B-3
AT	INHIBIT NEED	▼B-4			B-4
AU		B-2			▼D-1
AV	TDI	B-2	A-4		
AW			▼D-1		C-3
AX		▼B-3	A-4		
AZ	READ		A-1		A-4
BA		▼C-1	A-3		
BB		B-2	▼D-3	D-4	
BC		B-4	▼D-3		

		SHEET LØCATIØN 2	3	4	5
BD		C-2	▼D-3		
BE	Q10	D-4	▼C-4	D-4	B-4
BH		C-2	▼C-3		
BF		C-2	▼C-3		
BG		B-4	▼C-3	C-3	
BL		D-4	▼C-3		B-3
BN		B-4	▼D-1		C-3
BM		B-4	▼D-1		C-3
BQ		D-2	▼C-1		
BR		D-3	D-4		
BU	SECTOR GATED	B-4	▼C-1		
BV		C-4	C-4		
BP		A-4	▼B-3		
BY		▼B-4	A-4		
BZ		D-4	▼B-2		
MC	MC	B-3		C-4	
BT		B-4	▼B-1		
BK		C-3			B-2



NOTES: 1. ALL RESISTØRS ARE 0.25 WATT 5%
2. ▼ - DENØTES SIGNAL ØRIGIN.

SHEET REVISION STATUS							
1	2	3	4	5			
05	05	05	05	05			
06	06	06	06	06			
07	07	07	07	07			
08	08	08	08	08			
09	09	08	09	08			
10	09	10	09	10			
A	A	A	A	A			

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
05	CK 455	REDRAWN TO CDC STD.	Dayan	8 May 74		
06	CK 624	DWG. ERRORS	Ayan	8 May 74	Ayan	
07	CK 628	PINS AFFECTED: U15-10,11 P1B28, P1A20 U53-4, U60-12, U34-3, U47-4, U17-19, P2B11 USED IN PWB 89618101 REV. 02	Ayan	7 July 74		
08	CK 994	DWG. ERRORS CORRECTED SHEETS 1-5. CORRECTS LOGIC REV 05	R.S.	oct. 74		
09	CK1025	SH4, B-3: P1A19 (READ DATA) REPLACES U30-5 (SH2, B-2) AT U11-4. FITS ASSY 89381100 REV 01.		Aug 74	Ayan	
10	CK1035	SH 3, B-1; AT U3-1 U1-10 REPLACES U1-13. AT U3-13, U17-10 REPLACES U17-1 FITS ASSY 89897300 REV. 01	Ayan	Jan 5 75		
A	CK 1184	RELEASED CLASS A. USES PWB 89618101 REV. 01	R.S.	5.5.75	M.M.	
B	CK 1401	SH. 2, A-B U38-3 WAS ADDRESS SH. 2, B-8 U11-11 WAS CAU-SHIFTER. SH. 3, U11-10 WAS FREE U3-11 WAS CONNECTED TO U3-13. U1-10 WAS FREE U1-13 WAS CONNECTED TO U3-1. U13-13 WAS 811.	A.K.	11.11.75		
C	CK 1432	SH2 GATES U44-1,2,3, U18-12,4,5, U22-1,2,3,4,5,6, ADDED. P2A11 WAS CONNECTED TO U47-1. SH. 3 GATES U48-12,13, U56-1,2 U10-8,9,10,12,13, U5-11,12,13, ADDED U8-6 CONNECTED TO (F)	Lijot	4.8.76		

AW 89618101
AY 89963600
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
[redacted]

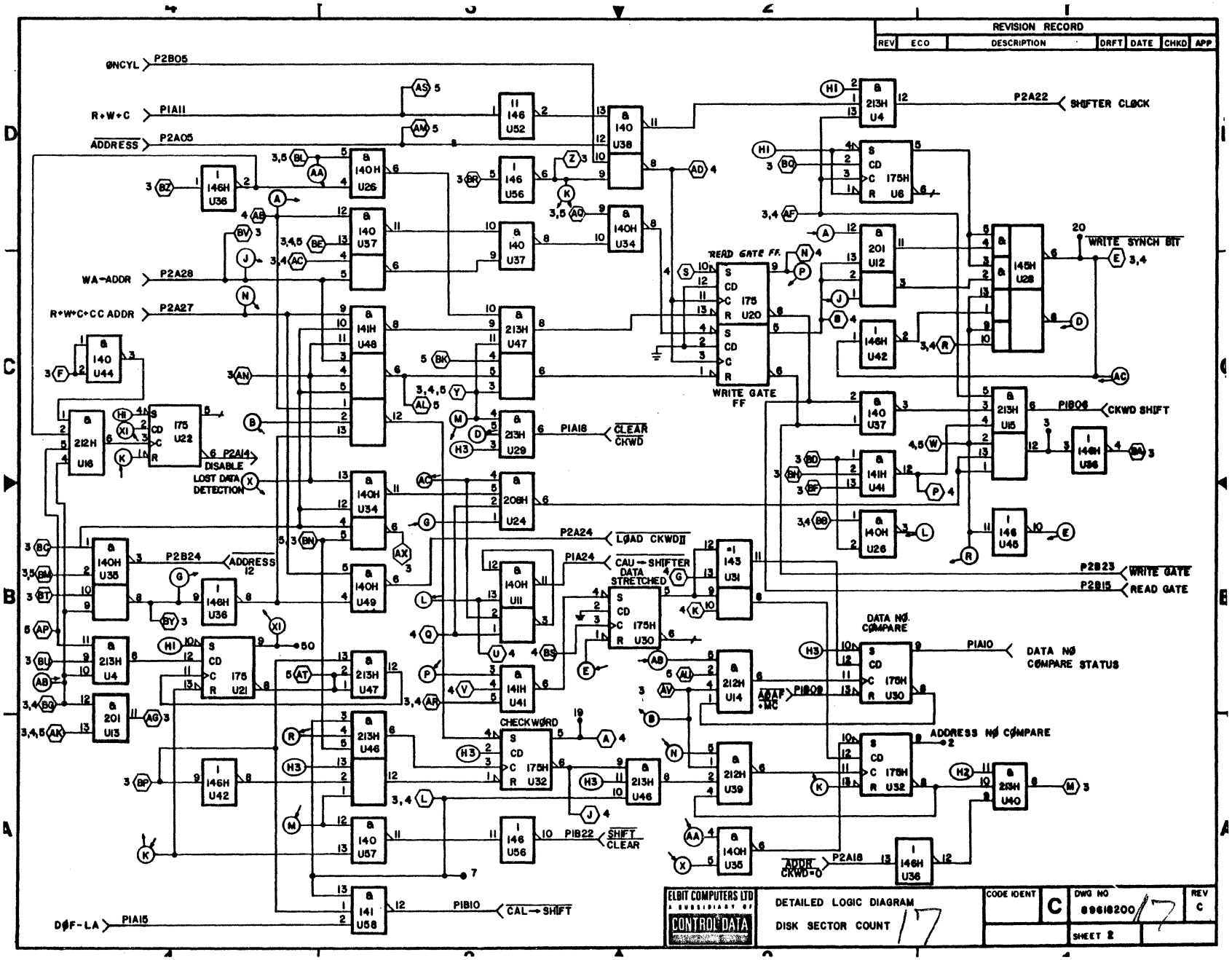
FIRST USED ON FA716-A

DWN	Dayan	Dec, 75
CHKD	Dayan	Jan. 2. 76
ENGR	[illegible]	[illegible]
MFG	[illegible]	25 MAY 76
APPR	HAIM J.	May 76
Q.A		

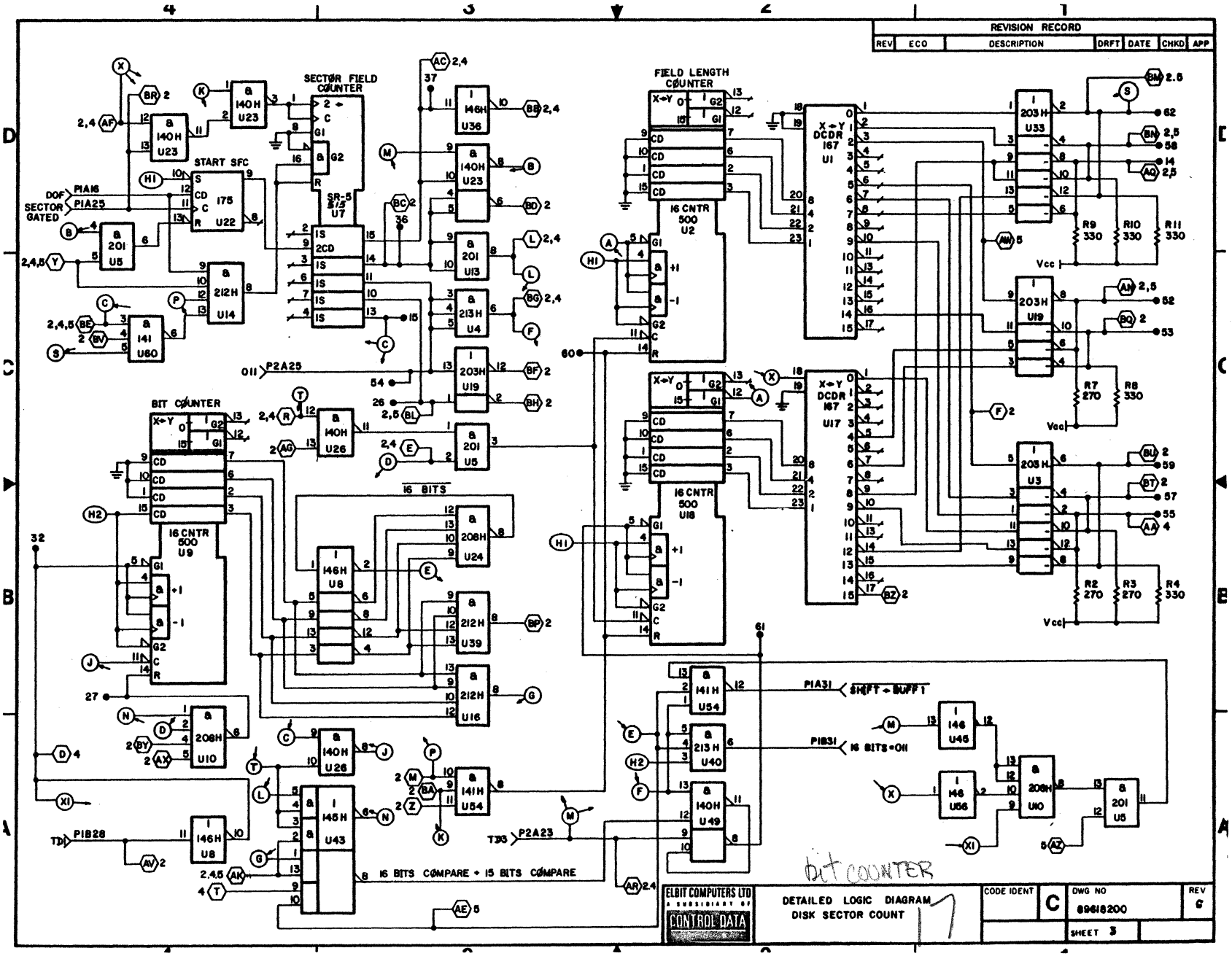
TITLE
DETAILED, LOGIC DIAGRAM
DISK SECTOR COUNT

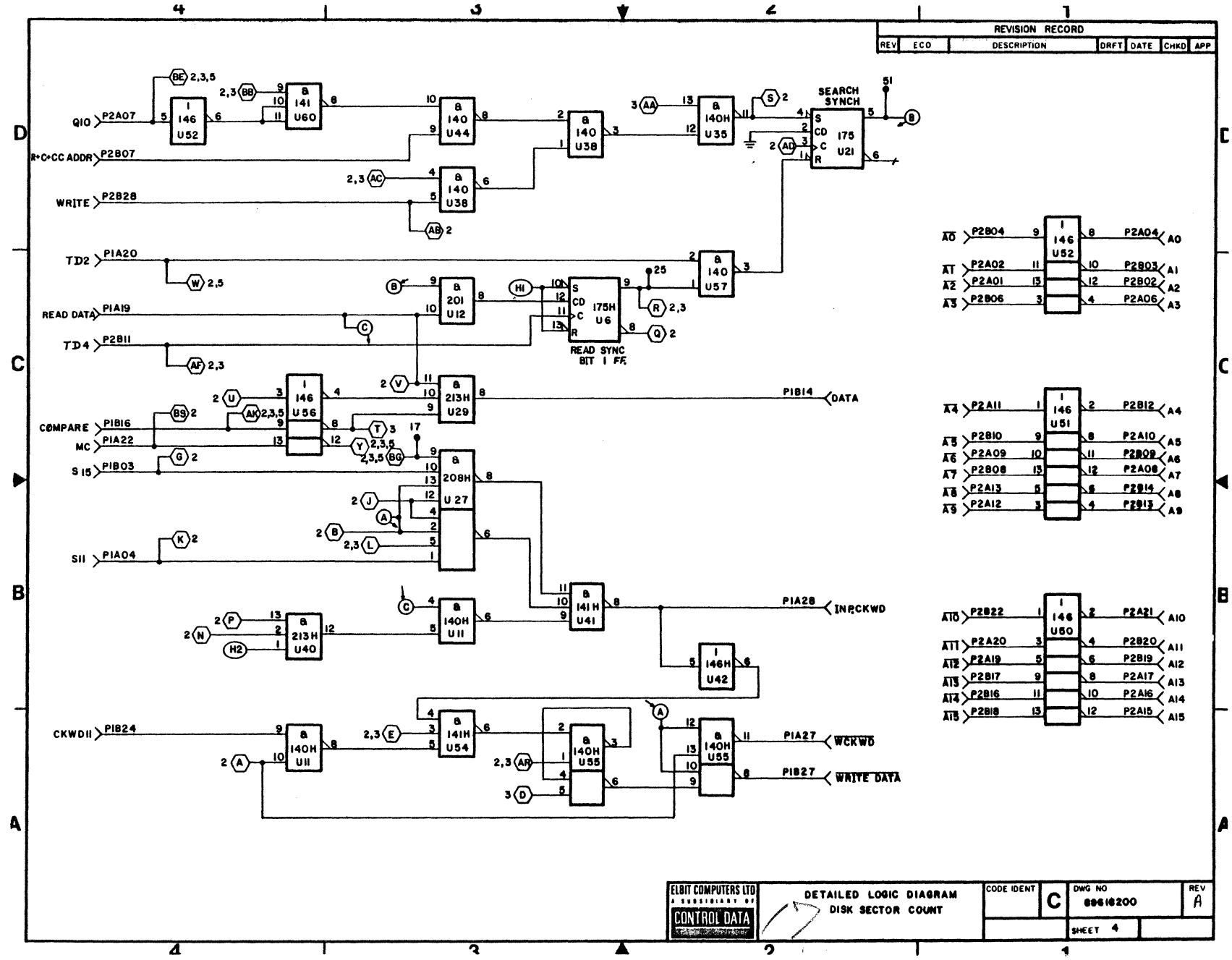
CODE IDENT	DRAWING NO
C	89618200 17

SCALE | SHEET 1 OF 5

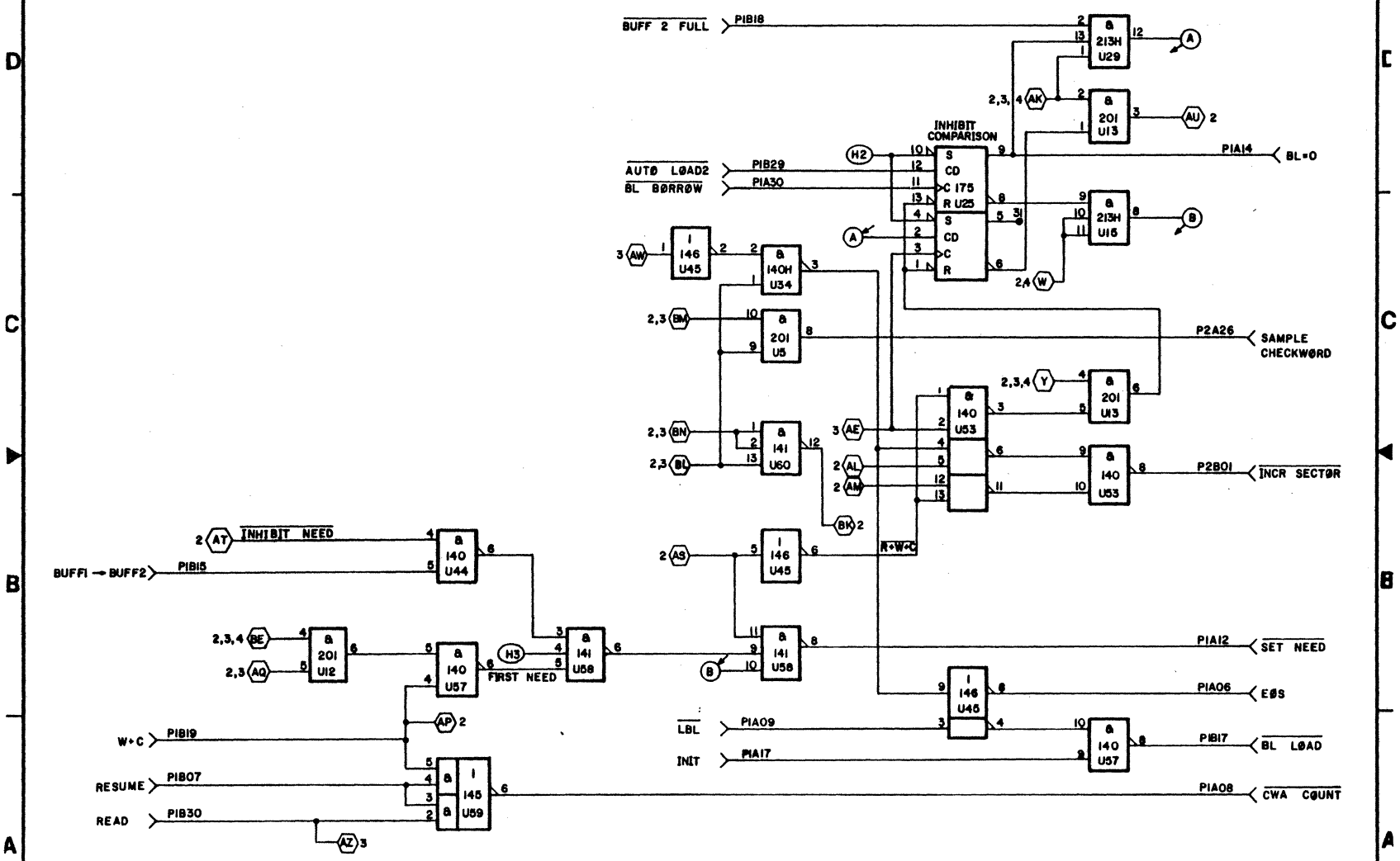


SEGMENTS THAT COMPOSE A SECTOR


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SECTOR FIELD COUNTER
START SFC
SR-5
BIT COUNTER
16 BITS
FIELD LENGTH COUNTER
16 CNTR 500 U2
16 CNTR 500 U9
16 CNTR 500 U17
16 CNTR 500 U18
X↔Y DCDR 167 U1
X↔Y DCDR 167 U17
16 BITS COMPARE + 15 BITS COMPARE
PIA31 SHIFT→BUFF1
PIB31 16 BITS→011
DOF SECTOR GATED
PIA16
PIA25
P2A25
PIB28
T35 P2A23
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK SECTOR COUNT
bit COUNTER
CODE IDENT C
DWG NO 89618200
REV G
SHEET 3


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
Q10 P2A07
R+C+CC ADDR P2807
WRITE P2828
TD2 P1A20
READ DATA P1A19
TD4 P2811
COMPARE P1B16
MC P1A22
S 15 P1B03
S11 P1A04
CKWD11 P1B24
SEARCH SYNCH
READ SYNC BIT 1 FF
P1B14 DATA
P1A28 INRCKWD
P1A27 WCKWD
P1B27 WRITE DATA
A0 P2B04 P2A04 A0
A1 P2A02 P2B03 A1
A2 P2A01 P2B02 A2
A3 P2B06 P2A06 A3
A4 P2A11 P2B12 A4
A5 P2B10 P2A10 A5
A6 P2A09 P2B09 A6
A7 P2B08 P2A08 A7
A8 P2A13 P2B14 A8
A9 P2A12 P2B13 A9
A10 P2B22 P2A21 A10
A11 P2A20 P2B20 A11
A12 P2A19 P2B19 A12
A13 P2B17 P2A17 A13
A14 P2B16 P2A16 A14
A15 P2B18 P2A15 A15
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK SECTOR COUNT
CODE IDENT C
DWG NO 89618200
REV A
SHEET 4

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM DISK SECTOR COUNT	CODE IDENT C	DWG NO 89618200	REV A
			SHEET 6	

"Pages 5-84 to 5-90 are unassigned."

DAISY CHAIN PW BOARD (Logic Diagram 89617900, Sheet 1-4).

The Daisy Chain card is divided into the following functional parts:

1. Unit Selection
2. Unit Busy FF's
3. Address Error Detection
4. Equipment Number Selection
5. Unit Protect
6. Unit Track Density Selection
7. Unit Seek Complete Logic
8. Head 0 Selection

Unit Selection (SHEET 2)

The rising edge of the DF GATED signal at U16-1 and the presence of the Select bit (A8) U16-2 allows the setting of the UNIT SELECTION FF's (U12). The particular FF is set according to a binary decode of bits A9 and A10 (A9 least significant). During Autoload, the leading edge of the signal $\overline{\text{TED AUTOLOAD}}$ ANDed through U16, causes the selection of Unit 0, because A09 and A10 are zero. The UNIT SELECTION FF's may be cleared by the rising edge of the DF Gated signal and the presence of the Deselect bit (A07), ANDed.

In addition the UNIT SELECTION FF's are cleared by the A/Q Clear signal.

The Unit Selection signals are transmitted to the CDD via the 180 drivers U6 and U7.

Unit Busy FF's

There is one UNIT BUSY FF for each of four possible disk files. The BUSY FF of the selected unit is set during an LA instruction by the presence of the TAS EXT. (Track Address Strobe External) signal. In the normal case an individual UNIT BUSY FF will be reset by the rising edge of the SEØSC (Seek Error or Seek Complete on SHEET 3) signal. In the case where the selected file is already on the addressed cylinder, the selected UNIT BUSY FF will be reset by the leading edge of the $\overline{\text{LADIFF=0}}$ signal (from Disk). In the case of a Drive Seek Error or an Address Error the selected unit will be reset by the $\overline{\text{RESET BUSY M}}$ signal (from DSA card). The UNIT BUSY FF's may also be reset by the MASTER CLEAR signal.

The $\overline{\text{BUSY RR}}$ signal is active when either the selected UNIT BUSY FF or CTRLR BUSY signal is low at U28-2, or when no unit is selected.

Equipment Number Selection (SHEET 3)

The Equipment Number Match signal becomes active when bits Q07 thru Q10 match the setting of jumpers marked Q7 through Q10, respectively, A "zero" in the equipment number is represented by the presence of a jumper. A "one" is represented by the absence of a jumper. The signal is presented to the selected disk as a high EQUIP NO MATCH.

Unit Seek Complete Logic (SHEET 3)

The 520 at U8 contains one FF for each of the four possible disk drives. At the leading edge of the T_1 after the signal SEØSC becomes active, the appropriate FF is set. At the leading edge of T_2, the corresponding FF in U9 will set. The 100ns pulse between T_1 and T_2 causes the setting of the EØPM FF. The EØPM FF will be reset by the $\overline{\text{AØAF+MC}}$ signal.

Head 0 Selection (SHEET 3)

When the Head 0 Selection jumper is present the $\overline{\text{CA6SM}}$ signal will be active when the CA6 (bit 6 of Cylinder Address register) is active. When the Head 0 Selection jumper is absent, the $\overline{\text{CA6SM}}$ signal will be active when the CA6 signal is inactive.

Address Error Detection (SHEET 4)

The ADDRESS ERROR FF will be set during a LA operation by the detection of a Sector Address greater than 28 or by a Cylinder Address greater than either 202 or 407, depending on the setting of the Track Density Selection jumpers. The ADDRESS ERROR FF (U10-9 and 8) will be set by the SET ADDR ERROR signal during a R+W+C operation when the Cylinder Address Register (Shifter card) is advanced beyond 202 or 405, depending on the

setting of the Track Density Selection. The ADDRESS ERROR FF is cleared by the $\overline{\text{AØAF+MC}}$ (any Output from A function or Master Clear) signal.

Unit Protect (SHEET 4)

The SELD UNIT PRØTD (selected unit protected) signal will be active if the Protect Selection jumper of the selected unit is absent. If the Protect Selection jumper of the selected unit is present, the SELD UNIT PRØTD signal will be inactive.

The PØKM (Protect OK Multiple) signal will be active if the selected unit is not protected (i.e. jumper present) or if the selected unit is protected and the A/Q PROTECT signal is active.

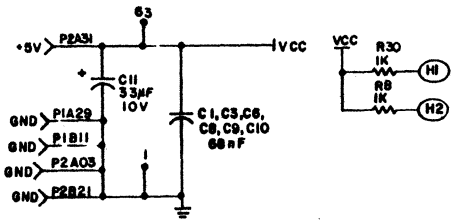
The ULTIMATE SOURCE PROTECTED FF will be set at the leading edge of the Read signal if the $\overline{\text{A/Q PROTECT}}$ signal is active, or during autoload by the $\overline{\text{TED AUTOLOAD}}$ signal (SHEET 2). The ULTIMATE SOURCE PROTECTED FF will be reset at the end of the operation by the $\overline{\text{RESET CTRLR}}$ $\overline{\text{BUSY}}$ - $\overline{\text{SET EØP}}$ signal.

Unit Track Density Selection (SHEET 4)

Each disk file attached may either be a 100 TPI or 200 TPI track density. 100 TPI is represented by the absence of a jumper and 200 TPI by the presence of a jumper. The SELD UNIT TPI 100 signal will be active if the jumper corresponding to the selected unit is absent.

ØFF SHEET REFERENCE

OFF SHEET REFERENCE LETTER	SIGNALS	SHEET LØCATIØN 2	3	4
A	A9	D-4		C-2
B	A10	D-4		C-2
C	A11(DESELECT)	C-4		C-2
D	A8(SELECT)	C-4		C-2
E	UNIT-0	▼D-3		D-3
F	UNIT-1	A-3		C-3
G	UNIT-2	A-3		C-3
J	UNIT-3	▼C-3		C-3
K	~~AUTØL ØAD~~ KED	D-3		D-1
M	LA	C-4		C-4
N	SCØSE0	A-3	▼B-3	
P	SCØSE1	A-3	▼B-3	
Q	SCØSE2	B-4	▼B-3	
R	SCØSE3	B-4	▼B-3	
S		▼B-1	A-2	
T	AØAF+MC		A-3	B-4
U	T32		C-4	B-4

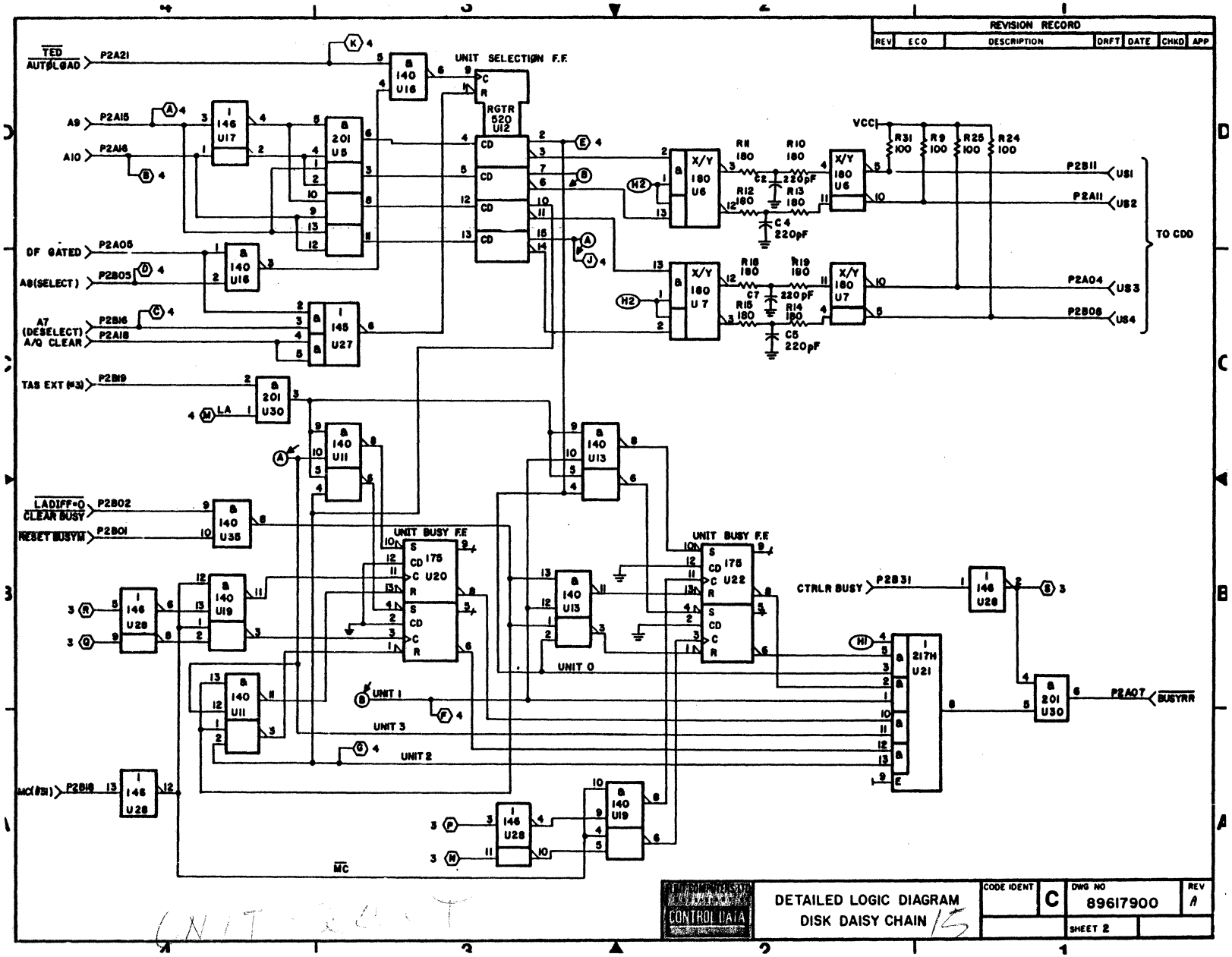


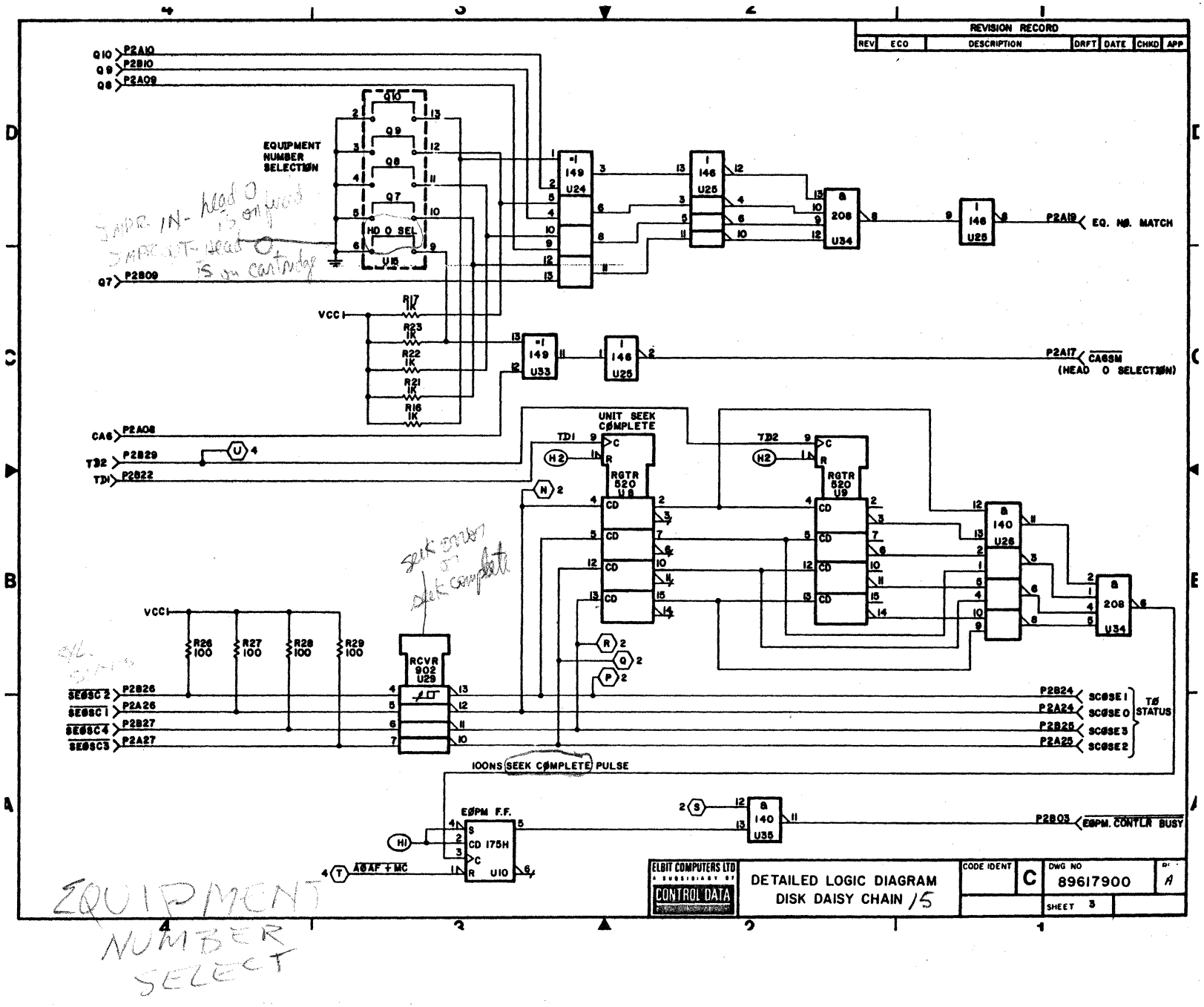
NOTES:
1. ALL RESISTØRS ARE 1/4 WATT 5%.
2. ▼ DENØTES SIGNAL ØRIGIN

SHEET REVISION STATUS			
1	2	3	4
04	04	04	04
05	05	05	05
06	05	05	05
07	07	07	07
08	08	08	08
09	09	09	09
A	A	A	A

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
04	CK 389	REDRAWN PER CDC STD	Rachel	Nov 16		
05	CK 629	CORRECTION OF DWG. ERRORS	Ayan	April 29 74		
06	CK 770	DETACHED LIST AY WAS 89017700	Ayan	31 July 74		
07	CK 1024	DWG. ERRORS CORRECTED TAGS ADDED. CORRECTS REV. 04	Ayan	oct. 74		
08	CK 1082	SH 1: REF. LTR V DELETED DETACHED LISTS UPDATED SH 8, C-2: P2B29(T2) REPLACES REF. LTR V AT U8-9 SH 4, B-3: GATE U16-8,9,10 REPLACES GATE U30-8,9,10 AT U10-11 FITS ASSY 89894100 REVS 01 AND 02. DWG. ERRORS CORRECTED PER CAR 184	Ayan	Dec. 8, 74		
09	CK 983	SH 4, B-2: U33-3/U34-11 REPL H4/U 34-11 (406 MAX. TRACK CAPACITY) SH 4, B-4: U36 FF ADDED. U36-6/U16-10 REPLACES H8/U16-10 (ADDRESS ERROR ON LAST LEGAL SECTOR) SH 4, B-3: H8/U18-9 REPL. P2B28/ U18-9, P2A28/U10-13 REPL. U18-8/ U10-13, U10-9/U17-11 REPL. P2A28/ U17-11, U18-10/P2B30 REPL. U10-8 P2B30, U18-8/P2A29 REPL U10-9/ P2A29. (TIMING PROBLEM IN RESET OF ADDR. ERROR FF) REF. LTR L DELETED REF LTR. H ADDED. VCC AND GROUND CONNECTIONS TO STD. FITS ASSY 89897600 REV. 01	M.L.	18.3.75	M.M.	
A	CK 1184	RELEASED CLASS A WCS ASSY 89617900 REV. A5 PLUS REWORK INSTR. ON ASSY SH 2	M.L.	5.5.75	M.M.	

AW 89617900	AY. 89897500	DETACHED LISTS	UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES 3 PLACE ± 2 PLACE ± ANGLES ±	ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	FIRST USED ON FA716-A	TITLE DETAILED LOGIC DIAGRAM DISK DAISY CHAIN 15	
			DO NOT SCALE DRAWING	DWN Rachel Nov 16		CODE IDENT C	DRAWING NO 89617900
			MATERIAL	CHKD Aubrey Kagan Dec. 9.74			
			FINISH	ENGR M. Tamir Dec. 23.74			
				MFG		SCALE	SHEET 1 OF 4
				APPR HAIM J. ZOI May 75			
				Q. A			


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
UNIT SELECTION F.F
RGTR 520 U12
UNIT BUSY F.F
UNIT BUSY F.F
UNIT 0
UNIT 1
UNIT 3
UNIT 2
TO CDD
P2B11 US1
P2A11 US2
P2A04 US3
P2B08 US4
P2A07 BUSYRR
P2B31 CTRLR BUSY
P2A21 TED AUTØLOAD
P2A15 A9
P2A16 A10
P2A05 DF GATED
P2B05 AS(SELECT)
P2B16 A7 (DESELECT) A/Q CLEAR
P2A18
P2B19 TAS EXT (#3)
P2B02 LADIFF=0 CLEAR BUSY
P2B01 RESET BUSYM
P2B19 MC(#3)
MC
DETAILED LOGIC DIAGRAM
DISK DAISY CHAIN
CONTROL DATA
CODE IDENT C
DWG NO 89617900
REV A
SHEET 2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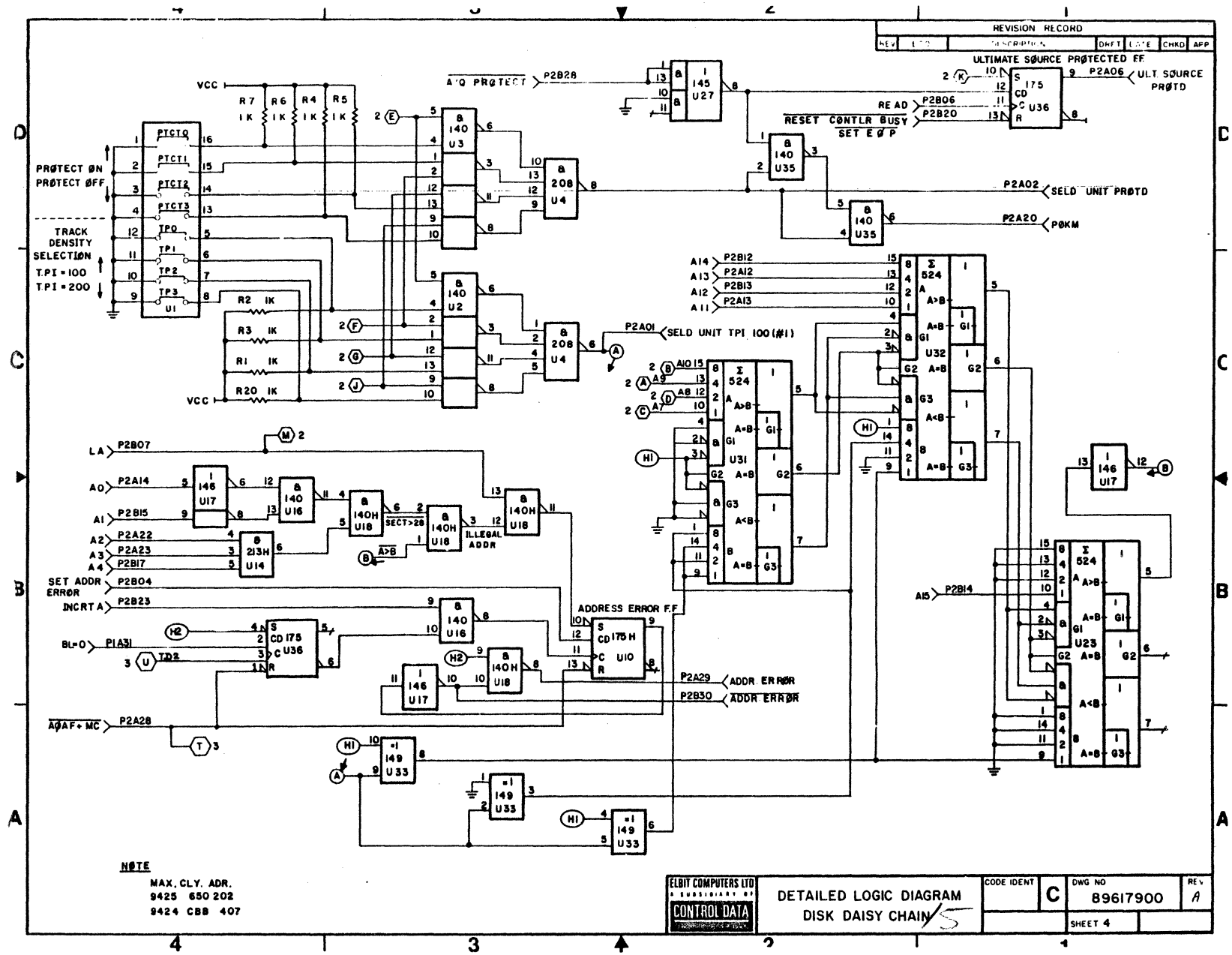
REV ECO DESCRIPTION DRFT DATE CHKD APP
Q10 P2A10
Q9 P2B10
Q8 P2A09
Q7 P2B09
EQUIPMENT NUMBER SELECTION
HD 0 SEL
U15
R17 1K
R23 1K
R22 1K
R21 1K
R16 1K
VCC
U24
U25
U34
P2A19 EQ. NO. MATCH
U33
P2A17 CAGSM (HEAD 0 SELECTION)
CA6 P2A06
T32 P2B29
TD1 P2B22
UNIT SEEK COMPLETE
TD1
TD2
RGTR 520 U8
RGTR 520 U9
U26
P2B24 SCOSE1
P2A24 SCOSE0
P2B25 SCOSE3
P2A25 SCOSE2
TØ STATUS
R26 100
R27 100
R28 100
R29 100
RCVR 902 U29
SEOSC2 P2B26
SEOSC1 P2A26
SEOSC4 P2B27
SEOSC5 P2A27
IOONS SEEK COMPLETE PULSE
EØPM F.F.
CD 175H U10
A0AF+MC
U35
P2B03 EØPM. CONTLR BUSY
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK DAISY CHAIN /5
CODE IDENT C
DWG NO 89617900
REV A
SHEET 3


REVISION RECORD
REV | DESCRIPTION | DRFT | DATE | CHKD | APP
ULTIMATE SOURCE PROTECTED FF
VCC
R7 1K
R6 1K
R4 1K
R5 1K
R2 1K
R3 1K
R1 1K
R20 1K
PROTECT ON
PROTECT OFF
TRACK DENSITY SELECTION
T.P.I = 100
T.P.I = 200
PTCT0
PTCT1
PTCT2
PTCT3
TP0
TP1
TP2
TP3
U1
A/Q PROTECT P2B28
READ P2B06
RESET CONTLR BUSY P2B20
SET E Ø P
P2A06 ULT. SOURCE PROTD
P2A02 SELD UNIT PROTD
P2A20 PØKM
P2A01 SELD UNIT TPI 100 (#1)
A14 P2B12
A13 P2A12
A12 P2B13
A11 P2A13
A10 P2B15
A9 P2A14
A8 P2A15
LA P2B07
A0 P2A14
A1 P2B15
A2 P2A22
A3 P2A23
A4 P2B17
SECT>28
ILLEGAL ADDR
A>B
SET ADDR ERROR P2B04
INCRT A P2B23
BL=0 P1A31
T2D2
ADDRESS ERROR F.F
P2A29 ADDR. ERROR
P2B30 ADDR. ERROR
A∅AF+MC P2A28
A15 P2B14
NOTE
MAX. CLY. ADR.
9425 650 202
9424 CBB 407
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
DISK DAISY CHAINS
CODE IDENT C
DWG NO 89617900
REV A
SHEET 4

SECTION 6

MAINTENANCE AND MAINTENANCE AIDS

SCOPE

This section gives maintenance references and procedures for the equipment listed in Section 1 of this manual.

TOOLS AND SPECIAL EQUIPMENT

The following is a list of maintenance tools required for this equipment.

Part Number	Part Description	Quantity
89688700	Board Extender	1
89670300	Board Extractor	1
	Tektronix 453 or Equivalent	1
	Voltmeter	1

The publications listed below are applicable to the equipment.

Publication	Pub. No.
1784 Computer Customer Engineering Manual	89633300
1784 Reference Manual	89633400
1700 Computer System Codes Manual	60163500
System Maintenance Monitor (SMM 17)	60182000

MAINTENANCE

Preventive maintenance of the controller is not required. After it is determined that the controller has failed, the controller PW board should be removed and replaced with an idential PW board. Failure should be located by removing and replacing each PW board with an identical problem-free board until the failed card is located. For removal and replacement of the card, refer to Section 3 of this manual. After replacement, a diagnostic check should be run.

SECTION 7

PARTS DATA

PARTS DATA

The following list is applicable to the FA716-A Cartridge Disk Drive Controller:

Designation/Assembly	Part Number
Disk Shifter PWA	89912100
Disk A/Q PWA	89778600
Disk DSA PWA	89864000
Disk Daisy Chain PWA	89897500
Disk Sector Count PWA	89897300
Internal Cable Assembly	89700200
External Cable Assembly	89700400
Interrupt Cable Assembly	89724702

SECTION 8

WIRE LIST

WIRE LIST

The included pin list is applicable to the FA716-A CDD Controller. Wire color, origin, destination and name of the signal normally found on that wire included in Table 8-1 for the internal cable and in Table 8-2 for the external cable.

TABLE 8-1. INTERNAL CABLE

CONDUCTOR IDENTITY	COLOR	ORIGIN	DESTINATION	REMARKS/ SIGNAL NAME
1	WHT-BLK	P2A01	1	$\overline{\text{SEØSC4}}$
2	BLK	GND	2	GND
3	WHT-BRN	P2A02	3	$\overline{\text{SEØSC3}}$
4	BLK	GND	4	GND
5	WHT-RED	P2A04	5	$\overline{\text{SEØSC2}}$
6	BLK	GND	6	GND
7	WHT-ORN	P2A05	7	TERM MØNITØR
8	BLK	P2A31	8	TERMINATØR PØWER
9	WHT-YEL	P2A06	9	$\overline{\text{SEØSCT}}$
10	BLK	GND	10	GND
11	WHT-GRN	P2A07	11	US4
12	BLK	GND	12	GND
13	WHT-BLU	P2A08	13	US3
14	BLK	GND	14	GND
15	WHT-VIO	P2A09	15	US2
16	BLK	GND	16	GND
17	WHT-GRA	P2A10	17	$\overline{\text{READ CLØCK}}$
18	BLK	GND	18	GND
19	WHT-BLK	P2A11	19	$\overline{\text{ØN CYL}}$
20	BRN	GND	20	GND
21	WHT-BRN	P2A12	21	$\overline{\text{INDEX}}$
22	BRN	GND	22	GND
23	WHT-RED	P2A13	23	$\overline{\text{SECTØR}}$
24	BRN	GND	24	GND
25	WHT-ORN	P2A14	25	$\overline{\text{UST}}$
26	BRN	GND	26	GND
27	WHT-YEL	P2A15	27	$\overline{\text{TA7}}$
28	BRN	GND	28	GND
29	WHT-GRN	P2A16	29	$\overline{\text{TA8}}$
30	BRN	GND	30	GND

CONT.

CONDUCTOR IDENTITY	COLOR	ORIGIN	DESTINATION	REMARKS/ SIGNAL NAME
31	WHT-BLU	P2A17	31	$\overline{W\emptyset}$
32	BRN	GND	32	GND
33	WHT-VIO	P2A18	33	$\overline{RG}$
34	BRN	GND	34	GND
35	WHT-GRA	P2A19	35	$\overline{HD.SEL.2^{0}}$
36	BRN	GND	36	GND
37	WHT-BLK	P2A20	37	$\overline{WG+EG}$
38	RED	GND	38	GND
39	WHT-BRN	P2A21	39	$\overline{TAT}$
40	RED	GND	40	GND
41	WHT-RED	P2A22	41	$\overline{TS}$
42	RED	GND	42	GND
43	WHT-ORN	P2A23	43	$\overline{HD.SEL.2^{0}}$
44	RED	GND	44	GND
45	WHT-YEL	P2A24	45	$\overline{TA2}$
46	RED	GND	46	GND
47	WHT-GRN	P2A25	47	$\overline{RTZS}$
48	RED	GND	48	GND
49	WHT-BLU	P2A26	49	$\overline{TA0}$
50	RED	GND	50	GND
51	WHT-VIO	P2A27	51	$\overline{TA3}$
52	RED	GND	52	GND
53	WHT-GRA	P2A28	53	$\overline{TA5}$
54	RED	GND	54	GND
55	WHT-BLK	P2A29	55	$\overline{TA6}$
56	ORN	GND	56	GND
57	WHT-BRN	P2A30	57	$\overline{TA4}$
58	ORN	GND	58	GND
59	WHT-RED	P2B11	59	$\overline{RD}$
60	ORN	GND	60	GND

CONT.

TABLE 8-1. INTERNAL CABLE (Cont'd.)

CONDUCTOR IDENTITY	COLOR	ORIGIN	DESTINATION	REMARKS/ SIGNAL NAME
61	WHT-ORN	P2B12	61	$\overline{\text{READY}}$
62	ORN	GND	62	GND
63	WHT-YEL	P2B23	63	$\overline{\text{FAULT}}$
64	ORN	GND	64	GND
65	WHT-GRN	P2B24	65	$\overline{\text{SEEK ERRØR}}$
66	ORN	GND	66	GND

TABLE 8-2. EXTERNAL CABLE

CONDUCTOR IDENTITY	COLOR	ORIGIN	DESTINATION	REMARKS/ SIGNAL NAME
1	WHT	CF	1	$\overline{\text{SEØSC4}}$
	BLK	CH	2	GND
2	ORN	BW	3	$\overline{\text{SEØSC3}}$
	BLK	CE	4	GND
3	RED	CB	5	$\overline{\text{SEØSC2}}$
	BLK	CC	6	GND
4	YEL	AH and Y	7	TERM MØNITØR
	BLK	CW	8	TERM PØWER
5	BRN	BZ	9	$\overline{\text{SEØSCT}}$
	BLK	CA	10	GND
6	BLU	BS	11	$\overline{\text{US4}}$
	BLK	BY	12	GND
7	GRN	BU	13	$\overline{\text{US3}}$
	BLK	BT	14	GND
8	VIO	BN	15	$\overline{\text{US2}}$
	BLK	BV	16	GND
9	ORN	AZ	17	$\overline{\text{READ CLØCK}}$
	WHT	BA	18	GND
10	RED	BD	19	$\overline{\text{ØN CYL}}$
	WHT	BE	20	GND
11	YEL	BF	21	$\overline{\text{INDEX}}$
	WHT	BP	22	GND
12	BRN	BL	23	$\overline{\text{SECTØR}}$
	WHT	BM	24	GND
13	BLU	BR	25	$\overline{\text{UST}}$
	WHT	BX	26	GND
14	GRN	T	27	$\overline{\text{TA7}}$
	WHT	S	28	GND
15	VIO	R	29	$\overline{\text{TA8}}$
	WHT	X	30	GND

CONT.

TABLE 8-2. EXTERNAL CABLE (Cont'd.)

CONDUCTOR IDENTITY	COLOR	ORIGIN	DESTINATION	REMARKS/ SIGNAL NAME
16	ORN	AS	31	$\overline{WO}$
	BLU	AT	32	GND
17	RED	AV	33	$\overline{RG}$
	BLU	AW	34	GND
18	YEL	AC	35	$\overline{HD.SEL.2^{\circ}}$
	BLU	AD	36	GND
19	BRN	AM and AP	37	$\overline{WG+EG}$
	BLU	AN and AR	38	GND
20	GRN	E	39	$\overline{TAT}$
	BLU	F	40	GND
21	VIO	A	41	$\overline{TA8}$
	BLU	B	42	GND
22	GRN	AE	43	$\overline{HD.SEL.2^{\circ}}$
	RED	AF	44	GND
23	YEL	H	45	$\overline{TA2}$
	RED	J	46	GND
24	BRN	AA	47	$\overline{RTZS}$
	RED	AB	48	GND
25	ORN	C	49	$\overline{TA0}$
	RED	D	50	GND
26	VIO	K	51	$\overline{TA3}$
	RED	L	52	GND
27	YEL	P	53	$\overline{TA5}$
	GRN	W	54	GND
28	ORN	V	55	$\overline{TA6}$
	GRN	U	56	GND
29	VIO	M	57	$\overline{TA4}$
	GRN	N	58	GND
30	BRN	AU	59	$\overline{RD}$
	GRN	AY	60	GND

CONT.

TABLE 8-2. EXTERNAL CABLE (Cont'd.)

CONDUCTOR IDENTITY	COLOR	ORIGIN	DESTINATION	REMARKS/ SIGNAL NAME
31	VIO	AX	61	$\overline{\text{READY}}$
	BRN	BC	62	GND
32	ORN	BB	63	$\overline{\text{FAULT}}$
	BRN	BH	64	GND
33	YEL	BJ	65	$\overline{\text{SEEK ERRØR}}$
	BRN	BK	66	GND

COMMENT SHEET

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CUSTOMER ENGINEERING MANUAL

PUBLICATION NO. 89638100 REVISION C

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