Burroughs

# B 5282

## INPUT / OUTPUT SUB-SYSTEM

TECHNICAL MANUAL

Burroughs

B 5000 DATA PROCESSING SYSTEM

PRINTED IN U.S.A. 3/16/64 B 5282.51

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

# LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1

# PREVENTIVE MAINTENANCE

## 1.1 DAILY

(Not Applicable)

## 1.2 WEEKLY

CHECKS

Voltage Regulator for proper voltage settings. Refer to Subject 5.5 of the B 5370 Power Supply Manual.

## 1.3 MONTHLY

FAN SCREENS & FILTERS

1. Clean all fan screens.
2. Inspect air filters and replace if necessary.

CHECKS

1. Clock pulse width (Subject 3.3).
2. Clock line variable bias (Subject 3.2).
3. All multivibrators for proper setting (Subject 3.4).
4. All delay circuits for proper settings (Subject 3.5).

## 1.4 QUARTERLY

CHECKS

1. Over and Under Voltage Sensing. Vary the -12V, -4.5V and 1.2V at the regulator and assure that power drops when the voltage is varied plus or minus 10%. (Refer to Subject 5.6 of the B 5370 Power Supply Manual.)

2. Excessive ripple in all DC voltages. (Refer to Subject 5.6 of the B 5370 Power Supply Manual.)

## 1.5 SEMI-ANNUALLY

FAN LUBRICATION

Lubricate Rotron Muffin fans with Anderol L-826 using special oil injector.

Oil Injector...............Pt. No. 11838588

Oil........................Pt. No. 11838596

PROCEDURE

The exhaust fans are lubricated by inserting the Oil Injector needle through a self-sealing rubber cap located in the center of the motor hub.

Note that on most units a Gold Seal label is mounted over the rubber plug; this series of fans is called the Gold Seal series.

1. Fan grill, remove and clean as necessary.

2. Remove air from Oil Injector by holding the needle up and pressing on the plunger.

3. Place Oil Injector needle at the center of circle marked on the Gold label (on the 034 series place needle approximately 1/8" from the edge of the rubber cap).

4. Position the needle at an angle of approximately 45° to the surface of the label and point it toward the center of the rubber cap.

5. Pierce the label and the concealed self-sealing rubber cap located under the label.

6. Insert the needle approximately 1/4".

7. Depress the plunger of the Oil Injector to allow approximately 1/16" of oil to escape. Rotating the fan will relieve air pressure and allow oil to flow into the oil chamber.

# SECTION 2

## TROUBLESHOOTING

### 2.1 INTRODUCTION

The following section contains descriptions of methods, procedures, aids and tools recommended to be used while troubleshooting the B 5282 I/O Sub-System.

## 2.2 SWITCHES & INDICATORS

Refer to Section 2 of the B 5290 D&D Manual for a description of all I/O Control Unit panel switches and indicators.

## 2.3 SPECIAL TOOLS

In addition to the normal tools provided for maintenance of the B 5282 I/O Sub-System, the following special tools are also provided:

1. Diode-stick cutters.

2. Wire-wrap tools.

3. Cover-removal tool.

4. Package handles.

DIODE STICK CUTTING TOOL (P/N 11838109)

The Diode Sticks provided as spares are uncut. The diode stick cutter is a plier-like device which can be used to cut the diode sticks as needed. Care must be taken when using the cutter to keep from breaking the bond between the diodes or resistors and the common bus. <u>The diode-stick tool must not be used for any other purpose</u>.

WIRE UNWRAP TOOL (P/N 11838058)

The hand unwrapping tool (see Figure 2.3-1) is used when it is necessary to remove a wire from a pin. The tool has two ends; one end is for wires which are wrapped in a clockwise direction; the other end is for wires which are wrapped in a counter-clock-wise direction. To use this tool, proceed as follows:

1. Determine the direction of wrap and insert the appropriate end of the tool over the pin.

2. Rotate the tool until the wire is sufficiently uncoiled so that it can be removed from the pin.

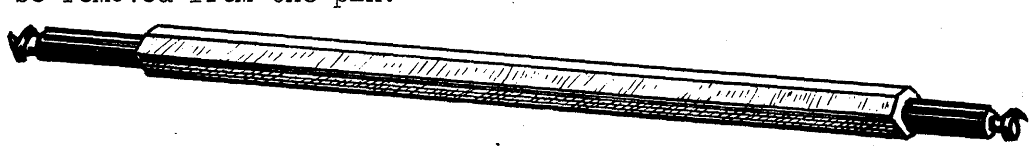


FIGURE 2.3-1 DUAL, RIGHT AND LEFT NO. 2 UNWRAPPING TOOL

WIRE WRAP TOOL (P/N 11838042)

The wire-wrap tool is a hand-wrapping tool and is shown in Figure 2.3-2. The tool will wrap a standard field change wire.

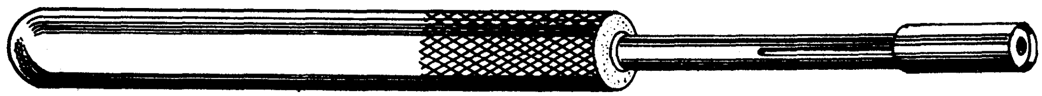


FIGURE 2.3-2 WIRE WRAP TOOL

Figure 2.3-3, A through F, shows the steps used to wrap a connection. If a wire was previously wrapped, the portion of the wire which was wrapped cannot be used again.

If the old wire is not long enough to strip off enough insulation to permit another wrap, a new wire must be routed in its place. To wrap a new wire, proceed as follows:

1. Remove the insulation from the end of the wire. Approximately 1 1/2" of wire is required for a six-turn connection of 24-guage wire.

2. Place the tool over the wire as shown in Figure 2.3-3B.

3. Anchor the wire as shown in Figure 2.3-3C and insert the tool over the pin as shown in Figure 2.3-3D.

4. Rotate the tool in a clockwise direction. The wire will wrap around the pin as shown in Figure 2.3-3E and F. Too much pressure will cause the wire to bunch.

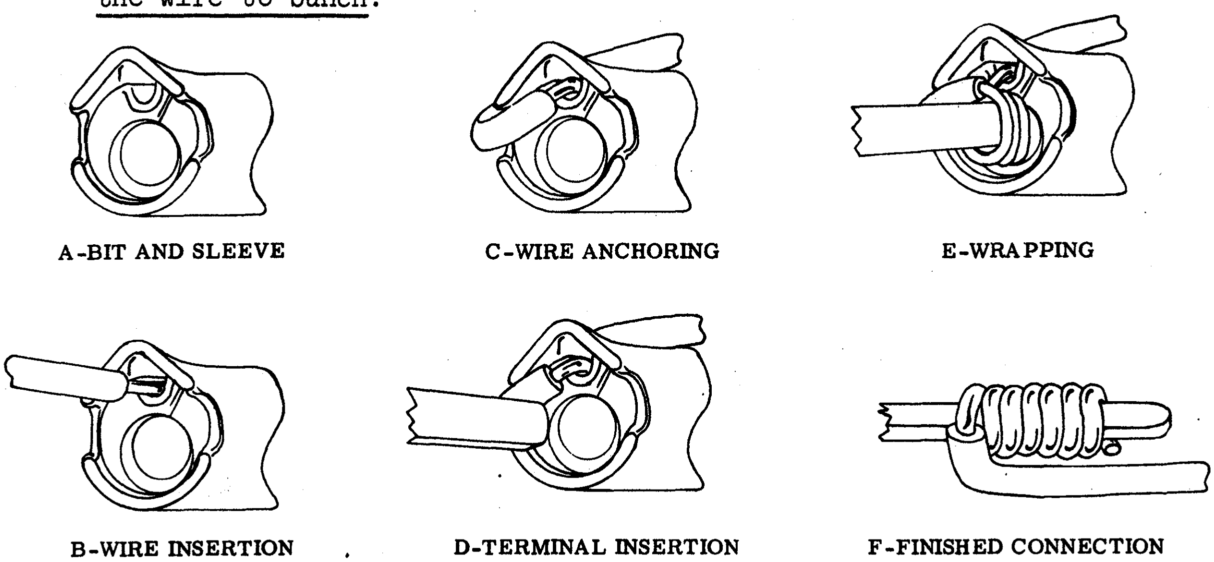



FIGURE 2.3-3 WIRE WRAPPING

The following should be used as a guide when installing FCNs, or when making wire wrap changes in the field.

1. Number of turns - The minimum number of turns (per connection) of bare wire is FIVE, and the maximum number is SEVEN. The maximum number of turns of insulation preceding the bare wire is THREE for any connection.

2. Insufficient Insulation - Wire insulation shall be no greater than 1/32" from wire wrap connections.

3. Wire and Terminal Contact - The bare wire and terminal must make contact on all corners following the point at which the origin of the number of turns is counted.

4. Separation of Turns - Turns may have a maximum separation of 1/2 the thickness of wire being used to make the wrapped connection.

5. Excessive Tail Wire - The wire tail shall be construed as being "That end of bare wire which follows the last wrap." The wire tail shall be parallel to the terminal surface within 1/32".

6. Overlapping of Turns - This condition is caused when succeeding wraps overlap the ones previously made. If this condition exists, it will be necessary to make a new connection.

7. Clearance - There shall be at least 1/32" clearance between grid pattern connections, terminals, bare wire or components.

8. Height - The maximum clearance between the connector block and the first turn of the first connection shall be 1/16".

9. Height for Single Wire Wrap - The maximum height for a single wire wrap shall be 1/4".

10. Height for Two Wire Wraps - The maximum height for two wire wrap connections shall be 1/2".

11. Unwrapping - The wire wrap connection shall be capable of being unwrapped from the wire wrap terminal without breaking. The unwrapping operation shall be done with a standard unwrapping tool only, so as to insure the life of the wire wrap terminal.

12. Wire Re-use - IF A WIRE WAS PREVIOUSLY WRAPPED, THE PORTION OF THE WIRE WHICH WAS WRAPPED CANNOT BE USED AGAIN. If the old wire is not long enough to strip off enough insulation to permit another wrap, a new wire must be routed in its place. Soldering a wire wrapped connection directly at the wire wrapped terminal shall not be permitted at any time.

13. Terminal Re-use - Prior to rewrapping, the terminal shall be inspected for planting loss, corrosion or other damage. The evidence of any damage, planting loss or corrosion will in effect cause the wire connection not to maintain the high degree of quality and reliability which is required. The terminal therefore, must be replaced with a new terminal.

COVER-REMOVAL TOOL (P/N 80551)

The cover-removal tool is a 3/8" Allen-set-screw wrench. The short end is cut off to approximately 1/2" and a plastic handle is inserted on the long portion of the wrench.

PACKAGE HANDLES (P/N 77213)

Special non-conduction handles are provided for use in removing sticks. These handles must be removed from the stick before the gates are closed.

## 2.4 MAINTENANCE AIDS

INTRODUCTION

The I/O Control Unit is provided with several maintenance switches which can be used at the discretion of the field engineers to check out the unit. These switches may be used for "On Line" or "Off Line" maintenance.

This section lists the rules for using the maintenance switches plus suggested methods of use.

PROCEDURE

Suggested rules for use of maintenance switches.

"On Line" and "Off Line" Maintenance

1. "On Line" maintenance is any maintenance on the I/O Control Unit while another portion of the B 5000 system is being used for productive purposes.

   The I/O Control Unit has the capability of being placed in local mode, independent of system control and unavailable for system use. While in this mode an I/O Control Unit may be used to control repetitive operation of any peripheral unit for diagnostic purposes, in such a way that it will not interfere with normal operation of the remainder of the system. "On Line" maintenance requires skillful and careful use of the maintenance controls in the I/O Control Unit to avoid inadvertently addressing a peripheral unit in use by the system, or otherwise interfering with system operation. It is not, therefore, recommended as a normal mode of maintenance.

2. "Off Line" maintenance is any maintenance on a B 5000 system while no production is being run on said system.

List of switches available.

1. Operation Recycle.
2. Memory Cycle.
3. Key Memory.
4. Memory Access.
5. Stop on Error.

6. Local/Remote.

7. Start Switch.

8. Input/Output Clear.

9. "W" - Register Clear.

10. "D" - Register Clear.

11. Bit Reset.

12. Bit Clear/Set (Neon Indicator Switch).

Rules for using the switches during "On Line" maintenance.

1. Switches that <u>cannot</u> be used.

    a. Key Memory.

    b. Any Bit Clear/Set Switch of the "D" Register.

2. Switches that <u>must be</u> in the position stated.

    a. Memory Access - Up.

    b. Local Remote - Up.

3. Switches that <u>may be</u> used in either position or depressed at any time.

    a. Operation Recycle.

    b. All Bit Clear/Set Switches except those of the "D" - Register.

    c. Memory Cycle.

    d. Start Switch.

    e. Input/Output Clear.

    f. "W" Register Clear.

    g. "D" Register Clear.

    h. Bit Reset.

    i. Stop on Error.

Rules for using the switches during "Off Line" maintenance.

1. All switches may be used as described at any time.

2. Causes a jump directly to SC=9 from SC=0.

3. Causes a jump directly to SC=0 from SC=10.

d. The Operation Recycle Switch being Up does the following:

1. Allows IMCF to be set when the following conditions are true.

   a. S10D

   b. AOFF'

   c. Memory Cycle Switch Up.

e. If D24F is "ON", a simulated write will occur into the Memory cell designated by the "D" register. If D24F is "OFF", a simulated Read will occur from the Memory cell designated by the "D" register.

f. The depression of the Start Switch starts the operation.

"Off Line" Maintenance Cycle

Refer to Maintenance Operation Cycle Flow Chart C-11852324A.

1. To check all control logic used with a particular I/O Descriptor, whose address is stored in Memory cell No. 8, during "Off Line" maintenance:

   a. Store the I/O Descriptor to be checked in a Memory cell. (Use procedure 2.4.D.2).

   b. Store the address of the Descriptor just stored in Memory cell No. 8. (Use procedure 2.4.D.3).

   c. <u>Local/Remote Switch</u> - Up.

   d. <u>Memory Access Switch</u> - Down.

   e. <u>Key Memory</u> - Down.

   f. <u>Memory Cycle</u> - Down.

   g. <u>Operation Recycle</u> - Up or Down.

   h. <u>Stop on Error</u> - Up or Down.

   i. Depress the Start Switch.

2. The above steps allow a normal function of an I/O Descriptor in the local mode.

"Off Line" Maintenance Memory Cycle

1. To check all Control Logic occurring at SC=9 and 10, except operational jumpouts, of any I/O Descriptor during "Off Lines" maintenance.

    a. Local/Remote - Up.

    b. Memory Access - Down.

    c. Key Memory - Down.

    d. Stop on Error - Up or Down.

    e. Memory Cycle - Up.

    f. Operation Recycle - Up or Down, depending on operation desired.

    g. Turn D24F "ON" for a Memory Read operation, turn D24F "OFF" for a Memory Write operation.

    h. Depress the Start Switch.

2. Storing an I/O Descriptor in Memory.

    a. Local/Remote - Up.

    b. Memory Access - Down.

    c. Memory Cycle - Up.

    d. Operation Recycle - Down.

    e. Key Memory - Down.

    f. Stop on Error - Up or Down.

    g. Load the "W" Register with the I/O Descriptor to be stored.

    h. Turn "ON" D24F.

    i. Set the desired Memory Address in D01F through D15F.

    j. Depress the Start Switch.

3. Storing an I/O Descriptor Address in Memory.

    a. Local/Remote - Up.

    b. Memory Access - Down.

    c. Memory Cycle - Up.

d. Key Memory - Down.

e. Stop on Error - Up or Down.

f. Operation Recycle - Down.

g. Load the "W" Register with the desired Descriptor address.

h. Set D24F and D04F.

i. Depress the Start Switch.

4. Reading the Result Descriptor from Memory Cells 12, 13, 14 or 15.

a. Local/Remote - Up.

b. Memory Access - Down.

c. Memory Cycle - Up.

d. Operation Recycle - Down.

e. Key Memory - Down.

f. Stop on Error - Up or Down.

g. Set up the Memory Address in D01F, D02F, D03F and D04F.

h. Clear the "W" Register.

i. Depress the Start Switch.

5. Keying Memory with its own address.

a. Local/Remote - Up.

b. Memory Access - Down.

c. Memory Cycle - Up.

d. Operation Recycle - Up.

e. Key Memory - Up.

f. Stop on Error - Up or Down.

g. Set the starting address in the "D" and "W" Registers.

h. Turn D24F on.

i. Depress the start switch.

The above suggestions are but a few of the many variations that can be made to satisfy the needs of the field engineer when checking and troubleshooting the I/O Control Unit and its associated peripheral units.

## 2.5 PRECAUTIONS

The following precautions are recommended to be observed when troubleshooting the I/O Control Unit.

1. Do not use a battery-buzzer for continuity checking. The buzzer current exceeds the maximum current rating for diodes and transistors in the system.

2. Do not use the first two low scales (X1 or X10) on the Triplett ohmmeter for continuity checking. For these scales, the meter current exceeds the maximum current rating for diodes and transistors in the system.

3. Do not remove packages or diode sticks when Power is Up.

4. Care must be taken when using Scope or Jumper Clip Leads to prevent touching adjacent pins. Use Minigator Clips with insulators or the Wire Wrap Pin Probe Tip (Part No. 11838547).

5. Use extreme caution when working on the plug-in side of the panels. Avoid hitting packages when moving the scope.

6. Do not attempt to force a TRUE level with -12V. In all cases, the desired effect can be obtained either by the use of a ground clip, or by taping off one or more diodes.

7. A ground jumper may be used to force a FALSE level.

NOTE

Connect clip to the point to be grounded prior to making ground connection.

8. Do not pull Cable Plugs with POWER ON at either end of the cable.

9. Only soldering irons that have an isolation transformer may be used.

10. Scope ground - to prevent ground loops and noise interference use only the ground clip on the scope probe. Attach it to a suitable ground as near as possible to the point being observed.

## 2.6 HINTS

INTRODUCTION

This section contains hints which may be used to check certain operations and/or locate troubles within the I/O Unit or a peripheral unit used with an I/O Unit.

MAGNETIC TAPE SKEW

A quick means of checking the skew of each MTU on the system follows below:

1. Perform a continuous read (Hi or Lo density) from the MTU to be checked.
2. Scope the output of TRPS (AA A4 W5).
3. The time that TRPS is true is the skew time per character. This time should not exceed 4.5 μs maximum and 1.5 μs minimum.
4. If the skew does not meet these requirements, refer to the Magnetic Tape Unit Technical Manual B 421.51 for the adjustment procedure.

## 2.7 RIN INDEX

RIN INDEX FOR THE B 5282 INPUT/OUTPUT SUB-SYSTEM (11831476)

| RIN NO. | INSTAL. TIME IN HOURS | PRE-REQUISITE | UNITS EFFECTED | DESCRIPTION |
|---|---|---|---|---|
| 5028 | 1.0 | | 102 ⇒ UP | Extends lower limit of the -4.5V regulator. |
| 5094 | 4.0 | | 102 ⇒ UP | Plug-in heatsink replacement to prevent the shorting of the collectors in common heatsinks. |
| 5094S1 | 1.0 | | 102 ⇒ UP | Supply transistors for installation of RIN 5094. |
| 5125 | 0.5 | | 102 ⇒ UP | Revised Magnetic Tape Flow Charts. These reflect changes incorporated by RIN 5116. |

RIN INDEX FOR THE B 5283 I/O CONTROL UNIT, MODEL 1, (78496)

| RIN NO. | INSTAL. TIME IN HOURS | PRE-REQUISITE | UNITS EFFECTED | DESCRIPTION |
|---|---|---|---|---|
| 5005 | 2.0 | | 102 ⇒ 122 | Improve the manner with which the cables are secured. |
| 5013 | 0.5 | | 102 ⇒ 122 | Correct wiring discrepancies. |
| 5015 | 3.5 per I/O | | 102 ⇒ 122 | AND stick cut changes and DA index correction. |
| 5015S1 | 3.5 per I/O | replaces 5015 | 102 ⇒ 122 | (Same as RIN 5015) |
| 5017 | 1.0 | | 102 ⇒ 122 | Tape multi timing changes. |
| 5018 | 1.5 | | 102 ⇒ 122 | Instructs electrical, mechanical and clerical changes to I/O. |
| 5018S1 | 1.5 | corrects 5018 | 102 ⇒ 122 | (Same as RIN 5018) |
| 5018S2 | 2.5 | replaces 5018 & S1 | 102 ⇒ 122 | (Same as RIN 5018) |
| 5020 | 1.0 | 5018S2 | 102 ⇒ 122 | "Z" level corrections. |
| 5021 | 1.5 | 5020 | 102 ⇒ 122 | Corrects errors in back-plane wiring. |
| 5021S1 | 0.5 | corrects 5021 | 102 ⇒ 122 | (Same as RIN 5021) |
| 5027 | 0.5 | | 102 ⇒ 122 | Update and revise I/O Flow Charts. |
| 5032 | 3.5 | 5021S1 | 102 ⇒ 122 | Corrects missing -12V to stick at ABD3IO; adds inter-lock logic to Drive Conflict Switch; improves Paper Tape logic. |
| 5032S1 | 6.0 | corrects 5032 | 102 ⇒ 122 | (Same as RIN 5032) |
| 5042 | 11.0 | 5032S1 | 102 ⇒ 122 | Implements the backspace lines for Paper Tape Readers. |
| 5052 | 1.0 | | 102 ⇒ 122 | Replace clock cables with standard types. |

| RIN NO. | INSTAL. TIME IN HOURS | PRE-REQUISITE | UNITS EFFECTED | DESCRIPTION |
|---|---|---|---|---|
| 5076 | 0.1 per cable | | 102 ⇒ 122 | Key pin support for all yellow and green single key pin cable connectors. |
| 5099 | 21.5 | 5042 | 102 ⇒ 122 | Installs changes to Paper Tape logic; removes Magnetic Tape turn-around logic; corrects logic for selection of B 304 Auxiliary Stacker; and installs Memory Race change. |
| 5100 | 4.0 | | 102 ⇒ 122 | Provide a quad connector retaining device to insure proper seating of the connector. |

RIN INDEX FOR THE B 5283 I/O CONTROL UNIT, MODEL 2 (11975331)

| RIN NO. | INSTAL. TIME IN HOURS | PRE-REQUISITE | UNITS EFFECTED | DESCRIPTION |
|---|---|---|---|---|
| 5045 | 1.0 | | 123 ➡ UP | "Z" level corrections for logic installed while implementing backspace logic for Paper Tape. |
| 5076 | 0.1 per cable | | 123 ➡ UP | Key pin support for all yellow and green single key pin cable connectors. |
| 5090 | 1.0 | 5045 | 123 ➡ UP | Correct cuts on diode sticks at AEB7Y8 and AEB8Y8. |
| 5098 | 44.0 | 5090 | 123 ➡ UP | Install wiring changes for Disk File and Data Communication implementation; remove Magnetic Tape turn-around logic; correct B 304 Auxiliary Stacker selection logic; plus miscellaneous wiring changes. |
| 5100 | 4.0 | | 123 ➡ UP | Provide a quad connector retaining device to insure proper seating of the connector. |
| 5109 | 3.0 | | 123 ➡ UP | Modify Processor Interrogate logic; correct a Disk File Logic error; correct logic error induced by the addition of the Memory Race change. |
| 5109S1 | 6.0 | 5098 | 123 ➡ UP | Installs Memory Race change in its entirety plus makes other changes listing under RIN 5109. |
| 5115 | 0.5 | | 123 ➡ UP | Revised released I/O Equation Book. |
| 5116 | 18.0 | | 123 ➡ UP | Incorporates logical changes for detecting Magnetic Tape dropouts, and alleviate character shift problem. |
| 5128 | 0.5 | 5116 | 123 ➡ UP | Revised pages to updated all I/O, Model 2 Documents. |

# SECTION 3

## ADJUSTMENTS

### 3.1 INTRODUCTION

The following section contains the necessary instructions for making all adjustments within the I/O Sub-System.

## 3.2 VARIABLE BIAS

PROCEDURE

To adjust the Variable Bias follow the procedure given below.

1. Set the clock to "Single Pulse" at the CC Control Panel in D&D.

2. Adjust the bias level at the Variable Bias packages to obtain -0.5V measured at the associated local driver input listed below.

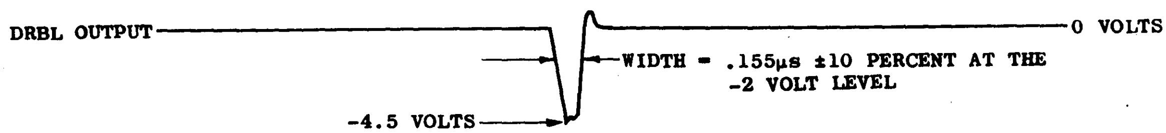
   a. VB Pkg. AA C7 N7 measure at AA B1 P8.

   b. VB Pkg. AC B8 A7 measure at AC B1 P7.

   c. VB Pkg. AE C7 N2 measure at AE B2 P1.

## 3.3 CLOCK PULSE WIDTH

With the Clock Mode Switch on the CC Control Panel in the "normal" position, and the scope connected to EA D3 RO (CC), adjust the potentiometer on package EA D2 N2 (CC) to obtain a pulse width of .155 µs at the -2V level using the pulse diagram shown below as a guide.



## 3.4 MULTIVIBRATORS

The adjustment of the I/O Multivibrators is performed during a series of tape operations. The table below lists the particular tape operation to be performed, the scope sync point, the multi output point and the multi timing for each multi to be adjusted:

TABLE 3.4-1 MULTIBIBRATOR TIMING

| NAME | SYNC POINT | OUTPUT | TIMING | TAPE OPERATION |
|---|---|---|---|---|
| BF1M | AB C2 U4 | AB B4 U0 | 96 µs | BACKWARD READ (HI DENSITY) |
| BF2M | AB C2 U4 | AB B4 F0 | 250 µs | BACKWARD READ (LO DENSITY) |
| BTDM | AA D8 P2 | AD B0 F0 | 6.6 ms | CONTINUOUS WRITE (HI OR LO DENSITY) |
| BWIM | AA B6 U0 | AA B6 U0 | 1.4 ms | CONTINUOUS BACKWARD READ (HI DENSITY) |
| DS1M | AA A4 W5 | AA B7 U0 | 6.0 µs | CONTINUOUS WRITE (HI DENSITY) |
| DS2M | AA A4 W5 | AA B7 F0 | 17 µs | CONTINUOUS WRITE (LO DENSITY) |
| LPIM | AA D7 P2 | AA B8 U0 | 15 ms | REWIND FOLLOWED BY A READ |
| LP1M | AB C2 U4 | AA B8 F0 | 300 µs | CONTINUOUS WRITE (HI DENSITY) |
| LP2M | AB C2 U4 | AA B9 F0 | 850 µs | CONTINUOUS WRITE (LO DENSITY) |
| WGBM | AA D7 P2 | AA B4 F0 | 67 ms | REWIND FOLLOWED BY A WRITE |
| WGNM | AA D7 P2 | AA B4 U0 | 4.4 ms | CONTINUOUS WRITE (HI OR LO DENSITY) |
| LD1M | | AA A9 U5 | 21 µs | LOST DIGIT (HI DENSITY) |
| LD2M | | AB A0 U0 | 60 µs | LOST DIGIT (LO DENSITY) |

## 3.5 DELAY CIRCUITS

The adjustment of the I/O delay circuits is performed during a series of tape operations. The procedure for making these adjustments is given below:

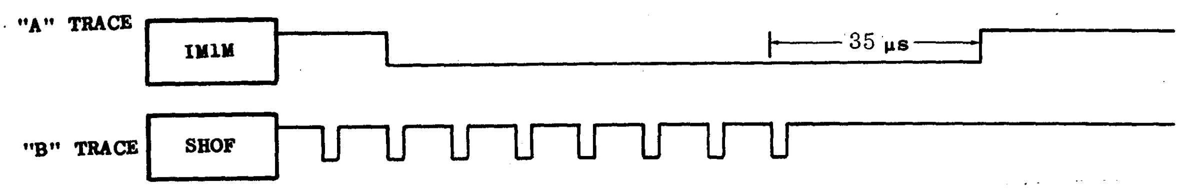
IM1M

1. Connect the scope sync to AA A4 W5 (TRPS), the "A" trace to AA B6 FO (IM1M) and the "B" trace to AA C9 F4 (SHOF).

2. Perform a continuous Hi Density write operation of a short record.

3. Set the scope for a chopped display and adjust the time base to display the complete record.

4. The "A" trace will show IM1M and the "B" trace will show SHOF. Adjust IM1M to time out 35 µs after the last time SHOF is turned "ON" as shown below:



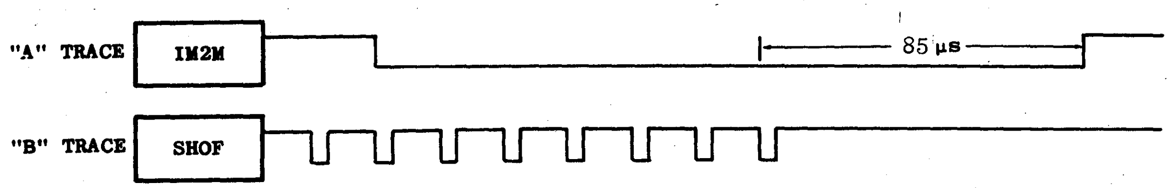

IM2M

1. Connect the scope sync to AA A4 W5 (TRPS), the "A" trace to AA B6 F5 (IM2M) and the "B" trace to AA C9 F4 (SHOF).

2. Perform a continuous Lo Density write operation of a short record.

3. Set the scope for a chopped display and adjust the time to display the complete record.

4. The "A" trace will show IM2M and the "B" trace will show SHOF. Adjust IM2M to time out 85 µs after the last time SHOF is turned "ON" as shown below:



BRIM

1. Sync the scope on the input going position (ABB4A7).
2. Connect the scope to AA B4 E9 (BRIM).
3. Perform a write followed by a backward read.
4. Adjust BRIM to time out in 6.6 ms.

## 3.6 VOLTAGE REGULATOR

Refer to Subject 5.5 of the B 5370 Power Supply Manual for the procedure used to adjust the Voltage Regulator.

# SECTION 4

## ASSEMBLY AND DISASSEMBLY

### 4.1 VOLTAGE REGULATOR

Refer to Section 4 of the B5370 Power Supply Manual for the procedure to disassemble and assemble the Voltage Regulator.

## 4.2 WIRE WRAP PINS

REMOVAL

1. Remove wires with unwrapping tool.

2. If pin is bent, straighten it with long nose pliers.

3. Push on pin from the wire side with long nose pliers. As soon as the pin clears the block (package side), grasp the pin with the pliers and pull it out.

4. If the pin is broken off flush with the pin block, use a small drift punch or another pin held with a pliers to drive the pin out.

REPLACEMENT

1. Insert the pin in the block from the package side of the gate. Make sure that the pin is inserted correctly (the contact side of the pin points away from the slot on the side of the pin hold).

2. Take the long-nose pliers and pull on the pin from the wire side until the pin is even with adjacent pins. Do not pull it too far or the pin block may be damaged.

NOTE

The M row pins are U shaped and do not extend through to the package side.

## 4.3 PACKAGES

Packages, diode sticks, and resistor sticks are removable. Handles are provided which fit on the extensions.

CAUTION

These handles must be removed from the sticks before the gate is closed.

WARNING

Power must be OFF before removing any element.

SECTION 5

# INSTALLATION

## 5.1 INTRODUCTION

The B5000 I/O Sub-System is that part of the B5000 System which contains from one to four I/O Control units. These units control the transfer of data to and from all peripheral units.

The instructions within this section apply to installing any I/O Sub-System from minimum to maximum configuration, plus instructions for adding additional I/O Control units to a non-maximum system.

The instructions assume that site preparation has been completed in accordance with customer specifications and pre-installation planning. They also assume that all packing material used for shipping has been removed, discarded, or returned, as directed.

## 5.2 POWER CONNECTIONS

The B5282 I/O Sub-System contains the Voltage Regulator which supplies power to all I/O Control units within the I/O Sub-System.

The Voltage Regulator receives its power via cables from the Distribution Panel within the Display and Distribution Unit.

NOTE

> The Display and Distribution Unit, Power Supply and the Central Control Unit installation must be performed prior to installing the I/O Sub-System in order to provide power voltage sensing for the I/O Sub-System.

1. Refer to Section 5 of the B5370 Power Supply Manual for the installation and check-out procedure for I/O Sub-System Voltage Regulator.

## 5.3 I/O-1 POWER AND INFORMATION CABLING

Install cables as listed in Table 5.3-1.

TABLE 5.3-1 I/O-1 Power and Information Cabling

| CABLE NO. | FUNCTION | FROM | | TO | | VIA TRAY |
|---|---|---|---|---|---|---|
| | | UNIT | CONNECTOR | UNIT | CONNECTOR | |
| 3-1 | INPUT LINES | I/O-1 | AC DO A7 | CC | EC AO A2 | 3F |
| 4-1A | MEMORY READ EXCHANGE | I/O-1 | AE AO N2 | CC | AC CO A7 | 7R |
| 4-1B | MEMORY READ EXCHANGE | I/O-1 | AE BO N2 | CC | AC CO N7 | 7R |
| 5-1A | MEMORY WRITE EXCHANGE | I/O-1 | AE CO N7 | CC | BA CO A2 | 5R |
| 5-1B | MEMORY WRITE EXCHANGE | I/O-1 | AE DO A7 | CC | BA CO N2 | 5R |
| 6-1 | OUTPUT LINES | I/O-1 | AC BO A7 | CC | EC AO N2 | 3F |
| 24-28 | HEAT & E.C. SENSE | I/O REG. | CT K1 02 | I/O-1 | AC C1 L7 | 1R |
| 29-1 | INDICATOR INPUT | I/O-1 | AA BO A2 | D & D | AY J1 | 3F |
| 30-1 | INDICATOR INPUT | I/O-1 | AC CO A2 | D & D | AY K1 | 3F |
| 31-1 | INDICATOR INPUT | I/O-1 | AE CO N2 | D & D | AY L1 | 3F |
| 32-1 | INDICATOR INPUT | I/O-1 | AE DO N2 | D & D | AY M1 | NT |
| 33-1 | MANUAL CONTROL | I/O-1 | AA BO N2 | D & D | AY N1 | 3F |
| 34-1 | MANUAL CONTROL | I/O-1 | AC CO N2 | D & D | AY P1 | 3F |
| 35-1 | MANUAL CONTROL | I/O-1 | AE CO A2 | D & D | AY R1 | 3F |
| 36-1 | MANUAL CONTROL | I/O-1 | AE DO A2 | D & D | AY S1 | 3F |
| 65-1 | DISPLAY POWER | D & D | AE AO N2 | D & D | AY T1 (A GATE) | NT |
| 141-1 | POWER | I/O REG. | CS 01 | I/O-1 | AA CO A7 | 1F |
| 142-1 | POWER | I/O REG. | CS 02 | I/O-1 | AC CO A7 | 1F |
| 143-1 | POWER | I/O REG. | CS 03 | I/O-1 | AE CO A7 | 1F |
| 228 | 115VAC FANS | D & D | FA K1 06/07 | I/O-SS | FA K1 06/07 | NT |
| 231 | 115VAC CONVENIENCE | D & D | DF D1 03/04 | I/O-SS | HB L1/L2 01/02 | NT |
| 238 | 115VAC REGULATOR FANS | I/O-SS | FA K1 01/12 | I/O-SS | CR J1 03/04 | NT |

## 5.4 APPLYING POWER TO I/O-1

PRELIMINARY CHECKS

1. Check for loose or broken wires and components.

2. Check all packages for proper seating and location.

3. Tighten all mechanical connections.

4. Recheck all cables to insure correct and tight connections.

POWER "ON"

1. Turn DC Lockout switch on and turn on Power Supply.

2. Turn DC Lockout switch off and again check for proper voltages at the Regulator.

3. Insure that the I/O Voltage Sensing Circuits are operating properly by increasing or decreasing the -12V, -4.5V and -1.2V at the I/O Voltage Regulator. A 10% increase or decrease in these voltages should turn off the Power Supply. Verify that the correct indicators remain lit.

After making these checks, set these voltages to their proper values.

4. Using the I/O-1 Display Panel in D&D, check the manual set and reset of all flip-flops. Check "D" and "W" register clear operation. Check I/O clear.

POWER "OFF"

1. Turn the DC Lockout switch on. Check the -12V, -4.5V, -1.2V and +20V, at the I/O Regulator, to insure that these voltages are removed.

## 5.5 CONNECTING THE CLOCK TO I/O-1

PROCEDURE

To connect the Clock to I/O-1 follow the steps listed below.

1. Connect I/O-1 Clock Cable:

| CABLE NO. | FROM | | TO | | VIA TRAY |
|---|---|---|---|---|---|
| | UNIT | CONNECTOR | UNIT | CONNECTOR | |
| 170 | CC | EA D2 Y6 | I/O-1 | AA C7 Y4 | 2R |
| | | | | AC B8 L4 | |
| | | | | AE C6 Y9 | |

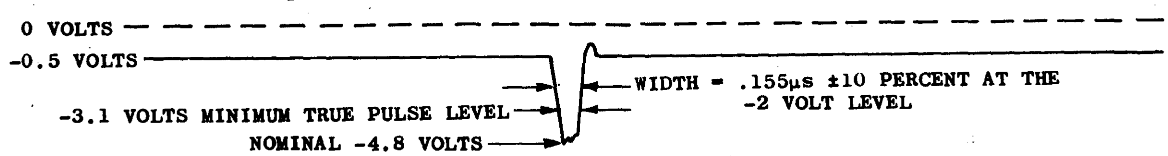
2. Set the clock to "Single Pulse" at the CC Control Panel in D&D. Adjust the bias level at the Variable Bias packages to obtain -0.5V measured at the associated local driver input listed:

   VB Pkg. AA C7 N7 Measure at AA B1 P8

   VB Pkg. AC B8 A7 Measure at AC B1 P7

   VB Pkg. AE C7 N2 Measure at AE B2 P1

3. Set the clock to "Start" at the CC Control Panel. Check for the presence of clock pulses at the following pins: (Each clock pulse should exceed the minimum requirements as indicated below).




(IF excessive ringing is observed at the terminating pins, verify that the circuits are actually terminated by the 750 ohm resistors to ground at the following locations.)

| | | |
|---|---|---|
| AA B1 P8 | AC B1 R7 | AD C3 K1 |
| AA B1 R8 | AC B1 S7 | |
| AA B1 S8 | AC B1 T7 | AE B2 P1 |
| AA B1 T8 | AC B1 U7 | AE B2 R1 |
| AA B1 U8 | AC B1 V7 | AE B2 S1 |
| AA B1 V8 | AC B1 W7 | AE B2 T1 |
| AA B1 W8 | AC B1 X7 | AE B2 U1 |
| AA B1 X8 | | AE B2 V1 |
| | AD A3 P5 | |
| AB B4 R7 | AD A3 V5 | AF C3 B1 |
| AB B4 S7 | AD A3 W5 | AF C3 C1 |
| | AD A3 X5 | AF C3 D1 |
| AC B1 P7 | AD C3 J1 | AF C3 E1 |

## 5.6 I/O-2 POWER AND INFORMATION CABLING

Install cables as listed in Table 5.6-1

TABLE 5.6-1 I/O-2 Power and Information Cabling

| CABLE NO. | FUNCTION | FROM | | TO | | VIA TRAY |
|---|---|---|---|---|---|---|
| | | UNIT | CONNECTOR | UNIT | CONNECTOR | |
| 3-2 | INPUT LINES | I/O-2 | AC DO A7 | CC | EC BO A2 | 3R |
| 4-2A | MEMORY READ EXCHANGE | I/O-2 | AE AO N2 | CC | AC DO A7 | 7R |
| 4-2B | MEMORY READ EXCHANGE | I/O-2 | AE BO N2 | CC | AC DO N7 | 7R |
| 5-2A | MEMORY WRITE EXCHANGE | I/O-2 | AE CO N7 | CC | BC AO A2 | 5R |
| 5-2B | MEMORY WRITE EXCHANGE | I/O-2 | AE DO A7 | CC | BC AO N2 | 5R |
| 6-2 | OUTPUT LINES | I/O-2 | AC BO A7 | CC | EC BO N2 | 3F |
| 29-2 | INDICATOR INPUT | I/O-2 | AA BO A2 | D & D | AY J1 | NT |
| 30-2 | INDICATOR INPUT | I/O-2 | AC CO A2 | D & D | AY K1 | NT |
| 31-2 | INDICATOR INPUT | I/O-2 | AE CO N2 | D & D | AY L1 | NT |
| 32-2 | INDICATOR INPUT | I/O-2 | AE DO N2 | D & D | AY M1 | NT |
| 33-2 | MANUAL CONTROL | I/O-2 | AA BO N2 | D & D | AY N1 | NT |
| 34-2 | MANUAL CONTROL | I/O-2 | AC CO N2 | D & D | AY P1 | NT |
| 35-2 | MANUAL CONTROL | I/O-2 | AE CO A2 | D & D | AY R1 | NT |
| 36-2 | MANUAL CONTROL | I/O-2 | AE DO A2 | D & D | AY S1 | NT |
| 65-2 | DISPLAY POWER | D & D | AE A2 N2 | D & D | AY T1 (A GATE) | NT |
| 141-2 | POWER | I/O-2 | AA CO A7 | I/O REG. | CS 11 | 1R |
| 142-2 | POWER | I/O-2 | AC CO A7 | I/O REG. | CS 12 | 1R |
| 143-2 | POWER | I/O-2 | AE CO A7 | I/O REG. | CS 13 | 1R |

## 5.7 APPLYING POWER TO I/O-2

PRELIMINARY CHECKS

1. Check for loose or broken wires and components.

2. Check all packages for proper seating and location.

3. Tighten all mechanical connections.

4. Recheck all cables to insure correct and tight connections.

POWER "ON"

1. Turn on the Power Supply and DC power.

2. Using the I/O-2 Display Panel in D&D, check the manual set and reset of all flip-flops. Check "D" and "W" register clear operation. Check I/O-2 clear.

## 5.8 CONNECTING THE CLOCK TO I/O-2

1. Connect I/O-2 Clock Cable as shown in chart below.

| CABLE NO. | FROM | | TO | | VIA TRAY |
|---|---|---|---|---|---|
| | UNIT | CONNECTOR | UNIT | CONNECTOR | |
| | CC | EA D2 Y1 | I/O-2 | AA C7 Y4 | 2R |
| 171 | | | | AC B8 L4 | |
| | | | | AE C6 Y9 | |

2. Use steps 2 and 3 of Subject 5.5 of this manual to check out the clock operation.

## 5.9 I/O-3 POWER AND INFORMATION CABLING

Install cables as listed in Table 5.9-1.

TABLE 5.9-1 I/O-3 Power and Information Cabling

| CABLE NO. | FUNCTION | FROM | | TO | | VIA TRAY |
|---|---|---|---|---|---|---|
| | | UNIT | CONNECTOR | UNIT | CONNECTOR | |
| 3-3 | INPUT LINES | I/O-3 | AC DO A7 | CC | EC CO A2 | 3R |
| 4-3A | MEMORY READ EXCHANGE | I/O-3 | AE AO N2 | CC | AE CO A7 | 10R |
| 4-3B | MEMORY READ EXCHANGE | I/O-3 | AE BO N2 | CC | AE CO N7 | 10R |
| 5-3A | MEMORY WRITE EXCHANGE | I/O-3 | AE CO N7 | CC | BC CO A2 | 7R |
| 5-3B | MEMORY WRITE EXCHANGE | I/O-3 | AE DO A7 | CC | BC CO N2 | 7R |
| 6-3 | OUTPUT LINES | I/O-3 | AC BO A7 | CC | EC CO N2 | 5R |
| 29-3 | INDICATOR INPUT | I/O-3 | AA BO A2 | D & D | AY J1 | 3R |
| 30-3 | INDICATOR INPUT | I/O-3 | AC CO A2 | D & D | AY K1 | 3R |
| 31-3 | INDICATOR INPUT | I/O-3 | AE CO N2 | D & D | AY L1 | 3R |
| 32-3 | INDICATOR INPUT | I/O-3 | AE DO N2 | D & D | AY M1 | 3R |
| 33-3 | MANUAL CONTROL | I/O-3 | AA BO N2 | D & D | AY N1 | 3R |
| 34-3 | MANUAL CONTROL | I/O-3 | AC CO N2 | D & D | AY P1 | 3R |
| 35-3 | MANUAL CONTROL | I/O-3 | AE CO A2 | D & D | AY R1 | 3R |
| 36-3 | MANUAL CONTROL | I/O-3 | AE DO A2 | D & D | SY S1 | 3R |
| 65-3 | DISPLAY POWER | D & D | AE BO A2 | D & D | AY T1 (B GATE) | NT |
| 141-3 | POWER | I/O-3 | AA CO A7 | I/O REG. | CS 04 | 1R |
| 142-3 | POWER | I/O-3 | AC CO A7 | I/O REG. | CS 05 | 1R |
| 143-3 | POWER | I/O-3 | AE CO A7 | I/O REG. | CS 06 | 1R |

## 5.10 APPLYING POWER TO I/O-3

PRELIMINARY CHECKS

1. Check for loose or broken wires and components.
2. Check all packages for proper seating and location.
3. Tighten all mechanical connections.
4. Recheck all cables to insure correct and tight connections.

POWER "ON"

1. Turn on the Power Supply and DC power.
2. Using the I/O-3 Display Panel in D&D, check the manual set and reset of all flip-flops. Check the "D" and "W" register clear operation. Check the I/O-3 clear.

## 5.11 CONNECTING THE CLOCK TO I/O-3

1. Connect I/O-3 Clock Cable as shown in the chart below.

| CABLE NO. | FROM | | TO | | VIA TRAY |
|---|---|---|---|---|---|
| | UNIT | CONNECTOR | UNIT | CONNECTOR | |
| 172 | CC | EA D2 Y8 | I/O-3 | AA C7 Y4 | 2R |
| | | | | AC B8 L4 | |
| | | | | AE C6 Y9 | |

2. Use steps 2 and 3 of Subject 5.5 of this manual to check out the clock operation.

## 5.12 I/O-4 POWER AND INFORMATION CABLING

Install cables as listed in Table 5.12-1.

TABLE 5.12-1 I/O-4 Power and Information Cabling

| CABLE NO. | FUNCTION | FROM | | TO | | VIA TRAY |
|---|---|---|---|---|---|---|
| | | UNIT | CONNECTOR | UNIT | CONNECTOR | |
| 3-4 | INPUT LINES | I/O-4 | AC DO A7 | CC | EC DO A2 | 5F |
| 4-4A | MEMORY READ EXCHANGE | I/O-4 | AE AO N2 | CC | AE DO A7 | 10F |
| 4-4B | MEMORY READ EXCHANGE | I/O-4 | AE BO N2 | CC | AE DO N7 | 10F |
| 5-4A | MEMORY WRITE EXCHANGE | I/O-4 | AE CO N7 | CC | BE CO A2 | 10R |
| 5-4B | MEMORY WRITE EXCHANGE | I/O-4 | AE DO A7 | CC | BE CO N2 | 10R |
| 6-4 | OUTPUT LINES | I/O-4 | AC BO A7 | CC | EC DO N2 | 5F |
| 29-4 | INDICATOR INPUT | I/O-4 | AA BO A2 | D & D | AY J1 | NT |
| 30-4 | INDICATOR INPUT | I/O-4 | AC CO A2 | D & D | AY K1 | NT |
| 31-4 | INDICATOR INPUT | I/O-4 | AE CO N2 | D & D | AY L1 | NT |
| 32-4 | INDICATOR INPUT | I/O-4 | AE DO N2 | D & D | AY M1 | NT |
| 33-4 | MANUAL CONTROL | I/O-4 | AA BO N2 | D & D | AY N1 | NT |
| 34-4 | MANUAL CONTROL | I/O-4 | AC CO N2 | D & D | AY P1 | NT |
| 35-4 | MANUAL CONTROL | I/O-4 | AE CO A2 | D & D | AY R1 | NT |
| 36-4 | MANUAL CONTROL | I/O-4 | AE DO A2 | D & D | AY S1 | NT |
| 65-4 | DISPLAY POWER | D & D | AE B2 A2 | D & D | AY T1 (B GATE) | NT |
| 141-4 | POWER | I/O-4 | AA CO A7 | I/O-SS | CS 14 | 1F |
| 142-4 | POWER | I/O-4 | AC CO A7 | I/O-SS | CS 15 | 1F |
| 143-4 | POWER | I/O-4 | AE CO A7 | I/O-SS | CS 16 | 1F |

## 5.13 APPLYING POWER TO I/O-4

PRELIMINARY CHECKS

1. Check for loose or broken wires and components.
2. Check all packages for proper seating.
3. Tighten all mechanical connections.
4. Recheck all cables to insure correct and tight connections.

POWER "ON"

1. Turn on the Power Supply and DC Power.
2. Using the I/O-4 Display Panel in D&D, check the manual set and reset of all flip-flops. Check the "D" and "W" register clear operation. Check I/O-4 clear.

## 5.14 CONNECTING THE CLOCK TO I/O-4

1. Connect the I/O-4 clock cable as shown in the chart below.

| CABLE NO. | FROM | | TO | | VIA TRAY |
|---|---|---|---|---|---|
| | UNIT | CONNECTOR | UNIT | CONNECTOR | |
| 173 | CC | EA D2 Y9 | I/O-4 | AA C7 Y4 | 2R |
| | | | | AC B8 L4 | |
| | | | | AE C6 Y9 | |

2. Use steps 2 and 3 of Subject 5.5 of this manual to check out the clock operation.

## 5.15 ADDING ADDITIONAL I/O CONTROL UNITS

### INTRODUCTION

It is Field Engineering's responsibility to install and check-out any I/O Control Units which may be added to the system whenever a customer's needs require additional units.

This Subject outlines the procedure for installing and checking out these additional I/O Control Units. The procedure for adding I/O Control Unit 2 will be explained first followed by the procedure for I/O Control Units 3 and 4.

### INSTALLING I/O CONTROL UNIT 2 (OUTER GATE)

#### Mounting Unit Within The Sub-System Cabinet

The following procedure should be used to mount unit within the sub-system cabinet.

1. I/O-2 Control Unit physically occupies the back gate position of the I/O sub-system. (Refer to Figure 5.15-1).

   The hinge blocks, stopper arm and etc., needed to mount the additional rack are supplied with the rack.

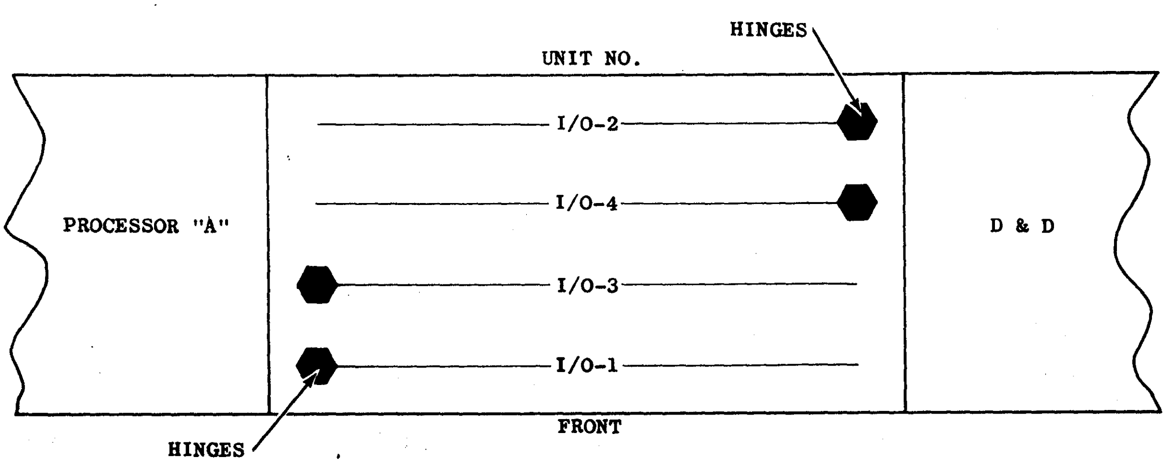



FIGURE 5.15-1 I/O UNIT AND GATE LOCATION

Figure 5.15-2 shows the location of each part in the mounting list.

Use Figure 5.15-2 and the following instructions to facilitate mounting the new unit. Numbers in brackets (NO.) refer to parts location shown in circles in Figure 5.15-2.

NOTE

Due to the weight of the gate complete with panels and packages it is advisable to remove at least two panels (if shipped complete) prior to installation.

2. Move the gate into position and place blocks under gate to assist holding it in place.

3. Put the upper dowel (1) in place and install upper door hinge mounting (2).

4. With the top of the gate now fastened into place move the bottom of the gate toward the center of the cabinet. Put the lower dowel pin (3) into place along with 3 thrust washers (4) and 1 spacer (5) as shown in Figure 5.15-2.

5. Lift up on the gate and move the bottom dowel pin into place. Install the lower door hinge mounting (6).

6. Install the upper outer gate friction arm bracket, the upper friction arm (7), the lower outer gate friction arm bracket (13) and the lower outer friction arm (14).

7. Install the outer gate latch bracket (8).

8. Install the lock hook (9).

9. Install the stop gate (10) in location "A".

10. The physical mounting of the new gate is now completed.

Cable Hook-Up and Power "ON" Check

1. Install all power, information and clock cables as described in Subjects 5.6, 5.7 and 5.8.

2. Check that the correct number of .02 ohm 90 watt resistors (location CA T L2) are installed in the -12V voltage regulator (refer to chart below).

   With power on, turn the over current sensing pot to the position where over current is sensed. The following indicators, on the power sense panel in D&D, should be "ON" and power should drop.

   I/O Indicator

   Over Current Indicator

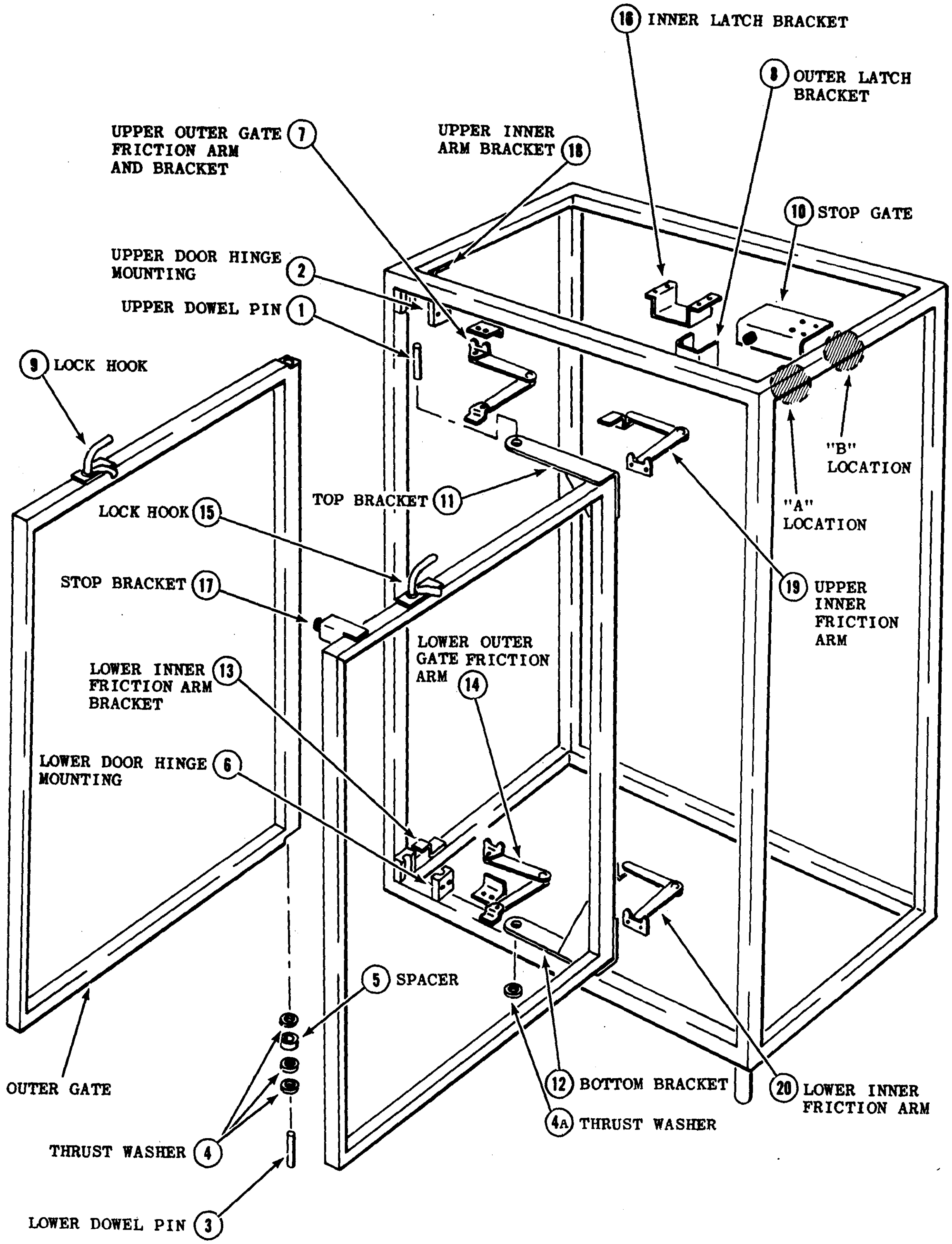



FIGURE 5.15-2 INNER AND OUTER GATE INSTALLATION

After verifying that the correct indicators are lit and power has dropped, turn the sensing pot back (from the point at which sensing occurred) the number of turns listed on the chart below. This will be the correct adjustment for over current sensing and for the number of I/O's installed.

| NO. OF I/Os INSTALLED | RESISTORS REQUIRED | OVER CURRENT ADJUSTMENT (TURNS BACK) |
|---|---|---|
| 1 | 1 | 1 |
| 2 | 2 | 1 |
| 3 | 2 | 1.5 |
| 4 | 2 | 2 |

Adding Additional Packages in CC

To complete the addition of the new I/O unit it is necessary to install additional packages in Central Control (I/O Exchange, Memory Exchange and etc.). The list of these packages will be furnished either as part of the kit or as an addenda to this manual.

INSTALLING I/O CONTROL UNITS 3 AND 4 (INNER GATE)

Mounting Unit Within The Sub-System Cabinet

1. I/O-3 and 4 gates are located as shown in Figure 5.15-1.

   Figure 5.15-2 shows the location of each part used in mounting the gates.

   Use Figure 5.15-2 and the following instructions to facilitate mounting the new unit. Numbers in brackets (NO.) refer to parts location shown in circles in Figure 5.15-2.

NOTE

> Due to the weight of the gate complete with panels and packages it is advisable to remove at least two panels (if shipped complete) prior to installation.

2. Open the outer gate to a 90° angle with the front or rear of the cabinet.

3. Place blocks under the gate to support it while removing the upper door hinge mounting (2).

4. Remove upper dowel pin (1).

5. Place the top inner gate bracket (11) into position and replace upper dowel pin (1) through the bracket into the outer gate.

6. Replace the upper door hinge mounting (2).

7. Remove the lower door hinge mounting (6).

8. Using a suitable lever (2 x 4, crowbar or pinch bar) lift the outer gate at the same time moving the bottom toward the center of the cabinet. Remove the lower dowel pin (3), thrust washers (4) and spacer (5).

9. Place the bottom inner gate bracket (12) on the lower dowel pin with 1 thrust washer (4a) above and below the bracket. Insert the dowel pin into the bottom of the gate.

10. Position the lower part of the gate into position to allow replacement of the lower door hinge mounting (6).

11. Install upper and lower stop bracket (17) on the inner gate.

12. Position the top and lower inner gate brackets to a suitable angle to allow moving the new gate into position to bolt it to the brackets.

13. Move the gate into position against the brackets using blocks to support the weight after aligning the holes for the bolts. Install bolts and tighten.

14. Install the upper inner friction arm bracket (18), the upper inner friction arm (14), the lower inner gate friction arm bracket (18) and the inner lower friction arm (20).

15. Install the inner gate lock hook (15).

16. Install the inner gate latch bracket (16).

17. Move the stop gate (10) from location "A" to location "B".

18. The physical mounting of the new gate is now completed.

Cable Hook-Up and Power "ON" Check

1. Install all power, information and clock cables as described in Subjects 5.9, 5.10 and 5.11.

2. Check that the correct number of .02 ohm 90 watt resistors (location CA T L2) are installed in the -12V voltage regulator (refer to chart below).

   With power on, turn the over current sensing pot to the position where over current is sensed. The following indicators, on the power sense panel in D&D, should be "ON" and power should drop.

   I/O Indicator

   Over Current Indicator

After verifying that the correct indicators are lit and power has dropped, turn the sensing pot back (from the point at which sensing occurred) the number of turns listed on the chart below. This will be the correct adjustment for over current sensing and for the number of I/O's installed.

| NO. OF I/Os INSTALLED | RESISTORS REQUIRED | OVER CURRENT ADJUSTMENT (TURNS BACK) |
|---|---|---|
| 1 | 1 | 1 |
| 2 | 2 | 1 |
| 3 | 2 | 1.5 |
| 4 | 2 | 2 |

Adding Additional Packages in CC

To complete the addition of the new I/O unit it is necessary to install additional packages in Central Control (I/O Exchange, Memory Exchange and etc.). The list of these packages will be furnished either as part of the kit or as an addenda to this manual.

# SECTION 6

## CIRCUIT ANALYSIS

Refer to Section 6 of the Power Supply manual for a description of the packages used in the I/O Sub-System.

# SECTION 7

## FUNCTIONAL DESCRIPTION

### 7.1 INTRODUCTION

This section of the manual contains a general description of the function of the I/O Control Unit plus an explanation, a sequence count state chart, and a glossary of each I/O Descriptor.

## 7.2 GENERAL DESCRIPTION

### INTRODUCTION

The B 5282 I/O Sub-System controls the transfer of data to and from all peripheral units connected to the B 5000 system.

The I/O Sub-System may consist of one to four I/O Control Units each operating independently.

Instructions to an I/O Control Unit are in the form of I/O Descriptor words received from a Memory Address specified by Processor number 1.

All input/output operations are directly to or from the High Speed Core Memory. In the event of conflict for access to the same memory unit, access is shared with one or two Processors and other I/O Control Units.

Input data flow is from peripheral unit through the I/O Control Unit to the High Speed Core Memory. Output data flow is from High Speed Core Memory through the I/O Control Unit to the peripheral unit. The W register (48 bits) serves as a one word buffer in the I/O Control Unit between High Speed Core Memory and the peripheral units for both input and output.

### SYSTEM CONFIGURATION

In a maximum system configuration the I/O Control Unit controls any of the following peripheral units:

| | MAXIMUM SYSTEM | |
|---|---|---|
| Drum Memory Units | 2 | |
| Magnetic Tape Transports | 16 | |
| 800 CPM Serial Card Reader | 2 | 2 Total |
| 200 CPM Serial Card Reader | 2 | |
| 100 CPM Card Punch | 1 | 1 Total |
| 300 CPM Card Punch | 1 | |
| Drum Printer | 2 | |
| Supervisory Printer-Keyboard | 1 | |
| Paper Tape Reader | 2 | 3 Total |
| Paper Tape Punch | 2 | |
| Disk File Control | 2 | |
| Data Communication Control | 1 | |

I/O SELECTION

Assignment of a particular I/O Control Unit to control an I/O operation is done automatically on the basis of availability. Any peripheral unit may be designated by any I/O Control Unit selectively.

An operation complete is signaled by returning a result descriptor to a specified Memory Address and setting the appropriate I/O Finished Interrupt.

I/O DATA DESCRIPTOR

All input/output operations are specified by means of data descriptors transmitted to an I/O Control Unit.

An Initiate I/O Operator in Processor number 1 causes the address of an I/O Data Descriptor to be stored in Memory Cell number 8 and activates the I/O Control Unit. The I/O Control Unit now begins its operation, independently of the Data Processor addressed by Memory Cell number 8.

The I/O Data Descriptor specifies the parameters of the I/O Operation such as unit designated, High Speed Memory Address, mode of operation, number of words, etc. Portions of the descriptor format are standard; the remainder of the descriptor is dependent on the particular peripheral unit addressed.

The basic I/O Descriptor is illustrated in Table 7.2-1.

TABLE 7.2-1 BASIC I/O DESCRIPTOR (EXCLUDING MAGNETIC DRUM)

| | D41-45 | D31-40 | D30 | | D24-27 | | D16-23 | D1-15 |
|---|---|---|---|---|---|---|---|---|
| | Unit Desig-nate | Word Count | Control | | | | Error and Control Field Result Descriptor | Core Memory Address |

(Bit positions that are crossed out are used primarily by the Processor and are not stored in the I/O Control Unit D Register).

RESULT DESCRIPTOR

At the completion of an I/O operation, or if no operation can be performed because of unavailability of the addressed peripheral unit, a Result Descriptor is returned to Memory showing the results of the operation.

Each I/O Unit transmits the Result Descriptor to a specific Memory Address:

| | |
|---|---|
| I/O-1 | Memory Cell 12 |
| I/O-2 | Memory Cell 13 |
| I/O-3 | Memory Cell 14 |
| I/O-4 | Memory Cell 15 |

The Result Descriptor is generated by modifying the original Data Descriptor stored in the D register during the I/O operation.

CORE MEMORY ADDRESS FIELD

The Memory Address field D1-D15 contains the Memory Address of the last access +1 except in the following cases:

1. For backward tape read, the Core Memory Address Field contains the address of the last access -1.

2. For Printer operations the Core Memory Address Field contains the address of the beginning record -1.

3. For Magnetic Tape read operations where the number of words read from tape is greater than the number of words stored in Memory, the Core Memory Address Field contains its original value plus (forward read) or minus (backward read) the number of words or fractions of words read from tape to the I/O Control Unit.

WORD COUNT FIELD

For Drum Read, Drum Write, Card Input and Output operations, the Word Count Field, which is used internally during the operation, is returned as zero if the operation has been validly completed.

For Magnetic Tape Read, Magnetic Tape Write, Paper Tape Read, and Paper Tape Punch operations, the Word Count Field is equal to its value in the Data Descriptor minus the number of words transferred to or from Memory.

UNIT DESIGNATE FIELD

The Unit Designate Field D41-45 is returned unchanged.

ERROR AND CONTROL FIELD

The bit positions D16 through D23 are used to flag control or error conditions encountered during the operation.

Portions of the error and control field D16 through D23 are standard for all units; the remainder of the field is dependent on the particular peripheral unit addressed. See Table 7.2-2.

The basic error and control field is as follows:

D16 Busy

If an Input/Output Control Unit addresses a peripheral unit and finds that unit "busy" as a result of being still connected to another Input/Output Control Unit, the Input/Output Control Unit returns a result descriptor with the busy condition indicated.

If an Input/Output Control Unit addresses a peripheral unit other than a Magnetic Tape or Paper Tape Unit, which is not currently attached to any other Input/Output Control Unit but still is "busy" completing a former operation, the Input/Output Control Unit "waits" indefinitely until the unit is no longer busy, then immediately initiates the new operation.

Whenever an Input/Output Control Unit addressed a Magnetic Tape or Paper Tape Unit that is not currently attached to another Input/Output Control Unit and that is still "busy" completing the former operation (decelerating or rewinding), the Input/Output Control Unit waits until the unit is no longer busy then immediately initiates the new operation, except that if the Input/Output Control Unit waits longer than 6 ms (tape rewinding), it terminates the operation and returns a result descriptor with a busy indication.

These conditions are true for all valid descriptors.

D17 Descriptor Error

Indicates either a parity error or a non-existent address error experienced in fetching the descriptor address from Memory Location 8 or in fetching the descriptor itself. Bits D19 and D22 further indicate the type of error experienced.

D18 Not Ready

If an Input/Output Control Unit, on attempting to access a peripheral unit, finds that unit in a Not Ready condition, it returns a result descriptor with the Not Ready condition indicated in D18. All conditions which constitute Not Ready are specified in the Technical Manuals of the individual units.

D22 Memory Access Error

Indicates an attempt to access a high speed memory location that is non-existent or not available. This check operates for all memory locations and is independent of the relative location of available Memory Modules.

This flag is also set if the Input/Output Control Unit is transferring a series of words to or from Memory, and the addresses extend above 32,767 reading or writing forward, or below 0 reading backward.

D19, D20, D21 and D23

See Table 7.2-2.

TABLE 7.2-2 RESULT DESCRIPTOR ERROR AND CONTROL FIELD

| | STANDARD ERROR FIELD | | | | 19 | 20 | 21 | 23 |
|---|---|---|---|---|---|---|---|---|
| | 16 | 17 | 18 Not Ready | 22 Memory Address | | | | |
| Printer | X | X | X | X | Parity-Mem. to I/O | Print Check Previous Line | End-of-Page | |
| Drum Write | X | X | X | X | Parity-Mem. to I/O | | Lockout | |
| Drum Read | X | X | X | X | Parity-Drum to I/O | | | |
| Card Input | X | X | X | X | Invalid Character | Read Check | End-of-File | |
| Card Output | X | X | X | X | Parity-Mem. to I/O | Punch Error | | |
| Mag. Tape Read | X | X | X | X | | Parity-Tape to I/O | End-of-File | |
| Mag. Tape Write | X | X | X | X / * See D20 | Parity-Mem. to I/O | Read-Back Parity / *Write Lock-Out (D20 and D22) | End-of-Tape | |
| Supv. Printer | X | X | X | X | Parity-Mem. to I/O | | | |
| Keyboard | X | X | X | X | Parity-Mem. to I/O | Parity or Operator Error | | |
| Paper Tape Read | X | X | X | X | Parity in Reader | Beginning of Tape | End-of-Tape | |
| Paper Tape Write | X | X | X | X | Parity-Mem. to I/O | | Low Tape | |
| Disk File Read | X | X | Control Unit | X | Parity-Mem. to I/O (Address Transfer) | Parity-Disk to I/O | Not Ready Electronics Unit | Read Check Error |
| Disk File Write | X | X | Control Unit | X | Parity-Mem. to I/O and I/O to Control | Write Lock-Out | Not Ready Electronics Unit | |
| Data Comm. Read | X | X | X | X | | Terminal Unit Busy | Terminal Unit Output Ready | |
| Data Comm. Write | X | X | X | X | Parity-Mem. to I/O | Terminal Unit Busy | Terminal Unit Input Ready | Multiple Output |

INTERRUPTS

At the completion of an I/O operation, each I/O Control Unit places a bit in a specified position of the Interrupt Register in CC. This bit will generate the following addresses which are placed in the C register when the Processor enters the control state to handle the Interrupt.

I/O NO. 1 FINISHED ADDRESS 23

I/O NO. 2 FINISHED ADDRESS 24

I/O NO. 3 FINISHED ADDRESS 25

I/O NO. 4 FINISHED ADDRESS 26

## 7.3 B 5000 CARD READ OPERATION

### PURPOSE

To read a punched card in either Alphanumeric or Binary mode in conjunction with the operation of either the 200 CPM (Program Card Reader) or 800 CPM Reader.

Information is read from the card serially by column starting with column one. The word is formed most significant character first. Memory is counted up as each word is stored. In alphanumeric mode, one column forms one character, eight characters form one word, ten words to a card. In Binary mode, each column forms two characters, four columns per word and twenty words per card. The upper half of the column is the most significant character of the pair. Unpunched bits are binary zero.

Card Readers are interchangeable to the I/O Control Unit.

### PROVISIONS

When the object program finds that the memory area designated for input information is empty, the Master Control Program will compile a Data Descriptor for the area which will identify it for the Card Reader. The Unit Designate Field of the Data Descriptor (Bit positions 45 ⇒ 41) calls for a Card Reader.

To connect the Card Reader to that part of memory, the object program will exit into the Master Control Program which will examine the various I/O descriptors. The one which has the capability of doing what is needed at the time will be executed next. Its address will be stored in location 8. The same operation will signal Central Control and Central Control will select the lowest numbered I/O Unit which is not busy. The I/O Unit will be initiated with an Admit Descriptor Level corresponding to the I/O Channel number (ADnS). This level will start the I/O Unit sequence of operations. Refer to Figure 7.3-1.

### SUMMARY OF OPERATIONS

Upon initiation from Central Control Unit (see Provisions) an I/O Descriptor will be transferred from memory to the I/O Control Unit. This Descriptor will be used to control the reading of the card. The Descriptor consists of the following information:

1. Unit Designation $\mu$ (D45 ⇒ 41) $\mu$=10 or 14 (Binary)

2. Alphanumeric input (D27=0) Binary input (D27=1)

3. Type of operation (D24=1)

4. Starting Memory Address (D15 ⇒ 1)

While the card is being read, a result descriptor is constructed. It is transferred to memory, indicating a successful or unsuccessful completion of the operation. The Result Descriptor contains the following information:

1. Unit Designation (unchanged from that above)

2. Unit Busy (D16F)

3. Unit Not Ready (D18F)

4. Descriptor Parity Error (D17F)

5. Memory Address Error (D22F)

6. Invalid Character (D19F)

7. Read Check Error (D20F)

8. End of File (D21F)

9. Memory Address of Last Access +1 (D15 $\Rightarrow$ 1)

INTERCONNECTION

This Supplementary Section describes the information and control signal lines between the 800 CPM or Program Serial Card Reader and the B 5000 Central Control.

Signals Delivered to 800 CPM or Program Serial Card Reader From the Central Control

| NAME | DESCRIPTION |
|---|---|
| $\overline{\text{SCCL}}$ | $\overline{\text{Start Card Cycle Level}}$ when positive causes a single card to feed and continue through a card cycle ending in the stacker. $\overline{\text{SCCL}}$ remains positive until the Card Cycle Level ($\overline{\text{CCL}}$) goes to positive indicating that a card cycle has been started. |
| $\overline{\text{CBIL}}$ | $\overline{\text{Card Reader Binary Level}}$ when positive selects Binary readout instead of Alpha recognition. |
| $\overline{\text{CBHL}}$ | $\overline{\text{Card Reader Binary Half Level}}$ is positive for the top 6 rows or half of any binary character. |

Signals From 800 CPM Serial Card Reader to the Central Control

| NAME | DESCRIPTION |
|---|---|
| CSP | Column Strobe Pulse is negative as a timing pulse which samples column information, be it a character or blank. There will be 80 pulses for all lengths of cards. |

| | |
|---|---|
| $\overline{\text{CREL}}$ | Card Read Error Level when positive indicates that one of the 12 photo read cells is malfunctioning. CREL is reset by SCCL, or the RESET Button. |
| CC1L<br>CC2L<br>CC4L<br>CC8L<br>CCAL<br>CCBL | Column Character lines contain the column character information before the column strobe pulse is received. This information is stored in flip-flops for a minimum of 300 µs in the Alpha mode. They will be reset and changed before the next column strobe pulse. |
| $\overline{\text{CCL}}$ | Card Cycle Level is positive from the time the Start Card Cycle Level is accepted until 300 µs after the 80th column strobe pulse is sent. CCL becomes positive within 10 µs of SCCL. |
| EOFL | End of File Level is negative if there is an empty hopper and the END OF FILE Button on the Card Reader has been pressed. |
| $\overline{\text{CRL}}$ | Card Ready Level is positive when the Card Reader is ready to accept SCCL pulses and results from the following conditions being met. |

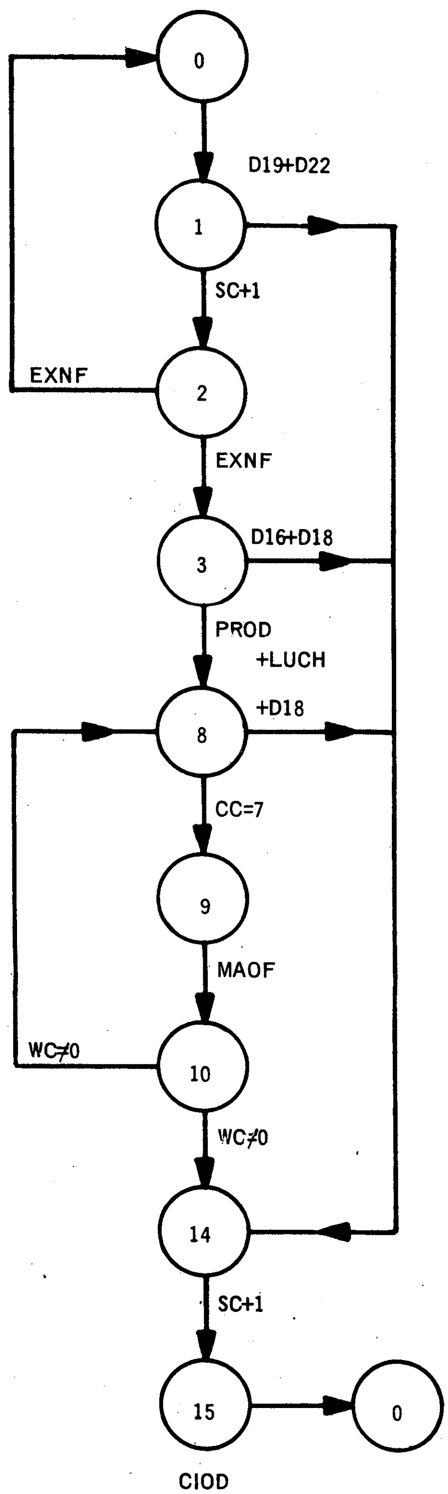
1. No jams.
2. Stacker not full.
3. Card line mechanism locked.
4. Covers are in place.
5. Power on.
6. Feeder ready (START Button depressed).
7. Empty hopper doesn't exist.

Power and Power Control Lines Between the Card Readers and Central Control

| NAME | DESCRIPTION | |
|---|---|---|
| -12 | Minus Twelve (-12) volts DC supplied by Central Control. | Program Reader Only |
| +20 | Plus Twenty (+20) volts DC supplied by Central Control. | |
| GND | Ground return for DC power are the TP returns. | |
| Power ON | Power On Signal Line from Central Control. | |
| Power Off | Power Off Signal Line from Central Control. | |

Emergency Power — Emergency Power Off Signal Line from Central Control.

Power Control Common




SC=0, 1 & 2: Operation initiated by ADNS or LOTS signal from Central Control. Two Memory Accesses are performed:

1. Read Descriptor Address from Memory Cell 8.
2. Read Descriptor from Memory.

SC=3: Interrogate Peripheral Unit trunk, Designate Peripheral Unit and interrogate Peripheral Unit's status (Ready-Busy).

SC=8: Transfer info, presented by Card Reader, into "Wr" (Word Register). Alpha Cards present 10 words of 8 characters each; Binary Cards present 20 words of 16 octates each.

SC=9, 10: Access Memory and transfer Data Word accumulated, in Wr, to Memory. Index - Word Counter, Address Counter.

SC=14: Shift Result Descriptor

SC=15: Transfer Result Descriptor to Memory and clear I/O unit.

FIGURE 7.3-1 B 5000 CARD READ SEQUENCE COUNT STATE CHART

B 5000 GLOSSARY CARD READER

(BINARY AND ALPHA)

| | |
|---|---|
| ADNS-C | Admit Descriptor Level - Comes from the Central Control Unit to an I/O Unit. |
| AOFF | Address Overflow Flip-flop - Indicates the Flip-flops D01F ⇒ D15F were all equal to one when a Memory Cycle took place. Inhibits any further transfer of information to or from Core Memory. |
| AUNS | Admit Unit Level - Comes from Central Control to an I/O Unit - indicates unit is not busy. |
| CBHL | Card Binary Half Level - Sent to the Card Reader by O23D during the operation to tell the Card Reader which half of the card column to read. |
| CBIL | Card Binary Level - Sent to the Card Reader by O22D at SC = 3 if the I/O Control Unit is in the Binary Mode. |
| CC=N, CC≠N | Character Counter is equal to or not equal to some number "N". The character counter consists of 3 flip-flops. |
| CC+1 | Character Counter plus One-in the logic book the driver is C+1D. |
| CCL | Card Cycle Level - Indicates the Card Reader is in its cycle of feeding a card. |
| CDRD-1 | Clear "D" Register Driver No. 1. This driver clears D01F ⇒ D15F. |
| CIOD | Clear I/O Driver. Clears the I/O Control Unit when true. |
| CREF | Card Reader Error Flip-flop - located in the Card Reader - Indicates the Photo Cells of Card Reader are not functioning properly. |
| CRL | Card Reader Ready Level. |
| CSP | Column Strobe Pulse - For each column of card there will be a pulse from 12 µs to 18 µs wide for Program Card Reader, and from 6 µs to 15 µs for 800 Card Per Minute Reader. |

| | |
|---|---|
| CC1L ⇒ CCBL | Column Character Lines - These lines come from the Card Reader to the Central Control. From the Central Control to the I/O Unit they are IO1D ⇒ IO6D. |
| D01F ⇒ D15F | These 15 flip-flops are part of the "D" register. During an operation they always contain the address of Core Memory that information is being sent to or taken from. |
| D16F | This flip-flop is part of the "D" Register. The state of W16F is never sent to D16F, the opposite state of D16F is always sent to W16F. During an operation it is the Not Busy Flip-flop in the I/O Unit, at the completion of an operation it is the Busy Flip-flop of the Result Descriptor. |
| D17F | This flip-flop is part of the "D" Register. The state of W17F is never sent to D17F. This flip-flop has many functions during an operation. It is used to remember that an Admit Descriptor level has been received at the beginning of an operation. It is used to turn MANF on at SC=0 time. If a Descriptor Parity error should occur, it remembers it. It is part of the Result Descriptor. During the Binary Card Cycle it is used to indicate to the Card Reader which half of the Card Column is needed by the I/O Unit. |
| D18F | This flip-flop is part of the "D" Register. The state of W18F is never sent to D18F. The opposite state of D18F is always sent to W18F. During an operation it is the Ready Flip-flop in the I/O Unit. At the completion of an operation it is the Not Ready Flip-flop of the Result Descriptor. |
| D19F | The flip-flop is part of the "D" Register. The state of W19F is never sent to D19F. If an Invalid Character should be read from a card this flip-flop remembers it. It is part of the Result Descriptor. |
| D20F | This flip-flop is part of the "D" Register. The state of W20F is never sent to D20F. If a read error should occur in the Card Reader, this flip-flop remembers it. It is part of the Result Descriptor. |
| D21F | This flip-flop is part of the "D" Register. The state of W21F is never sent to D21F. If an End of File condition is initiated in the Card Reader this flip-flop remembers it. It is part of the Result Descriptor. |
| D22F | This flip-flop is part of the "D" Register. The state of W22F is never sent to D22F. If a Memory Overflow or Memory Address Error should occur this flip-flop remembers it. It is part of the Result Descriptor. |

| | |
|---|---|
| D24F | This flip-flop is part of the "D" Register. If the Input/Output Descriptor contains a zero in the 24th bit position a Write Operation is indicated, if a one is contained in the 24th bit position a Read Operation is indicated. It is part of the Result Descriptor. |
| D25F | This flip-flop is part of the "D" Register. It is used to indicate if this operation uses the Word Counter portion of the "D" Register. |
| D26F | This flip-flop is part of the "D" Register. When this flip-flop is on, the Card Reader is being sent a Start Card Cycle level through the Central Control Unit. |
| D27F | This flip-flop is part of the "D" Register. If the Input/Output Descriptor contains a zero in the 27th bit position Alpha Mode operation is indicated, if a one is contained in the 27th bit position Binary Mode operation is indicated. It is part of the Result Descriptor. |
| D30F | This flip-flop is part of the "D" Register. It is not used during card read operation. |
| D31 ⇒ D40F | These flip-flops are part of the "D" Register. They make up the Word Counter for all operations. The Card Read operation uses D31F ⇒ D35F only. |
| D41F ⇒ D45F | These flip-flops are part of the "D" Register. They are used to designate the peripheral unit that is to be controlled or that is to receive or send information. They are part of the Result Descriptor. |
| DERS | "D" Register Error Level - If an error should occur during an operation, this level will be true. The level is used in Central Control during a LOAD operation only. |
| DR | The Descriptor Register - consists of 42 flip-flops numbered D01F ⇒ D22F, D24F ⇒ D27F, and D30F ⇒ D45F. |
| $\overline{\text{DROS}}$ | Not Drum Operation Switch - used to gate an action that happens on all operations except Drum operation. |
| DWSD | "D" Register to "W" Register Shift Driver. |
| EOFL | End of File Level - This level is sent to the Central Control Unit when an End of File Condition exists in the Card Reader. This level comes from the Central Control to the I/O Unit as I28D. |

| | |
|---|---|
| EXNF | External Control Flip-flop - This flip-flop has many functions. It is used to indicate how many times the actions of SC=2 have been executed during the Card Read operation. With the Card Read operation it has no further usage. |
| FIND | Finished Operation Driver |
| HOLF | Hold Over Flip-flop - Used to allow only one group of actions to take place for any one CSP during Card Read, Alpha. Allows two groups of actions to take place for any one CSP during Card Read, Binary. |
| IO1D ⇒ IO6D | These are the 6 drivers in the Central Control Unit that send across the 6 information bits of a character to the I/O Unit. Card Read, Alpha allows one character per card column. Card Read, Binary, allows two characters per card column. |
| I21D | This driver is located in Central Control and sends the Card Reader Level to the I/O Unit. |
| I22D | This driver is located in Central Control and sends the Card Cycle Level to the I/O Unit. |
| I24D | This driver is located in Central Control and sends the Column Strobe Pulse to the I/O Unit. |
| I25D | This driver is located in Central Control and sends the Card Read Error Flip-flop state, of the Card Reader, to the I/O Unit. |
| I28D | This driver is located in Central Control and sends the End of File Level to the I/O Unit. |
| I21S | This switch is located in the I/O Unit and is used to invert the level received from the driver I21D to Central Control. |
| I22S | This switch is located in the I/O Unit and is used to invert the level received from the driver I22D of Central Control. |
| I24S | This switch is located in the I/O Unit and is used to invert the level received from the driver I24D of Central Control. |
| IB1F ⇒ IBBF | These 6 flip-flops are used to accept information from the Card Reader, etc. by way of the Central Control Unit. |
| IB | Input Buffer - Information from the peripheral units is received in this buffer. It is made up of IB1F ⇒ IBPF. |
| IMCF | Initiate Maintenance Cycle Flip-flop. |
| IMCP | Initiate Maintenance Cycle Pulse. |

| | |
|---|---|
| I/O No. 1 | Input/Output Control Unit number one. |
| I/O No. 2 | Input/Output Control Unit number two. |
| I/O No. 3 | Input/Output Control Unit number three. |
| I/O No. 4 | Input/Output Control Unit number four. |
| KEML | Key Memory Level - Used in conjunction with the Memory Cycle switch to key the core memory with its own address. |
| LCHF | Last Character Flip-flop - This flip-flop is used to cause the Result Descriptor to be sent back to Core Memory. Also causes the Read Error Flip-flop (D20F) to be set. This flip-flop is set only when a card has been read, but all 80 CSP's were not received in the I/O Control Unit. |
| LØCL-C | Load Card Level - Derived from a toggle switch - used to cause a Card Read operation to occur without an Input/Output Descriptor from Core Memory. The card is read in Binary Mode. |
| LØTS-C | Load Timing Switch - used to initiate a Card Read cycle or an operation. |
| LPnF | Longitudinal Parity 1 $\Rightarrow$ P Flip-flops. Not used on Card Read operations. |
| MAED-C | Memory Address Error Level - Example: System has only one Memory Module, but D01F $\Rightarrow$ D15F address a non-existent Memory Module. |
| MANF | Memory Access Needed Flip-flop. |
| MAØF | Memory Access Obtained Flip-flop. |
| MAPS | Memory Access Permitted level. |
| MCYS | Memory Cycle level. Used during maintenance when only the logic of sequence counts 9 and 10 is to be executed. |
| MIR | Memory Information Register - Information register in each Memory Module (48 bits plus parity). |
| MISD | Memory Information Strobe Driver. Used to set information into the "W" Register. |
| MPED-M | Memory Parity Error Level - Level sent to Input/Output Control from a Memory Module at Memory Cycle time 4 to indicate a Parity error has occurred in MIR of that Module. |

| | |
|---|---|
| MTOD-M | Memory Time Zero Level - Level sent to Input/Output Control from a Memory Module. Level is true from $t_5$ to $t_0$ of Memory Cycle. |
| MT2D-M | Memory Time Two Level - Level sent to Input/Output Control from a Memory Module. Level is true from $t_1$ to $t_2$ of Memory Cycle. |
| MWRD | Memory Write Driver - Located in Input/Output Control. Used to indicate to the Memory Module a Memory Write Cycle is desired during this part of the operation. |
| Ø21D | This Driver is located in Input/Output Control and is used to send the Start Card Cycle to the Card Reader by way of Central Control. |
| Ø22D | This Driver is located in Input/Output Control and is used to send the Card Binary Level to the Card Reader by way of Central Control. |
| Ø23D | This Driver is located in Input/Output Control and is used to send the Card Binary Half Level to the Card Reader by way of Central Control. |
| PRØD | Proceed Driver - Made up of SC = 3 and CC = 5 and D16F on and D18F on. |
| $\overline{\text{PTØS}}$ | Not Printer Operation Level - Used to gate an action that happens on all operations except Printer operation. |
| RECF | Recycle Flip-flop - Used to allow consecutive maintenance cycles of a particular operation to occur. |
| REMF | Remote Flip-flop - On when the I/O Control Unit is in the remote mode. |
| SCCL | Start Card Cycle Level - Sent to the Card Reader by Ø21D at SC = 3 if the Card Reader is not busy and is ready. |
| SC=N | Sequence Counter equal to some value "N" - The Sequence Counter can be equal to any value from 0 - 15. Therefore the Sequence Counter consists of 4 flip-flops. |
| SC+1 | Sequence Counter plus one - Made up as a Driver called S+1D. |
| STRF | Strobe Flip-flop - This flip-flop is used for control purposes in the Input/Output Control Unit. It is turned on with every CSP from the Card Reader in Alpha Mode, twice in Binary Mode. |
| W01F ⇒ W15F | These flip-flops are part of the "W" Register. Usually contain the Core Memory address at the beginning of an operation, and data during an operation. |

| | |
|---|---|
| W16F ⇒ W22F | These flip-flops are part of the "W" Register. Their outputs are never sent to the "D" Register. They contain data during an operation. |
| W24F | This flip-flop is part of the "W" Register. Its output is sent to the "D" Register at the beginning of an operation. Determines an Input or Output operation. Contains data during an operation. |
| W27F | This flip-flop is part of the "W" Register. Its output is sent to the "D" Register at the beginning of an operation. Determines Alpha or Binary Mode operation. Contains data during operation. |
| W30F | This flip-flop is part of the "W" Register. Its output is sent to the "D" Register at the beginning of an operation. Contains data during an operation. |
| W31F ⇒ W40F | These flip-flops are part of the "W" Register. They contain the number of words per operation at the beginning of an operation. Contains data during an operation. |
| W41F ⇒ W45F | These flip-flops are part of the "W" Register. They contain the unit designation at the beginning of an operation. Contains data during an operation. |
| WC=N | Word Counter equal to some value "N" - The word counter can be equal to any value from 0 to 1023. |
| WC | Word Counter - It is made up of flip-flops D31F ⇒ D40F. In order to use this counter during an operation, D25F must be on. |
| WR | Word Register - Consists of 48 flip-flops W01F ⇒ W48F. All descriptors and data come from Core Memory and go to Core Memory through this register. |
| W(CC) | Portion of the W Register designated by the state of the CC. |

## 7.4 CARD PUNCH

### PURPOSE

To control the punching of a card in alphanumeric mode in conjunction with the operation of the 100 CPM Punch or the 300 CPM Punch. Information is read from Memory parallel by word and shifted to the Punch Unit serially by bit and punched by rows for ten words. Checking for punch errors is made in both Punch Units.

### PROVISIONS

When the object program finds that the memory area designated for output information is full of information, the Master Control Program will have compiled a Data Descriptor (I/O) for the area which will identify it for the Card Punch. To connect the Card Punch to that part of memory, the Master Control Program will examine the I/O Descriptors, mark the one which will accomplish the requirements as being the one to execute next and store its address in location 8. At the same time, it will signal Central Control that it has done this. Central Control will select the lowest numbered I/O Unit which is not busy and initiate it with an Admit Descriptor Level (ADnS). Refer to Figure 7.4-1.

### SUMMARY

Upon initiation from Central Control, an I/O Descriptor will be transferred out of memory to the I/O Control. The descriptor will be used to control punching of the card. The Descriptor contains the following information:

1. Unit Designation, u = 10 or 14 (Binary) for punches.
2. Type of operation (D24 = 0).
3. Selection of Stacker (D16 = 0/1) 300 CPM Punch only.
4. Starting Memory Address (D15 $\Rightarrow$ 1)

As the card is punched, a Result Descriptor is constructed and transferred to memory to indicate a successful (or unsuccessful) completion of the operation. The Result Descriptor contains the following information:

1. Unit Designation (unchanged from that above).
2. Unit Busy (D16F).
3. Descriptor Error (D17F).
4. Unit Not Ready (D18F).

5. Parity Error from Memory to I/O (D19F).

6. Punch Error (D20F).

7. Memory Address Error (D22F).

Since the card is fed twelve edge first, the information must be punched by rows, not columns. This means that all ten words must be examined for the appropriate bit to be sent to the punch buffer in the Punch Unit for all eighty columns of a row during each of twelve row counts. The actual punching is accomplished after all eighty bits have set up the interposers for each row. An internal compare network of the Punch will later perform a hole count check (Mod 8) of the information being sent for this card cycle.

Thus, the flow must make provisions for twelve repetitive reads of the ten words to be punched, send the proper bit to the Punch under control of Word Counter, Character Counter and the Card Punch decoder.

This supplementary section identifies the information and control signal lines and also the power lines between the 100/300 CPM Punch and the B 5000 Central Control.

Signals Delivered To Parallel Card Punch From Central Control

| NAME | DESCRIPTION |
|---|---|
| PBCL | Punch Bit Compare when positive indicates a true comparison between the row being addressed by the binary counter in the Punch (PRAL, PRBL, PRCL, PRDL) and the character bit for the addressed column. Maximum repetition rate is 66 KC. |
| SPOL | Start Punch Order Level is negative until PINL level from Punch is positive. |
| PUCP | Punch Clock Pulse is a series of 80 pulses produced by the pulse counter of I/O Control to permit the compare bit to transfer into the Punch Buffer. PUCP occurs during the compare bits and not at the end. Maximum repetition rate is 66 KC. |
| PASL | Punch Auxiliary Stacker Level. When negative indicates the card being punched will be ejected into the auxiliary stacker. |

Signals From 100/300 CPM Parallel Card Punch To Central Control

| | |
|---|---|
| PRAL | Punch Row Group A is negative whenever rows 12, 0, 2, 4, 6 and 8 are under the die and ready to receive information from the Processor. |
| PRBL | Punch Row Group B is negative whenever rows 11, 0, 3, 4, 7 and 8 are under the die and ready to receive information from the Processor. |

$\overline{\text{PRCL}}$ Punch Row Group C is negative whenever rows 1, 2, 3, 4 and 9 are under the die and ready to receive information from the Processor.

$\overline{\text{PRDL}}$ Punch Row Group D is negative whenever rows 5, 6, 7, 8 and 9 are under the die and ready to receive information from the Processor.

PUEF Punch Error Flip-Flop - Reset by initiation of a new punch cycle or the RESET button.

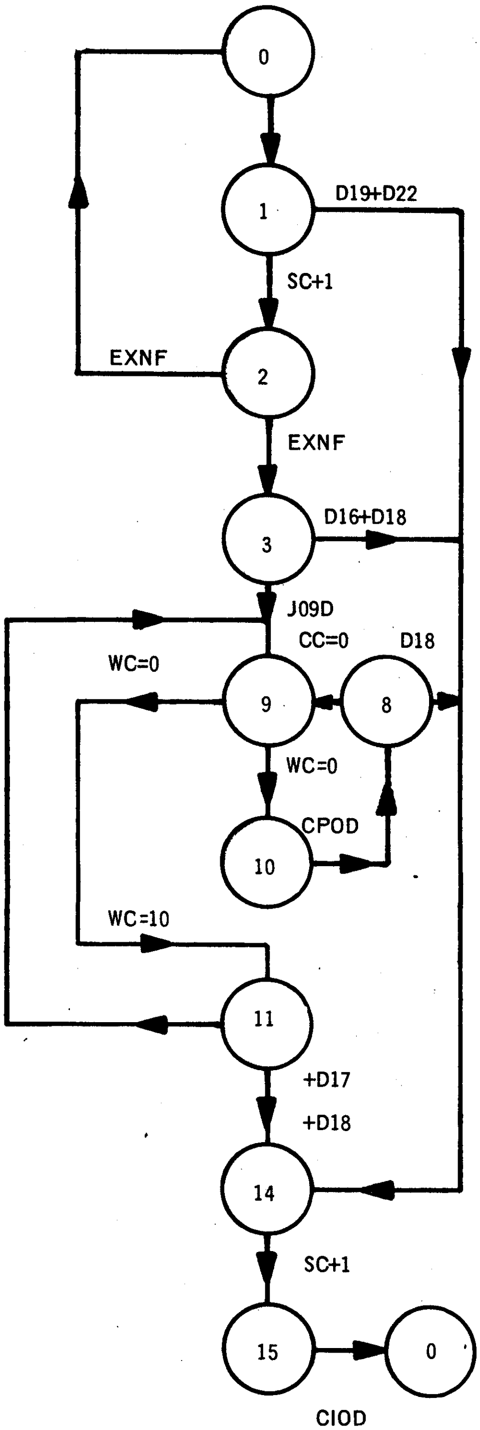
$\overline{\text{PINL}}$ $\overline{\text{Punch Information Needed Level}}$ is positive when a row is under the dies and the parallel punch is ready to accept row information. PINL is reset internally by address = 80.

$\overline{\text{PURL}}$ $\overline{\text{Punch Ready Level}}$ is positive when the following conditions are met:

1. Cards in the hopper
2. Die is in place
3. Card line mechanism is locked up
4. Card is in position to be punched
5. Stacker is not full
6. Power On
7. No jam condition exists (300 CPM Punch only)
8. Covers are in place.

$\overline{\text{PUCL}}$ $\overline{\text{Punch Cycle Level}}$ is positive from a Start Punch Order Level until the last row is punched and a new Start Punch may be initiated.

(Occurs within 20 µs of SPOL).




SC=0, 1 and 2: Operation initiated by ADNS signal from Central Control. Two memory accesses are performed.

1. Read Descriptor Address from Cell 8.

2. Read Descriptor from Memory.

SC=3: Interrogate Peripheral Unit Trunk, designate Peripheral Unit and interrogate Peripheral Units status (Ready - Busy - Punch Error).

SC=8: Transfer info to Punch. 10 words of 8 columns each are presented to the punch, via the Card Punch Decoder, for each of the 12 card rows.

SC=9 and 10: Access Memory for output data, index Address Counter, Word Counter, and test for memory errors.

SC=11: Restore Word Counter and Address Counter between punch rows. Test for last row and punch ready condition.

SC=14: Shift Result Descriptor to Wr.

SC=15: Transfer Result Descriptor to Memory.

FIGURE 7.4-1 B 5000 CARD PUNCH SEQUENCE COUNT STATE CHART

B 5000 GLOSSARY CARD PUNCH

| | |
|---|---|
| ADNS-C | Admit Descriptor Level - Comes from the Central Control Unit to an I/O Unit. |
| AØFF | Address Overflow Flip-Flop - Indicates the flip-flops DOIF ⇛ D15F were all equal to one when a Memory Cycle took place. Inhibits any further transfer of information to or from Core Memory. |
| AUNS-C | Admit Unit Level - Comes from Central Control to an I/O Unit - indicates unit is not busy. |
| CC=N, CC≠N | Character Counter is equal to or not equal to some number "N". The character counter consists of 3 flip-flops. |
| CC+1 | Character Counter plus One - in the logic book the driver is C+1D. |
| CDRD-1 | Clear "D" Register Driver No. 1. This driver clears D01F ⇛ D15F. |
| CIØD | Clear I/O Driver. Clears the I/O Control Unit when its output is true. |
| CØBD | Clear Ø. B. Register. |
| CPØD | Card Punch Operation. |
| CPTD | Card Punch Timing Driver. - It conditions the transfer of bit information to ØB1F. |
| D01F ⇛ D15F | These 15 flip-flops are part of the "D" register. During an operation they always contain the address of Core Memory that information is being sent to or taken from. |
| D16F | This flip-flop is part of the "D" register. The state of W16F is never sent to D16F, the opposite state of D16F is always sent to W16F. During an operation it is the Not Busy Flip-flop in the I/O Unit, at the completion of an operation it is the Busy Flip-flop of the Result Descriptor. |
| D17F | This flip-flop is part of the "D" register. The state of W17F is never sent to D17F. This flip-flop has many functions during an operation. It is used to remember that an Admit Descriptor Level has been received at the beginning of an operation. It is used to turn MANF on at SC = 0 time. |

If a Descriptor Parity error should occur it remembers it. It is part of the Result Descriptor. During the card punch cycle it is used to indicate the information for the last row has been sent to the Punch Unit.

D18F — This flip-flop is part of the "D" register. The state of W18F is never sent to D18F. The opposite state of D18F is always sent to W18F. During an operation it is the Ready Flip-flop in the I/O Unit, at the completion of an operation it is the Not Ready Flip-flop of the Result Descriptor.

D19F — This flip-flop is part of the "D" register. The state of W19F is never sent to D19F. If a parity error should occur during the transfer of information from core memory, this flip-flop remembers it. It is part of the Result Descriptor.

D20F — This flip-flop is part of the "D" register. The state of W20F is never sent to D20F. If a punch error should occur in the Card Punch, this flip-flop remembers it. It is part of the Result Descriptor.

D21F — This flip-flop is part of the "D" register. It is part of the Result Descriptor.

D22F= — This flip-flop is part of the "D" register. The state of W22F is never sent to D22F. If a Memory Overflow or Memory Address Error should occur, this flip-flop remembers it. It is part of the Result Descriptor.

D24F — This flip-flop is part of the "D" register. If the Input/Output Descriptor contains a zero in the 24th bit position, a Write Operation is indicated, if a one is contained in the 24th bit position a Read Operation is indicated. It is part of the Result Descriptor.

D25F — This flip-flop is part of the "D" register. It is used to indicate if this operation uses the Word Counter portion of the "D" register.

D26F — This flip-flop is part of the "D" register. When this flip-flop is on, the Card Punch is being sent a Start Punch Order Level through the Central Control Unit.

D27F — This flip-flop is part of the "D" register. If the Input/Output Descriptor contains a zero in the 27th bit position Alpha Mode operation is indicated, if a one is contained in the 27th bit position Binary Mode operation is indicated. It is part of the Result Descriptor.

D30F — This flip-flop is part of the "D" register. It is part of the Result Descriptor.

D31F ⇒ D40F — These flip-flops are part of the "D" register. They make up the Word Counter for all operations. The Card Punch operation uses D31F ⇒ D34F only.

D41F ⇒ D45F — These flip-flops are part of the "D" register. They are used to designate the peripheral unit that is to be controlled or that is to receive or send information. They are part of the Result Descriptor.

DERS — "D" Register Error Level. - If an error should occur during an operation this level will be true. The level is used in Central Control during a Load operation only.

DR — The Descriptor Register. - Consists of 42 flip-flops numbered D01F ⇒ D22F, D24F ⇒ D27F and D30F ⇒ D45F.

$\overline{\text{DRØS}}$ — Not Drum Operation Switch - used to gate an action that happens on all operations except Drum operation.

DWSD — "D" register to "W" register Shift Driver.

EXNF — External Control Flip-Flop - This flip-flop has many functions. It is used to indicate how many times the actions of SC=2 have been executed during the Card Punch operation. During the Card Punch operation it is used to re-establish the PINL level from the Punch Unit.

FIND — Finished Operation Driver.

HØLF — Hold Over Flip-Flop - used to allow only one group of actions to take place every 15 μs during Card Punch.

121D — This driver is located in Central Control and sends the Card Punch Ready level to the I/O unit.

122D — This driver is located in Central Control and sends the Punch Cycle level to the I/O unit.

123D — This driver is located in Central Control and sends the Punch Row A level to the I/O unit.

124D — This driver is located in Central Control and sends the Punch Row B level to the I/O unit.

125D — This driver is located in Central Control and sends the Punch Error Flip-flop state of the Card Punch to the I/O unit.

| | |
|---|---|
| 126D | This driver is located in Central Control and sends the Punch Row D level to the I/O unit. |
| 127D | This driver is located in Central Control and sends the Punch Information Needed level to the I/O unit. |
| 128D | This driver is located in Central Control and sends the Punch Row C level to the I/O unit. |
| 121S | This switch is located in the I/O unit and is used to invert the level received from the driver 121D of Central Control. |
| 122S | This switch is located in the I/O unit and is used to invert the level received from the driver 122D of Central Control. |
| 124S | This switch is located in the I/O unit and is used to invert the level received from the driver 124D of Central Control. |
| 127S | This switch is located in the I/O unit and is used to invert the level received from the driver 127D of Central Control. |
| IB | Input Buffer - Information from the Peripheral units is received in this buffer. It is made up of IB1F ⇒ IBPF. |
| IMCF | Initiate Maintenance Cycle Flip-flop. |
| IMCP | Initiate Maintenance Cycle Pulse. |
| I/Ø No. 1 | Input/Output Control Unit number one. |
| I/Ø No. 2 | Input/Output Control Unit number two. |
| I/Ø No. 3 | Input/Output Control Unit number three. |
| I/Ø No. 4 | Input/Output Control Unit number four. |
| JnnD | Jump to some number nn (0 ⇒ 15) Driver - used to set the Sequence Counter to a state 0 ⇒ 15. |
| KEML | Key Memory Level - Used in conjunction with the Memory Cycle switch to key the Core Memory with its own address. |
| LPnF | Longitudinal Parity 1 ⇒ P Flip-flops - Used during the Card Punch operation to retain the Punch Auxiliary Stacker Select level. |
| MAED-C | Memory Address Error Level - Example: System has only one Memory Module, but D01F ⇒ D15F address a non-existent Memory Module. |
| MANF | Memory Access Needed Flip-Flop. |

MAND — The output of the Memory Access Needed Driver is sent to the Memory Module designated by D13F ⇒ D15F. This output will only be true if the Memory Access Permitted level in the I/Ø unit is true.

MAØF — Memory Access Obtained Flip-Flop.

MAPS — Memory Access Permitted level.

MCYS — Memory Cycle level. Used during maintenance when only the logic of sequence counts 9 and 10 is to be executed.

MIR — Memory Information Register - Information register in each Memory Module (48 bits plus parity).

MISD — Memory Information Strobe Driver. Used to set information into the "W" register.

MPED-M — Memory Parity Error level. Level sent to Input/Output Control from a Memory Module at Memory Cycle time 4 to indicate a parity error has occurred in MIR of that Module.

MTOD-M — Memory Time Zero level - Level sent to Input/Output Control from a Memory Module. Level is true from $t_5$ to $t_0$ of Memory Cycle.

MT2D-M — Memory Time Two level - Level sent to Input/Output Control from a Memory Module. Level is true from $t_1$ to $t_2$ of Memory Cycle.

MWRD — Memory Write Driver - Located in Input/Output Control. Used to indicate to the Memory Module a Memory Write Cycle is desired during this part of the operation.

ØB — Output Buffer - Consists of six flip-flops and a parity generator. Card Punch operation uses OB1F only.

Ø24D — This Driver is located in Input/Output Control and is used to send the Start Punch Cycle to the Card Punch by way of Central Control.

Ø25D — This Driver is located in Input/Output Control and is used to send the Punch Clock Pulse to the Card Punch by way of Central Control.

Ø26D — This Driver is located in Input/Output Control and is used to send the Punch Auxiliary Stacker Select level to the Card Punch by way of Central Control.

| | |
|---|---|
| PASL | Punch Auxiliary Stacker Level - This level is sent to the Punch Unit by Ø26D and, when negative, indicates the card being punched will be sent to the auxiliary stacker. |
| PINL | Punch Information Needed Level - This level is from the Punch unit through 127D in the Central Control and is a request for more information from the I/O unit. |
| PC | Pulse Counter - The Pulse Counter counts at a one megacycle rate and is used to divide down the 1 MC clock to some predetermined rate. |
| PC = 14 | Pulse Counter equal Fourteen - The P.C. is recycled at 14 time for Punch Operation, thus providing a 66 KC recycle rate. |
| PRAL | Punch Row Group A level - 123D. |
| PRBL | Punch Row Group B level - 124D. |
| PRCL | Punch Row Group C level - 128D. |
| PRDL | Punch Row Group D level - 126D. |
| | The above four levels come from the Punch unit via the driver noted, and indicate which row of information is to be sent to the punch. |
| PRØD | Proceed Driver - Made up of SC = 3 and CC = 5 and D16F on and D18F on. |
| $\overline{\text{PTØS}}$ | Not Printer Operation Level - Used to gate an action that happens on all operations except Printer operation. |
| PUCL | Punch Unit Cycle Level - This level comes from the Punch Unit via 122D in Central Control, and when positive indicates a punch cycle is in progress. |
| PUCP | Punch Unit Clock Pulse - This is a 3 μs pulse sent to the Punch Unit by Ø25D. It occurs at PC = 9+10+11. |
| PUEF | Punch Unit Error Flip-Flop - This level comes from the Punch Unit via 125D in Central Control. |
| PURL | Punch Unit Ready level. |
| $\overline{\text{PURL}}$ | Punch Unit Not Ready Level - Produced by $\overline{\text{121S}}$ of the I/O unit. |
| RECF | Recycle Flip-Flop - Used to allow consecutive maintenance cycles of a particular operation to occur. |
| REMF | Remote Flip-Flop - On when the I/O Control unit is in the remote mode. |

| | |
|---|---|
| SC=N | Sequence Counter equal to some value "N". The Sequence Counter can be equal to any value from 0 - 15. Therefore, the Sequence Counter consists of 4 flip-flops. |
| SC+1 | Sequence Counter plus one - Made up as a Driver called S+1D. |
| SPØL | Start Punch Order Level - Sent to the Card Punch by Ø24D at SC=3 if the Card Punch is not busy and is ready. |
| STRF | Strobe Flip-Flop - This flip-flop is used for control purposes in the Input/Output Control Unit. It is turned on once every 15 µs when the Pulse Counter is equal to 14 during the Card Punch operation. |
| W01F ⇒ W15F | These flip-flops are part of the "W" register. Usually contain the Core Memory address at the beginning of an operation, and data during an operation. |
| W16F ⇒ W22F | These flip-flops are part of the "W" register. Their outputs are never sent to the "D" register. They contain data during an operation. |
| W24F | This flip-flop is part of the "W" register. Its output is sent to the "D" register at the beginning of an operation. Determines an input or output operation. Contains data during an operation. |
| W27F | This flip-flop is part of the "W" register. Its output is sent to the "D" register at the beginning of an operation. Determines Alpha or Binary Mode operation. Contains data during an operation. |
| W30F | This flip-flop is part of the "W" register. Its output is sent to the "D" register at the beginning of an operation. Contains data during an operation. |
| W31F ⇒ W40F | These flip-flops are part of the "W" register. They contain the number of words per operation at the beginning of an operation. Contain data during an operation. |
| W41F ⇒ W45F | These flip-flops are part of the "W" register. They contain the unit designation at the beginning of an operation. Contain data during an operation. |
| WC=N | Word Counter equal to some value "N" - The word counter can be equal to any value from 0 to 1023. |

| | |
|---|---|
| WC | Word Counter - It is made up of flip-flops D31F ⇒ D40F. In order to use this counter during an operation, D25F must be on. |
| WR | Word Register - Consists of 48 flip-flops W01F ⇒ W48F. All descriptors and data come from Core Memory and go to Core Memory through this register. |
| W[CC] | Portion of the "W" register designated by the state of the CC. |

## 7.5 MAGNETIC DRUM READ AND WRITE

PURPOSE

Read: To transfer up to a maximum of 1023 words from the Drum Unit to the High Speed Core Memory via the I/O Control Unit.

Write: To transfer up to a maximum of 1023 words from the High Speed Core Memory via the I/O Control Unit to the Drum Unit.

SUMMARY OF OPERATION

Upon initiation from Central Control Unit, an I/O Descriptor will be transferred to the I/O Control Unit from the High Speed Core Memory. The descriptor will control the reading from or the writing on the drum. This descriptor consists of the following information:

1. Type of operation (Drum Read or Write) (D46F)
2. Unit Designation (D41F ⇛ D45F)
3. Drum address (Source-Read, Destination-Write) (D16F ⇛ D30F)
4. Memory Address (Destination-Read, Source-Write) (D01F ⇛ D15F)
5. Number of Words (D31F ⇛ D40F)

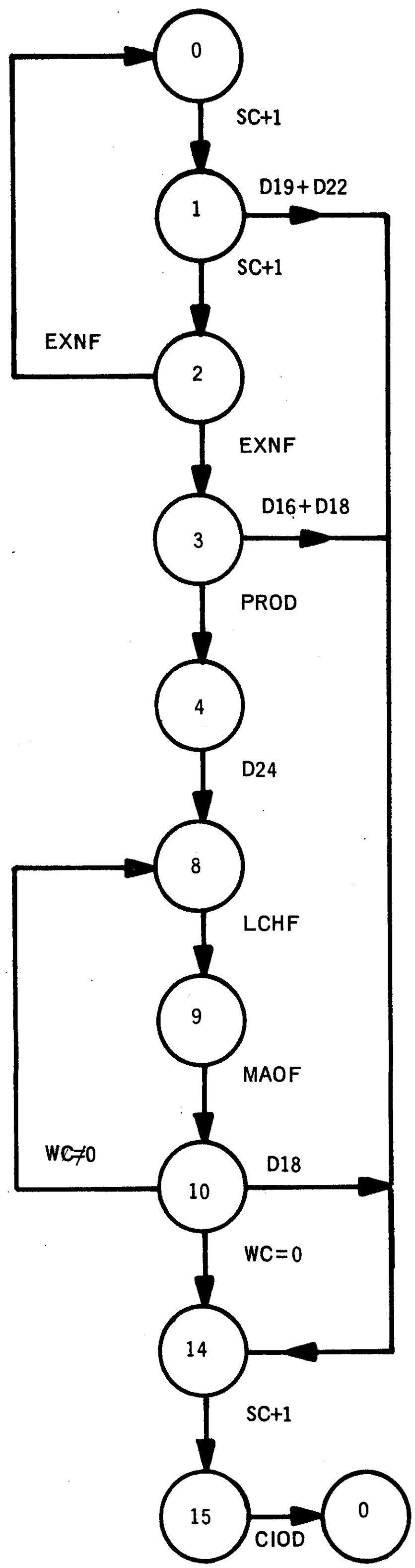
READ REFER TO FIGURE 7.5-1

Information is transferred from the Drum Unit during a Drum Read Operation, a character at a time, to the High Speed Core Memory via the I/O Control Unit. A single operation transfers a maximum of 1023 words. During a single read operation, it is possible to switch from one drum band to another.

If 1023 words are to be read from the drum with one descriptor, four drum revolutions are required to do so.

Longitudinal parity of each word is checked. During the execution of the operation, a Result Descriptor is constructed and transferred to memory indicating a successful or unsuccessful completion of the operation. This Result Descriptor contains the following information:

1. Unit designation (D41F ⇛ D45F)
2. Unit busy (D16F)
3. Unit not ready (D18F)




SC=0, 1 and 2: Operation initiated by ADNS or LOTS signal from Central Control. Two Memory Accesses are performed:

1. Read Descriptor Address from Memory Cell 8.

2. Read Descriptor from Memory.

SC=3: Interrogate Peripheral Unit Trunk, designate Peripheral Unit and interrogate Peripheral Units status (Ready - Busy).

SC=4: Transfer Drum starting address from Wr to the Drum Unit.

SC=8: Transfer info, presented by the Drum into "Wr" (Word Register). One word consists of 8 characters.

SC=9 and 10: Access Memory and transfer data word accumulated, in Wr, to Memory. Index - Word Counter, Address Counter

SC=14: Shift Result Descriptor.

SC=15: Transfer Result Descriptor to Memory and clear the I/O Unit.

FIGURE 7.5-1 B 5000 MAGNETIC DRUM READ SEQUENCE COUNT STATE CHART

4. Parity Error (from drum to I/O Control). (D19F)

5. Core Memory Address Error (D22F)

6. Descriptor Parity Error (D17F)

WRITE REFER TO FIGURE 7.5-2

During a Drum Write Operation, information is transferred from the High Speed Core Memory to the Drum Unit via the I/O Control Unit. One descriptor allows writing from one to 1023 words. If 1023 words are to be written on the drum with one descriptor, four drum revolutions are required to do so. A manual write lockout feature prevents writing on certain drum bands. A Result Descriptor is constructed during execution of the operation and is transferred to memory indicating a successful or unsuccessful completion of the operation. This Result Descriptor consists of the following information.

1. Unit designation (D41F ⇒ D45F)

2. Unit busy (D16F)

3. Unit not ready (D18F)

4. Parity error (from memory to I/O control) (D19F)

5. Drum address locked out (D21F)

6. Core Memory Address Error (D22F)

7. Descriptor parity error (D17F)

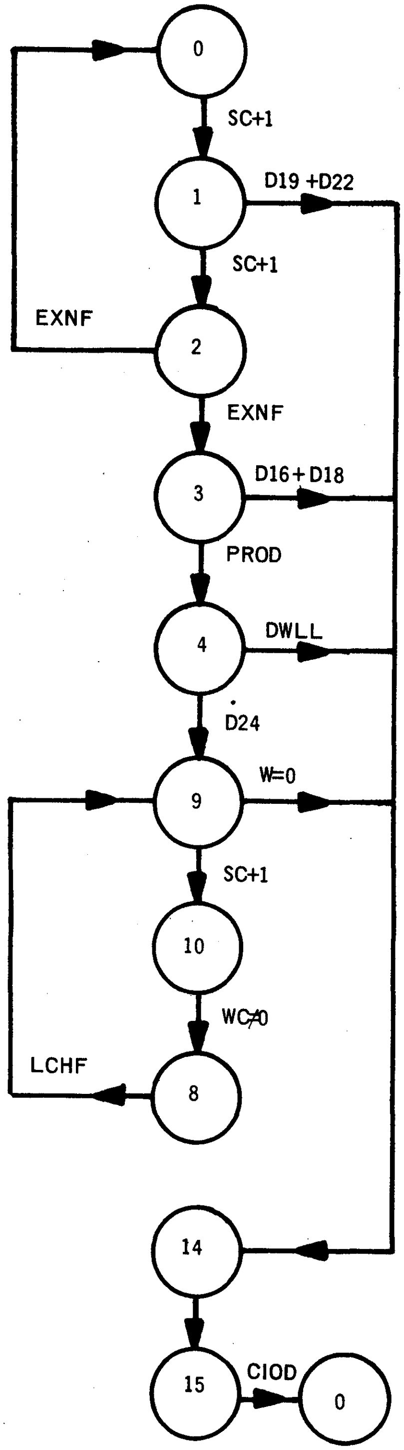
MAGNETIC DRUM - B 5000 CENTRAL CONTROL INTERCONNECTING CABLE

This defines all the Information and Control Signal Lines between the Magnetic Drum Unit and the B 5000 Central Control.

SIGNAL LINE DESCRIPTION

Signals Delivered to Magnetic Drum Unit From Central Control

| No. | Name | Description |
|---|---|---|
| 1. | DWI-1 | Drum Write Information Lines transfer one digit in |
| 2. | DWI-2 | parallel to the Drum Unit at a maximum repetition |
| 3. | DWI-4 | rate of 308 KC. |




SC=0, 1 and 2: Operation initiated by ADNS signal from Central Control. Two Memory Accesses are performed:

1. Read Descriptor Address from Memory Cell 8.

2. Read Descriptor from Memory.

SC=3: Interrogate Peripheral Unit trunk, designate Peripheral Unit, and interrogate Peripheral Units status (Ready - Busy).

SC=4: Transfer Drum starting address from Wr to the Drum unit.

SC=9, 10: Access Memory and Transfer one word, 8 characters, from Memory to Wr. Index the Word Counter and Address Counter.

SC=8: Transfer the contents of Wr to the Drum Unit.

SC=14: Shift Result Descriptor.

SC=15: Transfer Result Descriptor to Memory and Clear the I/O Unit.

FIGURE 7.5-2 B 5000 MAGNETIC DRUM WRITE SEQUENCE COUNT STATE CHART

| No. | Name | Description |
|---|---|---|
| 4. | DWI-8 | Each line, when negative, causes its corresponding |
| 5. | DWI-A | flip-flop to complement with a drum clock pulse. |
| 6. | DWI-B | |
| 7. | $\overline{\text{DWRL}}$ | Drum Write Level controls writing on or reading from the drum. When positive indicates "Write" - when negative indicates "Read". |
| 8. | $\overline{\text{DCL-1}}$ | Drum Control Levels 1-3 when positive indicate the |
| 9. | $\overline{\text{DCL-2}}$ | portion of Drum address available from I/O Control. |
| 10. | $\overline{\text{DCL-3}}$ | Repetition rate of 308 KC. |
| 11. | $\overline{\text{DCL-4}}$ | Drum Control Level -4 when positive indicates I/O is ready to receive information from or send information to the Drum Unit. |
| 12. | DCL-5 | Drum Control Level - 5 when negative inhibits clear of the Drum Unit. |
| 13. | $\overline{\text{DBSL}}$ | Drum Buffer Set Level when positive indicates: Set the Drum Buffer in order to write longitudinal parity. |
| 14. | Power On | |
| 15. | Power Off | |
| 16. | Power Interlock | |
| 17. | Power Control Common | |
| 21. | $\overline{\text{DURL}}$ | Drum Unit Ready Level when positive indicates the following conditions:<br>a. Drum address overflow does not exist.<br>b. Power is on.<br>c. Drum is up to speed.<br>d. Unit is in remote mode.<br>e. All covers are in place.<br>f. Word Counter Error does not exist. |
| 22. | $\overline{\text{DWLL}}$ | Drum Write Lockout Level when positive, indicates the I/O is trying to write in a drum address that is locked out by manual switches located in the Drum Unit. |

| | | |
|---|---|---|
| 23. | DRP-1 | Drum Read Information Pulse lines transfer one digit |
| 24. | DRP-2 | in parallel to the Input Character Buffer (IBIF-IBBF) |
| 25. | DRP-4 | in the I/O Control Unit at a maximum repetition rate of |
| 26. | DRP-8 | 308 KC. |
| 27. | DRP-A | |
| 28. | DRP-B | |
| 29. | DCLP | Drum Clock pulse is sent to the I/O Control Unit for control purposes. Repetition rate 308 KC. |
| 30. | $\overline{\text{DWCL}}$ | $\overline{\text{Drum Word Coinc. Level}}$ is sent to the I/O Control Unit for control purposes. Repetition rate 308 KC. |
| 31. | DSPL-1 | Drum Speed Line-1 is sent to Power Control to indicate the Drum is up to speed. |
| 32. | DSPL-2 | Drum Speed Line-2 is sent to Power Control to indicate the Drum is up to speed. |
| 33. | $\overline{\text{DRAL}}$ | $\overline{\text{Drum Available Level}}$ when positive indicates the Drum Unit is connected to Central Control. |

## SIGNAL LINE CHARACTERISTICS

### Definitions

1. Logical TRUE - A negative signal is defined as logical TRUE. A signal is negative if it is in the range of -3.0V to -4.8V.

2. Logical FALSE - A positive signal is defined as logical FALSE. A signal is positive if it is in the range of -0.3V to 0.0V.

3. LEVEL - A signal which is present for two or more clock times or whose pulse width is not critical is defined as a level, for example, the Unit Ready Level.

4. PULSE - A signal whose width is critical is defined as a pulse and the width is specified, for example, the Clock Pulse. Pulse width is measured at the minus 1.5V points.

5. DELAY TIME - Delay time is defined as the relationship between the specified signal at the receiving end of a cable and a reference signal in the receiving unit. It is measured at the minus 1.5V points.

6. SWITCHING TIME - Switching time is defined as the rise or fall time of a signal whichever is greater. It is specified between -0.3V and -2.0V. Unless specified otherwise, maximum switching time for signals is 1.0 μs.

B 5000 GLOSSARY DRUM MEMORY

ADNS-C — Admit Descriptor Level - Comes from the Central Control Unit to an I/O Unit.

AØFF — Address Overflow Flip-flop - Indicates the flip-flop D01F ⇛ D15F were all equal to one when a Memory Cycle took place. Inhibits any further transfer of information to or from Core Memory.

AUNS-C — Admit Unit level - Comes from Central Control to an I/O Unit - indicates unit is not busy.

CC=N, CC≠N — Character Counter is equal to or not equal to some number "N." The character counter consists of 3 flip-flops.

CC+1 — Character Counter plus One - in the logic book the driver is C+1D.

CDRD-1 — Clear "D" Register Driver No. 1 - This driver clears D01F ⇛ D15F.

CIØD — Clear I/O Driver - Clears the I/O Control Unit when its output is true.

D01F ⇛ D15F — These 15 flip-flops are part of the "D" register. During an operation they always contain the address of core memory that information is being sent to or taken from.

D16F — This flip-flop is part of the "D" register. The state of W16F is never sent to D16F, the opposite state of D16F is always sent to W16F. During an operation it is the Not Busy Flip-flop in the I/O Unit, at the completion of an operation it is the Busy Flip-flop of the Result Descriptor.

D17F — This flip-flop is part of the "D" register. The state of W17F is never sent to D17F. This flip-flop has many functions during an operation. It is used to remember that an Admit Descriptor level has been received at the beginning of an operation. It is used to turn MANF on at SC = 0 time. If a Descriptor Parity error should occur it remembers it. It is part of the Result Descriptor.

| | |
|---|---|
| D18F | This flip-flop is part of the "D" register. The state of W18F is never sent to D18F. The opposite state of D18F is always sent to W18F. During an operation it is the Ready Flip-flop in the I/O Unit, at the completion of an operation it is the Not Ready Flip-flop of the Result Descriptor. |
| D19F | This flip-flop is part of the "D" register. The state of W19F is never sent to D19F. If a parity error should occur during the transfer of information from core memory, this flip-flop remembers it. It is part of the Result Descriptor. |
| D20F | This flip-flop is part of the "D" register. The state of W20F is never sent to D20F. During the Drum Operation, D20F is used to develop the Drum Control levels 1, 2 and 3. It is part of the Result Descriptor. |
| D21F | This flip-flop is part of the "D" register. During the Drum Operation, D21F is used to develop the Drum Control levels 1, 2 and 3. If a Drum Write Lockout Condition should occur in the Drum Unit, this flip-flop remembers it. It is part of the Result Descriptor. |
| D22F | This flip-flop is part of the "D" register. The state of W22F is never sent to D22F. If a Memory Overflow or Memory Address Error should occur, this flip-flop remembers it. It is part of the Result Descriptor. |
| D24F | This flip-flop is part of the "D" register. If the Input/Output Descriptor contains a zero in the 24th bit position, a Write Operation is indicated, if a one is contained in the 24th bit position a Read Operation is indicated. It is part of the Result Descriptor. |
| D25F | This flip-flop is part of the "D" register. It is used to indicate if this operation uses the Word Counter portion of the "D" register. It is part of the Result Descriptor. |
| D26F | This flip-flop is part of the "D" register. It is part of the Result Descriptor. |
| D27F | This flip-flop is part of the "D" register. If the Input/Output Descriptor contains a zero in the 27th bit position Alpha Mode operation is indicated, if a one is contained in the 27th bit position Binary Mode operation is indicated. It is part of the Result Descriptor. |
| D30F | This flip-flop is part of the "D" register. It is part of the Result Descriptor. |
| D31F ⇒ D40F | These flip-flops are part of the "D" register. They make up the Word Counter for all operations. They are part of the Result Descriptor. |

| | |
|---|---|
| D41F ⇒ D45F | These flip-flops are part of the "D" register. They are used to designate the peripheral unit that is to be controlled or that is to receive or send information. They are part of the Result Descriptor. |
| DAR-9 | Drum Address Register Flip-flop Number 9 - Located in the Drum Unit and is used, along with IC, to indicate what Drum Revolution is being scanned. |
| DASD | Drum Address Shift Driver - Used at SC = 4 during the Magnetic Drum Operation. |
| DBSL | Drum Buffer Set Level - Level sent from the I/O Control Unit "LPWF Flip-flop" to the Drum Unit to control writing on the drum. |
| DCL-1 | Drum Control Level Number One - Used to tell the Magnetic Drum Unit when the "Lane" portion of the Drum Address is present on the information lines to the Drum Unit. (Ø22D) |
| DCL-2 | Drum Control Level Number Two - Used to tell the Magnetic Drum Unit when part of the "Word" portion of the Drum Address is present on the information lines to the Drum Unit. (Ø23D) |
| DCL-3 | Drum Control Level Number Three - Used to tell the Magnetic Drum Unit when part of the "Word" portion of the Drum Address is present on the information lines to the Drum Unit. (Ø24D) |
| DCL-4 | Drum Control Level Number Four - Used to tell the Magnetic Drum Unit when to begin looking for Word Coincidence. (Ø25D) |
| DCL-5 | Drum Control Level Number Five - Used to tell the Magnetic Drum Unit when to clear the flip-flops within the Drum Unit that will halt this operation. Certain flip-flops within the Drum Unit are never cleared. (Ø26D) |
| DCLP | Drum Clock Pulse - Sent from the Magnetic Drum Unit to the Input/Output Control Unit by way of Central Control (I24D). The Clock Pulses are present whenever the Drum Unit is designated. |
| DERS | "D" Register Error Level - If an error should occur during an operation this level will be true. The level is used in Central Control during a Load operation only. |
| DHSS | DROD • STRF • $\overline{\text{HOLF}}$ Switch - Used in those operations which require the conditions DROD true, STRF Flip-flop ON and HOLF Flip-flop OFF. |

| | |
|---|---|
| DIR | Drum Information Register - Located in the Drum Unit and is used to control the Drum Write amplifiers. |
| DM | Drum Marker Pulse - Pulse used in the Drum Unit and occurs once every drum revolution. |
| DR | The Descriptor Register - Consists of 42 flip-flops numbered D01F $\Rightarrow$ D22F, D24F $\Rightarrow$ D27F and D30F $\Rightarrow$ D45F. |
| DRCS | Drum Clear Switch - Located in the I/O Control Unit and is used to produce the DCL-5 level that is sent to the Magnetic Drum Unit by way of Central Control. (Ø26D) |
| DRØD | Drum Operation Driver. |
| DROS | Not Drum Operation Switch - Used to gate an action that happens on all operations except Drum operation. |
| DRP-n | Drum Read Pulse Lines - Pulses sent from the Magnetic Drum Unit to the I/O Control Unit "Input Buffer" when a one has been read from a particular channel of the drum. |
| DURL | Drum Unit Ready Level. (I21D) |
| DWCF | Drum Word Coincidence Flip-flop - Located in the Drum Unit and is used to produce the DWCL Level sent to I/O Unit by way of the Central Control. (I22D) |
| DWCL | Drum Word Coincidence Level - Produced in the Drum Unit and sent to the I/O Unit by way of the Central Control. (I22D) |
| DWI-n | Drum Write Information Lines - Levels sent from the I/O Control Unit "Output Buffer" to the Drum Unit to control writing on the Drum. |
| DWLL | Drum Write Lockout Level - Sent from the Magnetic Drum Unit to the Input/Output Control by way of Central Control. (I25D) Used to indicate the lane designated by descriptor is locked out in the Drum Unit. |
| DWRL | Drum Write Level - Produced in the I/O Control Unit by Ø21D and sent to the Magnetic Drum Unit. |
| DWSD | "D" register to "W" register Shift Driver. |
| EXNF | External Control Flip-flop - This flip-flop has many functions. It is used to indicate how many times the actions of SC=2 have been executed during the Magnetic Drum operation. |
| FIND | Finished Operation Driver. |
| HØLF | Hold Over Flip-flop - Used to allow only one group of actions to take place for every Drum Clock Pulse, when in SC=4 or when Drum Word Coincidence Level exists. |

| | |
|---|---|
| I01D ⇛ I06D | These drivers are located in Central Control and are used to send the 6 information levels to the I/O Unit. |
| I21D | This driver is located in Central Control and sends the Drum Unit Ready level to the I/O Unit. |
| I22D | This driver is located in Central Control and sends the Drum Word Coincidence level to the I/O Unit. |
| I24D | This driver is located in Central Control and sends the Drum Clock Pulse to the I/O Unit. |
| I25D | This driver is located in Central Control and sends the Drum Write Lockout Level to the I/O Unit. |
| I26D | This driver is located in Central Control. |
| I27D | This driver is located in Central Control. |
| I28D | This driver is located in Central Control. |
| I21S | This switch is located in the I/O Unit and is used to invert the level received from the driver I21D of Central Control. |
| I22S | This switch is located in the I/O Unit and is used to invert the level received from the driver I22D of Central Control. |
| I24S | This switch is located in the I/O Unit and is used to invert the level received from the driver I24D of Central Control. |
| I25S | This switch is located in the I/O Unit and is used to invert the level received from the driver I25D of Central Control. |
| IB | Input Buffer - Information from the peripheral units is received in this buffer. It is made up of IB1F ⇛ IBPF. |
| IC | Interlace Control Flip-flop - Located in the Drum Unit and is part of the Word Counter. This flip-flop complements with every Word Marker Pulse. It, along with DAR-9, essentially tells what revolution is being scanned. |
| IMCF | Initiate Maintenance Cycle Flip-flop. |
| IMCP | Initiate Maintenance Cycle Pulse. |
| I/Ø No. 1 | Input/Output Control Unit number one. |
| I/Ø No. 2 | Input/Output Control Unit number two. |
| I/Ø No. 3 | Input/Output Control Unit number three. |
| I/Ø No. 4 | Input/Output Control Unit number four. |

| | |
|---|---|
| IRCF | Information Register Control Flip-flop - Located in the Drum Unit and is used to allow the DIR's to sense the Information lines or levels from the Central Control. |
| JnnD | Jump to some number nn (0 $\Rightarrow$ 15) Driver - used to set the Sequence Counter to a state 0 $\Rightarrow$ 15. |
| KEML | Key Memory Level - Used in conjunction with the Memory Cycle switch to key the core memory with its own address. |
| LCHF | Last Character Flip-flop - Located in the I/O Control Unit and used to indicate a word has been accrued from or sent to the Drum. |
| LØDL-C | Load Drum Level - Derived from a toggle switch. - Used to cause a Magnetic Drum Read operation to occur without an Input/Output Descriptor from Core Memory. 512 words are transferred to Core Memory in the Binary Mode. |
| LØTS-C | Load Timing Switch - Used to initiate a Magnetic Drum Read operation. |
| LPnF | Longitudinal Parity 1 $\Rightarrow$ P Flip-flops - Used during the Magnetic Drum Read Operation to check Longitudinal Parity for each word read. |
| LPES | Longitudinal Parity Error Switch - Located in I/O Control Unit and is used to generate an error level should the LP[B $\Rightarrow$ 1] decade be anything other than 1's at parity time. |
| LPWF | Longitudinal Parity Write Flip-flop - Located in the I/O Control Unit and used to generate the DBSL level which is sent to the Drum Unit. |
| MAED-C | Memory Address Error Level - Example: System has only one Memory Module, but D01F $\Rightarrow$ D15F address a non-existent Memory Module. |
| MANF | Memory Access Needed Flip-flop. |
| MAND | The output of the Memory Access Needed Driver is sent to the Memory Module designated by D13F $\Rightarrow$ D15F. This output will only be true if the Memory Access Permitted level in the I/O is true. |
| MAØF | Memory Access Obtained Flip-flop. |
| MAPS | Memory Access Permitted Level. |
| MCYS | Memory Cycle Level - Used during maintenance when only the logic of sequence counts 9 and 10 is to be executed. |
| MIR | Memory Information Register - Information register in each Memory Module (48 bits plus parity). |

| | |
|---|---|
| MISD | Memory Information Strobe Driver - Used to set information into the "W" register. |
| MPED-M | Memory Parity Error Level - Level sent to Input/Output Control from a Memory Module at Memory Cycle time 4 to indicate a parity error has occurred in MIR of that Module. |
| MS10D | Maintenance Sequence Counter Ten Driver - Used to inhibit functions when the I/O Control Unit is in Maintenance Memory Cycle Operations. |
| MT0D-M | Memory Time Zero Level - Level sent to Input/Output Control from a Memory Module. Level is true from $t_5$ to $t_0$ of Memory Cycle. |
| MT2D-M | Memory Time Two Level - Level sent to Input/Output Control from a Memory Module. Level is true from $t_1$ to $t_2$ of Memory Cycle. |
| MWRD | Memory Write Driver - Located in Input/Output Control. Used to indicate to the Memory Module a Memory Write Cycle is desired during this part of the operation. |
| ØB | Output Buffer - Consists of six flip-flops and a parity generator. Magnetic Drum does not use the output of the parity generator. |
| Ø21D | This Driver is located in Input/Output Control and is used to send the Drum Write level to the Magnetic Drum Unit by way of Central Control. |
| Ø22D | This Driver is located in Input/Output Control and is used to send the Drum Control Level Number One to the Magnetic Drum Unit by way of Central Control. |
| Ø23D | This Driver is located in Input/Output Control and is used to send the Drum Control Level Number Two to the Magnetic Drum Unit by way of Central Control. |
| Ø24D | This Driver is located in Input/Output Control and is used to send the Drum Control Level Number Three to the Magnetic Drum Unit by way of Central Control. |
| Ø25D | This Driver is located in Input/Output Control and is used to send the Drum Control Level Number Four to the Magnetic Drum Unit by way of Central Control. |
| Ø26D | This Driver is located in Input/Output Control and is used to send the Drum Control Level Number Five to the Magnetic Drum Unit by way of Central Control. |

| | |
|---|---|
| Ø27D | This Driver is located in Input/Output Control and is used to send the Drum Buffer Set Level to the Magnetic Drum Unit by way of Central Control. |
| PRØD | Proceed Driver - Made up of SC = 3 and CC = 5 and D16F on and D18F on. |
| $\overline{\text{PTØS}}$ | Not Printer Operation Level - Used to gate an action that happens on all operations except Printer operation. |
| RECF | Recycle Flip-flop - Used to allow consecutive maintenance cycles of a particular operation to occur. |
| REMF | Remote Flip-flop - On when the I/O Control Unit is in the remote mode. |
| SC | Search Complete Flip-flop - Located in the Drum Unit and is used to indicate the word designated by the Descriptor has been found. It remains on until DCL-5 is sent to the Drum Unit. |
| SC=N | Sequence Counter equal to some value "N" in the I/O Unit - The Sequence Counter can be equal to any value from 0 - 15. Therefore, the Sequence Counter consists of 4 flip-flops. |
| SC+1 | Sequence Counter plus one - Made up as a Driver called S+1D. |
| STRF | Strobe Flip-flop - This flip-flop is used for control purposes in the Input/Outout Control Unit. It is turned on once every Drum Clock Pulse, when the Sequence Counter is equal to 4 or when Drum Word Coincidence level exists. |
| TWCD | Transfer From W Clocked Driver - Used to shift information a character at a time from the "W" Register to the Output Buffer Decade (ØB[B $\Rightarrow$ 1]) clocked. |
| TWUD | Transfer From W Unclocked Driver - Used to shift information a character at a time from the W register to the Output Buffer Decade (ØB[B $\Rightarrow$ 1]) unclocked. |
| W01F $\Rightarrow$ W15F | These flip-flops are part of the "W" register. Usually contain the Core Memory address at the beginning of an operation, and data during an operation. |
| W16F $\Rightarrow$ W22F | These flip-flops are part of the "W" register. Their outputs are never sent to the "D" register. They contain data during an operation. |
| W24F | This flip-flop is part of the "W" register. Its output is not sent to the "D" register at the beginning of an operation. Contains data during an operation. |

| | |
|---|---|
| W27F | This flip-flop is part of the "W" register. Its output is not sent to the "D" register at the beginning of an operation. Contains data during an operation. |
| W30F | This flip-flop is part of the "W" register. Its output is not sent to the "D" register at the beginning of an operation. Contains data during an operation. |
| W31F ⇒ W40F | These flip-flops are part of the "W" register. They contain the number of words per operation at the beginning of an operation. Contain data during an operation. |
| W41F ⇒ W45F | These flip-flops are part of the "W" register. They contain the unit designation at the beginning of an operation. Contain data during an operation. |
| W46F | This flip-flop is part of the "W" register. Its output is sent to the D24F of the "D" register at the beginning of an operation. Determines an input or output operation. Contains data during an operation. |
| WC=N | Word Counter equal to some value "N" - The word counter can be equal to any value from 0 to 1023. |
| WC | Word Counter - It is made up of flip-flops D31F ⇒ D40F. In order to use this counter during an operation, D25F must be on. |
| WR | Word Register - Consists of 48 flip-flops W01F ⇒ W48F. All descriptors and data come from Core Memory and go to Core Memory through this register. |
| W[CC] | Portion of the W register designated by the state of the CC. |

## 7.6 COMMON LANGUAGE DRUM PRINTER

### PURPOSE

The Data Descriptor for Printer operators will print one line of print (15 computer words). Most significant character in print position 1, least significant character in print position 120.

### SUMMARY OF OPERATION

Refer to Figure 7.6-1.

The print operation is started with an initiate level from the Central Control. This level sets the address register and initiates a memory cycle to bring the word in cell 8 of memory into the I/O Unit. This word contains the address of an I/O Data Descriptor. A second Memory Cycle is then initiated to bring the Data Descriptor into the I/O Control Unit ("D" register). If during this process a memory address or parity error condition occurs, the operation is terminated and a Result Descriptor, showing these errors, is sent back to the Processor.

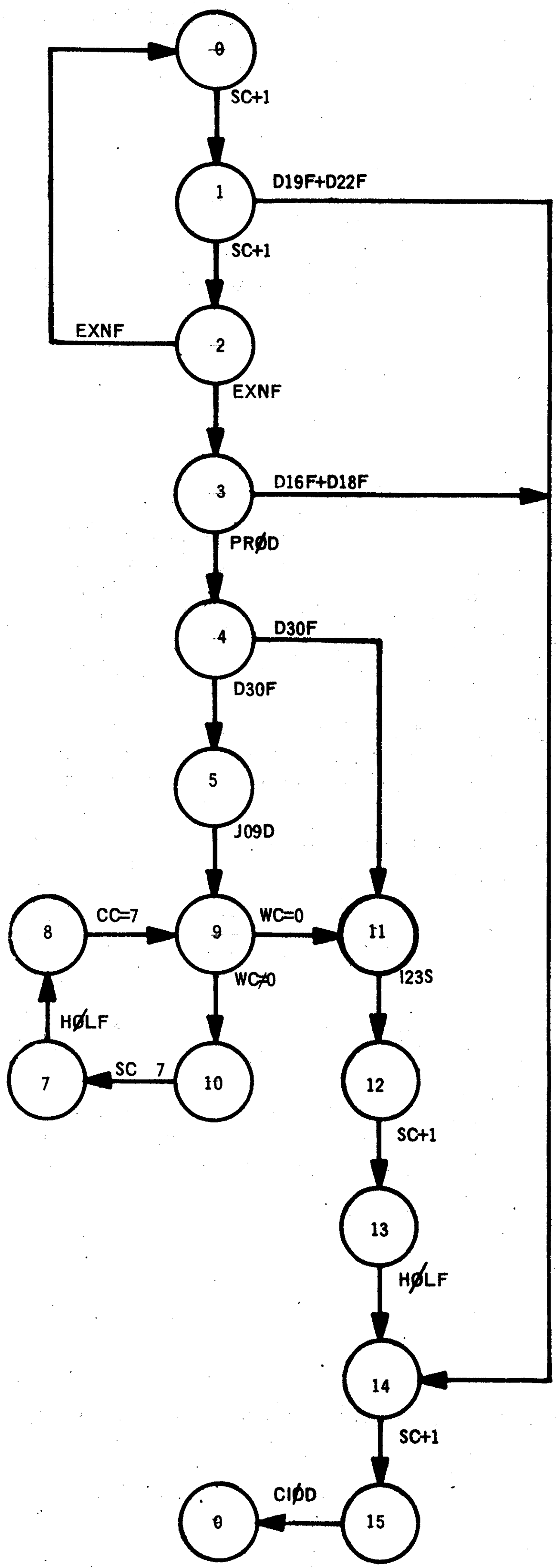
With the Data Descriptor in the "D" register the status of the peripheral unit (Printer) is checked. If the unit is ready and not busy the operation continues. Otherwise, the operation is terminated and a Result Descriptor is sent back to the Processor. The Data Descriptor address is increased by 15 to address the least significant word. Memory is then accessed to bring the 15th word into the Word Register of the I/O Control Unit. The transfer of characters commences with the least significant character. Characters are transferred from the Word Register to the output buffer and then to the printer information register. As each word is exhausted a new word is brought up and transferred character by character until 15 words have been transferred.

When all information is transferred, the Format Control digits are transferred to the output buffer and then to the format control flip-flops in the Printer. At the same time that the format digits are transferred the print cycle is initiated. End of Page sensing also occurs at this time. The Result Descriptor is sent back to memory and I/O Finished interrupt condition is set in Central Control and the Operation is complete. The Printer Print Cycle continues independent of the I/O Control Unit.

### COMMON LANGUAGE DRUM PRINTER - B 5000

### CENTRAL CONTROL INTERCONNECTING CABLE

This defines the information and control signal lines between the Common Language Drum Printer and the B 5000 Central Control Unit.




SC=0, 1, & 2: Operation initiated by AUNS from Central Control. Two Memory accesses performed.

1. Read Descriptor address from memory.
2. Read Descriptor from memory.

SC=3: Check peripheral unit for "ready" and "Not Busy".

SC=4: Check state of D30F.
1. D30F = Control Descriptor = Jump to [SC=11]
2. $\overline{\text{D30F}}$ = Not Control Descriptor = SC+1.

SC=5: Increase memory address by 15, set WC to 15.

SC=7: Sync on Printer Clock.

SC=8: Transfer data word to Printer.

SC=9 & 10: Access memory for data word.

SC=11: Wait for end of paper motion.

SC=12: Transfer format control bits from LP to OB.

SC=13: Transfer format control bits to printer and initiate print cycle.

SC=14: Construct result descriptor in "W" Register and address in D15 ⇒ 1

SC=15: Transfer result descriptor to memory and clear I/O Unit

FIGURE 7.6-1 B 5000 650 LPM PRINTER SEQUENCE COUNT STATE CHART

SIGNAL LINE DESCRIPTION

Signals Delivered to Drum Printer From Central Control

| NO. | NAME | DESCRIPTION |
|---|---|---|
| 1 | PI1L (FC1L) | Printer Information Lines transfer information, least significant digit first, to the Printer. The PIn Lines transfer information to the Printer's Information Register and Format Control Flip-flops. The actual transfer routing is controlled by the Printer Print Information Transfer and Printer Lister Command Levels. The PIn Levels are switched in the B 5000 I/O 2 μs after the occurrence of the Printer Lister Clock Pulse (PLCP). These lines are strobed in the Printer by PLCP. |
| 2 | PI2L (FC2L) | |
| 3 | PI4L (FC4L) | |
| 4 | PI8L (FC8L) | |
| 5 | PIAL (PDSL) | |
| 6 | PIBL (PSSL) | |
| 7 | PIPL | |

NOTE

The terms, in parenthesis, adjacent to the PInL denote the Format Control Function related to that line.

| NO. | NAME | DESCRIPTION |
|---|---|---|
| 15 | FC1L | Format Control Levels transfer the format control digit to the Format Control Flip-flops (FCF) in the Printer. They also set the Paper Motion Flip-flop (PMF) to initiate paper motion. These signals are clocked with the Data Processor Clock. |
| 16 | FC2L | |
| 17 | FC4L | |
| 18 | PC8L | |
| 19 | PDSL | Paper Double Space Level orders a double space by setting the Double Space Flip-flop (DSF) and initiates paper motion by setting PMF in the Printer. |
| 20 | PSSL | Paper Single Space Level initiates paper motion by setting PMF. PMF can be set by any one of lines 15 through 20, above. |

| | | |
|---|---|---|
| 22 | PLCL | Printer Lister Command Level when negative initiates Print Cycle after the transfer of information to the Print Buffer has been completed and paper has stopped.<br><br>PLCL also serves to route the transfer of Format Control Information into the Format Control Flip-flops. |
| 23 | PITL | Printer Print Information Transfer Level when negative indicates information is being transferred to the printer at a 100 KC rate. PITL serves to gate the information into the Information Register (IRF) in the Printer at least 10 μs after it goes true. PITL is true for one period before transfer of first character. Also used to clear the Parity Error Flip-flop. |
| 24 | EPRL | End of Page Reset Level, when negative, resets the End of Page Flip-flop (EOPF). |

Signals Delivered to Central Control Drum

| | | |
|---|---|---|
| 30 | PPEL | Printer Print Parity Error Level when negative indicates a parity error exists. |
| 31 | $\overline{\text{PRRL}}$ | $\overline{\text{Printer Ready Level}}$ when positive indicates the following conditions exist:<br><br>a. Power on, includes Drum Power<br><br>b. Paper loaded<br><br>c. No paper motion alarm and no 6-8 alarm and no slew alarm<br><br>d. START button depressed<br><br>e. Local/Remote switch in remote. |
| 32 | PCYL | Printer Print Cycle Level when negative indicates that a print cycle is in progress. |
| 33 | $\overline{\text{PAML}}$ | $\overline{\text{Paper Motion Level}}$, when positive, indicates that paper is in motion. |
| 34 | $\overline{\text{EOPL}}$ | $\overline{\text{End of Page Level}}$, when positive, indicates that end of page has been sensed. |
| 35 | PLCP | Printer Lister Clock Pulse is derived from the Printer Clock with a repetition rate of 100 KC. |

| | | |
|---|---|---|
| 36 | PIDL | Printer Interlock Level, when negative, indicates a Printer is connected. |

SIGNAL LINE CHARACTERISTICS

Definitions

1. Logical TRUE - A negative signal is defined as logical TRUE. A signal is negative if it is in the range of -3.0V to -4.8V.

2. Logical FALSE - A positive signal is defined as logical FALSE. A signal is positive if it is in the range of -0.3V to 0.0V.

3. LEVEL - A signal which is present for two or more clock times or whose pulse width is not critical is defined as a level, for example, the Unit Ready Level.

4. PULSE - A signal whose width is critical is defined as a pulse and the width is specified, for example, the Clock Pulse. Pulse width is measured at the minus 1.5V points.

5. DELAY TIME - Delay time is defined as the relationship between the specified signal at the receiving end of a cable and a reference signal in the receiving unit. It is measured at the minus 1.5V points.

6. SWITCHING TIME - Switching time is defined as the rise or fall time of a signal whichever is greater. It is specified between -0.3V and 2.0V. Unless specified otherwise, maximum switching time is 1.0 μs.

## 7.7 PAPER TAPE READ, SPACE AND REWIND

I/O DESCRIPTOR

The I/O Descriptor for the Paper Tape Reader is basically a Read descriptor but has Space and Rewind variants

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 | 45 | | | | | 30 | 27 | 24 | | | 15 | | | | |
| 47 | | 41 | | | | 29 | 26 | | | | | | | | |
| 46 | | 40 | | | 31 | 28 | 25 | | | | | | | | 1 |

48 - Always on for descriptor

47 - Always off for I/O descriptor

46 - Presence bit

41 => 45 - Unit designate (18 or 20)

31 => 40 - Word Counter (0 = No Op)

30 - 0 Paper Tape Read
1 Paper Tape Space

28 and 29 - Integer and Continuity bits

27 - 0 Alphanumeric read
1 Binary read

26 - 0 Read or Space as indicated by D30
1 Rewind

25 - Always on (use Word Counter)

24 - Always on (input operation)

1 => 15 - Starting memory address

RESULT DESCRIPTOR

A list of the result descriptor indicators follows:

D16F - I/O conflict

D17F - Failure to obtain I/O descriptor

D18F - Unit not ready

D19F - Parity error

D20F - Beginning of tape

D21F - End of tape

D22F - Memory overflow

SUBSYSTEM CONFIGURATION

A Paper Tape subsystem can consist of any one of the following configurations:

1 Reader and 0 Punches

1 Reader and 1 Punch

2 Readers and 1 Punch

0 Readers and 1 Punch

1 Reader and 2 Punches

Information is normally punched in BCL code but code translators are available. With code translators, the Reader can accept tapes from the following equipment: (1) P 1100 and P 1160; (2) Sensimatic with A 520 Punch; (3) E 101 Computer, and; (3) Teletype Model 28.

GENERAL DESCRIPTION OF READER

A list of general characteristics follows:

1. Reading speed = 1000 characters per second (high)
   500 characters per second (low)

2. Up to seven inch diameter reels can be used.

3. Capable of handling 5, 6, 7, or 8 level tape as selected by operator.

4. Capable of handling 11/16", 7/8", or 1" tape interchangeably.

5. Capable of performing off-line parity check. Reader stops when parity error is detected.

6. Beginning and end of tape are sensed via adhesive conductive strips on the tape being read. The adhesive strip holds for a period of one week.

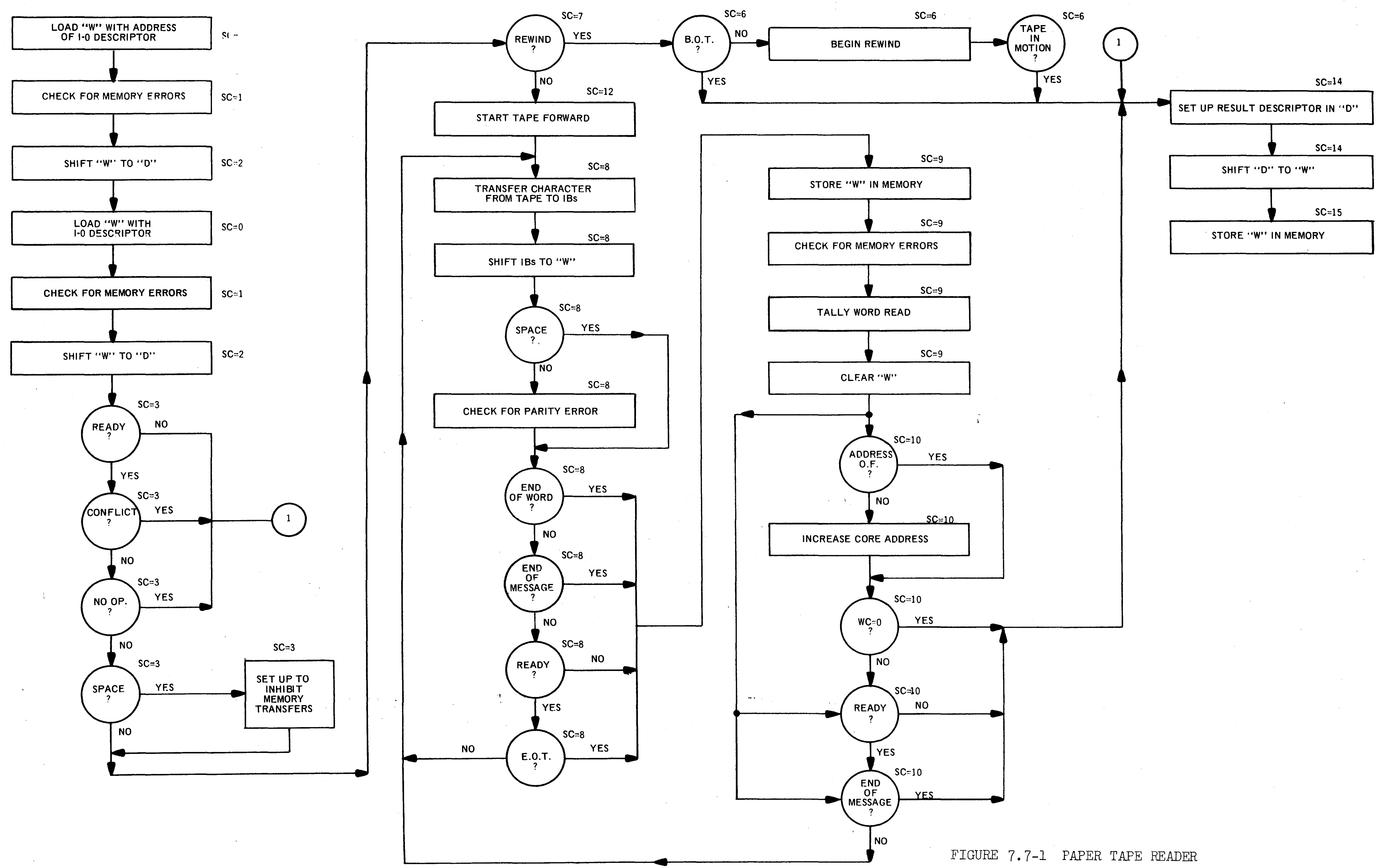



FIGURE 7.7-1 PAPER TAPE READER

7. The Reader is not ready for any one of the following reasons:

   a. In Local
   b. Broken tape
   c. Power Off

8. The Reader is in the busy state during Read, Space, and Rewind all of which are capable of being specified by the Reader I/O descriptor.

## GENERAL DESCRIPTION OF READER OPERATION

Refer to Figure 7.7-1.

Paper tape can only be read while tape is being driven in the forward direction. Words are read into successively higher memory locations.

During alphanumeric read, reading continues until the Paper Tape Reader senses a control code. If the Word Counter reaches zero before the control code is sensed, the Word Counter will terminate the operation.

During binary read, reading continues until the initial Word Counter setting has been reduced to zero. Record length can be from 1 to 1023 words.

Forward Space is a variant of the Read I/O descriptor. Forward Space can be alphanumeric (stop on control code or Word Counter equal 0) or binary (stop on Word Counter equal 0).

Rewind is also a variant of the Read I/O descriptor. Rewind operates independent of the I/O Control Unit after it has been initiated.

## SIGNAL LINE DESCRIPTION

$\overline{\text{CBIL}}$ - The $\overline{\text{Card Reader Binary Level}}$, when positive (false), selects binary read which bypasses the Code Translator used in alphanumeric read.

$\overline{\text{CCL}}$ - The $\overline{\text{Card Cycle Level}}$ is positive (false) from 10 μs after the time that $\overline{\text{SCCL}}$ or $\overline{\text{PRWL}}$ is accepted until at least 300 μs after a Stop CSP.

CC1L => CCBL - The Column Character Lines contain the column character information for a minimum period of 300 μs from CSP time. They are reset or changed prior to the next CSP.

$\overline{\text{CREL}}$ - The $\overline{\text{Card Reader Error Level}}$, when positive (false), indicates that there has been a Paper Tape Read Parity error. CREL can be reset by SCCL or the Parity On - Off switch.

$\overline{\text{CRL}}$ - The $\overline{\text{Card Ready Level}}$ is positive when the Paper Tape Reader is ready to accept $\overline{\text{SCCL}}$ signals and results from the following conditions being met.

1. Remote - Local switch in Remote.
2. Tape not broken.
3. Power on.
4. Ready button depressed.

CSP - The Column Strobe Pulse is a negative-going timing pulse which samples each character read from paper tape.

EOFL - The End of File Level is negative if the Paper Tape Reader is at the end of tape.

PBTL - The Paper Tape Begin Level is negative when the Paper Tape Reader is sensing the beginning of tape.

PEML - The Paper End Message Level goes negative for more than 300 µs after the stop character SCP goes positive.

$\overline{\text{PRWL}}$ - The $\overline{\text{Paper Tape Rewind Level}}$ goes positive to cause the Paper Tape Reader to start a Rewind operation. When CCL is positive, it resets $\overline{\text{PRWL}}$.

$\overline{\text{PSTL}}$ - The $\overline{\text{Paper Tape Stop Level}}$ goes positive after the CSP from the next to last character. This signals a paper tape stop. The CSP from the last character returns $\overline{\text{PSTL}}$ to negative.

$\overline{\text{SCCL}}$ - The $\overline{\text{Start Card Cycle Level}}$, when positive (false), causes the Paper Tape Reader to start a read operation. $\overline{\text{SCCL}}$ remains positive until the $\overline{\text{Card Cycle Level}}$ ($\overline{\text{CCL}}$), goes positive indicating that the Paper Tape Reader has been started.

## 7.8 PAPER TAPE PUNCH

rD

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 | 45 | 42 | 39 | 36 | 33 | 30 | 27 | 24 | | | 15 | 12 | 9 | 6 | 3 |
| 47 | 44 | 41 | 38 | 35 | 32 | | | | | | 14 | 11 | 8 | 5 | 2 |
| 46 | 43 | 40 | 37 | 34 | 31 | | 25 | | | | 13 | 10 | 7 | 4 | 1 |

D48, D47 = 1, 0(Flag & ID Bits)

D46 = X (Presence Bit)

D45 ⇛ D41 = Unit Designate

D40 ⇛ D31 = Word Counter (Max. = 1023; Minimum = 1; 0 = No. Op) Word Count n specifies the number of words to be punched in Binary Mode & the MAXIMUM number of words in Alpha Mode. In Alpha Mode an end of file character may terminate the punch operation before the word counter is equal to zero.

D30 = 1 - used with D27F on to indicate a tape feed operation (no information transferred).

D27 = 0 Alphanumeric
1 Binary

D26 = Not used

D25 = 1 Inhibit Memory Transfer after Word Count n has been satisfied. In Alphanumeric the record may be terminated by an end of message character or WC=0 (whichever occurs first). D25 is always on regardless of type (Binary/Alphanumeric) of record being punched.

D24 = 0 - Output operation.

D15 ⇛ D1 = Starting memory address. Words are written from successively higher addresses.

**RESULT DESCRIPTOR**

The basic error and control field of D16, D17, D18, and D22 is utilized. In addition to the basic field, the following bits are used as flags:

D19 = 1 Parity error from core memory

D21 = 1 End of tape flag. End of tape level (PETL) becomes true when the supply reel contains 35 feet or less of paper tape.

SUBSYSTEM CONFIGURATION

A paper tape subsystem can consist of any one of the following configurations:

1 Reader and 0 Punches

1 Reader and 1 Punch

2 Readers and 1 Punch

1 Reader and 2 Punches

GENERAL DESCRIPTION OF PUNCH

The basic unit of the Paper Tape Punch is a teletype Model BRPE11 Paper Tape Punch.

A list of general characteristics follows:

1. The Paper Tape Punch is capable of punching 5, 6, 7, or 8 level tape at a minimum rate of 100 characters per second.

2. Packing density is 10 characters per inch.

3. Standard tape widths of 11/16", 7/8" and 1" may be punched.

4. The punch is capable of punching oiled paper tape, dry paper tape, metalized mylar tape, or paper laminate mylar tape.

5. A Code Translator permits the translation of BCL to a single frame code via a removeable plugboard. Up to 64 different characters may be punched in up to 8 channels. A prewired, direct plugboard is used when BCL is to be punched.

6. The maximum payoff reel size is 8" outside diameter (1000 feet of 4 mil. tape). Reel hub diameter is 2".

   Maximum pickup reel size (Burroughs 220 reels) is 7" diameter (700 feet of 4 mil. tape). NARTB (STANDARD HUB) reels up to 8" diameter may be utilized. It requires less than 1/2 hour to change between 220 reels and NARTB reels. Tape can be punched without the use of a pickup reel.

7. The operator may interchange any of the 7 BCL input levels with any of the 8 possible output channels. Undesignated channels are not punched or sensed as controls.

8. Paper tape perforation sizes and standard spacing are the same as those specified for 220 paper tape.

9. The Paper Tape Punch is NOT READY to the associated Processor if any one of the following conditions is present:

   a. The Remote/Local switch is in the LOCAL position.
   b. Power is off.
   c. Feed reel tape breaks.

GENERAL DESCRIPTION OF PUNCH OPERATIONS

Refer to Figure 7.8-1.

Punch Request

A Paper Tape Punch operation request is initiated remotely by the admittance of an I/O Descriptor to an available I/O unit by CC. The following control information must be supplied by this descriptor:

| | |
|---|---|
| Always indicate WC control | D25F = 1 |
| Unit Designation | D[45 ⇒ 41] |
| Input/Output Operation | D24F/$\overline{\text{D24F}}$ |
| Alphanumeric/Binary information transfer | $\overline{\text{D27F}}$/D27F |
| Starting Address of record | D[15 ⇒ 1] |
| Number of words in record to be transferred | D[40 ⇒ 31] |

Trunk Availability

Punch Ready

With the admittance of the Punch Descriptor to an I/O unit the following interrogations and results of the interrogations are made:

Is the Punch Unit trunk busy?

Is the Punch Unit ready?

Store the results of the above interrogations in D16F and D18F respectively.

Results of Interrogations

If D16F is off, indicating that the Punch Unit trunk is being used by another I/O, then exit to SC14 and store this Result Descriptor. If D18F is off, indicating that the Punch Unit is NOT READY, then exit to SC14 and store this Result Descriptor.

If D16 and D18F are on, actuate the Punch Unit, transfer record information from Core Memory to the Word Register, allow Punch Unit to get up to speed and wait for "information needed" indication from the Punch.

Information Transfer

Information Strobe

Information Punch

An "information needed" indication from the Punch Unit initiates the following sequence of operations for all but the first character of the record.

1. Designated character to the Output Buffer.

2. Designated character in the Output Buffer.

3. Strobe Output Buffer lines and set up punch magnet register.

4. Actuate the punch magnets.

Record Transfer Completed

WC=0 flags the end of a Binary record.

WC=0 or "end of message character" (whichever occurs first) flags the end of the alphanumeric record.

NOTE

D25F is always equal to one during Paper Tape Punch operations.

Store the Result Descriptor

SIGNAL LINE DESCRIPTION

NAME

$\overline{\text{POPL}}$ (Parity bit)

$\overline{\text{POBL}}$ (B bit)

$\overline{\text{POAL}}$ (A bit)

$\overline{\text{PO8L}}$ (8 bit)

$\overline{\text{PO4L}}$ (4 bit)

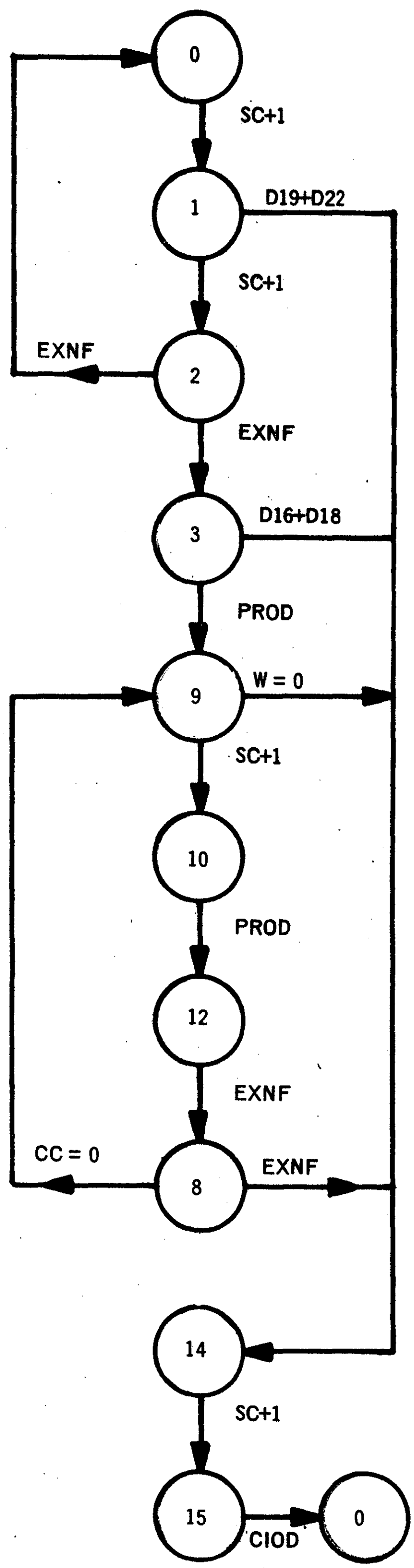
$\overline{\text{PO2L}}$ (2 bit)

$\overline{\text{PBCL}}$ (1 bit)

$\overline{\text{Punch Output n Levels}}$ when false, indicate the bits to be punched for the character being transmitted from the Data Processor. Maximum repetition rate of transfer is controlled by the level $\overline{\text{PINL}}$.

CONTROL LEVELS

| Description | I/O Exchange | Punch Level |
|---|---|---|
| Punch information needed | I24D | $\overline{\text{PINL}}$ |
| Paper Tape Punch Ready Level | I21D | $\overline{\text{PURL}}$ |
| Paper Tape Feed Level | O26D | SPOL |
| End of Message Level | I23D | PUEL |
| End of Tape Level | I25D | PETL |
| Info strobe pulse. (indicates information is present on the PONL and $\overline{\text{PBCL}}$ lines). | O21D | PUCP |
| Punch Binary Level | O22D | $\overline{\text{PBNL}}$ |




SC=0, 1 & 2: Operation initiated by AUNS from Central Control. Two memory accesses performed.

1. Read descriptor address from memory.

2. Read descriptor from memory.

SC=3: Check peripheral unit for "ready" and "not busy".

SC=9 & 10: Access memory for data word to be punched.

SC=12: Sync I/O Control will paper tape.

SC=8: Transfer word to be punched to the Punch.

SC=14: Construct result descriptor.

SC=15: Transfer result descriptor to memory and clear I/O unit.

FIGURE 7.8-1 B 5000 PAPER TAPE PUNCH SEQUENCE COUNT STATE CHART

## 7.9 SPO - KEYBOARD

PURPOSE

The SPO-Keyboard provides a means for the system to communicate with the operator and vise versa.

SUMMARY OF OPERATION

Keyboard Input (Refer to Figure 7.9-1)

Input from the keyboard is initiated by the depression of the Interrupt key which places a bit in the interrupt register, forming address 20.

The Master Control Program then assigns a portion of High Speed Memory for the keyboard input data and sends a keyboard read descriptor to an I/O Control Unit, lighting a Ready light on the keyboard.

The operator enters information from the keyboard. The data is accumulated by character in the W register, parity checked, and sent to memory. When finished with input, the operator depresses the End of Input key which places a group mark in memory and causes the remainder of the word to be filled with the character (00 000) internal code.

If an operator error occurs during input the information can be flagged by depressing the Error key which will transmit a character containing a parity error. This parity error will be indicated by D20 in the result descriptor.

Supervisory Printout (Refer to Figure 7.9-2)

The information to be printed is sent from High Speed Memory to the typewriter via the I/O Control Unit's W register. Printing continues until a group mark is encountered in Memory. The group mark results in a carriage return with a line feed.

There is no parity check on output data transferred from the I/O Control Unit to the Supervisory Printer.

SPO-KEYBOARD DESCRIPTOR

The descriptor will contain the following information:

| | | |
|---|---|---|
| D47, D48 | = | 1, 0 (Flag, I.D. Bits) |
| D46 | = | X (Presence Bit) |
| D45 $\Rightarrow$ D41 | = | Unit Designate u<br>u = 30 (Binary) |

| | | |
|---|---|---|
| D40 ⇒ D31 | = | Not used |
| D30 ⇒ D25 | = | Must be set to zero |
| D24 | = | 0 Printout |
| | = | 1 Keyboard Input |
| D23 ⇒ D16 | = | Not used |
| D15 ⇒ D1 | = | Starting memory address |

SPO Keyboard Result Descriptor

The basic error and control field of D16, D17, D18, D22 is used. See Subject 7.1.

In addition to the basic field, the following bits are used as flags:

Print Output: D19 - Memory to I/O Parity Error

Keyboard Input: D20 - Character Input Error

Signals to the SPO-Keyboard From I/O

1. $\overline{\text{ODRL}}$ - The Output Driver Level, when positive, activates the mechanical gear in the SPO when reading out a character from the I/O output buffer to the SPO.

2. $\overline{\text{TOPL}}$ - The Teletype Operation Level is positive for input (Keyboard Read) and negative for output (Supervisory Printout).

3. IN = n - The Output Buffer Information Levels are 6 information lines from the I/O output buffer to the SPO.

Signals From the SPO-Keyboard to I/O

1. $\overline{\text{ICRL}}$ - The Input Character Ready Level is positive when an input character is present in the SPO-Keyboard and is ready to be written into the I/O Input Buffer.

2. $\overline{\text{OCRL}}$ - The Output Character Ready Level is positive when the SPO-Keyboard is ready for a new character to be read out of the I/O Output Buffer.

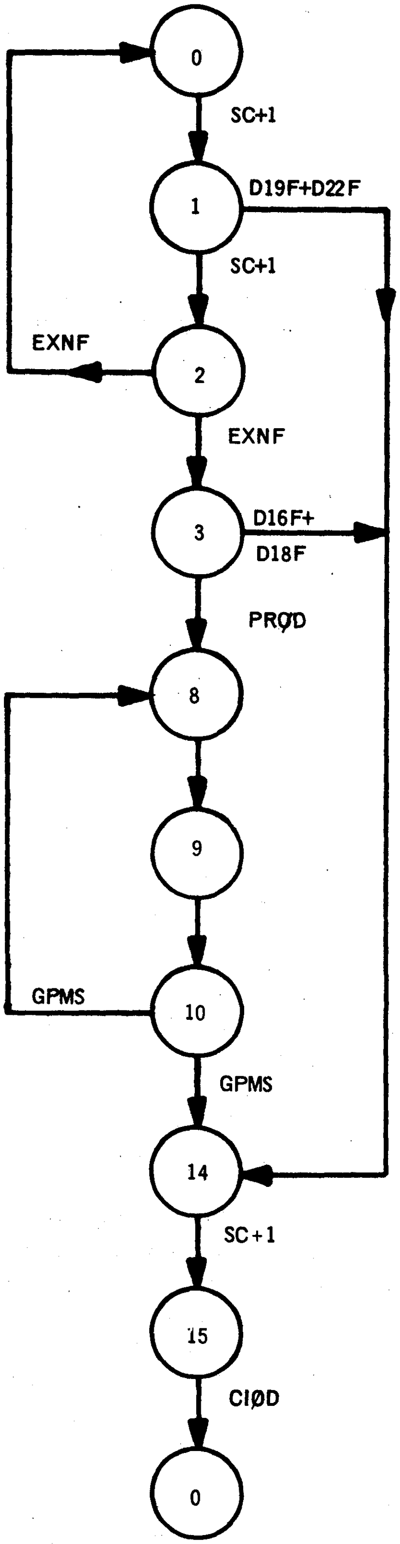
3. $\overline{\text{TRDL}}$ - The Teletype Ready Level is positive when power is "on" plus other interlock conditions and the SPO-Keyboard is ready for an input/output operation.

4. $\overline{\text{TINL}}$ - The Teletype Interrupt Level is positive when a "Keyboard Read" has been requested. This level is sent to the Central Control Interrupt Register.

5. ICL-N - The Teletype Information Levels are 7 information lines from the SPO-Keyboard to the I/O Input Buffer.

B 5000 GLOSSARY SPO/KEYBOARD

| | |
|---|---|
| ADNS-C | Admit Descriptor Level - Comes from the Central Control Unit to an I/O Unit. |
| AØFF | Address Overflow Flip-flop - Indicates the Flip-flops D01F ⇒ D15F were all equal to one when a Memory Cycle took place. Inhibits any further transfer of information to or from Core Memory. |
| AUNS-C | Admit Unit Level - Comes from Central Control to an I/O Unit - indicates unit is not busy. |
| CC=N, CC≠N | Character Counter is equal to or not equal to some number "N" - The character counter consists of 3 flip-flops. |
| CC+1 | Character Counter plus One - In the logic book the driver is C+1D. |
| CDRD-1 | Clear "D" Register Driver No. 1 - This driver clears D01F ⇒ D15F. |
| CIØD | Clear I/O Driver - Clears the I/O Control Unit when true. |
| D01F ⇒ D15F | These 15 flip-flops are part of the "D" register. During an operation they always contain the address of core memory that information is being sent to or taken from. |
| D16F | This flip-flop is part of the "D" Register. The state of W16F is never sent to D16F, the opposite state of D16F is always sent to W16F. During an operation it is the Not Busy Flip-flop in the I/O Unit, at the completion of an operation it is the Busy Flip-flop of the Result Descriptor. |
| D17F | This flip-flop is part of the "D" Register. The state of W17F is never sent to D17F. This flip-flop has many functions during an operation. It is used to remember that an Admit Descriptor level has been received at the beginning of an operation. It is used to turn MANF on at SC = 0 time. If a Descriptor Parity error should occur it remembers it. It is part of the Result Descriptor. |
| D18F | This flip-flop is part of the "D" Register. The state of W18F is never sent to D18F. The opposite state of D18F is always sent to W18F. During an operation it is the Ready Flip-flop in the I/O Unit. At the completion of an operation it is the Not Ready Flip-flop of the Result Descriptor. |




SC=0, 1 & 2: Operation initiated by AUNS from Central Control. Two Memory Accesses performed.

1. Read Descriptor Address from Memory.

2. Read Descriptor from Memory.

SC=3: Check Peripheral Unit for "READY" and "NOT BUSY".

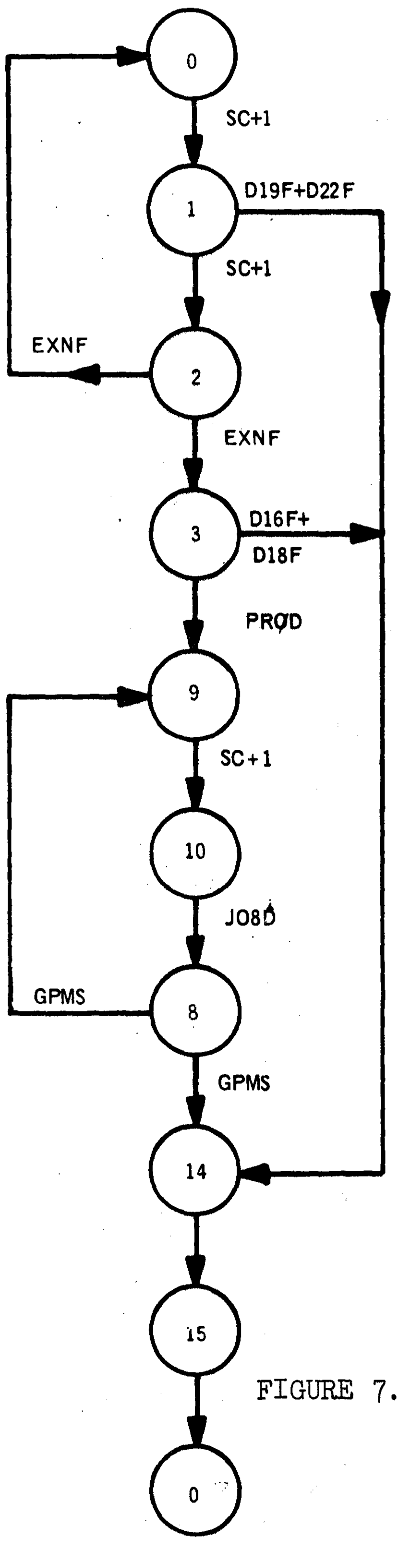
SC=8: Fill "W" Register with Data Word from Keyboard.

SC=9 & 10: Access High Speed Memory Store Data Word 8 characters.

SC=14: Construct Result Descriptor in "W" Register and Descriptor Address in D[15 ⇒ 1].

SC=15: Transfer Result Descriptor to High Speed Memory and Clear I/O Unit.

FIGURE 7.9-1 B 5000 KEYBOARD SEQUENCE COUNT STATE CHART




SC=0, 1 & 2: Operation initiated by AUNS from Central Control. Two Memory Accesses performed.

1. Read Descriptor Address from Memory.

2. Read Descriptor from Memory.

SC=3: Check Peripheral Unit for "READY" and "NOT BUSY".

SC=9 & 10: Access High Speed Memory for Data Word.

SC=8: Printout Data Word on SPO.

SC=14: Construct Result Descriptor in "W" Register and Descriptor Address in D[15 $\Rightarrow$ 1].

SC=15: Transfer Result Descriptor to High Speed Memory and clear I/O Unit.

FIGURE 7.9-2 B 5000 SPO SEQUENCE COUNT STATE CHART

| | |
|---|---|
| D20F | This flip-flop is part of the "D" Register. The state of W20F is never sent to D20F. If a parity error on Keyboard Read occurs, this flip-flop remembers it. It is part of the Result Descriptor. |
| D21F | This flip-flop is part of the "D" Register. The state of W21F is never sent to D21F. It is part of the Result Descriptor. |
| D22F | This flip-flop is part of the "D" Register. The state of W22F is never sent to D22F. If a Memory Overflow or Memory Address Error should occur this flip-flop remembers it. It is part of the Result Descriptor. |
| D24F | This flip-flop is part of the "D" Register. If the Input/Output Descriptor contains a zero in the 24th bit position a Write Operation is indicated, if a one is contained in the 24th bit position a Read Operation is indicated. It is part of the Result Descriptor. |
| D25F | This flip-flop is part of the "D" Register. It is used to indicate if this operation uses the Word Counter portion of the "D" Register. |
| D41F ⇒ D45F | These flip-flops are part of the "D" Register. They are used to designate the peripheral unit that is to be controlled or that is to receive or send information. They are part of the Result Descriptor. |
| DR | The Descriptor Register - Consists of 42 flip-flops numbered D01F ⇒ D22F, D24 ⇒ D27F, and D30F ⇒ D45F. |
| $\overline{\text{DRØS}}$ | Not Drum Operation Switch - Used to gate an action that happens on all operations except Drum operation. |
| DWSD | "D" Register to "W" Register Shift Driver. |
| EXNF | External Control Flip-flop - This flip-flop has many functions. It is used to indicate how many times the actions of SC=2 have been executed during an SPO/Keyboard operation. Allows one group of action to take place on SPO and Keyboard Read operations. |
| FIND | Finished Operation Driver. |
| GPMS | Group Mark Switch - Used to end operation during a Keyboard Read or Supervisory Printout. |
| HØLF | Hold Over Flip-flop - Used to allow only one group of actions to take place per character on SPO or Keyboard Read operations. |
| I01D ⇒ I07D | These are 7 drivers in the Central Control Unit that send across the information bits plus parity to the I/O Unit. |

| | |
|---|---|
| I21D | This driver is located in Central Control and sends the SPO/ Keyboard Ready Level to the I/O Unit. |
| I24D | This driver is located in Central Control and sends the Input Character Ready Level or Output Character Ready Level to the I/O Unit. |
| I21S | This switch is located in the I/O Unit and is used to invert the level received from the driver I21D of Central Control. |
| I24S | This switch is located in the I/O Unit and is used to invert the level received from the driver I24D of Central Control. |
| IB1F ⇒ IBBF | These 6 flip-flops are used to accept information from the Keyboard by way of the Central Control Unit. |
| IB | Input Buffer - Information from the peripheral units is received in this buffer. It is made up of IB1F ⇒ IBPF. |
| ICRL | Input Character Ready Level. |
| IMCF | Initiate Maintenance Cycle Flip-flop. |
| IMCP | Initiate Maintenance Cycle Pulse. |
| I/O #1 ⇒ #4 | Input/Output Control Unit (1 through 4). |
| KEML | Key Memory Level - Used in conjunction with the Memory Cycle switch to key the Core Memory with its own address. |
| KSØD | Keyboard - SPO Operation Driver. |
| MAED-C | Memory Address Error Level - Example: System has only one Memory Module, but D01F ⇒ D15F address a non-existent Memory Module. |
| MANF | Memory Access Needed Flip-flop. |
| MAØF | Memory Access Permitted Level. |
| MCYS | Memory Cycle Level - Used during maintenance when only the logic of sequence counts 9 and 10 is to be executed. |
| MIR | Memory Information Register - Information register in each Memory Module. (48 bits plus parity) |
| MISD | Memory Information Strobe Driver. Used to set information into the I/O "W" Register. |
| MPED-M | Memory Parity Error Level - Level sent to I/O Control from a Memory Module at Memory Cycle time and to indicate a Parity error has occurred in MIR of that Module. |

| | |
|---|---|
| MS10D | Maintenance SC = 10 Driver - Used during normal operation to permit sequence counter jumps from SC = 10, and used during maintenance memory cycles to inhibit sequence counter jumps from SC = 10. |
| MT0D-M | Memory Time Zero Level - Level sent to I/O Control from a Memory Module. Level is true from $t_5$ to $t_0$ of Memory Cycle. |
| MT2D-M | Memory Time Two Level - Level sent to I/O Control from a Memory Module. Level is true from $t_1$ to $t_2$ of Memory Cycle. |
| Ø21D | This driver is located in I/O Control and is used to start the SPO Print Cycle by way of Central Control. |
| Ø22D | This driver is located in I/O Control and is used to signal an SPO or Keyboard-Read Operation. Sent by way of Central Control. |
| ØCRL | Output Character Ready Level. |
| ØDRL | Output Driver Level. |
| PRØD | Proceed Driver - Made up of SC = 3, CC = 5 and D16F <u>on</u> and D18F <u>on</u>. |
| PELS | Parity Error Level Switch. |
| $\overline{\text{PTØS}}$ | Not Printer Operation Level - Used to gate an action that happens on all operations except Printer operation. |
| RECF | Recycle Flip-flop - Used to allow consecutive maintenance cycles of a particular operation to occur. |
| REMF | Remote Flip-flop - On when the I/O Control Unit is in the Remote mode. |
| SC=N | Sequence Counter equal to some value "N" - The Sequence Counter can be equal to any value from 0 - 15. Therefore the Sequence Counter consists of 4 flip-flops. |
| SC+1 | Sequence Counter plus one - Made up as a Driver called S+1D. |
| STRF | Strobe Flip-flop - This flip-flop is used for control purposes in the Input/Output Control Unit. It is turned on once per character on Read, and once per character on Write excluding the first character transfer in SC = 10 time. |
| TINL | Teletype Interrupt Level. |
| TRDL | Teletype Ready Level. |
| TØPL | Teletype Operation Level. |

| | |
|---|---|
| W01F ⇒ W15F | These flip-flops are part of the "W" Register. Usually contain the Core Memory address at the beginning of an operation, and data during an operation. |
| W16F ⇒ W22F | These flip-flops are part of the "W" Register. Their outputs are never sent to the "D" Register. They contain data during an operation. |
| W24F | This flip-flop is part of the "W" Register. Its output is sent to the "D" Register at the beginning of an operation. Determines an Input or Output operation. Contains data during an operation. |
| W27F | This flip-flop is part of the "W" Register and contains data during an operation. |
| W30F | This flip-flop is part of the "W" Register and contains data during an operation. |
| W31F ⇒ W40F | These flip-flops are part of the "W" Register and contain data during an operation. |
| W41F ⇒ W45F | These flip-flops are part of the "W" Register. They contain the unit designation at the beginning of an operation. Contains data during an operation. |
| WR | Word Register - Consists of 48 flip-flops W01F ⇒ W48F. All descriptors and data come from Core Memory and go to Core Memory through this register. |
| W(CC) | Portion of the W Register designated by the state of the CC. |

## 7.10 MAGNETIC TAPE

### PURPOSE

The Magnetic Tape I/O Descriptors allow the B 5000 system to communicate with the B 422 Tape Units.

These Tape Units are capable of reading, writing, backspacing, rewinding and erasing Magnetic Tape under control of the I/O Control Unit.

Writing is done in the forward direction only, using either the Binary or Alphanumeric modes. Tape may be written in Hi Density (555.5 bits per inch) or Lo Density (200 bits per inch). A dual gap head is used which allows reading during writing for checking purposes.

Reading may be performed in either the forward or backward direction.

Basically, there are only two Magnetic Tape operations - Read and Write. Erase and Rewind are available as variants of the Write operation; Space is available as a variant of the Read operation.

There are other minor variants of the Read and Write operations. A list of the 17 separable Magnetic Tape operations follows:

1. Magnetic Tape Read - Forward - Alpha - Word Counter Ending
2. Magnetic Tape Read - Backward - Alpha - Word Counter Ending
3. Magnetic Tape Read - Forward - Alpha - Longitudinal Parity Gap Ending.
4. Magnetic Tape Read - Backward - Alpha - Longitudinal Parity Gap Ending.
5. Magnetic Tape Read - Forward - Binary - Word Counter Ending.
6. Magnetic Tape Read - Backward - Binary - Word Counter Ending.
7. Magnetic Tape Read - Forward - Binary - Longitudinal Parity Gap Ending.
8. Magnetic Tape Read - Backward - Binary - Longitudinal Parity Gap Ending.
9. Magnetic Tape Space.
10. *Magnetic Tape Space Forward Two Records and Mark Inter-Record Gap.
11. *Magnetic Tape Space and Mark Time To Valid Record.

12. Magnetic Tape Rewind

13. Magnetic Tape Write - Alpha

14. Magnetic Tape Write - Binary

15. Magnetic Tape Write - Binary - No Operation

16. Magnetic Tape Erase - Alpha

17. Magnetic Tape Erase - Binary

Figure 7.10-1 shows the I/O descriptor for Magnetic Tape and how the control bits select different Write and Read Variants.

48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

| | | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Unit Designation | Word Counter | U/X | S | C/A | B/F | B/ | WC/GM | */I/O | Result Descrip. Flags | Core Memory Address & Maintenance Counter |

D48 and 47=1 for all I/O Descriptors.

D24=1 for Read; D24=0 for Write.
D25=1 Stop Read with Word Counter; D25=0 Stop at L.P. Gap.
D26=1 Drive Tape Backward; D26=0 Drive Tape Forward.
D27=1 Opr. in Binary Mode; D27=0 Opr. in Alpha Mode.
D30=1 Control Descriptor (no data transfer); D30=0 In/Out Descriptor.

B 5000 I/O MAGNETIC TAPE DESCRIPTORS

| | | D24 | D30 | D27 | D26 | D25 | Word Counter |
|---|---|---|---|---|---|---|---|
| 1. | Mag Tape Read - Forward - Alpha - Word Counter End | 1 | 0 | 0 | 0 | 1 | WC≠0 |
| 2. | Mag Tape Read - Backward - Alpha - Word Counter End | 1 | 0 | 0 | 1 | 1 | WC≠0 |
| 3. | Mag Tape Read - Forward - Alpha - Longitudinal Parity Gap End | 1 | 0 | 0 | 0 | 0 | - |
| 4. | Mag Tape Read - Backward - Alpha - Longitudinal Parity Gap End | 1 | 0 | 0 | 1 | 0 | - |
| 5. | Mag Tape Read - Forward - Binary - Word Counter End | 1 | 0 | 1 | 0 | 1 | WC≠0 |
| 6. | Mag Tape Read - Backward - Binary - Word Counter End | 1 | 0 | 1 | 1 | 1 | WC≠0 |
| 7. | Mag Tape Read - Forward - Binary - Longitudinal Parity Gap End | 1 | 0 | 1 | 0 | 0 | - |
| 8. | Mag Tape Read - Backward - Binary - Longitudinal Parity Gap End | 1 | 0 | 1 | 1 | 0 | - |
| 9. | Mag Tape Space | 1 | 0 | 1/0 | 1/0 | 1 | WC≠0 |
| 10. | *Mag Tape Space Forward 2 Records & Mark Inter Record Gap | 1 | 1 | 0 | 0 | 1 | WC≠0 |
| 11. | *Mag Tape Space & Mark Time to Valid Record | 1 | 1 | 1 | 1/0 | 1 | WC≠0 |
| 12. | Mag Tape Rewind | 0 | 1 | 0 | 1 | 0 | - |
| 13. | Mag Tape Write - Alpha | 0 | 0 | 0 | 0 | 0 | - |
| 14. | Mag Tape Write - Binary | 0 | 0 | 1 | 0 | 1 | WC≠0 |
| 15. | Mag Tape Write - Binary - No Operation | 0 | 1/0 | 1 | 0 | 1 | WC≠0 |
| 16. | Mag Tape Erase - Alpha | 0 | 1 | 0 | 0 | 0 | - |
| 17. | Mag Tape Erase - Binary | 0 | 1 | 1 | 0 | 1 | WC≠0 |

*Special Maintenance Descriptor

**FIGURE 7.10-1 MAGNETIC TAPE DESCRIPTORS**

PROVISIONS

This subsection of the description of Magnetic Tape operations is separated into two groups - Write and Read. The salient provisions of each of these general operations is given.

WRITE (SEE FIGURE 7.10-2)

1. In the alpha mode, the end of a record is indicated by a group mark (01 1111) which is stored in memory. The group mark activates circuitry which establishes a 3/4" inter-record gap but the mark itself is not written on tape.

2. In the binary mode, the end of a record is indicated by the Word Counter being equal to zero. The Word Counter can start out specifying from 1 to 1023 words.

3. An end-of-file indication which consists of approximately 3" of blank tape followed by an end-of-file mark (00 1111) can be written on tape. This is done programatically in the alpha mode on a tape which was written in the binary mode.

4. Information collected in memory for output to tape may contain "unique marks" to fill out the first word to be written on tape. The unique marks are placed in memory during a backward read from tape to fill out the last word read. The "unique mark" (00 1100) results in a blank being written on tape. This may add slightly to the length of the inter-record gap.

5. If memory overflows during a Magnetic Tape Operation the following actions result:

   Alpha - operation terminates after the memory access which causes the overflow.

   Binary - binary zeros are inserted in the record until the Word Counter equals zero.

6. If the D30 bit of the Result Descriptor is on, an erase will be performed. An erase can be performed in the binary or alpha modes.

   Binary - Word counter specifies how many words can be erased.

   1023 words = 15" of high-density tape
   (Maximum)
   42" of low-density tape

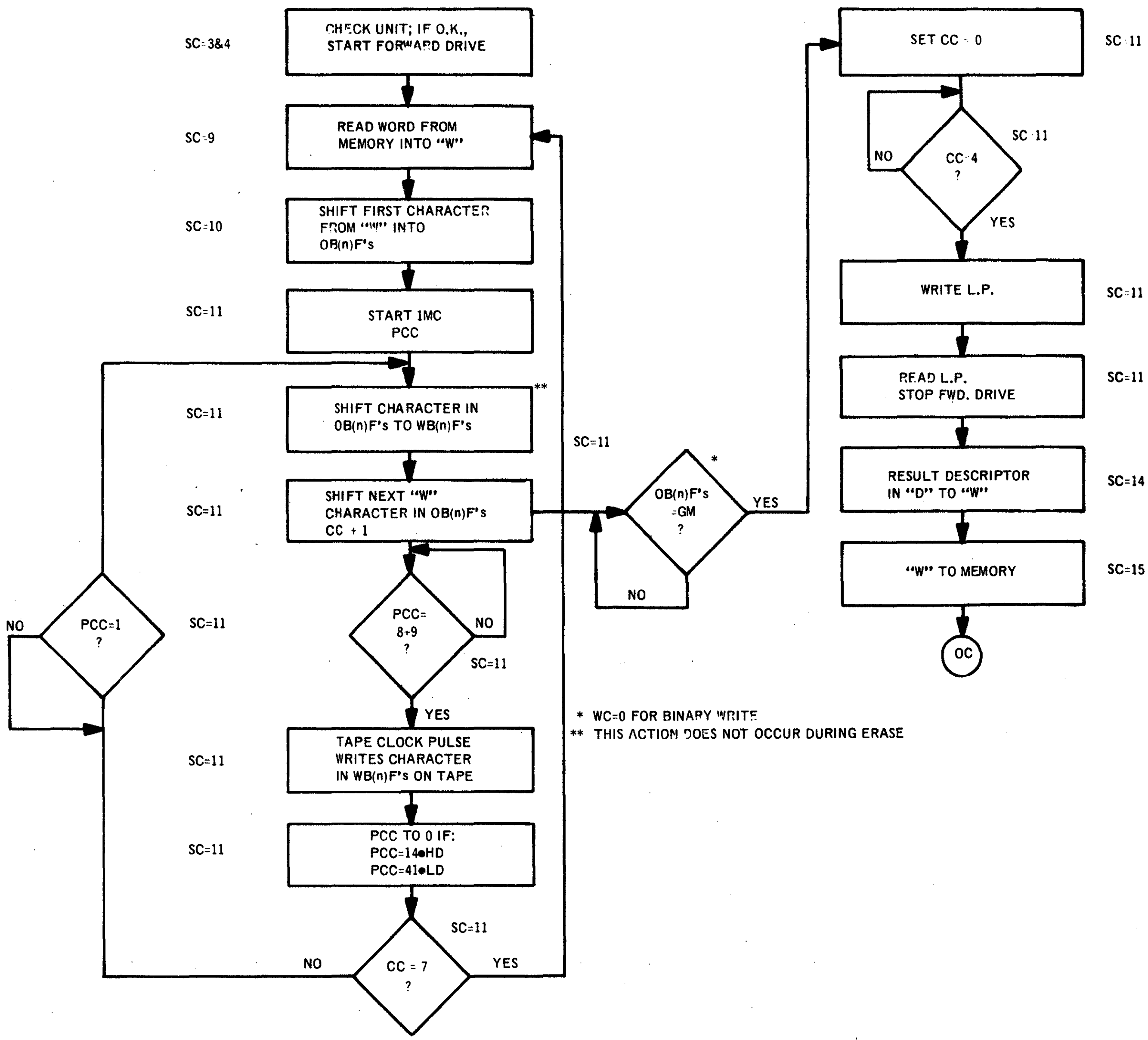



FIGURE 7.10-2 TAPE WRITE OR ERASE ALPHA AND BINARY

Alpha - Tape is erased until a group mark is encountered.

1.2 + NC(.04 for high-density)-inches
NC=No. of characters
1.2 + NC(.01 for low-density)-inches

7. A rewind will be executed if the following bit configurations exist:

   D30=1
   D27=0
   D26=1
   D25=0
   D24=0

8. D20 is turned on to indicate the detection of a parity error during write.

9. At the beginning of an operation, the I/O Control checks to see if the unit is busy. I/O Control allows sufficient time for the unit to get ready if it was busy due to indexing before it definitely assumes that the unit is busy.

READ (SEE FIGURE 7.10-3 AND 7.10-4)

1. Tape records can be read in either the forward or backward directions and in the alpha or binary modes.

2. During forward read, the descriptor describes the low-order memory address of the field into which words from tape will be stored.

3. During backward read, the descriptor describes the high-order memory address of the field in which words from tape will be stored.

4. Eight consecutive characters are accumulated in the "W" register and then sent to memory. This continues until an inter-record gap is encountered. If the Word Counter is being used, memory transfers will cease after the Word Counter has been reduced to zero. The I/O Control, however, remains connected to the Tape Unit until an inter-record gap is encountered.

5. A group mark (01 1111 internal code) is inserted in memory after an inter-record gap is encountered during alpha mode forward read. No group mark is inserted during binary mode or when the Word Counter is used to end alpha read.

6. If during binary or alpha read a record does not constitute an integral number of words, the remaining characters of the last word will be zeros. This is a function of "W" being cleared prior to reading a word.

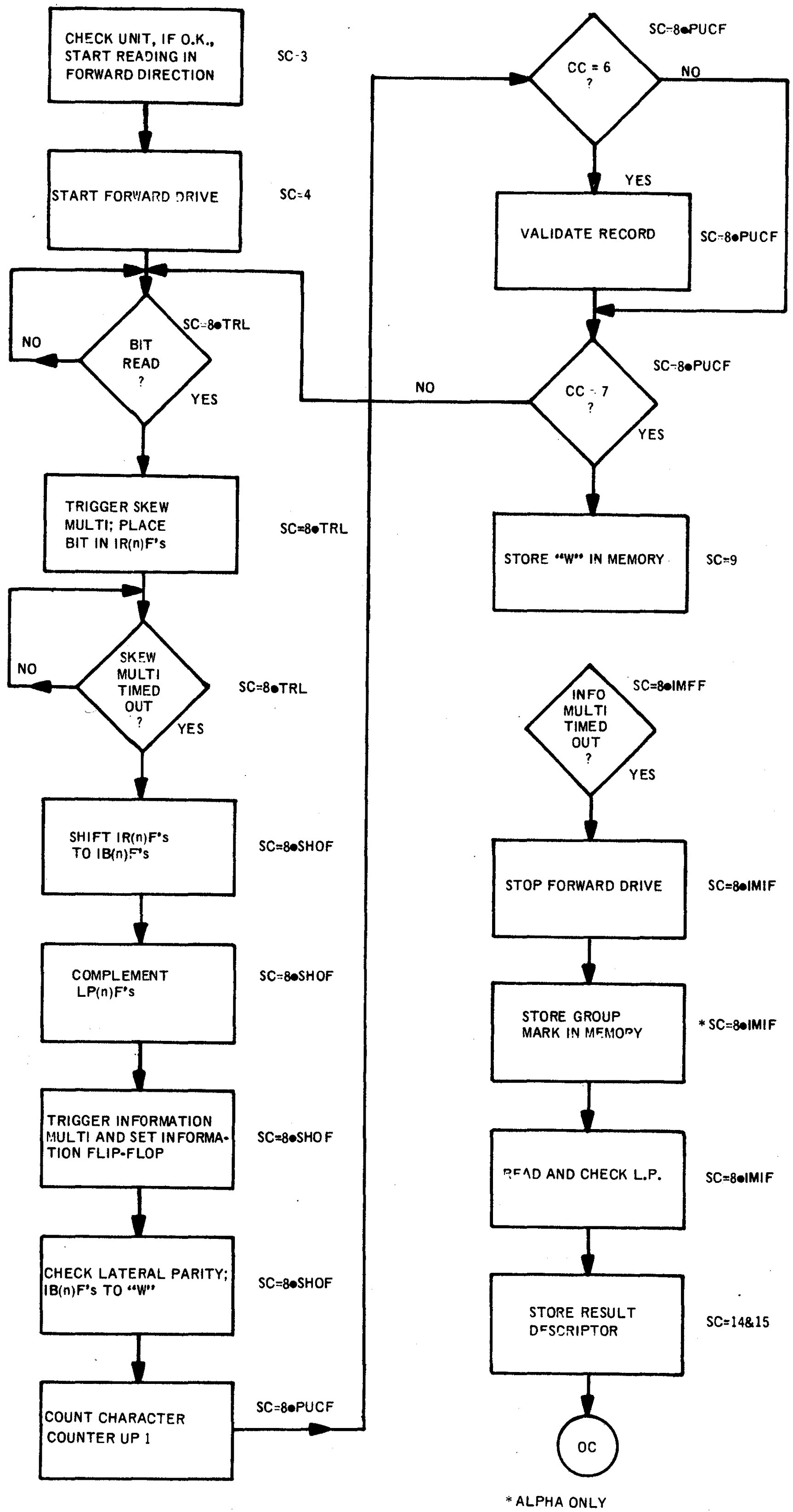



FIGURE 7.10-3 READ FORWARD (ALPHA AND BINARY)

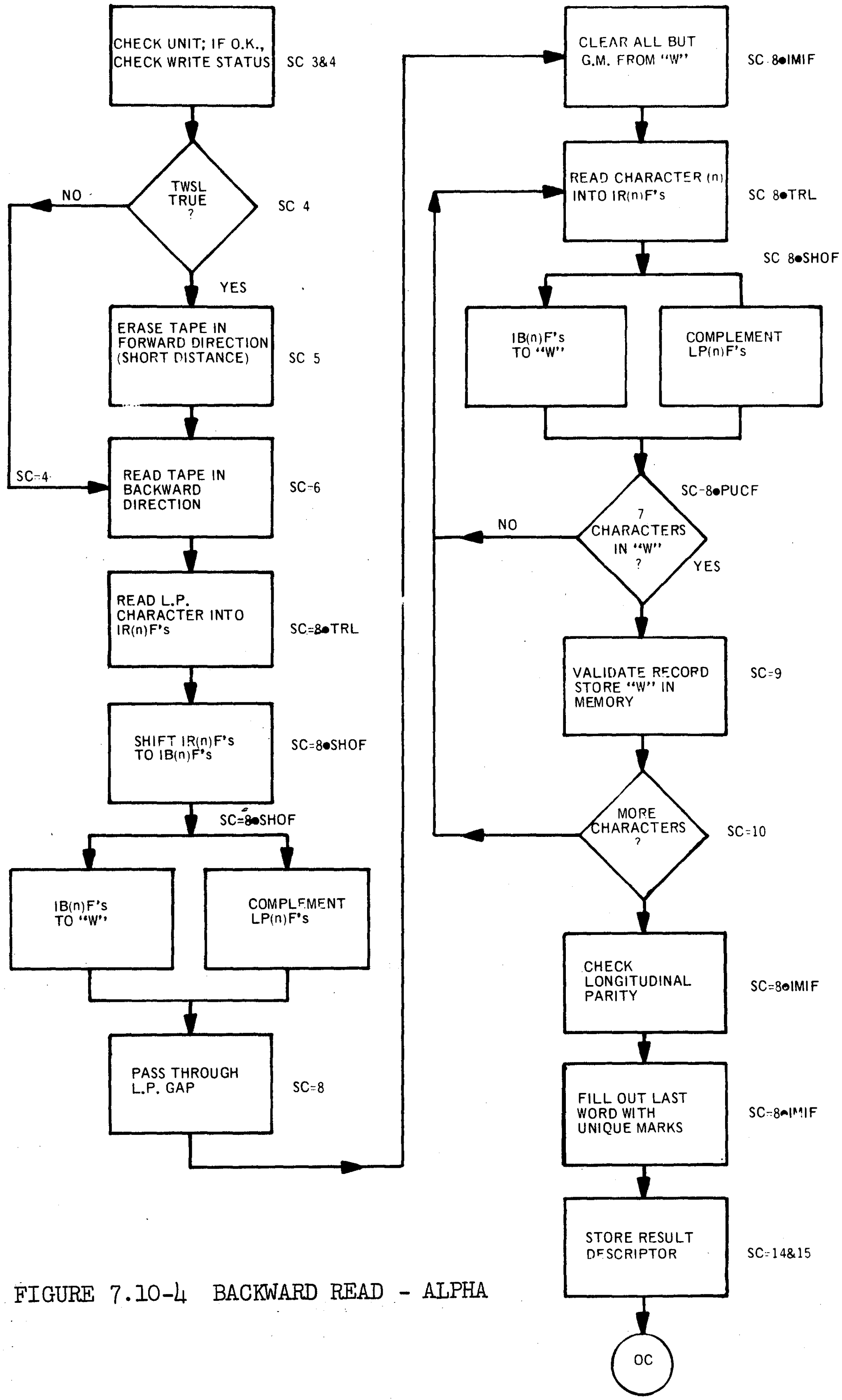



FIGURE 7.10-4 BACKWARD READ - ALPHA

7. There are two basic differences between alpha and binary read:

   a. In binary mode, the BCL to internal code converter is bypassed. In alpha mode, the converter is used.

   b. In binary mode, no group mark is inserted in memory. In alpha mode, a group mark is inserted.

8. If during backward read alpha, a record does not constitute an integral number of words, the remaining characters of the last word are filled out with "unique marks" (00 1100 internal code). These will translate to binary zeros if this information is later written on tape. This permits reading an alphanumeric record while going backwards and then rewriting it going forward in the same manner in which it was read.

9. If a read command overflows memory, the information following the overflow is not written in memory. The overflow is signaled in the Result Descriptor.

10. At the beginning of an operation, the I/O Control checks to see if the unit is busy. I/O Control allows sufficient time for the unit to get ready if it was busy due to indexing before it definitely assumes that the unit is busy.

11. If the Word Counter is at zero and D25 as well as D26 are on, there will be a one record backspace without memory transfers.

12. If the Word Counter is at zero, D25 is on, and D26 is off, there will be a one record forward space without memory transfers.

ERASE (SEE FIGURE 7.10-2)

Erase is identical to a write operation except that no characters are transferred to the output buffer or written on tape.

The amount of tape to be erased is determined by either the number of words specified by the Word Counter during a Binary Erase, or by a group mark in Memory during Alpha Erase.

SPACE (SEE FIGURE 7.10-3 AND 7.10-4

Space is a variant of Read and may be performed either in the forward or backward direction. No information is transferred to Memory.

REWIND

Rewind drives tape backward, at 375" per second, to the beginning of tape. Rewind is an independent tape unit operation once it is initiated.

TAPE SPACE - MARK START TIME AND MARK INTER-RECORD GAP (REFER TO FIGURES 7.10-5 AND 7.10-6

These are two maintenance descriptors to be used by the field engineer to check start time and the length of the inter-record gap.

Both operations make use of the 15 low order bits of the D register as a counter to record start time or inter-record gap distance. These counts are stored in the Result Descriptors and can be examined locally at the I/O Display Panel or programatically printed out on the SPO to determine the results of the test. The following tables give the acceptable times:

MARK START TIME

| ADDRESS COUNTER = START TIME | | |
|---|---|---|
| MIN | NOM | MAX |
| 5000 | 6000 | 7000 |

MARK INTER-RECORD GAP

| ADDRESS COUNTER = GAP DISTANCE | | |
|---|---|---|
| MIN | NOM | MAX |
| 5750 * | 6250 | 7300 |

B 5000 MAGNETIC TAPE GLOSSARY

ADNS-C — Admit Descriptor Level - Comes from the Central Control unit to an I/O unit.

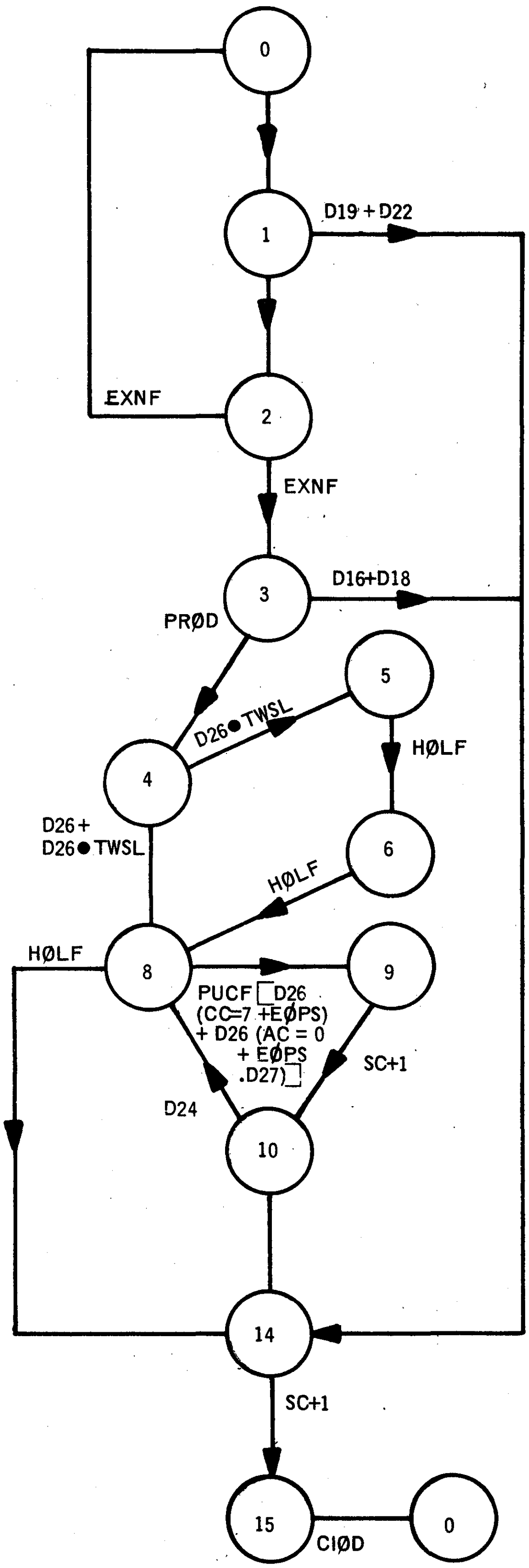
AØFF — Address Overflow Flip-flop - Indicates the flip-flops D01F ⇒ D15F were all equal to one when Memory Cycle took place. Inhibits any further transfer of information to or from Core Memory.

AUNS-C — Admit Unit Level - Comes from Central Control to an I/O unit. Indicates unit is not busy.

BDL — Backward Drive Level - This level is sent to the TTU by Ø23D of the I/O through Central Control and, when positive, causes tape to drive backward providing the TTU is designated and ready.

BF1M — Tape High Density Backward Flaw Multi-Functions to restore the I/O Control Unit read logics after a single flaw has been read from tape. Briefly, if BF1M is allowed to time out while in the longitudinal parity gap a second flux change is simulated which causes IM1F to be set.

BF2M — Tape Low Density Backward Flaw Multi - It is the low-density equivalent of BF1M.




SC=0, 1 & 2: Operation initiated by ADNS signal from Central Control. Two memory accesses are performed:

1. Read descriptor address from cell 8.

2. Read descriptor from memory.

SC=3: Interrogate peripheral unit trunk, designate peripheral unit and interrogate peripheral unit's status (Ready - Busy). Sense for a no operation read command (space). Sense for the mark start time to record command.

SC=4: Allow count of address counter portion of the "D" Register. Start tape motion. If a mark start time forward, start tape forward and sense for the load point marker. If a mark start time backward, start tape backward if the TTU is <u>not</u> in the "Write Status" or forward if the TTU is in the "Write Status". If the "Write Status" fire WGNM.

SC=5: Mark start time backward - write status. Fire brim. Count address counter up. Wait for WGNM to time out. When WGNM times out, stop controlling forward tape drive.

SC=6: Mark start time backward - write status. Fire brim. Wait for delays of the TTU. When delays are over, start tape moving backward.

FIGURE 7.10-5 B 5000 MAGNETIC TAPE (MARK START TIME) SEQUENCE COUNT STATE CHART

FIGURE 7.10-5 (Continued)

SC=8: Count up the address portion of the "D" Register until record read from tape is validated or it is determined an end of file record has been read from tape. Accrue characters read in WR. Perform normal indexing logic. Flag an end of file record.

SC=9: Do not send information read to core memory. Clear WR. Reset CC.

SC=10: Set the sequence counter to 8.

SC=14: Shift Result Descriptor to WR.

SC=15: Access memory to return the Result Descriptor and clear I/O Control.

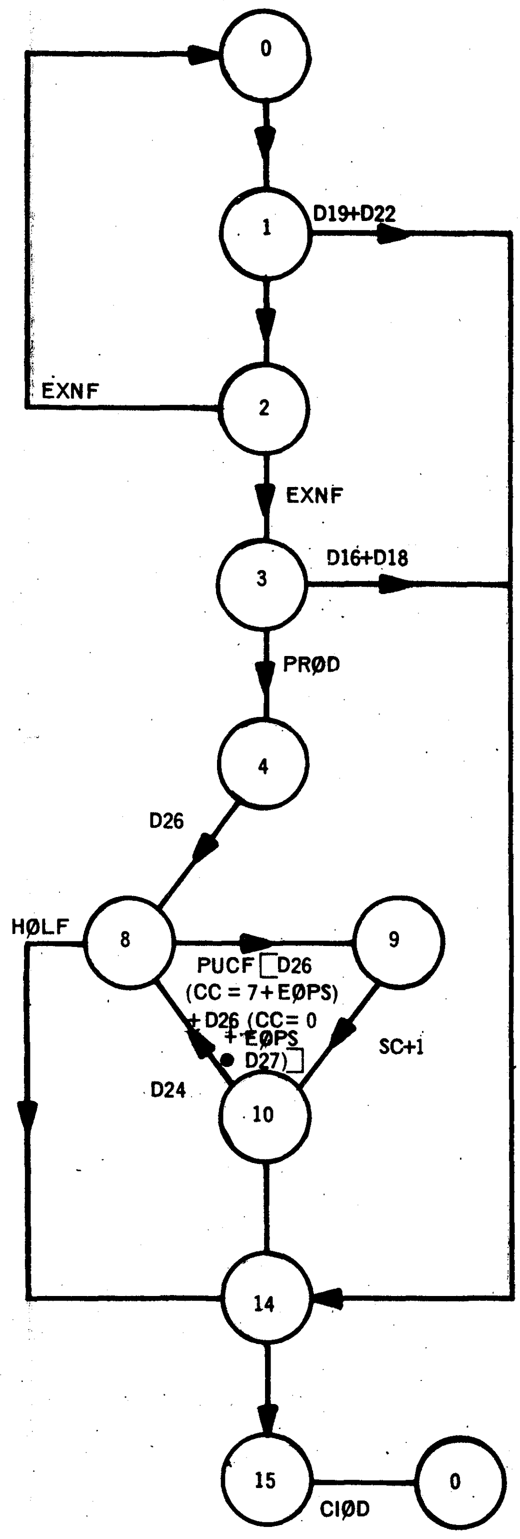



FIGURE 7.10-6
B 5000 MAGNETIC TAPE (MARK INTER-RECORD GAP) SEQUENCE COUNT STATE CHART

SC=0, 1 & 2: Operation initiated by ADNS signal from Central Control. Two memory accesses are performed:

1. Read descriptor address from cell 8.

2. Read descriptor from memory.

SC=3: Interrogate peripheral unit trunk, designate peripheral unit and interrogate peripheral unit's status (Ready - Busy). Sense for a no operation read command (space). Sense for a mark inter-record gap command.

SC=4: Start tape motion in the forward direction. Sense for the load point marker.

SC=8: Read flux changes from tape. Accrue characters read in WR. Validate record being read. If an end of file record was read, flag it. Do not index on the first record read. Allow the address portion of "D" Register to be counted up during the scanning of the inter-record gap that follows the first block scanned. Reset the CC so next record read is validated properly. Allow normal indexing logic to function after first record is scanned. When the second record has been validated or it has been determined to be an end of file record, stop counting address portion of DR.

SC=9: Do not send information read to core memory. Clear WR. Reset CC.

SC=10: Set the sequence counter to 8.

SC=14: Shift Result Descriptor to WR.

SC=15: Access memory to return the Result Descriptor and clear I/O Control.

| | |
|---|---|
| $\overline{\text{BFMS}}$ | Backward Flaw Multi Switch NOT - Its output is true when both BF1M and BF2M are "off." |
| BKWF | Backward Drive Flip-flop - Used to control Backward Tape Drive. |
| BRIM | Backward Read Inhibit Multi - Inhibits the Tape Read level while performing the tape turn around, which results from initiating a Backward Read with the Transport in the Write Status. |
| BTDM | TTU Busy Test Delay Multi - Delays the busy test if the TTU is found initially busy. |
| $\overline{\text{BTDS}}$ | TTU Busy Test Delay Multi Switch NOT - This is a switch whose output reflects the primed state of BTDM. $\overline{\text{BTDS}}$ is true if BTDM is "off." |
| BWIM | Backward Index Multi - This multi provides a time delay for tape drive control. It insures that the TTU will drive tape well into the Inter-Record Gap after reading a block in the backward direction. It also produces the End of Operation level for backward read operation. |
| CC=N, CC≠N | Character Counter is equal to or not equal to some number "N". The Character Counter consists of 3 flip-flops. |
| CC+1 | Character Counter Plus One - In the logic book the driver is C+1D. |
| CDRD-1 | Clear "D" Register Driver No. 1 - This driver clears D01F ⇛ D15F. |
| CIØD | Clear I/O Driver - Clears the I/O Control unit when its output is true. |
| CØBD | Clear O. B. Register. |
| $\overline{\text{CRØS}}$ | Not Card Read Operation. |
| D01F ⇛ D15F | These 15 flip-flops are part of the "D" register. Normally, during an operation they always contain the address of core memory that information is being sent to or taken from. During some operations they are used to measure tape start time and inter-record gaps. |
| D16F | This flip-flop is part of the "D" register. The state of W16F is never sent to D16F, the opposite state of D16F is always sent to W16F. During an operation it is the Not Busy Flip-flop in the I/O unit, at the completion of an operation it is the Busy Flip-flop of the Result Descriptor. |

D17F — This flip-flop is part of the "D" register. The state of W17F is never sent to D17F. This flip-flop has many functions during an operation. It is used to remember that an Admit Descriptor level has been received at the beginning of an operation. It is used to turn MANF on at SC=0 time. If a Descriptor Parity Error should occur it remembers it. It is part of the Result Descriptor. During the magnetic tape operation it is used to indicate the Mark Inter-Record Gap command, or Mark Start Time to Record command is to be executed.

D18F — This flip-flop is part of the "D" register. The state of W18F is never sent to D18F. The opposite state of D18F is always sent to W18F. During an operation it is the Ready Flip-flop in the I/O unit, at the completion of an operation it is the Not Ready Flip-flop of the Result Descriptor.

D19F — This flip-flop is part of the "D" register. The state of W19F is never sent to D19F. If a parity error should occur during the transfer of information from core memory, this flip-flop remembers it. It is part of the Result Descriptor.

D20F — This flip-flop is part of the "D" register. The state of W20F is never sent to D20F. If a Tape Storage unit is in the Write Lockout status when attempting to execute a Write Descriptor, this flip-flop remembers it along with D22F. If a Write Descriptor or Read Descriptor is executed and a lateral parity error or longitudinal parity error is sensed, this flip-flop remembers it. D20F is also used during the Mark Start Time and Mark Inter-Record Gap commands to enable the counting of D01F ⇒ D15F portion of the "D" register. It is part of the Result Descriptor.

D21F — This flip-flop is part of the "D" register. For read it flags an End of File Record; during write it flags the sensing of End of File Reflective strip. It is part of the Result Descriptor.

D22F — This flip-flop is part of the "D" register. The state of W22F is never sent to D22F. If a Memory Overflow or Memory Address Error should occur, this flip-flop remembers it. It is part of the Result Descriptor. For Tape Write, D22F is set in conjunction with D20F when the transport is found in the Write Lockout condition.

D24F — This flip-flop is part of the "D" register. If the Input/Output Descriptor contains a zero in the 24th bit position, a Write Operation is indicated, if a one is contained in the 24th bit position a Read Operation is indicated. It is part of the Result Descriptor.

D25F — This flip-flop is part of the "D" register. It is used to indicate if this operation uses the Word Counter portion of the "D" register.

| | |
|---|---|
| D26F | This flip-flop is part of the "D" register. When this flip-flop is on, tape is to be driven backward during this operation. When this flip-flop is off, tape is to be driven forward during this operation. |
| D27F | This flip-flop is part of the "D" register. If the Input/Output Descriptor contains a zero in the 27th bit position Alpha Mode operation is indicated, if a one is contained in the 27th bit position Binary Mode operation is indicated. It is part of the Result Descriptor. |
| D30F | This flip-flop is part of the "D" register. For Write Descriptors D30 being on causes an Erase Operation; for Read Descriptors D30 activates the Maintenance Logic. |
| D31F ⇒ D40F | These flip-flops are part of the "D" register. They make up the Word Counter for all operations. |
| D41F ⇒ D45F | These flip-flops are part of the "D" register. They are used to designate the peripheral unit that is to be controlled or that is to receive or send information. They are part of the Result Descriptor. |
| DERS | "D" Register Error Level - If an error should occur during an operation this level will be true. The level is used in Central Control during a Load operation only. |
| DR | The Descriptor Register - Consists of 42 flip-flops numbered D01F ⇒ D22F, D24F ⇒ D27F, and D30F ⇒ D45F. |
| $\overline{\text{DRØS}}$ | Not Drum Operation Switch - Used to gate an action that happens on all operations except Drum operation. |
| DS1M | Digit Skew Multi High Density. |
| DS2M | Digit Skew Multi Low Density. |
| $\overline{\text{DS1S}}$ | Is a switch whose output reflects the primed state of the High Density Digit Skew Multi (DS1M). |
| $\overline{\text{DS2S}}$ | Is a switch whose output reflects the primed state of the Low Density Digit Skew Multi (DS1M). |
| DSI | Delay Standard Index - Multi located in TTU that delays the stopping of tape drive in the forward direction. Tape will continue to drive forward after the FWDF Flip-flop is turned off in the I/O. |
| DWSD | "D" register to "W" register Shift Driver. |

| | |
|---|---|
| EØFL | End of File Level - This level is produced by sensing the output of the Input Buffer. IB[8 ⇛ 1] all equal to one and IB[B ⇛ A] both equal zero. |
| EØFS | Tape End of File Switch - The output of this switch is true when an End of File Marker is read from tape and the Character Counter and VRCF verify that only one flux change has been read in the forward or backward direction. |
| EØPS | End of Operation Switch - Its output is true when the end of the tape record has been sensed. EØPS indicates that either LP1M, LP2M or BWIM are on. |
| EXNF | External Control Flip-flop - This flip-flop has many functions. It is used to indicate how many times the actions of SC=2 have been executed. During the Magnetic Tape operation it is used to activate the pulse counter and interlock indexing logic while the I/O unit is transferring information to the transport. |
| FDL | Forward Drive Level - This level is sent to the TTU by Ø22D of the I/O through Central Control, and when positive causes tape to drive forward providing the TTU is designated and ready. |
| FIND | Finished Operation Driver. |
| FWDF | Forward Drive Flip-flop - Used to control forward tape drive. |
| GPMS | Group Marker Switch - The output of this switch will come true when OB[B ⇛ 1] all equal one during a write operation. |
| HOLF | Hold Over Flip-flop - Used in conjunction with STRF to synch various multi functions with the one megacycle clock. |
| I31D | This driver is located in Central Control and sends the Tape Transport Operate level to the I/O unit. |
| I32D | This driver is located in Central Control and sends the Tape Read Ready level to the I/O unit. |
| I34D | This driver is located in Central Control and sends the Tape Load Point level to the I/O unit. |
| I35D | This driver is located in Central Control and sends the Tape Write Ready level to the I/O unit. |
| I36D | This driver is located in Central Control and sends the Tape Write Status level to the I/O unit. |
| I37D | This driver is located in Central Control and sends the Tape High Density level to the I/O unit. |

| | |
|---|---|
| I38D | This driver is located in Central Control and sends the Tape End of File level to the I/O unit. |
| I21S | This switch is located in the I/O unit and is used to invert the level received from the driver I31D of Central Control. |
| I22S | This switch is located in the I/O unit and is used to invert the level received from the driver I32D of Central Control. |
| I24S | This switch is located in the I/O unit and is used to invert the level received from the driver I34D of Central Control. |
| I25S | This switch is located in the I/O unit and is used to invert the level received from I35D of Central Control. |
| I26S | This switch is located in the I/O unit and is used to invert the level received from I36D of Central Control. |
| I27S | This switch is located in the I/O unit and is used to invert the level received from the driver I37D of Central Control. |
| IB | Input Buffer - Information from the IR Buffer is transferred to this buffer. It is made up of IB1F ⇒ IBPF. |
| $\overline{\text{IIMS}}$ | Information Multi Switch NOT - Its output is true when both IM1M and IM2M are "off". |
| IM1M | Tape High Density Information Multi - It is set to "one" by the first flux change of the record and held over by subsequent flux changes if they occur at 67 KC. IM1M is activated during the high density mode only. |
| IM2M | Tape Low Density Information Multi - It is set to "one" by the first flux change of a record and held over by subsequent flux changes if they occur at 24 KC. IM2M is activated during the low density mode only. |
| IMCF | Initiate Maintenance Cycle Flip-flop. |
| IMCP | Initiate Maintenance Cycle Pulse. |
| IMFF | Information Flip-flop - It remembers that one of the Information Multis (IM1M or IM2M) had been set. |
| IMIF | Information Index Flip-flop - Used in conjunction with IMFF to synch the indexing logic with the one megacycle clock. |

| | |
|---|---|
| InnP | The InnP lines originate in Central Control and are used to transmit the Tape Read Pulses to the Input/Output Control. The Tape Read Pulses are reshaped to .5 μs pulses in Central Control. |
| I/Ø No. 1 | Input/Output Control Unit number one. |
| I/Ø No. 2 | Input/Output Control Unit number two. |
| I/Ø No. 3 | Input/Output Control Unit number three. |
| I/Ø No. 4 | Input/Output Control Unit number four. |
| IR | Tape Information Read Buffer - Information from the Tape Transport units is received in this buffer. It is made up of IR1F ⇛ IRPF. |
| JnnD | Jump to some number nn (0 ⇛ 15) Driver - Used to set the Sequence Counter to a state 0 ⇛ 15. |
| KEML | Key Memory Level - Used in conjunction with the Memory Cycle switch to key the core memory with its own address. |
| LCHF | Last Character Flip-flop - This flip-flop, along with LPWF, remembers that the last characters of a record are about to be written on tape. LCHF and LPWF on, along with the CC4F on and the Pulse Counter equal to zero or one, form the gate to produce the Tape Write Reset Pulse. |
| LP1M | Tape High Density Longitudinal Parity Multi - Used to delay the testing of Longitudinal Parity Character and to generate the End of Operation level. While LP1M is on the Longitudinal Parity Character is read from tape. |
| LP2M | Tape Low Density Longitudinal Parity Multi - It is the low density equivalent to LP1M. |
| LPIM | Load Point Inhibit Multi - This multi inhibits the Tape Read Level while traversing the gap between the Load Point Reflective Strip and the first record on tape. |
| LPnF | Longitudinal Parity 1 ⇛ P Flip-flops - Used during the tape operations to accumulate longitudinal parity. |
| LPWF | Longitudinal Parity Write Flip-flop - This flip-flop along with LCHF remembers that the last characters of a record are about to be written on tape. LCHF and LPWF on, along with the CC4F on and the Pulse Counter equal to zero or one, form the gate to produce the Tape Write Reset Pulse. |
| MAED-C | Memory Address Error Level - Indicates module selected by D13F ⇛ D15F is not available. |

| | |
|---|---|
| MAND | The output of the Memory Access Needed Driver is sent to the Memory Module designated by D13F ⇒ D15F. This output will only be true if the Memory Access Permitted level in the I/O unit is true. |
| MANF | Memory access Needed Flip-flop. |
| MAØF | Memory Access Obtained Flip-flop. |
| MAPS | Memory Access Permitted Level. |
| MCYS | Memory Cycle Level. Used during maintenance when only the logic of sequence counts 9 and 10 is to be executed. |
| MIR | Memory Information Register - Information register in each Memory Module (48 bits plus parity). |
| MISD | Memory Information Strobe Driver. Used to set information into the "W" register. |
| MPED-M | Memory Parity Error Level - Level sent to Input/Output Control from a Memory Module at Memory Cycle time 4 to indicate a parity error has occurred in MIR of that Module. |
| MRD | Multi Read Disable - Multi located in the TTU that delays reading from tape after stopping forward tape drive and starting backward tape drive. This condition would occur when trying to initiate a Backward Read operation when the TTU was in the Write Status. |
| MTOD-M | Memory Time Zero Level - Level sent to Input/Output Control from a Memory Module. Level is true from $t_5$ to $t_0$ of Memory Cycle. |
| MT2D-M | Memory Time Two Level - Level sent to Input/Output Control from a Memory Module. Level is true from $t_1$ to $t_2$ of Memory Cycle. |
| MWRD | Memory Write Driver - Located in Input/Output Control. Used to indicate to the Memory Module a Memory Write Cycle is desired during this part of the operation. |
| ØB | Output Buffer - Consists of six flip-flops and a parity generator. Its output gates the Write Buffer. |
| ØBCF | Output Buffer Call Flip-flop - When set to "one," signifies that new information is to be shifted to ØB. |
| Ø21D | This Driver is located in I/O Control and is used to send the Tape Clock Pulse to the TTU by way of Central Control. |

| | |
|---|---|
| Ø22D | This Driver is located in I/O Control and is used to send the Forward Drive Level to the TTU by way of Central Control. |
| Ø23D | This Driver is located in I/O Control and is used to send the Backward Drive level to the TTU by way of Central Control. |
| Ø24D | This Driver is located in Input/Output Control and is used to send the Tape Write level to the TTU by way of Central Control. |
| Ø25D | This Driver is located in Input/Output Control and is used to send the Tape Rewind level to the TTU by way of Central Control. |
| Ø26D | This Driver is located in Input/Output Control and is used to send the Tape Read level to the TTU by way of Central Control. |
| Ø27D | This Driver is located in I/O Control and is used to send the Tape Write Reset Pulse to the TTU by way of Central Control. |
| PC | Pulse Counter - The Pulse Counter counts at a one megacycle rate and is used to divide down the 1 MC clock to some predetermined rate. |
| PC=14/41 | Pulse Counter Equal Fourteen - The PC is recycled at 14 time or 41 time during a Magnetic Tape operation, thus providing a 66 KC or 24 KC recycle rate. |
| PELS | Parity Error Level Switch - Its output is true when the information in IB violates parity. |
| PRØD | Proceed Driver - Its output is true to signify that the peripheral unit was ready and not busy. |
| PSØS | Pulse Counter Set to Zero Switch. |
| $\overline{\text{PTØS}}$ | Not Printer Operation Level - Used to gate an action that happens on all operations except Printer operation. |
| PUCF | Pile Up Control Flip-flop - When on, signifies that the IB Buffer contains a character which is to be shifted to the "W" register. |
| RCNF | Record Control Flip-flop - When on, signifies that the body of a record is being read from tape. |
| RECF | Recycle Flip-flop - Used to allow consecutive maintenance cycles of a particular operation to occur. |

REMF — Remote Flip-flop - On when the I/O Control unit is in the remote mode.

$\overline{\text{RIMS}}$ — Read Inhibit Multi Switch NOT - Its output is true when both LPIM and BRIM have timed out.

SC=N — Sequence Counter equal to some value "N" - The Sequence Counter can be equal to any value from 0 - 15. Therefore, the Sequence Counter consists of 4 flip-flops.

SC+1 — Sequence Counter Plus One - Made up as a Driver called S+1D.

SHØF — Skew Holdover Flip-flop - Used in conjunction with SKFF to synch the input clocking logic with the one megacycle clock.

SKFF — Skew Flip-flop - Serves as a storage element to signify the setting of one of the Digit Skew Multis.

STRF — Strobe Flip-flop - This flip-flop is used for control purposes in the I/O Control unit. It is turned on when it is necessary to synch in on the one megacycle clock.

TAØD — Tape Operation Driver.

TCP — Tape Clock Pulse - This pulse is sent to the TTU by Ø21D of the I/O through Central Control, and when positive causes a flux change to be written on the tape. What is written on tape is controlled by the levels coming to the TTU from the outputs of the Write Buffer of the I/O.

TEFL — Tape End of File Level - This level comes from the TTU via I38D of Central Control, and when positive indicates the tape has been driven forward onto the end of file marker. TEFL remains positive until tape is driven backward off the end of file marker.

THDL — Tape High Density Level - This level comes from the TTU via I37D of Central Control and when positive indicates the High Density Switch is in the High Density position.

TLPL — Tape Load Point Level - This level comes from the TTU via I34D of Central Control, and when positive indicates the load point marker has been sensed while moving tape in reverse direction. Remains positive until tape is driven forward off the load point marker.

TREL — Tape Read Ready Level - This level comes from the Tape Transport via I32D of Central Control, and when positive indicates the unit is designated but not rewinding, and the Restart Delay Multi is not on.

| | |
|---|---|
| TRL | Tape Read Level - This level is sent to the TTU by Ø26D of the I/O through Central Control, and when positive activates the TTU's read circuitry. |
| TRP-n | Tape Read Pulses [B ⇒ 1] and Parity Bit - These pulses come to the I/O from the Central Control as I11P ⇒ I17P. The 2 μs wide pulses are reshaped to less than .5 μs wide. |
| TRWL | Tape Rewind Level - This level is sent to the TTU by Ø25D of the I/O through Central Control, and when positive indicates to the TTU to rewind tape. |
| TTØL | Tape Transport Operate Level - This level comes from the Tape Transport via I31D of Central Control, and when positive indicates the Transport is ready to operate or be designated. |
| TWCD | Transfer From W Clocked Driver - Used to shift information a character at a time from the "W" register to the Output Buffer (ØB[B ⇒ 1]) clocked. |
| TWFD | Tape Write Forward Driver - Used in the I/O Control unit at SC=4. |
| TWI-n | Tape Write Information Levels [B ⇒ 1] and Parity Level - These levels are sent to the TTU through Central Control. When positive, a flux change is written on tape when the TCP level goes positive. |
| TWL | Tape Write Level - This level is sent to the TTU by Ø24D of the I/O through Central Control, and when positive places the TTU in the Write Status. TWL sets the Write Status Flip-flop in the TTU if the TTU is write ready and designated. |
| TWRL | Tape Write Ready Level - This level comes from the TTU via I35D of Central Control, and when positive indicates the file protection ring is on the Tape Reel and TREL is positive. |
| TWRP | Tape Write Reset Pulse - This pulse is sent to the TTU by Ø27D of the I/O through Central Control, and when positive is used to reset the write flip-flops. The resetting of the write flip-flops causes the writing of the longitudinal parity character. |
| TWSL | Tape Write Status Level - This level comes from the TTU via I36D of Central Control, and when positive indicates the TTU is in the Write Status. |
| VRCF | Valid Record Flip-flop - It is set to the one state after seven characters have been read from tape. |
| W01F ⇒ W15F | These flip-flops are part of the "W" register. Usually contain the Core Memory address at the beginning of an operation, and data during an operation. |

| | |
|---|---|
| W16F ⇒ W22F | These flip-flops are part of the "W" register. Their outputs are never sent to the "D" register. They contain data during an operation. |
| W24F | This flip-flop is part of the "W" register. Its output is sent to the "D" register at the beginning of an operation. Determines an input or output operation. Contains data during an operation. |
| W27F | This flip-flop is part of the "W" register. Its output is sent to the "D" register at the beginning of an operation. Determines Alpha or Binary Mode operation. Contains data during an operation. |
| W30F | This flip-flop is part of the "W" register. Its output is sent to the "D" register at the beginning of an operation. Contains data during an operation. |
| W31F ⇒ W40F | These flip-flops are part of the "W" register. They contain the number of words per operation at the beginning of an operation. Contain data during an operation. |
| W41F ⇒ W45F | These flip-flops are part of the "W" register. They contain the unit designation at the beginning of an operation. Contain data during an operation. |
| WB | Tape Write Buffer - This buffer consists of 7 flip-flops and is used to reflect the state of the Output Character to the TTU. |
| WC=N | Word Counter equal to some value "N" - The Word Counter can be equal to any value from 0 to 1023. |
| WC | Word Counter - It is made up of flip-flops D31F ⇒ D40F. In order to use this counter during an operation, D25F must be on. |
| W[CC] | Portion of the "W" register designated by the state of the CC. |
| WGBM | Write Gap Beginning of Tape Multi - Used to provide a time delay between drive activation, while at Load Point of tape (TLPL=1), and the beginning of information transfer. WGBM will provide a gap of approximately 8" between the Load Point Marker and the beginning of the first record. |
| $\overline{\text{WGMS}}$ | Write Gap Multi Switch NOT - Its output is true when both of the Write Gap Multis are off. |

| | |
|---|---|
| WGNM | Write Gap Normal Multi - Used to provide a time delay between drive activation and the beginning of information transfer. The time delay is established so as to provide a 3/4" gap between successive records. |
| WR | Word Register - Consists of 48 flip-flops, W01F $\Rightarrow$ W48F. All descriptors and data come from Core Memory and go to Core Memory through this register. |

## 7.11 DISK FILE READ AND WRITE

### PURPOSE

To provide the system with a very large capacity storage device with rapid access to any information when required. System configuration allows for either one or two Disk File Control Units. Two units can control four hundred disks, which have a maximum storage capacity of 960 million characters.

### SUMMARY OF OPERATION

Upon initiating a Disk File operation, an I/O Descriptor will be transferred to the I/O from Core Memory. This descriptor will determine whether this is a read or a write command. The format of this descriptor is as follows.

| | |
|---|---|
| D48 | = always on for descriptor |
| D47 | = always off for descriptor |
| D46 | = presence bit |
| D45 thru D41 | = unit designate (6 or 12) |
| D40 thru D31 | = word counter |
| D30 | = 1 for read check (inhibit data transfer) |
| D27 | = 0 for alphanumeric<br>1 for binary |
| D25 | = 1 word counter override (use word counter) |
| D24 | = 0 for disk file write<br>1 for disk file read |
| D21 thru D16 | = number of segments |
| D15 thru D1 | = core memory address (NOTE; last seven (7) characters of first word contain Disk File Address) |

### READ

Information from the Disk File may be either BCL or Binary, as specified by D27 in the I/O Descriptor. Reading is modular by segments, with segment size established by D21 through D16. A single descriptor can control reading from one to sixty-three segments. Segment count is kept by the Disk File Control Unit, and the operation is terminated when the segment count is satisfied. Word count override can also be specified with a range of one to ten-hundred and twenty-three words available. If this option is utilized, then the operation is terminated when the word count is satisfied. If word counter override is not used, then the operation would be terminated when the segment size specified in the I/O Descriptor is reduced to zero.

WRITE

As in a read operation, data transfer may be either BCL or Binary. To initiate a Disk File write operation, D24 in the I/O Descriptor would be zero. D21 through D16 (segment size), D40 through D31 (word count) and D25 (word counter override) notify the Disk File Control Unit the number of words to be written and the required segment size. The option of writing by only segment and not word count, is specified by D25. Termination of the operation is determined by either reducing the segment size or the word count to zero. Word count takes precedence if word counter override is used.

If a write operation is terminated by word count override, any remaining part of the segment and any remaining segments are filled in with blanks for write operation with BCL translation, or with zeros for write operation without translation.

If a locked-out disk is addressed any time during a write operation or if a parity error is detected on any descriptor or address transfer, the operation is terminated and noted by the setting of D20 in the result descriptor.

RESULT DESCRIPTOR

During a write operation, the I/O is connected for the entire operation. I/O Finished is produced when the I/O is released by the Disk File Control Unit and the Result Descriptor has been stored. On a read operation, word count override can release the I/O before the Disk File Control Unit has terminated its operation. The format of the Result Descriptor is as follows.

| | |
|---|---|
| D40 thru D31 | = remaining word count |
| D24 | = 0 if operation was write<br>1 if operation was read |
| D23 | = read check error on prior operation |
| D22 | = core memory address error |
| D21 | = Disk File Electronics Unit not ready, or an attempt to access non-existent disk address |
| D20 | = parity error on transfer of data from disk to I/O or attempt to address a locked out disk address |
| D19 | = parity error, memory to I/O or I/O to Disk File Control |
| D18 | = not ready, Disk File Control Unit only |
| D17 | = busy, Disk File Control Unit only |
| D15 thru D1 | = last address accessed +1 for all read/write operations or initial address +1 for read check and interrogate operations |

READ CHECK

For the Read Check Descriptors, the I/O transfers the address word and segment count to the Disk File Control Unit, initiates a Read Check operation in that unit, and returns a result descriptor. The Read Check operation continues independently of the I/O. Termination of a Read Check operation is indicated by setting CC115F for Disk File 1, and CC116F for Disk File 2.

INTERROGATE

An Interrogate operation results in neither reading nor writing on a disk. The I/O transfers an address word and this is followed by construction of a result descriptor with indications for non-existent address, Electronics Unit not ready, Disk locked out, or Read Check error.

PRINCIPLES OF OPERATION AND GLOSSARY

Refer to Field Engineering Technical Manual B 470.51, Disk File Control.

## 7.12 DATA COMMUNICATIONS

PURPOSE

Data Communication provides the system with a device for transferring data, in either direction, from remote located stations. Communication between the system and the remote station may be through the B 481 Teletype (TTY), the B 483 Typewriter (TYP) or the B 484 Typewriter with Exchange (TWX).

SUMMARY OF OPERATION

An input operation is initiated when a Terminal Unit has received a complete message from a station. This condition places the Terminal Unit in the "input ready" state. The Data Communication Control Unit (DCCU) will scan the Terminal Units searching for a unit that requires attention. When addressing a unit that is "input ready", the DCCU will then cease its scanning and lock in on the unit. Providing no other terminals are "output ready", (output having priority over input), the DCCU enables logic for setting CCI13F (Data Communication Interrupt) in Central Control. Under program control, an I/O read descriptor is constructed and transferred to the I/O, indicating that it is ready to receive the input message.

The format of an I/O descriptor for Data Communication is as follows:

| | |
|---|---|
| D48 | = always on for descriptor |
| D47 | = always off for descriptor |
| D46 | = presence bit |
| D45 thru D41 | = unit designate (16) |
| D40 thru D25 | = not used |
| D24 | = 1 for read<br>0 for write |
| D23 thru D20 | = not used |
| D19 thru D16 | = for read operation<br>(a) if field is zero, read T.U. selected by DCCU<br>(b) if field is not zero, read T.U. as designated (1 thru 15)<br>for write operation<br>(a) field will not be zero, write T.U. as designated (1 thru 15) |
| D15 thru D1 | = initial memory address |

An input operation is terminated by a group mark in the data stream. The group mark is stored in memory and any remaining characters in the final word are filled out with blanks. The sensing of the group mark by the I/O at SC=8 sets D17F. Control is then transferred to SC=14 where the result descriptor is constructed.

The format of a Data Communication result descriptor is as follows:

| | |
|---|---|
| D38 thru D35 | = address of terminal unit involved in operation |
| D34 thru D24 | = not used |
| D23 | = 1 terminal unit buffer filled before group mark occurred during write<br>0 for read |
| D22 | = core memory address error during write |
| D21 | = terminal unit ready (input or output) |
| D20 | = terminal unit busy |
| D19 | = parity error, memory to I/O |
| D18 | = DCCU or T.U. not ready |
| D17 | = descriptor error |
| D16 | = DCCU busy |
| D15 thru D1 | = last address accessed +1 |

With the complete input message received, the Processor then assembles the reply message and initiates an output operation. A Data Communication descriptor, stored in memory, is transferred to the I/O. The Terminal Unit designate is passed to the DCCU to latch in the specified unit. The system reply will be addressed to the unit that originated the input request. Once the Terminal Unit is latched in, the I/O is notified and commences the transfer of the reply message. The operation is terminated by either a group mark or, in the case of a multiple output, a signal from the DCCU indicating that the Terminal Unit buffer is full.

In the case of a multiple output, the I/O is unlatched on the full buffer indication. A result descriptor is constructed and the multiple output condition noted by the setting of D23. While the Terminal Unit is unloading its buffer to its station, the DCCU will commence scanning for other units that require attention. When the unit involved in the multiple output operation is addressed by the DCCU and found to be "output ready", CCI13F is set in Central Control. The I/O is again latched up and the next segment of the reply message is transferred through to the Terminal Unit. This sequence of operation will continue until the I/O detects a group mark to signify the message is complete.

Only during a Teletype operation will the system program independently initiate an output operation. An I/O descriptor is transferred from memory to the I/O. If the DCCU is not busy, the scanner is set to the Terminal Unit specified by the descriptor (D45 through D41). The I/O is latched up and the transmission of data commenced. Termination will be by the detection of a group mark in the I/O. Should the designated Terminal Unit be not ready, busy or input ready, the operation is terminated and indicated in the result descriptor.

PRINCIPLES OF OPERATION AND GLOSSARY

Refer to Field Engineering Technical Manual B480.51, Data Communication Control Unit.

## 7.13 DATA TRANSMISSION

### PURPOSE

Data Transmission provides the System with a method of transferring data, either to or from certain remote devices. Transmission between the remote devices and the System may be through a B249 (Data Transmission Control Unit), a B487 (Data Transmission Terminal Unit) and an appropriate Adapter. The Adapter in turn is connected either directly or via a telephone data set to the remote device. For further information regarding Data Transmission equipment, refer to the B249 and B487 Technical Manuals.

### SUMMARY OF OPERATION

Data Transmission operation is initiated in the I/O when the MCP detects a Data Communications Interrupt (CCI13F). The System then responds with a Passive Interrogate operation to determine what Terminal Unit and what Buffer caused the Interrupt. The Result Descriptor will also contain the status of the Buffer. After examining the Result Descriptor, the System can determine subsequent operations from the status field.

The format of an I/O descriptor for Data Transmission is as follows:

| | |
| --- | --- |
| D48 | = 1 |
| D47 | = 0 |
| D46 | = Presence Bit |
| D45 thru D41 | = Unit Designate (16) |
| D40 | = 0 |
| D39 thru D36 | = Terminal Unit Number (1 → 15) |
| D35 | = Terminate buffer load or unload when GM (←) is detected or buffer is full |
| D34 thru D31 | = Buffer Number |
| D30 | = 1 Interrogate (D24 must be 0) |
| | = 0 Read or Write |
| D29, D28 | = Not Used |
| D27 | = 0 Use BCL to Internal Code Translator |
| | = 1 Bypass Translator |
| D26,D25 | = Not Used |
| D24 | = 0 Write or Interrogate |
| | = 1 Read |
| D23 thru D16 | = Not Used |
| D15 thru D1 | = Core Memory Address |

An output operation is terminated in the I/O at SC = 8 when GPMS is TRUE which will cause D17 to be set. With D17 on, the sequence proceeds to SC = 14 to generate the Result Descriptor.

An input operation is terminated in the I/O at SC = 10, during the completion of the Memory Write Cycle. As in an output operation, GPMS being TRUE will cause the sequence to proceed to SC = 14 to generate the Result Descriptor.

The format of the I/O Result Descriptor for Data Transmission is as follows:

| | |
|---|---|
| D48 thru D46 | = 0 |
| D45 thru D41 | = Unit Designate (16) |
| D40 | = 0 DTC Used |
| | = 1 DTC Not Used |
| D39 thru D36 | = Terminal Unit Number |
| D35 | = 0 DCC Translator Used |
| | = 1 DCC Translator Not Used |
| D34 thru D31 | = Buffer number |
| D30 | = 0 Read or Write operation |
| | = 1 Interrogate operation |
| D29,D28 | = Not Used |
| D27 | = 0 BCL to Internal Code Translator used |
| | = 1 BCL to Internal Code Translator not used. |
| D26 | = Not Used |
| D25 | = 1 Adapter sensed Abnormal condition |
| D24 | = 0 Write operation |
| | = 1 Read operation |
| D23 | = 0 Group Mark ending |
| | = 1 Buffer filled ending |
| D22 | = 1 Memory Overflow |
| D21,D20,D18 | = See Below |
| D19 | = 1 For Memory Parity Error |
| D17 | = 1 Parity Error during Descriptor Fetch |
| D16 | = 1 DTC Busy |
| D15 thru D1 | = Core Address |

Read or Write (D30 = 0)

| | 21 | 20 | 18 |
|---|---|---|---|
| Read or Write Completed | 0 | 0 | 0 |
| Read or Write Not Completed* | 1 | 0 | 0 |
| Read or Write Not Completed, Busy | 1 | 1 | 0 |
| Read or Write Not Completed, Not Ready | 1 | 1 | 1 |
| Read or Write Completed, Busy Flag | 0 | 1 | 0 |
| Read or Write Completed, Not Ready Flag | 0 | 1 | 1 |
| DTC Not Ready | 0 | 0 | 1 |

*Attempt to read a write-ready buffer or attempt to write a read-ready buffer.

Interrogate (D30 = 1)

| | 24 | 21 | 20 | 18 |
|---|---|---|---|---|
| Idle | 0 | 0 | 0 | 0 |
| Busy | 0 | 0 | 1 | 0 |
| Not Ready | 0 | 0 | 1 | 1 |
| Write Ready | 0 | 1 | 0 | 0 |
| Read Ready | 1 | 0 | 0 | 0 |
| DTC Not Ready | 0 | 0 | 0 | 1 |

Additional states as determined by individual adapters.

| | 24 | 21 | 20 | 18 |
|---|---|---|---|---|
| Write Ready, Busy | 0 | 1 | 1 | 0 |
| Write Ready, Not Ready | 0 | 1 | 1 | 1 |
| Read Ready, Busy | 1 | 0 | 1 | 0 |
| Read Ready, Not Ready | 1 | 0 | 1 | 1 |
| Read-Write, Ready | 1 | 1 | 0 | 0 |
| Read-Write Ready, Busy | 1 | 1 | 1 | 0 |
| Read-Write Ready, Not Ready | 1 | 1 | 1 | 1 |

## 8.1 GENERAL DESCRIPTION

The B5283 Model III I/O Control Unit includes all standard B5500 operating features, plus the addition of being compatible with the 132 Column Common Language Drum Printer and the three transfer rate Magnetic Tape option.

Significant changes have been made in improving control of a Magnetic Tape operation by narrowing the Write Skew gate, making a Transport speed check, and improvements in Tape Drive logic. The Magnetic Tape Result Descriptor has been extended to include Character Count, Beginning-of-Tape and End-of-Tape Flags, and a Flag for spacing over about six feet of blank tape during a Read operation.

Another feature of this Unit is a Word Count End for an Alpha Write operation.

The Model III I/O Control Unit is also compatible with the 120 Column Printer. However, if a 132 Column Printer is used on a System, then the second Printer must also be a 132 Column Printer.

The I/O Sub-System may consist of one to four I/O Control Units, each operating independently. When using a Model III I/O Control Unit on a System, it is required that all other I/O Units be Model III also.

The Model III I/O is capable of three Density Magnetic Tape operation. The Density Options available are shown in Table 8.1-1.

TABLE 8.1-1

| TAPE TRANSFER RATE OPTIONS | | | |
|---|---|---|---|
| TAPE SPEED / OPTION | 83.4 IPS / 1 | 90 IPS / 2 | 120 IPS / 3 |
| 200 BPI | 16.7 KC | 18.0 KC | 24.0 KC |
| 555 BPI | 46.3 KC | 49.9 KC | 66.7 KC |
| 800 BPI | 66.7 KC | 72.0 KC | |
| SYSTEM CLOCK | 1.0 MC | 1.0 MC | 1.0 MC |

## 8.2 GLOSSARY ADDITIONS FOR MAGNETIC TAPE INTERCONNECTIONS

| | |
|---|---|
| BF2M | Backward Flaw Check Multi - 200 BPI |
| BF5M | Backward Flaw Check Multi - 555 BPI |
| BF8M | Backward Flaw Check Multi - 800 BPI |
| BLTM | Blank Tape Multi |
| BLTS/ | Blank Tape Switch-Not |
| DS2M | Digit Skew Multi - 200 BPI |
| DS5M | Digit Skew Multi - 555 BPI |
| DS8M | Digit Skew Multi - 800 BPI |
| DSWM | Write Skew Multi |
| DWTM | D to W Register Shift - Tape Multi |
| DWWM | D to W Register Shift - Word Count Multi |
| HBIS | Hub Inhibit Switch |
| IM2M | Information Index Multi - 200 BPI |
| IM5M | Information Index Multi - 555 BPI |
| IM8M | Information Index Multi - 800 BPI |
| LD2M | Lost Digit Multi - 200 BPI |
| LD5M | Lost Digit Multi - 555 BPI |
| LD8M | Lost Digit Multi - 800 BPI |
| LP2M | Longitudinal Parity Gap Multi - 200 BPI |
| LP5M | Longitudinal Parity Gap Multi - 555 BPI |
| LP8M | Longitudinal Parity Gap Multi - 800 BPI |
| TSCM | Tape Speed Check Multi |
| TSCS | Tape Speed Check Multi Switch |
| WEQS | Word Counters Equal Switch |
| WGCM | Write Gap Continue Multi |
| WSHD | Word Count Shift Driver |

| | |
|---|---|
| 2BID | 200 Bits Per Inch - Driver |
| 5BID | 555 Bits Per Inch - Driver |
| 8BID | 800 Bits Per Inch - Driver |
| I39S | Input Level (from TSIL = DSI) |

## 8.3 SIGNALS TO MAGNETIC TAPE UNIT FROM B5500

| LEVEL | DESCRIPTION |
|---|---|
| TWI-1/<br>TWI-2/<br>TWI-4/<br>TWI-8/<br>TWI-A/<br>TWI-B/<br>TWI-P/ | Tape Write Information Lines-Not transfer information in parallel to the MTU at a maximum repetition rate of 67KC. |
| TCP/ | Tape Clock Pulse-Not times the writing in the MTU. The repetition rates for TCP are determined by Tape density and by speed of Tape Drive. |
| TUD-1/<br>TUD-2/<br>TUD-3/<br>TUD-4/<br>TUD-5/<br>TUD-6/ | FOR B200 OPERATION: The Tape Unit Designate lines-Not specify which MTU out of a maximum of six is being designated for the Tape Command in progress. Only one TUD-n can be positive at a time.<br><br>FOR B5500 OPERATION: TUD-6 is grounded. |
| FDL/ | Forward Drive Level-Not is derived from the Forward Drive Flip-flop and is positive to drive tape in a forward direction, providing the MTU is designated and ready. The MRD Interlock is removed from Forward Drive Circuit by Drive Holdover modification. |
| BDL/ | Backward Drive Level-Not is derived from the Backward Drive Flip-flop and is positive to drive tape in a backward direction, providing the MTU is designated and ready. |
| TWL/ | Tape Write Level-Not is positive to place the MTU in the Write Status. TWL sets the Write Status Flip-flop in the MTU if the MTU is Write Ready and FDL/ is ground. |
| TRWL/ | Tape Rewind Level-Not is positive to order the MTU or Rewind. |
| TRL/ | Tape Read Level-Not is positive while tape is being read. The Tape Read Level activates the Read Circuitry of the MTU. |

## 8.4 SIGNALS FROM MAGNETIC TAPE UNIT TO B5500

THDL/ — Tape High Density Level-Not - in two density MTUs. THDL/ is positive when the High Density switch is in HIGH DENSITY position. In the three density MTUs, see Table 8.4-1 under THVL/ for density selection.

THVL/ — Tape Very High Density-Not - along with THDL/ selects the Tape Density Option. This line is used only on three density MTUs. See Table 8.4-1 for density selections.

TABLE 8.4-1

| DENSITY SELECTION CHART | | |
|---|---|---|
| THDL/ | THVL/ | DENSITY |
| 0 VOLTS | 0 VOLTS | 200 BITS PER INCH |
| -12 VOLTS | 0 VOLTS | 555 BITS PER INCH |
| -12 VOLTS | -12 VOLTS | 800 BITS PER INCH |

TEFL/ — End Of File Level-Not - is positive after the End Of File marker has been sensed while tape is moving in the forward direction. TEFL then remains positive until tape is driven forward.

TLPL/ — Tape Load Point Level-Not - is positive after the Load Point marker has been sensed while moving tape in the reverse direction. TLPL remains positive until tape is driven forward.

TREL/ — Tape Read Ready Level-Not is positive and indicates the Unit is designated but not rewinding, and the Restart Delay Multi is not ON.

TR P-1
TR P-2
TR P-4
TR P-8
TR P-A
TR P-B
TR P-P

Tape Read Information Pulse - transfer information in parallel to the Input Register in I/O. Transfer rate depends on tape speed and density option used.

TSIL/ — Tape Standard Index Level-Not - is positive when the Standard Index Multi (DSI) and Unit Designate are true in the MTU.

TTOL/ — Tape Transport Operate Level-Not - when positive, indicates the Transport is ready to operate or be designated.

| | |
|---|---|
| TWRL/ | Tape Write Ready Level-Not - is positive when the File Protect Ring is on the Tape Reel and TREL is positive. |
| TWSL/ | Tape Write Status Level-Not - is positive to indicate that the MTU is in the Write Status. (Write Status Flip-flop is ON.) |

## 8.5 ADJUSTMENTS - MULTIVIBRATORS

The adjustment of the I/O Multis is performed during a series of tape operations. Table 8.5-1 lists the particular tape operations to be performed, scope set-up procedure, Multi location, D.A. page, and the Multi Timing for each Multi to be adjusted.

### Test Procedure for Tape Character Shift Detection Logic

Four tests have been devised to verify that the "Tape Character Shift" detection logic is functioning correctly. It is not necessary to scope D20F. Only check its status on the I/O Control Unit Panel to insure that it is being set. The three Multis involved in this logic are: LD2M (200BPI), LD5M (555 BPI) and LD8M (800 BPI).

NOTE

All tests are in the ALPHA Mode.

Procedure: Repeatedly, Write a seven (7) character pattern, followed by a question mark (?) and then one (1) more character. Make all characters the same.

Example:

| 7 characters | ? | 1 char. |
|---|---|---|

Results: The question mark will result in a drop-out and allow LDnM to time out. This condition and the following SHOF pulse enable logic for setting of D20F.

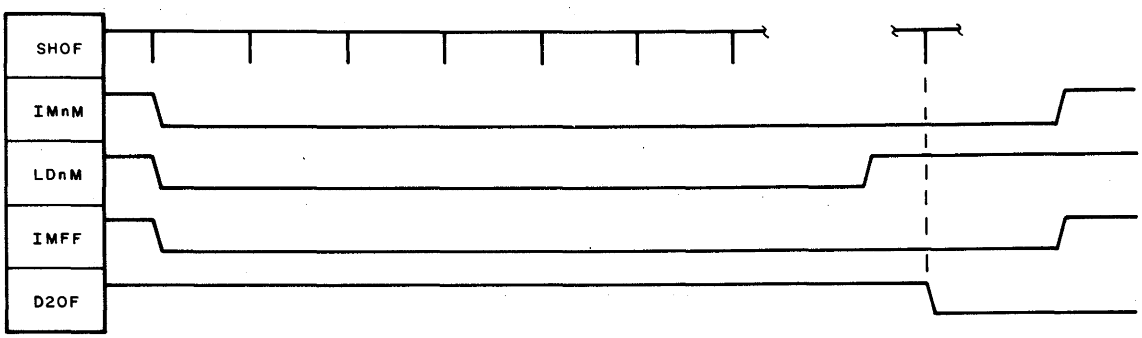



FIGURE 8.5-1
TEST 1

Procedure: Repeatedly, Write a pattern of eight (8) characters followed by three (3) question marks and two (2) more characters. Make all characters the same.

Example:

| 8 characters | ??? | 2 char. |
|---|---|---|

Results: The two characters following the question marks will be detected as two Longitudinal Parity characters. This error is detected by the logic EOPS · D30F/ · SHOF · RCNF.

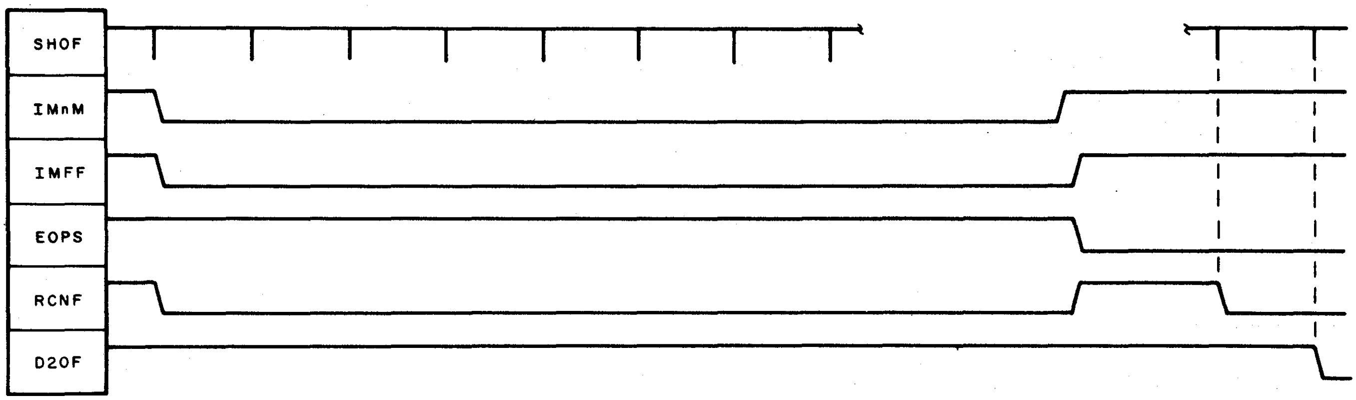



FIGURE 8.5-2
TEST 2

Procedure: Construct a pattern of two (2) characters followed with three (3) question marks, and then eight (8) more valid characters. With this pattern, Write approximately a quarter reel of tape. Do not rewind after making tape.

Example:

| 2 char. | ??? | 8 characters |
|---|---|---|

Next, insert a Backward Read command.

Results: This pattern will simulate an erroneous character following the End Of Record, and will be detected by this modification. The detecting logic enabled for this error is: EOPS · SHOS . D30F/ · BKWF.

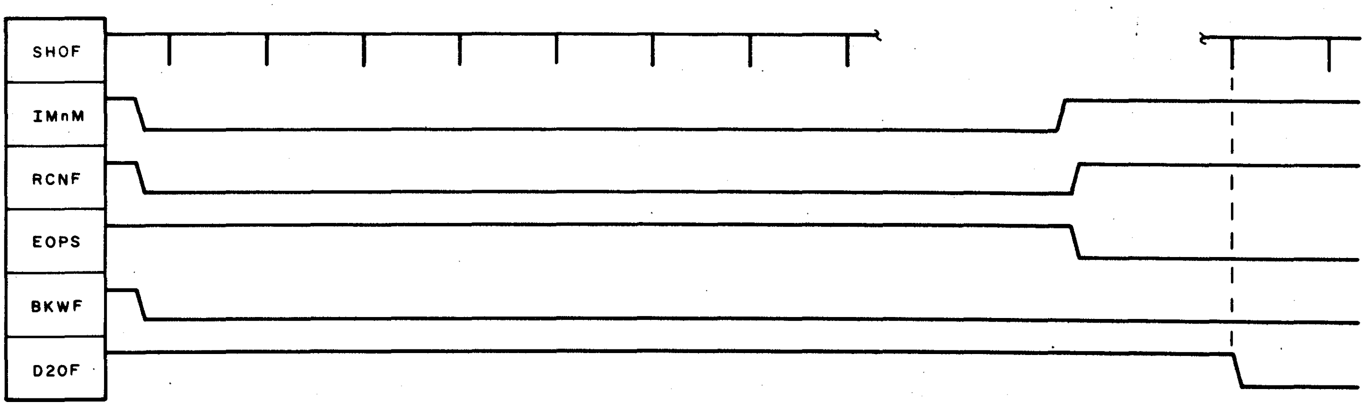



FIGURE 8.5-3
TEST 3

Procedure: Repeatedly, Write eight (8) characters followed with three (3) question marks, then a string of any eighty

(80) valid characters.

Example:

8 character ??? 80 characters

Results: The question marks simulate two or more character drop-outs on a Write operation. This error is detected by the timing out of IMnM. The complete logic enabled is: EXNS · IMIF · D24D/.

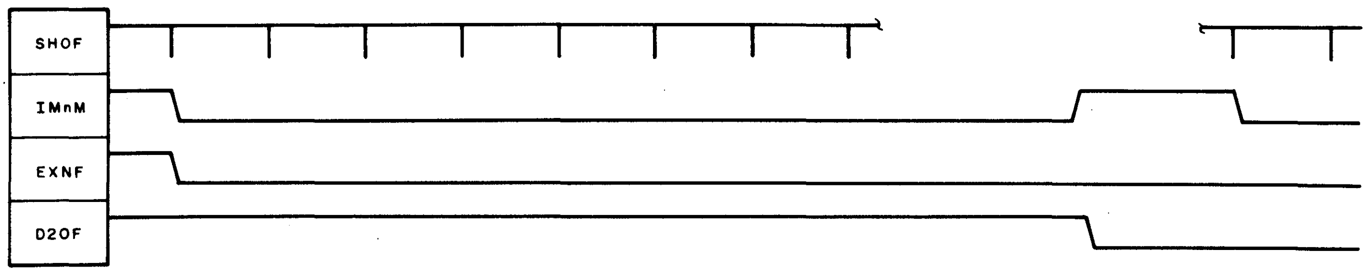



FIGURE 8.5-4
TEST 4

| NAME | LOCATION | TYPE | DA PAGE | SETTING | | | SCOPE SET-UP | | | | | | TAPE OPERATION | DENSITY | SPECIAL INSTRUCTIONS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 83.4 ips | 90 ips | 120 ips | OUTPUT | SYNC | SLOPE | A TRACE | B TRACE | MODE | | | |
| BTDM | AD B0 A2 | MMN | 63.03.17 | 7.8ms | 7.8ms | 6.6ms | AD B0 F0 | AA D8 P2 (S03D) | NEG | AD B0 F0 (BTDM) | —— | A ONLY | CONTINUOUS WRITE | ANY | SYNC POINT STARTS 6μs BEFORE BTDM. |
| | | | | | | | | | | | | | | | |
| DSWM | AA A6 A2 | MUM | 63.04.24 | 3.6μs | 3.3μs | 2.5μs | AA A6 F0 | INTERNAL | NEG | AA A6 F0 (DSWM) | —— | A ONLY | CONTINUOUS WRITE | ANY | |
| DS2M | AA B7 A2 | MUG | 63.03.03 | 28μs | 26μs | 19μs | AA B7 F0 | AA A6 F0 (DSWM) | NEG | AA B7 F0 (DS2M) | —— | A ONLY | CONTINUOUS READ | 200 bpi | |
| DS5M | AA B7 N2 | MUF | 63.03.03 | 9.3μs | 8.5μs | 6.0μs | AA B7 U0 | AA A6 F0 (DSWM) | NEG | AA B7 U0 (DS5M) | —— | A ONLY | CONTINUOUS READ | 500 bpi | |
| DS8M | AA A7 N2 | MUF | 63.03.03 | 6.0μs | 5.5μs | 3.9μs | AA A7 U0 | AA A6 F0 (DSWM) | NEG | AA A7 U0 (DS8M) | —— | A ONLY | CONTINUOUS READ | 800 bpi | |
| | | | | | | | | | | | | | | | |
| LP1M | AA B8 N2 | MUV | 63.03.10 | 21ms | 20ms | 15ms | AA B8 U0 | AA D8 V0 (S04D) | NEG | AA B8 U0 (LPIM) | —— | A ONLY | REWIND FOLLOWED BY READ | ANY | |
| LP2M | AA B9 A2 | MUJ | 63.03.09 | 1000ms | 900μs | 700μs | AA B9 F0 | AB C2 U4 (IMIF) | NEG | AA B9 F0 (LP2M) | —— | A ONLY | CONTINUOUS WRITE OF SHORT RECORDS | 200 bpi | |
| LP5M | AA B8 A2 | MUI | 63.03.09 | 360μs | 330μs | 250μs | AA B8 F0 | AB C2 U4 (IMIF) | NEG | AA B8 F0 (LP5M) | —— | A ONLY | CONTINUOUS WRITE OF SHORT RECORDS | 500 bpi | |
| LP8M | AA A7 N7 | MUI | 63.03.14 | 260μs | 240μs | 200μs | AA A7 U5 | AB C2 U4 (IMIF) | NEG | AA A7 U5 (LP8M) | —— | A ONLY | CONTINUOUS WRITE OF SHORT RECORDS | 800 bpi | |
| | | | | | | | | | | | | | | | |
| WGNM | AA B4 N2 | MMN | 63.03.10 | 4.7ms | 4.7ms | 4.7ms | AA B4 U0 | AA D8 V0 (S04D) | NEG | AA B4 U0 (WGNM) | —— | A ONLY | CONTINUOUS WRITE OF SHORT RECORDS | ANY | GROUND OUT AF B2 X2 (D21F) IF WRITES ARE DONE LOCALLY AND RECYCLE IS ON. |
| WGCM | AA B5 A2 | MMN | 63.03.10 | 5.7ms | 5.1ms | 5.5ms | AA B5 F0 | AA D8 V0 (S04D) | NEG | AA B5 F0 (WGCM) | —— | A ONLY | CONTINUOUS WRITE | ANY | |
| WGBM | AA B4 A2 | MMØ | 63.03.10 | 75ms | 68ms | 52ms | AA B4 F0 | AA D8 V0 (S04D) | NEG | AA B4 F0 (WGBM) | —— | A ONLY | REWIND FOLLOWED BY WRITE | ANY | |
| | | | | | | | | | | | | | | | |
| BF2M | AB B4 A2 | MUI | 63.03.02 | 400μs | 350μs | 250μs | AB B4 F0 | AB C2 U4 (IMIF) | NEG | AA B4 F0 (BF2M) | —— | A ONLY | BACKWARD READ | 200 bpi | USE A RECORD FORMAT WHICH CONTAINS AN LP CHARACTER. |
| BF5M | AB B4 N2 | MUH | 63.03.02 | 145μs | 130μs | 100μs | AB B4 U0 | AB C2 U4 (IMIF) | NEG | AB B4 U0 (BF5M) | —— | A ONLY | BACKWARD READ | 500 bpi | |
| BF8M | AB A4 N2 | MUH | 63.03.01 | 105μs | 95μs | 75μs | AB A4 U0 | AB C2 U4 (IMIF) | NEG | AB A4 U0 (BF8M) | —— | A ONLY | BACKWARD READ | 800 bpi | |
| | | | | | | | | | | | | | | | |
| BWIM | AA B6 N2 | MMQ | 63.03.02 | 1.2ms | 1.2ms | 1.2ms | AA B6 U0 | INTERNAL | NEG | AA B6 U0 (BWIM) | —— | A ONLY | BACKWARD READ | ANY | |
| BRIM | AB B4 A7 | DMJ | 63.03.02 | 6.6ms | 6.6ms | 6.6ms | AB B4 E9 | AB B4 H5 (BRIM-IN) | POS | AB B4 E9 (BRIM) | —— | A ONLY | WRITE FOLLOWED BY BACKWARD READ | ANY | |
| | | | | | | | | | | | | | | | |
| IM2M | AA B6 A7 | DUS | 63.03.08 | 135μs | 125μs | 95μs | AA B6 F5 | AA A4 W5 (TRPS) | NEG | AA B6 F5 (IM2M) | AA C9 F4 (SHOF) | ALGEBRAIC ADD | CONTINUOUS WRITE OF SHORT RECORDS | 200 bpi | ADJUST MULTI TIME DURATION FROM THE NEGATIVE SLOPE OF THE LAST SHOF PULSE OF THE RECORD. |
| IM5M | AA B6 A2 | DUR | 63.03.08 | 50μs | 45μs | 35μs | AA B6 F0 | AA A4 W5 (TRPS) | NEG | AA B6 F0 (IM5M) | AA C9 F4 (SHOF) | ALGEBRAIC ADD | CONTINUOUS WRITE OF SHORT RECORDS | 500 bpi | |
| IM8M | AA A6 N2 | DUE | 63.01.53 | 35μs | 32μs | 25μs | AA A6 U0 | AA A4 W5 (TRPS) | NEG | AA A6 U0 (IM8M) | AA C9 F4 (SHOF) | ALGEBRAIC ADD | CONTINUOUS WRITE OF SHORT RECORDS | 800 bpi | |
| | | | | | | | | | | | | | | | |
| LD2M | AB A0 N2 | DUF | 63.03.02 | 85μs | 78μs | 58μs | AB A0 U0 | AB C1 U4 (SKFF) | NEG | AB A0 U0 (LD2M) | AA C9 F4 (SHOF) | ALGEBRAIC ADD | CONTINUOUS WRITE ALPHA (7 CHARACTERS) | 200 bpi | USING DELAYED SWEEP, SELECT LAST SHOF PULSE BEFORE GAP AND EXPAND THIS PORTION TO MAKE PROPER MULTI ADJUSTMENT. |
| LD5M | AA A9 N7 | DUE | 63.03.02 | 30μs | 28μs | 21μs | AA A9 U5 | AB C1 U4 (SKFF) | NEG | AA A9 U5 (LD5M) | AA C9 F4 (SHOF) | ALGEBRAIC ADD | CONTINUOUS WRITE ALPHA (7 CHARACTERS) | 500 bpi | |
| ✓ LD8M | AB A0 A7 | DUQ | 63.02.01 | 21μs | 20.5μs | 16μs | AB A0 F5 | AB C1 U4 (SKFF) | NEG | AB A0 F5 (LD8M) | AA C9 F4 (SHOF) | ALGEBRAIC ADD | CONTINUOUS WRITE ALPHA (7 CHARACTERS) | 800 bpi | |
| | | | | | | | | | | | | | | | |
| BLTM | AA B5 N2 | DMS | 63.03.05 | .72sec | .67sec | .50sec | AA B5 U0 | AA B5 V4 (BLTM-IN) | NEG | AA B5 U0 (BLTM) | —— | A ONLY | CONTINUOUS READ | ANY | USE A DEGAUSSED TAPE. |
| | | | | | | | | | | | | | | | |
| TSCM | AB C4 A2 | MMQ | 63.03.03 | 2.1ms | 2.0ms | 1.5ms | AB C4 F0 | AB C3 U4 (FDWF) | NEG | AB C4 F0 (TSCM) | AA C9 F4 (SHOF) | ALGEBRAIC ADD | CONTINUOUS WRITE | ANY | SHOULD NOT TIME OUT PRIOR TO SHOF. TO CHECK LOGIC, CREATE TAPE DRAG WITH FINGER PRESSURE. D20F SHOULD SET. |

✓ Changes or additions since last issue.

CHART 8.5-1
MULTI VIBRATOR ADJUSTMENT

## 8.6 PULSE COUNTER FREQUENCY SELECTION

Adjust the Magnetic Tape Write Clock Pulse repetition rate for Tape Transport speed option to be used by installing one of the following pluggable options:

Pluggable Option 1: (for operation with 83.4 IPS MTUs - 2 or 3 density Units)

| | | |
|---|---|---|
| ANC | AB A1 L2 | (200 BPI - 17KC) |
| AB 2 | AB A1 L5 | (555 BPI - 46KC) |
| AB 2 | AB A1 L8 | (800 BPI - 67KC) |

Pluggable Option 2: (for operation with 90 IPS MTUs - 2 or 3 density Units)

| | | |
|---|---|---|
| ANC | AB A1 L1 | (200 BPI - 18KC) |
| AB 2 | AB A1 L4 | (555 BPI - 50KC) |
| AB 2 | AB A1 L7 | (800 BPI - 72KC) |

Pluggable Option 3: for operation with 120 IPS MTUs - 2 density only)

| | | |
|---|---|---|
| AB 1 | AB A1 L0 | (200 BPI - 24KC) |
| AB 1 | AB A1 L3 | (555 BPI - 67KC) |

## 8.7 RESULT DESCRIPTOR

Upon completion of an I/O operation, a Result Descriptor is formed and returned to an assigned Memory location. The format of this Descriptor other than for Magnetic Tape, remains as constructed by previous model I/Os. This description will explain the deviations and additions made in the Magnetic Tape Result Descriptor under the control of a Model III I/O Control Unit. These changes are not made directly in the "D" Register, but in the "W" Register during the "D" to "W" transfer (DWTD) at SC = 14.

Designated areas of the Result Descriptor have been allocated to contain information on the Character Count; End-Of-Tape or Beginning-Of-Tape having been sensed; and a Flag to signify that approximately six feet of blank tape was detected. An explanation of each is included later in this section.

The Error field extensions are defined in Table 8.7-1. W19F being ON, signals the MCP that Error Flags are present outside the normal Error field. W46F specifies a Model III I/O Result Descriptor.

TABLE 8.7-1

| W19 | W34 | W35 | W36 | W37 | W46 | DESCRIPTION |
|---|---|---|---|---|---|---|
| 1 | 0/1 | 0/1 | 0/1 | 0/1 | 0 | MEMORY PARITY - MODEL I OR II |
| 1 | 0 | 0 | 0 | 1 | 1 | MEMORY PARITY - MODEL III |
| 1 | 0 | 0 | 1 | 0 | 1 | BLANK TAPE - MODEL III |
| 1 | 0 | 1 | 0 | 0 | 1 | BEGINNING-OF-TAPE - MODEL III |
| 1 | 1 | 0 | 0 | 0 | 1 | END-OF-TAPE - MODEL III |

NOTE

D21 is not used during a Write Operation. W40 thru W31 is used as a Result Descriptor field. W19 and W46 are set if W34, W35, W36 or W37 is set. W37 is set if there is a Parity Error, Memory to I/O.

### Blank Tape Sensing

This logic detects the condition of spacing over approximately six feet of blank tape during a Read operation. This results in the operation being terminated and W36F set in the Result Descriptor to indicate the condition.

The timing of BLTM (Blank Tape Multi) determines the amount of blank tape permitted to pass before the Multi times out and terminates the operation. Adjustment of the Multi time-out point is dependent upon tape speed.

BLTM is initially triggered at SC = 4 through the logic of S04D · TAOD · HOLF and is held over by ensuing SHOF pulses if the record being Read is valid (VRCF is true). Refer to Figure 8.7-1.

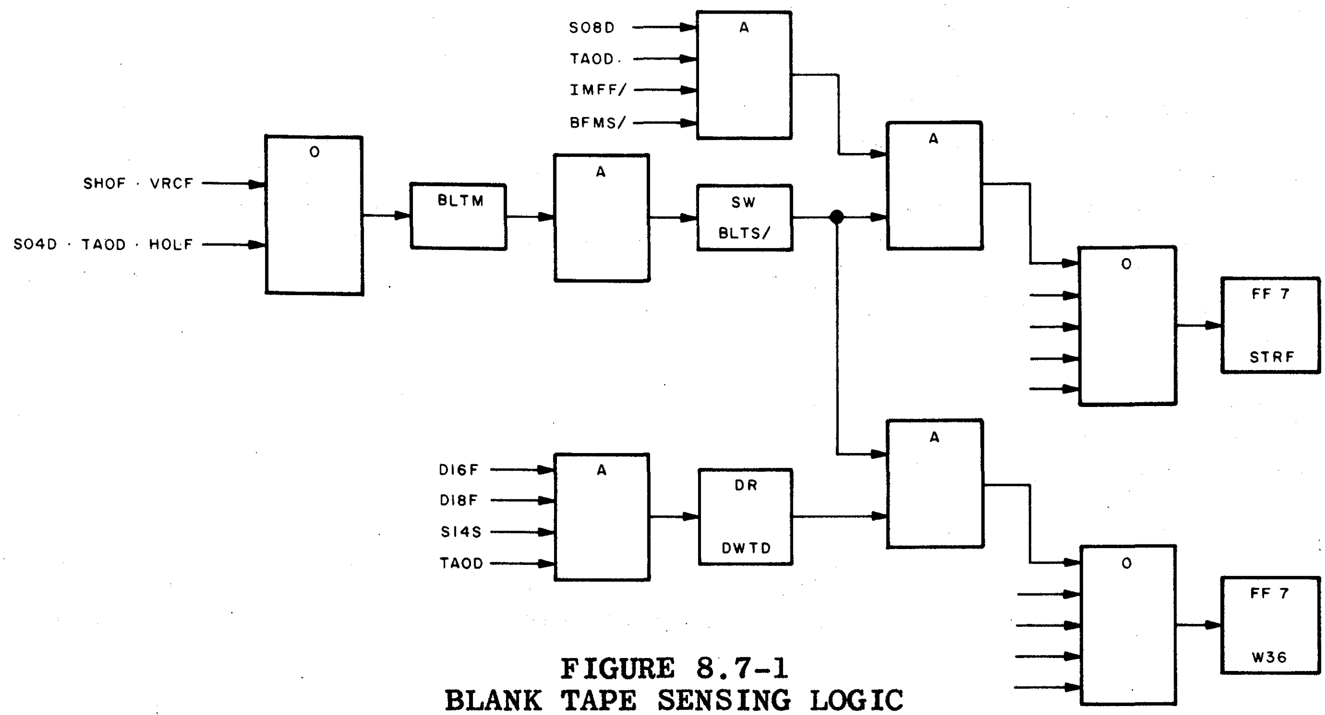



FIGURE 8.7-1
BLANK TAPE SENSING LOGIC

Should sufficient blank tape be encountered, no SHOF pulses are generated which would allow BLTM to time out. BLTS/ becomes true. This true level from BLTS/ enables logic to set STRF at SC = 8 and control is transferred to SC = 14 where the Result Descriptor is constructed. During the "D" to "W" (DWTD) transfer, W36F is set to indicate the blank Tape condition to the MCP.

The adjustment of BLTM is determined by MTU speed. For correct setting see listings below.

| | |
|---|---|
| | .72 seconds for 83.4 IPS |
| BLTM | .67 seconds for 90 IPS |
| | .50 seconds for 120 IPS |

## End-Of-Tape

When driving tape in a forward direction on either a Read or Write operation, the sensing of the End-Of-Tape Reflector Strip will be indicated in the Result Descriptor. During the "D" to "W" shift, W34F will be set as the Flag. A true level from I38D (TEFL) enables the setting of this bit. See Figure 8.7-2.

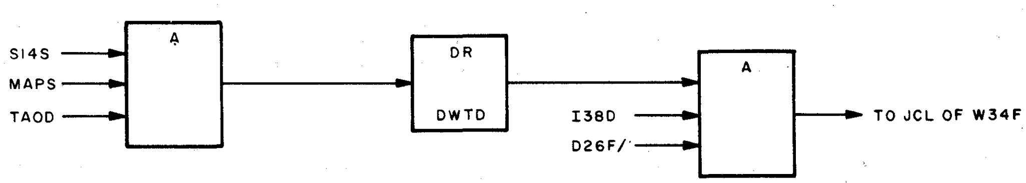



FIGURE 8.7-2
END-OF-TAPE LOGIC

Beginning-Of-Tape

During a Backward Read operation, sensing of the Beginning-Of-Tape Reflector Strip will be signified with the setting of W35F in the Result Descriptor. This Flag is set during the "D" to "W" transfer with I34D (Beginning-Of-Tape) enabling the logic. See Figure 8.7-3.

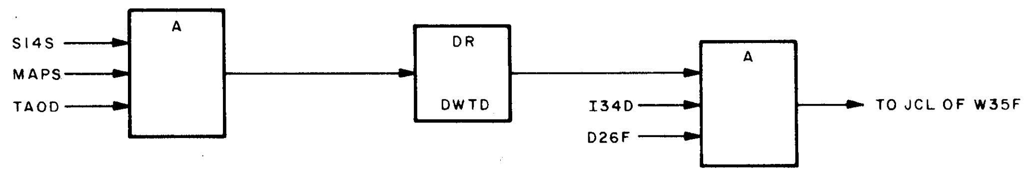



FIGURE 8.7-3
BEGINNING-OF-TAPE LOGIC

Character Count

The addition of the Character Count to the Result Descriptor is for MCP usage.

Position W31F through W33F to define the number of characters stored in the last Memory Address accessed during a Read operation. Interpretation is dependent upon direction of tape movement.

1. Forward Read:

   W31F thru W33F = 0 signifies last word read was complete.

   = n where "n" equals the number of characters stored in the last partial word.

2. Backward Read:

   W31F thru W33F = 7 signifies last word read was complete.

   = n where "n" equals the number of characters stored in the last partial word.

When the Indexing Control Cycle is initiated, IMIF is set; the 3-bit Character Count is transferred into PC4F, PC5F and PC6F for temporary storage. Refer to Figure 8.7-4.

The information is retained in these bit positions of the Pulse Counter until the Result Descriptor is constructed at SC = 14. At that time, and under the control of the tape "D" to "W" Driver (DWTD), the character count is shifted into W31f, W32F and W33F.

SEE NEXT PAGE FOR FIGURE 8.7-4.

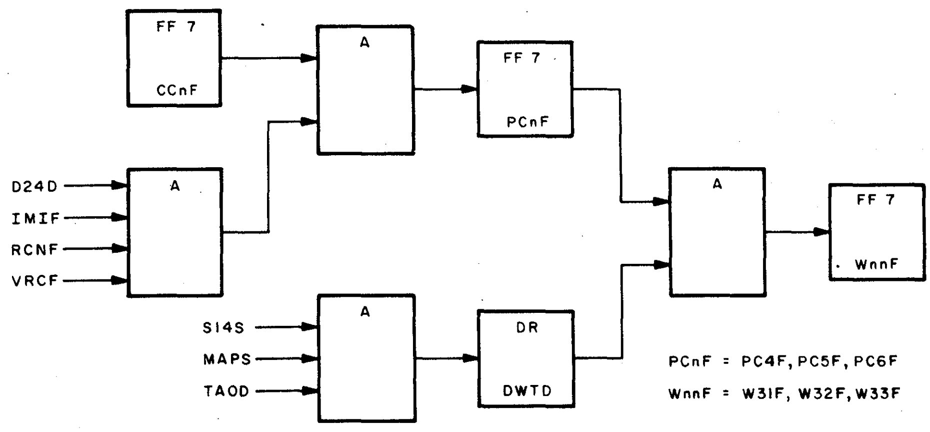



**FIGURE 8.7-4**
**CHARACTER COUNT LOGIC**

## 8.8 MAGNETIC TAPE SPEED CHECK

This added logic measures the time required for the first character written to move from the Write head to the Read head. If the Tape Unit is not up to speed, TSCM (Tape Speed Check Multi) will time out and D20F in the Result Descriptor is set to indicate the error.

TSCM is triggered as the first character is written (S11D · TAOD · HOLF). If the Tape Unit is up to speed, TSCM would not time out prior to this character passing under the Read head. If the Tape Drive is abnormal, the Multi times out and the logic of TSCM/ · SHOF · RCNF/ · D24D/ is enabled to set D20F in the Result Descriptor. Refer to Figure 8.8-1.

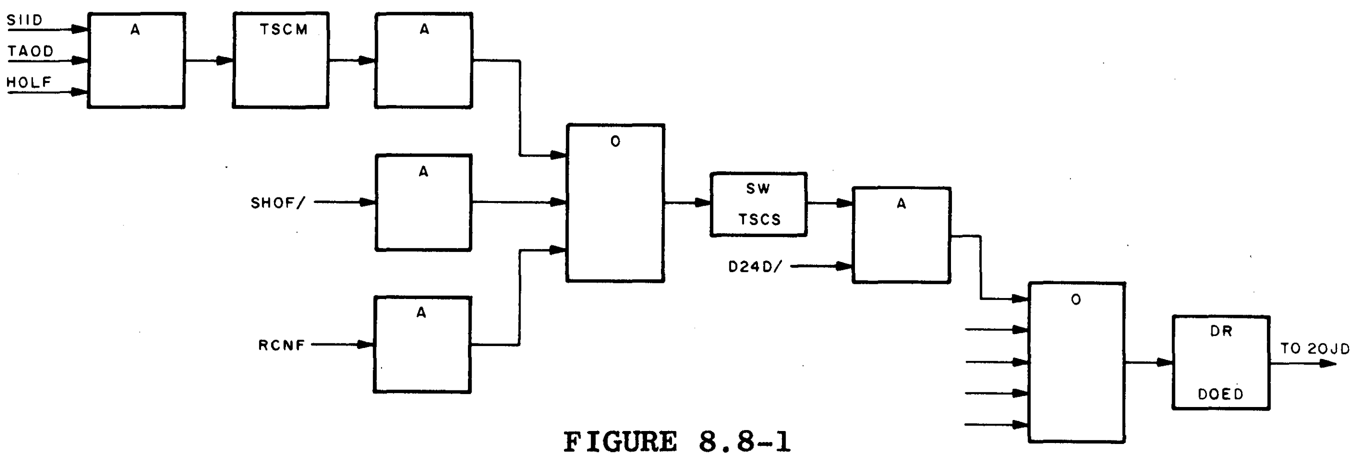



FIGURE 8.8-1
MAGNETIC TAPE SPEED CHECK LOGIC

The adjustment of the time out point for TSCM is determined by the tape speed. See listings below for proper settings.

| | |
|---|---|
| | 2.1 milliseconds for 83.5 IPS |
| TSCM | 2.0 milliseconds for 90 IPS |
| | 1.5 milliseconds for 120 IPS |

## 8.9 MAGNETIC TAPE DRIVE HOLDOVER

Drive Holdover can be activated during either a Read or a Write operation, but only when tape is moving in a Forward direction.

During successive Forward Read operations, this improvement provides the ability to activate Tape Drive without regard to the MRD Interlock. This in effect, will allow the Tape Unit to maintain a continuous drive between successive tape operations; providing that the successive operation is initiated before Tape Drive has started to decelerate. The Inter-Record Gap time will be reduced from the current 11.45 milliseconds to 6.25 milliseconds.

In order to maintain drive between successive Forward operations, the second command must be initiated before tape has started to decelerate. If not, the second drive activation is delayed until tape movement has stopped (MRD/). Therefore, in order to capitalize on the time savings, a Drive Holdover Window must be hit by the second command. If this Window is missed, then the time between tape recorde is increased from 6.25 milliseconds to 11.45 milliseconds.

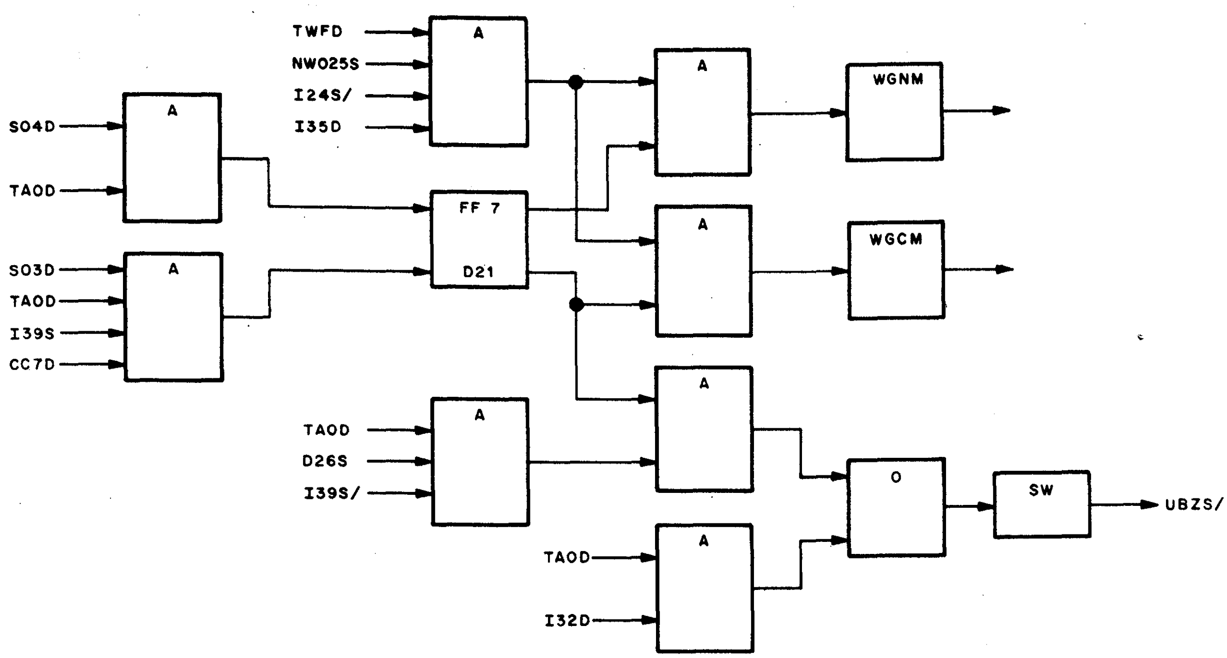



FIGURE 8.9-1
MAGNETIC TAPE DRIVE HOLDOVER LOGIC

To implement Drive Holdover, logic has been added for the purpose of monitoring the DSI condition in the designated MTU by the I/O. The normal Unit Interrogation conducted under the control of the Character Counter, remains unaltered up through CC = 3.

At CC = 4, one of two conditions can exist.

1. CC2 is SET <u>if</u> the designated MTU is in a "Ready" state and Not

Busy. With CC = 5, PROD is enabled.

2. When successive Tape operations are executed, the second command will be initiated with the Unit reflecting a Busy signal (UBZS) carried over from the first command. This Busy signal activates logic to set CC2F, thus bringing the total Character Count to seven. At this time, the Busy-Test Delay Mutli (BTDM) is triggered. A check on the status of DSI is also made at this time through Input Driver I39D. During successive commands, a true level will be reflected and D21F is set as a Flag. This is the Window referred to previously, and must occur to maintain constant drive. D21F and I39S are included in the equation for maintaining UBZS. Until DSI times out, a static condition exists and the Character Count remains at six.

It should be understood that at this time in the sequence, the I/O is disregarding the status of MRD. With the timing out of DSI, the Unit Busy level is removed and CC2F is reset. This adjusts the Character Count to five and enables PROD.

During successive Write commands, Record Gaps are governed by the Write Gap Continuous Multi (WGCM). D21F being set, signifies that Drive Holdover has been utilized and that WGCM will be triggered. The presently used Write Gap Normal Multi (WGNM) will be fired when Drive Holdover is bypassed.

## 8.10 WORD COUNT END FOR ALPHANUMERIC WRITE

A feature of the Model III I/O is the available option of an Alpha Write operation with Word Count ending. The configuration of D25F and D27F in the I/O Descriptor determines the type of ending utilized to terminate the operation. The Table 8.10-1 shows combinations and significance of each.

TABLE 8.10-1

| D25F | D27F | DESCRIPTION |
|---|---|---|
| 0 | 0 | ALPHA WRITE - GM END |
| 1 | 0 | ALPHA WRITE - WC END |
| 1 | 1 | BINARY WRITE - WC END |

When an Alpha Write by Word Count is specified, termination is through decrementing the Word Count to "zero" (WC = 0) as in normal binary Word Count ending.

## 8.11 NARROW WRITE SKEW GATE

The addition of DSWM provides a method for reducing the Skew gate timingfor Read checking during a Write operation.

DSWM is triggered by the initial TRP developed as the Read head senses the first flux change. The normal Read Multis will be inhibited by a false output from the HBIS switch. Refer to Figures 8.11-1 and 8.11-2.

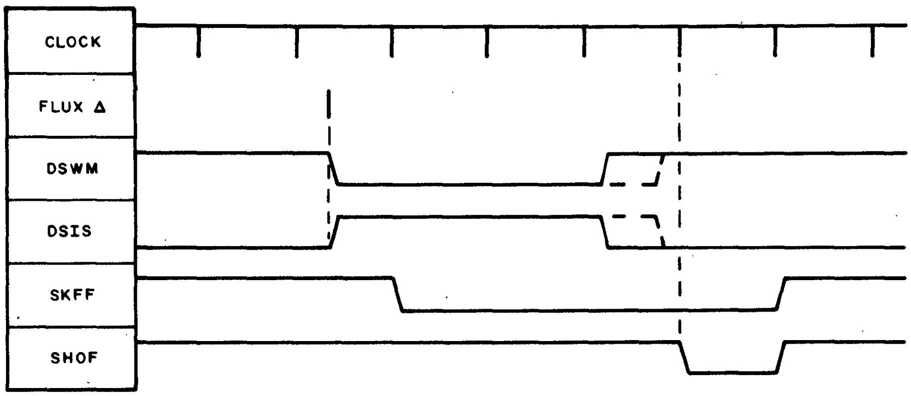



FIGURE 8.11-1
WRITE SKEW TIMING

The true output from DSWM is applied to the set input of SKFF and the Skew Flip-flop will be set with the next Clock pulse. As long as DSWM remains true, SHOF is inhibited from being set by DS1S. When the Multi times out, the inhibit term is removed and SHOF is set.

SHOF in turn resets SKFF and at the same time enables logic for transfer of the character just read, into the Input Buffer. The Lateral Parity Check of this character will now be made.

In summary, all bits of the character under test must be read into the Input Register prior to the timing out of DSWM plus one Clock pulse. In event the Skew of the Information bits exceed this period, PELS sets D20F to signify the Error.

The time duration of DSWM is determined by the tape speed. Refer to the listings below for proper adjustment.

| | |
|---|---|
| DSWM | 3.6 μs for 83.5 IPS |
| | 3.3 μs for 90 IPS |
| | 2.5 μs for 120 IPS |

SEE NEXT PAGE FOR FIGURE 8.11-2.

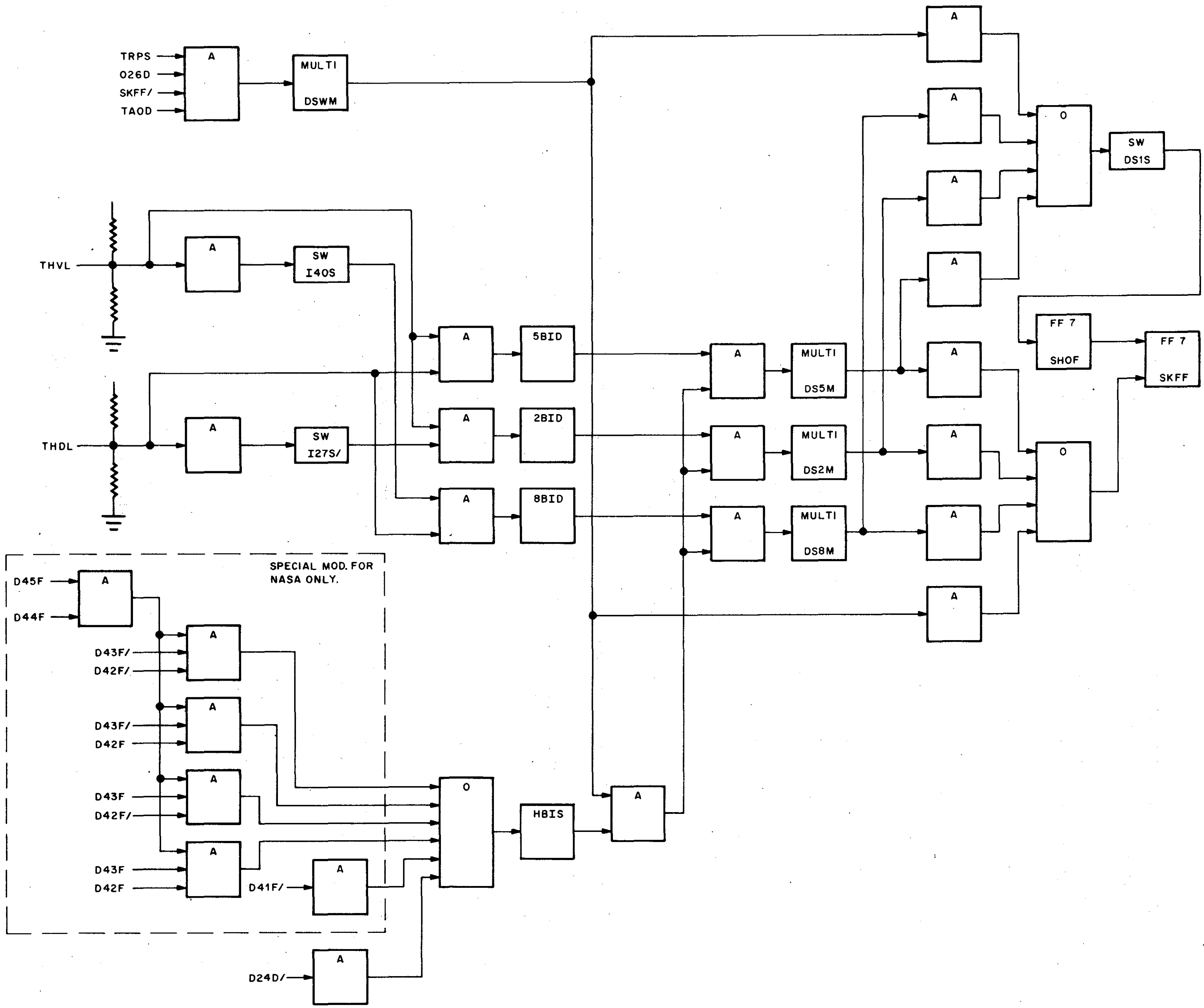



FIGURE 8.11-2
READ-WRITE SKEW LOGIC

## 8.12 COMMON LANGUAGE DRUM PRINTER

### General Description

A feature of the Model III I/O Control Unit is the compatability with either a 120 or 132 Column Printer. Certain restrictions must be adhered to in that when one 132 Column Printer is used on a System, then the second Printer must be of the same type.

With the I/O Descriptor in the "D" Register the status of the Printer is checked. If the Unit is Ready and Not Busy, the operation continues. Otherwise, the operation is terminated and a Result Descriptor is returned to Memory.

With the Unit Ready and Not Busy, an interrogation of the type of Printer on line is made. If it is a 132 Column Printer, then D26F will be set. D26F remains reset for the 120 Column Printer. The Descriptor Word Count is shifted into the five most significant bit positions (D36F through D40F) of the Word Count field. At the same time, D31F through D35F is adjusted to contain either a 14 or 16 depending upon the type of Printer operation.

During the Address Counter adjustment phase, D01F through D15F is advanced by the amount specified in D31F through D35F. This adjusts the Address to point to the top of the Printer Buffer area in Memory.

With D31F through D35F having been counted down to "zero", either a 15 or 17 will be set into these bit positions as designated by D26F. This figure specifies the maximum number of words required for one complete line of print. However, transfer of information to the Printer Buffer is controlled by D17F which is set when D36F through D40F (Descriptor Word Count) equals D31F through D35F (Set Word Count).

Memory is accessed to bring the first word pointed to by D01F through D15F into the "W" Register of the I/O Control Unit. The Word Counter is counted down one and comparison of the two-section Word Count field is made (D36F through D40F is compared to D31F through D35F). Until these two fields compare, D17F remains reset and blanks are automatically inserted into the Output Buffer of I/O.

NOTE

> Should the Descriptor Word Count exceed the allocated Printer Buffer area in Memory, then D17F would be ON at SC = 3 and CC = 5.

This two-section Word Counter comparison continues as each word is brought from Memory. When the two-sections of the Word Counter compare, this signifies that the present word in the "W" Register and all remaining information is to be transferred to the Printer. D17F will be set to indicate word comparison and also enable information transfer paths to the Printer.

When all remaining information is sent to the Printer, the Format Control digits are transferred to the Output Buffer of the I/O and then to the Format Control Flip-flops in the Printer. The Printer is released from the I/O Control Unit and a Result Descriptor constructed and returned to an assigned Memory location for MCP interrogation.

## 8.13 SIGNALS TO DRUM PRINTER FROM B5500

| LEVEL | | DESCRIPTION |
|---|---|---|
| PI1L | (FC1L) | Printer Information Lines transfer information, least significant digit first, to the Printer. The PIn Lines transfer information to the Printers Information Register and Format Control Flip-flops. The actual transfer routing is controlled by the Printer Print Information Transfer and Printer Lister Command Levels.<br><br>The PIn Levels are switched in the B5500 I/O 2μs after the occurrence of the Printer Lister Clock Pulse (PLCP). These lines are strobed in the Printer by PLCP. |
| PI2L | (FC2L) | |
| PI4L | (FC4L) | |
| PI8L | (FC8L) | |
| PIAL | (PDSL) | |
| PIBL | (PSSL) | |
| PIPL | | |

**NOTE**

The terms in parenthesis adjacent to the PInL, denote the Format Control Function related to that line.

| LEVEL | DESCRIPTION |
|---|---|
| FC1L<br>FC2L<br>FC4L<br>PC8L | Format Control Levels transfer the Format Control Digit to the Format Control Flip-flops (FCF) in the Printer. They also set the Paper Motion Flip-flops (PMF) to initiate paper motion. These signals are clocked with the Central Processor Clock. |
| PDSL | Paper Double Space Level orders a double space by setting the Double Space Flip-flop (DSF) and initiates paper motion by setting PMF in the Printer. |
| PSSL | Paper Single Space Level initiates paper motion by setting PMF. PMF can be set by any of the Format Control Levels. |
| PLCL | The Printer Lister Command Level when negative, initiates Print Cycle after the transfer of information to the Printer Buffer has been completed and paper has stopped.<br><br>PLCL also serves to route the transfer of Format Control Information into the Format Control Flip-flops. |
| PITL | Printer Print Information Transfer Level when negative, indicates information is being transferred to the Printer at a 100KC rate. PITL serves to gate the information into the Information Register (IRF) in the Printer at least 10μs after it goes true. PITL is true for one period before transfer of first character. Aslo used to clear the Parity Error Flip-flop. |

| | |
|---|---|
| EPRL | End of Page Reset Level when negative, resets the End of Page Flip-flop (EOPF). |

## 8.14 SIGNALS FROM DRUM PRINTER TO B5500

| LEVEL | DESCRIPTION |
| --- | --- |
| PPEL | Printer Print Parity Error Level when negative, indicates a Parity Error exists. |
| PRRL/ | Printer Ready Level-Not when positive, indicates the following conditions exist:<br>1. Power ON, includes Drum Power.<br>2. Paper loaded.<br>3. No Paper Motion Alarm, no 6-8 Alarm and no Skew Alarm.<br>4. START button depressed.<br>5. LOCAL/REMOTE switch in REMOTE. |
| PCYL | Printer Cycle Level when negative, indicates that a Print cycle is in progress. |
| PAML/ | Paper Motion Level-Not when positive, indicates that paper is in motion. |
| EOPL/ | End Of Page Level-Not when positive, indicates that end of page has been sensed. |
| PLCP | Printer Lister Clock Pulse is derived from the Printer Clock with a repetition rate of 100KC. |
| PIDL | Printer Interlock Level when negative, indicates a Printer is connected. |
| PLLL | 132 Column Printer when negative, indicates a 132 Column Printer on line. |

## 8.15 650 LPM SEQUENCE COUNT EXPLANATION

While following through the 650 LPM Sequence Count explanation, refer to either the State Chart Figure 8.15-1, or the Printer Flow Chart.

SC = 0:
SC = 1:
SC = 2: Operation initiated by AUNS from Central Control. Two Memory accesses performed.

1. Read Descriptor Address from Memory.
2. Read Descriptor from Memory.

SC = 3:

1. Check peripheral Unit for READY and NOT BUSY.
2. Interrogate for 120 or 132 Column Printer. If 132 Column Printer, D26F set to 1.
3. Shift lower five bits of Word Counter to upper 5-bit positions. Set D40F thru D36F to D35F thru D31F.
4. Set D35F thru D31F to either 14 or 16 depending upon status of D26F.
5. Set D17F to 1 if Word Count is above maximum buffer size.

SC = 4: Check state of D30F.

1. D30F = Control Descriptor = jump to SC = 11.
2. D30F/ = Control Descriptor-Not = SC + 1.

SC = 5:

1. Word Counter minus 1 and D15F thru D01F plus 1, until D35F thru D31F = 0.
2. D35F thru D31F = 0, branch to SC = 9.
3. D35F thru D31F = 0, set to either 15 or 17 depending upon D26F. (Adjust the Word Counter to 15 words for 120 Column Printer, and to 17 words for 132 Column Printer.)

SC = 9: Access Memory.

1. "D" to "W" transfer.
2. Adjust Character Counter for proper character selection. (3 for 132 Column Printer and 7 for 120 Column Printer.)
3. Perform Memory Access.
4. Compare the two-section Word Count Field, five lower bits against the five upper bits. When equal, set D17F to 1.
5. Completion of Memory Access, SC + 1.

SC = 10:

1. Decrement Address Counter and test Memory Parity.
2. Set D26F to 0 unconditionally.
3. Transfer character pointed to by CC from "W" Register to Output Buffer. CC - 1.
4. Transfer Control to SC = 7.

SC = 7:

1. Insert blanks, set Output Buffer A to 1, and set Output Buffer 1, 2, 4, 8, B to 0 if D17F is reset. This signifies that Word Comparison was not detected when the comparison was made at SC = 9. Blanks will be inserted until such time as the two-section Word Count Field compares and D17F is set.
2. SC + 1.

SC = 8: On the initial entrance to this Sequence Count, the Character Counter will be equal to 2 for the 132 Column Printer; and 7 for the 120 Column Printer. The state of D17F will determine whether or not blanks or information will be sent to the Printer. On each succeeding Memory Access, blanks will be inserted until such time that Word Coincidence is detected and D17F is set to 1.

1. CC - 1.
2. With CC = 7, SC + 1.

NOTE

The Sequence Count will loop between SC = 9, 10, 7 and 8 until Word Counter = 0.

SC = 9:

1. If WC = 0, exit to SC = 11.

SC = 11:

1. Delay Sequence Count advancement until completion of Paper Motion. Then set D25F to 0.
2. Set D21F to 1 if at End-Of-Page.
3. SC + 1.

SC = 12:

1. Set Output Buffer B thru 1 to Line Printer B thru 1 if not at End-Of-Page.
2. SC + 1.

SC = 13:

1. Release Printer from I/O.
2. If not End-Of-Page, allow End-Of-Page Reset Level (EPRL).
3. SC + 1.

SC = 14:

1. Construct Result Descriptor.

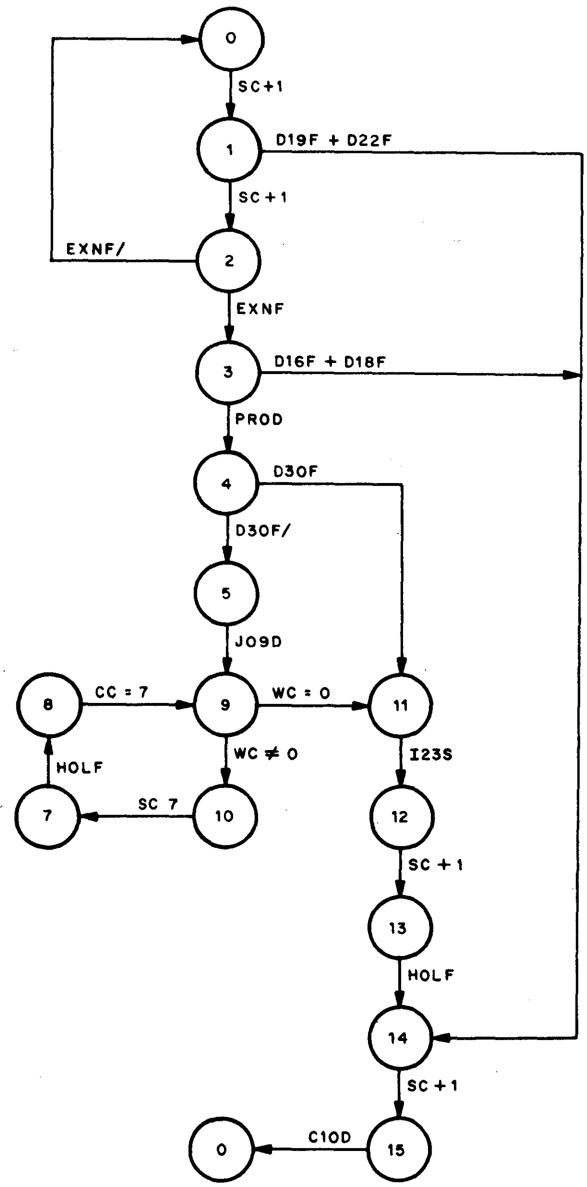



FIGURE 8.15-1
B5500 - 650 LPM PRINTER SEQUENCE COUNT STATE CHART

Installed in our 3 controllers 7/1/75 JH

| | | | |
|---|---|---|---|
| **Burroughs**<br>FIELD ENGINEERING<br>TECHNICAL OPERATIONS | RELIABILITY<br>IMPROVEMENT<br>NOTICE | SYSTEM SERIES<br>B5500/B5700 | No. 5282-010 |
| | | STYLE/MODEL<br>B5282 | PAGE<br>1 OF 1 |
| | | TOP UNIT NO.<br>1904 8370 & 1630 3125 | |
| STD. INSTALL. TIME<br>Up to 1/2 Hr. | UNITS AFFECTED<br>All | UNIT DESCRIPTION<br>I/O Control Model 3 & M3 File Protect | |
| TITLE<br>PREVENT RESULT DESCRIPTOR CONFLICT | | EI 30709/30710 | DATE<br>10-21-71 |

PREREQUISITE: None

PURPOSE: To prevent conflicting result descriptor when Datacom output message is an integral number of buffer lengths plus the group mark.

PARTS REQUIRED: None

INSTRUCTIONS:
Perform the following wiring changes:

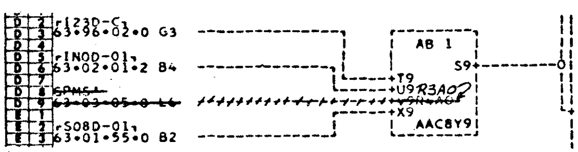
| Circuit No. | | | | |
|---|---|---|---|---|
| 6303050L66 | Delete | AAD3F6-Z2 | to | AAD3V1-Z2 |
| | Delete | AAB9X9-Z2 | to | AAC8V9-Z2 |
| | Delete | AAC8V9-Z1 | to | AAD3F6-Z1 |
| | Add | AAB9X9-Z2 | to | AAD3F6-Z1 |
| | Add | AAD3F6-Z2 | to | AAD3V1-Z2 |

Redline Circuit List to reflect the above changes.

Redline Logic Book Page 0119.10 as follows:

```
-JCL-    +
         +
         +  S08D-01 · INOD-01 · I23D-C [· GMPS'] <---- Delete
```

Redline Schematic 63.01.35.0 as follows:




10240802