Burroughs

B 5220

CENTRAL CONTROL

TECHNICAL MANUAL

B 5000 DATA PROCESSING SYSTEM

PRINTED IN U.S.A. 3/16/64 B 5220.51

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1. 10 ms LOAD delay multi for proper setting (Subject 3.4).
2. Excessive ripple in all DC supplies. (Refer to Subject 5.6 of the Power Supply Manual).

LUBRICATION

Fan Lubrication

Lubricate Rotron Muffin fans with Anderol L-826 using special oil injector.

Oil Injector . . . . . Pt. No. 11838588
Oil . . . . . Pt. No. 11838596

PROCEDURE

The exhaust fans are lubricated by inserting the Oil Injector needle through a self-sealing rubber cap located in the center of the motor hub.

Note that on most units a Gold Seal label is mounted over the rubber plug; this series of fans is called the Gold Seal series.

1. Fan grill, remove and clean as necessary.
2. Remove air from Oil Injector by holding the needle up and pressing on the plunger.
3. Place Oil Injector needle at the center of circle marked on the Gold Label (on the 034 series place needle approximately 1/8" from the edge of the rubber cap).
4. Position the needle at an angle of approximately 45° to the surface of the label and point it toward the center of the rubber cap.
5. Pierce the label and the concealed self-sealing rubber cap located under the label.
6. Insert the needle approximately 1/4".
7. Depress the plunger of the Oil Injector to allow approximately 1/16" of oil to escape. Rotating the fan will relieve air pressure and allow oil to flow into the oil chamber.

1.6 ANNUAL

CHECKS

1. Wiring and Cables.

    a. Check all wiring visually, paying special attention to voltage regulator area and any wires or cables carrying power.

SECTION 2

TROUBLESHOOTING

2.1 TEST SWITCHES AND INDICATORS

INTRODUCTION

The Functional Analysis of Central Control test switches and indicators is explained in the D & D Manual, Section 2.

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2.2 SPECIAL TOOLS

In addition to the normal tools provided for maintenance of the B 5220 Central Control Unit, the following special tools are also provided:

1. Diode-stick cutters
2. Wire-wrap tools
3. Cover-removal tool
4. Package handles

DIODE STICK CUTTING TOOL (P/N 11838109)

The Diode Sticks provided as spares are uncut. The diode stick cutter is a plier-type device which can be used to cut the diode sticks as needed. Care must be taken when using the cutter to keep from breaking the bond between the diodes or resistors and the common bus. The diode-stick tool must not be used for any other purpose.

WIRE UNWRAP TOOL (P/N 11838058)

The hand unwrapping tool (see Figure 2.2-1) is used when it is necessary to remove a wire from a pin. The tool has two ends; one end is for wires which are wrapped in a clock-wise direction; the other end is for wires which are wrapped in a counter-clock-wise direction. To use this tool, proceed as follows:

1. Determine the direction of wrap and insert the appropriate end of the tool over the pin.
2. Rotate the tool until the wire is sufficiently uncoiled so that it can be removed from the pin.

FIGURE 2.2-1 DUAL, RIGHT AND LEFT NO. 2 UNWRAPPING TOOL

WIRE WRAP TOOL (P/N 11838042)

The wire-wrap tool is a hand-wrapping tool and is shown in Figure 2.2-2. The tool will wrap a standard field change wire.

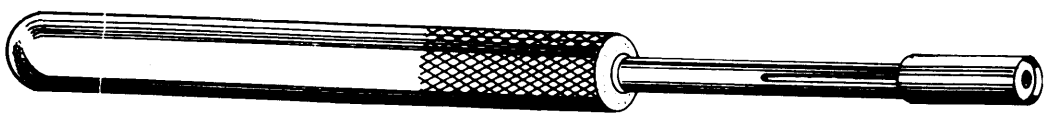


FIGURE 2.2-2 WIRE WRAP TOOL

Figure 2.2-3, A through F, shows the steps used to wrap a connection. If a wire was previously wrapped, the portion of the wire which was wrapped cannot be used again.

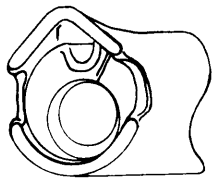
If the old wire is not long enough to strip off enough insulation to permit another wrap, a new wire must be routed in its place. To wrap a new wire, proceed as follows:

1. Remove the insulation from the end of the wire. Approximately 1 1/2" of wire is required for a six-turn connection of 24-gauge wire.

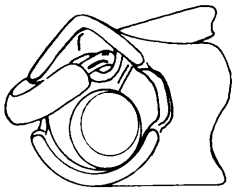
2. Place the tool over the wire as shown in Figure 2.2-3B.

3. Anchor the wire as shown in Figure 2.2-3C and insert the tool over the pin as shown in Figure 2.2-3D.

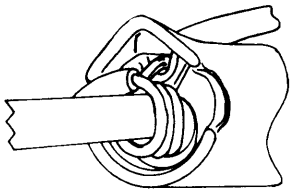
4. Rotate the tool in a clockwise direction. The wire will wrap around the pin as shown in Figure 2.2-3E and F. Too much pressure will cause the wire to bunch.



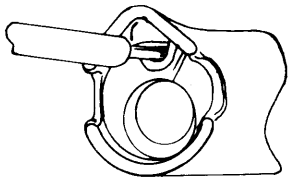
A-BIT AND SLEEVE



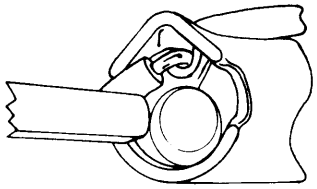
C-WIRE ANCHORING



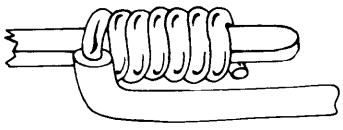
E-WRAPPING



B-WIRE INSERTION



D-TERMINAL INSERTION



F-FINISHED CONNECTION

FIGURE 2.2-3 WIRE WRAPPING

The following should be used as a guide when installing FCNs, or when making wire wrap changed in the field.

1. Number of turns - The minimum number of turns (per connection) of bare wire is FIVE, and the maximum number is SEVEN. The maximum number of turns of insulation preceding the bare wire is THREE for any connection.

2. Insufficient Insulation - Wire insulation shall be no greater than 1/32" from wire wrap connections.

3. Wire and Terminal Contact - The bare wire and terminal must make contact on all corners following the point at which the origin of the number of turns are counted.

4. Separation of Turns - Turns may have a maximum separation of 1/2 the thickness of wire being used to make the wrapped connection.

5. Excessive Tail Wire - The wire tail shall be construed as being "that end of bare wire which follows the last wrap." The wire tail shall be parallel to the terminal surface within 1/32".

6. Overlapping of Turns - This condition is caused when succeeding wraps overlap the ones previously made. If this condition exists, it will be necessary to make a new connection.

7. Clearance - There shall be at least 1/32" clearance between grid pattern connections, terminals, bare wire or components.

8. Height - The maximum clearance between the connector block and the first turn of the first connection shall be 1/16".

9. Height for Single Wire Wrap - The maximum height for a single wire wrap shall be 1/4".

10. Height for Two Wire Wraps - The maximum height for two wire wrap connections shall be 1/2".

11. Unwrapping - The wire wrap connection shall be capable of being unwrapped from the wire wrap terminal without breaking. The unwrapping operation shall be done with a standard unwrapping tool only, so as to insure the life of the wire wrap terminal.

12. Wire Re-use - IF A WIRE WAS PREVIOUSLY WRAPPED, THE PORTION OF THE WIRE WHICH WAS WRAPPED CANNOT BE USED AGAIN. If the old wire is not long enough to strip off enough insulation to permit another wrap, a new wire must be routed in its place. Soldering a wire wrapped connection directly at the wire wrapped terminal shall not be permitted at any time.

13. Terminal Re-use - Prior to rewrapping, the terminal shall be inspected for plating loss, corrosion or other damage. The evidence of any damage, plating loss or corrosion will in effect cause the wire connection not to maintain the high degree of quality and reliability which is required. The terminal, therefore, must be replaced with a new terminal.

COVER-REMOVAL TOOL (P/N 80551)

The cover-removal tool is a 3/8" Allen-Set-screw wrench. The short end is cut off to approximately 1/2" and a plastic handle is inserted on the long portion of the wrench.

PACKAGE HANDLES (P/N 77213)

Special non-conduction handles are provided for use in removing packages. These handles must be removed from the package before the gates are closed.

2.3 PRECAUTIONS

Adhere to the following steps to insure equipment safety.

1. Do not use a battery-buzzer for continuity checking. The buzzer current exceeds the maximum current rating for diodes and transistors in CC.

2. Do not use the first two low scales (X1 or X10) on the Triplet ohmmeter for continuity checking. On these scales, the meter current exceeds the maximum current rating for diodes and transistors in CC.

3. Do not remove packages or diode sticks when power is Up.

4. Care must be taken when using Scope or Jumper Clip Leads to prevent touching adjacent pins. Use Minigator Clips with insulators or the Wire Wrap Pin Probe Tip (Part No. 11838547).

5. Use extreme caution when working on the plug-in side of the panels. Avoid hitting packages when moving the scope.

6. Do not attempt to force a TRUE level with -12V.

7. A ground jumper may be used to force a FALSE level.

NOTE

Connect clip to the point to be grounded prior to making ground connection.

8. Do not pull Cable Plugs with POWER ON at either end of the cable.

9. Only soldering irons that have an isolation transformer may be used.

10. Scope ground - to prevent ground loops and noise interference, use only the ground clip on the scope probe. Attach it to a suitable ground as near as possible to the point being observed.

2.4 CLOCK CONTROL LOAD BUTTON

CHECKS

Refer to Figure 2.4-1 (Load Button Timing Chart) to aid in the check out of the LOAD logic.

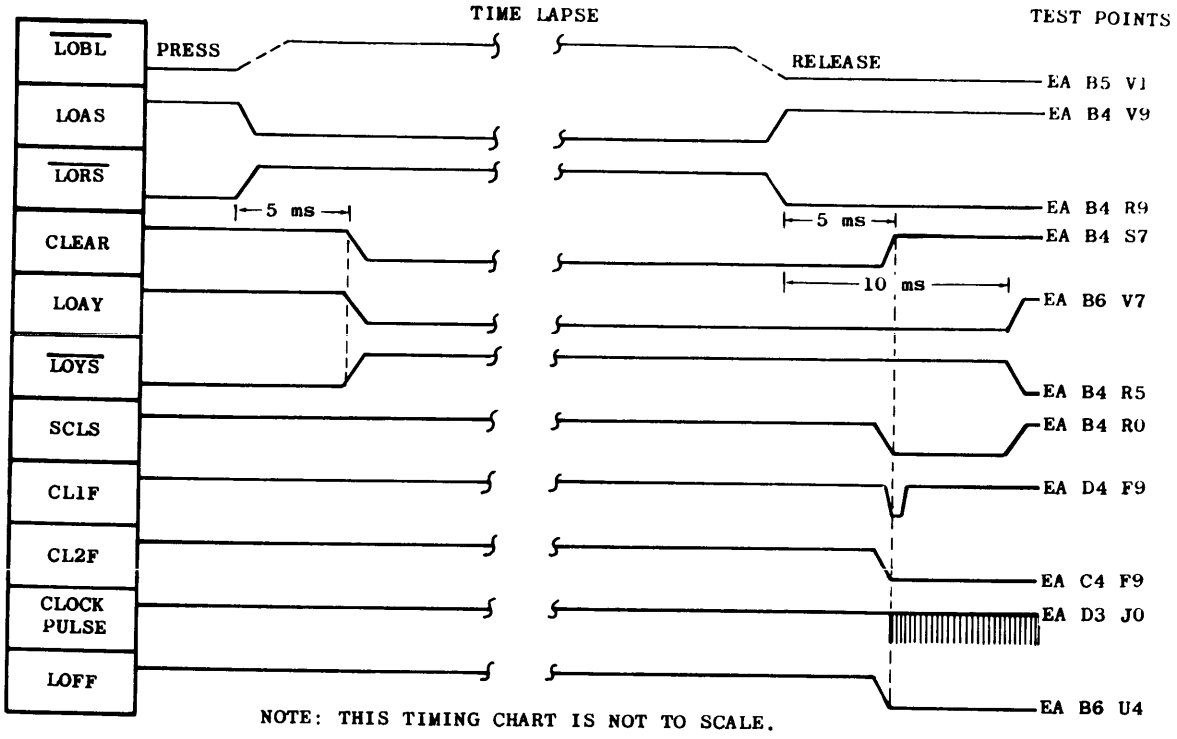


FIGURE 2.4-1 LOAD BUTTON TIMING CHART

The steps listed below should be taken to check the Clock Control Load Button Logic.

1. To check the CLEAR function of the LOAD logic, set a few flip-flops in the CC (CL1F and CL2F must be off). Pressing the LOAD button on the CC Display Panel will clear all flip-flops, releasing it will turn on LOFF and CL2F.

2. The Delay Multi LOAY (EA B6 V7), should be checked for proper delay.

3. Sync scope (positive) on LOAS (EA B4 V9) and measure the delay from the time LOAS goes false to the time LOAY goes false. Timing should be 10 ms.

4. Using the same sync (LOAS), scope SCIS (EA B4 R0) while pressing LOAD button. SCLS will be true for a period equal to the LOAY delay minus the CLEAR relay contacts delay. This time should be about 5 ms.

5. The LOAD button cannot be activated if Processor 1 is busy. This can be checked by testing the following two equations.

    1. + PA1L•PABUSL
    2. + PB1L•PBBUSL

NOTE

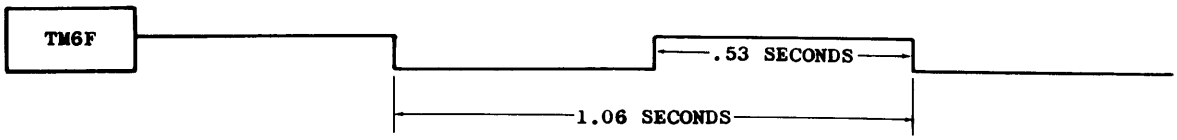
These equations are taken from page C006 of the CC Logic Book, IOAS input.

6. Check the 4 KCL inputs to LOFF making sure each interrupt clears it with a clock pulse.

2.5 CHECKOUT OF REAL TIME CLOCK

On the CC Display Panel, switch the Clock Mode switch to "NORMAL".

The Real Time Clock should be counting once every 16.6 ms. Scope the true output of TM6F (EA B5 F9). This is the "32 bit" flip-flop and should be going true every 1.06 seconds. See illustration below.



The proper complementing of TM6F will reflect the operation of the entire counter.

If counting seems erratic, switch the Clock Mode switch to "double pulse". Clear the Real Time counter register and pulse the counter with the Start Clock button.

A count may not be obtained with each depression of the Start button because the clock pulse must be ANDED with 60 cycles (TM0Y).

2.6 PHYSICAL ORIENTATION

INTRODUCTION

The Central Control Unit is an integral part of the B 5000 Main Frame. This frame is comprised of Processor, I/O, D & D, Central Control and Memory.

GENERAL RACK LAYOUT

The rack locations are shown in Figure 2.6-1. There are five racks in Central Control.

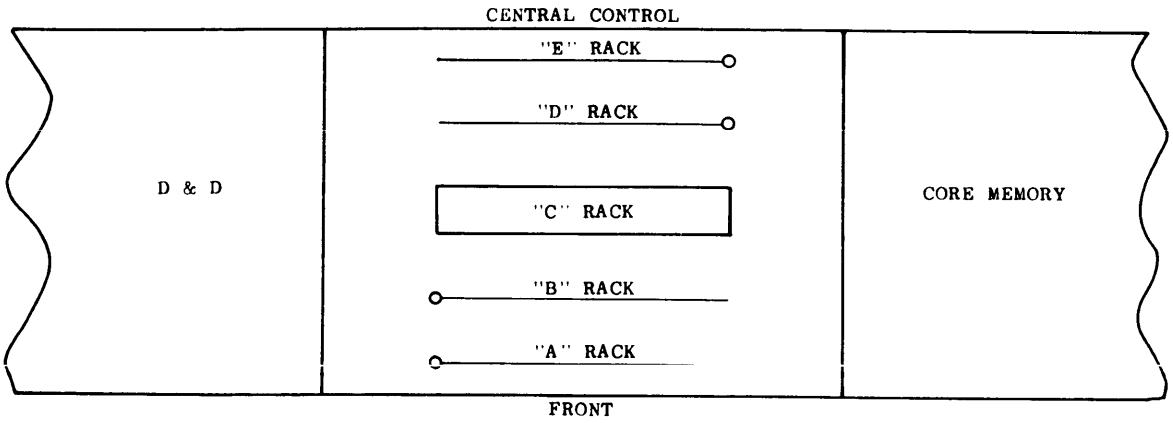


FIGURE 2.6-1 RACK LOCATIONS

Note that upon removal of the cover, the wiring side of the panel is exposed. The packages are found on the inside of the panel.

The C rack differs from the other racks and will be explained later. The remaining racks, A, B, D and E are devoted to Central Control Logic. Each of these racks have three frames, which are divided into two panels. Refer to Figure 2.6-2.

The layout of the rack, or gate as it is sometimes referred to, is shown with the orientation numbers used for reference. The numbers across the top of the rack are the column numbers used in referencing the location of packages. The letters in the large circles denote the panel letter. Notice that panels A, C and E are full panels utilizing all 10 columns, while panels B, D and F are half panels utilizing only five columns. Each panel is subdivided into four rows marked A, B, C and D. This subdividing locates a connector block which can hold four flip-flops or 20 diode sticks. The connector block is subdivided into strips of connectors which are designated by two coordinates. Across the top, the columns are marked 0 through 9, while along the side, the rows are lettered A through Y, with G, I, O and Q left out. Therefore the following location would have this meaning:

CONNECTOR BLOCK LOCATION, AND PIN LOCATION WITHIN THE CONNECTOR

AB C3 D4 is located approximately by block dot on Figure 2.6-2.

A = "A" Rack
B = "B" Panel
C = "C" Row
3 = 3rd Column
D = D Row of Connector Block
4 = Column of Connector Block

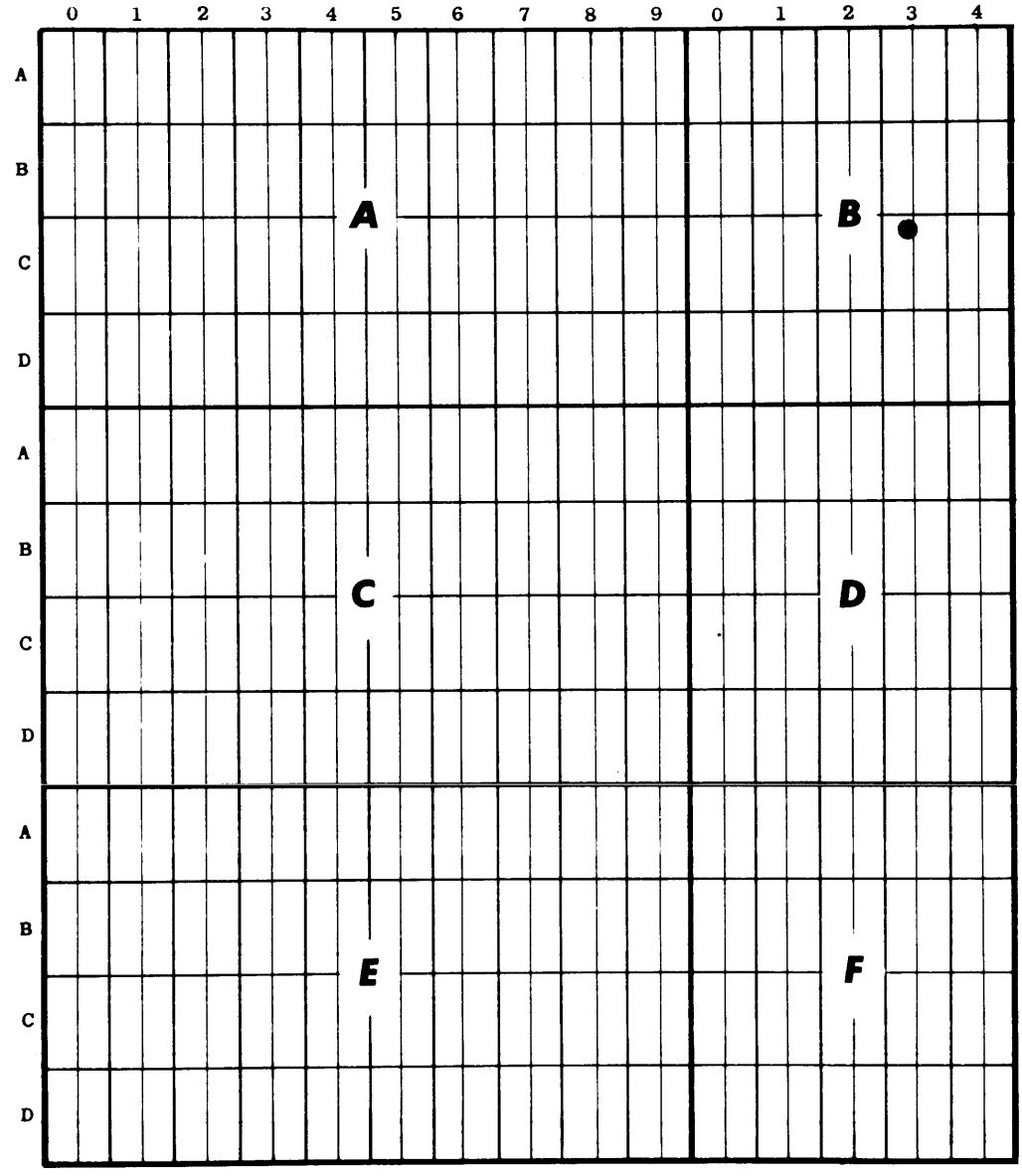


FIGURE 2.6-2 PANEL ORIENTATION (WIRING SIDE)

Because of the interaction of the various modules and wiring, the logical gates may not, mechanically, be located near each other. This makes it difficult to localize a certain area on the panels and assign it to a specific group of logics. The frames are fairly well assigned with the assignments shown in Figure 2.6-3.

"A" RACK

On the "A" rack, panels A and B contain the crosspoint flip-flops with the associated logic necessary to select the flip-flops.

Panels C, D, E and F contain part of the associated logic for the Memory Read Exchange. This includes the Memory Read Crosspoint Drivers.

"B" RACK

All panels of the "B" rack contain the Memory Write Exchange Crosspoint Drivers and the associated logical gating necessary to select them when the crosspoint flip-flops are set.

"C" RACK

This rack is a fixed unit within the cabinet for Central Control. The top section of this rack contains the Power Pack, which is a DC voltage regulator for the -1.2V, -4.5V, and the -12V supply to the Central Control and Display and Distribution units. The voltage regulator is described in the B 5000 System Power Supply Manual.

The lower section of this rack contains 12 troughs which are used to convey interconnecting cables from one cabinet to another.

"D" RACK

Panel A of the "D" rack contains the I/O and peripheral designate gating for I/O Exchange.

Part of Panel A and all of Panel B contain part of the Non-Tape Control and Information lines logic.

Panels C, D, E and F contain the rest of the logic for Non-Tape Control and Information lines.

"E" RACK

Panels A and B of the "E" rack contain the Incandescent Driver packages for the system, the Load Control, System Clock and Clock Control, the Interrupt Control logics, Interrupt Address Register and I/O selection logics.

Panels C, D, E and F contain the logic for Magnetic Tape Control and information lines.

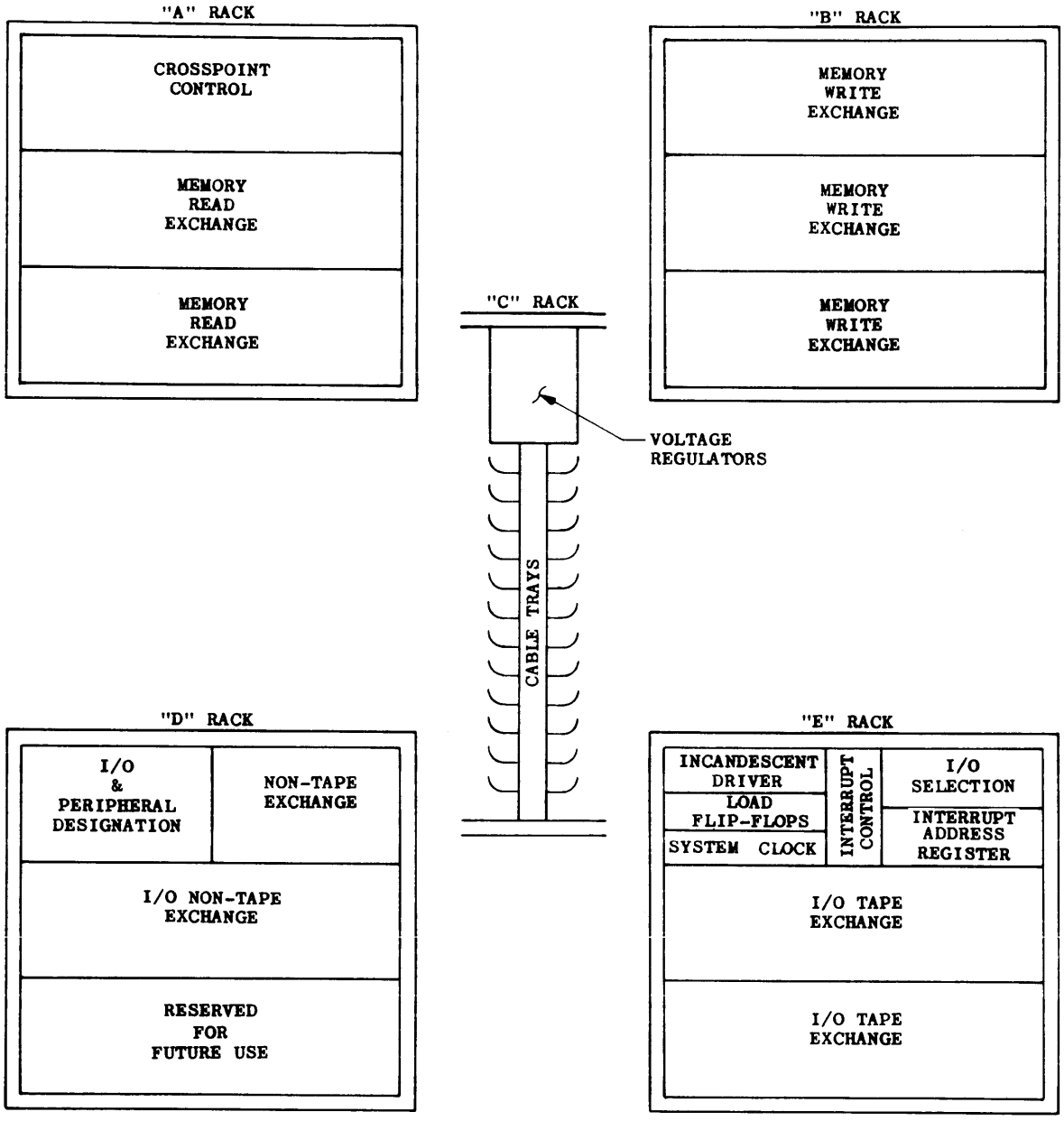


FIGURE 2.6-3 CENTRAL CONTROL RACK LAYOUT

2.7 RIN INDEX

RIN INDEX FOR THE B 5220 CENTRAL CONTROL UNIT, MODEL 1 (78493)

RIN NO.	INSTAL. TIME IN HOURS	PRE-REQUISITE	UNITS EFFECTED	DESCRIPTION
5005	2.0		102 ⇒ 113	Improved manner with which the cables are secured.
5010	2.0		102 ⇒ 113	Installation of adhesive identification labels on each cable connector.
5012	2.0		102 ⇒ 113	Change pulse per cycle rate at which the Real Time Clock is counted.
5019	0.5		102 ⇒ 113	Change clock cables between Central Control and Memory.
5028	0.5		102 ⇒ 113	Extends lower limit of the -4.5V regulator.
5029	0.5		102 ⇒ 113	Installation of cable supports to prevent pinching of cables.
5040	0.5		102 ⇒ 113	Correct the termination of P31S and P31S'.
5041	10.0		102 ⇒ 113	Implements backspace lines for Paper Tape Reader.
5043	4.0		102 ⇒ 113	Removes a portion of the frame to relieve cable stress.
5052	1.0		102 ⇒ 113	Replace clock cables with standard types.
5072	1.5		102 ⇒ 113	"A" Rack Document release and unused wiring removal.
5072S1	0.5	corrects 5072	102 ⇒ 113	(same as RIN 5072)
5076	0.1 per cable		102 ⇒ 113	Key pin support for all yellow and green single key pin cable connectors.
5078	1.0		102 ⇒ 113	Change to double driver package to eliminate oscillations.
5079	0.5		102 ⇒ 113	Release of updated documents for Central Control "E" Rack.

RIN NO.	INSTAL. TIME IN HOURS	PRE-REQUISITE	UNITS EFFECTED	DESCRIPTION
5079S1	2.5	5079	102 ⇒ 113	Change Stick cuts to conform with Documents released by RIN 5079.
5091	1.0	5103 5106	102 ⇒ 113	Provide additional cables for exchanging a B 5000 Processor to a B 5500.
5094	4.0		102 ⇒ 113	Plug-in heatsink replacement to prevent the shorting of the collectors in common heatsinks.
5094S1	1.0	5094	102 ⇒ 113	Supply transistors for installation of RIN 5094.
5100	4.0		102 ⇒ 113	Provide a quad connector retaining device to insure proper seating of the connector.
5103	7.0	5041	102 ⇒ 113	Installation of new cable connector during re-routing of peripheral signal lines.
5106	28.5	5103	102 ⇒ 113	Installation of re-routed peripheral ready lines for Interrogate operator, plus change to External Interrupt Priority.
5107	1.0	5106	102 ⇒ 113	Removal of PRRS termination. These signals are now terminated in the Processor.
5113	2.0	5114	102 ⇒ 113	Provide a $\overline{\text{single pulse}}$ or $\overline{\text{double pulse}}$ level to the 4μs Memory.
5124	0.5		102 ⇒ 113	Installation of a washer on the crystal pins, of the oscillator, to eliminate possible shorting.

RIN INDEX FOR THE B 5220 CENTRAL CONTROL UNIT, MODEL 2 (11975323)

RIN NO.	INSTAL. TIME IN HOURS	PRE-REQUISITE	UNITS EFFECTED	DESCRIPTION
5028	0.5		114 ⇒ UP	Extends lower limit of the -4.5V regulator.
5031	4.0		114 ⇒ UP	Add designate of Disk File for priority resolution and interrupts.
5043	4.0		114 ⇒ UP	Removes a portion of the frame to relieve cable stress.
5072	1.5		114 ⇒ UP	"A" Rack Document release and unused wiring removal.
5072S1	0.5	corrects 5072	114 ⇒ UP	(same as RIN 5072)
5076	0.1 per cable		114 ⇒ UP	Key pin support for all yellow and green single key pin cable connectors.
5078	1.0		114 ⇒ UP	Change to double driver package to eliminate oscillations.
5079	0.5		114 ⇒ UP	Release of updated documents for Central Control "E" Rack.
5079S1	2.5	5079	114 ⇒ UP	Change Stick cuts to conform with Documents released by RIN 5079.
5082	10.0		114 ⇒ UP	Correct Inquiry signal cable; correct logic to 06FW2L' and I3I250; add missing -4.5V and -12V.
5083	1.0	5031 5082	114 ⇒ UP	Add designate for Disk File for priority resolution and interrupts.
5084	10.0	5083	114 ⇒ UP	Implements backspace lines for Paper Tape Readers.
5085	1.5	5084	114 ⇒ UP	Removal of 16INPL input logic from I3I07D.
5091	1.0	5085	114 ⇒ UP	Provide additional cables for exchanging a B 5000 Processor to a B 5500.

RIN NO.	INSTAL. TIME IN HOURS	PRE-REQUISITE	UNITS EFFECTED	DESCRIPTION
5094	4.0		114 ⇒ UP	Plug-in heatsink replacement to prevent the shorting of the collectors in common heatsinks.
5094S1	1.0	5094	114 ⇒ UP	Supply transistors for installation of RIN 5094.
5100	4.0		114 ⇒ UP	Provide a quad connector retaining device to insure proper seating of the connector.
5102	8.5	5085	114 ⇒ UP	Installation of new cable connector during re-routing of peripheral signal lines.
5106	28.5	5102	114 ⇒ UP	Installation of re-routed peripheral ready lines for Interrogate operator, plus change to External Interrupt Priority.
5107	1.0	5106	114 ⇒ UP	Removal of PRRS termination. These signals are now terminated in the Processor.
5113	2.0	5114	114 ⇒ UP	Provide a $\overline{\text{single pulse}}$ or $\overline{\text{double pulse}}$ level to the 4μs Memory.
5124	0.5		114 ⇒ UP	Installation of a washer on the crystal pins, of the oscillator, to eliminate possible shorting.
5127	0.5		114 ⇒ UP	Correct an erroneous part number callout in Module Locator.

SECTION 3

ADJUSTMENTS

3.1 INTRODUCTION

This section contains the necessary instructions for making all adjustments within the Central Control unit.

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3.2 CLOCK PULSE WIDTH

The following steps should be taken to adjust the Clock Pulse Width:

1. With the Clock Mode switch in the "single pulse" position, sync scope (negative) on the leading edge of SCLS, EA B4 R0. Scope the local Clock Driver at EA B8 P7. When the START button is pressed, observe for a single pulse.

2. Change the Clock Mode to "double pulse" position. With the same sync and scope conditions as above, press the START button and observe for two pulses 1 μs apart.

3. Check the Master Oscillator for a 1 megacycle square wave by switching the Clock Mode to "normal" and pressing the START button while scoping the output of the Master Oscillator at EA D4 S2. A 1 megacycle pulse train should be present. (Refer to Figures 3.2-1 and 3.2-2).

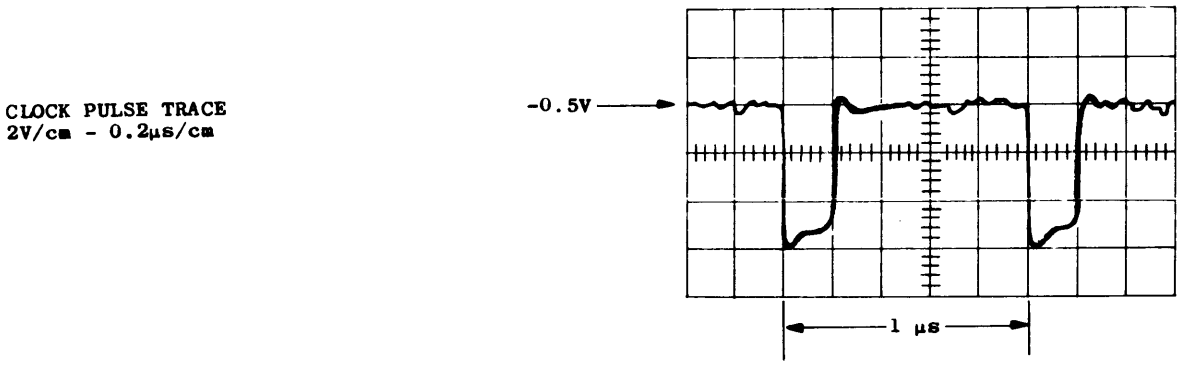

FIGURE 3.2-1 ONE MEGACYCLE PULSE TRAIN

4. Set the pulse width, (at the -2 volt level) to .155 microseconds by adjusting the pot on the DRBLs using Figure 3.2-2.

SCOPE POINT	POTENTIOMETER LOCATION
EA C3 C0	EA C3 A2
EA D3 C0	EA D3 A2

SCOPE POINT	POTENTIOMETER LOCATION
EA C3 R0	EA C3 N2
EA D3 R0	EA D3 N2

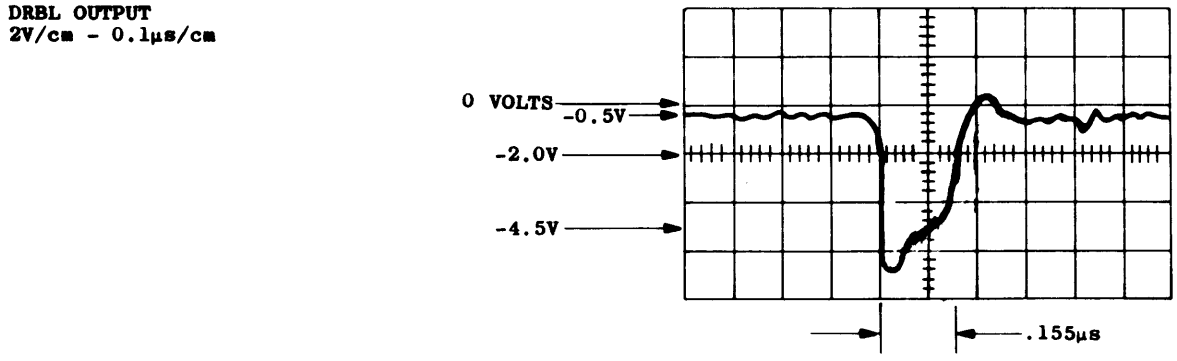

FIGURE 3.2-2 DRBL WAVE SHAPE AND ADJUSTMENT TABLE

3.3 VARIABLE BIAS

The following steps should be taken to adjust the Variable Bias:

1. Check the Master Oscillator output for a 1 megacycle square wave.

2. With the Clock Mode switch in "normal", press the START button and scope the output of the local clock driver, MCLD-EA (Pin EA B8 P7). A 1 megacycle pulse train should be present. (Refer to Figure 3.2-1).

3. Set the false level of the clock pulse to -.5V by adjusting the variable bias package at EA C8 A7.

4. Move the scope probe to the output of the other local clock driver, MCLD-AA (Pin AA B6 P7). Set the false level to -.5V by adjusting the variable bias at AA B7 N2. (Refer to Figure 3.3-1).

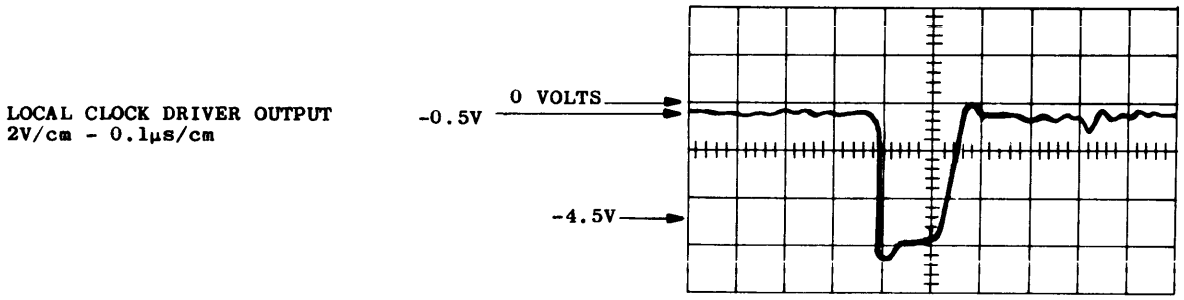

FIGURE 3.3-1 LOCAL CLOCK DRIVER WAVE SHAPE

3.4 DELAY MULTI

Figure 3.4-1 shows all pulses concerned with START Button Timing and includes each of the switch positions. If trouble is suspected in this area, Figure 3.4-1 will be of real value, but for DELAY adjustments, only the following steps are necessary.

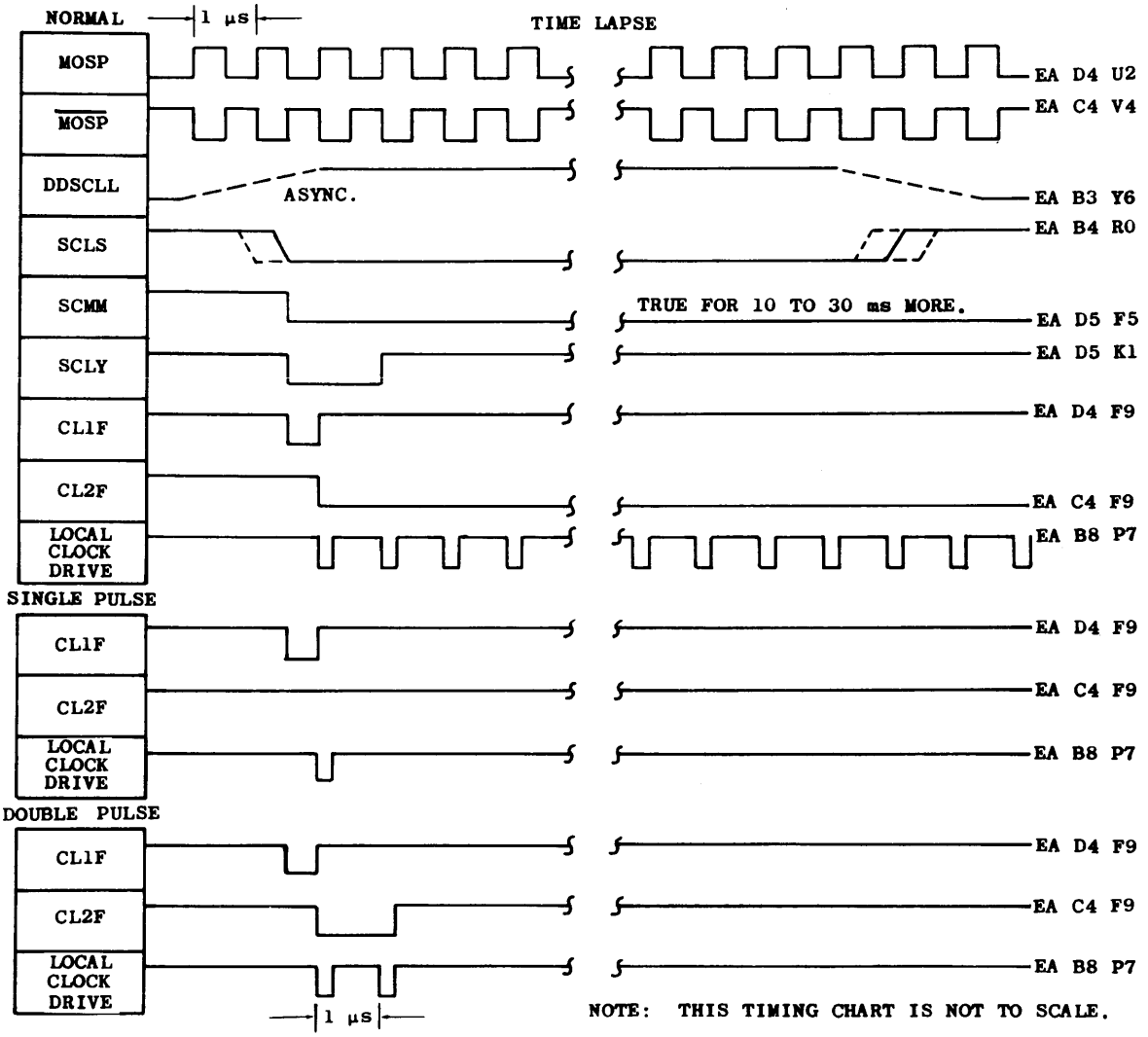

FIGURE 3.4-1 START BUTTON TIMING CHART

1. To adjust Delay Multi LOAY, EA B6 V7, sync scope (positive) on LOAS, EA B4 V9. Measure the delay from the time LOAS goes false to the time LOAY goes false. This should be about 10 ms but is not critical.

2. Using the same sync, scope SCLS at EA B4 R0 while pressing the LOAD button. SCLS should be true for a period equal to the LOAY delay minus the CLEAR relay contacts delay. This time should be about 5 ms.

NOTE

Be sure to use the LOAD button to start the checks as LOAY will not be obtained from using the START button.

3.5 DELAYED CLOCK PULSE

To adjust the delayed clock pulse:

1. Place the "A" probe on the normal clock at AAB6P7.
2. Place "B" probe on the delayed clock at AAC7J0.
3. Sync EXTERNAL-NEGATIVE on the normal clock at AAB6P7.
4. Adjust the DRSB (AAC7N2) for .5 usec delay between the leading edges of the normal and the delayed clock. See Figure 3.5-1.
5. Adjust the MUFW (AAC7A2) for a delayed clock width of .155 usec at the -2.0 volt level.
6. Set the false level to -.5V by adjusting the VB package at (AAC6A7).

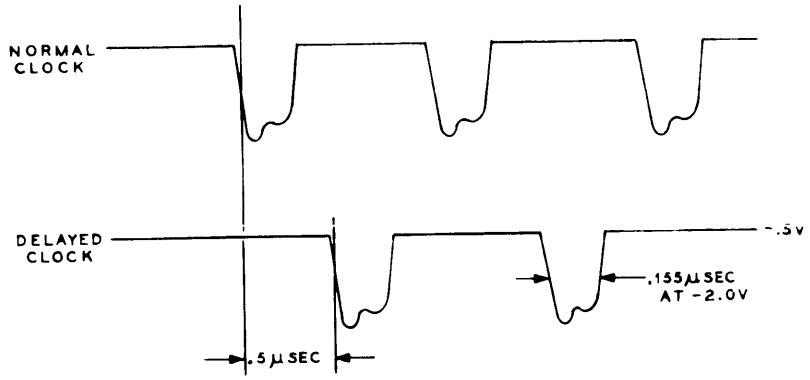

FIGURE 3.5-1 DELAYED CLOCK PULSE

Section 7.2 contains a functional description of the delayed clock.

SECTION 4

ASSEMBLY AND DISASSEMBLY

4.1 VOLTAGE REGULATOR

Refer to Section 4 of the Power Supply Manual for the procedure to disassemble and assemble the Voltage Regulator.

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4.2 WIRE WRAP PINS

REMOVAL

1. Remove wires with unwrapping tool.
2. If pin is bent, straighten it with long nose pliers.
3. Push on pin from the wire side with long nose pliers. As soon as the pin clears the block (package side), grasp the pin with the pliers and pull it out.
4. If the pin is broken off flush with the pin block, use a small drift punch or another pin held with the pliers to drive the pin out.

REPLACEMENT

1. Insert the pin in the block from the package side of the gate. Make sure that the pin is inserted correctly (the contact side of the pin points away from the slot on the side of the pin hole).
2. Take the long-nose pliers and pull on the pin from the wire side until the pin is even with adjacent pins. Do not pull it too far or the pin block may be damaged.

NOTE

The M row pins are U shaped and do not extend through to the package side.

4.3 PACKAGES

INSTALLATION AND REMOVAL

1. All parallel plate packages with the exception of the Local Clock Drivers will be fitted with a permanent handle for insertion and extraction.

2. Diode and resistor sticks will have a tool provided for insertion and extraction.

CAUTION

This tool must be removed before the gate is closed or the package may be damaged.

WARNING

Power must be OFF before removing any element.

SECTION 5

INSTALLATION

✓5.1 INTRODUCTION

The installation and check out of the Central Control Unit will follow the check out of primary power and cabinet regulators as described in the Power Supply Manual, Section 5.

All of the cables connecting to and used within Central Control are listed in Subject 5.2 of this manual.

The inter-gate cables in the latter part of the listing have already been installed, and are listed for reference only.

The cable listing is for a maximum system. However, those cables for units not part of the customer system will not be shipped.

To add new units to a system, refer to Subject 5.5.

✓Changes or additions since last issue.

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5.2 POWER AND INFORMATION CABLING

POWER CABLES

Previously installed cables for power checkout should include those numbered: 25-23, 25-32, 25-41 adn 209.

To complete the power wiring, the following cables should be installed: 25-11, 25-12, 225, 226, 231, 254 and 255.

Refer to the cable list (Table 5.2-1) for location and routing. When completed, check off all of the cables installed up to this time.

INFORMATION CABLES

The remaining CC cables are for information and control purposes. Install the cables in the order listed, follow the tray routing indicated and check off each cable as it is installed.

TABLE 5.2-1 INTER-UNIT CABLE LIST

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
1-0A	MEMORY WRITE, ADD EXCHANGE	CC	BA A0 A7	MEM-0	AJ J1 A2	3R
1-0B	MEMORY WRITE, ADD EXCHANGE	CC	BA A0 N7	MEM-0	AJ J1 N2	3R
1-1A	MEMORY WRITE, ADD EXCHANGE	CC	BA B0 A7	MEM-1	AJ J1 A2	4R
1-1B	MEMORY WRITE, ADD EXCHANGE	CC	BA B0 N7	MEM-1	AJ J1 N2	4R
1-2A	MEMORY WRITE, ADD EXCHANGE	CC	BA C0 A7	MEM-2	AJ J1 A2	3R
1-2B	MEMORY WRITE, ADD EXCHANGE	CC	BA C0 N7	MEM-2	AJ J1 N2	3R
1-3A	MEMORY WRITE, ADD EXCHANGE	CC	BC A0 A7	MEM-3	AJ J1 A2	8R
1-3B	MEMORY WRITE, ADD EXCHANGE	CC	BC A0 N7	MEM-3	AJ J1 N2	8R
1-4A	MEMORY WRITE, ADD EXCHANGE	CC	BC B0 A7	MEM-4	AJ J1 A2	4R
1-4B	MEMORY WRITE, ADD EXCHANGE	CC	BC B0 N7	MEM-4	AJ J1 N2	4R
1-5A	MEMORY WRITE, ADD EXCHANGE	CC	BC C0 A7	MEM-5	AJ J1 A2	8R
1-5B	MEMORY WRITE, ADD EXCHANGE	CC	BC C0 N7	MEM-5	AJ J1 N2	8R
1-6A	MEMORY WRITE, ADD EXCHANGE	CC	BE A0 A7	MEM-6	AJ J1 A2	5R
1-6B	MEMORY WRITE, ADD EXCHANGE	CC	BE A0 N7	MEM-6	AJ J1 N2	5R
1-7A	MEMORY WRITE, ADD EXCHANGE	CC	BE B0 A7	MEM-7	AJ J1 A2	9R
1-7B	MEMORY WRITE, ADD EXCHANGE	CC	BE B0 N7	MEM-7	AJ J1 N2	9R
2-0A	MEMORY READ EXCHANGE	MEM-0	AJ K1 A7	CC	AC A0 A2	3F
2-0B	MEMORY READ EXCHANGE	MEM-0	AJ K1 N7	CC	AC A0 N2	3F
2-1A	MEMORY READ EXCHANGE	MEM-1	AJ K1 A7	CC	AC B0 A2	6F
2-1B	MEMORY READ EXCHANGE	MEM-1	AJ K1 N7	CC	AC B0 N2	6F
2-2A	MEMORY READ EXCHANGE	MEM-2	AJ K1 A7	CC	AC C0 A2	5R
2-2B	MEMORY READ EXCHANGE	MEM-2	AJ K1 N7	CC	AC C0 N2	5R
2-3A	MEMORY READ EXCHANGE	MEM-3	AJ K1 A7	CC	AC D0 A2	7F
2-3B	MEMORY READ EXCHANGE	MEM-3	AJ K1 N7	CC	AC D0 N2	7F
2-4A	MEMORY READ EXCHANGE	MEM-4	AJ K1 A7	CC	AE A0 A2	4R

Continued on next page

Table 5.2-1 Power Cables

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
2-4B	MEMORY READ EXCHANGE	MEM-4	AJ K1 N7	CC	AE A0 N2	4R
2-5A	MEMORY READ EXCHANGE	MEM-5	AJ K1 A7	CC	AE B0 A2	8F
2-5B	MEMORY READ EXCHANGE	MEM-5	AJ K1 N7	CC	AE B0 N2	8F
2-6A	MEMORY READ EXCHANGE	MEM-6	AJ K1 A7	CC	AE C0 A2	6F
2-6B	MEMORY READ EXCHANGE	MEM-6	AJ K1 N7	CC	AE C0 N2	6F
2-7A	MEMORY READ EXCHANGE	MEM-7	AJ K1 A7	CC	AE D0 A2	9F
2-7B	MEMORY READ EXCHANGE	MEM-7	AJ K1 N7	CC	AE D0 N2	9F
3-1	I/O INPUT LINES	CC	EC A0 A2	I/O-1	AC D0 A7	3F
3-2	I/O INPUT LINES	CC	EC B0 A2	I/O-2	AC D0 A7	3R
3-3	I/O INPUT LINES	CC	EC C0 A2	I/O-3	AC D0 A7	5R
3-4	I/O INPUT LINES	CC	EC D0 A2	I/O-4	AC D0 A7	5F
4-1A	I/O MEMORY READ EXCHANGE	CC	AC C0 A7	I/O-1	AE A0 N2	7R
4-1B	I/O MEMORY READ EXCHANGE	CC	AC C0 N7	I/O-1	AE B0 N2	7R
4-2A	I/O MEMORY READ EXCHANGE	CC	AC D0 A7	I/O-2	AE A0 N2	7R
4-2B	I/O MEMORY READ EXCHANGE	CC	AC D0 N7	I/O-2	AE B0 N2	7R
4-3A	I/O MEMORY READ EXCHANGE	CC	AE C0 A7	I/O-3	AE A0 N2	10R
4-3B	I/O MEMORY READ EXCHANGE	CC	AE C0 N7	I/O-3	AE B0 N2	10R
4-4A	I/O MEMORY READ EXCHANGE	CC	AE D0 A7	I/O-4	AE A0 N2	10F
4-4B	I/O MEMORY READ EXCHANGE	CC	AE D0 N7	I/O-4	AE B0 N2	10F
5-1A	I/O MEMORY WRITE EXCHANGE	I/O-1	AE C0 N7	CC	BA C0 A2	5R
5-1B	I/O MEMORY WRITE EXCHANGE	I/O-1	AE D0 A7	CC	BA C0 N2	5R
5-2A	I/O MEMORY WRITE EXCHANGE	I/O-2	AE C0 N7	CC	BC A0 A2	5R
5-2B	I/O MEMORY WRITE EXCHANGE	I/O-2	AE D0 A7	CC	BC A0 N2	5R
5-3A	I/O MEMORY WRITE EXCHANGE	I/O-3	AE C0 N7	CC	BC C0 A2	7R
5-3B	I/O MEMORY WRITE EXCHANGE	I/O-3	AE D0 A7	CC	BC C0 N2	7R
5-4A	I/O MEMORY WRITE EXCHANGE	I/O-4	AE C0 N7	CC	BC C0 A2	10R
5-4B	I/O MEMORY WRITE EXCHANGE	I/O-4	AE D0 A7	CC	BE C0 N2	10R
6-1	I/O OUTPUT LINES	I/O-1	AC B0 A7	CC	EC A0 N2	3F
6-2	I/O OUTPUT LINES	I/O-2	AC B0 A7	CC	EC B0 N2	3F
6-3	I/O OUTPUT LINES	I/O-3	AC B0 A7	CC	EC C0 N2	5R
6-4	I/O OUTPUT LINES	I/O-4	AC B0 A7	CC	EC D0 N2	5F
7-A	INTERRUPT & CONTROL	CC	EA C0 A7	PA	DA C0 N2	8F
7-B	INTERRUPT & CONTROL	CC	EA C0 N7	PB	DA C0 N2	2F
8-AA	Pk MEMORY WRITE EXCHANGE	PA	DE C0 N7	CC	BA A0 A2	7F
8-AB	Pk MEMORY WRITE EXCHANGE	PA	DC B0 A7	CC	BA A0 N2	5F
8-BA	Pk MEMORY WRITE EXCHANGE	PB	DE C0 N7	CC	BE A0 A2	8F
8-BB	Pk MEMORY WRITE EXCHANGE	PB	DC B0 A7	CC	BE A0 N2	5F
9-AA	Pk MEMORY READ EXCHANGE	CC	AC A0 A7	PA	EE D0 A2	7F
9-AB	Pk MEMORY READ EXCHANGE	CC	AC A0 N7	PA	EE C0 N2	5F
9-BA	Pk MEMORY READ EXCHANGE	CC	AE A0 A7	PB	EE D0 A2	8F
9-BB	Pk MEMORY READ EXCHANGE	CC	AE A0 N7	PB	EE C0 N2	5F
10-A	INTERRUPT & CONTROL	PA	EA D0 A7	CC	EA C0 A2	7F
10-B	INTERRUPT & CONTROL	PB	EA D0 A7	CC	EA C0 N2	3F
11	PAPER TAPE - RDR/PUNCH SIGNAL	CC	DC A0 N7	D & D	DD J8	5F
12-1	MAGNETIC TAPE - TTU - A	CC	EE A0 A2	D & D	DE L1	7F
12-2	MAGNETIC TAPE - TTU - B	CC	EC D0 N7	D & D	DE L2	8R
12-3	MAGNETIC TAPE - TTU - C	CC	EE A0 N2	D & D	DE L3	7F
12-4	MAGNETIC TAPE - TTU - D	CC	EE A0 N7	D & D	DE L4	8R

Continued on next page

(Table 5.2-1 Continued)

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
12-5	MAGNETIC TAPE - TTU - E	CC	EE B0 A2	D & D	DE L5	7F
12-6	MAGNETIC TAPE - TTU - F	CC	EE B0 A7	D & D	DE L6	9F
12-7	MAGNETIC TAPE - TTU - H	CC	EE B0 N2	D & D	DE L7	9F
12-8	MAGNETIC TAPE - TTU - J	CC	EE B0 N7	D & D	DE L8	9F
12-9	MAGNETIC TAPE - TTU - K	CC	EE C0 A2	D & D	DE M1	11F
12-10	MAGNETIC TAPE - TTU - L	CC	EE C0 A7	D & D	DE M2	10F
12-11	MAGNETIC TAPE - TTU - M	CC	EE C0 N2	D & D	DE M3	11F
12-12	MAGNETIC TAPE - TTU - N	CC	EE C0 N7	D & D	DE M4	10F
12-13	MAGNETIC TAPE - TTU - P	CC	EE D0 A2	D & D	DE M5	11F
12-14	MAGNETIC TAPE - TTU - R	CC	EE D0 A7	D & D	DE M6	10F
12-15	MAGNETIC TAPE - TTU - S	CC	EE D0 N2	D & D	DE M7	11F
12-16	MAGNETIC TAPE - TTU - T	CC	EE D0 N7	D & D	DE M8	10F
13	PRINTER KEYBOARD SIGNAL	CC	DC A0 A2	D & D	DD J1	3F
15-1	100/500 CPM PUNCH SIGNAL	CC	DC C0 A2	D & D	DD K1	5F
17-1	#1 200/800 CPM READER SIGNAL	CC	DC C0 N2	D & D	DD K3	5F
17-2	#2 200/800 CPM READER SIGNAL	CC	DC C0 N7	D & D	DD K4	5F
19	INQUIRY SIGNAL	CC	DC A0 A7	D & D	DD J2	4F
20-1	#1 PRINTER SIGNAL	CC	DC D0 A2	D & D	DD K5	6F
20-2	#2 PRINTER SIGNAL	CC	DC D0 A2	D & D	DD K7	6F
21	PAPER TAPE PUNCH SIGNAL	CC	DC B0 A7	D & D	DD J6	4F
22	PAPER TAPE READ SIGNAL	CC	DC D0 A7	D & D	DD K2	8F
23-1	#1 DRUM SIGNAL	CC	DC B0 A2	D & D	DD J5	4F
23-2	#2 DRUM SIGNAL	CC	DC B0 N2	D & D	DD J7	4F
25-11	(#00 AWG) GROUND	D & D	DA J1 03	CC	CA K1 07	2R
25-12	(#00 AWG) GROUND	D & D	DA J1 03	CC	CU K1 07	2R
25-23	(#10 AWG) +20V	D & D	DB L4 05	CC	CS K1 12	1F
25-32	(#12 AWG) +50V	D & D	DB L1 05	CC	CT N2 04	1F
25-41	(#12 AWG) -33V	D & D	DB J2 05	CC	CT N2 01	1R
37	CC INDICATOR INPUT	CC	EA A0 A2	D & D	AH J1	2F
38	CC INDICATOR INPUT	CC	AA A0 A2	D & D	AH K1	2F
39	CC INDICATOR INPUT & MANUAL CONTROL	CC	AA A0 N2	D & D	AH L1	2F
40	CC MANUAL CONTROL	D & D	AH M1	CC	EA A0 N2	2F
41	CC MANUAL CONTROL	D & D	AH N1	CC	AA B0 A2	2F
42	CC MISCELLANEOUS	D & D	AH P1	CC	EA B0 A2	2F
140	POWER GATE "A" - D & D	CC	CS 07	D & D	AE A0 A7	1R
170	CLOCK CABLE I/O-1	CC	EA D2 Y6	I/O-1	AA C7 Y4	2R
					AC B8 L4	
					AE C6 Y9	
171	CLOCK CABLE I/O-2	CC	EA D2 Y7	I/O-2	AA C7 Y4	2R
					AC B8 L4	
					AE C6 Y9	
172	CLOCK CABLE I/O-3	CC	EA D2 Y8	I/O-3	AA C7 Y4	2R
					AC B8 L4	
					AE C6 Y9	
173	CLOCK CABLE I/O-4	CC	EA D2 Y9	I/O-4	AA C7 Y4	2R
					AC B8 L4	
					AE C6 Y9	
175	PA CLOCK CABLE "A" RACK	CC	EA C2 L6	PA	AA C5 L9	2R

Continued on next page

(Table 5.2-1 Continued)

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
175	PA CLOCK CABLE "A" RACK	CC	EA C2 L6	PA	AC C5 L9	2R
					AE C5 L9	
176	PA CLOCK CABLE "B" RACK	CC	EA C2 L7	PA	BA C6 L9	2R
					BC C6 L9	
					BE C5 L9	
177	PA CLOCK CABLE "D" RACK	CC	EA C2 L8	PA	DA C6 L9	2R
					DC C6 L9	
					DE C6 L9	
178	PA CLOCK CABLE "E" RACK	CC	EA C2 L9	PA	EA B6 Y9	2R
					EE B6 Y9	
179	PA CLOCK CABLE "J" RACK	CC	EA C2 L5		JC C6 L9	
					JE C6 L9	
180	PB CLOCK CABLE "A" RACK	CC	EA C2 Y6	PB	AA C5 L9	2R
					AC C5 L9	
					AE C5 L9	
181	PB CLOCK CABLE "B" RACK	CC	EA C2 Y7	PB	BA C6 L9	2R
					BC C6 L9	
					BE C5 L9	
182	PB CLOCK CABLE "D" RACK	CC	EA C2 Y8	PB	DA C6 L9	2R
					DC C6 L9	
					DE C6 L9	
183	PB CLOCK CABLE "E" RACK	CC	EA C2 Y9	PB	EA B6 Y9	2R
					EE B6 Y9	
184	PB CLOCK CABLE "J" RACK	CC	EA C2 Y5	PB	JC C6 L9	2R
					JE C6 L9	
187	M0 CLOCK CABLE	CC	EA D2 L2	MEM-0	AJ J1 Y9	2F
188	M1 CLOCK CABLE	CC	EA D2 L3	MEM-1	AJ J1 Y9	2F
189	M2 CLOCK CABLE	CC	EA D2 L4	MEM-2	AJ J1 Y9	NT
190	M3 CLOCK CABLE	CC	EA D2 L5	MEM-3	AJ J1 Y9	NT
191	M4 CLOCK CABLE	CC	EA D2 L6	MEM-4	AJ J1 Y9	2F
192	M5 CLOCK CABLE	CC	EA D2 L7	MEM-5	AJ J1 Y9	2F
193	M6 CLOCK CABLE	CC	EA D2 L8	MEM-6	AJ J1 Y9	2F
194	M7 CLOCK CABLE	CC	EA D2 L9	MEM-7	AJ J1 Y9	2F
209	(#0 AWG) -19V	PS	DA M4 B2	CC	CA J1 01	2R
225	(#14 AWG) 115VAC (FAN CIRCUIT)	D & D	FAK1 06/07	CC	FAK1 06/07	NT
226	(#14 AWG) 115VAC (FAN CIRCUIT)	CC	FAK1 06/07	M-SS1	FAK1 06/07	NT
231	(#12 AWG) 115VAC (CONVENIENCE CIRCUIT)	D & D	DFP1 03/04	CC	HBL1 01/02	NT
					HBL2 01/02	
254	POWER CONTROL	D & D	DC L1	CC	DC C0 A7	9F
265	POWER CONTROL	D & D	DC L1	CC	EC A0 N7	9F

Table 5.2-2 Inter-Gate Cable List

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
24-25	HEAT & EXCESS CURRENT SENSE	CC	AA A1 Y0	CC	VOLT. REG.	1R
70	CC INTER-GATE	CC	EA B0 A7	CC	AA B0 N2	3R
71-A	CC INTER-GATE	CC	AA C0 A7	CC	BA D0 A2	NT
71-B	CC INTER-GATE	CC	AA C0 N7	CC	BC D0 A2	NT
71-C	CC INTER-GATE	CC	AA D0 A7	CC	BE B0 A2	NT
72	CC INTER-GATE	CC	AE B0 A7	CC	AA C0 N2	NT
73	CC INTER-GATE	CC	DA D0 N2	CC	EA A0 N7	NT
75-1	CC INTER-GATE	CC	EC A0 A7	CC	DA A0 A2	NT
75-2	CC INTER-GATE	CC	EC B0 A7	CC	DA B0 A2	NT
75-3	CC INTER-GATE	CC	EC C0 A7	CC	DA C0 A2	NT
75-4	CC INTER-GATE	CC	EC D0 A7	CC	DA D0 A2	NT
128	CC POWER GATE "D"	CC	DA B0 N7	CC	CS 14	1F
129	CC POWER GATE "D"	CC	DC B0 N7	CC	CS 15	1F
131	CC POWER GATE "A"	CC	AA B0 N7	CC	CS 01	1R
132	CC POWER GATE "A"	CC	AC B0 N7	CC	CS 02	1R
133	CC POWER GATE "A"	CC	AE B0 N7	CC	CS 03	1R
134	CC POWER GATE "B"	CC	BA D0 A7	CC	CS 04	1R
135	CC POWER GATE "B"	CC	BC D0 A7	CC	CS 05	1R
136	CC POWER GATE "B"	CC	BE C0 A7	CC	CS 06	1R
137	CC POWER GATE "E"	CC	EA B0 N7	CC	CS 11	1F
138	CC POWER GATE "E"	CC	EC B0 N7	CC	CS 12	1F
139	CC POWER GATE "E"	CC	EE A0 A7	CC	CS 13	1F
195	CC CLOCK CABLE "E" RACK	CC	EA D2 Y5	CC	EA B7 Y9	NT
196	CC CLOCK CABLE "A" RACK	CC	EA D2 Y4	CC	AA B5 Y9	2F
197-9	CC "A" GATE - GROUND	CC	GATE "A"	CC	CA K1 01	NT
197-10	CC "B" GATE - GROUND	CC	GATE "B"	CC	CA K1 02	NT
197-11	CC "D" GATE - GROUND	CC	GATE "D"	CC	CU K1 02	NT
197-12	CC "E" GATE - GROUND	CC	GATE "E"	CC	CU K1 01	NT
235	(#14 AWG) 115VAC - REGULATOR FAN	CC	FA K1 01/12	CC	CR J1 03/04	NT

5.3 POWER AND SYSTEM CLOCK CHECKS

INTRODUCTION

It is assumed that all system power and information cables have been installed, the voltage regulators in all units and voltage control and sensing has been checked out according to instructions in the Power Supply Manual, Section 5.

CHECKS

The following steps should be taken before applying power to the system.

1. Check all units for broken wires, loose connections, etc.
2. See that all packages, plugs, cards etc., are firmly plugged in.
3. Put the DC Lockout switch in the LOCKOUT position and bring up power.
4. Assuming system power holds normally, throw the DC LOCKOUT switch down, while observing the voltage sensing panel in D & D for any indication of power failure.
5. If there are any indications of DC failure, refer to Section 3 of the Power Supply Manual for a recheck of voltage regulators and overcurrent sensing adjustments.
6. Turn the DC LOCKOUT switch again to the "LOCKOUT" position. Check the -12V, -4.5V, -1.2V and +20V at the CC regulators to verify that these voltages are removed.
7. Bring up DC power again (4 and 5), and check for proper set and reset of all flip-flops on the CC display panel in the D & D unit.
8. Check the System Clock as explained in Section 3 of this manual.

✓5.4 DUMMY PLUGS (GROUND CLOSURES)

INTRODUCTION

Certain points must be grounded by dummy plugs in Central Control to prevent floating levels when a unit is not present.

NOTE

Dummy plugs for I/O 4 and PB are not required starting with systems shipped after June 1966.

The following dummy plugs must be installed if the unit is not present.

PLUG	UNIT	LEVEL GROUNDED	LOCATION
X	PA	$\overline{\text{MA1L}}$, D02S, D07S	ACA0A7
X	PA	BUSL, CMIL	EAC0A2
X	PB	$\overline{\text{MA1L}}$, D02S, D07S	AEA0A7
X	PB	BUSL, CMIL	EAC0N2
X	I/O 2	MANF, R07S, R02S	ACD0A7
X	I/O 3	MANF, R07S, R02S	AEC0A7
X	I/O 4	MANF, R07S, R02S	AED0A7
Y	I/O 2	D16, Z46, $\overline{\text{Z46}}$	ECB0N2
Y	I/O 3	D16, Z46, $\overline{\text{Z46}}$	ECC0N2
Y	I/O 4	D16, Z46, $\overline{\text{Z46}}$	ECD0N2
Z	PB	I01F	EAC0N7

✓Changes or additions since last issue.

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5.5 ADDING UNITS TO THE SYSTEM

INTRODUCTION

To reduce the number of unused pluggables sent to the field, unused pluggables are unloaded from Central Controls shipped after June 1966. The Central Control is loaded, however, for the BASIC SYSTEM configuration as defined below.

BASIC SYSTEM

The BASIC SYSTEM consists of:

1 Data Processor "A"
1 Central Control
1 Display and Distribution
1 Disk File Control
1 Operators Console
1 Power Supply
3 I/O Control Units
5 Core Memories
8 Tape Transports
1 Data Communication Control
2 Card Readers
1 Card Punch
2 Printers

MODIFICATION KITS

Table 5.5-1 shows which modification kits must be installed when new units are added to the B5500 system. Each modification kit requires a set of instructions for adding pluggables and cables and for removing ground closures. These instructions are covered under MODIFICATION INSTRUCTIONS and are listed by kit designations (B*, C, etc.).

TABLE 5.5-1

UNIT		DP-B	I/O-4
		B*	M*
MEM-5	F*	C	G
MEM-6	H*	D	J
MEM-7	K*	E	L

NOTE

Those modification kits which have an asterisk (*) must be installed before those modification kits without an asterisk. For example, if DP-B is being added to a system which already has a MEM-5, then modification kit B* and C must be installed. Modification kit F* was installed previously with MEM-5. If I/O-4 is being added to a system, then those modification kits in Table 5.5-2 must also be installed.

Table 5.5-2 shows which modification kits must be installed when new peripheral units are added.

TABLE 5.5-2

UNIT		I/O-4
		M*
TTU-K	AA*	AK
TTU-L	AB*	AL
TTU-M	AC*	AM
TTU-N	AD*	AN
TTU-P	AE*	AP
TTU-R	AF*	AR
TTU-S	AG*	AS
TTU-T	AH*	AT
DFC #2	N*	P
PTR #1	R*	S
PTR #2	T*	U
PTP #1	V*	W
PTP #2	X*	Y
DRUM #1	A*	Q
DRUM #2	I*	Z

MODIFICATION INSTRUCTIONS

Instructions for Modification Kit B*

To add DP-B, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	AE A2 N2	1180 1883-29	AA D5 L2*	1182 8985-29	AE A6 Y7	1182 8985-29	AE B7 L9
"	AE A4 N7	"	AA D5 L5*	"	AE A6 Y8	"	AF A1 Y0
"	AE A5 N2	"	AA D5 L8*	"	AE A6 Y9	"	AF A1 Y1
"	AE B2 A2	"	AA D5 Y2*	"	AE A7 Y0	"	AF A1 Y2
"	AE B4 A7	"	AA D5 Y5*	"	AE A7 Y1	"	AF A1 Y3
"	AE B5 A2	"	AA D5 Y8*	"	AE A7 Y2	"	AF A1 Y4
"	AF A0 N2	"	AA D6 L1*	"	AE A7 Y3	"	AF A1 Y5
"	AF A0 N7	"	AA D6 L4*	"	AE A7 Y4	"	AF A1 Y6
"	AF B0 A2	"	AA D6 Y1*	"	AE A7 Y5	"	AF A1 Y7
"	AF B0 A7	"	AA D6 Y4*	"	AE A7 Y6	"	AF A1 Y8
				"	AE A7 Y7	"	AF A1 Y9
1180 1883-04	AA C4 Y2	1115 7377	AB A0 N7	"	AE A7 Y8	"	AF A2 Y0
"	AE A5 L6	"	AB A4 N2	"	AE A7 Y9	"	AF A2 Y1
"	AE A5 L7	"	AB B0 N7	"	AE B2 L7	"	AF A2 Y2
"	AE A8 L1	"	AB C0 N7	"	AE B2 L8	"	AF A2 Y3
		"	AB D0 N7	"	AE B2 L9	"	AF A2 Y4
1180 1883-16	AA C3 L2			"	AE B3 L0	"	AF A2 Y5
"	AA C3 L3	1193 3462	AE A1 Y9	"	AE B3 L1	"	AF A2 Y6
"	AA C3 L4	"	AE A4 Y4	"	AE B3 L2	"	AF A2 Y7
"	AA C3 L5	"	AE A5 L5	"	AE B3 L3	"	AF A2 Y8
"	AA C3 Y6	"	AE A9 Y9	"	AE B3 L4	"	AF A2 Y9
"	AA C3 Y7	"	AE B1 L9	"	AE B3 L5	"	AF A3 Y0
"	AA C3 Y8	"	AE B4 L4	"	AE B3 L6	"	AF A3 Y1
"	AA C3 Y9	"	AE B9 L9	"	AE B5 L5	"	AF A3 Y2
"	AB A0 Y4			"	AE B5 L6	"	AF A3 Y3
"	AB A3 Y9	1182 8985-29	AE A2 Y7	"	AE B5 L7	"	AF A3 Y4
"	AB B0 Y4	"	AE A2 Y8	"	AE B5 L8	"	AF B1 L0
"	AB C0 Y4	"	AE A2 Y9	"	AE B5 L9	"	AF B1 L1
"	AB D0 Y4	"	AE A3 Y0	"	AE B6 L0	"	AF B1 L2
		"	AE A3 Y1	"	AE B6 L1	"	AF B1 L3
1180 1883-17	AA C3 L6	"	AE A3 Y2	"	AE B6 L2	"	AF B1 L4
"	AA C3 L7	"	AE A3 Y3	"	AE B6 L3	"	AF B1 L5
"	AA C3 L8	"	AE A3 Y4	"	AE B6 L4	"	AF B1 L6
"	AA C3 L9	"	AE A3 Y5	"	AE B6 L5	"	AF B1 L7
"	AA C3 Y2	"	AE A3 Y6	"	AE B6 L6	"	AF B1 L8
"	AA C3 Y3	"	AE A5 Y5	"	AE B6 L7	"	AF B1 L9
"	AA C3 Y4	"	AE A5 Y6	"	AE B6 L8	"	AF B2 L0
"	AA C3 Y5	"	AE A5 Y7	"	AE B6 L9	"	AF B2 L1
		"	AE A5 Y8	"	AE B7 L0	"	AF B2 L2
1180 1883-23	AA A4 Y7	"	AE A5 Y9	"	AE B7 L1	"	AF B2 L3
"	AA A4 Y8	"	AE A6 Y0	"	AE B7 L2	"	AF B2 L4
"	AA A4 Y9	"	AE A6 Y1	"	AE B7 L3	"	AF B2 L5
"	AA A5 Y0	"	AE A6 Y2	"	AE B7 L4	"	AF B2 L6
"	AA A5 Y1	"	AE A6 Y3	"	AE B7 L5	"	AF B2 L7
"	AA A5 Y2	"	AE A6 Y4	"	AE B7 L6	"	AB B2 L8
"	AA A5 Y3	"	AE A6 Y5	"	AE B7 L7	"	AF B2 L9
"	AA A5 Y4	"	AE A6 Y6	"	AE B7 L8	"	AF B3 L0

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1182 8985-29	AF B3 L1	1183 2698-16	AA C4 Y0	1188 1067	AF A1 L0	1191 8299	AE A5 A2
"	AF B3 L2					"	AE A7 A2
"	AB B3 L3	1188 1067	AB D1 Y2	1190 0768	AA C1 Y0		
"	AF B3 L4	"	AD A1 L2				
		"	AD D1 Y0	1191 8299	AE A4 A7		
1183 2698-16	AA C4 L0						
1178 4147	BC D4 N2*	1182 8985-29	BA B9 L2	1182 8985-29	BB A3 Y6	1182 8985-29	BC B4 L5
		"	BA B9 L3	"	BB A3 Y7	"	BC B4 L6
1180 1883-04	BA A8 L3	"	BA B9 L4	"	BB A3 Y8	"	BC B4 L7
"	BB D0 Y9*	"	BA B9 Y0	"	BB A3 Y9	"	BC B4 L8
"	BC A8 L3	"	BA B9 Y1	"	BB B3 L5	"	BC B4 L9
		"	BA B9 Y2	"	BB B3 L6	"	BC B4 Y5
1180 1883-25	BA D6 L1	"	BA B9 Y3	"	BB B3 L7	"	BC B4 Y6
		"	BA B9 Y4	"	BB B3 L8	"	BC B4 Y7
1180 1883-29	BC D6 Y7	"	BA C4 L5	"	BB B3 L9	"	BC B4 Y8
"	BA D6 Y7	"	BA C4 L6	"	BB B3 Y5	"	BC B4 Y9
		"	BA C4 L7	"	BB B3 Y6	"	BC B9 L0
1182 8985-04	BA D3 Y5*	"	BA C4 L8	"	BB B3 Y7	"	BC B9 L1
"	BA D3 Y6*	"	BA C4 L9	"	BB B3 Y8	"	BC B9 L2
"	BA D3 Y8*	"	BA C4 Y5	"	BB B3 Y9	"	BC B9 L3
"	BC D3 Y5*	"	BA C4 Y6	"	BB C3 L5	"	BC B9 L4
"	BC D3 Y6*	"	BA C4 Y7	"	BB C3 L6	"	BC B9 Y0
		"	BA C4 Y8	"	BB C3 L7	"	BC B9 Y1
1182 8985-29	BA A4 Y5	"	BA C4 Y9	"	BB C3 L8	"	BC B9 Y2
"	BA A4 Y6	"	BA C9 L0	"	BB C3 L9	"	BC B9 Y3
"	BA A4 Y7	"	BA C9 L1	"	BB C3 Y5	"	BC B9 Y4
"	BA A4 Y8	"	BA C9 L2	"	BB C3 Y6	"	BC C4 L5
"	BA A4 Y9	"	BA C9 L3	"	BB C3 Y7	"	BC C4 L6
"	BA A9 Y0	"	BA C9 L4	"	BB C3 Y8	"	BC C4 L7
"	BA A9 Y1	"	BA C9 Y0	"	BB C3 Y9	"	BC C4 L8
"	BA A9 Y2	"	BA C9 Y1	"	BB D3 L5	"	BC C4 L9
"	BA A9 Y3	"	BA C9 Y2	"	BB D3 L6	"	BC C9 L0
"	BA A9 Y4	"	BA C9 Y3	"	BB D3 L7	"	BC C9 L1
"	BA B4 L5	"	BA C9 Y4	"	BB D3 L8	"	BC C9 L2
"	BA B4 L6	"	BA D4 L5	"	BB D3 L9	"	BC C9 L3
"	BA B4 L7	"	BA D4 L6	"	BC A4 Y5	"	BC C9 L4
"	BA B4 L8	"	BA D4 L7	"	BC A4 Y6	"	BD A3 Y5
"	BA B4 L9	"	BA D4 L8	"	BC A4 Y7	"	BD A3 Y6
"	BA B4 Y5	"	BA D4 L9	"	BC A4 Y8	"	BD A3 Y7
"	BA B4 Y6	"	BA D9 L0	"	BC A4 Y9	"	BD A3 Y8
"	BA B4 Y7	"	BA D9 L1	"	BC A9 Y0	"	BD A3 Y9
"	BA B4 Y8	"	BA D9 L2	"	BC A9 Y1	"	BD B3 L5
"	BA B4 Y9	"	BA D9 L3	"	BC A9 Y2	"	BD B3 L6
"	BA B9 L0	"	BA D9 L4	"	BC A9 Y3	"	BD B3 L7
"	BA B9 L1	"	BB A3 Y5	"	BC A9 Y4	"	BD B3 L8

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1182 8985-29	BD B3 L9	1188 1067	BC A5 L3	1188 1067	BC D5 Y4	1190 0768	BE A1 L4
"	BD B3 Y5	"	BA D5 Y4	"	BE A5 L4	"	BE A1 L5
"	BD B3 Y6	"	BC A5 L4	"	BC D9 Y8	"	BE A1 Y0
"	BD B3 Y7	"	BA D9 Y8	"	BE A9 L8	"	BE A1 Y2
"	BD B3 Y8	"	BC A9 L8	"	BC D9 Y9	"	BE A1 Y4
"	BD B3 Y9	"	BA D9 Y9	"	BE A9 L9	"	BE A1 Y5
"	BD C3 L5	"	BC A9 L9	"	BD D4 Y3		
"	BD C3 L6	"	BB D4 Y3	"	BF A4 L3	1191 8299	BA A8 A7*
"	BD C3 L7	"	BD A4 L3	"	BD D4 Y4	"	BA A9 A2*
"	BD C3 L8	"	BB D4 Y4	"	BF A4 L4	"	BB D1 N7*
"	BD C3 L9	"	BD A4 L4			"	BC A8 A7*
		"	BC D5 Y3	1190 0768	BE A1 L0	"	BC A9 A2*
1188 1067	BA D5 Y3	"	BE A5 L3	"	BE A1 L2		
1180 1883-02	EB B3 L1	1180 1883-04	EB C4 L2	1180 1883-29	EA B9 Y6	1193 3462	EA C2 Y0
		"	EB C4 Y2	"	EA B9 Y7	"	EB B0 Y6
1180 1883-03	EB B1 L8	"	EB C4 Y8	"	EA B9 Y8		
"	EB B3 Y2			"	EA B9 Y9	1182 8985-29	EB B0 L8
"	EB B4 Y6	1180 1883-17	EB B1 L9	"	EA C4 Y7	"	EB B0 L9
"	EB C4 L6			"	EA C7 L3		
"	EB C4 L8	1180 1883-23	EA C7 L4	"	EA C7 L5	1183 2698-03	EB B3 L0
"	EB C4 Y6			"	EB B0 Y7		
		1180 1883-25	EA A3 Y8	"	EB B1 L5	1190 0768	EA C1 Y0
1180 1883-04	EA A3 Y9	"	EB B3 L3	"	EB B1 L6	"	EA C1 Y2
"	EA C7 L2	"	EB C1 L9	"	EB B1 L7	"	EA C1 Y4
"	EB B3 L2			"	EB B4 L7		
"	EB B3 Y6	1180 1883-29	EA B9 Y5	"	EB C3 L2		

Remove ground jumpers:

EA C0 N8 Z2 to EA C0 Z8 Z1
EA C0 V0 Z2 to EA C0 Z9 Z1

Instructions for Modification Kit C

To add DP-B and MEM-5, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-16	AB B3 Y9	1182 8985-29	AE A3 Y8	1182 8985-29	AE B8 L0	1182 8985-29	AF A3 Y8
		"	AE A8 Y0	"	AE B8 L1	"	AF A3 Y9
1180 1883-29	AA D6 L7*	"	AE A8 Y1	"	AE B8 L2	"	AF B3 L5
"	AA D6 Y7*	"	AE A8 Y2	"	AE B8 L3	"	AF B3 L6
		"	AE A8 Y3	"	AE B8 L4	"	AF B3 L7
1115 7377	AB B4 N2	"	AE A8 Y4	"	AF A3 Y5	"	AF B3 L8
		"	AE B3 L7	"	AF A3 Y6	"	AF B3 L9
1182 8985-29	AE A3 Y7	"	AE B3 L8	"	AF A3 Y7		
1180 1883-04	BD D0 Y9*	1182 8985-29	BC C4 Y9	1182 8985-29	BC D4 L9	1182 8985-29	BD C3 Y9
		"	BC C9 Y0	"	BC D9 L0	"	BD D3 L5
1180 1883-25	BC D6 L1	"	BC C9 Y1	"	BC D9 L1	"	BD D3 L6
		"	BC C9 Y2	"	BC D9 L2	"	BD D3 L7
1182 8985-04	BC D3 Y8*	"	BC C9 Y3	"	BC D9 L3	"	BD D3 L8
		"	BC C9 Y4	"	BC D9 L4	"	BD D3 L9
1182 8985-29	BC C4 Y5	"	BC D4 L5	"	BD C3 Y5		
"	BC C4 Y6	"	BC D4 L6	"	BD C3 Y6	1191 8299	BD D1 N7*
"	BC C4 Y7	"	BC D4 L7	"	BD C3 Y7		
"	BC C4 Y8	"	BC D4 L8	"	BD C3 Y8		

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

Instructions for Modification Kit D

To add DP-B and MEM-6, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-04	AE A8 L2	1182 8985-29	AE A4 Y0	1182 8985-29	AE B8 L7	1182 8985-29	AF B4 L2
		"	AE A8 Y5	"	AE B8 L8	"	AF B4 L3
1180 1883-16	AB C3 Y9	"	AE A8 Y6	"	AE B8 L9	"	AF B4 L4
		"	AE A8 Y7	"	AF A4 Y0		
1180 1883-29	AA D7 L0*	"	AE A8 Y8	"	AF A4 Y1	1191 8299	AE A7 A7
"	AA D7 Y0*	"	AE A8 Y9	"	AF A4 Y2		
		"	AE B3 L9	"	AF A4 Y3		
1115 7377	AB C4 N2	"	AE B4 L0	"	AF A4 Y4		
		"	AE B8 L5	"	AF B4 L0		
1182 8985-29	AE A3 Y9	"	AE B8 L6	"	AF B4 L1		
1180 1883-04	BF A0 L8	1182 8985-29	BE A4 Y9	1182 8985-29	BE B4 L9	1182 8985-29	BF A3 Y9
		"	BE A9 Y0	"	BE B9 L0	"	BF B3 L5
1180 1883-29	BE A6 L7	"	BE A9 Y1	"	BE B9 L1	"	BF B3 L6
		"	BE A9 Y2	"	BE B9 L2	"	BF B3 L7
1182 8985-04	BC D3 Y9	"	BE A9 Y3	"	BE B9 L3	"	BF B3 L8
		"	BE A9 Y4	"	BE B9 L4	"	BF B3 L9
1182 8985-29	BE A4 Y5	"	BE B4 L5	"	BF A3 Y5		
"	BE A4 Y6	"	BE B4 L6	"	BE A3 Y6	1191 8299	BF A1 A2*
"	BE A4 Y7	"	BE B4 L7	"	BF A3 Y7		
"	BE A4 Y8	"	BE B4 L8	"	BF A3 Y8		

Instructions for Modification Kit E

To add DP-B and MEM-7, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-16	AB D3 Y9	1182 8985-29	AE A4 Y2	1182 8985-29	AE B9 L0	1182 8985-29	AF A4 Y8
		"	AE A9 Y0	"	AE B9 L1	"	AF A4 Y9
1180 1883-29	AA D7 L3*	"	AE A9 Y1	"	AE B9 L2	"	AF B4 L5
"	AA D7 Y3*	"	AE A9 Y2	"	AE B9 L3	"	AF B4 L6
		"	AE A9 Y3	"	AE B9 L4	"	AF B4 L7
1115 7377	AB D4 N2	"	AE A9 Y4	"	AF A4 Y5	"	AF B4 L8
		"	AE B4 L1	"	AF A4 Y6	"	AF B4 L9
1182 8985-29	AE A4 Y1	"	AE B4 L2	"	AF A4 Y7		
1182 8985-04	BE C3 Y9*	1182 8985-29	BE B9 Y2	1182 8985-29	BE C9 L1	1182 8985-29	BF C3 L5
		"	BE B9 Y3	"	BE C9 L2	"	BF C3 L6
1182 8985-29	BE B4 Y5	"	BE B9 Y4	"	BE C9 L3	"	BF C3 L7
"	BE B4 Y6	"	BE C4 L5	"	BE C9 L4	"	BF C3 L8
"	BE B4 Y7	"	BE C4 L6	"	BF B3 Y5	"	BF C3 L9
"	BE B4 Y8	"	BE C4 L7	"	BF B3 Y6		
"	BE B4 Y9	"	BE C4 L8	"	BF B3 Y7	1191 8299	BF A1 A7*
"	BE B9 Y0	"	BE C4 L9	"	BF B3 Y8		
"	BE B9 Y1	"	BE C9 L0	"	BF B3 Y9		

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

Instructions for Modification Kit F*

To add MEM-5, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	AB B1 N7	1182 8985-29	AA C6 Y6	1182 8985-29	AC D8 L2	1182 8985-29	AE C3 L7
		"	AC A3 Y7	"	AC D8 L3	"	AE C3 L8
1180 1883-04	AB B3 Y5	"	AC A3 Y8	"	AC D8 L4	"	AE C8 L0
"	AB B3 Y6	"	AC A8 Y0	"	AD A3 Y5	"	AE C8 L1
"	AB B3 Y7	"	AC A8 Y1	"	AD A3 Y6	"	AE C8 L2
"	AC A9 L8	"	AC A8 Y2	"	AD A3 Y7	"	AE C8 L3
		"	AC A8 Y3	"	AD A3 Y8	"	AE C8 L4
1180 1883-16	AB B3 Y8	"	AC A8 Y4	"	AD A3 Y9	"	AF B3 Y5
		"	AC B3 L7	"	AD B3 L5	"	AF B3 Y6
1180 1883-17	AB B2 L6	"	AC B3 L8	"	AD B3 L6	"	AB B3 Y7
"	AB B2 L7	"	AC B3 Y7	"	AD B3 L7	"	AF B3 Y8
"	AB B2 L8	"	AC B3 Y8	"	AD B3 L8	"	AF B3 Y9
"	AB B2 Y0	"	AC B8 L0	"	AD B3 L9	"	AF C3 L5
		"	AC B8 L1	"	AD B3 Y5	"	AF C3 L6
1180 1883-23	AB B2 Y6	"	AC B8 L2	"	AD B3 Y6	"	AF C3 L7
"	AB B2 Y7	"	AC B8 L3	"	AD B3 Y7	"	AF C3 L8
"	AB B2 Y8	"	AC B8 L4	"	AD B3 Y8	"	AF C3 L9
		"	AC B8 Y0	"	AD B3 Y9		
1180 1883-29	AA D6 L5	"	AC B8 Y1	"	AD C3 L5	1188 1067	
"	AA D6 L6	"	AC B8 Y2	"	AD C3 L6	"	AC D8 Y5
"	AA D6 Y5	"	AC B8 Y3	"	AD C3 L7	"	AE A8 L5
"	AA D6 Y6	"	AC B8 Y4	"	AD C3 L8	"	AC D8 Y6
"	AB B2 Y2	"	AC C3 L7	"	AD C3 L9	"	AE A8 L6
"	AB B2 Y3	"	AC C3 L8	"	AD C3 Y5	"	AD D4 Y0
		"	AC C3 Y7	"	AD C3 Y6	"	AF A4 L0
1115 7377	AB B4 A2	"	AC C3 Y8	"	AD C3 Y7	"	AD D4 Y1
		"	AC C8 L0	"	AD C3 Y8	"	AF A4 L1
1193 3462	AB B4 L5	"	AC C8 L1	"	AD C3 Y9		
"	AB B4 Y5	"	AC C8 L2	"	AD D3 L5	1190 0768	AE B1 L2
		"	AC C8 L3	"	AD D3 L6	"	AE B1 L4
1182 4448	AB B1 A7	"	AC C8 L4	"	AD D3 L7	"	AE B1 Y0
"	AB B2 A2	"	AC C8 Y0	"	AD D3 L8	"	AE B1 Y2
"	AB B3 A2	"	AC C8 Y1	"	AD D3 L9	"	AE B1 Y4
"	AB B3 N2	"	AC C8 Y2	"	AE B3 Y7	"	AE B1 Y5
		"	AC C8 Y3	"	AE B3 Y8		
1182 8985-04	AB B2 Y4	"	AC C8 Y4	"	AE B8 Y0	1191 8299	AD A0 A7
		"	AC D3 L7	"	AE B8 Y1		
1182 8985-19	AB B2 Y1	"	AC D3 L8	"	AE B8 Y2		
		"	AC D8 L0	"	AE B8 Y3		
1182 8985-29	AA C5 L6	"	AC D8 L1	"	AE B8 Y4		

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	BC C2 N2	1182 8985-29	BC C3 Y4	1182 8985-29	BC D3 L5	1182 8985-29	BD C2 Y6
"	BC C2 N7	"	BC C3 Y5	"	BC D3 L6	"	BD C2 Y7
"	BC C6 N7	"	BC C3 Y6	"	BC D3 L7	"	BD C2 Y8
"	BC C7 N2	"	BC C3 Y7	"	BC D3 L8	"	BD C2 Y9
"	BC D2 A2	"	BC C3 Y8	"	BC D3 L9	"	BD C3 Y0
"	BC D2 A7	"	BC C3 Y9	"	BC D4 L0	"	BD C3 Y1
"	BC D4 N2*	"	BC C4 Y0	"	BC D4 L1	"	BD C3 Y2
"	BC D4 N7	"	BC C4 Y1	"	BC D4 L2	"	BD C3 Y3
"	BC D6 A7	"	BC C4 Y2	"	BC D4 L3	"	BD C3 Y4
"	BC D7 A2	"	BC C4 Y3	"	BC D4 L4	"	BD C4 Y0
"	BD C1 N2	"	BC C4 Y4	"	BC D5 L0	"	BD C4 Y1
"	BD C1 N7	"	BC C5 Y0	"	BC D5 L1	"	BD C4 Y2
"	BD D1 A2	"	BC C5 Y1	"	BC D5 L2	"	BD C4 Y3
"	BD D1 A7	"	BC C5 Y2	"	BC D5 L3	"	BD C4 Y4
		"	BC C5 Y3	"	BC D5 L4	"	BD D2 L0
1180 1883-04	BC D8 Y4	"	BC C5 Y4	"	BC D7 L5	"	BD D2 L1
"	BD D0 Y8	"	BC C7 Y5	"	BC D7 L6	"	BD D2 L2
		"	BC C7 Y6	"	BC D7 L7	"	BD D2 L3
1180 1883-20	BC D6 Y1	"	BC C7 Y7	"	BC D7 L8	"	BD D2 L4
"	BC D6 Y2	"	BC C7 Y8	"	BC D7 L9	"	BD D2 L5
"	BC D6 Y3	"	BC C7 Y9	"	BC D8 L0	"	BD D2 L6
		"	BC C8 Y0	"	BC D8 L1	"	BD D2 L7
1180 1883-25	BC D6 L2	"	BC C8 Y1	"	BC D8 L2	"	BD D2 L8
		"	BC C8 Y2	"	BC D8 L3	"	BD D2 L9
1193 3462	BC C1 Y9	"	BC C8 Y3	"	BC D8 L4	"	BD D3 L0
"	BC C6 Y4	"	BC C8 Y4	"	BC D8 L5	"	BD D3 L1
"	BC D1 L9	"	BC C8 Y5	"	BC D8 L6	"	BD D3 L2
"	BC D6 L4	"	BC C8 Y6	"	BC D8 L7	"	BD D3 L3
"	BC D8 Y0	"	BC C8 Y7	"	BC D8 L8	"	BD D3 L4
"	BD C0 Y9	"	BC C8 Y8	"	BC D8 L9	"	BD D4 L0
"	BD D0 L9	"	BC C8 Y9	"	BC D9 L5	"	BD D4 L1
"	BD D0 Y5	"	BC C9 Y5	"	BC D9 L6	"	BD D4 L2
		"	BC C9 Y6	"	BC D9 L7	"	BD D4 L3
1182 8985-04	BC D3 Y7	"	BC C9 Y7	"	BC D9 L8	"	BD D4 L4
"	BC D1 Y9	"	BC C9 Y8	"	BC D9 L9		
		"	BC C9 Y9	"	BD C2 Y0	1190 0768	BC D1 L5
1182 8985-29	BC C3 Y0	"	BC D3 L0	"	BD C2 Y1		
"	BC C3 Y1	"	BC D3 L1	"	BD C2 Y2	1191 8299	BC D8 N7
"	BC C3 Y2	"	BC D3 L2	"	BD C2 Y3	"	BD D1 N2
"	BC C3 Y3	"	BC D3 L3	"	BD C2 Y4		
		"	BC D3 L4	"	BD C2 Y5		

Remove the following ground jumpers:

AE B0 E3 Z2 to AE A2 Z7 Z1
AC B1 H7 Z2 to AC B2 Z6 Z1

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

Instructions for Modification Kit G

To add I/O-4 and MEM-5, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	AB B2 L9	1182 8985-29	AE C3 Y8	1182 8985-29	AE D8 L2	1182 8985-29	AF D3 L7
		"	AE C8 Y0	"	AE D8 L3	"	AF D3 L8
1180 1883-23	AB B2 Y9	"	AE C8 Y1	"	AE D8 L4	"	AF D3 L9
		"	AE C8 Y2	"	AF C3 Y5		
1180 1883-29	AA D6 L7*	"	AE C8 Y3	"	AF C3 Y6		
"	AA D6 Y7*	"	AE C8 Y4	"	AF C3 Y7		
		"	AE D3 L7	"	AF C3 Y8		
1182 4448	AB B3 A7	"	AE D3 L8	"	AF C3 Y9		
		"	AE D8 L0	"	AF D3 L5		
1182 8985-29	AE C3 Y7	"	AE D8 L1	"	AF D3 L6		
1180 1883-04	BD D0 Y9*	1182 8985-29	BC C5 Y9	1182 8985-29	BD C0 Y4	1182 8985-29	BD D0 L4
		"	BC D5 L5	"	BD C4 Y5	"	BD D4 L5
1180 1883-25	BC D6 L3	"	BC D5 L6	"	BD C4 Y6	"	BD D4 L6
		"	BC D5 L7	"	BD C4 Y7	"	BD D4 L7
1182 8985-04	BC D3 Y8*	"	BC D5 L8	"	BD C4 Y8	"	BD D4 L8
		"	BC D5 L9	"	BD C4 Y9	"	BD D4 L9
1182 8985-29	BC C5 Y5	"	BD C0 Y0	"	BD D0 L0		
"	BC C5 Y6	"	BD C0 Y1	"	BD D0 L1	1191 8299	BD D1 N7*
"	BC C5 Y7	"	BD C0 Y2	"	BD D0 L2		
"	BC C5 Y8	"	BD C0 Y3	"	BD D0 L3		

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

Instructions for Modification Kit H*

To add MEM-6, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	AB C1 N7	1182 8985-19	AB C2 Y1	1182 8985-29	AC D8 L6	1182 8985-29	AE C3 L9
		1182 8985-29	AA C5 L7	"	AC D8 L7	"	AE C4 L0
1180 1883-04	AB C3 Y5	"	AA C6 Y7	"	AC D8 L8	"	AE C8 L5
"	AB C3 Y6	"	AC A3 Y9	"	AC D8 L9	"	AE C8 L6
"	AB C3 Y7	"	AC A4 Y0	"	AD A4 Y0	"	AE C8 L7
"	AC D9 Y8	"	AC A8 Y5	"	AD A4 Y1	"	AE C8 L8
"	AD A2 L2	"	AC A8 Y6	"	AD A4 Y2	"	AE C8 L9
"	AF A2 L3	"	AC A8 Y7	"	AD A4 Y3	"	AF B4 Y1
		"	AC A8 Y8	"	AD A4 Y4	"	AF B4 Y2
1180 1883-16	AB C3 Y8	"	AC A8 Y9	"	AD B4 L0	"	AF B4 Y3
		"	AC B1 L8	"	AD B4 L1	"	AF B4 Y4
1180 1883-17	AA C2 Y4	"	AC B3 L9	"	AD B4 L2	"	AF C4 L0
"	AB C2 L6	"	AC B3 Y9	"	AD B4 L3	"	AF C4 L1
"	AB C2 L7	"	AC B4 L0	"	AD B4 L4	"	AF C4 L2
"	AB C2 L8	"	AC B4 Y0	"	AD B4 Y0	"	AF C4 L3
"	AB C2 Y0	"	AC B8 L5	"	AD B4 Y1	"	AF C4 L4
		"	AC B8 L6	"	AD B4 Y2	"	AF B4 Y0
1180 1883-23	AB C2 Y6	"	AC B8 L7	"	AD B4 Y3	1188 1067	
"	AB C2 Y7	"	AC B8 L8	"	AD B4 Y4	"	AC D8 Y7
"	AB C2 Y8	"	AC B8 L9	"	AD C4 L0	"	AE A8 L7
		"	AC B8 Y5	"	AD C4 L1	"	AC D8 Y8
1180 1883-29	AA D6 L8	"	AC B8 Y6	"	AD C4 L2	"	AE A8 L8
"	AA D6 L9	"	AC B8 Y7	"	AD C4 L3	"	AD D4 Y2
"	AA D6 Y8	"	AC B8 Y8	"	AD C4 L4	"	AF A4 L2
"	AA D6 Y9	"	AC B8 Y9	"	AD C4 Y0	"	AD D4 Y3
"	AB C2 Y2	"	AC C3 L9	"	AD C4 Y1	"	AF A4 L3
"	AB C2 Y3	"	AC C3 Y9	"	AD C4 Y2		
		"	AC C4 L0	"	AD C4 Y3	1190 0768	AA C1 Y7
1115 7377	AB C4 A2	"	AC C4 Y0	"	AD C4 Y4	"	AE C1 L2
		"	AC C8 L5	"	AD D4 L0	"	AE C1 L4
1193 3462	AB C4 L5	"	AC C8 L6	"	AD D4 L1	"	AE C1 Y0
"	AB C4 Y5	"	AC C8 L7	"	AD D4 L2	"	AE C1 Y2
"	AC D9 Y9	"	AC C8 L8	"	AD D4 L3	"	AE C1 Y4
"	AD A2 L4	"	AC C8 L9	"	AD D4 L4	"	AE C1 Y5
"	AF A2 L4	"	AC C8 Y5	"	AE B1 L8		
		"	AC C8 Y6	"	AE B3 Y9	1191 8299	AD A2 A7
1182 4448	AB C1 A7	"	AC C8 Y7	"	AE B4 Y0	"	AD D0 N7
"	AB C2 A2	"	AC C8 Y8	"	AE B8 Y5	"	AF A3 A2
"	AB C3 A2	"	AC C8 Y9	"	AE B8 Y6		
"	AB C3 N2	"	AC D3 L9	"	AE B8 Y7		
		"	AC D4 L0	"	AE B8 Y8		
1182 8985-04	AB C2 Y4	"	AC D8 L5	"	AE B8 Y9		

Remove ground jumpers:

AE C0 E3 Z2 to AE B2 Z7 Z1

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	BE A2 N2	1182 8985-29	BE A3 Y8	1182 8985-29	BE B5 L0	1182 8985-29	BF B2 L2
"	BE A2 N7	"	BE A3 Y9	"	BE B5 L1	"	BF B2 L3
"	BE A6 N7	"	BE A4 Y0	"	BE B5 L2	"	BF B2 L4
"	BE A7 N2	"	BE A4 Y1	"	BE B5 L3	"	BF B2 L5
"	BE B2 A2	"	BE A4 Y2	"	BE B5 L4	"	BF B2 L6
"	BE B2 A7	"	BE A4 Y3	"	BE B7 L5	"	BF B2 L7
"	BE B6 A7	"	BE A4 Y4	"	BE B7 L6	"	BF B2 L8
"	BE B7 A2	"	BE A5 Y0	"	BE B7 L7	"	BF B2 L9
"	BE C4 N2	"	BE A5 Y1	"	BE B7 L8	"	BF B3 L0
"	BF A1 N2	"	BE A5 Y2	"	BE B7 L9	"	BF B3 L1
"	BF A1 N7	"	BE A5 Y3	"	BE B8 L0	"	BF B3 L2
"	BF B1 A2	"	BE A5 Y4	"	BE B8 L1	"	BF B3 L3
"	BF B1 A7	"	BE A7 Y5	"	BE B8 L2	"	BF B3 L4
		"	BE A7 Y6	"	BE B8 L3	"	BF B4 L0
1180 1883-04	BE A3 L8	"	BE A7 Y7	"	BE B8 L4	"	BF B4 L1
"	BE A3 L9	"	BE A7 Y8	"	BE B8 L5	"	BF B4 L2
"	BE A8 L3	"	BE A7 Y9	"	BE B8 L6	"	BF B4 L3
"	BE A8 L4	"	BE A8 Y0	"	BE B8 L7	"	BF B4 L4
		"	BE A8 Y1	"	BE B8 L8		
1180 1883-29	BE A6 L4	"	BE A8 Y2	"	BE B8 L9	1183 3829	BE A7 A2
"	BE A6 L5	"	BE A8 Y3	"	BE B9 L5		
"	BE A6 L6	"	BE A8 Y4	"	BE B9 L6	1188 1067	BC D3 Y2
"	BE A6 L8	"	BE A8 Y5	"	BE B9 L7	"	BE A3 L2
		"	BE A8 Y6	"	BE B9 L8	"	BC D3 Y1
1193 3462	BE A1 L9	"	BE A8 Y7	"	BE B9 L9	"	BE A3 L1
"	BE A1 Y9	"	BE A8 Y8	"	BF A2 Y0	"	BC D3 Y3
"	BE A6 L0	"	BE A8 Y9	"	BF A2 Y1	"	BE A3 L3
"	BE A6 Y4	"	BE A9 Y5	"	BF A2 Y2	"	BC D3 Y4
"	BE A8 L0	"	BE A9 Y6	"	BF A2 Y3	"	BE A3 L4
"	BE B1 L9	"	BE A9 Y7	"	BF A2 Y4	"	BC D5 Y1
"	BE B6 L4	"	BE A9 Y8	"	BF A2 Y5	"	BE A5 L1
"	BE C1 Y9	"	BE A9 Y9	"	BF A2 Y6	"	BC D5 Y2
"	BE C5 Y0	"	BE B3 L0	"	BF A2 Y7	"	BE A5 L2
"	BF A0 Y9	"	BE B3 L1	"	BF A2 Y8	"	BC D5 Y5
"	BF B0 L9	"	BE B3 L2	"	BF A2 Y9	"	BE A5 L5
		"	BE B3 L3	"	BF A3 Y0	"	BC D5 Y6
1182 8985-04	BE C3 Y5	"	BE B3 L4	"	BF A3 Y1	"	BE A5 L6
"	BE C3 Y6	"	BE B3 L5	"	BF A3 Y2	"	BC D7 Y6
		"	BE B3 L6	"	BF A3 Y3	"	BE A7 L6
1182 8985-29	BE A3 Y0	"	BE B3 L7	"	BF A3 Y4	"	BC D7 Y7
"	BE A3 Y1	"	BE B3 L8	"	BF A4 Y0	"	BE A7 L7
"	BE A3 Y2	"	BE B3 L9	"	BF A4 Y1	"	BC D7 Y8
"	BE A3 Y3	"	BE B4 L0	"	BF A4 Y2	"	BE A7 L8
"	BE A3 Y4	"	BE B4 L1	"	BF A4 Y3	"	BC D7 Y9
"	BE A3 Y5	"	BE B4 L2	"	BF A4 Y4	"	BE A7 L9
"	BE A3 Y6	"	BE B4 L3	"	BF B2 L0	"	BC D9 Y6
"	BE A3 Y7	"	BE B4 L4	"	BF B2 L1	"	BE A9 L6

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1188 1067	BC D9 Y7	1188 1067	BF A2 L1	1188 1067	BD D4 Y1	1188 1067	BF A4 L6
"	BD A9 L7	"	BD D2 Y2	"	BF A4 L1		
"	BD D0 Y0	"	BF A2 L2	"	BD D4 Y2	1190 0768	BE B1 L0
"	BF A0 L0	"	BD D2 Y3	"	BF A4 L2	"	BE B1 L2
"	BD D0 Y1	"	BF A2 L3	"	BD D4 Y5		
"	BF A0 L1	"	BD D2 Y4	"	BF A4 L5	1191 8299	BE A4 A2
"	BD D2 Y1	"	BF A2 L4	"	BD D4 Y6	"	BE A8 A7

Instructions for Modification Kit J

To add I/O-4 and MEM-6, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-04	AE D9 Y8	1182 4448	AB C3 A7	1182 8985-29	AE D4 L0	1182 8985-29	AF C4 Y4
				"	AE D8 L5	"	AF D4 L0
1180 1883-17	AB C2 L9	1182 8985-29	AE C3 Y9	"	AE D8 L6	"	AF D4 L1
		"	AE C4 Y0	"	AE D8 L7	"	AF D4 L2
1180 1883-23	AB C2 Y9	"	AE C8 Y5	"	AE D8 L8	"	AF D4 L3
		"	AE C8 Y6	"	AE D8 L9	"	AF D4 L4
1180 1883-29	AA D7 L0*	"	AE C8 Y7	"	AF C4 Y0		
"	AA D7 Y0*	"	AE C8 Y8	"	AF C4 Y1	1191 8299	AF D0 N7
		"	AE C8 Y9	"	AF C4 Y2		
1193 3462	AE D9 Y9	"	AE D3 L9	"	AF C4 Y3		
1180 1883-04	BF A0 L9	1182 8985-29	BE A5 Y7	1182 8985-29	BF A0 Y2	1189 8985-29	BF B0 L2
		"	BE A5 Y8	"	BF A0 Y3	"	BF B0 L3
1180 1883-29	BE A6 L9	"	BE A5 Y9	"	BF A0 Y4	"	BF B0 L4
		"	BE B5 L5	"	BF A4 Y5	"	BF B4 L5
1193 3462	BF A0 L5	"	BE B5 L6	"	BF A4 Y6	"	BF B4 L6
		"	BE B5 L7	"	BF A4 Y7	"	BF B4 L7
1182 8985-04	BC D3 Y9	"	BE B5 L8	"	BF A4 Y8	"	BF B4 L8
		"	BE B5 L9	"	BF A4 Y9	"	BF B4 L9
1182 8985-29	BE A5 Y5	"	BF A0 Y0	"	BF B0 L0		
"	BE A5 Y6	"	BF A0 Y1	"	BF B0 L1	1191 8299	BF A1 A2*

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

Instructions for Modification Kit K*

To add MEM-7, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	AB D1 N7	1182 8985-29	AC A4 Y2	1182 8985-29	AC D9 L4	1182 8985-29	AE C9 L0
		"	AC A9 Y0	"	AD A4 Y5	"	AE C9 L1
1180 1883-04	AB D3 Y5	"	AC A9 Y1	"	AD A4 Y6	"	AE C9 L2
"	AB D3 Y7	"	AC A9 Y2	"	AD A4 Y7	"	AE C9 L3
"	AD A2 L3	"	AC A9 Y3	"	AD A4 Y8	"	AE C9 L4
		"	AC A9 Y4	"	AD A4 Y9	"	AF B4 Y5
1180 1883-16	AB D3 Y8	"	AC B4 L1	"	AD B4 L5	"	AF B4 Y6
		"	AC B4 L2	"	AD B4 L6	"	AF B4 Y7
1180 1883-17	AB D2 L6	"	AC B4 Y1	"	AD B4 L7	"	AF B4 Y8
"	AB D2 L7	"	AC B4 Y2	"	AD B4 L8	"	AF B4 Y9
"	AB D2 L8	"	AC B9 L0	"	AD B4 L9	"	AF C4 L5
"	AB D2 Y0	"	AC B9 L1	"	AD B4 Y5	"	AF C4 L6
		"	AC B9 L2	"	AD B4 Y6	"	AF C4 L7
1180 1883-23	AB D2 Y6	"	AC B9 L3	"	AD B4 Y7	"	AF C4 L8
"	AB D2 Y7	"	AC B9 L4	"	AD B4 Y8	"	AF C4 L9
"	AB D2 Y8	"	AC B9 Y0	"	AD B4 Y9		
		"	AC B9 Y1	"	AD C4 L5	1188 1067	
1180 1883-29	AA D7 L1	"	AC B9 Y2	"	AD C4 L6	"	AC D8 Y9
"	AA D7 L2	"	AC B9 Y3	"	AD C4 L7	"	AE A8 L9
"	AA D7 Y1	"	AC B9 Y4	"	AD C4 L8	"	AC D9 Y0
"	AA D7 Y2	"	AC C4 L1	"	AD C4 L9	"	AE A9 L0
"	AB D2 Y2	"	AC C4 L2	"	AD C4 Y5	"	AD D4 Y4
"	AB D2 Y3	"	AC C4 Y1	"	AD C4 Y6	"	AF A4 L4
		"	AC C4 Y2	"	AD C4 Y7	"	AD D4 Y5
1115 7377	AB D4 A2	"	AC C9 L0	"	AD C4 Y8	"	AF A4 L5
		"	AC C9 L1	"	AD C4 Y9		
1193 3462	AB D4 L5	"	AC C9 L2	"	AD D4 L5	1190 0768	AE D1 L2
"	AB D4 Y5	"	AC C9 L3	"	AD D4 L6	"	AE D1 L4
		"	AC C9 L4	"	AD D4 L7	"	AE D1 Y0
1182 4448	AB D1 A7	"	AC C9 Y0	"	AD D4 L8	"	AE D1 Y2
"	AB D2 A2	"	AC C9 Y1	"	AD D4 L9	"	AE D1 Y4
"	AB D3 N2	"	AC C9 Y2	"	AE B4 Y1	"	AE D1 Y5
"	AB D3 A2	"	AC C9 Y3	"	AE B4 Y2		
1182 8985-04	AB D2 Y4	"	AC C9 Y4	"	AE B9 Y0	1191 8299	AD A3 A2
		"	AC D4 L1	"	AE B9 Y1		
1182 8985-19	AB D2 Y1	"	AC D4 L2	"	AE B9 Y2		
		"	AC D9 L0	"	AE B9 Y3		
1182 8985-29	AA C5 L8	"	AC D9 L1	"	AE B9 Y4		
"	AA C6 Y8	"	AC D9 L2	"	AE C4 L1		
"	AC A4 Y1	"	AC D9 L3	"	AE C4 L2		

Remove ground jumpers:

AE D0 E3 Z2 to AE C2 Z7 Z1
✓AC B1 H8 Z2 to AC B2 Z7 Z1

✓ Changes or additions since last issue

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	BE B2 N2	1182 8985-29	BE B5 Y1	1182 8985-29	BE C5 L1	1182 8985-29	BF B4 Y1
"	BE B2 N7	"	BE B5 Y2	"	BE C5 L2	"	BF B4 Y2
"	BE B6 N7	"	BE B5 Y3	"	BE C5 L3	"	BF B4 Y3
"	BE B7 N2	"	BE B5 Y4	"	BE C5 L4	"	BF B4 Y4
"	BE C2 A2	"	BE B7 Y5	"	BE C7 L5	"	BF C2 L0
"	BE C2 A7	"	BE B7 Y6	"	BE C7 L6	"	BF C2 L1
"	BE C4 N7	"	BE B7 Y7	"	BE C7 L7	"	BF C2 L2
"	BE C6 A7	"	BE B7 Y8	"	BE C7 L8	"	BF C2 L3
"	BE C7 A2	"	BE B7 Y9	"	BE C7 L9	"	BF C2 L4
"	BF B1 N2	"	BE B8 Y0	"	BE C8 L0	"	BF C2 L5
"	BF B1 N7	"	BE B8 Y1	"	BE C8 L1	"	BF C2 L6
"	BF C1 A2	"	BE B8 Y2	"	BE C8 L2	"	BF C2 L7
"	BF C1 A7	"	BE B8 Y3	"	BE C8 L3	"	BF C2 L8
		"	BE B8 Y4	"	BE C8 L4	"	BF C3 L0
1193 3462	BE B1 Y9	"	BE B8 Y5	"	BE C8 L5	"	BF C3 L1
"	BE B6 Y4	"	BE B8 Y6	"	BE C8 L6	"	BF C3 L2
"	BE C1 L9	"	BE B8 Y7	"	BE C8 L7	"	BF C3 L3
"	BE C6 L4	"	BE B8 Y8	"	BE C8 L8	"	BF C3 L4
"	BF B0 Y9	"	BE B8 Y9	"	BE C8 L9	"	BF C4 L0
"	BF C0 L9	"	BE B9 Y5	"	BE C9 L5	"	BF C4 L1
		"	BE B9 Y6	"	BE C9 L6	"	BF C4 L2
1182 8985-04	BE C3 Y7	"	BE B9 Y7	"	BE C9 L7	"	BF C4 L3
"	BE C3 Y8	"	BE B9 Y8	"	BE C9 L8	"	BF C4 L4
		"	BE B9 Y9	"	BE C9 L9	"	BF C2 L9
1182 8985-29	BE B3 Y0	"	BE C3 L0	"	BF B2 Y0	1190 0768	BE B1 L4
"	BE B3 Y1	"	BE C3 L1	"	BF B2 Y1		
"	BE B3 Y2	"	BE C3 L2	"	BF B2 Y2	1191 8299	BE A4 A7
"	BE B3 Y3	"	BE C3 L3	"	BF B2 Y3	"	BE A9 A2
"	BE B3 Y4	"	BE C3 L4	"	BF B2 Y4		
"	BE B3 Y5	"	BE C3 L5	"	BF B2 Y5		
"	BE B3 Y6	"	BE C3 L6	"	BF B2 Y6		
"	BE B3 Y7	"	BE C3 L7	"	BF B2 Y7		
"	BE B3 Y8	"	BE C3 L8	"	BF B2 Y8		
"	BE B3 Y9	"	BE C3 L9	"	BF B2 Y9		
"	BE B4 Y0	"	BE C4 L0	"	BF B3 Y0		
"	BE B4 Y1	"	BE C4 L1	"	BF B3 Y1		
"	BE B4 Y2	"	BE C4 L2	"	BF B3 Y2		
"	BE B4 Y3	"	BE C4 L3	"	BF B3 Y3		
"	BE B4 Y4	"	BE C4 L4	"	BF B3 Y4		
"	BE B5 Y0	"	BE C5 L0	"	BF B4 Y0		

Instructions for Modification Kit L

To add I/O-4 and MEM-7, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	AB D2 L9	1182 8985-29	AE C4 Y2	1182 8985-29	AE D9 L2	1182 8985-29	AF D4 L7
		"	AE C9 Y0	"	AE D9 L3	"	AF D4 L8
1180 1883-23	AB D2 Y9	"	AE C9 Y1	"	AE D9 L4	"	AF D4 L9
		"	AE C9 Y2	"	AF C4 Y5		
1180 1883-29	AA D7 L3*	"	AE C9 Y3	"	AF C4 Y6		
"	AA D7 Y3*	"	AE C9 Y4	"	AF C4 Y7		
		"	AE D4 L1	"	AF C4 Y8		
1182 4448	AB D3 A7	"	AE D4 L2	"	AF C4 Y9		
		"	AE D9 L0	"	AF D4 L5		
1182 8985-29	AE C4 Y1	"	AE D9 L1	"	AF D4 L6		
1182 8985-04	BE C3 Y9*	1182 8985-29	BE C5 L8	1182 8985-29	BF B4 Y8	1182 8985-29	BF C4 L8
		"	BE C5 L9	"	BF B4 Y9	"	BF C4 L9
1182 8985-29	BE B5 Y5	"	BF B0 Y0	"	BF C0 L0		
"	BE B5 Y6	"	BF B0 Y1	"	BF C0 L1	1191 8299	BF A1 A7*
"	BE B5 Y7	"	BF B0 Y2	"	BF C0 L2		
"	BE B5 Y8	"	BF B0 Y3	"	BF C0 L3		
"	BE B5 Y9	"	BF B0 Y4	"	BF C0 L4		
"	BE C5 L5	"	BF B4 Y5	"	BF C4 L5		
"	BE C5 L6	"	BF B4 Y6	"	BF C4 L6		
"	BE C5 L7	"	BF B4 Y7	"	BF C4 L7		

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

Instructions for Modification Kit M*

To add I/O-4, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	AE C2 N2	1180 1883-29	AA D5 L2*	1182 8985-29	AE C6 Y4	1182 8985-29	AE D7 L6
"	AE C4 N7	"	AA D5 L5*	"	AE C6 Y5	"	AE D7 L7
"	AE C5 N2	"	AA D5 L8*	"	AE C6 Y6	"	AE D7 L8
"	AE D2 A2	"	AA D5 Y2*	"	AE C6 Y7	"	AE D7 L9
"	AE D4 A7	"	AA D5 Y5*	"	AE C6 Y8	"	AF C1 Y0
"	AE D5 A2	"	AA D5 Y8*	"	AE C6 Y9	"	AF C1 Y1
"	AF C0 N2	"	AA D6 L1*	"	AE C7 Y0	"	AF C1 Y2
"	AF C0 N7	"	AA D6 L4*	"	AE C7 Y1	"	AF C1 Y3
"	AF D0 A2	"	AA D6 Y1*	"	AE C7 Y2	"	AF C1 Y4
"	AF D0 A7	"	AA D6 Y4*	"	AE C7 Y3	"	AF C1 Y5
				"	AE C7 Y4	"	AF C1 Y6
1180 1883-04	AA A4 L2	1193 3462	AE C1 Y9	"	AE C7 Y5	"	AF C1 Y7
"	AA A4 L6	"	AE C4 Y4	"	AE C7 Y6	"	AF C1 Y8
"	AA A4 L7	"	AE C9 Y9	"	AE C7 Y7	"	AF C1 Y9
"	AE D9 Y5	"	AE D1 L9	"	AE C7 Y8	"	AF C2 Y0
"	AE D9 Y6	"	AE D1 Y9	"	AE C7 Y9	"	AF C2 Y1
"	AE D9 Y7	"	AE D4 L4	"	AE D2 L7	"	AF C2 Y2
		"	AE D8 Y0	"	AE D2 L8	"	AF C2 Y3
1180 1883-17	AA A9 L4	"	AE D9 L9	"	AE D2 L9	"	AF C2 Y4
"	AA B9 L4			"	AE D3 L0	"	AF C2 Y5
"	AA C9 L4	1182 4448	AB A0 A2	"	AE D3 L1	"	AF C2 Y6
"	AA D9 L4	"	AB A3 A7	"	AE D3 L2	"	AF C2 Y7
"	AB A2 L9	"	AB B0 A2	"	AE D3 L3	"	AF C2 Y8
		"	AB C0 A2	"	AE D3 L4	"	AF C2 Y9
1180 1883-23	AA A6 Y8	"	AB D0 A2	"	AE D3 L5	"	AF C3 Y0
"	AA A6 Y9			"	AE D3 L6	"	AF C3 Y1
"	AA A7 Y0	1182 8985-16	AA C4 L3	"	AE D5 L5	"	AF C3 Y2
"	AA A7 Y1			"	AE D5 L6	"	AF C3 Y3
"	AA A7 Y2	1182 8985-29	AE C2 Y7	"	AE D5 L7	"	AF C3 Y4
"	AA A7 Y3	"	AE C2 Y8	"	AE D5 L8	"	AF D1 L0
"	AA A7 Y4	"	AE C2 Y9	"	AE D5 L9	"	AF D1 L1
"	AA A7 Y5	"	AE C3 Y0	"	AE D6 L0	"	AF D1 L2
"	AA A9 Y4	"	AE C3 Y1	"	AE D6 L1	"	AF D1 L3
"	AA B9 Y4	"	AE C3 Y2	"	AE D6 L2	"	AF D1 L4
"	AA C9 Y4	"	AE C3 Y3	"	AE D6 L3	"	AF D1 L5
"	AA D9 Y4	"	AE C3 Y4	"	AE D6 L4	"	AF D1 L6
"	AB A2 Y9	"	AE C3 Y5	"	AE D6 L5	"	AF D1 L7
		"	AE C3 Y6	"	AE D6 L6	"	AF D1 L8
1180 1883-29	AA A6 L9	"	AE C5 Y5	"	AE D6 L7	"	AF D1 L9
"	AA A7 L0	"	AE C5 Y6	"	AE D6 L8	"	AF D2 L0
"	AA A7 L1	"	AE C5 Y7	"	AE D6 L9	"	AF D2 L1
"	AA A7 L2	"	AE C5 Y8	"	AE D7 L0	"	AF D2 L2
"	AA A7 L3	"	AE C5 Y9	"	AE D7 L1	"	AF D2 L3
"	AA A7 L4	"	AE C6 Y0	"	AE D7 L2	"	AF D2 L4
"	AA A7 L5	"	AC C6 Y1	"	AE D7 L3	"	AF D2 L5
"	AA A7 L6	"	AE C6 Y2	"	AE D7 L4	"	AF D2 L6
"	AA A7 L7	"	AE C6 Y3	"	AE D7 L5	"	AF D2 L7

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1182 8985-29	AF D2 L8	1182 8985-29	AF D3 L2	1188 1067	AD D1 Y2	1191 8299	AE D8 N7
"	AF D2 L9	"	AF D3 L3	"	AF A1 L2	"	AE D9 N2
"	AF D3 L0	"	AF D3 L4	1190 0768	AA C1 Y5	"	AF D0 N2
"	AF D3 L1						
1178 4147	BC D4 N2*	1182 8985-29	BA C5 Y9	1182 8985-29	BB C0 Y0	1182 8985-29	BC C5 L6
		"	BA D5 L5	"	BB C0 Y1	"	BC C5 L7
1180 1883-04	BA A8 L4	"	BA D5 L6	"	BB C0 Y2	"	BC C5 L8
"	BB D0 Y9*	"	BA D5 L7	"	BB C0 Y3	"	BC C5 L9
"	BC A8 L4	"	BA D5 L8	"	BB C0 Y4	"	BD A0 Y0
		"	BA D5 L9	"	BB C4 L5	"	BD A0 Y1
1180 1883-25	BA D6 L3	"	BB A0 Y0	"	BB C4 L6	"	BD A0 Y2
		"	BB A0 Y1	"	BB C4 L7	"	BD A0 Y3
1180 1883-29	BA D6 Y9	"	BB A0 Y2	"	BB C4 L8	"	BD A0 Y4
"	BC D6 Y9	"	BB A0 Y3	"	BB C4 L9	"	BD A4 Y5
		"	BB A0 Y4	"	BB C4 Y5	"	BD A4 Y6
1182 8985-04	BA D3 Y5*	"	BB A4 Y5	"	BB C4 Y6	"	BD A4 Y7
"	BA D3 Y6*	"	BB A4 Y6	"	BB C4 Y7	"	BD A4 Y8
"	BA D3 Y8*	"	BB A4 Y7	"	BB C4 Y8	"	BD A4 Y9
"	BC D3 Y5*	"	BB A4 Y8	"	BB C4 Y9	"	BD B0 L0
"	BC D3 Y6*	"	BB A4 Y9	"	BB D0 L0	"	BD B0 L1
		"	BB B0 L0	"	BB D0 L1	"	BD B0 L2
1182 8985-29	BA A5 Y5	"	BB B0 L1	"	BB D0 L2	"	BD B0 L3
"	BA A5 Y6	"	BB B0 L2	"	BB D0 L3	"	BD B0 L4
"	BA A5 Y7	"	BB B0 L3	"	BB D0 L4	"	BD B0 Y0
"	BA A5 Y8	"	BB B0 L4	"	BB D4 L5	"	BD B0 Y1
"	BA A5 Y9	"	BB B0 Y0	"	BB D4 L6	"	BD B0 Y2
"	BA B5 L5	"	BB B0 Y1	"	BB D4 L7	"	BD B0 Y3
"	BA B5 L6	"	BB B0 Y2	"	BB D4 L8	"	BD B0 Y4
"	BA B5 L7	"	BB B0 Y3	"	BB D4 L9	"	BD B4 L5
"	BA B5 L8	"	BB B0 Y4	"	BC A5 Y5	"	BD B4 L6
"	BA B5 L9	"	BB B4 L5	"	BC A5 Y6	"	BD B4 L7
"	BA B5 Y5	"	BB B4 L6	"	BC A5 Y7	"	BD B4 L8
"	BA B5 Y6	"	BB B4 L7	"	BC A5 Y8	"	BD B4 L9
"	BA B5 Y7	"	BB B4 L8	"	BC A5 Y9	"	BD B4 Y5
"	BA B5 Y8	"	BB B4 L9	"	BC B5 L5	"	BD B4 Y6
"	BA B5 Y9	"	BB B4 Y5	"	BC B5 L6	"	BD B4 Y7
"	BA C5 L5	"	BB B4 Y6	"	BC B5 L7	"	BD B4 Y8
"	BA C5 L6	"	BB B4 Y7	"	BC B5 L8	"	BD B4 Y9
"	BA C5 L7	"	BB B4 Y8	"	BC B5 L9	"	BD C0 L0
"	BA C5 L8	"	BB B4 Y9	"	BC B5 Y5	"	BD C0 L1
"	BA C5 L9	"	BB C0 L0	"	BC B5 Y6	"	BD C0 L2
"	BA C5 Y5	"	BB C0 L1	"	BC B5 Y7	"	BD C0 L3
"	BA C5 Y6	"	BB C0 L2	"	BC B5 Y8	"	BD C0 L4
"	BA C5 Y7	"	BB C0 L3	"	BC B5 Y9	"	BD C4 L5
"	BA C5 Y8	"	BB C0 L4	"	BC C5 L5	"	BD C4 L6

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ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1182 8985-29	BD C4 L7	1188 1067	BB D4 Y7	1188 1067	BD D0 Y3	1190 0768	BE C1 Y2
"	BD C4 L8	"	BD A4 L7	"	BF A0 L3	"	BE C1 Y4
"	BD C4 L9	"	BB D4 Y8	"	BD D4 Y7	"	BE C1 Y5
		"	BD A4 L8	"	BF A4 L7		
1188 1067	BA D5 Y7	"	BC D5 Y7	"	BD D4 Y8	1191 8299	BA A8 A7*
"	BC A5 L7	"	BE A5 L7	"	BF A4 L8	"	BA A9 A2*
"	BA D5 Y8	"	BC D5 Y8			"	BB D1 N7*
"	BC A5 L8	"	BE A5 L8	1190 0768	BE C1 L0	"	BC A8 A7*
"	BB D0 Y2	"	BC D5 Y9	"	BE C1 L2	"	BC A9 A2*
"	BD A0 L2	"	BE A5 L9	"	BE C1 L4		
"	BB D0 Y3	"	BD D0 Y2	"	BE C1 L5		
"	BD A0 L3	"	BF A0 L2	"	BE C1 Y0		
1180 1883-17	DA D6 L2	1180 1883-29	DA D4 Y3	1180 1883-29	DB D3 L6	1183 2698-04	DB D0 Y5
"	DA D6 L3	"	DA D4 Y5	"	DB D3 L7	"	DB D2 L0
"	DA D6 L4	"	DA D4 Y8	"	DB D4 L5	"	DB D1 Y9
"	DA D6 Y1	"	DA D4 Y9	"	DB D4 L6	"	DB D3 L9
"	DA D6 Y4	"	DA D5 L2	"	DB D4 L7	"	DA D2 L4
"	DA D7 L2	"	DA D9 L6	"	DC A3 L8	"	DA D3 L0
"	DA D7 L4	"	DA D9 L7	"	DC A4 L7	"	DA D4 Y0
"	DA D7 Y1	"	DA D9 L8	"	DC A5 L6	"	DA D9 Y9
		"	DA D9 L9	"	DC C3 L9		
1180 1883-20	DB D1 Y2	"	DA D9 Y7	"	DC D2 L3	1183 3829	DA D2 A7
"	DB D4 L8	"	DA D9 Y8	"	DC D2 Y3	"	DA D3 N7
"	DC C4 L9	"	DB D0 L0	"	DC D3 L2	"	DA D5 A7
		"	DB D0 L1	"	DC D3 Y2	"	DA D5 N2
1180 1883-25	DA D5 L0	"	DB D0 L3	"	DC D4 L1	"	DA D5 N7
"	DB D1 Y1	"	DB D0 L6	"	DC D4 Y1	"	DA D6 A7
		"	DB D0 Y6	"	DC D5 L0	"	DA D6 N7
1180 1883-29	DA D1 L6	"	DB D0 Y8	"	DC D5 L4	"	DA D7 N7
"	DA D1 L7	"	DB D1 L5	"	DC D5 Y0	"	DA D7 A7
"	DA D1 L9	"	DB D1 L6	"	DC D5 Y4	"	DB D0 N2
"	DA D2 L2	"	DB D1 L7			"	DB D2 N2
"	DA D2 L3	"	DB D1 L8	1193 3462	DA D2 Y9	"	DB D4 A2
"	DA D2 Y5	"	DB D1 L9	"	DA D4 L9		
"	DA D3 L2	"	DB D1 Y6	"	DA D7 L1	1183 2698-02	DA D5 L1
"	DA D3 L3	"	DB D1 Y7	"	DA D7 Y3		
"	DA D3 L5	"	DB D1 Y8	"	DB D0 Y7		
"	DA D3 L9	"	DB D2 L1	"	DB D3 L8		
"	DA D3 Y0	"	DB D2 L2				
"	DA D3 Y3	"	DB D2 L4	1182 8985-29	DC C3 Y3		
"	DA D3 Y4	"	DB D3 L4	"	DC C4 Y8		
"	DA D4 Y2	"	DB D3 L5				

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	EA C9 N7	1180 1883-29	EC D1 L8	1180 1883-29	ED D3 L3	1182 8985-29	EE A6 Y3
		"	EC D1 L9	"	ED D3 L4	"	EE A6 Y8
1180 1883-02	EC D6 Y3	"	EC D2 Y1	"	ED D3 L5	"	EE A7 L3
		"	EC D2 Y2	"	ED D3 L6	"	EE A7 Y7
1180 1883-04	EB D2 L4	"	EC D2 Y3	"	ED D3 L7	"	EE A8 L2
"	EB D2 Y4	"	EC D2 Y4	"	ED D3 Y3	"	EE A8 L6
"	ED D3 Y1	"	EC D3 L0	"	ED D3 Y4	"	EE A8 Y1
		"	EC D3 L1	"	ED D4 L5	"	EE A9 L5
1180 1883-17	EA D8 Y1	"	EC D3 L2			"	EE A9 L9
"	EC D7 Y0	"	EC D3 L3	1193 3462	EC D4 L0	"	EE A9 Y0
"	EC D7 Y1	"	EC D3 Y6	"	EC D4 Y5	"	EE A9 Y4
"	EC D7 Y2	"	EC D3 Y7	"	EC D6 L4	"	EE A9 Y9
"	EC D7 Y3	"	EC D3 Y8	"	EC D9 L0	"	EE B2 L3
"	EC D7 Y4	"	EC D3 Y9	"	EC D9 Y0	"	EE B2 Y3
"	EC D7 Y5	"	EC D4 L1	"	ED D3 L9	"	EE B3 L3
"	EC D7 Y6	"	EC D4 L2	"	ED D3 Y9	"	EE B3 L8
"	EC D7 Y7	"	EC D4 L3			"	EE B3 Y2
		"		1182 4448	EA C6 N7	"	EE B3 Y6
1180 1883-23	EB D1 L6	"	EC D4 L4	"	EA D7 N2	"	EE B4 L7
"	EB C0 Y0	"	EC D4 Y6			"	EE B4 Y5
"	EB C0 Y2	"	EC D4 Y7	1182 8985-04	EA C9 Y1	"	EE B4 Y9
		"	EC D4 Y8			"	EE B5 L1
1180 1883-25	EA C5 Y9	"	EC D4 Y9	1182 8985-20	EB C0 L7	"	EE B5 Y4
"	EB C0 Y1	"	EC D5 L6			"	EE B6 L0
		"	EC D5 L7	1182 8985-23	EA C9 Y3	"	EE B6 L4
1180 1883-28	EA D8 Y0	"	EC D5 L8	"	EB C0 L4	"	EE B6 L8
"	EB D1 L8	"	EC D5 L9	1182 8985-25	EB C0 L9	"	EE B6 Y3
		"	EC D9 L1			"	EE B6 Y8
1180 1883-29	EA D7 Y7	"	EC D9 L2	1182 8985-29	EA D8 Y2	"	EE B7 L7
"	EB D1 L7	"	EC D9 L3	"	EA D8 Y3	"	EE B7 Y7
"	EB D1 L9	"	EC D9 L4	"	EA D8 Y4	"	EE B8 L1
"	EB D1 Y9	"	EC D9 L5	"	EB D4 L7	"	EE B8 Y1
"	EB D2 L0	"	EC D9 L6	"	EB D4 Y6	"	EE B9 L0
"	EB D2 L1	"	EC D9 L7	"	EB D4 Y7	"	EE B9 L4
"	EB D2 L2	"	EC D9 L8	"	EE A2 L3	"	EE B9 L9
"	EB D2 L3	"	ED D1 L5	"	EE A2 Y3	"	EE B9 Y0
"	EB D2 Y0	"	ED D1 L6	"	EE A3 L3	"	EE B9 Y4
"	EB D2 Y1	"	ED D1 L7	"	EE A3 L8	"	EE B9 Y9
"	EB D2 Y2	"	ED D1 L8	"	EE A3 Y2	"	EF A0 Y8
"	EB D2 Y3	"	ED D2 L3	"	EE A3 Y6	"	EF B0 L8
"	EB D2 Y6	"	ED D2 L4	"	EE A4 L7	"	EF B0 Y8
"	EB D2 Y7	"	ED D2 L5	"	EE A4 Y5	"	EF B1 L8
"	EB D2 Y8	"	ED D2 L6	"	EE A4 Y9	"	EF B1 Y3
"	EB D2 Y9	"	ED D2 L7	"	EE A5 L1	1182 8985-35	EA C9 Y2
"	EB D3 Y0	"	ED D2 L8	"	EE A5 Y4	"	EA C9 Y4
"	EC D1 L6	"	ED D2 L9	"	EE A6 L0	"	EB C0 L3
"	EC D1 L7	"	ED D3 L0	"	EE A6 L4	"	EB C0 L5

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1182 8985-35	EB C0 L6	1183 2698-04	EC D4 L9	1183 3829	EC D7 A2	1184 4370	EC D3 N2
"	EB C0 L8	"	EC D5 L5	"	EC D7 A7	"	EC D5 A2
		"	EC D9 L9	"	EC D8 A2	"	EC D5 N7
1183 2698-04	EB D2 L5	"	ED D2 Y4	"	ED D0 A2		
"	EB D2 Y5	"	ED D3 L8	"	ED D2 N7	1188 1067	EA D6 Y4
"	EB D3 Y2	"	ED D3 Y0	"	ED D4 A2	"	EC A6 L4
"	EC D2 L4					"	EB D0 Y8
"	EC D3 Y5	1183 3829	EC D6 A7	1184 4370	EC D2 A7	"	ED A0 L8

Remove the following ground jumpers:

FROM PIN	Z LEVEL	TO PIN	Z LEVEL	FROM PIN	Z LEVEL	TO PIN	Z LEVEL
DC B6 X3	Z2	DC B6 Z4	Z1	DB D1 F6	Z2	DB C1 Z6	Z1
DC A6 U3	Z2	DC A6 Z0	Z1	DB D0 D2	Z2	DB C1 Z9	Z1
DC B6 T8	Z2	DC B6 Z8	Z1	EE D2 X3	Z1	EE C4 Z8	Z1
DC C3 V1	Z2	DC C3 Z9	Z1	EC D0 D8	Z2	EC C2 Z8	Z1
DC D6 H2	Z2	DC C5 Z9	Z1	EE A2 D3	Z1	EE A3 Z5	Z1
DC C4 V6	Z2	DC C4 Z8	Z1	EE A2 K3	Z1	EE A2 Z9	Z1
DA D1 E7	Z2	DA C2 Z1	Z1	EE A2 S3	Z1	EE A3 Z0	Z1
DD A3 F5	Z2	DD A3 Z5	Z1	EE A2 X3	Z1	EE A3 Z6	Z1
DC B9 H8	Z2	DC B9 Z7	Z1	EE B2 D3	Z1	EE B4 Z4	Z1
DB D4 D6	Z2	DB C4 Z6	Z1	EE B2 K3	Z1	EE B4 Z5	Z1
DB D4 F6	Z2	DB C4 Z5	Z1	EE B2 S3	Z1	EE B2 Z0	Z1
DB D1 D8	Z2	DB C1 Z8	Z1	EE B2 X3	Z1	EE B2 Z1	Z1
DB D4 D5	Z2	DB C4 Z4	Z1	EE C2 D3	Z1	EE B3 Z1	Z1
				EB A3 E1	Z1	EB A3 Z1	Z1

Instructions for Modification Kit N*

To Add DFC #2, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	DC C6 N2	1180 1883-25	DB B4 L9	1182 8985-29	DC C5 Y1	1182 8985-29	DC C7 Y1
"	DC C6 N7	"	DB C4 L9	"	DC C5 Y2	"	DC C7 Y2
"	DD A0 A7			"	DC C5 Y3	"	DC C7 Y3
		1180 1883-29	DB A1 Y3*	"	DC C5 Y4		
1180 1883-02	DC D1 Y8	"	DB B1 Y3*	"	DC C5 Y5	1183 3829	DC D6 A7
		"	DB C1 Y3*	"	DC C5 Y6		
1180 1883-04	DC C6 L2	"	DC D6 L1	"	DC C5 Y7	1190 0768	DC D1 Y0
"	DD A0 L2	"	DC D6 L2	"	DC C5 Y8	"	DC D1 Y1
"	DD A0 L3	"	DC D6 L3	"	DC C6 L3		
		"	DC D6 L4	"	DC C6 L5		
1180 1883-17	DA A6 Y2			"	DC C6 L6		
"	DA B6 Y2	1193 3462	DC C5 Y9	"	DC C6 L7		
"	DA C6 Y2	"	DC C6 L4	"	DC C6 L8		
				"	DC C6 L9		
1180 1883-25	DB A4 L9	1182 8985-04	DD A0 L4	"	DC C7 Y0		

Install cable 18-2:

Part Number	From D & D	To CC
1188 3444	DD K8	DC D0 N7

Remove the following ground jumpers:

DD A0 H9 Z2 to DD A0 Z3 Z1

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

Instructions for Modification Kit P

To add I/O-4 and DFC #2, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	DA D6 Y2	1180 1883-25	DB D4 L9	1180 1883-29	DB D1 Y3*

Instructions for Modification Kit R*

To add PTR #1, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	DD A2 A7	1180 1883-20	DB C1 L2	1180 1883-29	DA B4 Y4	1182 8985-29	DD A1 L7
"	DD A4 A7*			"	DA B4 Y6	"	DD A1 L8
"	DD A4 N7*	1180 1883-29	DA A1 L8	"	DA C1 L8	"	DD A1 L9
		"	DA A2 L0	"	DA C2 L0	"	DD A2 L0
1180 1883-04	DD A4 L3	"	DA A3 L4	"	DA C3 L4	"	DD A2 L1
		"	DA A3 Y1	"	DA C3 Y1	"	DD A2 L2
1180 1883-17	DA A7 L0	"	DA A4 Y4	"	DA C4 Y4	"	DD A2 L3
"	DA B7 L0	"	DA A4 Y6	"	DA C4 Y6		
"	DA C7 L0	"	DA B1 L8				
		"	DA B2 L0	1182 8985-04	DD A4 L4		
1180 1883-20	DB A1 L2	"	DA B3 L4				
"	DB B1 L2	"	DA B3 Y1	1182 8985-29	DD A1 L6		

Install cable 22:

Part Number	From D & D	To CC
1192 5062	DD K2	DC D0 A7

Remove the following ground jumpers:

DD A4 C5 Z2 to DD A4 Z8 Z1
DD A4 D7 Z2 to DD A4 Z9 Z1

Instructions for Modification Kit S

To add I/O-4 and PTR #1, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	DA D7 L0	1180 1883-29	DA D1 L8	1180 1883-29	DA D3 L4	1180 1883-29	DA D4 Y4
1180 1883-20	DB D1 L2	"	DA D2 L0	"	DA D3 Y1	"	DA D4 Y6

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

Instructions for Modification Kit T*

To add PTR #2, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	DD B0 N7*	1180 1883-20	DC B8 Y7	1180 1883-29	DB B1 Y4*	1182 8985-29	DD B1 Y7
"	DD B2 N2*			"	DB C0 L2*	"	DD B1 Y8
"	DD B3 N7*	1180 1883-25	DB A2 L3	"	DB C0 Y9*	"	DB B2 Y8
		"	DB B2 L3	"	DB C1 L3*	"	DD B2 Y9
1180 1883-04	DD B3 L7	"	DB C2 L3	"	DB C1 Y4*	"	DD B3 Y3
				"	DC B9 L7	"	DD B3 Y4
1180 1883-17	DA A6 Y3	1180 1883-29	DB A0 L2*	"	DC B9 L8		
"	DA B6 Y3	"	DB A0 Y9*			1183 2698-04	DD B2 Y5*
"	DA C6 Y3	"	DB A1 L3*	1182 8985-04	DD B3 L5*		
		"	DB A1 Y4*	"	DD B3 L6*	1183 3829	DC B9 N2*
1180 1883-20	DA A9 L5	"	DB B0 L2*				
"	DA B9 L5	"	DB B0 Y9*	1182 8985-29	DC B9 Y7		
"	DA C9 L5	"	DB B1 L3*	"	DD B1 Y2		

Install cable 11:

Part Number	From D & D	To CC
1188 3436	DD J8	DC A0 N7

Remove the following ground jumpers:

DD B3 R9 Z2 to DD B3 Z9 Z1
DD B3 W5 Z2 to DD B3 Z5 Z1

Instructions for Modification Kit U

To add I/O-4 and PTR #2, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	DA D6 Y3	1180 1883-25	DB D2 L3	1180 1883-29	DB D0 Y9*	1180 1883-29	DB D1 Y4*
1180 1883-20	DA D9 L5	1180 1883-29	DB D0 L2*	"	DB D1 L3*		

Instructions for Modification Kit V*

To add PTP #1, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	DD B2 A2	1180 1883-29	DB A0 Y9*	1180 1883-29	DC B9 L6	1182 8985-29	DD B1 L2
		"	DB A1 Y4*			"	DD B1 L3
1180 1883-17	DA A7 Y2	"	DB B0 Y9*	1182 8985-29	DD B0 L1	"	DD B1 L6
"	DA B7 Y2	"	DB B1 Y4*	"	DD B0 L2	"	DD B1 L7
"	DA C7 Y2	"	DB C0 Y9*	"	DD B0 L3	"	DD B2 L5
		"	DB C1 Y4*	"	DD B0 L4	"	DD B2 L6
1180 1883-20	DA A9 Y5	"	DC B8 L8			"	DD B2 L7
"	DA B9 Y5	"	DC B8 L9	1182 8985-29	DD B1 L0	"	DD B2 L8
"	DA C9 Y5	"	DC B9 L5	"	DD B1 L1		

Install cable 21:

Part Number	From D & D	To CC
1188 3451	DD J6	DC B0 A7

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

Instructions for Modification Kit W

To add I/O-4 and PTP #1, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	DA D7 Y2	1180 1883-20	DA D9 Y5	1180 1883-29	DB D0 Y9*	1180 1883-29	DB D1 Y4*

Instructions for Modification X*

To add PTP #2, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	DD B0 N7*	1180 1883-29	DB B1 L3*	1182 8985-29	DC B9 Y8	1182 8985-29	DD B2 Y6
"	DD B2 N2*	"	DB B1 Y3*	"	DD B0 Y0	"	DD B2 Y7
"	DD B3 N7*	"	DB C0 L2*	"	DD B0 Y1	"	DD B3 Y1
		"	DB C1 L3*	"	DD B0 Y2	"	DD B3 Y2
1180 1883-17	DA A7 A4	"	DB C1 Y3*	"	DD B0 Y3		
"	DA B7 Y4	"	DC B8 Y8	"	DD B0 Y4	1183 2698-04	DD B2 Y5*
"	DA C7 Y4	"	DC B8 Y9	"	DD B1 Y0		
		"	DC B9 Y5	"	DD B1 Y1	1183 3829	DC B9 N2*
1180 1883-29	DB A0 L2*	"	DC B9 Y6	"	DD B1 Y3		
"	DB A1 L3*			"	DD B1 Y4		
"	DB A1 Y3*	1182 8985-04	DD B3 L5*	"	DD B1 Y5		
"	DB B0 L2*	"	DD B3 L6*	"	DD B1 Y6		

Install cable 11:

Part Number	From D & D	To CC
1188 3436	DD J8	DC A0 N7

Remove the following ground jumpers:

DD B3 W5 Z2 to DD B3 Z5 Z1
DD B3 R9 Z2 to DD B3 Z9 Z1

Instructions for Modification Y

To add I/O-4 and PTP #2, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	DA D7 Y4	1180 1883-29	DB D0 L2*	1180 1883-29	DB D1 L3*	1180 1883-29	DB D1 Y3*

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

✓Instructions for Modification Kit AA*.

To add TTU-K, install the following pluggables:

ASSEMBLY NO.	LOCATION	ASSEMBLY NO.	LOCATION	ASSEMBLY NO.	LOCATION	ASSEMBLY NO.	LOCATION
1178 4147	EE C2 A7	1180 1883-29	EC B3 Y5	1180 1883-29	ED C3 L0	1182 8985-29	EE C7 L8
"	EE C4 A2	"	EC B4 L5	1182 8985-04	EF C2 L6	"	EE C7 L9
"	EE C5 A7	"	EC B4 Y5	1182 8985-29	EE C2 L0	"	EE C8 L0
"	EE C7 A2	"	EC B6 L0	"	EE C2 L1	"	EE C8 L2
"	EE C8 A7	"	EC B9 Y1	"	EE C2 L2	"	EE C8 L3
"	EF C0 A2	"	EC B9 Y5	"	EE C3 L0	"	EE C8 L4
"	EF C2 A2	"	EC C2 L0	"	EE C3 L1	"	EE C9 L1
"	EF C3 A7	"	EC C2 Y0	"	EE C3 L2	"	EE C9 L2
1180 1883-04	EF C2 L5	"	EC C3 L4	"	EE C3 L5	"	EE C9 L3
"	EF C2 L7	"	EC C3 Y5	"	EE C3 L6	"	EE C9 L6
"	EF C2 L8	"	EC C4 L5	"	EE C3 L7	"	EE C9 L7
"	EF C4 L0	"	EC C4 Y5	"	EE C3 L9	"	EE C9 L8
"	EF C4 L1	"	EC C6 L0	"	EE C4 L5	"	EF C0 L5
"	EF C4 L2	"	EC C9 Y1	"	EE C4 L6	"	EF C0 L6
1180 1883-17	EC A7 Y8	"	EC C9 Y5	"	EE C4 L8	"	EF C0 L7
"	EC B7 Y8	"	ED A0 Y9	"	EE C4 L9	1184 6532	EE C1 L2
"	EC C7 Y8	"	ED A1 Y0	"	EE C5 L0	1193 3462	EE C3 L4
1180 1883-29	EC A2 L0	"	ED A2 L1	"	EE C5 L2	"	EE C6 L9
"	EC A2 Y0	"	ED A2 Y5	"	EE C5 L3	"	EE C9 L5
"	EC A3 L4	"	ED A3 L0	"	EE C5 L4	"	EF C2 L9
"	EC A3 Y5	"	ED B0 L9	"	EE C6 L1		
"	EC A4 L5	"	ED B1 Y0	"	EE C6 L2		
"	EC A4 Y5	"	ED B2 L1	"	EE C6 L3		
"	EC A5 Y5	"	ED B2 Y5	"	EE C6 L5		
"	EC A9 Y1	"	ED B3 L0	"	EE C6 L6		
"	EC A9 Y5	"	ED C0 L9	"	EE C6 L7		
"	EC B2 L0	"	ED C1 Y0	"	EE C6 Y4		
"	EC B2 Y0	"	ED C2 L1	"	EE C7 L5		
"	EC B3 L4	"	ED C2 Y5	"	EE C7 L6		

Install cable 12-9:

Part Number	From D & D	To CC
1192 5039	DE M1	EE C0 A2

Remove the following ground jumper:

EF C2 C0 Z2 to EF C1 Z9 Z1

✓Instructions for Modification Kit AB*.

To add TTU-L, install the following pluggables:

ASSEMBLY NO.	LOCATION	ASSEMBLY NO.	LOCATION	ASSEMBLY NO.	LOCATION	ASSEMBLY NO.	LOCATION
1178 4147	EF C3 A2	1180 1883-17	EC A8 Y7	1183 3829	EC A8 A7	1184 6532	EE C1 L7
"	EF C4 A7	"	EC B8 Y7	"	EC B8 A7		
		"	EC C8 Y7	"	EC C8 A7		

✓Changes or additions since last issue

Install cable 12-10:

Part Number	From D & D	To CC
1192 5005	DE M2	EE C0 A7

Remove the following ground jumpers:

EF C3 C0	Z2	to	EF B3 Z8	Z1		EE C2 S1	Z1	to	EE B2 Z2	Z1
EE C2 K0	Z1	to	EE C2 Z8	Z1		EE C2 X1	Z1	to	EE B2 Z3	Z1
EE C2 S0	Z1	to	EE C2 Z9	Z1		EE C2 K2	Z1	to	EE B2 Z8	Z1
EE C2 X0	Z1	to	EE C2 Z0	Z1		EE C2 S2	Z1	to	EE B2 Z9	Z1
EE C2 K1	Z1	to	EE B3 Z9	Z1		EE C2 X2	Z1	to	EE B3 Z0	Z1

Instructions for Modification Kit AC*

To add TTU-M, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	EE C2 N7	1180 1883-29	EC B2 L1	1180 1883-29	ED C1 Y1	1182 8985-29	EE C5 Y2
"	EE C4 N2	"	EC B2 Y1	"	ED C2 L2	"	EE C5 Y3
"	EE C5 N7	"	EC B3 L5	"	ED C2 Y6	"	EE C6 Y0
"	EE C7 N2	"	EC B3 Y6	"	ED C3 L1	"	EE C6 Y1
"	EE C8 N7	"	EC B4 L6			"	EE C6 Y2
"	EF C0 N2	"	EC B4 Y6	1193 3462	EE C5 Y0	"	EE C6 Y5
"	EF C2 N2	"	EC B6 L1	"	EE C9 Y5	"	EE C6 Y6
"	EF C3 N7	"	EC B9 Y2	"	EE D6 L9	"	EE C6 Y7
		"	EC B9 Y6	"	EF C2 Y9	"	EE C6 Y9
1180 1883-04	EF C2 Y5	"	EC C2 L1	"	EE C1 Y9	"	EE C7 Y5
"	EF C2 Y7	"	EC C2 Y1			"	EE C7 Y6
"	EF C2 Y8	"	EC C3 L5	1182 8985-04	EF C2 Y6	"	EE C7 Y8
"	EF C4 Y0	"	EC C3 Y6			"	EE C7 Y9
"	EF C4 Y1	"	EC C4 L6	1182 8985-29	EE C2 Y0	"	EE C8 Y0
"	EF C4 Y2	"	EC C4 Y6	"	EE C2 Y1	"	EE C8 Y2
		"	EC C6 L1	"	EE C2 Y2	"	EE C8 Y3
1180 1883-17	EC A8 Y8	"	EC C9 Y2	"	EE C2 Y4	"	EE C8 Y4
"	EC B8 Y8	"	EC C9 Y6	"	EE C3 Y0	"	EE C9 Y1
"	EC C8 Y8	"	ED A1 L0	"	EE C3 Y1	"	EE C9 Y2
		"	ED A1 Y1	"	EE C3 Y3	"	EE C9 Y3
1180 1883-29	EC A2 L1	"	ED A2 L2	"	EE C3 Y4	"	EE C9 Y6
"	EC A2 Y1	"	ED A2 Y6	"	EE C3 Y5	"	EE C9 Y7
"	EC A3 L5	"	ED A3 L1	"	EE C3 Y7	"	EE C9 Y8
"	EC A3 Y6	"	ED B1 L0	"	EE C3 Y8	"	EF C0 Y5
"	EC A4 L6	"	ED B1 Y1	"	EE C3 Y9	"	EF C0 Y6
"	EC A4 Y6	"	ED B2 L2	"	EE C4 Y6	"	EF C0 Y7
"	EC A5 Y6	"	ED B2 Y6	"	EE C4 Y7	"	
"	EC A9 Y2	"	ED B3 L1	"	EE C4 Y8	1184 6532	EE C1 Y2
"	EC A9 Y6	"	ED C1 L0	"	EE C5 Y1		

Install cable 12-11:

Part Number	From D & D	To CC
1188 3576	DE M3	EE C0 N2

Remove the following ground jumper:

EF C2 R0 Z2 to EF C1 Z8 Z1

Instructions for Modification Kit AD*

To add TTU-N, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	EF C3 N2	1180 1883-17	EC A8 Y9	1180 1883-17	EC C8 Y9	1184 6532	EE C1 Y7
"	EF C4 N7	"	EC B8 Y9				

Install cable 12-12:

Part Number	From D & D	To CC
1192 5013	DE M4	EE C0 N7

Remove the following ground jumper:

EF C3 R0 Z2 to EF B3 Z9 Z1

Instructions for Modification Kit AE*

To add TTU-P, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	EE D2 A7	1180 1883-29	EC B2 Y2	1180 1883-29	ED C2 Y7	1182 8985-29	EE D6 L5
"	EE D4 A2	"	EC B3 L6	"	ED C3 L2	"	EE D6 L6
"	EE D5 A7	"	EC B3 Y7			"	EE D6 L7
"	EE D7 A2	"	EC B4 L7	1193 3462	EE D3 L4	"	EE D6 Y4
"	EE D8 A7	"	EC B4 Y7	"	EE D9 L5	"	EE D7 L5
"	EF D0 A2	"	EC B6 L2	"	EE D2 L9	"	EE D7 L6
"	EF D2 A2	"	EC B9 Y3			"	EE D7 L8
"	EF D3 A7	"	EC B9 Y7	1182 8985-04	EF D2 L6	"	EE D7 L9
		"	EC C2 L2			"	EE D8 L0
1180 1883-04	EF D2 L5	"	EC C2 Y2	1182 8985-29	EE D2 L0	"	EE D8 L2
"	EF D2 L7	"	EC C3 L6	"	EE D2 L1	"	EE D8 L3
"	EF D2 L8	"	EC C3 Y7	"	EE D2 L2	"	EE D8 L4
"	EF D4 L0	"	EC C4 L7	"	EE D3 L0	"	EE D9 L1
"	EF D4 L1	"	EC C4 Y7	"	EE D3 L1	"	EE D9 L2
"	EF D4 L2	"	EC C6 L2	"	EE D3 L2	"	EE D9 L3
		"	EC C9 Y3	"	EE D3 L5	"	EE D9 L6
1180 1883-17	EC A7 Y9	"	EC C9 Y7	"	EE D3 L6	"	EE D9 L7
"	EC B7 Y9	"	ED A1 L1	"	EE D3 L7	"	EE D9 L8
"	EC C7 Y9	"	ED A1 Y2	"	EE D3 L9	"	EF D0 L5
		"	ED A2 Y1	"	EE D4 L5	"	EF D0 L6
1180 1883-29	EC A2 L2	"	ED A2 Y7	"	EE D4 L6	"	EF D0 L7
"	EC A2 Y2	"	ED A3 L2	"	EE D4 L8		
"	EC A3 L6	"	ED B1 L1	"	EE D4 L9	1183 3829	EC A8 N2
"	EC A3 Y7	"	ED B1 Y2	"	EE D5 L0	"	EC B8 N2
"	EC A4 L7	"	ED B2 Y1	"	EE D5 L2	"	EC C8 N2
"	EC A4 Y7	"	ED B2 Y7	"	EE D5 L3		
"	EC A5 Y7	"	ED B3 L2	"	EE D5 L4	1184 6532	EE D1 L2
"	EC A9 Y3	"	ED C1 L1	"	EE D6 L1		
"	EC A9 Y7	"	ED C1 Y2	"	EE D6 L2		
"	EC B2 L2	"	ED C2 Y1	"	EE D6 L3		

Install cable 12-13:

Part Number	From D & D	To CC
1188 3550	DE M5	EE D0 A2

Remove the following ground jumpers:

EF	D2	C0	Z2	to	EF	C1	Z7	Z1	EE	D2	K1	Z1	to	EE	C3	Z7	Z1
EE	D2	D0	Z1	to	EE	C3	Z1	Z1	EE	D2	S1	Z1	to	EE	C3	Z8	Z1
EE	D2	K0	Z1	to	EE	C3	Z2	Z1	EE	D2	D2	Z1	to	EE	C3	Z9	Z1
EE	D2	S0	Z1	to	EE	C3	Z5	Z1	EE	D2	K2	Z1	to	EE	C4	Z6	Z1
EE	D2	D1	Z1	to	EE	C3	Z6	Z1	EE	D2	S2	Z1	to	EE	C4	Z7	Z1

Instructions for Modification Kit AF*

To add TTU-R, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	EF D3 A2	1180 1883-17	EC A8 Y5	1180 1883-17	EC C8 Y5	1184 6532	EE D1 L7
"	EF D4 A7	"	EC B8 Y5				

Install cable 12-14:

Part Number	From D & D	To CC
1188 3477	DE M6	EE D0 A7

Remove the following ground jumper:

EF D3 C0 Z2 to EF C1 Z5 Z1

Instructions for Modification Kit AG*

To add TTU-S, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	EE D2 N7	1180 1883-29	EC B2 L3	1180 1883-29	ED C2 Y2	1182 8985-29	EE D6 Y1
"	EE D4 N2	"	EC B2 Y3	"	ED C2 Y8	"	EE D6 Y2
"	EE D5 N7	"	EC B3 L7	"	ED C3 L3	"	EE D6 Y5
"	EE D7 N2	"	EC B3 Y8			"	EE D6 Y6
"	EE D8 N7	"	EC B4 L8	1193 3462	EE D1 Y9	"	EE D6 Y7
"	EE D0 N2	"	EC B4 Y8	"	EE D5 Y0	"	EE D6 Y9
"	EF D2 N2	"	EC B6 L3	"	EE D9 Y5	"	EE D7 Y5
"	EF D3 N7	"	EC B9 Y4	"	EF D2 Y9	"	EE D7 Y6
		"	EC B9 Y8			"	EE D7 Y8
1180 1883-04	EF D2 Y5	"	EC C2 L3	1182 8985-04	EF D2 Y6	"	EE D7 Y9
"	EF D2 Y7	"	EC C2 Y3			"	EE D8 Y0
"	EF D2 Y8	"	EC C3 L7	1182 8985-29	EE D2 Y0	"	EE D8 Y2
"	EF D4 Y0	"	EC C3 Y8	"	EE D2 Y1	"	EE D8 Y3
"	EF D4 Y1	"	EC C4 L8	"	EE D2 Y2	"	EE D8 Y4
"	EF D4 Y2	"	EC C4 Y8	"	EE D2 Y4	"	EE D9 Y1
		"	EC C6 L3	"	EE D3 Y0	"	EE D9 Y2
1180 1883-17	EC A8 Y6	"	EC C9 Y4	"	EE D3 Y1	"	EE D9 Y3
"	EC B8 Y6	"	EC C9 Y8	"	EE D3 Y3	"	EE D9 Y6
"	EC C8 Y6	"	ED A1 L2	"	EE D3 Y4	"	EE D9 Y7
		"	ED A1 Y3	"	EE D3 Y5	"	EE D9 Y8
1180 1883-29	EC A2 L3	"	ED A2 Y2	"	EE D3 Y7	"	EF D0 Y5
"	EC A2 Y3	"	ED A2 Y8	"	EE D3 Y8	"	EF D0 Y6
		"	ED A3 L3	"	EE D3 Y9	"	EF D0 Y7
1180 1883-29	EC A3 L7	"	ED B1 L2	"	EE D4 Y6		
"	EC A3 Y8	"	ED B1 Y3	"	EE D4 Y7	1184 6532	EE D1 Y2
"	EC A4 L8	"	ED B2 Y2	"	EE D4 Y8		
"	EC A4 Y8	"	ED B2 Y8	"	EE D5 Y1		
"	EC A5 Y8	"	ED B3 L3	"	EE D5 Y2		
"	EC A9 Y4	"	ED C1 L2	"	EE D5 Y3		
"	EC A9 Y8	"	ED C1 Y3	"	EE D6 Y0		

Install cable 12-15:

Part Number	From D & D	To CC
1188 3568	DE M7	EE D0 N2

Remove the following ground jumper:

EF D2 R0 Z2 to EF C1 Z6 Z1

Instructions for Modification Kit AH*

To add TTU-T, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	EF D3 N2	1180 1883-17	EC A6 Y9	1180 1883-17	EC C6 Y9	1184 6532	EE D1 Y7
"	EF D4 N7	"	EC B6 Y9				

Install cable 12-16:

Part Number	From D & D	To CC
1188 3493	DE M8	EE D0 N7

Remove the following ground jumper:

EF D3 R0 Z2 to EF C1 Z4 Z1

Instructions for Modification Kit AK

To add I/O-4 and TTU-K, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	EC D7 Y8	1180 1883-29	EC D6 L0	1182 8985-29	EE C2 L3	1182 8985-29	EE C7 L7
		"	EC D9 Y1	"	EE C3 L3	"	EE C8 L1
1180 1883-29	EC D2 L0	"	ED C4 Y0	"	EE C3 L8	"	EE C9 L0
"	EC D2 Y5	"	ED D0 L5	"	EE C4 L7	"	EE C9 L4
"	EC D3 L4	"	ED D1 L9	"	EE C5 L1	"	EE C9 L9
"	EC D4 L5	"	ED D2 Y0	"	EE C6 L0	"	EF C0 L8
"	EC D4 Y0	"	ED D3 L1	"	EE C6 L4		
"	EC D5 Y0	"	ED D3 Y5	"	EE C6 L8		

Instructions for Modification Kit AL

To add I/O-4 and TTU-L, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	EC D8 Y7	1183 3829	EC D8 A7

Remove the following ground jumpers:

EE C2 K3 Z1 to EE B3 Z2 Z1
EE C2 S3 Z1 to EE B3 Z5 Z1
EE C2 X3 Z1 to EE B3 Z6 Z1

Instructions for Modification Kit AM

To add I/O-4 and TTU-M, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	EC D8 Y8	1180 1883-29	EC D6 L1	1182 8985-29	EE C2 Y3	1182 8985-29	EE C7 Y7
		"	EC D9 Y2	"	EE C3 Y2	"	EE C8 Y1
1180 1883-29	EC D2 L1	"	ED C4 Y1	"	EE C3 Y6	"	EE C9 Y0
"	EC D2 Y6	"	ED D0 L6	"	EE C4 Y5	"	EE C9 Y4
"	EC D3 L5	"	ED D2 L0	"	EE C4 Y9	"	EE C9 Y9
"	EC D4 L6	"	ED D2 Y1	"	EE C5 Y4	"	EF C0 Y8
"	EC D4 Y1	"	ED D3 L2	"	EE C6 Y3		
"	EC D5 Y1	"	ED D3 Y6	"	EE C6 Y8		

Instructions for Modification Kit AN

To add I/O-4 and TTU-N, install the following pluggable:

ASSEMBLY #	LOCATION
1180 1883-17	EC D8 Y9

Instructions for Modification Kit AP

To add I/O-4 and TTU-P, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	EC D7 Y9	1180 1883-29	EC D6 L2	1182 8985-29	EE D2 L3	1182 8985-29	EE D7 L7
		"	EC D9 Y3	"	EE D3 L3	"	EE D8 L1
1180 1883-29	EC D2 L2	"	ED C4 Y2	"	EE D3 L8	"	EE D9 L0
"	EC D2 Y7	"	ED D0 L7	"	EE D4 L7	"	EE D9 L4
"	EC D3 L6	"	ED D2 L1	"	EE D5 L1	"	EE D9 L9
"	EC D4 L7	"	ED D2 Y2	"	EE D6 L0	"	EF D0 L8
"	EC D4 Y2	"	ED D3 Y1	"	EE D6 L4		
"	EC D5 Y2	"	ED D3 Y7	"	EE D6 L8	1183 3829	EC D8 N2

Remove the following ground jumpers:

EE D2 D3 Z1 to EE B3 Z7 Z1
EE D2 K3 Z1 to EE B3 Z8 Z1
EE D2 S3 Z1 to EE C4 Z9 Z1

Instructions for Modification Kit AR

To add I/O-4 and TTU-R, install the following pluggable:

ASSEMBLY #	LOCATION
1180 1883-17	EC D8 Y5

Instructions for Modification Kit AS

To add I/O-4 and TTU-S, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	EC D8 Y6	1180 1883-29	EC D6 L3	1182 8985-29	EE D2 Y3	1182 8985-29	EE D7 Y7
		"	EC D9 Y4	"	EE D3 Y2	"	EE D8 Y1
1180 1883-29	EC D2 L3	"	ED C4 Y3	"	EE D3 Y6	"	EE D9 Y0
"	EC D2 Y8	"	ED D0 L8	"	EE D4 Y5	"	EE D9 Y4
"	EC D3 L7	"	ED D2 L2	"	EE D4 Y9	"	EE D9 Y9
"	EC D4 L8	"	ED D2 Y3	"	EE D5 Y4	"	EF D0 Y8
"	EC D4 Y3	"	ED D3 Y2	"	EE D6 Y3		
"	EC D5 Y3	"	ED D3 Y8	"	EE D6 Y8		

Instructions for Modification Kit AT

To add I/O-4 and TTU-T, install the following pluggable:

ASSEMBLY #	LOCATION
1180 1883-17	EC D6 Y4

MODIFICATION INSTRUCTIONS - DRUM

Instructions for Modification Kit A.

To add DRUM #1, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	DC B5 N2	1180 1883-29	DA B2 L1	1180 1883-29	DB B1 Y5	1193 3462	DC B7 Y0
"	DC B6 A2	"	DA B3 L1	"	DB C0 L5		
"	DD A4 A7*	"	DA B3 Y2	"	DB C1 L4	1182 8985-29	DC B4 Y3
		"	DA B4 Y1	"	DB C1 Y5	"	DC B4 Y4
1180 1883-04	DD A4 L1	"	DA B4 Y7	"	DC B2 Y0	"	DC B4 Y5
		"	DA B9 Y6	"	DC B2 Y1	"	DC B4 Y6
1180 1883-17	DA A6 L1	"	DA C1 L5	"	DC B2 Y2	"	DC B4 Y7
"	DA B6 L1	"	DA C2 L1	"	DC B2 Y4	"	DC B4 Y8
"	DA C6 L1	"	DA C3 L1	"	DC B3 Y0	"	DC B6 Y0
		"	DA C3 Y2	"	DC B3 Y2	"	DC B6 Y1
1180 1883-29	DA A1 L5	"	DA C4 Y1	"	DC B3 Y4	"	DC B6 Y2
"	DA A2 L1	"	DA C4 Y7	"	DC B4 Y0		
"	DA A3 L1	"	DA C9 Y6	"	DC B4 Y1	1183 3829	DC B2 N7
"	DA A3 Y2	"	DB A0 L5	"	DC B6 Y5	"	DC B3 N7
"	DA A4 Y1	"	DB A1 L4	"	DC B6 Y6	"	DC B6 A7
"	DA A4 Y7	"	DB A1 Y5				
"	DA A9 Y6	"	DB B0 L5	1193 3462	DC B3 Y1		
"	DA B1 L5	"	DB B1 L4	"	DC B7 L0		

Install cable 23-1:

Part Number	From D & D	To CC
1188 3568	DD J5	DC B0 A2

Remove the following ground jumpers:

DD A4 D7 Z2 to DD A4 Z9 Z1
DD A4 C5 Z2 to DD A4 Z8 Z1

✓Instructions for Modification Kit I.

To add DRUM #2, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1178 4147	DC B5 A2	1180 1883-29	DC B2 L2	1193 3462	DC B3 L1	1182 8985-29	DC B4 L8
"	DD A4 N7*	"	DC B2 L4			"	DC B5 L6
		"	DC B3 L0	1182 8985-04	DD A4 Y3*	"	DC B5 L7
1180 1883-17	DA A6 Y0	"	DC B3 L2			"	DC B5 L8
"	DA B6 Y0	"	DC B3 L4	1182 8985-29	DC B4 L3		
"	DA C6 Y0	"	DC B4 L0	"	DC B4 L4	1183 3829	DC B2 A7
		"	DC B4 L1	"	DC B4 L5	"	DC B3 A7
1180 1883-29	DC B2 L0	"	DC B6 Y7	"	DC B4 L6		
"	DC B2 L1	"	DC B6 Y8	"	DC B4 L7		

NOTE: Those pluggables that have asterisks (*) are shared by other units and may be installed already.

✓Changes or additions since last issue

✓Install cable 23-2:

Part Number	From D & D	To CC
1188 3600	DD J7	DC B0 N2

✓Remove the following ground jumper:

DD A4 S7 Z2 to DD A3 Z9 Z1

Instructions for Modification Kit Q.

To add DRUM #1 and I/O-4, install the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	DA D6 L1	1180 1883-29	DA D3 Y2	1180 1883-29	DB D1 L4	1182 8985-29	DC B4 Y9
		"	DA D4 Y1	"	DB D1 Y5	"	DC B5 Y5
1180 1883-29	DA D1 L5	"	DA D4 Y7	"	DC B2 Y3	"	DC B6 Y3
"	DA D2 L1	"	DA D9 Y6	"	DC B3 Y3		
"	DA D3 L1	"	DB D0 L5	"	DC B4 Y2		

Instructions for Modification Kit Z.

To add DRUM #2 and I/O-4, add the following pluggables:

ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION	ASSEMBLY #	LOCATION
1180 1883-17	DA D6 Y0	1180 1883-29	DC B3 L3	1182 8985-29	DC B4 L9	1182 8985-29	DC B5 L9
		"	DC B4 L2	"	DC B5 L5		
1180 1883-29	DC B2 L3						

SECTION 6

CIRCUIT ANALYSIS

Refer to Section 6 of the B 5370 Power Supply Technical Manual for a description of the packages used in the Central Control Unit.

Printed in U.S.A.

SECTION 7

FUNCTIONAL DESCRIPTION

7.1 INTRODUCTION

GENERAL DESCRIPTION

The communication link and control center of a B5000 system is the Central Control Unit. This unit is divided into several logical sections which are as follows:

1. System Control
2. Interrupt Control
3. Memory Exchange
4. Input/Output Exchange
5. Miscellaneous Logic and Hardware

The System Control section of the Central Control Unit contains the logical circuitry for controlling LOAD, System Clock, Processor A (PA), Processor B (PB), and Processor 2. The Master Clock oscillator and Clock Drivers are also located in System Control.

The Clock Pulses are sent through the system to provide Clock Pulses for the units.

The only way an operator can start the System Clock is through the LOAD button on the Master Console. This logic clears the system and starts the Master Clock Pulses for the system.

The Interrupt Control section of Central Control provides logics to handle various unit Interrupts in a sequential priority-controlled arrangement. The center of Interrupt Control is the Interrupt Address Register.

When the Central Processor or I/O Control Unit develops a need for Interrupt action, the level is transmitted to the Central Control Unit and the Interrupt priority gates. These gates are so arranged as to permit the highest priority Interrupt to set a reference address into the Interrupt Address Register.

At the end of the execution of each syllable, Processor 1 interrogates the Interrupt Address Register. If the register is set to any number, Processor 1 will immediately execute the necessary steps to handle this Interrupt. If more than one Interrupt level is present, the Interrupts will be handled one at a time sequentially, on a priority scale until all Interrupts are processed. Once all Interrupts are handled by Processor 1, it signals the Processor Control section to return Processor 1 back to normal data processing.

The Memory Exchange provides linkage for information and control between a Memory Module and either a Processor or an I/O Control Unit. This type of exchange is referred to as "crosspoint connection" because of its ability to connect any one of 8 Memory Modules to any computer, or any one of the 4 channels within the I/O

Control Unit. The Memory Exchange also contains logic to establish priority and prevent multiple access of any connected unit. For example; one unit connected erroneously to two other units.

The Input/Output Exchange (referred to as I/O Exchange) is similar to the Memory Exchange except that its purpose is to provide a path for information and control signals between the I/O Control Unit and the peripheral equipment.

The Miscellaneous Logic and Hardware section of Central Control includes the following:

1. The Central Control Display and Control Panel.
2. Cable Interlocks and System Ready Logics (SNRD).
3. Incandescent Drivers.
4. I/O Designation.
5. Real Time Clock.

7.2 CLOCK CONTROL

GENERAL DESCRIPTION

The Clock Control involves the starting and transmitting of pulses to the system.

Clock Blocking Oscillator & Line Driver Package (DRBL)

Figure 7.2-1 illustrates the System Clock which is controlled by the Central Control unit. A 1 megacycle Master Oscillator which is running all the time that power is ON, drives four packages located in the Central Control unit. Each of these packages contain a Clock Blocking Oscillator and a Line Driver. The outputs of these drivers transmit pulses to local drivers in the system. Twisted-pair Clock cables of equal length radiate from the packages to the Local Clock Drivers throughout the system.

The Master Oscillator (CLSA) produces a square wave output which is an input to the DRBL. Each of these DRBL packages is controlled through an enabling input (Inhibit IN) by the state of a logical Clock Blocking Oscillator Switch (XX) CBOS.

Generally, the DRBLs are ON if either one of the Clock Control flip-flops (CL1F, CL2F) is on.

When operating, the DRBL supplies the essential clock streams for the Local Clock Drivers in each unit. The enabling input (Inhibit IN) to the DRBL is connected to switch (XX) CBOS. When (XX) CBOS is ON, its output is false, and the DRBL is inhibited (outputs always false). The (XX) CBOS is ON when its input is true.

(XX) CBOS SWITCH H (PACBOS, PBCBOS, CMCBOS, I_nCBOS)

-I- $\overline{CL1F} \cdot \overline{CL2F}$

Conversely, the (XX) CBOS will be OFF and the DRBL will be operating if either the CL1F or CL2F flip-flop is ON.

When operating, the Master Clock Pulse (MCLP-I(n) DRBL supplies the basic clock streams to the Local Clock Drivers in the I/O Control Units. The operation of the MnMCLP DRBL is analogous to that of the MCLP I(n).

The other two DRBL packages, PAMCLP and PBMCLP, each drive up to 13 to 16 Clock cables to the respective Processor units, designated PA and PB.

The PAMCLP and PBMCLP DRBLs are controlled respectively by the PACBOS and PBCBOS switches. Two conditions can turn ON the PACBOS to inhibit the PANCLP DRBL:

PACBOS SWITCH H

-I- + $\overline{CL1F} \cdot \overline{CL2F}$

+ $\overline{CL1F} \cdot$ PAIMCL

The first AND gate consists of the Clock Control condition. The PAIMCL term in the second AND gate is an Inhibit Master Clock signal, normally false, from Processor A.

PAIMCL becomes true when certain test conditions in the Processor are satisfied. For example, PAIMCL can become true at a selected J Register count and establish a dynamic HALT in that state by inhibiting clock pulses to the Processor. Such a HALTED condition can be overridden by setting the CL1F flip-flop (normally OFF) which always turns OFF the PACBOS switch. It will be seen that CL1F is the single pulse control flip-flop.

The PBMCLP DRBL is controlled analogously.

START CLOCK LOGIC

Depression Of A Start Clock Button

Several pushbuttons throughout the system can act as Start Clock buttons. The Start Clock button expected to be used the most is located on the Central Control Display Panel. Each Memory Unit and each Processor Unit Display Panel also has such a pushbutton.

The Start Clock buttons are normally open, so the lines coming from them are true in negative logic. The various Start Clock lines are bussed together along with a simple filter which is effective against contact bounce. The resultant signal can be referred to as SCLL (Start Clock Level), normally true.

SCLS SWITCH H

-I- + (XX) $\overline{\text{SCLL}} \cdot \overline{\text{LOYS}}$

+ CLEAR

When any Start Clock Button is depressed, (XX) $\overline{\text{SCLL}}$ goes false. SCLS will go true, and SCMM (Multi) will go true.

With the Start Clock Multivibrator (SCMM) true and $\overline{\text{MOSP}}$ true, the synchronizer is primed. As soon as $\overline{\text{MOSP}}$ goes false, SCLY will go true for 1 microsecond.

Setting The CL1F Flip-Flop

When SCLY and MOSP are true, the CL1F Flip-flop is set at the next pulse from the Clock Oscillator:

CL1F FLIP-FLOP 7

-S- SCLY $\cdot$ $\overline{\text{CL1F}} \cdot \overline{\text{MOSP}}$

The unclocked set input is used.

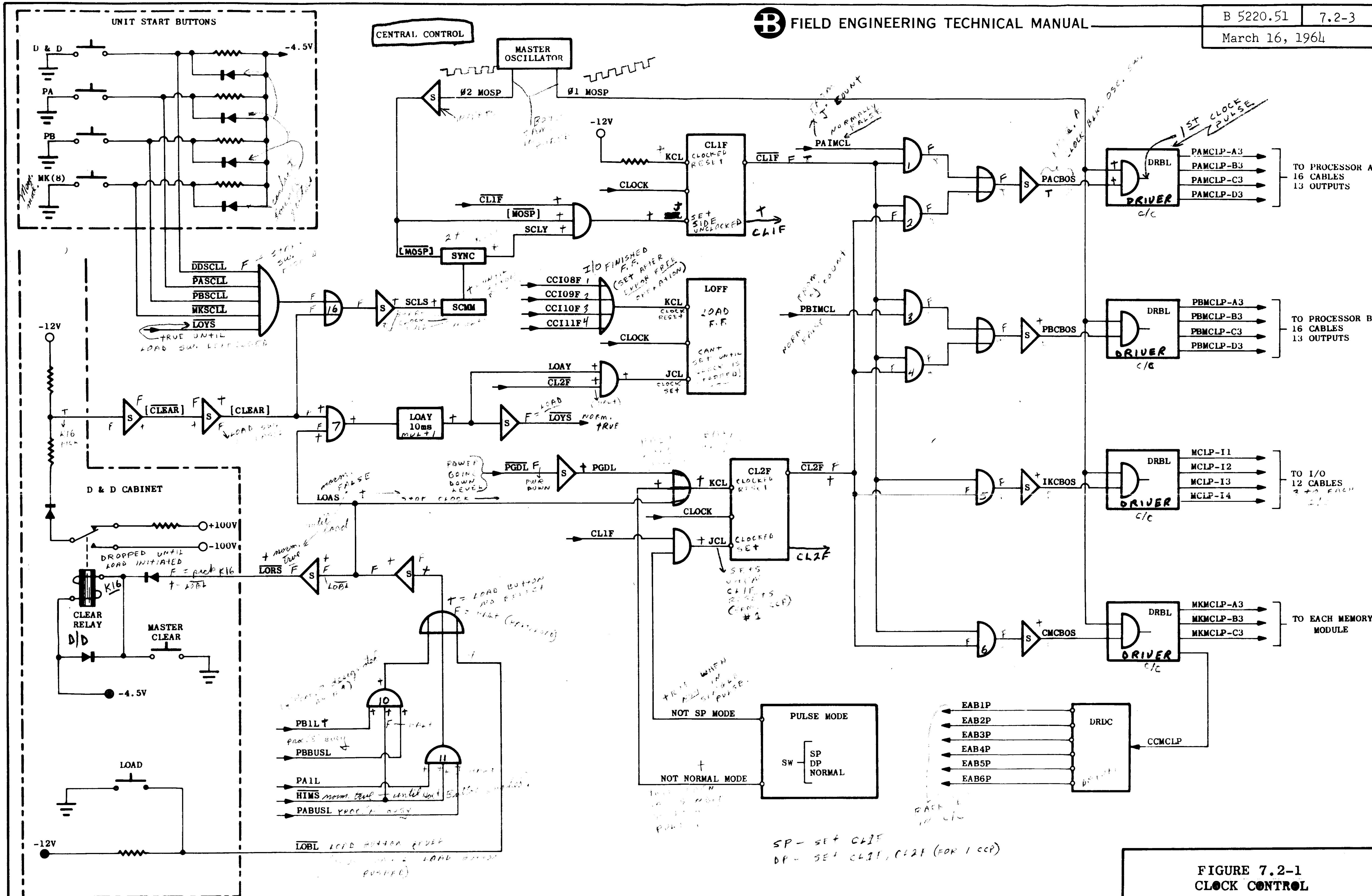


FIGURE 7.2-1
CLOCK CONTROL

First Clock Pulse

The DRBLs are enabled when the CL1F Flip-flop is ON and CL1F is false. The leading edge of the first oscillator pulse occurring when the CL1F Flip-flop is ON, is transformed into a System Clock pulse.

The first clock pulse always resets the CL1F Flip-flop. The gate into its clocked reset input can either be left open or connected to a true level such as CL1F. For Single Pulse Mode, refer to Figure 7.2-2.

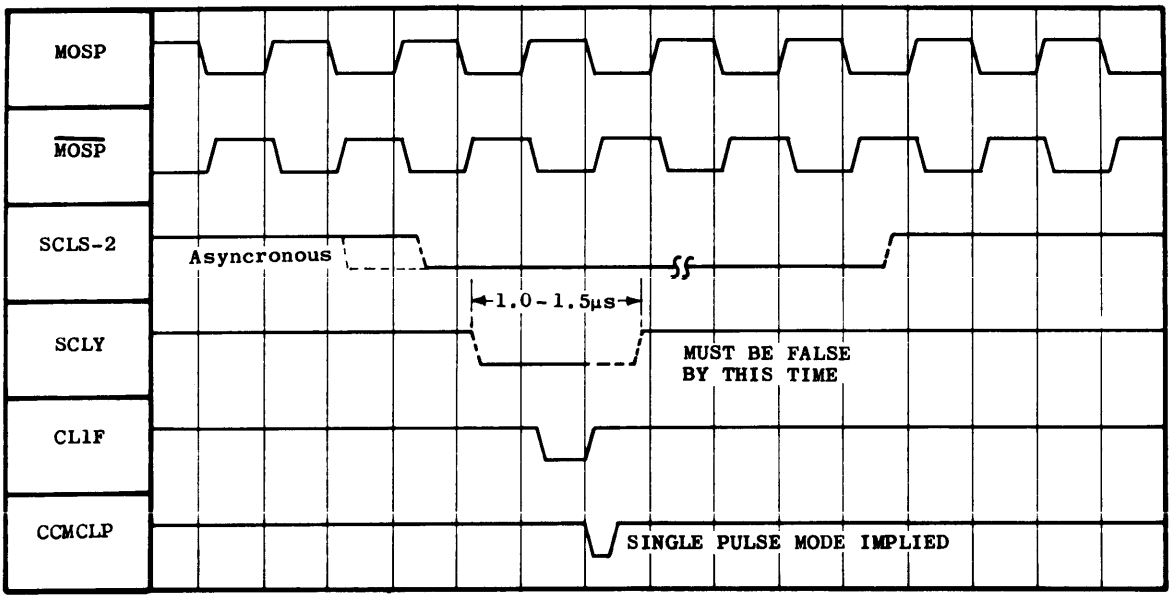


FIGURE 7.2-2 START CLOCK TIMING - SINGLE PULSE MODE

If the Clock Mode switch (a three-position toggle switch on the Central Control Display Panel) is in either the normal or the double-pulse position, then it is NOT in the single-pulse position, and the term NOT SP MODE is true. When both CL1F and NOT SP MODE are true, the CL2F Flip-flop is set.

CL2F FLIP-FLOP 7

-JCL- CL1F • NOT SP MODE

Second Clock Pulse

Because the CL2F Flip-flop normally enables the DRBLs, the second System Clock pulse is created only if the CL2F Flip-flop was set by the first clock pulse.

If the Clock Mode switch is in the double-uplse position, then the term NOT NORM MODE is true and the CL2F Flip-flop is reset.

CL2F FLIP-FLOP 7

-KCL- + NOT NORM MODE + PGDL + LOAS

It is in this way that the double-pulse facility is incorporated.

Subsequent Clock Pulses

Pulses from the DRBLs are sent throughout the system as long as the CL2F Flip-flop remains set (except when external signals act to inhibit the DRBLs).

To stop the stream of System Clock pulses, the CL2F Flip-flop can be reset 3 ways as follows:

CL2F FLIP-FLOP 7

-KCL- + NOT NORM MODE + PGDL + LOAS

1. NOT NORM MODE

   Manually setting the Clock Mode switch to either the single-pulse or the double-pulse position makes this term true.

2. PGDL

   This term is true at the beginning of a Power OFF sequence. Its function is to cause an immediate, neat STOP to system operation.

3. LOAS

   This term is true at the beginning of an initial LOAD operation (described later) prior to activation of the MASTER CLEAR bus. Like PGDL, the function of LOAS is to cause an immediate STOP to any system operation.

LOAD Operation

Refer back to Figure 2.4-1 which illustrates the following elements or logical levels which are important in beginning an initial LOAD cycle. The normal states are the unactivated states.

1. LOAS - LOAD activate switch. Normally ON.
2. LOAY DM C - LOAD activate delay circuit; nominal 10 ms holdover. Normally OFF.
3. $\overline{\text{LOBL}}$ - Level from LOAD button; normally true.
4. LOFF - LOAD Flip-flop, defines initial LOAD cycle. Normally OFF.
5. $\overline{\text{LORS}}$ - LOAD relay switch; when ON, operates the MASTER CLEAR relay. Normally OFF.
6. $\overline{\text{LOYS}}$ - Inverter for LOAD activate delay circuit; normally OFF.
7. $\overline{\text{HIMS}}$ - From HALT Immediate Switch, normally true, which indicates that the HALT button has NOT been depressed.

The switches referred to in the following text are simply used as buffers. The CLEAR SENSE signal is obtained from a divider which senses the state of the MASTER CLEAR bus. This bus is normally NOT activated.

1. $\overline{\text{CLLS}}$ - Inverter for buffering the CLEAR SENSE line. Normally OFF.

2. CLLS - Inverter for $\overline{\text{CLLS}}$ switch output. It produces logical signal CLEAR. Normally ON (CLEAR false).

Depression of LOAD Button

There are 2 normally-open LOAD buttons in the system. One is on the Operators Console, the other is on the Central Control Display Panel. They are connected in parallel and returned to ground so that the depression of either one of them makes the LOAD Button Level ($\overline{\text{LOBL}}$) appear false in a negative logic sense. A contact-bounce filter is connected to the line.

When a LOAD button is depressed, the $\overline{\text{LOBL}}$ input to the LOAS switch is false, and the LOAS switch will turn OFF unless Processor 1 in the system is operating.

LOAS SWITCH H

-I- + $\overline{\text{LOBL}}$

+ PA1F • PABUSL • $\overline{\text{HIMS}}$

+ PB1L • PBBUSL • $\overline{\text{HIMS}}$

The system is presumably BUSY if the Processor 1 is operating, in which case the LOAD order should be ignored. A LOAD cycle will be initiated only if the LOAS switch is turned OFF. If Processor 1 is operating, then it is necessary to depress the HALT button before starting a LOAD operation.

System Clear

When the Master Clear relay is operated, all flip-flops in the system receive a CLEAR signal through their manual control inputs.

Before beginning a LOAD operation, it is desirable to clear the system in order to insure an inactive system status. Because there is no CLEAR button on the Console, the LOAD button has a logical capability of operating the Master Clear relay. When LOAS is true, the $\overline{\text{LORS}}$ switch is turned ON.

LORS SWITCH H

-I- LOAS

The $\overline{\text{LORS}}$ switch provides a ground return for the coil of the Master Clear relay. The relay will operate within a few milliseconds, and it will remain in operation as long as the LOAD button is held down. The logical signal CLEAR will also be true at this time.

LOAD Activate Delay (Holdover)

The LOAY holdover circuit receives an input when LOAS and CLEAR are true.

LOAY DM J

-I- LOAD • CLEAR

The output signal LOAY is inverted by the LOYS switch to produce the level $\overline{\text{LOYS}}$ which is now false.

At the input to the SCLS switch, $\overline{\text{LOYS}}$ makes the AND gate $\overline{\text{LOYS}} \cdot \overline{\text{SCLL}}$ false, just as $\overline{\text{SCLL}}$ did when a Start Clock button was depressed. However, the true signal CLEAR, preceding the false signal $\overline{\text{LOYS}}$, holds the SCLS switch in its normally ON state.

Release of LOAD Button

The states described above are maintained until the LOAD button is released. When it is released, $\overline{\text{LOBL}}$ is true, and the following actions ensue:

1. The LOAS switch turns ON, making LOAS false.
2. The LOAY DM enters its holdover period.
3. The $\overline{\text{LORS}}$ switch turns OFF.
4. The Master Clear relay releases.
5. CLEAR becomes false.

Before the LOAY DM times out, there should be a period when both CLEAR and $\overline{\text{LOYS}}$ are false. Such a condition turns OFF the SCLS switch.

SCLS SWITCH H

-I- + $\overline{\text{SCLL}} \cdot \overline{\text{LOYS}}$

+ CLEAR

Consequently, the CL1F and then the CL2F Flip-flops are set, and clock pulses are delivered to the system.

Setting the LOFF Flip-Flop

The LOFF Flip-flop is set by the first System Clock pulse after the LOAD button is released.

LOFF FLIP-FLOP 7

-JCL- LOAY • $\overline{\text{CL2F}}$

Note that the LOAY DM delay period must overlap the first clock pulse.

The LOFF Flip-flop being ON starts the initial LOAD cycle and subsequently defines this cycle. The LOFF Flip-flop is reset after the error-free read-in of the starting program.

✓Delayed Clock Pulse

A delayed clock is produced in Central Control to set the Crosspoint flip-flops between normal clock pulses.

In Figure 7.2-3, the output of the DRDC (Local Clock Driver), in the A Rack of Central Control, is delayed .5 usec by a DRSB (Strobe Driver). This driver feeds the input to a MUFW (Multi, Type W) which controls the width of the delayed clock pulse. A VB (Variable Bias) package gives the delayed clock a -.5 false level. Adjustment of the delayed clock is covered in Section 3.5.

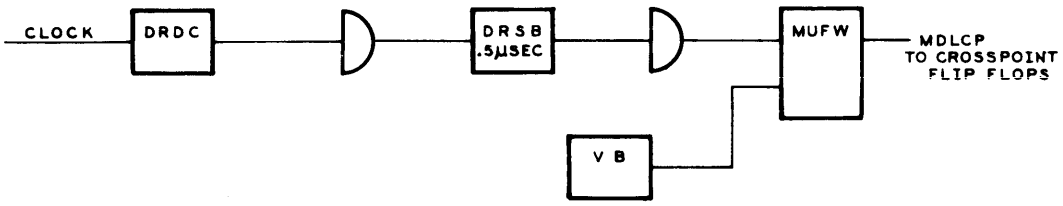


FIGURE 7.2-3 DELAYED CLOCK PULSE

✓Changes or additions since last issue.

7.3 PROCESSOR A, PROCESSOR B, and PROCESSOR 2 CONTROL

INTRODUCTION

Two Processors can be placed on the B 5000 System and are labeled PA or PB by the physical position of plugging into Central Control.

Figure 7.3-1 illustrates logical circuitry for the Processors. Either one of these Processors can be designated P1 or P2 by a toggle switch which is located on the Central Control Display Panel in the Display and Distribution cabinet. Therefore, PA or PB refer to a physical Processor, and P1 or P2 refer to a functional Processor.

P1 can only be initiated upon completion of a successful LOAD operation and P2 can only be initiated by an Initiate P2 operator from P1.

P2 Control performs the following functions:

1. The necessary means of halting P2 when told to do so.
2. Indications that P2 is halted.
3. The P2 busy logics.
4. Control when an Interrupt occurs in P2.

If P1 must halt, the P2, HP2F Flip-flop is turned ON and signals P2. P2 may not be able to halt as soon as it is told to do so, therefore, an indication of when it does halt is necessary for P1.

If P2 comes up with an Interrupt condition during an operation, P1 must handle the Interrupt, but not until AFTER P2 has completed its HOUSEKEEPING.

If P2 is busy and an Initiate P2 operator comes up in P1, an Interrupt must be set to signal P1.

PA and PB Control

A Processor which is plugged into the PA location of Central Control can be designated as P1 or P2. This is accomplished by a toggle switch in the Display & Distribution cabinet which produces one of two levels, PA1L or PB1L, depending on the position of the switch.

If the switch is in the PB1L position, the PB1L line is true and indicates that PB is P1. At the same time the line PA1L would be false, thus indicating that PA is not P1, and therefore must be in P2. PA1L and PB1L are sent to their respective Processors as well as Central Control to designate which Processor is P1.

Each Processor is initiated by a term CAAPKD or CBAPKD although the logic originating the initiation may be under different circumstances.

P1 may ONLY be initiated upon the successful completion of a LOAD operation.

CAAPKD is TRUE (assuming that PA is designated P1) when; LOFF, PA1L and one (1) of the four (4) I/O finished Interrupts flip-flop is set ON (indicating LOAD completed) and PA is available.

If PB was designated P1 (PB1L TRUE), then the line PA1L would be false and PA, now being P2, could not be initiated by a LOAD operation.

The level $\overline{\text{PAAVLL}}$ from PA is false if the Processor which holds PAAVLS OFF is available thus making its output PAAVLS, true, and indicating its availability.

Assuming that PA is designated P2, then it can be initiated by an Initiate P2 operator in P1. This is accomplished in the following manner: BPMCIL, which is a level from PB (P1), is held false. This holds $\overline{\text{CMIS}}$ OFF, and the output $\overline{\text{CMIS}}$ (Commence I/O Switch Not) is true. At the same time a level PBCMTL permits CMTF (Commence Timing Flip-flop) to be clocked ON. These two levels along with PAAVLS, $\overline{\text{LOFF}}$ (Load Not), $\overline{\text{P2BF}}$ (P2 NOT BUSY) and PB1L, will permit APKD-A to be true and initiate P2 (PA). CMTF is clocked OFF at the next pulse which permits PAAPKD true for 1 μs.

Whenever P2 is initiated, Central Control must remember that such a signal was sent to P2. This is accomplished by P2BF (P2 Busy Flip-flop) and is turned ON with the same signal (APKD-A or B) which initiates P2. The APKD lines used to set P2BF are ANDED with a term which says the other Processor is P1 thus insuring against setting P2BF following a LOAD operation.

P2BF may ordinarily be reset by two different types of conditions:

1. After P2 has Halted following a HALT signal from P1.
   HP2F and $\overline{\text{Pk2AB}}$ (Pk is No. 2, available and not busy) K = A or B.

2. After P2 has halted following an Interrupt within P2.
   PkINT and $\overline{\text{Pk2AB}}$.

The HALT P2 Flip-flop (HP2F) is turned ON whenever it is necessary for P1 to cause P2 to stop processing. P1 will send a signal PkHP2L to set HP2F = 1, which in turn signals P2 (via HP2S-k) to stop processing.

Although P2 has been told to HALT, it cannot do so immediately. It must complete the syllable it is executing and then store its registers in preparation for examination by P1. This HOUSEKEEPING may take from 20 to 300 μs. P1 will idle during this time and wait for P2 to signal that it has stopped.

The signal for P2 to HALT and the signal that P2 has stopped comes from two switches, CAHP2S and CBHP2S. If PB1L is true, CAHP2S signals P2 to HALT and CBHP2S will signal P1 that P2 has stopped. To make CAHP2S true, the logic basically is HP2F = 1 and PA1L false. This will then tell PA (P2) to HALT.

The logic necessary to tell PB (P1) that P2 has stopped is HP2F = 1 and P2BF = 0. P2BF is reset (= 0) when P2 becomes NOT busy and HP2F = 1.

PROCESSOR A

PROCESSOR B

D & D

-4.5V

PB1L

PA1L

CAHP2S

CAAPKD

PABUSL

PABUSS

PAAVLL

PAAVLS

PACMTL

PACMIL

PBCMIL

PBCMTL

PBAVLL

PBAVLS

PBBUSL

PBBUSS

CBAPKD

CBHP2S

C M T F

CMTF

CMIS

PB1L

P2BF

LOFF

CCI04F (I/O BUSY)

CCI11F

CCI10F

CCI09F

CCI08F

PA LOAD

PB LOAD

LOAD F.F.

PA2AB

PB2AB

PA INT.

PB INT.

HP2F

PAHP2L

PBHP2L

P2BF

CBHP2S

HP2F

† = P2 BUSY OR N/AVAIL.

(P2 BUSY)

FIGURE 7.3-1
PA, PB & P2 CONTROL

HP2F can be reset by an initiate P2 operator in P1.

When an Interrupt condition occurs in P2, the level PkINT will be true. This primes P2BF for being reset as soon as P2 goes NOT busy. The Interrupt condition also gates itself (P2) to do its own HOUSEKEEPING.

After completing the HOUSEKEEPING, P2 will go NOT busy ($\overline{\text{PkBUSS}}$ True) which will make the level $\overline{\text{Pk2AB}}$ true and permit P2BF to be reset. As soon as P2BF goes OFF, the P2 Interrupt will take its place in line of priority if other Interrupts exist.

P2 will then idle until again initiated from P1.

HALT P2 and P2 BUSY Logic

The P2 BUSY Flip-flop (P2BF) is turned ON at the time PA activates PB, or PB activates PA, depending upon which one is controlling Processor 1.

Ordinarily, P2BF will be turned OFF when ANY P2 Interrupt occurs. When P2 completes its program a COMMUNICATION OPERATOR Interrupt occurs causing either PA INT or PB INT term to be true.

The HALT P2 Flip-flop (HP2F) is turned ON when it is necessary for P1 to cause P2 to stop processing. Located in the Interrupt section is a Real-Time-Clock. The length of time ordinarily required by P2 to complete a program is contained in the Operations Log of the Master Control Program.

P1 can compare the elapsed time of the P2 program currently running (by means of the Real-Time-Clock) with the maximum time requirements as indicated by the Master Control Program.

If P2 exceeds the maximum time, P1 may HALT P2 by turning HP2F ON. HP2F will remain ON until P1 again activates P2. It is necessary for HP2F to remain ON at least until P2 reaches the end of its syllable. This permits P1 to continue processing during the time P2 is completing its syllable. This time may be considerable during some character mode syllables. At the completion of the syllable, P2 will store its registers and become NOT busy. There will be no Interrupt. P2BF will be clocked OFF as soon as the NOT Busy line from P2 becomes true.

The switch P2BS, used in the P2 BUSY Interrupt Flip-flop gate, may indicate three (3) BUSY conditions. P2BS will be true if:

1. P2BF is ON, or
2. P2 is BUSY (PA1L and PB BUSY or PB1L and PA BUSY), or
3. P2 is NOT available (PA1L and PB not available or PB1L and PA not available.

7.4 I/O SELECTION

INTRODUCTION

In order for an I/O Control Unit to be initiated, it must receive an Initiate I/O Level (PA or PB CMIL) from the controlling Processor (P1) and the Commence Timing Level (PA or PB CMTL).

Operation of I/O Selection

Refer to Figure 7.4-1 for the logical circuitry of the I/O Selection.

The Initiate I/O Level from P1 sets $\overline{\text{CMIS}}$ switch false and the Commence Timing Level turns ON the CMTF in Central Control which together provide a Starting Level to the I/O. The Processor 1 does not control the selection of the I/O to be initiated.

Selection of the I/O to be initiated is determined in Central Control. The lowest numbered I/O that is available and NOT BUSY will be selected when an Initiate Level is received from the controlling Processor.

If all I/O Units are NOT BUSY, I/O-1 will receive the Initiate Level. If I/O-1 is not available and I/O-2 is BUSY, then I/O-3 will receive the Initiate Level. If all I/O Units are BUSY when the Initiate Level is received, an I/O BUSY Interrupt will be set by the Initiate Level.

During an operating program, the I/O Unit receiving the Initiate Level will request Memory Cell 0008 in MEM-0 to obtain the Address location of the I/O Descriptor. Coincident with the Initiate Level to the I/O, a BUSY Flip-flop (ADnF) will be set in Central Control. When the I/O has completed the execution of its descriptor, an I/O Finished Interrupt will be SET. The BUSY Flip-flop will be RESET at this time.

There are four (4) BUSY switches; I1BS, I2BS, I3BS and I4BS.

If any one of the following conditions exist, I1BS will be true, and I/O-1 will be BUSY.

1. If I/O-1 is NOT available.
2. If the I/O-1 BUSY Flip-flop (AD1F) is ON.
3. If the I/O-1 Finished Interrupt (CCI08F) is ON.

If any one of the following conditions exist, I2BS will be true, and I/O-2 will be BUSY.

1. If I/O-2 is NOT available.
2. If the I/O-2 BUSY Flip-flop (AD2F) is ON.

3. If the I/O-2 Finished Interrupt (CCIO9F) is ON.

4. If I/O-1 is NOT BUSY.

   a. If I/O-1 is BUSY, then I2BS may indicate a NOT BUSY condition for I/O-2 depending upon the remaining terms of the I2BS equation.

I3BS and I4BS are logically similar to I2BS except for the additional InBS terms.

In the case of I4BS, it may only indicate a NOT BUSY condition if the other three (3) BUSY switches are true.

The four (4) AVAILABLE switches (InAVLS) generally indicate the physical availability of the I/O Control Units.

I1AVLS will be true to indicate I/O-1 is available if the term $\overline{\text{I1REMF}}$ is held false by a line from I/O-1 . If the line from I/O-1 is true or not present, the I1AVLS switch will be false to indicate the non-availability of the unit. I1AVLS will also be driven false during a LOAD operation if an error is sensed in the D Register of I/O-1.

I2AVLS, I3AVLS and I4AVLS are similar to I1AVLS and are used with I/O-2, I/O-3 and I/O-4 Control Units respectively.

In order for the controlling Processor (P1) to initiate I/O-1, the switch ADNS-1 must be made true for a duration of 1 μs. The Initiate I/O operator from P1 will provide a level, PkCMIL, to cause the switch CMIS to be false. During the execution of the Initiate I/O operator from P1, a 1 μs initiate level (PkCMTL) will be provided by P1. PkCMTL will turn ON the CMTF Flip-flop for a single microsecond. CMTF gates itself OFF.

ADNS-1 will be true during the microsecond that CMTF is ON. Therefore, to initiate I/O-1, it is necessary that I/O-1 is NOT BUSY (I1BS false); that there is an Initiate I/O operator level ($\overline{\text{CMIS}}$ false); and that the Initiate Flip-flop (CMTF) is ON.

If at the time the CMTF is turned ON, I/O-1 is BUSY and I/O-2 is NOT BUSY, I/O-2 will receive the Initiate Level via ADNS-2.

The other I/O Control Units are initiated in the same manner. The ADNS-n switches also gate the I/O BUSY Flip-flops in Central Control (ADnF). AD1F will be turned ON at the time I/O-1 is initiated. The BUSY switch I1BS will indicate I/O-1 is BUSY during the time AD1F is ON. The finished level from I/O-1 will turn ON the Finished Interrupt Flip-flop for I/O-1 (CCIO8F). AD1F will be turned OFF 1 μs later.

The I/O will appear to be BUSY until the finished Interrupt CCIO8F has been turned OFF. The following paragraphs explain the reason for causing the I/O to be BUSY until the Interrupt has been cleared.

At the time the I/O completes its operation, it WRITES a result descriptor in an appropriate cell in Memory (0014 thru 0017) and signals that it is FINISHED by setting an appropriate Finished Interrupt. P1 must be prevented from initiating this I/O again until the Result Descriptor has been sampled. If P1 were permitted to initiate the I/O as soon as the I/O was finished, the I/O might WRITE another Result Descriptor into the appropriate cell in Memory and destroy a previously written descriptor that had not been sampled by P1.

I/O-1
I/O-2
I/O-3
I/O-4
C1ADNS
C2ADNS
C3ADNS
C4ADNS
I1REMF
I2REMF
I3REMF
I4REMF
I1DERS
I2DERS
I3DERS
I4DERS
LOFF
I1AVLS
I2AVLS
I3AVLS
I4AVLS
I1BS
I2BS
I3BS
I4BS
AD1F
AD2F
AD3F
AD4F
CCI08F
CCI09F
CCI10F
CCI11F
CMIS
CMTF
C1LOTS
C2LOTS
C3LOTS
C4LOTS
PROCESSOR "A"
D & D
PROCESSOR "B"
PACMIL
PACMTL
PA1L
PB1L
PBMCIL
PBMCTL
CCI04F
(I/O BUSY)
I1FINL
I2FINL
I3FINL
I4FINL

FIGURE 7.4-1
I/O SELECTION

To LOAD the Master Control Program (MCP) into the first 512 words of Memory, a different method of I/O selection is used other than the one previously described.

With the system idle, the LOAD button on the Operators Console is pressed. The Clock and the LOAD Flip-flop (LOFF) is turned ON. No ADnFs will be ON, therefore, CMTF will be turned ON.

$\overline{\text{CMIS}}$ will be gated false by LOFF to prevent a normal I/O Initiate. The lowest numbered I/O Control Unit will receive a 1 μs gate from a LOTS switch. If I/O-1 is available, it will receive a 1 μs level from LOTS-1.

If I/O-1 is NOT available, but I/O-2 is available, then I/O-2 will receive a 1 μs level from LOTS-2.

The gating to LOTS-3 and LOTS-4 is similar.

At the same time that the selected I/O is initiated; the corresponding ADnF (BUSY Flip-flop) is turned ON to prevent further LOADS from taking place. CMTF is inhibited.

The I/O receiving the initiate LOAD will begin reading a program from either Drum 1 or Cards, depending upon the position of either the LOAD from Drum or LOAD from Cards switch on the Operators Console. The program will be READ into consecutive Memory locations beginning with cell 0016.

Upon completion of the LOAD operation, the I/O will set its finished Interrupt. The LOAD Flip-flop (LOFF), BUSY Flip-flop (ADnF) and the Interrupt Bit (CCInnF) will be turned OFF with the next Clock Pulse.

P1 will be initiated at this time by PAAPKD or PBHPKD depending upon which Processor is P1.

7.5 INTERRUPT CONTROL

INTRODUCTION

An Interrupt system furnishes a means for continuous automatic recognition of exception conditions which otherwise would have to be checked programmatically at intervals.

The Interrupt system is capable of automatically responding or recognizing External (not in the program) EXCEPTION signals and Processor dependent EXCEPTION signals which are those generated by the program itself.

It is now apparent that two distinct areas are necessary for recognizing these basic types of Interrupts; one for External Interrupts and one for Internal Interrupts.

The External Interrupts are temporarily stored in flip-flops in Central Control. Internal, or Processor dependent Interrupts are temporarily stored in flip-flops in the Processor itself.

The presence of Interrupt conditions existing is recognized by the Central Control which returns a signal to P1.

P1, at each SECL time, interrogates to see if this Interrupt signal exists. If an Interrupt does exist, P1 will prepare itself to handle this EXCEPTION condition by storing its registers etc.

Associated with each possible Interrupt is an Address unique to the Interrupt, to which the Processor may branch to the Master Control Program for the purpose of determining the nature of the Interrupt.

It is possible to have a second Processor which may have Interrupts generated within itself, as with P1. Unlike P1, P2 CANNOT handle its own Interrupt conditions. Again, P1 must handle these conditions.

There are now three (3) areas of Interrupt origin. The need is now evident for an Interrupt Priority system because of the different areas in which Interrupts occur, and because they are asynchronous to one another.

With the exception of P1 Memory Parity Error Interrupt and P1 Invalid Address Interrupt, the External Interrupts have higher priority than Processor Interrupts. All P2 Interrupts have the next priority and P1 Interrupts are generally of the lowest priority.

There are three (3) general classifications of Interrupts:

1. External
2. Processor 2.
3. Processor 1.

Table 7.5-1 lists the Interrupts in priority sequence, with their Address location and designation. Also, this list shows the Memory Address location with the derivation of the base figures for Address location.

TABLE 7.5-1 INTERRUPTS AND ADDRESS LOCATIONS

OCTAL ADDRESS	DECIMAL ADDRESS	UNIT	NO.	FUNCTION	SYLLABLE DEPENDENT
60	48	Pk	I01F	P1 MEMORY PARITY ERROR	
61	49	Pk	I02F	P1 INVALID ADDRESS	
22	18	CC	I03F	TIME INTERVAL	
23	19	CC	I04F	I/O BUSY	
24	20	CC	I05F	KEYBOARD REQUEST	
25	21	CC	I06F	PRINTER #1 FINISHED	
26	22	CC	I07F	PRINTER #2 FINISHED	
27	23	CC	I08F	I/O-1 FINISHED	
30	24	CC	I09F	I/O-2 FINISHED	
31	25	CC	I10F	I/O-3 FINISHED	
32	26	CC	I11F	I/O-4 FINISHED	
33	27	CC	I12F	P2 BUSY	
34	28	CC	I13F	INQUIRY REQUEST	
35	29	CC	I14F	SPECIAL INTERRUPT 1	
36	30	CC	I15F	SPECIAL INTERRUPT 2	
37	31	CC	I16F	SPECIAL INTERRUPT 3	
40	32	Pk	I01F	P2 MEMORY PARITY ERROR	
41	33	Pk	I02F	P2 INVALID ADDRESS	
42	34	Pk	I03F	P2 STACK OVERFLOW	
44	36	Pk	1 I05F	COMMUNICATION OPERATOR	P2
45	37	Pk	2 I06F	PROGRAM RELEASE OPERATOR	P2
46	38	Pk	4 I07F	CONTINUITY BIT	P2
47	39	Pk	8 I08F	PRESENCE BIT (I/O STATUS BIT)	P2
50	40	Pk		FLAG BIT	P2
51	41	Pk		INVALID INDEX	P2
52	42	Pk		EXPONENT UNDERFLOW	P2
53	43	Pk		EXPONENT OVERFLOW	P2
54	44	Pk		INTEGER OVERFLOW	P2
55	45	Pk		DIVIDE BY ZERO	P2
62	50	Pk	I03F	P1 STACK OVERFLOW	
64	52	Pk	1 I05F	COMMUNICATIONS OPERATOR	P1
65	53	Pk	2 I06F	PROGRAM RELEASE OPERATOR	P1
66	54	Pk	4 I07F	CONTINUITY BIT	P1
67	55	Pk	8 I08F	PRESENCE BIT (I/O STATUS BIT)	P1
70	56	Pk		FLAG BIT	P1
71	57	Pk		INVALID INDEX	P1
72	58	Pk		EXPONENT UNDERFLOW	P1
73	59	Pk		EXPONENT OVERFLOW	P1
74	60	Pk		INTEGER OVERFLOW	P1
75	61	Pk		DIVIDE BY ZERO	P1

REGISTER CONTENTS

REGISTER CONTENTS

NOTE: OTHER LOCATIONS USED:

I/O RESULT DESCRIPTORS 12 ⇒ 15
INITIATE - WORD 8
CONTROL STATE MARK STACK 7

Figure 7.5-1 is a Block Diagram which can be used for reference throughout this section. This figure shows the External Interrupt Register at the top of the Central Control box. These are CCnnF flip-flops which are listed in Table 7.5-1. The other two boxes are Processor A and Processor B.

The syllable dependent Interrupts in the Processors set PkI05F, PkI06F, PkI07F and PkI08F Flip-flops. These are set to binary numbers by the Processor and are added to the Base Interrupt Address location of the unit.

The Processor non-syllable dependent Interrupts are:

1. Memory Parity Error PkI01F
2. Invalid Address PkI02F
3. Stack Overflow PkI03F
4. Not assigned PkI04F

Pk = Processor A or B (whichever one is designated as P1).

These are high-priority Interrupts and each is a separate flip-flop in the Processor.

When Processor 1 processes Interrupts, it could have an error. Therefore, non-syllable Interrupts in P1 are of the highest priority.

The lines from the external flip-flops enter the priority logics and the encoder logics. These Interrupts will then set IAR5 Flip-flop, which is Address 16, plus the encoded numbers. PA1L and PB1L determine the base location for the Processors. Any Processor Interrupt will always set IAR6 Flip-flop, which is Address 32.

If Pk1L is true, the Processor is P1 and IAR5F is set. This advances the Base Address to 48. The set of IAR5F and IAR6F is under control of the priority logics, although for simplicity, this is not shown. The Interrupt Address Sync Set (IASS) level is the gating level to set the IAR numbers into the C Register of P1.

INTERRUPTS

There are forty (40) Interrupts that may occur if a maximum system configuration is used. Of these 40, twelve (12) are considered to be EXTERNAL Interrupts. For example, Non-Processor Interrupts.

Of the remaining twenty-eight (28) Interrupts, fourteen (14) are caused by PA and 14 are caused by PB.

There are twelve (12) flip-flops associated with the 12 External Interrupts. Each flip-flop defines a single Interrupt condition. There are two (2) low-priority unused flip-flops, CCI15F and CCI16F, which can be used for future expansion.

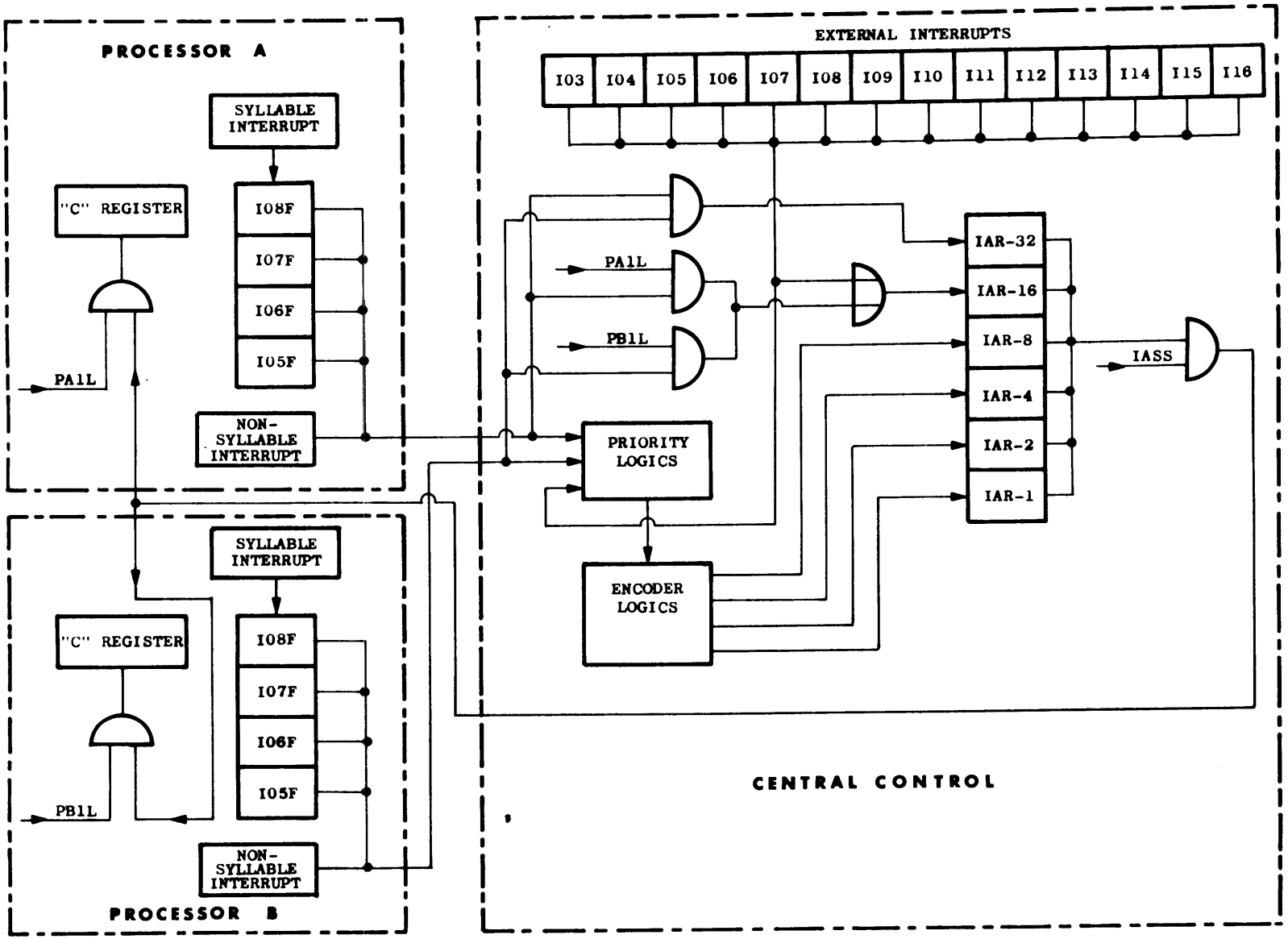


FIGURE 7.5-1 BLOCK DIAGRAM OF INTERRUPT SYSTEM

Eight (8) flip-flops are used by the Processor to define the 14 Processor Interrupts. 4 Of the 8 flip-flops define only four (4) conditions (PkI01F thru PkI04F). The remaining 4 flip-flops PkI07F thru PkI08F may define any one of ten (10) Interrupt conditions, depending upon the binary value of the bits. Only 1 of the 10 Interrupt conditions may be defined by these 4 bits at any time.

It is unlikely but possible for there to be twenty-two (22) individual Interrupt conditions occurring simultaneously. It is necessary for P1 to examine only one (1) Interrupt at a time. Furthermore, it is necessary that the Interrupt to be examined by P1 be of the highest priority.

Generally, there are three (3) levels of priority to be established as follows:

1. P1 Memory Parity Error Interrupt and P1 Invalid Address Interrupt are of the Highest priority and exceed the priority of the External Interrupts.

2. All P2 Interrupts are of lower priority than the External Interrupts, but of higher priority than most P1 Interrupts.

3. P1 Interrupts are generally of the lowest priority.

An Interrupt is sensed by the Interrupt priority logic. The priority logic gates the Interrupt Register to set an Address into the Register corresponding to the highest priority Interrupt occurring at a single Clock time. At the following Clock time, an Interrupt of high priority may cause the Interrupt Register to be set to a new Address. Even though the lower priority Address is destroyed by the new Address, the lower priority Interrupt still exists. An Interrupt Bit is reset at the time P1 takes the Address from the Interrupt Address Register.

The following example may be useful:

> Suppose I/O-1 and I/O-2 are controlling Tape Units and P1 is running a program. When I/O-2 finishes, an Interrupt Bit (CCI09F) will be set. The Clock time following the setting of CCI09F will set the Interrupt Address Register to 24. P1 senses the Address in the Register and begins to store its Registers (A, B, G, etc.). Before P1 has completed the storing of its Registers, I/O-1 finishes. The Address in the Interrupt Address Register will be changed to 23. Both CCI08F and CCI09F will be ON, but only the Address corresponding to the highest priority Interrupt will be in the Interrupt Address Register.

As soon as P1 completes the storage of its Registers, the Interrupt Register Sync Flip-flop is turned ON for a single microsecond. At the Clock time that the Sync Flip-flop is reset, the Address in the Interrupt Address Register is sent to the Processor. With the Interrupt Address Register equaling 23 and the Sync Flip-flop ON, CCI08F is reset. The Interrupt Address Register is cleared at this time.

With the next Clock Pulse, the Register will be set to 24. The 24 will remain in the Interrupt Address Register until P1 takes it, or, an Interrupt of higher priority occurs. At the time CCI08F is reset, the I1 BUSY switch (I1BS) will be restored to a NOT BUSY condition.

The highest priority External Interrupt which is the Time Interval Interrupt (CCI03F) will be turned ON every time the Real Time Clock overflows. The Real Time Clock is a standard 6 bit binary counter. It counts once per cycle of 60 cycle AC or roughly every 16 2/3 ms. Once every 1.07 seconds the counter will overflow to set CCI03F. This Interrupt is used to time programs etc.

The synchronizer TMOY provides a 1 μs level for each cycle of the 60 cycle AC. The reset terms for the Interrupts will be discussed later.

CCI04F will be turned ON if all the I/Os are BUSY and the controlling P1 is initiating an I/O. The CMIS and CMTF terms will be true during the Initiate I/O operator.

CCI05F will be turned ON if a keyboard entry from SPO is ready to be READ. The asynchronous level provided by the Supervisory Printer is defined by a switch and synchronizer.

CCI06F will be turned ON at the end of Printer #1 print cycle to signal that the Print Buffer is empty. Cross-coupled Holdover switches are used to define a single Clock time at the END of the print cycle and prevents Printer #1 Interrupts from occurring at other times when the buffer is also empty.

The initial states of the various levels are as follows:

1. 22PCYL is false (Print cycle NOT in progress).
2. $\overline{\text{22PCYS}}$ is true.
3. 22PCYL is true.
4. 22PCFS is false.
5. CCI06F is OFF.

When Power is applied to the system, the CLEAR term will be made true to reset the cross-coupled Holdover switch so that 22PCFS is false and $\overline{\text{22PCFS}}$ is true. The gate to turn CCI06F ON will have 22PCFS false and 22PCYS true. All that is required to set the Interrupt is the switching of the cross-coupled switches. When the Print Cycle Level 22PCYL becomes true at the end of a Print cycle, the switches change state and turn CCI06F ON. The cross-coupled switches will remain in the SWITCHED state until the CCI06F has been cleared by P1.

CCI07F operates exactly as CCI06F except that it is used with Printer #2. The prefix 26 (26PCYL) implies Printer Unit Driver 26, whereas, the preceding Printer #1 Interrupt terms were numbered 22 (22PCYL). The reset terms for CCI06F and CCI07F are inherently different.

The I/O Finished Interrupt flip-flops (CCI08F thru CCI11F) are essentially identical. Only one Finished Interrupt flip-flop (CCI08F) will be described.

CCI08F is turned ON at the time I/O-1 provides a Finished Level (I1FINL). The Finished Level may turn the flip-flop ON providing the I/O is BUSY (AD1F ON) and the unit is available (ON LINE). AD1F will be reset following the turn ON of CCI08F. The BUSY status of I/O-1 is still maintained by the gating to I1BS.

CCI12F will be turned ON if P1 executes an activate P2 operator AND P2 is BUSY. The terms CMIS and CMTF will be true during the Activate P2 operator.

CCI13F will be turned ON if an Inquiry Interrupt occurs. The Interrupt Level from the Inquiry Unit is synchronized by means of the synchronizer IS6Y. CCI15F and CCI16F are undefined at this time.

The reset logic for preceding flip-flops is uncomplicated if two (2) details are kept in mind.

1. To reset an Interrupt flip-flop, the controlling P1 must be TAKING the Interrupt Address from the Interrupt Address Register. This occurs only at the Clock time when the flip-flop IASF is ON. IASF is ON for only 1 μs.

2. The reset gating to an Interrupt flip-flop contains terms that correspond to the Address that that particular flip-flop can set into the Interrupt Address Register. For example; the reset terms for CCI03F will be true only at the time the Interrupt Address Register is equal to 18, and the Sync Flip-flop (IASF) is ON.

The switch $\overline{\text{CCINTS}}$ combines terms common to the reset logic used with External Interrupts. The Sync Flip-flop (IASF) will be ON, IA6F will be OFF, and IA5F will be ON.

The 32 bit of Register IA6F is always OFF during External Interrupts and the 16 bit (IA5F) is always ON. Hence, these are common terms for Addresses 18 thru 31.

The I00S switch combines other terms common to four (4) of the Interrupt flip-flop Addresses. The output of the switch says IASF • $\overline{\text{IA6F}}$ • IA5F • $\overline{\text{IA4F}}$ • $\overline{\text{IA3F}}$. This will be true for Interrupt Addresses 16, 17, 18 and 19. 16 and 17 are unused.

The I04S switch combines terms common to Interrupt Addresses 20, 21, 22 and 23. The output of the switch says IASF • $\overline{\text{IA6F}}$ • IA5F • $\overline{\text{IA4F}}$ • IA3F.

The I08S switch combines terms common to Interrupt Addresses 24, 25, 26 and 27. The output of the switch says IASF • $\overline{\text{IA6F}}$ • IA5F • IA4F • $\overline{\text{IA3F}}$.

The I12S switch combines terms common to Interrupt Addresses 28, 29, 30 and 31. The output of the switch says IASF • $\overline{\text{IA6F}}$ • IA5F • IA4F • IA3F.

The switches IN0S thru IN3S define the four (4) possible states of the 1 bit and 2 bit of the Register.

Examining the reset gate at CCI03F, the terms I00s and IN2S are required. These can easily be decoded to the following equation: IASF • $\overline{\text{IA6F}}$ • IA5F • $\overline{\text{IA4F}}$ • $\overline{\text{IA3F}}$ • IA2F • $\overline{\text{IA1F}}$ which is equal to the Interrupt Address 18. The reset logic for any one of the remaining Interrupts may be decoded similarly.

Processor Interrupts differ from the External Interrupts in that the flip-flop storage of the Processor Interrupt condition is located in the Processor rather than in Central Control.

The four (4) flip-flops PkI01F thru PkI04F, hold Interrupt conditions that are not directly associated with Program Control. These 4 conditions are the result of conditions occurring in the Memory in use by the Processor.

The remaining 4 flip-flops, PkI05F thru PkI08F may hold any ONE of ten (10) Interrupts occurring during the course of Program Execution.

The Interrupt Addresses that correspond to the various Interrupts may be separated into three (3) groups.

1. The External Interrupt group may contain Addresses between the numbers 16 and 31.
2. P2 Interrupts may contain Addresses between the numbers of 32 and 47.
3. P1 Interrupts may contain Addresses between the numbers of 48 and 63.

It will be observed that the PkI05F thru PkI08F Interrupt Bits are coded to represent numbers higher than the number 3. These four bits are a separate 4 Bit Register weighted in the Common Binary form.

The I05F bit will be the "1" bit; I06F, the "2" bit; I07F, the "4" bit; and I08F, the "8" bit.

The Communication Operator Interrupt will turn ON the I07F bit to represent a value of a 32 bit ON and the 16 bit OFF in the Interrupt Address. Combining the four bits, I05F thru I08F with the 32 bit ON and the 16 bit OFF, results in an Interrupt Address of 36. The Address gating of the Syllable Interrupts can be simply determined by adding the "weighted" value of the four bits to the two high order bits of the Processor Interrupt Address.

The P1 Syllable Interrupts are added to form the Interrupt Address in the same manner. The P1 Interrupt Address has both the 32 and the 16 bits ON.

INTERRUPT PRIORITY

PA and PB Interrupt priority is similar. Only the PA priority is considered here.

In order for PA to SET an Address into the Interrupt Register, it is necessary for the term PA to IAR to be true. This term may be true under any one of the following conditions:

1. PA has SET one of its Interrupt bits.
   a. PA is P2.
   b. P2 is idle (Registers have been stored).
   c. There is no External Interrupt (higher priority).
   d. Neither of the two high priority P1 Interrupts are true.

NOTE

The above conditions encompass all P2 Interrupt priority conditions if PA is P2.

2. PA has SET an Interrupt.

   a. PA is P1.

   b. There is no External Interrupt.

   c. There is no PB Interrupt.

NOTE

This gate covers all LOW priority Interrupts.

3. PA has SET an Interrupt.

   a. PA is P1.

   b. There are no External Interrupts.

   c. The P2 BUSY Flip-flop is ON.

NOTE

This gate covers the time during which a PB Interrupt may have occurred, but PB has not completed storage of its Registers.

4. PA has SET an Interrupt.

   a. PA is P1.

   b. The PA Interrupt is the high priority Memory Parity Error Interrupt.

5. PA has SET an Interrupt.

   a. PA is P1.

   b. The PA Interrupt is the high Priority Memory Invalid Address Interrupt.

External Interrupt priority is simply an arrangement of switches gating other switches to SET an Address into the Interrupt Address Register.

$\overline{S19S}$ switch is false if there is an I/O BUSY Interrupt and no Time Interval Interrupt. The Time Interval Interrupt is the highest priority Interrupt and inhibits a false level from any of the other $\overline{SnnS}$ switches.

The $\overline{S31S}$ switch may only be false if there are no higher priority External Interrupts. It is apparent that only one of the $\overline{SnnS}$ switches may be false even though many Interrupts may be present at the same time. Only the Interrupt of highest priority will cause its corresponding switch to be false.

$\overline{IEIS}$ (Inhibit External Interrupt Switch) is used to inhibit setting of the Interrupt Address Register with an External Interrupt Address if P1 has a Memory Parity Error or has requested an Invalid Address from Memory.

LOFF prevents the Interrupt at the completion of LOAD from disturbing P1.

IASS is used only to limit the number of true gates into the Interrupt Address Register Flip-flop at any one time. The eight (8) Set Interrupt Address Bit Switches S01S, $\overline{\text{S01S}}$ thru S04S, $\overline{\text{S04S}}$ are used to set the Interrupt Address Register according to the highest priority Interrupt.

INTERRUPT ADDRESS REGISTER

The Interrupt Address Register is a six bit Register used by Processor P1 to obtain a Memory Location. The Memory location held in the Interrupt Register will correspond to the highest priority Interrupt that was ON at the preceding Clock period. There is a 1 μs delay from the time the Interrupt is SET to the time the Interrupt Register may be set. The Address appearing in the Register is transferred to P1 when requested by P1. The Address is used by P1 to obtain a BRANCH into the Master Control Program for the purpose of determining the nature of the Interrupt condition.

P1 becomes aware of an Interrupt by sensing a NOT EQUAL TO ZERO condition in the Interrupt Register. If no Interrupts are present, the Register is cleared. When P1 finds the Interrupt Register NOT EQUAL TO ZERO, it stores its Registers.

In order for P1 to transfer the Address from the Interrupt Register, a 1 μs level (PkIASL) is necessary. This level permits the Sync Flip-flop, IASF, in Central Control to turn ON for 1 μs. The Interrupt Register is cleared at the Clock time IASF is ON. A new Interrupt Address may appear in the Register with the next Clock Pulse.

The 32 bit flip-flop IA6F will be turned ON any time PA or PB Interrupt occurs. However, it will be turned OFF if an External Interrupt occurs, providing a P1 Interrupt of higher priority is not present.

The 16 bit flip-flop IA5F will be turned ON for P1 Interrupts, and OFF for P2 Interrupts. IA5F will also be turned ON for all External Interrupts providing a P1 Interrupt of higher priority is not present.

The 8 bit flip-flop IA4F will be turned ON with the PkIO8F of either Processor Syllable Interrupt providing a higher priority Interrupt is not present.

If both Processors had identical Syllable Interrupts, the P2 Interrupt would take precedence (determined by PA and PB priority drivers).

External Interrupts requiring the 8 bit in the Address, turn IA4F ON by means of the S04S, providing a P1 Interrupt of higher priority is not present.

The Addresses of 0024 and above, require S04S. IA4F will be turned OFF if a Processor Syllable Interrupt has its 8 bit OFF; if the Processor Interrupt is NOT a Syllable Interrupt; or an External Interrupt requires the 8 bit to be OFF.

The 4 bit flip-flop, IA3F, is gated in the same way as IA4F, except that the 4 bit of Syllable Interrupts is used. External Interrupts requiring a 4 bit in Interrupt Address turn IA3F ON, and those requiring the 4 bit OFF turn it OFF.

The 2 bit flip-flop, IA3F, carries terms similar to those used with IA3F and IA4F, plus a few others to make sure the bit is set properly in cases of Non-Syllable Interrupts. These should be immediately apparent.

The 1 bit flip-flop IA1F, is similar to the 2 bit. The difference being that the 1 bit is required for Syllable Interrupt Addresses 33 and 35, or, 49 and 51.

The 2 bit is required for Syllable Interrupt Addresses 34 and 35, or, 50 and 51.

The IASS switch clears all bits of the Register when IASF is true.

7.6 MEMORY EXCHANGE

INTRODUCTION

The Memory Exchange Unit contains all information and control lines to each Memory Unit. Some of these lines originate within the Memory Exchange, while some of them are amplified and passed on from the Requesting Unit to Memory. In most cases, the signal from the Requesting Unit will not have the same mnemonic as the signal from the Central Control to Memory Unit.

Refer to Figure 7.6-1 for a Block Diagram of the Memory Exchange.

MEMORY INTERCOMMUNICATION LINES

Central Control to Memory

C(N)AOOS	Memory START level. 1 μs pulse, initiates to Memory cycle when true.
C(N)WOOD	Memory WRITE level. 1 μs pulse. When true, this signal ANDED with AOOS results in a WRITE Memory cycle. When false, this signal ANDED with AOOS results in a READ Memory cycle.
CLOCK PULSE CLOCK GROUND	This standard Clock signal is generated in Central Control and transmitted to Memory via a standard length twisted-pair cable to a Local Clock Driver in Memory.
C(N) A01S thru C(N) A12S	Memory ADDRESS information, 12 bits, 1 μs pulse. These lines when true set one-sided Address information from Central Control into the Memory Address Register MAR-1 thru MAR-12. The lines are ANDED with AOOS.
C(N)W01S thru C(N)W48S	Memory WRITE information, 48 bits, 1 μs pulse. These lines when true set one-sided Central Control WRITE information into the Memory Information Register MIR-1 thru MIR-48.

Memory to Central Control

C(N) R01S thru C(N)R48S	Memory READ information, 48 bits, 5 μs pulse during WRITE, 3 μs pulse during READ. These lines set single ended READ information into the I/O "W" Register.
M(N)MPEF	Memory Parity Error, 2 μs. This line, when true at MT4, indicates a READ Parity Error. M(N)MPEF (Memory Module N) is set at T3, and checked in Central Control at T4.

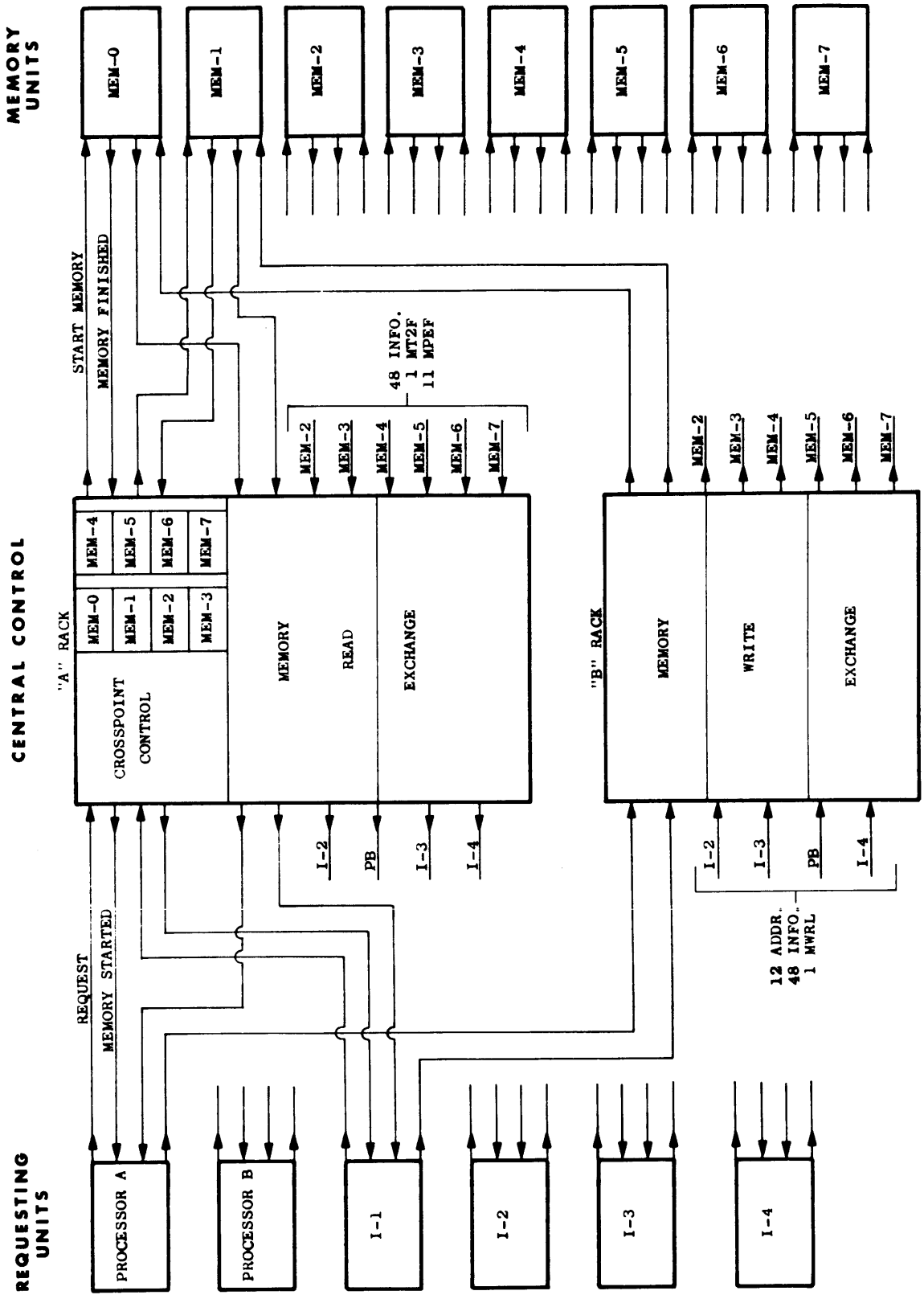


FIGURE 7.6-1 CENTRAL CONTROL MEMORY EXCHANGES

M(N)$\overline{\text{MT2F}}$ — Memory Timing Level 2, 1 μs pulse. This line provides the Central Control Unit with a Memory Timing indication. (N = 0 thru 7; M0 thru M7).

M(N)$\overline{\text{MT4F}}$ — Memory Timing Level 4, 1 μs pulse. This line provides the Central Control Unit with a Memory Timing indication. (N = 0 thru 7; M0 thru M7.)

M(N)MNAL — Memory Not Available Level. When true, this level indicates to Central Control that the Memory is not available (Local or POWER UP). (N = 0 thru 7; M0 thru M7.)

I/O Intercommunication Lines

The Intercommunication lines from I/O through Central Control to Memory are illustrated in Figure 7.6-2.

The signal lines between I/O and Central Control are as follows:

$\overline{\text{D01F}}$ thru $\overline{\text{D15F}}$ — "D" Register bits are used to locate the Address area in Memory.

$\overline{\text{D13F}}$ thru $\overline{\text{D15F}}$ / D13F thru D15F — "D" Register bits are used by Central Control to Address correct Memory Module Unit.

I(N)MANF — Memory Access needed. Originating level to Central Control which indicates I/O Unit Memory request. (N - 1 thru 4; I1 thru I4.)

C(K)MAED — Memory Address Error. A non-existent Memory Module is Addressed. (K = A or B; DPA or DPB.)

C(K)MPED — Memory Parity Error. A Parity Error existed during Memory Access cycle. (K = A or B; DPA or DPB.)

C(K)MTOD — Memory Time 0. Indicates start of Memory cycle and releases of Requesting Unit during Memory WRITE operations. (K = A or B; DPA or DPB.)

M(N)$\overline{\text{MT2F}}$ — Memory Time 2. A 1 μs pulse which indicates READ information is in MIR. (N = 0 thru 7; M0 thru M7.)

I(N)MWRD — Memory WRITE Driver. A level from I/O to Central Control where it becomes WOOD to Memory (N = 1 thru 4; I1 thru I4.)

C(N)R01S thru R48S — Information READ signals from Central Control to I/O. Initiated by I01F thru I48F. (N = 0 thru 7; C0 thru C7.)

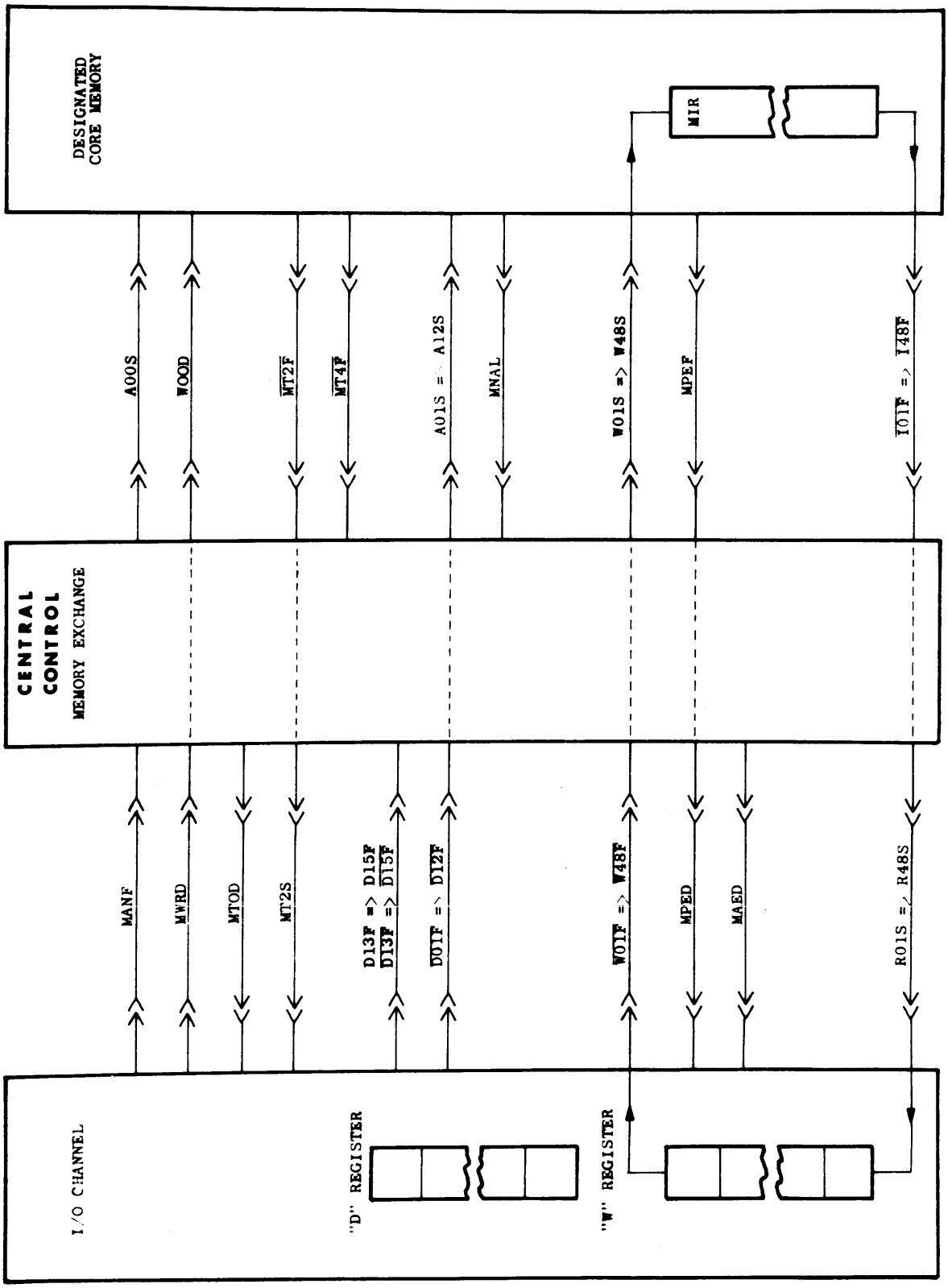


FIGURE 7.6-2 I/O INTERCOMMUNICATION LINES

C(N)W01S thru C(N)W48S	Information WRITE signals from Central Control to Memory. Initiated by W01F thru W48F from I/O to Central Control. (N = 0 thru 7; C0 thru C7.

In the I/O Control Unit, the "W" Register is the buffer Register for the incoming or outgoing information words between the Memory Unit and a peripheral unit.

Many peripheral units require the information in serial sequence. For example, character by character. Therefore, it requires time to LOAD the "W" Register from a peripheral unit.

Once LOADED, the information is shifted to Memory during the character to character time of the peripheral unit. A Memory ACCESS requires approximately 6 to 18 μs, depending on the priority of the request. This time is adequate for the information from the "W" Register to be successfully shifted to Memory before additional information pulses from the peripheral unit are received.

The "D" Register in the I/O Control Unit contains the Descriptor Word for any operation. In this Register, the control portion of the I/O Descriptor remains during the peripheral cycle.

The Memory Module designation is found in D13, 14 and 15 position in this Register. This is gated to Central Control where it is used to select the crosspoint flip-flop. The "D" Register positions, D1 thru D12, store the Base Address location within a Memory Module area. As each word is written into Memory, D1 thru D12 is counted by one to Address the next word location in Memory.

Processor Intercommunication Lines

The Communication Lines and Processor Signal Channels are illustrated in Figure 7.6-3.

Since the source of information in the Processor is quite involved, an understanding of the Processor flow is necessary to ascertain the communication necessary between the Processor and Memory through Central Control.

A Memory request is started in the Processor by the setting of the "E" Register to a significant digit. This Register has three functions:

1. To initiate a Memory Cycle.
2. To select the proper Processor Information Register.
3. To select the proper Processor Address Register.

The "E" Register is a Mod 16 Register which is set directly by the Program Operators being processed. The Address and Information Register designation is determined by the Program Syllable itself which will set the "E" Register as one of its functions.

Basically, the "E" Register is divided into the following four functions:

1. The "1" bit controls Processor selection of information Registers, "A" or "B". If the "1" bit is OFF, "A" Register is accessed; if ON, "B" Register is accessed.

2. The "2" bit, if ON, and the "4" bit if OFF, use the "S" Register for Addressing a Memory cell.

3. The "4" bit, if ON, uses the "M" Register for Addressing a Memory cell.

4. Any number less than "8" in the "E" Register calls for a READ Information from Memory to Processor. Any number greater than "8" calls for a WRITE Operation from Processor to Memory.

5. A setting of 16 indicates a Memory Fetch cycle (which can be executed separately) to LOAD the "P" Register with information Addressed by the "C" Register.

By following the simplified gating in Figure 7.6-3, a better understanding of the purpose of the "E" Register can be ascertained.

Once the "E" Register gates the proper Registers, the information and control lines leave the Processor where they signal Central Control to initiate a Memory cycle.

The signal lines between the Processor and Central Control are as follows:

D01S thru D48S — READ information lines between Central Control and Processor.

$\overline{\text{M01S}}$ thru $\overline{\text{M12S}}$ — ADDRESS lines between Processor and Central Control. These lines become A01S thru A12S between Central Control and Memory.

M13D thru M15D — Module selection lines between Processor and Central Control.

C(N)MT2S — Memory time 2. From Memory through Central Control to indicate Memory READ cycle is complete. In Processor, this becomes MRAF or MROF.

C(N)MTOD — Memory time 0. From Central Control to indicate Memory ACCESS started, and Memory WRITE Information obtained. In Processor, this level becomes MWOF.

CROSSPOINT LOGIC

For a detailed illustration of Crosspoint Logic refer to Figure 7.6-4.

This is the Memory Request Control section of Central Control. There are a maximum of eight (8) Memory Modules within a system and a maximum of six (6) Requesting Units in a system. The Memory Request priority system has previously been discussed (APAS, APBS and ARnS).

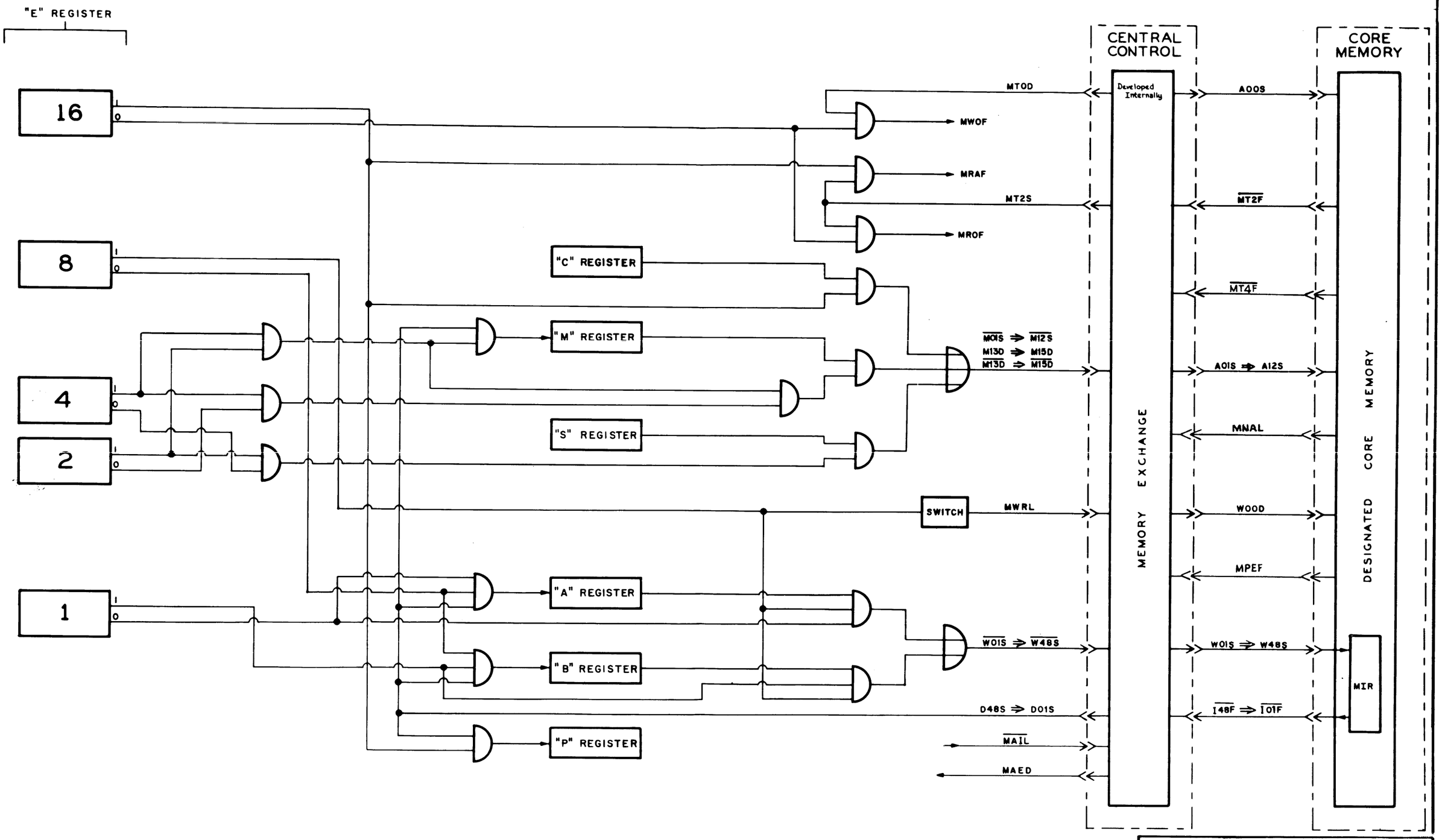


FIGURE 7.6-3
PROCESSOR INTERCOMMUNICATION LINES

The Crosspoint Logic is a 6 x 8 switching Matrix. With the 8 Memory Modules numbered across the top from 0 to 7, and the 6 Requesting Units listed vertically along the side of the Matrix, there are 48 possible combinations of Memory Module and Requesting Unit connections. PA may request access to any one of the 8 Memory Modules, PB may also request access to any one of the 8 Memories, and so on.

It is important that only one Requesting Unit at a time gain access to a Memory. There are 48 interlock flip-flops corresponding to the 48 different connections that may be made. The flip-flop MOPAXF will be turned ON if PA requests, and is granted access to Memory Module zero. The flip-flop M3I4XF will be turned ON if I/O-4 requests, and is granted access to Memory Module 3, and so on.

When one of the Crosspoint flip-flops is turned ON, a number of significant things happen. Sixty (60) Address and Information lines from the Requesting Unit are gated into the Memory Module designated by the Crosspoint flip-flop. The setting of all other Crosspoint flip-flops associated with the particular Memory are inhibited. Forty-eight (48) Information lines from the Memory Module are gated to the Requesting Unit. A Memory cycle begins within the Memory. The Memory cycle takes approximately 6 μs. However, the Requesting Unit may be released from Memory Control before 6 μs has elapsed.

The idle state of a Memory Module is considered to be Memory Time 0. The Memory Clock counts from 0 to 1 when it is started. The counts continue 2, 3, 4, 5, and then 0, which is the idle state again. Memory Times 0, 2, 4 and 5 are made available for various control purposes. Memory Times 0 and 2 are available to the Requesting Units.

In order for PA to be connected to MEM-0 (Memory Module Zero), the Crosspoint flip-flop MOPAXF must be turned ON. PA Addresses a Memory Module by means of the three (3) high order bits 13, 14, and 15 of the Address Register in use. MOPAXF then has as part of its gating the 3 bits PA13, PA14 and PA15 equal to zero. APAS will be true providing PB is P2 and has not been inhibited by requesting the same Memory.

$\overline{\text{MOIORS}}$ will be true if there is no I/O request for MEM-0. Any Memory request for MEM-0 by an I/O will inhibit either of the Processor requests for MEM-0. MOXFOS will be true any time the Memory is idle. The Memory is BUSY any time that one of the 6 Crosspoint flip-flops are ON. $\overline{\text{PAMAIL}}$ (Memory Access Inhibit Level) will be true unless one of the first 512 Memory locations (0000 thru 0511) in MEM-0 is to be Addressed while the Processor is in the NORMAL state. The first 512 Memory locations are reserved for essential parts of the Master Control Program.

The following conditions must exist for MOPAXF to be turned ON:

1. PA requests MO.
2. PB as P2 does not inhibit the request.
3. There is no I/O request present.

4. The Memory is idle and available.

5. PA is in CONTROL state or not prepared to Address 0000 thru 0511 if in NORMAL state.

The gating for MOPBXF and all Memory and Processor combinations is similar to the gating of MOPAXF.

The Crosspoint gating for the I/O Memory combinations is the same as that described for the PA MEM-0 connection. The following conditions must be true for I/O-1 to gain access to MEM-0:

1. The high order Memory Address bits 13, 14 and 15 of I/O-1 must be equal to zero.

2. I/O-1 must indicate its request by turning ON its Request flip-flop I1MANF (Memory Access Needed Flip-flop).

3. The "Admit" term AR1S must be true (no priority conflict etc.).

4. The Memory must be idle and available.

Inspection of any one of the other I/O Memory Crosspoint flip-flop gates will point out the similarity of the terms. All of the Crosspoint flip-flops are reset at Memory Time 4.

It will be observed that there is no Memory Access Inhibit term used in the I/O Memory Crosspoint gates. The I/O must use locations within the first 512 locations of the MEM-0 to WRITE Descriptors as well as Writing into these locations at other times. However, the I/O may not Address these locations in the case of Memory "fold-over". For example, Addressing consecutive locations above 32,767 during a Memory operation. This is a situation handled by the I/O.

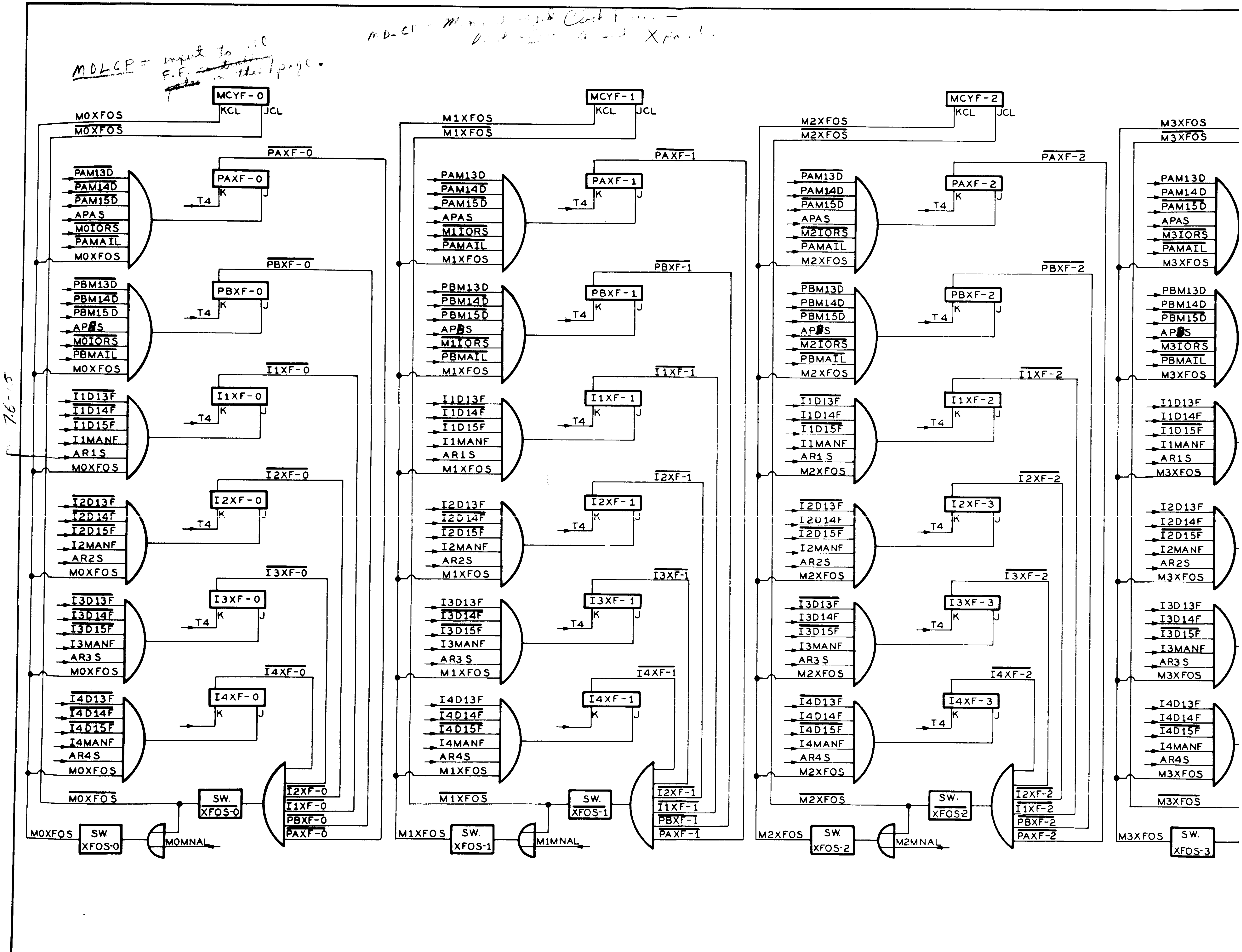
$\overline{\text{MOXFOS}}$ is true throughout the complete Memory cycle from 0 Time through 4 Time. Any MEM-0 Crosspoint flip-flop can hold the switch true. MOXFOS will be false throughout the Memory cycle, then true at all other times unless the Memory is not available.

MOMT4S will be true at Memory Time 4 unless the Memory is not available. MOMT4S is used to clear the Crosspoint flip-flops.

$\overline{\text{MOIORS}}$ is used to inhibit the setting of Processor Crosspoint flip-flops if any I/O request for MEM-0 exists at the time of the Processor request.

COAOOS provides a starting level to Memory. This switch will be true at Memory Time 0 only. This time is during the 1 μs between the setting of a Crosspoint flip-flop and the setting of MOMCYF (MEM-0 Memory Cycle Flip-flop).

The Driver COWOOD provides Memory with a WRITE or NOT WRITE level. The WRITE or NOT WRITE level from the Requesting Unit furnishes the input to the Driver.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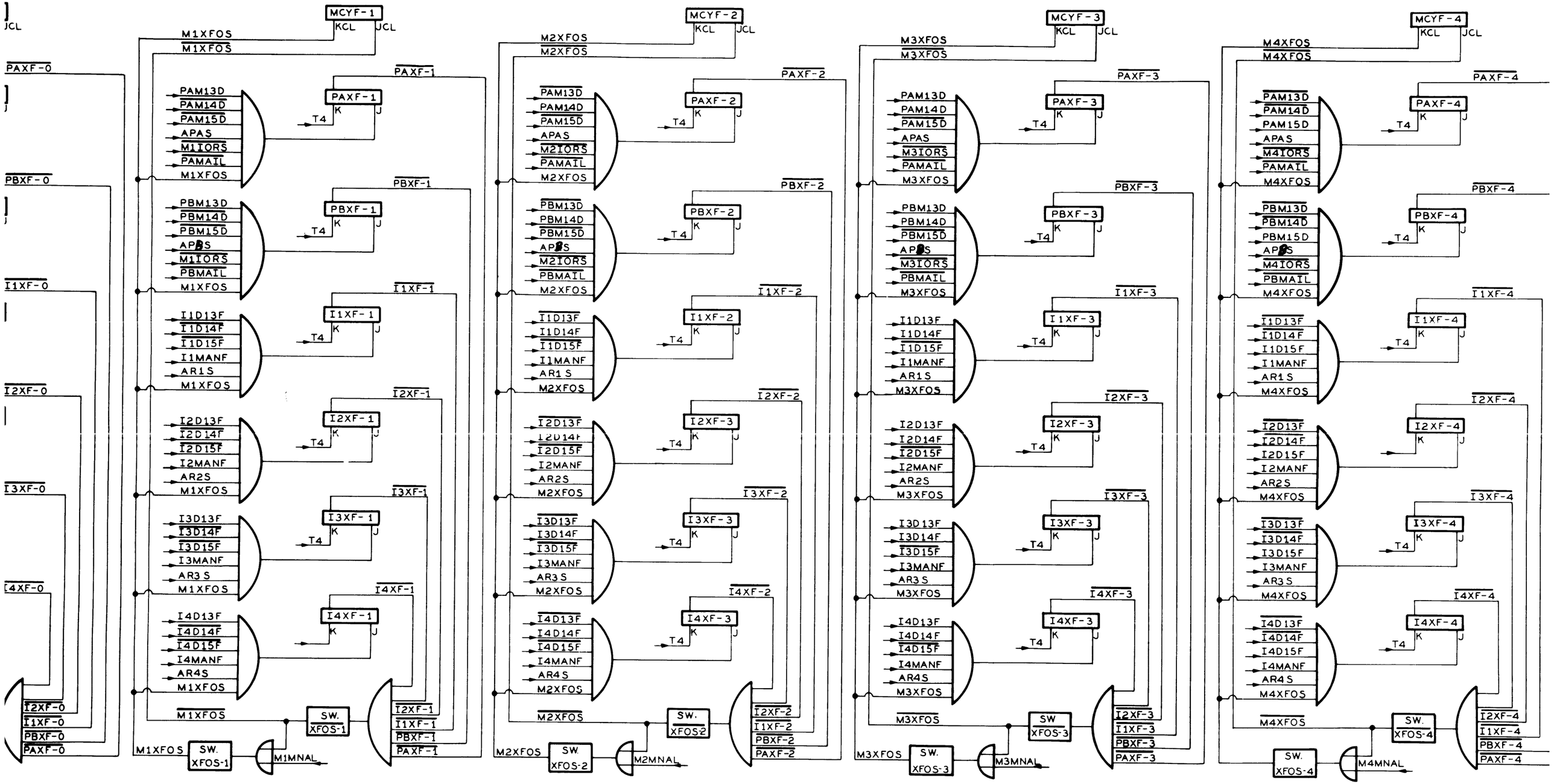
JCL
M0XFOS
M0XFOS
PAXF-0
PAM13D
PAM14D
PAM15D
APAS
M0IORS
PAMAIL
T4
PBXF-0
PBM13D
PBM14D
PBM15D
PBMAIL
I1XF-0
I1D13F
I1D14F
I1D15F
I1MANF
AR1S
I2XF-0
I2D13F
I2D14F
I2D15F
I2MANF
AR2S
I3XF-0
I3D13F
I3D14F
I3D15F
I3MANF
AR3 S
I4XF-0
I4D13F
I4D14F
I4D15F
I4MANF
AR4S
SW. XFOS-0
M0MNAL
MCYF-1
M1XFOS
PAXF-1
PBXF-1
I1XF-1
I2XF-1
I3XF-1
I4XF-1
M1IORS
SW. XFOS-1
M1MNAL
MCYF-2
M2XFOS
PAXF-2
PBXF-2
I1XF-2
I2XF-2
I2XF-3
I3XF-2
I3XF-3
I4XF-2
I4XF-3
M2IORS
SW. XFOS2
SW. XFOS-2
M2MNAL
M3XFOS
M3IORS
SW. XFOS-3
MDLCP = input to all F.F. in this page.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MCYF-2
MCYF-3
MCYF-4
KCL
JCL
M1XFOS
M2XFOS
M3XFOS
M4XFOS
PAXF-0
PAXF-1
PAXF-2
PAXF-3
PAXF-4
PBXF-0
PBXF-1
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PBXF-3
PBXF-4
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I3XF-3
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I4XF-0
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I4XF-2
I4XF-3
I4XF-4
PAM13D
PAM14D
PAM15D
APAS
M1IORS
M2IORS
M3IORS
M4IORS
PAMAIL
PBM13D
PBM14D
PBM15D
APBS
PBMAIL
I1D13F
I1D14F
I1D15F
I1MANF
AR1S
I2D13F
I2D14F
I2D15F
I2MANF
AR2S
I3D13F
I3D14F
I3D15F
I3MANF
AR3S
I4D13F
I4D14F
I4D15F
I4MANF
AR4S
T4
K
J
SW.
XFOS-1
XFOS-2
XFOS-3
XFOS-4
M1MNAL
M2MNAL
M3MNAL
M4MNAL

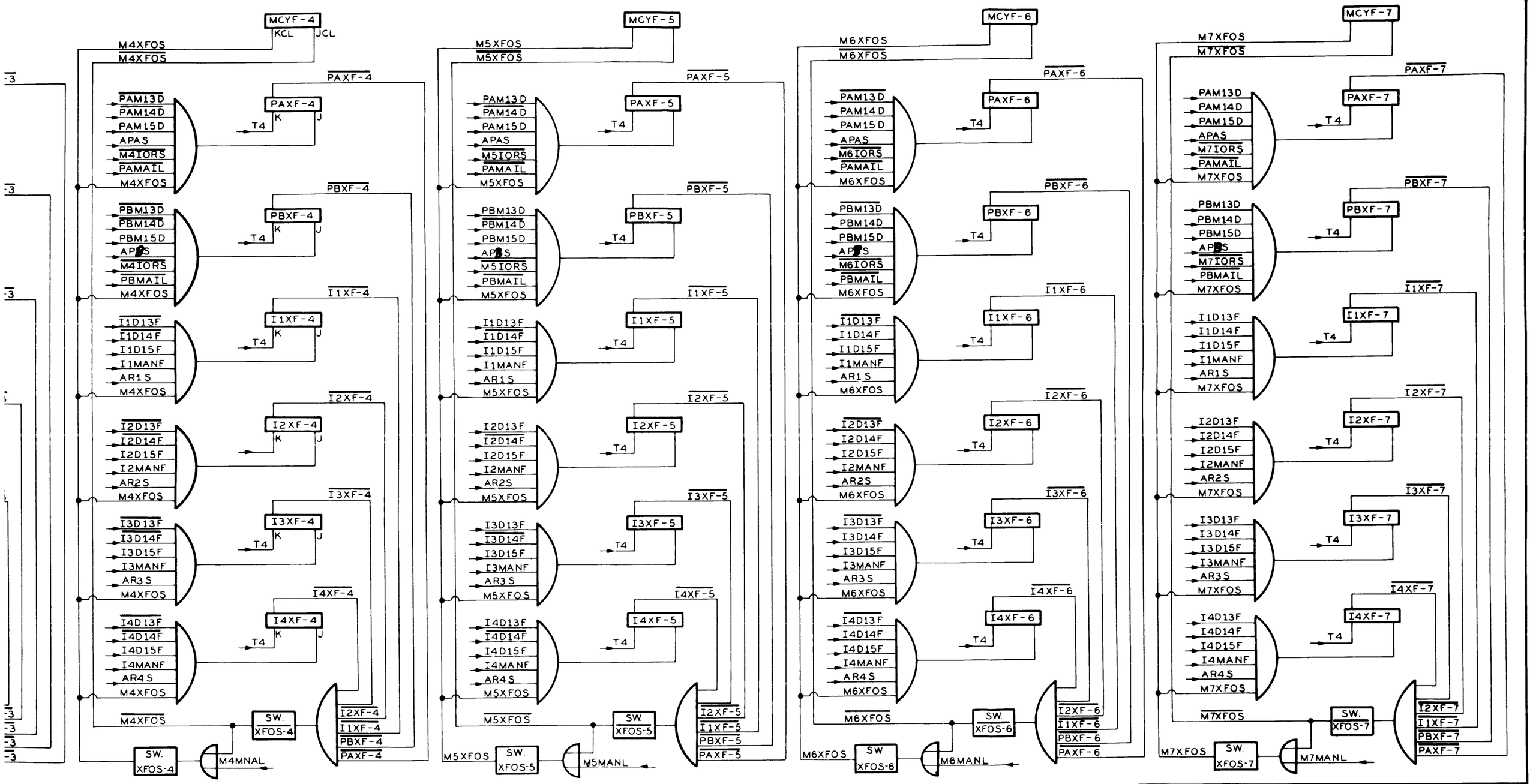


FIGURE 7.6-4
CROSSPOINT LOGIC

COA01S thru COA12S are Memory Address switches driven by the Address lines from the Requesting Unit. The appropriate Crosspoint flip-flop gates these lines by means of a switch. If PA is granted Memory Access, the lower order Address bits 01 thru 12 will be gated to the Memory through these switches.

COW01S thru COW48S are Memory WRITE Information switches driven by the 48 Information lines from the Requesting Unit. The appropriate Crosspoint flip-flop gates these lines by means of two (2) Drivers.

The Crosspoint Logic for MEM-1 thru MEM-7 is similar to that described for MEM-0.

The Memory READ Exchange requires the same Crosspoint flip-flop gating as does the Memory WRITE Exchange. The information from Memory is gated through the C01S or R01S switches, depending upon the type of Requesting Unit. CAD01S thru CAD48S are the Memory READ Information switches for information transfer to PA. Memory Information from any of the eight Memory Modules is gated through these switches when the appropriate Crosspoint flip-flop is ON.

Memory Times 0 and 2 are supplied to the Requesting Unit by the Driver MT0D and the switch MT2S. These levels are required for WRITE and READ timing. Parity Error Information is gated through Central Control to the Requesting Unit during Memory READ only. This information may be sampled at Memory Time 4.

The MAED Drivers are used to detect non-available Memory Modules. PA, for example, may determine the available Memory size by Addressing each of the Memory Modules. Modules not available will permit CAMAED to be true when Addressed. If Memory 3 is not available, M3MNAL will be connected to an open line. By Addressing MEM-3, PA will cause CAMAED to be true. If MEM-3 is available, M3MNAL will be grounded (false) within the Memory Module.

MEMORY REQUEST CONFLICT LEVELS

The Memory Module Address Conflicts are determined by comparison.

There are six (6) possible combinations of Memory Module Address Conflicts as illustrated in the Primary Logic of Figure 7.6-5. These are between I/O-1 and I/O-2; I/O-1 and I/O-3; I/O-1 and I/O-4; I/O-2 and I/O-3; I/O-2 and I/O-4; and I/O-3 and I/O-4.

The Conflicts are detected by C12S, C13S, C14S, C23S, C24S and C34S respectively.

The gating to C12S compares three (3) high order Memory Module Address bits D13, D14 and D15 of I/O-1 and I/O-2. If any bit in the I/O-1 Address is different than the corresponding bit of the I/O-2 Address, C12S will be false, indicating NO Conflict. If the Addresses are identical, there will be no true gate at the input to C12S. Hence, C12S will be true. .

The five (5) other CnnS switches operate in the same manner.

ADMIT I/O REQUEST LOGIC

Refer to Figure 7.6-5 for Memory Request Conflict Levels.

The ARnS switches provide ADMIT levels (normally true) for the Crosspoint flip-flop gates. AR1S (Admit I/O-1 Request Switch) will permit Memory Access by I/O-1 if AR1S is true, and an I/O-1 request exists. AR1S will be false if any one of its 3 input OR gates is true. There are three (3) ways in which a Memory request by I/O-1 may be inhibited. Note that only OTHER I/O Control Units may inhibit I/O-1. Processors may not inhibit a Memory request of an I/O Unit. It should be apparent that the Memory requests considered here are simultaneous requests for the same Memory Module.

Any one of the following AR1S input conditions can inhibit an I/O-1 Memory Module request:

1. I/O-2 is requesting.
    a. There is a Memory Module Address Conflict.
    b. I/O-2 has priority over I/O-1.
2. I/O-3 is requesting.
    a. There is a Memory Module Address Conflict.
    b. I/O-3 has priority over I/O-1.
3. I/O-4 is requesting.
    a. There is a Memory Module Conflict.
    b. I/O-4 has priority over I/O-1.

The gating to AR2S, AR3S and AR4S is similar.

ADMIT PROCESSOR REQUEST LOGIC (APAS & APBS)

The terms APAS and APBS are used in the Memory Crosspoint Control section. For example, in the gating to the Crosspoint flip-flops.

APAS SAYS: admit Processor A Memory request unless Processor B is requesting the same Memory Module and Processor A is Processor 1.

APBS is identical to APAS except that Processor B as Processor 1 is considered. The gating to APAS is a complete comparison of PA and PB Memory Module Addresses and the term PA1L (PA is P1).

If PA and PB Memory Module Addresses are identical and PA is P1, APAS will be false. APAS will then inhibit the setting of the Crosspoint flip-flop that the request would normally set.

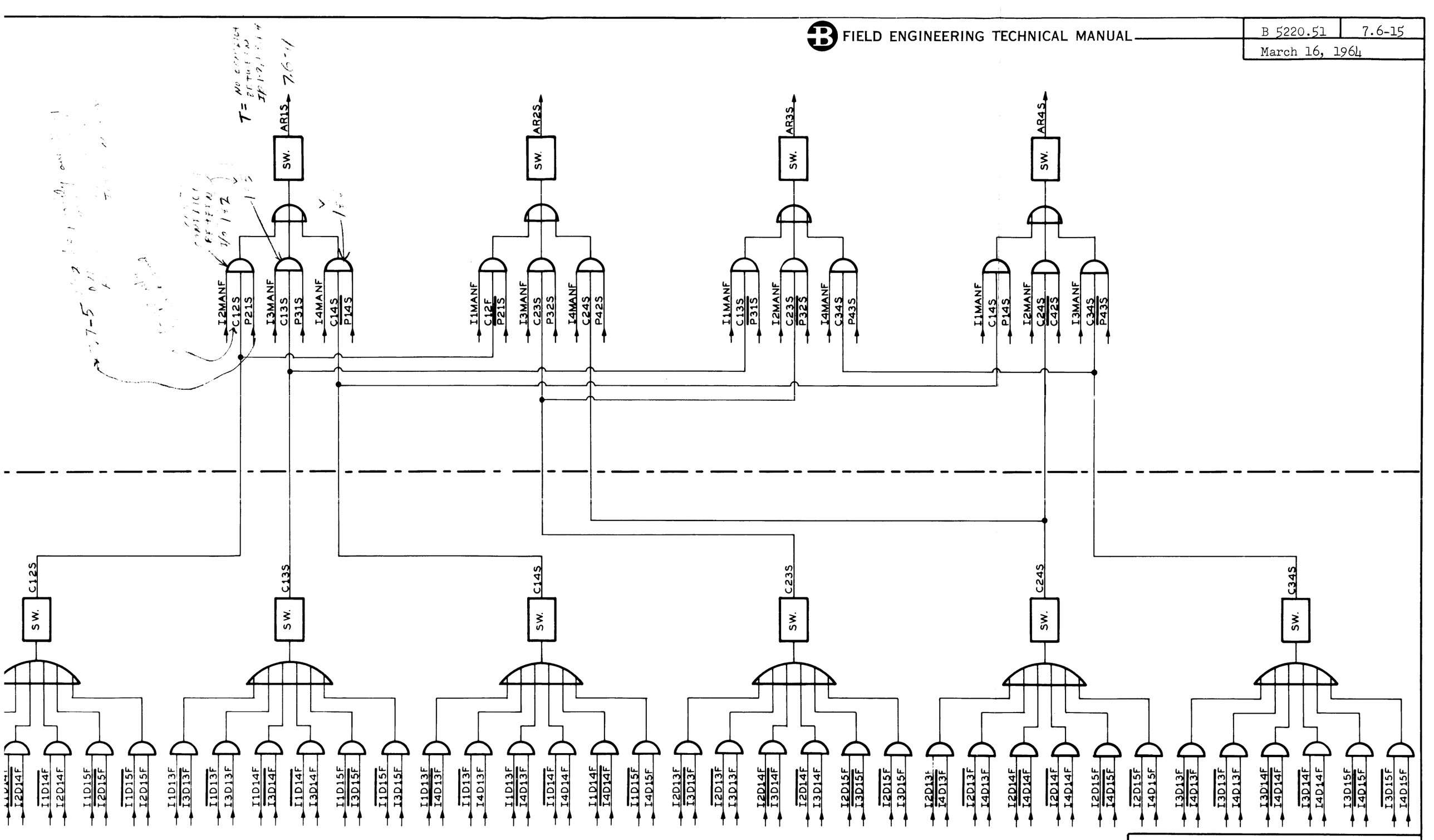


FIGURE 7.6-5
MEMORY REQUEST CONFLICT LEVELS

The reason the APAS and APBS terms are required is as follows: It is necessary that Processor 2 has Memory Module priority over Processor 1 under certain circumstances. This is immediately following the Initiate P2 operation. In order for P2 to begin any processing, it must first be started. It is started by the controlling Processor (P1).

In order for P1 to start P2, P1 stores an Address in cell 0008 of MEM-0 and then executes an initiate operator. The information in cell 0008 is the Address that P2 will use to locate the top of the stack to begin its program. The Initiate operator from P1 causes P2 to request MEM-0.

If P2 is temporarily inhibited from gaining access to MEM-0 by I/O requests in progress, P1 may execute an Initiate I/O operator.

Now, if P2 does not have Memory priority over P1, P1 will store another Address in cell 0008. If this were to happen, the word in cell 0008 which was intended for P2 would be destroyed by the storage of a new word intended for an I/O. Hence, by the time P2 finally was allowed access to cell 0008, the Address received by P2 would be incorrect.

MEMORY WRITE EXCHANGE

The Memory WRITE Exchange contains the necessary switches, drivers and gating for routing information from Requesting Units to the Memory Modules for the purpose of WRITING information in a particular Memory Module. Refer to Figure 7.6-6.

The primary control for the correct routing is the Crosspoint flip-flops. Each Crosspoint flip-flop will gate a double driver in the WRITE Exchange which will gate 48 Information lines from its associated Requesting Unit to 48 Information switches. Forty-eight Information switches are associated with each Memory Module and, as before, these switches drive 48 lines of information to the desired Memory Module. These switches are C0W01S thru C0W48S for MEM-0, C1W01S thru C1W48S for MEM-1, and so on. Each information switch has a six-legged OR gate input which will be corresponding bit information from the 6 Requesting Units.

MEMORY READ EXCHANGE

Figure 7.6-7 is a logical illustration of the READ EXCHANGE.

The Memory READ Exchange is a means of sending information from any Memory Module to any Requesting Unit. The Crosspoint flip-flops are the primary control for gating the information from the Memory Module to the Requesting Unit. Each Crosspoint flip-flop will gate a double driver in the READ Exchange which in turn will gate 48 Information switches. The Information switches to PA are labeled CnD01S thru CnD48S. The switches to the I/O Control Units are labeled CnR01S thru CnR48S. Each READ Information switch has an eight-legged OR gate input which contains the corresponding bit information from 8 Memory Modules.

ADDRESS SWITCHING

Figure 7.6-8 illustrates the Address switching section which provides for routing of the actual cell location desired to a particular Memory Module. The low order 12 bits (01 thru 12) of the Addressing Register in the Requesting Unit are gated to the desired Memory Module. The primary control is the Crosspoint flip-flop which drives a switch whose output gates 12 Address lines to 12 Address Switches CnA01S thru CnA12S. The Address switches are driven by a six-legged OR gate. Each leg of this gate contains a corresponding Address bit from 6 Requesting Units.

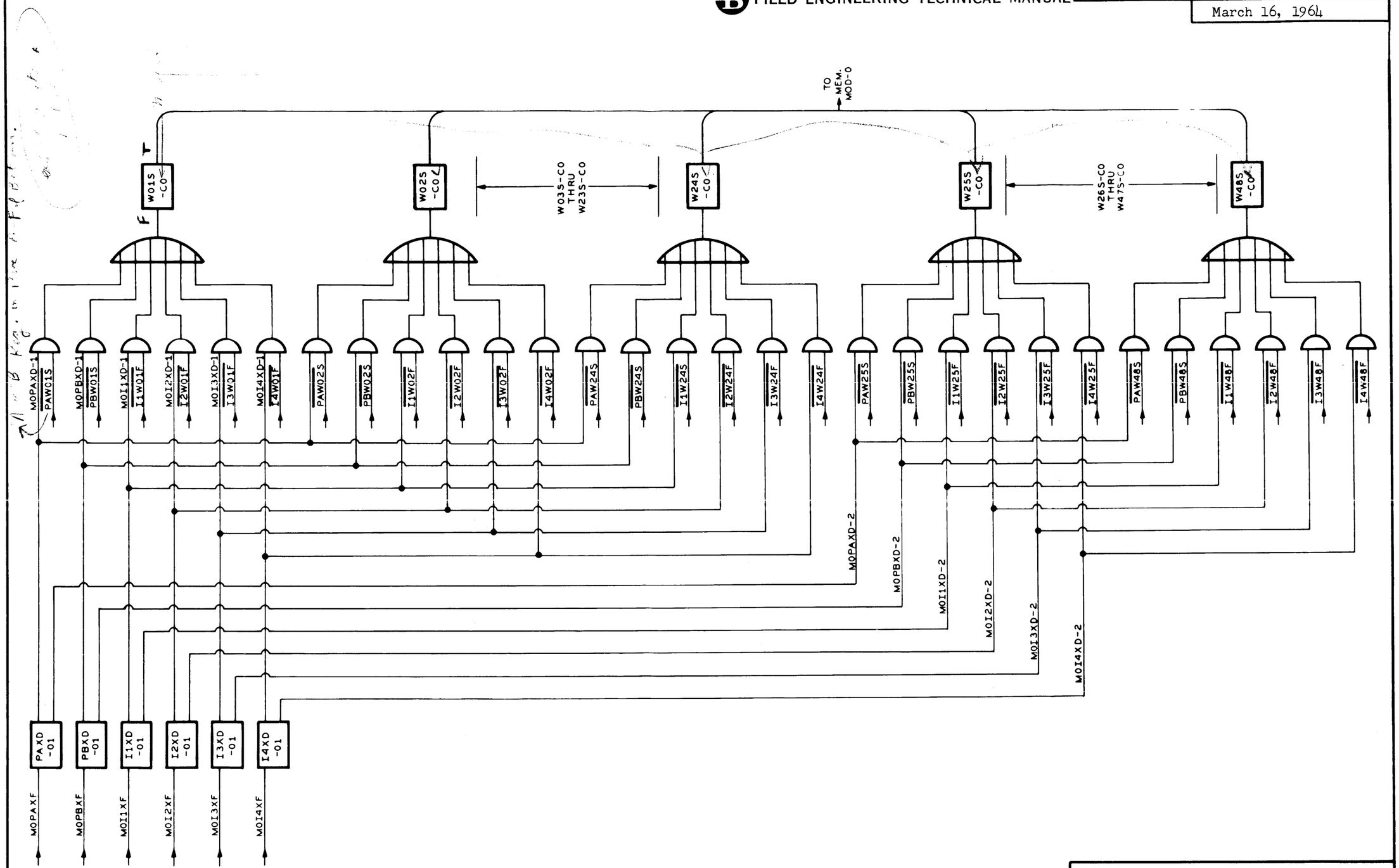


FIGURE 7.6-6
MEMORY WRITE EXCHANGE

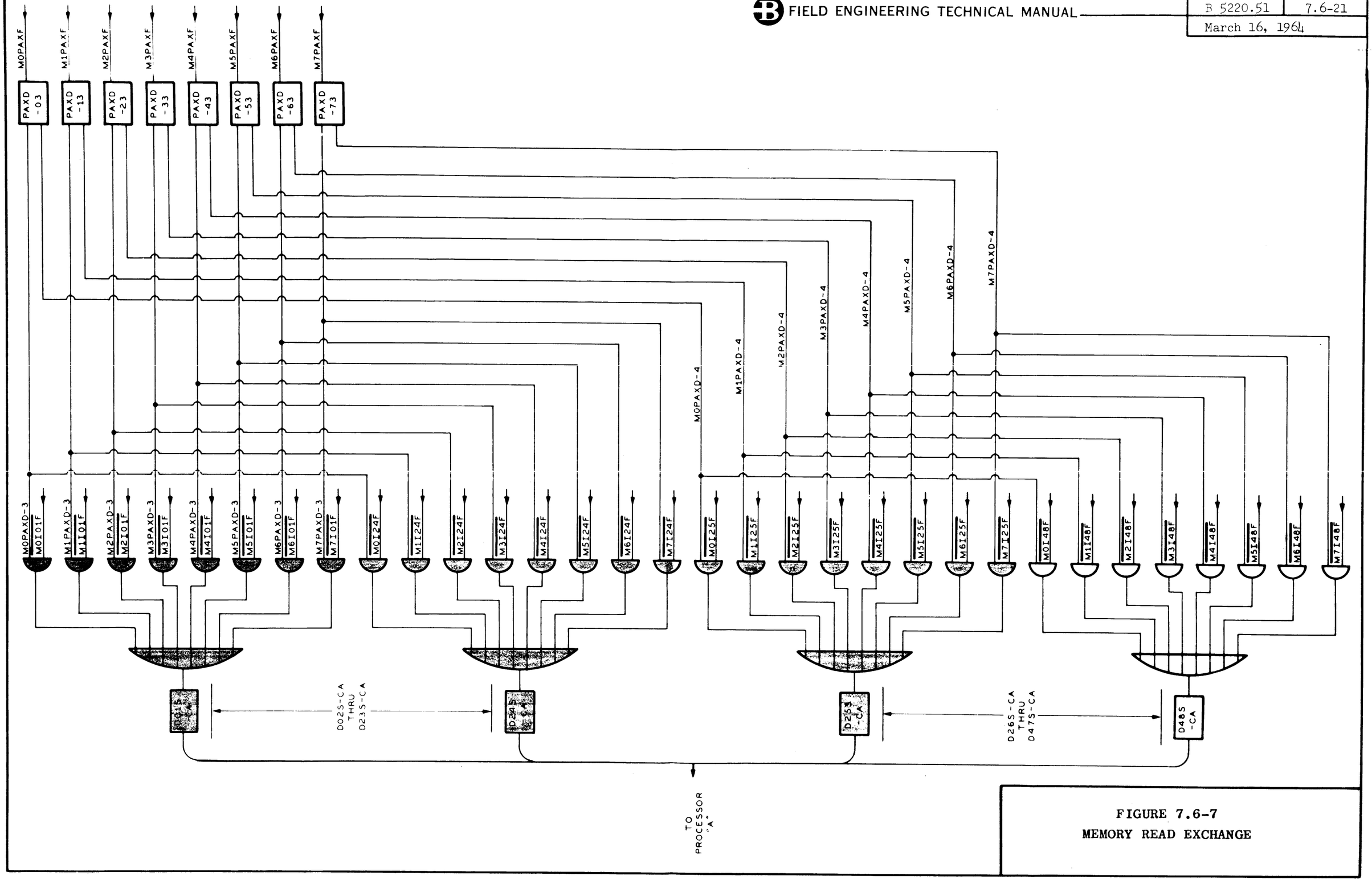


FIGURE 7.6-7
MEMORY READ EXCHANGE

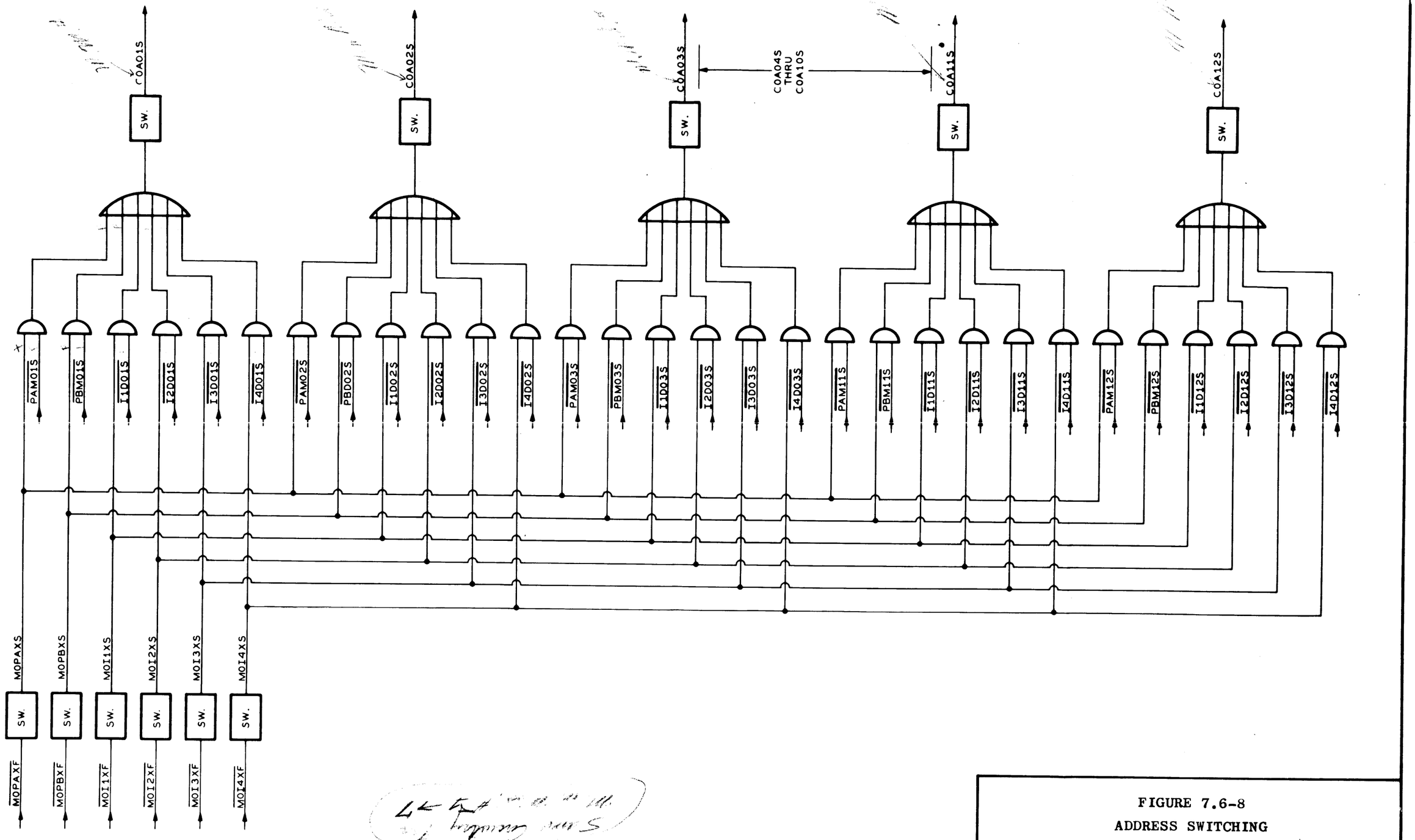


FIGURE 7.6-8
ADDRESS SWITCHING

7.7 INPUT/OUTPUT EXCHANGE

INTRODUCTION

The Input/Output (I/O) Exchange section of Central Control permits communication between any one of the four (4) I/O Units and any one of the thirty (30) peripheral units. This section is comprised of a repetitious diode matrix. The Output Drivers are driven directly by the I/O Registers Decoding Matrix.

Unit BUSY and Conflict Detection is established before the I/O Control Unit is permitted to designate access to the Peripheral Units.

A simplified layout of the I/O Exchange is illustrated in Figure 7.7-1.

The I/O Exchange Unit provides two distinct channels for each unit which are referred to as follows:

1. Input Channels - For information from Peripheral Unit to Memory.

2. Output Channels - For information from Memory to a Peripheral Unit.

NOTE

In this section, the word TAPE will refer to Magnetic Tape Units. Paper Tape Units will carry the words PAPER TAPE.

I/O PRIORITY DETERMINATION

There are three (3) levels of I/O priority considered in this section. The levels of priority are dictated by the information transfer rates of the Peripheral Units under control of the individual I/O Control Units. Figure 7.7-2 along with the following text will explain this determination.

Listed below are the three (3) priority levels.

1. I/O Control Units designating Tape Transport Units.

2. I/O Control Units designating Drum Units.

3. I/O Control Units designating any other Peripheral Units.

In cases of simultaneous Memory requests by the I/O Control Unit(s) designating similar types of Peripheral Units, the lower number designation of the I/O will be granted access. For example:

If I/O-1 and I/O-3 make simultaneous requests for MEM-1, and both I/O Control Units are controlling Tapes, I/O-1 will be admitted and I/O-3 will be inhibited. The I/O Peripheral Unit designation bits D41 thru D45 and D16 are used in the determination of the priority levels.

There are twelve (12) priority levels developed by comparison of the 3 BASIC priority levels. Six (6) of the 12 are merely inversions. For example:

> The $\overline{\text{P21S}}$ switch indicates the priority of I/O-2 is not greater than I/O-1. P21S indicates the priority of I/O-2 is greater than I/O-1. However, the actual priority is determined by the gates at the input of $\overline{\text{P21S}}$ only.

There are eight (8) Tape and Drum levels developed for use in the priority determination. These are $\overline{\text{I1TS}}$, $\overline{\text{I1DS}}$, $\overline{\text{I2TS}}$, $\overline{\text{I2DS}}$, $\overline{\text{I3TS}}$, $\overline{\text{I3DS}}$, $\overline{\text{I4TS}}$ and $\overline{\text{I4DS}}$.

To analyze the priority determination between I/O-1 and I/O-2, it may be more readily discerned by considering the priority of I/O-1 over I/O-2.

P21S (priority of switch 2 is greater than switch 1) will be true if the gate to $\overline{\text{P21S}}$ is true. Therefore, the priority of I/O-2 will be greater than the priority I/O-1 if I/O-2 is designated and one of the following conditions exist:

1. I/O-2 is controlling Tape and I/O-1 is NOT controlling Tape.

   a. $\overline{\text{I1TS}}$ is the term used for I/O-1 is NOT controlling Tape.

2. I/O-2 is controlling Drum 1 and I/O-1 is NOT controlling a Tape or a Drum.

   a. I1DS is the term used for I/O-1 is NOT controlling a Tape or a Drum.

3. I/O-2 is controlling Drum 2 and I/O-1 is NOT controlling a Tape or a Drum.

From the preceding three conditions, several details should be observed. All of the basic three levels of priority mentioned initially should be satisfied.

1. If both I/O Control Units are controlling Tape, I/O-1 will be granted Memory access priority because the $\overline{\text{I1TS}}$ and $\overline{\text{I1DS}}$ switches will be false, thus, P21S will be false. If P21S is false, its input is true. Then $\overline{\text{P21S}}$ is true, indicating that the priority of I/O-1 is greater than the priority of I/O-2.

2. If I/O-2 is controlling Tape and I/O-1 is controlling a Drum, then P21S will be true to indicate I/O-2 has priority. P21S will be true because I2D41D and $\overline{\text{I1TS}}$ terms are true.

3. If I/O-1 is controlling a Drum and I/O-2 is also controlling a Drum, then $\overline{\text{P21S}}$ will be true because there is no true gate into $\overline{\text{P21S}}$.

Note that the gates to $\overline{\text{P21S}}$, $\overline{\text{P31S}}$, $\overline{\text{P32S}}$, $\overline{\text{P42S}}$ and $\overline{\text{P43S}}$ are all similar. Therefore, the priority determination is made on the same basis for all of these switches. However, the priority determination between I/O-1 and I/O-4 is different. The reason the logic is different in this case is to provide more balanced loading of the Drivers D41D thru D45D.

To understand the logic here, it is preferable to consider the priority of I/O-1 over I/O-4 rather than the priority of I/O-4 over I/O-1.

P14S (priority of switch 1 is greater than switch 4) will be true if the gate to $\overline{\text{P14S}}$ is true. Therefore, the priority of I/O-1 will be greater than the priority of I/O-4 if I/O-1 is designated and one of the following conditions exist.

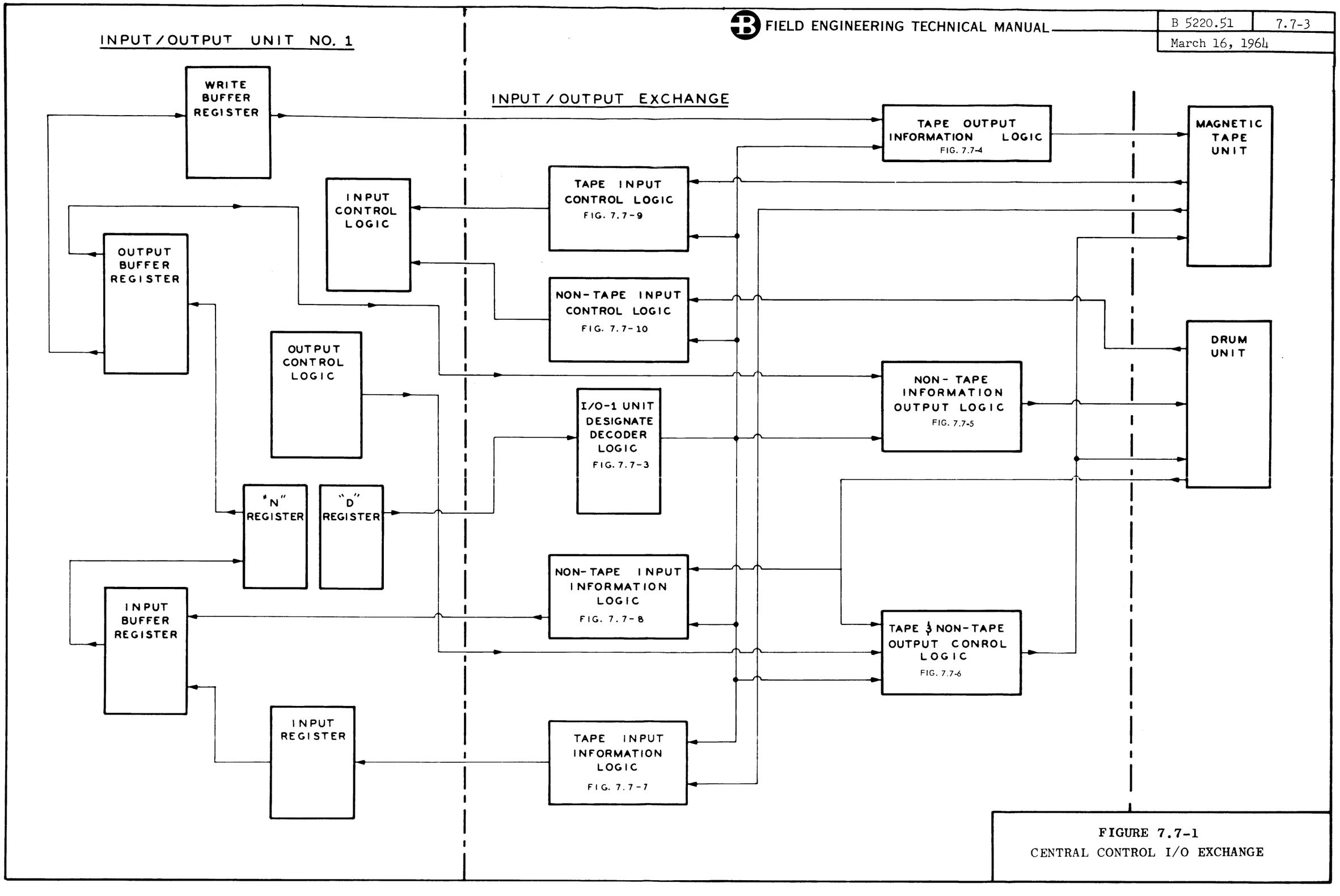


FIGURE 7.7-1
CENTRAL CONTROL I/O EXCHANGE

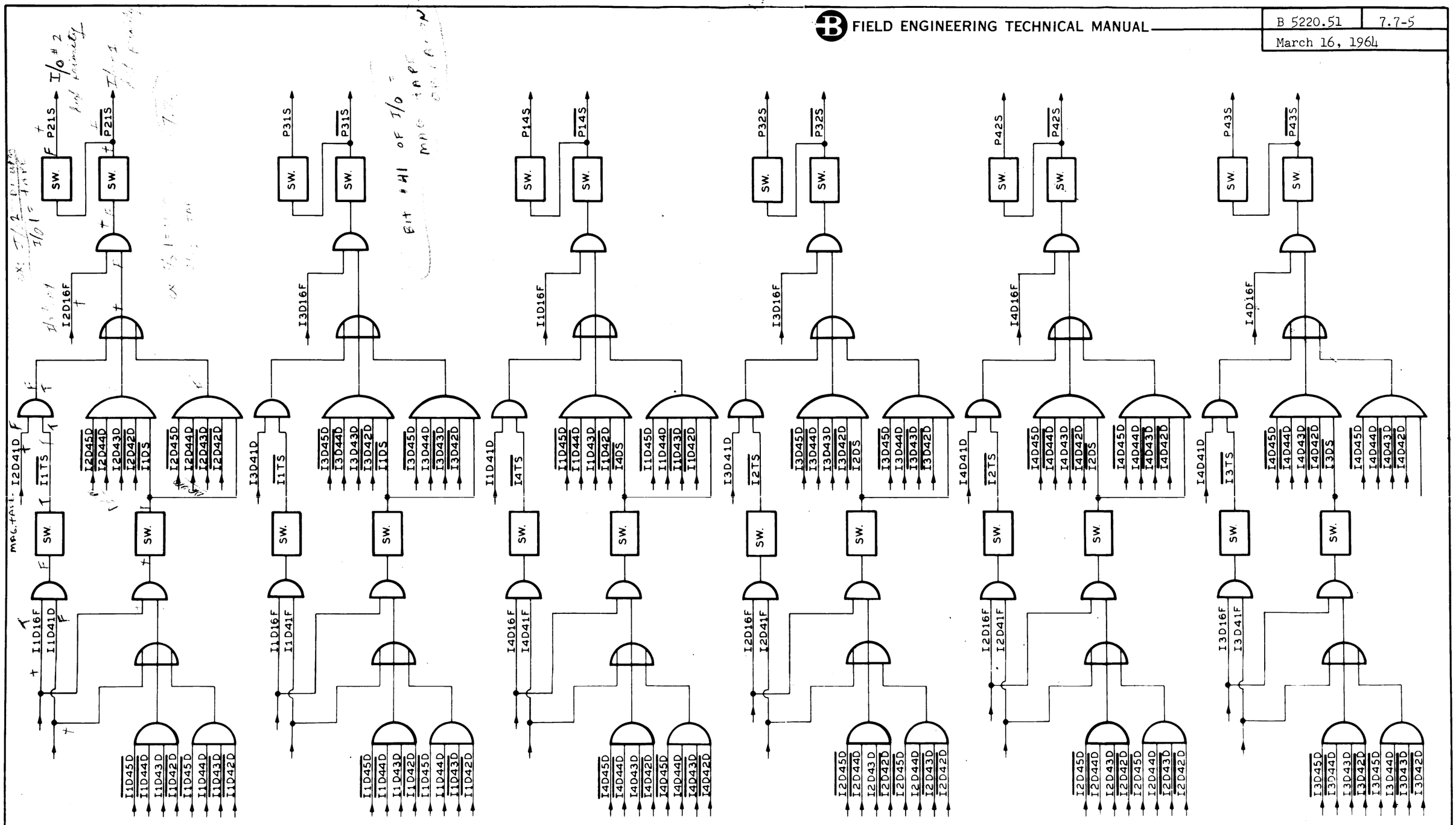


FIGURE 7.7-2
I/O PRIORITY DETERMINATION LOGIC

1. I/O-1 is controlling a Tape Unit.

2. I/O-1 is controlling a Drum 1 and I/O-4 is NOT controlling Tape.

3. I/O-1 is controlling Drum 2 and I/O-4 is NOT controlling Tape.

The gate to $\overline{\text{P14S}}$ will also be true if I/O-4 is NOT controlling a Tape Unit or a Drum (I14D3). This term allows I/O-1 priority in cases where both I/O Control Units are controlling Peripheral Units other than Tapes and Drums.

To review the complete Admit I/O gating: The purpose of the ARnS switches is to furnish Inhibit levels for the Crosspoint flip-flops associated with the I/O Memory Requests. The ARnS levels are ONLY required when there are simultaneous Memory Requests of the same Memory. The levels would be unnecessary if the requesting Memory Units of the I/O Control Units were requesting different Memory Units.

In cases of simultaneous requests for the same Memory, it is then necessary to determine which I/O Requesting Unit needs to be admitted. The need is determined by comparing the relative weights of the Peripheral Unit designations held by the I/O Control Units. The higher priority is assigned to ONE of the Requesting Units and this unit is permitted Memory access.

It may be noted that all four I/O Control Units and both Processors may request access to the same Memory at the same time. As will be seen later, the Processor requests are inhibited directly by any I/O request. Therefore, Processor requests are of the lowest priority. The four I/O requests are then assigned priority according to the peripheral unit designations. There should never be a situation, in the case of I/O requests, where more than TWO I/O Control Units controlling Tape are requesting the same Memory Unit. The scheduling route (a part of the Master Control Program) will prevent this situation from happening. If more than two I/O Control Units are using the same Memory, there is insufficient time between Tape words to execute a Memory cycle.

I/O EXCHANGE INFORMATION & CONTROL LINE LAYOUT

The I/O Exchange is laid out into two distinct sections. One section contains the transfer hardware for Magnetic Tape Control and Information Lines, while the second section contains the hardware for Non-Magnetic Tape Control and Information Lines.

In the I/O Control Unit there are three Registers which buffer the Information and Control Lines from Memory. The output from these lines have each bit gated to, and in some cases, through the I/O Exchange Unit.

Under these conditions, the I/O Control Unit can access through I/O Exchange the maximum of:

16 ..... Tape Transport Units

2 ..... Disk Files

2 ..... Card Readers

1 ..... Card Punch

2 ..... Drums

1 ..... Keyboard

* 2 ..... Paper Tape Readers

* 2 ..... Paper Tape Punches

2 ..... Printers

1 ..... Supervisory Printer

* Paper Tape is limited to 2 Readers and 1 Punch or, 1 Reader and 2 Punches.

The Tape section is repetitious logic repeated 16 times. The Non-Tape section is composed of individual gating which is designed to satisfy only the Peripheral Unit designated. For this reason, the Tape Units can be interchanged in the Display and Distribution Panel. However, the Non-Tape Units can be interchanged where provision is made in I/O Exchange to handle two units. A Printer and a Drum cannot be interchanged, but Printer 1 and Printer 2 can be interchanged.

The various lines are grouped as follows:

1. Unit Designation (13 lines) from I/O Control Units to Central Control only.
2. Output Information and Control from an I/O.
   a. Tape Information (7 lines).
   b. Non-Tape Information (7 lines).
   c. Control, Tape and Non-Tape (7 lines).
3. Input Information and Control to an I/O.
   a. Tape Information (7 lines).
   b. Non-Tape Information (7 lines).
   c. Tape Control (7 lines).
   d. Non-Tape Control (7 lines).

Tape and Non-Tape Information Lines are separate and operate into and out of different Character Registers. Tape Output Information comes from the WB Register in the I/O and Non-Tape Output Information comes from the OB Register. Tape Information enters the IR Register in the I/O and Non-Tape Information enters the IB Register.

UNIT DESIGNATE DECODER

The primary control for routing or gating the flow of Information and Control Lines between the Peripheral Unit and an I/O, is the Unit Designate Decoder Drivers. There are four groups of drivers, one for each I/O. They are similar, except the

gating to these drivers comes from different I/O Control Units as illustrated in Figure 7.7-3.

Each I/O sends 13 lines to the Designate Decoder. Ten of these lines are the 0 and 1 side of D41F thru D45F. One line is the 1 side of D16F, and the two remaining lines are from Z46D and $\overline{Z46D}$.

One driver exists for each Peripheral Unit in each of the four groups. In general form they are IkUnnD. The k is the I/O number and nn is the Peripheral Unit designation number.

The Input gating to these drivers is basically the designation bits and the Designate Control Flip-flop D16.

If a Unit Designation Conflict does not exist, an AUNS term will be true and return to the I/O to permit the D16F to be set. As soon as D16F is set, it will permit one of the Unit Designate Drivers in the Central Control to be true. This will connect the desired Peripheral Unit and I/O together. When a Unit Designate Driver goes true, it will gate the necessary Information and Control Lines between the I/O and Peripheral Unit.

Some of the Peripheral Units communicate in only one direction with information. For example; the Card Punch or Paper Tape Punch would only RECEIVE Information from the I/O: the Card Reader or Paper Tape Reader would only SEND Information to the I/O.

The D24F in the I/O indicates in which direction this information will flow. For a READ or an Input operation, D24F would be ON and a WRITE or Output operation D24F would be OFF. The Unit Designation of these "single direction" units could then be used for another "single direction" unit if the D24 bit was ANDED in these Unit Designate Drivers and thus permit more Unit Designates. This is precisely what is done for the Card Reader, Card Punch, Paper Tape Reader and Paper Tape Punch.

The Card Reader and the Card Punch have the same Unit Designation (U10) except the D24 is ON during the READ and OFF for the WRITE.

To indicate this WRITE OR NOT WRITE status, two drivers in the I/O Z46D and $\overline{Z46D}$ are sent directly to the Central Control in place of D24F and D16F.

$$Z46D = \overline{D24F}\ D16F$$

$$\overline{Z46D} = D24F\ D16F$$

The Unit Designate Driver in Central Control for Card Reader is U10D-In and has the $\overline{Z46D}$ Driver on its Input, while the Unit Designate Driver in Central Control for Card Punch is U42D-In and has the Z46D term on its Input.

INPUT CONTROL INVERTERS

These Inverters are used to invert some of the signal lines to obtain the necessary polarity for operation.

OUTPUT FROM I/O

The Drivers or Switches which transmit information or control to Peripheral Units are driven by four-legged OR gates. Each leg on an OR gate has the corresponding signals from the four I/O Control Units and their associated Unit Designate Drivers.

TAPE INFORMATION OUTPUT

Figure 7.7-4 illustrates the manner in which Tape Information comes from a seven (7) bit Character Register in the I/O, WB1F thru WBPF. Seven (7) switches associated with each Tape Unit transmit the Information to the Unit.

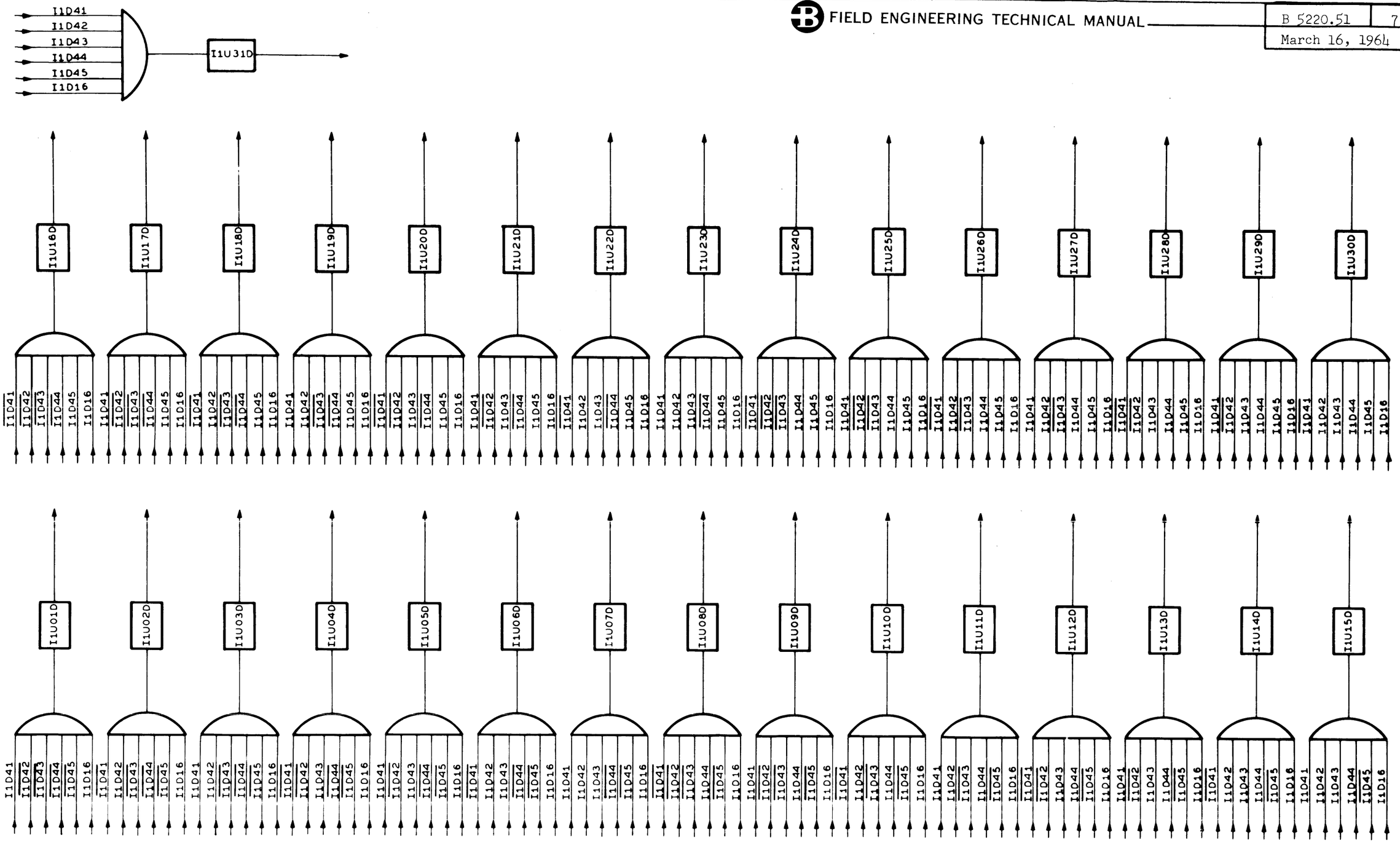
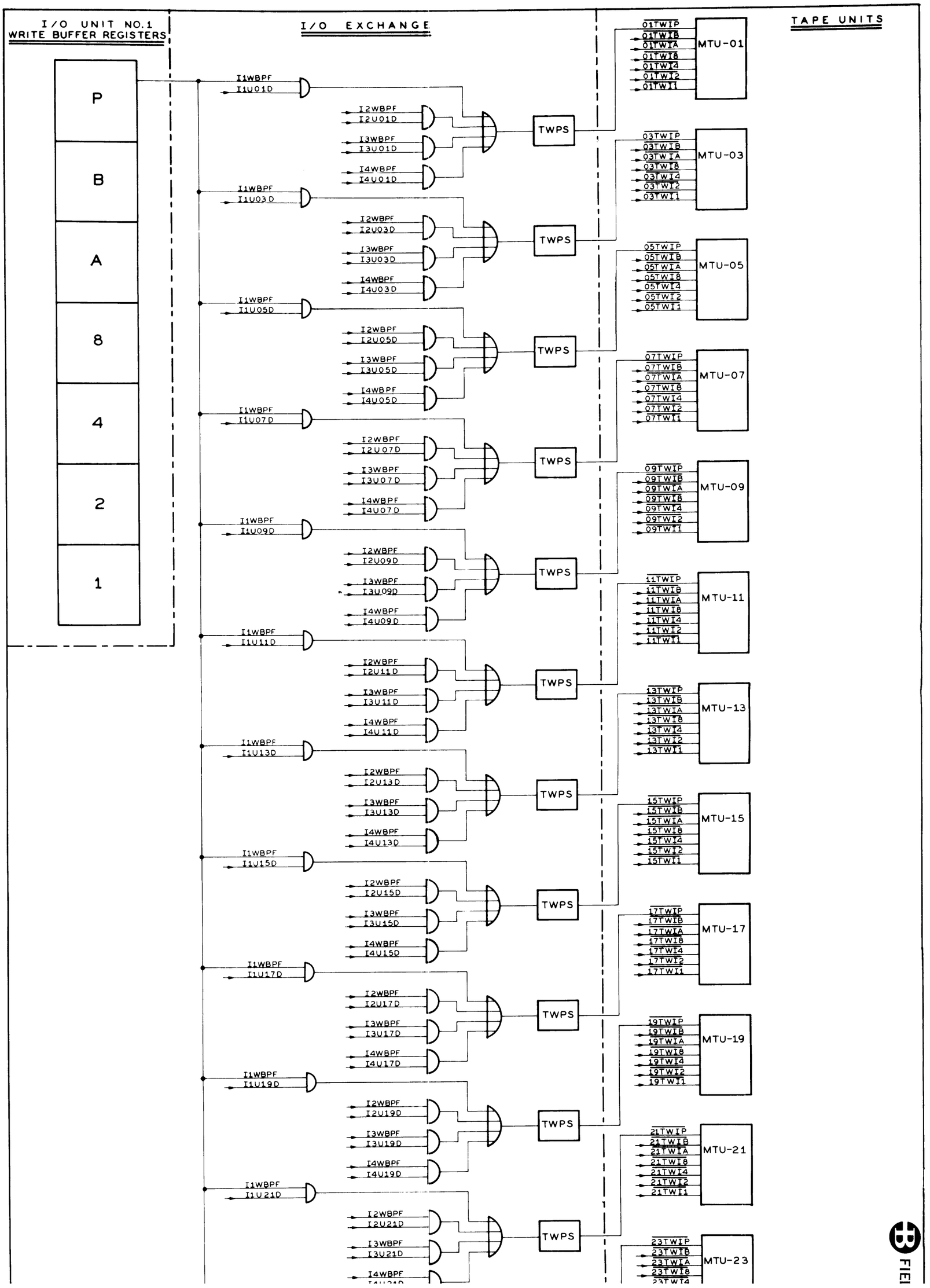


FIGURE 7.7-3
UNIT DESIGNATE DECODER LOGIC


I/O UNIT NO.1
WRITE BUFFER REGISTERS
P
B
A
8
4
2
1
I/O EXCHANGE
I1WBPF
I1U01D
I2WBPF
I2U01D
I3WBPF
I3U01D
I4WBPF
I4U01D
I1WBPF
I1U03D
I2WBPF
I2U03D
I3WBPF
I3U03D
I4WBPF
I4U03D
I1WBPF
I1U05D
I2WBPF
I2U05D
I3WBPF
I3U05D
I4WBPF
I4U05D
I1WBPF
I1U07D
I2WBPF
I2U07D
I3WBPF
I3U07D
I4WBPF
I4U07D
I1WBPF
I1U09D
I2WBPF
I2U09D
I3WBPF
I3U09D
I4WBPF
I4U09D
I1WBPF
I1U11D
I2WBPF
I2U11D
I3WBPF
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I4WBPF
I4U11D
I1WBPF
I1U13D
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I4U13D
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I3WBPF
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I4WBPF
I4U19D
I1WBPF
I1U21D
I2WBPF
I2U21D
I3WBPF
I3U21D
I4WBPF
TWPS
TWPS
TWPS
TWPS
TWPS
TWPS
TWPS
TWPS
TWPS
TWPS
TWPS
TAPE UNITS
01TWIP
01TWIB
01TWIA
01TWI8
01TWI4
01TWI2
01TWI1
MTU-01
03TWIP
03TWIB
03TWIA
03TWI8
03TWI4
03TWI2
03TWI1
MTU-03
05TWIP
05TWIB
05TWIA
05TWI8
05TWI4
05TWI2
05TWI1
MTU-05
07TWIP
07TWIB
07TWIA
07TWI8
07TWI4
07TWI2
07TWI1
MTU-07
09TWIP
09TWIB
09TWIA
09TWI8
09TWI4
09TWI2
09TWI1
MTU-09
11TWIP
11TWIB
11TWIA
11TWI8
11TWI4
11TWI2
11TWI1
MTU-11
13TWIP
13TWIB
13TWIA
13TWI8
13TWI4
13TWI2
13TWI1
MTU-13
15TWIP
15TWIB
15TWIA
15TWI8
15TWI4
15TWI2
15TWI1
MTU-15
17TWIP
17TWIB
17TWIA
17TWI8
17TWI4
17TWI2
17TWI1
MTU-17
19TWIP
19TWIB
19TWIA
19TWI8
19TWI4
19TWI2
19TWI1
MTU-19
21TWIP
21TWIB
21TWIA
21TWI8
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MTU-21
23TWIP
23TWIB
23TWIA
23TWI8
23TWI4
MTU-23

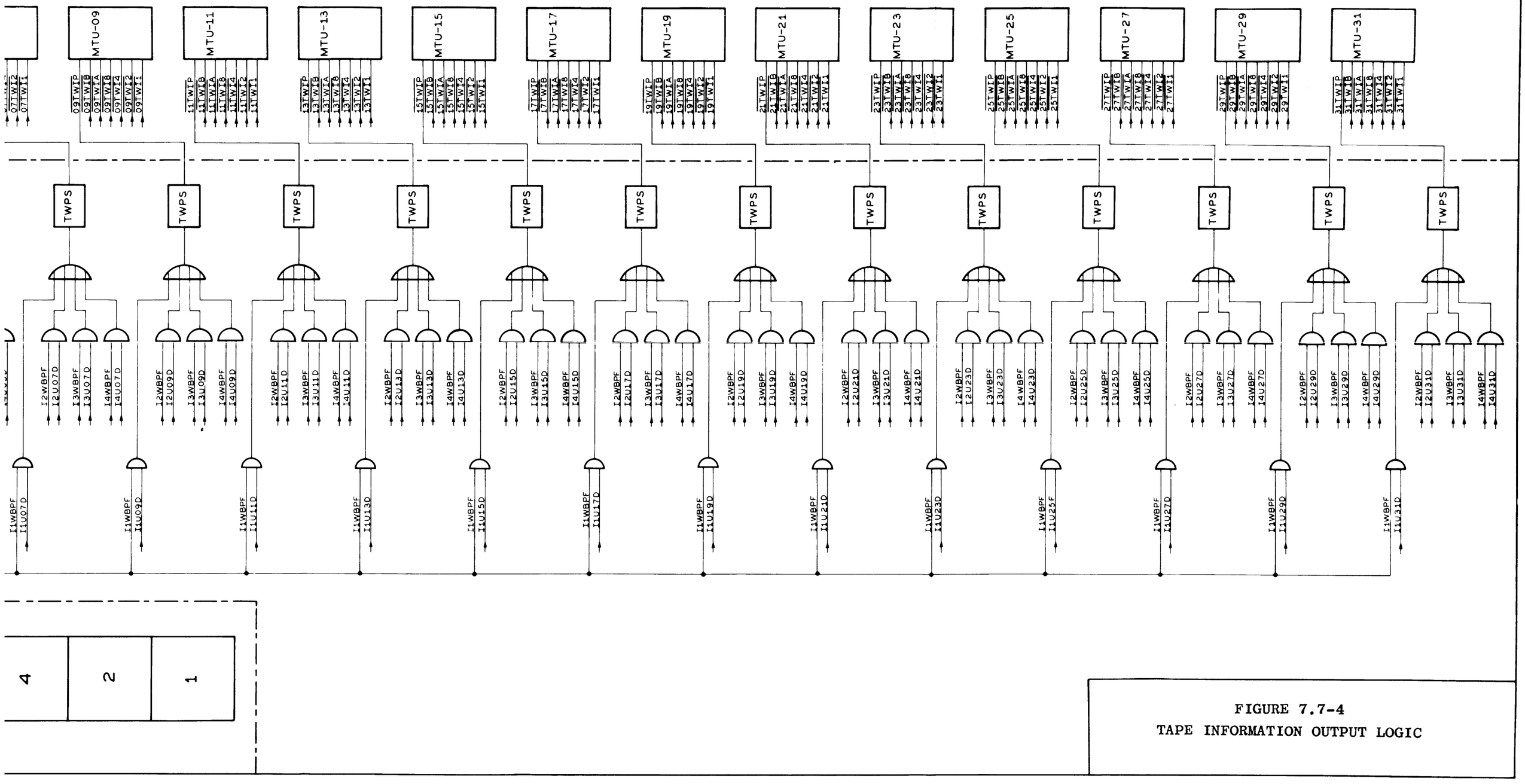


FIGURE 7.7-4
TAPE INFORMATION OUTPUT LOGIC

NON-TAPE INFORMATION OUTPUT

Figure 7.7-5 illustrates that all Non-Tape information comes from a seven (7) bit Character Register in the I/O, OB1F thru OBBF and OBRD. All seven bits from OB Register do not go to every Peripheral Unit. The Peripheral Unit and its required information are listed below:

1. Printer - OB1F thru OBBF and OBPD (7 lines).
2. Inquiry - OB1F thru OBBF and OBPD (7 lines).
3. SPO/KD - OB1F thru OBBF (6 lines)

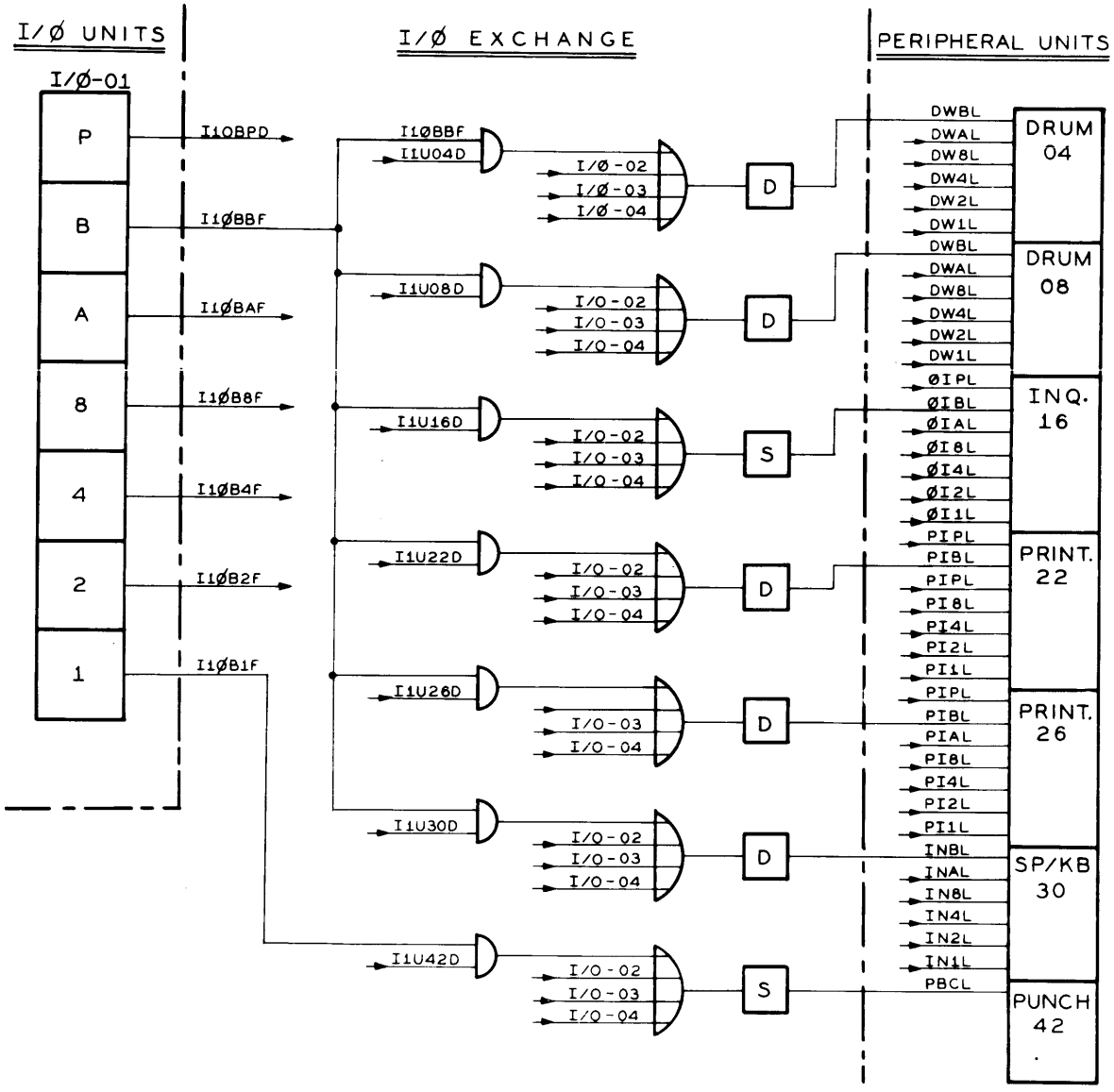


FIGURE 7.7-5 NON-TAPE INFORMATION OUTPUT LOGIC

4. Drum - OB1F thru OBBF (6 lines).

5. Punch - OB1F (1 line).

6. Paper Tape - PBCL, PO2L thru POBL, and POPL (7 lines).

OUTPUT CONTROL LINES

Figure 7.7-6 illustrates the seven (7) Output Control Lines originating in the I/O Channel. They are time shared with all Peripheral Units.

All 7 lines are not needed by all Peripheral Units.

The control functions for various types of peripheral units are ORed together in the I/O and feed common Drivers. These Drivers are 021D thru 027D.

The Driver Outputs are sent to the I/O Exchange where each line is ANDed with the appropriate Unit Designate Drivers.

Only those types of units requiring a particular control function will be ANDed with a particular control line.

The Output of the AND gate is then ORed with three other AND gates from three remaining I/O Control Units, and then drives a switch or Driver to the Peripheral Units.

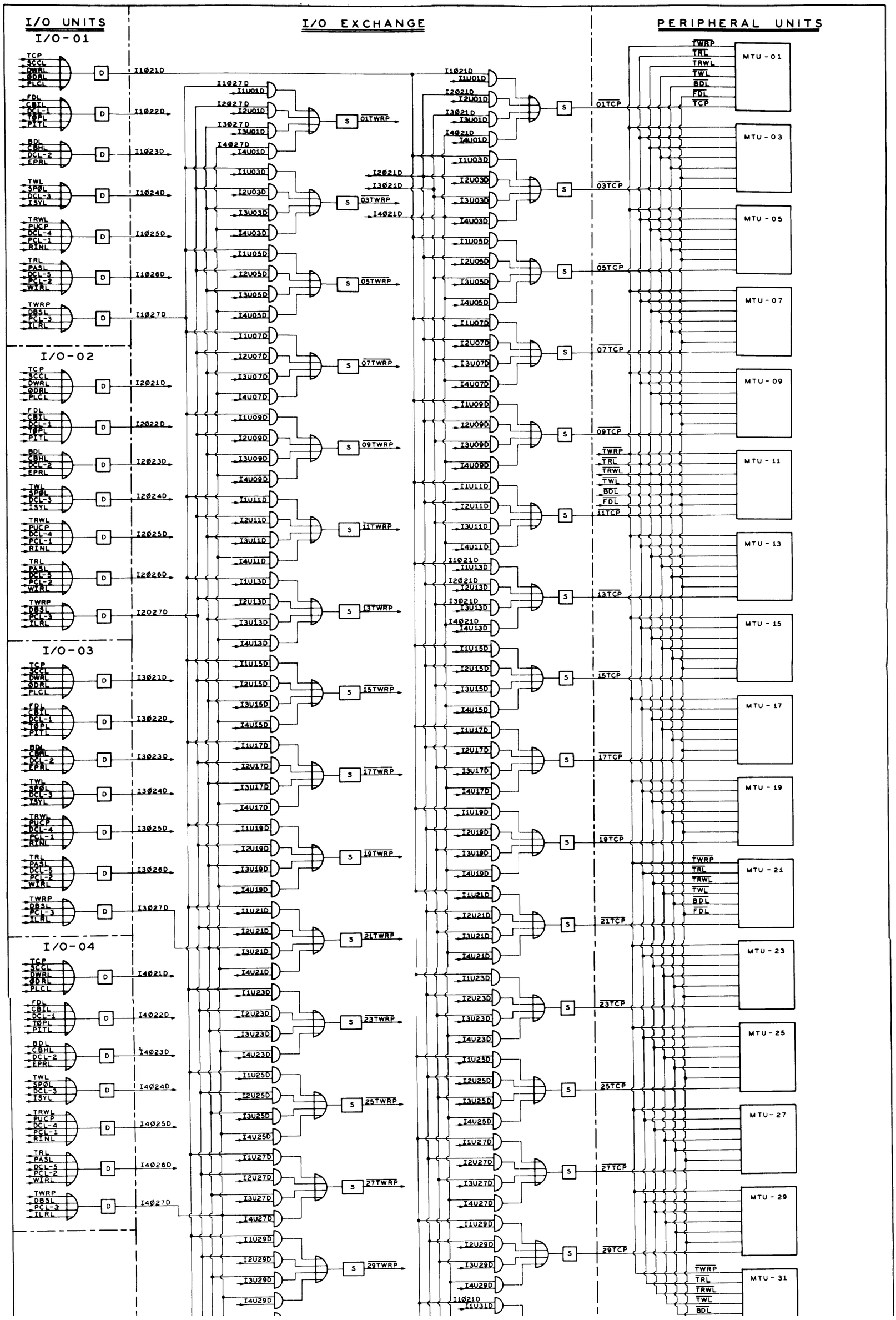
The following chart gives the Output Driver and the control function it carries.

TAPE AND NON-TAPE OUTPUT CONTROL

	TAPE	CARD READ	CARD PUNCH	DRUM	SP/KB	PAPER TAPE	PRINTER	INQUIRY
021D	TCP	SCCL		SWRL	ODRL	PUCP	PLCL	
022D	FDL	CBIL		DCL-1	TOPL	PBNL	PITL	
023D	BDL	CBHL		DCL-2			EPRL	
024D	TWL		SPOL	DCL-3				ISYL
025D	TRWL		PUCP	DCL-4				RINL
026D	TRL		PASL	DCL-5		SPOL		WIRL
027D	TWRP		DBSL					ILRL

INPUT TO AN I/O

The Drivers or Compressors which transmit information or control to an I/O are driven by OR gates whose inputs vary in number according to the signals from the Peripheral Units. The quantity of packages driving to any one I/O must be duplicated for each I/O on the system.


I/O UNITS
I/O-01
I/O-02
I/O-03
I/O-04
I/O EXCHANGE
PERIPHERAL UNITS
MTU-01
MTU-03
MTU-05
MTU-07
MTU-09
MTU-11
MTU-13
MTU-15
MTU-17
MTU-19
MTU-21
MTU-23
MTU-25
MTU-27
MTU-29
MTU-31
TCP
SCCL
DWRL
ODRL
PLCL
FDL
CBIL
DCL-1
TOPL
PITL
BDL
CBHL
DCL-2
EPRL
TWL
SPOL
DCL-3
ISYL
TRWL
PUCP
DCL-4
PCL-1
RINL
TRL
PASL
DCL-5
PCL-2
WIRL
TWRP
DBSL
PCL-3
XLRL
D
S

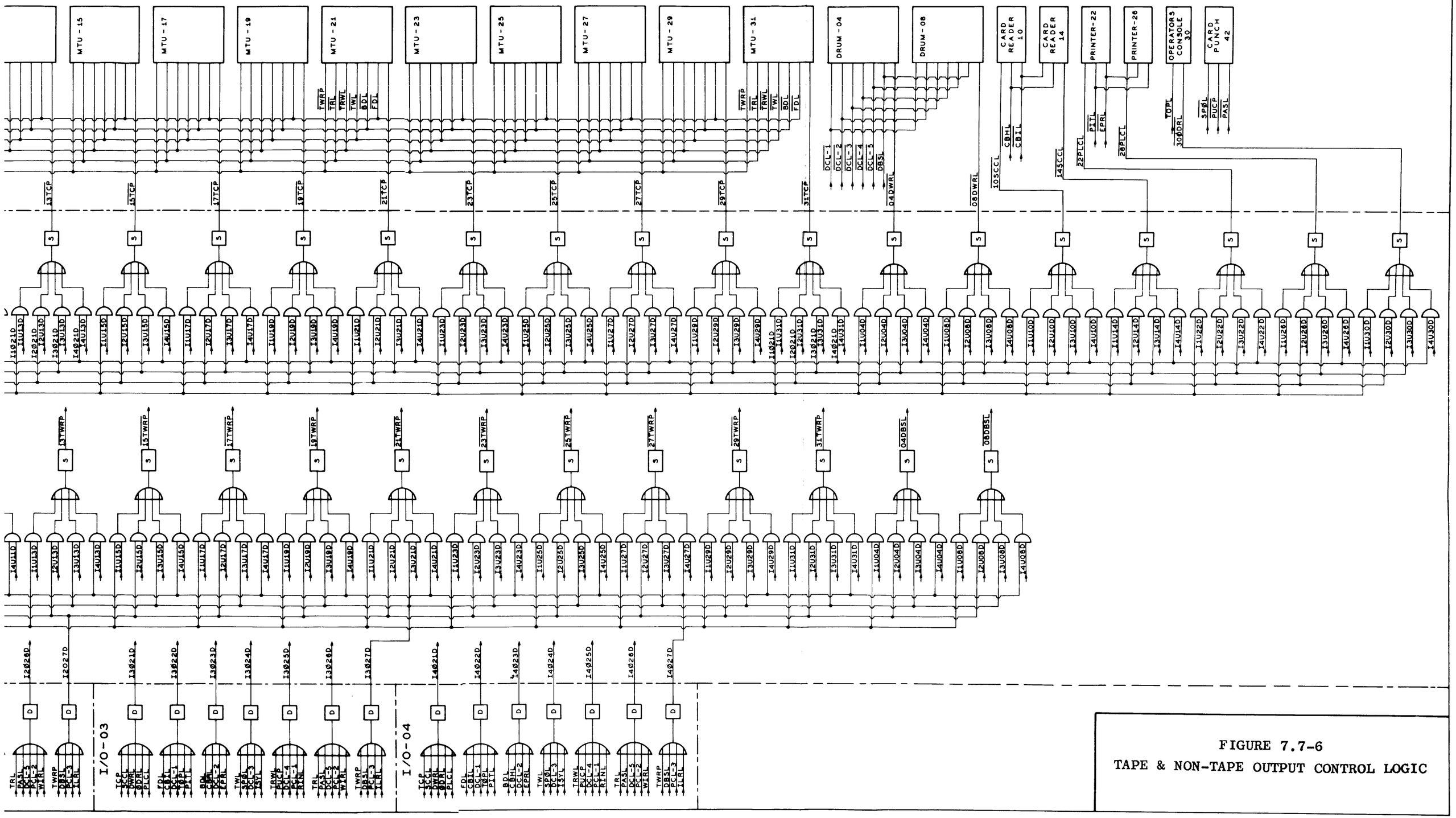


FIGURE 7.7-6
TAPE & NON-TAPE OUTPUT CONTROL LOGIC

TAPE INFORMATION INPUT

Figure 7.7-7 illustrates that seven Information lines leave each MTU and each line drives four two-legged AND gates.

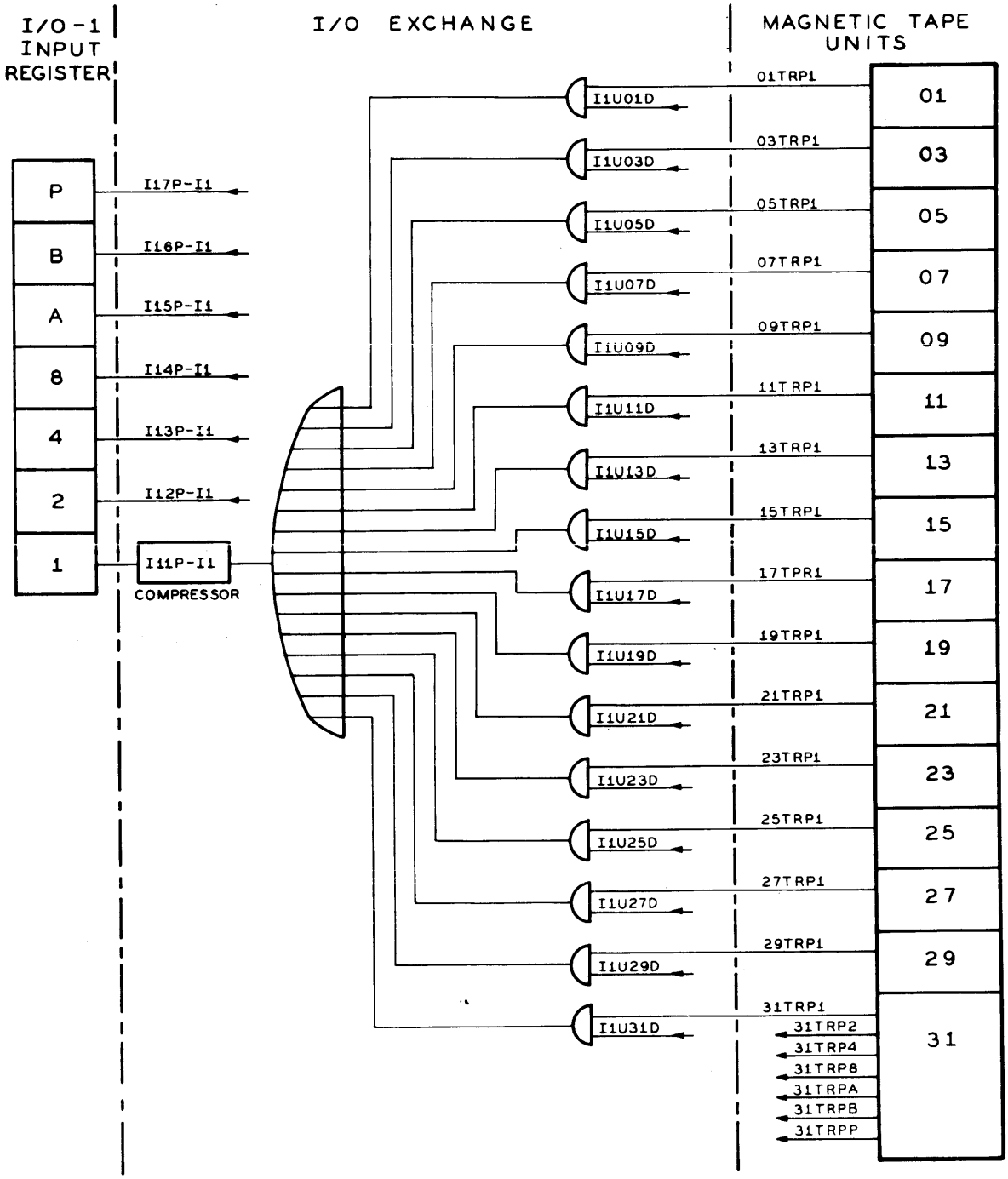


FIGURE 7.7 7 TAPE INFORMATION INPUT LOGIC

Each AND gate will feed one of four I/O Control Units. The other leg of the AND gate is driven by the Unit Designate Driver for the particular I/O communicating with that MTU.

All sixteen AND gates with the same information bit from all MTUs designated by the same I/O Channel are then ORed together and drive a Compressor package.

The purpose of the Compressors is to reduce the width of the Information pulses from the MTU from approximately 2.3 to 0.5 μs.

One Compressor package drives its corresponding flip-flop in the IR Register.

NON-TAPE INFORMATION INPUT

Figure 7.7-8 illustrates six Non-Tape Units capable of sending information into the I/O. These Non-Tape Units and Designations are:

DRUM	04	INQUIRY	16
DRUM	08	PAPER TAPE	18
CARD READER	10	PAPER TAPE	20
CARD READER	14	SP/KB	30

Each of these Units sends six or seven lines of Information and each line drives four two-legged AND gates, similar to Tape Information Input.

The AND gates containing the same Information bit from the different units and same I/O Designation are then ORed together and drive a Driver Package.

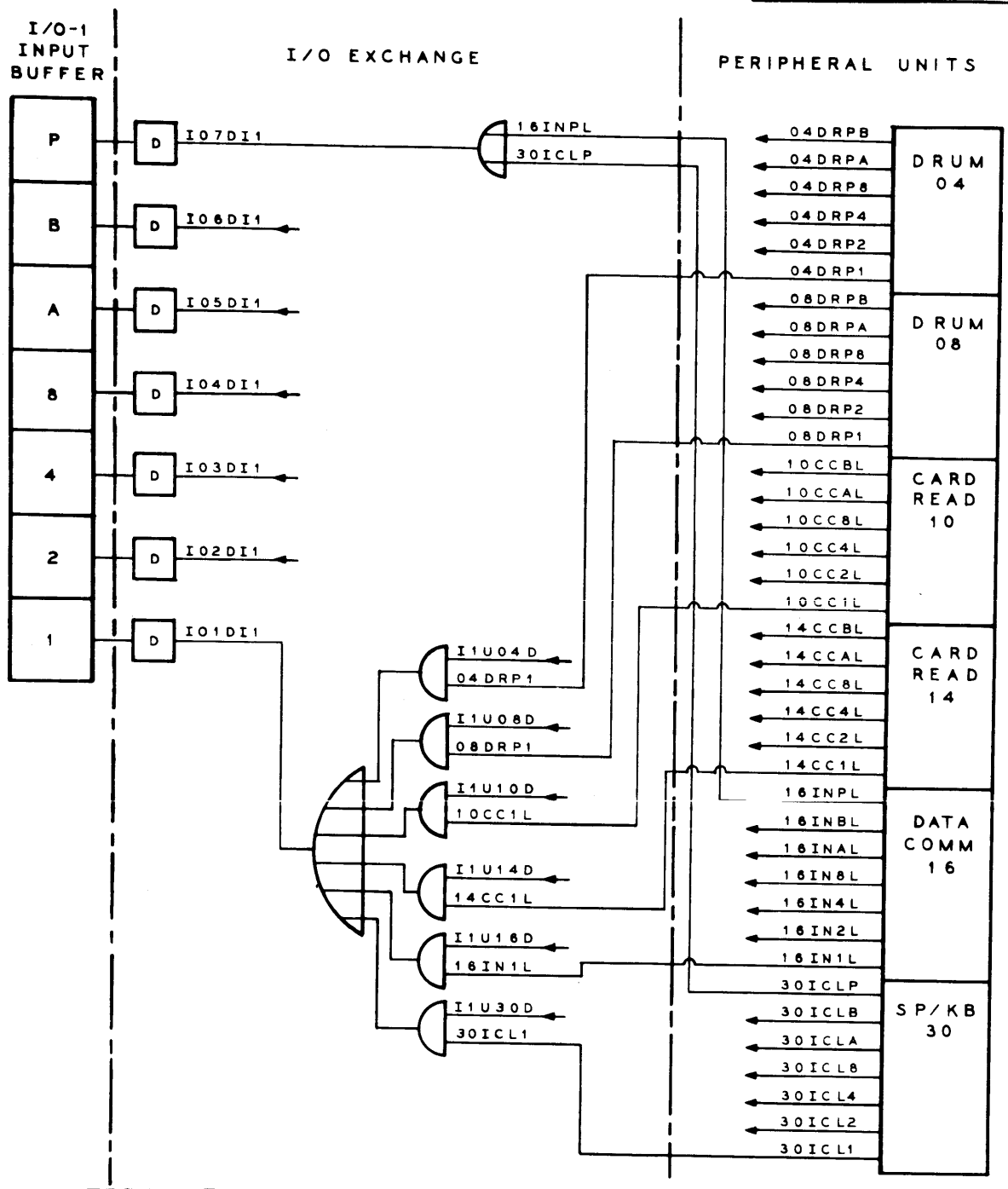
This Driver drives its corresponding flip-flop in the IB Register in the I/O.

TAPE INPUT CONTROL LINES

Figure 7.7-9 illustrates seven Control lines from each MTU. These lines are connected through the I/O Exchange to the Designating I/O Channel.

The Control lines are first put through switches in the I/O Exchange for inversion purposes. Each line is then ANDed with an I/O Unit Designate Driver. The AND gate then is fed into a sixteen-legged OR gate (the remaining 15 legs are the same Control function from the remaining MTUs and their Unit Designate Driver).

The OR gate drives a Driver Package whose Output goes to one I/O.



✓ FIGURE 7.7-8 NON-TAPE INFORMATION INPUT LOGIC

✓ TAPE INPUT CONTROL LINES

SIGNAL	SWITCH	LINE
$\overline{\text{TTOL}}$	TTOS	I31D
$\overline{\text{TREL}}$	TRES	I32D
$\overline{\text{TLPL}}$	TLPS	I34D
$\overline{\text{TWRL}}$	TWRS	I35D
$\overline{\text{TWSL}}$	TWSS	I36D
$\overline{\text{THDL}}$	THDS	I37D
$\overline{\text{TEFL}}$	TEFS	I38D
$\overline{\text{TSIL}}$		$\overline{\text{I39D}}$
$\overline{\text{THVL}}$		$\overline{\text{I40D}}$

✓Changes or additions since last issue.

NON-TAPE INPUT CONTROL LINES

Figure 7.7-10 illustrates the eight lines which are needed to carry all the Control functions from the Non-Tape Peripheral Units to any of the I/O Control Units.

These lines are shared as to the type of Control function for the different types of Peripheral Units. All eight lines are not needed by all of these Non-Tape Peripheral Units.

Some of the Control lines from the Peripheral Units must be inverted; therefore, they are first put through a switch. Each line is then ANDed with an I/O Unit Designate Driver.

The AND's are then assembled into groups, ORed together, and put through a driver.

The chart below gives the Input Driver name and the Control function it carries.

✓ NON-TAPE INPUT CONTROL

	CARD READ	CARD PUNCH	DRUM	SP/KB	PAPER TAPE	PRINTER	DATA COMM
I21D	CRL	PURL	DURL	TRDL	$\overline{\text{PURL}}$	PRRL	ISRL
I22D	CCL	PUCL	DWCL			PCYL	ILFL
I23D		PRAL			PUEL	PLLL	IFAL
I24D	CSP	PRBL	DCLP	ICRL + OCRL	$\overline{\text{PINL}}$	PLCP	IRTL
I25D	CREF	PUEF	DWLL		PETL	PPEL	IWRL
I26D		PRDL					IRRL
I27D		PINL				PAML	
I28D	EOFL	PRCL				EOPL	

MAGNETIC TAPE UNITS

01 | 03 | 05 | 07 | 09 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 | 27 | 29 | 31

01TTØ
01TREL
01TLPL
01TWRL
01TWSL
01THDL
01TEFL
03TTØ
03TREL
03TLPL
03TWRL
03TWSL
03THDL
03TEFL
05TTØ
05TREL
05TLPL
05TWRL
05TWSL
05THDL
05TEFL
07TTØ
07TREL
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27TTØ
27TREL
27TLPL
27TWRL
27TWSL
27THDL
27TEFL
29TTØ
29TREL
29TLPL
29TWRL
29TWSL
29THDL
29TEFL
31TTØ
31TREL
31TLPL
31TWRL
31TWSL
31THDL
31TEFL

S

01TTØS I1U01D
03TTØS I1U03D
05TTØS I1U05D
07TTØS I1U07D
09TTØS I1U09D
11TTØS I1U11D
13TTØS I1U13D
15TTOS I1U15D
17TTOS I1U17D
19TTOS I1U19D
21TTOS I1U21D
23TTOS I1U23D
25TTOS I1U25D
27TTOS I1U27D
29TTOS I1U29D
31TTOS I1U31D

I/O EXCHANGE

D

I31D-I1
I32D-I1
I34D-I1
I35D-I1
I36D-I1
I37D-I1
I38D-I1

I/O UNITS

I/O-01

FIGURE 7.7-9
TAPE INPUT CONTROL LOGIC

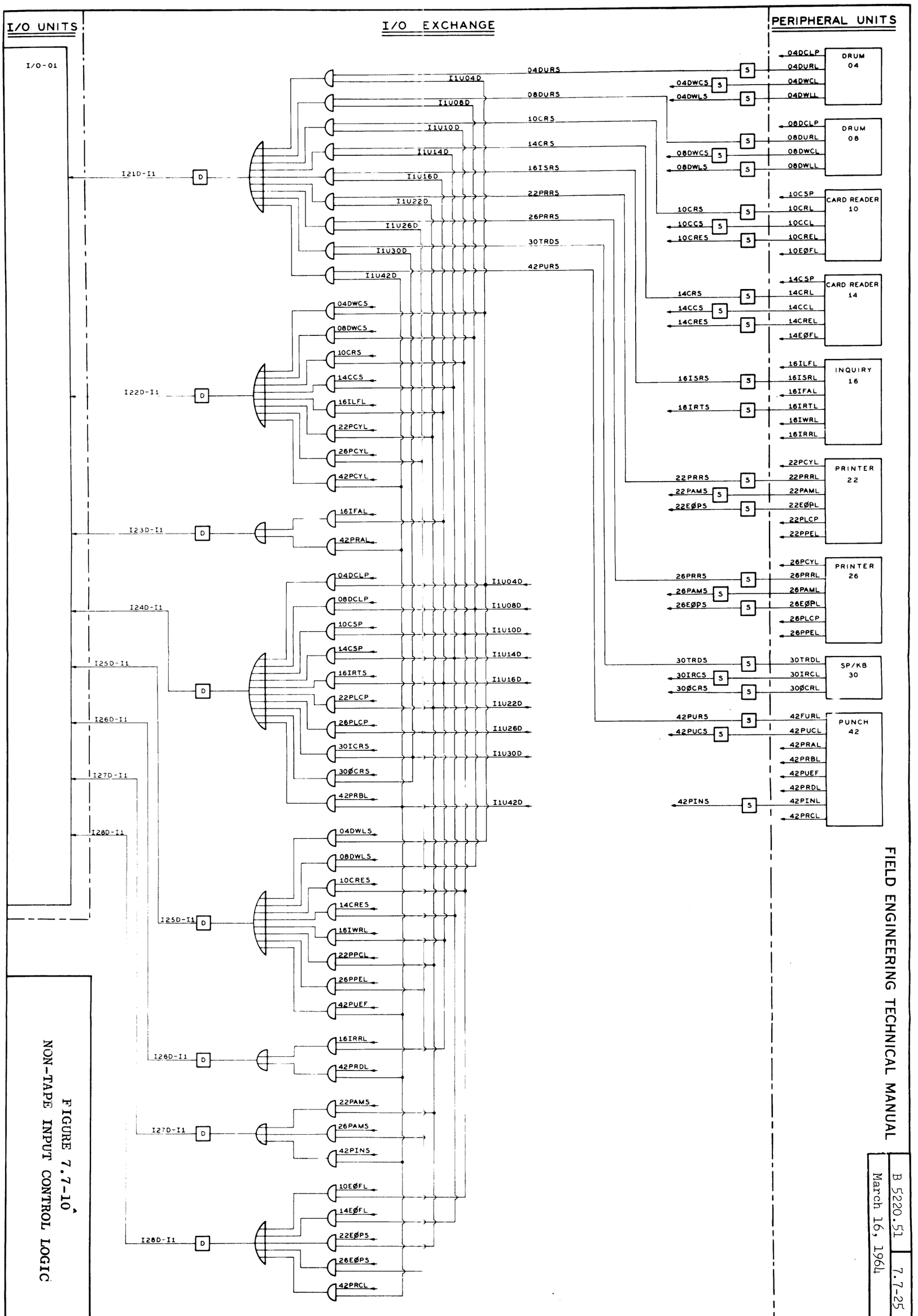

FIGURE 7.7-10.
NON-TAPE INPUT CONTROL LOGIC

7.8 MISCELLANEOUS LOGIC AND HARDWARE

DISPLAY PANEL

The Central Control Maintenance Panel which is located at the top of the "A" Rack in the Display & Distribution Cabinet, contains all the necessary switches and indicators for the Central Control Unit.

All flip-flops in the Central Control have a neon indicator on the Display Panel. These indicators are the familar Switch Light Driver Assembly, and are considered in two groups; the Crosspoint Flip-flops and the Control Flip-flops.

The Crosspoint group has 56 indicators; 8 for the Memory Cycle Flip-flops, and the remaining 48 for the Crosspoint Flip-flops.

The Control group contains 37 indicators which are; 2 Clock Flip-flops, 4 ADnFs, 14 Interrupt Flip-flops, 7 Interrupts Address and Sync Flip-flops, 6 Real Time Flip-flops, and 4 Miscellaneous Control Flip-flops.

The CLEAR or RESET buttons are as follows:

1. MASTER CLEAR - Clear all flip-flops in the system.
2. CROSSPOINT - Clears the 56 flip-flops mentioned above.
3. CONTROL - Clears the 37 flip-flops mentioned above.
4. BIT RESET - In conjunction with any particular set button on the Central Control Display Panel, that associated flip-flop will be reset to "0".

POWER OFF BUTTON

A Power OFF button will cycle the entire system Power Down except convenience outlets. Three such buttons are located on the system; one on the Operators Console, one on the Power Supply Meter Panel, and the third is located on the Central Control Display Panel.

DC LOCKOUT SWITCH

When placed in the LOCKOUT position, this switch will pick K19 and turn OFF the +20V Supply. Turning OFF +20V forces the Series Regulators in all cabinets to turn OFF (-4.5V, -1.2V and -12V). The DC ON light will also go OFF if LOCKOUT or POWER OFF are activated.

PA1L/PB1L SWITCH

The Toggle Switch PA1L/PB1L will select whether Processor A or Processor B is designated P1.

LOAD BUTTON

When depressed, the LOAD button will cause a Card Read or Drum Read depending on the LOAD Select Switch on the Console, and cause the system to START.

HALT BUTTON

When depressed, the HALT button on the Console or D & D will HALT Processor 1 and Processor 2 after completion of the Syllables being executed.

The HIBL level will go false when the HALT button is depressed and cause a false level, HIMD, to the Processors. Also, an incandescent Driver HIND, will send a true level to the HALT light on the Console.

DOUBLE-NORMAL-SINGLE SWITCH

A three position toggle switch, Double-Normal-Single, selects the Mode of Operation for the Clock. Regardless of the Mode of Operation for the Clock, the CLOCK button must be depressed to start the Clock. In SINGLE position, only one pulse will be emitted for every depression of the CLOCK button. When in DOUBLE position, two pulses will be emitted to the system for every depression of the CLOCK button. In NORMAL position, the depression of the CLOCK button will provide a continuous string of pulses to the system.

INHIBIT CCIO3F

The toggle switch marked INHIBIT CCIO3F inhibits a Real Time Interrupt when in the UP position.

CONTROL STATE

The Control Indicators are ON when that corresponding Processor is in the Control State (only P1 can be in the Control State).

NORMAL STATE

The Normal Indicators are ON when that corresponding Processor is in the Normal State. (Both Processors may be in the Normal State.)

HALT INDICATOR

The HALT Indicator will be ON as soon as the HALT button is depressed and will stay ON until the system is cleared or Power is OFF.

CABLE INTERLOCKS

Included in one of the cables from each of the eight (8) Memory Units, each of the I/O Control Units, and two of the Peripheral Units (Drum Units), is a line that is grounded in the particular unit.

If the Unit is connected to Central Control, then Central Control is aware of the presence of the Unit by the ground (false) level. If the Unit is not present, or caused to be made not present, the ground will not be on the line. The line will instead be open. An R1A diode stick is connected to the input of each Cable Interlock Switch. With the Interlock line open, the switch will be turned ON to present a false level to the Central Control logic. If the line is grounded, the switch will be true to indicate the presence of the particular Unit.

A System NOT READY Incandescent Driver is used to indicate a PRESENT BUT NOT AVAILABLE status of any of the Interlocked Units and the SPO and Keyboard. The Incandescent Indicator will not indicate a NOT READY condition for units that are not present in the system.

REAL TIME CLOCK

The Real Time Clock is a standard six bit binary counter which counts once per cycle of 60 cycle AC, or roughly, every 16 2/3 ms. Approximately once every 1.07 seconds, the counter will overflow and set an Interrupt and is used to time programs etc. The 60 cycles comes from the Power Supply and goes through two switches in Central Control to increase Rise Time. The switch output goes to a synchronizer which in turn will count the TM1F counter thru TM6F.

I/O DESIGNATION

The I/O Designation is dependent on where it is plugged into the Central Control. It must know which Unit it is (No. 1, 2, 3 or 4) for the Result Descriptor Address.

To determine this, four lines are sent to each I/O. These lines are CD1L, $\overline{\text{CD1L}}$, CD2L and $\overline{\text{CD2L}}$. Two of these lines are grounded and two are left floating which will be a true (approximately -3V) due to its termination in the I/O. For I/O-1, the lines CD1L and CD2L will be grounded in Central Control, and $\overline{\text{CD1L}}$ and $\overline{\text{CD2L}}$ will be left open.

I/O-02 = CD1L $\overline{\text{CD2L}}$

I/O-03 = $\overline{\text{CD1L}}$ CD2L

I/O-04 = CD1L CD2L

INCANDESCENT DRIVERS

Seven Incandescent Drivers located in the Central Control Unit control seven indicators on the Console. The seven indicators and the drivers are listed below:

1. NOT READY - SNRD
2. MEMORY CHECK - MPID
3. "A" CONTROL - PACOSD
4. "A" NORMAL - PANOSD
5. "B" NORMAL - PBNOSD
6. "B" CONTROL - PBCOSD
7. HALT - HIND

The Memory Check indicator will be ON if there is a Memory Parity Error in either one of the Processors.

7.9 GLOSSARY

MISCELLANEOUS LINES

CLEAR SENSE	This line from D & D will be true when the MASTER CLEAR in D & D is actuated.
$\overline{\text{CLEAR}}$	$\overline{\text{CLEAR SENSE}}$ - This line will be false for a true input from CLEAR SENSE in D & D.
$\overline{\text{EXT INT}}$	$\overline{\text{EXTERNAL INTERRUPT}}$ - A true level output indicates that an External Interrupt exists.
$\overline{\text{INH PA SYL}}$	$\overline{\text{INHIBIT PROCESSOR A SYLLABLE INTERRUPT}}$ - This level is used in priority gating to set the Interrupt Address Register. When this level is false, there is a Non-Syllable PA Interrupt and this takes priority over all Processor Syllable Interrupts.
$\overline{\text{INH PB SYL}}$	$\overline{\text{INHIBIT PROCESSOR B SYLLABLE INTERRUPT}}$ - This level is used in the priority gating to get the Interrupt Address Register into Processor B. (See preceding definition.)
INITIATE P2	INITIATE PROCESSOR 2 COMMON AND GATE - This level when true will drive CA AP KD or CB AP KD to initiate Processor 2.
$\overline{\text{INT 1-4}}$	NO CC INTERRUPT 1-4 COMMON AND GATE - When true, this level indicates that CCIO3 and CCIO4 are not ON.
$\overline{\text{INT 1-6}}$	NO CC INTERRUPT 1-6 COMMON ANG GATE - When true, this level indicates that CCIO3, CCIO4, CCIO5 and CCIO6 are not ON.
$\overline{\text{INT 7-9}}$	NO CC INTERRUPT 7-9 COMMON AND GATE - When this level is true, it indicates that CCIO7, CCIO8 and CCIO9 are not ON.
$\overline{\text{INT 1-12}}$	NO CC INTERRUPT 1-12 COMMON AND GATE - When true, this level indicates that no CC Interrupt Flip-flop is ON from CCIO3 to CCI12.
$\overline{\text{MOSP}}$	$\overline{\text{MASTER OSCILLATOR OUTPUT}}$ - This is O2MOSP level switched.
$\overline{\text{PA INT}}$	NO PROCESSOR A INTERRUPT COMMON AND GATE - When true, this level indicates that there is no Processor A Interrupt.
PA INT	PROCESSOR A INTERRUPT - When true, this level indicates that a Processor A Interrupt exists. $\overline{\text{PA INT}}$ switched.
PA NON SYL	PROCESSOR A NON-SYLLABLE INTERRUPT - If there is one or more Interrupts in the group PAIO1F thru PAIO4F, then PA NON SYL is ON.
PA TO IAR	PROCESSOR A INTERRUPT TO INTERRUPT ADDRESS REGISTER DRIVER - When true, this level indicates that a Processor A Interrupt has priority to be shifted to the Interrupt Address Register.

PA LOAD — PROCESSOR A LOAD FLIP-FLOP COMMON AND GATE - This level will initiate Processor A (as P1) thru CA AP KD following a successful LOAD cycle.

$\overline{\text{PA 2AB}}$ — PROCESSOR A IS P2 - AVAILABLE - NOT BUSY COMMON AND GATE - When true, this level indicates that Processor A is Processor 2. It is AVAILABLE and is NOT BUSY.

$\overline{\text{PB INT}}$ — NO PROCESSOR B INTERRUPT COMMON AND GATE - When true, this level indicates that there is no Processor B Interrupt.

PB INT — PROCESSOR B INTERRUPT - When true, this level indicates that a Processor B Interrupt exists. PB INT switched.

PB NON SYL — PROCESSOR B NON-SYLLABLE INTERRUPT - If there is one or more Interrupts in the group PAIO1F thru PAIO4F, then PB NON SYL is ON.

PB TO IAR — PROCESSOR B INTERRUPT TO INTERRUPT ADDRESS REGISTER DRIVER - When true, this level indicates that a Processor B Interrupt has priority to be shifted to the Interrupt Address Register.

PB LOAD — PROCESSOR B LOAD FLIP-FLOP COMMON AND GATE - This level will initiate Processor B (as P1) thru CB AP KD following a successful LOAD cycle.

$\overline{\text{PB INT}}$ — NO PROCESSOR B INTERRUPT COMMON AND GATE - When true, this level indicates that there is no Processor B Interrupt.

PB INT — PROCESSOR B INTERRUPT - When true, this level indicates that a Processor B Interrupt exists. $\overline{\text{PB INT}}$ switched.

$\overline{\text{PB 2AB}}$ — PROCESSOR B IS P2 - AVAILABLE - NOT BUSY COMMON AND GATE - When true, this level indicates that Processor B is Processor 2. It is AVAILABLE and is NOT BUSY.

TMO 1, 2, 3 — TIMER SYNC & TIMER FLIP-FLOPS 1-2-3 COMMON AND GATE - This is a gate condition of TMOY • TM1F • TM2F • TM3F used in higher counts of the Real Time Clock.

AAB(n)P — RACK A FRAME AB LOCAL CLOCK OUTPUT (n) (n = 1 thru 6) - These are the LOCAL Clock Drivers on A Rack in Central Control.

AD(n)F — ADMIT I/O DESCRIPTOR FLIP-FLOP (n = 1 thru 4; I1 thru I4) - These are set by AUnS and reset by the I/O Interrupt. They indicate that I/O Unit is BUSY.

APAS — ADMIT MEMORY ACCESS REQUEST - PROCESSOR A SWITCH - This level is used to give Processor A priority when there is a conflict between Processor A and Processor B.

APBS — ADMIT MEMORY ACCESS REQUEST - PROCESSOR B SWITCH - This level is used to give Processor B priority when there is a conflict between Processor A and Processor B.

AR(n)S — ADMIT MEMORY ACCESS REQUEST I/O (n) SWITCH (n = 1 thru 4; I1 thru I4) - This level establishes that an I/O Request has been initiated and there is no conflict. Priority has been granted. Therefore, admit this I/O Request.

ADNS	ADMIT DESCRIPTOR NOW SWITCH - See C(n)ADNS (n = 1 thru 4; I1 thru I4).
BOLD-M	BLOCKING OSCILLATOR & LINE DRIVER - See PAMCLP - PBMCLP or I(n) MCLP.
$\overline{\text{BUSS}}$	PROCESSOR NOT BUSY SWITCH - See PA $\overline{\text{BUSS}}$ or PB $\overline{\text{BUSS}}$.
CA AP KD	ADMIT PROCESSOR DRIVER TO PROCESSOR A - Level from Central Control to initiate Processor A.
CAD(nn)S	MEMORY READ INFORMATION TO PROCESSOR A BIT (nn) SWITCH - Information levels (bits 01 thru 48) from Memory Read Exchange (CC) to Processor A.
CAHP2S	HALT PROCESSOR 2 SWITCH TO PROCESSOR A - This level from Central Control HALTS Processor A when operating as Processor 2.
CAMAED	INVALID ADDRESS TO PROCESSOR A - This is a system Error which indicates that Processor A has designated a Memory Module which is NOT AVAILABLE to the system.
CAMPED	MEMORY PARITY ERROR TO PROCESSOR A DRIVER - This level indicates that the Memory Module has detected a Parity Error during the Memory cycle and an Interrupt will be set.
CAMTOD	MEMORY TIME ZERO DRIVER TO PROCESSOR A - This level is from Central Control to Processor A to indicate that Memory has started a cycle.
CAMT2S	MEMORY TIME TWO SWITCH TO PROCESSOR A - This level from Central Control to Processor A indicates that the Memory Module is through with the Input Unit during the READ cycle, and releases the Input Unit at this time.
CBAPKD	ADMIT PROCESSOR DRIVER TO PROCESSOR B - Level from Central Control to initiate Processor B.
CBD(nn)S	MEMORY READ INFORMATION TO PROCESSOR B - BIT (nn) SWITCH (nn = 01 thru 48) - These are the 48 Information lines from the Memory Read Exchange to Processor B.
CBHP2S	HALT PROCESSOR TWO SWITCH TO PROCESSOR B - This level from Central Control HALTS Processor B when operating as Processor 2.
CBMAED	MEMORY ADDRESS ERROR DRIVER TO PROCESSOR B - This is a system Error which indicates that Processor B has designated a Memory Module which is NOT AVAILABLE to the system.
CBMPED	MEMORY PARITY ERROR DRIVER TO PROCESSOR B - This level indicates that the Memory Module has detected a Parity Error during the Memory cycle and an Interrupt will be set.
CBMTOD	MEMORY TIME ZERO DRIVER TO PROCESSOR B - This level from Central Control to Processor B indicates that a Memory cycle has started.

CBMT2S — MEMORY TIME TWO SWITCH TO PROCESSOR B - This level from Central Control to Processor B indicates that the Memory Module is through with the Input Unit during the READ cycle and releases the Input Unit at this time.

$\overline{\text{CCINTS}}$ — $\overline{\text{CC INTERRUPT SWITCH}}$ (NO CC INTERRUPT) - This level is a common term in the reset logics of all of the External Interrupt Flip-flops.

CCI(nn)F — CC INTERRUPT (nn) FLIP-FLOP (nn = 03 thru 16) - These are the levels from the Central Control Flip-flops.

CCMCLP — MASTER CLOCK PULSE TO CENTRAL CONTROL - This is the Clock Driver line which furnishes the input for the Local Clock Drivers in Central Control E Rack and A Rack.

CL1F — CLOCK CONTROL 1 FLIP-FLOP (SINGLE PULSE) - Primarily used to control the Special Mode output of the Master Clock to the system.

CL2F — CLOCK CONTROL 2 FLIP-FLOP (RUN) - Primarily used to control the normal output of the Master Clock to the system.

CMCBOS — CENTRAL CONTROL CLOCK BLOCKING OSCILLATOR CONTROL SWITCH - When false, this level will inhibit the Clock Drivers to the Memory Units and Central Control.

$\overline{\text{CMIS}}$ — $\overline{\text{COMMENCE I/O SWITCH}}$ (LEVEL FOR INITIATE PROCESSOR) - When CMTF is true (1 μs) this level determines whether an I/O or Processor 2 will be initiated.

CMIS — COMMENCE I/O SWITCH (LEVEL FOR INITIATE I/O) - This level ($\overline{\text{CMIS}}$ switched) is used to set the CIO4 Flip-flop if all available I/O Channels are BUSY.

C(n)A(nn)S — MEMORY(n)ADDRESS (nn) BIT SWITCH (n = 0 thru 7; MEM-0 thru MEM-7) (nn = 00 thru 12) (C0A00S thru C7A12S) - These lines transmit the Address requested from Central Control to the Memory Unit specified.

C(n)WOOD — MEMORY(n) WRITE DRIVER TO MEMORY (n = 0 thru 7; MEM-0 thru MEM-7) - This level signals the Memory Module that the Memory cycle now in progress is a WRITE cycle.

C(n)W(nn)S — MEMORY (n) WRITE INFORMATION (nn) BIT SWITCH (n = 0 thru 7; MEM-0 thru MEM-7)(nn = 01 thru 48) (C0W01S thru C7W48S) - These switches gated by I1 thru I4, PA or PB, carry the Memory WRITE Information (48 bits) from the Central Control Memory WRITE Exchange to the selected Memory Module.

C(n)ADNS — I/O (n) ADMIT DESCRIPTOR NOW SWITCH (n = 1 thru 4; I1 thru I4) - This level is the start signal for the associated I/O Channel.

C(n)A00S — MEMORY (n) START MEMORY SWITCH (n = 1 thru 7; MEM-1 thru MEM-7) - This is a 1 μs start signal to the selected Memory Module from Central Control.

C(n)AUNS	I/O (n) ADMIT UNIT DESCRIPTOR SWITCH (n = 1 thru 4; I1 thru I4) - This level when true, indicates to its associated I/O that no conflict exists for the selected Peripheral Unit.
C(n)LOTS	I/O (n) LOAD TIMING SWITCH (START LOAD) (n = 1 thru 4; I1 thru I4) - In a LOAD operation, this switch level is the START signal for the Associated I/O Channel.
C(n)MAED	I/O (n) MEMORY ADDRESS ERROR DRIVER (n = 1 thru 4; I1 thru I4) - This is a system Error which indicates that the associated I/O Unit has designated a Memory Module which is NOT AVAILABLE to the system.
C(n)MPED	I/O (n) MEMORY PARITY DRIVER (n = 1 thru 4; I1 thru I4) - This level indicates that the Memory Module has detected a Parity Error during the Memory cycle and an Interrupt will be set.
C(n)MTOD	I/O (n) MEMORY TIME ZERO DRIVER (n = 1 thru 4; I1 thru I4) - This is a level from Central Control to the selected I/O Unit (n) to indicate that Memory has started a cycle.
C(n)MT2S	I/O (n) MEMORY TIME TWO SWITCH (n = 1 thru 4; I1 thru I4) - This level from Central Control to the selected I/O Unit (n) indicates that the Memory is through with the Input Unit during a READ cycle and releases the Input Unit at this time.
C(n)R(nn)S	I/O (n) READ INFORMATION (nn) BIT SWITCH (n = 1 thru 4; I1 thru I4) (nn = 01 thru 48) (C0R01S thru C7R48S) - These are the 48 Read Information lines from the Central Control Memory Exchange to the selected I/O Unit (n).
C12S	CONFLICT I/O-01 & I/O-02 SWITCH - The following six levels are the Memory Request Conflict levels. These levels are used to resolve conflicts between I/O Channels for the same Memory Module.
C13S	CONFLICT I/O-01 & I/O-03 SWITCH - See C12S.
C14S	CONFLICT I/O-01 & I/O-04 SWITCH - See C12S.
C23S	CONFLICT I/O-02 & I/O-03 SWITCH - See C12S.
C24S	CONFLICT I/O-02 & I/O-04 SWITCH - See C12S.
C34S	CONFLICT I/O-03 & I/O-04 SWITCH - See C12S.
DRAS	DRUM AVAILABLE SWITCH - See (nn)DRAS.
EAB(n)P	RACK E FRAME AB LOCAL CLOCK OUTPUT (n) (n = 1 thru 6) - Local Clock Driver outputs from Rack E.
HIMD	HALT IMMEDIATE DRIVER - HALT Immediate level resulting from depressing the HALT button ($\overline{\text{HIBL}}$) on the Console.

HIMS
$\overline{\text{HIMS}}$ — HALT IMMEDIATE SWITCH (SWITCH FLIP-FLOP) - This is the $\overline{\text{HIBL}}$ level switched.

HIND — HALT INDICATOR DRIVER - This level energizes the HALT Indicator on the Console.

HP2F — HALT PROCESSOR 2 FLIP-FLOP - This flip-flop is set by the PAHP2L or PBHP2L level sent by Processor to HALT Processor 2.

IASF — INTERRUPT ADDRESS SYNC FLIP-FLOP - This flip-flop controls the 1 μs level (IASS) to reset the Interrupt Address Register.

IASS — INTERRUPT ADDRESS SYNC SWITCH - This level ($\overline{\text{IASF}}$ switched) resets the Interrupt Address Register before the next Address is entered.

IA(n)F — INTERRUPT ADDRESS (n) REGISTER BIT FLIP-FLOP (n = 1 thru 6) - This Register is used by Processor 1 to obtain a Memory location from a branch to the Interrupt handling routine.

$\overline{\text{IEIS}}$ — $\overline{\text{INHIBIT EXTERNAL INTERRUPT SWITCH}}$ - This level is used to Inhibit setting the Interrupt Address Register with an External Interrupt Address if P1 has a higher priority Interrupt (Parity Error or Invalid Address).

IKCBOS — I/O CLOCK BLOCKING OSCILLATOR CONTROL SWITCH - When false, the line will Inhibit the Master Clock pulses to the I/O Control Unit.

IN(n)S — INTERRUPT ADDRESS BIT (n) SWITCH (n = 0 thru 3) - These levels with IO4S, IO8S and I12S levels make up the reset logics of the Interrupt Flip-flops.

IOOS — INTERRUPT ADDRESS EQUAL TO (00 thru 03) SWITCH - This level together with the IN(n)S level make up the reset logics of the Central Control Interrupt Flip-flops.

IO4S — INTERRUPT ADDRESS EQUAL TO 04 thru 07 SWITCH - See IOOS description.

IO8S — INTERRUPT ADDRESS EQUAL TO 08 thru 11 SWITCH - See IOOS description.

I12S — INTERRUPT ADDRESS EQUAL TO 12 thru 15 SWITCH - See IOOS description.

IS(n)Y — INTERRUPT SYNCHRONIZER (n) (n = 3, 6, 8 & 9; 3 = SPO, 6 = INQUIRY, 8 = SPEC. 2, 9 = SPEC 3) - These synchronizer levels will go true with a true level from a Peripheral Unit to set the associated Interrupt Flip-flops.

I(n)AVLS — I/O (n) AVAILABLE SWITCH (n = 1 thru 4; I1 thru I4) - When true, these levels indicate that the associated I/O Channel is ready for system operation.

I (n) BS — I/O (n) BUSY SWITCH (n = 1 thru 4; I1 thru I4) - When true, these levels indicate that the associated I/O Channel is in the process of an Input/Output operation; or, the associated Interrupt Flip-flop is still ON from the completion of an I/O operation.

I(n)CINS	I/O (n) CABLE INTERLOCK SWITCH (n = 1 thru 4; I1 thru I4) - When true, this level indicates that the I/O Channel is physically connected to the system.
$\overline{\text{I(n)DS}}$	$\overline{\text{I/O (n) DESIGNATE DRUM SWITCH}}$ - When true, this level indicates that I/O (n) is NOT controlling a Drum. These levels are used in I/O priority resolution logics which are P(nn)S.
I(n)D16D	I/O (n) D16 DRIVER (n = 1 thru 4; I1 thru I4) - Driver level in Central Control derived from I(n)D16F level from I/O (n).
I(n)I(nn)D	I/O (n) INPUT INFORMATION (nn) DRIVER (n = 1 thru 4; I1 thru I4) (nn = 01 thru 07) - Non-Tape Input Information bits to the IB Register in I/O Channel (n).
I(n)2(n)D	NON-TAPE INPUT CONTROL DRIVERS (n = 1 thru 4; I1 thru I4) (n = 1 thru 8; 21 thru 28; I121D thru I428D) - These are Non-Tape Input levels to the D Register and control the flip-flops in I/O.
I(n)FINL	I/O (n) FINISHED LEVEL (n = 1 thru 4; I1 thru I4) - This level is sent to Central Control when Memory Access is obtained to store the Result Descriptor which indicates that the I/O Channel has completed its operation.
I(n)I1(n)P	I/O (n) TAPE INPUT BIT 1 (n) SWITCH (n = 1 thru 4; I1 thru I4) (n = 1 thru 7; I11 thru I17) I1I11P thru I4I17P - Input Information bits (n) to the IR Input Buffer in the I/O Channel (n).
I(n)I3(n)D	I/O (n) TAPE INPUT BIT 3 (n) DRIVER (n = 1 thru 4; I1 thru I4) (n = I31, I32, I34, I35, I36, I37 & I38) I1I31D thru I4I38D - Tape Input Control lines to I/O Register and Control Flip-flops in I/O Channel (n).
I(n)MCLP	I/O (n) MASTER CLOCK PULSE (n = 1 thru 4; I1 thru I4) - These lines come from Central Control and drive the LOCAL Clock Drivers in the I/O Control Unit.
$\overline{\text{I(n)TS}}$	$\overline{\text{I/O (n) DESIGNATE SWITCH}}$ (n = 1 thru 4; I1 thru I4) - When true, this level indicates that I/O (n) is NOT controlling a Magnetic Tape Unit. These levels are used in I/O priority resolution logics. P(nn)S switches.
I(n)U(nn)D	I/O (n) UNIT DESIGNATE (nn) DRIVER (n = 1 thru 4; I1 thru I4) (nn = 01 thru 31, 42, 50 & 52) I1U01D thru I4U52D.
LOAS	LOAD SWITCH - This is $\overline{\text{LOBL}}$ level switched. It will WRITE a LOAD operation.
LOAY	LOAD DELAY MULTI - This Multivibrator, energized by LOAS, drives the $\overline{\text{LOYS}}$ switch to START the system Clock in a LOAD Operation.

LOFF — LOAD FLIP-FLOP - This flip-flop is SET at the beginning of the LOAD cycle.

$\overline{\text{LORS}}$ — $\overline{\text{LOAD RELAY SWITCH}}$ (Operates MASTER CLEAR) - This switch driven by LOAS will operate the MASTER CLEAR Relay.

$\overline{\text{LOYS}}$ — $\overline{\text{LOAD DELAY SWITCH}}$ - This level, the switched output, and LOAY start the System Clock during a LOAD operation.

MCMCLP-A3, B3, C3 — MASTER CLOCK PULSE TO MEMORY UNITS - These lines come from Central Control to drive the LOCAL Clock Drivers in the Memory Units.

$\overline{\text{MKSCLL}}$ — $\overline{\text{START CLOCK LEVEL FROM MEMORY UNITS}}$ - This level comes from the START Clock button on each Memory Module. It STARTS the system Clock.

MPID — MEMORY PARITY ERROR INDICATOR DRIVER - This driver will light the Memory Parity Error Indicator on the Console to show that there was a Parity Error to Processor A or Processor B.

$\overline{\text{MNRS}}$, MNRS — $\overline{\text{MEMORY NOT READY SWITCH}}$ - These levels check that the connected (nnClNL) Memory Modules are ready for REMOTE operation. MNRS true will drive SNRD to light the system NOT READY Indicator.

M(n)CINS — MEMORY (n) CABLE INTERLOCK SWITCH (n = 0 thru 7; MEM-0 thru MEM-7) - When grounded in their respective Memory Module, these lines indicate to Central Control that the Memory Module is connected to the system.

$\overline{\text{M(n)IORS}}$ — $\overline{\text{MEMORY (n) I/O REQUEST SWITCH}}$ - When true, this level indicates that there is NO I/O request for this Memory Module.

M(n)I(n)XF — MEMORY (n) I/O (n) CROSSPOINT FLIP-FLOP (n = 0 thru 7; MEM-0 thru MEM-7) (n = 1 thru 4; I1 thru I4) - When true, these levels indicate that Memory Module (n) is connected to I/O (n).

M(n)I(n)XD-1 — MEMORY (n) & I/O (n) CROSSPOINT DRIVER 1 (MWX) (n = 0 thru 7; MEM-0 thru MEM-7) (n = 1 thru 4; I1 thru I4) M0I1XD-1 thru M7I4XD-1 - Driver with input of M(n)I(n)XF for control in the Memory WRITE Exchange.

M(n)I(n)XD-2 — MEMORY (n) & I/O (n) CROSSPOINT DRIVER 2 (MWX) (n = 0 thru 7; M0 thru M7) (n = 1 thru 4; I1 thru I4) M0I1XD-2 thru M7I4XD-2 - Second output of M(n)I(n)XD-1 Driver.

M(n)I(n)XD-3 — MEMORY (n) & I/O (n) CROSSPOINT DRIVER 3 (MRX) (n = 0 thru 7; M0 thru M7) (n = 1 thru 4; I1 thru I4) M0I1XD-3 thru M7I4XD-3 - Driver with input of M(n)I(n)XF for control in the Memory Read Exchange.

M(n)I(n)XD-4 — MEMORY (n) & I/O (n) CROSSPOINT DRIVER 4 (MRX) (n = 0 thru 7; M0 thru M7) (n = 1 thru 4; I1 thru I4) M0I1XD-4 thru M7I4XD-4 - Second output of M(n)I(n)XD3 driver.

M(n)I(n)XS — MEMORY (n) & I/O (n) CROSSPOINT SWITCH (MWX) (n = 0 thru 7; M0 thru M7) (n = 1 thru 4; I1 thru I4) M0I1XS thru M7I4XS - Switched level of M(n)IXF for use in the Memory WRITE Exchange.

M(n)MCYF — MEMORY (n) MEMORY CYCLE FLIP-FLOP (n = 0 thru 7; M0 thru M7) M0MCYF thru M7MCYF - When true, this level indicates that the Memory Module (n) is connected to a Processor or an I/O Channel and is in a Memory cycle.

M(n)MT4S — MEMORY (n) MEMORY CYCLE T4 SWITCH (n = 0 thru 7; M0 thru M7) M0MT4S thru M7MT4S - When true, this level received from Memory will clear the Crosspoint flip-flops associated with Memory Module (n).

M(n)PAXF — MEMORY (n) & PROCESSOR A CROSSPOINT FLIP-FLOP (n = 0 thru 7; M0 thru M7) M0PAXF thru M7PAXF - When true, this level indicates that Memory Module (n) is connected to Processor A.

M(n)PAXD-1 — MEMORY (n) & PROCESSOR A CROSSPOINT DRIVER 1 (n = 0 thru 7; M0 thru M7) - This is a level derived from M(n)PAXD-1.

M(n)PAXD-2 — MEMORY (n) & PROCESSOR A CROSSPOINT DRIVER 2 - This is a parallel driver to M(n)PAXD-1.

M(n)PAXD-3 — MEMORY (n) & PROCESSOR A CROSSPOINT DRIVER 3 - This is a level derived from M(n)PAXF for use in the Memory READ Exchange.

M(n)PAXD-4 — MEMORY (n) & PROCESSOR A CROSSPOINT DRIVER 4 - This is a parallel driver to M(n)PAXD-3.

M(n)PAXS — MEMORY (n) & PROCESSOR A CROSSPOINT SWITCH - This is the M(n)PAXF level switched for use in the Memory WRITE Exchange.

M(n)PBXD-1 — MEMORY (n) & PROCESSOR B CROSSPOINT DRIVER 1 (n = 0 thru 7; M0 thru M7) - This is a level derived from M(n)PBXF for use in the Memory WRITE Exchange.

M(n)PBXD-2 — MEMORY (n) & PROCESSOR B CROSSPOINT DRIVER 2 - This is a parallel driver to M(n)PBXD-1.

M(n)PBXD-3 — MEMORY (n) & PROCESSOR B CROSSPOINT DRIVER 3 - This is a level derived from M(n)PBXF for use in the Memory READ Exchange.

M(n)PBXD-4 — MEMORY (n) & PROCESSOR B CROSSPOINT DRIVER 4 - This is a parallel driver to M(n)PBXD-3.

M(n)PBXF — MEMORY (n) & PROCESSOR B FLIP-FLOP (n = 0 thru 7; M0 thru M7) - When true, this level indicates that the Memory Module (n) is connected to Processor B.

M(n)PBXS — MEMORY (n) & PROCESSOR B CROSSPOINT SWITCH - This is the M(n)PBXF level switched for use in the Memory WRITE Exchange.

M(n)XFOS — MEMORY (n) CROSSPOINT FLIP-FLOPS EQUAL TO 0 SWITCH (n = 0 thru 7; M0 thru M7) - This level will be false when any Crosspoint flip-flop is SET. It will inhibit setting any other Crosspoint flip-flop during the Memory cycle in progress.

PAAVLS — PROCESSOR A AVAILABLE SWITCH - This is level $\overline{\text{PAAVLL}}$ (Processor A Available) from Processor A switched. When true, PAAVLS indicates that Processor A is available for operation.

$\overline{\text{PABUSS}}$ — $\overline{\text{PROCESSOR A BUSY SWITCH}}$ - This is level PABUSL (Processor A BUSY) from Processor A switched.

PACBOS — PROCESSOR A CLOCK BO CONTROL SWITCH - This is the Inhibit level controlled by PAIMCL from Processor A which may STOP the Clock Drivers to Processor A.

$\overline{\text{PACOSS}}$ — $\overline{\text{PROCESSOR A CONTROL STATE SWITCH}}$ - This is PACOSL level switched. When this level is true, its drivers PANOSD light the NORMAL state indicator on the Console.

PACOSD — PROCESSOR A CONTROL STATE INCANDESCENT DRIVER - This indicator level lights the CONTROL state indicator for Processor B on the Console.

PAMCLP-A3, B3, C3 — MASTER CLOCK PULSE TO PROCESSOR A - These lines are the output of the Clock Drivers in Central Control which go to Processor A to drive the LOCAL Clock Drivers.

PANOSD — PROCESSOR A NORMAL STATE INCANDESCENT DRIVER - This indicator level lights the NORMAL state indicator for Processor A on the Console.

PBAVLS — PROCESSOR B AVAILABLE SWITCH - This is the switched $\overline{\text{PBAVLL}}$ level from Processor B and when true indicates that Processor B is available for operation.

$\overline{\text{PBBUSS}}$ — $\overline{\text{PROCESSOR B BUSY SWITCH}}$ - This is level PBBUSL switched from Processor B.

PBCBOS — PROCESSOR B CLOCK BO CONTROL SWITCH - This is the inhibit level, controlled by PBIMCL from Processor B which may STOP the Clock Drivers to Processor B.

$\overline{\text{PBCOSS}}$ — $\overline{\text{PROCESSOR B CONTROL STATE SWITCH}}$ - This is the PACOSL level switched. When this level is true, it drives PANSOD to light the NORMAL state Indicator on the Console.

PBMCLP-A3, B3, C3, D3 — MASTER CLOCK PULSE TO PROCESSOR B - These lines are the output A of the Clock Drivers in Central Control which go to the Processor B to drive the LOCAL Clock Drivers.

PBNOSD — PROCESSOR B NORMAL STATE INCANDESCENT DRIVER - This indicator level lights the NORMAL state indicator for Processor B on the Console.

PGDL — POWER GOING DOWN LEVEL - This is the switched level of $\overline{\text{PGDL}}$ which functions as a STOP Clock level (CLEAR CL2FF) whenever the DC LOCKOUT line is grounded in D & D.

$\overline{\text{POAL}}$	$\overline{\text{PAPER TAPE PUNCH OUTPUT "A" LEVEL NOT}}$
$\overline{\text{PRWL}}$	$\overline{\text{PAPER TAPE REWIND LEVEL NOT}}$
$\overline{\text{POBL}}$	$\overline{\text{PAPER TAPE PUNCH OUTPUT "B" LEVEL NOT}}$
$\overline{\text{SCCL}}$	$\overline{\text{START CARD CYCLE LEVEL NOT}}$
$\overline{\text{PO8L}}$	$\overline{\text{PAPER TAPE PUNCH OUTPUT "8" LEVEL NOT}}$
$\overline{\text{PSTL}}$	$\overline{\text{PAPER TAPE STOP LEVEL NOT}}$
PUCP	PUNCH CLOCK PULSE
$\overline{\text{CB1L}}$	$\overline{\text{CARD BINARY LEVEL NOT}}$
P(nn)S $\overline{\text{P(nn)S}}$	PRIORITY I/O (n) OVER I/O (n) SWITCH (nn = 14, 21, 31, 32, 42 & 43) - These switch levels are used in the Admit I/O Memory Request Priority resolving logics.
P2BF	PROCESSOR 2 BUSY FLIP-FLOP - When true, this level indicates that Processor 2 has received an Initiate level.
P2BS	PROCESSOR 2 BUSY SWITCH - When true, this level indicates that P2BF is ON and that Processor 2 is NOT AVAILABLE and BUSY.
SCLL	START CLOCK LEVEL - When a Unit START Clock button is depressed, this level is at a ground potential.
SCLS	START CLOCK SWITCH - This level is true when a START Clock button on a system unit is depressed.
SCLY	START CLOCK SYNCHRONIZER - This synchronizer emits a 1 μs level from the inputs of SCMM and $\overline{\text{MOSP}}$ to set CL1F.
SCMM	START CLOCK MULTIVIBRATOR - This multivibrator enabled by SCLS is ANDed with $\overline{\text{MOSP}}$ to energize the synchronizer SCLY.
SI1S	SPECIAL INTERRUPT 1 SWITCH - This switch is not used at this time.
SI2S	SPECIAL INTERRUPT 2 SWITCH - This switch is not used at this time.
SI3S	SPECIAL INTERRUPT 3 SWITCH - This switch is not used at this time.
SNRD	SYSTEM NOT READY INCANDESCENT DRIVER - This driver energizes the system NOT READY indicator on the Console when a Unit connected to the system is NOT READY for system operation.
S(nn)S	SET INTERRUPT ADDRESS BIT (nn) SWITCH (nn = 01 thru 04; 19 thru 31) - These switch levels provide logical gating to determine external interrupt priority in order to set an Address into the Interrupt Address Register.

TMOY	TIMER SYNCHRONIZER - This synchronizer output provides a level at a 60 cycle rate to gate the counting pulses to the Real Time Clock.
TM(n)F	TIMER BIT (n) FLIP-FLOP (n = 1 thru 6) - These levels come from the Real Time Clock flip-flops.
$\overline{\text{U(n)BS}}$	$\overline{\text{UNIT DESIGNATE I/O (n) BI-DIRECTIONAL SWITCH}}$ (n = 2, 3 & 4)
U(nn)S	UNIT DESIGNATE CONFLICT I/O (n) & I/O (n) SWITCH (nn = 12, 13, 14, 23, 24 & 34)
$\overline{\text{(nn)BDL}}$	$\overline{\text{UNIT (nn) TAPE BACKWARD DRIVE LEVEL}}$ (nn = 01, 03, 05 thru 31) $\overline{\text{01BDL}}$ thru $\overline{\text{31BDL}}$
$\overline{\text{(nn)FDL}}$	$\overline{\text{UNIT (nn) TAPE FORWARD DRIVE LEVEL}}$ $\overline{\text{01FDL}}$ thru $\overline{\text{31FDL}}$
$\overline{\text{(nn)TCP}}$	$\overline{\text{UNIT (nn) TAPE CLOCK PULSE}}$ $\overline{\text{01TCP}}$ thru $\overline{\text{31TCP}}$
(nn)TEFS	UNIT (nn) TAPE END OF FILE SWITCH 01TEFS thru 31TEFS
(nn)THDS	UNIT (nn) TAPE HIGH DENSITY LEVEL SWITCH 01THDS thru 31THDS
(nn)TLPS	UNIT (nn) TAPE LOAD POINT LEVEL 01TLPS thru 31TLPS
(nn)TRES	UNIT (nn) TAPE READ READY SWITCH 01TRES thru 31TRES
$\overline{\text{(nn)TRL}}$	$\overline{\text{UNIT (nn) TAPE READ LEVEL}}$ $\overline{\text{01TRL}}$ thru $\overline{\text{31TRL}}$
$\overline{\text{(nn)TRWL}}$	$\overline{\text{UNIT (nn) TAPE REWIND LEVEL}}$ $\overline{\text{01TRWL}}$ thru $\overline{\text{31TRWL}}$
(nn)TTOS	UNIT (nn) TAPE TRANSPORT OPERATE LEVEL 01TTOS thru 31TTOS
(nn)TWI(n)	UNIT (nn) TAPE WRITE INFORMATION BIT (n) (nn = 01, 03, 05 thru 31) (n = 1, 2, 4, 8, A, B, P)
$\overline{\text{(nn)TWL}}$	$\overline{\text{UNIT (nn) TAPE WRITE LEVEL}}$
(nn)TWRS	UNIT (nn) TAPE WRITE READY LEVEL
$\overline{\text{(nn)TWRP}}$	$\overline{\text{UNIT (nn) TAPE WRITE RESET PULSE}}$
(nn)TWSS	UNIT (nn) TAPE WRITE STATUS SWITCH
$\overline{\text{(nn)DBSL}}$	$\overline{\text{UNIT (nn) DRUM BUFFER SET LEVEL}}$ (nn = 04, 08)
(nn)DCL(n)	UNIT (nn) DRUM CONTROL LEVEL (n) (nn = 04, 08) (n = 1 thru 4)
(nn)DRAS	UNIT (nn) DRUM AVAILABLE SWITCH
(nn)DURS	UNIT (nn) DRUM READY LEVEL SWITCH
(nn)DWCS	UNIT (nn) DRUM WORD COINCIDENCE SWITCH
(nn)DWI(n)	UNIT (nn) DRUM INFORMATION LEVELS (nn = -4, 08) (n = 1, 2, 4, 8, A, B)

(nn)DWLS	UNIT (nn) DRUM WRITE LOCKOUT SWITCH (nn = 04, 08)
(nn)DWRL	UNIT (nn) DRUM WRITE LEVEL
(nn)CBHL	UNIT (nn) CARD READER BINARY HALF LEVEL (nn = 10, 14)
(nn)CBIL	UNIT (nn) CARD READER BINARY LEVEL (nn = 10, 14)
(nn)CCS	UNIT (nn) CARD CYCLE LEVEL (nn = 10, 14, 18, 20)
(nn)CRES	UNIT (nn) CARD READ ERROR SWITCH (nn = 10, 14) - Also Paper Tape Parity Error.
(nn)SCCL	UNIT (nn) START CARD CYCLE LEVEL (nn = 10, 14, 18)
(nn)EOPS	(nn) PRINTER - END OF PAGE SWITCH (nn = 22, 26)
(nn)EPRL	(nn) PRINTER - END OF PAGE RESET LEVEL
(nn)PAMS	(nn) PRINTER - PAPER MOTION SWITCH
(nn)PCFS	(nn) PRINTER - PRINT CYCLE FINISHED SWITCH
(nn)PCYS	(nn) PRINTER - PRINT CYCLE SWITCH
(nn)PITL	(nn) PRINTER - INFORMATION TRANSFER LEVEL
(nn)PLCL	(nn) PRINTER - LISTER COMMAND LEVEL
(nn)PRRS	(nn) PRINTER - PRINTER READY SWITCH
(nn)PI(n)L	(nn) PRINTER - INFORMATION (n) LEVEL (nn = 22, 26) (n = P, B, A, 8, 4, 2, 1)
(nn)PINS	(nn) PUNCH - INFORMATION NEEDED SWITCH (nn = 42, 50, 52)
(nn)PBCL	(nn) PUNCH - BIT COMPARE LEVEL
(nn)PUCS	(nn) PUNCH - CYCLE SWITCH
(nn)PUCP	(nn) PUNCH - CLOCK PULSE
(nn)PURS	(nn) PUNCH - READY SWITCH
(nn)SPOL	(nn) PUNCH - START PUNCH ORDER LEVEL
(nn)PO(n)L	(nn) PUNCH - OUTPUT INFORMATION (n) BIT LEVEL (nn = 50, 52) (n = B, A, 8, 4, 2)
16ILRL	INQUIRY LATCH RELEASE LEVEL
16IRTS	INQUIRY READ TIMING SWITCH

16ISYL	INQUIRY SYNC LEVEL
160I(n)L	OUTPUT INFORMATION LEVEL (TO INQUIRY UNIT) (n = P, B, A, 8, 4, 2, 1)
16RIWL	READ INQUIRY LEVEL
16SIIS	SET INQUIRY INTERRUPT SWITCH
16WIRL	WRITE INQUIRY LEVEL
18PRWL	PAPER TAPE REWIND LEVEL
18PSTL	PAPER TAPE STOP LEVEL
30ICRS	SPO - INPUT CHARACTER READY SWITCH
30IN(n)L	SPO - INFORMATION (n) LEVEL (n = B, A, 8, 4, 2, 1)
30ØCRS	SPO - OUTPUT CHARACTER READY SWITCH
30ØDRL	SPO - OUTPUT DRIVER LEVEL
30TINS	SPO - TYPEWRITER INTERRUPT SWITCH
30TOPL	SPO - TYPEWRITER OPERATION LEVEL
30TDRS	SPO - TYPEWRITER READY SWITCH
42PASL	PUNCH - AUXILIARY STACKER LEVEL
$\overline{60\ CS}$	$\overline{60\ CYCLE\ SWITCH}$ - This switch is activated by the 60 cycle AC.
60 CM	60 CYCLE MULTIVIBRATOR - This multivibrator, triggered by 60 CS is SET for 12 ms in order to provide a stable timing trigger for the Real Clock Synchronizer TMOY.
01MOSP	MASTER OSCILLATOR OUTPUT 1 - This is the No. 1 Output of the Master Oscillator which is running whenever DC is applied.
02MOSP	MASTER OSCILLATOR OUTPUT 2 - Second continuous output of the Master Oscillator.