FIELD ENGINEERING TECHNICAL MANUAL

Burroughs

B 471

DISK FILE ELECTRONICS UNIT

B

INDEX - SECTION I

1 INTRODUCTION

1.1   GENERAL DESCRIPTION

Figure 1.1-1 shows the Disk File Electronics Unit (E.U.) with one
Disk File Storage Unit (S.U.). One E.U. can control from one to five
S.U.'s, while up to ten E.U.'s may be connected to one Disk File Con-
trol Unit (D.F.C.U.). A maximum Disk File Subsystem will consist of
one D.F.C.U., 10 E.U.'s, and 50 S.U.'s. Only one Disk File Subsystem
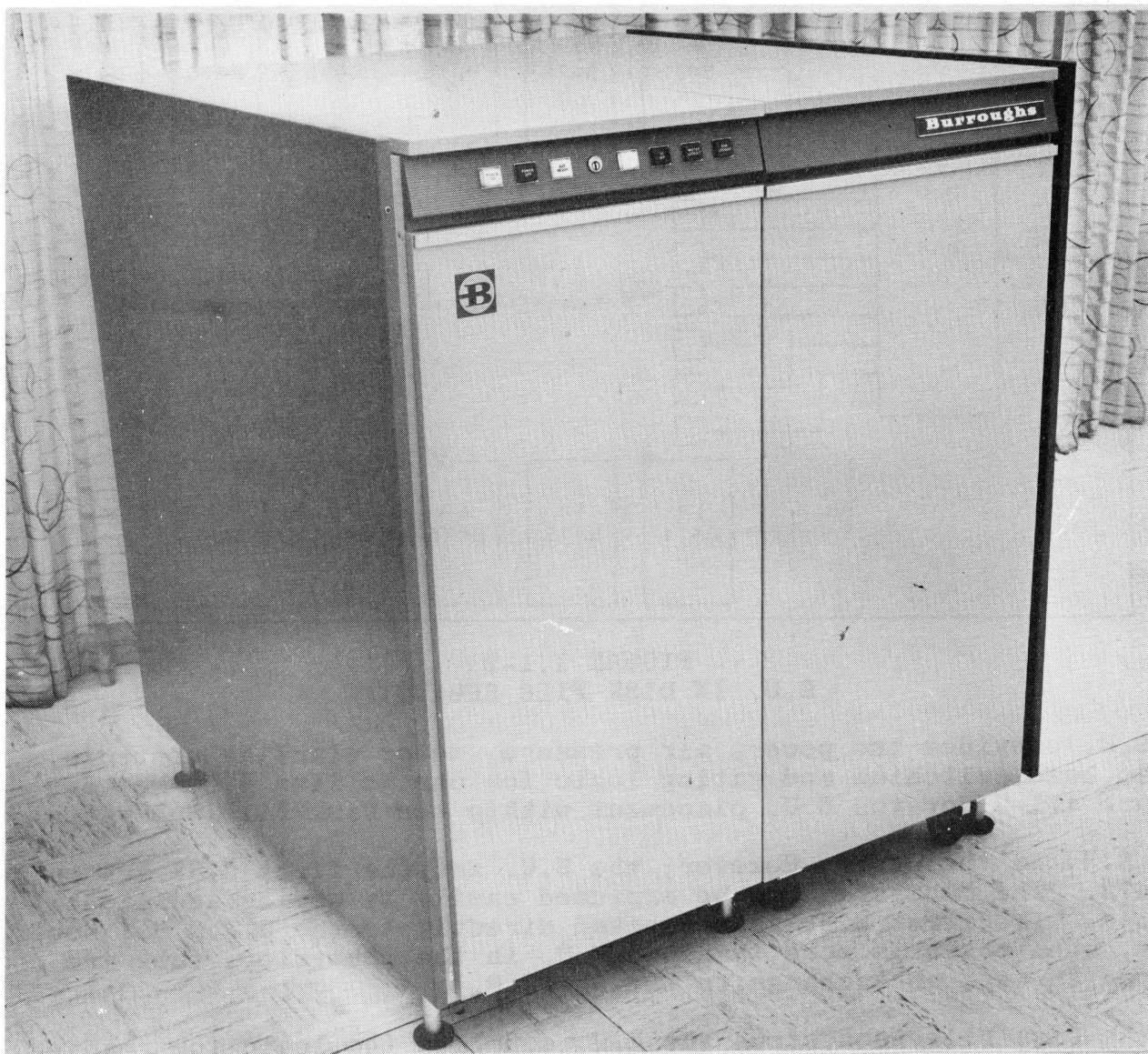can be controlled by the B200; the B5500 can control two Subsystems.

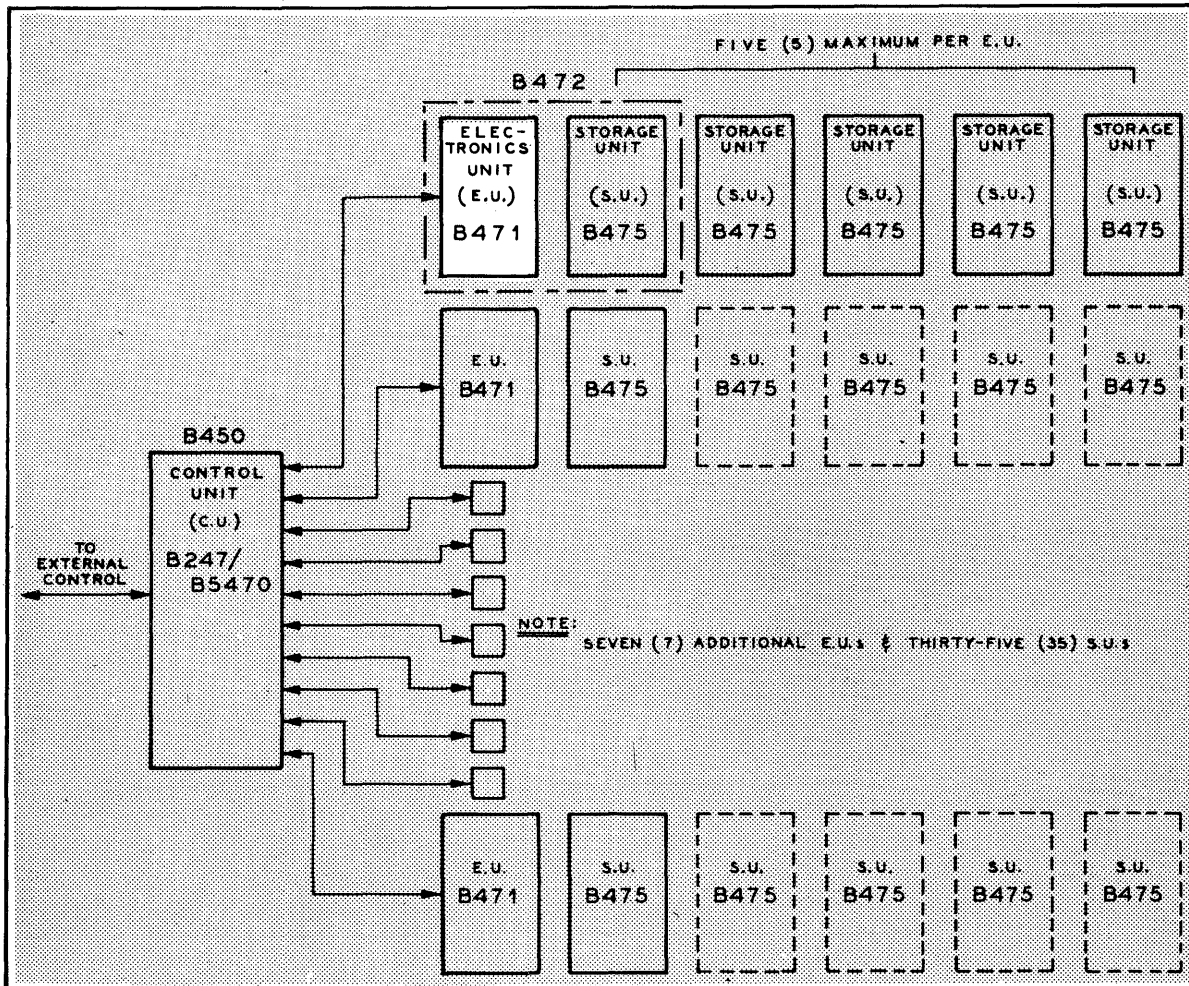FIGURE 1.1-1
E.U. IN DISK FILE SUBSYSTEM

FIGURE 1.1-2
E.U. IN DISK FILE SUBSYSTEM

An E.U. provides the power, air pressure, motor starting controls, basic head switching and gating logic for one to five S.U.'s. See Figure 1.1-2 for the E.U. placement within the Disk File Subsystem.

The E.U. is the B471. However, the E.U. and the first S.U. are called a B472. The Subsystem can be expanded easily by adding additional S.U.'s. The first E.U. is connected directly to the D.F.C.U.; however, when there is more than one E.U. in the Subsystem, they are connected through an Exchange to the D.F.C.U.

In the Disk File Subsystem, the E.U. supplies the logic for reading and writing. Before an operation may take place, a segment (record) must be located on the disk. Each segment has an address which is read and compared with the desired address. When the correct segment address is found, the operation proceeds.

A write operation transfers characters from the Processor to the D.F.C.U., to the E.U., and finally to a disk in the S.U. The E.U. accepts a six-bit character from the D.F.C.U. parallel by bit, then

passes the character to the Module serially by bit since data is written serially on the disk.

In a read operation, the serial by bit information read from the disk is accumulated into a character in the E.U. and then sent to the D.F.C.U. and on to the Processor.

1.2   EQUIPMENT SPECIFICATIONS

Height ..... 53 inches
Width ..... 23 inches
Length ..... 45 inches
Weight ..... 450 pounds

POWER REQUIREMENTS

208VAC or 230VAC from two phases and neutral. Maximum current, 63 amps for five S.U.'s.

Maximum cable length to D.F.C.U. - 50 feet.

1.3 PHYSICAL DESCRIPTION

The Electronics Unit supplies the power and power controls for the Storage Units as well as providing the read/write logic. All operator controls are located on the front of the E.U. Figure 1.3-1 shows the left side of the E.U. The logic gate contains control logic for the E.U. and S.U.'s. The Maintenance Panel to the right allows the engineer quick access to information on the status of the E.U. and associated S.U.'s.
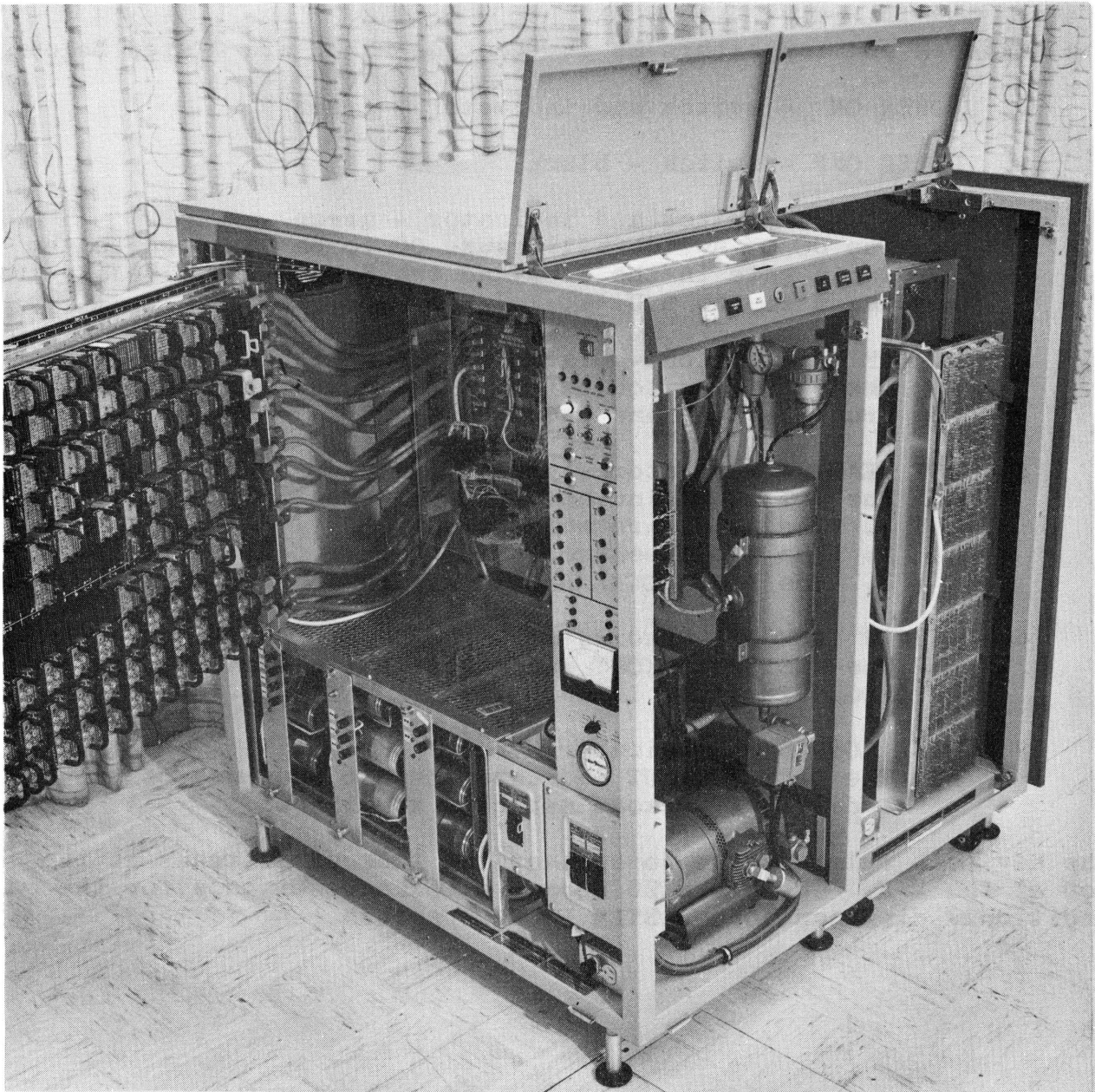

FIGURE 1.3-1
COMPONENT LAYOUT - E.U.

The Control Panel on the E.U. (Figure 1.3-2) provides the operator controls for the E.U. and its Modules.

```
┌─────────────────────────────────────────────────────────────────────────┐
│  ┌───────┐ ┌───────┐ ┌───────┐       ┌───────┐ ┌───────┐ ┌───────┐ ┌───────┐ │
│  │ POWER │ │ POWER │ │  DC   │  (P)  │  DC   │ │ NOT   │ │MASTER │ │ DISK  │ │
│  │  ON   │ │  OFF  │ │  ON   │       │  OFF  │ │READY  │ │LOCKOUT│ │LOCKOUT│ │
│  └───────┘ └───────┘ └───────┘       └───────┘ └───────┘ └───────┘ └───────┘ │
└─────────────────────────────────────────────────────────────────────────┘
```
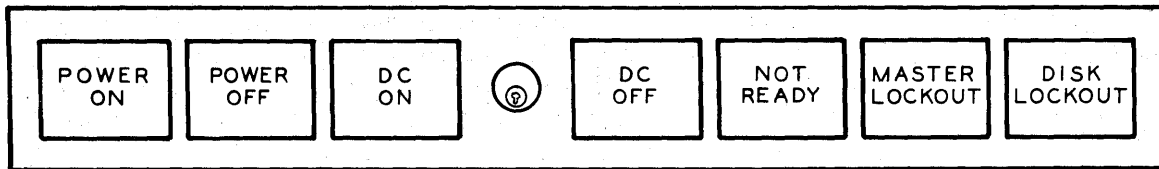
FIGURE 1.3-2
E.U. CONTROL PANEL

The switches and indicators on the Control Panel are listed below:

    1.   POWER ON - switch and indicator - green

    2.   POWER OFF - switch - black

    3.   DC ON   - switch and indicator - green
        a. The DC ON switch will cause DC to be supplied to the logic gate in the E.U. and the S.U.'s and also fly the heads in the S.U.'s.

    4.   DC OFF   - switch - black
        a. The DC OFF switch retracts the heads and removes DC from the E.U. and the S.U.'s.

    5.   NOT READY - indicator - white
        a. The NOT READY indicator is lit when:
           1. The heads are not flying.
           2. The air pressure is not normal.
           3. The E.U. LOCAL/REMOTE switch is in LOCAL.

    6.   MASTER LOCKOUT - indicator - red
        a. The MASTER LOCKOUT indicator is lit when the MASTER LOCKOUT switch is thrown.

    7.   DISK LOCKOUT - indicator - red
        a. The DISK LOCKOUT indicator is lit when any of the individual Lockout switches are thrown.

The Key Lock releases the cover over the Lockout switches at the top of the E.U. There are 20 separate Lockout switches for the individual disks and one MASTER LOCKOUT switch.

The Maintenance Panel (Figure 1.3-3) has the following:

1. A POWER ON meter.

2. Five NOT READY indicators for the S.U.'s.

3. The AC ON and DC ON indicators which parallel POWER ON and DC ON on the Control Panel.

4. RELAY SUPPLY ON indicator.

5. The LOCAL/REMOTE switch.

6. DC LOCKOUT switch.

7. A CLOCK switch which must be on for normal operation. It is off for single pulsing with the BITP and WØMP buttons.

8. Indicators for flip-flops in the E.U.

9. Test points.

10. A voltmeter for monitoring the power supplies.

11. An AIR PRESSURE meter.
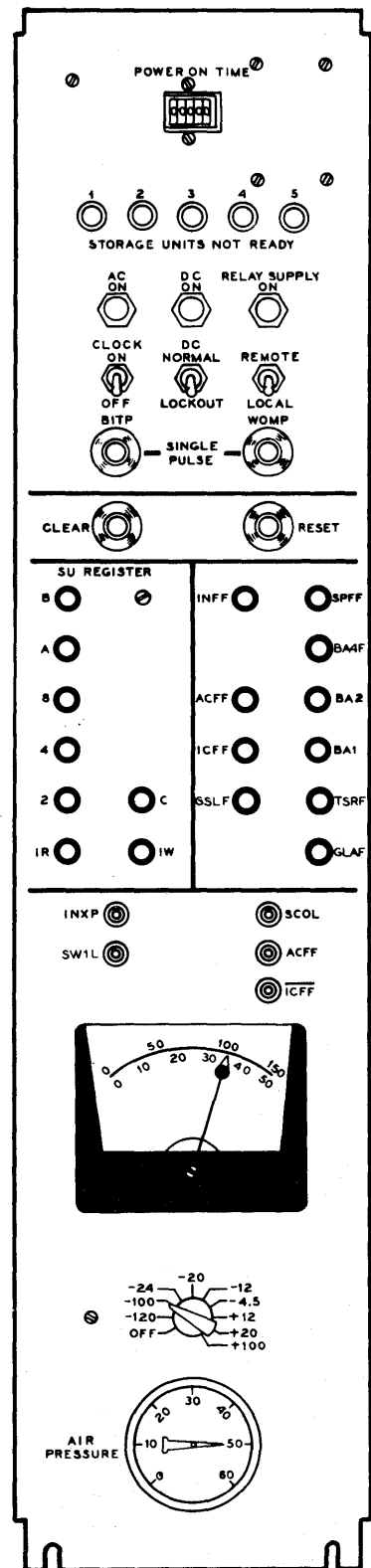
FIGURE 1.3-3
MAINTENANCE PANEL

Figure 1.3-4 shows a B471 and one B475 viewed from the front with the skins removed to show the physical location of many of the components.

Note the Winchester type connector mounted just above and behind the compressor. This is the connector for the logic cable from the associated D.F.C.U.
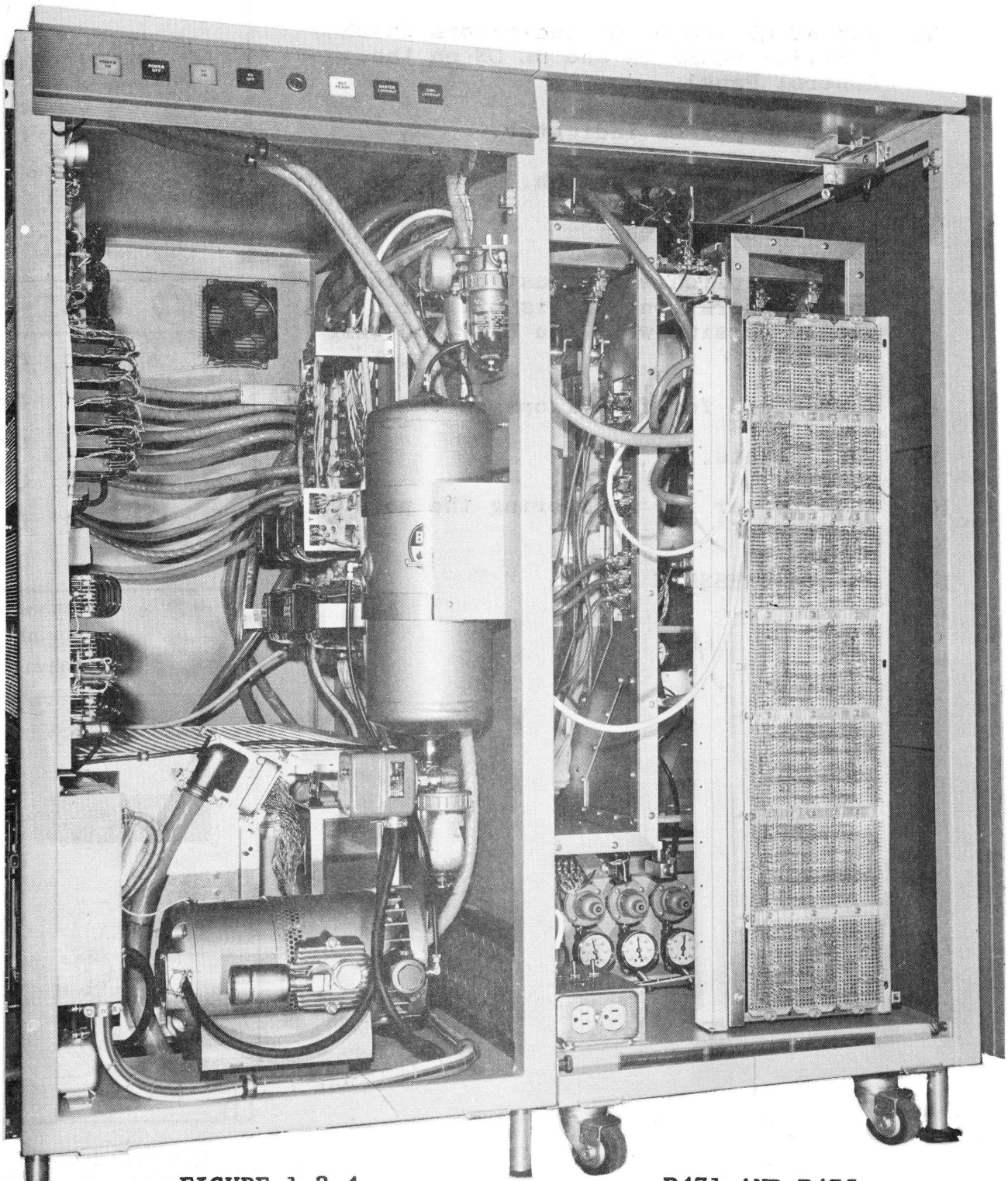

FIGURE 1.3-4   **B471 AND B475**

1.4 GLOSSARY

ACFF	Action FF is on during a disk file access except during a second revolution cross-over.
ASRL ASRL/	Address Read Levels from the Storage Module.
ASRS ASRS/	Cross-coupled switches set by the Address Read Levels at BITP time. The outputs of the switches are set into SUBF when ICFF is off.
BA1F BA2F BA4F	Address Count FFs. Normally only count to three. BA4F indicates a Maintenance Segment address.
BCLP	Output of the Bit Clock Multi. Pulse width 150 nanoseconds. Input is BITP or DBIT.
BITL-01 BITL-02 BITL-03 BITL-04 BITL-05	Bit pulse levels from the five possible modules.
BITP	Delayed output of the Bit Pulse Multi. Pulse width 150 nanoseconds. Input is BITL-nn. Produces a BCLP delayed 250 nanoseconds after input.
BSPL	Bit Single Pulse Level. Effectively, this is the output of the Bit Single Pulse switch to BITM.
BUDP	Undelayed output of Bit Pulse Multi. Pulse width is 250 nanoseconds. Input is BITL-nn.
CBAS	Count Address Count Switch. Negative output causes a count-up of BAnFs.
CCEL-C	Continuous Clock Enable Level. Makes CCIL-A negative when Clock Switch is ON.
CCIL-A	Continuous Clock Inhibit Level. Ground when Clock Switch is OFF.
CSIL-A	Clock Single Inhibit Level. Ground when Clock Switch is ON. (This should be SCIL. See SCEL.)
CSUS	Clears SU1FR, SU2F, SU4F and SU8F.

CS1L/ CS2L/	Characters per Segment Levels. Both ground for 96 characters per segment. 1 negative and 2 ground for 240 characters per segment. 1 ground and 2 negative for 480 characters per segment.
DBIT	Delayed Bit Pulse from an adjustable multi. Output is a negative pulse 675 nanoseconds after BUDP. Used to fire BCLP while reading an active word.
DFSL/	Disk Face Select Level. Negative to select a clock head on the lower face of a disk--tracks 00=>49. Must be opposite of DFSS.
DFSS	Disk Face Select Switch. Negative to select a clock head on the upper face of a disk--tracks 50=>99. Must be opposite of DFSL/.
DISC-01/ DISC-02/ DISC-03/ DISC-04/	Disk Select Levels. Ground to select disk "n" in each Storage Module. Only one line ground at one time. Derived from the decoded outputs of the Disk Switches.
DIXP	Delayed Index Pulse from DIXM. DIXM is 600 microseconds and is set during second revolution cross-over. In case the cross-over results in a Not Ready condition (non-existent disk), DIXP resets INFF and produces one more SCLP.
D01L/ D02L/ D04L/ D08L/ D16L/	Disk Switch Levels inverted from Disk File Control address levels.
ECCS	Enable Character Clock Switch. If a BITP was missed, ECCS ensures that SCLP cannot occur out of sync due to the set of SUCF by the BITP that occurs at WØMP.
FWLS-OR1 FWLS-OR2 FWLS-OR3	File Write Lockout decoding.
GLAF	Gain Latch FF latches the Gain Select circuit.
GSLF	Gain Select FF is set to the state of TSRF at each Word Mark (SPFF).
GSSL	Gain Select Switch Level is negative to select low gain in the Module read amplifiers.

HFML-01/ HFML-02/ HFML-03/ HFML-04/ HFML-05/	Storage Module Ready Levels are positive when: a. Unit is Ready (disks up to speed, no touch circuits triggered, air pressure up, heat exchange blowers on). b. Unit is in LOCAL and not designated.
HSDL-00 thru HSDL-99	Head Select Drive Level is positive to select track "nn". Only one line can be positive at a time.
HSTL-00/ HSTL-10/ HSTL-20/ thru HSTL-90/	Head Select Tens Levels.
HSUL-00/ thru HSUL-09/	Head Select Units Levels.
ICFF	Interlace Control FF is set during the active word and is reset during the inactive word or "idle" condition.
INFF	Index FF is set during first and second revolution cross-overs. Its purpose is to "blank out" the maintenance segments and to index the continuation of the operation on the correct word.
INHS	Index Holdover Switch. The output level is a gate to the holdover of IXHM and is used to produce the pseudo INXP in a second rveolution cross-over.
INXP	Index Pulse. The output of the Index Holdover Multi when it times out. IXHM = BCLP·INHS.
IRAL IRAL/	Information Read Levels from the Storage Module.
IRAS IRAS/	Cross-coupled switches set by the Information Read Levels by BCLPs (DBIT). The switch outputs are set into SUBF when ICFF is on.
LØSW-01/ thru LØSW-20/	Write Lockout Switches 1 through 20 for each of the possible 20 disks. Ground level when disk is locked out.
MLØS/	Master Lockout Switch. Ground level when the whole file is locked out.
MO1L MO2L MO3L MO4L MO5L	Module Designate Levels derived from the five Disk Switch Levels.

RDHM   Read Delay Holdover Multi. 32 microsecond multi is set to inhibit BITPs during a second revolution cross-over when clock tracks are being changed.

REMS/   Remote Level. Ground when the LOCAL-REMOTE switch is in REMOTE.

RIHS   Read Inhibit Holdover Switch. Controlled by RDHM.

SARL/   Segment Address Read Level. Ground level to D.F.C.U. after the Address Count FFs indicate an address has been read.

SCEL-A   Single Clock Enable Level. Negative when the Clock switch is off to enable the use of the single pulse button.

SCLP   Storage Clock Pulse (Character Clock) is a negative pulse for each character. Is also sent to D.F.C.U. to generate clock pulses.

SCØL/   Segment Coincidence Level is ground from D.F.C.U. when address coincidence has been found.

SCØS   SCØL/ switched for gating logic in the E.U.

SEQ-LOC-OUT Normally a ground level to enable a DC ON cycle in the E.U. When the DC Lockout switch is thrown, the ground level is removed inhibiting DC ON.

SPBL-01
SPBL-02   The output levels of two cross-coupled switches which, when in Single Pulse Mode, will provide a negative pulse from SPBL-01 to produce one BITP for each depression of the single pulse button.

SPFF   Space FF. Set by WØMP and cleared by the next BITP (second space bit). Is the first "flag" bit for each word.

SRAL   Storage Read A Level. Negative level to D.F.C.U. when SUAF is set at Character Clock time (SCLP).

SRBL
SR8L
SR4L   Storage Read Levels. Negative level to D.F.C.U. when
SR2L   associated FF is set.
SR1L

SR1L-IND/   Storage Ready "n" Level Indicators. When ground, the
SR2L-IND/   associated indicator will light. They correspond to
SR3L-IND/   HFML-nn/ inputs.
SR4L-IND/
SR5L-IND/

SSUD   Shift SUnFs Driver.

SU1FR   Storage Unit 1 Read FF.

SU1FW   Storage Unit 1 Write FF.

SU2F
SU4F
SU8F   Storage Unit "n" FFs.
SUAF
SUBF

SUCF   Storage Unit Character FF. This FF is set to indicate character time; that is, a complete character. It generates an SCLP.

SUID   Storage Unit Input Strobe. The character to be written is set into the SUnFs.

SURL/   Storage Unit Ready Level. Ground level through a relay contact from SURS/. SURS/ is derived from HFML-nn, Clock On and REMOTE.

SW1L
SW2L
SW4L   Storage Write Levels. Negative level will cause the
SW8L   appropriate SUnF to be set by SUID.
SWAL
SWBL

SWLL   Storage Write Lockout Level. Negative level to D.F.C.U. when an attempt is made to write to a locked out disk.

TD1L
TD2L
TD3L   Threshold Detect Levels. Negative pulses from a Module
TD4L   set the gain control circuit for low gain.
TD5L

TSRF   Threshold Store FF. Set by TDnL from a designated Module.

TO1L/
TO2L/
TO4L/
TO8L/   Track Select Levels. Ground levels from D.F.C.U. to
T10L/   select Track 00 through 99 when combined with DFSL/ and
T20L/   DFSS.
T40L/

WICD Write Information Control Level. Negative during the active word to enable information to be written on the selected track.

WØHF Word Mark FF. Set by the Word Mark Multi. Reset by WØHS/ (WØHM after time out). Used to inhibit the generation of WØMPs by flux changes when an address is being read.

WØHM Word Mark Multi. The multi has 7.8 microseconds duration and is fired and held over by any flux changes read from the address track.

WØHS/ Word Mark Switch. The switched output of WØHM.

WØMD Word Mark Driver. The negative output is the Word Mark pulse to the D.F.C.U.

WØMP Word Mark Pulse. Generated by a flux change in the address track corresponding to the beginning of each word.

WRSD/ Write Storage Level. When positive, indicates a write operation is to be performed.

WSPL-01 Word Single Pulse Level. The output of the Word Single Pulse switch.

ZØ1L/ Zone 1 and 2 Levels from the D.F.C.U. These are decoded
ZØ2L/ to form three levels--ZØ1L-01/, ZØ2L-01/ and ZØ3L-01/ which are used to select the correct zone.

INDEX – SECTION II

2 PRINCIPLES OF OPERATION

2.1 ELECTRONICS UNIT

GENERAL OPERATION

The Disk File Subsystem provides the B200 and B5500 systems with a very large capacity storage device with rapid access to any record. In the Subsystem the Electronics Unit provides the local logical control of up to five Storage Modules.

To write on a disk, first a specified area is identified by its unique address and then the six-bit BCL characters are written serially by bit in that area. The B5500 can write in the binary mode if required. All characters may be written.

To read from the disk, the area to be read must first be located by head selection and address comparison. Then the serial bit information is assembled into characters which are transferred to the Processor one at a time.

Head selection entails the selection of the Module, disk, face, zone and track. Each information track is found in three zones so three heads are designated. Each zone has unique clock tracks and an address will be read for each segment in the selected zone. Once the required segment is located, the read or write operation begins. The E.U. provides logic for head selection, clocking, information read and information write.

HEAD SELECTION

An address is shifted into the A Register in the D.F.C.U. by the Processor. This is the unique address of one segment; 96, 240 or 480 characters on one side of one disk, in one Module, in one E.U. The decoded output levels of A Register are sent to the E.U. which further decodes them into head select lines to the Module and disk face. The levels from the D.F.C.U. are: (Refer to Figure 2.1-1.)

1. The DnnL's which select one Module of five and one of four disks in that Module.

2. Disk Face Select Level (DFSL/) to select the lower or upper face.

3. The ZnnL's which select the 100 heads in one zone (both sides of the disk).

4. The TnnL's which select one of 50 tracks in each zone.

The E.U. decodes the fifty TnnL's and DFSL/ into 100 center tap levels called HSDL's to enable the center taps of the information heads.
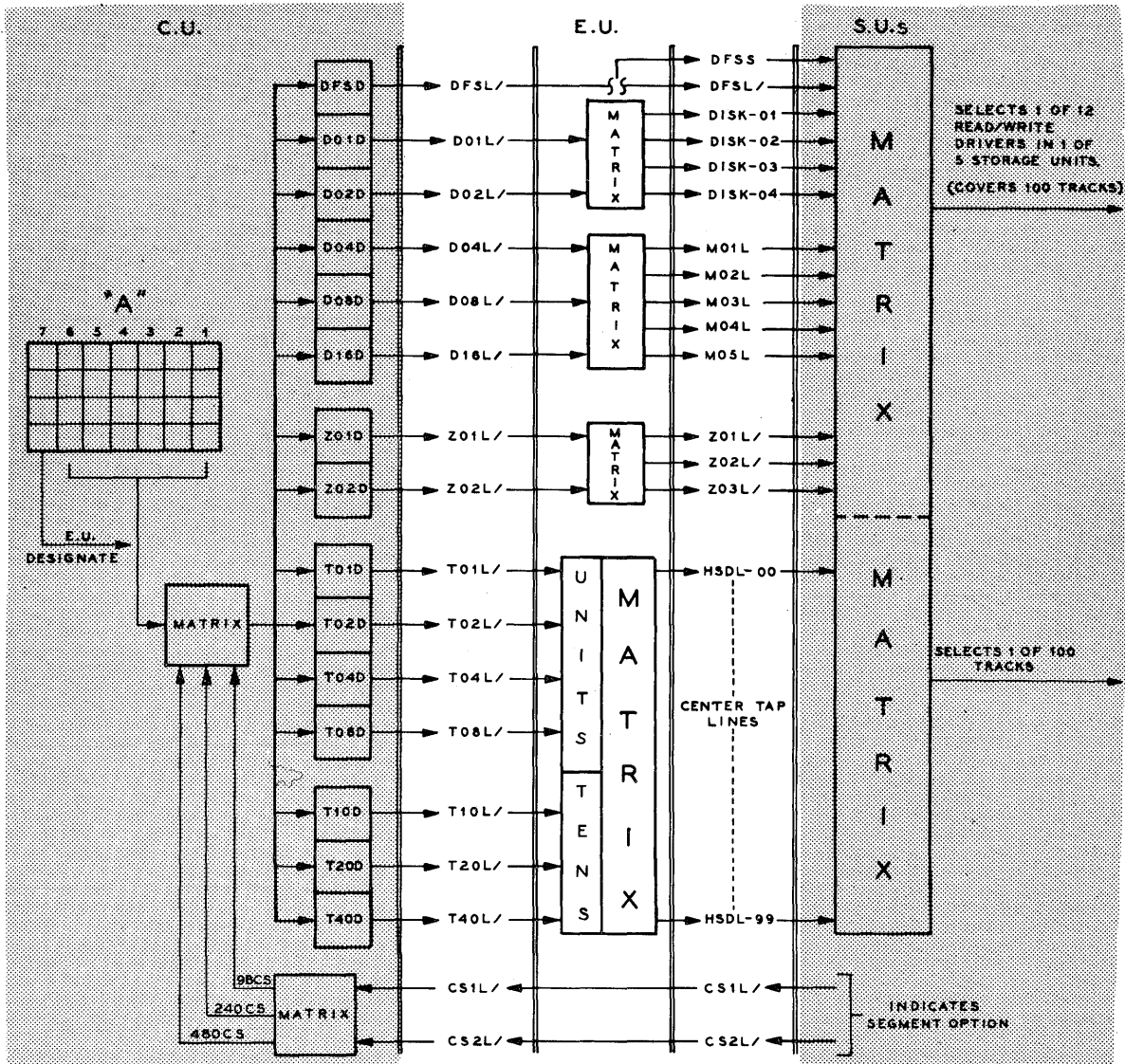
FIGURE 2.1-1
E.U. IN THE DISK FILE SUBSYSTEM

Each HSDL enables 12 heads; one head in each zone of one face of each
disk. With the 480 option, the information head enabled in zone 1
can read and write segments 0 - 11. The corresponding head in zone 2
can read and write segments 12 - 27 and the enabled head in zone 3
can read and write segments 28 - 49. The opposite face on the disk
will have segments 50 - 99. Refer to Figure 2.1-2.

The ZnnL's and Disk-nn will select the 100 heads in one zone of one
disk (both faces). These levels will also enable the center taps of
the four clock heads for that zone of the disk (both faces). The
desired face is selected by DFSL/ and DFSS.

ZONE	480 OPTION		240 OPTION	96 OPTION				
	CW/CCW FACE		ONE FACE	DISK 1		DISK 2		
				CW FACE	CCW FACE	CW FACE	CCW FACE	
1	0→11	50→61	0→23	0→59	250→309	750→809	500→559	
2	12→27	62→77	24→55	60→139	310→389	810→889	560→639	
3	28→49	78→99	56→99	140→249	390→499	890→999	640→749	

FIGURE 2.1-2
SEGMENT ADDRESSES BY OPTION

ADDRESS SEARCH

The selected Word Mark clock head reads three digit addresses from
the Word Mark track and sends them serially by bit, serially by digit,
to the E.U. From the point of view of timing, these addresses are
read during the word time preceding the first word of the segment.
When an address is read by the Word Mark clock head, a new segment
will pass under the selected information head after the next Word
Mark. The segment address is sent back to the D.F.C.U. to be compared
with the address in the A Register. If the segment address compares,
Segment Coincidence Level (SCØL/) is sent to the E.U. to indicate that
the segment has been found. The E.U. will now go into an active read or
write operation. Figure 2.1-3 shows the block diagram of the Address
Search operation.

The selected Bit clock track in the S.U. will generate clock pulses
which are sent to the E.U. The E.U. uses these Bit pulses for all
clocking purposes. Information and addresses are handled in similar
ways by the E.U.; that is, either information levels or address levels
are strobed into the Stack-Up Register (SUnF's) by Bit pulses. When
a complete character has been assembled, it is sent to the D.F.C.U.
parallel by bit.

The Word Mark track generates Word Mark pulses (WØMP) as well as
segment addresses. The Bit track generates timing for writing or
reading one bit at a time. Each zone has its own Word Mark and bit
tracks since, to maintain a reasonably constant packing density in all
three zones, the frequency must vary. There are a total of six clock
tracks on each disk face located between zone 2 and zone 3.

Refer to Figure 2.1-8 for the E.U. logical flow diagram.

The Interlace Control Flip-Flop (ICFF) is the control to determine
active and inactive words. ICFF is off until segment coincidence is
found. After SCØL to the E.U., ICFF is complemented by each WØMP
until the write or read operation is completed. When ICFF is off,
the Word Mark track (ASRL) is scanned for an address (inactive word).
When ICFF is on, reading or writing is being done during the active
word.

The S.U. Register is comprised of seven flip-flops - 1, 2, 4, 8, A, B,
C. The function during write is to receive a character at a time from
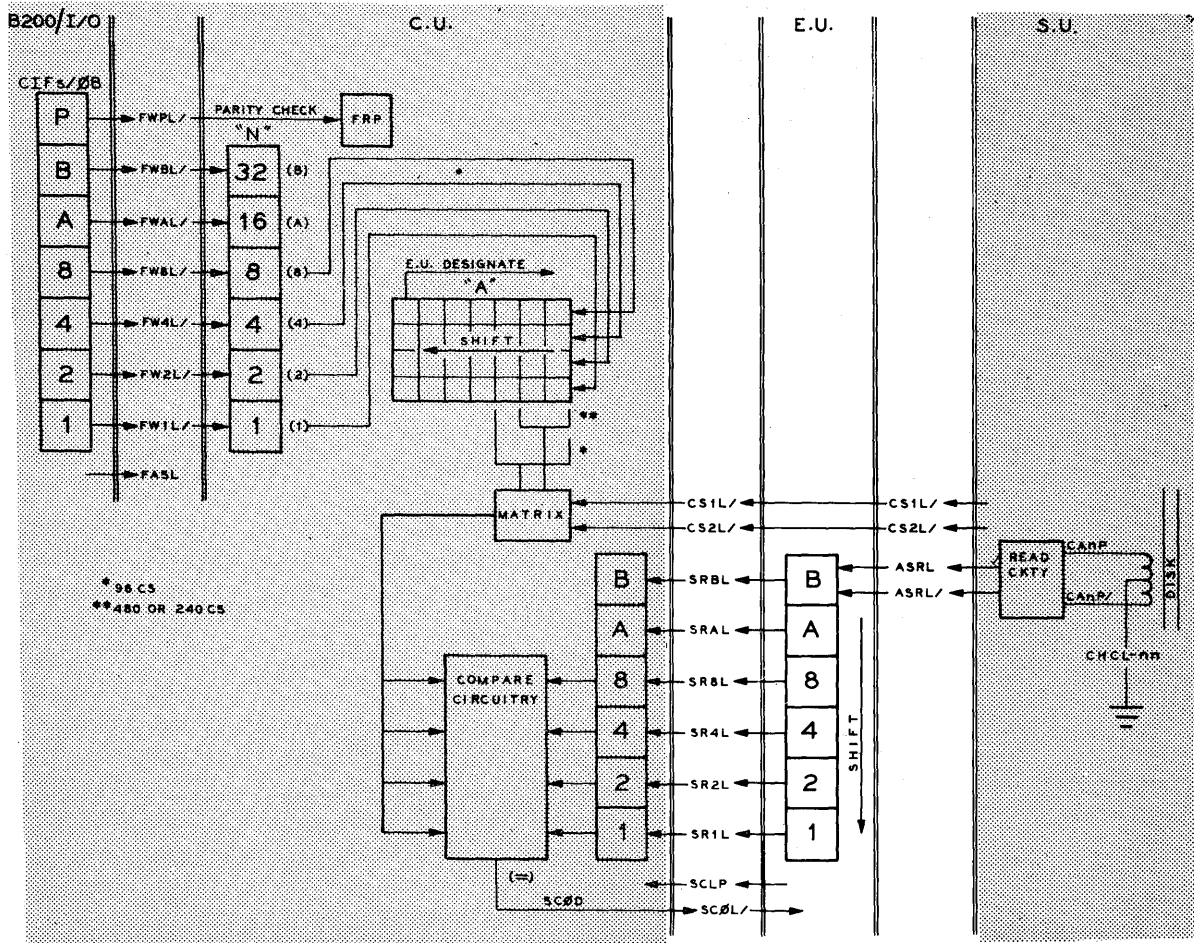
FIGURE 2.1-3
INFORMATION FLOW – ADDRESS SEARCH

the D.F.C.U. and send it serially by bit to the S.U. During read, the bits are stacked up in the S.U. Register until the character is complete and then it is sent to the D.F.C.U.

Address Read Level, ASRL, will produce a WØMP (Word Mark Pulse) with the following logic:

WØMP = ASRS • WØHF/ • BITP

ASRS is also the segment address input to the E.U. after WØMP has been recognized and WØHF inhibits WØMP being generated by address information.

WØMP triggers the Space Flip-Flop (SPFF). SPFF signifies the beginning of a word, either active or inactive.

SPFF = WØMP • SPFF/

The address bits read from the Word Mark track are shifted into SUBF.
Refer to Figure 2.1-4. Notice that SPFF starts the operation by
clearing the S.U. Register and placing a flag bit in SUBF. The flag
bit is circulated through the SUnF's and each time it shifts into
SUCF, an SCLP is sent to the D.F.C.U. to indicate a complete char-
acter has been stacked up.

SCLP = SUCF
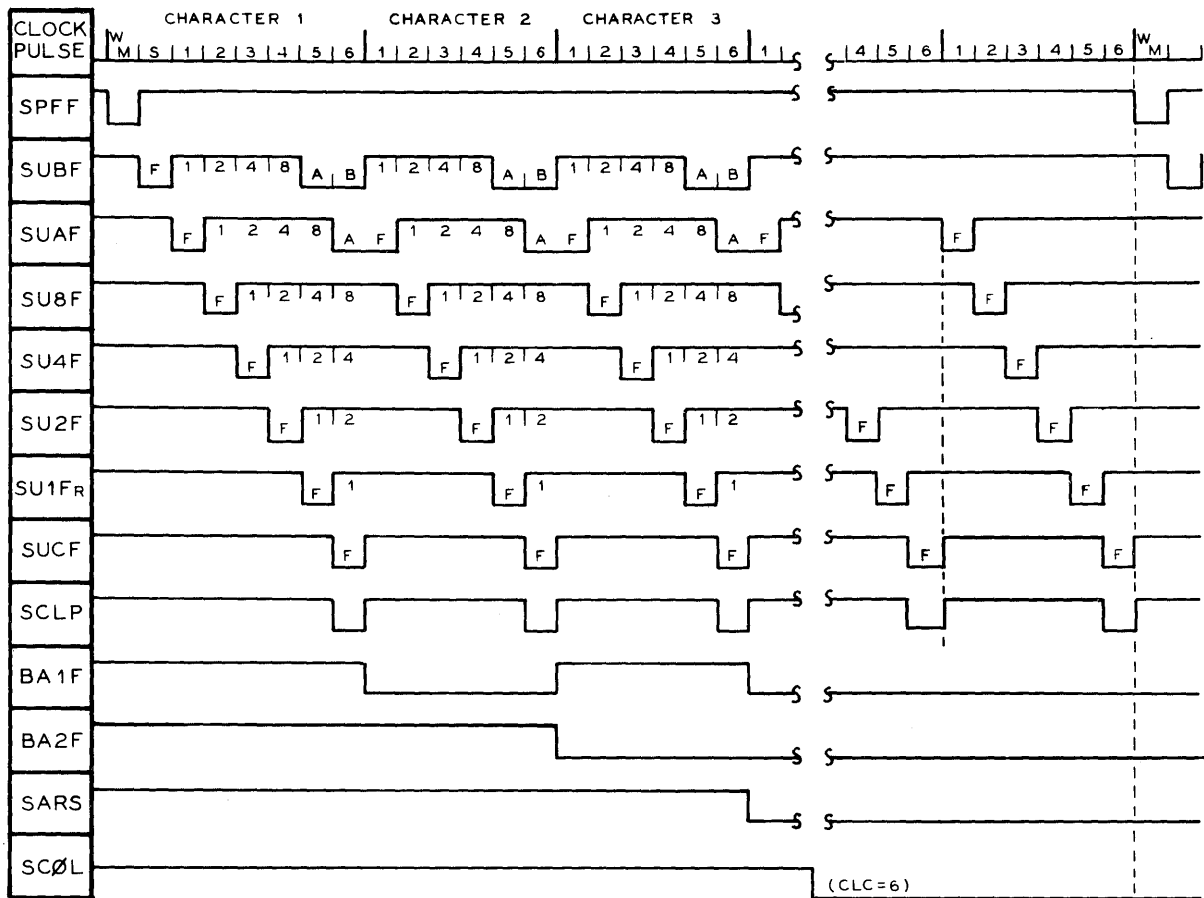
FIGURE 2.1-4
ADDRESS DIGIT ACCUMULATION

Reading continues after this transfer so that the next bit will again
set or reset SUBF. Since the flag bit must precede the character,
SUAF is set.

SUBF = ASRS · SPFF/ · ICFF/
SUAF = ICFF/ · SPFF/ · SUCF

Three address characters will be read for a normal address. The A and
B bits will always be ones to indicate an address digit. (Since the
numeric part of the digit is in binary code, the A and B bits must be
used to indicate a zero.) Each address character causes a count up
of the BA Flip-flops.

BAnF's serve as a counter for the number of address characters read.
Address coincidence cannot be made until three characters have been
compared. The addresses of the maintenance segments have more than
three digits; therefore, BA4F will be set to indicate a maintenance
function.

When three characters have been read, Segment Address Read Level
(SARL) is sent to the D.F.C.U. to indicate a complete address.

$$SARL = BA1F \cdot BA2F$$

If segment coincidence is found, then two SCLP's later, SCØL is sent
to the E.U. to initiate action on the next WØMP.

With SCØL true, the next WØMP sets ICFF and ACFF (Action). ACFF will
remain set during the Read or Write operation unless there is a
change of track. ICFF is complemented with each WØMP for the inactive
words interlaced with the active words.
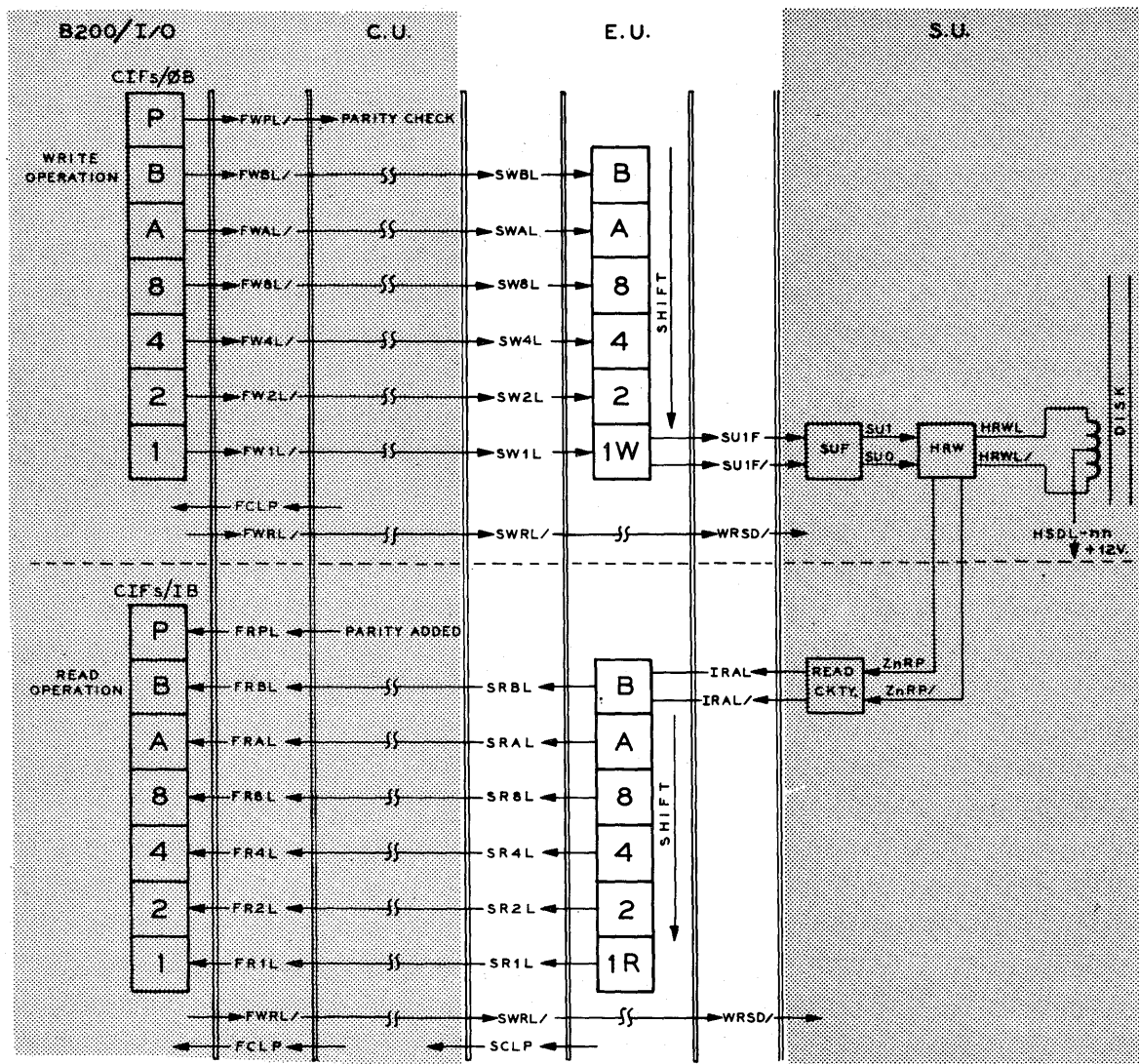
FIGURE 2.1-5
READ/WRITE INFORMATION FLOW

INFORMATION WRITE

Refer to Figure 2.1-5 for the READ/WRITE Information Flow.

The level SWRL from the D.F.C.U. will denote a Write operation. SWRL/ indicates a Read operation. With SWRL, ACFF $\cdot$ ICFF true, WRSD/ will be false to the S.U. for a Write operation.

During a Write operation, the S.U. Register will receive a character at a time from the D.F.C.U. Each bit pulse shifts the character through the Register. SU1Fw replaces SU1Fr during a Write operation. The output of SU1Fw will condition the Bit flip-flop in the S.U. to write a one or a zero on the disk. Refer to the timing diagram, Figure 2.1-6.
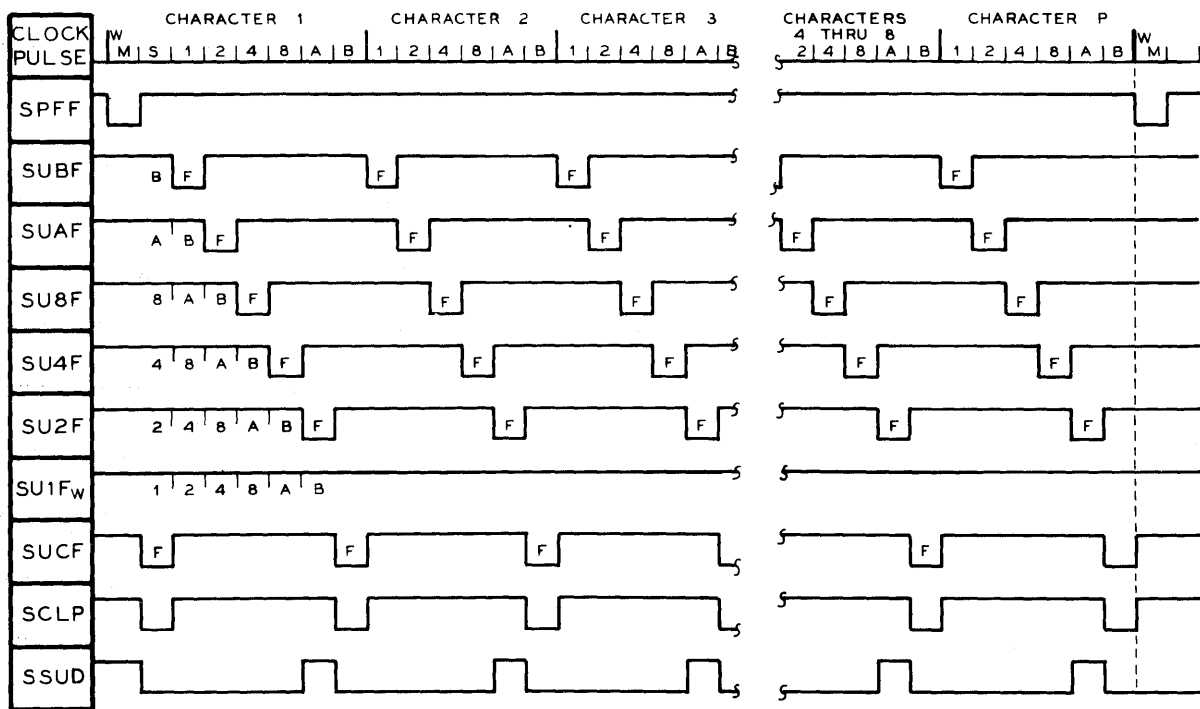
FIGURE 2.1-6
WRITE TIMING

With SPFF, ACFF, ICFF and a Write operation, the first character from the D.F.C.U. is strobed into the S.U. Register and a flag bit is set into SUCF by Storage Unit Input Strobe Driver (SUID).

$$SUID = SPFF \cdot ACFF \cdot ICFF \cdot SWRS$$
$$SUnF \longleftarrow SWnL's = SUID \cdot BCLP$$
$$SUCF = SUID \cdot BCLP$$

With the S.U. Register loaded, the next BITP will write the state of SU1Fw on the disk. The next BCLP will shift the S.U. Register; SUCF to SUBF, SUBF to SUAF, etc.

$$SSUD = SUID/$$

The flag bit is also shifted through the S.U. Register. When it reaches SU2F, the last bit of the character is in SU1Fw being written on the disk. The next BCLP will strobe in the next character from D.F.C.U. and set a new flag bit in SUCF.

$$SUID = SU2F \cdot SU4F/ \cdot SU8F/ \cdot SUAF/ \cdot SUBF/ \cdot SUCF/$$

The Write operation will continue until from 1 to 10 segments have been written when the B200 Processor is connected. The B5500 is capable of writing from 1 to 63 segments with one instruction.

INFORMATION READ

The Read operation is similar to the Address Search operation previously discussed. Instead of ASRL, the Information Read Level, IRAL, which is conditioned by the information track, is strobed into SUBF.
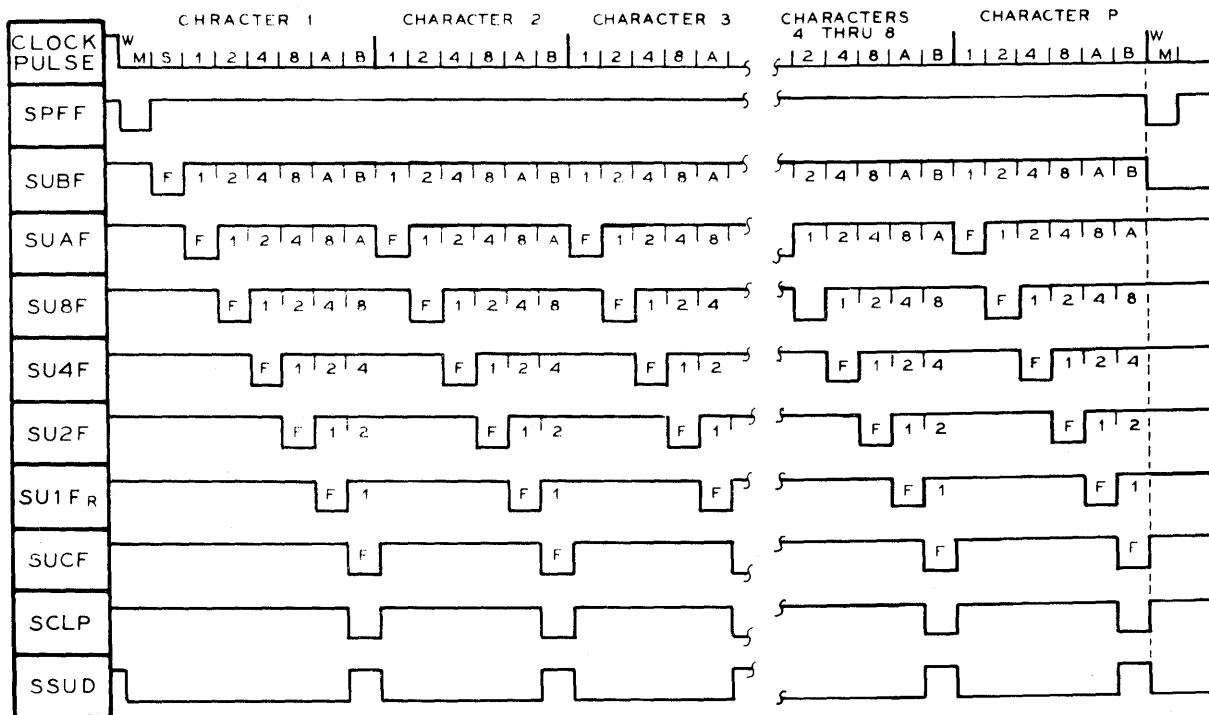
FIGURE 2.1-7
READ TIMING

The Information Read Timing Chart, Figure 2.1-7, starts with the flag bit set into SUBF and the remaining flip-flops being cleared. SU1Fr replaces SU1Fw for Read. The first BCLP after SPFF has been reset will place the first information bit into SUBF and will shift the S.U. Register.

$$SUBF = IRAS \cdot SPFF/ \cdot WRSD/ \cdot ICFF$$

Since the information was written on the disk with word interlace, it must be read in a similar manner. ICFF is set to read the information word and then reset to allow reading of the address track.

As each bit is read off the disk, the S.U. Register is shifted. When the flag bit reaches SUCF, a complete character has been assembled in the S.U. Register and SUCF gates the character to the D.F.C.U.

$$SRnL = SUnF \cdot SUCF$$

The Read operation will continue until the number of segments specified have been read.

FLOATING LOGIC

Label	Action	Condition	#
	BCLP	BITP	1
	SPFF ← 0		
STORAGE CLOCK	SCLP	SUCF	2
	SUCF ← 0	BCLP + DBIT	3
CLEAR PRIOR TO ADDRESS READ	BA4F ← 0	SPFF · INFF/ · BCLP	4
	BA2F ← 0	+ SPFF · ACFF/ · BCLF	5
	BA1F ← 0	+ INXP · INFF	6
END OF OPERATION	ACFF ← 0	SCØL/ · BA2F · BA1F · SUCF · BCLP	7
CLEAR	*SU1FW ← 0	WØMP	8
SET FLAG	*SPFF ← 1	SPFF/	9
	*INFF ← 1	ACFF · BA4F	10
	*INFF ← 0	ACFF · BA4F/	11
	*ICFF ← 0	INXP	12
	*BA4F ← 0		13
	*BA2F ← 0	INFF	14
	*BA1F ← 0		15
	*ACFF ← 0	(ACFF · BA4F · BA2F) + SCØL/	16
	*INFF ← 0	ACFF/ · DIXS/	17

ICFF/

Label	Action	Condition	#
SET INITIAL FLAG	SUBF ← 1	SPFF · BCLP	18
	SUAF ← 0		19
CLEAR SUnFs	SU[8 ⇒ 1R] ← 0	CSUS · BCLP	20
		(CSUS = SPFF + SUCF)	21
COLLECT BITS	↑SUnF (SHIFT)	SSUD · BCLP	22
		(SSUD = SPFF/ · SUCF/)	23
WORD/ADDRESS TRACK	SUBF ← ASRS	SPFF/ · BCLP	24
COUNT ADDRESS CHARACTERS	BA COUNTER + 1	CBAS · BCLP	25
		[CBAS = SUAF · SUBF · SUCF · (BA2F/ + BA4F/)	26
		· SPFF/ · (INFF/ + ACFF/)]	27
SECONDARY FLAG	SUAF ← 1	SPFF/ · SUCF · BCLP	28
SEGMENT ADDRESS HAS BEEN READ	SARL	BA1F · BA2F + BA2F/ · BA4F + BA4F/	29
		· INFF · ACFF + BA4F · ACFF/	30
		WØMP · INFF/	31
START ACTIVE OPERATION NOW	*ACFF ← 1	SCØS · ACFF/	32
	*ICFF ← 1		33
BACK TO ACTIVE	*ICFF ← 1	ACFF · BA4F/	34

ICFF · ACFF

Label	Action	Condition	#
	*ICFF ← 0	WØMP	35
WRITE OPERATION	WRSD	SWRL	36
SET FLAG BIT START OF WORD AFTER EACH CHARACTER	SUCF ← 1	SUID · ECCS · BCLP	37
		(SUID = SPFF + SU2F · SU[C ⇒ 4] = 0)	38
		(ECCS = ASRS/ + WØHF)	39
STROBE IN NEW CHARACTER	SUnF ← SWnL	SUID · BCLP	40
SHIFT FLAG BIT (UNTIL IT REACHES SU2F) CLEAR B-A-8-4 IN TURN	SUBF ← SUCF	SSUD · BCLP	41
			42
		(SSUD = SUBF + SUAF + SU8F	43
SHIFT OUT BITS	↑SUnF (SHIFT)	+ SU4F + SU2F/)	44
FLUX CHANGE ON BIT CHANGE	SUF ← SU1FW		45
READ OPERATION	WRSD/	SWRL/	46
SET INITIAL FLAG	SUBF ← 1	SPFF · BCLP	47
	SUAF ← 0		48
CLEAR FOR CHARACTER COLLECTION	SU[8 ⇒ 1R] ← 0	CSUS · BCLP	49
	SUCF ← 0	(CSUS = SPFF + SUCF)	50
INFO BIT	SUBF ← IRAS	SPFF/ · BCLP	51
LOOK FOR FLAG	SUCF ← SU1FR		52
COLLECT CHARACTER	↑SUnF (SHIFT)	SPFF/ · SUCF/ · BCLP	53
SECONDARY FLAG	SUAF ← 1	SUCF · SPFF/ · BCLP	54

NOTES:

* = UNCLOCKED

CSUS = CLEAR STORAGE UNIT FLIP-FLOPS
SSUD = SHIFT STORAGE UNIT FLIP-FLOPS
CBAS = COUNT ADDRESS CHARACTERS
SUID = STORAGE UNIT FLIP-FLOP INPUT STROBE
ECCS = ENABLE CHARACTER CLOCK

FIGURE 2.1-8
E.U. LOGIC FLOWS

FIGURE 2.1-9
SUBSYSTEM BLOCK SCHEMATIC

2.2 DISK FORMAT

Information on the disk is organized in words and segments. One word consists of 8 characters plus a longitudinal parity character. There is a two bit space between words so that a word time is a total of 56 bit pulses. During a write or read operation an active word is followed by an inactive word. Interlace is controlled by ICFF. The words from two segments are interlaced to allow the address track to be scanned during the inactive word. The bit frequency on the disk varies from 1 mc in zone 1 to approximately 1.8 mc in zone 3.
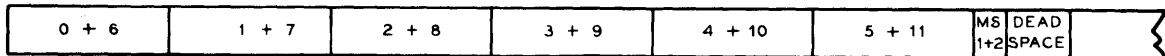
The segment layout for a track in zone 1 using the 480 option is as follows:

0 + 6	1 + 7	2 + 8	3 + 9	4 + 10	5 + 11	MS 1+2	DEAD SPACE	

Each word of segment 0 is followed by a word of segment 6, completely interlacing the two segments. The following diagram depicts this word interlace:

WORD 59 SEG 6	WORD 60 SEG 0	WORD 60 SEG 6	WORD 1 SEG 1	WORD 1 SEG 7	WORD 2 SEG 1

The address for each segment is written in the word mark track during the word time preceding the first word of that segment. The following diagram illustrates this:

NOTE

The address digits are in REVERSE order.

WØMP WORD 59 SEG 6	WORD 60 SEG 0	100 WORD 60 SEG 6	700 WORD 1 SEG 1	WORD 1 SEG 7	WORD 2 SEG 1
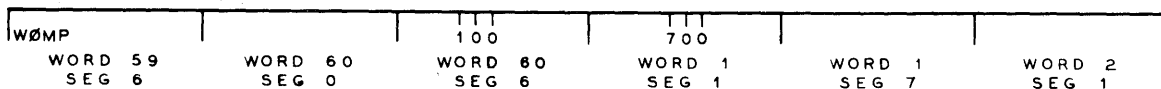
It takes two revolutions of the disk to completely read or write one track. On each revolution a dead space is encountered which is a physical reference on the disk. One maintenance segment can be operated on in each revolution. The first revolution may read segments 0 through 5 or MS1, and the second revolution will read segments 6 through 11 or MS2.

Preceding the dead space on each track are the two maintenance segments which are available to the engineer for checking purposes. The maintenance segments are 96 characters long regardless of the S.U. option.

When a read or write operation is in progress, the dead space and maintenance segments must be taken into account. Refer to Figure 2.2-1 for first revolution crossover. The figure reflects the 480 option, though the action is similar for the 240 and 96 options.
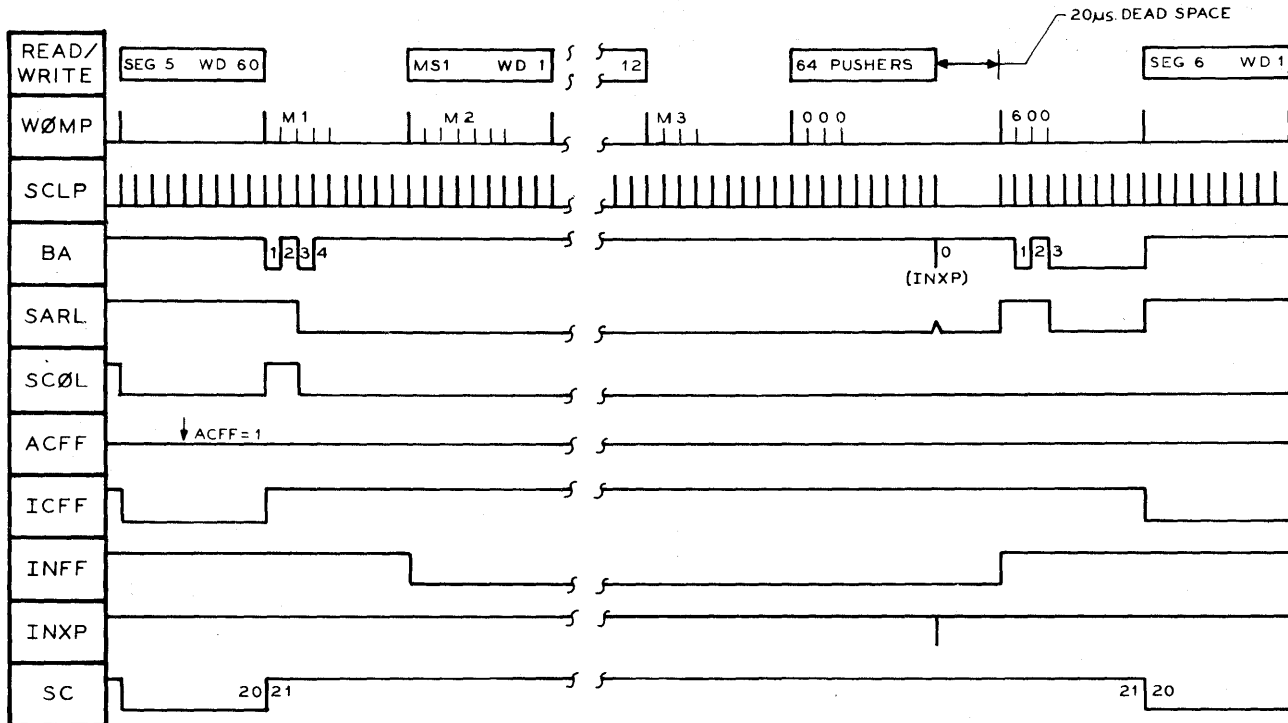
FIGURE 2.2-1
FIRST REVOLUTION CROSSOVER

Assume the operation has proceeded through the last word of segment 5 (the 6th segment). The next WØMP signals the start of an inactive word during which the address for Maintenance Segment 1 will be read. The address consists of four binary 10's. The 4 character address results in BA4F being set. INFF will be set by the next WØMP to inhibit further action during the maintenance segments and dead space. BA4F is cleared by INXP, which is generated by the absence of BITPs.

$$INFF = WØMP \cdot ACFF \cdot BA4F$$

Notice that ACFF remains set to indicate further action is required on this track. INFF is reset by the first WØMP after dead space so that ICFF will not be set until the second word after the dead space. This second word is the first word of segment 6.

$$ICFF = WØMP \cdot INFF/$$

SCLP pulses occur each time SUCF is set with the flag bit. The flag bit circulates until cleared by WØMP; therefore SCLP pulses are produced up to the dead space. Sixty four extra bit pulses occur after the last word of MS2 and before the dead space occurs. They are called "pusher" pulses and create SCLPs for the pseudo word time during which is read the address of the first segment after the dead space.

The crossover on the second revolution involves the selection of another information head and different clock tracks. The "A" Register in the DFCU is counted up as each segment is completed. After two revolutions on one track, the address in the "A" Register will activate new head select lines. The new address may be on another disk face or disk, so dead space is used to ensure the logic stays in sync.
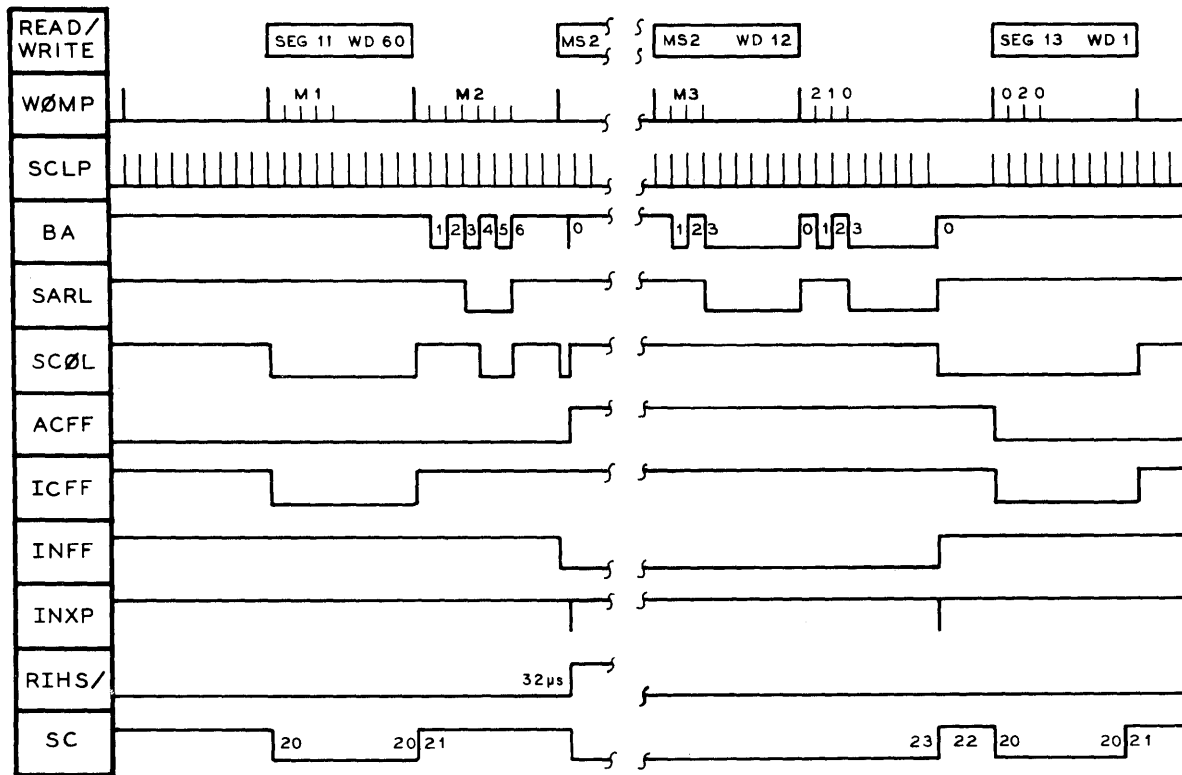
FIGURE 2.2-2
SECOND REVOLUTION CROSSOVER

Refer to Figure 2.2-2. After the last word of the last segment on the track the six digit (all binary 12's) MS2 address is read during the inactive word. The 6 digit address will set BA4F . BA2F to indicate a change of track. INFF is set by WØMP and, with BA4F and BA2F, enables a simulated INXP to be generated. This INXP will reset ACFF and the "A" Register counts up the segment address and a new head is selected. DIXM is fired by INXP. BITPs are inhibited by RIHS/ to prevent extraneous pulses occurring during the clock track change.

RIHS/ = RDHM (32 microseconds) • IXHS/ • DIXM

With INFF on, no further action can take place until it is reset by INXP. This will occur when the newly selected head reads into dead space. SCØL from the DFCU will permit the first WØMP after dead space to set ACFF and ICFF, and the operation will continue in sequence on the new track.

INDEX - SECTION III

3 FUNCTIONAL DESCRIPTION - ELECTRONIC

3.1 DISK FILE ELECTRONICS AND STORAGE UNITS POWER SEQUENCING

Reference Figure 3.1-1.

Power for an Electronics Unit and its associated Storage Modules is supplied from the E.U. power supplies. Disk drive motors in the Storage Modules start in consecutive sequence from the first Module. Successive Modules can only start after the motor in the preceeding Module is up to speed. No DC voltages can be applied to the E.U. gate or the Modules until the disk drive motors in all Modules associated with that E.U. are up to normal running speed. If the Motor Run Switch of a Module is in the Off position, that Module's motor will not start and the sequence continues with the next Module in line.

UNDER VOLTAGE FAIL SENSOR

Each E.U. has a voltage fail sensor which monitors the DC output voltages of the power supplies. When the supplies are correct, a ground level is supplied to the power sequencing which allows a normal DC On cycle. If any DC voltage falls below normal, DC power will cycle off as in a normal DC Off cycle. Ref. Fig. 3.1-2 for detailed schematic.

ELECTRONICS UNIT DC LOCKOUT SWITCH

Each E.U. has a lockout switch which disables the DC On sequence. With DC locked out, AC may be applied but no DC voltages will be supplied to the Modules and E.U. gate.

ELECTRONICS LOCAL-REMOTE SWITCH

Each E.U. has a Local-Remote switch. In the Remote position the -24V to start the DC On cycle may come from either the associated Disk File Control or the DC On switch on the E.U. control panel. If the switch is in the Local position, the -24V must come from the DC On switch on the E.U. control panel only.

MODULE MOTOR RUN SWITCH

Each Module has a motor run switch which, if on, enables the pick of its motor power relay when SMIL (Start Motor Input Level) from the preceeding Module is present. If off, it disables the pick of the motor power relay and transfers SMIL to the next Module as SMOL (Start Motor Output Level).

ELECTRONICS UNIT POWER SEQUENCING PANEL

Inputs

    208VAC Leg A
    208VAC Leg B   Main line voltage inputs.
    AC Neutral

    Remote-DC-ON
    Remote-DC-OFF   Remote power control lines from asso-
    Emergency-Power-Off   ciated Disk File Control cabinet.
    Pwr-Cont-Comm

    AC-ON-IND
    AC-ON
    AC-OFF
    DC-ON-IND
    DC-ON   Power control levels from switches and
    DC-OFF   indicators on E.U. Control Panel and
    LOC-REM-DC-ON   Under-Voltage Fail Sensor.
    DC-Sense-Control
    SEQ-LOC-OUT

    Power Supply Voltages
    (Rack F)   +100V, -100V, -120V, -24V, GND

    Power Supply Voltages
    (Rack G)   -12V, +12V, -4.5V, GND

    Power Supply Voltages
    (Rack H)   +20V, -20V, GND

    SMOL   Ground level from last storage module in
                            a file to E.U. power sequencing panel.

    -24D   Return from Air Compressor Pressure Switch.

Outputs

Electronics Gate and Modules:

    -4.5V
    -20V
    +20V
    +12V
    -12V
    -24D

Modules:

    208VAC   Legs A and B to disk drive motors and heat
                           exchange fans (2 per module), garage fans
                           (3 per module) and Running Time Meter.

115VAC	208VAC Leg A for convenience outlets.
SMIL	Ground level to Motor Run Switch in first module.

Electronics Unit Maintenance Panel:

+100V -100V -120V	Indicator drivers.
208VAC Legs A and B	Running Time Meter.
115VAC (Leg A 208VAC)	Convenience outlets and air compressor.
115VAC (Leg B 208VAC)	E.U. fans (2 per unit).

All voltages metered at E.U. panel.

POWER ON SEQUENCE

Conditions:

70 Amp. Circuit Breaker On.
E.U. Local-Remote switch in Local or Remote position.
E.U. DC Lockout switch off.
Motor Run switches in all Modules in Run position.

AC-ON-Cycle

AC Circuit Breaker "ON" (15 Amp.)	208VAC Legs A and B to -24V power supply in E.U. and air compressor motor. Leg A to contact 8 ECJO, convenience outlets in E.U. and modules. Leg B to contact 10 ECJO.
-24V Power Supply	Supplies relay control voltage to E.U. and modules.
AC Circuit Breaker "ON" (50 Amp.)	208VAC Legs A and B to motor power relay contacts in all Modules.
AC-On-Switch "ON" EFJO contacts 8-10	Pick EFJO (ground pin 1 coil circuit). Hold EFJO (ground pin 1 coil circuit through NC contacts 7-8 EFKO and NC AC-Off-Switch).
contacts 7-9	SMIL to first Module (ground to Module Motor Run Switch. Picks Motor Power Relay and starts disk drive motor). Pick ECJO (ground pin 1 coil circuit).

ECJO contacts 5-6   Enable pick and hold EFJ1 circuit. (Close line from DC-On and Local-Remote switch to pin 1 EFJ1 coil and contact 10 EFJ1 through NC contacts 6-8 EFK1.)

        contacts 3-4   AC-On-Indicator lit (-24V to indicator).

        contacts 7-8   208VAC Legs A and B to DC Power Supplies, Running Time Meter, and E.U. and module garage fans.

When all module disk drive motors are up to speed, SMOL from last module in sequence supplies ground level to contact 7 EFJ1 and enables pick of ECMO.

DC-ON-Cycle

DC-ON-Switch "ON" or Remote DC "ON"   Pick EFJ1 (-24V to pin 1 coil circuit through contacts 5-6 ECJO and 6-8 EFK1). Ground to pin 4 coil EFJ1 supplied from Under-Voltage Fail Sensor (ground when Power Supply voltages normal) through NC DC-Off-Switch, NC DC-Lockout-Switch, NC AC-Off-Switch, NC contacts 3-4 EFKO, and NC contacts 6-8 EFJ2.

EFJ1 contacts 14-16   Enable pick EDMO and EDJ1. (Ground pin 1 coil circuit on both relays.)

        contacts 7-9   Pick ECMO (ground pin 2 coil circuit with SMOL from last module when module motors up to speed).

        contacts 8-10   Hold EFJ1 (-24V to pin 1 coil circuit).

        contacts 13-15   Pick EFK1 (-24V to pin 1 coil circuit through contacts 3-4 ECJO). Ground to pin 4 EFK1 coil circuit supplied through NC contacts 5-7 EFJ2 and NC DC-Off-Switch.

EFK1 contacts 7-9   Hold EFK1 (-24V to pin 1 coil circuit through contacts 3-4 ECJO).

        contacts 6-8   Open -24V line from DC-On-Switch to pin 1 coil circuit EFJ1.

ECMO contacts 17-18   Pick EDMO (-24V to pin 2 coil circuit).

        contacts 15-16   -4.5V to E.U. gate and modules.

contacts 13-14 11-12	-20V to E.U. gate and Modules.
contacts 7-8 9-10	+20V to E.U. gate and Modules.
contacts 5-6	Hold ECJO (ground pin 1 coil circuit).
contacts 3-4	-24D to E.U. gate and Modules when Air Compressor Pressure Switch is closed.
EDMO contacts 9-10	Hold ECMO (ground pin 2 coil circuit).
contacts 7-8	Pick EDJ1 (-24V to pin 2 coil circuit).
contacts 5-6	+12V to E.U. gate and Modules.
contacts 3-4	-12V to E.U. gate and Modules.
EDJ1 contacts 13-14	DC-On-Indicator lit (-24V to indicator).
contacts 11-12	Hold ECMO (ground pin 2 coil circuit).
contacts 7-8	-120V to Maintenance Panel.
contacts 5-6	-100V to Maintenance Panel.
contacts 3-4	+100V to Maintenance Panel.

Relays EFJO, ECJO, EFJ1, EFK1, ECMO and EDJ1 are energized, EFKO and EFJ2 are de-energized. Module motors all running and power supply voltages normal.

DC-OFF-Cycle (Local)

Depress DC-Off-Switch	Drop EFJ1 (remove ground from pin 4 coil circuit through NC contacts 3-4 EFKO and 8-6 EFJ2).
	Drop EFK1 (remove ground from pin 4 coil circuit through NC contacts 5-7 EFJ2).
Open EFJ1 contacts 14-16	Drop EDJ1 (remove ground from pin 1 coil circuit).
	Drop EDMO (remove ground from pin 1 coil circuit).
contacts 7-9	Remove SMOL ground to pin 2 coil circuit ECMO. ECMO will hold until EDJ1 and EDMO drop.

contacts 8-10	Open hold EFJ1 line (remove -24V from pin 1 coil circuit).
contacts 13-15	Open pick EFK1 line (-24V to pin 1 EFK1 coil circuit).
Open EFK1 contacts 7-9	Open hold EFK1 line (remove -24V pin 1 coil circuit).
close contacts 6-8	Enable pick EFJ1 line.
Open EDJ1 contacts 13-14	DC-On-Indicator off (remove -24V from indicator).
contacts 11-12	Open one hold ECM0 line (remove ground from pin 2 coil circuit).
contacts 7-8	Remove -120V from Maintenance Panel.
contacts 5-6	Remove -100V from Maintenance Panel.
contacts 3-4	Remove +100V from Maintenance Panel.
Open EDM0 contacts 9-10	Drop ECM0 (remove ground from pin 2 coil circuit). Last hold ECM0 in DC-Off-Cycle.
contacts 7-8	Open pick EDJ1 line (remove -24V from pin 2 coil circuit).
contacts 5-6	Remove +12V from E.U. gate and Modules.
contacts 3-4	Remove -12V from E.U. gate and Modules.
Open ECM0 contacts 17-18	Open pick EDM0 line (remove -24V from pin 2 coil circuit).
contacts 15-16	Remove -4.5V from E.U. gate and Modules.
contacts 13-14 11-12	Remove -20V from E.U. gate and Modules.
contacts 7-8 9-10	Remove +20V from E.U. gate and Modules.
contacts 5-6	Open hold ECJ0 line (remove ground from pin 1 coil circuit).
contacts 3-4	Remove -24D from E.U. gate, Air Pressure Switch and Modules.

AC-OFF-Cycle (Local)

Depress AC-Off-Switch	Drop EFJ0 (open hold EFJ0 line and remove ground from pin 1 coil circuit, through NC contacts 7-8 EFK0). Start normal DC-Off-Cycle by dropping EFJ1 (AC-Off-Switch and DC-Off-Switch in series). See "Drop EFJ1" in DC-Off-Cycle (Local).
Open EFJ0 contacts 8-10	Open hold EFJ0 line (remove ground from pin 1 coil circuit).
contacts 7-9	Open pick ECJ0. Drop ECJ0 only when ECM0 (last relay to drop in DC-Off-Cycle) removes ground from pin 1 coil circuit ECJ0; Module motors will stop due to loss of ground level (SMIL) to motor power relays.
Open ECJ0 contacts 5-6	Open pick EFJ1 line from DC-On-Switch to pin 1 coil circuit EFJ1.
contacts 3-4	AC-On-Indicator off (remove -24V to indicator).
	Open hold EFK1 line (remove -24V from contact 9 EFK1). Open pick EFK1 line (remove -24V from contact 15 EFJ1).
contacts 7-8 9-10	DC power supplies off (remove 208VAC Legs A and B to power supply racks F, G and H).
	Running Time Meter and E.U. fans off. (Remove 208VAC Legs A and B to RTM and Leg B to fans.)

DC-OFF-Cycle (Remote)

Remote DC-Off pulse from D.F.C.U.	Pick EFJ2 (-24V pulse from Processor to pin 4 coil circuit).
Open EFJ2 contacts 8-10	Drop EFJ1 (remove ground from pin 4 coil circuit).
contacts 5-7	Drop EFK1 (remove ground from pin 4 coil circuit).

Dropping EFJ1 and EFK1 starts normal DC-Off-Cycle. Refer to "Open EFJ1" in DC-Off-Cycle (Local) for further details. Note that the AC On condition is not affected and the Module motors continue to run.

Emergency-Power-Off-Cycle

Emergency-Power-Off pulse from Processor	Pick EFK0 (-24V pulse from Processor to pin 1 coil circuit).
Open EFK0 contacts 3-4	Drop EFJ1 (remove ground from pin 1 coil circuit through contacts 8-6 EFJ2, NC AC-OFF-Switch, NC DC-OFF-Switch and DC Lockout-Switch from the Under Voltage Fail Sensor).
contacts 7-8	Drop EFJ0 (open hold EFJ0 line from NC AC-OFF-Switch to contact 10 EFJ0).

Dropping EFJ1 and EFJ0 starts AC and DC Off-Cycles. Refer to "Open EFJ1" in DC-Off-Cycle (Local) and "Open EFJ0" in AC-Off-Cycle (Local) for further details.

BLDG. GND. L3

NEUT. L3

NOTE:
1. CONNECT JUMPER FROM PIN 1 OF ECKO TO PIN 6, 5, 4, 3 OR 2 OF ECKO DEPENDING UPON NUMBER OF MODULES USED.

EAMO
01
02 NEUT. MODS. 1 & 2
03 NEUT. MODS. 3 & 4
04 NEUT. MOD. 5

FILTER BKT. MTG. SCREW
CONV. OUTLET

MOTOR START LEVELS

ECKO
MOD. 1 06
MOD. 2 05
MOD. 3 04
MOD. 4 03
MOD. 5 02
SEE NOTE 01

ECLO
MOD. 1 06
05 MOD. 2
04 MOD. 3
03 MOD. 4
02 MOD. 5
01

SMIL

SMØL

EDJO
208B 04 P.S.-F, E.U. & MODULE GARAGE FANS
05 P.S.-G
06 P.S.-H

EEJ1
17 208B
16 208A
E.U. RTM

EDJO
208A 01 P.S.-F, E.U. & MODULE GARAGE FANS
02 P.S.-G
03 P.S.-H

EEJ1
02
03 P.S.+100
04 P.S.-100
05 P.S.-120

TO METER ON MAINTENANCE PANEL

MTG. SCREW ON TERMINAL STRIP

EBRO
GND P.S.-F 01 MOD. 1 GATE & BACKPLANE
GND P.S.-G 02 MOD. 2 & 3 GATE & MOD. 2 BACKPLANE
GND P.S.-H 03 MOD. 4 & 5 GATE & MOD. 3 BACKPLANE
MTG. SCREW ON B PANEL 04 MOD. 4 & 5 & E.U. BACKPLANE

EAPO
02 MOD. 1 & 2 PS -12
03 MOD. 3 & 4 PS +12
-24V. 04 MOD. 5

EEJO
09
08
10 DC SENSE VOLTAGE TO GATE & METER ON MAINT. PANEL
11
12
13

EEJO
02
03
04 GATE
05
06
19 DC -ON INDICATOR

EEJ1
13
19
20 E.U. AIR PRESSURE SWITCH

EBPO
-12 02 MOD. 1
03 MOD. 2 & 3
04 MOD. 4 & 5
GATE

EBNO
+12 01 MOD. 1
02 MOD. 2 & 3
03 MOD. 4 & 5
04 GATE

EBMO
01 MOD. 1
02 MOD. 2 & 3
-24D 03 MOD. 4 & 5
SEQ. PANEL

EBLO
+20 01 MOD. 1
02 MOD. 2 & 3
03 MOD. 4 & 5
04 GATE

EBKO
-20 01 MOD. 1
02 MOD. 2 & 3
03 MOD. 4 & 5
04 GATE

EBJO
-4.5 01 MOD. 1
02 MOD. 2 & 3
03 MOD. 4 & 5
04 GATE

L1 P.S. 15A
EALO
01
02 115VAC MODS. 1 & 2
03 115VAC MODS. 3 & 4
04 115VAC MOD. 5
24V. P.S.

CONVENIENCE OUTLETS IN MODULES
115VAC

AS M AIR COMP.

L2 P.S. 15A
EARO
01
02
03
04 24V. P.S.

LOCAL/ REMOTE SW
REMOTE DC-ON-E
AC-ON-IND.
DC-ON-SW
-24V
AC-ON-SW
AC-OFF-SW
DC LOCKOUT SW
DC-OFF-SW

EEJ1
07
06
05 EDLO
08
09
11
12

ECJO
EDKO ECJO EDKO

EFJO
EDPO EDPO

EFK1
EDNO EDNO

EFKO
EDNO EDNO EDKO

EFJ1
EDPO EDPO

50A
EAKO
01
02 208VAC MODS. 1 & 2
03 208VAC MODS. 3 & 4
04
208VAC MOD. 5

UVFS
+20V
+12V
-4.5V
-12V
-20V
-24V

50A
EAJO
01
02 208VAC MODS. 1 & 2
03 208VAC MODS. 3 & 4
04 208VAC MOD. 5

REMOTE DC-OFF
EMERGENCY PWR-OFF
EEJO
16
17
PWR. CONT. COMM. 18
REM-DC-ON 14
DC SENSE CONT. 15

EEJ1
14 REM-DC-ON-E
15 DC-SENSE-CONT.-P
18

ECMO
EDKO ECMO EDKO

EFJ2
EDNO EDNO

AUTO XFMR WIRED FOR 208V AC
L3 1
L3 0
70A
LEG B
LEG A
208V AC
220V AC
230V AC
240V AC
SOURCE

P.S. +20
P.S. -20
P.S. -4.5

EDMO
EDLO

EDLO

EDJ1
EDLO EDLO

NOTE: ALL TERMINALS ON SEQUENCE BUS BARS LOCATED AT RACK "E", PANELS "A" & "B", ARE BUSED TOGETHER.

FIGURE 3.1-1
E.U. POWER SEQUENCING

FIGURE 3.1-2
UNDER VOLTAGE FAIL SENSOR

-20V

CR2
18V ZENER
IN967B

CR33
TYPE 5

R1
1.8K

+12V

R24
20K

-12V

R23
2K

-12V

R21
6.19K

-24V

CR15

D.C.
SENSE
CONTROL
TO
POWER
SEQUENCING
RACK "E"

CR22   CR20

Q3
2N586

R19
100K

+20V

-4.5V

R28
348

CR30

R29
1.87K

+20V

-12V

R8
1.8K

CR9
18V ZENER
IN9678

CR7   CR6

Q2
TYPE F

-20V

+20V

R11
1.96K

CR10

R12
1K

R13
31.6

+12V

R5
100K

+20V

-12V

R3
2K

CR4

Q1
TYPE F

-12V

R25
1.21K

CR27   CR22

R26
2.26K

+20V

R34
18.7K

-12V

R31
82.5K

+20V

CONNECTOR-WIRE SIDE

	0	1	2	3	4		5	6	7	8	9
(OR) A N											
B P	o	o	o	o	o		o	o	o	o	o
C R	o	o	o	o	o		●	o	o	●	o
D S	●	o	o	o	o		o	o	o	o	o
E T	o	o	o	●	o		o	o	o	o	o
F U	o	o	o	o	o		o	o	o	o	o
H V	o	o	o	o	o		o	o	o	●	o
J W	o	o	o	o	o		o	o	●	o	o
K X	●	o	o	o	o		o	o	o	o	o
L Y											

-20V INPUT → D S
GND → E T
SENSE OUTPUT → H V
-24V INPUT → K X

+12V INPUT
-12V INPUT
+20V INPUT
-4.5V INPUT

NOTE:
ALL DIODES ARE TYPE 11 UNLESS OTHERWISE SPECIFIED.

3.2 CABLING

All the lines in the logic and power cables associated with an Electronics Unit are shown on pin cross-reference tables. The following is a list of the cables with table references. Refer to Figure 3.2-1 for sub-system cabling diagram.

LOGIC CABLES INTER-UNIT

Table 3.2-1.

ACB0N7------GAK4	Information center tap select cables
ACB0N2------GAL4	from E.U. logic gate to center tap
ACB0A7------GAJ4	distribution board in Module 1.

Table 3.2-2.

AAB0A2------ B450 Panel K (C.U. 1 or 3) B450 Panel N (C.U. 2 or 4)	E.U. logic gate to Control.

Figure 3.2-2.

AAB0N2------AAB0A2 (Module 1)	E.U. logic gate to first Module.

LOGIC CABLES INTERNAL

Table 3.2-3.

AAA0A2------Maintenance Panel	E.U. logic gate to Maintenance Panel. Switch and indicator levels.

Table 3.2-4.

AAA0A7------Write Lockout Panel	E.U. logic gate to Write Lockout Panel. Switch levels.

POWER CABLES INTER-UNIT

Table 3.2-5.

Rack E _____Motor power relay Panel A in Modules 1 through 5	AC power cables from E.U. sequence panel to each Module.

Table 3.2-6.

Rack E _____AAB0N2 (Modules Panel B 1 through 5)	DC power cables from E.U. sequence panel to each Module.

POWER CABLES INTERNAL

Table 3.2-7.

AAAON2-----Maintenance Panel   Maintenance Panel power cable.

Table 3.2-8.

Rack E
Panel B _____-AACOA2   Power control cable.

Table 3.2-9.

Rack E
Panel B _____-AACON2   DC - Panels A and B.

Table 3.2-10.

Rack E
Panel B _____-ACAOA2   DC - Panels C and D.
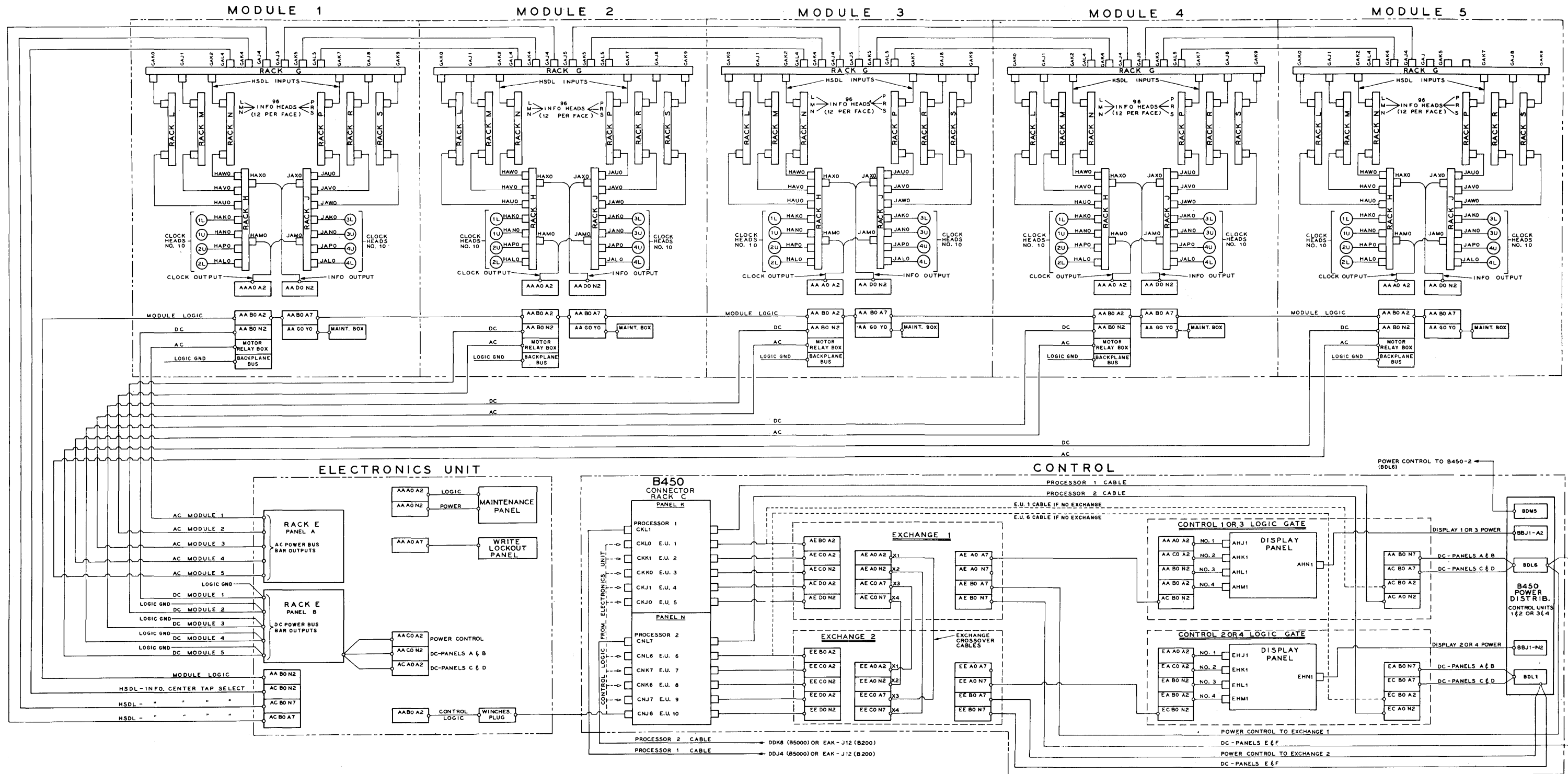
FIGURE 3.2-1
SUBSYSTEM CABLING DIAGRAM
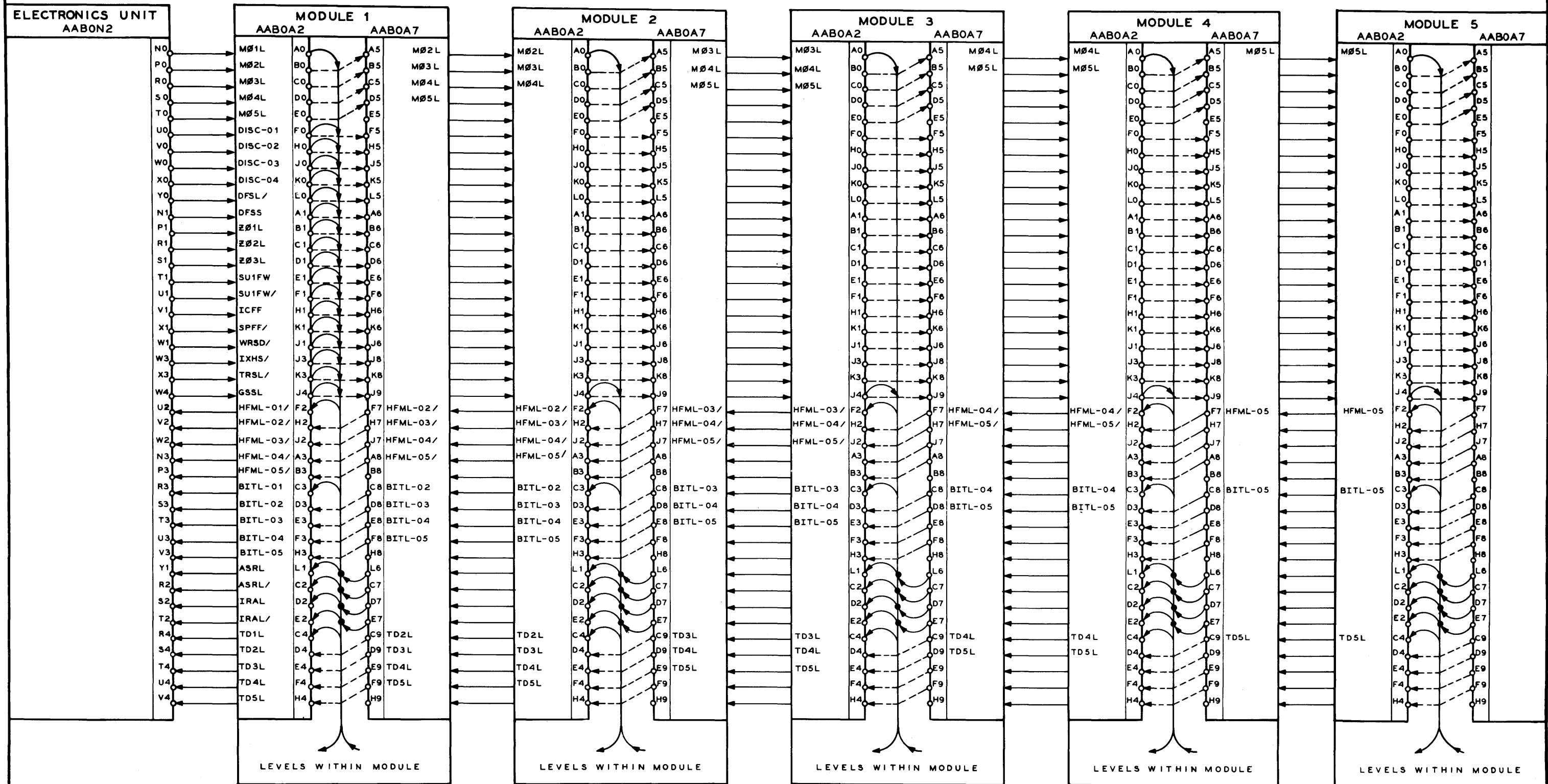
FIGURE 3.2-2
MODULE LOGIC CABLE

TABLE 3.2-1

*E.U. ACBOA7	**MOD. GAJ5	LEVEL	MOD. GAJ4	*E.U. ACBON2	**MOD. GAL5	LEVEL	MOD. GAL4	*E.U. ACBON7	**MOD. GAK5	LEVEL	MOD. GAK4
A5	19	HSDL-90	1	N0	19	HSDL-08	1	19	N5	HSDL-13	1
B5	18	HSDL-88	2	P0	18	HSDL-06	2	18	P5	HSDL-11	2
C5	17	HSDL-74	3	R0	17	HSDL-12	3	17	R5	HSDL-33	3
D5	16	HSDL-98	4	S0	16	HSDL-00	4	16	S5	HSDL-05	4
E5	15	HSDL-96	5	T0	15	HSDL-26	5	15	T5	HSDL-03	5
F5	14	HSDL-89	6	U0	14	HSDL-16	6	14	U5	HSDL-29	6
H5	13	HSDL-67	7	V0	13	HSDL-32	7	13	V5	HSDL-45	7
J5	12	HSDL-69	8	W0	12	HSDL-34	8	12	W5	HSDL-47	8
K5	11	HSDL-85	9	X0	11	HSDL-20	9	11	X5	HSDL-25	9
A6	10	HSDL-59	10	N1	10	HSDL-40	10	10	N6	HSDL-60	10
B6	9	HSDL-61	11	P1	9	HSDL-42	11	9	P6	HSDL-54	11
C6	8	HSDL-81	12	R1	8	HSDL-24	12	8	R6	HSDL-52	12
D6	7	HSDL-51	13	S1	7	HSDL-48	13	7	S6	HSDL-64	13
E6	6	HSDL-53	14	T1	6	HSDL-23	14	6	T6	HSDL-78	14
F6	5	HSDL-77	15	U1	5	HSDL-39	15	5	U6	HSDL-80	15
H6	4	HSDL-99	16	V1	4	HSDL-17	16	4	V6	HSDL-68	16
J6	3	HSDL-97	17	W1	3	HSDL-15	17	3	W6	HSDL-86	17
A7	2	GND-03	18	N2	2	GND-01	18	2	N7	GND-02	18
B7	1	GND-03	19	P2	1	GND-01	19	1	P7	GND-02	19
A8	37	HSDL-72	20	N3	37	HSDL-10	20	37	N8	HSDL-35	20
B8	36	HSDL-94	21	P3	36	HSDL-04	21	36	P8	HSDL-09	21
C8	35	HSDL-92	22	R3	35	HSDL-02	22	35	R8	HSDL-07	22
D8	34	HSDL-91	23	S3	34	HSDL-14	23	34	S8	HSDL-31	23
E8	33	HSDL-71	24	T3	33	HSDL-28	24	33	T8	HSDL-01	24
F8	32	HSDL-73	25	U3	32	HSDL-30	25	32	U8	HSDL-43	25
H8	31	HSDL-87	26	V3	31	HSDL-18	26	31	V8	HSDL-27	26
J8	30	HSDL-63	27	W3	30	HSDL-36	27	30	W8	HSDL-49	27
K8	29	HSDL-65	28	X3	29	HSDL-38	28	29	X8	HSDL-58	28
A9	28	HSDL-83	29	N4	28	HSDL-22	29	28	N9	HSDL-56	29
B9	27	HSDL-55	30	P4	27	HSDL-44	30	27	P9	HSDL-62	30
C9	26	HSDL-57	31	R4	26	HSDL-46	31	26	R9	HSDL-50	31
D9	25	HSDL-79	32	S4	25	HSDL-41	32	25	S9	HSDL-76	32
E9	24	HSDL-95	33	T4	24	HSDL-21	33	24	T9	HSDL-66	33
F9	23	HSDL-93	34	U4	23	HSDL-19	34	23	U9	HSDL-82	34
J9	22	HSDL-75	35	W4	22	HSDL-37	35	22	W9	HSDL-84	35
L9	21	SPARE-2	36	X4	21	SPARE-1	36	21	X9	HSDL-70	36
L7	20	GND-03	37	X2	20	GND-01	37	20	X7	GND-02	37

*3 Center Tap Cables from E.U. to 1st Module.

ACBOA7
ACBON2 ⎤– Quad Connectors in E.U. Logic Gate
ACBON7

**3 Center Tap Cables from a Module to the next Module.

GAJ5
GAL5 ⎤– Connectors - Rack G Storage Module.
GAK5

TABLE 3.2-2

ELECTRONICS UNIT			LEVEL	B450		EXCHANGE 1 or 2	
AAB0A2 E.U. 1 thru 10	WINCHESTER E.U. 1 thru 10			E.U. 1 thru 5 PANEL K		ACB0A2 E.U. 1 ONLY AEB0A2 - E.U. 1 & 6 AEC0A2 - E.U. 2 & 7	
				E.U. 6 thru 10 PANEL N		AED0A2 - E.U. 4 & 9 AECON2 - E.U. 3 & 8 AEDON2 - E.U. 5 & 10	
PIN NO.	SIGNAL	GND PIN		SIGNAL	GND PIN	A2	N2
E4	104	111	REM-POW-ON	104	111	E4	T4
H4	115	121	REM-PWR-OFF	115	121	H4	V4
K3	82	87	EMERG-PWR-OFF	82	87	K3	X3
B4	93	100	PWR-CONT-COMM	93	100	B4	P4
C3	65	60	DFSL/	65	60	C3	R3
H3	75	71	D01L/	75	71	H3	V3
L3	84	79	D02L/	84	79	L3	Y3
C4	95	90	D04L/	95	90	C4	R4
F4	107	102	D08L/	107	102	F4	U4
K4	117	113	D16L/	117	113	K4	X4
D0	7	2	Z01L/	7	2	D0	S0
J0	16	12	Z02L/	16	12	J0	W0
B1	25	21	SW1L	25	21	B1	P1
F1	33	29	SW2L	33	29	F1	U1
L0	23	27	SW4L	23	27	L0	Y0
D1	31	35	SW8L	31	35	D1	S1
J2	57	53	SWAL	57	53	J2	W2
D3	66	62	SWBL	66	62	D3	S3
J3	76	72	SWRL/	76	72	J3	W3
A4	85	80	SCØL/	85	80	A4	N3
C0	5	1	T01L/	5	1	C0	R0
H0	15	11	T02L/	15	11	H0	V0
A1	24	20	T04L/	24	20	A1	N1
E1	32	28	T08L/	32	28	E1	T1
K1	40	36	T10L/	40	36	K1	X1
D2	48	44	T20L/	48	44	D2	S2
H2	56	52	T40L/	56	52	H2	V2
D4	97	92	INXP	97	92	D4	S4
J1	39	43	WDMP	39	43	J1	W1
L4	120	114	SWLL	120	114	L4	Y4
A0	3	8	SR1L	3	8	A0	N0
E0	13	17	SR2L	13	17	E0	T0
K0	22	26	SR4L	22	26	K0	X0
C1	30	34	SR8L	30	34	C1	R1
H1	38	42	SRAL	38	42	H1	V1
L1	46	50	SRBL	46	50	L1	Y1
E2	54	58	SCLP	54	58	E2	T2
A3	63	67	SURL/	63	67	A3	N3
E3	73	77	SARL/	73	77	E3	T3
B0	4	10	CS1L/	4	10	B0	P0
F0	14	18	CS2L/	14	18	F0	U0

TABLE 3.2-3

AAA0A2 PIN	LEVEL	MAINTENANCE PANEL LOCATION	PIN
E0	SR5L-IND/	DAK0 (IND)	2
D0	SR4L-IND/	DAK1 (IND)	2
C0	SR3L-IND/	DAK2 (IND)	2
B0	SR2L-IND/	DAK3 (IND)	2
A0	SR1L-IND/	DAK4 (IND)	2
E2	SC0S	DDJ0 (JT)	1
L1	INXP-01	DDJ2 (JT)	1
F2	ACFF	DDK0 (JT)	1
C2	W0MP-01	DDK2 (JT)	1
H2	ICFF-2A/	DDL0 (JT)	1
D2	BITP-D	DDL2 (JT)	1
E1	SPFF-IND	DCJ0A2 (DRI)	7
K1	BA2F-IND	DCL0A2 (DRI)	7
J1	BA1F-IND	DCM0A2 (DRI)	7
D1	INFF-IND	DCJ1A2 (DRI)	7
F1	ACFF-IND	DCL1A2 (DRI)	7
H1	ICFF-IND	DCM1A2 (DRI)	7
F4	SPFF-MC	DCJ0A2 (DRI)	2
L4	BA2F-MC	DCL0A2 (DRI)	2
K4	BA1F-MC	DCM0A2 (DRI)	2
E4	INFF-MC	DCJ1A2 (DRI)	2
H4	ACFF-MC	DCL1A2 (DRI)	2
J4	ICFF-MC	DCM1A2 (DRI)	2
C1	SUCF-IND	DCN2A2 (DRI)	7
B1	SU1FW-IND	DCP2A2 (DRI)	7
F0	SUBF-IND	DCJ3A2 (DRI)	7
H0	SUAF-IND	DCK3A2 (DRI)	7
J0	SU8F-IND	DCL3A2 (DRI)	7
K0	SU4F-IND	DCM3A2 (DRI)	7
L0	SU2F-IND	DCN3A2 (DRI)	7
A1	SU1FR-IND	DCP3A2 (DRI)	7
D4	SUCF-MC	DCN2A2 (DRI)	2
C4	SU1FW-MC	DCP2A2 (DRI)	2
H3	SUBF-MC	DCJ3A2 (DRI)	2
J3	SUAF-MC	DCK3A2 (DRI)	2
K3	SU8F-MC	DCL3A2 (DRI)	2
L3	SU4F-MC	DCM3A2 (DRI)	2
A4	SU2F-MC	DCN3A2 (DRI)	2
B4	SU1FR-MC	DCP3A2 (DRI)	2

TABLE 3.2-4

AAA0A7 PIN	LEVEL	LOCKOUT PANEL RACK B LOC	UNIT	DISK	PIN
A5	L0SW-01/	BAJ0	1	1	
B5	L0SW-02/	BAJ1	1	2	
C5	L0SW-03/	BAJ2	1	3	
D5	L0SW-04/	BAJ3	1	4	
E5	L0SW-05/	BBJ0	2	1	
F5	L0SW-06/	BBJ1	2	2	
H5	L0SW-07/	BBJ2	2	3	
J5	L0SW-08/	BBJ3	2	4	
K5	L0SW-09/	BCJ0	3	1	3
L5	L0SW-10/	BCJ1	3	2	
A6	L0SW-11/	BCJ2	3	3	
B6	L0SW-12/	BCJ3	3	4	
C6	L0SW-13/	BDJ0	4	1	
D6	L0SW-14/	BDJ1	4	2	
E6	L0SW-15/	BDJ2	4	3	
F6	L0SW-16/	BDJ3	4	4	
H6	L0SW-17/	BEJ0	5	1	
J6	L0SW-18/	BEJ1	5	2	
K6	L0SW-19/	BEJ2	5	3	
L6	L0SW-20/	BEJ3	5	4	
C7	ML0S/	BFJ0	MASTER LOCKOUT		3
D7	SWRL-IND/	CAJ3	INDICATOR		2

TABLE 3.2-5

E.U. RACK E PANEL A	VOLTAGE	MODULE CAJ0
EAR0	-24V	A
EAM0	110VAC-CONV.	B
EAJ0	208VAC-A	D
EAK0	208VAC-B	E
EAN0	NEUTRAL	F
ECL0	SMIL	G
ECK0	SM0L	H

TABLE 3.2-6

ELECTRONICS UNIT SEQUENCE PANEL	VOLTAGE	MODULE RACK A
RACK E PANEL B		AABON2
EBNO	+12V – AB	NO
EBRO	GND – AB	UO
	GND – CD	VO
	GND – E	WO
	GND – F	XO
	GND – G	YO
EBJO	-4.5VDC – AB	N3
	-4.5VDC – CD	P3
	-4.5VDC – E	R3
	-4.5VDC – F	S3
	-4.5VDC – G	T3
EBKO	-20VDC – AB	U3
	-20VDC – CD	V3
EBPO	-12VDC – AB	N4
	-12VDC – CD	P4
	-12VDC – E	R4
	-12VDC – F	S4
	-12VDC – G	T4
EBLO	+20VDC – AB	U4
	+20VDC – CD	V4
	+20VDC – E	W4
	+20VDC – F	X4
	+20VDC – G	Y4

TABLE 3.2-7

AAAON2 PIN	LEVEL	MAINTENANCE PANEL LOCATION	PIN
S3	CLOCK-SWITCH	DBK2	1
X1	CLOCK-SWITCH	DBK2	6
T3	WORD-SP	DBLO	A5,A2
V1	BIT-SP	DBL2	A5,A2
J2	LOCAL-REMOTE	DBKO	5
Y1	CLOCK-SWITCH	DBK2	2
R2	CLOCK-SWITCH	DBK2	5
U3	WORD-SP	DBLO	5
V3	WORD-SP	DBLO	2
U1	BIT-SP	DBL2	B5
T1	BIT-SP	DBL2	B2
RO	-4.5VDC-A-P	DBKO (LOC-REM)	6
TO	-24VDC-A-P	CAJ1 (IND)	2
		CAJ2 (IND)	2
		CAJ3 (IND)	2
SO	+20VDC-A-P	DCN2A2 (DRI)	3
		DCP2A2 (DRI)	3
		DCJ3A2 (DRI)	3
		DCK3A2 (DRI)	3
		DCL3A2 (DRI)	3
		DCM3A2 (DRI)	3
		DCN3A2 (DRI)	3
		DCP3A2 (DRI)	3
		DCJOA2 (DRI)	3
		DCLOA2 (DRI)	3
		DCMOA2 (DRI)	3
		DCJ1A2 (DRI)	3
		DCL1A2 (DRI)	3
		DCM1A2 (DRI)	3
N1	-1.2VDC-A-P	*SEE NOTE	1
JO	+100VDC-A-P	*SEE NOTE	8
		DBMO (BIT-RES)	A2
		DCJ2 (CAP)	K
VO	-100VDC-A-P	*SEE NOTE	5
		DBMO (BIT-RES)	A5
		DBM2 (CLEAR)	A5
WO	-120VDC-A-P	DAKO (IND)	1
		DAK1 (IND)	1
		DAK2 (IND)	1
		DAK3 (IND)	1
		DAK4 (IND)	1
		DDJO (IND)	1
		DDJ2 (IND)	1
		DDKO (IND)	1
		DDK2 (IND)	1
		DDLO (IND)	1
		DDL2 (IND)	1
		*SEE NOTE	4

*LOCATIONS ARE IDENTICAL TO THE +20VAC-A-P LEVEL.

TABLE 3.2-8

AACOA2	VOLTAGE LEVEL	RACK E	
PIN		LOC	PIN
A0	+12VDC-A-J	EBN0	4
A1	-24VDC-A-J	EBM0	4
B1	-24VDC-B-J		
A2	+100VAC-A-J	EEJ0	2
F2	TRSL		5
J2	-24VDC SENSE		13
B3	REM-POW-ON		14
C3	REM-DC-OFF		16
D3	EMERG-PWR-OFF		17
E3	PWR-CONT-COMM		18
F3	-100VDC-A-J		3
A4	-120VDC-A-J		4
E4	DC-SENSE-CONT		15
F4	+20VAC SENSE		10
H4	-20VDC SENSE		11
J4	+12VDC SENSE		8
K4	-12VDC SENSE		9
L4	-4.5VDC SENSE		12

TABLE 3.2-10

ACA0A2	VOLTAGE LEVEL	RACK E	
PIN		LOC	PIN
A3	-4.5V ACDA-L	EBJ0	4
B2	+12V ACDA-Y	EBN0	4
C2	+12V ACDB-L		
D2	+12V ACDB-Y		
A1	-12V ACDA-L	EBP0	4
B1	-12V ACDA-Y		
C1	-12V ACDB-L		
D1	-12V ACDB-Y		
A4	+20V ACDA-L	EBL0	4
B4	+20V ACDA-Y		
C4	+20V ACDB-L		
D4	+20V ACDB-Y		

TABLE 3.2-9

AACON2	VOLTAGE LEVEL	RACK E	
PIN		LOC	PIN
N0	-20VDC-A-J	EBK0	4
N1	-12V AABA-L	EBP0	4
P1	-12V AABA-Y		
R1	-12V AABB-L		
S1	-12V AABB-Y		
V1	-12V AABC-L		
W1	-12V AABC-Y		
N3	-4.5V AABA-L	EBJ0	4
P3	-4.5V AABA-Y		
R3	-4.5V AABB-L		
S3	-4.5V AABB-Y		
V3	-4.5V AABC-L		
W3	-4.5V AABD-L		
N4	+20V AABA-L	EBL0	4
P4	+20V AABA-Y		
R4	+20V AABB-L		
S4	+20V AABB-Y		
V4	+20V AABC-L		
W4	+20V AABC-Y		

3.3   POWER SUPPLIES

CONSTANT VOLTAGE TRANSFORMERS (C.V. TR.)

The C.V. Tr. is a ferroresonant type operating on a nominal line voltage of 208VAC at 60 C.P.S. + 1%. Line voltage regulation, measured at the secondary winding at full load, is + 1.25% for 90% to 110% line voltage range and + 3% over the range of 70% to 90%.

	228.8VAC	110%	
Line	208VAC	100%	+ 1.25%
Voltage	187.2VAC	90%	
	145.6VAC	70%	+ 3%

Load regulation measured at the DC output of the rectifier filter circuit used should not exceed 5%.

C.V. TR. TUNING CAPACITORS

Tuning capacitors for the C.V. Trs. are rated at 660V. Each C.V. Tr. is designed in such a manner that the peak voltage measured across the capacitor does not exceed 590V.

+20V, -20V P.S. - RACK H

Reference Figure 3.3-1.

+20V

        C.V. Tr. T1 and tuning capacitor C4.
        Full wave rectifier: CR1 and CR3.
        Filter network: C1, C2, L2 and a 100 ohm resistor.
        Output: +20 + 1V.
        Ripple: .01V at full load.

-20V

        C.V. Tr. T1 and tuning capacitor C4.
        Full wave rectifier: CR2 and CR4.
        Filter network: C3, C5, L1 and a 200 ohm resistor.
        Output: -20V + 1V.
        Ripple: .01V at full load.

FIGURE 3.3-1
+20V, -20V P.S. - RACK H

NOTE:
CR1 & CR3 ON TB1. ALL OTHER COMPONENTS WITH PIN NUMBERING ON TB2.
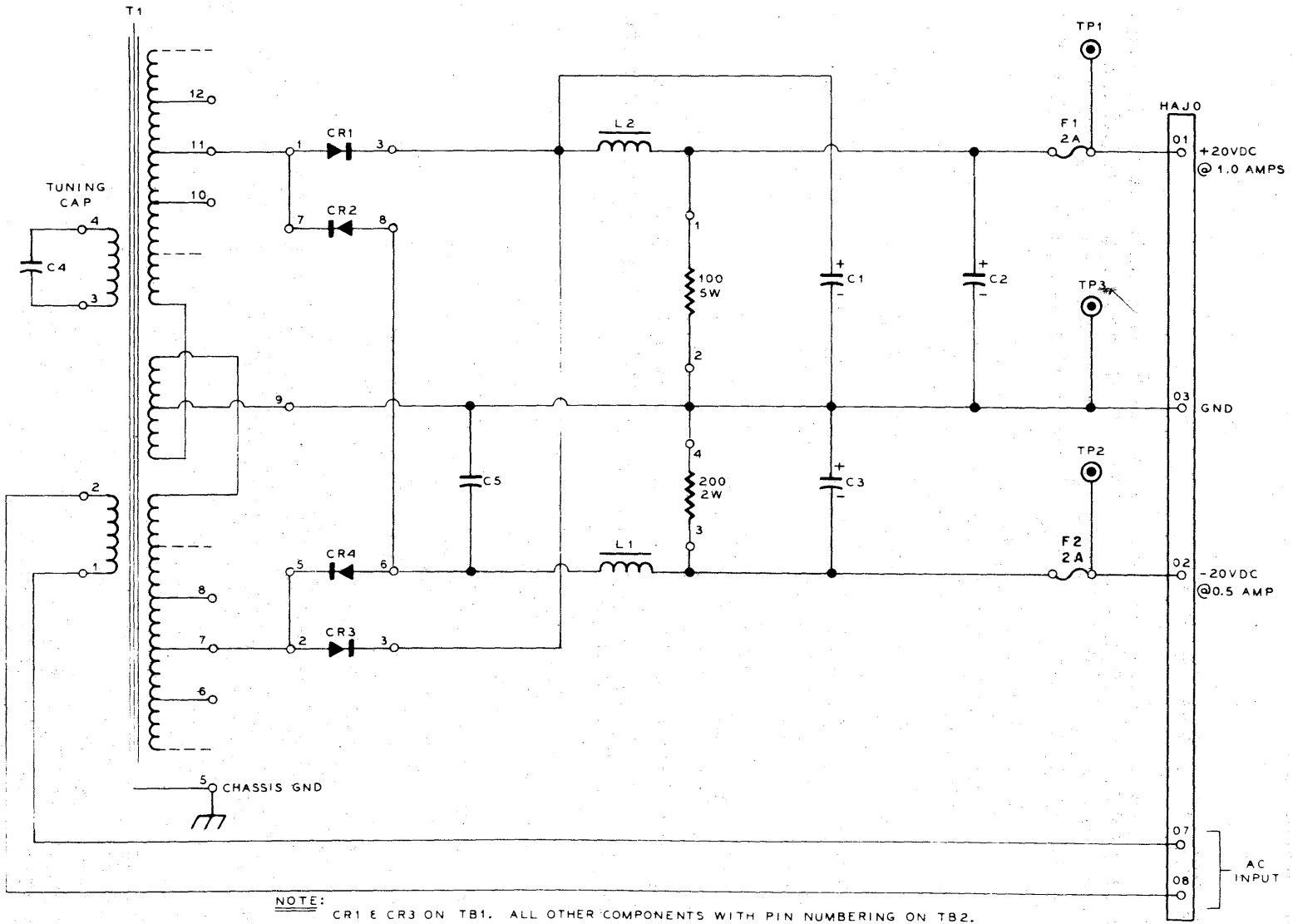
+100V, -100V, -120V AND -24V P.S.

Reference Figure 3.3-2.

-120V

      C.V. Tr. T2 and tuning capacitor C5.
      Full wave rectifier: CR2 and CR4.
      Filter network: 12K ohm resistor and a 10 micro-farad capacitor.
      Output: -120V $\pm$ 6V.

+100V

      C.V. Tr. T2 and tuning capacitor C5.
      Full wave rectifier: CR5 and CR6.
      Filter network: C2 and a 2.5K ohm resistor.
      Output: +100V $\pm$ 5V.

-100V

      C.V. Tr. T2 and tuning capacitor C5.
      Full wave rectifier: CR7 and CR8.
      Filter network: C3 and a 2.5K ohm resistor.
      Output: -100V $\pm$ 5V.

-24V

      C.V. Tr. T1 and tuning capacitor C4.
      Full wave rectifier: CR1 and CR3.
      Filter network: C1 and R1 (25 ohm).
      Output: -24V $\pm$ 1.2V.

+12V, -12V AND -4.5V P.S.

Reference Figure 3.3-3.

+12V

      C.V. Tr. T1 and tuning capacitor C8.
      Full wave rectifier: CR2 and CR4.
      Filter network: C7 and a 240 ohm resistor.
      Output: +12V $\pm$ .5V.

-12V

      C.V. Tr. T1 and tuning capacitor C8.
      Full wave rectifier: CR1 and CR3.
      Filter network: R10, C3, C4, C5 and C6.
      Output: -12V $\pm$ .5V.

FIGURE 3.3-2
+100V, -100V, -120V AND -24V P.S.
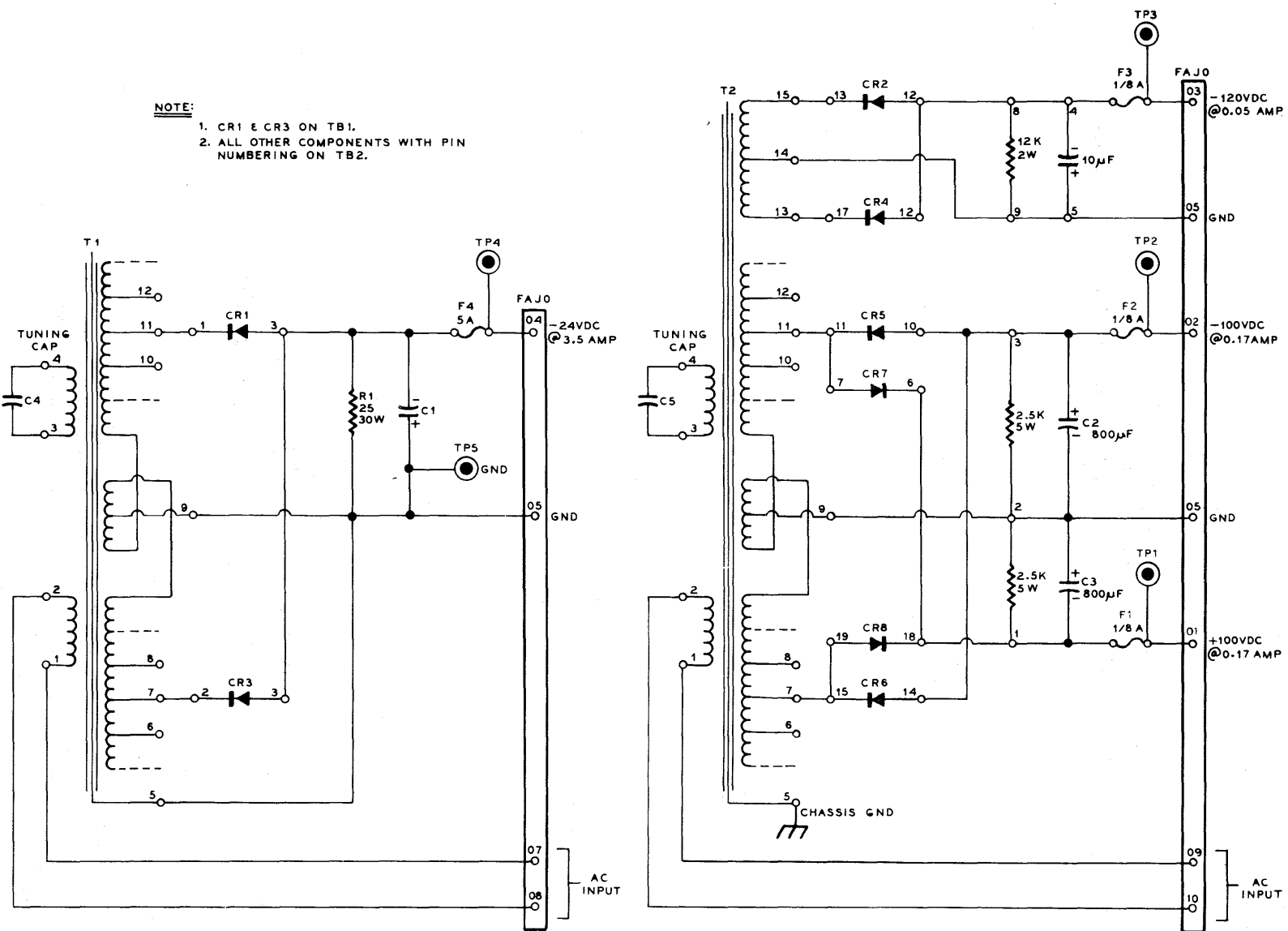
-4.5V REGULATOR

The -4.5V regulator is a shunt type consisting of a 5.3V Zener (1N705A); power diode IN3208; transistors 2N1557, 2N1172, 2N444A and 2N1193; and resistors and capacitors associated with the circuit.

The 2N444A acts as a sensing transistor to fluctuations in the -12V felt at its base through the action of the 2N1193, and the -4.5 tied directly to its emitter. A fluctuation in either voltage is amplified through the 2N1172 which in turn affects the conduction of the 2N1557 and compensates the -4.5V output. The 1N705A is used to keep the base of 2N1193 at a constant voltage.

Output: -4.5V $\pm$ .2V.
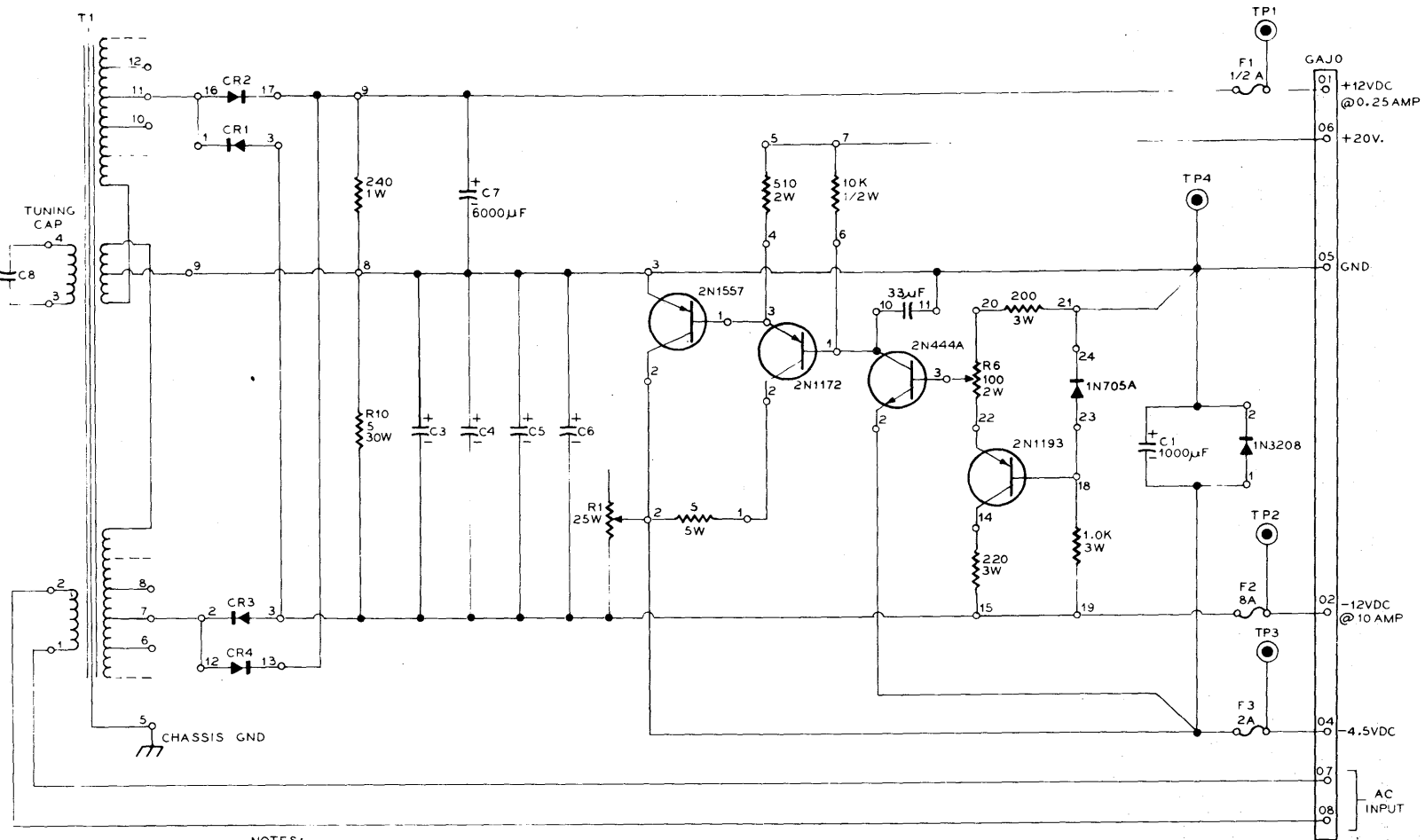
FIGURE 3.3-3
+12V, -12V AND -4.5V P.S.

T1

TP1

F1
1/2 A

GAJO

01 +12VDC
@ 0.25 AMP

06 +20V.

12

11

10

16 CR2 17

1 CR1 3

9

240
1W

C7
6000 µF

5   7

510
2W

10K
1/2W

TP4

TUNING
CAP

4

C8

3

9

8

4   6

3

2N1557

33 µF

20 200 21
     3W

05 GND

10 || 11

1

2N444A

24

R6
100
2W

1N705A

C1
1000µF

2

1N3208

1

R10
5
30W

C3   C4   C5   C6

2

1

2

2

22

23

2N1193

18

TP2

R1
25W

2   5   1
       5W

14

220
3W

1.0K
3W

F2
8A

02 -12VDC
@ 10 AMP

TP3

2

8

7 2 CR3 3

15

19

6

12 CR4 13

F3
2A

1

5 CHASSIS GND

04 -4.5VDC

07

08

AC
INPUT

NOTES:
1. CR1 & CR3 ON TB1.
2. 1N3208 ON TB2.
3. 2N1557 ON TB3.
4. 2N1172 ON TB4.
5. ALL OTHER COMPONENTS WITH NO PIN NOS. ARE ON TB5.

2N1172

3.4 ADDRESSING

Address decoding accomplishes the following:

1. Selects one of five Modules.

2. Selects one of four disks in a Module.

3. Selects the disk face.

4. Selects one of three zones on a disk face.

5. Selects one of fifty information heads in a zone.

Reference Figure 3.4-1.

MODULE SELECTION

The Module is selected by Disk Select Levels D04L/, D08L/ and D16L/.
A binary configuration of zero selects Module 1, one selects Module 2
.....four selects Module 5.

DISK SELECTION

The Disk is selected by Disk Levels D01L/ and D02L/. A binary config-
uration of zero selects Disk 1.....three selects Disk 4.

DISK FACE SELECTION

The disk face is selected by DFSL/ and DFSS (DFSL switched). The
state of DFSL/ is determined by address decoding in the D.F.C.U.

ZONE SELECTION

The Zone is selected by the levels Z01L/ and Z02L. A binary config-
uration of zero selects Zone 1, one selects Zone 2 and two selects
Zone 3.

INFORMATION HEAD SELECTION

The information head is selected by the combination of DFSL/ and the
track levels. These levels make up the Head Select Units and Tens
Levels which are gated into the Head Select Drivers to produce
HSDD 00→99.
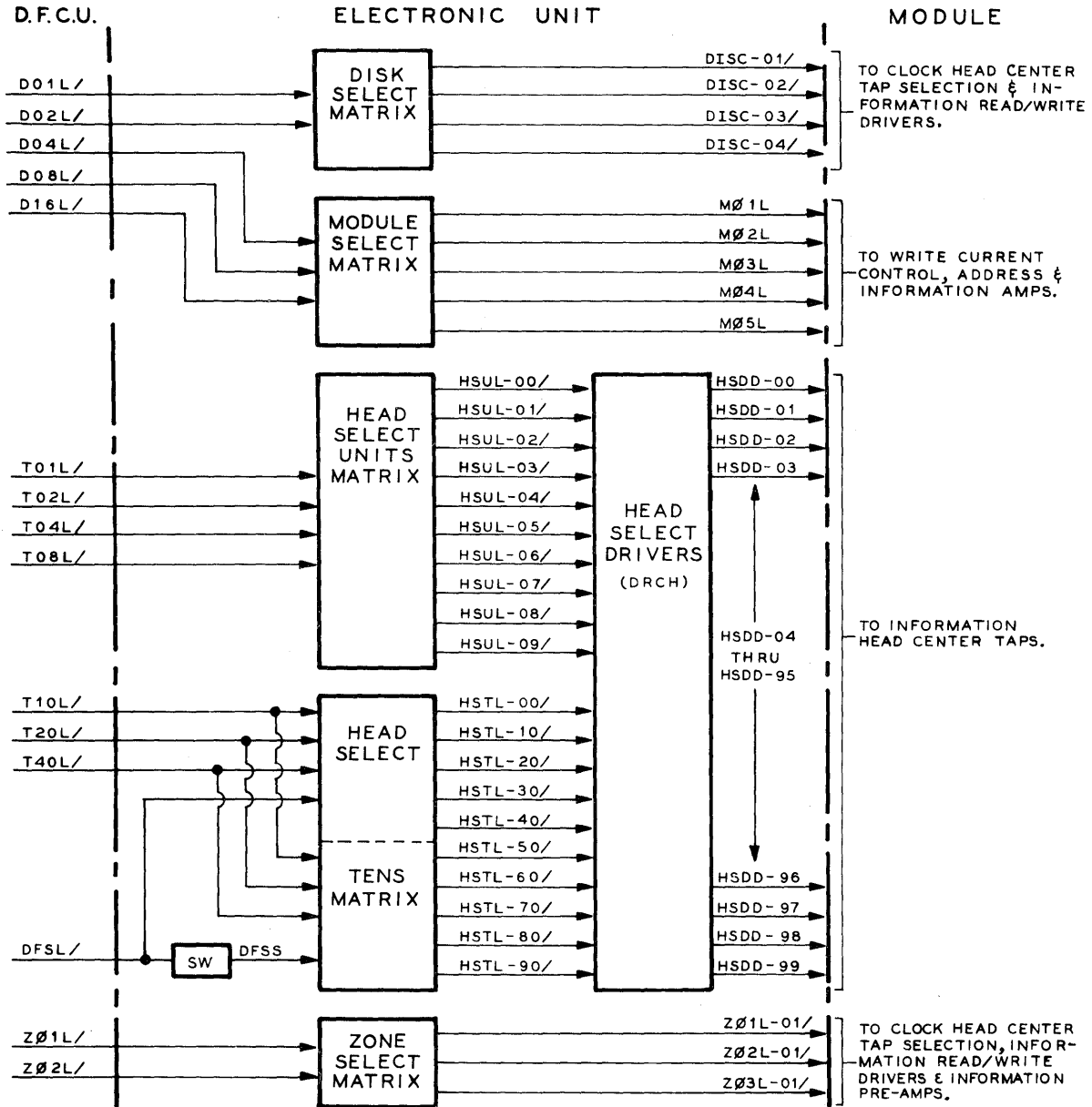
FIGURE 3.4-1
ADDRESS DECODING

3.5   CLOCKING

There are two basic clock pulses used in the E.U. which are received from the module being addressed. Each face of each disk has two clock tracks for each of the three zones on that face. One track output is used to generate BITL (Bit Level). The other track will generate a pulse at Word Mark time and also address information. Word Mark Pulses (WØMPs) and address information are transferred to the E.U. on the ASRL lines (Address Read Level). From BITL and ASRL the E.U. will generate the following clock pulses: INXP, WØMP, BITP, BCLP, BUDP and DBIT.

INXP

Index Pulse is generated once per revolution of the disk. It is the basic reference point of each disk face. INXP is generated in the E.U. when the beginning of the dead space is determined by the absence of BCLPs. The absence of bit pulses will permit IXHM (Index Holdover Multi) to time out after 3 microseconds, generating two pulses by use of a multi and a pulse compressor. Refer to Figure 3.5-1. INXP-01, 400 nanoseconds and INXP-02, 150 nanoseconds. INXP-01 is used to enable a driver to send INXP to the D.F.C.U.
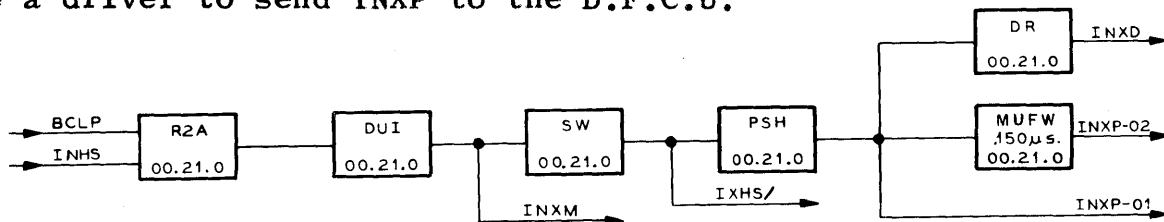
FIGURE 3.5-1
INXP CIRCUIT

WØMP

A Word Mark Pulse is generated to indicate the beginning of a word. Refer to Figure 3.5-2. A WØMP is generated in Local with the Clock Switch off by depressing the WØMP single pulse button. The normal enabling logic will come from the ASRL lines. WØHF/ is the controlling logic which inhibits the generation of WØMPs from address information. The pulse width of WØMP is 150 nanoseconds.

BITP

Refer to Figure 3.5-2. Bit Pulse is a 150 nanosecond pulse and is generated in the E.U. by BITL from a selected S.U. The delay between BITL and BITP is necessary to prevent a marginal strobing condition during active read time in zone three.

The pulse rate of BITP will be determined by the selected zone of the addressed S.U. The bit frequency for zone one is 1.043 MC; zone two, 1.380 MC; and zone three, 1.884 MC.

BCLP

Bit Clock Pulse is a 150 nanoseconds clock pulse occurring at the bit time or delayed bit time depending on gating. Refer to Figure 3.5-3. The gating for BCLP will enable an output for Read, Write, Inactive Word and Word Mark Times.
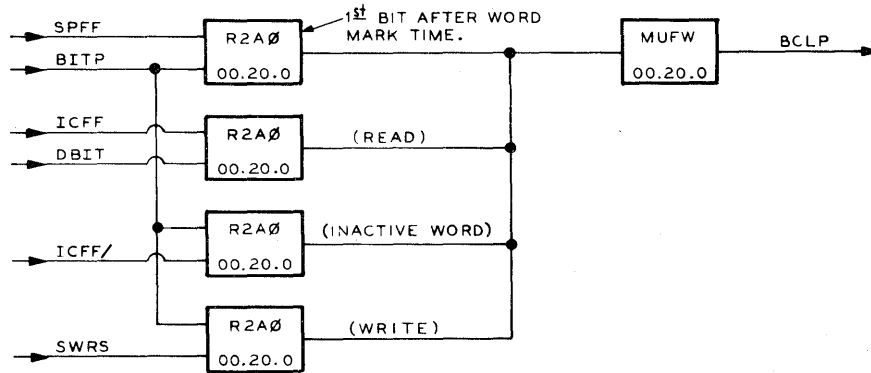
FIGURE 3.5-3
BCLP CIRCUIT

BUDP

Refer to Figure 3.5-2. The Bit Undelayed Pulse is a 250 nanosecond pulse which is generated in the E.U. by BITL from a selected S.U. A BUDP will produce a DBIT during the active word of a read operation.

DBIT

Delayed Bit Time is a BUDP delayed 675 nanoseconds and generates BCLP which is used to clock the SUnFs during the active word of a read operation. DBIT is a 150 nanosecond pulse. Refer to Figure 3.5-4. The delay is necessary for correct strobing of information into the S.U. register.

FIGURE 3.5-4
DBIT CIRCUIT
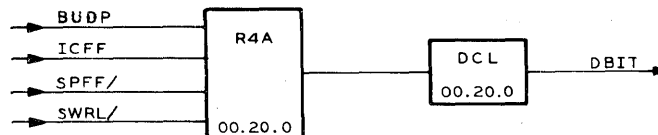
FIGURE 3.5-2
WØMP & BITP CIRCUITRY

MULTI AJ

The Multi AJ is used to provide both an undelayed bit pulse and a 250 nanosecond delayed bit pulse. BUDP (BIT UNDELAYED) is 250 nanoseconds in width and becomes true at BITL time. BITP (BIT PULSE) is 150 nano-seconds wide, delayed 250 nanoseconds from BITL. Refer to Figure 3.5-5.

With a false input, Q1 and Q3 are on; Q2 is cutoff. Both Out 1 and Out 2 are false. Base drive is supplied to Q2 with a true input at CR7. The positive change across C1 removes base drive from Q1. Q1 remains off for the RC time constant of C1, R26 and R27. Out 1, BUDP, is true for 250 nanoseconds as adjusted by R27. With the turn on of Q1, a positive charge across C19 removes base drive from Q3. Out 2, BITP, is true, clamped to -4.5V by CR13. Q3 remains off for 150 nano-seconds, the RC time constant of C19 and R18.
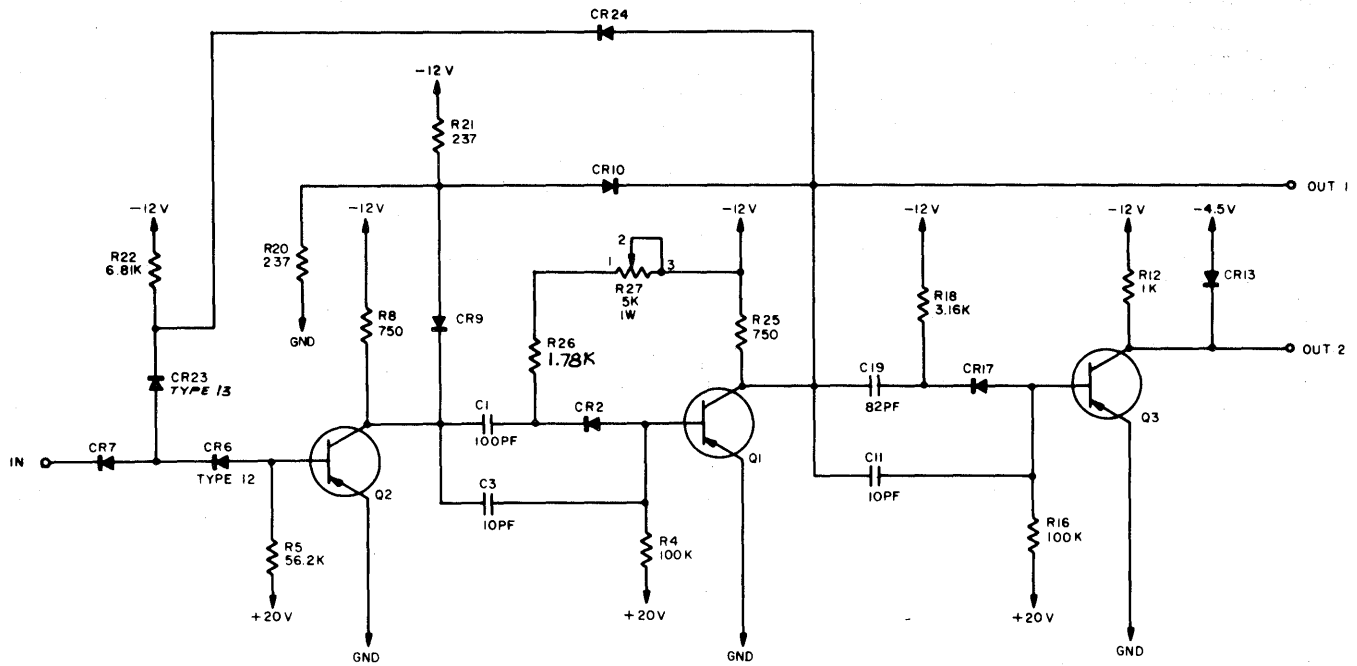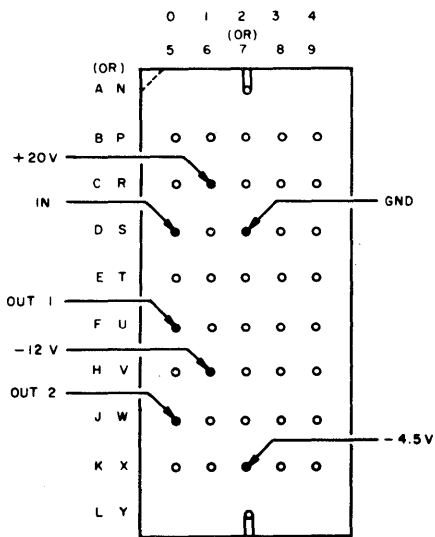
4. ALL CAPACITORS ARE 5%, 100V.
3. ALL TRANSISTORS ARE TYPE L.
2. ALL DIODES ARE TYPE II.
1. ALL RESISTORS ARE 2%, 1/2 W.

NOTE: UNLESS OTHERWISE SPECIFIED

FIGURE 3.5-5
MULTI AJ

3.6 READY CIRCUITS

The Ready Circuit in the E.U. is shown in Figure 3.6-1. The logic to produce SURL/ is as follows:

-∅-SURL/

-I-REMS·HFML-01·HFML-02·HFML-03·HFML-04·HFML-05·CCIL-A

The three requirements are that the LOCAL/REMOTE switch be in REMOTE, the heads must be flying and the CLOCK switch must be ON. A false level SURL/ to the D.F.C.U. indicates that the E.U. and its associated S.U.'s are ready.
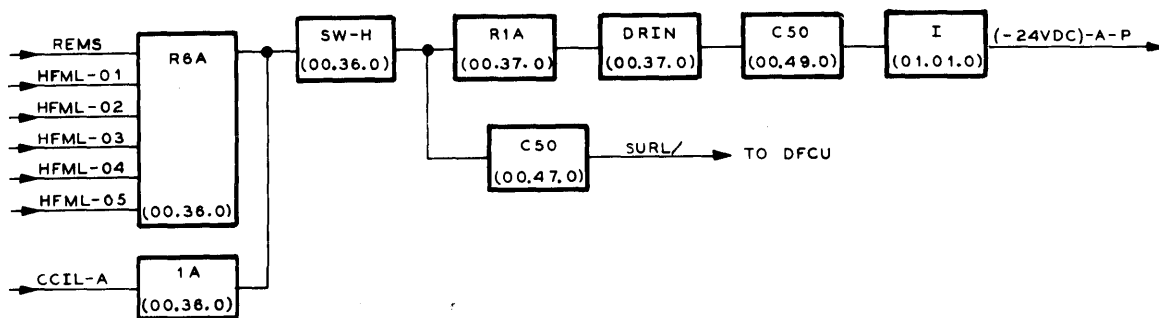
FIGURE 3.6-1
READY CIRCUIT LOGIC

3.7   WRITE LOCKOUT

The Write Lockout Panel on the E.U. has one MASTER and 20 individual
DISK LOCKOUT switches. Any or all of the possible 20 disks associated
with the S.U. may be disabled as far as writing is concerned. The
Lockout switches protect master files or other permanent data. In
the 96 option the disks should be locked out two at a time since
segment addresses pertain to pairs of disks.

Refer to Figure 3.7-1 for the logic associated with the Lockout
switches. With the MASTER LOCKOUT and DISK LOCKOUT switches as
shown, SWLL will be false. If the signal SWRL/ is also false, a
write operation will be initiated by WRSD. When the MASTER LOCKOUT
switch is thrown, SWLL is true holding WRSD/ true thus inhibiting
writing regardless of SWRL/. If a locked out disk is addressed, SWLL
will be true and will stay true as long as that disk is being
addressed.

The two red indicators on the Control Panel in the E.U. show the
condition of the MASTER LOCKOUT switch and any DISK LOCKOUT switch.
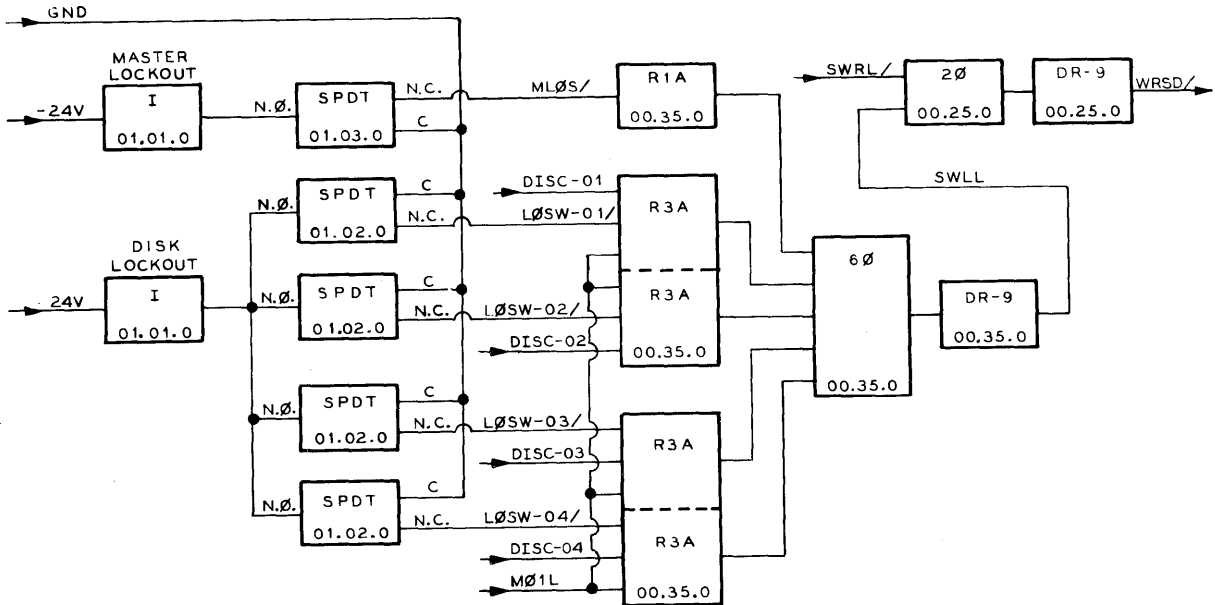
FIGURE 3.7-1
WRITE LOCKOUT LOGIC

3.8 READ SIGNAL AUTOMATIC STEP GAIN CONTROL

An automatic "normal/hi" gain control is part of the information read circuitry. Each module has its own amplitude sensing. The gain is selected by a level generated in the E.U. as a result of feed-back from the module. Refer to the block diagram in Figure 3.8-1 during the following description.

The Storage Module components used in the gain control circuitry are the Information Sense Amp, Clipper and Gain Threshold Detector. The E.U. has the Threshold Store Flip-flop (TSRF), Gain Select Flip-flop (GSLF), Gain Latch Flip-flop (GLAF), and a switch to supply the output level (GSSL).

The gain of the Information Sense Amp is controlled by the true or false state of the Gain Select Level, GSSL. Normal sense amp gain is selected until GSSL goes false to select high gain. The GC Sense Amp "0" and "1" outputs are sent to the GC Clipper package. One output from the Clipper is routed to the Gain Threshold Detector. The Threshold Detector produces a true output 150 nanosecond pulse at bit rate if the signal level received from the Clipper does not fall below 1.2 volts, zero to peak. The TD pulse is sent through the logic cable to the E.U. where the pulse is ANDED with SPFF/ and MØnL for the same module. The absence of TD pulses will cause a switch to high gain.

The E.U. is constantly monitoring the TD output from the particular module being selected by the Control Unit. (During System Idle, Module 1, Track 00, Zone 1 is selected.)

The correct gain for a track is selected before the required record is read from that track. Whichever gain is selected is held until there is a change of track or the end of the Read operation occurs. The Gain Latch Flip-flop, GLAF, controls this sequence. GLAF cannot be turned on except at segment address time. Once on, it latches GSLF to hold the gain condition selected. GSLF is ordinarily latched in the "ON" state during Read which indicates normal gain is adequate. If high gain is required, GSLF must be latched off. The Action FF, ACFF, prevents GLAF from being reset until a track change is made or the Read operation is terminated. For any track, the gain is selected by the signal amplitude in the word preceding the address of the segment desired. Each time a new track is selected, the gain must be re-checked. In a crossover to a new track, ACFF will be set by the WØMP after dead space. In that case, gain must be selected from the signal amplitude in the last word of MS1. The "worst case" time available for completing a change in gain selection occurs during a track crossover in Zone 3. A change at that time must be completed in approximately 80 microseconds in order for the Sense Amp to be in the proper condition to read the first word after dead space. There is ample time, however, since the recovery time of the Sense Amp after a gain selection change is only 20 - 30 microseconds.

The following step-by-step descriptions are given as examples of the gain control operation during System Idle, Read, and Read with a track crossover. In each case, arbitrary assumptions are made as to the signal levels of the tracks selected.

SYSTEM IDLING (CONTROL SEC = 00)

This example describes how the gain circuitry would try to select high gain at segment address time if Track 00, Zone 1 of Module 1 had a signal level below the threshold. Between segment addresses, the gain level would return to normal because the circuit could not latch.

Assume the disk is being read somewhere in the middle of a Zone 1 segment. TD1L is false.

TSRF has been reset by SPFF.

GSLF is set to 0 due to TSRF being off.

One leg of the input gate to GSSL SW is true from GSLF/, but GLAF is false, keeping GSSL true.

GSSL being true selects normal gain.

An address is encountered in the address track and a complete address character is stacked up in the S.U. register making CBAS true.

GLAF is set with CBAS.

GSLF is latched in the off state with GLAF/.

Both GLAF and GSLF/ are true at the input gate to GSSL SW making GSSL false to select high gain.

Sense Amp gain goes high 20 - 30 microseconds after GSSL goes false.

TD1L will then go true for 150 nanoseconds with each information bit.

BA counter reaches full address count, is reset by following SPFF since INFF is off, tallies next address since addresses are recorded back to back, and finally is reset again by the following SPFF. TSRF goes true during this time, but has no effect on GSLF due to the latch gate.

GLAF is reset by next SPFF following BA = 0 since ACFF is off.

GLAF being false causes GSSL to go true and also releases the latch on GSLF.

GSSL true allows the gain to return to normal and, after the 20 - 30 microsecond Sense Amp recovery, TD1L goes false again since the disk is idling on a low signal amplitude track.

This cycle will repeat each time segment addresses are encountered.
The gain will not remain latched in the high state beyond segment
address time while the system is idling since ACFF is off.

READ OPERATION (CONTROL SEC = 10, 11, 13 AND 14)

This example describes how the gain circuitry would latch in normal
gain if the track being addressed had normal signal amplitude.

Assume the disk is being read somewhere between segment addresses
searching for coincidence.

TDnL is true at bit time with normal signal amplitude.

TSRF is set by TDnL.

GSLF is turned on at the next SPFF. (This same SPFF resets TSRF, but
TDnL turns TSRF on immediately following SPFF/.)

When a segment address is encountered, GLAF is set with CBAS.

GSLF is latched on by false from GLAF/.

If the address did not compare, ACFF remains off and SPFF resets the
BA counter.

The interlaced segment address would be read immediately after and,
if it did not compare, ACFF remains off and SPFF resets the BA counter.

GLAF is reset by the next SPFF following BA = 0 since ACFF is off.
This cycle will repeat until address coincidence is found.

Control SEC = 15, 20 and 21 - coincidence found, read (n) segments.

GLAF is set with CBAS.

GSLF is latched on and the GSSL output remains true.

ACFF will go on with SCØL and prevent the reset of GLAF until the end
of the Read operation.

ACFF will go off at the end of the last segment of the Read.

READ OPERATION (CONTINUED)

This example describes how the gain circuitry would select high gain
after a track change if the new track addressed had a signal level
below the threshold.

Control SEC = 23, 22 and 20 - end of second revolution with N ≠ 0.

BA counter = 6 since the address for Maintenance Segment 2 is the last address read at the end of the second revolution.

A simulated index pulse (INXP) is generated due to BA counter = 6 with INFF and ACFF on.

BA counter is reset by the simulated INXP.

ACFF is reset by the simulated INXP.

GLAF is reset by the next SPFF following BA = 0 and ACFF/.

GLAF/ being true releases the latch on GSLF. The track selection change is made while reading the maintenance segments.

TDnL goes false since the signal amplitude of the track now selected is below the Threshold.

TSRF is false after reset by SPFF.

GSLF is turned off by the following SPFF. Nothing further happens until Maintenance Segment 3 address is encountered in the address track of the new zone/disk.

GLAF goes on with CBAS to latch GSLF.

GSSL goes false due to true inputs from GSLF/ and GLAF. Approximately 20 - 30 microseconds after GSSL goes false, Sense Amp gain goes high.

TSRF resets at the next SPFF, but GSLF is latched as GLAF cannot be reset.

BA counter is reset by SPFF when BA = 3 because ACFF is off; when the address for the next active segment is read during the next word time, the BA counter tallies up to 3. TSRF goes true during this time but has no effect on GSLF due to the latch gate. The dead space is encountered at the end of the segment address word time and INXP resets the BA counter and INFF.

The first WØMP after dead space turns on ACFF and ICFF.

ACFF on prevents SPFFs from reseting GLAF.

The Read operation continues until the last segment has been read at which time SEC is set to 00.

SCØL is lost and ACFF goes false.

GLAF will reset with the next SPFF following ACFF/.

With GLAF false, GSSL is true, selecting normal gain.

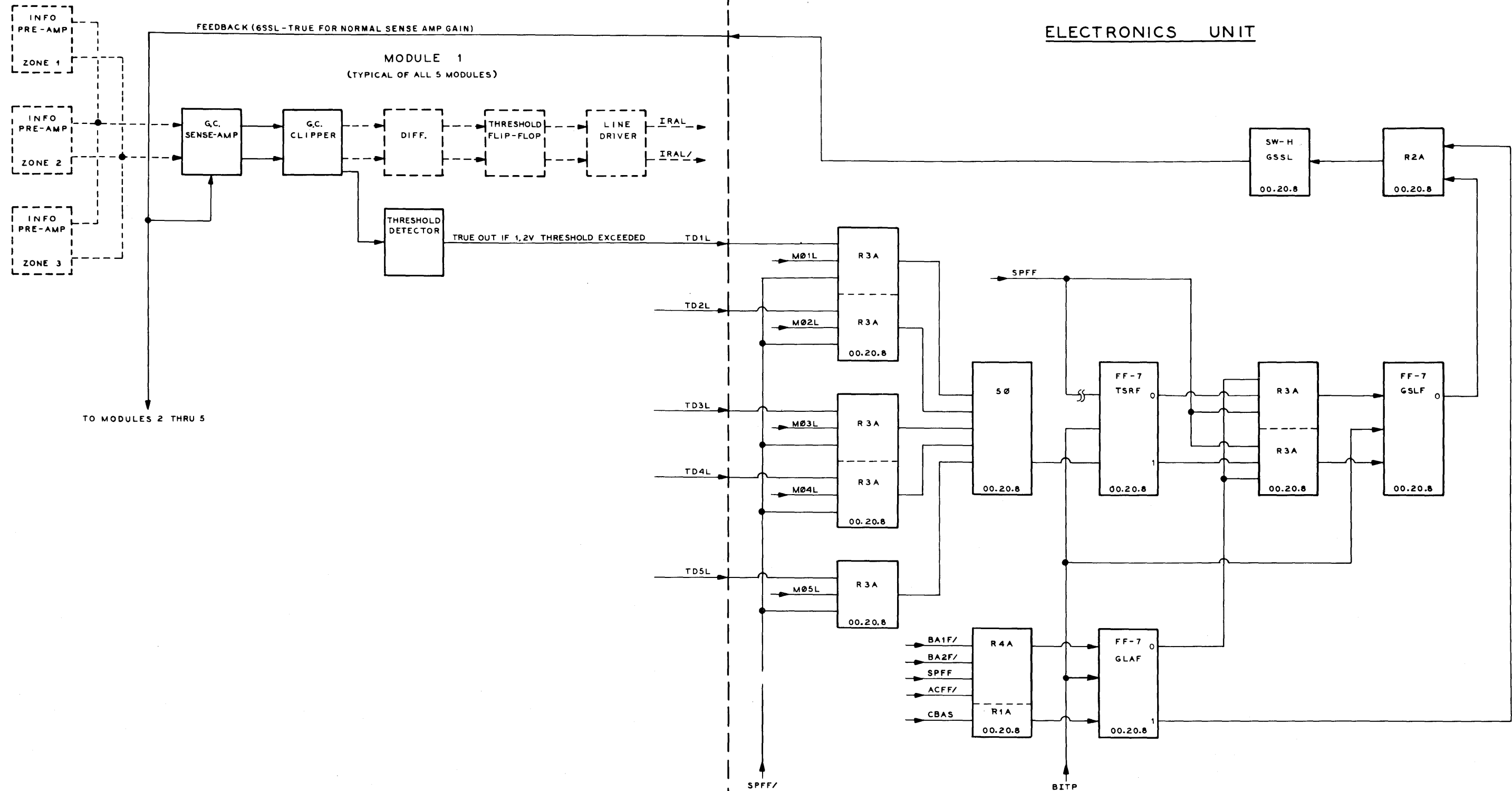The system goes into an idle condition addressing Module 1, Zone 1, Track 00.

FIGURE 3.8-1
AUTOMATIC STEP GAIN CONTROL

INDEX – SECTION IV

4   FUNCTIONAL DESCRIPTION – MECHANICAL

4.1 AIR SYSTEM

The Disk File Storage Modules require a sealed, filtered, compressed
air system to actuate the heads. The Electronics Unit contains the
air source and is capable of supplying up to five Modules with
filtered air regulated to 50 psi. "T" connections, with snap-in air
fittings, are provided for each Module along the output air trunk line
from the E.U.

Refer to Figure 4.1-1. The air supply components are located in the
front of the E.U. A 1/4 H.P., 208V, single phase motor drives the
compressor directly. The compressor is an "oil-less", single stage
(one cylinder) type. Its piston has graphite rings to eliminate the
need for oil base lubricants which would tend to contaminate the air.
All motor and compressor bearings are permanently lubricated and
sealed. An unloader valve is provided to release cylinder pressure
during idle periods and a check valve in the output manifold prevents
line pressure from backing up into the cylinder. A disposable filter-
muffler cleans and silences the air intake.

The output line from the compressor is connected to a tank where the
air supply for the Modules is maintained at 60 - 80 psi. There is a
sediment bowl assembly at the bottom of the tank to collect moisture
condensation. A pressure sensitive switch connected to the bowl
assembly monitors the tank pressure. This switch starts the compres-
sor motor if tank pressure drops to 60 psi and stops the motor when
the pressure rises to 80 psi.

The output air line leaves the top of the tank through a pressure
switch. This is a safety device which de-energizes the Storage Mod-
ule Air Solenoids by removing -24V if an air supply malfunction allows
the tank pressure to drop below 50 psi.

The output line goes to another 10 micron, bowl-type filter. The
filtered air then passes through a pressure gauge which registers
the tank pressure. Finally, the air goes through the output regulator.
This adjustable regulator maintains 50 psi in the Storage Module air
trunk line. The Maintenance Panel has a pressure gauge which monitors
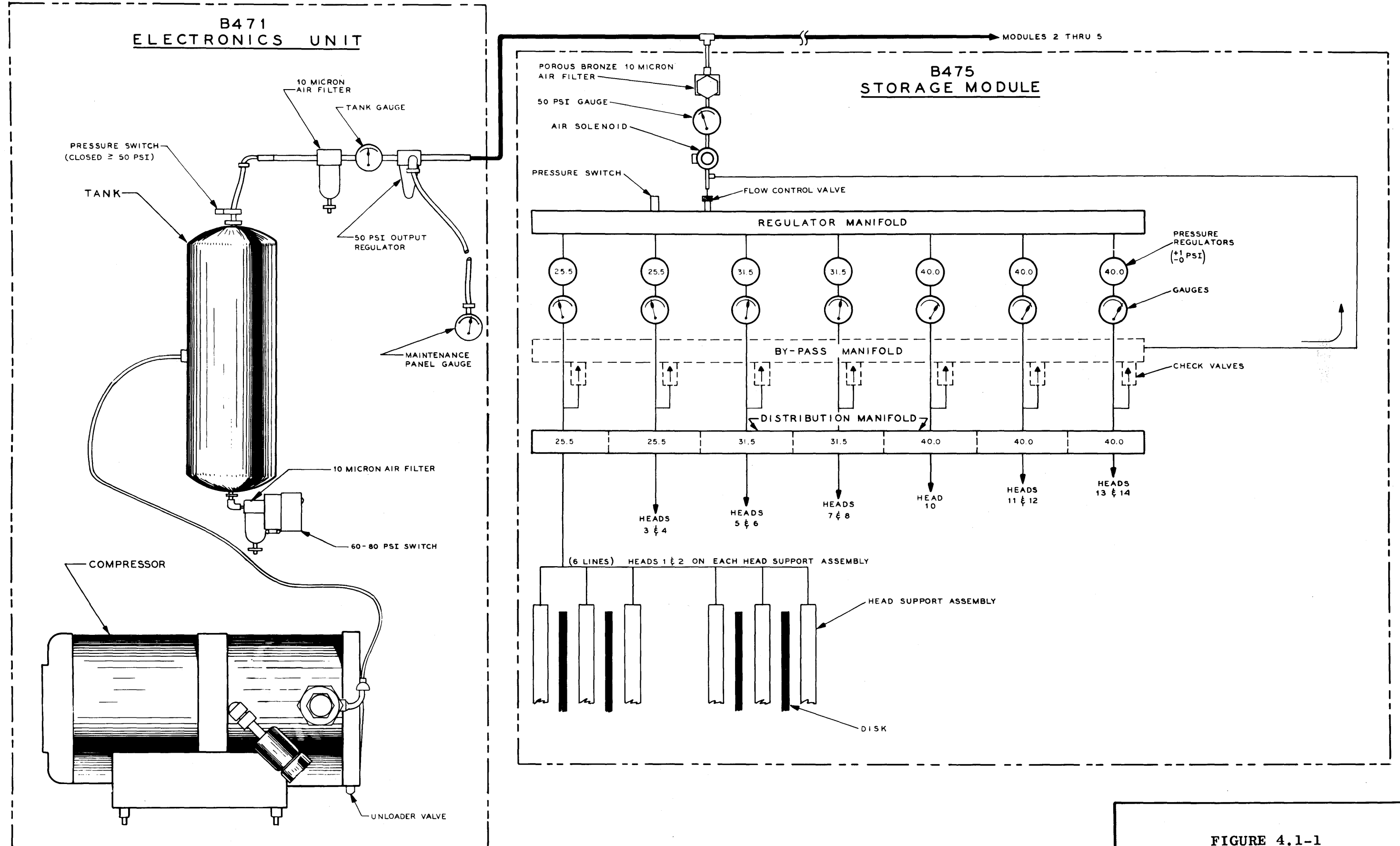the regulator output to display the air trunk line pressure.

B471
ELECTRONICS UNIT

10 MICRON
AIR FILTER

TANK GAUGE

PRESSURE SWITCH
(CLOSED ≥ 50 PSI)

TANK

50 PSI OUTPUT
REGULATOR

MAINTENANCE
PANEL GAUGE

10 MICRON AIR FILTER

60-80 PSI SWITCH

COMPRESSOR

UNLOADER VALVE

MODULES 2 THRU 5

POROUS BRONZE 10 MICRON
AIR FILTER

B475
STORAGE MODULE

50 PSI GAUGE

AIR SOLENOID

PRESSURE SWITCH

FLOW CONTROL VALVE

REGULATOR MANIFOLD

PRESSURE
REGULATORS
($^{+1}_{-0}$ PSI)

| 25.5 | 25.5 | 31.5 | 31.5 | 40.0 | 40.0 | 40.0 |

GAUGES

BY-PASS MANIFOLD

CHECK VALVES

DISTRIBUTION MANIFOLD

| 25.5 | 25.5 | 31.5 | 31.5 | 40.0 | 40.0 | 40.0 |

HEADS
3 & 4

HEADS
5 & 6

HEADS
7 & 8

HEAD
10

HEADS
11 & 12

HEADS
13 & 14

(6 LINES) HEADS 1 & 2 ON EACH HEAD SUPPORT ASSEMBLY

HEAD SUPPORT ASSEMBLY

DISK

FIGURE 4.1-1
AIR SYSTEM FUNCTIONAL DIAGRAM

INDEX - SECTION V

5 ASSEMBLY - DISASSEMBLY - ADJUSTMENTS

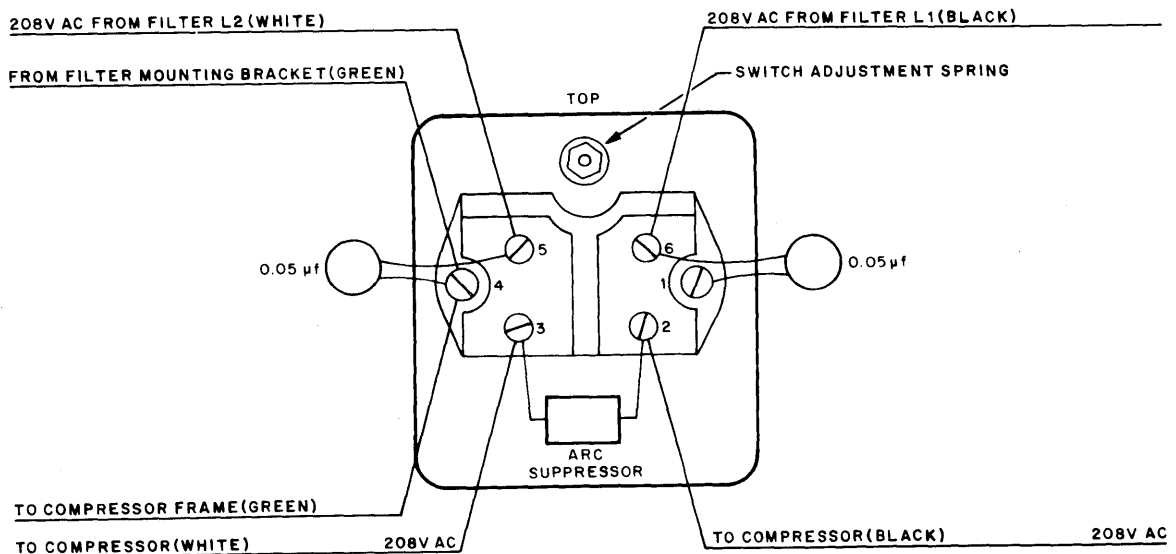## 5.1 60-80 AIR SWITCH - REMOVAL AND REPLACEMENT

The following procedure should be followed for the removal and re-placement of the 60 - 80 Air Switch.

<u>CAUTION</u>

Refer to Section 5.7 of this Man-ual when working on the Air System.

Removal:

1. Turn off the Electronic Unit DC and AC power.

2. Turn off the 70 amp main AC Circuit Breaker.

3. Bleed off the Tank pressure.

4. Remove the cover from the 60 - 80 Switch.

5. Remove the leads, capacitors, and arc suppressor from the switch terminals. Refer to Figure 5.1-1.

208V AC FROM FILTER L2(WHITE)   208V AC FROM FILTER L1(BLACK)

FROM FILTER MOUNTING BRACKET(GREEN)   SWITCH ADJUSTMENT SPRING

TOP

0.05 μf   0.05 μf

ARC SUPPRESSOR

TO COMPRESSOR FRAME(GREEN)

TO COMPRESSOR(WHITE)   208V AC   TO COMPRESSOR(BLACK)   208V AC

FIGURE 5.1-1
60 - 80 SWITCH CONNECTIONS

6. Remove the 60 - 80 Switch from the Air System plumbing. Use a 3/4" wrench to turn the Switch Assembly and a 9/16" wrench to prevent the pipe nipple from turning. Do <u>NOT</u> remove the nipple.

Replacement:

1. Ensure the 70 amp main AC Circuit Breaker is off.

2. Install the 60 - 80 Switch on the pipe coming from the Tank Sed-iment Bowl. Use a 9/16" wrench to hold the nipple and a 3/4" wrench to tighten the Switch Assembly. Ensure the Switch is oriented with the Adjustment Spring at the top after the Assembly

has been tightened.

3. Connect the leads, capacitors, and arc suppressor to the switch terminals. Refer to Figure 5.1-1.

4. Install the cover on the Switch Assembly.

5. Turn the 70 amp AC Circuit Breaker on. The Compressor should go on, pressurize the Tank, and go off when the pressure reaches 80 PSI.

6. Ensure there is no air leak at the pipe connection made in Step 2.

7. Refer to Section 5.21 of this Manual for the 60 - 80 Switch check and adjustment procedure.

8. Restore the Electronic Unit to normal operation.

5.3 POWER SUPPLIES – REMOVAL AND REPLACEMENT

Power supply assemblies, Racks F, G and H, are removed and replaced in the following manner.

REMOVAL

1. Cycle down all power and open the 15, 50 and 70 amp AC circuit breakers.

2. Unscrew the two knurled bolts which secure the power supply assembly to the frame.

3. Slide assembly out until the terminal board on the base of the assembly is clear of the frame. Slack is provided in the power supply harness for approximately seven inches of movement.

4. Remove screws which secure harness to terminal board.

5. Remove and carry assembly by handles provided.

REPLACEMENT

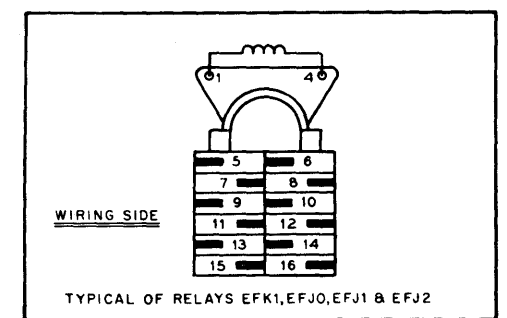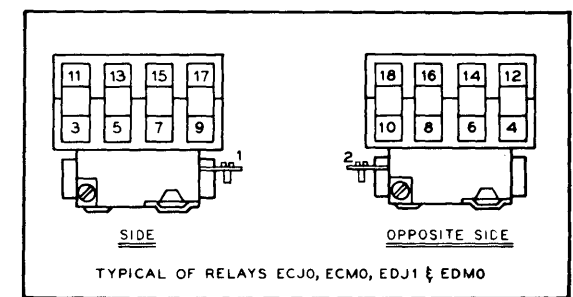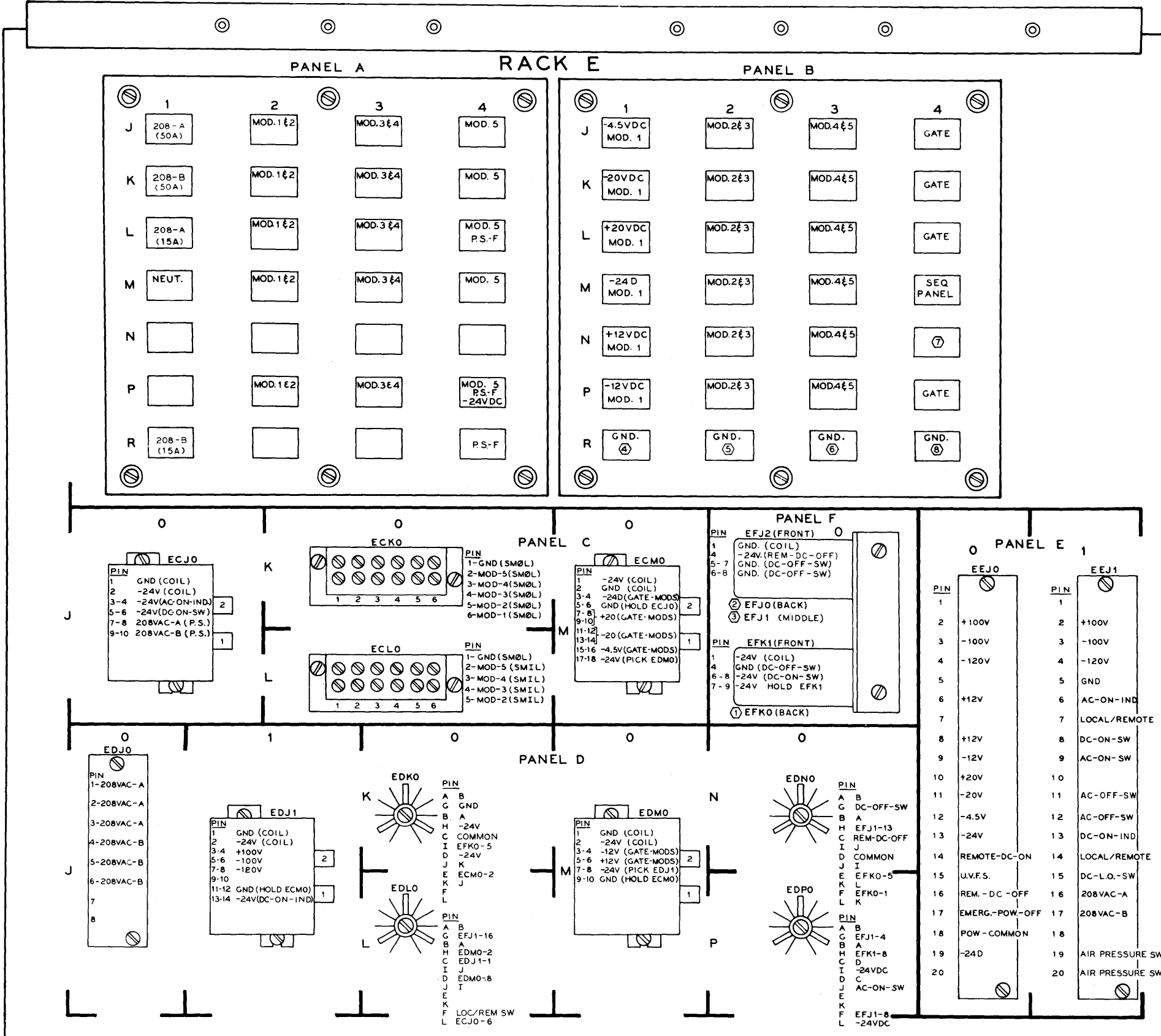To replace an assembly, reverse the above procedure.

Care should be taken not to drop or jar the power supplies. If the assembly is laid on its base on a work bench, a soft pad should be inserted between bench and terminal board to prevent damage to the plastic terminal strip.

5.4 RELAYS - REMOVAL AND REPLACEMENT

All relays in the Electronics Unit are mounted on the Power Sequence Panel, Rack E. Reference Figure 5.4-1.

REMOVAL AND REPLACEMENT

1. Before removing any relay, cycle all power down and throw AC circuit breakers off.

2. Remove protective shield from sequence panel.

3. DC contactor relays ECJO, ECMO, EDJ1 and EDMO are mounted to the panel with screws and weldnuts. Telephone type relays EFKO, EFJO, EFK1, EFJ1 and EFJ2 are mounted to a bracket with locknuts. All relays may be removed and replaced from the front of the panel without removing cables or harnesses.

4. Check unit for loose connections, fallen washers, etc., and shorts before replacing protective shield and applying power.

RACK E

PANEL A

	1	2	3	4
J	208-A (50A)	MOD.1&2	MOD.3&4	MOD. 5
K	208-B (50A)	MOD.1&2	MOD.3&4	MOD. 5
L	208-A (15A)	MOD.1&2	MOD.3&4	MOD.5 P.S.-F
M	NEUT.	MOD.1&2	MOD.3&4	MOD. 5
N				
P		MOD.1&2	MOD.3&4	MOD. 5 P.S.-F -24VDC
R	208-B (15A)			P.S.-F

PANEL B

	1	2	3	4
J	-4.5VDC MOD. 1	MOD.2&3	MOD.4&5	GATE
K	-20VDC MOD. 1	MOD.2&3	MOD.4&5	GATE
L	+20VDC MOD. 1	MOD.2&3	MOD.4&5	GATE
M	-24 D MOD. 1	MOD.2&3	MOD.4&5	SEQ PANEL
N	+12VDC MOD. 1	MOD.2&3	MOD.4&5	⑦
P	-12VDC MOD. 1	MOD.2&3	MOD.4&5	GATE
R	GND. ④	GND. ⑤	GND. ⑥	GND. ⑧

SIDE   **OPPOSITE SIDE**

TYPICAL OF RELAYS ECJO, ECMO, EDJ1 & EDMO

WIRING SIDE

TYPICAL OF RELAYS EFK1, EFJO, EFJ1 & EFJ2

① **PIN**   **EFKO**
- 1 -24V (COIL)
- 5 GND (COIL)
- 3-4 GND. (AC-OFF-SW)
- 7-8 GND (HOLD EFJO)

② **PIN**   **EFJO**
- 1 GND (COIL)
- 4 -24V (COIL)
- 7-9 GND (PICK ECJO)
- 8-10 GND (HOLD EFJO)

③ **PIN**   **EFJ1**
- 1 -24V (COIL)
- 4 GND (DC-ON-SW)
- 7-9 GND (SMØL)
- 8-10 -24V (HOLD EFJ1)
- 13-15 -24V (PICK EFK1)
- 14-16 GND (DC RELAYS)

④ GND TO P.S.-F E.U. MAINTENANCE PANEL, SEQUENCE PANEL RELAYS & MOD. 1 GATE & BACKPLANE.

⑤ GND TO P.S.-G, MOD.2 & 3 GATE & MOD.2 BACKPLANE.

⑥ GND TO P.S.-H, MOD.4 & 5 GATE & MOD.3 BACKPLANE.

⑦ +12VDC TO GATE & SEQUENCE PANEL.

⑧ GND TO MOD. 4 & 5 BACKPLANE & E.U. BACKPLANE

PANEL C

ECJO
PIN
- 1 GND (COIL)
- 2 -24V (COIL)
- 3-4 -24V(AC-ON-IND)
- 5-6 -24V(DC-ON-SW)
- 7-8 208VAC-A (P.S.)
- 9-10 208VAC-B (P.S.)

ECKO PIN
- 1-GND (SMØL)
- 2-MOD-5(SMØL)
- 3-MOD-4(SMØL)
- 4-MOD-3(SMØL)
- 5-MOD-2(SMØL)
- 6-MOD-1(SMØL)

ECLO PIN
- 1-GND (SMIL)
- 2-MOD-5 (SMIL)
- 3-MOD-4 (SMIL)
- 4-MOD-3 (SMIL)
- 5-MOD-2(SMIL)

ECMO PIN
- 1 -24V (COIL)
- 2 GND (COIL)
- 3-4 -24D(GATE-MODS)
- 5-6 GND (HOLD ECJO)
- 7-8 +20 (GATE-MODS)
- 9-10
- 11-12 -20 (GATE-MODS)
- 13-14 -4.5V(GATE-MODS)
- 15-16
- 17-18 -24V (PICK EDMO)

PANEL F

EFJ2 (FRONT) PIN
- 1 GND. (COIL)
- 4 -24V.(REM-DC-OFF)
- 5-7 GND.(DC-OFF-SW)
- 6-8 GND. (DC-OFF-SW)

② EFJO (BACK)
③ EFJ1 (MIDDLE)

EFK1(FRONT) PIN
- 1 -24V (COIL)
- 4 GND. (DC-OFF-SW)
- 6-8 -24V (DC-ON-SW)
- 7-9 -24V HOLD EFK1

① EFKO (BACK)

PANEL E

EEJO PIN
1	
2	+100V
3	-100V
4	-120V
5	
6	+12V
7	
8	+12V
9	-12V
10	+20V
11	-20V
12	-4.5V
13	-24V
14	REMOTE-DC-ON
15	U.V.F.S.
16	REM.-DC -OFF
17	EMERG.-POW-OFF
18	POW-COMMON
19	-24D
20	

EEJ1 PIN
1	
2	+100V
3	-100V
4	-120V
5	GND
6	AC-ON-IND
7	LOCAL/REMOTE
8	DC-ON-SW
9	AC-ON-SW
10	
11	AC-OFF-SW
12	AC-OFF-SW
13	DC-ON-IND
14	LOCAL/REMOTE
15	DC-L.O.-SW
16	208VAC-A
17	208VAC-B
18	
19	AIR PRESSURE SW.
20	AIR PRESSURE SW

PANEL D

EDJO PIN
- 1-208VAC-A
- 2-208VAC-A
- 3-208VAC-A
- 4-208VAC-B
- 5-208VAC-B
- 6-208VAC-B
- 7
- 8

EDJ1 PIN
- 1 GND (COIL)
- 2 -24V (COIL)
- 3-4 +100V
- 5-6 -100V
- 7-8 -120V
- 9-10
- 11-12 GND (HOLD ECMO)
- 13-14 -24V(DC-ON-IND)

EDKO PIN
- A B
- G GND
- B A
- H EFJ1-13
- C REM-DC-OFF
- I J
- D -24V
- J K
- E ECMO-2
- K J
- F

EDMO PIN
- 1 GND (COIL)
- 2 -24V (COIL)
- 3-4 -12V (GATE-MODS)
- 5-6 +12V (GATE-MODS)
- 7-8 -24V (PICK EDJ1)
- 9-10 GND (HOLD ECMO)

EDLO PIN
- A B
- G EFJ1-16
- B A
- H EDMO-2
- C EDJ1-1
- I J
- D EDMO-8
- J I
- E
- K
- F LOC/REM SW
- L ECJO-6

EDNO PIN
- A B
- G DC-OFF-SW
- B A
- H EFJ1-13
- C REM-DC-OFF
- I J
- D COMMON
- J I
- E EFKO-5
- K
- F EFKO-1
- L K

EDPO PIN
- A B
- G EFJ1-4
- B A
- H EFK1-8
- C D
- I -24VDC
- D C
- J AC-ON-SW
- E
- K
- F EFJ1-8
- L -24VDC

FIGURE 5.4-1
RACK E COMPONENT LOCATOR

5.5 FANS - REMOVAL AND REPLACEMENT

Before removing fans, cycle down all power and open AC circuit breakers.

The two muffin fans located on the inside of the rear skin are accessible by removing the side skin and opening the logic gate. The fans are held to the rear skin by mounting clips with spring tabs which may be sprung apart with a screwdriver far enough to allow the fan to be removed from the clip. If complete removal is necessary, the two AC wires must be removed from the small terminal board below the fan.

5.6 COMPRESSOR ASSEMBLY - REMOVAL AND REPLACEMENT

The following procedure should be followed for the removal and replacement of the compressor.

CAUTION

Refer to Section 5.7 for general precautions when working on the air system.

REMOVAL

1. Turn off the E.U. DC and AC power.

2. Turn off the 70 amp main AC circuit breaker.

3. Bleed off the tank pressure.

4. Disconnect the output air line.

5. Remove the nuts (under the E.U. base) from the four compressor assembly mounting studs. Move the compressor for better access to the motor leads.

6. Disconnect the frame ground lead from the top of the compressor.

7. Remove the motor lead cover plate. The motor ground lead (green) is disconnected at the same time.

8. Disconnect the black power lead from the black motor lead by removing the "wire nut" and separating the leads. Separate the white leads in the same manner.

9. Remove the compressor assembly from the cabinet.

REPLACEMENT

1. Ensure the 70 amp main circuit breaker is off.

2. Place the compressor assembly in the E.U. cabinet but do not mount to the base at this time.

3. Pass the incoming black, white and green motor leads through the motor lead hole.

4. Connect the black power lead to the black motor lead using a "wire nut". Connect the white leads in the same manner.

5. Install the motor lead cover plate. The green motor ground lead must be connected at the same time with one of the cover plate mounting screws.

6. Mount the compressor assembly in the E.U. cabinet.

7. Connect the frame ground lead to the top of the compressor assembly.

8. Connect the output air line to the compressor output manifold.

9. Turn on the 70 amp main circuit breaker. The compressor should go on, pressurize the tank and turn off when the tank pressure reaches 80 psi.

10. Ensure there is no air leak from the output air line to manifold connection before restoring the E.U. to normal operation.

5.7 GENERAL PRECAUTIONS FOR AIR CONNECTIONS

The following precautions should be observed when performing work re-
quiring the removal and replacement of any air fitting and connection.

1. Turn off the E.U. DC and AC power.

2. Turn off the E.U. 70 amp main AC circuit breaker to de-acti-
    vate the compressor motor prior to the removal of any air
    connection, except the snap-on type used on the S.U. air
    trunk line.

                    CAUTION

        Bleed off the tank pressure completely
        before disconnecting or opening any air
        connection, except the snap-on type. A
        convenient method of bleeding tank pres-
        sure is to "crack" loose the tank sedi-
        ment bowl drain cock.

3. Whenever any air pipe fitting is disconnected, plastic seal-
    ant (P/N 11117165) should be used on the threads before
    replacement.

4. Polyethylene tube fittings do not require sealant. Refer to
    Figure 5.7-1. These fittings should be tightened finger
    tight and then up to 1/2 turn with a wrench, if required.
    Do not overtighten or the plastic ring seal may be damaged.

BLACK POLYETHYLENE
TUBING

PLASTIC RING
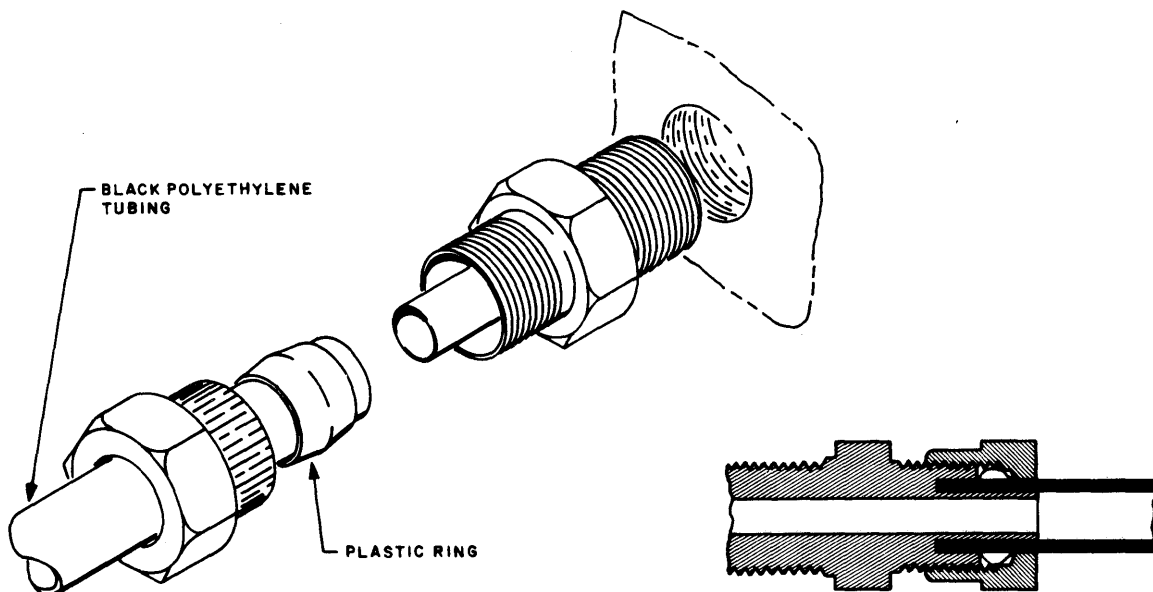
FIGURE 5.7-1
POLYETHYLENE TUBE FITTING

5. Check for air leaks after any air fitting is reconnected and the System pressurized. Apply a small amount of liquid leak detector around the joint and then check for bubbles. Use a cloth to catch any excess liquid and wipe off the joint after the test.

5.11 POWER SUPPLY ADJUSTMENTS

RACK F

+100V, -100V, -120V and -24V

None.

RACK H

+20V and -20V

None.

RACK G

+12V, -12V and -4.5V

The -4.5V may be adjusted by potentiometer R6 mounted on the face of
the power supply rack.

5.12   VARIABLE BIAS ADJUSTMENTS

Before making the Variable Bias Adjustments, check the -4.5V supply.
It must be -4.5V ± 0.25V.

The three VB supplies are adjusted as follows:

MUVB-01	Word Mark Multi Bias	AAC6X2	-0.2V
MUVB-02	BCLP Bias	AAA7X7	-0.2V
VB	Flip-flop Bias	AAC1X2	-1.2V

5.13 MULTI ADJUSTMENTS

Before making any of the following adjustments, check the -4.5V Supply.
It must be -4.5V ± 0.25V. Then check the Variable Bias adjustments.
Refer to Section 5.12.

1. LOCAL/REMOTE Switch to LOCAL.

2. CLOCK ON/OFF Switch to OFF.

3. Depress BIT SINGLE PULSE button for checking the following:

   a. IXHM (AA4N2) should be 2 microseconds ± 0.1. Scope at
       AA4U0, sync internal negative.

   b. RDHM (AC5A2) should be 32 microseconds ± 5. Scope at
       AC5F0, sync internal negative.

   c. WØHM (AB6N7) should be 7.86 microseconds ± 0.25. Scope at
       AB6U5, sync internal negative. Ground input to ASRS at
       AC7F0.

   d. DIXM (BB1A2) should be 600 microseconds ± 20.
       Set ACFF, INFF, BA2 and BA4.
       Hold ACFF and BA2 ON or they will reset.
       Scope at AA9W0 (DIXS/), sync internal positive.

4. Return LOCAL/REMOTE Switch to REMOTE.

5. Return CLOCK ON/OFF Switch to ON.

6. BITP/DBIT – Bit Pulse and Delay Bit Pulse multis are to be
    adjusted by observing the time delay between BITL and BCLP.
    The adjustment of these two multis is performed in the following
    manner:

   a. Connect A trace to BCLP (AAB8J0).

   b. Connect B trace to BITL-01 (AAA6V2).

   c. Sync on BITL-01.

   d. With ICFF false, the delay between BITL-01 and BCLP should
       be 250 nanoseconds. Adjust at AAA6N7 (MUAJ) if necessary.

   e. Hold ICFF ON. The delay between BITL-01 and BCLP should
       be 675 nanoseconds. Adjust at ABA0N2 (DCL) if necessary.

5.21   60-80 AIR SWITCH CHECK AND ADJUSTMENT

The 60-80 Air Switch has a built in 20 PSI differential between its actuated (points closed) and de-actuated (points open) positions. The switch is set by adjusting it to ACTUATE at the proper pressure.

The following procedure should be followed when performing the Check and Adjustment:

1. Depress the DC OFF Switch to retract the heads on the Module(s).

2. Depress the AC OFF Switch.

3. Loosen the Drain Cock on the Tank Sediment Bowl and slowly release the air from the Tank. As the pressure falls, watch the gauge to determine when the switch actuates to turn the Compressor ON. THE COMPRESSOR SHOULD GO ON AT 60 ±2 PSI.

4. Tighten the Drain Cock on the Sediment Bowl and let the pressure build up until the switch de-actuates.

5. Repeat Steps 3 & 4 to verify the actuation point of the switch.

6. If the switch actuates at 60 ±2PSI, bring up Power and restore the System to normal operation.
    If the switch is NOT actuating at the proper pressure, proceed to Step 7.

CAUTION

With the 70 amp main AC and the 20 amp Circuit Breakers ON, 208VAC is present inside the 60-80 switch box.

7. Turn OFF the 70 amp main AC Circuit Breaker.

8. Remove the cover of the 60-80 switch.

9. Use a 11/32" spin-tight to turn the nut on the Adjustment Spring. Tightening the spring raises the switch actuation point; loosening the spring lowers the actuation point. Turn the nut approximately one turn.

10. Replace the switch cover as a safety measure.

11. Turn ON the 70 amp main AC Circuit Breaker which applies AC through the 20 amp Circuit Breaker to the 60-80 switch.

12. Begin this procedure again at Step 3.

5.22 AIR LINE REGULATOR ADJUSTMENT

The Air Line Regulator is set to maintain 50 PSI +2 -0 on the Air Trunk Line as indicated by the Maintenance Panel Air Gauge.

Adjustments are made by turning the screw at the bottom of the regulator in or out to increase or decrease the pressure, respectively.

While under pressure, the regulator does not respond accurately to manual adjustment intended to lower the pressure of the output. Therefore, to make that adjustment, it is necessary to de-pressurize the input, back out the Adjustment Screw, re-pressurize and increase the pressure output to the proper operating point.

The following procedure should be followed when making adjustments on the Air Line Regulator:

1. Turn OFF DC to retract the heads in the Module(s).

2. Turn OFF AC.

3. Use a 1/2" wrench to loosen the Lock Nut on the Adjustment Screw.

4. To INCREASE the pressure, turn the Adjusting Screw IN until the Maintenance Panel Air Gauge reads 50 PSI +2 -0. Turn the screw slowly to prevent regulator overshoot. An offset screw driver is useful as an adjustment tool.

5. To DECREASE the pressure, perform the following Steps.

    a. Turn OFF the 70 amp main AC Circuit Breaker.

    b. Bleed off the Tank pressure by loosening the Sediment Bowl Drain Cock. Retighten the Drain Cock.

    c. Back out the regulator Adjustment Screw one or two turns.

    d. Turn ON the 70 amp Circuit Breaker.

    e. When the Tank pressure has been in the normal operating range for five minutes, slowly increase the pressure to 50 PSI +2 -0 by turning the Adjustment Screw in. Check the pressure at the Maintenance Panel Air Gauge as the adjustment is being made.

    f. To ensure the adjustment has stabilized, re-check the pressure output approximately five minutes after performing the adjustment.

6. After the adjustment has been completed, tighten the Lock Nut on the Adjustment Screw.

INDEX - SECTION VI

6 MAINTENANCE PROCEDURES AND AIDS

6.2   MONTHLY PREVENTIVE MAINTENANCE

1.   **FILTER**

There is one fiberglass disposable filter located at the bottom front of the unit. It should be checked frequently and changed at least once a month or when necessary.

Since the filter is readily accessible by removing the front skin, power need not be dropped from the unit or normal operation interrupted during changing.

2.   **POWER SUPPLIES**

Power Supply output voltages should be checked on a monthly basis. Test jacks are provided on the power supply assemblies for all voltages.

Rack H

+20V ± 1V

-20V ± 1V

Rack F

+100V ± 5V

-100V ± 5V

-120V ± 6V

-24V ± 1.2V

Rack G

+12V ± .5V

-12V ± .5V

-4.5V ± .2V

3.   **PRESSURE TO AIR TRUNK LINE**

The pressure applied to the S.U. air trunk line should be 50 psi +2 -0. This pressure should be checked at the air gauge on the

Maintenance Panel. If the pressure is not within tolerance, perform the output regulator adjustment procedure as outlined in Section 5.22.

NOTE

Whenever the tank pressure has been released and then re-pressurized, always allow approximately five minutes for the regulator to stabilize before taking a reading.

4. TANK SEDIMENT BOWL

The Tank Sediment Bowl should be removed and cleaned. The amount of moisture which collects in the bowl will vary with the environment and how often the compressor runs. Do not allow the bowl to become more than approximately 1/3 full of water. Use the drain cock to empty the bowl as needed between P.M. periods. (Have a large absorbent cloth available to catch the moisture when the drain cock is loosened.) The following steps should be performed when the Sediment Bowl is removed:

a. Turn off DC and AC power.

b. Turn off the 70 amp main AC circuit breaker.

c. Loosen the drain cock to discharge the tank and relieve the pressure on the bowl retainer ring. Use an absorbent cloth to catch the moisture.

d. Unscrew the large retainer ring which holds the bowl to the metal part of the assembly.

e. Remove the bowl and clean by wiping it out with a lint free cloth.

f. Replace the bowl by reversing the above procedure. Do not over tighten the retainer ring. Turn on the 70 amp circuit breaker to pressurize the tank and check for leaks before DC and AC power are restored. Apply liquid leak detector around the bowl at the retainer ring and watch for bubbles. Wipe off any remaining liquid after the test.

5. 60-80 AIR SWITCH

The 60-80 Air Switch should maintain tank pressure between 60 and 80 ± 2 psi. Check the operation of this switch. Refer to Section 5.21 for the check and adjustment procedure.

6. VARIABLE BIAS

On a monthly basis, the three VB packages in the E.U. should be checked for proper output level.

Test point and desired output are as follows:

MUVB-01	Word Mark Multi Bias	AAC6X2	-0.2V
MUVB-02	BCLP Bias	AAA7X7	-0.2V
VB	Flip-flop Bias	AAC1X2	-1.2V

7. MULTIS

Verify multis for proper timing. Refer to Multi Adjustments, page 5.13-1.

6.4 SEMI-ANNUAL PREVENTIVE MAINTENANCE

1. COMPRESSOR FILTER

The intake filter on the compressor should be replaced semi-annually. Unscrew the filter from the brass elbow on the intake manifold and replace with a new filter.

6.5   ANNUAL PREVENTIVE MAINTENANCE

1.   10 MICRON AIR FILTER

The 10 micron filter element should be replaced <u>annually</u>. The
following procedure should be followed when replacing the element:

a.   Turn off DC and AC power.

b.   Turn off the 70 amp main AC circuit breaker.

c.   Bleed off the tank pressure by loosening the drain cock on the
     sediment bowl.

<div align="center">

CAUTION

Do not use the drain cock on the
10 micron filter to discharge
the tank even when the element
is being replaced. Contaminants
which normally are trapped in
the sediment bowl are apt to be
forced into the filter assembly.

</div>

d.   Unscrew the retaining ring which holds the bowl to the assem-
     bly. Remove the bowl. Refer to Figure 6.5-1.

e.   Remove the brass, knurled retaining nut at the bottom of the
     shaft.

f.   Unscrew and remove the baffle.

g.   Remove the shield, washer and filter element.

h.   Install the new 10 micron element by reversing steps e, f and
     g of the above procedure.

i.   Wipe out the filter bowl with a clean, lint-free cloth.

j.   Replace the filter bowl. Do not overtighten the retaining ring.

k.   Turn on the 70 amp breaker to repressurize the tank and check
     for leaks before restoring AC and DC power. Apply liquid leak
     detector around the top of the bowl and then watch for bubbles.
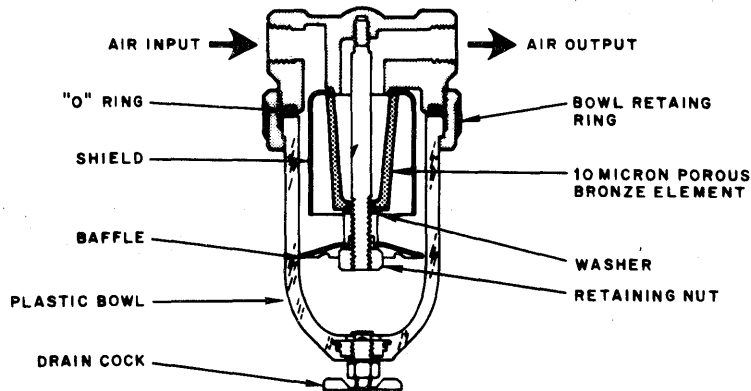   Wipe off any remaining liquid after the test is completed.

FIGURE 6.5-1
10 MICRON AIR FILTER

2. FANS

The two cabinet exhaust fans located on the inside of the rear skin should be oiled annually using the following procedure:

Oil   EDD Part #11838596
Oil injector   EDD Part #11838588

a. Remove air from oil injector by holding the needle up and pressing on the plunger.

b. Project the injector needle through the louvres (in back skin) and place the needle at the center of circle marked on the gold label.

c. Position the needle at an angle of approximately 45° to the label surface and point it toward the center of the rubber cap. (These fans are lubed by inserting the oil injector needle through a self-sealing rubber cap located in the center of the motor hub.)

d. Pierce the label and the concealed self-sealing rubber cap located under the label.

e. Insert the needle approximately 1/4".

f. Depress the plunger of the oil injector approximately 1/16" to force the oil to flow. Rotating the fan will relieve air pressure and allow oil to flow into the oil chamber.

6.6 SIGNALS AND TEST POINTS

The following is a list of signals with test point locations. The listing includes input levels as monitored at the output of the input switches, output levels as monitored at the last output switch or driver and internal levels as monitored at the outputs of Flip-Flops, Multi's, Delays, etc. HSDL (Information Center Tap Driver) outputs are not covered in this list; refer to DA Schematics, pages 00.07.0 through 00.16.0.

INPUT LEVELS FROM D.F.C.U.

Level	Test Point
D01S	AAA9C4
D02S	AAA9C0
D04S	AAA9D2
D08S	AAA9H4
D16S	AAA9J0
ZØ1L/	AAB9C9
ZØ2L/	AAB9C5
ZØ3L/	AAB9D7
T01S	ACA1C9
T02S	ACA1C5
T04S	ACA1D7
T08S	ACA1H9
T10S	ACA4C9
T20S	ACA4C5
T40S	ACA4D7
SW1L/	AAB2C9
SW2L/	AAB2C5
SW4L/	AAB2D7
SW8L/	AAB2H9
SWAL/	AAB2J5
SWBL/	AAA2R9
DFSS	ACA4H9
SWRS	AAA2R5
SCØL	AAA2V9

OUTPUT LEVELS TO D.F.C.U.

Level	Test Point
SR1L	AAC2B7
SR2L	AAC2H5
SR4L	AAC2H9
SR8L	AAC3B7
SRAL	AAC1B7
SRBL	AAC1H5
CS1L/	AAB0B0
CS2L/	AAB0F0
SCLP	AAC1H9
SURL/	AAA4R5
SARL/	AAC8C9
SWLL	AAA4H4
WØMD	AAB6H5
INXD	AAA4B2

OUTPUT LEVELS TO STORAGE MODULES		INPUT LEVELS FROM STORAGE MODULES	
Level	Test Point	Level	Test Point
MØ1L	ABB0P7	HFML-01	AAA8C4
MØ2L	ABB0V5	HFML-02	AAA8C0
MØ3L	ABB0V9	HFML-03	AAA8D2
MØ4L	ABB1P7	HFML-04	AAA8H4
MØ5L	ABB1V5	HFML-05	AAA8J0
DISC-01/	AAA9R4	BITL-01	AAB0R3
DISC-02/	AAA9R0	BITL-02	AAB0S3
DISC-03/	AAA9S2	BITL-03	AAB0T3
DISC-04/	AAA9V4	BITL-04	AAB0U3
		BITL-05	AAB0V3
ZØ1L-01/	AAB9C9		
ZØ2L-01/	AAB9C5	TD1L	AAB0R4
ZØ3L-01/	AAB9D7	TD2L	AAB0S4
		TD3L	AAB0T4
DFSL/	AAB0Y0	TD4L	AAB0U4
DFSS	ACA4H9	TD5L	AAB0V4
SU1FW	AAB1U9	CS1L/	AAB0N4
SU1FW/	AAB1U6	CS2L/	AAB0P4
ICFF-1B	AAA5W9	ASRS	AAC7D2
		ASRS/	AAC7H4
WRSD/	AAB6B7		
		IRAS	AAC7C4
SPFD	AAA4H0	IRAS/	AAC7C0
IXHS/	AAA4R9		
TRSL/	AAC8J5		
GSSL	AAB9H9		

INTERNAL LEVELS

Level	Test Point	Level	Test Point
ACFF	AAA1U9	GLAF	AAC4U9
ASRS	AAC7D2	GSLF	AAC5W0
BA1F	AAB9U9	GSSL	AAB9H9
BA2F	AAC9F9	TRSF	AAC3U9
BA4F	AAC9U9	WØHF	AAB7F6
CBAS	AAC8C5	BCLP	AAB8J0
CSUS	AAA2W5	BITP	AAA6W5
DBIT	ABA0W3	INXP-01	AAA3V4
DIXM	ABB1F0	RIHS/	AAC8U7
DIXP	AAA3S4	RDHM	AAC5F0
ECCS	AAC8H9		

6.7 MAINTENANCE PANEL

Reference Figure 6.9-2.

The Maintenance Panel (Rack D) consists of switches, indicators, indicator-switches and test jacks for power control and maintenance functions. A DC meter with switch, power on time meter and air pressure gauge are also provided.

POWER CONTROL

Switches   Indicators

DC LOCKOUT   AC ON
                            DC ON
                            RELAY SUPPLY ON

MAINTENANCE

Switches   Indicators

LOCAL/REMOTE   Storage Units 1 through 5 Not Ready
CLOCK
BITP (PB)   Test Jacks
WØMP (PB)
CLEAR (PB)   INXP - Index Pulse
RESET (PB)   SW1L - FERL (S04F) during Read
                            SCØL - Segment Coincidence
                            ACFF - Action FF
                            ICFF/- Interlace Control

Indicator-Switches

S.U. Register
INFF - Index FF
ACFF - Action FF
ICFF - Interlace Control FF
GSLF - Gain Select FF
SPFF - Space FF
BA1, BA2 and BA4 - BA Counter
TRSF - Threshold Store FF
GLAF - Gain Latch FF

LOCAL/REMOTE SWITCH

Reference Figure 6.7-1.

Remote

1. Couples REM-DC-ON-E pulse from D.F.C.U. to Rack E.

2. REMS-A true to Gate A enabling ready levels (HFML-nn) from Modules to control SURL/ (Storage Units Ready Level) when CLOCK switch is ON.

3. REMS/ false to CAG 107 disabling Bit and Word Mark Single Pulse switches.

Local

1. Opens REMOTE DC ON line to Rack E. DC can be cycled on from operator's panel only.

2. REMS-A false to Gate A making SURL/ true (Storage Units Not Ready).

3. REMS/ true to CAG 107 enabling Bit and Word Mark Single Pulse switches.

CLOCK SWITCH

On

1. CCIL-A true enabling ready levels (HFML-nn) from Modules to control SURL/ when in REMOTE.

2. CCIL-A true to clock logic enables BITP and WØMP to be generated from Module inputs (BITL-nn and ASRS).

3. CSIL-A false to CAG 107 disabling Bit and Word Mark Single Pulse switches.

Off

1. CCIL-A false making SURL/ true (Storage Units Not Ready).

2. Disables Module inputs (BITL-nn and ASRS) from generating BITP and WØMP in clock logic.

3. CSIL-A true to CAG 107 enabling Bit and Word Mark Single Pulse switches.
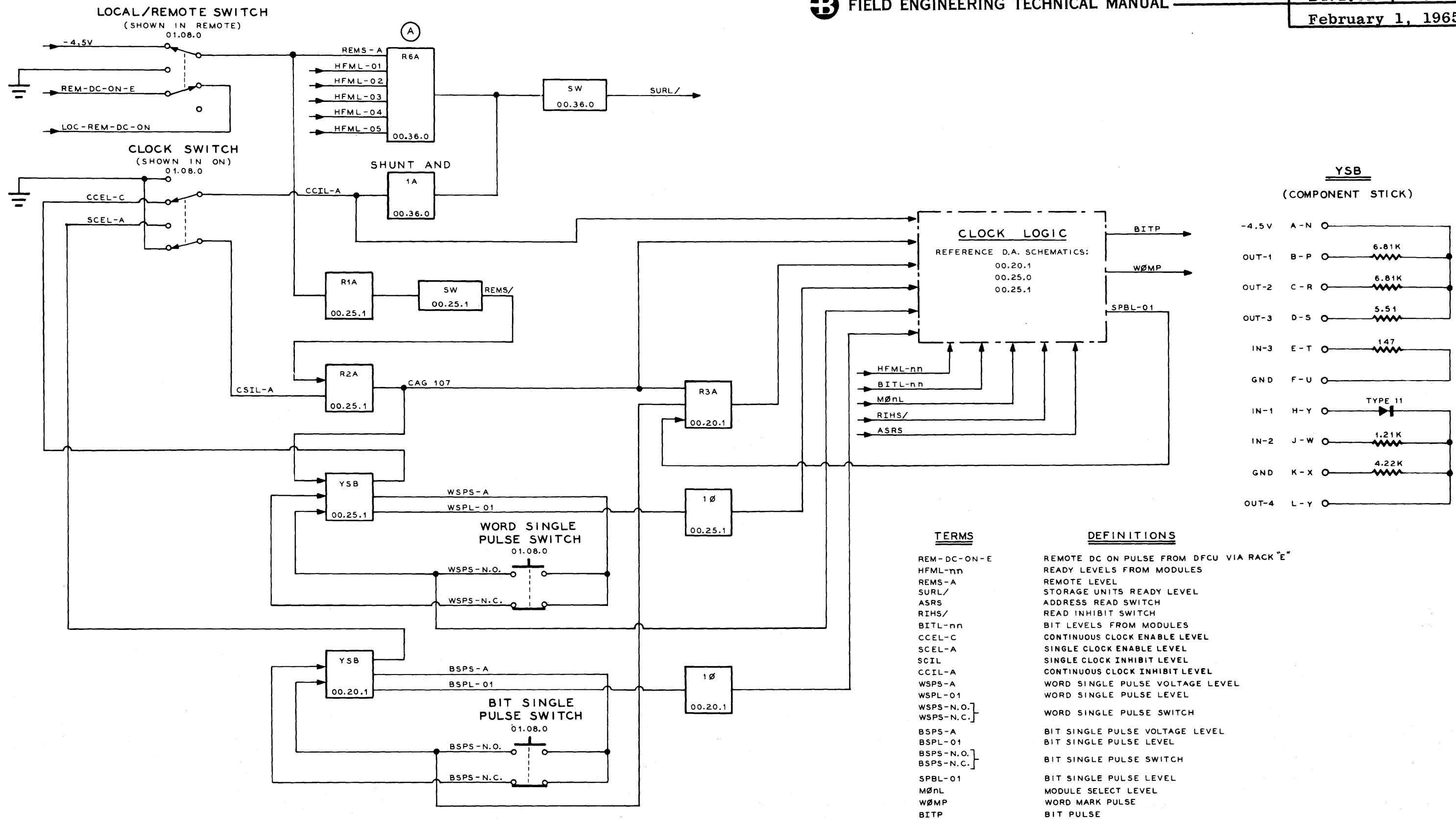
FIGURE 6.7-1
MAINTENANCE PANEL SWITCHES
AND LOGIC

TERMS

REM-DC-ON-E
HFML-nn
REMS-A
SURL/
ASRS
RIHS/
BITL-nn
CCEL-C
SCEL-A
SCIL
CCIL-A
WSPS-A
WSPL-01
WSPS-N.O.
WSPS-N.C.
BSPS-A
BSPL-01
BSPS-N.O.
BSPS-N.C.
SPBL-01
MØnL
WØMP
BITP

DEFINITIONS

REMOTE DC ON PULSE FROM DFCU VIA RACK "E"
READY LEVELS FROM MODULES
REMOTE LEVEL
STORAGE UNITS READY LEVEL
ADDRESS READ SWITCH
READ INHIBIT SWITCH
BIT LEVELS FROM MODULES
CONTINUOUS CLOCK ENABLE LEVEL
SINGLE CLOCK ENABLE LEVEL
SINGLE CLOCK INHIBIT LEVEL
CONTINUOUS CLOCK INHIBIT LEVEL
WORD SINGLE PULSE VOLTAGE LEVEL
WORD SINGLE PULSE LEVEL
WORD SINGLE PULSE SWITCH
BIT SINGLE PULSE VOLTAGE LEVEL
BIT SINGLE PULSE LEVEL
BIT SINGLE PULSE SWITCH
BIT SINGLE PULSE LEVEL
MODULE SELECT LEVEL
WORD MARK PULSE
BIT PULSE

6.8   TEST ROUTINES

The following are the Test Routines available for use with the Disk File Subsystem and a brief description of their use.

B200   - TR 2122   This routine will test the subsystem under the control of the B200. The operator has control of the program section to be run by use of the Operator's Panel. The routine is made up of eight sections and will test any and all subsystem configurations and character options.

B5500 - TR 5561   This routine will test the subsystem under control of the B5500. The operator has control of the program section to be run by the use of the Supervisory Printer. The routine is made up of three sections and will test any and all subsystem configurations and character options.

6.9   COMPONENT LOCATIONS

1.   ELECTRONICS UNIT DA RACK LOCATOR - Figure 6.9-1

2.   ELECTRONICS UNIT RACK D DETAIL - Figure 6.9-2

3.   ELECTRONICS UNIT RACK A COMPONENTS - Figure 6.9-3

4.   ELECTRONICS UNIT POWER SUPPLY COMPONENTS - Figure 6.9-4

RACK "E"
POWER SEQUENCE

RACK "A"
LOGIC GATE

RACK "B"
WRITE LOCKOUT

RACK "C"
CONTROL PANEL

RACK "D"
MAINT.
PANEL

RACK "F"
+100
-100
-120
-24

RACK "G"
+12
-12
-4.5

RACK "H"
+20
-20

C B

C B
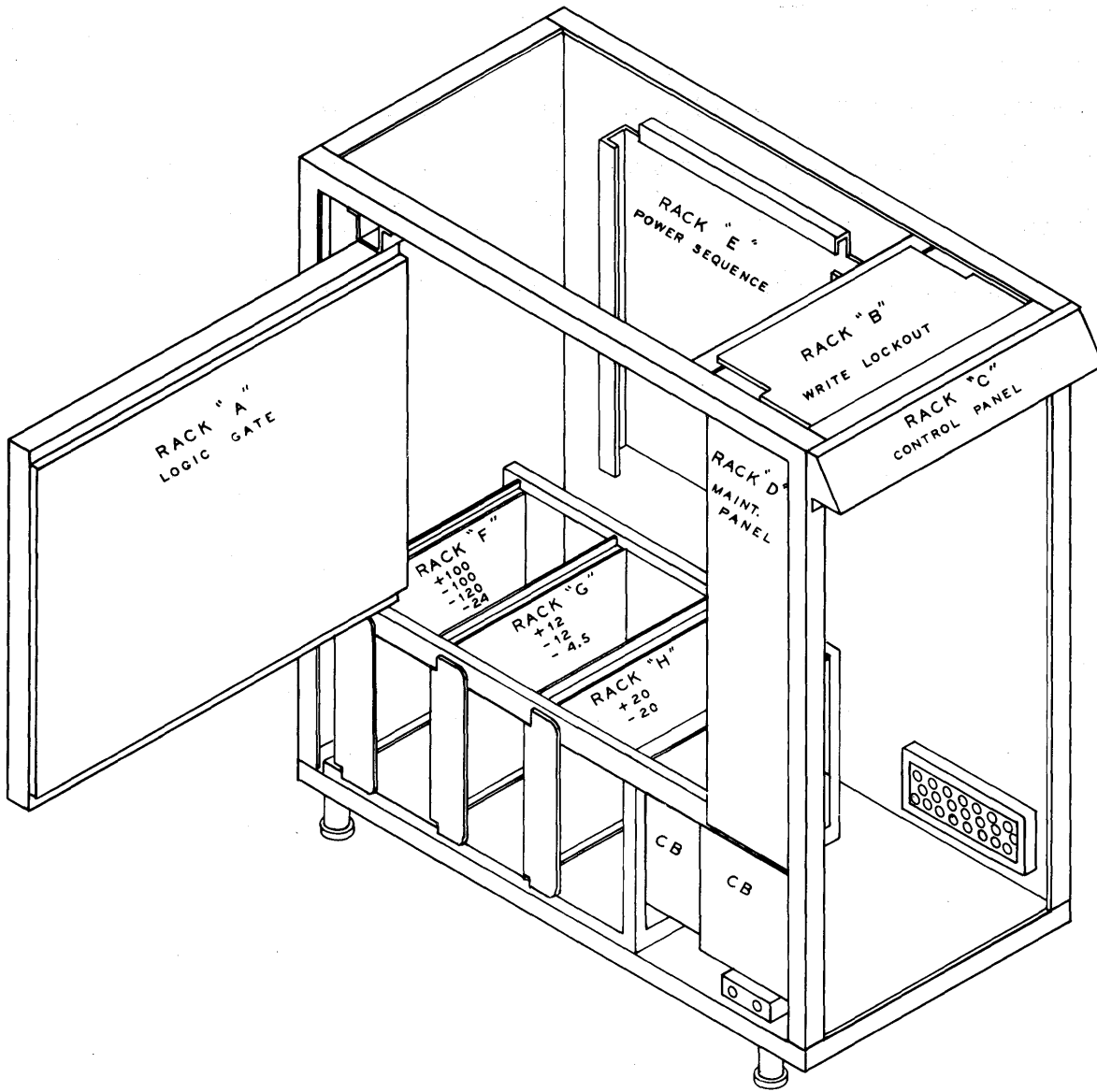
FIGURE 6.9-1
ELECTRONICS UNIT DA RACK LOCATOR
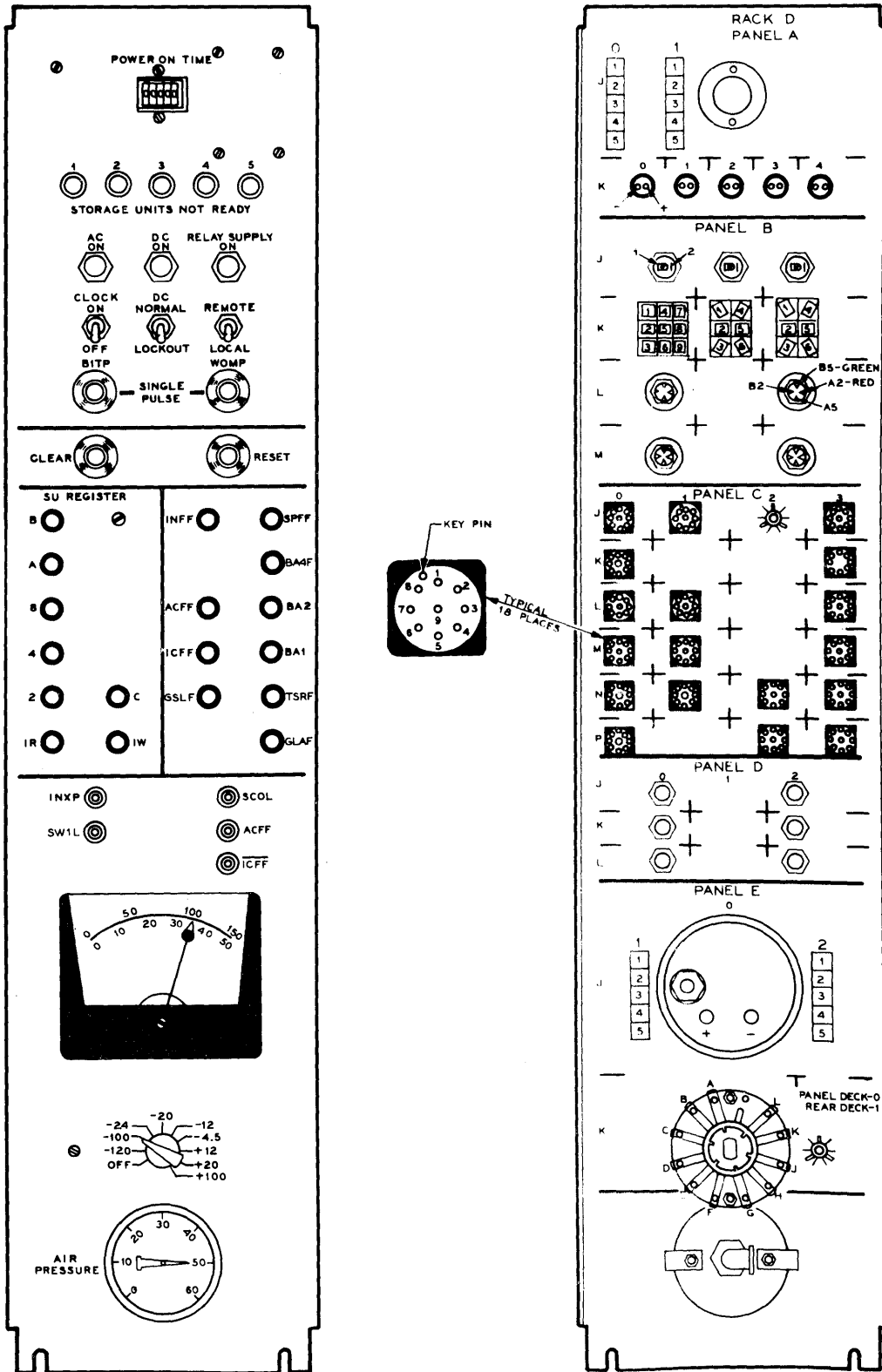
FIGURE 6.9-2
ELECTRONICS UNIT RACK D DETAIL

Column markers (left to right): 1 0 9 8 7 6 5 4 3 2 1 0

Row A (top band)

| SW-H Z01S·01 Z02S-02 | SW-H D01S D02S D04S D08S D16S | SW-H H̅F̅M̅S̅-01 H̅F̅M̅S̅-02 H̅F̅M̅S̅-03 H̅F̅M̅S̅-04 H̅F̅M̅S̅-05 | DRIN S̅U̅R̅D̅ | DRAN SR1L SR2L SR3L SR4L SR5L | DR-9 INXD SPFD SWLD | MUFW INXP-02 | FF-7 INFF | FF-7 ICFF | C50 LOCKOUT PANEL CABLE | C50 MAINT PANEL CABLE |

Row A (second band)

| DCL — BIT CLOCK DELAY | SW-H D̅S̅L̅S̅-01 D̅S̅L̅S̅-02 D̅S̅L̅S̅-03 D̅S̅L̅S̅-04 D̅I̅X̅S̅ | SW-H DSLS-01 DSLS-02 DSLS-03 DSLS-04 INHS | VB MUVB-02 | MUFW BITP | AMFF I̅C̅F̅F̅-01 I̅C̅F̅F̅-01 | SW-H I̅X̅H̅S̅ SURS SPBS-01 SPBS-02 W̅Ø̅H̅S̅ | DU-1 IXHM | PSH INXP-01 DIXP | SW-H SWBS SWRS SCØS SCUB | FF-7 ACFF | C50 MAINT. PANEL CABLE |

Row B (third band)

| MUJ DIXM | SW-H Z̅Ø̅1̅S̅-01 Z̅Ø̅2̅S̅-01 Z̅Ø̅3̅S̅-01 GSSL | MUAJ BCLP | FF-7 WØHF | DR-9 WRSD WØMD | FF-7 SUCF | FF-7 SUAF | FF-7 SU4F | SW-H SW1S SW2S SW4S SW8S SWAS | FF-7 SU1F-R | C50 CONTROL LOGIC CABLE |

Row B (fourth band)

| DR-9 MØ4D MØ5D | DR-9 MØ1D MØ2D MØ3D | FF-7 BA1F | FF-7 SPFF | DU-J WØHM | FF-7 SUBF | FF-7 SUBF | FF-7 SU2F | FFN7 SU1F-W | C50 MODULE LOGIC CABLE |

Row C (fifth band)

| FF-7 BA2F | SW-H S̅A̅R̅S̅ CBAS R̅I̅H̅S̅ ECCS T̅R̅S̅S̅ | SW-H I̅R̅A̅S̅ I̅R̅A̅S̅ ASRS A̅S̅R̅S̅ | MUFW WØMP-01 | DU-E RDHM | DR-9 SR8D SU1D SSUD | DR-9 SR1D SR2D SR4D | DR-9 SRAD SRBD SCLD | C50 POWER CABLE |

Row C (sixth band)

| FF-7 BA4F | VB MUVB-01 | FF-7 GSLF | FF-7 GLAF | FF-7 TSRF | UVFS — POWER SENSING | VB (-1.2V) | C50 POWER CABLE |

Row A (seventh band)

| SW-H H̅S̅T̅S̅-50 H̅S̅T̅S̅-60 H̅S̅T̅S̅-70 H̅S̅T̅S̅-80 H̅S̅T̅S̅-90 | SW-H H̅S̅T̅S̅-00 H̅S̅T̅S̅-10 H̅S̅T̅S̅-20 H̅S̅T̅S̅-30 H̅S̅T̅S̅-40 | SW-H T10S T20S T40S DFSS | SW-H H̅S̅U̅S̅-05 H̅S̅U̅S̅-06 H̅S̅U̅S̅-07 H̅S̅U̅S̅-08 H̅S̅U̅S̅-09 | SW-H H̅S̅U̅S̅-00 H̅S̅U̅S̅-01 H̅S̅U̅S̅-02 H̅S̅U̅S̅-03 H̅S̅U̅S̅-04 | SW-H T01S T02S T04S T08S | C50 POWER CABLE |

Row A (eighth band) — DRCH

| HSDD-90 HSDD-91 HSDD-92 | HSDD-81 HSDD-82 HSDD-83 | HSDD-72 HSDD-73 HSDD-74 | HSDD-63 HSDD-64 HSDD-65 | HSDD-54 HSDD-55 HSDD-56 | HSDD-45 HSDD-46 HSDD-47 | HSDD-36 HSDD-37 HSDD-38 | HSDD-27 HSDD-28 HSDD-29 | HSDD-18 HSDD-19 HSDD-20 | HSDD-09 HSDD-10 HSDD-11 | HSDD-00 HSDD-01 HSDD-02 |

Row B (ninth band) — DRCH

| HSDD-93 HSDD-94 HSDD-95 | HSDD-84 HSDD-85 HSDD-86 | HSDD-75 HSDD-76 HSDD-77 | HSDD-66 HSDD-67 HSDD-68 | HSDD-57 HSDD-58 HSDD-59 | HSDD-48 HSDD-49 HSDD-50 | HSDD-39 HSDD-40 HSDD-41 | HSDD-30 HSDD-31 HSDD-32 | HSDD-21 HSDD-22 HSDD-23 | HSDD-12 HSDD-13 HSDD-14 | HSDD-03 HSDD-04 HSDD-05 | C50 HEAD SELECT CABLE |

Row B (tenth band) — DRCH

| DRCH HSDD-99 | HSDD-96 HSDD-97 HSDD-98 | HSDD-87 HSDD-88 HSDD-89 | HSDD-78 HSDD-79 HSDD-80 | HSDD-69 HSDD-70 HSDD-71 | HSDD-60 HSDD-61 HSDD-62 | HSDD-51 HSDD-52 HSDD-53 | HSDD-42 HSDD-43 HSDD-44 | HSDD-33 HSDD-34 HSDD-35 | HSDD-24 HSDD-25 HSDD-26 | HSDD-15 HSDD-16 HSDD-17 | HSDD-06 HSDD-07 HSDD-08 | C50 HEAD SELECT CABLE | C50 HEAD SELECT CABLE |

FIGURE 6.9-3
ELECTRONICS UNIT
RACK A COMPONENT LOCATOR
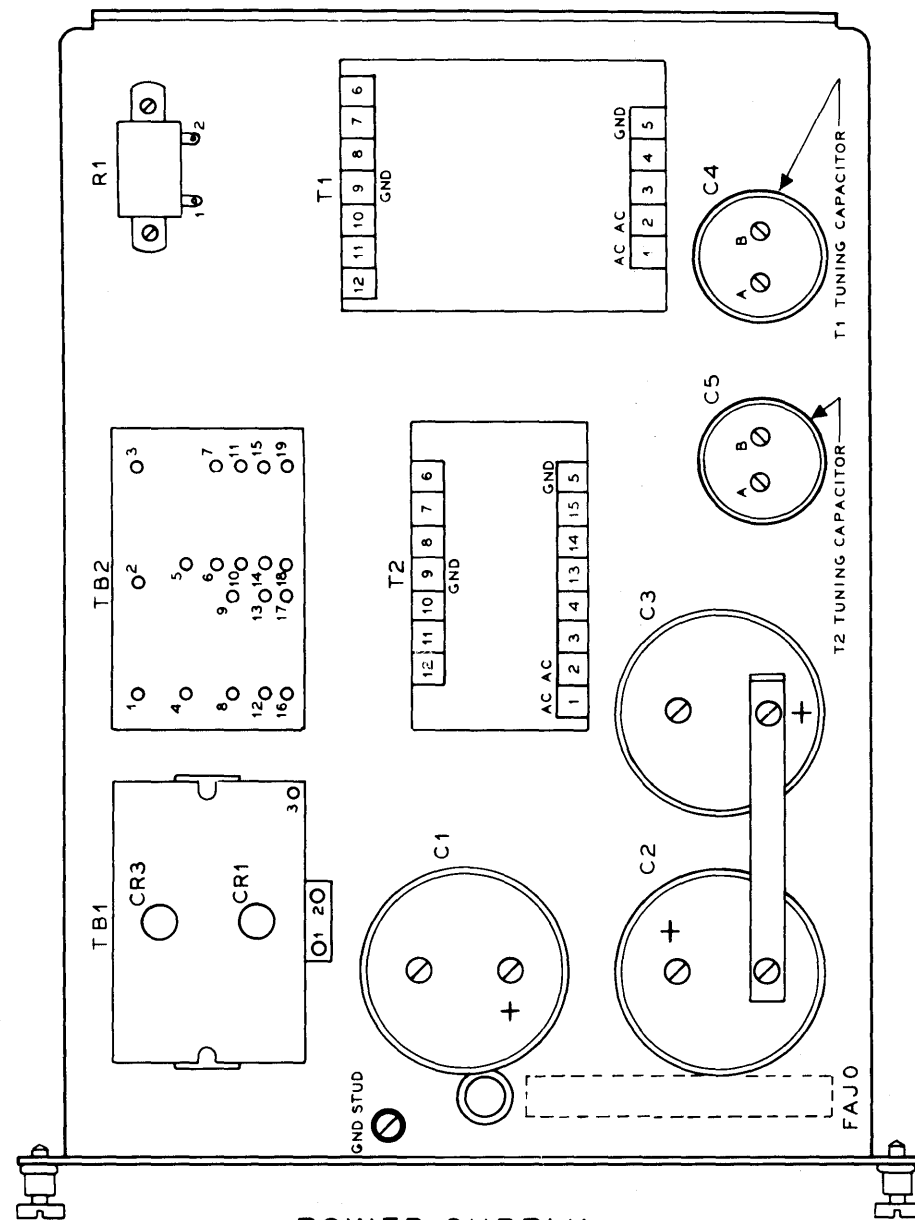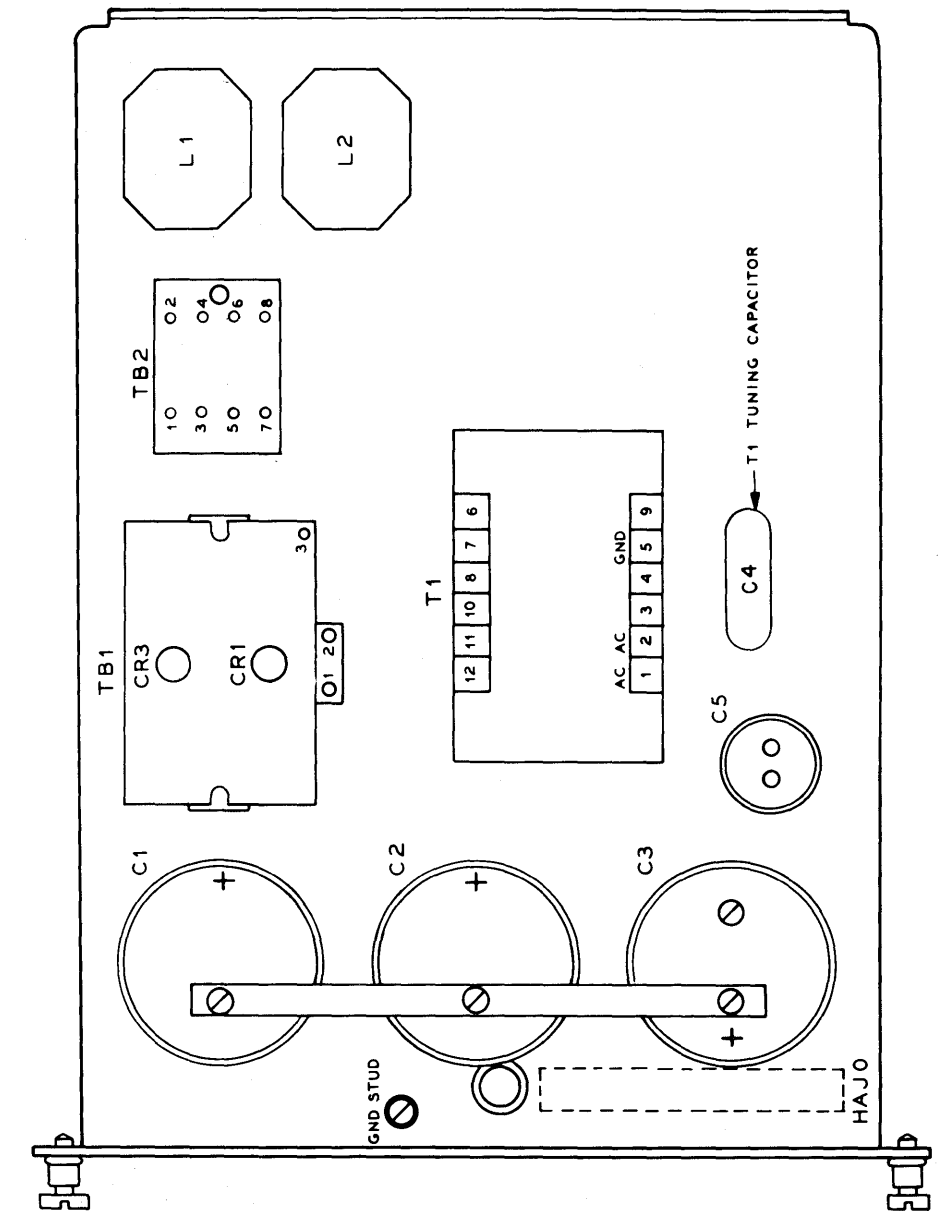
POWER SUPPLY

±100, -120 & 24VDC

FAJO

PIN		
1	+100VDC	(0.17 AMP)
2	-100VDC	(0.17 AMP)
3	-120VDC	(0.05 AMP)
4	-24VDC	(3.5 AMP)
5	GND	
7	AC ⎤ T1	
8	AC ⎦	
9	AC ⎤ T2	
10	AC ⎦	
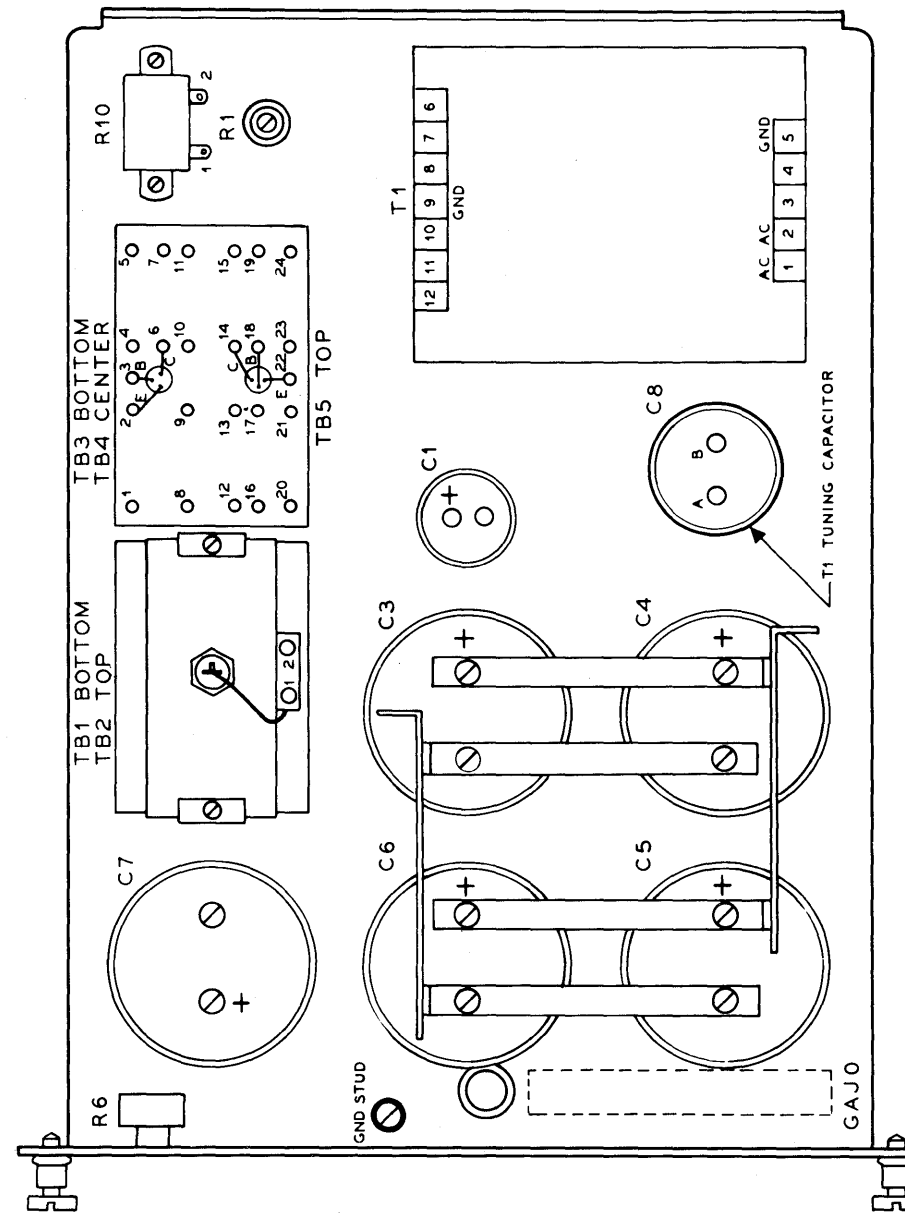
POWER SUPPLY

±12 & -4.5VDC

GAJO

PIN		
1	+12VDC	(.25 AMP)
2	-12VDC	(10 AMP)
4	-4.5VDC	(2 AMP)
5	GND	
6	+20VDC	
7	AC ⎤ T1	
8	AC ⎦	

POWER SUPPLY

±20VDC

HAJO

PIN		
1	+20VDC	(1 AMP)
2	-20VDC	(0.5 AMP)
3	GND	
7	AC ⎤ T1	
8	AC ⎦	

FIGURE 6.9-4
ELECTRONICS UNIT
POWER SUPPLIES COMPONENT LOCATOR

6.11   RIN INDEX FOR DISK FILE ELECTRONICS UNIT 11980224

RIN NO.	INSTALL. TIME IN HOURS	PRE-REQUISITE	UNITS AFFECTED	DESCRIPTION
4802	0.5	None	103 ⇒ 127	Undervoltage fail sensor pkg. improvement.
4804	1.0	None	103 ⇒ 127	Compressor sw. sup. network improvement.
4807	2.0	None	103 ⇒ 127	Compressor line shield & filter improvement.
4809	0.5	None	103 ⇒ 127	-20V supply fuse change.
4812	2.5	None	103 ⇒ 127	Document update & wiring compatibility change.
4823	0.5	None	103 ⇒ 127	E.U. Backplane noise reduction.

RIN INDEX FOR DISK FILE 60 CYCLE POWER KIT 11106739

RIN NO.	INSTALL. TIME IN HOURS	PRE-REQUISITE	UNITS AFFECTED	DESCRIPTION
4818	0.5	None	103 ⇒ 175	Corrects wiring error to convenience outlet.

INDEX - SECTION VII

7.1 INSTALLATION

This procedure begins after the E.U. has been unpacked and is in place. For pre-installation information, refer to Installation Planning, Field Facilities, Pasadena, California.

PRIMARY POWER

Primary power may be supplied from a 208 or 230VAC, single phase, 60 cycle, four-wire source (two AC legs, one neutral and a building ground). Power cabling from source to the E.U. must be furnished by the customer. The number of Storage Modules attached to an E.U. will determine the power cable size and circuit breaker rating. An E.U. with one S.U. will require 35 amps at a maximum load. Each additional Module will require another 8 amps.

Refer to Figure 7.1-1

The power cable should be routed under the E.U. and enter through the small access hole provided in the base. The two AC legs and neutral line enter the 70 amp circuit breaker box through the knock-out hole in the back; the two AC legs go to terminals 1 and 2 and the neutral line goes to terminal 3. The power cable building ground routes directly to terminal 7 of the line filter L3.

An auto-transformer is provided to allow use of 208 or 230VAC inputs. The wire from terminal 4 of L3 must be connected to the proper terminal on the auto-transformer; to auto-transformer terminal 1 for 208VAC or to auto-transformer terminal 3 for 230VAC.
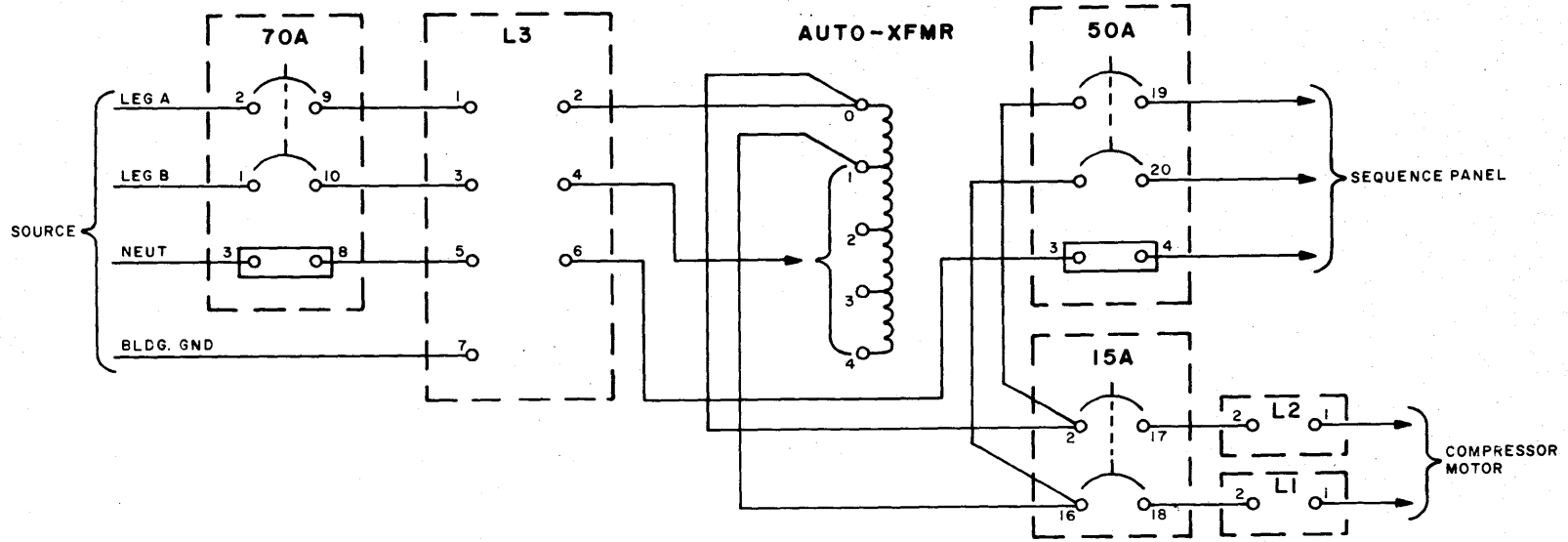
LOGIC CABLES

There is one logic cable connecting the D.F.C.U. to the E.U. It should be routed under the E.U. and enter through the hole provided. The two-piece metal plate covering the hole must be removed in order to get the Winchester connector through the base. This plate should be replaced after the cable is connected.
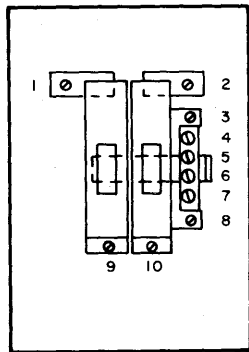
MODULE CABLING

The following cables, plus an air line to the first S.U., are routed through the access hole in the side of the E.U.
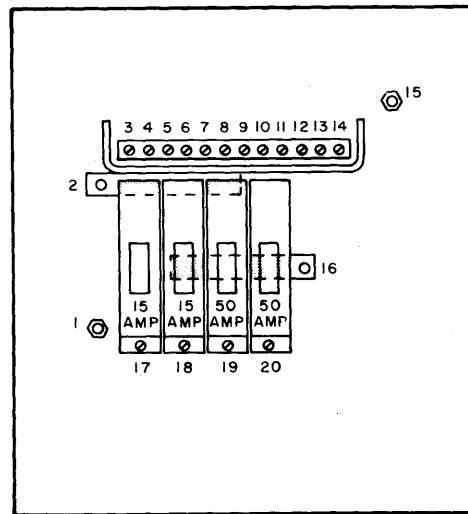
Power

From sequence panel (Rack E) to each module:

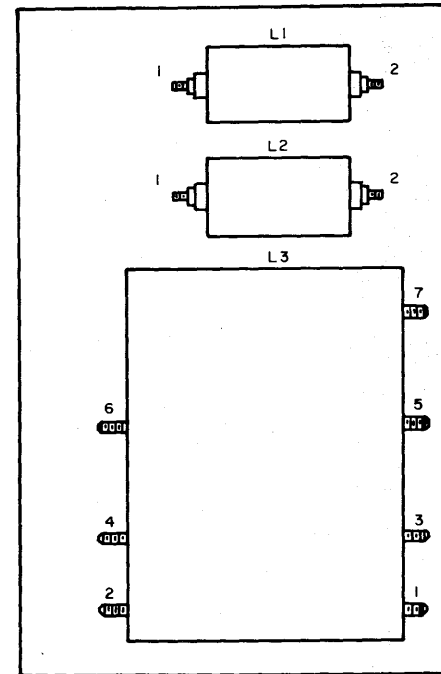FIGURE 7.1-1
PRIMARY POWER CONNECTIONS

NOTE:
TERMINAL 2 COMMON TO TERMINALS
17 & 19. TERMINAL 16 COMMON TO
TERMINALS 18 & 20.

70 AMP
CIRCUIT BREAKER

15 & 50 AMP
CIRCUIT BREAKER

INPUT LINE FILTER

    1 AC cable (Cannon)

    1 DC cable (quad)

    1 ground wire

Logic

From E.U. logic gate to first S.U.:

    3 head select cables (Amphenol C37)

    1 logic cable (quad)

Complete the Module installation before PRE-POWER CHECK. Refer to Section 7 of the B475 Technical Manual.

PRE-POWER CHECKS

    1. Pull power supply racks out and check for loose nuts, bolts, terminal board screws, etc.

    2. Check for tightness and correct location of plug-ins on logic rack. Refer to Figure 6.9-3.

    3. Make sure drain cock on bottom of sediment bowl is tight.

INITIAL POWER-ON

70 amp circuit breaker ON - AC to 15 and 50 amp circuit breakers.

15 amp circuit breaker ON - Air compressor, garage fans and -24 relay power.

                                        Relay Supply indicator on.

50 amp circuit breaker ON - Module motor power.