FIELD ENGINEERING TECHNICAL MANUAL

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Burroughs

B 470

DISK FILE CONTROL ASSEMBLY

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INDEX - SECTION I

1 INTRODUCTION

1.1 GENERAL DESCRIPTION

The Disk File Subsystem shown in Figure 1.1-1 is a high speed random access, large capacity storage device. A read/write head for every track allows access to any record in the file in an average time of 20 milliseconds. There is no arm positioning so access time involves only a factor called latency. Latency is the time required for the disk to revolve to the point where the selected head is located at the beginning of the record specified by the instruction/descriptor. Maximum latency is 40 milliseconds which is one complete revolution at 1500 rpm.

The Disk File Subsystem contains the equipment shown in Figure 1.1-2. The External Control shown to the left of the B450 cabinet is the computer system. This could be the B200 Processor or the B5000 I/O.

The B450 cabinet houses the B470 Disk File Control Unit (D.F.C.U.). If the D.F.C.U. is used with the B200, it is called the B247; if the D.F.C.U. is used with the B5000, it is called the B5470. The unit numbers are different because they include the additional logic required in the respective computer systems.

One D.F.C.U. is able to control from one to ten B471's. The B471 has been called a "storage unit", but will be referred to as the Disk File Electronics Unit (E.U.). Each E.U. contains the electronic circuitry necessary to control from one to five B475's. The B475 Disk File Storage Unit (S.U.) is also referred to as a Storage Module. Each S.U. contains four magnetic disks.

NOTE

An E.U. and the first S.U. form a combination called a B472.

SEGMENT OPTIONS

Information in the Disk File Subsystem is handled in segments. A segment is a group of 96, 240 or 480 six-bit characters. Each segment has a separate address which is written in the timing tracks of the disk. The option is chosen by the customer and is implemented at the factory during manufacture. Segment options cannot be changed in the field.

The D.F.C.U. is able to handle any of the three options. The segment option determines where the information is to be physically located on the disks. The S.U. option is indicated by sending the two logic levels, CS1L/ and CS2L/, through the E.U. to the D.F.C.U. where the levels determine the correct logic gating to access the required area on the disk.

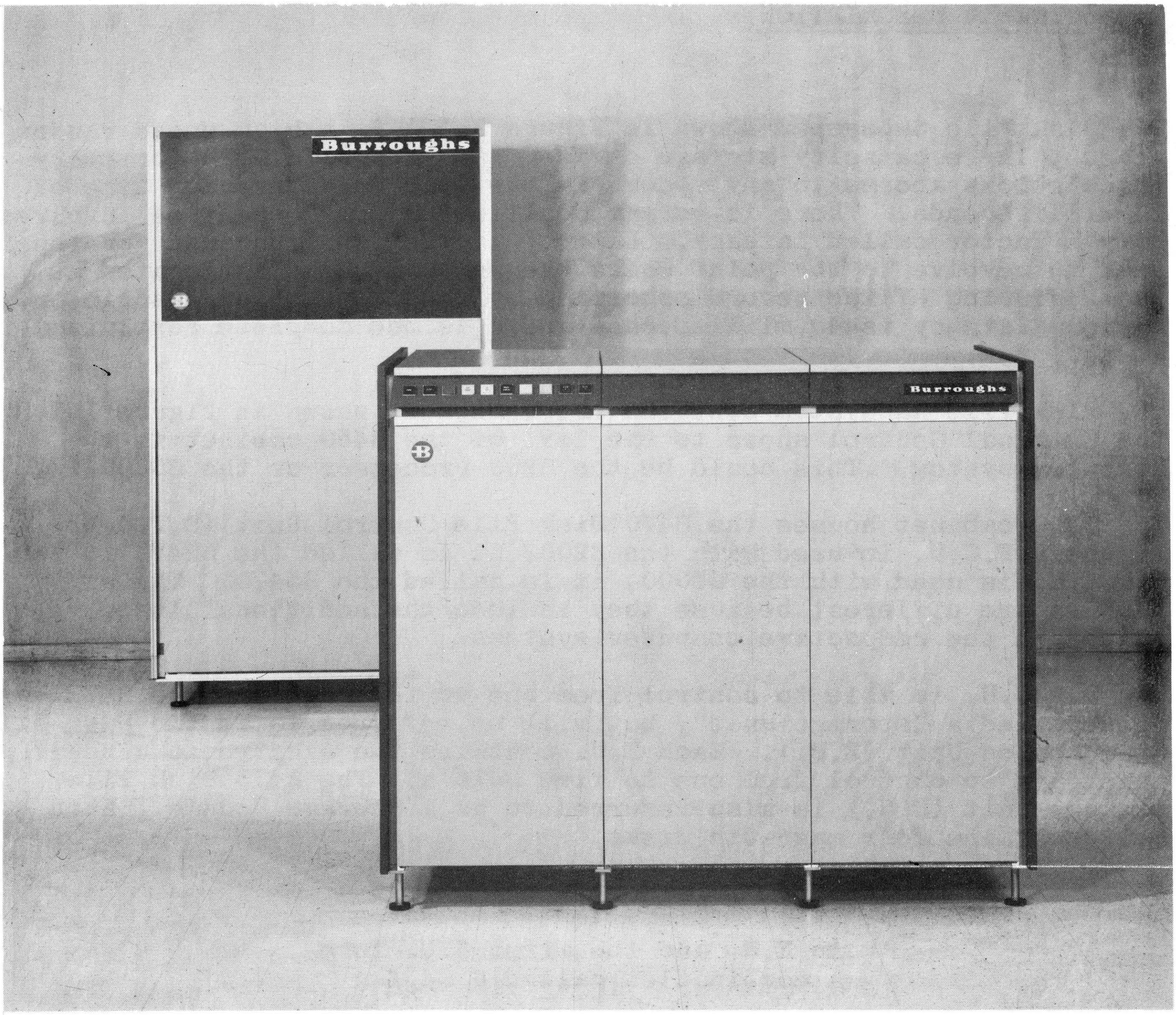


FIGURE 1.1-1
DISK FILE SUBSYSTEM

The CSnL/ levels are called the Characters per Segment Levels and indicate the segment options as follows:

CS1L/ false and CS2L/ false: 96 characters per segment
CS1L/ true and CS2L/ false: 240 characters per segment
CS1L/ false and CS2L/ true: 480 characters per segment

"False" is approximately ground potential and "true" is -4.5V.

Information is transferred to and from the Disk File Subsystem through the D.F.C.U. It is physically connected as shown in Figure 1.1-3.

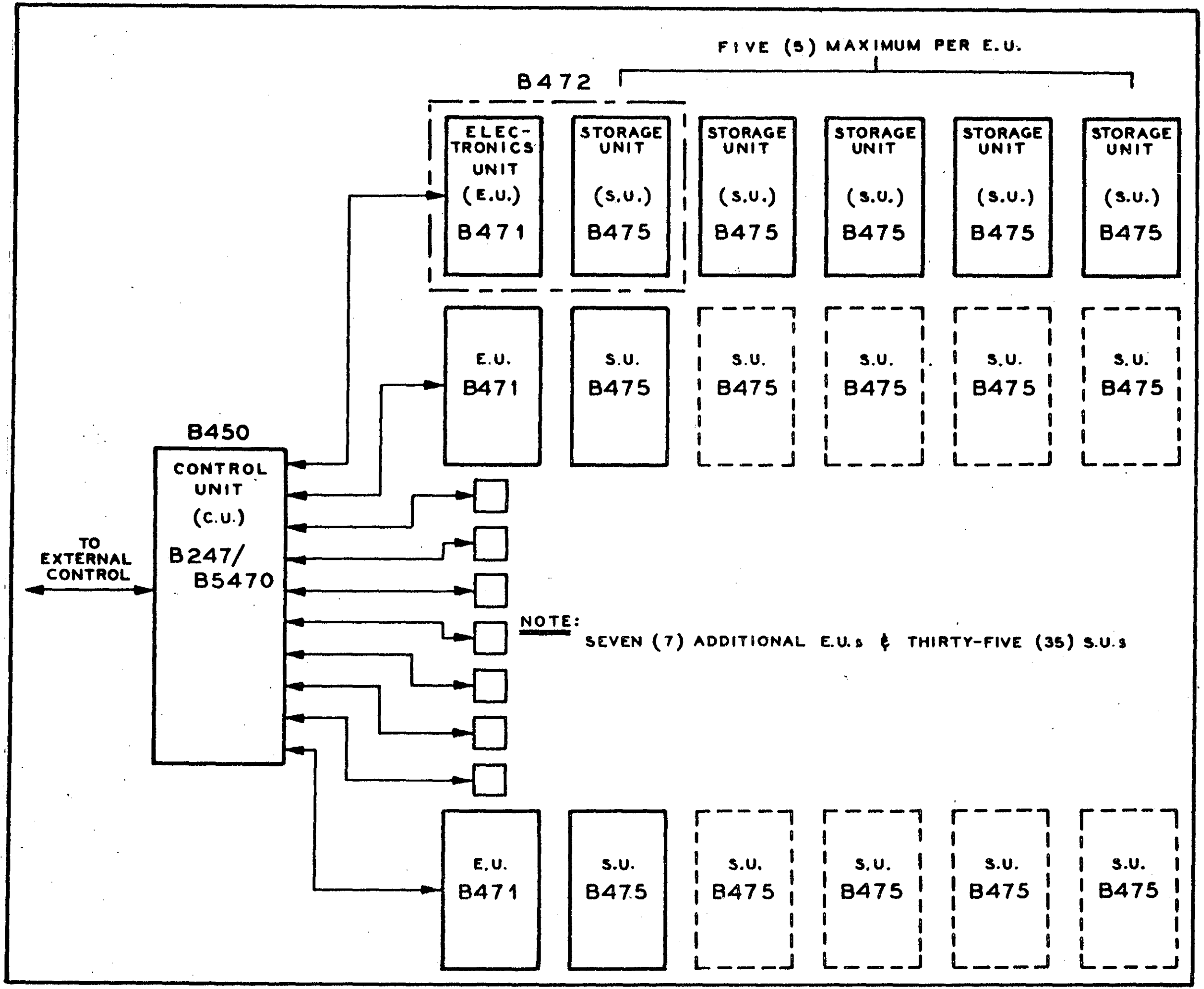


FIGURE 1.1-2
BLOCK DIAGRAM OF DISK FILE SUBSYSTEM

The D.F.C.U. is a gate mounted in the B450 cabinet and the layout is illustrated in Figure 1.1-4. There is a control and display panel at the tope of the gate.

Figure 1.1-5, D.F.C.U. Display Panel, and Figure 1.1-6, Subsystem Address Flow, should be referred to during the following explanation.

At the beginning of a Read, Read Check or Write Disk File operation, the Disk File Address is shifted serially by character into the CIF's/ØB. Because it is File Address Select Time (FASL), the characters are shifted into the Number of Segments (N) Register. From N, the 1-2-4-8 bits are shifted into the LSD position of the Address (A) Register and then through the A Register. The Disk File Address is followed by the number of segments to be read/written. The first digit sent to the D.F.C.U. is the E.U. Designate Digit. This digit is shifted into the MSD position of the A Register when the "Number of Segments" digit is shifted into the N Register.

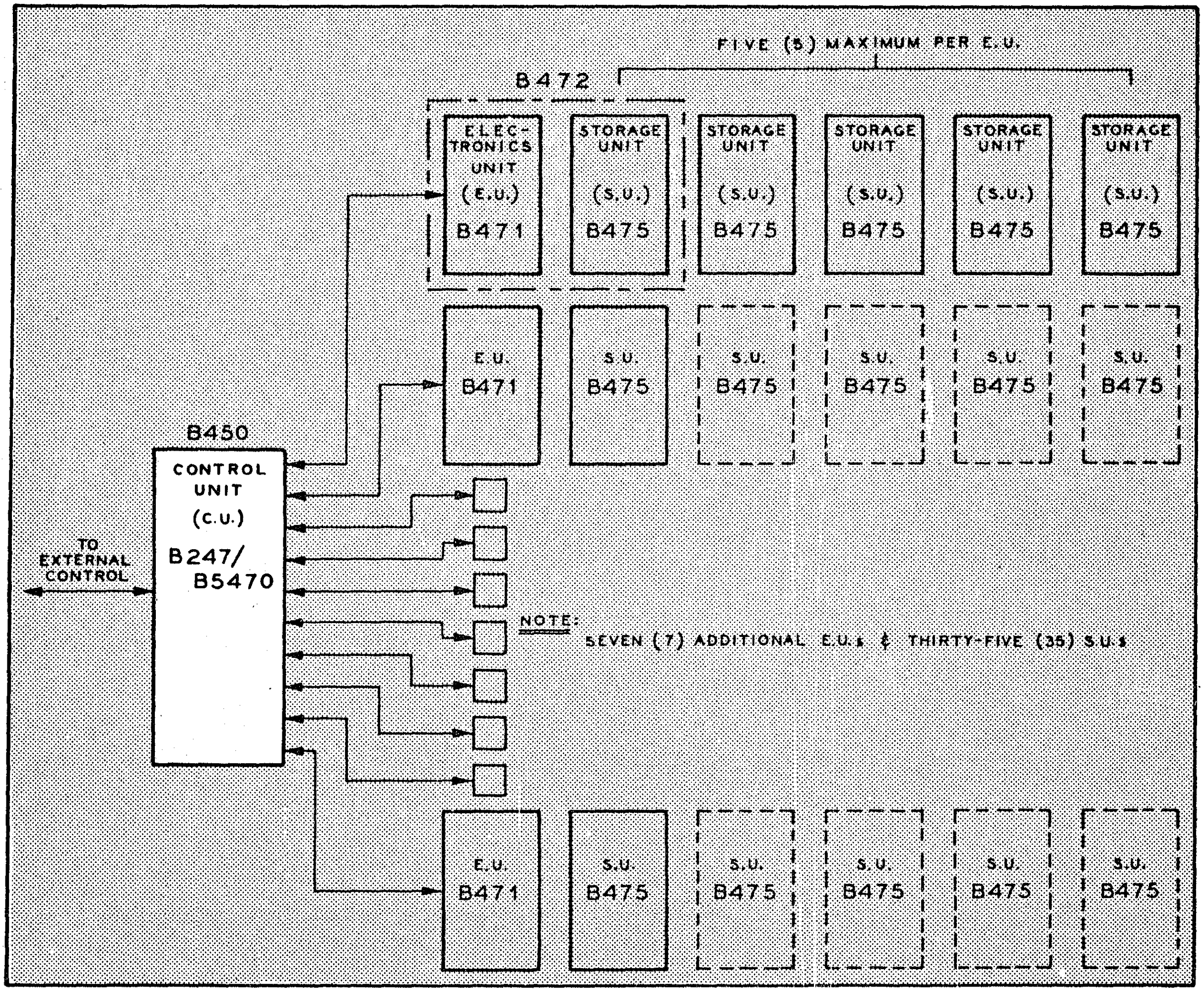


FIGURE 1.1-3
D.F.C.U. IN DISK FILE SUBSYSTEM

The N Register is counted down during the Disk File Operation and, when it reaches zero, signals the end of the operation.

The transfer rate between the D.F.C.U. and the External Control can be higher than the B200 Processor can handle so the B Register is used to provide a four character buffer. The B5000 does not need a buffer, but the LSD position of the B Register is used for address comparison.

The D.F.C.U. has parity checking circuits to detect errors in the transfer of the Disk File Address and information to and from the D.F.C.U. A longitudinal parity character is written on the disk after each word. The LP Register is used to generate and check this character.

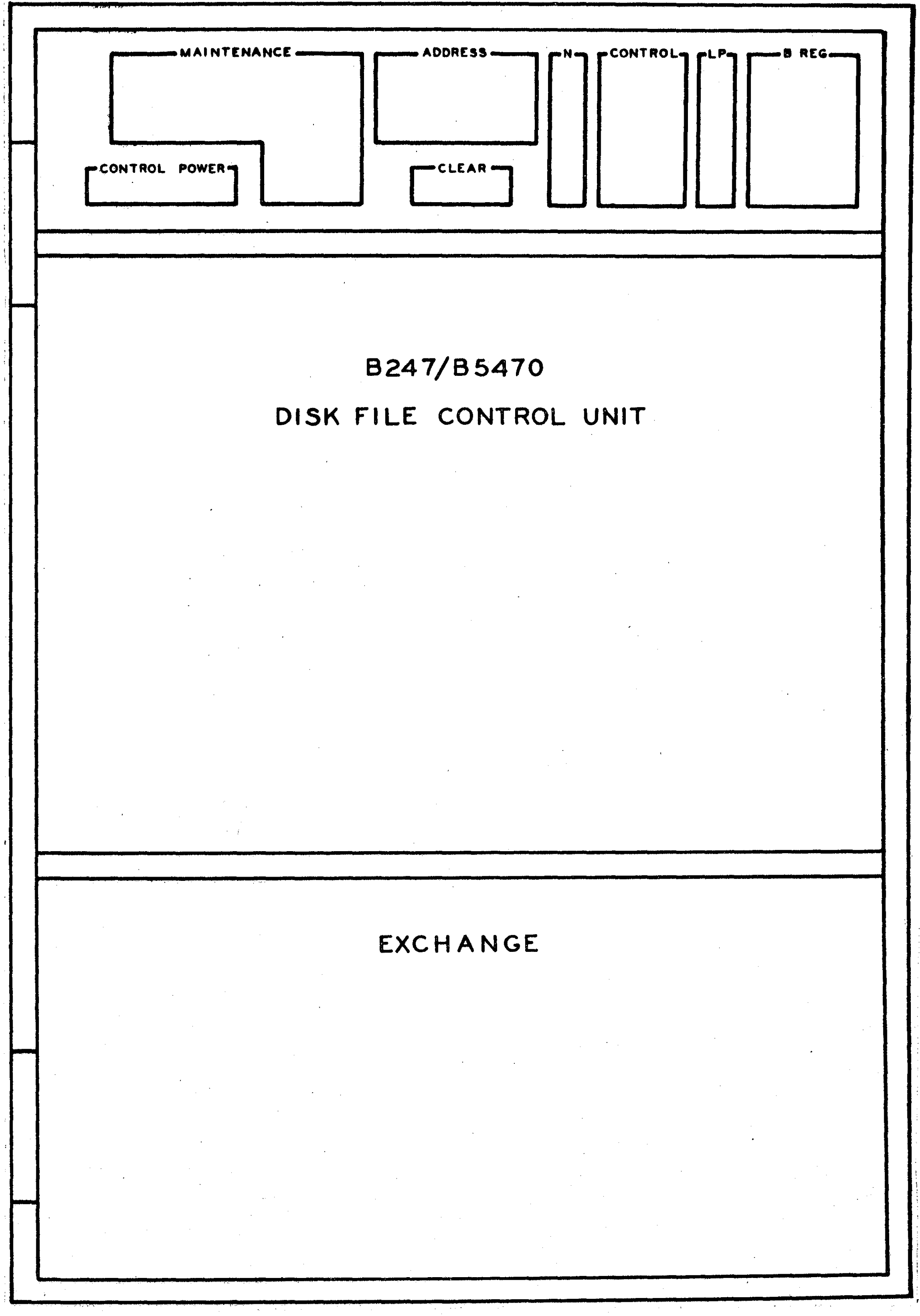


FIGURE 1.1-4
D.F.C.U. LAYOUT

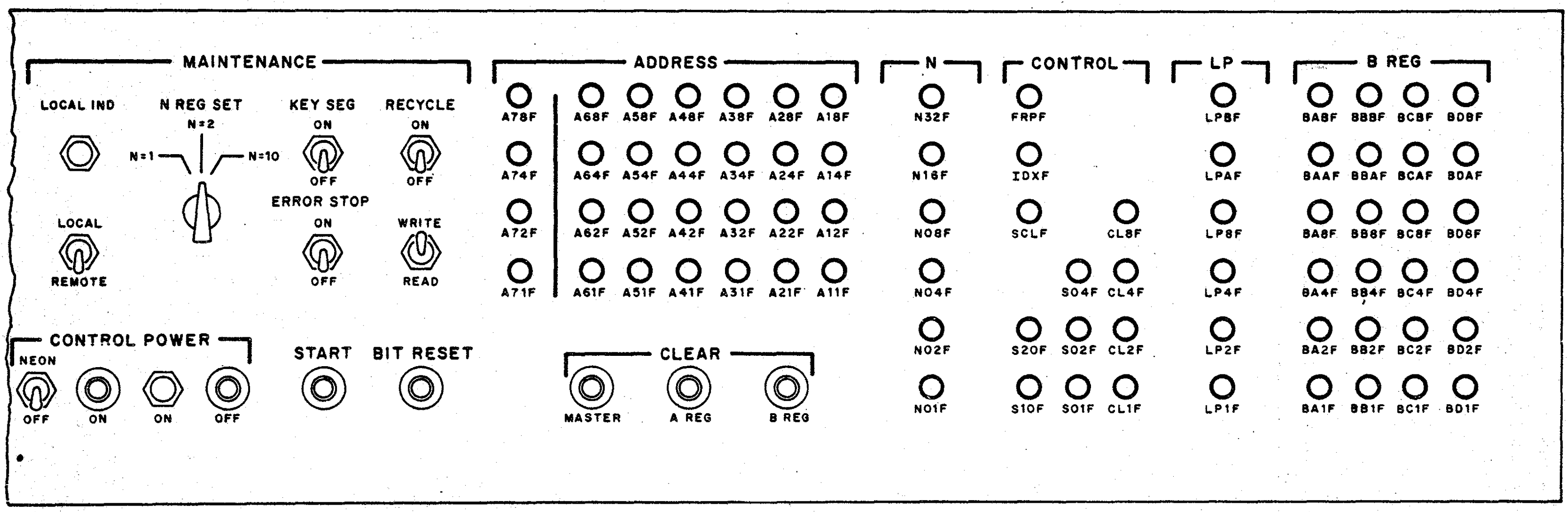


FIGURE 1.1-5
D.F.C.U. DISPLAY PANEL

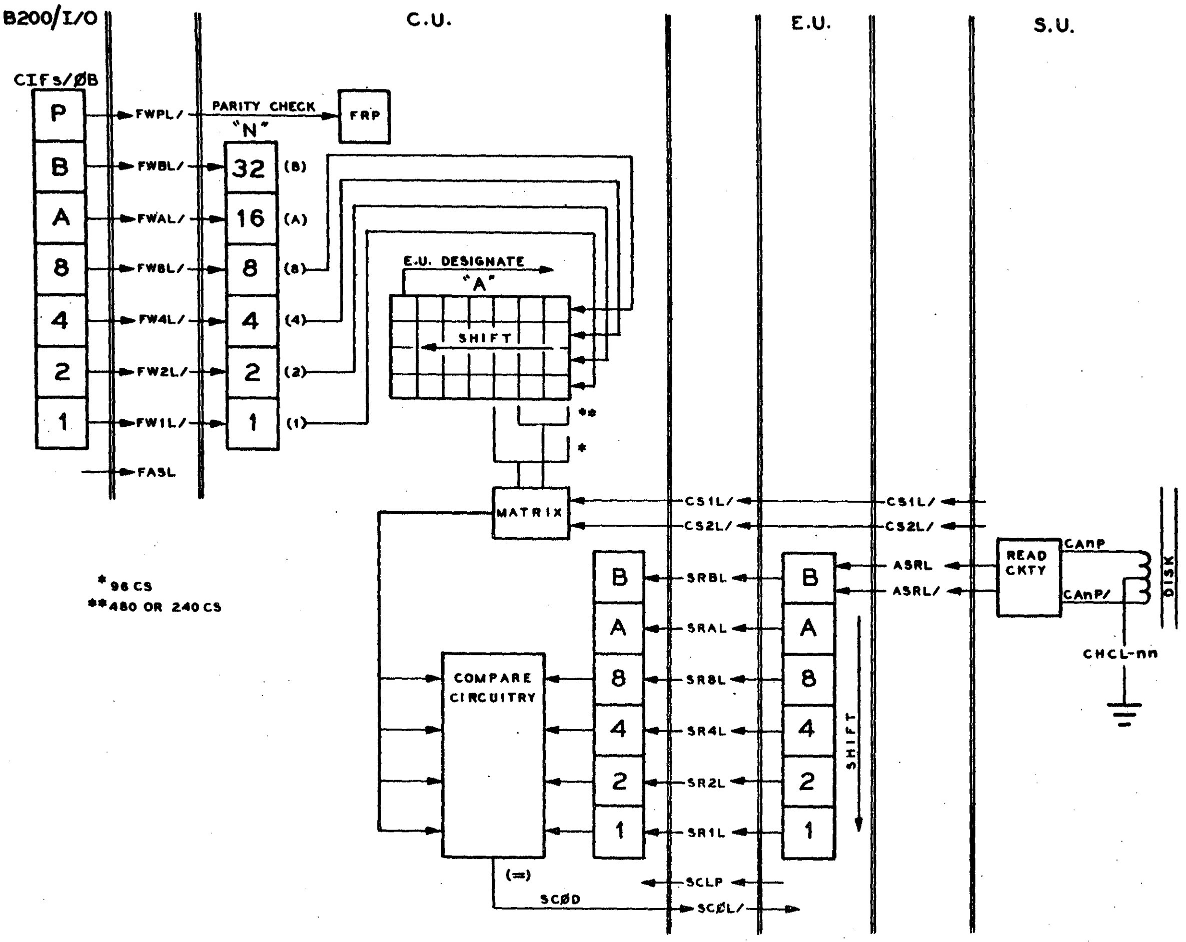


FIGURE 1.1-6
SUBSYSTEM ADDRESS FLOW

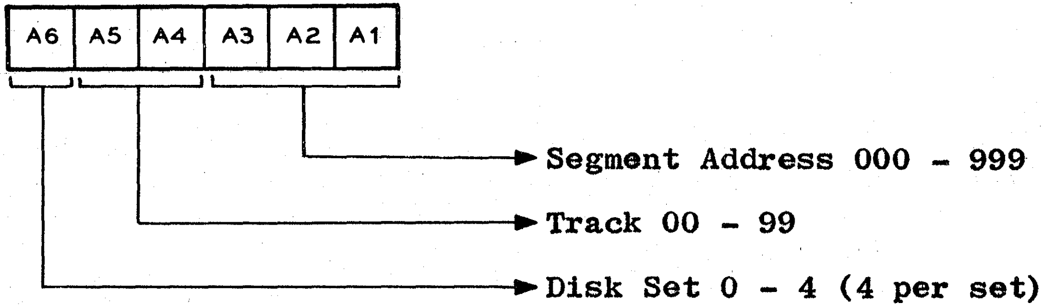
DISK FILE ADDRESSES

A Disk File Address consists of seven decimal numbers. The seven digits are shifted into the A Register of the D.F.C.U. as shown in Figure 1.1-6.

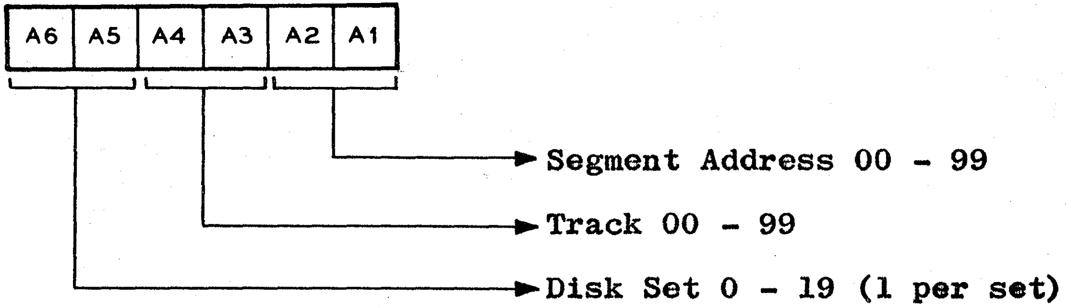
The A Register output levels are gated by the 96CS, 240CS or 480CS levels, developed from CS1L/ and CS2L/, for the correct address decoding and, in turn, provide the logic levels to the E.U. to select the required address.

The A7 digit of the Disk File Address indicates the designated E.U.; 0 through 9 being E.U. 1 through 10. The other digits of the Disk File Address have the following significance:

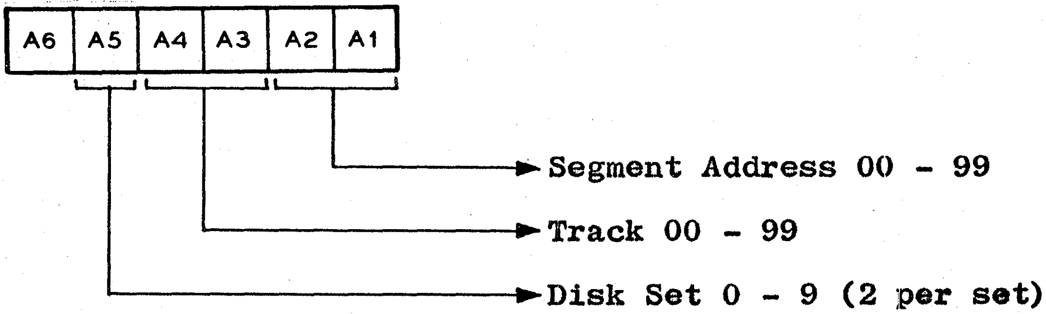
96CS



240CS



480CS



The limits of the Disk File Addresses with the different segment options are as follows: (Not including A7 which designates the E.U.)

96CS	000000 ⇉ 499999
240CS	000000 ⇉ 199999
480CS	000000 ⇉ 099999

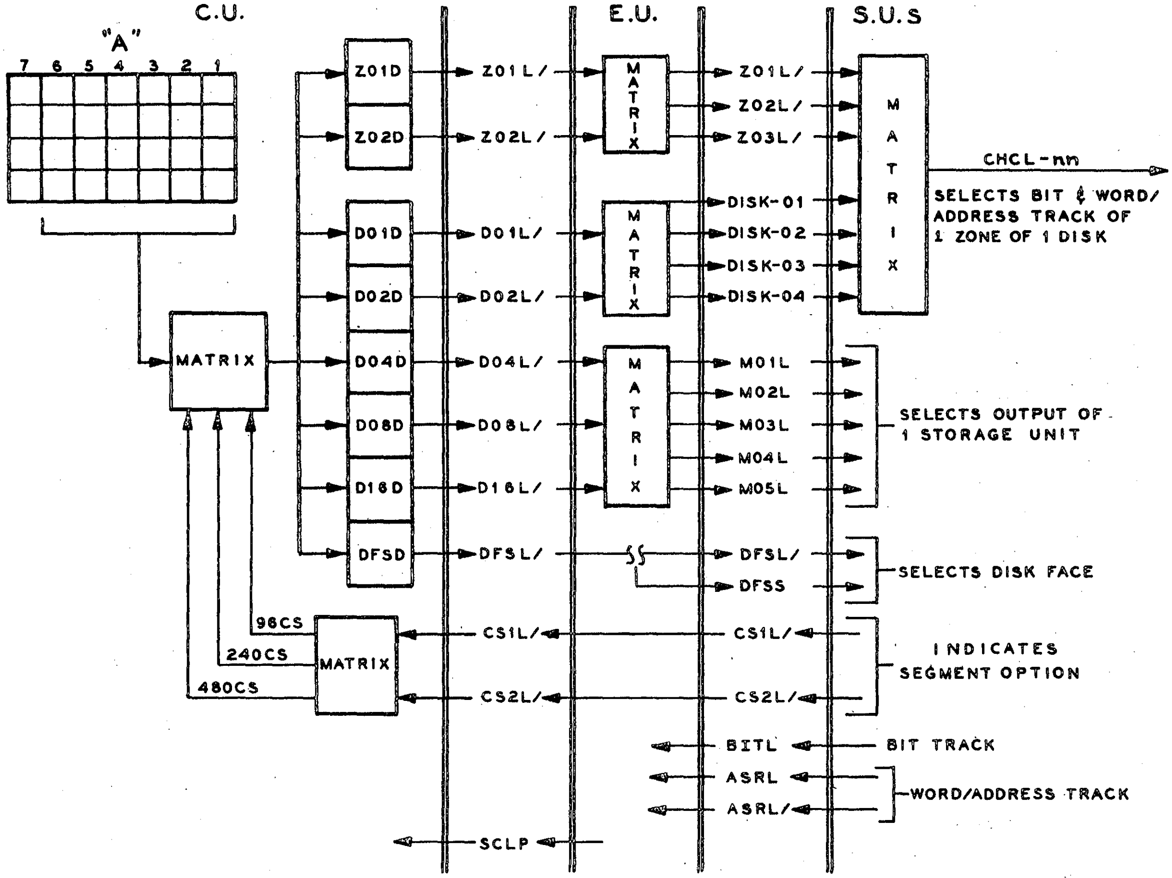


FIGURE 1.1-7
BIT AND WORD/ADDRESS TRACK SELECTION

The decoding of the address produces the logic levels shown in Figure 1.1-7 and Figure 1.1-8. Figure 1.1-7 shows the selection of the timing tracks of the required disk and Figure 1.1-8 shows the selection of the information track.

With the selection of the timing tracks, address digits are read from the disk as shown in Figure 1.1-6 and compared against the segment address contained in the A Register. If they are equal, the level SC0L/ is sent to the E.U. to start the active operation.

During a WRITE operation, the information written on the disk follows the path shown in the upper part of Figure 1.1-9 and, during a READ operation, the information read from the disk follows the path shown in the lower part.

The characters transferred to or from the disk may be Binary or BCL. There is no encoding or decoding of the characters in the D.F.C.U.

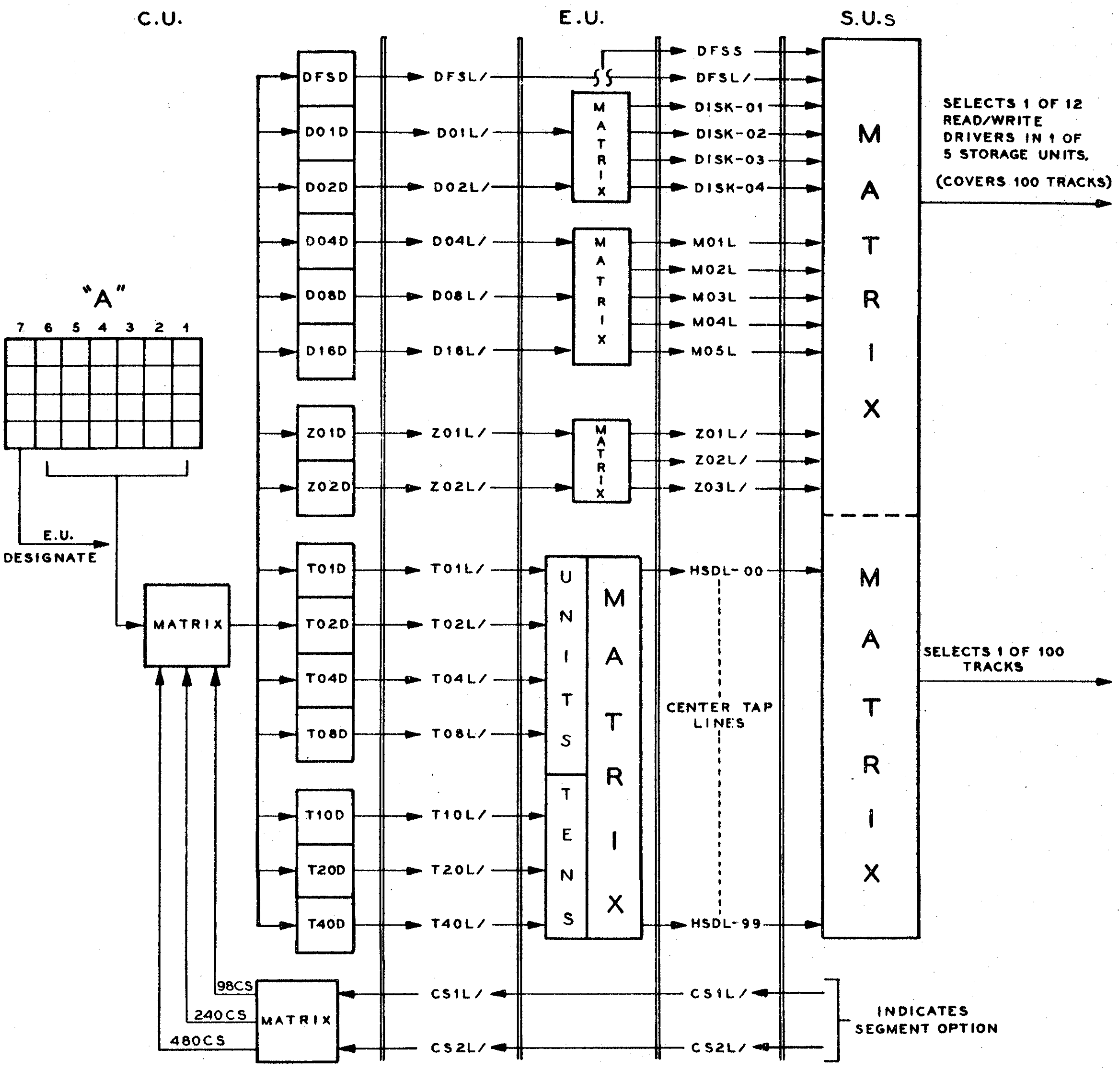


FIGURE 1.1-8
INFORMATION TRACK SELECTION

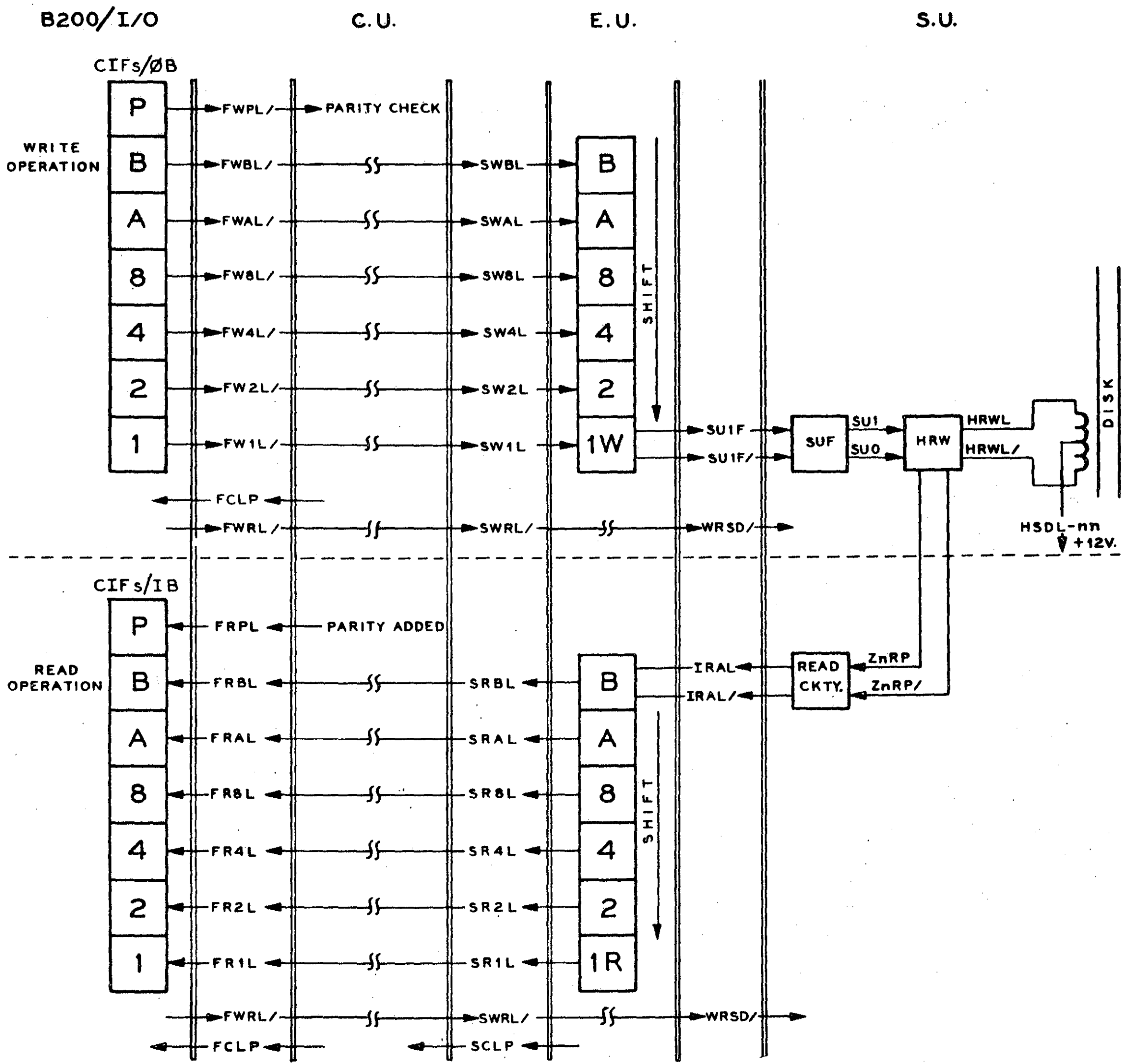


FIGURE 1.1-9
SUBSYSTEM INFORMATION FLOW

DISK FILE SUBSYSTEM CAPACITY

	MAX ALPHA CHARACTERS PER	MAX SEGMENTS PER	MAX DISKS PER	MAX STORAGE MODULES PER	MAX DISK FILE ELEC. UNITS PER	MAX DISK FILE CONT. UNIT PER
SEGMENT	96 240 480					
DISK	2,400,000	5,000 480 CHAR. 10,000 240 CHAR. 25,000 96 CHAR.				
MODULE	9,600,000	20,000 480 CHAR. 40,000 240 CHAR. 100,000 96 CHAR.	4			
ELEC. UNIT	48,000,000	100,000 480 CHAR. 200,000 240 CHAR. 500,000 96 CHAR.	20	5		
CONT. UNIT	480,000,000	1,000,000 480 CHAR. 2,000,000 240 CHAR. 5,000,000 96 CHAR.	200	50	10	
B200	480,000,000	1,000,000 480 CHAR. 2,000,000 240 CHAR. 5,000,000 96 CHAR.	200	50	10	1
B5000	960,000,000	2,000,000 480 CHAR. 4,000,000 240 CHAR. 10,000,000 96 CHAR.	400	100	20	2

1.2 EQUIPMENT SPECIFICATIONS

Specifications for size, weight, space, power and air conditioning are covered under Section 1.2 of the B450 Technical Manual.

Maximum cable length to Processor - 50 feet.

Maximum cable length to any Electronics Unit - 50 feet.

1.3 INSTRUCTIONS AND DESCRIPTORS

B200 OPERATION (B273/283)

Disk File Write DFW

O M N AAA BBB CCC

CCC	Branch on E.U. not ready
BBB	MSD Memory Address of information to be written
AAA	MSD Memory Address of Disk File Address
N	Number of Segments to be written; 0 - 9, where 0 = 10 segments
M	Must be zero (0) to indicate Disk File Write Operation
O	Must be "K" to indicate Disk File Operation

Notes

1. Detection of Disk File Address transfer error terminates the operation and no information is written.
2. Information is written in BCL Code and all characters can be used.
3. An attempt to write in a locked out area terminates the operation.
4. Detection of an information transfer error does not terminate the operation.
5. The Comparison Indicators are not affected.

Disk File Read DFR

O M N AAA BBB CCC

CCC	Branch on E.U. not ready
BBB	MSD Memory Address where information is to be stored
AAA	MSD Memory Address of Disk File Address
N	Number of Segments to be read; 0 - 9, where 0 = 10 segments
M	Must be "2" to indicate Disk File Read Operation
O	Must be "K" to indicate Disk File Operation

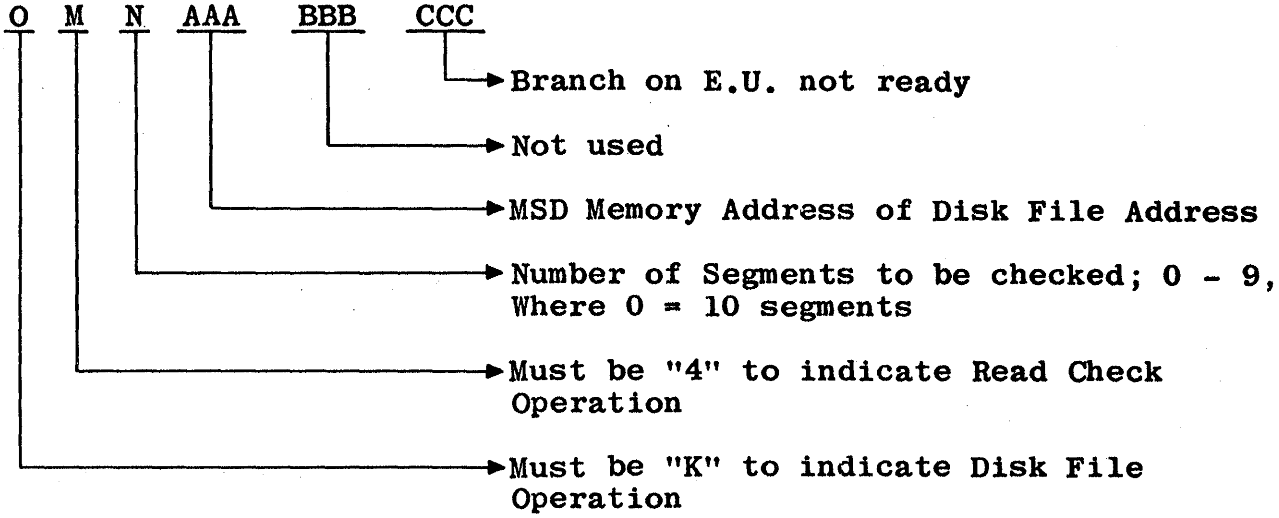
Notes

1. Detection of Disk File Address transfer error terminates the operation and no information is read.

2. Detection of an information transfer error does not terminate the operation.

3. The Comparison Indicators are not affected.

Disk File Read Check DFC



O M N AAA BBB CCC

CCC → Branch on E.U. not ready

BBB → Not used

AAA → MSD Memory Address of Disk File Address

N → Number of Segments to be checked; 0 - 9, Where 0 = 10 segments

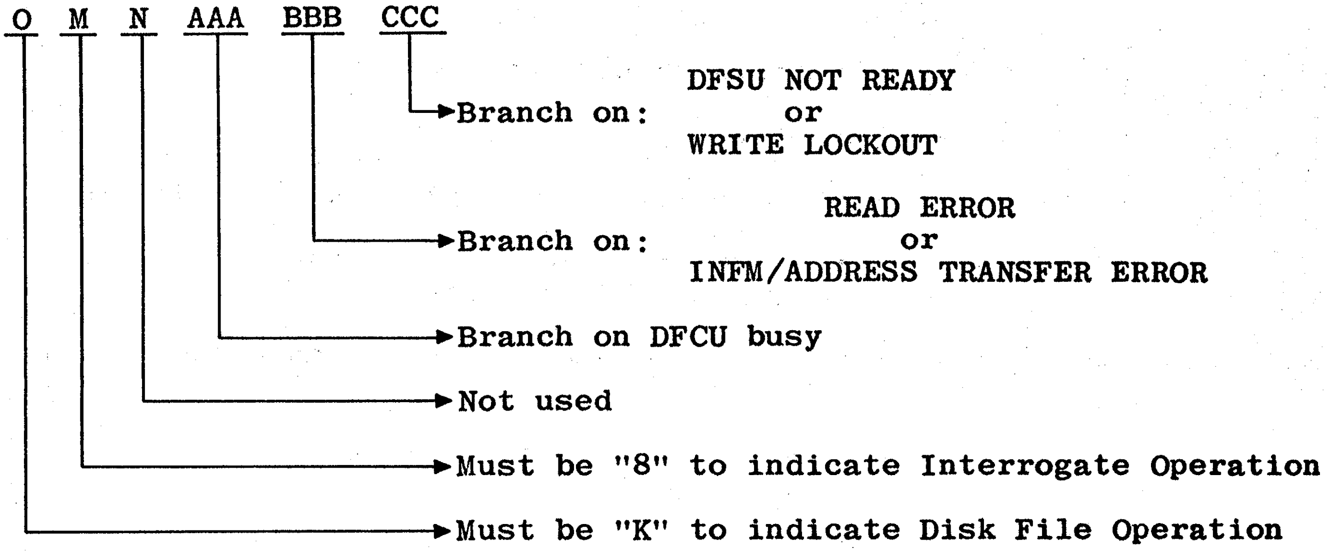
M → Must be "4" to indicate Read Check Operation

O → Must be "K" to indicate Disk File Operation

Notes

1. This instruction transfers the Disk File Address and the number of segments to the D.F.C.U. and then the B200 operation is terminated.
2. The Comparison Indicators are not affected.

Disk File Interrogate DFI


O M N AAA BBB CCC

CCC → Branch on: DFSU NOT READY or WRITE LOCKOUT

BBB → Branch on: READ ERROR or INFM/ADDRESS TRANSFER ERROR

AAA → Branch on DFCU busy

N → Not used

M → Must be "8" to indicate Interrogate Operation

O → Must be "K" to indicate Disk File Operation

Notes

1. Branch Priority:

    a. Disk File Control Busy
    b. Error
    c. Write Lockout or Not Ready

2. The Comparison Indicators are not affected.

Information transfer to and from the Disk File Subsystem is in BCL Code. All characters are allowed.

The maximum number of segments that can be read or written by the B200 is ten indicated by the N Variant equal to zero. In the 480CS option, this would consist of 4800 characters.

A sequence of instructions to update a file in the Disk File Subsystem could be as follows:

DFR	Read old record.
DFI	Interrogate for read errors.
DFW	Write updated record.
DFI	Interrogate for lockout or transfer error.
DFC	Check for parity errors.
DFI	Interrogate until D.F.C.U. is finished.

NOTE

When formulating a Disk File Address, zeros (0) and blanks (b) are not interchangeable. A blank constitutes a forbidden combination.

B5000 DESCRIPTORS AND OPERATION

48	45					30	27	24	21		15				
		41													
46		40			31		25			16					1

48 = Flag Bit; 1 if Descriptor

46 = Presence Bit; 1 if Core Memory assigned

45 → 41 = Unit Designate

BCD 6 = DFCU 1
or 14ø (ø = octal)

BCD 12 = DFCU 2
or 30ø

40 → 31 = Word Count (Values of 0000 - 1777ø)

30 = 1 Read Check - Inhibit Data Transfer

27 = 1 for Binary, 0 for Alpha (BCL) translation

25 = 1 to use Word Counter Override

24 = 1 for Disk File Read, 0 for Disk File Write

21 → 16 = Number of Segments (Values of 00 - 77ø, where 77ø = 63 segments)

15 → 1 = Core Memory Address**

****NOTE:**

Last seven (7) characters of first word addressed by 15 - 1 contain Disk File Address; first character is not used.

DESCRIPTOR COMBINATIONS

40 - 31 WORD COUNT	30	27	25	24	21 - 16 SEGMENT COUNT "n"	OPERATION
	1				$1 \leq n \leq 770$	READ CHECK
		0	0	1	$1 \leq n \leq 770$	Read with BCL translation; ignore Word Count
		1	0	1	$1 \leq n \leq 770$	Read without translation (Binary); ignore Word Count
$1 \leq WC \leq 17770$		0	1	1	$1 \leq n \leq 770$	Read with BCL translation; Word Count Override
$1 \leq WC \leq 17770$		1	1	1	$1 \leq n \leq 770$	Read without translation; Word Count Override
		0	0	0	$1 \leq n \leq 770$	Write with BCL translation; ignore Word Count
		1	0	0	$1 \leq n \leq 770$	Write without translation; ignore Word Count
$1 \leq WC \leq 17770$		0	1	0	$1 \leq n \leq 770$	Write with BCL translation; Word Count Override
$1 \leq WC \leq 17770$		1	1	0	$1 \leq n \leq 770$	Write without translation; Word Count Override
$WC = 0$			1			Interrogate

NOTE: The "0" and "1" are required where shown, and blanks are irrelevant.

DISK FILE RESULT DESCRIPTOR

	45							24	21	18	15				
		41						23	20						
		40			31			22	19	16					1

48 → 46 = 0

45 → 41 = Unit Designate

BCD 6 = DFCU 1
or 140

BCD 12 = DFCU 2
or 300

40 ⇛ 31 = Remaining Word Count

24 = 1 if Operation was Read, 0 if Operation was Write

23 = 1 if Read Check Error on prior operation

22 = 1 for Core Memory Address Error

21 = 1 if DFEU NOT READY, or an attempt to access non-existent Disk Address

20 = 1 if PARITY ERROR on transfer of data from Disk to I/O during Read Operation

19 = 1 if Core Memory Parity Error; Parity Error during: Disk File Address Transfer, or Data Transfer during Write Operation, to DFCU.

18 = 1 if DFCU NOT READY

16 = 1 if DFCU is busy with another I/O channel

15 ⇛ 1 = last address accessed + 1 for all Read/Write Operations or, initial address + 1 for Read Check and Interrogate Operations

Information to and from the Disk File Subsystem may be in BCL or Binary code; all characters may be used in both codes. The code is specified in bit 27 of the I/O Descriptor; zero for Alpha and one for Binary.

The number of segments is specified in bits 21 ⇉ 16 of the I/O Descriptor. The maximum number of segments that can be read/written by the B5000 is sixty-three. If the segment option is 480, this would amount to 30,240 characters or 3,780 B5000 words.

The general sequence of descriptors used could be as follows:

READ	Read old record.
WRITE n WORDS	Write updated record.
READ CHECK	Check information on disk for parity errors.
INTERROGATE	Check last operation.

During a Write operation, the I/O is connected for the entire operation. "I/O Finished" is produced when the I/O is released by the D.F.C.U. and the Result Descriptor has been stored. During a Read operation, Word Count Override can release the I/O before the D.F.C.U. has terminated its operation.

For a Read Check operation, the I/O transfers the Disk File Address and the number of segments to the D.F.C.U. The I/O then releases the D.F.C.U. for an independent operation. When the D.F.C.U. has completed the Read Check, an interrupt is produced.

The File Interrupt Pulse (FINP/) of D.F.C.U. 1 sets CCI15F of Central Control; D.F.C.U. 2 sets CCI16F. The Disk File Subsystem will not usually be accessed once a Read Check has been initiated until the D.F.C.U. produces FINP/.

MAINTENANCE FACILITIES

The Disk File Subsystem can be checked both on-line and off-line. The method of checking in an off-line status is detailed in Section 6 of this manual. On-line, the customer information may be retained and read/write checking can be performed with a test routine using the maintenance segments. The maintenance segments are provided specifically to enable the field engineer to check the read/write circuitry without destroying any of the customer's information that may be on the disks.

1.4 GLOSSARY

DISK FILE CONTROL INTERCONNECTION

		TO/FROM EXTERNAL
EMG-OFF	Emergency Power Off	From
FASL	File Address Select Level	From
FBIL	File Binary Information Level	From
FCBL/	File Control Busy Level	To
FCLP	File Clock Pulse	To
FCRL/	File Control Ready Level	To
FDTL/	File Data Transfer Control Line	From
FERL/	File Error Received Level	To
FINP/	File Interrupt Pulse (B5000)	To
FR1L FR2L FR4L FR8L FRAL FRBL FRPL	File Read Information Lines	To
FSRL/	File Storage Ready Level	To
FWCL/	File Word Coincidence Level	To
FWLL/	File Write Lockout Level	To
FWRL/	File Write Level	From
FW1L FW2L FW4L FW8L FWAL FWBL FWPL	File Write Information Lines	From
PC-COM	Power Control Common	From
PWR-OFF	Power Off	From

		TO/FROM EXTERNAL
PWR-ON	Power On	From
SIDL2/	System Identification Level 2	From

		TO/FROM E.U.
CS1L/ CS2L/	Characters per Segment Levels	From
DACL	Designate Achieved Level (from Exchange)	
DFSL/	Disk Face Select Line	To
D01L/ D02L/ D04L/ D08L/ D16L/	Disk Select Lines	To
EMG-PWR-OFF	Emergency Power Off	To
INXP	Index Pulse	From
ØTRD/	Open Trunk Driver (to Exchange)	
PWR-CONT-COM	Power Control Common	To
REM-DC-OFF	Power Off	To
REM-DC-ON	Power On	To
SARL/	Segment Address Read Level	From
SCLP	Storage Clock Pulse	From
SCØL/	Segment Coincidence Level	To
SR1L/ SR2L/ SR4L/ SR8L/ SRAL/ SRBL/	Storage Read Information Lines	From
SURL/	Storage Unit Ready Level	From
SWLL	Storage Write Lockout Level	From
SWRL/	Storage Write Level	To

		TO/FROM E.U.
SW1L SW2L SW4L SW8L SWAL SWBL	Storage Write Information Lines	To
T01L/ T02L/ T04L/ T08L/	Track Select Units Lines	To
T10L/ T20L/ T40L/	Track Select Tens Lines	To
WDMP	Word Mark Pulse	From
Z01L/ Z02L/	Zone Select Lines	To

INDEX - SECTION II

2 PRINCIPLES OF OPERATION

2.1 CONTROL FUNCTIONS AND LOGIC FLOW

The Display and Control Panel, shown in Figure 1.1-5, shows the indicators for the logic control flip-flops of the Sequence Counter and Clock Counter. The Sequence Counter is the primary logic control of the D.F.C.U. The Clock Counter is a secondary control used with the Sequence Counter.

The five Sequence Counter flip-flops (SnnF's) are: S10F and S20F for values of 00, 10, 20 and 30, and S01F, S02F and S04F for values of 0, 1, 2, 3, 4, 5, 6 and 7. The logic is expressed as SC = nn or sometimes as SEC = nn.

The four Clock Counter Flip-flops (CLnF's) are: CL1F, CL2F, CL4F and CL8F for values of 0→15. The logic is expressed as CLC = n or sometimes as CC = n.

The Sequence Counter, Clock Counter, A Register, B Register and other logical elements are shown in Figure 2.1-1. This is a block diagram of the D.F.C.U.

Each Sequence Count indicates a specific action. The following is a list of the sequence counts and the associated action:

At end of operation:

00 = Idle Condition (successful completion).

01 = Parity Error, Forbidden Combination, Alpha Character, excessive or insufficient address digits. (Latter three conditions called Invalid Address.)

02 = Disk Write Lockout.

03 = Storage Unit Not Ready.

04 = Parity correct in address characters.

05 = Parity Error or Invalid Address.

06 = Valid address, E.U. selection made (DACL).

07 = SURL/.

10 = Wait for Word Mark Pulse from disk.

11 = First WDMP from disk, System I.D. and command determine next Sequence Count (13 = B200 Read, B5000 - Read/Write; 12 = B200 Write only).

12 = B200 Write, Load first 3 characters.

13 = B200 Read or B5000 Read/Write. Wait for WDMP sync.

14 = Check for Segment Coincidence. B200 Write - load fourth character.

15 = Segment Coinicdence, SC0L to E.U.

20 = Active word, Read operation.

21 = Inactive word, Read operation.

24 = Active word, Read, with Parity Error in information from disk.

25 = Inactive word, Read, with Parity Error in information from disk.

30 = Active word, Write operation.

31 = Inactive word, Write operation.

34 = Active word, Write, with Parity Error in information from System.

35 = Inactive word, Write, with Parity Error in information from System.

23 = Read, change zone, disk face or disk, No Error.

22 = Read, wait for WDMP sync, No Error.

27 = Read, Information Parity Error, change zone, disk face or disk.

26 = Read, Information Parity Error. Wait for WDMP sync.

33 = Write, change zone, disk face or disk, No Error.

32 = Write, wait for WDMP sync, No Error.

37 = Write, Information Parity Error, change zone, disk face or disk.

36 = Write, Information Parity Error. Wait for WDMP sync.

Information on the disk is divided into words. A word consists of eight six-bit characters plus a six-bit, odd parity, word check character called the longitudinal parity character. Information transfer to and from the disk is handled in two phases - Active and Inactive. Alternate words are referred to as active and inactive words. The E.U. sends a Word Mark Pulse (W0MD in the D.F.C.U. and WDMP coming from E.U. to the D.F.C.U.) at the beginning of every word before Segment Coincidence is found. Control uses the Word Mark Pulse as a sync.

After coincidence has been found and an operation begun, Control receives a WDMP at the beginning of an active word only and characters

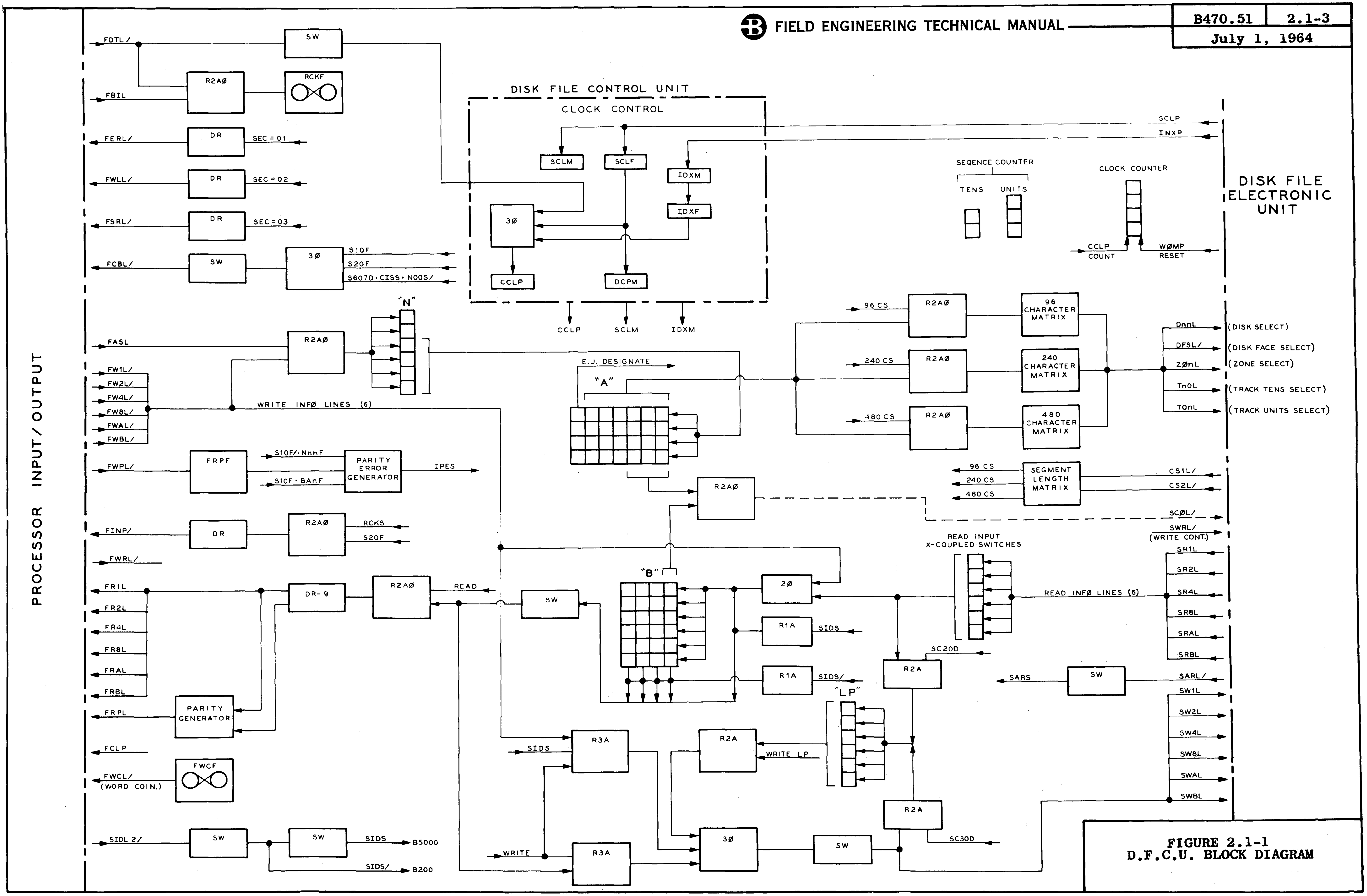


FIGURE 2.1-1
D.F.C.U. BLOCK DIAGRAM

are transferred to or from the E.U. The D.F.C.U. uses the Clock Counter to determine the end of the active word and the beginning of an inactive word. During an inactive word, the D.F.C.U. performs many functions, depending on the operation, while waiting for the next WDMP to signal the beginning of the next active word.

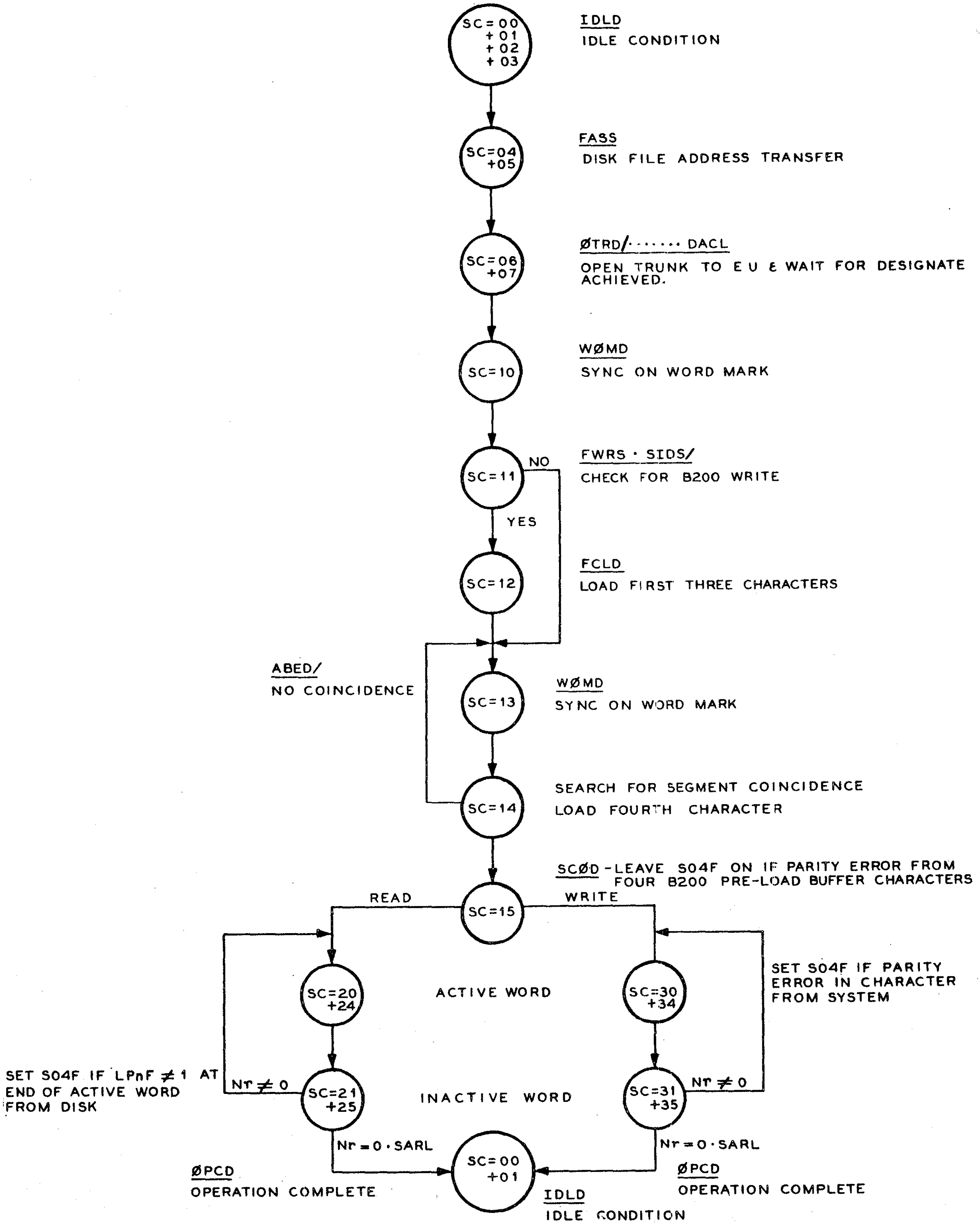


FIGURE 2.1-2
SEQUENCE COUNTS READ/WRITE OPERATION

2.2 SYSTEM OPERATION

B200

NOTE

CCP = FCLP

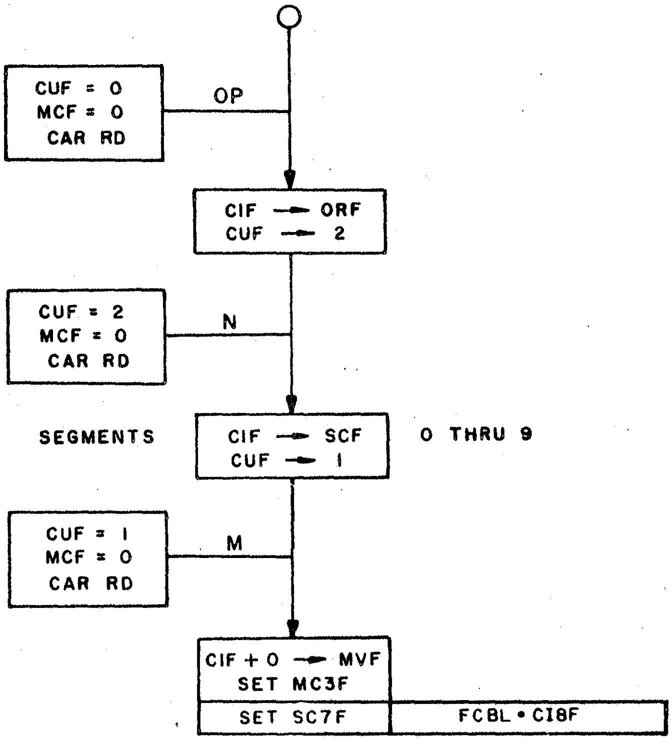


FIGURE 2.2-1
CUF = 0,2,1·MCF = 0

CUF = 0 MCF = 0	Set the op-code (K=34) into ORF's, set CUF's =2 and start a memory cycle.
CUF = 2 MCF = 0	Set the N Variant (number of segments) into SCF's, set CUF's = 1 and start a memory cycle.
CUF = 1 MCF = 0	Set the M Variant (operation) into MVF's and set MC3F. Set SC7F if Control is busy and CI8F (Interrogate).

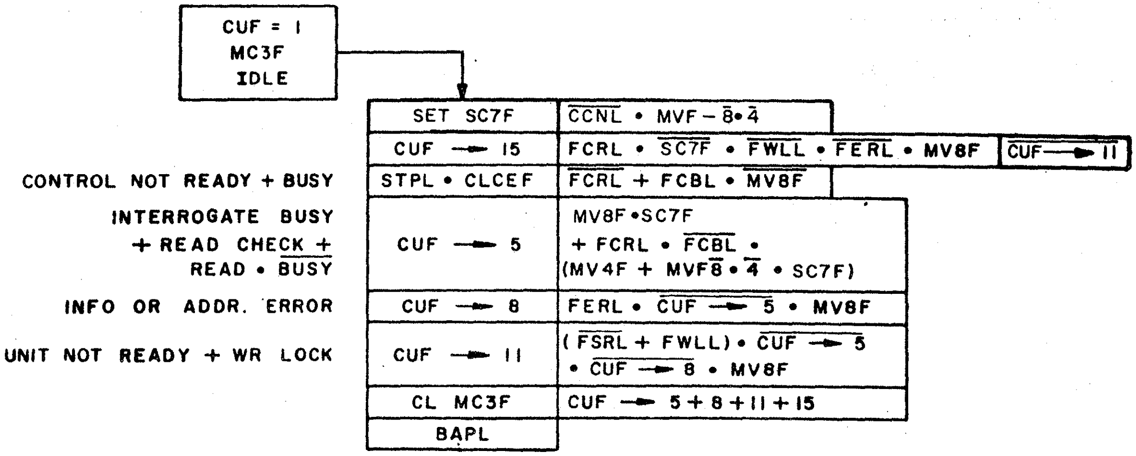


FIGURE 2.2-2
CUF = 1•MC3F

CUF = 1
MC3F

Depending on the M Variant, the following actions occur:

MV8F - Interrogate

If D.F.C.U. is Ready, Not Busy and the previous operation did not encounter a lockout or error condition and the logic to set CUF→11 is not present, then set CUF→15.

If D.F.C.U. is Busy, set CUF→5.

If an Error condition occurred in the previous operation and the logic to set CUF→5 is not present, then set CUF→8.

If a previous operation found FSRL/ (Storage Unit Not Ready) or lockout condition, D.F.C.U. is not Busy and no Error condition, then set CUF→11.

If D.F.C.U. is Not Ready, bring up STPL (Stop Level) and reset CEF.

MVF = 0 + 2 + 4 - Write or Read or Read Check

If D.F.C.U. is Not Ready or Busy, bring up STPL to reset CEF.

If D.F.C.U. is Ready and Not Busy, set CUF→5.

In the case of a READ or WRITE, wait for CCNL/ (card or paper-tape to stop).

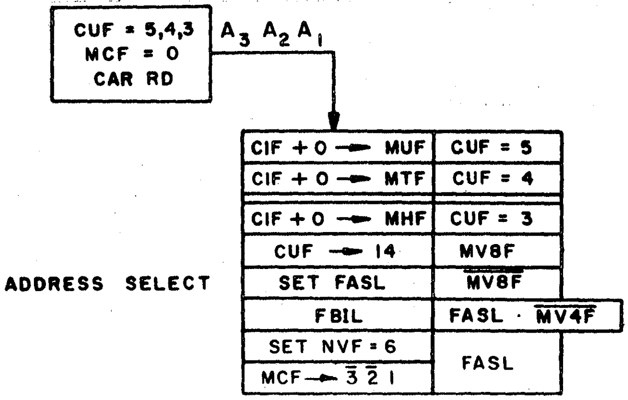


FIGURE 2.2-3
CUF = 5,4,3·MCF=0

CUF = 5,4,3
MCF = 0

Set AAA into MAR.

If this is an Interrogate, AAA is the D.F.C.U. Busy branch. Set CUF's→14.

For Read, Write or Read Check, AAA is the address of the Disk File Address word. Set DI1F to produce FASL. If Read or Write, produce FBIL. Note that for Read Check, FBIL is false for the first clock to D.F.C.U. Set NVF→6 to count the seven Disk File Address digits and MCF = $\overline{3} \cdot \overline{2} \cdot 1$ for a MAR read.

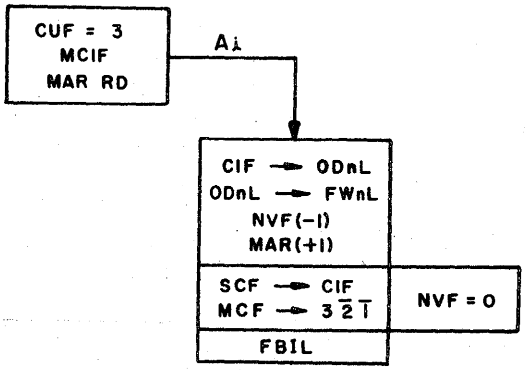


FIGURE 2.2-4
CUF = 3·MC1F

CUF = 3
MCF = 1

Transfer Disk File Address digits to the D.F.C.U. When the seventh digit has been sent, the number of segments digit is shifted from SCF's to the CIF's. Set MCF→3 · $\overline{2}$ · $\overline{1}$ to idle.

The FBIL term is also produced by:
  FBIL = FASL · CAU = 3 · MCF - 2 · 1
This ensures that the Address digits are not encoded.

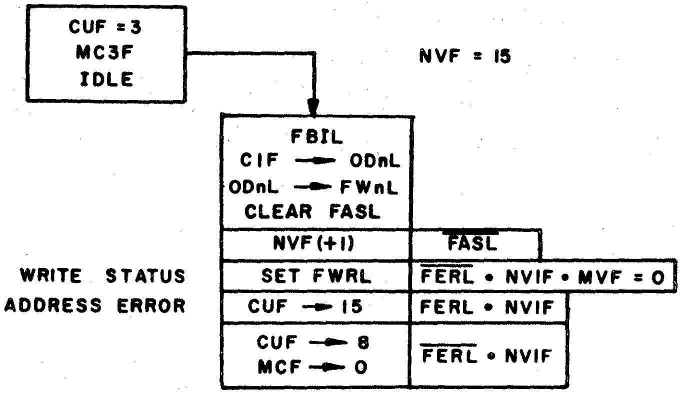


FIGURE 2.2-5
CUF = 3•MC3F

CUF = 3
MC3F

Transfer the Number of Segments digit to the D.F.C.U., set DI2F (FWRL) if a Write operation and reset DI1F (FASL). If D.F.C.U. sensed an error during the Address transfer (FERL), set CUF = 15.

If address transfer was correct, set CUF→8.

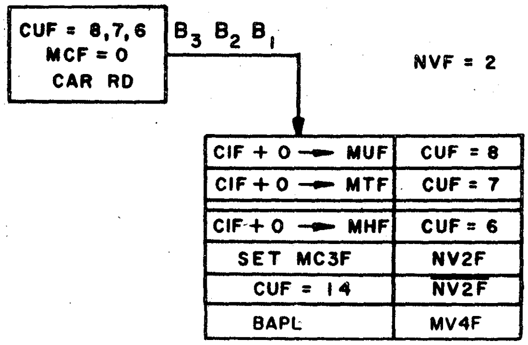


FIGURE 2.2-6
CUF = 8,7,6•MCF=0

CUF = 8,7,6
MCF = 0

Read BBB into MAR.

NVF's = 0 coming from CUF = 1 • MC3F due to an Interrogate and an Error condition, set CUF →14.

NVF's = 2 for a Read or Write operation. Set MC3F to idle.

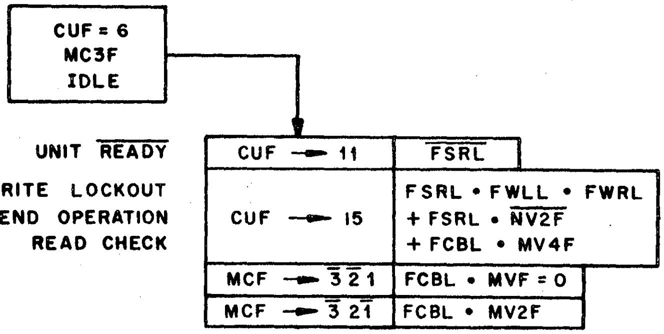


FIGURE 2.2-7
CUF = 6·MC3F

CUF = 6
MC3F

The following can occur:

1. The Storage Unit addressed is Not Ready (FSRL/); set CUF→11.
2. Write operation but disk is locked out (FWLL); set CUF→15.
3. End of operation (FSRL · NV2F/); set CUF→15.
4. Read Check operation and D.F.C.U. has become Busy (FCBL); set CUF→15.
5. Write operation; set MCF→$\overline{3} \cdot \overline{2} \cdot 1$.
6. Read operation; set MCF→$\overline{3} \cdot 2 \cdot \overline{1}$.

NOTE

Processor CCP's produce FDTL's to the D.F.C.U. While FASL is true, FDTL's produce CCLP's in the D.F.C.U. Subsequently, the D.F.C.U. is clocked by converted pulses from the E.U.

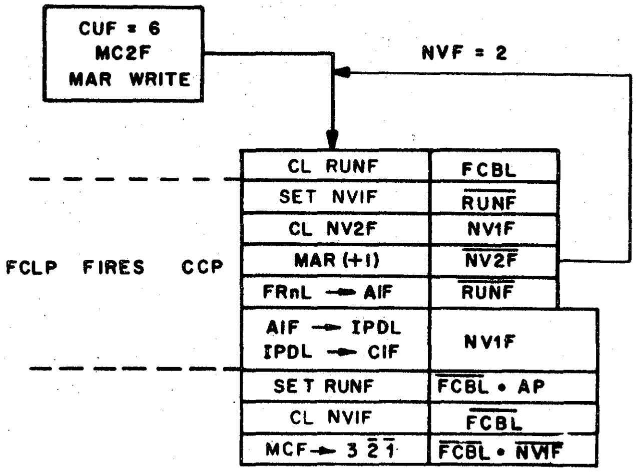


FIGURE 2.2-8
CUF = 6•MC2F

CUF = 6
MC2F

Disk File Read operation. MC2F is a MAR Write condition so information coming into the Processor will be stored.

RUNF is cleared and CCP's are produced by FCLP's from the D.F.C.U.

CCP = FCLP • OR = 34 • RUNF/

The first FCLP from Control sets NV1F and clocks the character on the Read lines (FRnL) into the AIF's. The next FCLP transfers the character (BCL in the AIF's) through the decoding matrix into the CIF's and starts a memory cycle to store it. It sets the second character into AIF's and clears NV2F to permit MAR to be counted by subsequent FCLP's. FCLP's produce CCP's until the D.F.C.U. becomes Not Busy. See Figure 2.2-9.

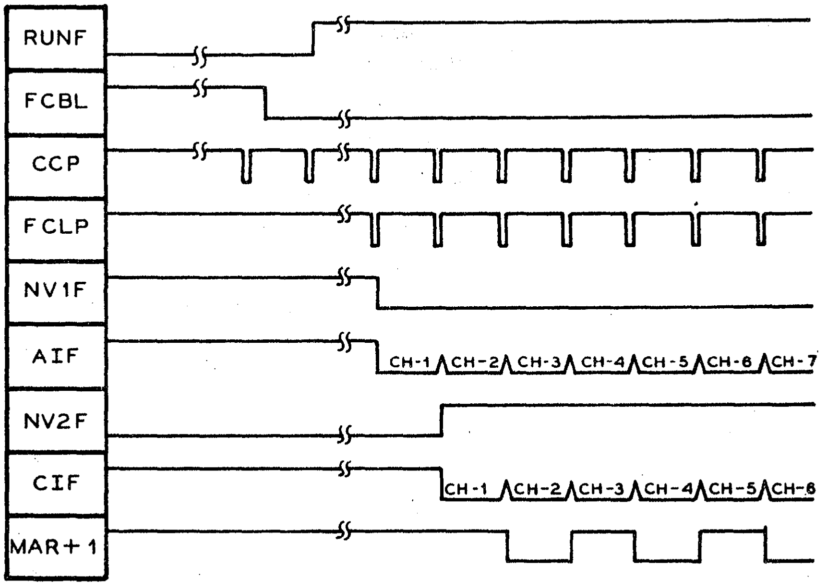


FIGURE 2.2-9
INPUT CHARACTER TIMING

When the specified segments have been read, D.F.C.U. becomes Not Busy. The first clock pulse from the Master Oscillator (AP) after FCBL/ sets RUNF to allow the Processor to resume operation on its own. The first clock pulse after RUNF clears NV1F and the following clock pulse sets MCF→3 • $\overline{2}$ • 1. See Figure 2.2-10. Refer to CUF = 6 • MC3F item 3.

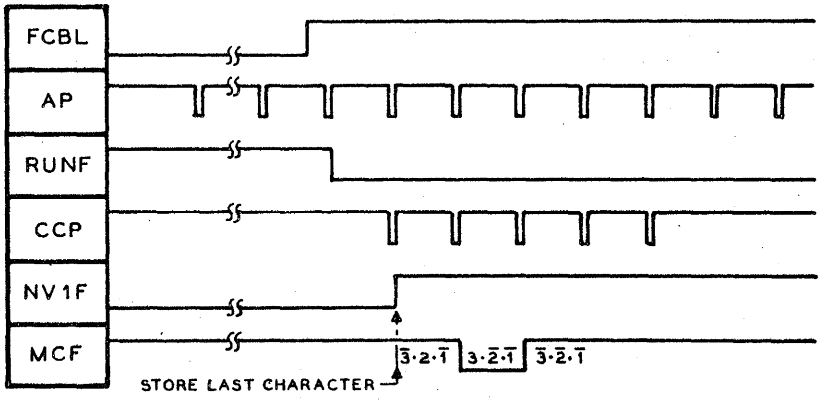


FIGURE 2.2-10
RESUME PROCESSOR CLOCK AFTER READ

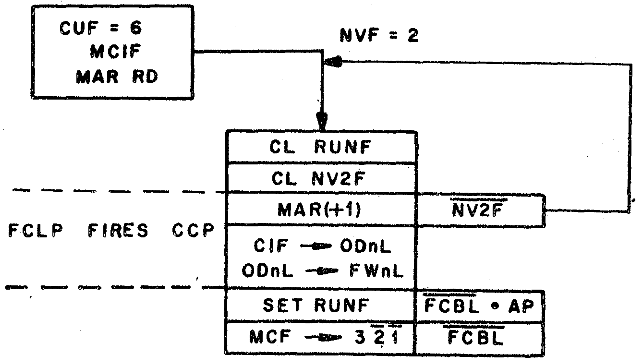


FIGURE 2.2-11
CUF = 6•MC1F

CUF = 6
MC1F

Disk File Write operation. MC1F is a MAR Read condition so information is read from memory into the CIF's and the File Write Lines are driven by the levels from the Output Encoder.

The clock pulse that occurs at CUF = 6 • MC1F clears RUNF, clears NV2F and rereads the first character into CIF's (redundant memory cycle). MAR was not counted up as NV2F was on. The following CCP's, which are produced by FCLP's from the D.F.C.U., count MAR +1 to access the next character.

When the specified segments have been written, the D.F.C.U. becomes Not Busy and the first AP after this sets RUNF to turn the Processor clock back on. The first clock pulse after RUNF sets MCF→3 • $\overline{2}$ • $\overline{1}$. See Figure 2.2-12. Refer to CUF = 3 • MC3F item 3.

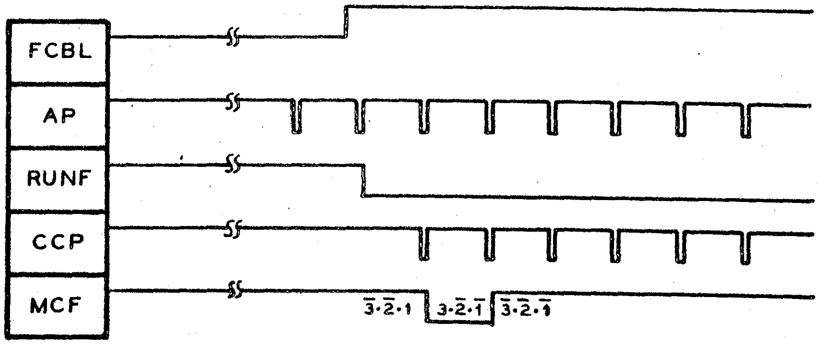


FIGURE 2.2-12
RESUME PROCESSOR CLOCK AFTER WRITE

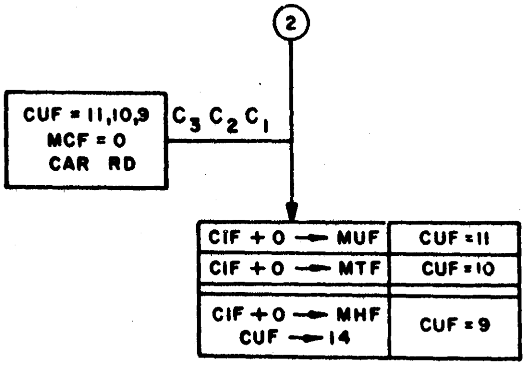


FIGURE 2.2-13
CUF = 11,10,9·MCF=0

CUF = 11,10,9 MCF = 0	Addressed Storage Unit was Not Ready. Read CCC into MAR Register, set CUF→14 and take CCC branch.

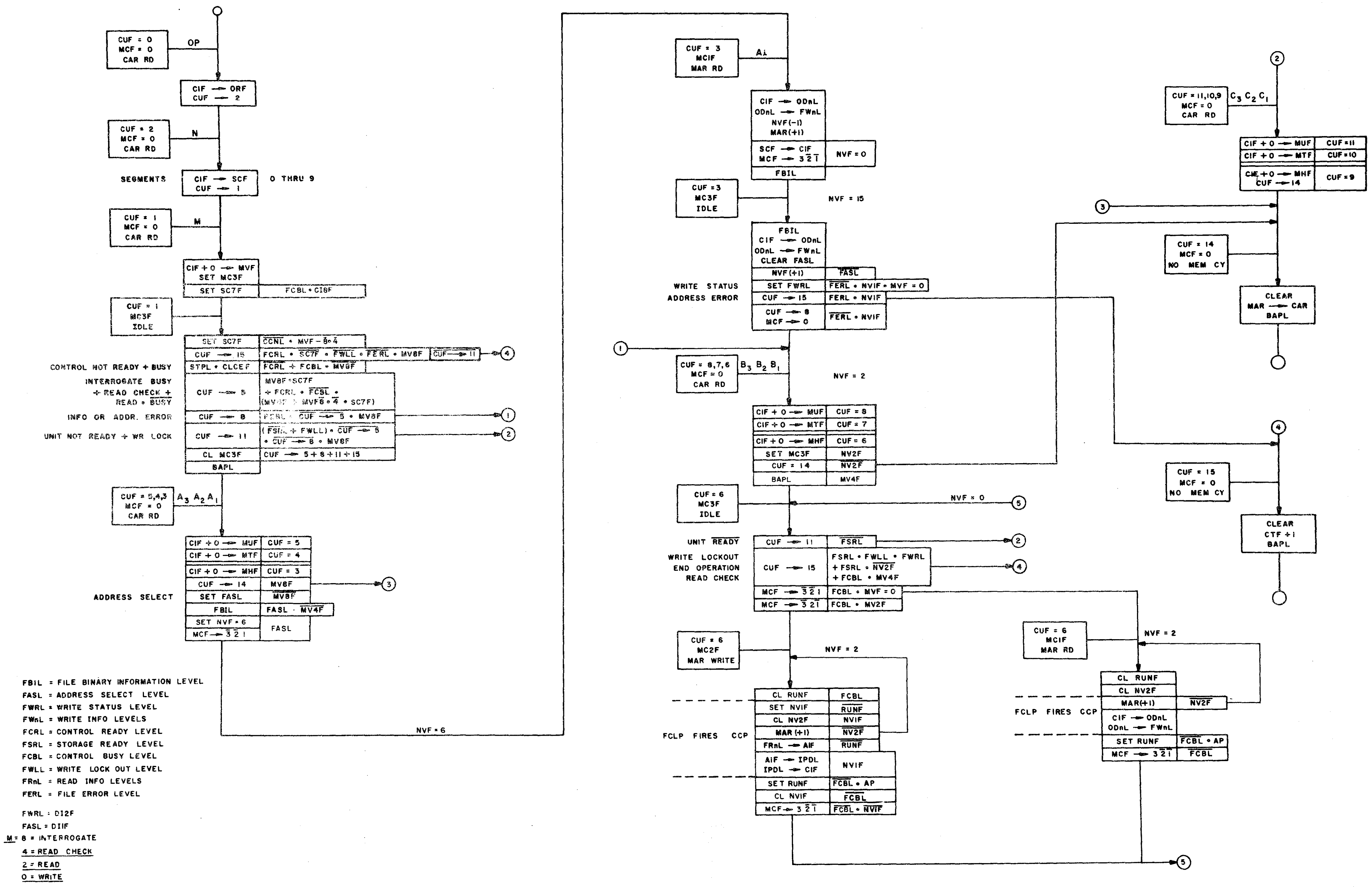


FIGURE 2.2-14
B200 LOGIC FLOW

Model II I/O Control Standard Logic is identical to Model I I/O with one exception; if LPPF is on at SC = 14, then bit 23 is set in the Result Descriptor.

SC=3

	CC + 1	$\overline{CC4F}$
NO CONFLICT UNIT READY	D16F ← 1	AUNS • [CC = 1]
	D18F ← 1	[CC = 3] • (I21D • $\overline{D41F}$ + I31D • D41F)
	CC1F ← 1	[CC = 4]
	CC2F ← 1	[CC = 4] • D16F • D18F • UBZS
	BTDM ← 1	[CC = 7] • (PA0D + TA0D)
	CC1F ← 0	[CC = 7]
	D16F ← 0	[CC = 6] • $\overline{BTDS}$ • (PA0D + TA0D)
	CC2F ← 0	[CC = 6] • ($\overline{D16F}$ + $\overline{UBZS}$)

FIGURE 2.2-15
SC = 3 STANDARD LOGIC

In a Disk File operation, the I/O proceeds through Standard Logic until SC = 3. At SC = 3, the I/O checks for D.F.C.U. Ready. If the D.F.C.U. is Ready but is Busy, the I/O idles until the D.F.C.U. is Not Busy (FCBL/ from the D.F.C.U. and UBZS/ in the I/O).

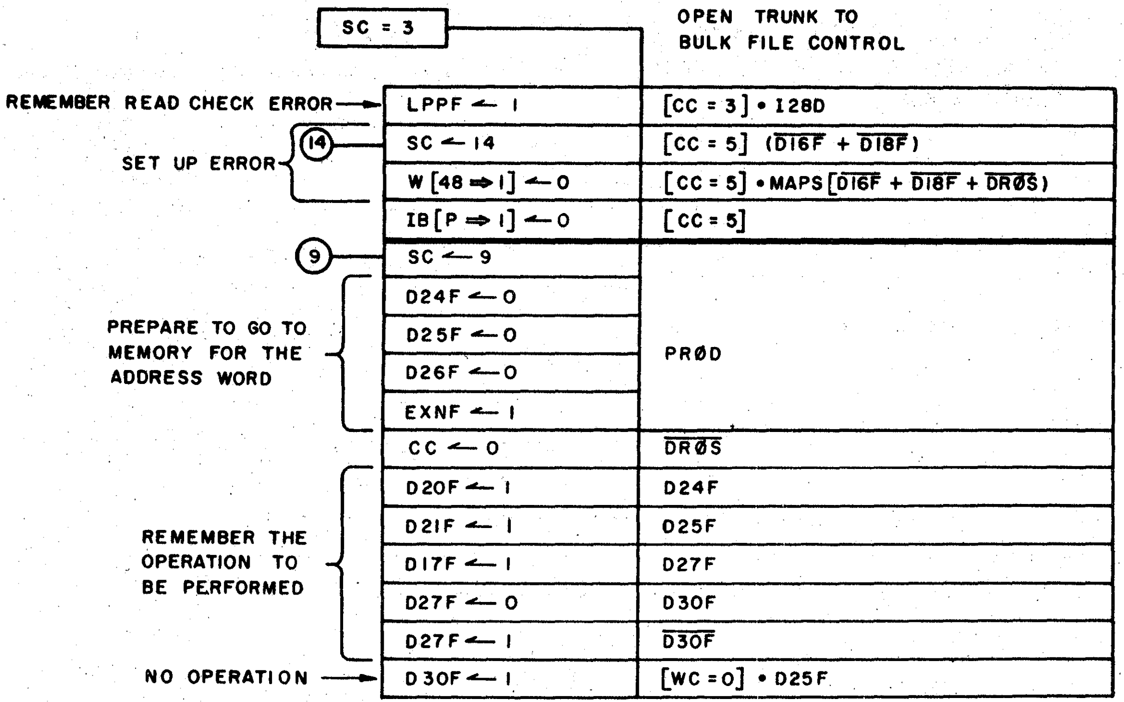
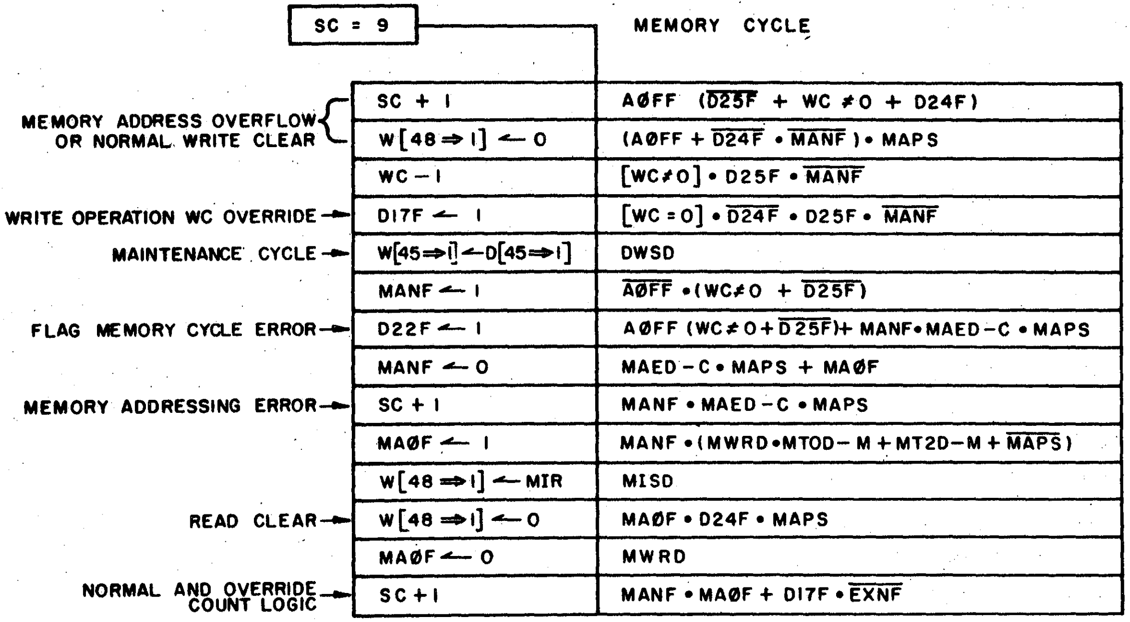


FIGURE 2.2-16
SC = 3 DISK FILE LOGIC

SC = 3 If the D.F.C.U. is Not Ready or is Busy with another I/O, set SC = 14 to produce and store Result Descriptor. If the D.F.C.U. is Ready and Not Busy, set SC = 9 to access core memory for the Disk File Address. The number of segments was placed in the LPnF's at SC = 2.



SC = 9

MEMORY CYCLE

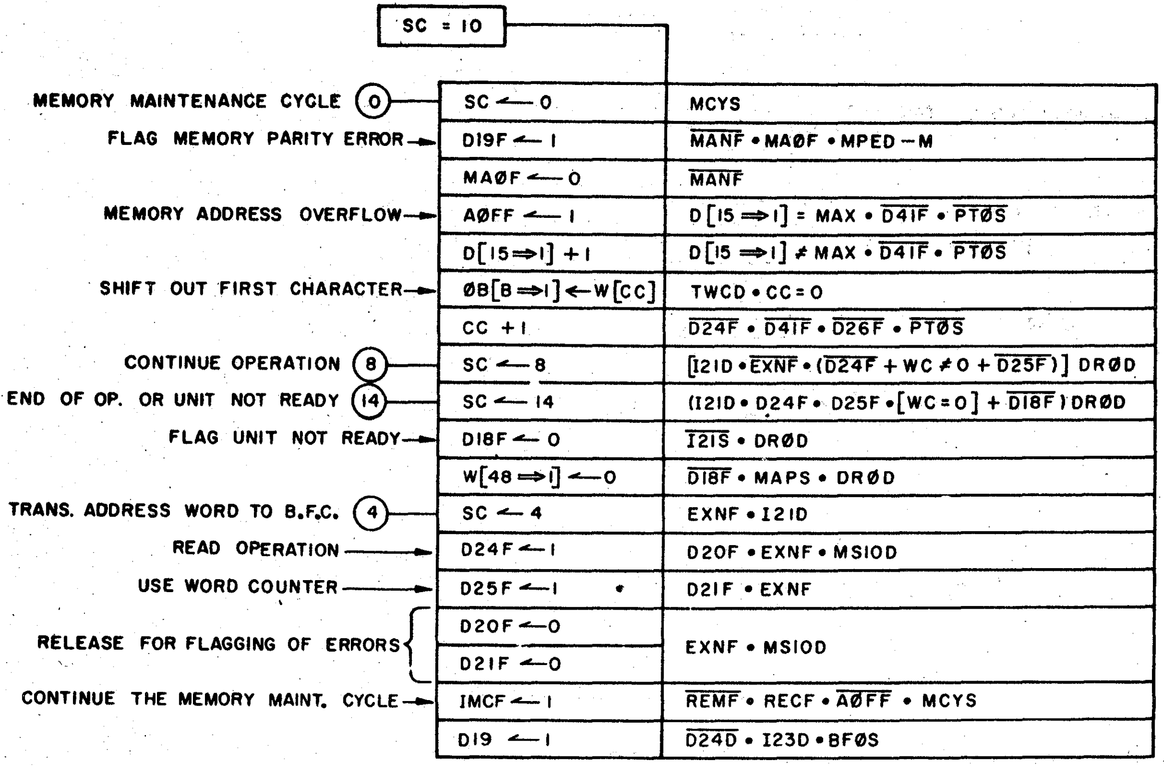
MEMORY ADDRESS OVERFLOW OR NORMAL WRITE CLEAR	SC + 1	A0FF ($\overline{D25F}$ + WC ≠ 0 + D24F)
	W[48 ⇒ 1] ← 0	(A0FF + $\overline{D24F}$ • $\overline{MANF}$) • MAPS
	WC − 1	[WC ≠ 0] • D25F • $\overline{MANF}$
WRITE OPERATION WC OVERRIDE	D17F ← 1	[WC = 0] • $\overline{D24F}$ • D25F • $\overline{MANF}$
MAINTENANCE CYCLE	W[45 ⇒ 1] ← D[45 ⇒ 1]	DWSD
	MANF ← 1	$\overline{A0FF}$ • (WC ≠ 0 + $\overline{D25F}$)
FLAG MEMORY CYCLE ERROR	D22F ← 1	A0FF (WC ≠ 0 + $\overline{D25F}$) + MANF • MAED-C • MAPS
	MANF ← 0	MAED-C • MAPS + MA0F
MEMORY ADDRESSING ERROR	SC + 1	MANF • MAED-C • MAPS
	MA0F ← 1	MANF • (MWRD • MTOD-M + MT2D-M + $\overline{MAPS}$)
	W[48 ⇒ 1] ← MIR	MISD
READ CLEAR	W[48 ⇒ 1] ← 0	MA0F • D24F • MAPS
	MA0F ← 0	MWRD
NORMAL AND OVERRIDE COUNT LOGIC	SC + 1	MANF • MA0F + D17F • $\overline{EXNF}$

FIGURE 2.2-17
SC = 9 ACCESS CORE MEMORY

SC = 9 With SC = 9 for the first time, D25F would be off because it was reset at SC = 3. D25F being off inhibits WC - 1 so the Disk File Address word will not be included in the Word Count.

If WC = 0 • D24F/ • D25F, set D17F to indicate that the Word Count has been satisfied, the I/O will remain tied to the D.F.C.U. until the end of the Write operation.

When memory access is complete or no access is required due to Word Count Override, count SC + 1 to SC = 10.



SC = 10

MEMORY MAINTENANCE CYCLE ⓪	$SC \leftarrow 0$	$MCYS$
FLAG MEMORY PARITY ERROR	$D19F \leftarrow 1$	$\overline{MANF} \bullet MA0F \bullet MPED-M$
	$MA0F \leftarrow 0$	$\overline{MANF}$
MEMORY ADDRESS OVERFLOW	$A0FF \leftarrow 1$	$D[15 \Rightarrow 1] = MAX \bullet \overline{D41F} \bullet \overline{PT0S}$
	$D[15 \Rightarrow 1] + 1$	$D[15 \Rightarrow 1] \neq MAX \bullet \overline{D41F} \bullet \overline{PT0S}$
SHIFT OUT FIRST CHARACTER	$0B[B \Rightarrow 1] \leftarrow W[CC]$	$TWCD \bullet CC = 0$
	$CC + 1$	$\overline{D24F} \bullet \overline{D41F} \bullet \overline{D26F} \bullet \overline{PT0S}$
CONTINUE OPERATION ⑧	$SC \leftarrow 8$	$[I21D \bullet \overline{EXNF} \bullet (\overline{D24F} + WC \neq 0 + \overline{D25F})]\ DR0D$
END OF OP. OR UNIT NOT READY ⑭	$SC \leftarrow 14$	$(I21D \bullet D24F \bullet D25F \bullet [WC = 0] + \overline{D18F})\ DR0D$
FLAG UNIT NOT READY	$D18F \leftarrow 0$	$\overline{I21S} \bullet DR0D$
	$W[48 \Rightarrow 1] \leftarrow 0$	$\overline{D18F} \bullet MAPS \bullet DR0D$
TRANS. ADDRESS WORD TO B.F.C. ④	$SC \leftarrow 4$	$EXNF \bullet I21D$
READ OPERATION	$D24F \leftarrow 1$	$D20F \bullet EXNF \bullet MSIOD$
USE WORD COUNTER	$D25F \leftarrow 1$	$D21F \bullet EXNF$
RELEASE FOR FLAGGING OF ERRORS	$D20F \leftarrow 0$	$EXNF \bullet MSIOD$
	$D21F \leftarrow 0$	
CONTINUE THE MEMORY MAINT. CYCLE	$IMCF \leftarrow 1$	$\overline{REMF} \bullet RECF \bullet \overline{A0FF} \bullet MCYS$
	$D19 \leftarrow 1$	$\overline{D24D} \bullet I23D \bullet BF0S$

FIGURE 2.2-18
SC = 10 MEMORY ADDRESS LOGIC

SC = 10 At this sequence count:

1. Set D19F if a memory parity error occurred at SC = 9.
2. Increase the memory address in D $[15 \Rightarrow 1]$ to point at the next word of information.
3. For a WRITE operation, shift the first character of the new word into the Output Buffer (0B) and count CC + 1.
4. First time at SC = 10, EXNF is on (set at SC = 3) so set SC = 4 to transfer the Disk File Address word to the D.F.C.U.
5. Set SC = 8 if the operation is not complete.
6. Set SC = 14 to produce and store Result Descriptor if: D.F.C.U. went Not Ready during the current operation or the end of a Read operation due to Word Count Override.

SC = 4

TRANSFER ADDRESS WORD AND NUMBER OF SEGMENTS TO B.F.C.

NORMAL AND ERROR CLEAR →	W[48 ⇒ 1] ← 0	LCHF + DERS
ERROR, NO OP, OR READ CHECK EXIT ⑭	SC ← 14	DERS + (D30F • D17F • LCHF)
TRANSFER ADDRESS WORD AND NUMBER OF SEGMENTS TO B.F.C	STRF ← 1	$\overline{HØLF}$
	HØLF ← 1	STRF • $\overline{D41F}$
	STRF ← 0	STRF • HØLF
	HØLF ← 0	
	EXNF ← 0	
	D27F ← 1	EXNF • STRF • HØLF
	ØB[B ⇒ 1] ← W[CC]	TWUD • (CC = n)
	CC + 1	$\overline{EXNF}$ • STRF • HØLF • CC ≠ 0
	ØB[B ⇒ 1] ← 0	STRF • HØLF • CC = 7
	ØB[B ⇒ 1] ← LP[B ⇒ 1]	[CC = 0] • $\overline{STRF}$ • (WC ≠ 0 + $\overline{D25F}$)
THE ADDRESS WORD AND NUMBER OF SEGMENTS HAS BEEN SENT TO B.F.C	LP[B ⇒ 1] ← 0	[CC = 0] • STRF • HØLF
	LCHF ← 1	
	D17F ← 0	
	D27F ← 0	$\overline{D17F}$ • $\overline{LCHF}$
	D17F ← 0	J14S[SC2F + SC4F + SC8F]
		LCHF
CONTINUE OPERATION →	D17F ← 1	I22D
TRANSFER "PARITY ERROR" →	D19F ← 1	I28D
STORAGE UNIT NOT READY →	D21F ← 1	$\overline{I26S}$
STORAGE UNIT LOCKED OUT →	D20F ← 1	I25D • $\overline{D24F}$
	LCHF ← 0	LCHF • D17F • STRF • HØLF
READ EXIT ⑧	SC ← 8	D24F
WRITE EXIT ⑨	SC ← 9	$\overline{D24F}$

FIGURE 2.2-19
SC = 4 TRANSFER DISK FILE ADDRESS

SC = 4 Transfer the Disk File Address and the number of segments to the D.F.C.U.

The I/O sends clock pulses to the D.F.C.U. called FDTL's (File Data Transfer Control) and the timing is shown in Figure 2.2-20.

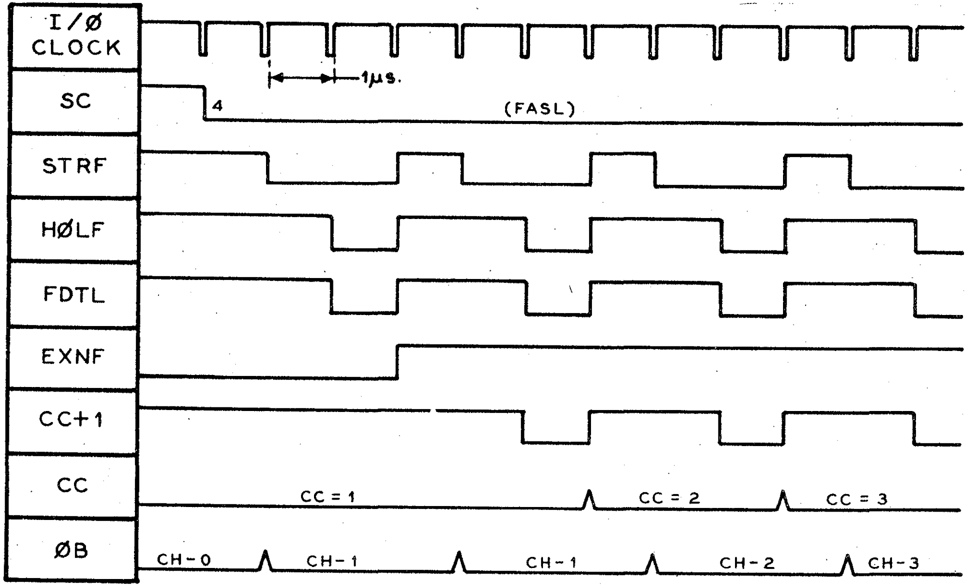


FIGURE 2.2-20
TIMING OF FDTL

The first FDTL shown in Figure 2.2-20 will cause the D.F.C.U. to change from an idle state to an active state to receive the Disk File Address.

The timing diagram in Figure 2.2-20 also shows that the first character in the W Register (CH #0) is not used in any way and is not transferred to the D.F.C.U.

When all seven digits of the Disk File Address have been transferred to the D.F.C.U., the number of segments, which was temporarily stored in the LPnF's of the I/O, is set into the ØBnF's and transferred to the D.F.C.U. The D.F.C.U. uses the FDTL's to generate internal clock pulses until the D.F.C.U. becomes Busy; after that, pulses from the E.U. will generate the internal clock pulses.

When the D.F.C.U. becomes Busy, I22D becomes true, the I/O sets D17F and the next STRF • HØLF sets SC = 8 for a READ operation or SC = 9 to access the first information word for a WRITE operation (after SC = 9, then set SC = 10 and return to SC = 8).

See Figure 2.2-21 for timing of Disk File Address and segment number transfer and the action of the I/O when the D.F.C.U. becomes Busy.

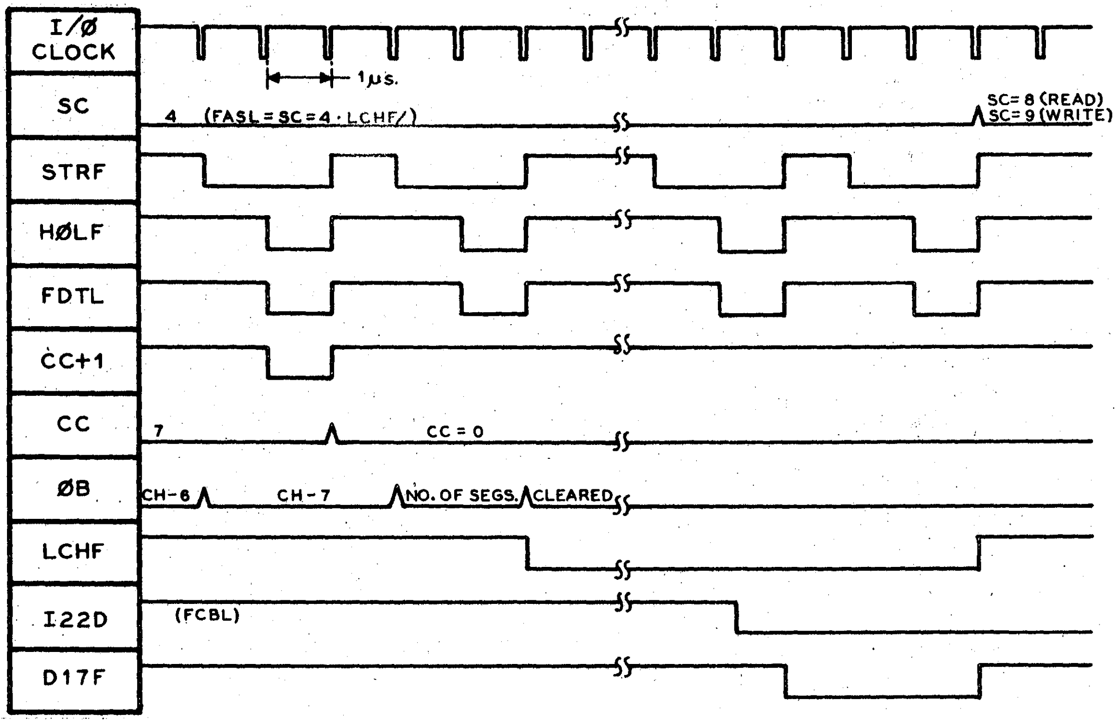
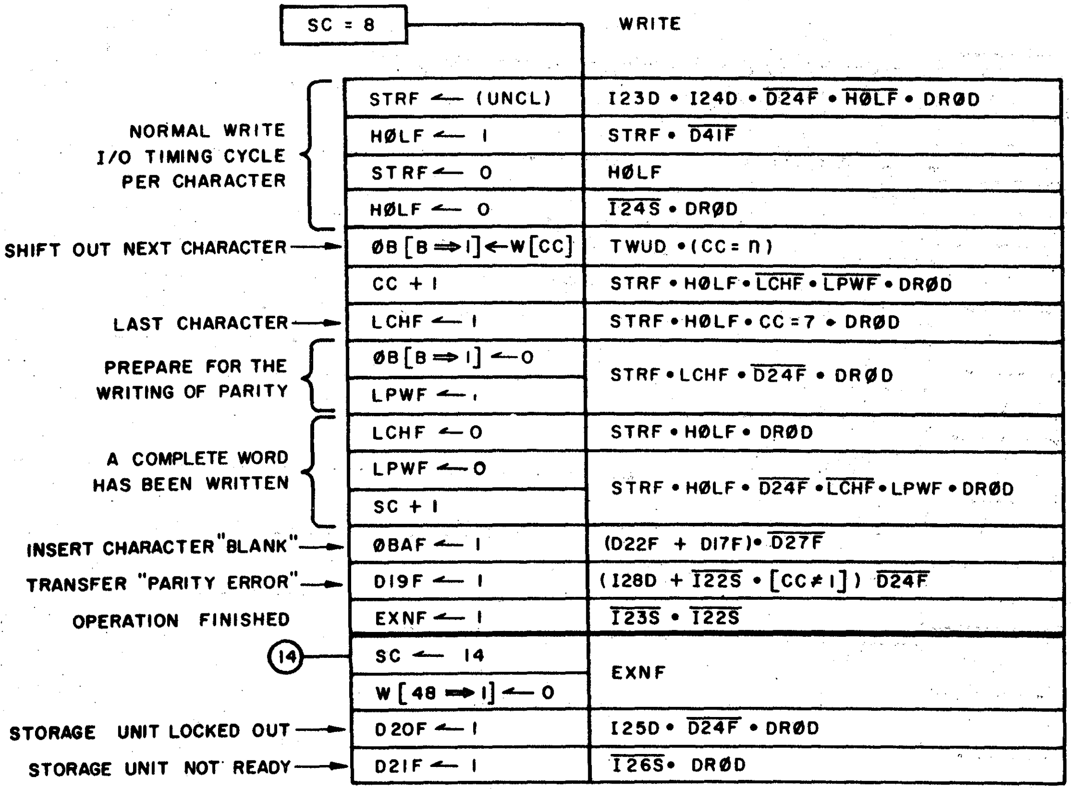


FIGURE 2.2-21
END OF DISK FILE ADDRESS TRANSFER



SC = 8

WRITE

NORMAL WRITE I/O TIMING CYCLE PER CHARACTER	STRF ← (UNCL)	I23D • I24D • $\overline{D24F}$ • $\overline{HØLF}$ • DRØD
	HØLF ← 1	STRF • $\overline{D41F}$
	STRF ← 0	HØLF
	HØLF ← 0	$\overline{I24S}$ • DRØD
SHIFT OUT NEXT CHARACTER →	ØB [B ⇒ 1] ← W [CC]	TWUD • (CC = n)
	CC + 1	STRF • HØLF • $\overline{LCHF}$ • $\overline{LPWF}$ • DRØD
LAST CHARACTER →	LCHF ← 1	STRF • HØLF • CC = 7 • DRØD
PREPARE FOR THE WRITING OF PARITY	ØB [B ⇒ 1] ← 0 LPWF ← 1	STRF • LCHF • $\overline{D24F}$ • DRØD
A COMPLETE WORD HAS BEEN WRITTEN	LCHF ← 0	STRF • HØLF • DRØD
	LPWF ← 0 SC + 1	STRF • HØLF • $\overline{D24F}$ • $\overline{LCHF}$ • LPWF • DRØD
INSERT CHARACTER "BLANK" →	ØBAF ← 1	(D22F + D17F) • $\overline{D27F}$
TRANSFER "PARITY ERROR" →	D19F ← 1	(I28D + $\overline{I22S}$ • [CC ≠ 1]) $\overline{D24F}$
OPERATION FINISHED	EXNF ← 1	$\overline{I23S}$ • $\overline{I22S}$
⑭	SC ← 14 W [48 ⇒ 1] ← 0	EXNF
STORAGE UNIT LOCKED OUT →	D20F ← 1	I25D • $\overline{D24F}$ • DRØD
STORAGE UNIT NOT READY →	D21F ← 1	$\overline{I26S}$ • DRØD

FIGURE 2.2-22
SC = 8 WRITE OPERATION

SC = 8
D24F

Transfer characters serially from the I/O to the D.F.C.U. The D.F.C.U. sends a File Clock Pulse (I24D in I/O, FCLP in the D.F.C.U.; 1.6µsec in duration) to the I/O when it is ready to receive a character.

Coming after SC = 10, CC would equal 1 and ØB would contain Character #0 upon entering SC = 8. See Figure 2.2-17.

Figure 2.2-23 shows the timing of the character transfer from the I/O to the D.F.C.U. The time between FCLP's will vary from about 3µsec up to about 6µsec depending on the Disk File Address being accessed.

The I/O remains at SC = 8 until the Longitudinal Parity Character for the word is written. The D.F.C.U. generates this character. Figure 2.2-24 shows the timing until the I/O goes to SC = 9 for the next word of information. After the next word is in W Register, the I/O returns to SC = 8.

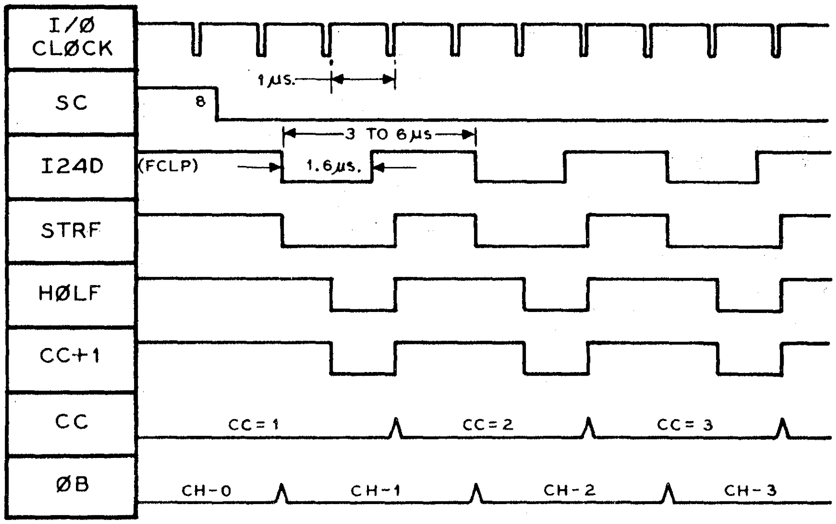


FIGURE 2.2-23
CHARACTER TRANSFER DURING WRITE

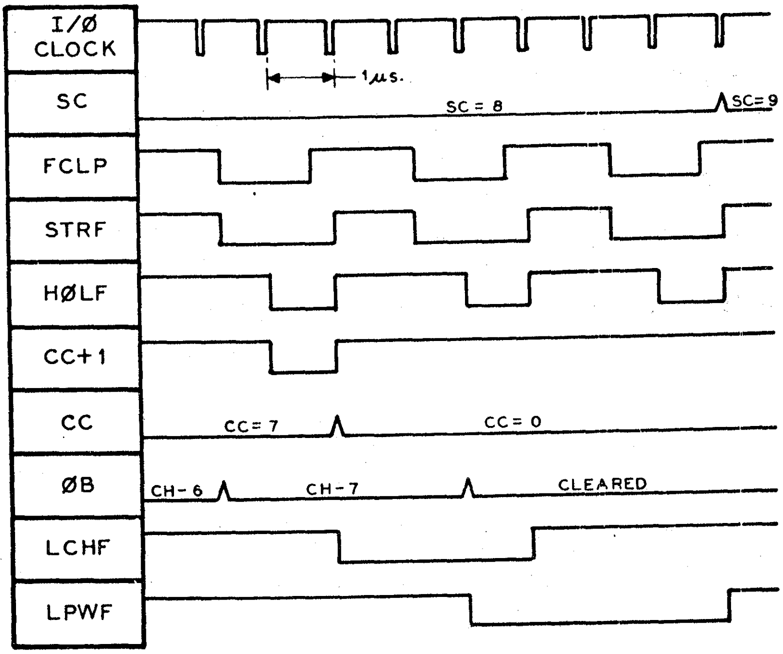


FIGURE 2.2-24
END OF WORD TRANSFER DURING WRITE

	SC = 8	READ
NORMAL READ I/O TIMING CYCLE PER CHARACTER	STRF ← 1	I23D • I24D • D24F • $\overline{\text{H0LF}}$ • DR0D
	H0LF ← 1	STRF • $\overline{\text{D41F}}$
	STRF ← 0	H0LF
	H0LF ← 0	DR0D • $\overline{\text{I24S}}$
READ IN NEXT CHARACTER →	IB∩F ← 1 (UNCL)	I23D • D24F • (FRP − ∩) • $\overline{\text{H0LF}}$ • DR0D
GENERATE PARITY →	LP∩F ← ΔLP∩F	STRF • $\overline{\text{H0LF}}$ • IB∩F • DR0D
TRANS. CHAR. TO "W" REG. →	W[CC] ← IB[8 ⇒ 1]	STRF • H0LF • $\overline{\text{LPWF}}$ • $\overline{\text{LCHF}}$ • MAPS • (CC = ∩) • D24D • DR0D
	IB[8 ⇒ 1] ← 0	STRF • H0LF • $\overline{\text{D41F}}$ • $\overline{\text{GPMS}}$
	CC + 1	STRF • H0LF • $\overline{\text{LCHF}}$ • $\overline{\text{LPWF}}$ • DR0D
LAST CHARACTER →	LCHF ← 1	STRF • H0LF • CC = 7 • DR0D
A COMPLETE WORD HAS BEEN READ	LCHF ← 0	STRF • H0LF • LCHF • DR0D
	LP[8 ⇒ 1] ← 0	
	SC + 1	STRF • H0LF • LCHF • D24F • DR0D
CHECK LONG. PARITY →	D20F ← 1	STRF • H0LF • LCHF • LPES • D24F
TRANSFER PARITY ERROR →	D20F ← 1	STRF • H0LF • PELS • D24F + $\overline{\text{I22S}}$ • [CC ≠ 0] • D24F
OPERATION FINISHED →	EXNF ← 1	$\overline{\text{I23S}}$ • $\overline{\text{I22S}}$
⑭	SC = 14	EXNF
	W[48 ⇒ 1] ← 0	
STORAGE UNIT NOT READY →	D21F ← 1	$\overline{\text{I26S}}$ • DR0D

FIGURE 2.2-25
SC = 8 READ OPERATION

SC = 8
D24F

The characters being transferred serially from the D.F.C.U. are set into the W Register. When a full word has been collected, SC + 1 to SC = 9 to store the word and return to SC = 8 if the Word Count has not been satisfied.

The D.F.C.U. send a File Clock Pulse (FCLP) to the I/O when a character is ready to be transferred to the I/O. See Figure 2.2-25 for timing.

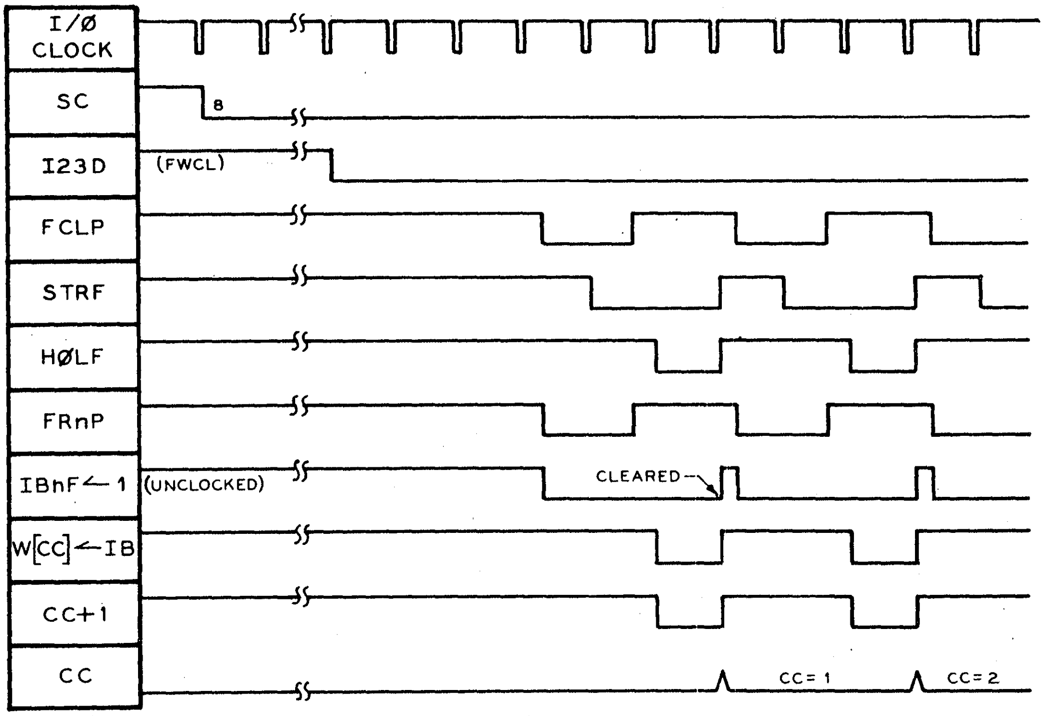


FIGURE 2.2-26
INPUT CHARACTER TIMING TO I/O DURING READ

The level FWCL (File Word Coincidence) is sent to the I/O to indicate when an Active word begins and remains true during the Active word. The File Read Levels (FRnL's) are present for the duration of the File Clock Pulse (FCLP). The IBnF's are set single-endedly; if the FRnL's return to a false level, the IBnF's remain in their set state until the Character is transferred to the W Register.

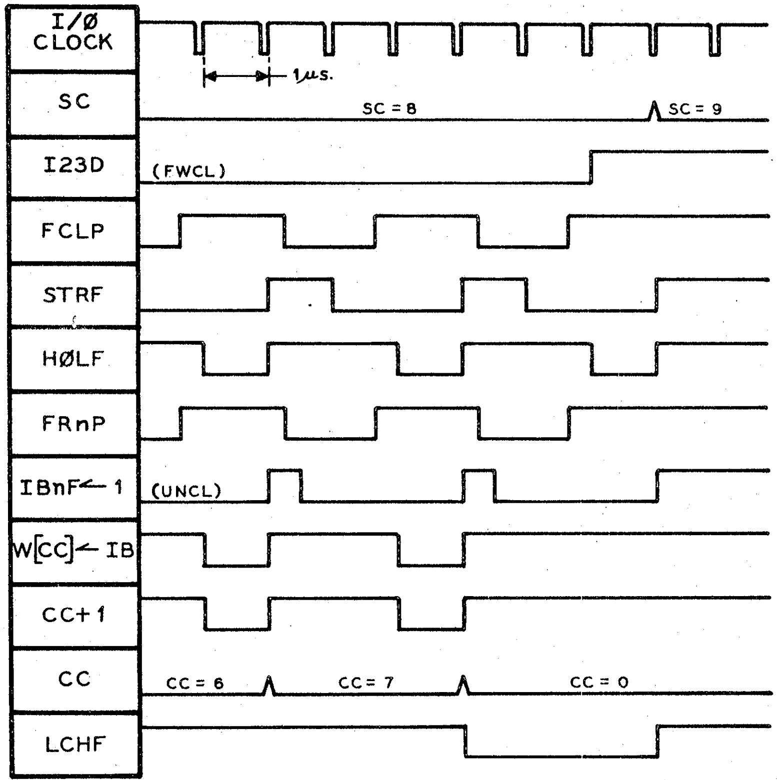
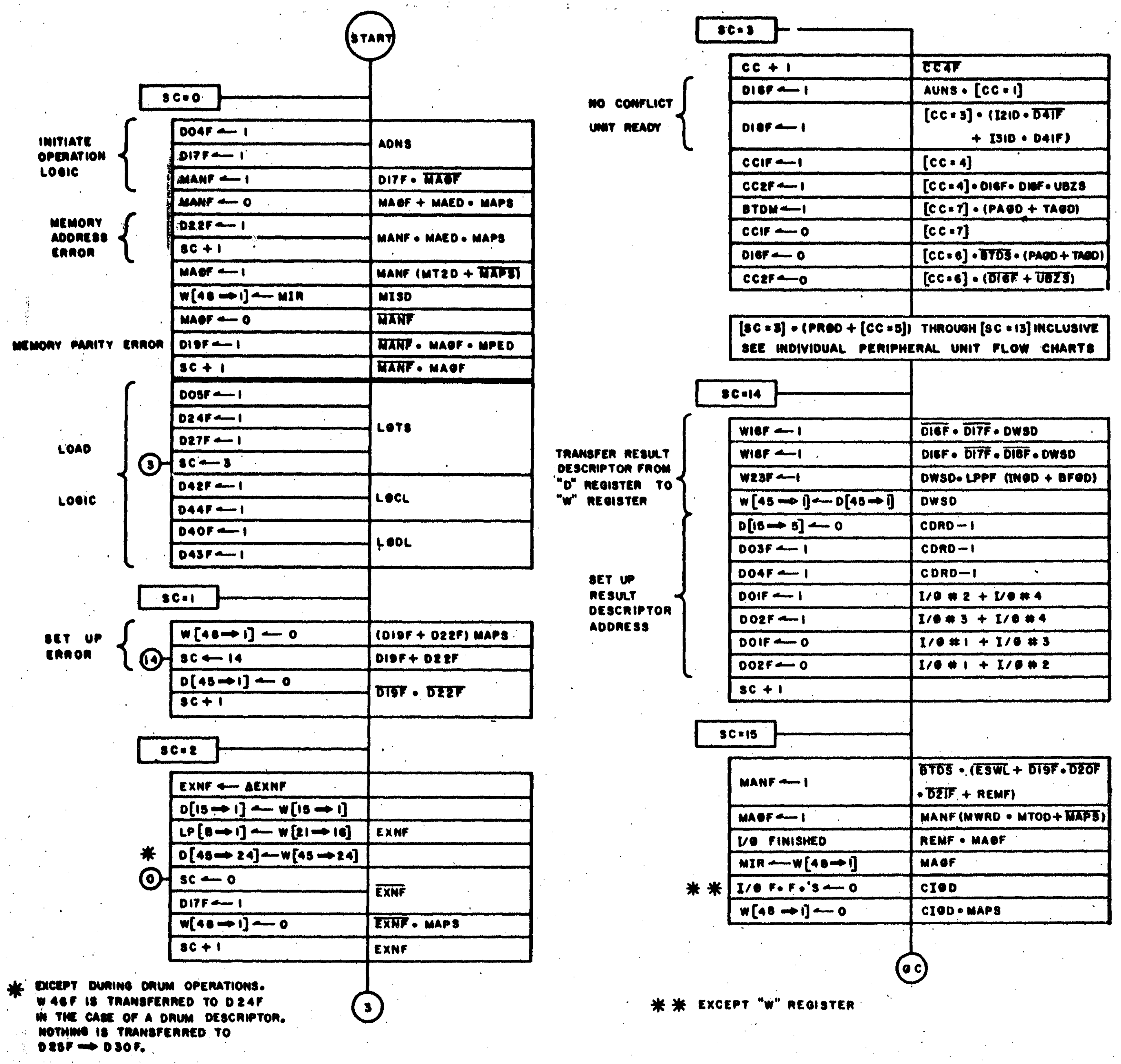


FIGURE 2.2-27
END OF WORD TRANSFER DURING READ

When the I/O has collected a word of information, count SC + 1 to SC = 9 to store the word in memory.

It should be noted that, if the I/O goes to SC = 9 and then SC = 10 and the word count has been reduced to zero, the I/O exits to SC = 14 to produce the Result Descriptor. The D.F.C.U. will continue to read the remainder of the segment (s). If another Disk File operation is initiated, the I/O will find the D.F.C.U. Busy and must wait until the D.F.C.U. is finished.

If Word Count Override is not used, then the end of the operation is indicated by both FWCL and FCBL being false from the D.F.C.U. This causes EXNF to be set and the next I/O clock sets SC = 14 to produce a Result Descriptor.



SC=0

D04F ← 1	ADNS
D17F ← 1	
MANF ← 1	D17F • $\overline{\text{MAOF}}$
MANF ← 0	MAOF + MAED • MAPS
D22F ← 1	MANF • MAED • MAPS
SC + 1	
MAOF ← 1	MANF (MT2D + $\overline{\text{MAPS}}$)
W[48 → 1] ← MIR	MISD
MAOF ← 0	$\overline{\text{MANF}}$
D19F ← 1	$\overline{\text{MANF}}$ • MAOF • MPED
SC + 1	$\overline{\text{MANF}}$ • MAOF
D05F ← 1	LOTS
D24F ← 1	
D27F ← 1	
SC ← 3	
D42F ← 1	LOCL
D44F ← 1	
D40F ← 1	LODL
D43F ← 1	

SC=1

W[48 → 1] ← 0	(D19F + D22F) MAPS
SC ← 14	D19F + D22F
D[45 → 1] ← 0	$\overline{\text{D19F}}$ • $\overline{\text{D22F}}$
SC + 1	

SC=2

EXNF ← ΔEXNF	EXNF
D[15 → 1] ← W[15 → 1]	
LP[8 → 1] ← W[21 → 16]	
D[48 → 24] ← W[45 → 24]	
SC ← 0	$\overline{\text{EXNF}}$
D17F ← 1	
W[48 → 1] ← 0	$\overline{\text{EXNF}}$ • MAPS
SC + 1	EXNF

* EXCEPT DURING DRUM OPERATIONS. W 46F IS TRANSFERRED TO D 24F IN THE CASE OF A DRUM DESCRIPTOR. NOTHING IS TRANSFERRED TO D 25F → D 30F.

SC=3

CC + 1	$\overline{\text{CC4F}}$
D16F ← 1	AUNS • [CC = 1]
D18F ← 1	[CC = 3] • (I21D • $\overline{\text{D41F}}$ + I31D • D41F)
CC1F ← 1	[CC = 4]
CC2F ← 1	[CC = 4] • D16F • D18F • UBZS
BTDM ← 1	[CC = 7] • (PAOD + TAOD)
CC1F ← 0	[CC = 7]
D16F ← 0	[CC = 6] • $\overline{\text{BTDS}}$ • (PAOD + TAOD)
CC2F ← 0	[CC = 6] • ($\overline{\text{D16F}}$ + $\overline{\text{UBZS}}$)

[SC = 3] • (PROD + [CC = 5]) THROUGH [SC = 13] INCLUSIVE SEE INDIVIDUAL PERIPHERAL UNIT FLOW CHARTS

SC=14

W16F ← 1	$\overline{\text{D16F}}$ • $\overline{\text{D17F}}$ • DWSD
W18F ← 1	D16F • $\overline{\text{D17F}}$ • $\overline{\text{D18F}}$ • DWSD
W23F ← 1	DWSD • LPPF (INOD + BFOD)
W[45 → 1] ← D[45 → 1]	DWSD
D[15 → 5] ← 0	CDRD − 1
D03F ← 1	CDRD − 1
D04F ← 1	CDRD − 1
D01F ← 1	I/O # 2 + I/O # 4
D02F ← 1	I/O # 3 + I/O # 4
D01F ← 0	I/O # 1 + I/O # 3
D02F ← 0	I/O # 1 + I/O # 2
SC + 1	

SC=15

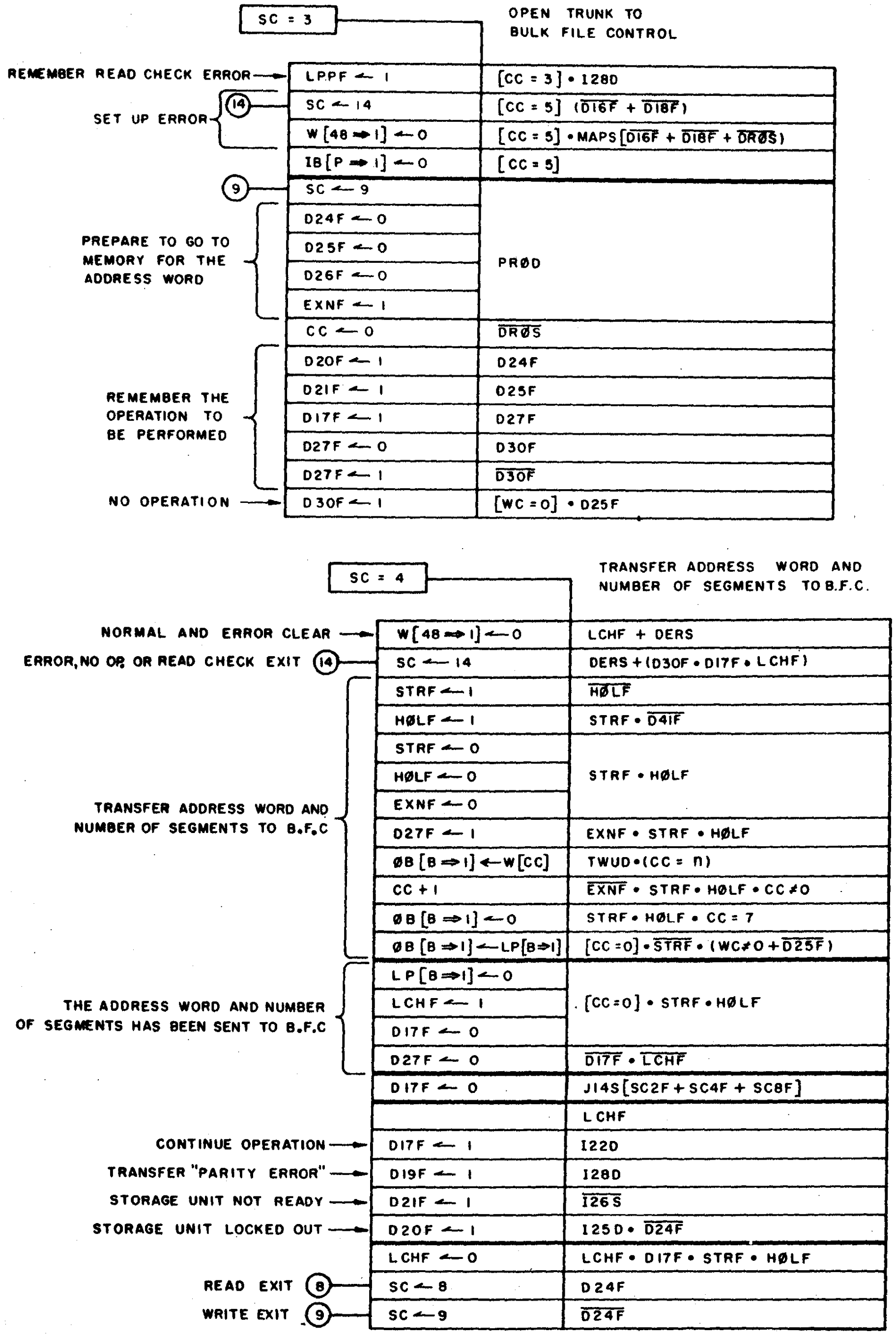
MANF ← 1	$\overline{\text{BTDS}}$ • ($\overline{\text{ESWL}}$ + $\overline{\text{D19F}}$ • $\overline{\text{D20F}}$ • $\overline{\text{D21F}}$ + REMF)
MAOF ← 1	MANF (MWRD • MTOD + $\overline{\text{MAPS}}$)
I/O FINISHED	REMF • MAOF
MIR ← W[48 → 1]	MAOF
I/O F. F.'S ← 0	CIOD
W[48 → 1] ← 0	CIOD • MAPS

* * EXCEPT "W" REGISTER

ADNS = ADMIT DESCRIPTOR LEVEL (FROM CENTRAL CONTROL)
MAED = MEMORY ADDRESS ERROR LEVEL (FROM CENTRAL CONTROL)
MAPS = MEMORY ACCESS PERMIT LEVEL (CONTROLLED BY MAINTENANCE SWITCH)
MTOD = MEMORY TIME ZERO LEVEL (FROM MEMORY UNITS)
MT2D = MEMORY TIME TWO LEVEL (FROM MEMORY UNITS)
MPED = MEMORY PARITY ERROR LEVEL (FROM MEMORY UNITS)
LOTS = LOAD TIME SWITCH (FROM OPERATORS CONSOLE)
LOCL = LOAD CARD LEVEL (FROM OPERATORS CONSOLE)
LODL = LOAD DRUM LEVEL (FROM OPERATORS CONSOLE)
DWSD = [SC = 14] • MAPS = "D" REGISTER TO "W" REGISTER SHIFT DRIVER
MWRD = [SC = 9] • D24F + [SC = 15] = MEMORY WRITE LEVEL
REMF = REMOTE FLIP—FLOP (CONTROLLED BY MAINTENANCE SWITCH)

FIND = REMF • MAOF • [SC = 15] = FINISHED LEVEL
MAND = MANF • MAPS = MEMORY ACCESS NEEDED LEVEL
MISD = MANF • MAOF • MAPS • [SC = 0] = MEMORY INPUT STROBE DRIVER
CIOD = [SC = 15] • MAOF = CLEAR I/O DRIVER
DERS $\overline{\text{D16F}}$ + $\overline{\text{D18F}}$ + D19F + D20F + D21F + D22F = D REGISTER ERROR SWITCH
ESWL = ERROR STOP LEVEL (CONTROLLED BY MAINTENANCE SWITCH)
UBZS = UNIT BUSY
$\overline{\text{UBZS}}$ = UNIT NOT BUSY

FIGURE 2.2-28
I/O LOGIC FLOW (1 of 4)



SC = 3

OPEN TRUNK TO BULK FILE CONTROL

REMEMBER READ CHECK ERROR →	LPPF ← 1	[CC = 3] • 128D
SET UP ERROR ⑭	SC ← 14	[CC = 5] ($\overline{D16F}$ + $\overline{D18F}$)
	W [48 ⇒ 1] ← 0	[CC = 5] • MAPS [$\overline{D16F}$ + $\overline{D18F}$ + $\overline{DRØS}$)
	IB [P ⇒ 1] ← 0	[CC = 5]
⑨	SC ← 9	PRØD
PREPARE TO GO TO MEMORY FOR THE ADDRESS WORD	D24F ← 0	
	D25F ← 0	
	D26F ← 0	
	EXNF ← 1	
	CC ← 0	$\overline{DRØS}$
REMEMBER THE OPERATION TO BE PERFORMED	D20F ← 1	D24F
	D21F ← 1	D25F
	D17F ← 1	D27F
	D27F ← 0	D30F
	D27F ← 1	$\overline{D30F}$
NO OPERATION →	D30F ← 1	[WC = 0] • D25F

SC = 4

TRANSFER ADDRESS WORD AND NUMBER OF SEGMENTS TO B.F.C.

NORMAL AND ERROR CLEAR →	W [48 ⇒ 1] ← 0	LCHF + DERS
ERROR, NO OP, OR READ CHECK EXIT ⑭	SC ← 14	DERS + (D30F • D17F • LCHF)
TRANSFER ADDRESS WORD AND NUMBER OF SEGMENTS TO B.F.C	STRF ← 1	$\overline{HØLF}$
	HØLF ← 1	STRF • $\overline{D41F}$
	STRF ← 0	STRF • HØLF
	HØLF ← 0	
	EXNF ← 0	
	D27F ← 1	EXNF • STRF • HØLF
	ØB [B ⇒ 1] ← W [CC]	TWUD • (CC = n)
	CC + 1	$\overline{EXNF}$ • STRF • HØLF • CC ≠ 0
	ØB [B ⇒ 1] ← 0	STRF • HØLF • CC = 7
	ØB [B ⇒ 1] ← LP [B ⇒ 1]	[CC = 0] • $\overline{STRF}$ • (WC ≠ 0 + $\overline{D25F}$)
THE ADDRESS WORD AND NUMBER OF SEGMENTS HAS BEEN SENT TO B.F.C	LP [B ⇒ 1] ← 0	[CC = 0] • STRF • HØLF
	LCHF ← 1	
	D17F ← 0	
	D27F ← 0	$\overline{D17F}$ • $\overline{LCHF}$
	D17F ← 0	J14S [SC2F + SC4F + SC8F]
		LCHF
CONTINUE OPERATION →	D17F ← 1	I22D
TRANSFER "PARITY ERROR" →	D19F ← 1	I28D
STORAGE UNIT NOT READY →	D21F ← 1	$\overline{I26S}$
STORAGE UNIT LOCKED OUT →	D20F ← 1	I25D • $\overline{D24F}$
	LCHF ← 0	LCHF • D17F • STRF • HØLF
READ EXIT ⑧	SC ← 8	D24F
WRITE EXIT ⑨	SC ← 9	$\overline{D24F}$

BASD = SO4D • BFØD • STRF • HØLF
DERS = $\overline{D16F}$ + $\overline{D18F}$ + D19F + D20F + D21F + D22F
I22D = FCBL
I25D = FWLL
$\overline{I26S}$ = $\overline{FSRL}$
I28D = FERL
J14S = JUMP SC TO 14 SWITCH
Ø21D = FWRL = $\overline{D24F}$ • BFØD • [SC ≠ 15] • [SC ≠ 3]
Ø22D = FBIL = BFØD (D27D + [SC = 4] • [CC ≠ 1])
Ø23D = FDTL = BASD + BFØD • [SC = 4] • J14S • $\overline{D22F}$
Ø24D = FASL = [SC = 4] • $\overline{LCHF}$ • BFØD
TWUD = [CC ≠ 0] • STRF • $\overline{HØLF}$ • BFØD [SC = 4]

FIGURE 2.2-28
I/O LOGIC FLOW (2 of 4)

SC = 8 READ

NORMAL READ I/O TIMING CYCLE PER CHARACTER	STRF ← 1	I23D • I24D • D24F • $\overline{\text{HØLF}}$ • DRØD
	HØLF ← 1	STRF • $\overline{\text{D41F}}$
	STRF ← 0	HØLF
	HØLF ← 0	DRØD • $\overline{\text{I24S}}$
READ IN NEXT CHARACTER →	IBnF ← 1 (UNCL)	I23D • D24F • (FRP−n) • $\overline{\text{HØLF}}$ • DRØD
GENERATE PARITY →	LPnF ← ΔLPnF	STRF • $\overline{\text{HØLF}}$ • IBnF • DRØD
TRANS. CHAR. TO "W" REG. →	W[CC] ← IB[B→1]	STRF • HØLF • $\overline{\text{LPWF}}$ • $\overline{\text{LCHF}}$ • MAPS • (CC = n) • D24D • DRØD
	IB[B→1] ← 0	STRF • HØLF • $\overline{\text{D41F}}$ • $\overline{\text{GPMS}}$
	CC + 1	STRF • HØLF • $\overline{\text{LCHF}}$ • $\overline{\text{LPWF}}$ • DRØD
LAST CHARACTER →	LCHF ← 1	STRF • HØLF • CC = 7 • DRØD
A COMPLETE WORD HAS BEEN READ	LCHF ← 0	STRF • HØLF • LCHF • DRØD
	LP[B→1] ← 0	
	SC + 1	STRF • HØLF • LCHF • D24F • DRØD
CHECK LONG. PARITY →	D20F ← 1	STRF • HØLF • LCHF • LPES • D24F
TRANSFER PARITY ERROR →	D20F ← 1	STRF • HØLF • PELS • D24F + $\overline{\text{I22S}}$ • [CC≠0] • D24F
OPERATION FINISHED →	EXNF ← 1	$\overline{\text{I23S}}$ • $\overline{\text{I22S}}$
⑭	SC = 14	EXNF
	W[48→1] ← 0	
STORAGE UNIT NOT READY →	D21F ← 1	$\overline{\text{I26S}}$ • DRØD

SC = 8 WRITE

NORMAL WRITE I/O TIMING CYCLE PER CHARACTER	STRF ← (UNCL)	I23D • I24D • $\overline{\text{D24F}}$ • $\overline{\text{HØLF}}$ • DRØD
	HØLF ← 1	STRF • $\overline{\text{D41F}}$
	STRF ← 0	HØLF
	HØLF ← 0	$\overline{\text{I24S}}$ • DRØD
SHIFT OUT NEXT CHARACTER →	ØB[B→1] ← W[CC]	TWUD • (CC = n)
	CC + 1	STRF • HØLF • $\overline{\text{LCHF}}$ • $\overline{\text{LPWF}}$ • DRØD
LAST CHARACTER →	LCHF ← 1	STRF • HØLF • CC = 7 • DRØD
PREPARE FOR THE WRITING OF PARITY	ØB[B→1] ← 0	STRF • LCHF • $\overline{\text{D24F}}$ • DRØD
	LPWF ← 1	
A COMPLETE WORD HAS BEEN WRITTEN	LCHF ← 0	STRF • HØLF • DRØD
	LPWF ← 0	STRF • HØLF • $\overline{\text{D24F}}$ • $\overline{\text{LCHF}}$ • LPWF • DRØD
	SC + 1	
INSERT CHARACTER "BLANK" →	ØBAF ← 1	(D22F + D17F) • $\overline{\text{D27F}}$
TRANSFER "PARITY ERROR" →	D19F ← 1	(I28D + $\overline{\text{I22S}}$ • [CC≠1]) $\overline{\text{D24F}}$.
OPERATION FINISHED	EXNF ← 1	$\overline{\text{I23S}}$ • $\overline{\text{I22S}}$
⑭	SC ← 14	EXNF
	W[48→1] ← 0	
STORAGE UNIT LOCKED OUT →	D20F ← 1	I25D • $\overline{\text{D24F}}$ • DRØD
STORAGE UNIT NOT READY →	D21F ← 1	$\overline{\text{I26S}}$ • DRØD

DRØD = BFØD • SC8F
$\overline{\text{I22S}}$ = $\overline{\text{FCBL}}$
I23D = FWCL
$\overline{\text{I23S}}$ = $\overline{\text{FWCL}}$
I24D = FCLP
I24S = $\overline{\text{FCLP}}$
I25D = FWLL
$\overline{\text{I26S}}$ = $\overline{\text{FSRL}}$
I28D = FERL
Ø21D = FWRL = $\overline{\text{D24F}}$ • BFØD • [SC≠15]
Ø22D = FBIL = BFØD • D27D
TWUD = [SC=8] • STRF • DRØD • $\overline{\text{LCHF}}$ • $\overline{\text{LPWF}}$ • $\overline{\text{D24D}}$ • $\overline{\text{D22F}}$ • $\overline{\text{D17F}}$

FIGURE 2.2-28
I/O LOGIC FLOW (3 of 4)

SC = 9 — MEMORY CYCLE

MEMORY ADDRESS OVERFLOW OR NORMAL WRITE CLEAR	SC + 1	AØFF ($\overline{D25F}$ + WC ≠ 0 + D24F)
	W[48 ⇒ 1] ← 0	(AØFF + $\overline{D24F}$ • $\overline{MANF}$) • MAPS
	WC − 1	[WC ≠ 0] • D25F • $\overline{MANF}$
WRITE OPERATION WC OVERRIDE →	D17F ← 1	[WC = 0] • $\overline{D24F}$ • D25F • $\overline{MANF}$
MAINTENANCE CYCLE →	W[45 ⇒ 1] ← D[45 ⇒ 1]	DWSD
	MANF ← 1	$\overline{AØFF}$ • (WC ≠ 0 + $\overline{D25F}$)
FLAG MEMORY CYCLE ERROR →	D22F ← 1	AØFF (WC ≠ 0 + $\overline{D25F}$) + MANF • MAED − C • MAPS
	MANF ← 0	MAED − C • MAPS + MAØF
MEMORY ADDRESSING ERROR →	SC + 1	MANF • MAED − C • MAPS
	MAØF ← 1	MANF • (MWRD • MTOD − M + MT2D − M + $\overline{MAPS}$)
	W[48 ⇒ 1] ← MIR	MISD
READ CLEAR →	W[48 ⇒ 1] ← 0	MAØF • D24F • MAPS
	MAØF ← 0	MWRD
NORMAL AND OVERRIDE COUNT LOGIC →	SC + 1	MANF • MAØF + D17F • $\overline{EXNF}$

SC = 10

MEMORY MAINTENANCE CYCLE ⓪	SC ← 0	MCYS
FLAG MEMORY PARITY ERROR →	D19F ← 1	$\overline{MANF}$ • MAØF • MPED − M
	MAØF ← 0	$\overline{MANF}$
MEMORY ADDRESS OVERFLOW →	AØFF ← 1	D[15 ⇒ 1] = MAX • $\overline{D41F}$ • $\overline{PTØS}$
	D[15 ⇒ 1] + 1	D[15 ⇒ 1] ≠ MAX • $\overline{D41F}$ • $\overline{PTØS}$
SHIFT OUT FIRST CHARACTER →	ØB[8 ⇒ 1] ← W[CC]	TWCD • CC = 0
	CC + 1	$\overline{D24F}$ • $\overline{D41F}$ • $\overline{D26F}$ • $\overline{PTØS}$
CONTINUE OPERATION ⑧	SC ← 8	[I21D • $\overline{EXNF}$ • ($\overline{D24F}$ + WC ≠ 0 + $\overline{D25F}$)] DRØD
END OF OP. OR UNIT NOT READY ⑭	SC ← 14	(I21D • D24F • D25F • [WC = 0] + $\overline{D18F}$) DRØD
FLAG UNIT NOT READY →	D18F ← 0	$\overline{I21S}$ • DRØD
	W[48 ⇒ 1] ← 0	$\overline{D18F}$ • MAPS • DRØD
TRANS. ADDRESS WORD TO B.F.C. ④	SC ← 4	EXNF • I21D
READ OPERATION →	D24F ← 1	D20F • EXNF • MSIOD
USE WORD COUNTER →	D25F ← 1	D21F • EXNF
RELEASE FOR FLAGGING OF ERRORS	D20F ← 0	EXNF • MSIOD
	D21F ← 0	
CONTINUE THE MEMORY MAINT. CYCLE →	IMCF ← 1	$\overline{REMF}$ • RECF • $\overline{AØFF}$ • MCYS
	D19 ← 1	$\overline{D24D}$ • I23D • BFØS

BFØS = BULKFILE OPERATION SWITCH
DRØD = BFØD • SC8F
DWSD = [SC = 9] • $\overline{MANF}$ • MCYS • KEML
I21D = FCRL
I21S = $\overline{FCRL}$
I23D = FWCL
MAED = MEMORY ADDRESS ERROR
MISD = [SC = 9] • $\overline{D24F}$ • MAPS • MANF • MAØF
MPED = MEMORY PARITY ERROR
MSIOD = $\overline{MCYS}$ • [SC = 10]
MWRD = [SC = 9] • D24D
O21D = FWRL = $\overline{D24F}$ • BFØD • [SC ≠ 15]
Ø22D = FBIL = BFØD • D27D
$\overline{PTØS}$ = PRINTER OPERATION NOT
TWCD = [SC = 10] • $\overline{D24D}$ • BFØD • $\overline{D17F}$ • $\overline{D22F}$

FIGURE 2.2-28
I/O LOGIC FLOW (4 of 4)

2.3 DISK FILE CONTROL UNIT OPERATION

The D.F.C.U. serves to connect an E.U. to the External Control. The External Control could be a B200 Processor or a B5000 I/O Channel. A D.F.C.U. can only be connected to one system. The level SIDL2/ indicates to the D.F.C.U. which system is connected.

SIDL2/ False = SIDS/ True = B200
SIDL2/ True = SIDS True = B5000

The System Identification levels cause information to be routed through the D.F.C.U. in the manner required by that system. The information lines are shown in Figure 2.3-1. Information flow paths are shown in the block diagram of the D.F.C.U. in Figure 2.1-1. Note that SIDS/ will route information through the B Register. This buffer is required by the B200 because the Disk File clock can exceed the Processors's capabilities.

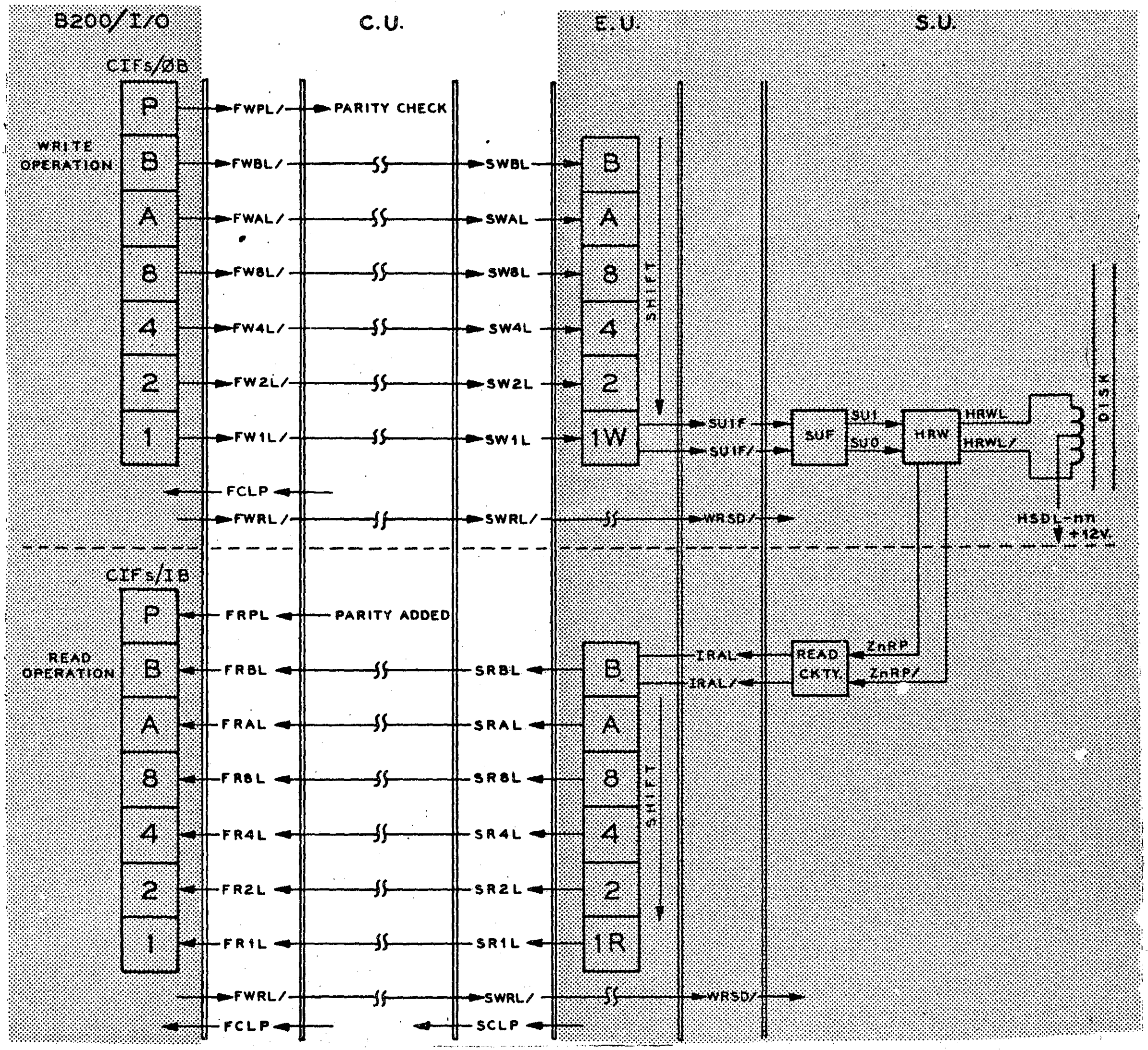


FIGURE 2.3-1
D.F.C.U. IN SUBSYSTEM INFORMATION FLOW

Words are interlaced on the disk and in a Read or Write operation are treated as Active and Inactive. In a Write operation, the B200 uses the time during the Inactive word to transfer the first four characters which will be written during the next Active word. The last character of the second half of the word is transferred to the D.F.C.U. just before the end of the Active word. The D.F.C.U. then goes into the Inactive word and the B200 transfers another four characters.

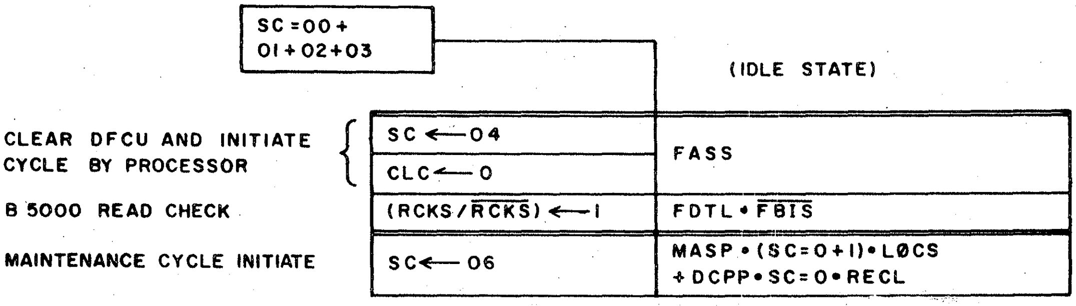


FIGURE 2.3-2
SC = 00 + 01 + 02 + 03

SC = 00 Idle state at the beginning and end of every operation:
+ 01
+ 02 00 = Cleared, or previous operation completed successfully.
+ 03

01 = Parity Error in Address or Information.

02 = Accessed disk was Write Lockout.

03 = Accessed S.U. was Not Ready.

FASL/ to the D.F.C.U. and the first FDTL cause the Sequence Counter to set SC = 4 to receive the Disk File Address. FASL/ is switched to produce FASS within the D.F.C.U. Clock pulses are generated by the system (FDTL) until SC = 10. If the level FBIS/ is true at the first FDTL, the Read Check Cross-coupled Switch is set to cause the D.F.C.U. to perform a Read Check operation.

Refer to Figure 2.3-3 during the following explanations.

SC = 04 Receive the Address digits from the system.
+ 05

The digits are in Binary coding and are set in the N Register from which they are transferred to the LSD position of the A Register. Within the A Register the digits are shifted toward the MSD position as the incoming digits are set into the LSD.

The Clock Counter keeps track of the number of address digits. The clock pulse that counts CLC to 8 should coincide with FASS going false. If FASS is false before CLC = 8 or if FASS is true with the next clock pulse after CLC = 8, set S01F to flag an invalid address (too few or too many address digits).

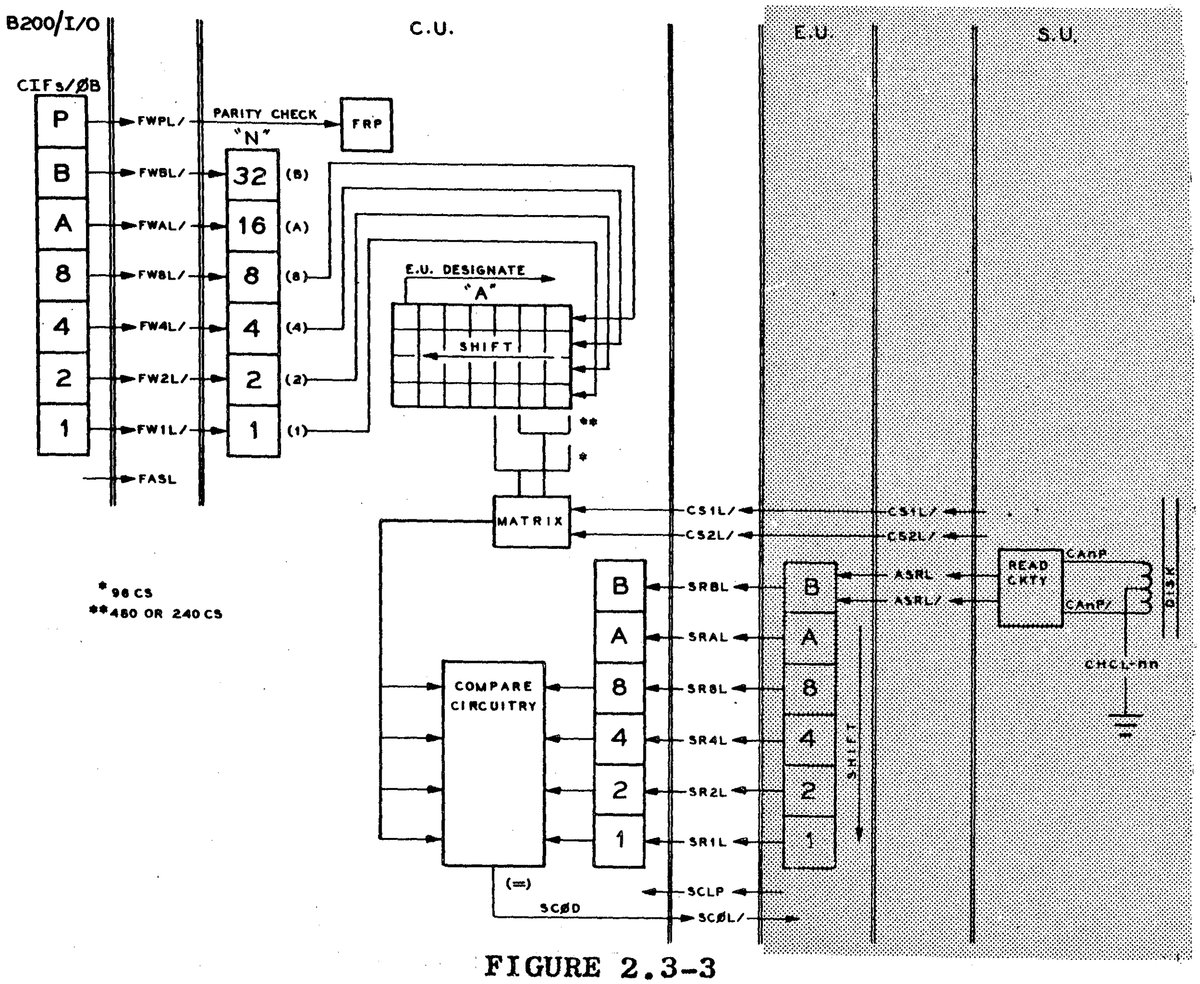


FIGURE 2.3-3
ADDRESS FLOW IN THE D.F.C.U.

SC=04+05

(CONTROL RECEIVES ADDRESS FROM D.P.)

	CLC+1	CLC≠9
SHIFT ADDRESS WORD INTO ADDRESS REGISTER	NnnF ← FWnL AnNF ← A(n-1)NF AInF ← NnnF	FASS•$\overline{CL8F}$
ADDRESS WORD CONTAINS A PARITY ERROR OR F. C.	S0IF ← 1	$[PES \cdot CC \neq 0 + [(N_r = FC) \cdot (\overline{SIDS} + CLC \neq 8) \cdot CC \neq 0 \cdot CC \neq 2 \cdot CC \neq 9]$
INCORRECT NO. OF ADDRESS DIGITS	S0IF ← 1	$\overline{CL8F} \cdot \overline{FASS} + CL8F \cdot FASS$
B200 CHANGE "0" SEGMENTS TO "10"	Nr ← 10	$CLC = 8 \cdot Nr = 0 \cdot \overline{SIDS}$
	CLC ← 0	CLC=9
ADDRESS OK 06	S02F ← 1	$\overline{S0IF}$
ADDRESS WORD INVALID 01	S04F ← 0	S0IF

FIGURE 2.3-4
SC = 04 + 05

The parity of the address digits is checked as they enter the D.F.C.U. They are also checked in the N Register for an FC (Forbidden Combination) condition. A bits, B bits and a number greater than 9 constitutes an FC. S01F is set for parity error or FC.

The segment number is transferred into the N Register as the CLC counts to 8. The clock pulse occurring when CLC = 8 sets N = 10 if a B200 transfers a segment number of zero.

The clock pulse at CLC = 9 clears the Clock Counter and, if no address error occurred during the transfer, sets SC = 06. If an error had occurred, then set SC = 01.

See Figure 2.3-5 for timing.

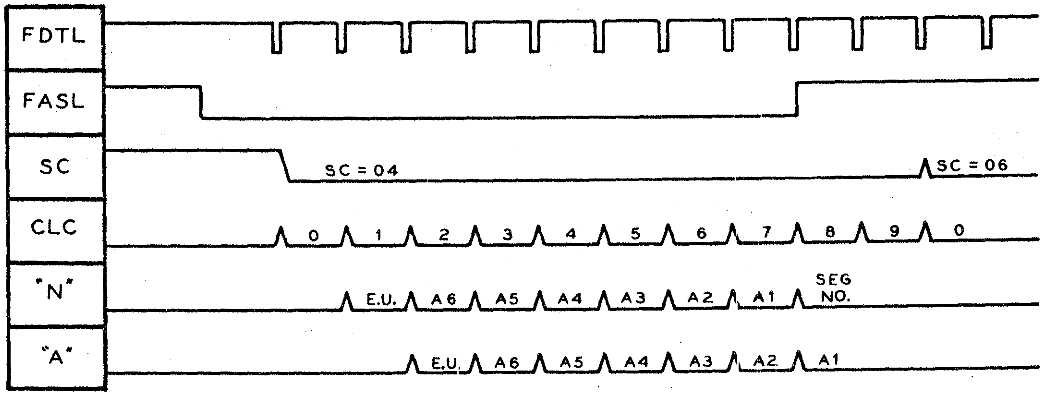


FIGURE 2.3-5
ADDRESS TRANSFER TIMING

B200	B5000
The Processor is at CUF = 3 • MC1F to transfer the Disk File Address. The characters are transferred out of the CIF's with no encoding into BCL. When NVF's = 0, indicating that the address has been transferred, MCF $\rightarrow 3 \cdot \overline{2} \cdot \overline{1}$ to transfer the number of segments and then check to see that no error occurred during address transfer. Clear FASL. If no error, set BBB into MAR to access the area for Read/Write. Set CUF = 6 • MC3F and wait until the D.F.C.U. becomes Busy (FCBL), indicating that the specified address is being sought. Set MCF $\rightarrow \overline{3} \cdot \overline{2} \cdot 1$ for a Write operation, or MCF $\rightarrow \overline{3} \cdot 2 \cdot \overline{1}$ for a Read operation. Clear RUNF and fire the clock B.O. with FCLP's from the D.F.C.U.	When the address word was accessed, the I/O went to SC = 4 to transfer the address digits. The Character Counter points to the digit that must be transferred. When CC = 0, LCHF ← 1 to disable FASL to the D.F.C.U. The I/O remains at SC = 4 until I22D becomes true to indicate that the D.F.C.U. has become Busy. The I/O then sets SC = 9 to access the first word of information for a Write operation, or SC = 8 to collect the characters in a Read operation.

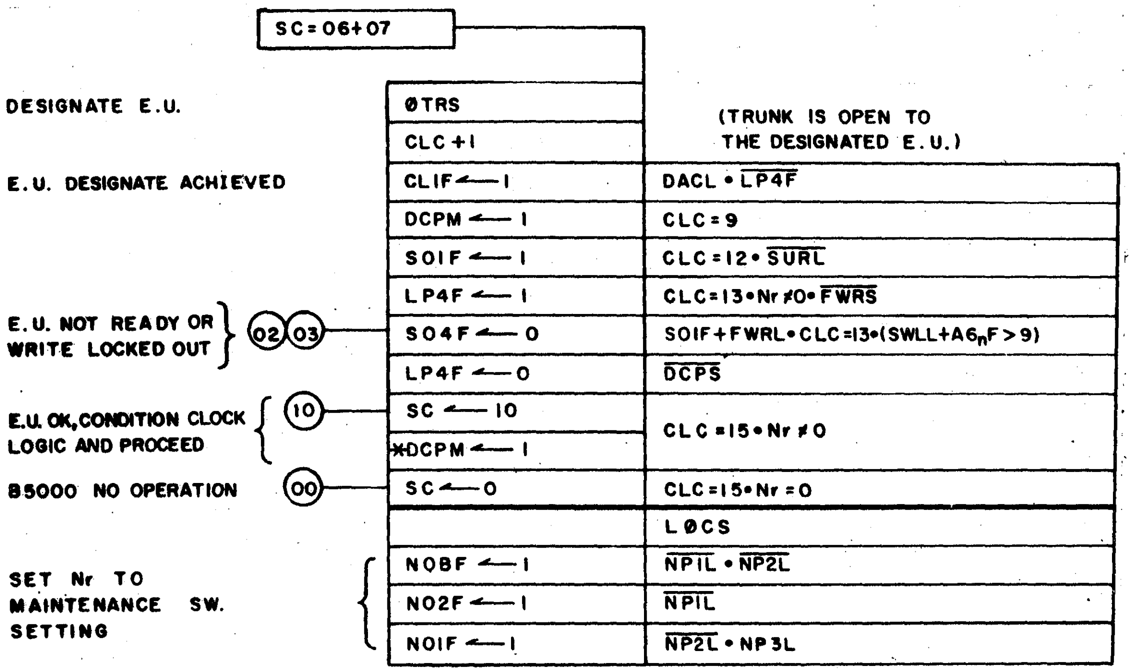


FIGURE 2.3-6
SC = 06 + 07

SC = 06 + 07 The D.F.C.U. decodes the A Register with CS1L/ to access the correct area on the disk as dictated by the segment option and, at the same time, uses the A7nF's which contain the E.U. designate to access the required E.U. The fact that the D.F.C.U. is attempting to access a particular E.U. is indicated by 0TRD/ being false. If the D.F.C.U. is connected to an Exchange, the D.F.C.U. must wait at SC = 06 + 07 until Exchange sends back DACL (Designate Achieved) to indicate that the required E.U. is now logically connected to the D.F.C.U. If the D.F.C.U. is not connected to an Exchange, there is no waiting for a logical connection to the only E.U. in the Subsystem. Therefore, DACL is true immediately and the D.F.C.U. can proceed.

In either case, the address selection lines are sent to the E.U. See Figures 2.3-7 and 2.3-8.

The lines eventually select one S.U., one disk in that S.U., one face of that disk and specific tracks on that face. Three tracks are selected; two clock tracks and one Information track. One of the two clock tracks enables the E.U. to generate Storage Clock Pulses (SCLP's) to the D.F.C.U. The D.F.C.U., when actually performing a Read or Write operation, uses the SCLP's to generate internal clock pulses (CCLnP's) and as a sync pulse for character transfer.

While at SC = 06 + 07, the System is still sending FDTL's to produce CCLnP's (Control Clock Pulses) in the D.F.C.U. The logic CLC + 1 is present, but the Clock Counter cannot count until CL1F is set by DACL being true.

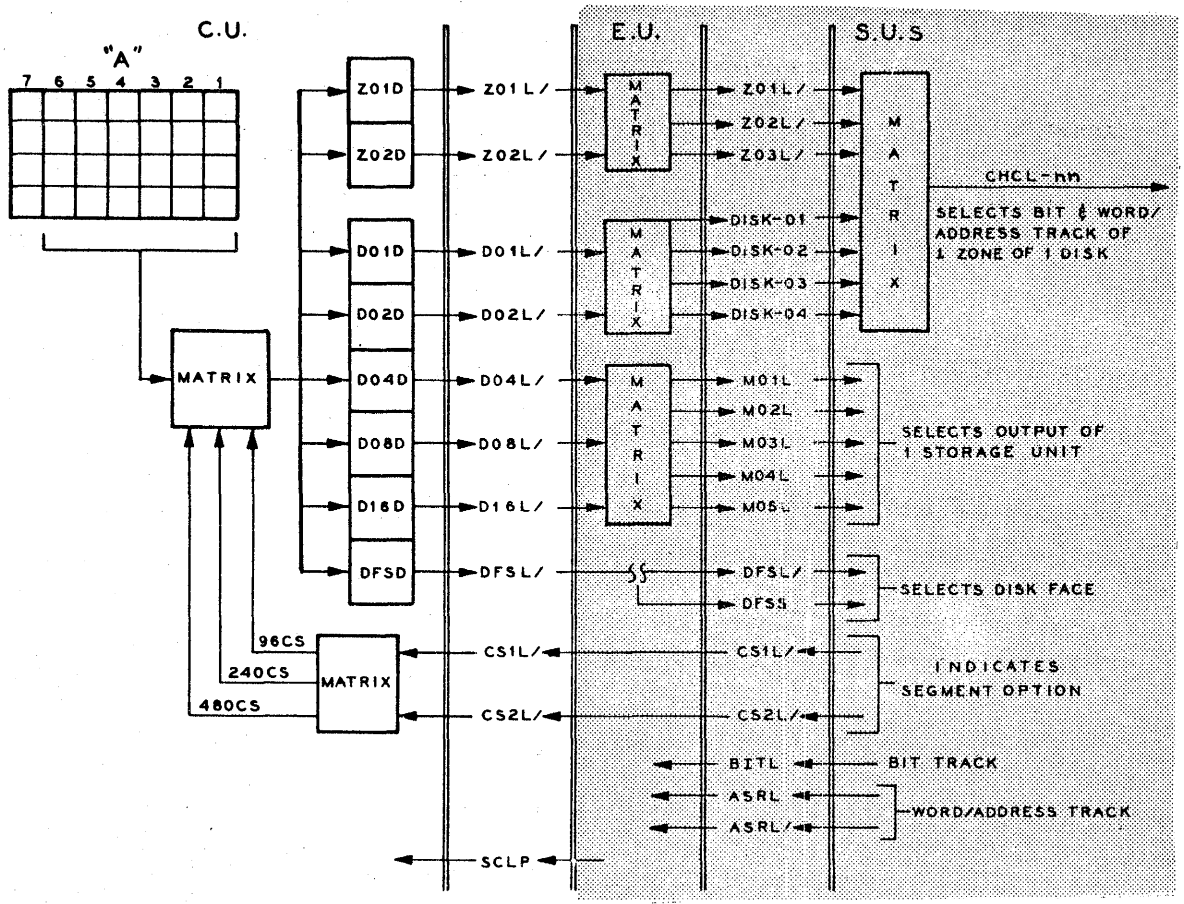


FIGURE 2.3-7
CLOCK TRACK SELECTION

When DACL becomes true, CL1F is set and the Clock Counter begins counting. The E.U. sends levels to the D.F.C.U. to indicate its status and the status of the S.U. If the selected E.U. or S.U. is Not Ready when CLC = 12, S01F is set. If a Write operation is indicated and the selected disk is Locked Out or S01F was set, when CLC = 13, reset S04F to leave SC = 02 + 03.

Note that the DCPM is set when CLC = 9. The Disk Clock Present Multi is 600 microseconds. When CLC = 13, if this is a Read operation (FWRS/), set LP4F. CLC will be counted to 14 by the same clock pulse but cannot count to 15 as LP4F is on. LP4F will be reset when DCPM times out (DCPS/) and CLC = 15 can be set. This logic ensures that gain control has been latched in the E.U. prior to reading.

If the Clock Counter reaches a count of CLC = 15 with no errors, set SC = 10. At this time, FCBL is sent to the System.

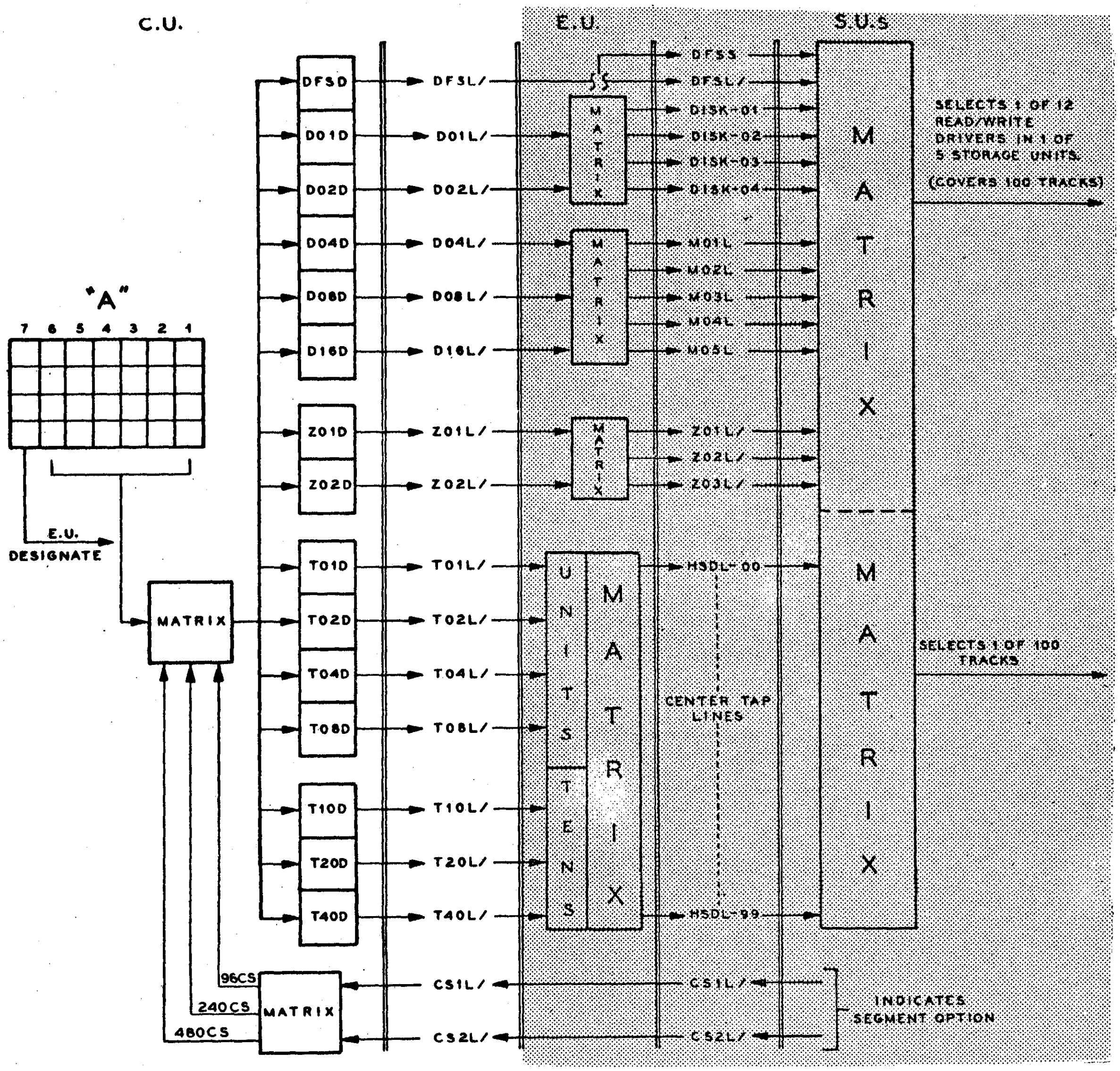


FIGURE 2.3-8
INFORMATION TRACK SELECTION

B200

The CCP after FCBL goes true clears RUNF. CCP's are now produced when the D.F.C.U. sends an FCLP to the Processor.

B5000

FCBL to the I/O sets D17F to 1 to cause the I/O to proceed to SC = 8 for a Read operation or SC = 9 for a Write operation. In either case, the I/O will arrive at SC = 8 for character transfer as FCLP's are sent to the I/O.

The same pulse that set SC = 10 sets DCPM (600 microsecond multi). If this multi is allowed to time out, the D.F.C.U. is forced to SC = 03 (Storage Unit Not Ready) regardless of the existing Sequence Count. Normally, SCLP's from the designated E.U. will continually trigger DCPM inhibiting time out.

The E.U. sends Word Mark Pulses (WØMP) to the D.F.C.U. at the beginning of each word prior to segment coincidence. After segment coincidence, WØMP only occurs at the beginning of an active word. WØMP is a sync pulse for the D.F.C.U. logic.

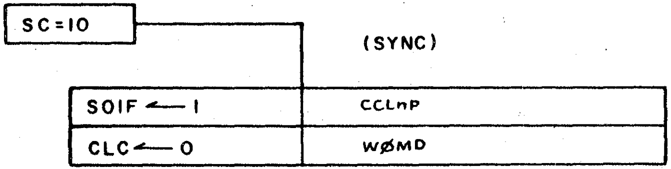


FIGURE 2.3-9
SC = 10 SYNC ON DISK CLOCK

SC = 10 Wait for the first SCLP from the E.U. The CLC was counted to zero in SC = 6 so, if WØMD (WØMP through a driver) occurs, CLC is cleared redundantly. CCLnP from the first SCLP sets S01F for SC = 11.

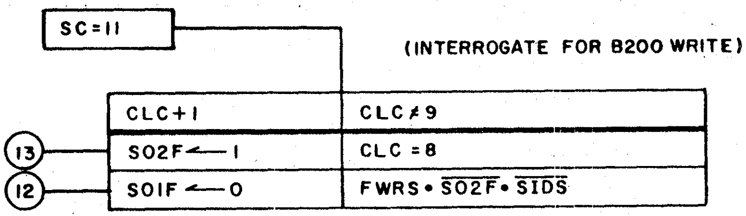


FIGURE 2.3-10
SC = 11 INTERROGATE FOR B200 WRITE

SC = 11 If the System is a B200 Processor (SIDS/) and a Write operation is indicated, set S02F to 1 and clear S01F to leave SC = 12 ready to load the first three characters. For all other operations, set S02F to 1 for SC = 13.

The CLC = 8 logic is necessary to keep the D.F.C.U. in character sync as well as word sync. The D.F.C.U. uses CLC counts to time FCLP's to the B200 Processor during SC = 12. See Figure 2.3-11.

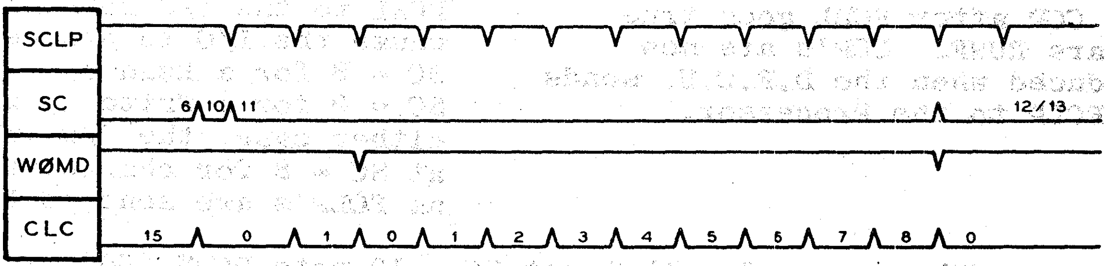
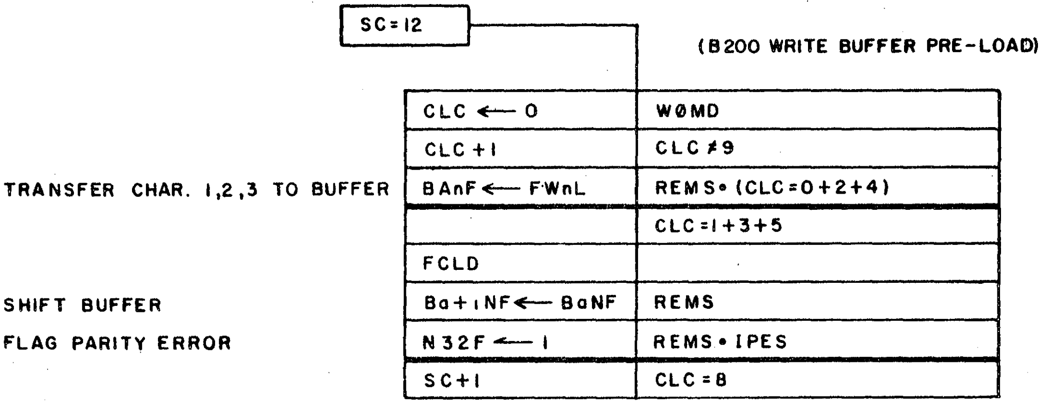


FIGURE 2.3-11
CONTROL LOGIC SYNC ON WORD MARK



SC=12

(B200 WRITE BUFFER PRE-LOAD)

	CLC ← 0	W0MD
	CLC + 1	CLC ≠ 9
TRANSFER CHAR. 1,2,3 TO BUFFER	BAnF ← FWnL	REMS• (CLC=0+2+4)
		CLC=1+3+5
	FCLD	
SHIFT BUFFER	Ba+1NF ← BaNF	REMS
FLAG PARITY ERROR	N32F ← 1	REMS•IPES
	SC+1	CLC=8

FIGURE 2.3-12
SC = 12 B200 WRITE BUFFER PRE-LOAD

SC = 12 For a B200 Write operation only, transfer the first three characters from the B200 Processor to the B Register. The B Register consists of the BAnF's, BBnF's, BCnF's and the BDnF's where n = 1, 2, 4, 8, A or B. Obviously, the register can contain four six-bit characters, but BAnF's are used to compare for the correct Segment Address during SC = 13 and 14, so only three characters are transferred at this time. They are routed from the File Write Lines (FWnL's) into the BAnF's and then shifted toward the BDnF's.

When CLC = 8, the next clock pulse causes SC + 1 to SC = 13. See Figure 2.3-13 for timing.

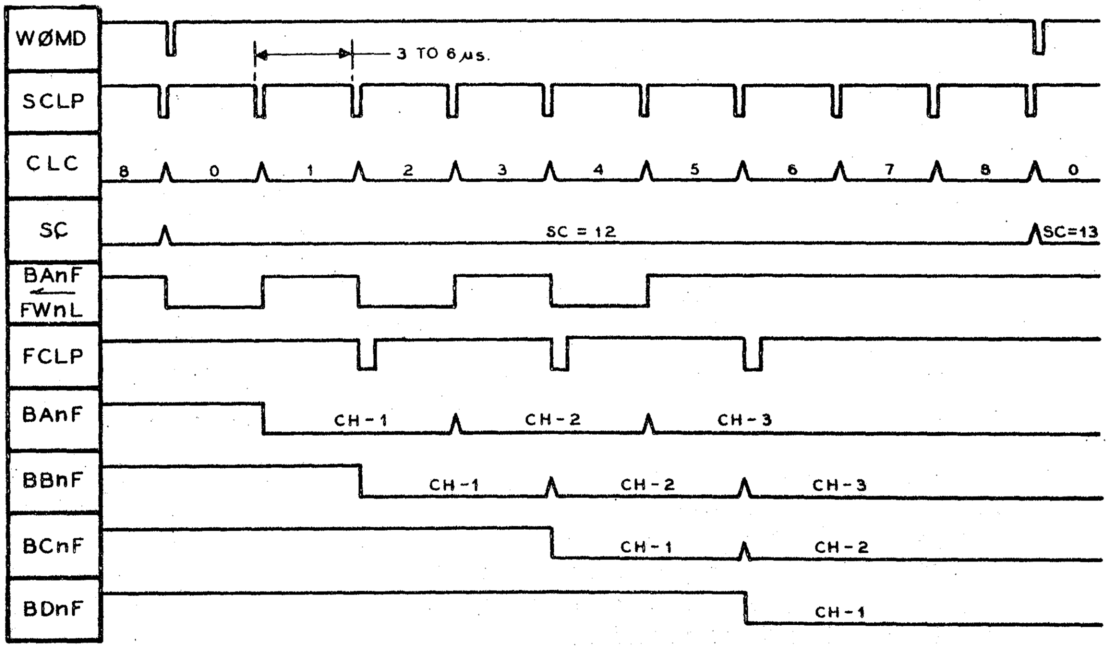


FIGURE 2.3-13
B REGISTER PRE-LOAD TIMING

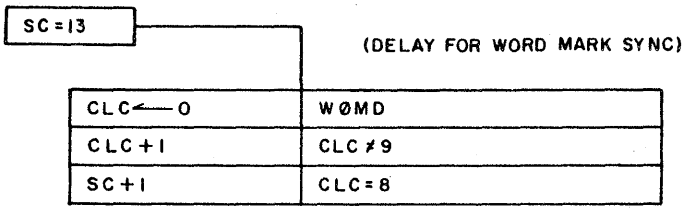


FIGURE 2.3-14
SC = 13 DELAY FOR WORD MARK SYNC

SC = 13 With SC = 13 after SC = 12, the D.F.C.U. will wait one full word time before proceeding while CLC counts from zero to eight. With CLC = 8, set SC = 14. However, when SC = 13 after SC = 14, CLC may be 2, 3, 4 or 5. This situation exists when the comparison for segment address coincidence at SC = 14 was unequal. The action at SC = 13 will count CLC to 8 to maintain the logic in sync with the disk. With CLC = 8, set SC = 14.

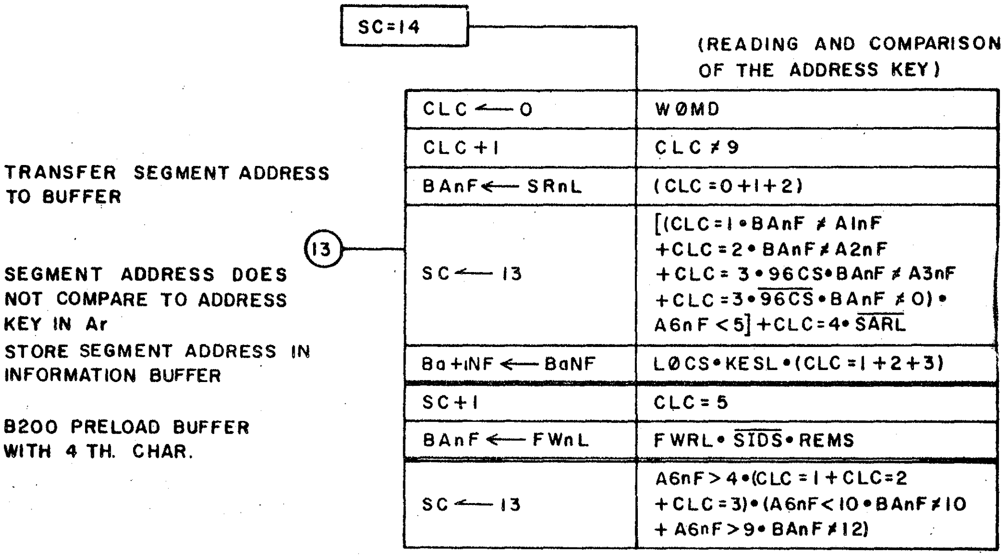


FIGURE 2.3-15
SC = 14 SEGMENT ADDRESS COMPARE

SC = 14 When the designated E.U. is a 240 or 480 option, the Segment Address is contained in A1 and A2. For the 96 option, the Segment Address is in A1, A2 and A3.

The Segment Address digits are read from the disk, LSD first, and set into the BAnF's. BAnF's are compared with the A Register. If the two (or three) address digits do not compare, A and B being unequal will set SC = 13. At SC = 13, CLC is counted to 8 and then at SC = 14, another attempt is made to find comparison.

The Clock Counter, during SC = 14, is keeping a count of the Segment Address digits sent from the E.U. CLC = 1 is the first digit, CLC = 2 is the second, etc. As long as the

BAnF's equal the corresponding digit in the A Register, the D.F.C.U. remains at SC = 14. If the D.F.C.U. is still at SC = 14 when the Clock Counter reached the value of five, SC + 1 to SC = 15. This signifies that comparison existed, segment coincidence has been found.

Also, at CLC = 5, if this is a B200 Write operation, set the fourth character in BAnF's. (No longer needed for compare function.)

The Maintenance Segment Addresses are not compared against the A Register as they are FC's. A6nF's having a value greater than four indicate a Maintenance Segment operation and inhibit the normal comparison at SC = 14.

The first Maintenance Segment Address consists of four 10's (8 and 2 bits); the second consists of six 12's (8 and 4 bits). The first Maintenance Segment, MS1, is specified by the A6nF's greater than four and less than ten. The second, MS2, is specified by the A6nF's greater than nine and less than fifteen.

	MS1	MS2
A6nF's =	5	10
	6	11
	7	12
	8	13
	9	14

READ

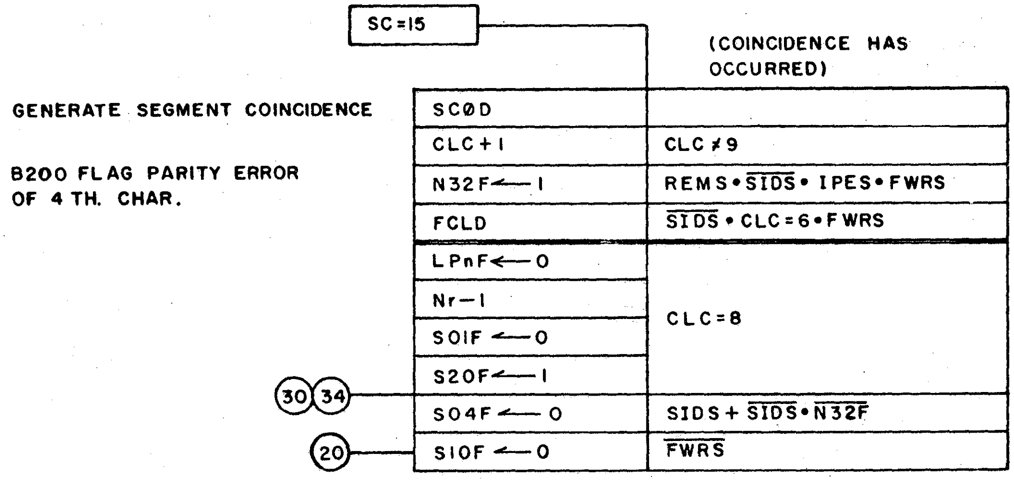


FIGURE 2.3-16
SC = 15 SEGMENT COINCIDENCE

SC = 15 The Following actions occur:

1. Generate SCØD to the E.U. to indicate Segment Coincidence.

2. At CLC = 6, send an FCLP to the System, if this is a B200 Write operation, to enable the Processor to access the fifth character. Set N32F to 1 if a parity error occurred on the fourth character.

3. When CLC = 8, set SC = 20 for a Read operation or SC = 30 for a Write operation. CLC = 8 indicates the end of a word, so SC = 20 or 30 just prior to the Word Mark beginning the first Active word.

4. The N Register is counted down by one as this is the beginning of a segment.

SC=20+24

(READ-ACTIVE WORD)

	SC0D	
	CLC ← 0	W0MD
	CLC + 1	$\overline{\text{CL8F}}$
TRANSFER CHARACTERS READ	BAnF ← SRnS	
INTO BUFFER AND SHIFT	Ba+1NF ← BaNF	
GENERATE LONGITUDINAL PARITY CHARACTER	LPnF ← Δ LPnF	CLC ≠ 9 · SRnS
	SC+1	CLC = 8
	CL8F ← 0	
B 5000		SIDS
SET WORD COINCIDENCE	(FWCS/$\overline{\text{FWCS}}$) ← 1	CLC = 0 • $\overline{\text{SCLS}}$
REGENERATE E. U. READ	FRnD	SRnS
AND CLOCK LINES	FCLD	SCLM
B200		$\overline{\text{SIDS}}$
TRANSFER CHARACTERS 1, 2, 3, 4 TO PROCESSOR	FRnL	BAnF • CLC = 1 + BBnF • CLC = 3 + BCnF • CLC = 5 + BDnF • CLC = 7
	FCLD	SCLS • (CLC = 1+3+5+7)

FIGURE 2.3-17
SC = 20 + 24 READ-ACTIVE WORD

SC = 20 + 24 S04F could have been set as a result of a parity error. Accept nine characters from the E.U. An SCLP from the E.U. indicates that a character is ready for transfer. The character is held in the Storage Read Cross-coupled Switches (SRnS) for 1.6 microseconds.

The true state of the six bits of the character will complement their respective Longitudinal Parity Flip-Flops LPnF's). At the end of the word, since odd parity is used, the bits of the LP character should leave all the LPnF's set.

The characters are shifted into the BAnF's from the Storage Read Switches and shifted through the B Register. The set and shift occurs at each clock pulse until CLC = 8. See Figure 2.3-18 for timing.

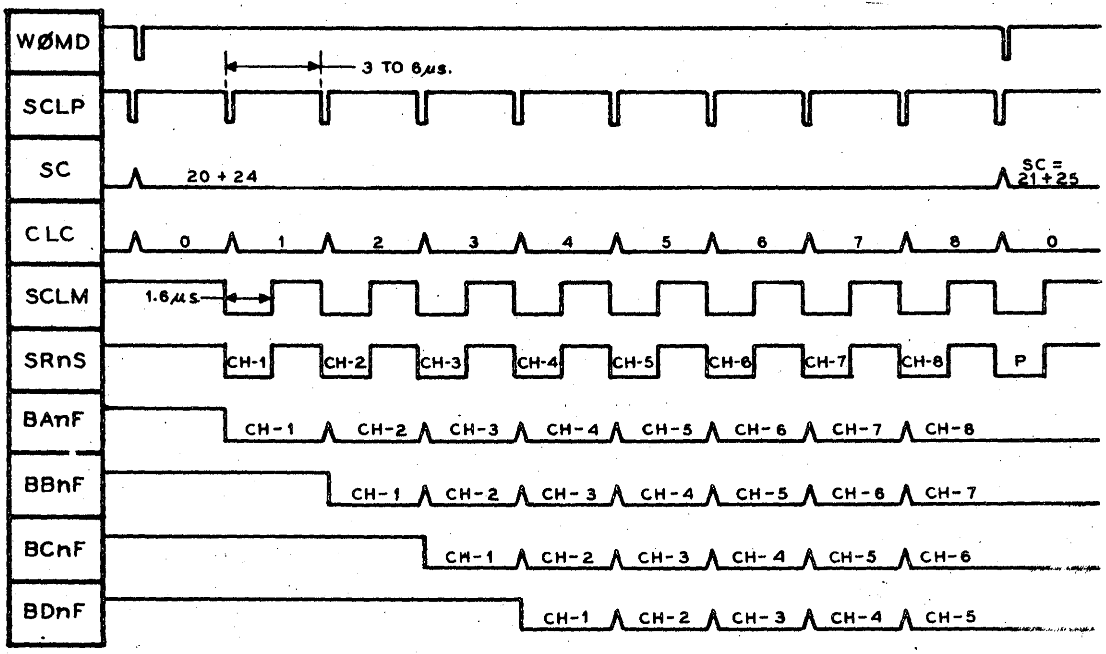


FIGURE 2.3-18
READ TIMING DURING ACTIVE WORD

The B Register action occurs regardless of the type of System.

Notice that, at the end of the Active word, the B Register contains the last four characters. This is only significant for B200 operation where buffering is required. The Longitudinal Parity Character will not be shifted into the B Register, but will complement LPnF's.

B200

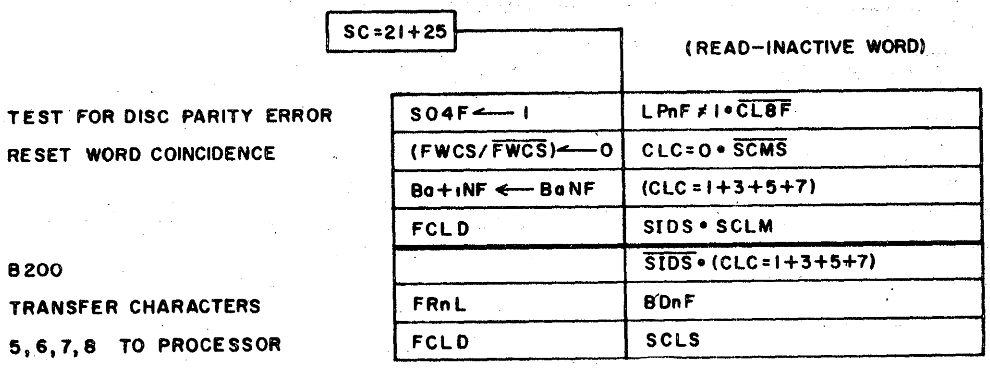
The Processor is at CUF = 6 • MC2F for a Read operation. Each FCLP from the D.F.C.U. sets a character into the AIF's and transfers a character from the AIF's through the encoder into the CIF's. The same FCLP starts a memory cycle which writes CIF's into memory. The B200 cannot handle FCLP's and characters every 3 microseconds, so an FCLP is only produced at CLC = 1 + 3 + 5 + 7. In Figure 2.3-18, the first, second, third and fourth characters are found in the BAnF's,

B5000

The I/O is at SC = 8 during a Read operation. The File Word Coincidence Switch (FWCS) is latched at SC = 20. FCLP's are produced continuously during Active and Inactive words. The FWCS level (FWCL/ to the I/O) indicates an Active word. I23D (FWCL) must be true to transfer characters to the IB. The FCLP to the I/O is 1.6 microseconds because the multi SCLM produces it. STRF is set with an FCLP and a one-megacycle clock pulse. SCLM in the D.F.C.U. also holds the SRnS (FRnL's to the

BBnF's, BCnF's and BDnF's, respectively. The FRnL's are gated by the BnnF's selected by the CLC.

I/O) latched for the 1.6 microseconds.



TEST FOR DISC PARITY ERROR	S04F ← 1	LPnF ≠ 1 • $\overline{CL8F}$
RESET WORD COINCIDENCE	(FWCS/$\overline{FWCS}$) ← 0	CLC=0 • $\overline{SCMS}$
	Ba+1NF ← BaNF	(CLC=1+3+5+7)
	FCLD	SIDS • SCLM
B200		$\overline{SIDS}$ • (CLC=1+3+5+7)
TRANSFER CHARACTERS	FRnL	B'DnF
5,6,7,8 TO PROCESSOR	FCLD	SCLS

FIGURE 2.3-19
SC = 21 + 25 READ-INACTIVE WORD

SC = 21 + 25 Inactive word in a Read operation. The LPnF's should be set. If LPnF ≠ 1, set S04F to remember that a Parity Error occurred.

B200

The B Register is shifted at CLC = 1 + 3 + 5 + 7 which causes the last four characters to appear in the BDnF's at the respective CLC counts. This and the FCLP's to the B200 allow the Processor to receive and store the last four characters during the Inactive word.

B5000

FWCS-0 inhibits FCLP's in the I/O while a word is being transferred to memory during SC = 9 and 10.

WRITE

SC=30+34

(WRITE-ACTIVE WORD)

	SCØD	
	CLC ← 0	WØmD
	CLC+1	CLC<7
	Ba+NF ← BaNF	$\overline{CL8F}$
GENERATE L.P. CHARACTER	LPnF ← ΔLPnF	SWnS• $\overline{CL8F}$
(MAINTENANCE) CIRCULATE BUFFER	BAnF ← BDnF	$\overline{CL8F}$ •LØCS
FLAG PARITY ERROR FORM PROCESSOR	SO4F ←	IPES•(CLC=1+2+3+4+5+6+7+15)•REMS
	CL8F ← 1	CLC=7
	SC+1	CLC=15
B5000		SIDS
SET WORD COINCIDENCE	(FWCS/ $\overline{FWCS}$) ← 1	CLC=0
REGENERATE PROCESSOR WRITE LINES	SWnL	CLC≠15•FWnL+CLC=15• $\overline{LPnF}$
TRANSFER INFORMATION INTO THE BAnF'S TO CHECK LATERAL PARITY	BAnF ← FWnL	$\overline{CL8F}$
	FCLD	SCLM• $\overline{SCLS}$
B200		$\overline{SIDS}$
SHIFT LAST 4 CHARACTERS INTO BUFFER	BAnF ← FWnL	REMS•(CLC=0+2+4+6)
TRANSFER 8 CHARACTERS AND L.P. CHARACTER TO E.U.	SWnL	BDnF·(CLC=0+1+2+3+4) +BCnF•CLC=5 +BBnF•CLC=6 +BAnF•CLC=7 + $\overline{LPnF}$ •CLC=15
	FCLD	(CLC=1+3+5+7)

FIGURE 2.3-20
SC = 30 + 34 WRITE-ACTIVE WORD

SC = 30 + 34 Transfer nine characters to the E.U. An SCLP indicates transfer time for each character.

The LPnF's are complemented by the Storage Write Levels (SWnS) to the E.U. After eight characters have been sent to the E.U., the "0" output levels of the LPnF's represent odd word parity and are transferred to the E.U.

The B Register is shifted to enable the last four characters from a B200 to be loaded.

When CLC = 7, the next clock pulse sets S08F to make CLC = 15. This causes the SWnL's to be gated from LPnF/'s to write Longitudinal Parity.

B200

The first four characters of the word are already contained in the B Register. The BDnF's contain the first character, the BCnF's the second, etc. The SWnL's are gated from the BDnF's while the characters coming from the Processor at CLC = 0 + 2 + 4 + 6 are being placed into the BAnF's. When the first four characters have been written from the BDnF's, the last four have been loaded into the B Register. The SWnL's are gated by the BnnF's selected by CLC. FCLP's are sent to the Processor at CLC = 1 + 3 + 5 + 7 to access the last four characters. See Figure 2.3-21 for timing.

B5000

File Word Coincidence (FWCS) is latched immediately upon entering this block. FCLP's to the I/O transfer characters from the ØB to the D.F.C.U. The lines are gated through the D.F.C.U. to the E.U. and the characters are set into BAnF's for lateral parity check. The FCLP's cause the Character Counter (CC) to count +1 to point at the next character in the W Register. Refer to Figure 2.2-21.

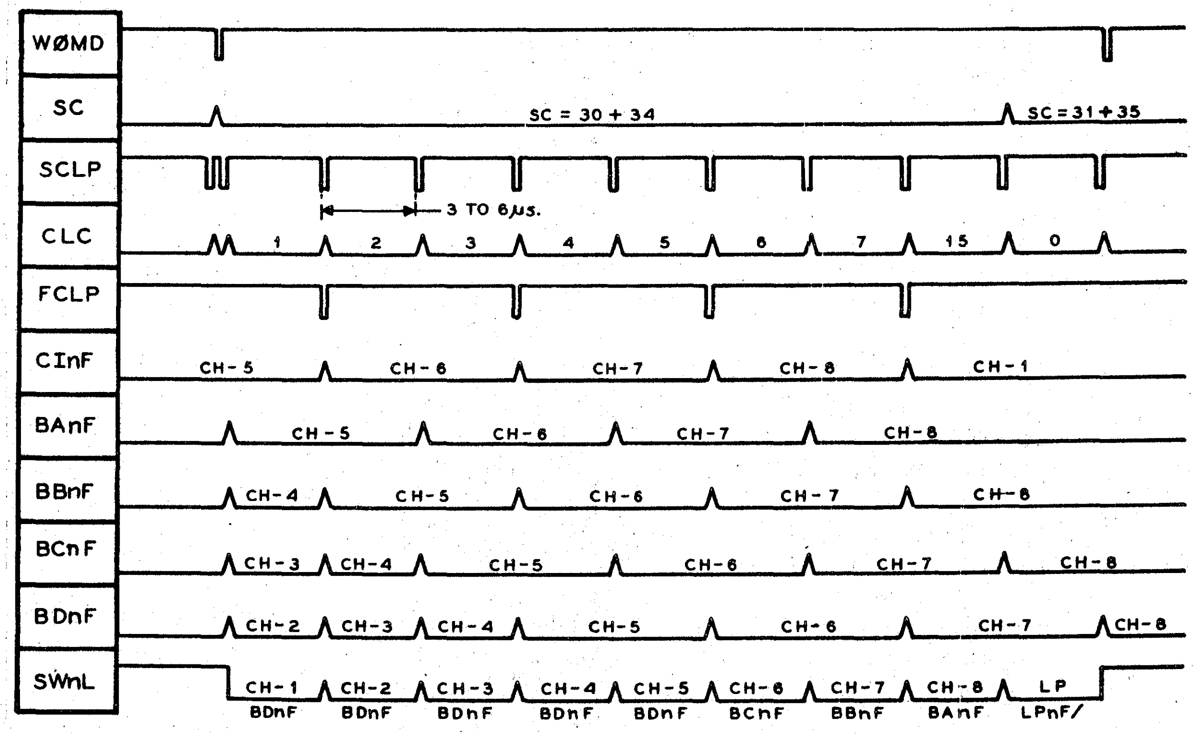
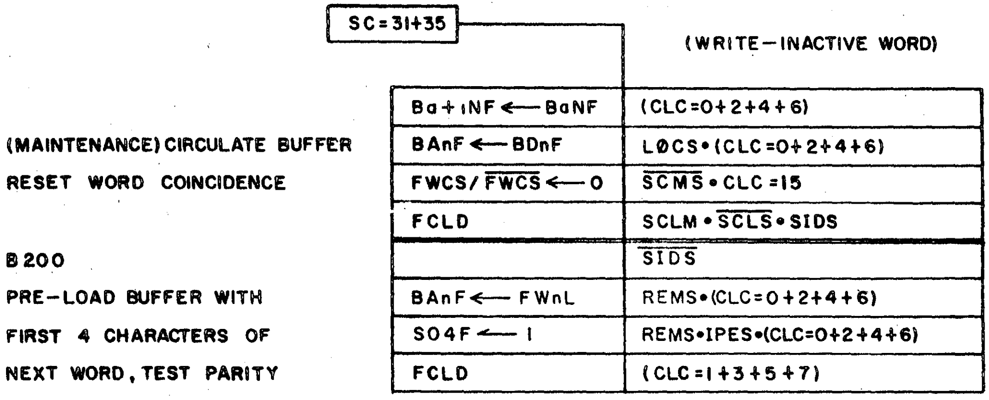


FIGURE 2.3-21
B200 WRITE TIMING



SC=31+35

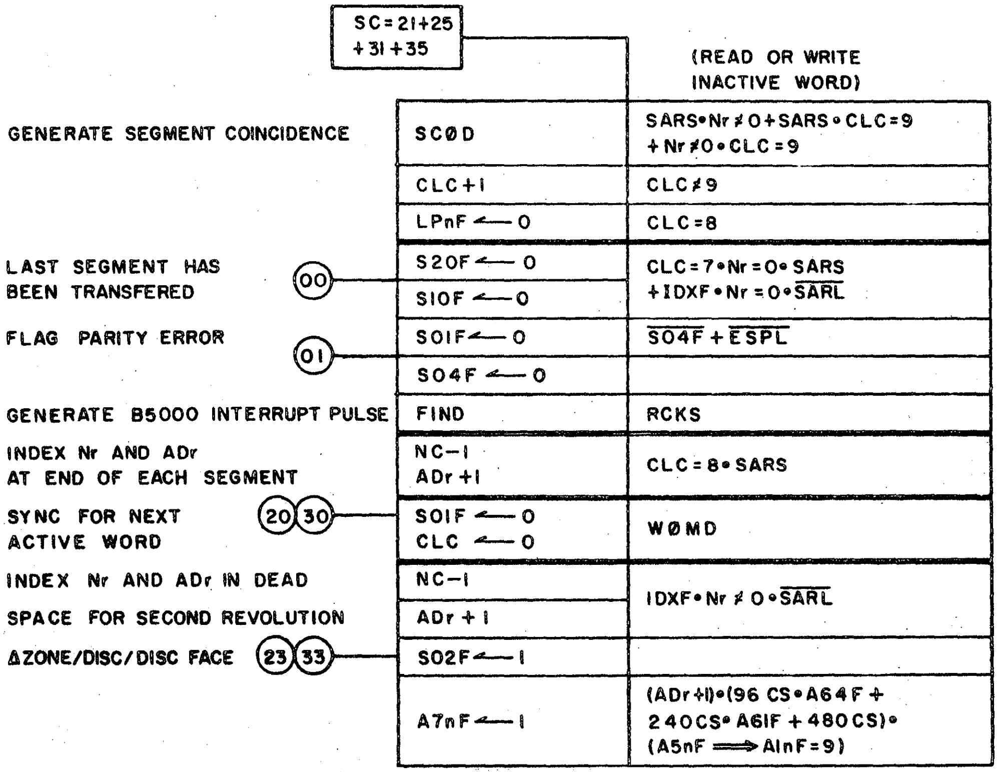
(WRITE-INACTIVE WORD)

	Ba+1NF ← BaNF	(CLC=0+2+4+6)
(MAINTENANCE) CIRCULATE BUFFER	BAnF ← BDnF	L0CS•(CLC=0+2+4+6)
RESET WORD COINCIDENCE	FWCS/$\overline{FWCS}$ ← 0	$\overline{SCMS}$•CLC=15
	FCLD	SCLM•$\overline{SCLS}$•SIDS
B200		$\overline{SIDS}$
PRE-LOAD BUFFER WITH	BAnF ← FWnL	REMS•(CLC=0+2+4+6)
FIRST 4 CHARACTERS OF	S04F ← 1	REMS•IPES•(CLC=0+2+4+6)
NEXT WORD, TEST PARITY	FCLD	(CLC=1+3+5+7)

FIGURE 2.3-22
SC = 31 + 35 WRITE-INACTIVE WORD

SC = 31 + 35 The B Register is shifted as part of the pre-load operation required if the System is a B200.

Set FWCS to 0 to inhibit FCLP's in the B5000 I/O. If the System is a B200, generate four FCLP's and transfer the first four characters of the next word into the B Register. Set S04F if a Parity Error occurs.



SC=21+25 +31+35

(READ OR WRITE INACTIVE WORD)

GENERATE SEGMENT COINCIDENCE		SC0D	SARS•Nr≠0+SARS•CLC=9 +Nr≠0•CLC=9
		CLC+1	CLC≠9
		LPnF ← 0	CLC=8
LAST SEGMENT HAS BEEN TRANSFERED	(00)	S20F ← 0 S10F ← 0	CLC=7•Nr=0•SARS +IDXF•Nr=0•$\overline{SARL}$
FLAG PARITY ERROR	(01)	S01F ← 0	$\overline{S04F}$+$\overline{ESPL}$
		S04F ← 0	
GENERATE B5000 INTERRUPT PULSE		FIND	RCKS
INDEX Nr AND ADr AT END OF EACH SEGMENT		NC−1 ADr+1	CLC=8•SARS
SYNC FOR NEXT ACTIVE WORD	(20)(30)	S01F ← 0 CLC ← 0	W0MD
INDEX Nr AND ADr IN DEAD SPACE FOR SECOND REVOLUTION		NC−1 ADr+1	IDXF•Nr≠0•$\overline{SARL}$
ΔZONE/DISC/DISC FACE	(23)(33)	S02F ← 1	
		A7nF ← 1	(ADr+1)•(96 CS•A64F+ 240CS•A61F+480CS)• (A5nF ⟹ A1nF=9)

FIGURE 2.3-23
SC = 21 + 25 + 31 + 35

SC = 21
+ 25
+ 31
+ 35

During the Inactive word of a Read or Write operation, the following actions can occur:

1. If the Read or Write operation is complete, set SC = 00 or SC = 01 if S04F was on. The operation is complete when N = 0 and an address (SARL) is read.

   If RCKS is latched at this time, a File Pulse (FIND/) is sent to the B5000 System to set CCI15F if D.F.C.U. 1 or CCI16G if D.F.C.U. 2.

2. At the end of the segment, the A Register is counted +1 and the N Register counted -1 if the operation is not complete.

3. If a second revolution cross-over is required (IDXF • $N \neq 0$ • $\overline{SARL}$), set S02F for SC = 23 + 27 + 33 + 37 to sync on the next zone/face/disk. The Index FF, IDXF, would have been set by a simulated INXP at Maintenance Segment 2 address (MS2).

   NOTE

   A change of zone/face/disk is allowed, but a change from a legitimate segment to a Maintenance Segment operation must not occur. If this condition is sensed in the A Register, set all A7nF's to 1 which will be interpreted as a non-existent E.U. DCPM will time out and set SC←03.

4. If none of the above conditions exist, the next Word Mark causes a return to SC = 20 + 30 for next Active word.

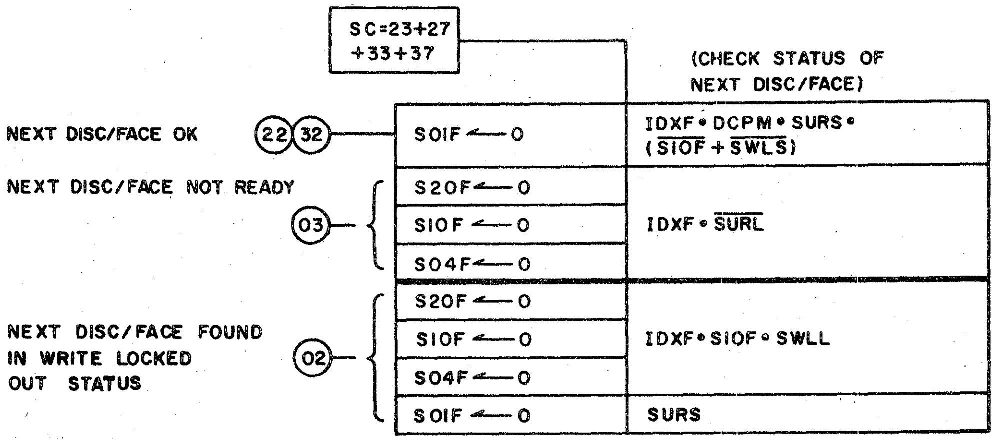


FIGURE 2.3-24
SC = 23 + 27 + 33 + 37

SC = 23
+ 27
+ 33
+ 37

A second revolution cross-over with a change of zone/face/disk requires the operation resume immediately after the Dead Space on the next zone/face/disk. An Index Pulse (INXP) from the E.U. indicates that the Dead Space has been encountered and DCPM (600 microseconds) would start to time out. SURS only requires checking after a change of Module. With SURS true, clear S01F. If the next S.U. is Not Ready (SURL/), the clock pulse generated when DCPM time out will clear S10F, S20F and S04F (if set) to leave SC = 03.

If the next disk is Locked Out and a Write operation is being performed, set SC = 02 to indicate a Write Lockout condition.

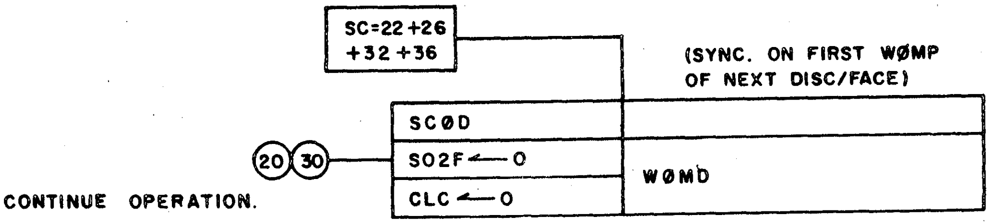


FIGURE 2.3-25
SC = 22 + 26 + 32 + 36

SC = 22
+ 26
+ 32
+ 36

An Active word operation must begin with the next Word Mark from the E.U. When it occurs, clear S02F for SC = 20 + 24 + 30 + 34.

SC=00+ 01+02+03

(IDLE STATE)

CLEAR DFCU AND INITIATE CYCLE BY PROCESSOR	SC ← 04	FASS
	CLC ← 0	
B 5000 READ CHECK	(RCKS/$\overline{RCKS}$) ← 1	FDTL • $\overline{FBIS}$
MAINTENANCE CYCLE INITIATE	SC ← 06	MASP • (SC=0+1) • L0CS + DCPP • SC=0 • RECL

SC=04+05

(CONTROL RECEIVES ADDRESS FROM D.P.)

	CLC+1	CLC≠9
SHIFT ADDRESS WORD INTO ADDRESS REGISTER	NnnF ← FWnL	FASS • $\overline{CL8F}$
	AnNF ← A(n-1)NF	
	A1nF ← NnnF	
ADDRESS WORD CONTAINS A PARITY ERROR OR F. C.	S0IF ← 1	IPES • CC≠0 + [(N_r=FC) • ($\overline{SIDS}$ + CLC≠8) • CC≠0 • CC≠2 • CC≠9]
INCORRECT NO. OF ADDRESS DIGITS	S0IF ← 1	$\overline{CL8F}$ • $\overline{FASS}$ + CL8F • FASS
B200 CHANGE "0" SEGMENTS TO "10"	Nr ← 10	CLC=8 • Nr=0 • $\overline{SIDS}$
	CLC ← 0	CLC=9
ADDRESS OK (06)	S02F ← 1	$\overline{S0IF}$
ADDRESS WORD INVALID (01)	S04F ← 0	S0IF

SC=06+07

(TRUNK IS OPEN TO THE DESIGNATED E.U.)

DESIGNATE E.U.	0TRS	
	CLC+1	
E.U. DESIGNATE ACHIEVED	CL1F ← 1	DACL • $\overline{LP4F}$
	DCPM ← 1	CLC=9
	S0IF ← 1	CLC=12 • $\overline{SURL}$
	LP4F ← 1	CLC=13 • Nr≠0 • $\overline{FWRS}$
E.U. NOT READY OR WRITE LOCKED OUT (02)(03)	S04F ← 0	S0IF + FWRL • CLC=13 • (SWLL + $A6_nF$ > 9)
	LP4F ← 0	$\overline{DCPS}$
E.U. OK, CONDITION CLOCK LOGIC AND PROCEED (10)	SC ← 10	CLC=15 • Nr≠0
	*DCPM ← 1	
B5000 NO OPERATION (00)	SC ← 0	CLC=15 • Nr=0
		L0CS
SET Nr TO MAINTENANCE SW. SETTING	N0BF ← 1	$\overline{NP1L}$ • $\overline{NP2L}$
	N02F ← 1	$\overline{NP1L}$
	N01F ← 1	$\overline{NP2L}$ • NP3L

FLOATING CLOCK LOGIC

REGENERATE PROCESSOR CLOCK	CCLNP	FDTS • $\overline{S1OF}$ • $\overline{S2OF}$ • REMS
REGENERATE E.U. CHARACTER CLOCK	SCLF	SCLS • (S1OF + S2OF + LOCS • SC=6) • CISS
	CCLNP	SCLF • $\overline{SCLS}$
REGENERATE E.U. INDEX CLOCK	IDXM ← 1	INXP • (SC≠6+7)
	IDXF	IDXM(S1OF + S2OF + LOCS • SC=6)
	CCLNP	IDXF • $\overline{IDXS}$
TEST FOR ABSENCE OF E.U. CLOCK, SET DFCU TO E.U. NOT READY STATE (SC=3) ON CLOCK FAILURE	*/DCPM	SCLF • (SC≠6+7)
	DCPP	DCPM!
	IDXM	DCPP • $\overline{RECS}$ · (SC≠6+7)
	IDXF	IDXM (S1OF + S2OF + LOCS • SC=6)
	CCLNP	IDXF • $\overline{IDXS}$
	NCLS	$\overline{DCPS}$ • IDXF (S1OF + S2OF)
	SC ← 03	NCLS
GENERATE B5000 INTERRUPT PULSE	FIND	NCLS • RCKS
RE-ESTABLISH E.U. WORD MARK	W0MD	WDMP (SC≠6+7) • $\overline{SCLS}$ • $\overline{SCIS}$

FIGURE 2.3-26 (1 of 4)
DISK FILE CONTROL LOGIC FLOWS

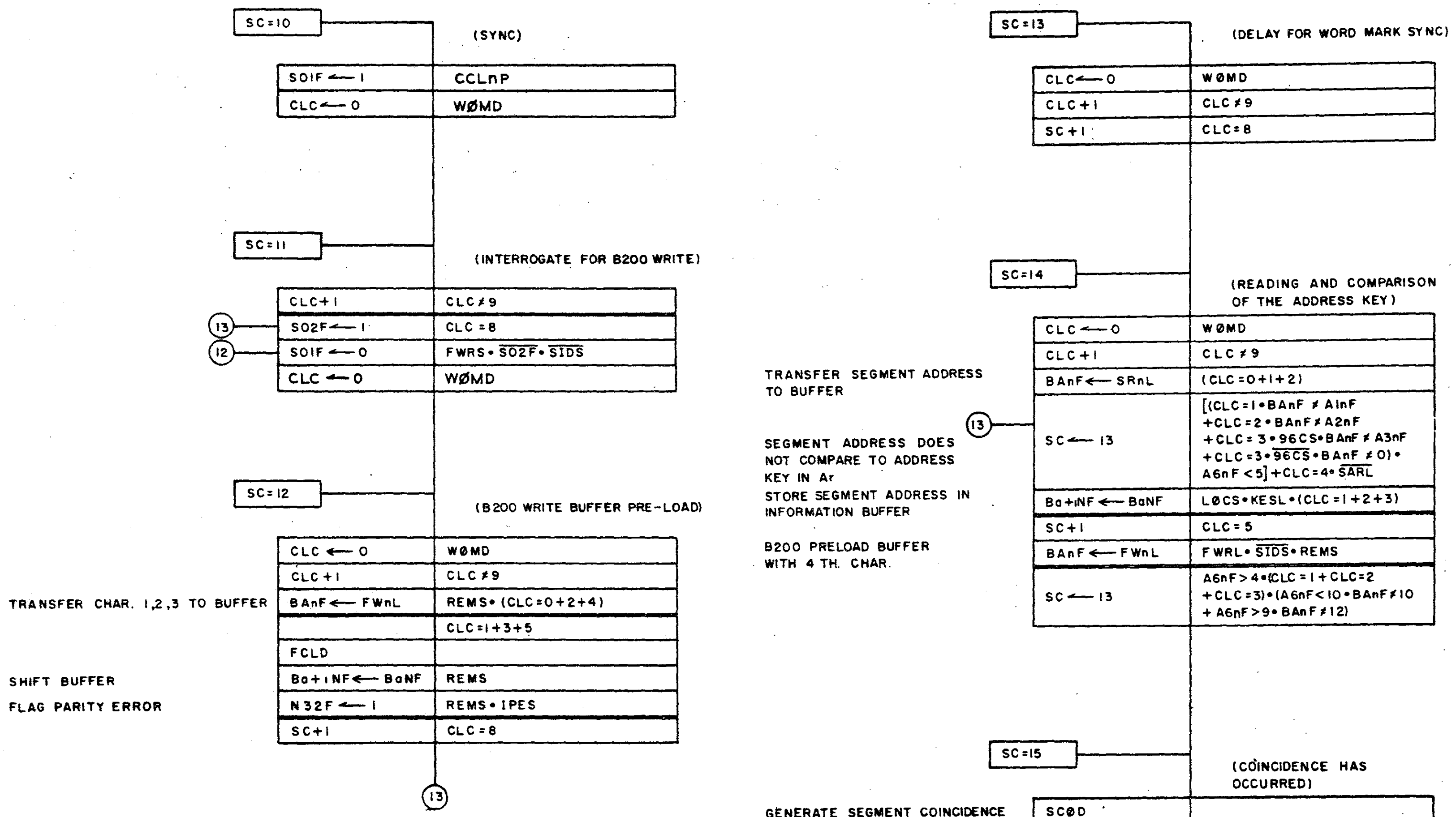
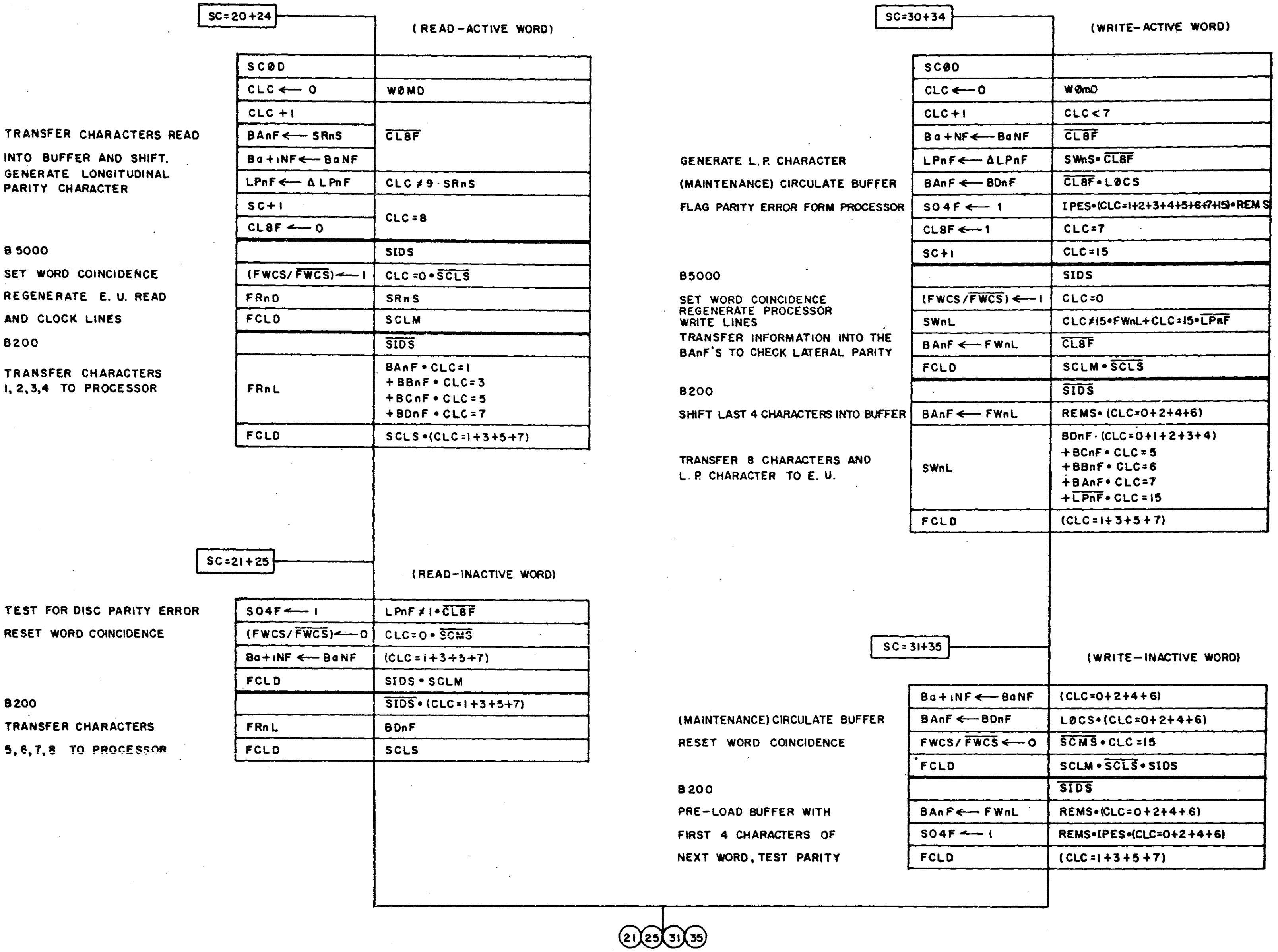


FIGURE 2.3-26 (2 of 4)



SC=20+24

(READ–ACTIVE WORD)

TRANSFER CHARACTERS READ INTO BUFFER AND SHIFT. GENERATE LONGITUDINAL PARITY CHARACTER

B 5000

SET WORD COINCIDENCE

REGENERATE E. U. READ AND CLOCK LINES

B200

TRANSFER CHARACTERS 1, 2,3,4 TO PROCESSOR

SC0D	
CLC ← 0	W0MD
CLC +1	$\overline{CL8F}$
BAnF ← SRnS	
Ba+1NF ← BaNF	
LPnF ← Δ LPnF	CLC ≠ 9 · SRnS
SC+1	CLC=8
CL8F ← 0	
	SIDS
(FWCS/$\overline{FWCS}$) ← 1	CLC=0 • $\overline{SCLS}$
FRnD	SRnS
FCLD	SCLM
	$\overline{SIDS}$
FRnL	BAnF • CLC=1 +BBnF • CLC=3 +BCnF • CLC=5 +BDnF • CLC=7
FCLD	SCLS •(CLC=1+3+5+7)

SC=21+25

(READ–INACTIVE WORD)

TEST FOR DISC PARITY ERROR

RESET WORD COINCIDENCE

B200

TRANSFER CHARACTERS 5,6,7,8 TO PROCESSOR

S04F ← 1	LPnF ≠ 1•$\overline{CL8F}$
(FWCS/$\overline{FWCS}$) ← 0	CLC=0 • $\overline{SCMS}$
Ba+1NF ← BaNF	(CLC=1+3+5+7)
FCLD	SIDS • SCLM
	$\overline{SIDS}$ • (CLC=1+3+5+7)
FRnL	BDnF
FCLD	SCLS

SC=30+34

(WRITE–ACTIVE WORD)

GENERATE L.P. CHARACTER

(MAINTENANCE) CIRCULATE BUFFER

FLAG PARITY ERROR FORM PROCESSOR

B5000

SET WORD COINCIDENCE
REGENERATE PROCESSOR WRITE LINES
TRANSFER INFORMATION INTO THE BAnF'S TO CHECK LATERAL PARITY

B200

SHIFT LAST 4 CHARACTERS INTO BUFFER

TRANSFER 8 CHARACTERS AND L. P. CHARACTER TO E. U.

SC0D	
CLC ← 0	W0mD
CLC+1	CLC<7
Ba+NF ← BaNF	$\overline{CL8F}$
LPnF ← ΔLPnF	SWnS• $\overline{CL8F}$
BAnF ← BDnF	$\overline{CL8F}$ • L0CS
S04F ← 1	IPES•(CLC=1+2+3+4+5+6+7+15)•REMS
CL8F ← 1	CLC=7
SC+1	CLC=15
	SIDS
(FWCS/$\overline{FWCS}$) ← 1	CLC=0
SWnL	CLC≠15•FWnL+CLC=15•$\overline{LPnF}$
BAnF ← FWnL	$\overline{CL8F}$
FCLD	SCLM • $\overline{SCLS}$
	$\overline{SIDS}$
BAnF ← FWnL	REMS• (CLC=0+2+4+6)
SWnL	BDnF · (CLC=0+1+2+3+4) +BCnF • CLC=5 +BBnF • CLC=6 +BAnF • CLC=7 +$\overline{LPnF}$ • CLC=15
FCLD	(CLC=1+3+5+7)

SC=31+35

(WRITE–INACTIVE WORD)

(MAINTENANCE) CIRCULATE BUFFER

RESET WORD COINCIDENCE

B200

PRE–LOAD BUFFER WITH FIRST 4 CHARACTERS OF NEXT WORD, TEST PARITY

Ba+1NF ← BaNF	(CLC=0+2+4+6)
BAnF ← BDnF	L0CS•(CLC=0+2+4+6)
FWCS/$\overline{FWCS}$ ← 0	$\overline{SCMS}$ • CLC=15
FCLD	SCLM • $\overline{SCLS}$ • SIDS
	$\overline{SIDS}$
BAnF ← FWnL	REMS•(CLC=0+2+4+6)
S04F ← 1	REMS•IPES•(CLC=0+2+4+6)
FCLD	(CLC=1+3+5+7)

FIGURE 2.3-26 (3 of 4)

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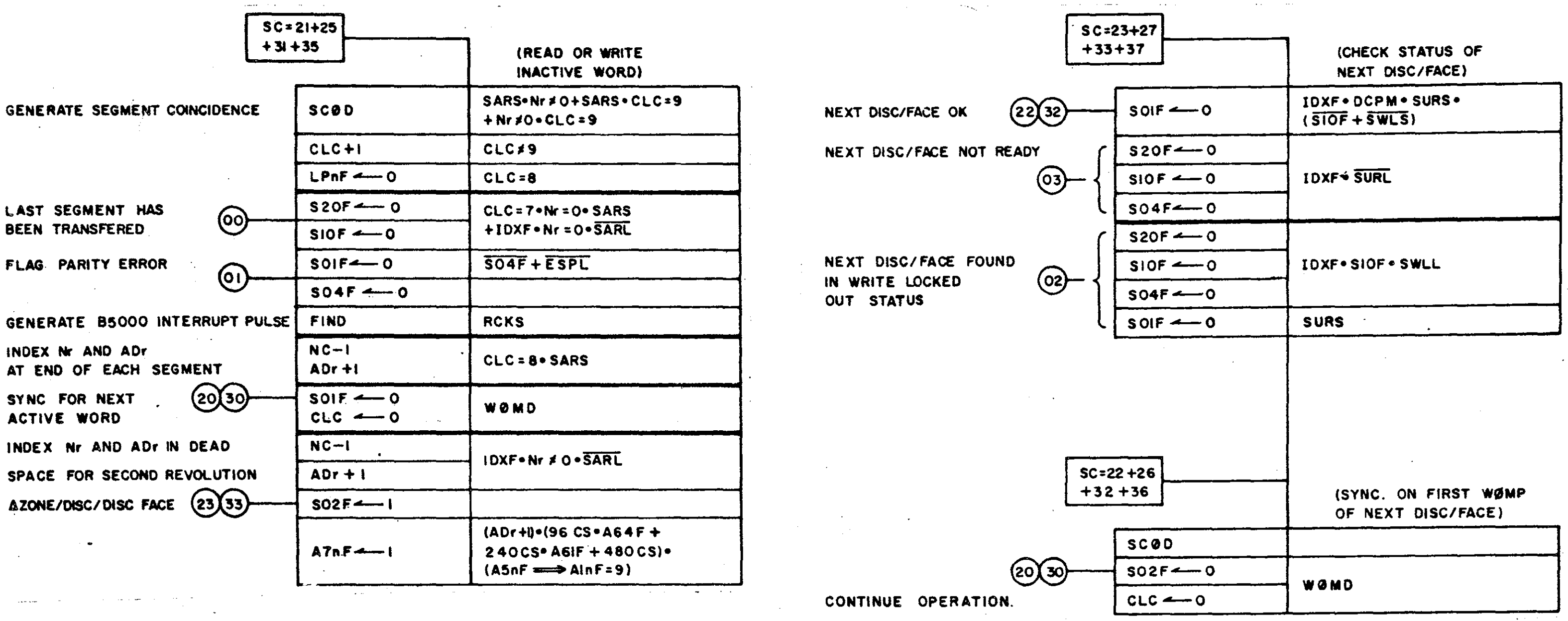


FIGURE 2.3-26 (4 of 4)

INDEX - SECTION III

3 FUNCTIONAL DESCRIPTION - ELECTRONIC

3.1 CLOCK CONTROL

The clock pulses generated and used internally in the D.F.C.U. are called CCLnP's and are produced by a B.O. and associated driver. The B.O. is not a true clock generator, however, since it is controlled and driven from the System, the E.U. or Maintenance Panel depending on the operation.

Figure 3.1-1 is a condensed drawing of the clock control. Refer to this figure throughout the following description.

SEC = 00 THROUGH 06 IN REMOTE

Gate A is true for FDTS with SEC $<$ 10 and REMOTE. It allows the System to generate CCLnP's during SEC = 00 through 06.

SEQUENCE COUNTER > 10 IN REMOTE (OR LOCAL AND SEC = 6 OR 7)

Gate B allows SCLP's from the E.U. to generate CCLnP's. This gate is controlled by SCLF, the Storage Clock FF. The second leg of the gate is SCLS/ to prevent the CCLnP from being generated until the SCLP has gone.

SCLF is controlled by Gate C which consists of SCLS, CISS (Crossover Inhibit SCLF) and SCIS/ (Storage Clock Inhibit Not). SCLS is the Storage Clock double switched. CISS is derived from SEC = 21 or 31, CLC = 9 and SARL/. Normally CISS is true, but during a second revolution crossover it is possible for a SCLP to occur during the turn on time of IDXF. A clock count of 9 occurring with SARL/ during SEC = 21 or 31 indicates the M2 address has been read and it is the last Inactive word before a second revolution crossover. These conditions being true cause CISS to go false which inhibits the set of SCLF, preventing a CCLnP from being generated by SCLP. Inhibiting this CCLnP ensures the Sequence Counter is not set to 23 or 33 before N and Address Registers have been indexed by IDXF.

SCIS/ is true for all sequence counts equal to or greater than 10 since the shunt AND term (S10F/ • S20F/) holds the input to SCIS false. When the Sequence Counter is less than 10, SCIS/ is normally false to prevent SCLP's from generating CCLnP's. Local operation during SEC = 6 or 7 is an exception. At that time, all three OR terms REMS, S02F/ and S04F/ are false. With the input false, SCIS/ becomes true.

INDEX TIME (OR NO CLOCK)

Gate D allows Index Time (IDXF) to generate a single CCLnP for each INXP when the Sequence Counter is not equal to 6 or 7. An INXP with S607S/ true triggers the Index Multi, IDXM. With SCIS/ true, IDXM sets the Index FF, IDXF, but IDXS/ goes false. When IDXM times out in 2.5 microseconds, IDXS/ goes true allowing Gate D to go true to generate a CCLnP. The same CCLnP resets IDXF.

Gate D also allows a "No Clock" condition to generate a CCLnP. The Disk Clock Present Multi, DCPM, produces a true output with a true input but, if the input goes false, it will time out after 600 microseconds to produce a false output. The input to DCPM is true for each SCLF through Gate E if the Sequence Counter is not equal to 6 or 7. If SCLF's are absent for 600 microseconds, DCPM goes false and DCPS/ goes true. The Pulse Standardizer senses a false to true change and produces a DCPP. The negative DCPP triggers IDXM if SEC ≠ 6 or 7 and 2.5 microseconds later, a CCLnP is generated. The CCLnP sets the Sequence Counter = 03.

1. Gate F allows DCPM to be used as a 600 microsecond delay during SEC = 6.
2. Triggering DCPM interrupts the clock count at CLC = 14.
3. When the multi times out, DCPS/ sets LP4F to zero which allows the Clock Counter to resume counting.
4. This delay ensures there is ample time to make a track gain selection in the E.U. prior to SC = 10.

A clock count of 15 with N ≠ 0 allows the exit from SEC = 6 to SEC = 10. Gate G is used at that time to trigger DCPM for a normal check on disk clock pulses.

MAINTENANCE START PULSE (MASP)

Gate H is used in LOCAL to allow MASP to generate a CCLnP each time the Maintenance Start switch is depressed.

CROSS-COUPLED READ SWITCH STROBING

Since the SCLP can vary in width from 540 nanoseconds to 1.2 microseconds, depending on the zone, the B5000 I/O could fail to strobe the FRnL's when the SCLP is narrower than 1.0 microsecond. To avoid this possibility, the Storage Clock Multi, SCLM, is used to expand and standardize the read pulses from the SRnS lines to 1.6 microseconds. Triggered by the leading edge of SCLS, with Clock Multi Inhibit Not true (CMIS/), SCLM holds the SRnS/ outputs latched for 1.6 microseconds. For example, if a 1's bit existed in the character coming from the E.U., SR1L would make SR1S/ false. Due to cross-coupling, SR1S would be true and fed back to Gate I where it is latched with the true from SCLM to hold the input to the SR1S/ switch true until SCLM times out. However, if an SRnL level had been false at SCLP time, SCLM cannot prevent the erroneous set of SRnS/ by noise or a change of SRnL. The Strobe Storage Read Line Multi, STSM, is used to prevent this possibility. STSM is triggered at the leading edge of SCLP and strobes the SRnL levels at the J gates. The cross-coupled switches can only be set during the 200 nanosecond time that STSM is true.

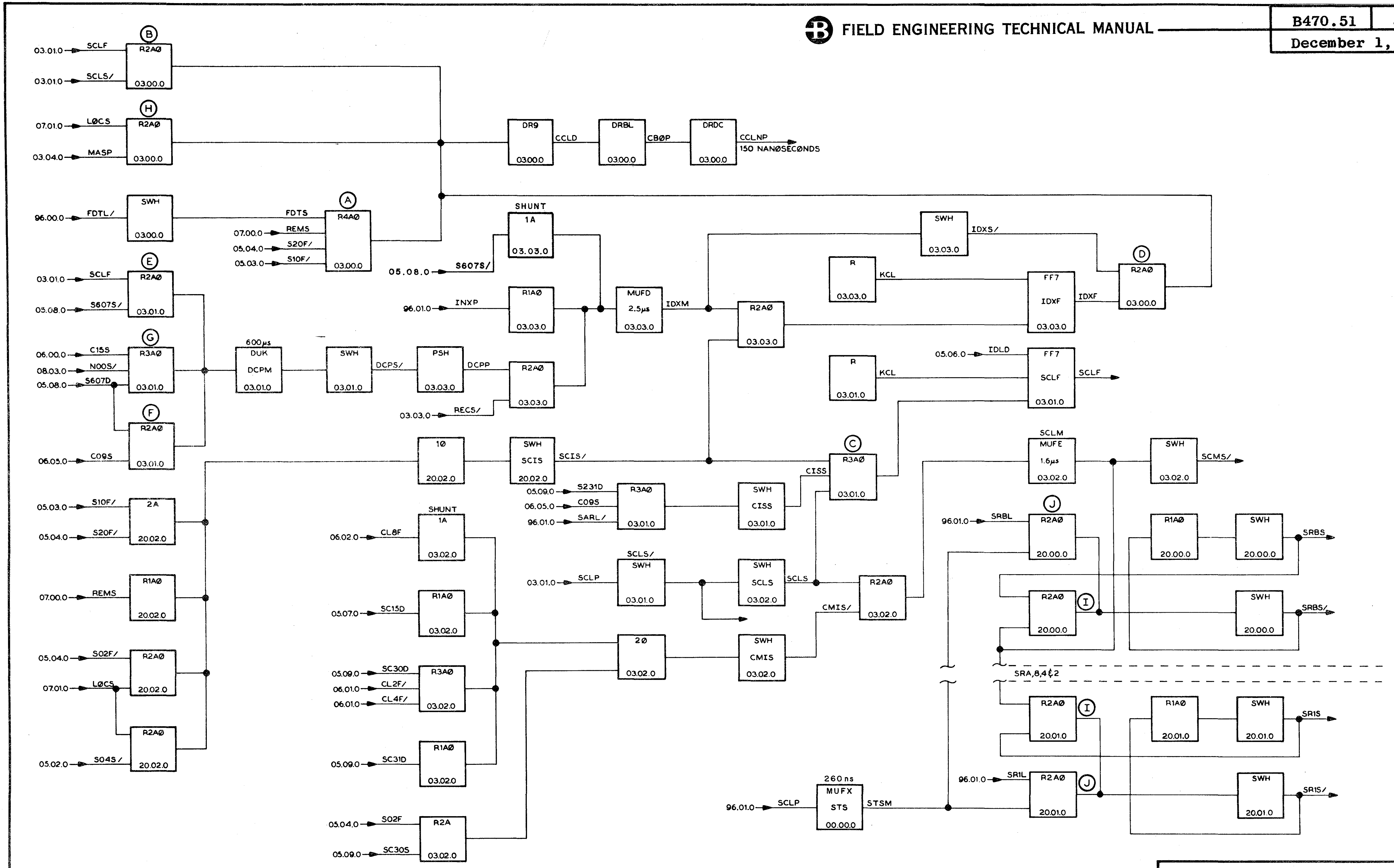


FIGURE 3.1-1
CLOCK LOGIC

3.2 CABLING

All logic and power cables internal to, leaving from, or coming to a Control Unit are shown on pin cross-reference tables. Refer to Figure 3.2-1.

LOGIC CABLES

TABLE 3.2-1

PROCESSOR 1		LEVEL	B450-1		CONTROL UNIT 1 or 3
DDJ4 (B5000) EAK-J12 (B200)			PANEL K	CKL1	ACAON2
PROCESSOR 2			B450-2		CONTROL UNIT 2 or 4
DDK8 (B5000) EAK-J12 (B200) (WINCHESTER)			PANEL N (WINCHESTER)	CNL7	ECAON2 (QUAD)
SIGNAL	GROUND	TWISTED PAIRS	SIGNAL	GROUND	PIN NO.
1	2	FASL	1	2	NO
8	4	FWRL/	8	4	SO
15	12	FW1L/	15	12	VO
22	18	FW2L/	22	18	YO
28	25	FW4L/	28	25	R1
34	31	FW8L/	34	31	U1
40	37	FWAL/	40	37	X1
46	43	FWBL/	46	43	P3
52	49	FWPL/	52	49	T3
5	10	FDTL/	5	10	PO
13	16	S1DL2/	13	16	TO
20	23	FBIL	20	23	WO
73	70	POWER ON	73	70	V4
79	76	POWER OFF	79	76	Y4
65	62	E-POWER-OFF	65	62	S4
58	55	POWER-CONT-COM	58	55	W3
26	29	FCRL/	26	29	N1
32	35	FSRL/	32	35	S1
38	41	FCBL/	38	41	V1
44	47	FWLL/	44	47	Y1
50	53	FR1L	50	53	R3
56	59	FR2L	56	59	U3
63	66	FR4L	63	66	X3
71	74	FR8L	71	74	T4
77	80	FRAL	77	80	W4
7	11	FRBL	7	11	RO
14	17	FRPL	14	17	UO
21	24	FWCL/	21	24	XO
27	30	FCLP	27	30	P1
39	42	FERL/	39	42	W1
45	48	FINP/	45	48	N3

Refer to Table 3.2-1.

DDJ4 (B5000) EAK-J12 (B200)	CKL1	Logic cable from Data Processor 1 to B450 connector Panel K (Control Unit 1 or 3).

DDK8 (B5000) EAK-J12 (B200)	CNL7	Logic cable from Data Processor 2 to B450 connector Panel N (Control Unit 2 or 4).
CKL1....ACAON2		Processor 1 logic cable from B450 connector Panel K to Control 1 or 3 logic gate.
CNL7....ECAON2		Processor 2 logic cable from B450 connector Panel N to Control 2 or 4 logic gate.

Refer to Table 3.2-2.

AABOA2	CKLO (E.U. 1) CKK1 (E.U. 2) CKKO (E.U. 3) CKJ1 (E.U. 4) CKJO (E.U. 5)	Logic cable from Electronics Unit to B450 connector Panel K.
AABOA2	CNL6 (E.U. 6) CNK7 (E.U. 7) CNK6 (E.U. 8) CNJ7 (E.U. 9) CNJ6 (E.U. 10)	Logic cable from Electronics Unit to B450 connector Panel N.
CKLO···ACBOA2		Logic cable from B450 connector Panel K to Control logic gate. Used when only one Electronics Unit in Sub-System.
CKLO .... AEBOA2 (E.U. 1) CKKL .... AECOA2 (E.U. 2) CKKO .... AECON2 (E.U. 3) CKJ1 .... AEDOA2 (E.U. 4) CKJO .... AEDON2 (E.U. 5)		Logic cables from B450 connector Panel K to Exchange 1 (E.U. 1 thru 5).
CNL6 .... EEBOA2 (E.U. 6) CNK7 .... EECOA2 (E.U. 7) CNK6 .... EECON2 (E.U. 8) CNJ7 .... EEDOA2 (E.U. 9) CNJ6 .... EEDON2 (E.U. 10)		Logic cables from B450 connector Panel N to Exchange 2 (E.U. 6 thru 10).

Refer to Table 3.2-3.

AAAOA2 .... AHJ1 EAAOA2 .... EHJ1 Refer to Table 3.2-4. AACOA2 .... AHK1 EACOA2 .... EHK1	Switch and Indicator logic cables from Control 1, 2, 3 or 4 logic gate to Display Panel.

TABLE 3.2-2

ELECTRONICS UNIT			LEVEL	B450		EXCHANGE 1 or 2	
AABOA2 E.U. 1 thru 10	WINCHESTER E.U. 1 thru 10			E.U. 1 thru 5 PANEL K E.U. 6 thru 10 PANEL N		ACBOA2 E.U. 1 ONLY AEBOA2 - E.U. 1 & 6 AECOA2 - E.U. 2 & 7 AEDOA2 - E.U. 4 & 9 AECON2 - E.U. 3 & 8 AEDON2 - E.U. 5 & 10	
PIN NO.	SIGNAL	GND PIN		SIGNAL	GND PIN	A2	N2
E4	104	111	REM-POW-ON	104	111	E4	T4
H4	115	121	REM-PWR-OFF	115	121	H4	V4
K3	82	87	EMERG-PWR-OFF	82	87	K3	X3
B4	93	100	PWR-CONT-COMM	93	100	B4	P4
C3	65	60	DFSL/	65	60	C3	R3
H3	75	71	D01L/	75	71	H3	V3
L3	84	79	D02L/	84	79	L3	Y3
C4	95	90	D04L/	95	90	C4	R4
F4	107	102	D08L/	107	102	F4	U4
K4	117	113	D16L/	117	113	K4	X4
D0	7	2	Z01L/	7	2	D0	S0
J0	16	12	Z02L/	16	12	J0	W0
B1	25	21	SW1L	25	21	B1	P1
F1	33	29	SW2L	33	29	F1	U1
L0	23	27	SW4L	23	27	L0	Y0
D1	31	35	SW8L	31	35	D1	S1
J2	57	53	SWAL	57	53	J2	W2
D3	66	62	SWBL	66	62	D3	S3
J3	76	72	SWRL/	76	72	J3	W3
A4	85	80	SC0L/	85	80	A4	N3
C0	5	1	T01L/	5	1	C0	R0
H0	15	11	T02L/	15	11	H0	V0
A1	24	20	T04L/	24	20	A1	N1
E1	32	28	T08L/	32	28	E1	T1
K1	40	36	T10L/	40	36	K1	X1
D2	48	44	T20L/	48	44	D2	S2
H2	56	52	T40L/	56	52	H2	V2
D4	97	92	INXP	97	92	D4	S4
J1	39	43	WDMP	39	43	J1	W1
L4	120	114	SWLL	120	114	L4	Y4
A0	3	8	SR1L	3	8	A0	N0
E0	13	17	SR2L	13	17	E0	T0
K0	22	26	SR4L	22	26	K0	X0
C1	30	34	SR8L	30	34	C1	R1
H1	38	42	SRAL	38	42	H1	V1
L1	46	50	SRBL	46	50	L1	Y1
E2	54	58	SCLP	54	58	E2	T2
A3	63	67	SURL/	63	67	A3	N3
E3	73	77	SARL/	73	77	E3	T3
B0	4	10	CS1L/	4	10	B0	P0
F0	14	18	CS2L/	14	18	F0	U0

TABLE 3.2-3

AAA0A2	LEVEL	AHJ1
EAA0A2		EHJ1
A0	A78F-IND	01
B0	A68F-IND	02
C0	A58F-IND	03
D0	A48F-IND	04
E0	A38F-IND	05
F0	A28F-IND	06
H0	A18F-IND	07
J0	BDBF-IND	08
K0	BDAF-IND	09
L0	BD8F-IND	10
A1	BD4F-IND	11
B1	BD2F-IND	12
C1	BD1F-IND	13
D1	A74F-IND	14
E1	A64F-IND	15
F1	A54F-IND	16
H1	A44F-IND	17
J1	A34F-IND	18
K1	A24F-IND	19
L1	A14F-IND	20
A2	BCBF-IND	21
B2	BCAF-IND	22
C2	BC8F-IND	23
D2	BC4F-IND	24
E2	BC2F-IND	25
F2	BC1F-IND	26
H2	A72F-IND	27
J2	A62F-IND	28
K2	A52F-IND	29
L2	A42F-IND	30
A3	A32F-IND	31
B3	A22F-IND	32
C3	A12F-IND	33
D3	BBBF-IND	34
E3	BBAF-IND	35
F3	BB8F-IND	36
H3	BB4F-IND	37
J3	BB2F-IND	38
K3	BB1F-IND	39

TABLE 3.2-4

AAC0A2	LEVEL	AHK1
EAC0A2		EHK1
A0	A71F-MC	01
B0	A61F-MC	02
C0	A51F-MC	03
D0	A41F-MC	04
E0	A31F-MC	05
F0	A21F-MC	06
H0	A11F-MC	07
J0	BABF-MC	08
K0	BAAF-MC	09
L0	BA8F-MC	10
A1	BA4F-MC	11
B1	BA2F-MC	12
C1	BA1F-MC	13
D1	IDXF-MC	14
E1	LPAF-MC	15
F1	LPBF-MC	16
H1	LP8F-MC	17
J1	FRPF-MC	18
K1	S01F-MC	19
L1	SCLF-MC	20
A2	LP4F-MC	21
B2	LP2F-MC	22
C2	LP1F-MC	23
D2	N01F-MC	24
E2	N08F-MC	25
F2	S10F-MC	26
H2	S20F-MC	27
J2	CL8F-MC	28
K2	CL4F-MC	29
L2	N02F-MC	30
A3	N16F-MC	31
B3	S02F-MC	32
C3	S04F-MC	33
D3	CL2F-MC	34
E3	CL1F-MC	35
F3	N04F-MC	36
H3	N32F-MC	37
J3	LWRL/	38
K3	NP1L/	39
L3	NP2L/	40

Refer to Table 3.2-5.

AABON2 .... AHL1
EABON2 .... EHL1

Refer to Table 3.2-6.

AABOA2 .... AHM1
EABOA2 .... EHM1

Switch and Indicator logic cables from Control 1, 2, 3 or 4 logic gate to Display Panel.

TABLE 3.2-5.

AABON2	LEVEL	AHL1
EABON2		EHL1
N0	A71F-IND	01
P0	A61F-IND	02
R0	A51F-IND	03
S0	A41F-IND	04
T0	A31F-IND	05
U0	A21F-IND	06
V0	A11F-IND	07
W0	BABF-IND	08
X0	BAAF-IND	09
Y0	BA8F-IND	10
N1	BA4F-IND	11
P1	BA2F-IND	12
R1	BA1F-IND	13
S1	IDXF-IND	14
T1	LPAF-IND	15
U1	LPBF-IND	16
V1	LP8F-IND	17
W1	FRPF-IND	18
X1	S01F-IND	19
Y1	SCLF-IND	20
N2	LP4F-IND	21
P2	LP2F-IND	22
R2	LP1F-IND	23
S2	N01F-IND	24
T2	N08F-IND	25
U2	S10F-IND	26
V2	S20F-IND	27
W2	CL8F-IND	28
X2	CL4F-IND	29
Y2	N02F-IND	30
N3	N16F-IND	31
P3	S02F-IND	32
R3	S04F-IND	33
S3	CL2F-IND	34
T3	CL1F-IND	35
U3	N04F-IND	36
V3	N32F-IND	37

TABLE 3.2-6.

AABOA2	LEVEL	AHM1
EABOA2		EHM1
A0	A78F-MC	01
B0	A68F-MC	02
C0	A58F-MC	03
D0	A48F-MC	04
E0	A38F-MC	05
F0	A28F-MC	06
H0	A18F-MC	07
J0	BDBF-MC	08
K0	BDAF-MC	09
L0	BD8F-MC	10
A1	BD4F-MC	11
B1	BD2F-MC	12
C1	BD1F-MC	13
D1	A74F-MC	14
E1	A64F-MC	15
F1	A54F-MC	16
H1	A44F-MC	17
J1	A34F-MC	18
K1	A24F-MC	19
L1	A14F-MC	20
A2	BCBF-MC	21
B2	BCAF-MC	22
C2	BC8F-MC	23
D2	BC4F-MC	24
E2	BC2F-MC	25
F2	BC1F-MC	26
H2	A72F-MC	27
J2	A62F-MC	28
K2	A52F-MC	29
L2	A42F-MC	30
A3	A32F-MC	31
B3	A22F-MC	32
C3	A12F-MC	33
D3	BBBF-MC	34
E3	BBAF-MC	35
F3	BB8F-MC	36
H3	BB4F-MC	37
J3	BB2F-MC	38
K3	BB1F-MC	39

Refer to Table 3.2-7.

ACBON2 .... AEAOA7	Logic cable from Exchange 1 to Control 1 or 3 logic gate.
ECBON2 .... EEAON7	Logic cable from Exchange 2 to Control 2 or 4 logic gate.

TABLE 3.2-7.

C.U. 13 or 14	LEVEL	EXCHANGE	
ACBON2		C.U. 13 AEAOA7	C.U. 14 EEAON7
R0	T01D	C5	R5
S0	Z01D	D5	S5
V0	T02D	H5	V5
W0	Z02D	J5	W5
Y0	SW4S	L5	Y5
N1	T04S	A6	N6
P1	SW1S	B6	P6
S1	SW8S	D6	S6
T1	T08D	E6	T6
U1	SW2S	F6	U6
X1	T10D	K6	X6
S2	T20D	D7	S7
V2	T40D	H7	V7
W2	SWAS	J7	W7
P3	A71F	B8	P8
R3	DFSD	C8	R8
S3	SWBS	D8	S8
U3	A72F	F8	U8
V3	D01D	H8	V8
W3	SWRS	J8	W8
X3	A74F	K8	X8
Y3	D02D	L8	Y8
N4	SC0D	A9	N9
P4	A78F	B9	P9
R4	D04D	C9	R9
U4	D08D	F9	U9
V4	0TRD/	H9	V9
X4	D16D	K9	X9
N0	SR1L	A5	N5
P0	CS1L/	B5	P5
T0	SR2L	E5	T5
U0	CS2L/	F5	U5
X0	SR4L	K5	X5
R1	SR8L	C6	R6
V1	SRAL	H6	V6
W1	WDMP	J6	W6
Y1	SRBL	L6	Y6
T2	SCLP	E7	T7
N3	SURL/	A8	N8
T3	SARL/	E8	T8
S4	INXP	D9	S9
W4	DACL	J9	W9
Y4	SWLL	L9	Y9

Refer to Table 3.2-8.

AEA0A2 .... EEC0A7 (X1 - X3)
AEA0N2 .... EEC0N7 (X2 - X4)
AEC0A7 .... EEA0A2 (X3 - X1)
AEC0N7 .... EEA0N2 (X4 - X2)

Exchange 1 and 2 Cross-Over logic cables.

TABLE 3.2-8.

EXCHANGE 1 or 2		LEVEL	EXCHANGE 1 or 2	
X1	X2		X3	X4
AEA0A2	EEA0N2		AEC0A7	EEC0N7
C0	R0	T01L	C5	R5
D0	S0	Z01L	D5	S5
H0	V0	T02L	H5	V5
J0	W0	Z02L	J5	W5
L0	Y0	SW4L	L5	Y5
A1	N1	T04L	A6	N6
B1	P1	SW1L	B6	P6
D1	S1	SW8L	D6	S6
E1	T1	T08L	E6	T6
F1	U1	SW2L	F6	U6
K1	X1	T10L	K6	X6
D2	S2	T20L	D7	S7
H2	V2	T40L	H7	V7
J2	W2	SWAL	J7	W7
B3	P3	A71F	B8	P8
C3	R3	DFSL	C8	R8
D3	S3	SWBL	D8	S8
F3	U3	A72F	F8	U8
H3	V3	D01L	H8	V8
J3	W3	SWRL	J8	W8
K3	X3	A74F	K8	X8
L3	Y3	D02L	L8	Y8
A4	N4	SC0L	A9	N9
B4	P4	A78F	B9	P9
C4	R4	D04L	C9	R9
F4	U4	D08L	F9	U9
H4	V4	0TRL/	H9	V9
K4	X4	D16L	K9	X9
A0	N0	SR1L	A5	N5
B0	P0	CS1L	B5	P5
E0	T0	SR2L	E5	T5
F0	U0	CS2L	F5	U5
K0	X0	SR4L	K5	X5
C1	R1	SR8L	C6	R6
H1	V1	SRAL	H6	V6
J1	W1	WDMP	J6	W6
L1	Y1	SRBL	L6	Y6
E2	T2	SCLP	E7	U7
A3	N3	SURL	A8	N8
E3	T3	SARL	E8	T8
D4	S4	INXP	D9	S9
J4	W4	DACL	J9	W9
L4	Y4	SWLL	L9	Y9

POWER CABLES

Refer to Table 3.2-9.

AABON7
EABON7 - B450 Power Distribution DC cable for Panels A and B.

Refer to Table 3.2-10.

AABOA7
EABOA7 - B450 Power Distribution DC cable for Panels C and D.

TABLE 3.2-9.

AABON7 (C.U. 1 or 3) EABON7 (C.U. 2 or 4)	VOLTAGE	BDL6 (B450-1) BDL1 (B450-2)
N9	+20V AABA-L	6
P9	+20V AABA-Y	
R9	+20V AABB-L	
S9	+20V AABB-Y	
V9	+20V AABC-L	
W9	+20V AABC-Y	
X9	+20V AABD-L	
Y9	+20V AABD-Y	
N8	-4.5V AABA-L	9
P8	-4.5V AABA-Y	
R8	-4.5V AABB-L	
S8	-4.5V AABB-Y	
V8	-4.5V AABC-L	
W8	-4.5V AABC-Y	
X8	-4.5V AABD-L	
Y8	-4.5V AABD-Y	
N6	-12V AABA-L	12
P6	-12V AABA-Y	
R6	-12V AABB-L	
S6	-12V AABB-Y	
V6	-12V AABC-L	
W6	-12V AABC-Y	
X6	-12V AABD-L	
Y6	-12V AABD-Y	

TABLE 3.2-10.

AABOA7 (C.U. 1 or 3) EABOA7 (C.U. 2 or 4)	VOLTAGE	BDL6 (B450-1) BDL1 (B450-2)
A5	EMERG-OFF	15
A7	PC-COM	1
A9	+20V ACDA-L	6
B9	+20V ACDA-Y	
C9	+20V ACDB-L	
D9	+20V ACDB-Y	
A8	-4.5V ACDA-L	9
B8	-4.5V ACDA-Y	
C8	-4.5V ACDB-L	
D8	-4.5V ACDB-Y	
A6	-12V ACDA-L	12
B6	-12V ACDA-Y	
C6	-12V ACDB-L	
D6	-12V ACDB-Y	

Refer to Table 3.2-11.

AEBON7
EEBON7 B450 Power Distribution DC cable for Panels E and F.

Refer to Table 3.2-12.

AEBOA7 .. B450 Power Distribution Power Control cable to Exchange 1.

EEBOA7 .. B450 Power Distribution Power Control cable to Exchange 2.

TABLE 3.2-11.

EXCHANGE	VOLTAGE	B450
AEBON7-1 EEBON7-2		BDL6-1 BDL1-2
N9	+20V AEFA-L	10
P9	+20V AEFA-Y	
R9	+20V AEFB-L	
S9	+20V AEFB-Y	
V9	+20V AEFC-L	
W9	+20V AEFC-Y	
X9	+20V AEFD-L	
Y9	+20V AEFD-Y	
N8	-4.5V AEFA-L	13
P8	-4.5V AEFA-Y	
R8	-4.5V AEFB-L	
S8	-4.5V AEFB-Y	
V8	-4.5V AEFC-L	
W8	-4.5V AEFC-Y	
X8	-4.5V AEFD-L	
Y8	-4.5V AEFD-Y	
N6	-12V AEFA-L	16
P6	-12V AEFA-Y	
R6	-12V AEFB-L	
S6	-12V AEFB-Y	
V6	-12V AEFC-L	
W6	-12V AEFC-Y	
X6	-12V AEFD-L	
Y6	-12V AEFD-Y	

TABLE 3.2-12.

EXCHANGE	LEVEL	B450
AEBOA7-1 EEBON7-2		BDL6-1 BDL1-2
A5	EMER-OFF-E1,6	18
B5	EMER-OFF-E2,7	
C5	EMER-OFF-E3,8	
D5	EMER-OFF-E4,9	
E5	EMER-OFF-E5,10	
A6	POWER-ON-E1,6	7
B6	POWER-ON-E2,7	
C6	POWER-ON-E3,8	
D6	POWER-ON-E4,9	
E6	POWER-ON-E5,10	
A8	POWER-OFF-E1,6	4
B8	POWER-OFF-E2,7	
C8	POWER-OFF-E3,8	
D8	POWER-OFF-E4,9	
E8	POWER-OFF-E5,10	
A9	PC-COM-E1,6	1
B9	PC-COM-E2,7	
C9	PC-COM-E3,8	
D9	PC-COM-E4,9	
E9	PC-COM-E5,10	

Refer to Table 3.2-13.

AHN1 ... BBJ1-A2	Power cable to Control 1 or 3 Display Panel from B450 power quad.
EHN1 ... BBJ1-N2	Power cable to Control 2 or 4 Display Panel from B450 power quad.

TABLE 3.2-13.

CONTROL UNIT 1 or 3			CONTROL UNIT 2 or 4		
DISPLAY PANEL	VOLTAGE	B450	DISPLAY PANEL	VOLTAGE	B450
AHN1		BBJ1A2	EHN1		BBJ1N2
1	COMMON-1	HO	1	COMMON-2	NO
2		BO	2		PO
3		CO	3		RO
4		DO	4		SO
5		EO	5		TO
6		FO	6		UO
7	-24VDC-1	HO	7	-24VDC-2	VO
8		JO	8		WO
9		KO	9		XO
10		LO	10		YO
11		A1	11		N1
12		B1	12		P1
14	-120VDC-1	D1	14	-120VDC-2	S1
18	-12VDC-1	J1	18	-12VDC-2	W1
20	-100VDC-1	L1	20	-100VDC-2	Y1
22	+20VDC-1	B2	22	+20VDC-2	P2
24	+100VDC-1	D2	24	+100VDC-2	S2
27	MASTER CLEAR-1	H2	27	MASTER CLEAR-2	V2
29	SEQ. COMPLETE-1	K2	29	SEQ. COMPLETE-2	X2
30	-4.5VDC-1	L2	30	-4.5VDC-2	Y2
33	C1-ON-P	C3	33	C2-ON-P	R3
35	C1-OFF-P	E3	35	C2-OFF-P	T3
50	P1-E-OFF	L3	50	P2-E-OFF	Y4

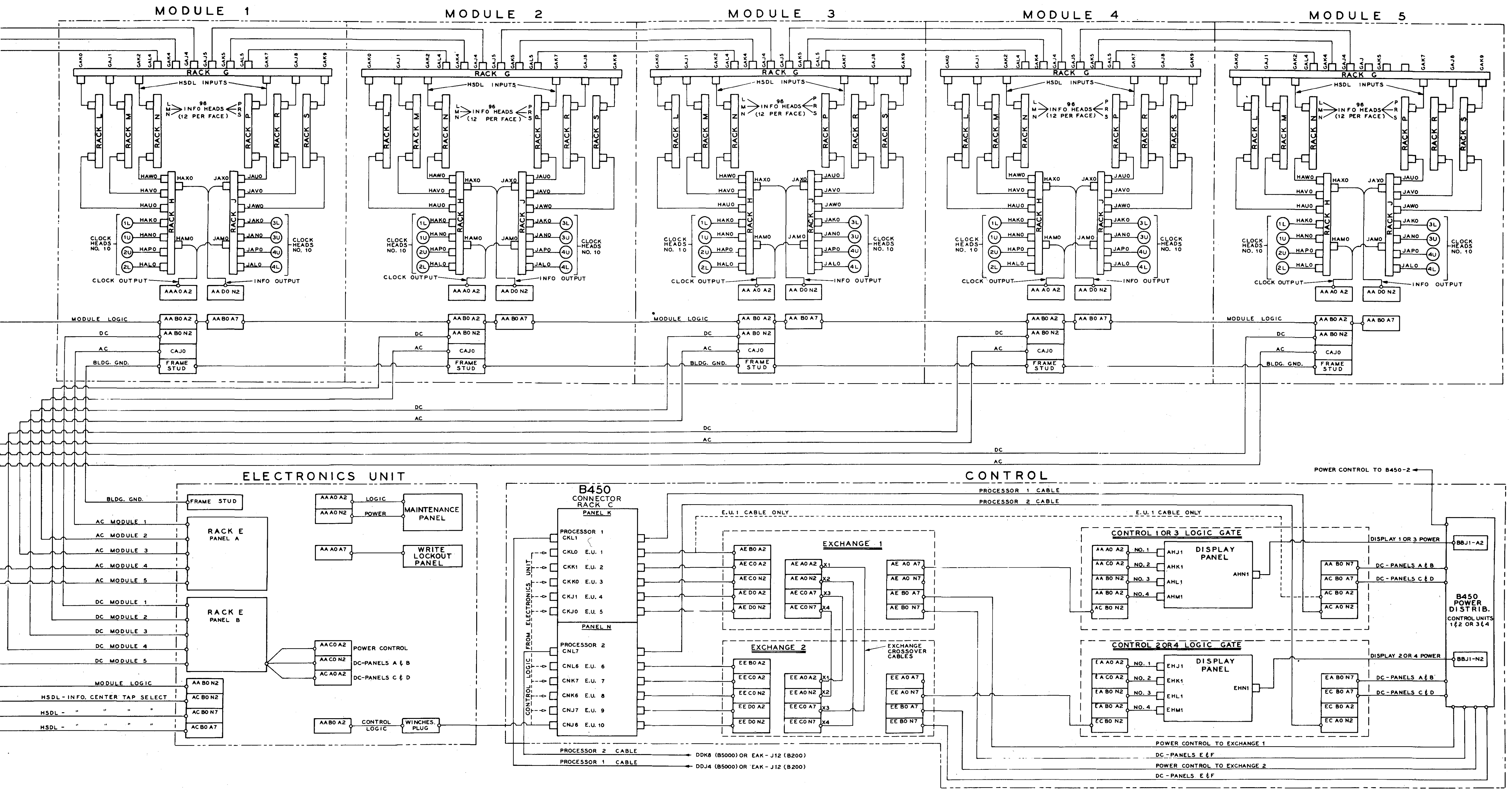


FIGURE 3.2-1
SUBSYSTEM CABLING DIAGRAM

3.3 READY CIRCUITS

The level FCRL/ that is sent to the System to indicate the READY status of the Disk File Control Unit is developed by the following circuitry:

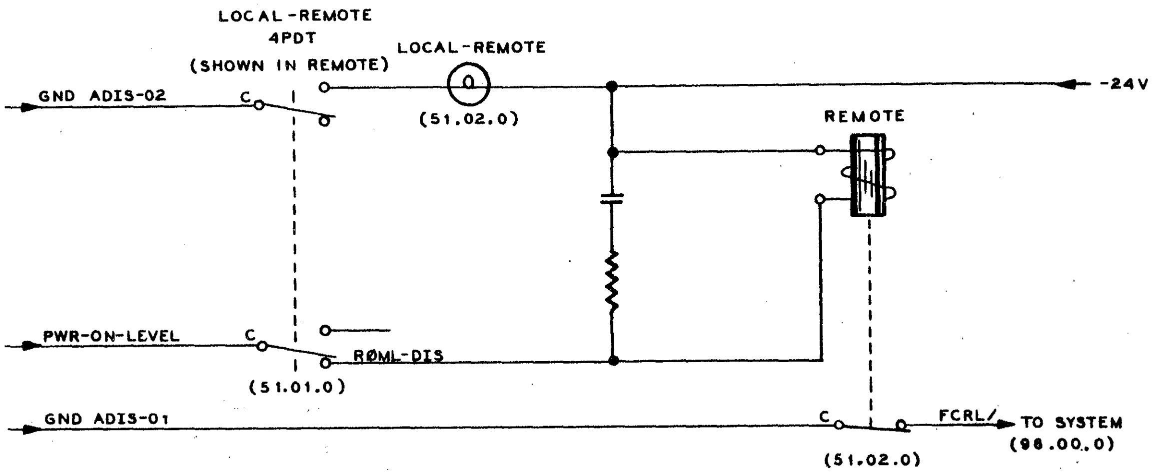


FIGURE 3.3-1
DISK FILE CONTROL READY CIRCUIT

With power up and the LOCAL/REMOTE switch in the LOCAL position, the LOCAL/REMOTE light on the Maintenance Panel will be lit.

With power on and the LOCAL/REMOTE switch in the REMOTE position, the LOCAL/REMOTE light will be out, the Remote relay will be picked and the level FCRL/ will be false to the external control.

NOTE

> A power-off sequence of the D.F.C.U. can not be initiated from the Maintenance Panel with the LOCAL/REMOTE switch in REMOTE.

3.4 INFORMATION FLOW PATHS

INPUT PARITY ERROR CHECKING

Information from the System to the D.F.C.U. is checked for correct parity. The Parity Checking Matrix decides if the number of bits in each character is even or odd. The System sends a level called File Binary Information Level (FBIL) to the D.F.C.U. to indicate whether the number of bits should be even or odd. If FBIL is true, the total number of bits in each character should be odd. If FBIL is false, the number of bits should be even.

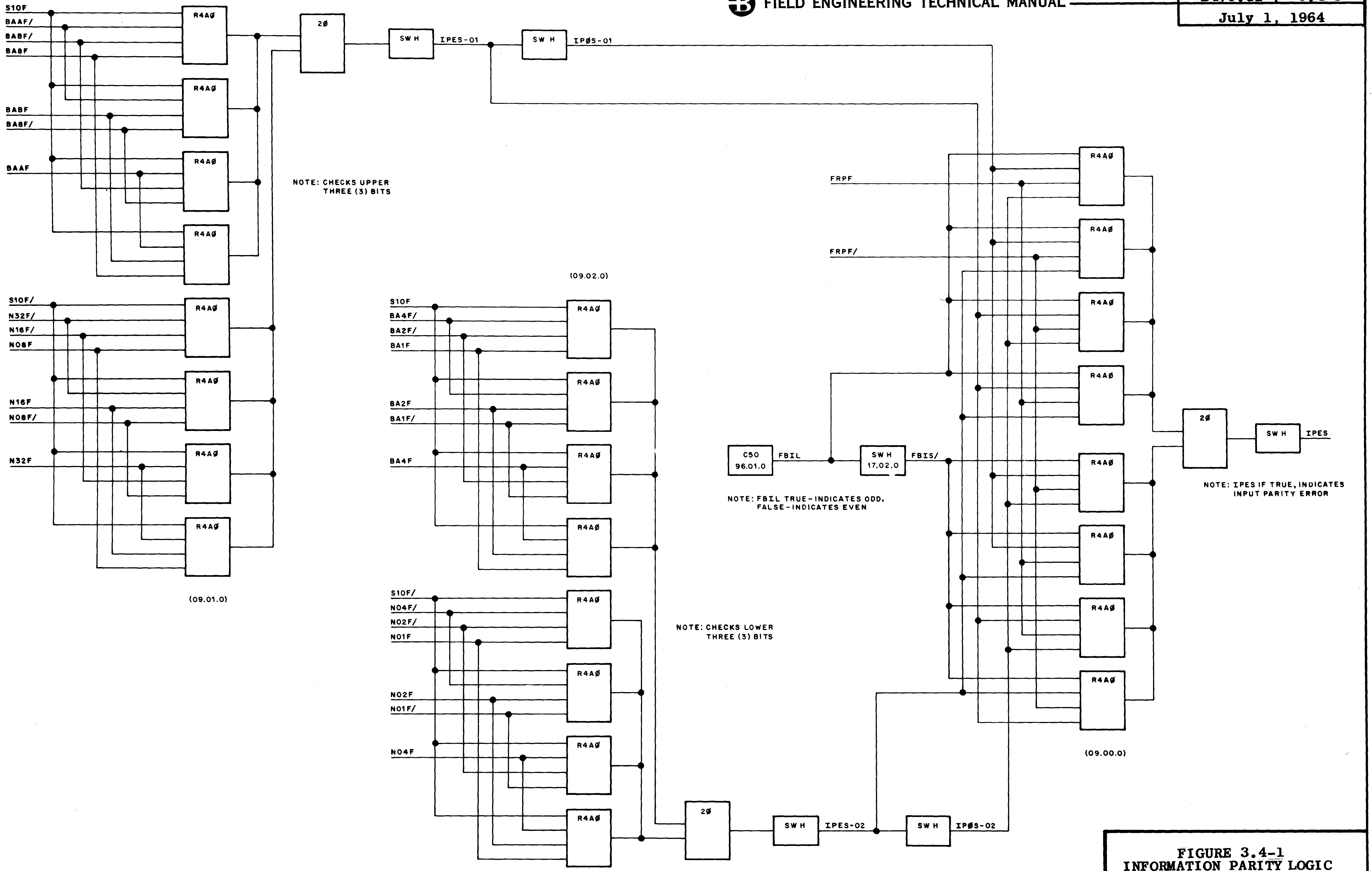
Characters coming into the D.F.C.U. from the System are shifted into either the NnnF's or the BAnF's; both are able to contain six bits. The characters are sent in seven bit form from the System, so an additional flip-flop called File Write Parity Flip-Flop (FRPF) is used to contain the parity bit that is sent with each character. The status of FRPF is gated with the six-bit character held in the NnnF's or BAnF's to check for correct parity. See Figure 3.4-1.

OUTPUT PARITY GENERATION

Information characters are transferred from the D.F.C.U. on the File Read Lines (FRnL). The characters are in six-bit form from the disk and the D.F.C.U. adds the parity level to the six bits to make the number of bits in each character even or odd as required. FBIL from the System indicates if the number of bits should be even or odd. FBIL true indicates odd; FBIL false indicates even. See Figure 3.4-2.

STORAGE READ LEVELS

In a Read operation, the E.U. reads characters from the disk and sends an SCLP to the D.F.C.U. to indicate that a character is ready to be transferred on the Storage Read Lines (SRnL's). The SCLP will fire a 200 nanosecond multi, STSM, which strobes the SRnL's into the Storage Read Switches (SRnS's). The SRnS's are latched by SCLM for 1.6 microseconds. See Figure 3.4-3.



NOTE: CHECKS UPPER THREE (3) BITS

NOTE: CHECKS LOWER THREE (3) BITS

NOTE: FBIL TRUE-INDICATES ODD, FALSE-INDICATES EVEN

NOTE: IPES IF TRUE, INDICATES INPUT PARITY ERROR

FIGURE 3.4-1
INFORMATION PARITY LOGIC

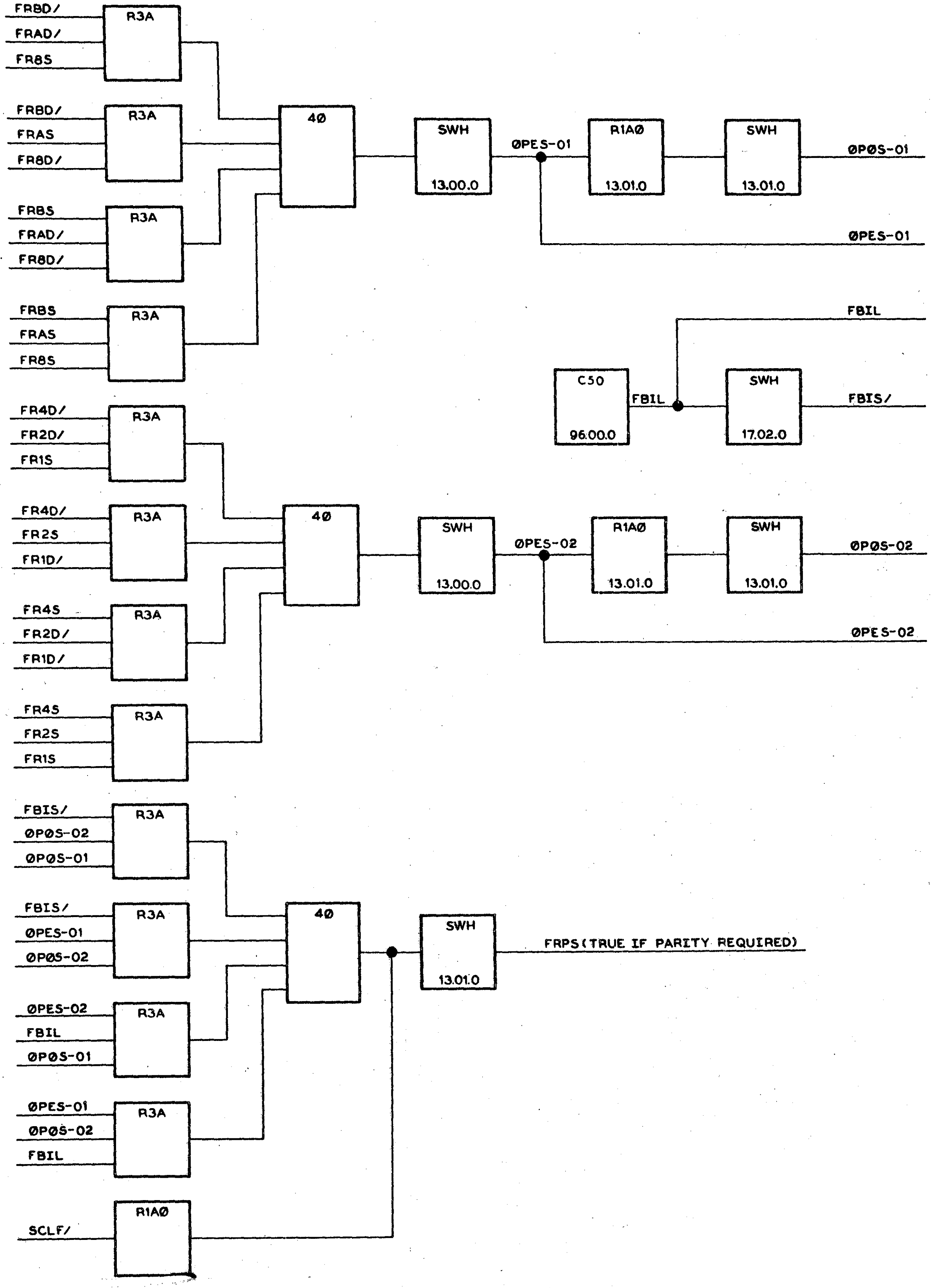


FIGURE 3.4-2
OUTPUT PARITY GENERATION

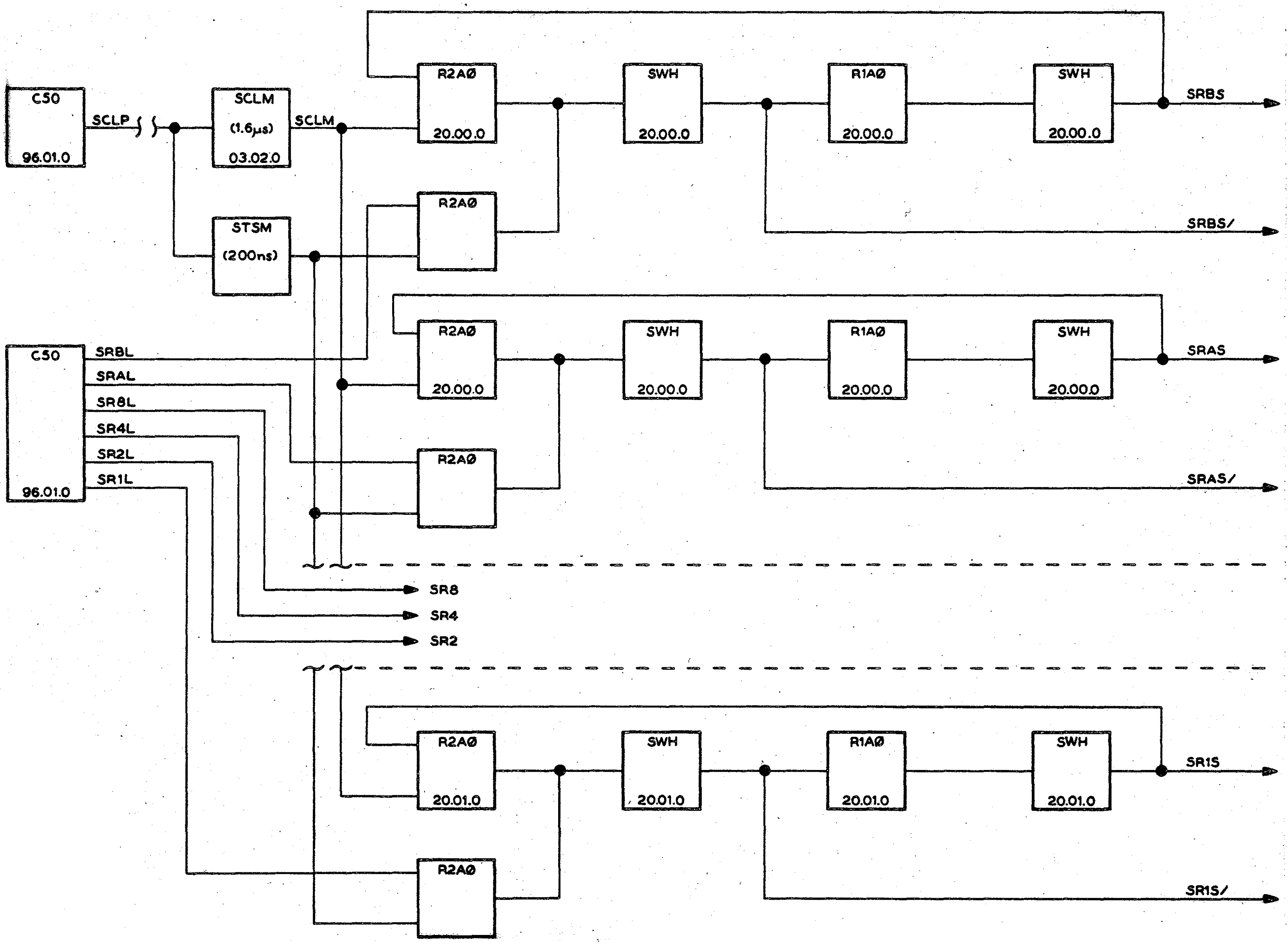


FIGURE 3.4-3
STORAGE READ SWITCHES

3.5 ADDRESSING

GENERAL DESCRIPTION

The 480, 240 and 96 options are the three character per segment options available in the Disk File Sub-System. The number of characters per segment determines segment length, number of segments per disk face, segment address range, and "A" Register decoding.

For any option, a "disk set" is the disk or disks required for two complete sequences of segment addresses and one complete track sequence. The track sequence is 00 thru 99 for all options.

In the 480 option, there are fifty segments per disk face, and the range of segment addresses is 00 thru 99. Thus a "disk set" is two disks. Segments 00 thru 49 are on the "lower" face of disk one, and 50 thru 99 are on the "upper" face of the same disk. Another complete sequence of addresses on disk two for tracks 50 thru 99 make up the set.

In the 240 option, a "disk set" is made up of one disk with addresses 00 thru 99 on both faces. Tracks 00 thru 49 are on the "lower" face and 50 thru 99 on the "upper" face.

In the 96 option, four disks make up a set with segment addresses 000 thru 249 on the "lower" face of disk one; 250 thru 499 on the "upper" face of disk one; 500 thru 749 on the "lower" face of disk two and 750 thru 999 on the "upper" face of disk two. Another complete sequence of segment addresses on disks three and four make up the set.

In addition to the information segments, each Zone has two Maintenance segments located after the high order segment in the zone and before the dead space. These segments are M1, which can be read or written; and M2, which can be read only. Regardless of the Storage Unit option, the Maintenance segments will always be 96 characters.

In time with word twelve of M2, there is a fictitious address called M3. This address does not represent a Maintenance segment, but is extra insurance for the termination of an MS1 Write operation and gives symmetry to the addressing scheme.

Maintenance segment addresses differ from Information addresses in that they are forbidden combinations.

1. M1 address is four binary tens.
2. M2 address is six binary twelves.
3. M3 address is three binary thirteens.

For detailed description of Information and Address layout, refer to the B475.51 Technical Manual, Section 3.6.

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File Address Word

The File Address Word sent from the System to D.F.C.U. consists of eight digits. The first seven digits represent the starting segment address and the eighth is the number of segments to be read from the file.

File Address transfer from System to D.F.C.U. is paralled by bit. Address digits on the File Write Lines (FWnL) are shifted through the "N" Register into the "A" Register.

When the complete File Address Word has shifted into the "A" Register, it is decoded and the output trunk level (0TRD/) seeks the designated E.U. The decoded output levels of the "A" Register select the disk face, track and zone. The Addresses are then read from the selected zone's address track. They are transferred, parallel by bit, on the Storage Read Lines (SRnL) to the Read Cross-Coupled Switches (SRnS) in the D.F.C.U. They are then shifted into the BAnFs. The BAnFs are compared to the segment address in the "A" Register.

The decoded File Address Word will indicate whether an Information or Maintenance segment is being addressed. If the desired address is that of an Information segment and the character option is the 480 or 240, the first digit shifted into BAnF is compared to A1nF. If they are equal, the second character in BAnF is compared to A2nF. If they are equal, the third character in BAnF is compared to zero.

If the desired address is that of an Information segment and the character option used is the 96, the first and second digits are compared as before, but the third character is compared to A3nF.

If the desired address is that of a Maintenance segment, the first three address digits shifted into BAnF are compared to ten for M1 and twelve for M2.

In all cases when comparison exists, the File operation begins. The first address digit that does not compare causes the address to be disregarded and the reading of the address track will continue.

File Address Decoding

File Address decoded outputs accomplish the following:

1. Select the E.U.
2. Select the disk.
3. Select the disk face.
4. Select the track.
5. Select the zone.
6. Determine whether an Information or Maintenance segment is being addressed and set up the comparison logic accordingly.

Decoded outputs are as follows:

A71F A72F A74F A78F	Electronic Unit Select Levels
D01L/ D02L/ D04L/ D08L/ D16L/	Disk Select Levels
DFSL/	Disk Face Select Level
T01L/ T02L/ T04L/ T08L/ T10L/ T20L/ T40L/	Track Select Levels
Z01L/ Z02L/	Zone Select Levels

Character Option Select Levels

The characters per segment levels, CS1L/ and CS2L/, from the E.U. determine the manner in which the File Address Word is decoded.

Figure 3.5-1 is a simple block diagram showing how these levels are decoded in Control.

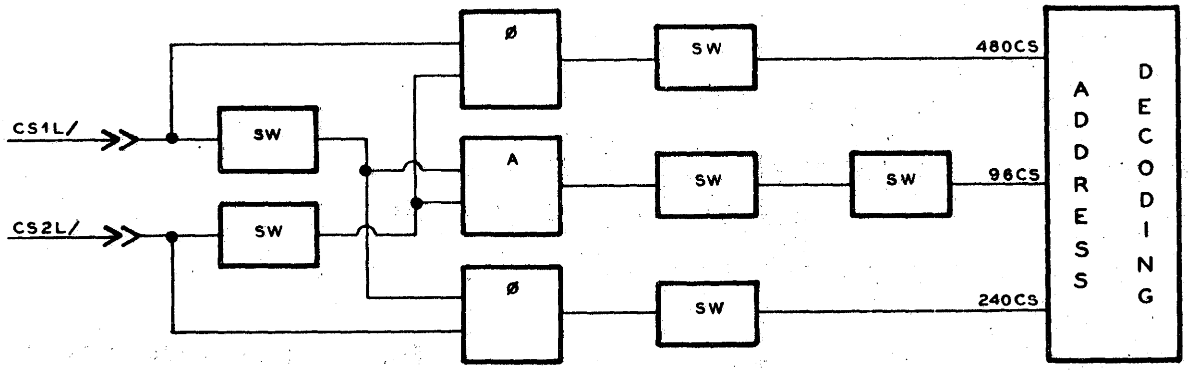


FIGURE 3.5-1
OPTION SELECT

File Address Decoding for 480 Option

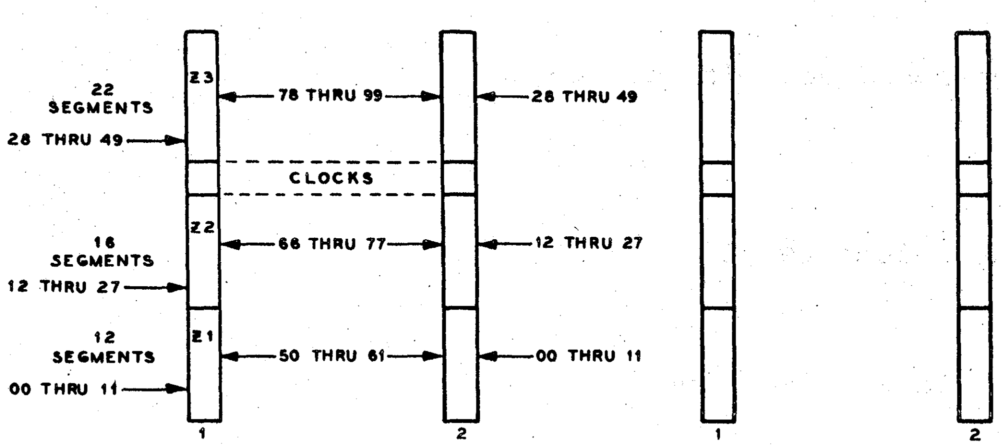
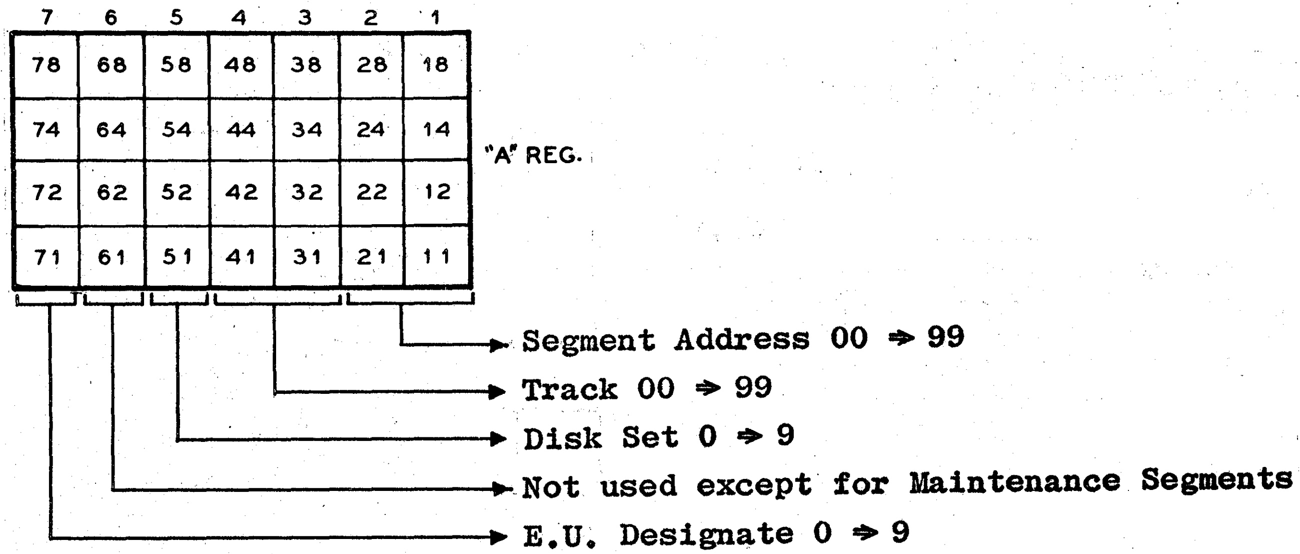


FIGURE 3.5-2
DISK SET-480 OPTION

A disk set in this option consists of two disks holding two complete ranges of segment addresses with one complete track range.

1. Segment 00 ➾ 49 on disk 1 and 2 "lower" face.
2. Segment 50 ➾ 99 on disk 1 and 2 "upper" face.
3. Track 00 ➾ 49 on disk 1.
4. Track 50 ➾ 99 on disk 2.

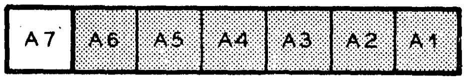


7	6	5	4	3	2	1
78	68	58	48	38	28	18
74	64	54	44	34	24	14
72	62	52	42	32	22	12
71	61	51	41	31	21	11

FIGURE 3.5-3
"A" REGISTER DECODING-480 OPTION

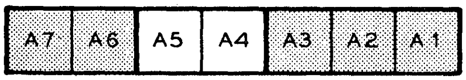
The following is a description of how each decoded output is generated. The "A" Register is represented by decade.

E.U. Designation



A binary configuration of zero selects E.U. 1; one selects E.U.2; nine selects E.U. 10.

Disk Selection



The disk is selected by the fourth and fifth decades. A5 selects the disk set, A4 selects the disk.

D01L
480 CS • (+ A44F • A41F
+ A44F • A42F
+ A48F) → Track equals 50 ⇒ 99

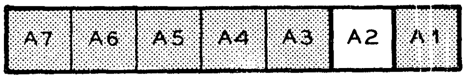
D02L
480 CS • A51F → Disk set 1, 3, 5, 7 or 9

D04L
480 CS • A52F → Disk set 2, 3, 6 or 7

D08L
480 CS • A54F → Disk set 4, 5, 6 or 7

D16L
480 CS • A58F → Disk set 8 or 9

Disk Face Selection

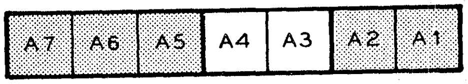


The Disk Face is selected by the second decade.

DFSL/
480 CS • (+ A24F • A21F
+ A24F • A22F
+ A28F) → Segment address equals 50 ⇒ 99

Segment address equals 00 ⇒ 49 for "lower" face, 50 ⇒ 99 for "upper" face.

Track Selection



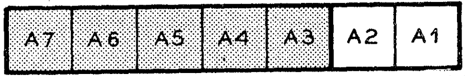
The track is selected by the third and fourth decades. Although these decades may be 00 ⇒ 99, the Track Select outputs (TnnL) will never exceed 49.

A3 & A4	TnnL
00 OR 50	00
01 OR 51	01
02 THRU 47 OR 52 THRU 97	02 THRU 47
48 OR 98	48
49 OR 99	49

```
T01L
    96 CS/ • A31F]─────────────────────► Track one level
T02L
    96 CS/ • A32F]─────────────────────► Track two level
T04L
    96 CS/ • A34F]─────────────────────► Track four level
T08L
    96 CS/ • A38F]─────────────────────► Track eight level
T10L                                           TRACK
    96 CS/ • (+ A48F/ • A44F/ • A41F ]       [10 ⇛ 19
              + A44F  • A42F  • A41F/ ]├    ┤30 ⇛ 39
              + A48F  • A44F/ • A41F/)]      |60 ⇛ 69
                                             [80 ⇛ 89
                                               TRACK
T20L
    96 CS/ • (+ A42F  • A41F           ]     [20 ⇛ 29
              + A44F/ • A42F           ]├   ┤30 ⇛ 39
              + A48F  • A44F/ • A41F/) ]     |70 ⇛ 79
                                             [80 ⇛ 89

T40L                                           TRACK
    96 CS/ • (+ A44F • A42F/ • A41F/ ]├     ┤[40 ⇛ 49
              + A48F • A41F)         ]       [90 ⇛ 99
```

Zone Selection

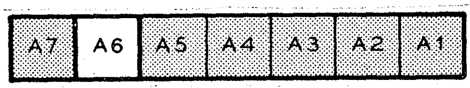


The zone is selected by the first and second decades.

1. (LT) indicates segment address Less Than
2. (GE) indicates segment address Greater Than or Equal To

```
Z01L
   (+ 480 CS • LT050S • LT012S]──────────► Zone 1, "lower" face
    + 480 CS • LT050S • GE028S]──────────► Zone 3, "lower" face
    + 480 CS • GE050S • LT062S]──────────► Zone 1, "upper" face
    + 480 CS • GE050S • GE078S)]─────────► Zone 3, "upper" face
Z02L
   (+ 480 CS • LT050S • GE012S]──────────► Zone 2 or 3, "lower" face
    + 480 CS • GE050S • GE062S)]─────────► Zone 2 or 3, "upper" face
```

Information/Maintenance
Segment Indicator



The type of segment addressed is indicated by the sixth decade.

1. A6 0 ⇛ 4 for Information segment.
2. A6 5 ⇛ 9 for Maintenance segment one.
3. A6 10 ⇛ 14 for Maintenance segment two.

ADDRESS RANGE - 480 OPTION

A6			A5	A4	A3	A2	A1	DISK	DISK SET
INF	MS1	MS2							
0	5	10	0	0	0	0	0	1	0
			0	4	9	9	9		
			0	5	0	0	0	2	
			0	9	9	9	9		
			1	0	0	0	0	3	1
			1	4	9	9	9		
			1	5	0	0	0	4	
			1	9	9	9	9		
			2	0	0	0	0	5	2
			2	4	9	9	9		
			2	5	0	0	0	6	
			2	9	9	9	9		
			3	0	0	0	0	7	3
			3	4	9	9	9		
			3	5	0	0	0	8	
			3	9	9	9	9		
			4	0	0	0	0	9	4
			4	4	9	9	9		
			4	5	0	0	0	10	
			4	9	9	9	9		
			5	0	0	0	0	11	5
			5	4	9	9	9		
			5	5	0	0	0	12	
			5	9	9	9	9		
			6	0	0	0	0	13	6
			6	4	9	9	9		
			6	5	0	0	0	14	
			6	9	9	9	9		
			7	0	0	0	0	15	7
			7	4	9	9	9		
			7	5	0	0	0	16	
			7	9	9	9	9		
			8	0	0	0	0	17	8
			8	4	9	9	9		
			8	5	0	0	0	18	
			8	9	9	9	9		
			9	0	0	0	0	19	9
			9	4	9	9	9		
			9	5	0	0	0	20	
			9	9	9	9	9		

File Address Decoding for 240 Option

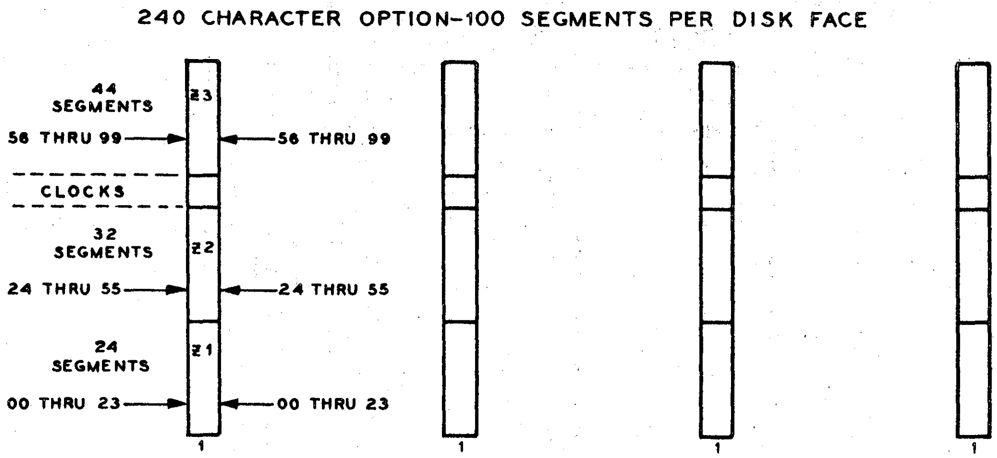
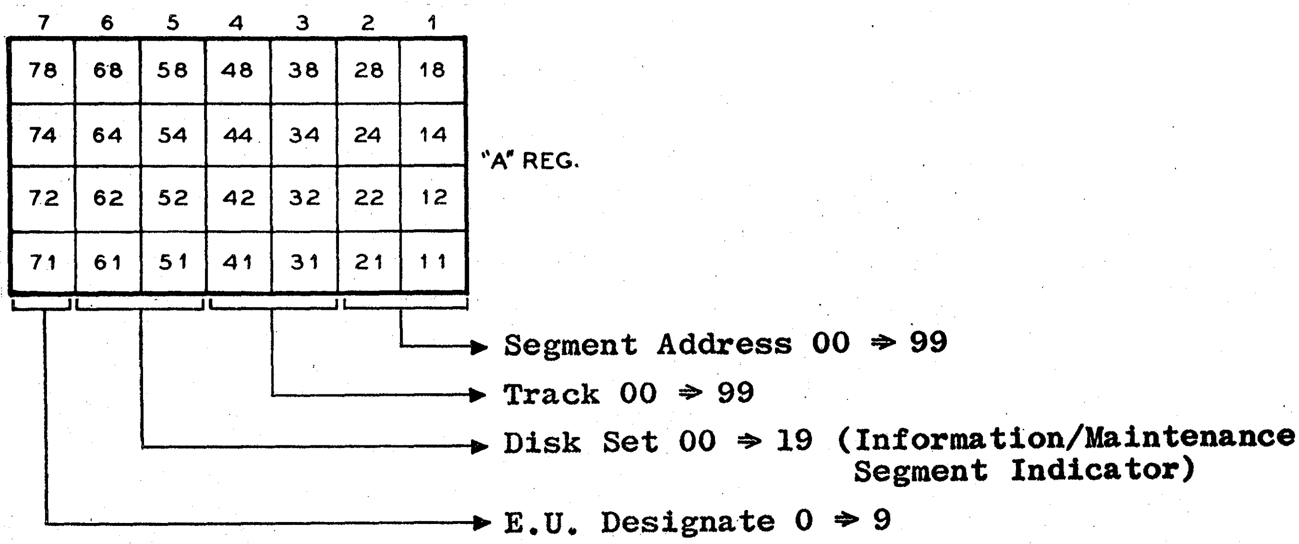


FIGURE 3.5-4
DISK SET-240 OPTION

A disk set in this option consists of one disk holding two complete ranges of segment addresses with one complete track range.

1. Segment 00 ⇛ 99 on both faces.
2. Track 00 ⇛ 49 on "lower" face.
3. Track 50 ⇛ 99 on "upper" face.

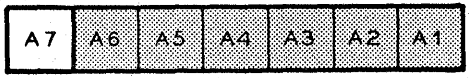


7	6	5	4	3	2	1
78	68	58	48	38	28	18
74	64	54	44	34	24	14
72	62	52	42	32	22	12
71	61	51	41	31	21	11

FIGURE 3.5-5
"A" REGISTER DECODING-240 OPTION

The following is a description of how each decoded output is generated. The "A" Register is represented by decade.

E.U. Designation

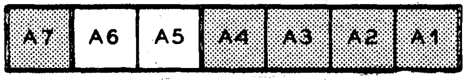


A7	A6	A5	A4	A3	A2	A1

A binary configuration of zero selects E.U. 1; one selects E.U. 2;

nine selects E.U. 10.

Disk Selection



The disk is selected by the fifth and sixth decades. Since the disk set can never exceed 19 and A6 may be any value of 0 → 14, A6 outputs are first decoded to determine an Information or Maintenance segment operation and then given pseudo-values of 0 → 4. The final address decoding then disregards all but the ones bit of the pseudo-values for disk selection.

```
D01L
    240 CS · A51F]─────────────────────→ Disk set 1, 3, 5, 7, 9, 11,
                                                  13, 15, 17 or 19
D02L
    240 CS · (+ A52F · A61S/ ┐
               + A52F/ · A61S)┘────────→ Disk set 2, 3, 6, 7, 10, 11,
                                                  14, 15, 18 or 19
D04L
    240 CS · (+ A61S/ · A58F/ · A54F ┐
               + A58F/ · A54F · A52F/ ├──→ Disk set 4, 5, 6, 7, 12, 13,
               + A61S · A58F/ · A54F/ │           14 or 15
                              · A52F) ┘
D08L
    240 CS · (+ A61S/ · A58F · A54F/ ┐
                              · A52F/ ├──→ Disk set 8, 9, 10, 11, 12,
               + A61S · A58F/ · A54F/ │           13, 14 or 15
               + A61S · A58F/ · A52F/)┘
D16L
    240 CS · (+ A61S · A58F · A54F/ ┐
                             · A52F/ │
                                     ├───→ Disk set 16, 17, 18 or 19
               + A61S . A58F/ · A54F │
                              · A52F)┘
```

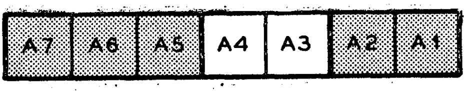
Disk Face Selection

The disk face is selected by the fourth decade.

```
DFSL/
     240 CS · (+ A44F · A41F┐
                + A44F · A42F├─────────────→ Track equals 50 → 99
                + A48F)      ┘
```

Track equals 00 → 49 for "lower" face, 50 → 99 for "upper" face.

Track Selection



The track is selected by the third and fourth decades. Although these may take on a value of 00 → 99, the binary configuration of the track select outputs (TnnL) will never exceed 49.

A3 & A4	TnnL
00 OR 50	00
01 OR 51	01
02 THRU 47 OR 52 THRU 97	02 THRU 47
48 OR 98	48
49 OR 99	49

T01L
96 CS/ · A31F → Track one level

T02L
96 CS/ · A32F → Track two level

T04L
96 CS/ · A34F → Track four level

T08L
96 CS/ · A38F → Track eight level

T10
96 CS/ · (+ A48F/ · A44F/ · A41F
+ A44F · A42F · A41F/
+ A48F · A44F/ · A41F/)

TRACK
10 ⇒ 19
30 ⇒ 39
60 ⇒ 69
80 ⇒ 89

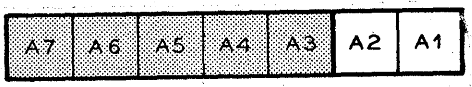
T20L
96 CS/ · (+ A42F · A41F
+ A44F/ · A42F
+ A48F · A44F/ · A41F/)

TRACK
20 ⇒ 29
30 ⇒ 39
70 ⇒ 79
80 ⇒ 89

T40L
96 CS/ · (+ A44F · A42F/ · A41F/
+ A48F · A41F)

TRACK
40 ⇒ 49
90 ⇒ 99

Zone Selection

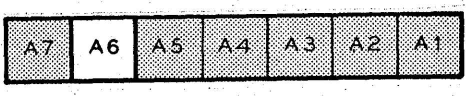


The zone is selected by the first and second decades.

1. (LT) indicates segment address Less Than.
2. (GE) indicates segment address Greater Than or Equal To.

Z01L
(+ 240 CS · LT024S → Zone 1, either face
+ 240 CS · GE024S) → Zone 3, either face

Maintenance/ Information Segment Indicator



The type of segment addressed is indicated by the sixth decade.

1. A6 0 ⇒ 4 for Information segment.
2. A6 5 ⇒ 9 for Maintenance segment one.

3. A6 10 ➡ 14 for Maintenance segment two.

ADDRESS RANGE - 240 OPTION

A6			A5	A4	A3	A2	A1	DISK	DISK SET
INF	MS1	MS2							
0	5	10	0	0	0	0	0	1	0
			0	9	9	9	9		
			1	0	0	0	0	2	1
			1	9	9	9	9		
			2	0	0	0	0	3	2
			2	9	9	9	9		
			3	0	0	0	0	4	3
			3	9	9	9	9		
			4	0	0	0	0	5	4
			4	9	9	9	9		
			5	0	0	0	0	6	5
			5	9	9	9	9		
			6	0	0	0	0	7	6
			6	9	9	9	9		
			7	0	0	0	0	8	7
			7	9	9	9	9		
			8	0	0	0	0	9	8
			8	9	9	9	9		
			9	0	0	0	0	10	9
			9	9	9	9	9		
1	6	11	0	0	0	0	0	11	10
			0	9	9	9	9		
			1	0	0	0	0	12	11
			1	9	9	9	9		
			2	0	0	0	0	13	12
			2	9	9	9	9		
			3	0	0	0	0	14	13
			3	9	9	9	9		
			4	0	0	0	0	15	14
			4	9	9	9	9		
			5	0	0	0	0	16.	15
			5	9	9	9	9		
			6	0	0	0	0	17	16
			6	9	9	9	9		
			7	0	0	0	0	18	17
			7	9	9	9	9		
			8	0	0	0	0	19	18
			8	9	9	9	9		
			9	0	0	0	0	20	19
			9	9	9	9	9		

File Address Decoding for 96 Option

96 CHARACTER OPTION-250 SEGMENTS PER DISK FACE

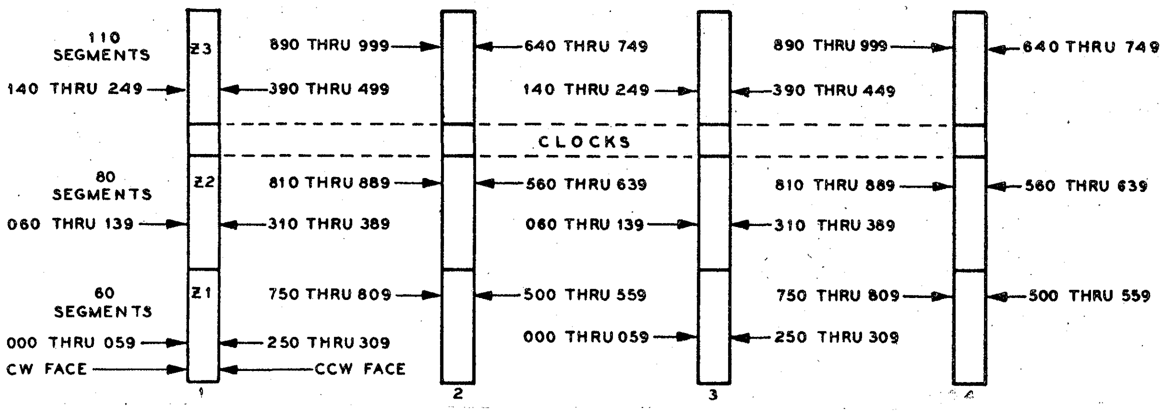


FIGURE 3.5-6
DISK SET - 96 OPTION

A disk set in this option consists of four disks holding two complete ranges of segment addresses with one complete track range.

1. Segment 000 ⇒ 249 on "lower" face of disk 1 and 3.
2. Segment 250 ⇒ 499 on "upper" face of disk 1 and 3.
3. Segment 500 ⇒ 749 on "lower" face of disk 2 and 4.
4. Segment 750 ⇒ 999 on "upper" face of disk 2 and 4.

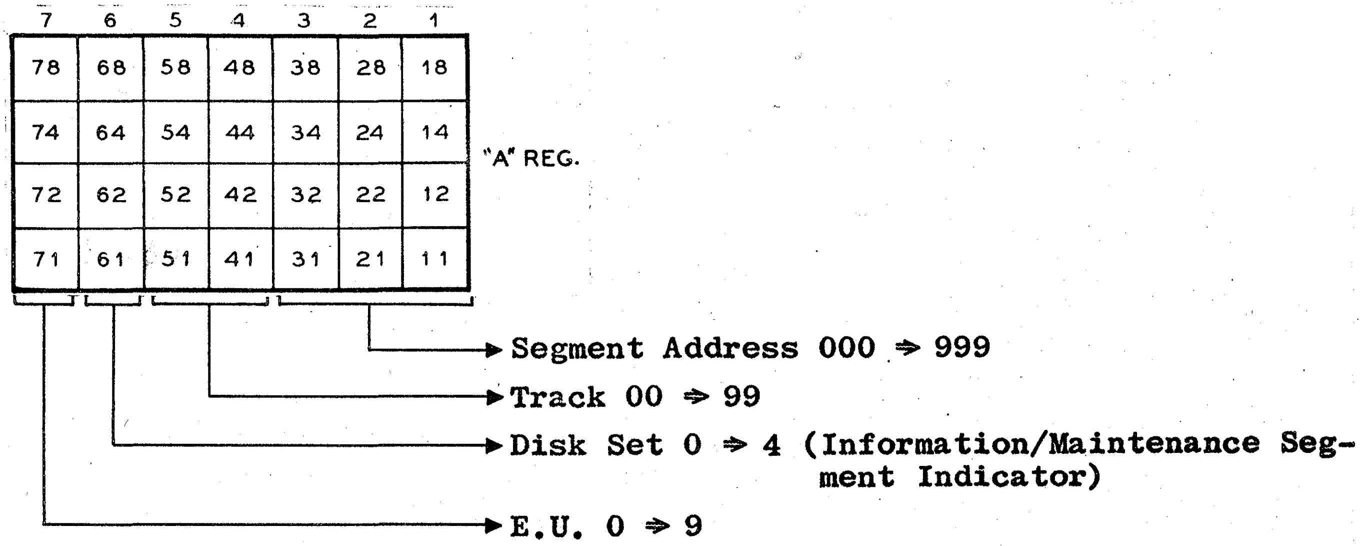
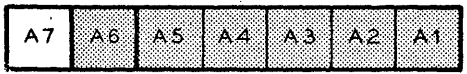


FIGURE 3.5-7
"A" REGISTER DECODING - 96 OPTION

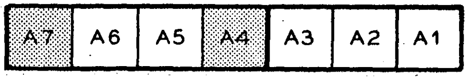
The following is a description of how each decoded output is generated. The "A" Register is represented by decade.

E.U. Designation



A binary configuration of zero selects E.U. 1; one selects E.U. 2; nine selects E.U. 10.

Disk Selection



The disk is selected by the first, second, third, fifth and sixth decades. The disk set is selected by A6 and the one disk out of four in the set is selected by A1, A2, A3 and A5. Since the disk set can never exceed 4 and A6 may be any value of 0 ⇒ 14, A6 outputs are first decoded to determine an Information or Maintenance segment operation and then given pseudo-values of 0 ⇒ 4. The final address decoding logic decodes the four two and one levels of the pseudo-values for disk selection.

(GE) indicates segment address Greater Than or Equal To.

D01L
96 CS · GE500S] → Segment addresses 500 ⇒ 999

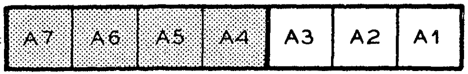
D02L
96 CS · (+ A54F · A51F
+ A54F · A52F] → Track equals 50 ⇒ 99
+ A58F)

D04L
96 CS · A61S] → Disk set 1 or 3

D08L
96 CS · A62S] → Disk set 2 or 3

D16L
96 CS · A64S] → Disk set 4

Disk Face Selection



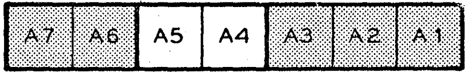
The disk face is selected by the first, second and third decades.

DFSL/
96 CS · (+ GE250S · LT500S] → Segment Address equals 250 ⇒ 749 "upper" faces of disks 1 and 3

+ GE750S)] → Segment address equals 750 ⇒ 999 "upper faces of disks 2 and 4

Segment address 000 ⇒ 249 for "lower" faces of disks 1 and 3, and 500 ⇒ 749 for "lower" faces of disks 2 and 4.

Track Selection



The track is selected by the fourth and fifth decades. Although these may be 00 ⇒ 99, the track select outputs (TnnL) will never exceed 49.

A3 & A4	TnnL
00 OR 50	00
01 OR 51	01
02 THRU 47 OR 52 THRU 97	02 THRU 47
48 OR 98	48
49 OR 99	49

T01L

96 CS · A41F → Track one level

T02L

96 CS · A42F → Track two level

T04L

96 CS · A44F → Track four level

T08L

96 CS · A48F → Track eight level

T10L

96 CS · (+ A58F/ · A54F/ · A51F
+ A54F · A52F · A51F/
+ A58F · A54F/ · A51F/)

TRACK
10 = 19
30 = 39
60 = 69
80 = 89

T20L

96 CS · (+ A52F · A51F
+ A54F/ · A52F
+ A58F · A54F/ · A51F/)

TRACK
20 = 29
30 = 39
70 = 79
80 = 89

T40L

96 CS · (+ A54F · A52F/ · A51F/
+ A58F · A51F)

TRACK
40 = 49
90 = 99

Zone Selection

A7	A6	A5	A4	A3	A2	A1

The zone is selected by the first, second and third decades.

1. (LT) indicates segment address Less Than.
2. (GE) indicates segment address Greater Than or Equal To.

Z01L

(+96 CS · LT250S · LT060S → Zone 1, Disks 1 or 3 "lower" face

+96 CS · GE250S · LT500S · LT310S → Zone 1, Disks 1 or 3 "upper" face

+96 CS · GE500S · LT750S · LT560S → Zone 1, Disks 2 or 4 "lower" face

+96 CS · GE750S · LT810S → Zone 1, Disks 2 or 4 "upper face

+96 CS · GE250S · LT500S · GE390S → Zone 3, Disks 1 or 3 "upper" face

+96 CS · GE500S · LT750S · GE640S] → Zone 3, Disks 2 or 4 "lower" face

+96 CS · GE750S · GE890S] → Zone 3, Disks 2 or 4 "upper" face

+96 CS · LT250S · GE140S)] → Zone 3, Disks 1 or 3 "lower" face

Z02L
(+96 CS · LT250S · GE060S] → Zone 2 or 3, Disks 1 or 3 "lower" face

+96 CS · GE250S · LT500S · GE310S] → Zone 2 or 3, Disks 1 or 3 "upper" face

+96 CS · GE500S · LT750S · GE560S] → Zone 2 or 3, Disks 2 or 4 "lower" face

+96 CS · GE750S · GE810S)] → Zone 2 or 3, Disks 2 or 4 "upper" face

Information/Maintenance Segment Indicator

Information/Maintenance Segment Indicator	A7	A6	A5	A4	A3	A2	A1

The type of segment addressed is indicated by the sixth decade.

A6 0 ⇒ 4 for Information segment.

A6 5 ⇒ 9 for Maintenance segment one.

A6 10 ⇒ 14 for Maintenance segment two.

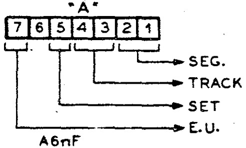
ADDRESS RANGE - 96 OPTION

A6			A5	A4	A3	A2	A1	DISK	DISK SET
INF	MS1	MS2							
0	5	10	0	0	0	0	0	1	0
			4	9	4	9	9		
			0	0	5	0	0	2	
			4	9	9	9	9		
			5	0	0	0	0	3	
			9	9	4	9	9		
			5	0	5	0	0	4	
			9	9	9	9	9		
1	6	11	0	0	0	0	0	5	1
			4	9	4	9	9		
			0	0	5	0	0	6	
			4	9	9	9	9		
			5	0	0	0	0	7	
			9	9	4	9	9		
			5	0	5	0	0	8	
			9	9	9	9	9		
2	7	12	0	0	0	0	0	9	2
			4	9	4	9	9		
			0	0	5	0	0	10	
			4	9	9	9	9		
			5	0	0	0	0	11	
			9	9	4	9	9		
			5	0	5	0	0	12	
			9	9	9	9	9		
3	8	13	0	0	0	0	0	13	3
			4	9	4	9	9		
			0	0	5	0	0	14	
			4	9	9	9	9		
			5	0	0	0	0	15	
			9	9	4	9	9		
			5	0	5	0	0	16	
			9	9	9	9	9		
4	9	14	0	0	0	0	0	17	4
			4	9	4	9	9		
			0	0	5	0	0	18	
			4	9	9	9	9		
			5	0	0	0	0	19	
			9	9	4	9	9		
			5	0	5	0	0	20	
			9	9	9	9	9		

480 CHARACTER OPTION

ZONE	1	2	3	SET	TRACK	SEGMENTS	MOD	1								2								3								4								5							
							DISK	1		2		3		4		5		6		7		8		9		10		11		12		13		14		15		16		17		18		19		20	
							FACE	L	U	U	L	L	U	U	L	L	U	U	L	L	U	U	L	L	U	U	L	L	U	U	L	L	U	U	L	L	U	U	L	L	U	U	L	L	U	U	L
SEGMENTS	00 - 11	12-27	28-49			00 → 49		X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X
	50 - 61	62-77	78-99			50 → 99			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X	
					00 → 49			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X		
					50 → 99					X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X
				0				X	X	X	X																																				
				1								X	X	X	X																																
				2												X	X	X	X																												
				3																X	X	X	X																								
				4																				X	X	X	X																				
				5																								X	X	X	X																
				6																												X	X	X	X												
				7																																X	X	X	X								
				8																																				X	X	X	X				
				9																																								X	X	X	X

"A"



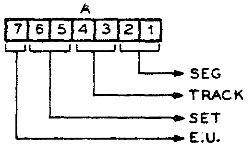
A6nF

NORM	0
M1	5
M2	10

240 CHARACTER OPTION

	00 - 23	24 - 55	56-99			00 — 99		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
					00 — 49			X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X
					50 — 99				X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X	
				0				X	X																																						
				1						X	X																																				
				2								X	X																																		
				3										X	X																																
				4												X	X																														
				5														X	X																												
				6																X	X																										
				7																		X	X																								
				8																				X	X																						
				9																						X	X																				
				10																								X	X																		
				11																										X	X																
				12																												X	X														
				13																														X	X												
				14																																X	X										
				15																																		X	X								
				16																																				X	X						
				17																																						X	X				
				18																																								X	X		
				19																																										X	X

A



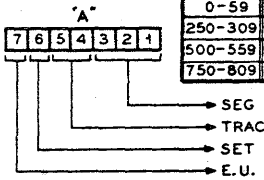
A6nF

NORM	0	1
M1	5	6
M2	10	11

96 CHARACTER OPTION

	0-59	60-139	140-249			000 → 249		X				X				X				X				X				X				X				X				X				X			
	250-309	310-389	390-499			250 → 499			X				X				X				X				X				X				X				X				X				X		
	500-559	560-639	640-749			500 → 749					X				X				X				X				X				X				X				X				X				X
	750-809	810-889	890-999			750 → 999				X				X				X				X				X				X				X				X				X				X	
					00 → 49			X	X	X	X					X	X	X	X					X	X	X	X					X	X	X	X					X	X	X	X				
					50 → 99							X	X	X	X					X	X	X	X					X	X	X	X					X	X	X	X					X	X	X	X
				0				X	X	X	X	X	X	X	X																																
				1												X	X	X	X	X	X	X	X																								
				2																				X	X	X	X	X	X	X	X																
				3																												X	X	X	X	X	X	X	X								
				4																																				X	X	X	X	X	X	X	X

"A"



A6nF

NORM	0	1	2	3	4
M1	5	6	7	8	9
M2	10	11	12	13	14

FIGURE 3.5-8
ADDRESS LOCATOR

3.6 EXCHANGE

A Disk File Exchange consists of a Matrix to allow one or two D.F.C.Us to select any one of up to five E.Us. A second Matrix, when used in conjunction with the first, allows from one to four D.F.C.Us to select any one of up to ten E.Us. See Figure 3.6-1.

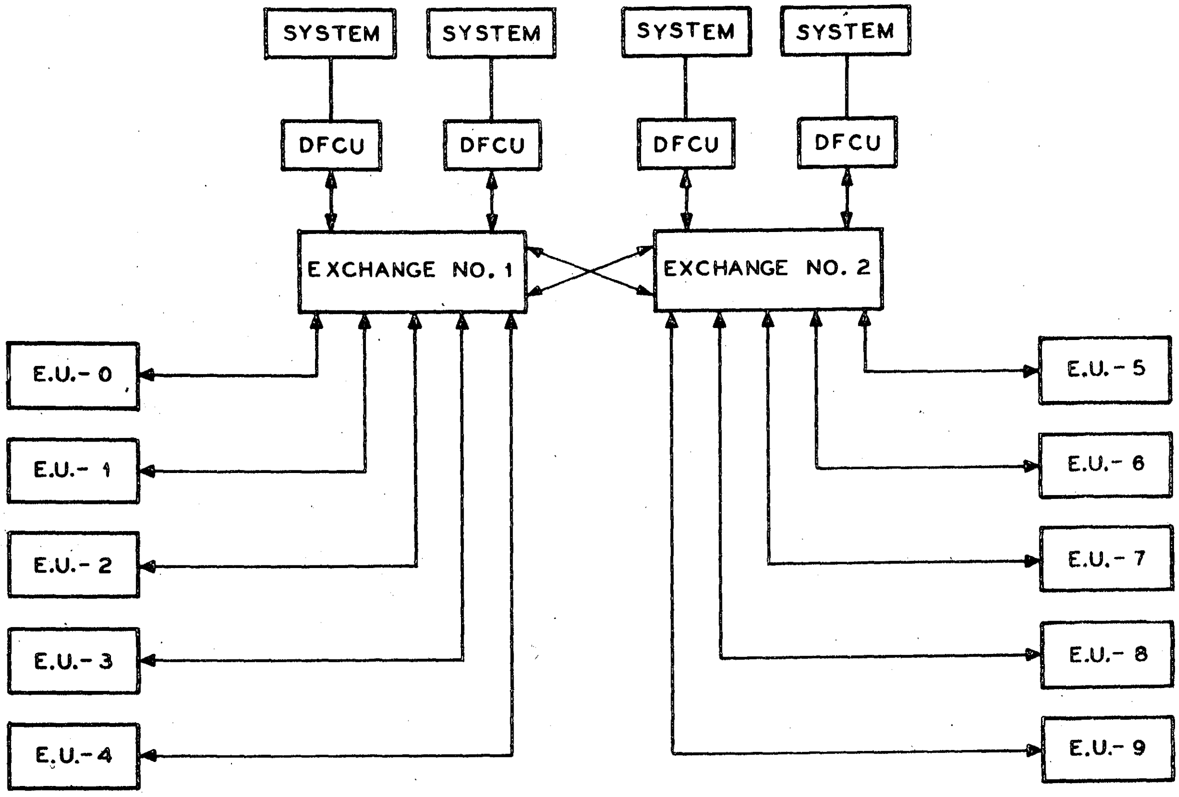


FIGURE 3.6-1
EXCHANGE BLOCK DIAGRAM

Exchange 1 hardware occupies the E/F Panel, "A" Gate, of the B450 Cabinet and is mounted below the D.F.C.U. designated Control 1 - 3 or just simply Control 13.

> NOTE: Control 13 is pronounced Control one - three, NOT Control thirteen. Similarly, Control 24 is Control two - four. Control 13 is abbreviated C13 and Control 24 is abbreviated C24 in the D.As.

Exchange 2 hardware (if present) occupies the E/F Panel, "E" Gate, of the same B450 Cabinet.

Each D.F.C.U. has twenty-three output lines and six designate lines to the Exchange. The twenty-three output lines carry the Address and Information Track Select Levels and the Write Levels. The fourteen input lines carry the Read Information Levels, and signals. The six designate lines are the outputs of the A7nFs, and determine which E.U. will be selected.

The Exchanges 1 & 2 are cabled as shown in Figure 3.6-2.

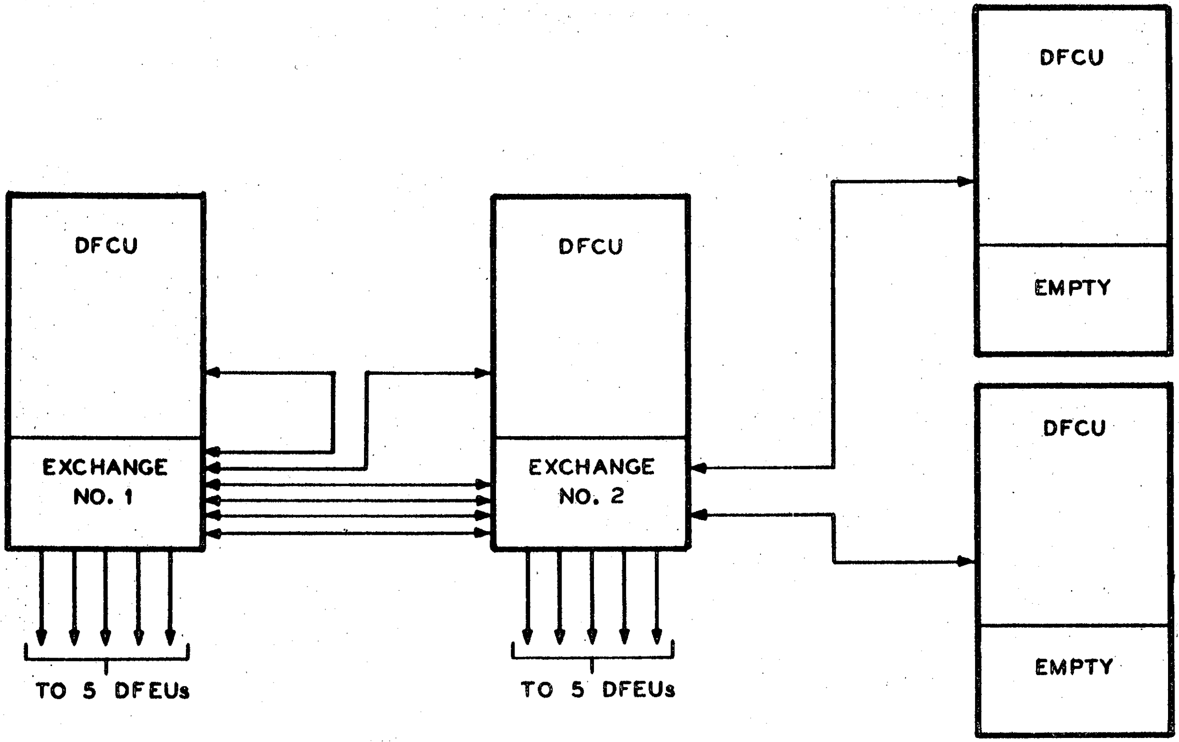


FIGURE 3.6-2
EXCHANGE CABLING BLOCK DIAGRAM

The input/output connections are labelled as shown in Figure 3.6-3.

Exchange 1 and Exchange 2 are identical. The D.F.C.Us may be connected to each Exchange. Within an Exchange, the inputs from the DFCUs are abbreviated C13 or C24, and the inputs from the other Exchange are abbreviated X3 or X4. The five E.Us connected to each Exchange are abbreviated E1, E2, E3, E4 and E5. When following signals from one Exchange to the other, C13 becomes X3 and C24 becomes X4 in the other Exchange.

As both Exchanges are identical, only Exchange 1 will be considered in detatil.

Logic levels from the D.F.C.U. to the Exchange are present at all times, but the Exchange performs no active gating until the Open Trunk Level (0TRL) goes false to indicate that the D.F.C.U. is attempting to access an E.U. designated by the "A" Register. The Designate Achieved Level (DACD in Exchange, DACL in the D.F.C.U.) being true, indicates that access has been achieved, and the D.F.C.U. logic can proceed.

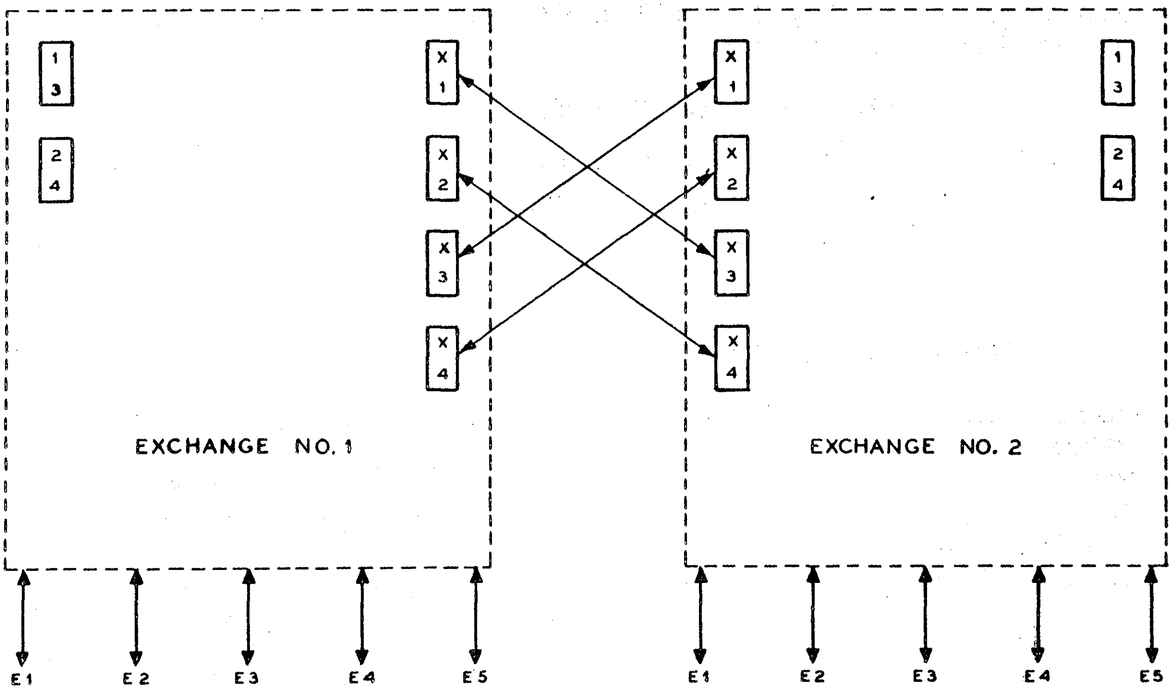
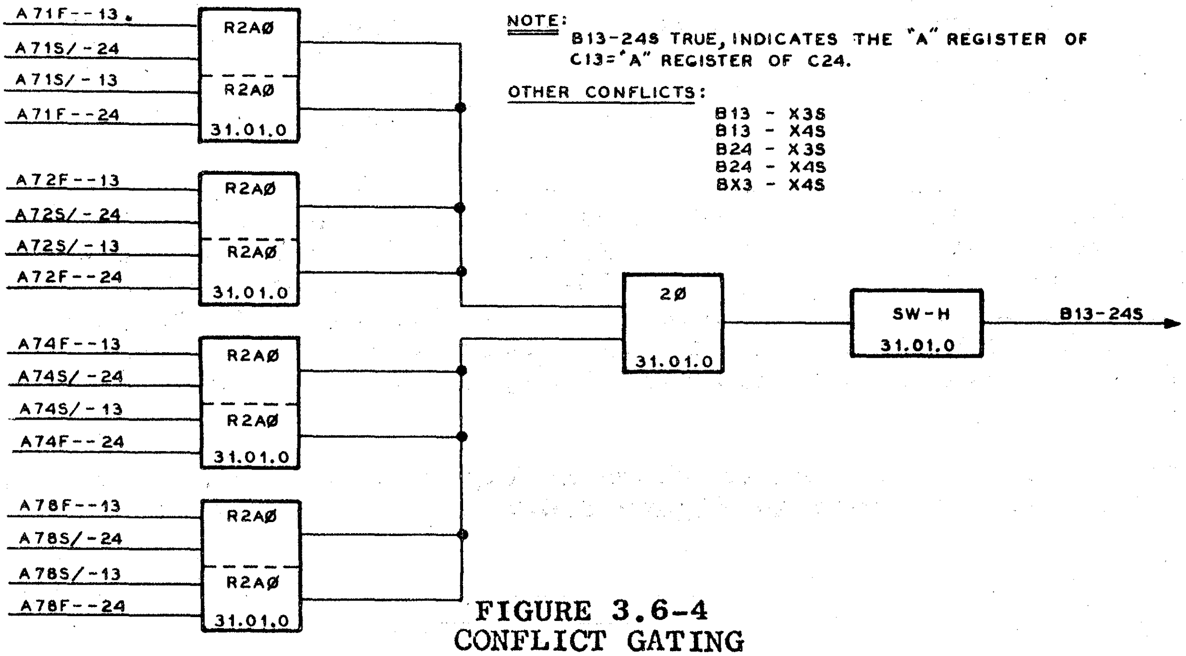


FIGURE 3.6-3
CONNECTIONS

Once DACL goes true, it will remain true for the duration of the operation.

Conflict may inhibit the D.F.C.U. from accessing the required E.U. With more than one D.F.C.U. and one E.U. in the Subsystem, the possibility of two D.F.C.U.s attempting to access the same E.U. exists. This situation is called Conflict. See Figure 3.6-4.



NOTE:
B13-24S TRUE, INDICATES THE "A" REGISTER OF C13="A" REGISTER OF C24.

OTHER CONFLICTS:
B13 - X3S
B13 - X4S
B24 - X3S
B24 - X4S
BX3 - X4S

FIGURE 3.6-4
CONFLICT GATING

The D.F.C.U. sends the outputs of the A7nFs to the Exchange where they are decoded to produce levels called E1, E2, E3, E4 and E5. These levels are produced as follows:

A7nFs = 0 or 5 = E1
1 or 6 = E2
2 or 7 = E3
3 or 8 = E4
4 or 9 = E5

The gating is shown in Figure 3.6-5.

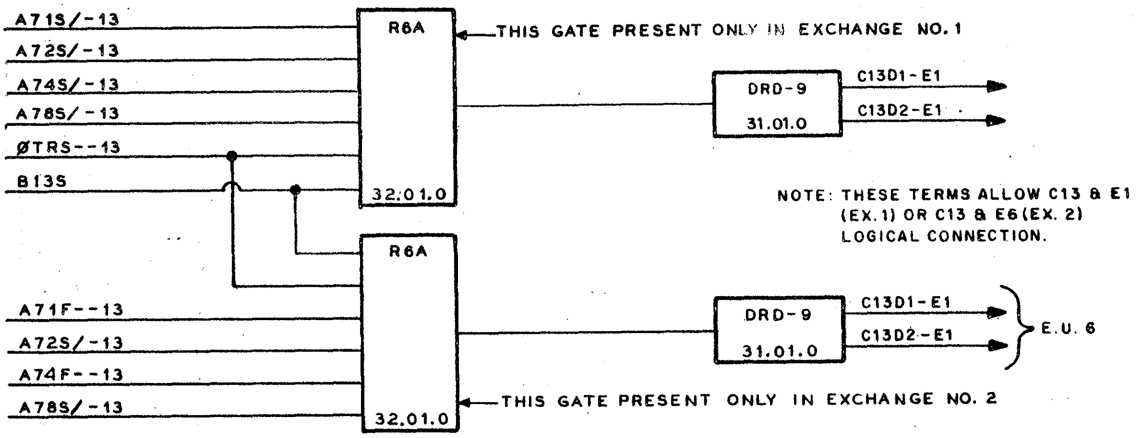


FIGURE 3.6-5
E.U. DESIGNATE DRIVERS

ØTRS (ØTRL/ switched) is true as long as the D.F.C.U. is at SC ≥ 6. ØTRS going false releases the logical connection between the D.F.C.U. and the E.U. The gating levels B13S, B24S, BX3S and BX4S allow the D.F.C.U. to become logically connected to an E.U. B13S allows C13, B24 allows C24, etc. The generation of these levels is shown in Figure 3.6-6.

Each of the four outputs shown represent similar situations.

For explanation, refer to the top AND gate of Figure 3.6-6. The level B13-24S would be true if a conflict existed between C13 and C24 (the "A" Registers designating the same E.U.). If the other D.F.C.U. C24, already had access to that E.U., DACD--24 would be true. The two terms would cause B13S to be false, and the D.F.C.U. C13 would have to wait until the other D.F.C.U. C24 had finished with its operation, DACD--24 had become false, and B13S true, before D.F.C.U. C13 could proceed.

The lower output of the driver shown in Figure 3.6-5 when true, will produce DACD--13 as shown in Figure 3.6-7.

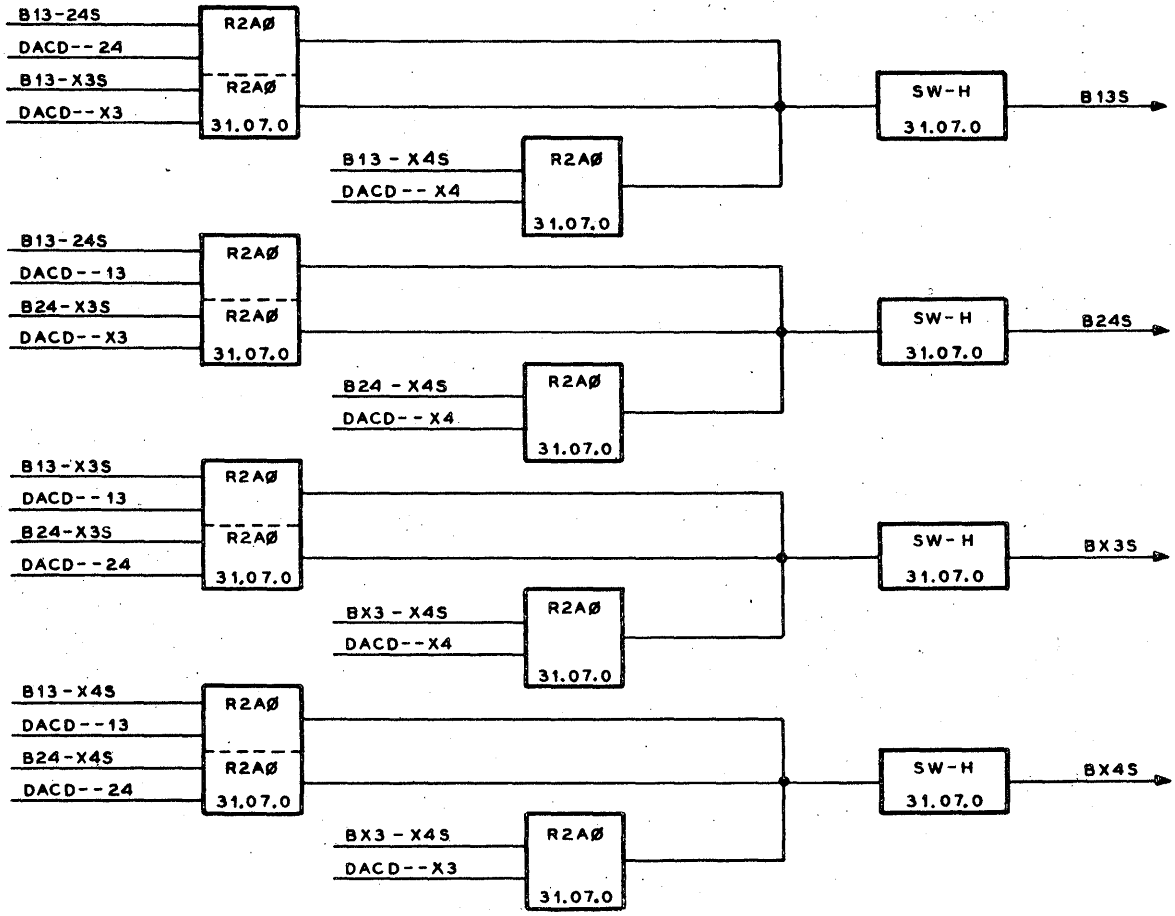


FIGURE 3.6-6
CONFLICT INTER-LOCK SWITCHES

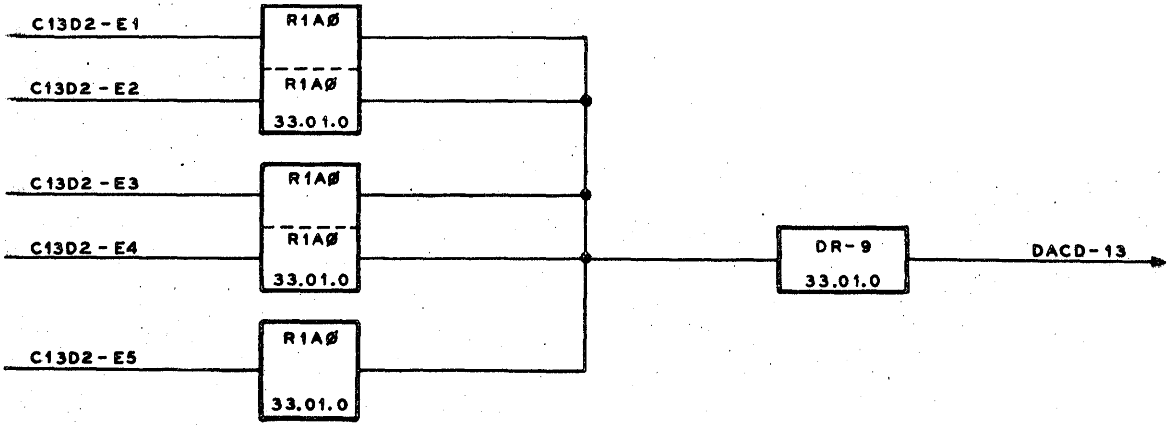


FIGURE 3.6-7
DESIGNATE ACHIEVED DRIVERS

INDEX - SECTION IV

4 FUNCTIONAL DESCRIPTION - MECHANICAL (Not Applicable)

INDEX - SECTION V

5 ASSEMBLY - DISASSEMBLY - ADJUSTMENTS

5.11 VARIABLE BIAS ADJUSTMENTS

There are five VB packages in DFCU. The output levels are adjusted as follows:

VB	Flip-Flop	AAD7K2	-1.2V
VB	"	AAB0K7	-1.2V
VB	"	AAC0K7	-1.2V
VB	"	AAB6X7	-1.2V
VB	Clock Bias	AAC8K2	-.5V

5.12 CLOCK CONTROL ADJUSTMENTS

Before checking the Clock Control adjustments, check that the Variable Bias adjustments, covered in Section 5.11, are correct.

Clock B.O. (AAB7N2) 140 nanoseconds ± 10 nanoseconds at the -1.5V level (with respect to ground). Scope at AAC7B7, sync internal negative. Recycle in LOCAL.

SCLM (AAC7N2) 1.6 microseconds ± .1 microsecond. Scope at AAC5H4 (SCMS/), sync external negative with SCLS at AC5C0. Recycle in LOCAL. There is no adjustment.

DCPM (AAC6N2) 600 microseconds ± 60 microseconds. Scope at AAC6U0, sync internal negative.

To accurately check DCPM requires an external R1A0. The field engineer should permanently attach three leads to the B, C and D pins of a B diode stick. Terminate the leads in "crocodile" clips or scope lead spring tips. Insulate the stick with electrical tape or other convenient media. Attach the C lead to -12V (available at any diode stick location on either C or J pins for an L location or R or W pins for a Y location). Attach the B lead to the Clock B.O. output (AAC7B7). Set the Clock ON/OFF switch to OFF in the first E.U. With Control in LOCAL, each depression of the START switch will create a clock pulse to fire DCPM.

This external R1A0 is a convenient way of firing any multi for checking purposes.

INDEX - SECTION VI

6 MAINTENANCE PROCEDURES AND AIDS

6.6 MAINTENANCE PANEL

Refer to Figure 1.1-5.

The Maintenance Panel consists of switches, indicators and indicator-switches for power control and maintenance functions.

POWER CONTROL

Switches	Indicators
POWER ON	POWER ON
POWER OFF	
NEON POWER	

MAINTENANCE

Switches	Indicators
LOCAL-REMOTE	LOCAL
READ-WRITE	
ERROR STOP	
RECYCLE	
N-REGISTER SET	
KEY SEGMENT	
MAINTENANCE START	
A-REGISTER CLEAR	
B-REGISTER CLEAR	
BIT RESET	

Indicator-Switches

ADDRESS REGISTER
N REGISTER
B REGISTER
LP REGISTER

CL1F, CL2F, CL4F and CL8F - Clock Counter
SO1F, SO2F, SO4F, S10F and S20F - Sequence Counter
SCLF - Storage Character Clock
IDXF - Index FF
FRPF - Information Write Parity

LOCAL-REMOTE

Refer to Figure 6.6-1.

REMOTE - 1. Couples Processor Power On and Off pulses (P1-ON-P and P1-OFF-P) to B450 and disables Maintenance Panel power switches.

2. ESPL/ false to ERROR STOP switch.

3. Picks Local-Remote relay with Power-On-Level from B450. FCRL/ false indicating D.F.C.U. ready, RECL false to RECYCLE switch and LØCL true to READ-WRITE switch.

LOCAL - 1. Enables Maintenance Panel power switches and disables Processor power control.

2. LOCAL indicator "ON".

3. ESPL/ true to ERROR STOP switch.

4. FCRL/ true indicating D.F.C.U. not ready, RECL true to RECYCLE switch and LØCL false to READ-WRITE switch.

5. Conditions D.F.C.U. to operate in B200 mode for all LOCAL operations (SIDS/).

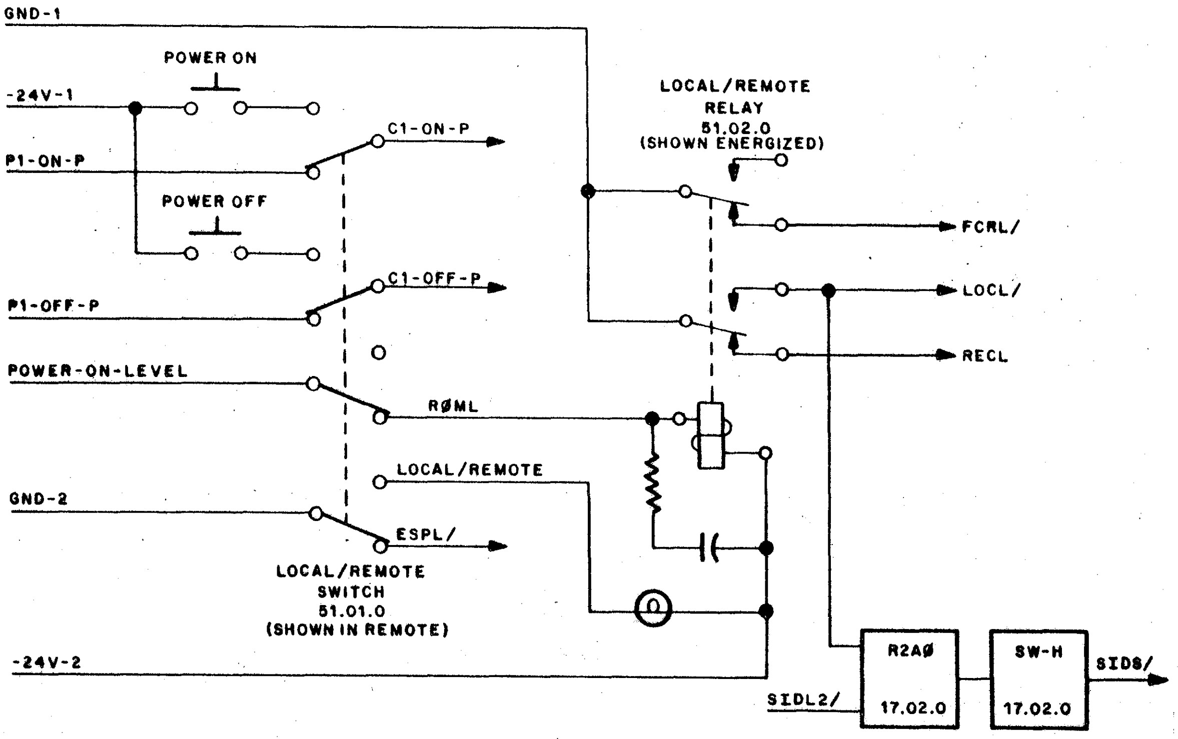


FIGURE 6.6-1
LOCAL-REMOTE SWITCH

READ-WRITE

Refer to Figure 6.6-2.

In LOCAL, the READ-WRITE switch conditions FWRS (File Write Switch) for a read or write operation. In REMOTE, this switch is disabled by LØCS and FWRS is controlled by FWRL (File Write Level) from the associated Data Processor.

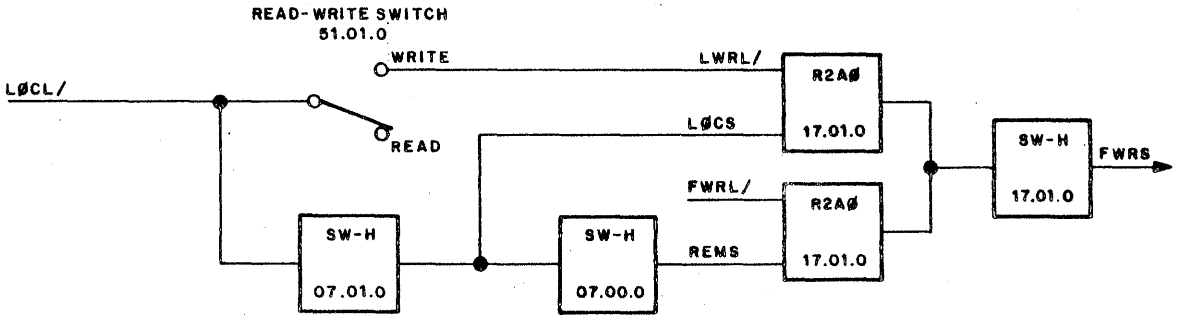


FIGURE 6.6-2
READ/WRITE SWITCH

ERROR STOP

Refer to Figure 6.6-3.

In LOCAL, with ERROR STOP on, file operations are halted when an error is encountered. This is done by disabling the reset of S01F. In REMOTE, ESPL/ is false, inhibiting the reset of S01F at ØPCD (Operation Complete) time.

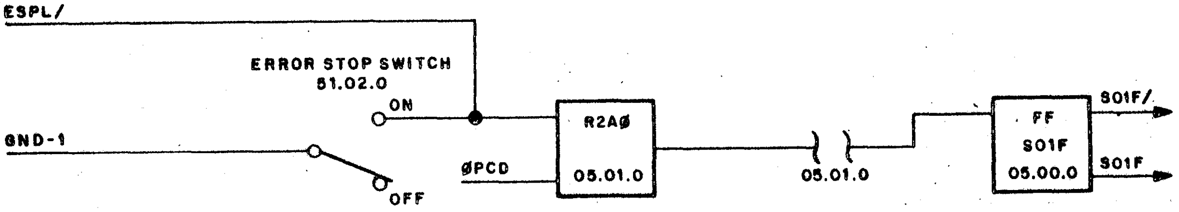


FIGURE 6.6-3
ERROR STOP SWITCH

RECYCLE

Refer to Figure 6.6-4.

In LOCAL, with RECYCLE on, a count of six is automatically set into the sequence counter when the following levels are true.

IDLD - Idle condition
DCPP - Disk Clock present
S01F/
S02F/ - No error present

By advancing the sequence count to six, file address transfer from Data Processor to control (sequence count = 4) is by-passed and the address word, which may be manually set in A, is used. In REMOTE, RECL is false, disabling this switch.

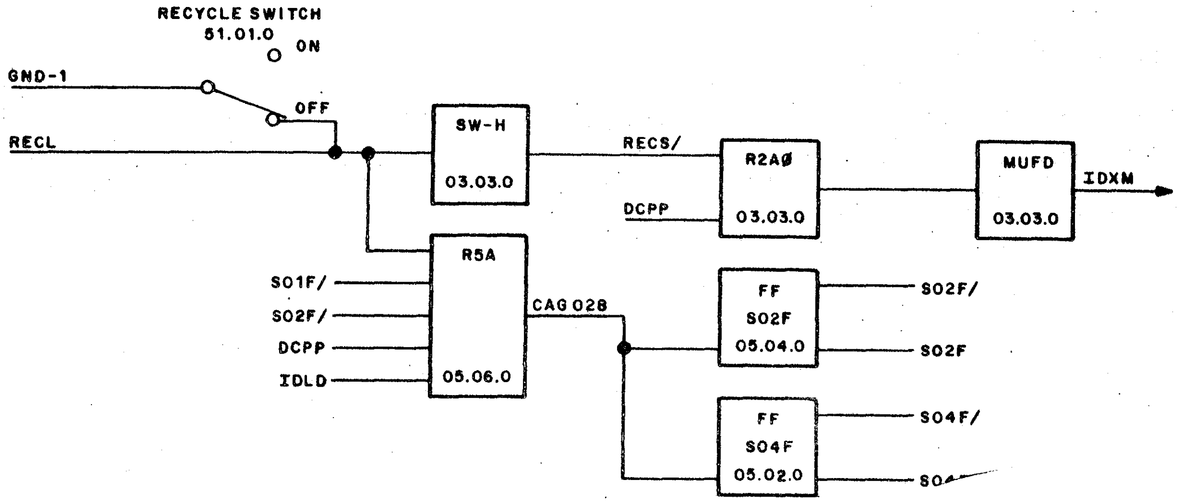


FIGURE 6.6-4
RECYCLE SWITCH

N-SET

Refer to Figure 6.6-5.

In LOCAL, the N-SET switch will set the Number of Segments register to 1, 2 or 10 at a sequence count of six or seven. In REMOTE, LOCS is false, disabling this switch.

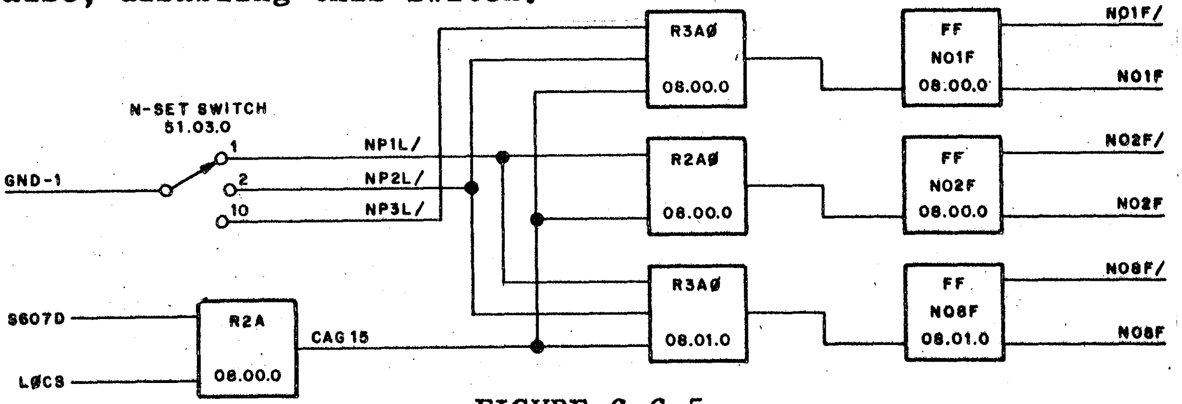


FIGURE 6.6-5
N-SET SWITCH

KEY SEGMENT

Refer to Figure 6.6-6.

In REMOTE, at a sequence count of fourteen, incoming segment address characters from the E.U. are compared to a desired address in A for Segment Coincidence (SCOL). Each character is shifted into BAnf, compared, then dropped as the next character is shifted in. In LOCAL, with KEY SEGMENT on, B register shift pulses (BBSD) are generated during the shift-in of characters and the segment address is stored in B instead of being dropped.

In REMOTE, at a sequence count of thirty (Write Operation), characters to be written are transferred to the SWnL's (Storage Write Lines) from B. As characters are transferred, the new characters are shifted into B from the Data Processor. In LOCAL, with KEY SEGMENT on, the segment address characters, previously stored in B at sequence count fourteen, are transferred to the SWnL's and circulated in B by an end-around shift from BDnF to BAnF. Loading of the B register by the Data Processor is inhibited and the file will write and circulate only the segment address characters.

The overall function of KEY SEGMENT is to read and store a desired segment address, then write that address back into the information track while circulating it in B.

KEY SEGMENT has no function in a read operation or in REMOTE since SC30S (Write) and L0CS enable the end-around shift in B (CAG 13 and 14).

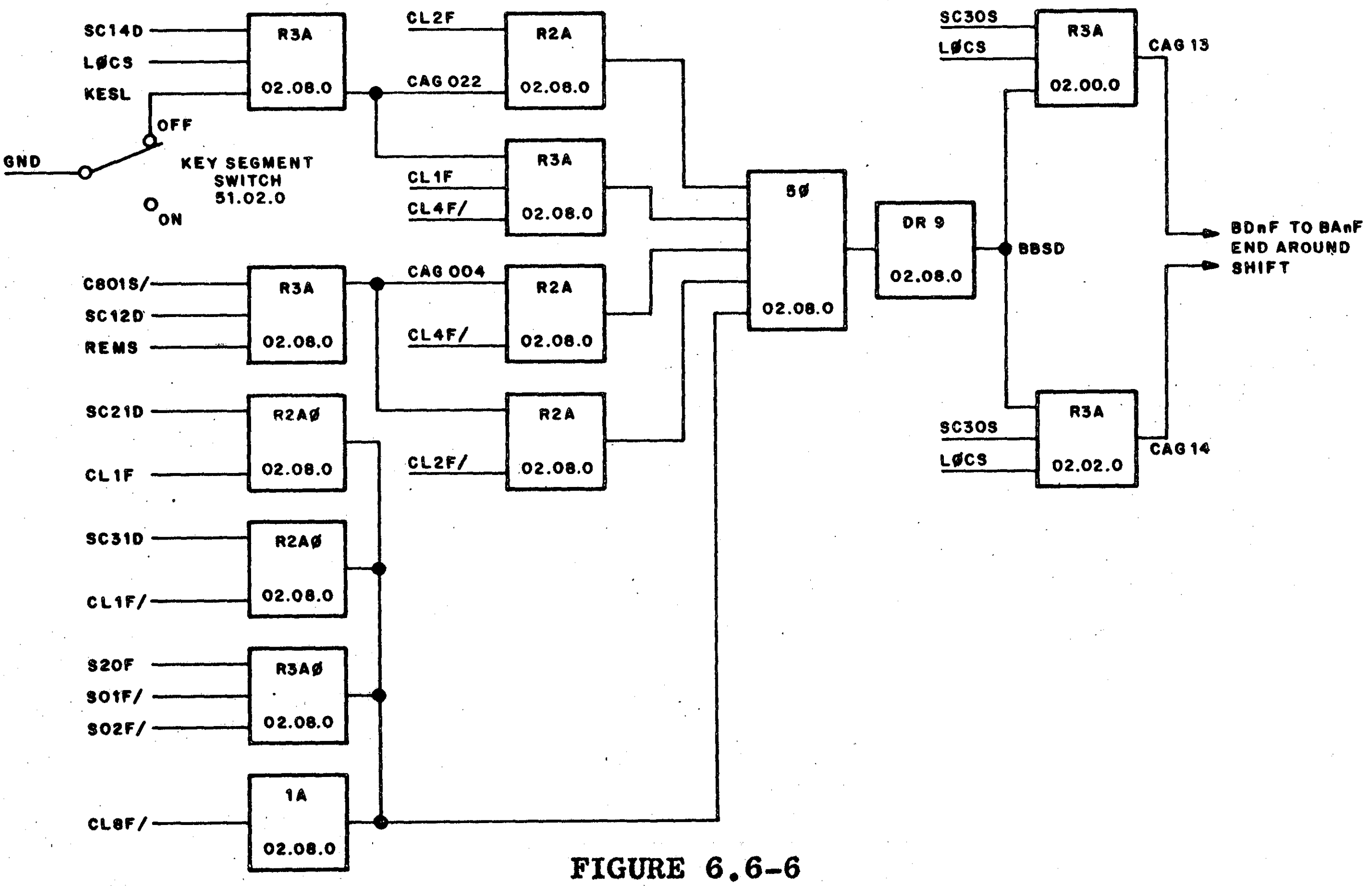


FIGURE 6.6-6
KEY SEGMENT SWITCH

MAINTENANCE START

Refer to Figure 6.6-7.

In LOCAL, the MAINTENANCE START switch initiates a maintenance operation by:

1. Starting the clock counter (CCLD).
2. Resetting S01F (error condition).
3. Set a sequence count of six.

In REMOTE, this switch is disabled by LØCS.

The PSH generates a 350 to 400 nanosecond, negative going pulse, the leading edge of which coincides with a negative going input. The cross-coupled switch is set when MAINTENANCE START is depressed (MASS true) and reset when returned to its normal position.

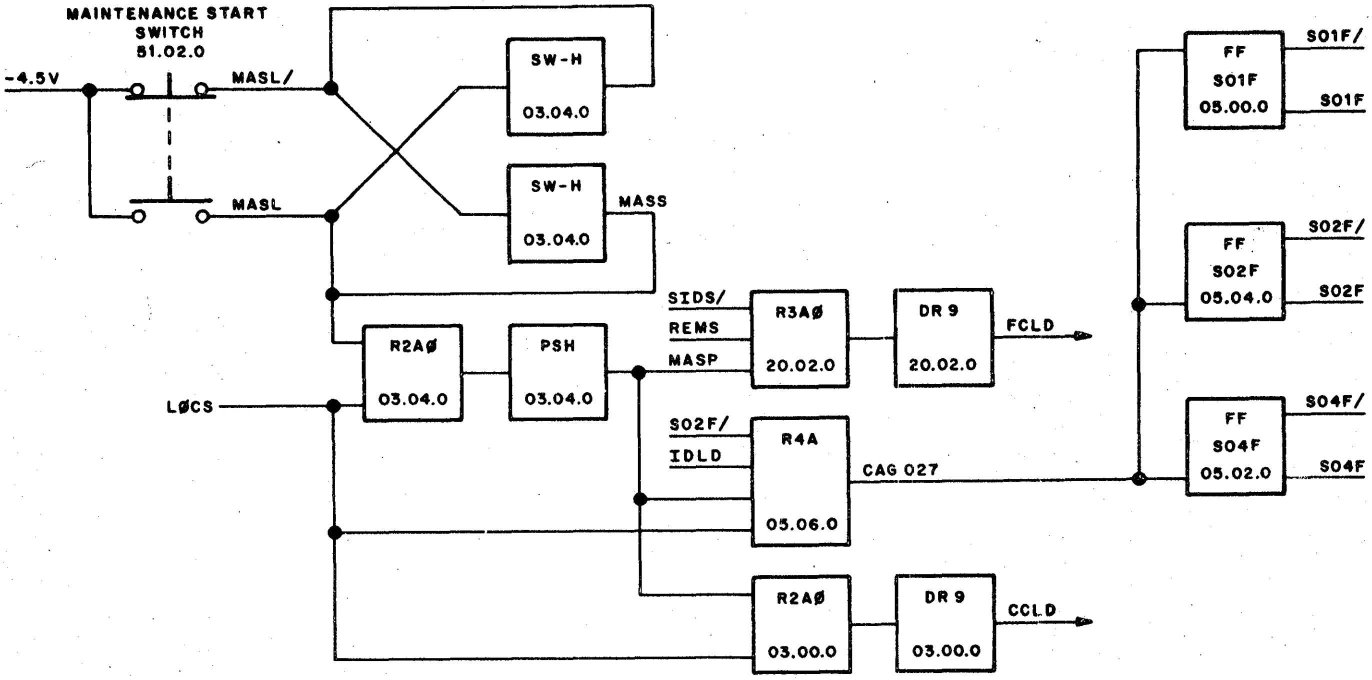


FIGURE 6.6-7
MAINTENANCE START SWITCH

EXAMPLE USES

Read one segment address continually.

1. LOCAL-REMOTE to LOCAL
2. Depress MASTER CLEAR
3. Set desired segment address in A register indicator-switches
4. READ-WRITE to READ

5. N-REGISTER SET to 1
6. RECYCLE "ON"
7. ERROR STOP "ON" if a stop on error is desired
8. KEY SEGMENT "OFF"
9. Depress MAINTENANCE START

Read ten segments sequentially beginning at a desired segment address.

1. LOCAL-REMOTE to LOCAL
2. Depress MASTER CLEAR
3. Set desired address in A register indicator-switches
4. READ-WRITE to READ
5. N-REGISTER SET to 10
6. RECYCLE "OFF"
7. ERROR STOP "ON" if a stop on error is desired
8. KEY SEGMENT "OFF"
9. Depress MAINTENANCE START

Read sequentially from address 0000000, two segments at a time.

1. LOCAL-REMOTE to LOCAL
2. Depress MASTER CLEAR
3. READ-WRITE to READ
4. N-REGISTER SET to 2
5. RECYCLE "ON
6. ERROR STOP "ON" if a stop on error is desired
7. KEY SEGMENT "OFF"
8. Depress MAINTENANCE START

Write zeros in ten sequential segments beginning at a desired segment address.

1. LOCAL-REMOTE to LOCAL
2. Depress MASTER CLEAR

3. Set desired address in A register indicator-switches
4. READ-WRITE to WRITE
5. N-REGISTER SET to 10
6. RECYCLE "ON"
7. KEY SEGMENT OFF
8. Depress MAINTENANCE START

6.8 COMPONENT LOCATIONS

1. MAINTENANCE PANEL - COMPONENT LOCATOR - Figure 6.8-1.

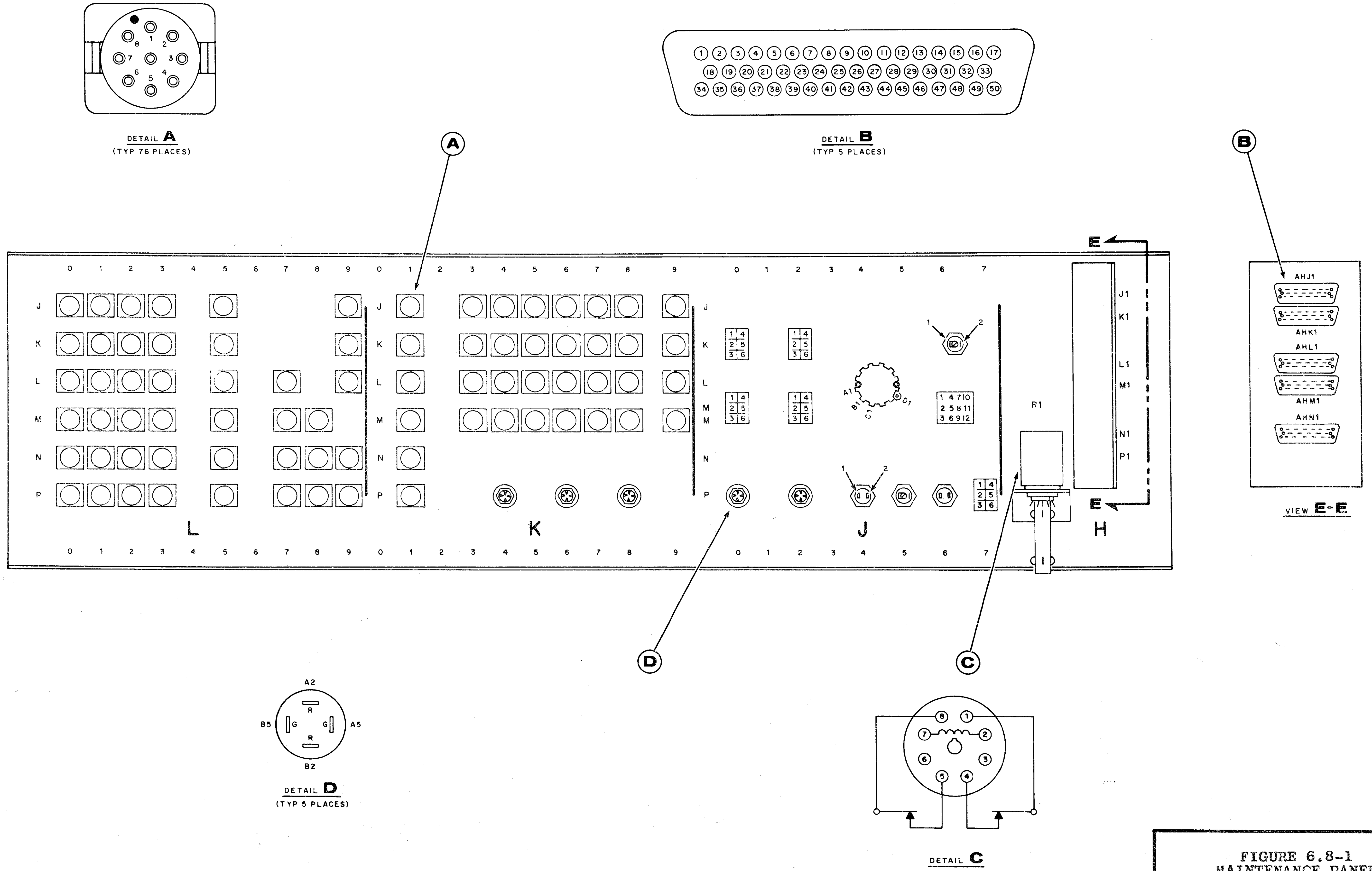


FIGURE 6.8-1
MAINTENANCE PANEL
COMPONENT LOCATOR

6.9 SIGNALS AND TEST POINTS

The following is a list of signals with test point locations. The listing includes input levels as monitored at the output of the input switches, output levels as monitored at the last output switch or driver and internal levels as monitored at the outputs of Flip-Flops, Multi's, Delays, etc.

INPUT LEVELS FROM DATA PROCESSOR

Level	Test Point
FW1S	ACA1D2
FW2S	ACA1H4
FW4S	ACA1J0
FW8S	ACA2C9
FWAS	ACA1C4
FWBS	ACA1C0
FWPS	ACA2C5
FBIS/	ACA1R4
FASS/	ACA2D7
FDTS	AAC4C9
FWRS	ACA2J5
SIDS	ACA1R0

OUTPUT LEVELS TO DATA PROCESSOR

Level	Test Point
FRPS	ACA5V9
FWCS/	AAD5V9
FCRL/	AAB0C4
FCLD	ACB3H5
FSRD/	AAD7P7
FCBS/	AAD5W5
FERS/	AAD5R5
FWLS/	AAD6J5
FIND/	AAD7V5
FR1S	ACA3W5
FR2S	ACA3V8
FR4S	ACA4J5
FR8S	ACA4H8
FRAS	ACA2W5
FRBS	ACA2V8

INPUT LEVELS FROM EXCHANGE

Level	Test Point
SR1S/	ACB2R5
SR2S/	ACB2S7
SR4S/	ACB2V9
SR8S/	ACB2W5
SRAS/	ACB1R4
SRBS/	ACB2R9
CS1S	ACB1H4
CS2S	ACB1J0
SCLS/	AAC5D2
SURS	ACA1V4
SARS	ACB1W0

OUTPUT LEVELS TO EXCHANGE

Level	Test Point
T01D	ACB3P7
T02D	ACB3V5
T04D	ACB5P7
T08D	ACB7P2
T10D	ACB9V5
T20D	ADB1V4
T40D	ACB5V5
Z01D	ACB3V9
Z02D	ACB5V9
D01D	ACB7V0
D02D	ACB9V9
D04D	ADB1P2
D08D	ACB9P7
D16D	ADB1V0

INPUT LEVELS FROM EXCHANGE (cont.)

Level	Test Point
SWLS/	ACB1S2
DACL	ABD0T1
IDXM	AAC7W5
WØMD	ACB3B7

OUTPUT LEVELS TO EXCHANGE (cont.)

Level	Test Point
SW1S	ACA7R0
SW2S	ACA7S2
SW4S	ACA7S7
SW8S	ACA7V9
SWAS	ACA7R5
SWBS	ACA7R9
A71F	AAB1U4
A72F	AAB1F4
A74F	AAA1U4
A78F	AAA1F4
DFSD	ACB7V4
SWRS	ACA7R4
SCØD	ACA9H5
ØTRD/	ACA9H9

INTERNAL LEVELS

Level	Test Point
ABED/	AAA7B7
ADSD	AAC1B7
BBSD	AAB7B7
CCLD	AAC6B2
CCLNP	AAC7A2
DCPM	AAC6U0
FCØS	ACA6J5
IDLD	AAD0H4
IPES	ABB4S2
LPES	ABC2D7
LØCS	AAA0C9
MASP	AAC5S9
NCLS	AAC4C5
ØPCD	AAD0B2
RECS	AAD6C5
REMS	AAA0C5
SFWD	AAB7H9
SSRD	AAA7H5