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	CHIO MULTIPLEXER SPECIFICATION	NCHIO/S-17 .1

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ABSTRACT and CONTENTS

This document is a replacement of CHIOM/S-1 "Phase I CHIO Interface Specification", which is obsolete. This document describes the hardware, operation, and programming conventions for use with the BCC CHIO multiplexer.

CONTENTS

PREFACE

As of this date, the specifications of the data concentrator and of the Phase II CHIO have not been completed. The Phase I CHIO will operate with a multiplexer consisting of 16 low-speed lines, two 2400-baud lines, and a high-speed line connected to the IBM Model 30. The specification of the Phase I multiplexers capability in handling the first two types of lines is given in this document. The Model 30 interface specifications are not yet available.

The Phase II CHIO will use a multiplexer which will handle at least 64 lines at 2400, 4800, or 9600-baud (the latter speed not being used initially). Whether or not the Phase II CHIO will handle some low-speed lines, has not yet been decided.

The specification of the data concentrator will not be available for several weeks.

I. Introduction

Because of the standardization requirements placed on the I/O system, special functions, and branches in the BCC Microprocessor, the "Phase I" CHIO multiplexer is abolished. The multiplexer described herein will be initially constructed to accept 16 local teletypes and a small number of high speed (2400 or 4800 band) serial synchronous modems, but it is capable of being expanded to service up to 64 high speed lines and an undefined but large (>100) number of teletypes. Expansion requires no changes to pre-existing hardware.

It is expected that the first few data concentrators will be built using this multiplexer with the only differences between the CHIO and the concentrator being:

1) The CHIO has a large number of high speed lines and a small number of local teletypes. The concentrator will have a small number of high speed lines (probably only two), and a large number of local low speed I/O lines.
2) The concentrator will be able to exercise full control over 103A data sets connected to it via a (as yet unspecified) controller. The CHIO does not have this facility, although it could be added if necessary.
3) The concentrator will have a smaller local core memory than the CHIO, probably 1K or 2K x 8 or 16 bits. The memory will probably be 1.5 μsec instead of 1 μsec cycle time.

4) The concentrator may operate at a clock rate of 5 mhz rather than 10 mhz. This would allow the microprocessor to be implemented with standard T^2L rather than with "H" series logic, with some cost reduction.

II. Local Teletypes (and other low speed devices)

Local teletypes will be bit scanned for input by the CHIO. The 16 input lines are grouped into 1 logical device, with multiplexer device address 4B7+1. When the CHIO does an ALERT-PIN on device 4B7+1, it will be presented with a 16 bit word on the E2 bus. Each bit of this word corresponds to the current state of an input line with a ONE on E2 corresponding to a MARK on the input line. Similarly, when the CHIO does an ALERT-POT to device 4B7+1, the low order 16 bits of Z will be loaded into a set of latches which will drive the local TTY printers. A ONE in Z corresponds to a mark on the line. There will be no provision for controlling 103A data sets. If it is desired to operate the system with 103's they will be placed in 'automatic answer' mode. The cards in the multiplexer will be electrically compatible with both 103's and with teletypes.

The instruction sequence to do output to the local teletypes is:

device address → Z, ALERT

output word → Z, POT

The instruction sequence for input is:

device address → Z, ALERT

TE2Y, Y → internal register, VCY, PIN

The device address has the following format:

BIT	MEANING
Ø	1 to specify I/O equipment
1	1 for input, Ø for output
2-16	not interpreted
17-23	1

The device address decoding in the I/o multiplexer interprets only the sign bit and bits 17-23. Devices with addresses <Ø are either teletypes or modems. Addresses with the sign bit off are reserved for other (as yet undefined) I/o gadgetry.

When the CHIO executes an ALERT with a word in Z which has bit 1 set, it must follow this ALERT with a PIN. Likewise, if Z(1) = Ø when an ALERT is executed, a POT must follow.

The data word has the following format:

BIT	MEANING if device 4B7+1 is addressed
0-7	NOT USED
8	LINE Ø
9	LINE 1
10	LINE 2
.	.
.	.
.	.
23	LINE 17B

III. High Speed Modems

The high speed modems are each separate logical devices, with unique device addresses between 4B7+100B and 4B7+200B. Each modem has associated with it a serial-to-parallel converter for input, and a parallel-to-serial converter for output. These line receivers and transmitters exchange 8 bit parallel characters with the CHIO. Each receiver and transmitter has a one character buffer to reduce the servicing speed required of the CHIO. The receiver and transmitters are 8 bit serial synchronous devices. The clocks for serialization and deserialization are generated by the modem.

A block diagram of the receiver is shown in Figure 1. The bit counter counts to 8 as data is being shifted into the shift register. When 8 bits have been gathered, they are transferred in parallel to the buffer. The buffer full indicator is set when the buffer is loaded, unless the CHIO is reading the buffer at the same time it is being loaded. The rate error indicator is set if the buffer is loaded while the full indicator is set, unless the CHIO is reading the buffer simultaneously.

The receiver achieves initial synchronization (and

resynchronization in case of an error) by receiving two or more ASCII NULL characters followed by a SYNC character from the sending end of the data path. When the receiver detects 16 or more contiguous zeros on the line, the bit counter is stopped until a 'one' is encountered on the input line. The sending end will be expected to follow a group of null characters with an ASCII 'sync' character. When the receiver sees a '1' after receiving a group of nulls, it interprets it as the first 'one' bit of a sync character, and goes back to normal mode. If it is not a sync, the CHIO should notify the sending end to attempt resynchronization again.

A block diagram of a typical transmitter is shown in Figure 2. The shift register is loaded from the parallel buffer when the bit counter = 7. The empty flag on the buffer is simultaneously set to 1, and a request is made to the CHIO for a new character. If the CHIO has not loaded the buffer by the time the bit counter has reached 7, an ASCII 'SYNC' character will be loaded into the shift register and transmitted. At the same time, the rate error flag will be set. A rate error in transmission is not serious, but is provided to give the CHIO information concerning its own efficiency.

The receiver and transmitter for a given modem constitute a single logical device with a unique address. When the CHIO does a PIN for a given line, it will receive the following input word on the E2 bus:

BIT	MEANING	
0-8	Not used (=Ø)	
9	Carrier detector	Signals generated by the modem
10	Clear to send	
11	Data set ready	
12	Transmitter ready to send a new character	
13	Transmitter rate error	
14	Receiver request to deliver a character	
15	Receiver rate error	
16-23	The input character from the receiver parallel buffer	

The carrier detector, clear to send, and data set ready bits are status signals generated by the modem. For their significance, see the modem specification (Appendix 1)

The 'transmitter ready' bit is the full/empty indicator on the transmitter's parallel buffer. It is reset when the CHIO executes an ALERT-POT directed to the transmitter. The transmitter rate error bit is also reset when the transmitter buffer is loaded. The receiver request is the full/empty indicator on the receiver's parallel buffer. Both this bit and the receiver rate error bit are reset when the CHIO executes a PIN for the device's input word, providing that bit 16 in the ALERT word (the device address) is set.

The output word for a line consists of the character for transmission and a number of control bits for the modem, the receiver, and the transmitter. Its format is:

BIT	MEANING
0-9	Not interpreted
10	Request to send
11	Not interpreted
12	Transmit character in bits 16-23, reset transmitter request, reset transmitter rate error
13	Transmitter ON
14	Receiver ON
15	COPY Z(10), Z(13), and Z(14) into the indicated bits
16-23	The output character

Z(10), Z(13), and Z(14) are copied into latches in the modem interface only if bit 15 is set in the output word sent on a POT. If bit 15 is off, the latches are not modified. Beware! Initialization is required. When the receiver is off, it will continue to receive characters, but will refrain from making requests to the CHIO. As a result, there will be an immediate rate error. The receiver will discard characters until it is again enabled, at which time it will make an immediate request for service to the CHIO (with the rate error bit set). When a transmitter is off, it sends ASCII null characters to the modem. If a receiver with characteristics similar to the local receiver is at the far end of the line (i.e., a data concentrator) it will interpret these nulls as an attempt at resynchronization. As soon as the transmitter is enabled, it will make a request to the

CHIO. If the first character the CHIO sends is a SYNC, instant synchronization will have been achieved. When the CHIO executes a POT to turn the transmitter off, it should not send a character for transmission at the same time.

The instruction sequence to be executed by the CHIO to read the input word from a line is:

```
device address -> Z, ALERT;
TE2Y, Y --> internal register, VCY, PIN;
```

To do output on a line, the CHIO should execute:

```
device address -> Z, ALERT;
data -> Z, POT;
```

The format of the device address is as follows:

BIT	MEANING
Ø	1 to specify I/O hardware
1	1 for input, Ø for output
2-15	Not interpreted
16	If this bit is on and bit 1 is on, the receiver flag and receiver rate error bits are cleared
17-23	Line number (100B $\leq$ L.N $<$ 200B)

The purpose of bit 16 is to allow the CHIO to read the input word from a device without modifying the flags.

The request bits for all the receivers and transmitters in the system are continuously being examined by a scanner which runs at 5mhz. Line requests are divided into two priority groups. High priority requests are receiver requests for which the receiver buffer is full and the incoming character has more than 4 bits in the shift register. Low priority requests include all transmitter requests and receiver requests for devices which have less than four bits of the next character in the shift register. If there are no high priority requests pending from any device, the scanner runs until it finds the first low priority request, stops, and sends an ATTENTION 2 pulse to the CHIO. If there are any high priority requests pending, the scanner will only stop on high priority requests. When the scanner stops on a high priority request, it sets attention latches 2 and 3 in the CHIO. The CHIO will be expected to do a PIN for device 4B7+10B. This device is a status word which will govern the further actions of the CHIO. The scanner is restarted as soon as the PIN is done for the status word; if the CHIO hasn't serviced the line by the next time the scanner examines it ($\approx$13μsec. later), another request will be sent for the same line. To read the status register after receipt of an ATTENTION 2 or ATTENTION 3, the CHIO should execute:

6B7+10B ⟶ Z, ALERT;

TE2Y, Y ⟶ internal CHIO register, VYC, PIN;

The word it will receive on E2 has the following format:

BIT	MEANING
Ø-13	Not used (=Ø)
14	Error
15	Receiver request
16	Transmitter request
17-23	The line number of the line that initiated the attention (100B $\leq$ L.N. $<$ 200B) (The line number is taken from the scanner position counter.)

Reading the status word does not change any of the bits associated with a line, but only restarts the scanner. This is the only way in which the scanner will be restarted if it is stopped, so the initialization routine should read the status word at least once. A POT directed to device 4B7+10B is illegal, as are all POTs following ALERTs to devices whose addresses have bit 1 set. The receiver request and transmitter request bits are copies of the bits in the input word of the device pointed to by the line number. Error is a bit which specifies that something is amiss with the receiver or transmitter. If this bit is set, the CHIO should examine the input word for the device to find the problem. Error will be set:

1) If the request is a transmitter request and 'data set ready' is off,
2) If the request is a transmitter request and the transmitter rate error bit is set,

3) If the request is a transmitter request and "clear to send" is off,

4) If the request is a receiver request and the receiver rate error bit is set,

5) If the request is a receiver request and the 'data carrier detector' signal is off.

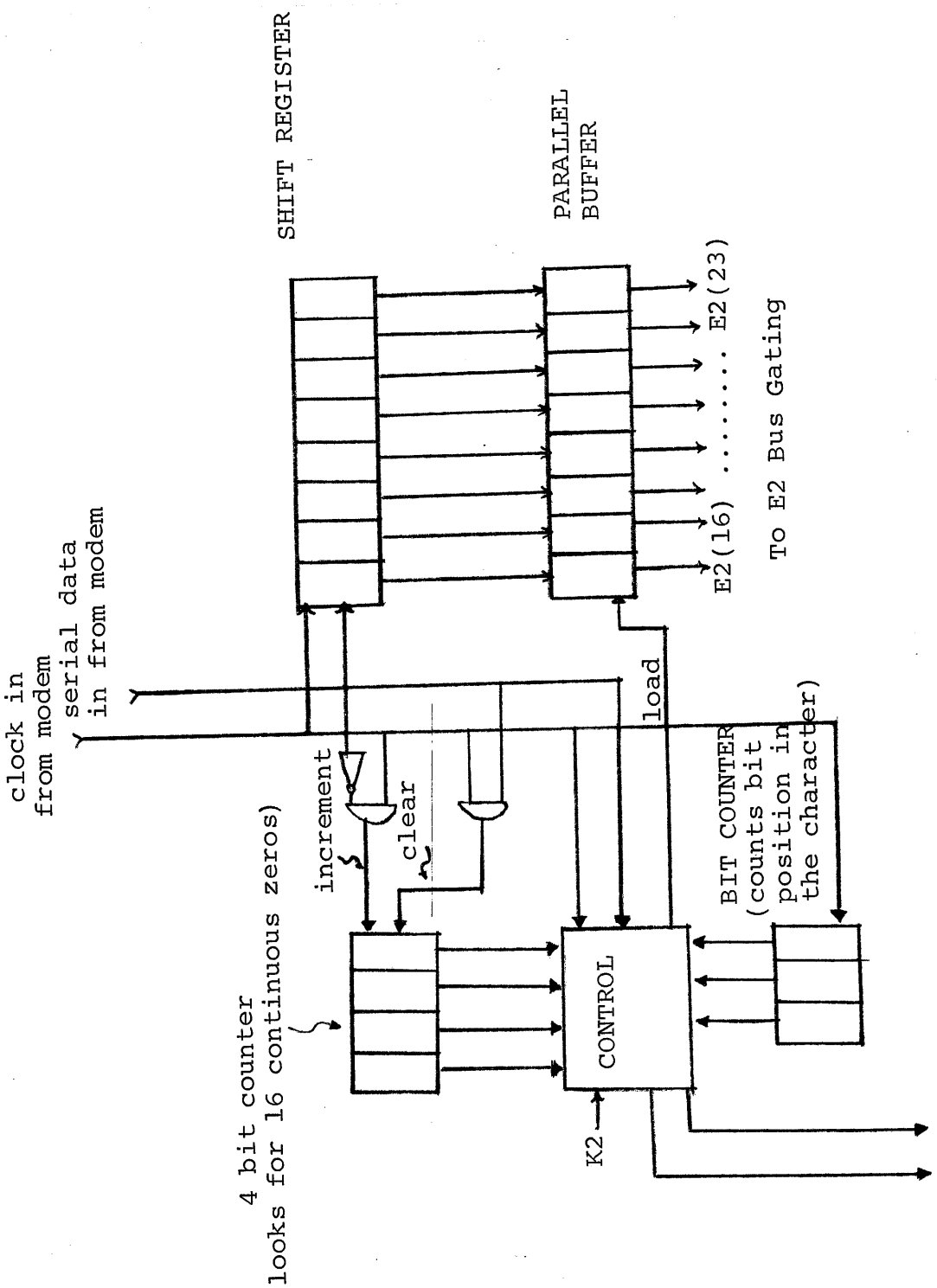


Fig. I RECEIVER

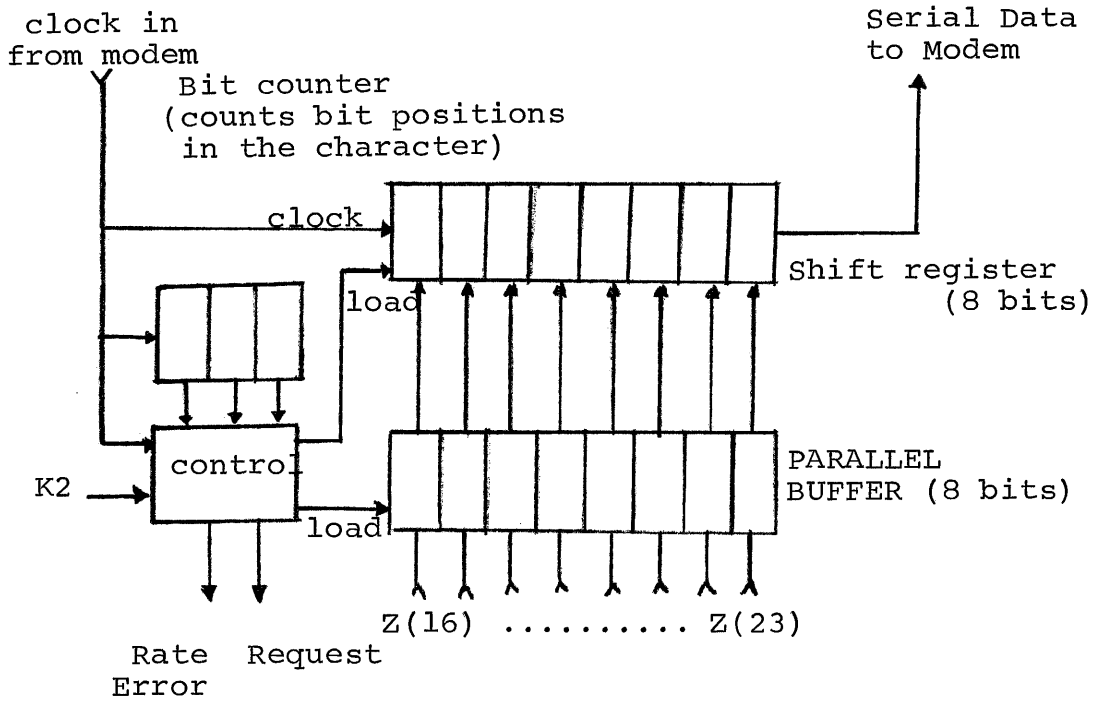


Fig. 2 TRANSMITTER

APPENDIX I

Modem Specifications

Technical Summary

DATA RATE
Fixed at .....4800 bits per second

MODULATION
In the modulator, serial data is encoded three bits at a time to produce an eight-phase line signal. This signal is filtered prior to entering the voice frequency link by a narrow band filter. In the demodulator, the voice frequency signal is also filtered by a narrow band filter and the phase shifted signal is detected and decoded. The decoded digital data is serially shifted out of the demodulator by the data derived internal clock.

OPERATING MODES
Full duplex or simplex, half-duplex optional.

LINE REQUIREMENTS
Modem 4400/48 is designed to operate over typical unconditioned telephone lines* Type 3002, (Tariff FCC260) or other unconditioned voice frequency channels including submarine cable, microwave UHF, coaxial cable, etc. Line conditioning to grades C1, C2, or C4 has no significant effect on the performance of Modem 4400/48.

EQUALIZER
Fixed and simplified variable equalizers are provided in standard unit. The fixed equalizer complements amplitude and envelope distortions of the average unconditioned voice frequency channel.* Variable equalizer allows fine adjustments to optimize performance.

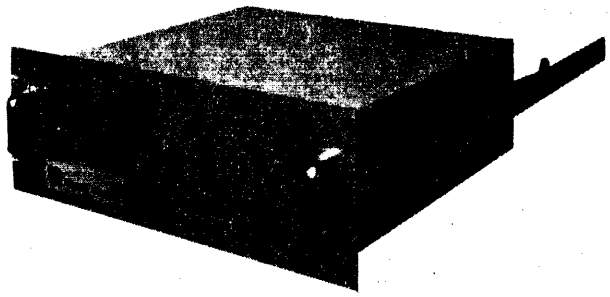
INTERFACE
EIA RS232B and CCITT V.24 is standard (See details in I/O connector chart). MIL-STD-188B, and special interfaces are available as options.

PRIMARY POWER
Nominal AC input either 105-125 or 210-250 vac, 45-65 cps, single phase, approx. 60 watts. Power connector cable with twist lock connector to modem and 3 pin U.S. type plug for primary power connection is supplied with modem.

OPERATING ENVIRONMENT
Ambient Temperature 0° to +55°C
Relative Humidity (max) 95%
Altitude .....10,000 feet

SIZE AND WEIGHT

	In Cabinet	In Rack
Height	6½ inches	7 inches
Width	18 inches	19 inches
Depth	18⅝"	17½"
Weight	46 lbs.	56 lbs.



Modem 4400 for rack mounting.

Transmitter

DATA INPUT

Format	Serial Binary Data
Amplitude	EIA Standard, ±3V to ±25V (+) = "0", (−) = "1"
Input Lines	Single wire, ground return
Input Load	5600 ohms, ±10%
Flexibility	For special interface adaptability, an additional circuit board connector is available.

OUTPUT TO LINE

Output Signal	Differentially phase shifted 1700 Hz carrier, 8 phase.
Frequency Spectrum	900 to 2500 Hz
*Output Level	Adjustable, −16 to +4 dbm (−19 to +1 dbm for certain European countries)
Output Impedance	600 ohms, balanced

CLOCK

Waveform	Squarewave, negative-going edges coincide with the center of the data bits. Positive-going edges coincide with change of input data.
Frequency	For External Use, 4800 ±0.0005% Hz From External Source 4800±0.0005% Hz

Amplitude

For external use	±6 volts from approx. 330 ohm source
From external source	EIA Standard, ±3V to ±25V, into 5600 ±10% ohms

Receiver

DATA OUTPUT

Format	Serial Binary Data
Amplitude	±6V EIA Standard +6V = "0", −6V = "1"
Output Line	Single wire, ground return
Output Impedance	Approx. 330 ohms
Flexibility	For special interface adaptability, an additional circuit board connector is available.

INPUT FROM LINE

Input Signal	Differentially phase shifted 1700 Hz carrier, 8 phase
Frequency Spectrum	900 to 2500 Hz
Input Level	+5 to −55 dbm
AGC Dynamic Range	30 db. Strapping adjustment allows 30 db dynamic range within the limits specified.
Input Impedance	600 ohms, balanced

CLOCK

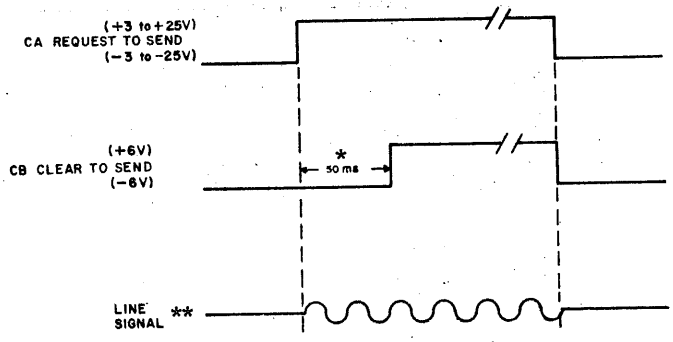
Waveform	Squarewave, negative-going edges coincide with the center of data bits. Positive-going edges coincide with change of output data. Derived from received line signal.
Frequency	Equal to the data bit rate and synchronized with the transmitter clock.

Amplitude

For external use	±6 volts from approx. 330 ohm source

*For most European countries, a special V.F. transformer is used, reducing output to line to a maximum of 0 dbm.

Transmitter Control Signals



*Is reduced to 12 ms if New Sync. feature used.

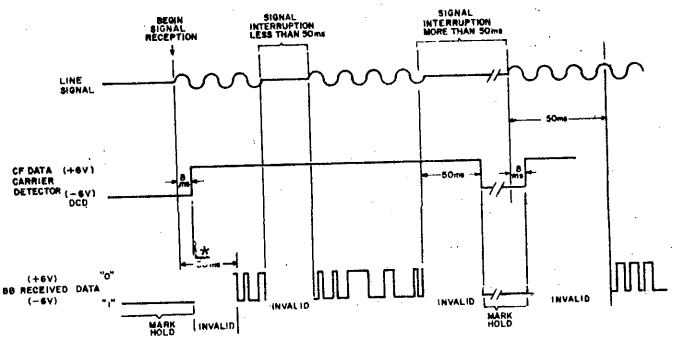
**As shown, line signal follows RTS. It may also be programmed to be independent of RTS and remain on continuously (except with New Sync).

CA — Request to Send — is received by modem

CB — Clear to Send — is generated by modem

Receiver Control Signals

Relation of Data Carrier Detector (CF), (BB) Data, and Line Signal



CF — Data Carrier Detector — is generated by modem

*Receiver clock synchronization time. Reduced to 12 ms. when New Sync. feature used.

Input / Output Connections

Connector Pin	CCITTV-24 Designation	RS232B Designation	Lead	Description
1	1	AA	Protective Ground	This lead is an electrical equipment frame and a-c power ground.
2	3	BA	Transmitted Data	This lead contains the signals that originate in the terminal equipment and are to be transmitted by the data modem to a distant station. An input to the modem.
3	4	BB	Received Data	This lead contains the signals that are generated by the data modem in response to signals from a distant station. An output from the modem.
4	5	CA	Request to Send	An "on" condition on this lead indicates that the data terminal equipment is ready to transmit data. An input to the modem.
5	6	CB	Clear to Send	An "on" condition on this lead indicates that the data modem is ready to transmit data from the data terminal equipment to a distant terminal. An output from the modem.
6	7	CC	Data Set Ready	An "on" condition on this lead indicates that the power to the data modem is on, that the modem is not in the Test mode, and that the modem is ready to process data. An output from the modem.
7	2	AB	Signal Ground	This lead establishes the common ground reference potential for all circuits except protective ground.
8	9	CF	Data Carrier Detector	This lead provides an indication that data carrier signals from the remote station are being received. Optionally, this lead may reepond to data carrier signals from the local transmitter. An output from the modem.
9	—	—	Data Modem Testing	+12 Volts
10	—	—	Data Modem Testing	−12 Volts
11	—	—	—	—
12	—	—	—	—
13	—	—	—	—
14	—	—	New Sync	This lead is provided for use at the receiving station, for multi-party operation, so the customer may effect a more rapid transition in synchronization between messages. An input to the modem.
15	14	DB	Transmitted Signal Element	Signals on this circuit are used to provide the data terminal equipment with signal element timing information. An output from the modem. Not used with DA.
16	—	—	—	—
17	15	DD	Receiver Signal Element Timing	Signals on this circuit are used to provide the data terminal equipment with signal element timing information. An output from the modem.
18	—	—	—	Spare
19	—	—	—	Spare
20	—	—	—	Spare
21	—	CG	Data Modulation Detector	An "on" condition on this lead is an indication that the receiver signal element timing is synchronized with the transmit signal element timing at the distant terminal. An output from the modem.
22	—	—	—	—
23	—	—	—	Spare
24	13	DA	Transmitter Signal Element Timing	Signals on this circuit are used to provide the transmitting modem with signal element timing information. An input to the modem. Not used with DB.
25	—	—	—	Spare

Connector described above mates with customer provided Cinch or Cannon DB-19604-432 plus a DB-51226-1 hood (Cinch only), or equivalent, connector to the EDP equipment. VF line connections are made to a terminal strip with 1 & 2 Transmit, 3 & 4 Receive, 5 Signal Ground and 6 Chassis Ground. Three wire power cord furnished with modem.