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ABSTRACT and CONTENTS

This document describes the functional characteristics and implementation of the BCC microprocessor for operation with read only memory larger than 1024_{10} words.

The memory in the expanded microprocessor is divided into two areas, referred to below as bank A and bank B. There is no area of memory common to the two banks.

The extra hardware required to implement a microprocessor of greater than 1024_{10} words consists of:

1) a new I Register card which will accept input from 32 ROM cards instead of 16, and drive 32 XS and YS lines from the 0 Register outputs.
2) a flip flop which is set and cleared by two special conditions. This flip flop will select the bank of ROM's to be accessed by gating the clock to the appropriate section of the I Register.
3) a flip flop to store the state of the bank select flip flop. This flip flop will allow subroutines to return automatically to the bank from which they were called.

The BSELECT flip is essentially an 11th bit of the 0 Register, with the exception that it is not incremented over the bank boundary. When a normal branch occurs, BSELECT is:

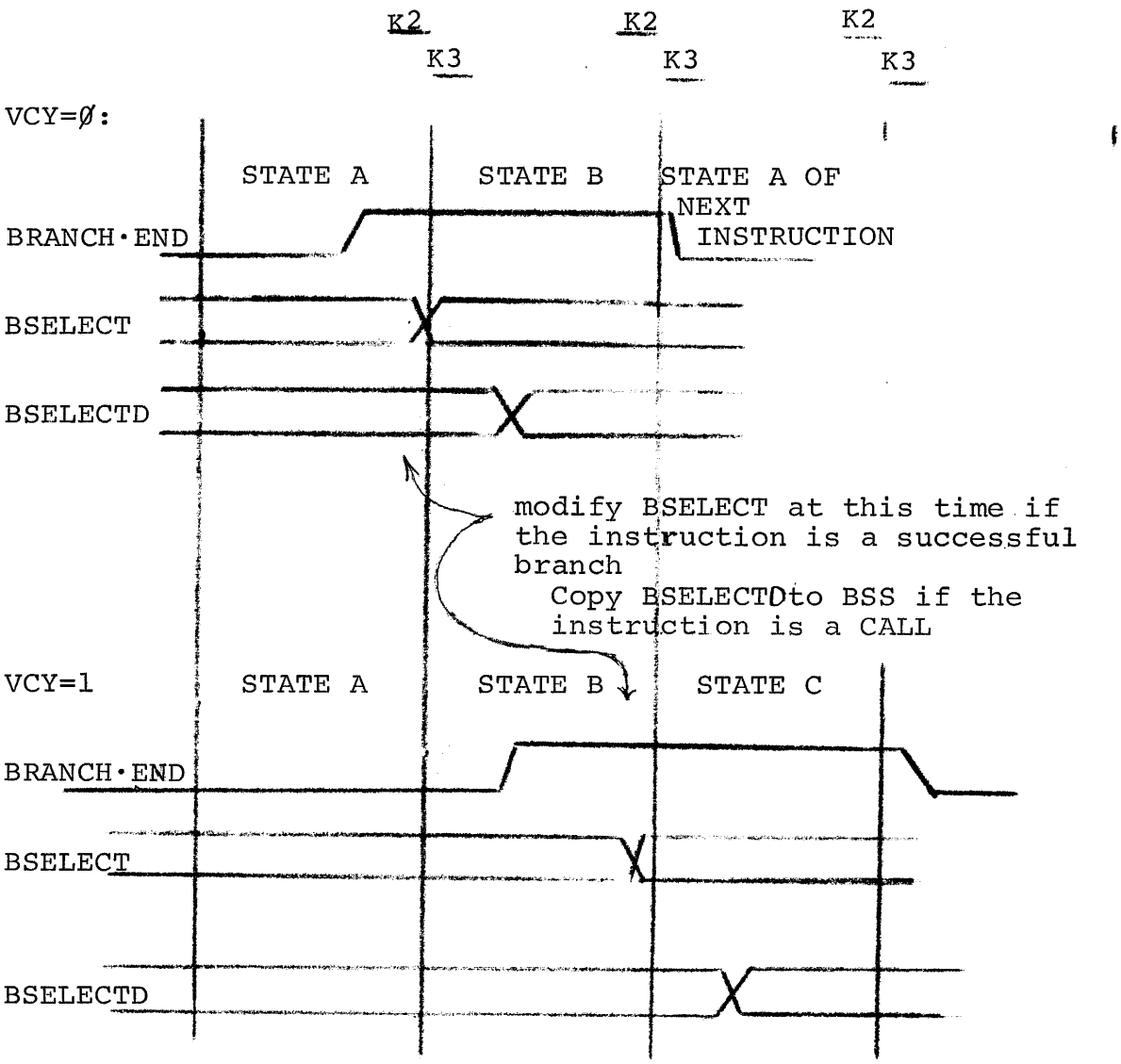
1) Set if the SELECT B special condition is executed
2) Cleared if the SELECT A special condition is executed
3) Not changed if neither special condition is

executed.

The BSELECT flip flop is loaded at the same time 0 is normally loaded from the B field of the micro-instruction. When the microprocessor initialized, BSELECT will be returned to 0 (Bank A).

The BSS (bank select saved) flip flop is loaded from the BSELECT flip flop whenever a CALL is executed and it succeeds. When a RETURN is executed, the BSELECT flip flop is loaded from BSS at the same time 0 is loaded from OS. The BSS flip flop will be read onto bit 13 of the Y bus whenever TOSY is executed. When a computed go-to is executed (GO TO X), the bank select flip flop will be loaded from bit 13 of the X bus (in a manner analogous to the loading of OS).

Timing of BSELECT and BSS



Instruction Sequencing:

The instructions:

A77			
A100	GO TO 302; SELECTB	B300	CALL 103; SELECTA
A101	DGO TO 300; SELECTB	B301	GO TO 104; SELECTA
A102		B302	GO TO 101; SELECTA
A103	RETURN	B303	
A104		B304	

result in the following execution sequence.

A77, A100, B302, A101, A102, B300, A103, B301, A104

Implementation:

The control logic card generates the following signals in the polarities shown.

END	TBO'
K2	
K2'	
TXO'	
TOSO'	
LOAD OSREG'	

The control logic card requires BSELECT' to generate the correct clocks for the I Register.

All remaining logic should be implemented on the special function card.

SET AND CLEAR TERMS FOR BSELECT AND BSS

SET BSELECT

Special Condition

= $\overbrace{\text{SET BANK B}}\cdot TBO \cdot K2$

+ BSS·TOSO·K2

+ X(13)·TXO·K2

CLEAR BSELECT = SET BANK A·TBO·K2

+ BSS'·TOSO·K2

+ X(13)'·TXO·K2

+ RESET BSELECT

Set BSS = BSELECTd·LOAD OSREG

Clear BSS = BSELECTd'·LOAD OSREG