

B O L T B E R A N E K A N D N E W M A N I N C

C O N S U L T I N G • D E V E L O P M E N T • R E S E A R C H

Manual for the IMP-10 Special Interface
to the Interface Message Processor
and the ARPA Computer Network

October 1973

Computer Systems Division
Bolt Beranek and Newman Inc.
50 Moulton Street
Cambridge, Massachusetts 02138

IMP INTERFACE (NEW 12/73)

BOOK 1 of 1

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1. INTRODUCTION

The ARPA Network is being constructed to provide a capability for geographically-separated Host computers to communicate with each other. However, Host computers generally differ from one another in manufacturer, type, size, speed, word length, operating systems, etc. To allow these different computers to communicate, each Host is connected into the network through an Interface Message Processor (IMP) located on the Host premises. The complete network is formed by interconnecting these IMPs through wideband communication lines (initially 50 kilobits/sec) supplied by the telephone company. Each IMP is then programmed to store and forward messages to the neighboring IMPs in the network. During a typical operation, a Host passes a message to its IMP. This message is then passed from IMP to IMP through the network until it finally arrives at the destination IMP, which passes the message to the destination Host.*

The interconnection of a Host and an IMP is a joint effort that requires the Host personnel to provide interfacing hardware and software. Bolt Beranek and Newman Inc. (BBN) has built a special interface to connect the IMP to a Digital Equipment Corp. PDP-10 Host computer. This report describes the design, installation, and operation of such a special interface.

Appendix A to this report reproduces Section 4 of the BBN Report No. 1822, "Specifications for the Interconnection of a Host and an IMP", which discusses the hardware requirements for the special Host/IMP interface unit and describes the standard

*The initial IMP design is described in Bolt Beranek and Newman Inc. Report No. 1763 (January 1969), AD-682-905. The specifications for IMP-Host interconnection are described in BBN Report No. 1822 (February 1970).

Host/IMP interface unit in the IMP.

Appendix B contains the device code and jumpering for specific installations.

Appendix C contains miscellaneous specific details of the hardware, including drawings of the display panel circuitry.

2. INSTALLATION

The interface will normally connect to an IMP that is no more than 30 feet from the interface. A special Distant Host option is required if the IMP is between 30 and 2000 feet from the interface. This option includes special cable drivers and receivers required to deal with the Distant Host version of the standard interface on the IMP itself.

The IMP-1Ø interface deals with the PDP-10 I/O BUS exclusively. The interface is built out of DEC R, B, and W-series modules, mounted in two Type 1943 mounting panels. A Type 728 power supply is supplied, together with a Type 844 power control for protecting the I/O BUS circuits during power turn-on and turn-off. The circuit breaker and power switch on the back of the 844 control power to the interface.

The interface mounts in a PDP-1Ø rack, occupying 10-1/2 inches of front panel space for two baskets of logic cards, and 16 inches of back panel space for the 728 power supply and 844 power controller. The 5 1/4" display panel mounts at the front of the rack in the usual manner. Standard single-phase 115-volt power with a third-wire ground should be provided by the Host. The Host should also provide switched 115-volt power to drive the remote control relays in the 844.

The I/O BUS plugs into slots 25 through 28, and slots 29 through 32 of racks C and D, the lower basket. A type HØØ4 block is supplied for mounting the I/O BUS connectors.

The IMP cable plugs into slot D1, or, in the case of a distant Host, D1 and D2.

The device selection code is determined by jumpers on the W99Ø modules in slots D6 and D7. The jumpers should be placed as follows:

In order to effect the
device code in bit no. 3 4 5 6 7 8 9
then pin E J M E J M R
on the W99Ø in D6 D6 D6 D7 D7 D7 D7
should be connected
(to get a 0) to pin F K N F K N S
or (to get a 1) to pin D H L D H L P

For the specific jumpering used, see Appendix B.

3. INTERFACE OPERATION

To the program, the entire full duplex interface appears as a single device that has one DATAO (Data Out), one DATAI (Data In), and one CONO (Conditions Out), and one CONI (Conditions In) instruction. Three interrupts are employed — to indicate completion of an output word, completion of an input word, and completion of a message received from the IMP. These interrupts may be individually program-assigned to any of the seven interrupt channels. Thus, BLKO and BLKI instructions may reside in dedicated interrupt locations, or one interrupt routine may service two or all three interrupts, doing DATAO and DATAI instructions functions. (Figure 1 shows the I/O Bus connections.)

Communication from the PDP-10 to the IMP is started by a DATAO from the PDP-10. The interface will cause an interrupt on the "out" line to the PDP-10 on the 35th bit of each word. The PDP-10 may then respond either with an additional DATAO, which transmits the next word, or with a CONO, with the "END OUT" bit set (see Figure 2). In the latter case, the interface will transmit the last bit to the IMP, with the "last bit" indicator set, and then interrupt the PDP-10 again. The PDP-10 may now respond either with another DATAO, to start transmitting a new buffer to the IMP, or with a CONO with the "STOP OUT" bit set, which merely clears the interrupt. Input from the IMP to the PDP-10 will cause an interrupt on the IN line each time a complete word is available. Upon receipt of the "last bit" indicator from the IMP, the interface will pad with zeroes to the end of a PDP-10 word and then cause an interrupt, both on the IN line, to indicate a full word, and on the END IN line, to indicate end of message. Note that the IN interrupt should be honored first, to complete the message, before servicing

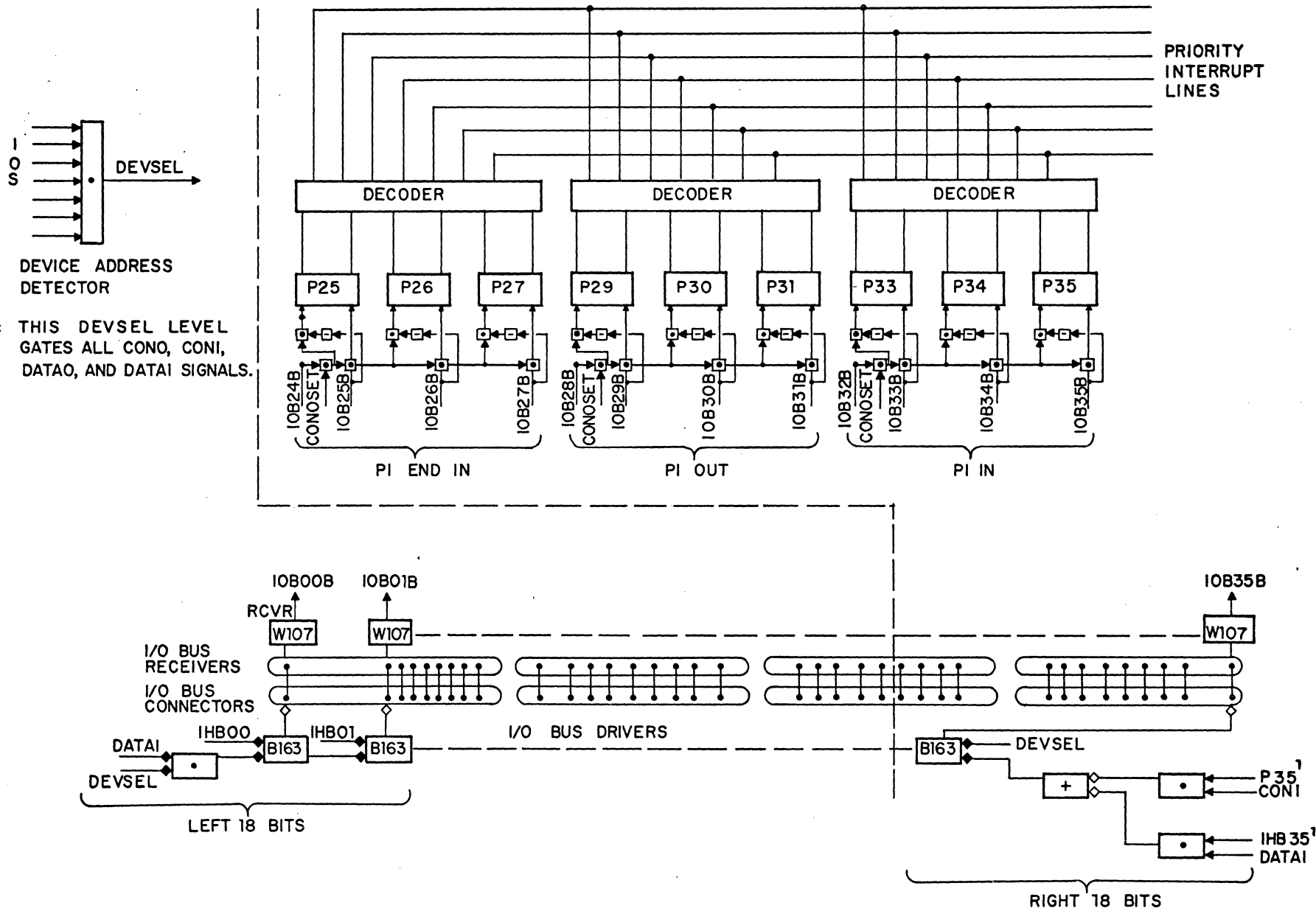
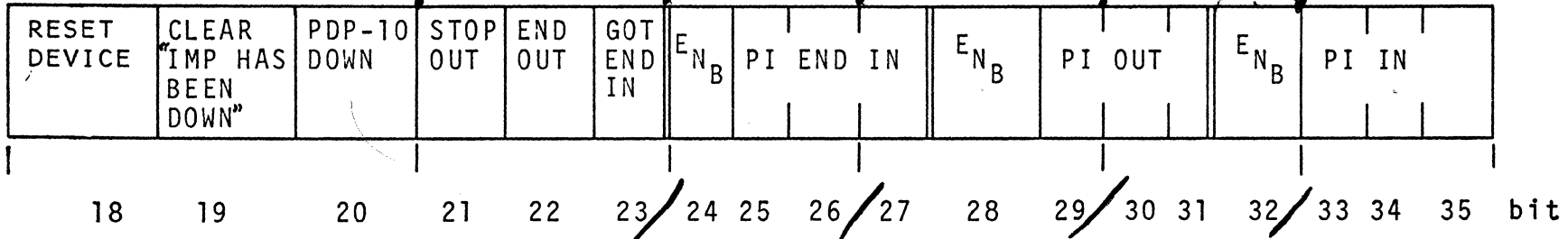


FIGURE 1 - I/O BUS CONNECTIONS

CONO FORMAT:



CONI FORMAT:

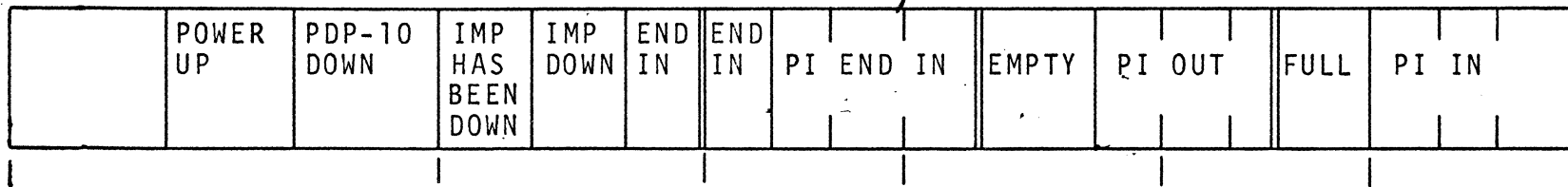


FIGURE 2 CONO AND CONI FORMATS

the completed buffer. However, the state of the END IN line should be tested before executing the DATAI or BLOCKI, if the two are being serviced at the same priority level, since a new word (the last) may have come in between the execution of the DATAI and the next instruction. If that instruction concludes that the word it just took was the last, a word will be lost.

3.1 Error Detection Logic

IMP failures are indicated by an opening of the IMP relay that connects the IMP Ready Test (ground) to the IMP Master Ready line in the Host/IMP cable (see Figure 3). The IMP Master Ready line provides a bit in the CONI word and any opening of the IMP's relay is captured in the IMP-Has-Been-Down flip-flop, which provides another bit in the CONI word. This bit is cleared by one bit of the CONO instruction. Thus, the PDP-10 program can at any time test the state of the IMP. In addition, an IN END interrupt will be generated whenever the IMP becomes not ready.

The PDP-10 has a corresponding relay which is controlled by a bit in the CONO word. If the CONO IMP is issued with this bit clear, the relay is closed. If this bit is set on the CONO, the relay will open, and the Host will appear unready. The relay is also opened by CROBAR from the 844, or by IOB Reset.

3.2 Operation of the Host-to-IMP Section

Figure 4 is a block diagram of the logic of the Host-to-IMP section. IOB reset presets the FIRST flip-flop to one. Upon receipt of the first DATAO from the PDP-10, the 36-bit shift register is loaded from the 36 data lines. The MARK bit, to the right of the shift register, is set to one. One microsecond later, the shift register is shifted left by one position and the left-most bit appears in the HSDTA flip-flop and on the Host

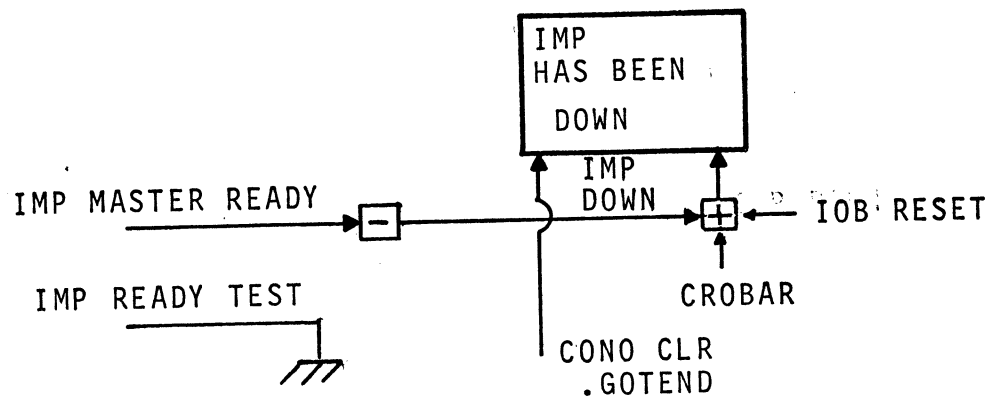
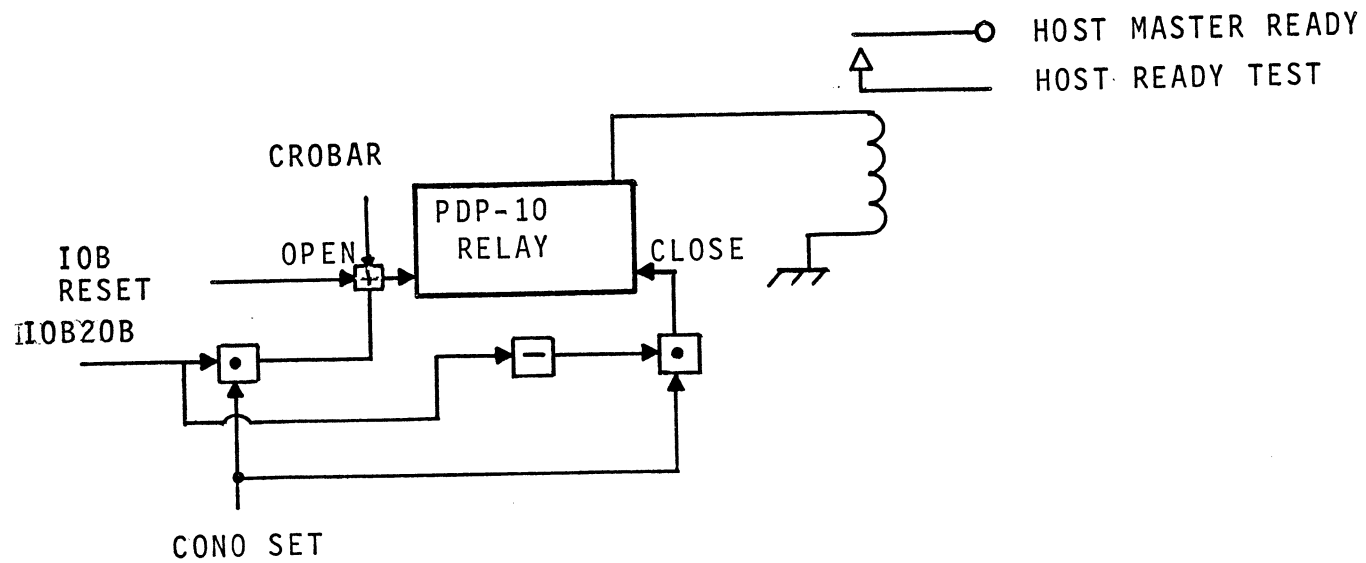


FIGURE 3 - ERROR DETECTION LOGIC

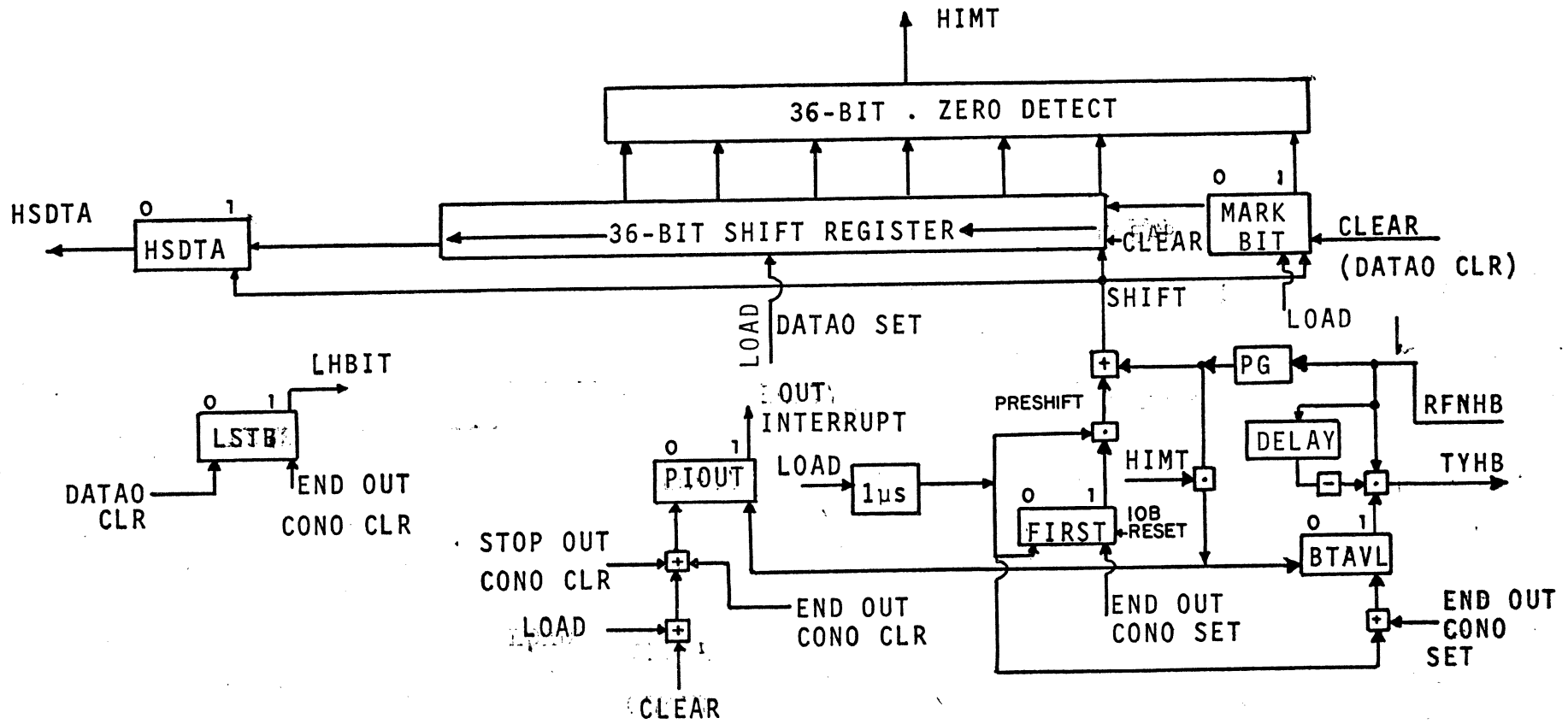


FIGURE 4 - HOST-TO-IMP LOGIC

Data Line. The FIRST flip-flop is cleared at this point and the Bit Available (BTAVL) flip-flop is set. At that time, if the IMP is holding the Ready-For-Next-Bit (RFNHB) line true (or shortly after the IMP brings this line true), the There's-Your-Host-Bit (TYHB) line is brought true. When the IMP indicates that it has taken the bit, by bringing the Ready-For-Next-Host-Bit line false, the pulse generator is fired, shifting the buffer one bit to the left. A short time later, the interface again becomes ready to give a bit to the IMP. On each shift, zeroes move into the right end of the register.

This process continues for 35 bits. When the IMP confirms taking the 35th bit, the interface shifts the 36th bit into HSDTA and turns on the PIOUT flip-flop which presents an OUT interrupt request to the PDP-10. It also clears the Bit Available flip-flop, so that the IMP will not be given the There's-Your-Host-Bit signal (for the 36th bit) until the program has given the interface more information.

To send more words to the interface, the PDP-10 does further DATAO's (or a BLKO, which looks like a DATAO to the interface). Note that the "preshift", one microsecond after the DATAO, does not occur on words other than the first, since the FIRST flip-flop is not set. The DATAO causes the data word to be loaded into the shift register, puts a one into the MARK bit and turns on BTAVL. This gives the IMP the last bit of the previous word (which has been held in the HSDTA flip-flop of the shift register), followed by the first 35 bits of the present word.

This process will continue until, after one of the interrupts, the PDP-10 informs the interface via CONO END OUT that the previous word was the last word of the message. At this point, the interface will raise the Last-Host-Bit line and pass the last bit of

the previous word to the IMP. The CONO END OUT also turns the FIRST flip-flop back on, so that the first DATAO of the next message will cause the "preshift" to occur.

When the IMP confirms receipt of the last bit, by bringing down the Ready-For-Next-Host-Bit line, the interface again interrupts the PDP-10. The PDP-10 may clear this interrupt either by a CONO STOP OUT, or by the first DATAO of a new buffer.

3.3 Operation of the IMP-to-Host Section

Figure 5 is a block diagram of the logic of the IMP-to-Host section. IOB reset sets the I'm-Ready-For-Next-Bit (IRFNB) flip-flop. Upon receipt of a bit from the IMP, as indicated by the There's-Your-IMP-Bit (TYIMB) line coming true, the INPUT shift register is shifted one position to the left. Successive TYIMB's have the same effect until MARK bit is shifted into the leftmost position, indicating that the buffer is full. This causes an interrupt request on the IN line, and also clears the IRFNB flip-flop, to prevent bringing up the Ready-For-Next IMP-Bit line until the word has been taken by the PDP-10.

The trailing edge of the DATAI instruction clears the buffer, sets the MARK bit, and raises the Ready-For-Next-IMP-Bit (RFNIB) line.

Upon receipt of the Last IMP bit indication, the interface clears the IRFNB flip-flop, to prevent bringing the Ready-For-Next IMP-Bit line true, and checks whether the input buffer is full. If it is full, an interrupt request is raised on the END IN line. If not, additional shift pulses are generated until the buffer is full. Note that the IMP Data line is gated off during this period by the falsity of the IRFNB flip-flop, thus forcing zeroes to be shifted into the buffer.

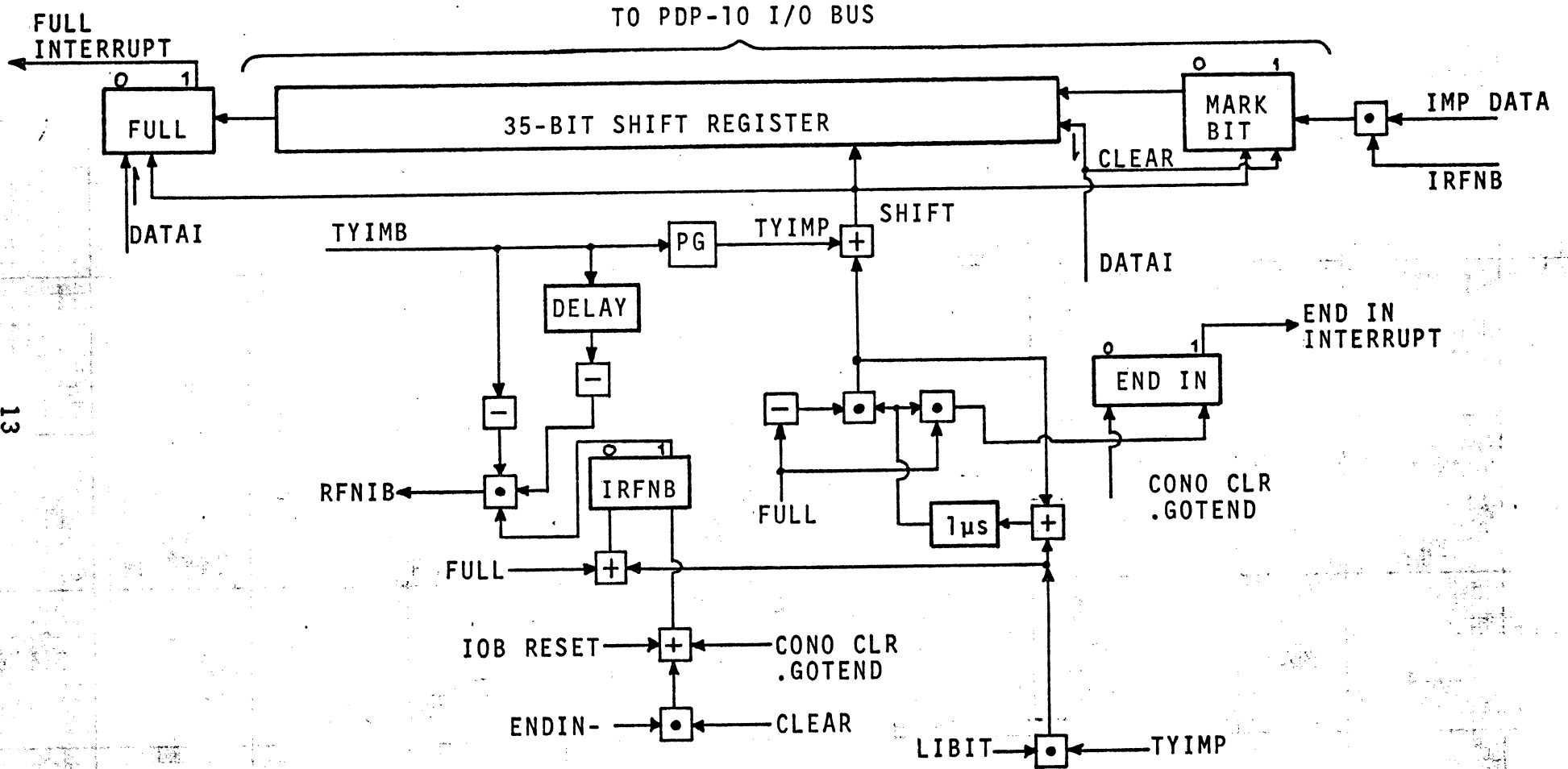


FIGURE 5 - IMP-TO-HOST LOGIC

4. LOGIC DRAWINGS

This section contains the following illustrations:

- Figure 6 — IMP Error Detection Logic
- Figure 7 — P1 OUT Channel Assignment
- Figure 8 — P1 IN Channel Assignment
- Figure 9 — P1 END IN Channel Assignment
- Figure 10 — I/O BUS Data Line Drivers-Receivers
- Figure 11 — I/O BUS Control, Host Ready Logic
- Figure 12 — Device Selection, Initialization
- Figure 13 — Host-to-IMP (Output) Buffer
- Figure 14 — Host-to-IMP (Output) Control Logic
- Figure 15 — IMP-to-Host (Input) Buffer
- Figure 16 — IMP-to-Host (Input) Control Logic
- Figure 17a — Local Host, Line Drivers and Receivers

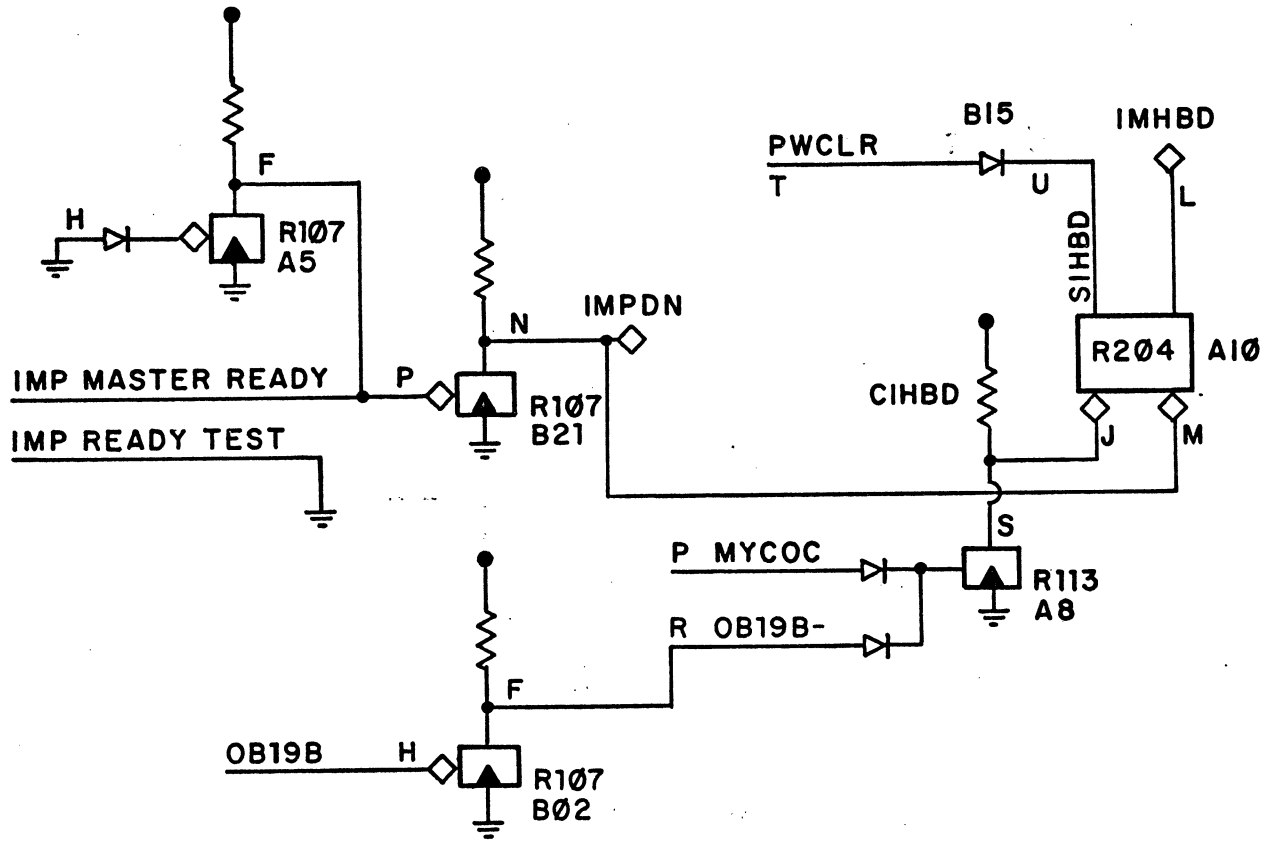


FIGURE 6 IMP ERROR DETECTION LOGIC

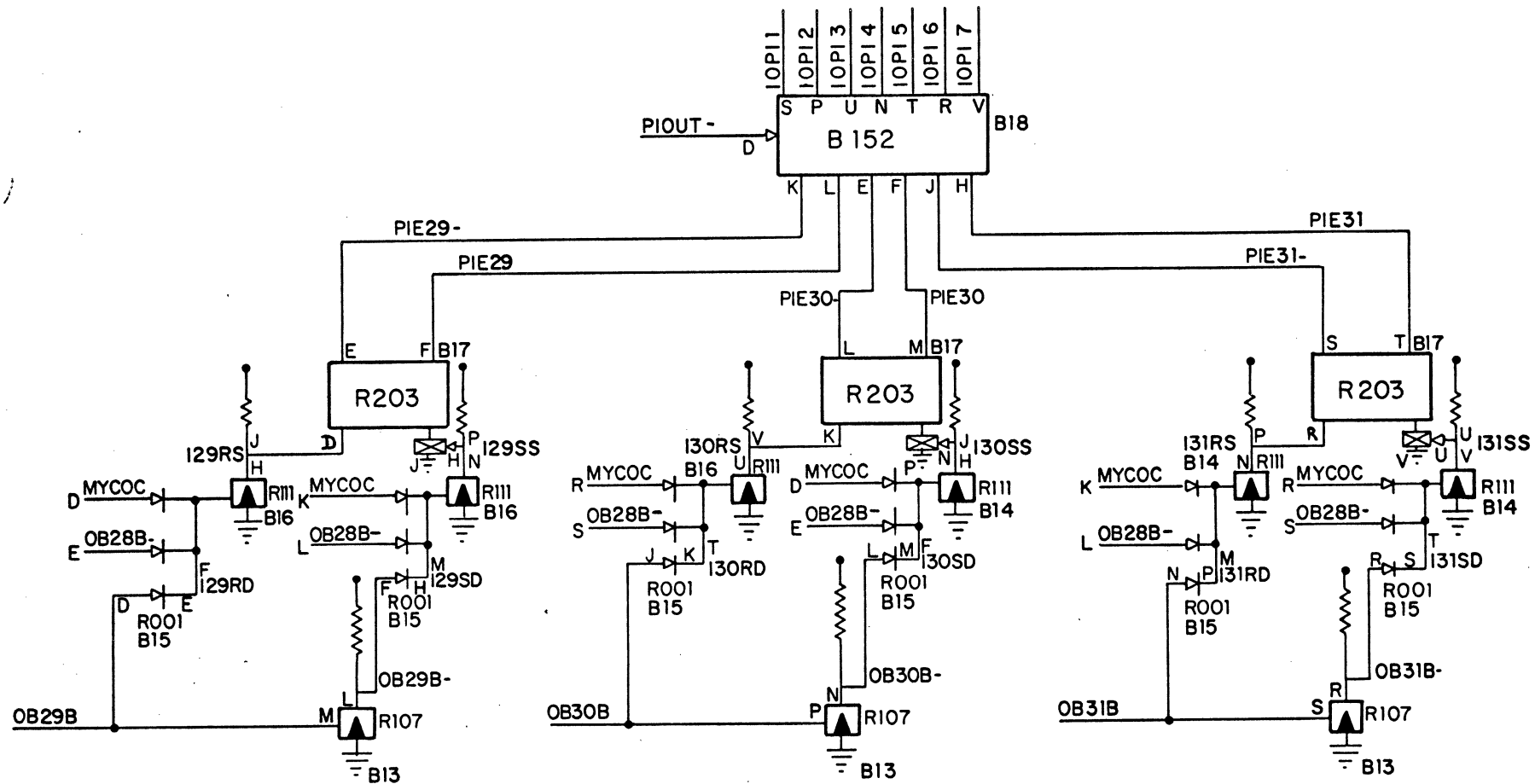


FIGURE 7 - PI OUT CHANNEL ASSIGNMENT

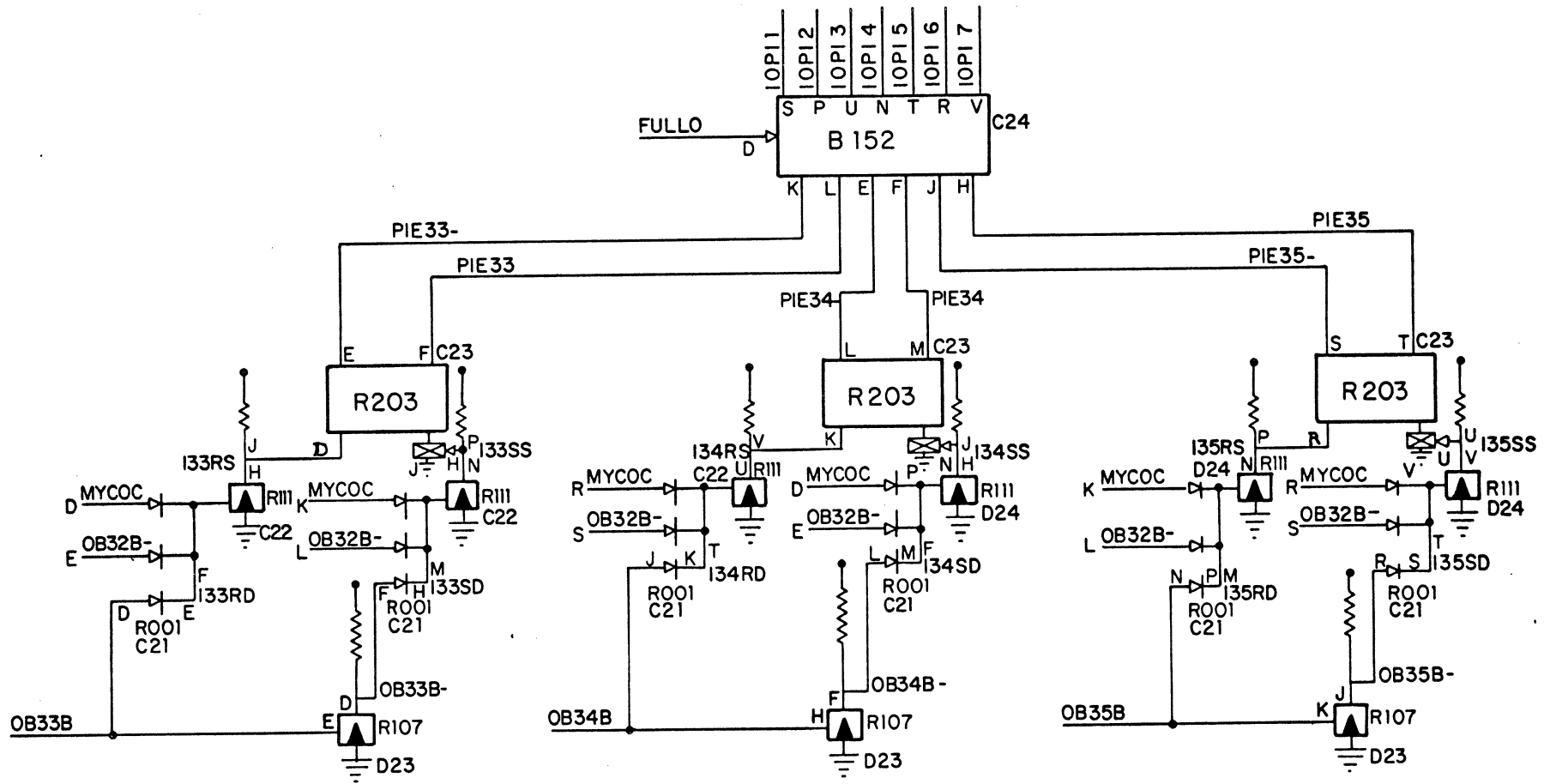


FIGURE 8 - PI IN CHANNEL ASSIGNMENT

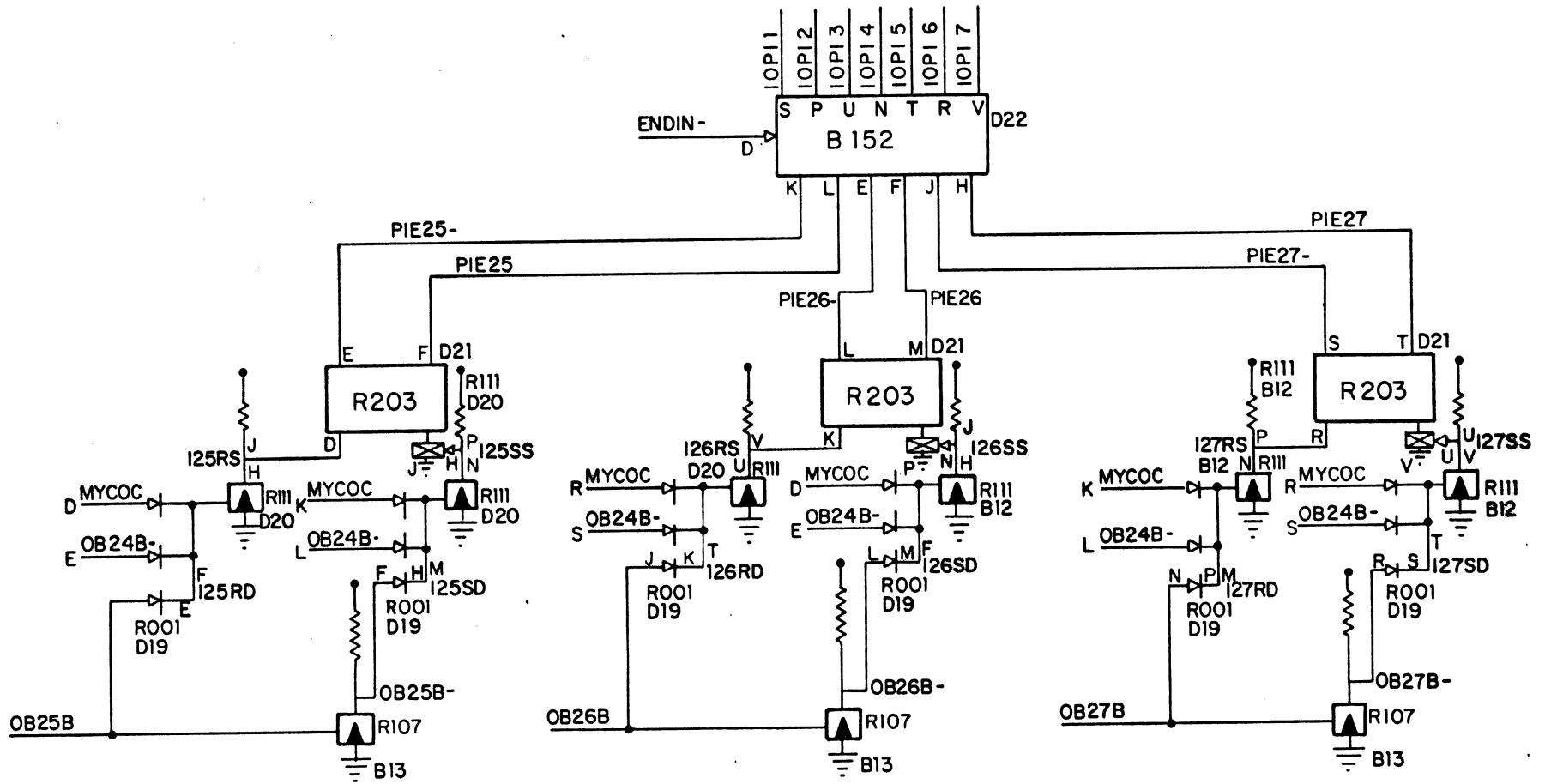


FIGURE 9 - PI END IN CHANNEL ASSIGNMENT

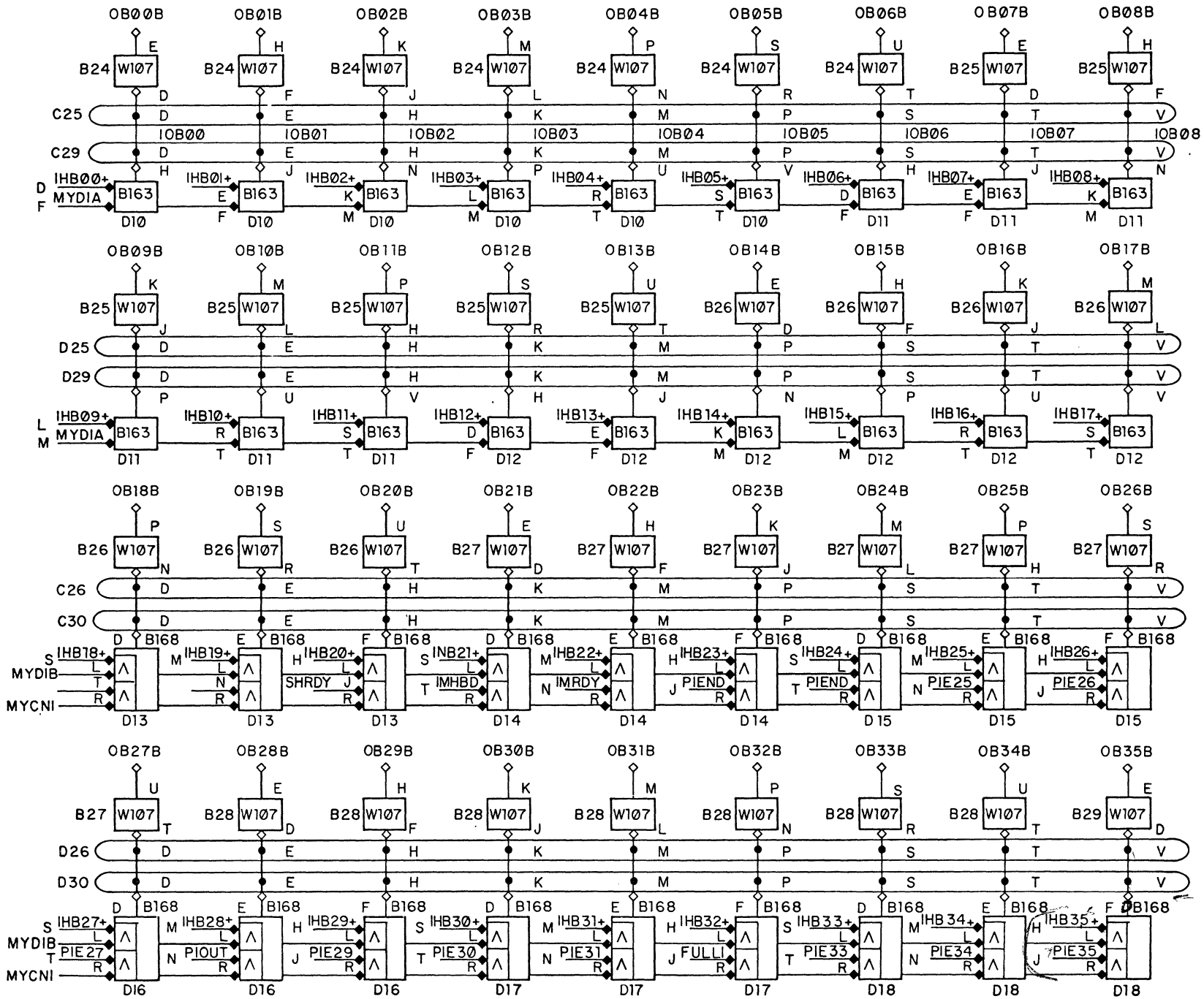


FIGURE 10 - I/O BUS DATA LINE DRIVERS-RECEIVERS

MA Register in KA10 pins

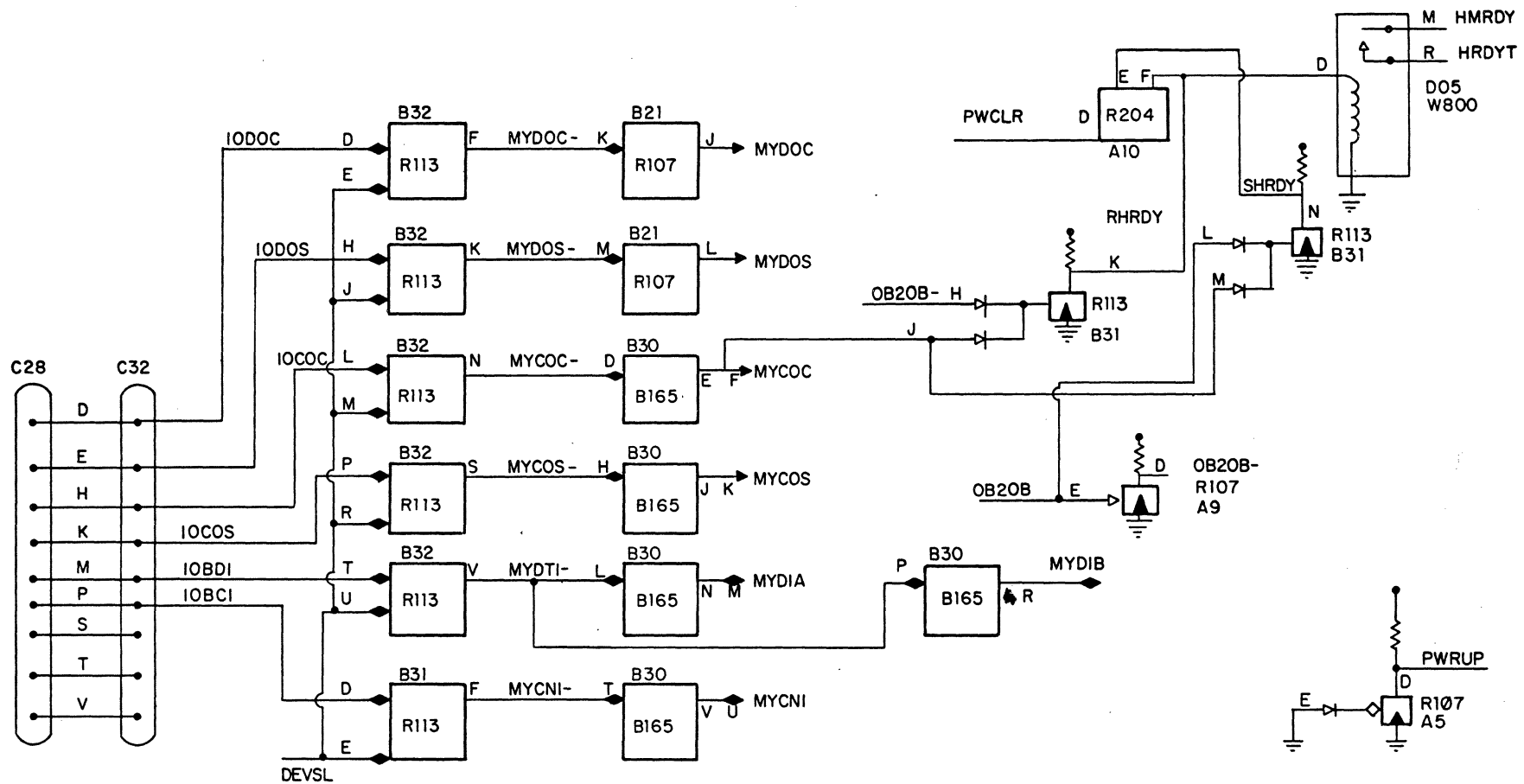


FIGURE 11 - I/O BUS CONTROL, HOST READY LOGIC

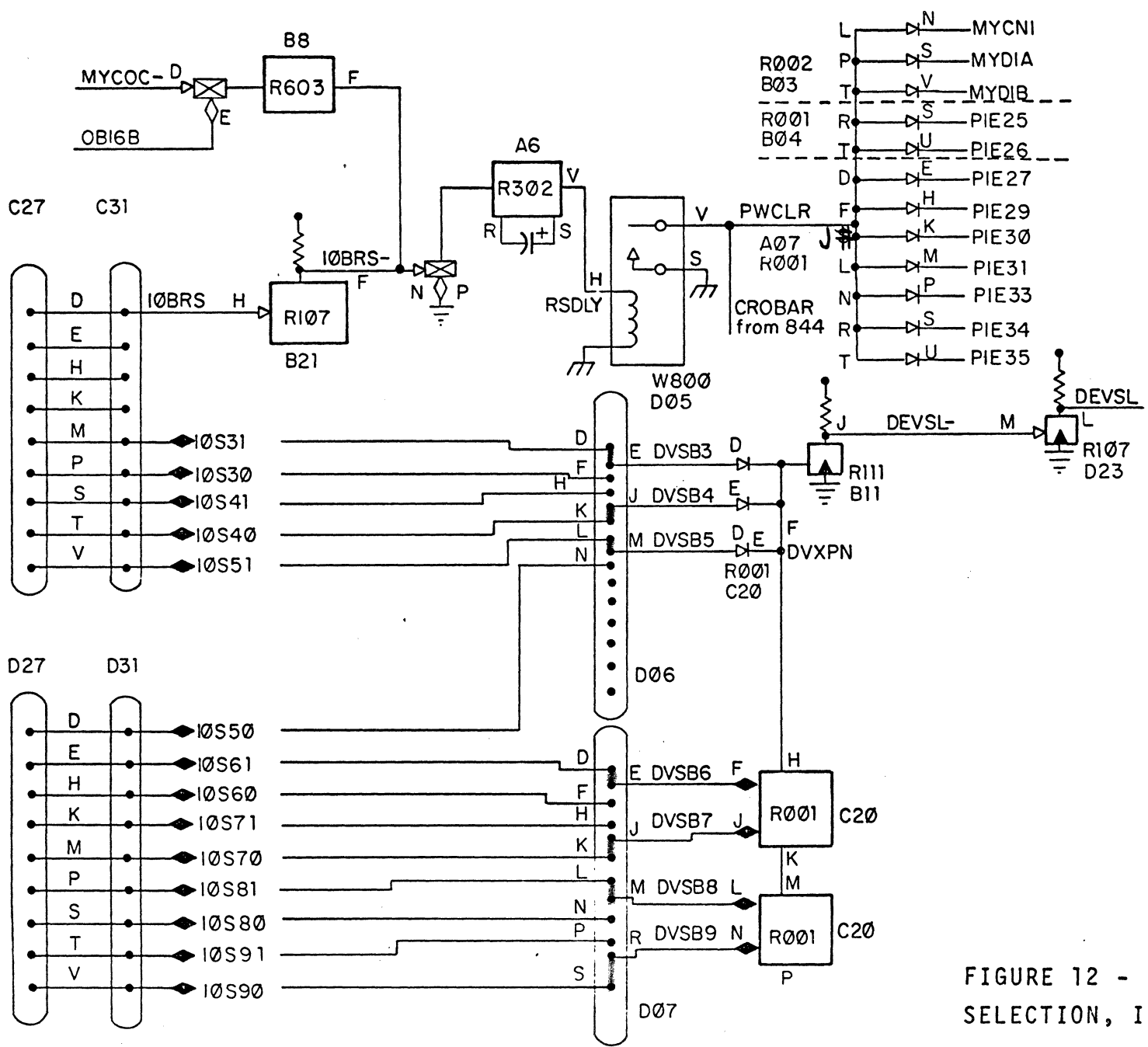


FIGURE 12 - DEVICE SELECTION, INITIALIZATION

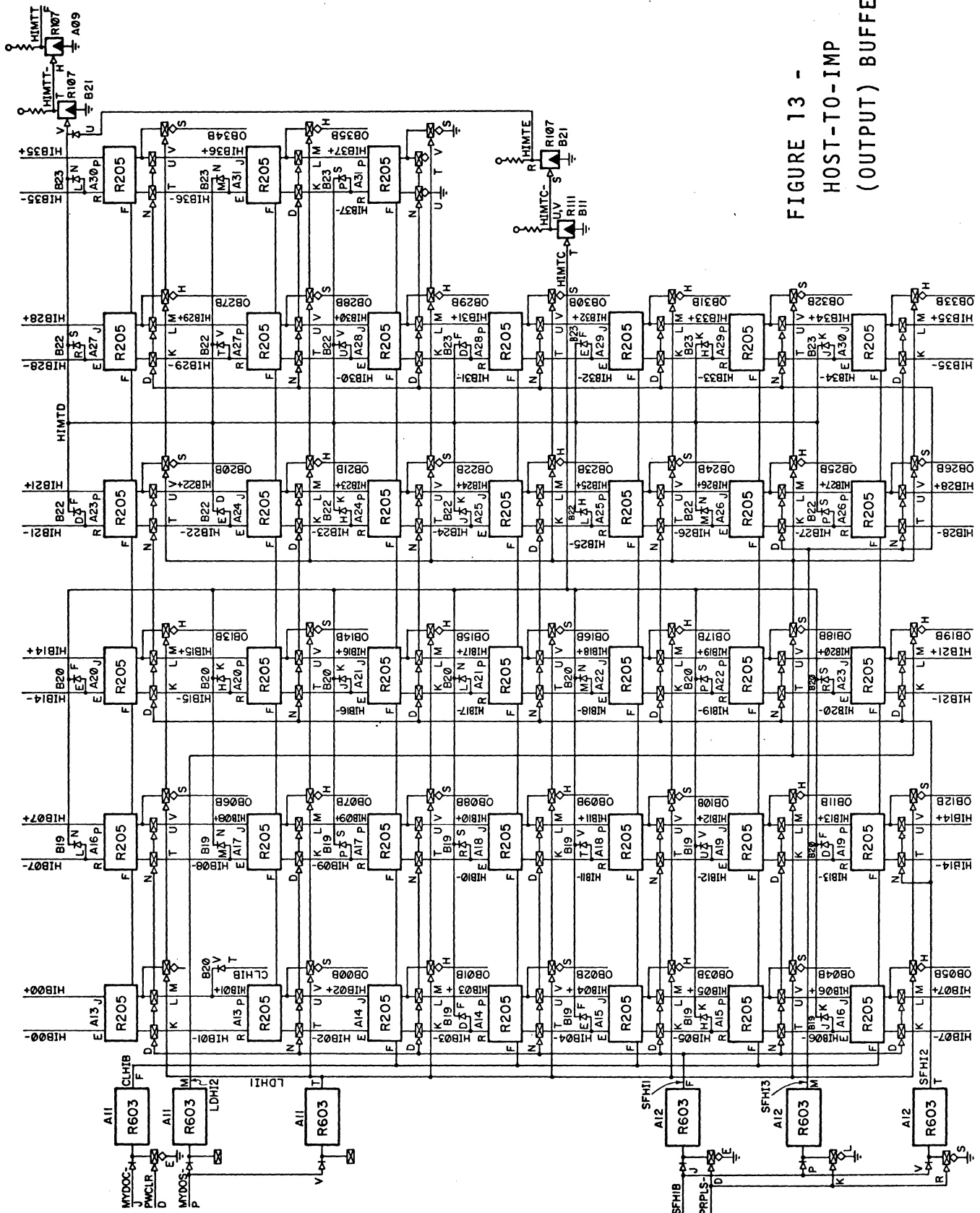


FIGURE 13 -
HOST-TO-IMP
(OUTPUT) BUFFER

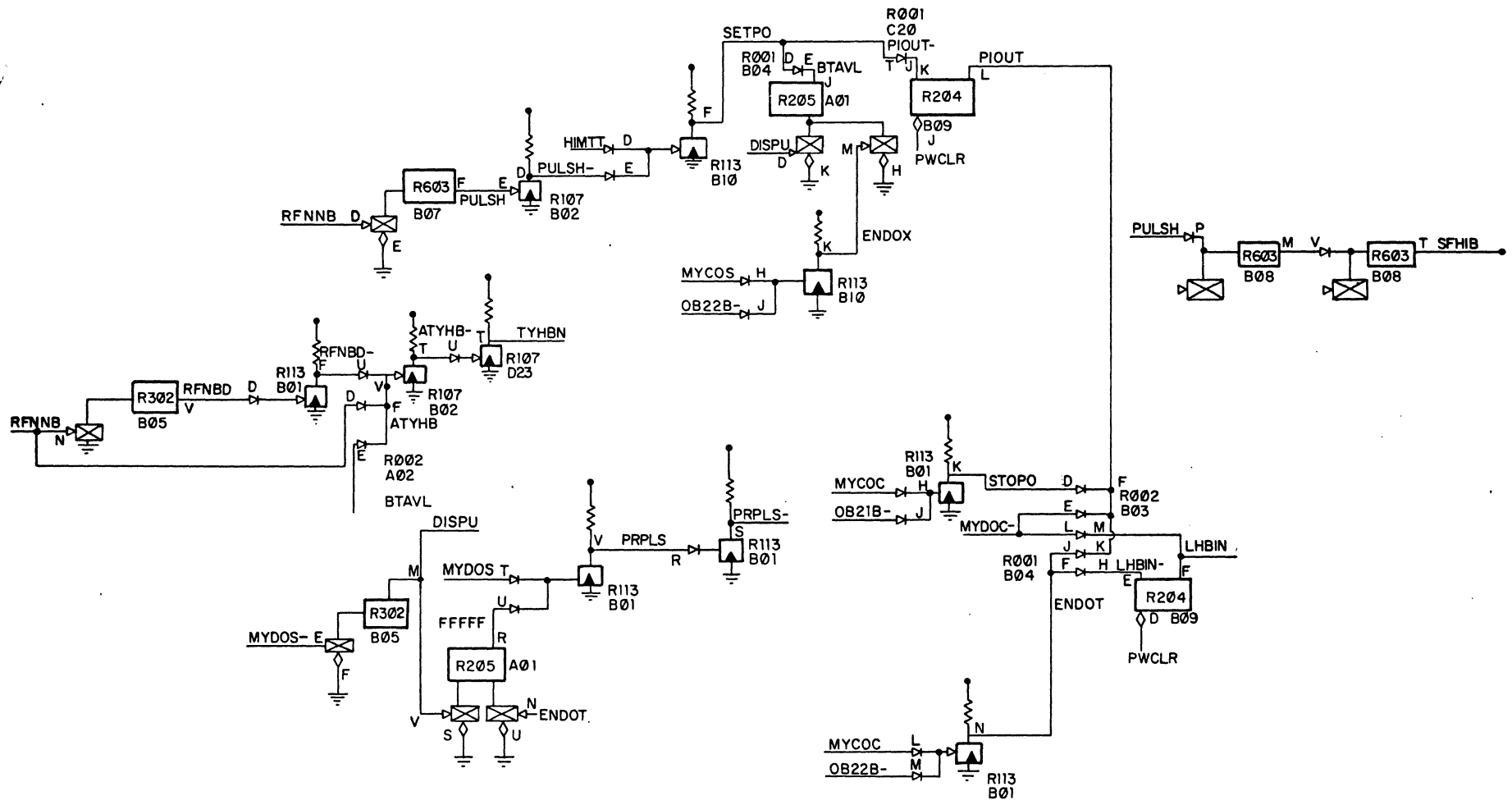


FIGURE 14 - HOST-TO-IMP (OUTPUT) CONTROL LOGIC

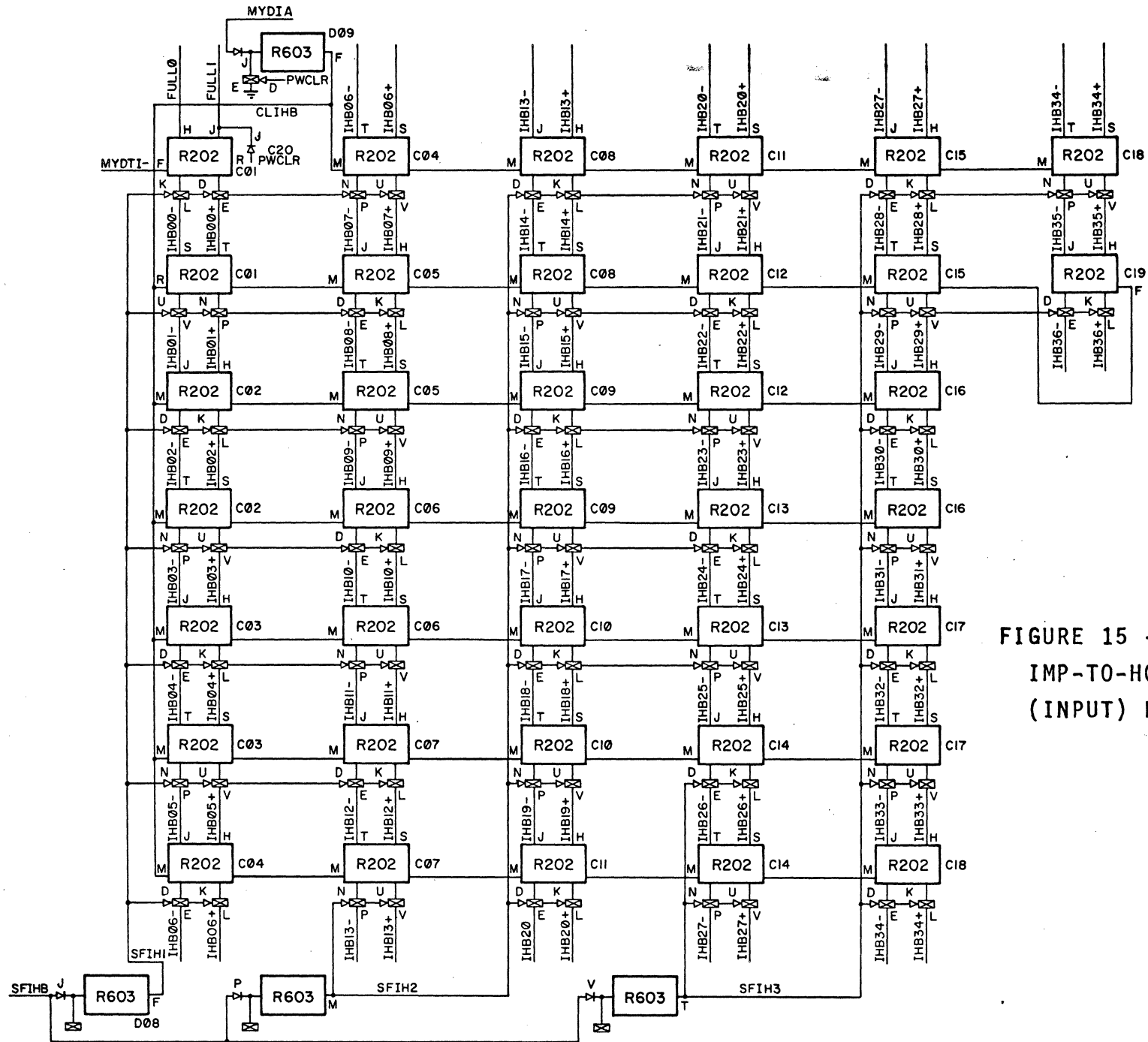
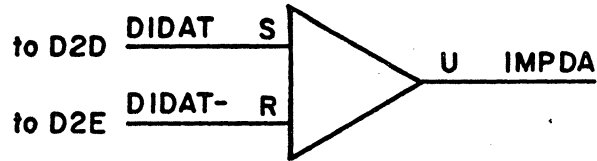
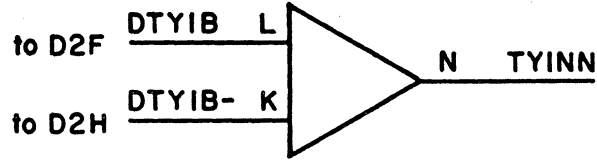
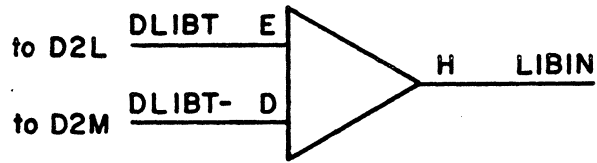
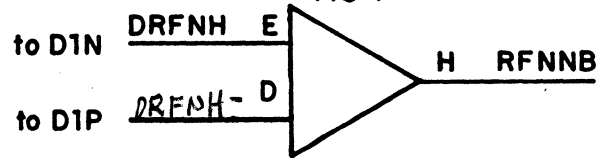


FIGURE 15 -
IMP-TO-HOST
(INPUT) BUFFER

W520 A03

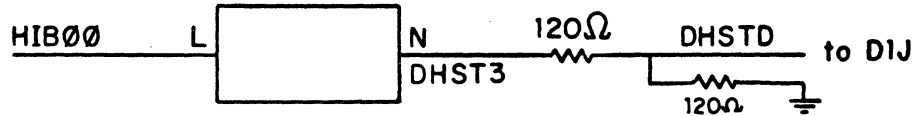
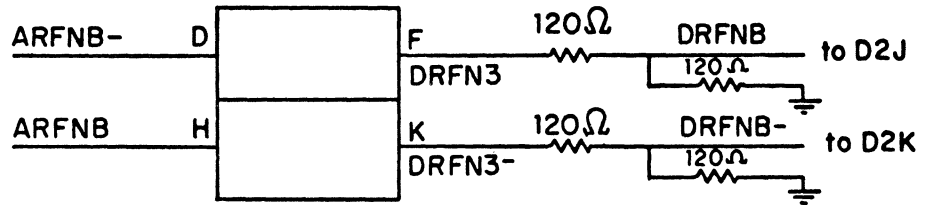


A04

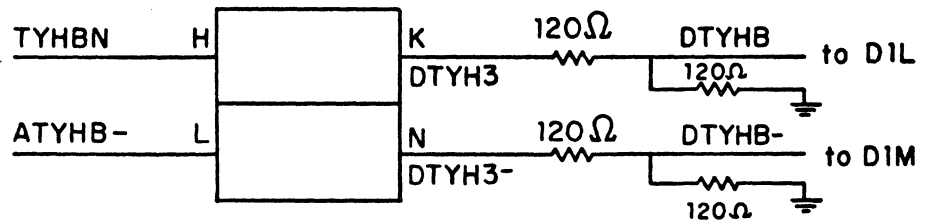
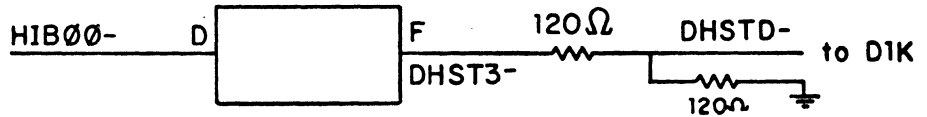


all resistors 1/4 watt

W602 D3



D4



A32

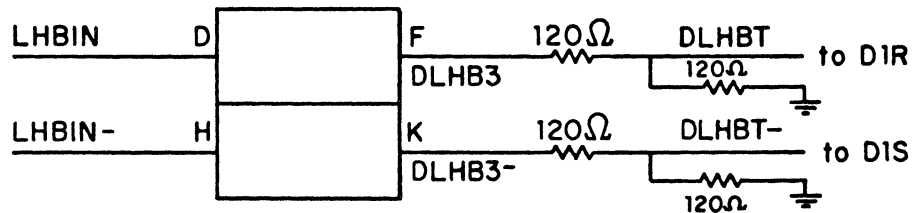


FIGURE 17 DISTANT HOST, LINE DRIVERS AND RECEIVERS

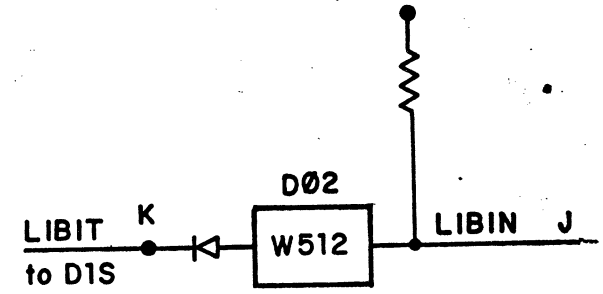
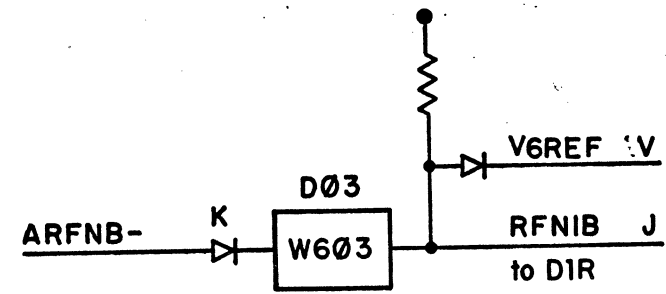
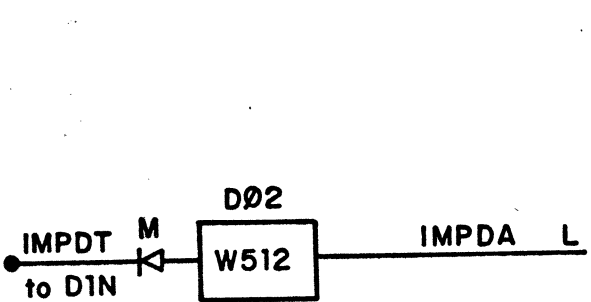
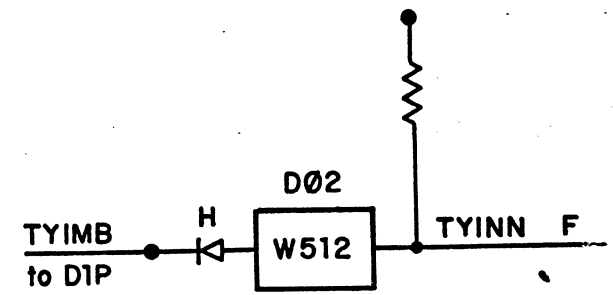
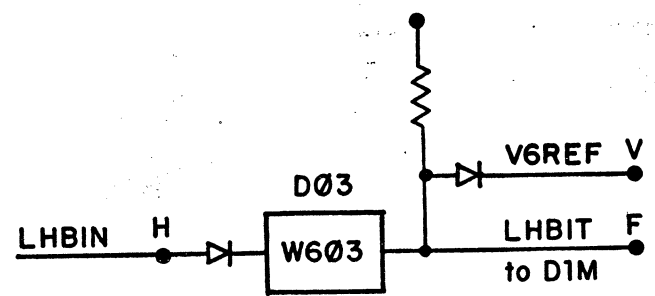
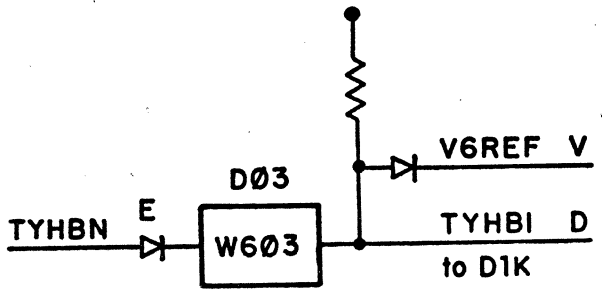
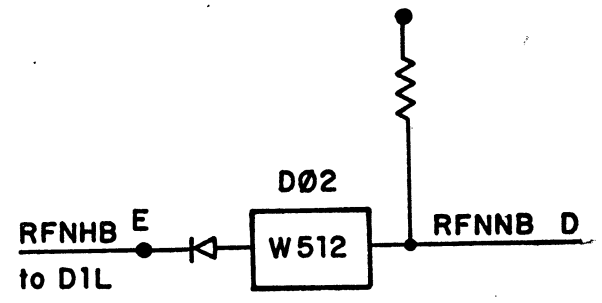
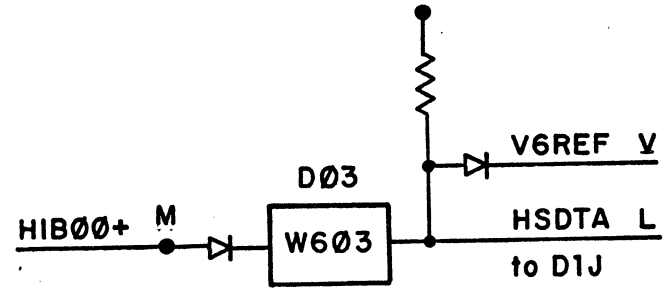
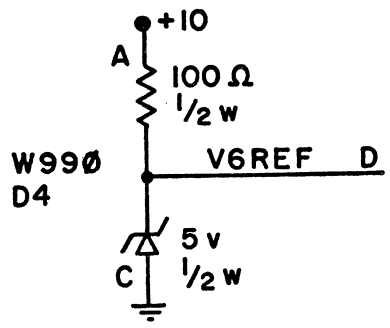


FIGURE 17a LOCAL HOST, LINE DRIVERS AND RECEIVERS

5. TEST PROGRAM DESCRIPTION AND PROGRAM LISTINGS

The test program runs on the PDP-10 under any of three modes: as a stand-alone program, as a program under a DEC 10/50 monitor using user I/O, or as a program under a TENEX system running in monitor space.

The program tests the interface by communicating with the standard IMP system, repetitively sending to itself two messages on separate links. These messages contain sequence numbers which are indexed with each consecutive transmission. Upon receipt of one of these messages from itself, the program verifies the data including the sequence number against that transmitted and types out any discrepancies.

A queue of messages waiting for transmission is kept, and on receipt of the RFNM for a given message, another copy of that message is placed on the queue, with the sequence number indexed. If the sequence numbers for the two messages ever differ by more than one, a RFNM has probably been dropped. A message to this effect is typed out and the program is reinitialized.

The program is organized as three co-routines: an input routine, an output routine, and a background routine. The background routine polls the interface for input completion and output completion, and calls the appropriate co-routine. It also tests for a number of error conditions including sequence number differences of two or more, interface power down, IMP not ready, IMP was down, and TIMEOUT (a long period with no activity).

Upon initialization the program clears the interface, makes the Host appear down to the IMP, waits one second, then brings the ready line true. It then places four no-op messages on the

queue of messages to be sent to the IMP, clears both sequence counts and puts one copy of each of the two main messages on the queue to be sent. The initial calling points of the input and output routines are then set up and the timeout count is initialized. The program then falls through to the background routine.

The input routine initializes the block-in pointer, then loops, first calling the background routine to wait for an input word. It then reads the interface conditions so that if the word just input happens to be the last of the message, the ENDIN bit can be reliably read. A BLKI is then executed to input the word. This BLKI should never overflow, as the last word should be received from the IMP before the input buffer is filled. The ENDIN bit is then tested, and if not true, the input routine loops to get another word. If the ENDIN bit was true, a CONO GOT ENDIN is issued to the interface. The message is then tested for a number of error conditions, any of which will cause a typeout. A normal message from another Host, which is generally not an error condition, will also cause a typeout. In addition, whenever the sequence number on either link reaches a multiple of 10,000 octal, a typeout to that effect is given.

The output routine waits for the output buffer to be emptied, then interrogates the queue to find whether there is anything waiting to be sent. If not it returns to the background routine to test the other background conditions. If it finds something on the queue it removes it, then loops, first waiting for the output buffer to be empty, then executing the BLKO to actually output a word. If the BLKO does not overflow, the routine loops to wait for the buffer to be empty again. If it does overflow, after waiting for the buffer to be empty, a CONO END OUT is issued. The routine then loops to again test the queue.

There are three assembly parameters which are installation specific. One is SYSTEM, which may be set either to BARE for a stand-alone program, to DEC to run under a DEC 10/50 monitor with user I/O privilege, or to TENEX to run under a TENEX system in monitor address space. In stand-alone mode, the program will assemble in RIM10B mode, with an origin of 4000. If it is to run under a 10/50 it will ordinarily load at location 140. If it is to run under a TENEX, its origin is 274000.

The remaining installation-specific parameters are the IMP device code, called IMP, and the network address, called ADRES. These three parameters must be set at assembly time to the relevant settings for the installation.

; <DIAGNOSTICS>IMPBBN.A;3 22-NOV-72 13:58:08 EDIT BY CHIPMAN

TITLE IMPTST
SUBMITL SENDS MESSAGES TO SELF VIA IMPSYS
BAR1==0
DEC==1
TENEX==2

; INSTALLATION-SPECIFIC ASSEMBLY PARAMETERS *****
; WHAT KIND OF SYSTEM AM I RUNNING UNDER? *

SYSTEM==TENEX ; *

; IMP DEVICE CODE ; *

IMP==+0554 ; *

; MY NETWORK ADDRESS ; *

ADR1S==+0105 ; *

; *****

; SYSTEM CALL DEFINITIONS

IFE SYSTEM-TENEX, <

SEARCH STENIX

>

; LINK NUMBER TO BE USED

LINK==+0340

LINK2==LINK+1

; INPUT BUFFER SIZE

INSIZ==+0225

STKSIZ==+0500 ; PUSH DOWN LIST SIZE

QUESIZ==+0100 ; SIZE OF OUTGOING MESSAGE QUEUE

CP=17 ; STACK POINTER

; OTHER AC'S

BLOCKI=<BLOCKO=<INAC=<OUTAC=CP-1>-1>-1>-1

WHICH=<FLAGS=<TIME=<CONDS=<QP=<OFFQ=BLOCKI-1>-1>-1>-1>-1>-1

; CONO BITS

CLRERR==200000

MAK10D==100000

STPOUT==40000

ENDOUT==20000

GCIEND==10000

ENBEND==4000

ENBOUT==200

ENBIN==10

; CONI BITS

PWRUP==200000

DOWN10==100000

ERR==40000

IMPDWN==20000

ENDIN==14000

EMPTY==200

FULL==10

+L

```
IFE SYSTEM-BARE, <LOC 4000
RIM10B>
;DEFINE TTY OUTPUT MACROS IN CASE NOT 10-50
IFE SYSTEM-BARE, <DEFINE OUTSTR (ADDRESS)
<HRRZI 1, ADDRESS
PUSHJ CP, TTYOUT>
DEFINE OUTCHR
<PUSHJ CP, TTYCHR>
>
IFE SYSTEM-TENEX, <DEFINE OUTSTR (ADDRESS)
<HRROI 1, ADDRESS
PSOUT>
DEFINE OUTCHR
<PUSHJ CP, TTYCHR>
>
;MACRO TO PUT A MESSAGE ON THE OUTGOING QUEUE
DEFINE POQ (WORD)
<MOVE 0, WORD
PUSHJ CP, PUTONQ>
DEFINE EROR (STRING)
<[PUSH CP, 7
PUSH CP, 1
OUTSTR <[ASCIZ/
STRING
/]>
PUSHJ CP, PHEADR
POP CP, 1
POP CP, 2
JRSI .+1]>
```

↑L

```
;IF RUNNING UNDER 12-50, CALL TRPSET
START:  IFE SYSTEM-TENEX,<USRIO
        JRST [OUTSTR<[ASCIZ*
USER I/O PRIVELEGE NOT AVAILABLE- ARE YOU ENABLED?
*]>
        HALIF]>
        IFE SYSTEM-DEC, <CALLI 0,0
        MOVEI 1, 0
        CALLI 1, 25
        JRST [OUTSTR<[ASCIZ*
USER I/O PRIVELEGE NOT AVAILABLE
*]>
        EXII]>
        IFE SYSTEM-BARE, <CONO TTY, 3410>
        MOVE CP, [IOWD STKSIZ, STACK]
        OUTSTR<[ASCIZ/
IMP TESTER
/]>
        CONO IMP, MAK10D+ENBEND+ENBOUT+ENBIN
;NOW WAIT FOR THE IMP TO SEE THAT YOU ARE DOWN
        IFE SYSTEM-DEC, <MOVSI 0, -4
        ACJL .>
        IFE SYSTEM-DEC, <MOVEI 3, 1
        SLEEP>
;INITIALIZE QUEUE POINTERS
        MOVE QP, [IOWD QUESIZ, QUEUE]
        MOVE OFFQ, QP
;INITIALIZE THE INTERFACE
        DATAI IMP, 0
        CONO IMP, CLRERR+ENDOUT+GOTEND
;PUT 4 NOPs ON THE OUTGOING MESSAGE QUEUE
        MOVEI 1, 4
NOPLOP: PCQ <[IOWD 1, NOPMES]>
        SCJG 1, NOPLOP
;CLEAR BOTH SEQUENCE COUNTERS
        SETZM MESC1
        SETZM MESC2
;QUEUE BOTH MAIN MESSAGES
        PCQ IOWD1
        PCQ IOWD2
;SET UP RETURN POINTERS TO POINT TO THE BEGINNING OF THE
;INPUT AND OUTPUT ROUTINES
        MOVEI INAC, STRTIN
        MOVEI OUTAC, STARTO
        MOVSI TIME, 40
↑L
```

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BCKGND: C=NI IMP, CONDS ;BACKGROUND LOOP TESTS WHETHER
        TRNE CONDS, FULL ;INPUT WANTS SERVICE
        JRST (INAC)
        TRNE CONDS, EMPTY ;OR OUTPUT WANTS SERVICE
        JRST (OUTAC)
TIMCNT: MOVE 1, MESC1 ;NOW TEST WHETHER SEQUENCE COUNTS
        SUB 1, MESC2 ;DIFFER BY MORE THAN 1, TO CHECK
        JUMPL 1, STEP ;FOR DROPPED RFNMS
        SCJG 1, STEP
;NOW TEST VARIOUS INTERFACE ERROR CONDITIONS
        TRNN CONDS, PWRUP
        JRST [OUTSTR <[ASCIZ/
NO POWER IN INTERFACE/]>
        JRST START]
        TRNN CONDS, IMPDWN
        JRST [OUTSTR <[ASCIZ/
IMP IS DOWN/]>
        JRST START]
        TRNN CONDS, ERR
        JRST [OUTSTR <[ASCIZ/
IMP WAS DOWN ERROR
/]>
        C=NO IMP, CLRERR
        HIRZI TIME, 100000 ;TIME OUT QUICKLY AFTER "IMP WAS DOWN"
        JRST BCKGND]
        SCJG TIME, BCKGND ;TOO LONG SINCE THE LAST MESSAGE?
        JRST EROR <TIME OUT, RESTARTING>
        JRST START
STEP: OUTSTR <[ASCIZ/
LINKS OUT OF STEP, RFNM DRCP?
RESTARTING
/]>
        JRST START
+L

```

```

;INPUT ROUTINE
STRIN: MOVE BLOCKI, [IOWD INSIZ, IBUF] ;SET UP BLKI POINTER
INLOP: JSP INAC, BCKGND ;WAIT FOR A WORD
      CONI IMP, CONDS ;SAVE STATUS FOR ENDIN TEST
      BLKI IMP, BLOCKI ;GET THE WORD
      JPSI EROR <MESSAGE FROM IMP TOO BIG> ;IF BUFFER OVERFLOWS
      TENN COMES, ENDIN;WAS IT THE LAST ONE?
      JRSI INLOP ;NO
      C NO IMP, GOTEND ;YES. RELEASE INTERFACE
;HAVE WHOLE MESSAGE IN CORE, CHECK IT
      LDB 1, [POINT 4, IBUF, 7] ;MESS TYPE
      CAIE 1, 5 ;RFNM?
      JUNPN 1, CONTRL ;IF UNUSUAL MESSAGE TYPE
      LDB 0, [POINT 4, IBUF, 3]
      JUNPN WEIRDO ;IF IT IS FROM IMP, ETC
      LDB 0, [POINT 8, IBUF, 15]
      CAIE ADRES
      JPSI WEIRDO ;IF IT IS NOT FROM ME
      LDR WHICH, [POINT 8, IBUF, 23] ;LINK #
      SUBI WHICH, LINK2
      JUMPG WHICH, EROR <LINK # TOO LARGE>
      ASSL WHICH, EROR <LINK # TOO SMALL>
      ANDI WHICH, 1
      JUNPE 1, NORMAL
RFNM:  ARI 1,@CNTADR(WHICH) ;INCREMENT MESSAGE COUNT
      POC <IOWD1(WHICH)> ;PUT MESSAGE ON OUTGOING QUEUE
      TENE 1, 7777 ;TIME TO PRINT "0000TH MESSAGE" ?
      JPSI STRIN ;NO
      MOVE 0,1
      PUSHJ CP, PRNUM
      OUTSTR <[ASCIZ/TH MESSAGE ON LINK /]>
      MOVEI LINK(WHICH)
      PUSHJ CP, PRNUM
      OUTSTR <[ASCIZ/
/]>
      JRSI STRIN
+L

```

```
WEIRDO: OUPSTR <[ASCIZ/  
MESSAGE FROM SITE /]>  
LDB [POINT 8,IBUF, 5]  
PUSHJ CP, PRNUM  
PUSHJ CP, PHEADR  
JRST STRTIN  
;IS THE RECEIVED MESSAGE THE RIGHT SIZE?  
NORMAL: HLRB 0, BLOCKI  
CAME 0, SIZTAB(WHICH)  
JRST BROR<RIGHT MESSAGE, WRONG LENGTH>  
;NOW CHECK THE DATA  
MOVE 2, IOWD1(WHICH)  
ADD 2, [XWD -1,1]  
MOVBI 3, IBUF  
COMPAR: MOVE 0, (3)  
CAME 0, (2)  
JRST MISMAT  
MATCH: ADD 3, [XWD 1,1]  
ACBJN 2, COMPAR  
MOVSI TIME, 20 ;RESET TIME COUNTER  
JRST STRTIN  
STRANG: OUPSTR @TYPTAB-1(1)  
PUSHJ CP, PHEADR  
POPJ CP,  
CONTRL: LDB 1, [POINT 4, IBUF, 7]  
PUSHJ CP, STRANG  
JRST STRTIN
```

*L

; NAMES OF MESSAGE TYPES

DEFINE CONCAT(A,B) <A'B>

DEFINE NXTYPE (NAME)

<CONCAT(TYP,\N): ASCIZ/NAME/

N=N+1>

N=1

NXTYPE ERROR WITHOUT ID

NXTYPE IMP GOING DOWN

NXTYPE BLOCKED LINK

NXTYPE NOP

NXTYPE RFRM

NXTYPE LINK TABLE FULL

NXTYPE DESTINATION DEAD

NXTYPE ERROR WITH ID

NXTYPE INCOMPLETE TRANSMISSION

NXTYPE CEASE ON LINK

NXTYPE CEASE TIMEOUT

NXTYPE CEASE SENT

NXTYPE TYPE 13

NXTYPE TYPE 14

NXTYPE TYPE 15

I=1

TYPIAB: REPEAT N-1,<

Z CONCAT(TYP,\I)

I=I+1>

*L

MISMAT: OUTSTR <[ASCIZ/DATA MISMATCH ON THE /]>
HLRZ 3
PUSHJ CP, PRNUM
OUTSTR <[ASCIZ/TH WORD OF THE /]>
MOVE @CNTADR (WHICH)
PUSHJ CP, PRNUM
OUTSTR <[ASCIZ/TH MESSAGE ON LINK /]>
MOVEI LINK(WHICH)
PUSHJ CP, PRNUM
OUTSTR <[ASCIZ/
SENT /]>
MOVE (2)
PUSHJ CP, PRNUM
RECEIVED /]>
OUTSTR <[ASCIZ/
MOVE (3)
PUSHJ CP, PRNUM
XOR /]>
OUTSTR <[ASCIZ/
MOVE (2)
XOR (3)
PUSHJ CP, PRNUM
OUTSTR <[ASCIZ/
/]>
JRST MATCH
↑L

;OUTPUT ROUTINE

STARTO: JSP OUTAC, BCKGND ;WAIT FOR THE BUFFER TO BE EMPTY

OUT: CAMN OFFQ, QP ;ANYTHING WAITING TO BE SENT?

JRST TIMCNT ;NO

AMBUN OFFQ, .+2 ;YES. GET IT

MOVE OFFQ, [<IOWD QUESIZ, QUEUE>+<1,,1>]

MOVE BLOCKO, (OFFQ)

OUTLOP: JSP OUTAC, BCKGND ;WAIT FOR BUFFER TO BE EMPTY

BLKO IMP, BLOCKO ;SEND A WORD

JRST FINALO ;IF THAT WAS THE LAST WORD

JRST OUTLOP

FINALO: JSP OUTAC, BCKGND ;WAIT FOR THE BUFFER TO EMPTY

CONO IMP, ENDOUT ;TELL THE INTERFACE THAT'S ALL

JRST STARTO

+L

;ROUTINE TO TYPE A CHARACTER

IFE SYSTEM-BARE,

<TTYCHR:MOVEM 0, CHAR

DATAI APR, 2

TENN 0, 3

JRST DOCHAR

TRNE 0, 2

CONSO TTY, 10

POPJ CP,

DATAO TTY, [7]

POPJ CP,

DOCHAR: CONSO TTY, 10

JRST .-1

DATAO TTY, CHAR

POPJ CP,

CHAR: Z

TTYOUT: HBLI 1, (POINT 7,0)

JRST TTYNIR

TTYLOP: OUTCHR

TTYNIR: ILDB 1

JUMPN TTYLOP

POPJ CP,>

IFE SYSTEM-TENEX,

<TTYCHR: EXCH 0,1

EBOUT

EXCH 0,1

POPJ CP,>

;ROUTINE TO ADD AN ENTRY TO THE OUTGOING QUEUE

PUTONQ: A'BJN QP, .+2

MOVE QP, [<IOWD QUESIZ, QUEUE>+<1,,1>]

MOVEM (QP)

POPJ CP,

;ROUTINE TO PRINT OCTAL NUMBER

PRNUM: LSHC 0, -3

JUMPE PREM

PUSH CP, 1

PUSHJ CP, PRNUM

POP CP, 1

PREM: SETZ

LSHC 0, 3

ICRI 0, '060

OUTCHR

POPJ CP,

*L

;ROUTINE TO PRINT MESSAGE HEADER
PHEADR: OUTSTR <[ASCIZ/
HEADER /]>

LDB [POINT 4, IBUF, 3]
PUSHJ CP, PRNUM
OUTSTR <[ASCIZ/, /]>
LDB [POINT 4, IBUF, 7]
PUSHJ CP, PRNUM
OUTSTR <[ASCIZ/, /]>
LDB [POINT 8, IBUF, 15]
PUSHJ CP, PRNUM
OUTSTR <[ASCIZ/, /]>
LDB [POINT 8, IBUF, 23]
PUSHJ CP, PRNUM
OUTSTR <[ASCIZ/, /]>
LDB [POINT 8, IBUF, 31]
PUSHJ CP, PRNUM
OUTSTR <[ASCIZ/

/]>

PCPJ CP,
QUEUE: BLOCK QUESIZ
STACK: BLOCK STKSIZ
IOWD1: IOWD <END1-MES1>+1, MES1
IOWD2: IOWD <END2-MES2>+1, MES2
SIZTAB: <END1-MES1+2>-INSIZ
<END2-MES2+2>-INSIZ
CNTADR: Z MESC1
Z MESC2

+L

;THE MESSAGES

MES1: <ADRES>B15 + <LINK>B23 ;HEADER
MESC1: 0 ;MESSAGE SEQUENCE NUMBER
;DATA

-1
0
525252525252
252525252525
123456765432
45636,,737134
757726,,666735
375714,,446357
773350,,432653
262347,,513752
61563,,733471
724527,,757030
535532,,647141
736710,,671303

END1: 172317,,221743
400000,,0

MES2: <ADRES>B15 + <LINK2>B23 ;HEADER
MESC2: 0 ;MESSAGE SEQUENCE NUMBER
;DATA

1
2
4
10
20
40
400000,,0
200000,,0
100000,,0
40000,,0
20000,,0
10000,,0

-1,, -2
-1,, -3

END2: 377777,, -1
400000,, 0

NOPMES: BYT (4) 2,4,0,11, 7
IBUF: BLOCK INSIZ
END START

+L

6. WIRE LISTS

PART I: IMP/10 pin list

PART II: IMP/10 list sorted by signal

A	1	C	GDA01+
A	1	D	DS1PU+
A	1	F	PWCLR+
A	1	H	GDA01+
A	1	J	BTAVL+
A	1	K	GDA01+
A	1	M	ENDOX+
A	1	N	ENDOT+
A	1	R	FFFFF+
A	1	S	GDA01+
A	1	U	GDA01+
A	1	V	DS1PU+

A	2	D	RFNNB+
A	2	E	BTAVL+
A	2	F	ATYHB+
A	2	H	TYIND-
A	2	J	TYINN-
A	2	K	TYIDN+

A	3	D	DLIBT-
A	3	E	DLIBT+
A	3	H	LIBIN+
A	3	K	DTYIB-
A	3	L	DTYIB+
A	3	N	TYINN+
A	3	R	DIDAT-
A	3	S	DIDAT+
A	3	U	IMPDA+

A	4	D	DRFNH-
A	4	E	DRFNH+
A	4	H	RFNNB+

A	5	C	GDA05+
A	5	D	PWRUP+
A	5	E	GDA05+
A	5	F	IMRDY+
A	5	H	GDA05+
A	5	R	TYIND-
A	5	S	TYIND+
A	5	T	ARFNB+
A	5	U	IRFNB+
A	5	V	TYIDN+

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GDA06+
TYINN-
GDA06+
A6JKJ+
A6JKJ+
TYIND+
IOBRS-
GDA06+
A6RCJ+
A6STJ+
A6STJ+
RSDLY+

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PWCLR+
PIE27+
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PIE29+
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PIE30+
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PIE31+
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PIE33+
PWCLR+
PIE34+
PWCLR+
PIE35+

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FULL0+
NPADP-
PADPP+
FULL1+
NPADP-
ENDIN-
MYCOC+
OB23B-
COGTE+
MYCOC+
OB19B-
CIHBD+
PADPP+
LTYMP+
STPAD+

A

9

D

OB20B-

FORM 5310

PRINTED IN U.S.A.

A	9	E	OB20B+
A	9	F	HIMTT+
A	9	H	HIMTT-
A	9	J	TYIMP-
A	9	K	TYIMP+
A	9	L	OB24B-
A	9	M	OB24B+
A	9	N	OB28B-
A	9	P	OB28B+
A	9	R	OB32B-
A	9	S	OB32B+
A	9	T	OB23B-
A	9	U	OB23B+

A	10	D	PWCLR+
A	10	E	SHRDY+
A	10	F	RHRDY+
A	10	J	CIHBD+
A	10	K	SIHBD+
A	10	L	IMHBD+
A	10	M	IMPDN+

A	11	C	GDA11+
A	11	D	PWCLR+
A	11	E	GDA11+
A	11	F	CLHIB+
A	11	H	GDA11+
A	11	J	MYDOC-
A	11	M	LDHI2+
A	11	P	MYDOS-
A	11	T	LDHI1+
A	11	V	MYDOS-

A	12	C	GDA12+
A	12	D	PRPLS-
A	12	E	GDA12+
A	12	F	SFHI1+
A	12	J	SFHIB+
A	12	K	PRPLS-
A	12	L	GDA12+
A	12	M	SFHI2+
A	12	P	SFHIB+
A	12	R	PRPLS-
A	12	S	GDA12+
A	12	T	SFHI3+
A	12	V	SFHIB+

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SFHI1+
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 HIB00+
 HIB01-
 HIB01+
 LDHI1+
 SFHI1+
 HIB01+
 HIB01-
 QB00B+
 HIB02-
 HIB02+
 LDHI1+

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SFHI1+
 HIB02-
 CLHIB+
 QB01B+
 HIB02+
 HIB03-
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 LDHI1+
 SFHI1+
 HIB03+
 HIB03-
 QB02B+
 HIB04-
 HIB04+
 LDHI1+

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SFHI1+
 HIB04-
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 SFHI1+
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 QB04B+
 HIB06-
 HIB06+
 LDHI1+

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SFHI1+
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 OB05B+
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 HIB07-
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 LDHI1+
 SFHI1+
 HIB07+
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 OB06B+
 HIB08-
 HIB08+
 LDHI1+

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 LDHI1+

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 OB16B+
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 SFHI2+
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 OB18B+
 HIB20-
 HIB20+
 LDHI2+

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SFHI2+
 HIB20-
 CLHIB+
 OB19B+
 HIB20+
 HIB21-
 HIB21+
 LDHI2+
 SFHI2+
 HIB21+
 HIB21-
 OB20B+
 HIB22-
 HIB22+
 LDHI2+

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SFHI2+
 HIB22-
 CLHIB+
 OB21B+
 HIB22+
 HIB23-
 HIB23+
 LDHI2+
 SFHI2+
 HIB23+
 HIB23-
 OB22B+
 HIB24-
 HIB24+

A	24	V	LDHI2+
A	25	D	SFHI2+
A	25	E	HIB24-
A	25	F	CLHIB+
A	25	H	OB23B+
A	25	J	HIB24+
A	25	K	HIB25-
A	25	L	HIB25+
A	25	M	LDHI2+
A	25	N	SFHI2+
A	25	P	HIB25+
A	25	R	HIB25-
A	25	S	OB24B+
A	25	T	HIB26-
A	25	U	HIB26+
A	25	V	LDHI2+
A	26	D	SFHI3+
A	26	E	HIB26-
A	26	F	CLHIB+
A	26	H	OB25B+
A	26	J	HIB26+
A	26	K	HIB27-
A	26	L	HIB27+
A	26	M	LDHI2+
A	26	N	SFHI3+
A	26	P	HIB27+
A	26	R	HIB27-
A	26	S	OB26B+
A	26	T	HIB28-
A	26	U	HIB28+
A	26	V	LDHI2+
A	27	D	SFHI3+
A	27	E	HIB28-
A	27	F	CLHIB+
A	27	H	OB27B+
A	27	J	HIB28+
A	27	K	HIB29-
A	27	L	HIB29+
A	27	M	LDHI2+
A	27	N	SFHI3+
A	27	P	HIB29+
A	27	R	HIB29-
A	27	S	OB28B+
A	27	T	HIB30-

A	27	U	HIB30+
A	27	V	LDHI2+
A	28	D	SFHI3+
A	28	E	HIB30-
A	28	F	CLHIB+
A	28	H	OB29B+
A	28	J	HIB30+
A	28	K	HIB31-
A	28	L	HIB31+
A	28	M	LDHI2+
A	28	N	SFHI3+
A	28	P	HIB31+
A	28	R	HIB31-
A	28	S	OB30B+
A	28	T	HIB32-
A	28	U	HIB32+
A	28	V	LDHI2+
A	29	D	SFHI3+
A	29	E	HIB32-
A	29	F	CLHIB+
A	29	H	OB31B+
A	29	J	HIB32+
A	29	K	HIB33-
A	29	L	HIB33+
A	29	M	LDHI2+
A	29	N	SFHI3+
A	29	P	HIB33+
A	29	R	HIB33-
A	29	S	OB32B+
A	29	T	HIB34-
A	29	U	HIB34+
A	29	V	LDHI2+
A	30	D	SFHI3+
A	30	E	HIB34-
A	30	F	CLHIB+
A	30	H	OB33B+
A	30	J	HIB34+
A	30	K	HIB35-
A	30	L	HIB35+
A	30	M	LDHI2+
A	30	N	SFHI3+
A	30	P	HIB35+
A	30	R	HIB35-
A	30	S	OB34B+

A	30	T	HIB36-
A	30	U	HIB36+
A	30	V	LDHI2+

A	31	C	GDA31+
A	31	D	SFHI3+
A	31	E	HIB36-
A	31	F	CLHIB+
A	31	H	OB35B+
A	31	J	HIB36+
A	31	K	HIB37-
A	31	L	HIB37+
A	31	M	LDHI2+
A	31	N	SFHI3+
A	31	P	HIB37+
A	31	R	HIB37-
A	31	S	GDA31+
A	31	U	GDA31+
A	31	V	LDHI2+

A	32	D	LHBIN+
A	32	F	DLHB3+
A	32	H	LHBIN-
A	32	K	DLHB3-

B	1	D	RFNBD+
B	1	F	RFNBD-
B	1	H	MYCOC+
B	1	J	OB21B-
B	1	K	STOPO+
B	1	L	MYCOC+
B	1	M	OB22B-
B	1	N	ENDOT+
B	1	R	PRPLS+
B	1	S	PRPLS-
B	1	T	MYDOS+
B	1	U	FFFFF+
B	1	V	PRPLS+

B	2	D	PULSH-
B	2	E	PULSH+
B	2	F	OB19B-
B	2	H	OB19B+
B	2	J	TYINN-
B	2	K	TYINN+
B	2	L	SFIHB+

FORM 5310

PRINTED IN U.S.A.

B	2	M	SFIHB-
B	2	N	ARFNB-
B	2	P	ARFNB+
B	2	R	STPAD-
B	2	S	STPAD+
B	2	T	ATYHB-
B	2	U	RFNBD-
B	2	V	ATYHB+

B	3	D	STOPO+
B	3	E	MYDOC-
B	3	F	PIOUT+
B	3	H	FULL0+
B	3	J	LTYPF+
B	3	K	IRFNB+
B	3	L	PWCLR+
B	3	N	MYCNI+
B	3	P	PWCLR+
B	3	S	MYDIA+
B	3	T	PWCLR+
B	3	V	MYDIB+

B	4	D	SETPO+
B	4	E	BTAVL+
B	4	F	ENDOT+
B	4	H	LHBIN-
B	4	J	ENDOT+
B	4	K	PIOUT+
B	4	L	MYDOC-
B	4	M	LHBIN+
B	4	N	COGTE+
B	4	P	IRFNB-
B	4	R	PWCLR+
B	4	S	PIE25+
B	4	T	PWCLR+
B	4	U	PIE26+

B	5	C	GDB05+
B	5	E	MYDOS-
B	5	F	GDB05+
B	5	J	JKJB5+
B	5	K	JKJB5+
B	5	M	DS1PU+
B	5	N	RFNNB+
B	5	P	GDB05+
B	5	S	STJB5+
B	5	T	STJB5+

B	5	V	RFNBD+
B	6	C	GDB06+
B	6	E	STPAD-
B	6	F	GDB06+
B	6	J	B6JKJ+
B	6	K	B6JKJ+
B	6	M	AAAPAD+
B	6	N	AAAPAD+
B	6	P	GDB06+
B	6	S	B6STJ+
B	6	T	B6STJ+
B	6	V	APADP+

B	7	C	GDB07+
B	7	D	RFNNB+
B	7	E	GDB07+
B	7	F	PULSH+
B	7	K	TYINN-
B	7	L	GDB07+
B	7	M	TYIMP+
B	7	R	APADP+
B	7	S	GDB07+
B	7	T	NPADP+

B	8	D	MYCOC-
B	8	E	QB18B+
B	8	F	IOBRS-
B	8	M	B8MVJ+
B	8	P	PULSH+
B	8	T	SFHIB+
B	8	V	B8MVJ+

B	9	D	PWCIR+
B	9	E	LHBIN-
B	9	F	LHBIN+
B	9	J	PWCIR+
B	9	K	PIOUT-
B	9	L	PIOUT+
B	9	N	PWCIR+
B	9	P	ENDIN-
B	9	R	ENDIN+
B	9	T	IRFNB+
B	9	U	IRFNB-

FOKIA 8510

PRINTED IN U.S.A.

B 10
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HIMTT+
 PULSH-
 SETPO+
 MYCOS+
 OB22B-
 ENDOX+
 PADPP+
 TYIMP+
 SFIHB-
 TYIMP-
 LIBIN+
 LTYMP+

B 11
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DVSB3+
 DVSB4+
 DVXPN+
 DEVSL-
 DEVSL-
 IRFNB+
 IMPDA+
 IHB36-
 IHB36-
 HIMTC+
 HIMTC-
 HIMTC-

B 12
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MYCOC+
 OB24B-
 I26SD+
 I26SS+
 I26SS+
 MYCOC+
 OB24B-
 I27RD+
 I27RS+
 I27RS+
 MYCOC+
 OB24B-
 I27SD+
 I27SS+
 I27SS+

B 13
 B 13
 B 13
 B 13
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OB25B-
 OB25B+
 OB26B-
 OB26B+
 OB27B-

B	13	K	OB27B+
B	13	L	OB29B-
B	13	M	OB29B+
B	13	N	OB30B-
B	13	P	OB30B+
B	13	R	OB31B-
B	13	S	OB31B+
B	13	T	IHB36+
B	13	U	IHB36-

B	14	D	MYCOC+
B	14	E	OB28B-
B	14	F	I30SD+
B	14	H	I30SS+
B	14	J	I30SS+
B	14	K	MYCOC+
B	14	L	OB28B-
B	14	M	I31RD+
B	14	N	I31RS+
B	14	P	I31RS+
B	14	R	MYCOC+
B	14	S	OB28B-
B	14	T	I31SD+
B	14	U	I31SS+
B	14	V	I31SS+

B	15	D	OB29B+
B	15	E	I29RD+
B	15	F	OB29B-
B	15	H	I29SD+
B	15	J	OB30B+
B	15	K	I30RD+
B	15	L	OB30B-
B	15	M	I30SD+
B	15	N	OB31B+
B	15	P	I31RD+
B	15	R	OB31B-
B	15	S	I31SD+
B	15	T	PWCLR+
B	15	U	SIHBD+

B	16	D	MYCOC+
B	16	E	OB28B-
B	16	F	I29RD+
B	16	H	I29RS+
B	16	J	I29RS+
B	16	K	MYCOC+

FORM 8510

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B	16	L	OB28B-
B	16	M	I29SD+
B	16	N	I29SS+
B	16	P	I29SS+
B	16	R	MYCOC+
B	16	S	OB28B-
B	16	T	I30RD+
B	16	U	I30RS+
B	16	V	I30RS+

B	17	C	GDB17+
B	17	D	I29RS+
B	17	E	PIE29-
B	17	F	PIE29+
B	17	H	I29SS+
B	17	J	GDB17+
B	17	K	I30RS+
B	17	L	PIE30-
B	17	M	PIE30+
B	17	N	I30SS+
B	17	P	GDB17+
B	17	R	I31RS+
B	17	S	PIE31-
B	17	T	PIE31+
B	17	U	I31SS+
B	17	V	GDB17+

B	18	D	PIQVT-
B	18	E	PIE30-
B	18	F	PIE30+
B	18	H	PIE31+
B	18	J	PIE31-
B	18	K	PIE29-
B	18	L	PIE29+
B	18	N	IOPI4+
B	18	P	IOPI2+
B	18	R	IOPI6+
B	18	S	IOPI1+
B	18	T	IOPI5+
B	18	U	IOPI3+
B	18	V	IOPI7+

B	19	D	HIB03-
B	19	E	HIB04-
B	19	F	HIMTC+
B	19	H	HIB05-
B	19	J	HIB06-

B	19	K	HIMTC+
B	19	L	HIB07-
B	19	M	HIB08-
B	19	N	HIMTC+
B	19	P	HIB09-
B	19	R	HIB10-
B	19	S	HIMTC+
B	19	T	HIB11-
B	19	U	HIB12-
B	19	V	HIMTC+

B	20	D	HIB13-
B	20	E	HIB14-
B	20	F	HIMTC+
B	20	H	HIB15-
B	20	J	HIB16-
B	20	K	HIMTC+
B	20	L	HIB17-
B	20	M	HIB18-
B	20	N	HIMTC+
B	20	P	HIB19-
B	20	R	HIB20-
B	20	S	HIMTC+
B	20	T	CLHIB+
B	20	V	HIB01+

B	21	D	NPADP-
B	21	E	NPADP+
B	21	F	IOBRS-
B	21	H	IOBRS+
B	21	J	MYDOC+
B	21	K	MYDOC-
B	21	L	MYDOS+
B	21	M	MYDOS-
B	21	N	IMPDN+
B	21	P	IMRDY+
B	21	R	HIMTE+
B	21	S	HIMTC-
B	21	T	HIMTT-
B	21	U	HIMTE+
B	21	V	HIMTD+

B	22	D	HIB21-
B	22	E	HIB22-
B	22	F	HIMTD+
B	22	H	HIB23-
B	22	J	HIB24-

B	22	K	HIMTD+
B	22	L	HIB25-
B	22	M	HIB26-
B	22	N	HIMTD+
B	22	P	HIB27-
B	22	R	HIB28-
B	22	S	HIMTD+
B	22	T	HIB29-
B	22	U	HIB30-
B	22	V	HIMTD+

B	23	D	HIB31-
B	23	E	HIB32-
B	23	F	HIMTD+
B	23	H	HIB33-
B	23	J	HIB34-
B	23	K	HIMTD+
B	23	L	HIB35-
B	23	M	HIB36-
B	23	N	HIMTD+
B	23	P	HIB37-
B	23	S	HIMTD+
B	23	T	COGTE+
B	23	V	ENDIN+

B	24	C	GDB24+
B	24	D	IOB00+
B	24	E	OB00B+
B	24	F	IOB01+
B	24	H	OB01B+
B	24	J	IOB02+
B	24	K	OB02B+
B	24	L	IOB03+
B	24	M	OB03B+
B	24	N	IOB04+
B	24	P	OB04B+
B	24	R	IOB05+
B	24	S	OB05B+
B	24	T	IOB06+
B	24	U	OB06B+
B	24	V	GDB24+

B	25	C	GDB25+
B	25	D	IOB07+
B	25	E	OB07B+
B	25	F	IOB08+
B	25	H	OB08B+

FORM 8-10

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B	25	J	IOB09+
B	25	K	OB09B+
B	25	L	IOB10+
B	25	M	OB10B+
B	25	N	IOB11+
B	25	P	OB11B+
B	25	R	IOB12+
B	25	S	OB12B+
B	25	T	IOB13+
B	25	U	OB13B+
B	25	V	GDB25+

B	26	C	GDB26+
B	26	D	IOB14+
B	26	E	OB14B+
B	26	F	IOB15+
B	26	H	OB15B+
B	26	J	IOB16+
B	26	K	OB16B+
B	26	L	IOB17+
B	26	M	OB17B+
B	26	N	IOB18+
B	26	P	OB18B+
B	26	R	IOB19+
B	26	S	OB19B+
B	26	T	IOB20+
B	26	U	OB20B+
B	26	V	GDB26+

B	27	C	GDB27+
B	27	D	IOB21+
B	27	E	OB21B+
B	27	F	IOB22+
B	27	H	OB22B+
B	27	J	IOB23+
B	27	K	OB23B+
B	27	L	IOB24+
B	27	M	OB24B+
B	27	N	IOB25+
B	27	P	OB25B+
B	27	R	IOB26+
B	27	S	OB26B+
B	27	T	IOB27+
B	27	U	OB27B+
B	27	V	GDB27+

B	28	C	GDB28+
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FORM 5010

PRINTED IN U.S.A.

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IOB28+
 OB28B+
 IOB29+
 OB29B+
 IOB30+
 OB30B+
 IOB31+
 OB31B+
 IOB32+
 OB32B+
 IOB33+
 OB33B+
 IOB34+
 OB34B+
 GDB28+

B 29
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C
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GDB29+
 IOB35+
 OB35B+
 GDB29+

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MYCOC-
 MYCOC+
 MYCOC+
 MYCOS-
 MYCOS+
 MYCOS+
 MYDTI-
 MYDIA+
 MYDIA+
 MYDTI-
 MYDIB+
 MYDIB+
 MYCNI-
 MYCNI+
 MYCNI+

B 31
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IOBCI+
 DEVSL+
 MYCNI-
 OB20B-
 MYCOC+
 RHRDY+
 OB20B+
 MYCOC+
 SHRDY+
 CLIH-

B	31	R	ENDIN-
B	31	S	IRFNB-
B	31	T	CLHNB+
B	31	V	CLHNB-

B	32	D	IODOC+
B	32	E	DEVSL+
B	32	F	MYDOC-
B	32	H	IODOS+
B	32	J	DEVSL+
B	32	K	MYDOS-
B	32	L	IOCOC+
B	32	M	DEVSL+
B	32	N	MYCOC-
B	32	P	IOCOS+
B	32	R	DEVSL+
B	32	S	MYCOS-
B	32	T	IOBDI+
B	32	U	DEVSL+
B	32	V	MYDTI-

C	1	D	SFIH1+
C	1	E	IHB00+
C	1	F	MYDTI-
C	1	H	FULL0+
C	1	J	FULL1+
C	1	K	SFIH1+
C	1	L	IHB00-
C	1	N	SFIH1+
C	1	P	IHB01+
C	1	R	CLHNB+
C	1	S	IHB00-
C	1	T	IHB00+
C	1	U	SFIH1+
C	1	V	IHB01-

C	2	D	SFIH1+
C	2	E	IHB02-
C	2	H	IHB01+
C	2	J	IHB01-
C	2	K	SFIH1+
C	2	L	IHB02+
C	2	M	CLHNB+
C	2	N	SFIH1+
C	2	P	IHB03-
C	2	S	IHB02+
C	2	T	IHB02-

FORM 8510

PRINTED IN U.S.A.

C	2	U	SFIH1+
C	2	V	IHB03+

C	3	D	SFIH1+
C	3	E	IHB04-
C	3	H	IHB03+
C	3	J	IHB03-
C	3	K	SFIH1+
C	3	L	IHB04+
C	3	M	CLIHB+
C	3	N	SFIH1+
C	3	P	IHB05-
C	3	S	IHB04+
C	3	T	IHB04-
C	3	U	SFIH1+
C	3	V	IHB05+

C	4	D	SFIH1+
C	4	E	IHB06-
C	4	H	IHB05+
C	4	J	IHB05-
C	4	K	SFIH1+
C	4	L	IHB06+
C	4	M	CLIHB+
C	4	N	SFIH1+
C	4	P	IHB07-
C	4	S	IHB06+
C	4	T	IHB06-
C	4	U	SFIH1+
C	4	V	IHB07+

C	5	D	SFIH1+
C	5	E	IHB08-
C	5	H	IHB07+
C	5	J	IHB07-
C	5	K	SFIH1+
C	5	L	IHB08+
C	5	M	CLIHB+
C	5	N	SFIH1+
C	5	P	IHB09-
C	5	S	IHB08+
C	5	T	IHB08-
C	5	U	SFIH1+
C	5	V	IHB09+

C	6	D	SFIH1+
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<THROPE>PIN10D.LST;2

C	6	E	IHB10-
C	6	H	IHB09+
C	6	J	IHB09-
C	6	K	SFIH1+
C	6	L	IHB10+
C	6	M	CLIHB+
C	6	N	SFIH1+
C	6	P	IHB11-
C	6	S	IHB10+
C	6	T	IHB10-
C	6	U	SFIH1+
C	6	V	IHB11+

C	7	D	SFIH1+
C	7	E	IHB12-
C	7	H	IHB11+
C	7	J	IHB11-
C	7	K	SFIH1+
C	7	L	IHB12+
C	7	M	CLIHB+
C	7	N	SFIH1+
C	7	P	IHB13-
C	7	S	IHB12+
C	7	T	IHB12-
C	7	U	SFIH1+
C	7	V	IHB13+

C	8	D	SFIH2+
C	8	E	IHB14-
C	8	H	IHB13+
C	8	J	IHB13-
C	8	K	SFIH2+
C	8	L	IHB14+
C	8	M	CLIHB+
C	8	N	SFIH2+
C	8	P	IHB15-
C	8	S	IHB14+
C	8	T	IHB14-
C	8	U	SFIH2+
C	8	V	IHB15+

C	9	D	SFIH2+
C	9	E	IHB16-
C	9	H	IHB15+
C	9	J	IHB15-
C	9	K	SFIH2+
C	9	L	IHB16+

FORM 8510

PRINTED IN U.S.A.

C	9	M	CLHB+
C	9	N	SFIH2+
C	9	P	IHB17-
C	9	S	IHB16+
C	9	T	IHB16-
C	9	U	SFIH2+
C	9	V	IHB17+

C	10	D	SFIH2+
C	10	E	IHB18-
C	10	H	IHB17+
C	10	J	IHB17-
C	10	K	SFIH2+
C	10	L	IHB18+
C	10	M	CLHB+
C	10	N	SFIH2+
C	10	P	IHB19-
C	10	S	IHB18+
C	10	T	IHB18-
C	10	U	SFIH2+
C	10	V	IHB19+

C	11	D	SFIH2+
C	11	E	IHB20-
C	11	H	IHB19+
C	11	J	IHB19-
C	11	K	SFIH2+
C	11	L	IHB20+
C	11	M	CLHB+
C	11	N	SFIH2+
C	11	P	IHB21-
C	11	S	IHB20+
C	11	T	IHB20-
C	11	U	SFIH2+
C	11	V	IHB21+

C	12	D	SFIH2+
C	12	E	IHB22-
C	12	H	IHB21+
C	12	J	IHB21-
C	12	K	SFIH2+
C	12	L	IHB22+
C	12	M	CLHB+
C	12	N	SFIH2+
C	12	P	IHB23-
C	12	S	IHB22+
C	12	T	IHB22-

C	12	U	SFIH2+
C	12	V	IHB23+

C	13	D	SFIH2+
C	13	E	IHB24-
C	13	H	IHB23+
C	13	J	IHB23-
C	13	K	SFIH2+
C	13	L	IHB24+
C	13	M	CLIHB+
C	13	N	SFIH2+
C	13	P	IHB25-
C	13	S	IHB24+
C	13	T	IHB24-
C	13	U	SFIH2+
C	13	V	IHB25+

C	14	D	SFIH3+
C	14	E	IHB26-
C	14	H	IHB25+
C	14	J	IHB25-
C	14	K	SFIH3+
C	14	L	IHB26+
C	14	M	CLIHB+
C	14	N	SFIH3+
C	14	P	IHB27-
C	14	S	IHB26+
C	14	T	IHB26-
C	14	U	SFIH3+
C	14	V	IHB27+

C	15	D	SFIH3+
C	15	E	IHB28-
C	15	H	IHB27+
C	15	J	IHB27-
C	15	K	SFIH3+
C	15	L	IHB28+
C	15	M	CLIHB+
C	15	N	SFIH3+
C	15	P	IHB29-
C	15	S	IHB28+
C	15	T	IHB28-
C	15	U	SFIH3+
C	15	V	IHB29+

C	16	D	SFIH3+
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C	16	E	IHB30-
C	16	H	IHB29+
C	16	J	IHB29-
C	16	K	SFIH3+
C	16	L	IHB30+
C	16	M	CLIHB+
C	16	N	SFIH3+
C	16	P	IHB31-
C	16	S	IHB30+
C	16	T	IHB30-
C	16	U	SFIH3+
C	16	V	IHB31+

C	17	D	SFIH3+
C	17	E	IHB32-
C	17	H	IHB31+
C	17	J	IHB31-
C	17	K	SFIH3+
C	17	L	IHB32+
C	17	M	CLIHB+
C	17	N	SFIH3+
C	17	P	IHB33-
C	17	S	IHB32+
C	17	T	IHB32-
C	17	U	SFIH3+
C	17	V	IHB33+

C	18	D	SFIH3+
C	18	E	IHB34-
C	18	H	IHB33+
C	18	J	IHB33-
C	18	K	SFIH3+
C	18	L	IHB34+
C	18	M	CLIHB+
C	18	N	SFIH3+
C	18	P	IHB35-
C	18	S	IHB34+
C	18	T	IHB34-
C	18	U	SFIH3+
C	18	V	IHB35+

C	19	D	SFIH3+
C	19	E	IHB36-
C	19	F	CLIHB+
C	19	H	IHB35+
C	19	J	IHB35-
C	19	K	SFIH3+

C	19	L	IHB36+
C	20	D	DVSB5+
C	20	E	DVXPN+
C	20	F	DVSB6+
C	20	H	DVXPN+
C	20	J	DVSB7+
C	20	K	DVXPN+
C	20	L	DVSB8+
C	20	M	DVXPN+
C	20	N	DVSB9+
C	20	P	DVXPN+
C	20	R	PWCLR+
C	20	S	FULL1+
C	20	T	SETPO+
C	20	U	PIOUT-
C	21	D	OB33B+
C	21	E	I33RD+
C	21	F	OB33B-
C	21	H	I33SD+
C	21	J	OB34B+
C	21	K	I34RD+
C	21	L	OB34B-
C	21	M	I34SD+
C	21	N	OB35B+
C	21	P	I35RD+
C	21	R	OB35B-
C	21	S	I35SD+
C	22	D	MYCOC+
C	22	E	OB32B-
C	22	F	I33RD+
C	22	H	I33RS+
C	22	J	I33RS+
C	22	K	MYCOC+
C	22	L	OB32B-
C	22	M	I33SD+
C	22	N	I33SS+
C	22	P	I33SS+
C	22	R	MYCOC+
C	22	S	OB32B-
C	22	T	I34RD+
C	22	U	I34RS+
C	22	V	I34RS+

C	23	C	GDC23+
C	23	D	I33RS+
C	23	E	PIE33-
C	23	F	PIE33+
C	23	H	I33SS+
C	23	J	GDC23+
C	23	K	I34RS+
C	23	L	PIE34-
C	23	M	PIE34+
C	23	N	I34SS+
C	23	P	GDC23+
C	23	R	I35RS+
C	23	S	PIE35-
C	23	T	PIE35+
C	23	U	I35SS+
C	23	V	GDC23+

C	24	D	FULL0+
C	24	E	PIE34-
C	24	F	PIE34+
C	24	H	PIE35+
C	24	J	PIE35-
C	24	K	PIE33-
C	24	L	PIE33+
C	24	N	IOPI4+
C	24	P	IOPI2+
C	24	R	IOPI6+
C	24	S	IOPI1+
C	24	T	IOPI5+
C	24	U	IOPI3+
C	24	V	IOPI7+

C	25	C	GDC25+
C	25	D	IOB00+
C	25	E	IOB01+
C	25	F	GDC25+
C	25	H	IOB02+
C	25	J	GDC25+
C	25	K	IOB03+
C	25	L	GDC25+
C	25	M	IOB04+
C	25	N	GDC25+
C	25	P	IOB05+
C	25	R	GDC25+
C	25	S	IOB06+
C	25	T	IOB07+
C	25	U	GDC25+
C	25	V	IOB08+

C	26	C	GDC26+
C	26	D	IOB18+
C	26	E	IOB19+
C	26	F	GDC26+
C	26	H	IOB20+
C	26	J	GDC26+
C	26	K	IOB21+
C	26	L	GDC26+
C	26	M	IOB22+
C	26	N	GDC26+
C	26	P	IOB23+
C	26	R	GDC26+
C	26	S	IOB24+
C	26	T	IOB25+
C	26	U	GDC26+
C	26	V	IOB26+

C	27	C	GDC27+
C	27	D	IOBRS+
C	27	E	RSRVD+
C	27	F	GDC27+
C	27	H	SBC2H+
C	27	J	GDC27+
C	27	K	BDRSP+
C	27	L	GDC27+
C	27	M	IOS31+
C	27	N	GDC27+
C	27	P	IOS30+
C	27	R	GDC27+
C	27	S	IOS41+
C	27	T	IOS40+
C	27	U	GDC27+
C	27	V	IOS51+

C	28	C	GDC28+
C	28	D	IODOC+
C	28	E	IODOS+
C	28	F	GDC28+
C	28	H	IOCOC+
C	28	J	GDC28+
C	28	K	IOCOS+
C	28	L	GDC28+
C	28	M	IOBDI+
C	28	N	GDC28+
C	28	P	IOBCI+
C	28	R	GDC28+

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C	28	S	BRDIP+
C	28	T	BRDID+
C	28	U	GDC28+
C	28	V	SBC2V+

C	29	C	GDC29+
C	29	D	IOB00+
C	29	E	IOB01+
C	29	F	GDC29+
C	29	H	IOB02+
C	29	J	GDC29+
C	29	K	IOB03+
C	29	L	GDC29+
C	29	M	IOB04+
C	29	N	GDC29+
C	29	P	IOB05+
C	29	R	GDC29+
C	29	S	IOB06+
C	29	T	IOB07+
C	29	U	GDC29+
C	29	V	IOB08+

C	30	C	GDC30+
C	30	D	IOB18+
C	30	E	IOB19+
C	30	F	GDC30+
C	30	H	IOB20+
C	30	J	GDC30+
C	30	K	IOB21+
C	30	L	GDC30+
C	30	M	IOB22+
C	30	N	GDC30+
C	30	P	IOB23+
C	30	R	GDC30+
C	30	S	IOB24+
C	30	T	IOB25+
C	30	U	GDC30+
C	30	V	IOB26+

C	31	C	GDC31+
C	31	D	IOBRs+
C	31	E	RSRVD+
C	31	F	GDC31+
C	31	H	SBC2H+
C	31	J	GDC31+
C	31	K	BDRSP+
C	31	L	GDC31+

FORM 8-10

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C	31	M	IOS31+
C	31	N	GDC31+
C	31	P	IOS30+
C	31	R	GDC31+
C	31	S	IOS41+
C	31	T	IOS40+
C	31	U	GDC31+
C	31	V	IOS51+

C	32	C	GDC32+
C	32	D	IODOC+
C	32	E	IODOS+
C	32	F	GDC32+
C	32	H	IOCOC+
C	32	J	GDC32+
C	32	K	IOCOS+
C	32	L	GDC32+
C	32	M	IOBDI+
C	32	N	GDC32+
C	32	P	IOBCI+
C	32	R	GDC32+
C	32	S	BRDIP+
C	32	T	BRDID+
C	32	U	GDC32+
C	32	V	SBC2V+

D	1	C	GDD01+
D	1	D	IMRDY+
D	1	E	GDD01+
D	1	F	HMRDY+
D	1	H	HRDYT+
D	1	J	DHSTD+
D	1	K	DHSTD-
D	1	L	DTYHB+
D	1	M	DTYHB-
D	1	N	DRFNH+
D	1	P	DRFNH-
D	1	R	DLHBT+
D	1	S	DLHBT-

D	2	D	DIDAT+
D	2	E	DIDAT-
D	2	F	DTYIB+
D	2	H	DTYIB-
D	2	J	DRFNB+
D	2	K	DRFNB-
D	2	L	DLIBT+

D	2	M	DLIBT-
D	3	D	ARFNB-
D	3	F	DRFN3+
D	3	H	ARFNB+
D	3	K	DRFN3-
D	3	L	HIB00+
D	3	N	DHST3+
D	4	D	HIB00-
D	4	F	DHST3-
D	4	H	TYHBN+
D	4	K	DTYH3+
D	4	L	ATYHB-
D	4	N	DTYH3-
D	5	C	GDD05+
D	5	D	RHRDY+
D	5	H	RSDLY+
D	5	M	HMRDY+
D	5	R	HRDYT+
D	5	S	GDD05+
D	5	V	PWCLR+
D	6	D	IOS31+
D	6	E	DVSB3+
D	6	F	IOS30+
D	6	H	IOS41+
D	6	J	DVSB4+
D	6	K	IOS40+
D	6	L	IOS51+
D	6	M	DVSB5+
D	6	N	IOS50+
D	7	D	IOS61+
D	7	E	DVSB6+
D	7	F	IOS60+
D	7	H	IOS71+
D	7	J	DVSB7+
D	7	K	IOS70+
D	7	L	IOS81+
D	7	M	DVSB8+
D	7	N	IOS80+
D	7	P	IOS91+
D	7	R	DVSB9+

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D	7	S	IOS90+
D	8	F	SFIH1+
D	8	J	SFIHB+
D	8	M	SFIH2+
D	8	P	SFIHB+
D	8	T	SFIH3+
D	8	V	SFIHB+

D	9	C	GDD09+
D	9	D	PWCLR+
D	9	E	GDD09+
D	9	F	CLIH+
D	9	J	MYDIA+
D	9	U	GDD09+

D	10	D	IHB00+
D	10	E	IHB01+
D	10	F	MYDIA+
D	10	H	IOB00+
D	10	J	IOB01+
D	10	K	IHB02+
D	10	L	IHB03+
D	10	M	MYDIA+
D	10	N	IOB02+
D	10	P	IOB03+
D	10	R	IHB04+
D	10	S	IHB05+
D	10	T	MYDIA+
D	10	U	IOB04+
D	10	V	IOB05+

D	11	D	IHB06+
D	11	E	IHB07+
D	11	F	MYDIA+
D	11	H	IOB06+
D	11	J	IOB07+
D	11	K	IHB08+
D	11	L	IHB09+
D	11	M	MYDIA+
D	11	N	IOB08+
D	11	P	IOB09+
D	11	R	IHB10+
D	11	S	IHB11+
D	11	T	MYDIA+
D	11	U	IOB10+

D 11 V IOB11+

D	12	D	IHB12+
D	12	E	IHB13+
D	12	F	MYDIA+
D	12	H	IOB12+
D	12	J	IOB13+
D	12	K	IHB14+
D	12	L	IHB15+
D	12	M	MYDIA+
D	12	N	IOB14+
D	12	P	IOB15+
D	12	R	IHB16+
D	12	S	IHB17+
D	12	T	MYDIA+
D	12	U	IOB16+
D	12	V	IOB17+

D	13	C	GDIQB+
D	13	D	IOB18+
D	13	E	IOB19+
D	13	F	IOB20+
D	13	H	IHB20+
D	13	J	SHRDY+
D	13	L	MYDIB+
D	13	M	IHB19+
D	13	R	MYCNI+
D	13	S	IHB18+
D	13	V	GDIQB+

D	14	D	IOB21+
D	14	E	IOB22+
D	14	F	IOB23+
D	14	H	IHB23+
D	14	J	ENDIN+
D	14	L	MYDIB+
D	14	M	IHB22+
D	14	N	IMRDY+
D	14	R	MYCNI+
D	14	S	IHB21+
D	14	T	IMHBD+
D	14	V	GDIQB+

D	15	D	IOB24+
D	15	E	IOB25+
D	15	F	IOB26+

D	15	H	IHB26+
D	15	J	PIE26+
D	15	L	MYDIB+
D	15	M	IHB25+
D	15	N	PIE25+
D	15	R	MYCNI+
D	15	S	IHB24+
D	15	T	ENDIN+
D	15	V	GDIOB+

D	16	D	IOB27+
D	16	E	IOB28+
D	16	F	IOB29+
D	16	H	IHB29+
D	16	J	PIE29+
D	16	L	MYDIB+
D	16	M	IHB28+
D	16	N	PIOUT+
D	16	R	MYCNI+
D	16	S	IHB27+
D	16	T	PIE27+
D	16	V	GDIOB+

D	17	D	IOB30+
D	17	E	IOB31+
D	17	F	IOB32+
D	17	H	IHB32+
D	17	J	FULL1+
D	17	L	MYDIB+
D	17	M	IHB31+
D	17	N	PIE31+
D	17	R	MYCNI+
D	17	S	IHB30+
D	17	T	PIE30+
D	17	V	GDIOB+

D	18	D	IOB33+
D	18	E	IOB34+
D	18	F	IOB35+
D	18	H	IHB35+
D	18	J	PIE35+
D	18	L	MYDIB+
D	18	M	IHB34+
D	18	N	PIE34+
D	18	R	MYCNI+
D	18	S	IHB33+
D	18	T	PIE33+

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D	18	V	GDI0B+
D	19	D	OB25B+
D	19	E	I25RD+
D	19	F	OB25B-
D	19	H	I25SD+
D	19	J	OB26B+
D	19	K	I26RD+
D	19	L	OB26B-
D	19	M	I26SD+
D	19	N	OB27B+
D	19	P	I27RD+
D	19	R	OB27B-
D	19	S	I27SD+
D	20	D	MYCOC+
D	20	E	OB24B-
D	20	F	I25RD+
D	20	H	I25RS+
D	20	J	I25RS+
D	20	K	MYCOC+
D	20	L	OB24B-
D	20	M	I25SD+
D	20	N	I25SS+
D	20	P	I25SS+
D	20	R	MYCOC+
D	20	S	OB24B-
D	20	T	I26RD+
D	20	U	I26RS+
D	20	V	I26RS+
D	21	C	GDD21+
D	21	D	I25RS+
D	21	E	PIE25-
D	21	F	PIE25+
D	21	H	I25SS+
D	21	J	GDD21+
D	21	K	I26RS+
D	21	L	PIE26-
D	21	M	PIE26+
D	21	N	I26SS+
D	21	P	GDD21+
D	21	R	I27RS+
D	21	S	PIE27-
D	21	T	PIE27+
D	21	U	I27SS+
D	21	V	GDD21+

D	22	D	ENDIN-
D	22	E	PIE26-
D	22	F	PIE26+
D	22	H	PIE27+
D	22	J	PIE27-
D	22	K	PIE25-
D	22	L	PIE25+
D	22	N	IOPI4+
D	22	P	IOPI2+
D	22	R	IOPI6+
D	22	S	IOPI1+
D	22	T	IOPI5+
D	22	U	IOPI3+
D	22	V	IOPI7+

D	23	D	OB33B-
D	23	E	OB33B+
D	23	F	OB34B-
D	23	H	OB34B+
D	23	J	OB35B-
D	23	K	OB35B+
D	23	L	DEVSL+
D	23	M	DEVSL-
D	23	N	OB22B-
D	23	P	OB22B+
D	23	R	OB21B-
D	23	S	OB21B+
D	23	T	TYHBN+
D	23	U	ATYHB-

D	24	D	MYCOC+
D	24	E	OB32B-
D	24	F	I34SD+
D	24	H	I34SS+
D	24	J	I34SS+
D	24	K	MYCOC+
D	24	L	OB32B-
D	24	M	I35RD+
D	24	N	I35RS+
D	24	P	I35RS+
D	24	R	MYCOC+
D	24	S	OB32B-
D	24	T	I35SD+
D	24	U	I35SS+
D	24	V	I35SS+

D	25	C	GDD25+
D	25	D	IOB09+
D	25	E	IOB10+
D	25	F	GDD25+
D	25	H	IOB11+
D	25	J	GDD25+
D	25	K	IOB12+
D	25	L	GDD25+
D	25	M	IOB13+
D	25	N	GDD25+
D	25	P	IOB14+
D	25	R	GDD25+
D	25	S	IOB15+
D	25	T	IOB16+
D	25	U	GDD25+
D	25	V	IOB17+

D	26	C	GDD26+
D	26	D	IOB27+
D	26	E	IOB28+
D	26	F	GDD26+
D	26	H	IOB29+
D	26	J	GDD26+
D	26	K	IOB30+
D	26	L	GDD26+
D	26	M	IOB31+
D	26	N	GDD26+
D	26	P	IOB32+
D	26	R	GDD26+
D	26	S	IOB33+
D	26	T	IOB34+
D	26	U	GDD26+
D	26	V	IOB35+

D	27	C	GDD27+
D	27	D	IOS50+
D	27	E	IOS61+
D	27	F	GDD27+
D	27	H	IOS60+
D	27	J	GDD27+
D	27	K	IOS71+
D	27	L	GDD27+
D	27	M	IOS70+
D	27	N	GDD27+
D	27	P	IOS81+
D	27	R	GDD27+
D	27	S	IOS80+

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D	27	T	IOS91+
D	27	U	GDD27+
D	27	V	IOS90+
D	28	C	GDD28+
D	28	D	SBC2D+
D	28	E	SBC2E+
D	28	F	GDD28+
D	28	H	IOPI1+
D	28	J	GDD28+
D	28	K	IOPI2+
D	28	L	GDD28+
D	28	M	IOPI3+
D	28	N	GDD28+
D	28	P	IOPI4+
D	28	R	GDD28+
D	28	S	IOPI5+
D	28	T	IOPI6+
D	28	U	GDD28+
D	28	V	IOPI7+
D	29	C	GDD29+
D	29	D	IOB09+
D	29	E	IOB10+
D	29	F	GDD29+
D	29	H	IOB11+
D	29	J	GDD29+
D	29	K	IOB12+
D	29	L	GDD29+
D	29	M	IOB13+
D	29	N	GDD29+
D	29	P	IOB14+
D	29	R	GDD29+
D	29	S	IOB15+
D	29	T	IOB16+
D	29	U	GDD29+
D	29	V	IOB17+
D	30	C	GDD30+
D	30	D	IOB27+
D	30	E	IOB28+
D	30	F	GDD30+
D	30	H	IOB29+
D	30	J	GDD30+
D	30	K	IOB30+
D	30	L	GDD30+
D	30	M	IOB31+

FORM 3510

D	30	N	GDD30+
D	30	P	IOB32+
D	30	R	GDD30+
D	30	S	IOB33+
D	30	T	IOB34+
D	30	U	GDD30+
D	30	V	IOB35+

D	31	C	GDD31+
D	31	D	IOS50+
D	31	E	IOS61+
D	31	F	GDD31+
D	31	H	IOS60+
D	31	J	GDD31+
D	31	K	IOS71+
D	31	L	GDD31+
D	31	M	IOS70+
D	31	N	GDD31+
D	31	P	IOS81+
D	31	R	GDD31+
D	31	S	IOS80+
D	31	T	IOS91+
D	31	U	GDD31+
D	31	V	IOS90+

D	32	C	GDD32+
D	32	D	SBC2D+
D	32	E	SBC2E+
D	32	F	GDD32+
D	32	H	IOPI1+
D	32	J	GDD32+
D	32	K	IOPI2+
D	32	L	GDD32+
D	32	M	IOPI3+
D	32	N	GDD32+
D	32	P	IOPI4+
D	32	R	GDD32+
D	32	S	IOPI5+
D	32	T	IOPI6+
D	32	U	GDD32+
D	32	V	IOPI7+

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FORM 9310

PRINTED IN U.S.A.

A	6	J	A6JKJ+
A	6	K	A6JKJ+
A	6	R	A6RCJ+
A	6	S	A6STJ+
A	6	T	A6STJ+
B	6	N	AAPAD+
B	6	M	AAPAD+
B	6	V	APADP+
B	7	R	APADP+
A	5	T	ARFNB+
B	2	P	ARFNB+
D	3	H	ARFNB+
B	2	N	ARFNB-
D	3	D	ARFNB-
A	2	F	ATYHB+
B	2	V	ATYHB+
B	2	T	ATYHB-
D	4	L	ATYHB-
D	23	U	ATYHB-
B	6	J	B6JKJ+
B	6	K	B6JKJ+
B	6	S	B6STJ+
B	6	T	B6STJ+
B	8	M	B8MVJ+
B	8	V	B8MVJ+

FORM 8510

PRINTED IN U.S.A.

C	27	K	BDRSP+
C	31	K	BDRSP+

C	28	T	BRDID+
C	32	T	BRDID+

C	28	S	BRDIP+
C	32	S	BRDIP+

A	1	J	BTAVL+
A	2	E	BTAVL+
B	4	E	BTAVL+

A	8	S	CLHBD+
A	10	J	CLHBD+

A	11	F	CLHIB+
A	14	F	CLHIB+
A	15	F	CLHIB+
A	16	F	CLHIB+
A	17	F	CLHIB+
A	18	F	CLHIB+
A	19	F	CLHIB+
A	20	F	CLHIB+
A	21	F	CLHIB+
A	22	F	CLHIB+
A	23	F	CLHIB+
A	24	F	CLHIB+
A	25	F	CLHIB+
A	26	F	CLHIB+
A	27	F	CLHIB+
A	28	F	CLHIB+
A	29	F	CLHIB+
A	30	F	CLHIB+
A	31	F	CLHIB+
B	20	T	CLHIB+

B	31	T	CLHIB+
C	1	R	CLHIB+
C	2	M	CLHIB+
C	3	M	CLHIB+
C	4	M	CLHIB+
C	5	M	CLHIB+

C	6	M	CLINB+
C	7	M	CLINB+
C	8	M	CLINB+
C	9	M	CLINB+
C	10	M	CLINB+
C	11	M	CLINB+
C	12	M	CLINB+
C	13	M	CLINB+
C	14	M	CLINB+
C	15	M	CLINB+
C	16	M	CLINB+
C	17	M	CLINB+
C	18	M	CLINB+
C	19	F	CLINB+
D	9	F	CLINB+
B	31	P	CLINB-
B	31	V	CLINB-
A	8	N	COGTE+
B	4	N	COGTE+
B	23	T	COGTE+
B	31	E	DEVSL+
B	32	E	DEVSL+
B	32	J	DEVSL+
B	32	M	DEVSL+
B	32	R	DEVSL+
B	32	U	DEVSL+
D	23	L	DEVSL+
B	11	H	DEVSL-
B	11	J	DEVSL-
D	23	M	DEVSL-
D	3	N	DHST3+
D	4	F	DHST3-
D	1	J	DHSTD+
D	1	K	DHSTD-

FORM 8510

PRINTED IN U.S.A.

A	3	S	DIDAT+
D	2	D	DIDAT+
A	3	R	DIDAT-
D	2	E	DIDAT-
A	32	F	DLHB3+
A	32	K	DLHB3-
D	1	R	DLHBT+
D	1	S	DLHBT-
A	3	E	DLIBT+
D	2	L	DLIBT+
A	3	D	DLIBT-
D	2	M	DLIBT-
D	3	F	DRFN3+
D	3	K	DRFN3-
D	2	J	DRFNB+
D	2	K	DRFNB-
A	4	E	DRFNH+
D	1	N	DRFNH+
A	4	D	DRFNH-
D	1	P	DRFNH-

FORM 8310

PRINTED IN U.S.A.

A	1	D	DS1PU+
A	1	V	DS1PU+
B	5	M	DS1PU+
D	4	K	DTYH3+
D	4	N	DTYH3-
D	1	L	DTYHB+
D	1	M	DTYHB-
A	3	L	DTYIB+
D	2	F	DTYIB+
A	3	K	DTYIB-
D	2	H	DTYIB-
B	11	D	DVSB3+
D	6	E	DVSB3+
B	11	E	DVSB4+
D	6	J	DVSB4+
C	20	D	DVSB5+
D	6	M	DVSB5+
C	20	F	DVSB6+
D	7	E	DVSB6+
C	20	J	DVSB7+
D	7	J	DVSB7+
C	20	L	DVSB8+
D	7	M	DVSB8+
C	20	N	DVSB9+

FORM 5310

PRINTED IN U.S.A.

D	7	R	DVSB9+
B	11	F	DVXPN+
C	20	E	DVXPN+
C	20	H	DVXPN+
C	20	K	DVXPN+
C	20	M	DVXPN+
C	20	P	DVXPN+
B	9	R	ENDIN+
B	23	V	ENDIN+
D	14	J	ENDIN+
D	15	T	ENDIN+
A	8	K	ENDIN-
B	9	P	ENDIN-
B	31	R	ENDIN-
D	22	D	ENDIN-
A	1	N	ENDOT+
B	1	N	ENDOT+
B	4	F	ENDOT+
B	4	J	ENDOT+
B	10	K	ENDOX+
A	1	M	ENDOX+
A	1	R	FFFFF+
B	1	U	FFFFF+
A	8	D	FULL0+
B	3	H	FULL0+
C	1	H	FULL0+
C	24	D	FULL0+
A	8	H	FULL1+
C	1	J	FULL1+
C	20	S	FULL1+
D	17	J	FULL1+
A	1	C	GDA01+

A	1	H	GDA01+
A	1	K	GDA01+
A	1	S	GDA01+
A	1	U	GDA01+
A	5	C	GDA05+
A	5	E	GDA05+
A	5	H	GDA05+
A	6	C	GDA06+
A	6	F	GDA06+
A	6	P	GDA06+
A	11	C	GDA11+
A	11	E	GDA11+
A	11	H	GDA11+
A	12	C	GDA12+
A	12	E	GDA12+
A	12	L	GDA12+
A	12	S	GDA12+
A	31	C	GDA31+
A	31	S	GDA31+
A	31	U	GDA31+
B	5	C	GDB05+
B	5	F	GDB05+
B	5	P	GDB05+
B	6	C	GDB06+
B	6	F	GDB06+
B	6	P	GDB06+
B	7	C	GDB07+
B	7	E	GDB07+
B	7	L	GDB07+
B	7	S	GDB07+
B	17	C	GDB17+
B	17	J	GDB17+

B	17	P	GDB17+
B	17	V	GDB17+
B	24	C	GDB24+
B	24	V	GDB24+
B	25	C	GDB25+
B	25	V	GDB25+
B	26	C	GDB26+
B	26	V	GDB26+
B	27	C	GDB27+
B	27	V	GDB27+
B	28	C	GDB28+
B	28	V	GDB28+
B	29	C	GDB29+
B	29	V	GDB29+
C	23	C	GDC23+
C	23	J	GDC23+
C	23	P	GDC23+
C	23	V	GDC23+
C	25	C	GDC25+
C	25	F	GDC25+
C	25	J	GDC25+
C	25	L	GDC25+
C	25	N	GDC25+
C	25	R	GDC25+
C	25	U	GDC25+
C	26	C	GDC26+
C	26	F	GDC26+
C	26	J	GDC26+
C	26	L	GDC26+
C	26	N	GDC26+
C	26	R	GDC26+
C	26	U	GDC26+

FORM 8510
PRINTED IN U.S.A.

C	27	C	GDC27+
C	27	F	GDC27+
C	27	J	GDC27+
C	27	L	GDC27+
C	27	N	GDC27+
C	27	R	GDC27+
C	27	U	GDC27+

C	28	C	GDC28+
C	28	F	GDC28+
C	28	J	GDC28+
C	28	L	GDC28+
C	28	N	GDC28+
C	28	R	GDC28+
C	28	U	GDC28+

C	29	C	GDC29+
C	29	F	GDC29+
C	29	J	GDC29+
C	29	L	GDC29+
C	29	N	GDC29+
C	29	R	GDC29+
C	29	U	GDC29+

C	30	C	GDC30+
C	30	F	GDC30+
C	30	J	GDC30+
C	30	L	GDC30+
C	30	N	GDC30+
C	30	R	GDC30+
C	30	U	GDC30+

C	31	C	GDC31+
C	31	F	GDC31+
C	31	J	GDC31+
C	31	L	GDC31+
C	31	N	GDC31+
C	31	R	GDC31+
C	31	U	GDC31+

C	32	C	GDC32+
C	32	F	GDC32+
C	32	J	GDC32+

FORM 8510

PRINTED IN U.S.A.

C	32	L	GDC32+
C	32	N	GDC32+
C	32	R	GDC32+
C	32	U	GDC32+
D	1	C	GDD01+
D	1	E	GDD01+
D	5	C	GDD05+
D	5	S	GDD05+
D	9	C	GDD09+
D	9	E	GDD09+
D	9	U	GDD09+
D	21	C	GDD21+
D	21	J	GDD21+
D	21	P	GDD21+
D	21	V	GDD21+
D	25	C	GDD25+
D	25	F	GDD25+
D	25	J	GDD25+
D	25	L	GDD25+
D	25	N	GDD25+
D	25	R	GDD25+
D	25	U	GDD25+
D	26	C	GDD26+
D	26	F	GDD26+
D	26	J	GDD26+
D	26	L	GDD26+
D	26	N	GDD26+
D	26	R	GDD26+
D	26	U	GDD26+
D	27	C	GDD27+
D	27	F	GDD27+
D	27	J	GDD27+
D	27	L	GDD27+
D	27	N	GDD27+
D	27	R	GDD27+
D	27	U	GDD27+

FORM 35-10

D	28	C	GDD28+
D	28	F	GDD28+
D	28	J	GDD28+
D	28	L	GDD28+
D	28	N	GDD28+
D	28	R	GDD28+
D	28	U	GDD28+

D	29	C	GDD29+
D	29	F	GDD29+
D	29	J	GDD29+
D	29	L	GDD29+
D	29	N	GDD29+
D	29	R	GDD29+
D	29	U	GDD29+

D	30	C	GDD30+
D	30	F	GDD30+
D	30	J	GDD30+
D	30	L	GDD30+
D	30	N	GDD30+
D	30	R	GDD30+
D	30	U	GDD30+

D	31	C	GDD31+
D	31	F	GDD31+
D	31	J	GDD31+
D	31	L	GDD31+
D	31	N	GDD31+
D	31	R	GDD31+
D	31	U	GDD31+

D	32	C	GDD32+
D	32	F	GDD32+
D	32	J	GDD32+
D	32	L	GDD32+
D	32	N	GDD32+
D	32	R	GDD32+
D	32	U	GDD32+

D	13	C	GDI0B+
D	13	V	GDI0B+
D	14	V	GDI0B+

FORM 8310
PRINTED IN U.S.A.

D	15	V	GDIOB+
D	16	V	GDIOB+
D	17	V	GDIOB+
D	18	V	GDIOB+
A	13	J	HIB00+
D	3	L	HIB00+
A	13	E	HIB00-
D	4	D	HIB00-
A	13	L	HIB01+
A	13	P	HIB01+
B	20	V	HIB01+
A	13	K	HIB01-
A	13	R	HIB01-
A	13	U	HIB02+
A	14	J	HIB02+
A	13	T	HIB02-
A	14	E	HIB02-
A	14	L	HIB03+
A	14	P	HIB03+
A	14	K	HIB03-
A	14	R	HIB03-
B	19	D	HIB03-
A	14	U	HIB04+
A	15	J	HIB04+
A	14	T	HIB04-
A	15	E	HIB04-
B	19	E	HIB04-
A	15	L	HIB05+

A	15	P	HIB05+
A	15	K	HIB05-
A	15	R	HIB05-
B	19	H	HIB05-
A	15	U	HIB06+
A	16	J	HIB06+
A	15	T	HIB06-
A	16	E	HIB06-
B	19	J	HIB06-
A	16	L	HIB07+
A	16	P	HIB07+
A	16	K	HIB07-
A	16	R	HIB07-
B	19	L	HIB07-
A	16	U	HIB08+
A	17	J	HIB08+
A	16	T	HIB08-
A	17	E	HIB08-
B	19	M	HIB08-
A	17	L	HIB09+
A	17	P	HIB09+
A	17	K	HIB09-
A	17	R	HIB09-
B	19	P	HIB09-
A	17	U	HIB10+
A	18	J	HIB10+
A	17	T	HIB10-
A	18	E	HIB10-

B	19	R	HIB10-
A	18	L	HIB11+
A	18	P	HIB11+
A	18	K	HIB11-
A	18	R	HIB11-
B	19	T	HIB11-
A	18	U	HIB12+
A	19	J	HIB12+
A	18	T	HIB12-
A	19	E	HIB12-
B	19	U	HIB12-
A	19	L	HIB13+
A	19	P	HIB13+
A	19	K	HIB13-
A	19	R	HIB13-
B	20	D	HIB13-
A	19	U	HIB14+
A	20	J	HIB14+
A	19	T	HIB14-
A	20	E	HIB14-
B	20	E	HIB14-
A	20	L	HIB15+
A	20	P	HIB15+
A	20	K	HIB15-
A	20	R	HIB15-
B	20	H	HIB15-
A	20	U	HIB16+
A	21	J	HIB16+

A	20	T	HIB16-
A	21	E	HIB16-
B	20	J	HIB16-
A	21	L	HIB17+
A	21	P	HIB17+
A	21	K	HIB17-
A	21	R	HIB17-
B	20	L	HIB17-
A	21	U	HIB18+
A	22	J	HIB18+
A	21	T	HIB18-
A	22	E	HIB18-
B	20	M	HIB18-
A	22	L	HIB19+
A	22	P	HIB19+
A	22	K	HIB19-
A	22	R	HIB19-
B	20	P	HIB19-
A	22	U	HIB20+
A	23	J	HIB20+
A	22	T	HIB20-
A	23	E	HIB20-
B	20	R	HIB20-
A	23	L	HIB21+
A	23	P	HIB21+
A	23	K	HIB21-
A	23	R	HIB21-
B	22	D	HIB21-

A	23	U	HIB22+
A	24	J	HIB22+
A	23	T	HIB22-
A	24	E	HIB22-
B	22	E	HIB22-
A	24	L	HIB23+
A	24	P	HIB23+
A	24	K	HIB23-
A	24	R	HIB23-
B	22	H	HIB23-
A	24	U	HIB24+
A	25	J	HIB24+
A	24	T	HIB24-
A	25	E	HIB24-
B	22	J	HIB24-
A	25	L	HIB25+
A	25	P	HIB25+
A	25	K	HIB25-
A	25	R	HIB25-
B	22	L	HIB25-
A	25	U	HIB26+
A	26	J	HIB26+
A	25	T	HIB26-
A	26	E	HIB26-
B	22	M	HIB26-
A	26	L	HIB27+
A	26	P	HIB27+

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A	26	K	HIB27-
A	26	R	HIB27-
B	22	P	HIB27-
A	26	U	HIB28+
A	27	J	HIB28+
A	26	T	HIB28-
A	27	E	HIB28-
B	22	R	HIB28-
A	27	L	HIB29+
A	27	P	HIB29+
A	27	K	HIB29-
A	27	R	HIB29-
B	22	T	HIB29-
A	27	U	HIB30+
A	28	J	HIB30+
A	27	T	HIB30-
A	28	E	HIB30-
B	22	U	HIB30-
A	28	L	HIB31+
A	28	P	HIB31+
A	28	K	HIB31-
A	28	R	HIB31-
B	23	D	HIB31-
A	28	U	HIB32+
A	29	J	HIB32+
A	28	T	HIB32-
A	29	E	HIB32-
B	23	E	HIB32-

A	29	L	HIB33+
A	29	P	HIB33+
A	29	K	HIB33-
A	29	R	HIB33-
B	23	H	HIB33-
A	29	U	HIB34+
A	30	J	HIB34+
A	29	T	HIB34-
A	30	E	HIB34-
B	23	J	HIB34-
A	30	L	HIB35+
A	30	P	HIB35+
A	30	K	HIB35-
A	30	R	HIB35-
B	23	L	HIB35-
A	30	U	HIB36+
A	31	J	HIB36+
A	30	T	HIB36-
A	31	E	HIB36-
B	23	M	HIB36-
A	31	L	HIB37+
A	31	P	HIB37+
A	31	K	HIB37-
A	31	R	HIB37-
B	23	P	HIB37-
B	11	T	HIMTC+
B	19	F	HIMTC+
B	19	K	HIMTC+
B	19	N	HIMTC+

B	19	S	HIMTC+
B	19	V	HIMTC+
B	20	F	HIMTC+
B	20	K	HIMTC+
B	20	N	HIMTC+
B	20	S	HIMTC+

B	11	U	HIMTC-
B	11	V	HIMTC-
B	21	S	HIMTC-

B	21	V	HIMTD+
B	22	F	HIMTD+
B	22	K	HIMTD+
B	22	N	HIMTD+
B	22	S	HIMTD+
B	22	V	HIMTD+
B	23	F	HIMTD+
B	23	K	HIMTD+
B	23	N	HIMTD+
B	23	S	HIMTD+

B	21	R	HIMTE+
B	21	U	HIMTE+

A	9	F	HIMTT+
B	10	D	HIMTT+

A	9	H	HIMTT-
B	21	T	HIMTT-

D	1	F	HMRDY+
D	5	M	HMRDY+

D	1	H	HRDYT+
D	5	R	HRDYT+

D	19	E	I25RD+
D	20	F	I25RD+

D	20	H	I25RS+
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FORM 8510

PRINTED IN U.S.A.

D	20	J	I25RS+
D	21	D	I25RS+
D	19	H	I25SD+
D	20	M	I25SD+
D	20	N	I25SS+
D	20	P	I25SS+
D	21	H	I25SS+
D	19	K	I26RD+
D	20	T	I26RD+
D	20	U	I26RS+
D	20	V	I26RS+
D	21	K	I26RS+
B	12	F	I26SD+
D	19	M	I26SD+
B	12	H	I26SS+
B	12	J	I26SS+
D	21	N	I26SS+
B	12	M	I27RD+
D	19	P	I27RD+
B	12	N	I27RS+
B	12	P	I27RS+
D	21	R	I27RS+
B	12	T	I27SD+
D	19	S	I27SD+
B	12	U	I27SS+
B	12	V	I27SS+
D	21	U	I27SS+
B	15	E	I29RD+

FORM 8510

PRINTED IN U.S.A.

B	16	F	I29RD+
B	16	H	I29RS+
B	16	J	I29RS+
B	17	D	I29RS+
B	15	H	I29SD+
B	16	M	I29SD+
B	16	N	I29SS+
B	16	P	I29SS+
B	17	H	I29SS+
B	15	K	I30RD+
B	16	T	I30RD+
B	16	U	I30RS+
B	16	V	I30RS+
B	17	K	I30RS+
B	14	F	I30SD+
B	15	M	I30SD+
B	14	H	I30SS+
B	14	J	I30SS+
B	17	N	I30SS+
B	14	M	I31RD+
B	15	P	I31RD+
B	14	N	I31RS+
B	14	P	I31RS+
B	17	R	I31RS+
B	14	T	I31SD+
B	15	S	I31SD+
B	14	U	I31SS+
B	14	V	I31SS+

B	17	U	I31SS+
C	21	E	I33RD+
C	22	F	I33RD+
C	22	H	I33RS+
C	22	J	I33RS+
C	23	D	I33RS+
C	21	H	I33SD+
C	22	M	I33SD+
C	22	N	I33SS+
C	22	P	I33SS+
C	23	H	I33SS+
C	21	K	I34RD+
C	22	T	I34RD+
C	22	U	I34RS+
C	22	V	I34RS+
C	23	K	I34RS+
C	21	M	I34SD+
D	24	F	I34SD+
C	23	N	I34SS+
D	24	H	I34SS+
D	24	J	I34SS+
C	21	P	I35RD+
D	24	M	I35RD+
C	23	R	I35RS+
D	24	N	I35RS+
D	24	P	I35RS+
C	21	S	I35SD+
D	24	T	I35SD+

C	23	U	I35SS+
D	24	U	I35SS+
D	24	V	I35SS+
C	1	E	IHB00+
C	1	T	IHB00+
D	10	D	IHB00+
C	1	L	IHB00-
C	1	S	IHB00-
C	1	P	IHB01+
C	2	H	IHB01+
D	10	E	IHB01+
C	1	V	IHB01-
C	2	J	IHB01-
C	2	L	IHB02+
C	2	S	IHB02+
D	10	K	IHB02+
C	2	E	IHB02-
C	2	T	IHB02-
C	2	V	IHB03+
C	3	H	IHB03+
D	10	L	IHB03+
C	2	P	IHB03-
C	3	J	IHB03-
C	3	L	IHB04+
C	3	S	IHB04+
D	10	R	IHB04+
C	3	E	IHB04-
C	3	T	IHB04-

C	3	V	IHB05+
C	4	H	IHB05+
D	10	S	IHB05+

C	3	P	IHB05-
C	4	J	IHB05-

C	4	L	IHB06+
C	4	S	IHB06+
D	11	D	IHB06+

C	4	E	IHB06-
C	4	T	IHB06-

C	4	V	IHB07+
C	5	H	IHB07+
D	11	E	IHB07+

C	4	P	IHB07-
C	5	J	IHB07-

C	5	L	IHB08+
C	5	S	IHB08+
D	11	K	IHB08+

C	5	E	IHB08-
C	5	T	IHB08-

C	5	V	IHB09+
C	6	H	IHB09+
D	11	L	IHB09+

C	5	P	IHB09-
C	6	J	IHB09-

C	6	L	IHB10+
C	6	S	IHB10+
D	11	R	IHB10+

C	6	E	IHB10-
C	6	T	IHB10-
C	6	V	IHB11+
C	7	H	IHB11+
D	11	S	IHB11+
C	6	P	IHB11-
C	7	J	IHB11-
C	7	L	IHB12+
C	7	S	IHB12+
D	12	D	IHB12+
C	7	E	IHB12-
C	7	T	IHB12-
C	7	V	IHB13+
C	8	H	IHB13+
D	12	E	IHB13+
C	7	P	IHB13-
C	8	J	IHB13-
C	8	L	IHB14+
C	8	S	IHB14+
D	12	K	IHB14+
C	8	E	IHB14-
C	8	T	IHB14-
C	8	V	IHB15+
C	9	H	IHB15+
D	12	L	IHB15+
C	8	P	IHB15-
C	9	J	IHB15-

FORM 8510

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C	9	L	IHB16+
C	9	S	IHB16+
D	12	R	IHB16+
C	9	E	IHB16-
C	9	T	IHB16-
C	9	V	IHB17+
C	10	H	IHB17+
D	12	S	IHB17+
C	9	P	IHB17-
C	10	J	IHB17-
C	10	L	IHB18+
C	10	S	IHB18+
D	13	S	IHB18+
C	10	E	IHB18-
C	10	T	IHB18-
C	10	V	IHB19+
C	11	H	IHB19+
D	13	M	IHB19+
C	10	P	IHB19-
C	11	J	IHB19-
C	11	L	IHB20+
C	11	S	IHB20+
D	13	H	IHB20+
C	11	E	IHB20-
C	11	T	IHB20-
C	11	V	IHB21+
C	12	H	IHB21+
D	14	S	IHB21+

C	11	P	IHB21-
C	12	J	IHB21-
C	12	L	IHB22+
C	12	S	IHB22+
D	14	M	IHB22+
C	12	E	IHB22-
C	12	T	IHB22-
C	12	V	IHB23+
C	13	H	IHB23+
D	14	H	IHB23+
C	12	P	IHB23-
C	13	J	IHB23-
C	13	L	IHB24+
C	13	S	IHB24+
D	15	S	IHB24+
C	13	E	IHB24-
C	13	T	IHB24-
C	13	V	IHB25+
C	14	H	IHB25+
D	15	M	IHB25+
C	13	P	IHB25-
C	14	J	IHB25-
C	14	L	IHB26+
C	14	S	IHB26+
D	15	H	IHB26+
C	14	E	IHB26-
C	14	T	IHB26-

C	14	V	IHB27+
C	15	H	IHB27+
D	16	S	IHB27+
C	14	P	IHB27-
C	15	J	IHB27-
C	15	L	IHB28+
C	15	S	IHB28+
D	16	M	IHB28+
C	15	E	IHB28-
C	15	T	IHB28-
C	15	V	IHB29+
C	16	H	IHB29+
D	16	H	IHB29+
C	15	P	IHB29-
C	16	J	IHB29-
C	16	L	IHB30+
C	16	S	IHB30+
D	17	S	IHB30+
C	16	E	IHB30-
C	16	T	IHB30-
C	16	V	IHB31+
C	17	H	IHB31+
D	17	M	IHB31+
C	16	P	IHB31-
C	17	J	IHB31-
C	17	L	IHB32+
C	17	S	IHB32+
D	17	H	IHB32+

C	17	E	IHB32-
C	17	T	IHB32-
C	17	V	IHB33+
C	18	H	IHB33+
D	18	S	IHB33+
C	17	P	IHB33-
C	18	J	IHB33-
C	18	L	IHB34+
C	18	S	IHB34+
D	18	M	IHB34+
C	18	E	IHB34-
C	18	T	IHB34-
C	18	V	IHB35+
C	19	H	IHB35+
D	18	H	IHB35+
C	18	P	IHB35-
C	19	J	IHB35-
B	13	T	IHB36+
C	19	L	IHB36+
B	11	N	IHB36-
B	11	P	IHB36-
B	13	U	IHB36-
C	19	E	IHB36-
A	10	L	IMHBD+
D	14	T	IMHBD+
A	3	U	IMPDA+
B	11	L	IMPDA+
A	10	M	IMPDN+

B	21	N	IMPDN+
A	5	F	IMRDY+
B	21	P	IMRDY+
D	1	D	IMRDY+
D	14	N	IMRDY+
B	24	D	IOB00+
C	25	D	IOB00+
C	29	D	IOB00+
D	10	H	IOB00+
B	24	F	IOB01+
C	25	E	IOB01+
C	29	E	IOB01+
D	10	J	IOB01+
B	24	J	IOB02+
C	25	H	IOB02+
C	29	H	IOB02+
D	10	N	IOB02+
B	24	L	IOB03+
C	25	K	IOB03+
C	29	K	IOB03+
D	10	P	IOB03+
B	24	N	IOB04+
C	25	M	IOB04+
C	29	M	IOB04+
D	10	U	IOB04+
B	24	R	IOB05+
C	25	P	IOB05+
C	29	P	IOB05+
D	10	V	IOB05+
B	24	T	IOB06+
C	25	S	IOB06+
C	29	S	IOB06+
D	11	H	IOB06+

FORM 8510

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B	25	D	IOB07+
C	25	T	IOB07+
C	29	T	IOB07+
D	11	J	IOB07+

B	25	F	IOB08+
C	25	V	IOB08+
C	29	V	IOB08+
D	11	N	IOB08+

B	25	J	IOB09+
D	11	P	IOB09+
D	25	D	IOB09+
D	29	D	IOB09+

B	25	L	IOB10+
D	11	U	IOB10+
D	25	E	IOB10+
D	29	E	IOB10+

B	25	N	IOB11+
D	11	V	IOB11+
D	25	H	IOB11+
D	29	H	IOB11+

B	25	R	IOB12+
D	12	H	IOB12+
D	25	K	IOB12+
D	29	K	IOB12+

B	25	T	IOB13+
D	12	J	IOB13+
D	25	M	IOB13+
D	29	M	IOB13+

B	26	D	IOB14+
D	12	N	IOB14+
D	25	P	IOB14+
D	29	P	IOB14+

B	26	F	IOB15+
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FORM 8910

PRINTED IN U.S.A.

D	12	P	IOB15+
D	25	S	IOB15+
D	29	S	IOB15+
B	26	J	IOB16+
D	12	U	IOB16+
D	25	T	IOB16+
D	29	T	IOB16+
B	26	L	IOB17+
D	12	V	IOB17+
D	25	V	IOB17+
D	29	V	IOB17+
B	26	N	IOB18+
C	26	D	IOB18+
C	30	D	IOB18+
D	13	D	IOB18+
B	26	R	IOB19+
C	26	E	IOB19+
C	30	E	IOB19+
D	13	E	IOB19+
B	26	T	IOB20+
C	26	H	IOB20+
C	30	H	IOB20+
D	13	F	IOB20+
B	27	D	IOB21+
C	26	K	IOB21+
C	30	K	IOB21+
D	14	D	IOB21+
B	27	F	IOB22+
C	26	M	IOB22+
C	30	M	IOB22+
D	14	E	IOB22+
B	27	J	IOB23+
C	26	P	IOB23+
C	30	P	IOB23+

D	14	F	I0B23+
B	27	L	I0B24+
C	26	S	I0B24+
C	30	S	I0B24+
D	15	D	I0B24+
B	27	N	I0B25+
C	26	T	I0B25+
C	30	T	I0B25+
D	15	E	I0B25+
B	27	R	I0B26+
C	26	V	I0B26+
C	30	V	I0B26+
D	15	F	I0B26+
B	27	T	I0B27+
D	16	D	I0B27+
D	26	D	I0B27+
D	30	D	I0B27+
B	28	D	I0B28+
D	16	E	I0B28+
D	26	E	I0B28+
D	30	E	I0B28+
B	28	F	I0B29+
D	16	F	I0B29+
D	26	H	I0B29+
D	30	H	I0B29+
B	28	J	I0B30+
D	17	D	I0B30+
D	26	K	I0B30+
D	30	K	I0B30+
B	28	L	I0B31+
D	17	E	I0B31+
D	26	M	I0B31+
D	30	M	I0B31+

FORM 5010

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B	28	N	IOB32+
D	17	F	IOB32+
D	26	P	IOB32+
D	30	P	IOB32+

B	28	R	IOB33+
D	18	D	IOB33+
D	26	S	IOB33+
D	30	S	IOB33+

B	28	T	IOB34+
D	18	E	IOB34+
D	26	T	IOB34+
D	30	T	IOB34+

1) B 28-30
2) D 30-V
P 02-07

B	29	D	IOB35+
D	18	F	IOB35+
D	26	V	IOB35+
D	30	V	IOB35+

B	31	D	IOBCI+
C	28	P	IOBCI+
C	32	P	IOBCI+

B	32	T	IOBDI+
C	28	M	IOBDI+
C	32	M	IOBDI+

B	21	H	IOBRS+
C	27	D	IOBRS+
C	31	D	IOBRS+

A	6	N	IOBRS-
B	21	F	IOBRS-
B	8	F	IOBRS-

B	32	L	IOCOC+
C	28	H	IOCOC+
C	32	H	IOCOC+

B	32	P	IOCOS+
C	28	K	IOCOS+
C	32	K	IOCOS+
B	32	D	IODOC+
C	28	D	IODOC+
C	32	D	IODOC+
B	32	H	IODOS+
C	28	E	IODOS+
C	32	E	IODOS+
B	18	S	IOPI1+
C	24	S	IOPI1+
D	22	S	IOPI1+
D	28	H	IOPI1+
D	32	H	IOPI1+
B	18	P	IOPI2+
C	24	P	IOPI2+
D	22	P	IOPI2+
D	28	K	IOPI2+
D	32	K	IOPI2+
B	18	U	IOPI3+
C	24	U	IOPI3+
D	22	U	IOPI3+
D	28	M	IOPI3+
D	32	M	IOPI3+
B	18	N	IOPI4+
C	24	N	IOPI4+
D	22	N	IOPI4+
D	28	P	IOPI4+
D	32	P	IOPI4+
B	18	T	IOPI5+
C	24	T	IOPI5+
D	22	T	IOPI5+
D	28	S	IOPI5+
D	32	S	IOPI5+

B	18	R	IOPI6+
C	24	R	IOPI6+
D	22	R	IOPI6+
D	28	T	IOPI6+
D	32	T	IOPI6+

B	18	V	IOPI7+
C	24	V	IOPI7+
D	22	V	IOPI7+
D	28	V	IOPI7+
D	32	V	IOPI7+

C	27	P	IOS30+
C	31	P	IOS30+
D	6	F	IOS30+

C	27	M	IOS31+
C	31	M	IOS31+
D	6	D	IOS31+

C	27	T	IOS40+
C	31	T	IOS40+
D	6	K	IOS40+

C	27	S	IOS41+
C	31	S	IOS41+
D	6	H	IOS41+

D	6	N	IOS50+
D	27	D	IOS50+
D	31	D	IOS50+

C	27	V	IOS51+
C	31	V	IOS51+
D	6	L	IOS51+

D	7	F	IOS60+
D	27	H	IOS60+
D	31	H	IOS60+

D	7	D	IOS61+
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FORM 8510

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D	27	E	IOS61+
D	31	E	IOS61+
D	7	K	IOS70+
D	27	M	IOS70+
D	31	M	IOS70+
D	7	H	IOS71+
D	27	K	IOS71+
D	31	K	IOS71+
D	7	N	IOS80+
D	27	S	IOS80+
D	31	S	IOS80+
D	7	L	IOS81+
D	27	P	IOS81+
D	31	P	IOS81+
D	7	S	IOS90+
D	27	V	IOS90+
D	31	V	IOS90+
D	7	P	IOS91+
D	27	T	IOS91+
D	31	T	IOS91+
A	5	U	IRFNB+
B	3	K	IRFNB+
B	9	T	IRFNB+
B	11	K	IRFNB+
B	4	P	IRFNB-
B	9	U	IRFNB-
B	31	S	IRFNB-
B	5	J	JKJB5+
B	5	K	JKJB5+
A	11	T	LDHI1+

FORM 8510

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A	13	M	LDHI1+
A	13	V	LDHI1+
A	14	M	LDHI1+
A	14	V	LDHI1+
A	15	M	LDHI1+
A	15	V	LDHI1+
A	16	M	LDHI1+
A	16	V	LDHI1+
A	17	M	LDHI1+
A	17	V	LDHI1+
A	18	M	LDHI1+
A	18	V	LDHI1+
A	19	M	LDHI1+
A	19	V	LDHI1+
A	20	M	LDHI1+
A	20	V	LDHI1+
A	21	M	LDHI1+
A	21	V	LDHI1+
A	22	M	LDHI1+

A	11	M	LDHI2+
A	22	V	LDHI2+
A	23	M	LDHI2+
A	23	V	LDHI2+
A	24	M	LDHI2+
A	24	V	LDHI2+
A	25	M	LDHI2+
A	25	V	LDHI2+
A	26	M	LDHI2+
A	26	V	LDHI2+
A	27	M	LDHI2+
A	27	V	LDHI2+
A	28	M	LDHI2+
A	28	V	LDHI2+
A	29	M	LDHI2+
A	29	V	LDHI2+
A	30	M	LDHI2+
A	30	V	LDHI2+
A	31	M	LDHI2+
A	31	V	LDHI2+

A	32	D	LHBIN+
B	4	M	LHBIN+
B	9	F	LHBIN+

A	32	H	LHBIN-
B	4	H	LHBIN-

B	9	E	LHBIN-
A	3	H	LIBIN+
B	10	U	LIBIN+
A	8	U	LTYP+
B	3	J	LTYP+
B	10	V	LTYP+
B	3	N	MYCNI+
B	30	U	MYCNI+
B	30	V	MYCNI+
D	13	R	MYCNI+
D	14	R	MYCNI+
D	15	R	MYCNI+
D	16	R	MYCNI+
D	17	R	MYCNI+
D	18	R	MYCNI+
B	30	T	MYCNI-
B	31	F	MYCNI-
A	8	L	MYCOC+
A	8	P	MYCOC+
B	1	H	MYCOC+
B	1	L	MYCOC+
B	12	D	MYCOC+
B	12	K	MYCOC+
B	12	R	MYCOC+
B	14	D	MYCOC+
B	14	K	MYCOC+
B	14	R	MYCOC+
B	16	D	MYCOC+
B	16	K	MYCOC+
B	16	R	MYCOC+
B	30	E	MYCOC+
B	30	F	MYCOC+
B	31	J	MYCOC+
B	31	M	MYCOC+
C	22	D	MYCOC+
C	22	K	MYCOC+
C	22	R	MYCOC+
D	20	D	MYCOC+
D	20	K	MYCOC+
D	20	R	MYCOC+

D	24	D	MYCOC+
D	24	K	MYCOC+
D	24	R	MYCOC+

B	30	D	MYCOC-
B	32	N	MYCOC-
B	8	D	MYCOC-

B	10	H	MYCOS+
B	30	J	MYCOS+
B	30	K	MYCOS+

B	30	H	MYCOS-
B	32	S	MYCOS-

B	3	S	MYDIA+
B	30	M	MYDIA+
B	30	N	MYDIA+
D	9	J	MYDIA+
D	10	F	MYDIA+
D	10	M	MYDIA+
D	10	T	MYDIA+
D	11	F	MYDIA+
D	11	M	MYDIA+
D	11	T	MYDIA+
D	12	F	MYDIA+
D	12	M	MYDIA+
D	12	T	MYDIA+

B	3	V	MYDIB+
B	30	R	MYDIB+
B	30	S	MYDIB+
D	13	L	MYDIB+
D	14	L	MYDIB+
D	15	L	MYDIB+
D	16	L	MYDIB+
D	17	L	MYDIB+
D	18	L	MYDIB+

B	21	J	MYDOC+
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A	11	J	MYDOC-
B	3	E	MYDOC-

FORM 8510

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B	4	L	MYDOC-
B	21	K	MYDOC-
B	32	F	MYDOC-
B	1	T	MYDOS+
B	21	L	MYDOS+
A	11	P	MYDOS-
A	11	V	MYDOS-
B	5	E	MYDOS-
B	21	M	MYDOS-
B	32	K	MYDOS-
B	30	L	MYDTI-
B	30	P	MYDTI-
B	32	V	MYDTI-
C	1	F	MYDTI-
B	7	T	NPADP+
B	21	E	NPADP+
A	8	E	NPADP-
A	8	J	NPADP-
B	21	D	NPADP-
A	13	S	QB00B+
B	24	E	QB00B+
A	14	H	QB01B+
B	24	H	QB01B+
A	14	S	QB02B+
B	24	K	QB02B+
A	15	H	QB03B+
B	24	M	QB03B+
A	15	S	QB04B+
B	24	P	QB04B+

A	16	H	OB05B+
B	24	S	OB05B+
A	16	S	OB06B+
B	24	U	OB06B+
A	17	H	OB07B+
B	25	E	OB07B+
A	17	S	OB08B+
B	25	H	OB08B+
A	18	H	OB09B+
B	25	K	OB09B+
A	18	S	OB10B+
B	25	M	OB10B+
A	19	H	OB11B+
B	25	P	OB11B+
A	19	S	OB12B+
B	25	S	OB12B+
A	20	H	OB13B+
B	25	U	OB13B+
A	20	S	OB14B+
B	26	E	OB14B+
A	21	H	OB15B+
B	26	H	OB15B+
A	21	S	OB16B+
B	26	K	OB16B+
A	22	H	OB17B+

FORM 8510

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B	26	M	OB17B+
B	8	E	OB18B+
A	22	S	OB18B+
B	26	P	OB18B+
A	23	H	OB19B+
B	2	H	OB19B+
B	26	S	OB19B+
A	8	R	OB19B-
B	2	F	OB19B-
A	9	E	OB20B+
A	23	S	OB20B+
B	26	U	OB20B+
B	31	L	OB20B+
A	9	D	OB20B-
B	31	H	OB20B-
A	24	H	OB21B+
B	27	E	OB21B+
D	23	S	OB21B+
B	1	J	OB21B-
D	23	R	OB21B-
A	24	S	OB22B+
B	27	H	OB22B+
D	23	P	OB22B+
B	10	J	OB22B-
B	1	M	OB22B-
D	23	N	OB22B-
A	9	U	OB23B+
A	25	H	OB23B+
B	27	K	OB23B+

A	8	M	OB23B-
A	9	T	OB23B-
A	9	M	OB24B+
A	25	S	OB24B+
B	27	M	OB24B+
A	9	L	OB24B-
B	12	E	OB24B-
B	12	L	OB24B-
B	12	S	OB24B-
D	20	E	OB24B-
D	20	L	OB24B-
D	20	S	OB24B-
A	26	H	OB25B+
B	13	E	OB25B+
B	27	P	OB25B+
D	19	D	OB25B+
B	13	D	OB25B-
D	19	F	OB25B-
A	26	S	OB26B+
B	13	H	OB26B+
B	27	S	OB26B+
D	19	J	OB26B+
B	13	F	OB26B-
D	19	L	OB26B-
A	27	H	OB27B+
B	13	K	OB27B+
B	27	U	OB27B+
D	19	N	OB27B+
B	13	J	OB27B-
D	19	R	OB27B-
A	9	P	OB28B+

A	27	S	QB28B+
B	28	E	QB28B+

A	9	N	QB28B-
B	14	E	QB28B-
B	14	L	QB28B-
B	14	S	QB28B-
B	16	E	QB28B-
B	16	L	QB28B-
B	16	S	QB28B-

A	28	H	QB29B+
B	13	M	QB29B+
B	15	D	QB29B+
B	28	H	QB29B+

B	13	L	QB29B-
B	15	F	QB29B-

A	28	S	QB30B+
B	13	P	QB30B+
B	15	J	QB30B+
B	28	K	QB30B+

B	13	N	QB30B-
B	15	L	QB30B-

A	29	H	QB31B+
B	13	S	QB31B+
B	15	N	QB31B+
B	28	M	QB31B+

B	13	R	QB31B-
B	15	R	QB31B-

A	9	S	QB32B+
A	29	S	QB32B+
B	28	P	QB32B+

A	9	R	QB32B-
C	22	E	QB32B-

FORM 5310

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C	22	L	OB32B-
C	22	S	OB32B-
D	24	E	OB32B-
D	24	L	OB32B-
D	24	S	OB32B-
A	30	H	OB33B+
B	28	S	OB33B+
C	21	D	OB33B+
D	23	E	OB33B+
C	21	F	OB33B-
D	23	D	OB33B-
A	30	S	OB34B+
B	28	U	OB34B+
C	21	J	OB34B+
D	23	H	OB34B+
C	21	L	OB34B-
D	23	F	OB34B-
A	31	H	OB35B+
B	29	E	OB35B+
C	21	N	OB35B+
D	23	K	OB35B+
C	21	R	OB35B-
D	23	J	OB35B-
A	8	F	PADPP+
A	8	T	PADPP+
B	10	L	PADPP+
B	4	S	PIE25+
D	15	N	PIE25+
D	21	F	PIE25+
D	22	L	PIE25+
D	21	E	PIE25-
D	22	K	PIE25-

FORM 8510

PRINTED IN U.S.A.

B	4	U	PIE26+
D	15	J	PIE26+
D	21	M	PIE26+
D	22	F	PIE26+
D	21	L	PIE26-
D	22	E	PIE26-
A	7	E	PIE27+
D	16	T	PIE27+
D	21	T	PIE27+
D	22	H	PIE27+
D	21	S	PIE27-
D	22	J	PIE27-
A	7	H	PIE29+
B	17	F	PIE29+
B	18	L	PIE29+
D	16	J	PIE29+
B	17	E	PIE29-
B	18	K	PIE29-
A	7	K	PIE30+
B	17	M	PIE30+
B	18	F	PIE30+
D	17	T	PIE30+
B	17	L	PIE30-
B	18	E	PIE30-
A	7	M	PIE31+
B	17	T	PIE31+
B	18	H	PIE31+
D	17	N	PIE31+
B	17	S	PIE31-
B	18	J	PIE31-

A	7	P	PIE33+
C	23	F	PIE33+
C	24	L	PIE33+
D	18	T	PIE33+

C	23	B	PIE33-
C	24	K	PIE33-

A	7	S	PIE34+
C	23	M	PIE34+
C	24	F	PIE34+
D	18	N	PIE34+

C	23	L	PIE34-
C	24	E	PIE34-

A	7	U	PIE35+
C	23	T	PIE35+
C	24	H	PIE35+
D	18	J	PIE35+

C	23	S	PIE35-
C	24	J	PIE35-

B	3	F	PIOUT+
B	4	K	PIOUT+
B	9	L	PIOUT+
D	16	N	PIOUT+

B	9	K	PIOUT-
B	18	D	PIOUT-
C	20	U	PIOUT-

B	1	R	PRPLS+
B	1	V	PRPLS+

A	12	D	PRPLS-
A	12	K	PRPLS-
A	12	R	PRPLS-

B 1 S PRPLS-

B 2 E PULSH+

B 7 F PULSH+

B 8 P PULSH+

B 2 D PULSH-

B 10 E PULSH-

A 1 F PWCLR+

A 7 D PWCLR+

A 7 F PWCLR+

A 7 J PWCLR+

A 7 L PWCLR+

A 7 N PWCLR+

A 7 R PWCLR+

A 7 T PWCLR+

A 10 D PWCLR+

A 11 D PWCLR+

B 3 L PWCLR+

B 3 P PWCLR+

B 3 T PWCLR+

B 4 R PWCLR+

B 4 T PWCLR+

B 9 D PWCLR+

B 9 J PWCLR+

B 9 N PWCLR+

B 15 T PWCLR+

C 20 R PWCLR+

D 5 V PWCLR+

D 9 D PWCLR+

A 5 D PWRUP+

B 1 D RFNBD+

B 5 V RFNBD+

B 1 F RFNBD-

B 2 U RFNBD-

A 2 D RFNNB+

A 4 H RFNNB+

B 5 N RFNNB+

B 7 D RFNNE+

A 10 F RHRDY+
B 31 K RHRDY+
D 5 D RHRDY+

A 6 V RSDLY+
D 5 H RSDLY+

C 27 E RSRVD+
C 31 E RSRVD+

D 28 D SBC2D+
D 32 D SBC2D+

D 28 E SBC2E+
D 32 E SBC2E+

C 27 H SBC2H+
C 31 H SBC2H+

C 28 V SBC2V+
C 32 V SBC2V+

B 4 D SETPO+
B 10 F SETPO+
C 20 T SETPO+

A 12 F SFHI1+
A 13 D SFHI1+
A 13 N SFHI1+
A 14 D SFHI1+
A 14 N SFHI1+
A 15 D SFHI1+
A 15 N SFHI1+
A 16 D SFHI1+
A 16 N SFHI1+
A 17 D SFHI1+
A 17 N SFHI1+
A 18 D SFHI1+
A 18 N SFHI1+

A	19	D	SFHI1+
A	12	M	SFHI2+
A	19	N	SFHI2+
A	20	D	SFHI2+
A	20	N	SFHI2+
A	21	D	SFHI2+
A	21	N	SFHI2+
A	22	D	SFHI2+
A	22	N	SFHI2+
A	23	D	SFHI2+
A	23	N	SFHI2+
A	24	D	SFHI2+
A	24	N	SFHI2+
A	25	D	SFHI2+
A	25	N	SFHI2+

A	12	T	SFHI3+
A	26	D	SFHI3+
A	26	N	SFHI3+
A	27	D	SFHI3+
A	27	N	SFHI3+
A	28	D	SFHI3+
A	28	N	SFHI3+
A	29	D	SFHI3+
A	29	N	SFHI3+
A	30	D	SFHI3+
A	30	N	SFHI3+
A	31	D	SFHI3+
A	31	N	SFHI3+

A	12	J	SFHIB+
A	12	P	SFHIB+
A	12	V	SFHIB+
B	8	T	SFHIB+

C	1	D	SFIH1+
C	1	K	SFIH1+
C	1	N	SFIH1+
C	1	U	SFIH1+
C	2	D	SFIH1+
C	2	K	SFIH1+
C	2	N	SFIH1+
C	2	U	SFIH1+
C	3	D	SFIH1+
C	3	K	SFIH1+

C	3	N	SFIH1+
C	3	U	SFIH1+
C	4	D	SFIH1+
C	4	K	SFIH1+
C	4	N	SFIH1+
C	4	U	SFIH1+
C	5	D	SFIH1+
C	5	K	SFIH1+
C	5	N	SFIH1+
C	5	U	SFIH1+
C	6	D	SFIH1+
C	6	K	SFIH1+
C	6	N	SFIH1+
C	6	U	SFIH1+
C	7	D	SFIH1+
C	7	K	SFIH1+
C	7	N	SFIH1+
C	7	U	SFIH1+
D	8	F	SFIH1+
C	8	D	SFIH2+
C	8	K	SFIH2+
C	8	N	SFIH2+
C	8	U	SFIH2+
C	9	D	SFIH2+
C	9	K	SFIH2+
C	9	N	SFIH2+
C	9	U	SFIH2+
C	10	D	SFIH2+
C	10	K	SFIH2+
C	10	N	SFIH2+
C	10	U	SFIH2+
C	11	D	SFIH2+
C	11	K	SFIH2+
C	11	N	SFIH2+
C	11	U	SFIH2+
C	12	D	SFIH2+
C	12	K	SFIH2+
C	12	N	SFIH2+
C	12	U	SFIH2+
C	13	D	SFIH2+
C	13	K	SFIH2+
C	13	N	SFIH2+
C	13	U	SFIH2+
D	8	M	SFIH2+
C	14	D	SFIH3+
C	14	K	SFIH3+

C	14	N	SFIH3+
C	14	J	SFIH3+
C	15	D	SFIH3+
C	15	K	SFIH3+
C	15	N	SFIH3+
C	15	U	SFIH3+
C	16	D	SFIH3+
C	16	K	SFIH3+
C	16	N	SFIH3+
C	16	U	SFIH3+
C	17	D	SFIH3+
C	17	K	SFIH3+
C	17	N	SFIH3+
C	17	U	SFIH3+
C	18	D	SFIH3+
C	18	K	SFIH3+
C	18	N	SFIH3+
C	18	U	SFIH3+
C	19	D	SFIH3+
C	19	K	SFIH3+
D	8	T	SFIH3+

B	2	L	SFIHB+
D	8	J	SFIHB+
D	8	P	SFIHB+
D	8	V	SFIHB+

B	2	M	SFIHB-
B	10	N	SFIHB-

A	10	E	SHRDY+
B	31	N	SHRDY+
D	13	J	SHRDY+

A	10	K	SIHBD+
B	15	U	SIHBD+

B	5	S	STJB5+
B	5	T	STJB5+

B	1	K	STOPO+
B	3	D	STOPO+

A	8	V	STPAD+
B	2	S	STPAD+
B	2	R	STPAD-
B	6	E	STPAD-
D	4	H	TYHBN+
D	23	T	TYHBN+
A	2	K	TYIDN+
A	5	V	TYIDN+
A	9	K	TYIMP+
B	7	M	TYIMP+
B	10	M	TYIMP+
A	9	J	TYIMP-
B	10	T	TYIMP-
A	5	S	TYIND+
A	5	M	TYIND+
A	2	H	TYIND-
A	5	R	TYIND-
A	3	N	TYINN+
B	2	K	TYINN+
A	2	J	TYINN-
A	6	E	TYINN-
B	2	J	TYINN-
B	7	K	TYINN-

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APPENDIX A

Reprinted from Section 4 of BBN Report No. 1822

"Specifications for the Interconnection of
a Host and an IMP"

4. HARDWARE REQUIREMENTS AND DESCRIPTION

A local Host is connected to the IMP through a Host cable (provided with the IMP), which joins a *standard Host/IMP interface unit* in the IMP to a *special Host/IMP interface unit* in the Host. A distant Host is connected to an augmented standard Host/IMP interface through a cable provided by the Host. The structure of the standard Host/IMP interface, the IMP/Host handshaking procedure, the end-of-message indication, the Master Ready lines, and the signals on the Host cable are all described in detail below. A very distant Host is connected via communications circuits to a *modem interface unit* as described in Appendix F.

The special interface should be designed by the Host personnel to operate in conjunction with the standard Host/IMP interface or the augmented interface as the case may be. *We have not, however, attempted to specify the special Host/IMP interface in any detail.* We recommend that the special interface be modeled after the standard interface, and, in the remainder of this section, we assume that it will be. It should be noted that the special interface must be operated in a *full duplex* mode*. A simplified schematic drawing of a special Host/IMP interface is included in Appendix B to assist Host personnel in the design of the special interface. The distant Host modification to the standard interface affects only the cable and the method of cable driving; it does not change the basic operation of the interface.

*Those few Hosts which originally implemented half duplex interfaces have had inordinate difficulties of various kinds. See, for example, Section 3.1.

4.1 Structure of the Standard Host/IMP Interface

The standard Host/IMP interface is a full duplex bit-serial unit that is logically divided into a Host-to-IMP section and an IMP-to-Host section. Each section contains a 16-bit shift register (and control logic), one of which is for shifting bits to the Host and the other for receiving bits from the Host. A simplified picture of the Host/IMP interface is shown in Figure 4-1.

The technique of transferring information between the Host and the IMP is identical in each direction; we will, therefore, refer to the *sender* and the *receiver* without specifying the Host or IMP explicitly. In general, words are taken one by one from the sender's memory and transferred bit serially across the interface to the receiver, where they are reassembled into words of the appropriate (i.e., receiver's) length and stored into the receiver's memory. The transmission thus consists of a bit train containing no special indications of word boundaries but delayed occasionally while the sender fetches, or the receiver stores, a word. *The high-order bit of each word is transmitted first.*

Bit transfer is asynchronous, the transmission of each bit being controlled by a *Ready-For-Next-Bit, There's-Your-Bit* handshaking procedure. Each bit is transferred only when both sender and receiver indicate preparedness. This permits either the sender or the receiver to hold up the transmission between any two bits in order to take as much time as necessary to get a new word from memory, to tuck an assembled word into memory, or to activate an interrupt routine that sets up new input or output buffers. Neither the sender nor the receiver should expect transmission to take place at a pre-determined bit rate and each must be able to accept arbitrary delays introduced by the other at any point in the bit train.

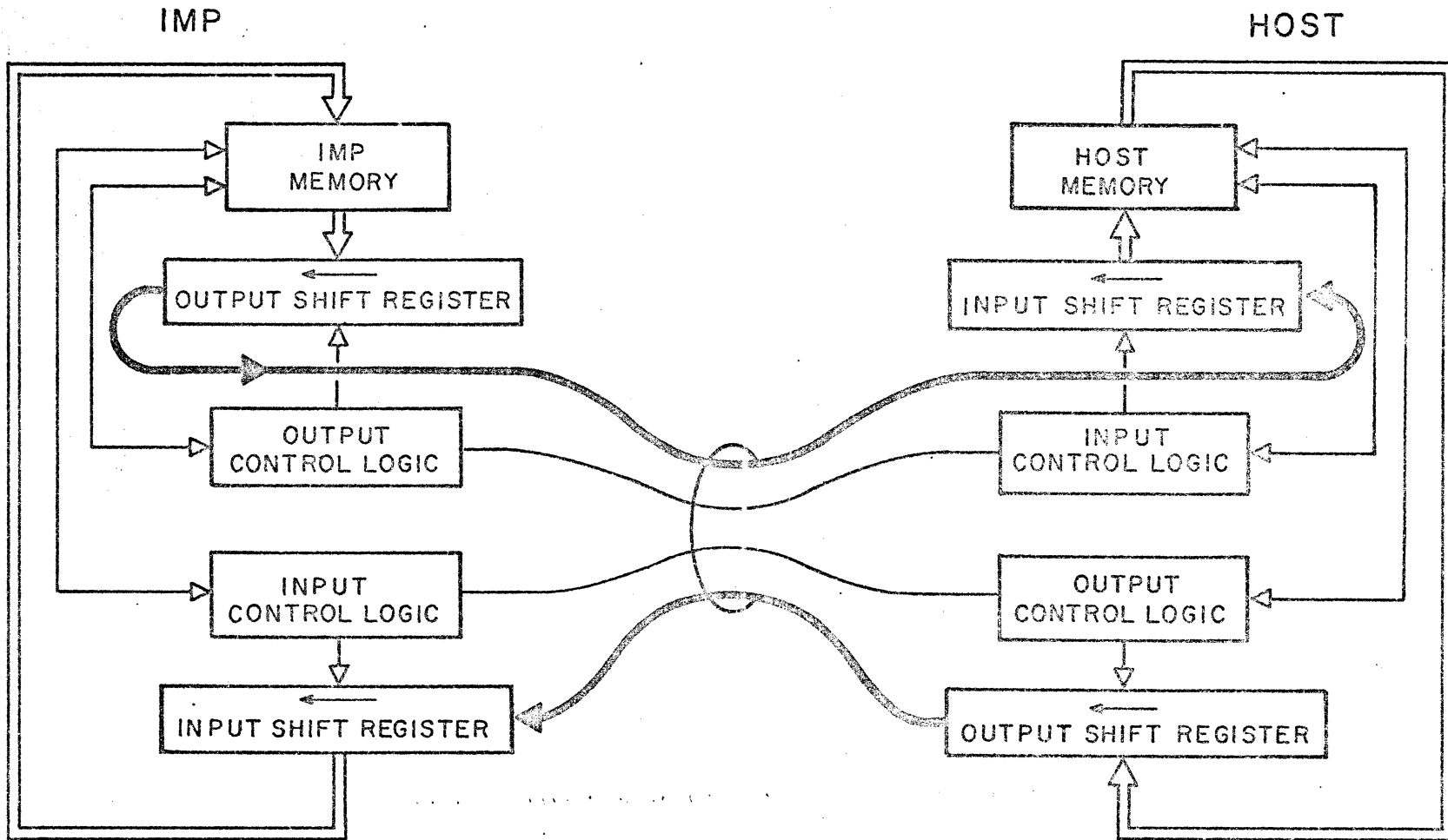


Figure 4-1. Simplified Illustration of Host/IMP Interface

The design of an asynchronous interface was selected for two reasons: first, because of the inherently asynchronous nature of the process by which words of one length are fetched from one machine and reformed into words of another length and stored in another machine; and, secondly, because such a design allows a variety of special Host/IMP interfaces to be designed independent of stringent timing specifications that may be difficult or impossible for certain Hosts to meet.

4.2 IMP/Host Handshaking

Figure 4-2 shows a much simplified version of the control logic for the bit-by-bit handshaking procedure. When PG #1 (Pulse Generator) fires, it turns off the Bit Available flip-flop and a new data bit is shifted into position by the sender. The Bit Available flip-flop is then turned back on, and, if (or when) the receiver is ready to receive a bit, a *There's-Your-Bit* signal is sent to him. This triggers PG #2*, which shifts in the new bit and shuts off the *Ready-For-Next-Bit* flip-flop. When this indicator goes off, the sender knows that the bit has been taken by the receiver. PG #1 then fires and shuts off the Bit Available flip-flop in preparation for getting the next bit ready for transmission. After the receiver has taken in the bit and is ready to accept a new one, it turns the Ready-For-Next-Bit flip-flop back on. The cycle then repeats.

*The *on* (↑) transition of *There's-Your-Bit* triggers PG #2.
The *off* (↓) transition of *Ready-For-Next-Bit* triggers PG #1.

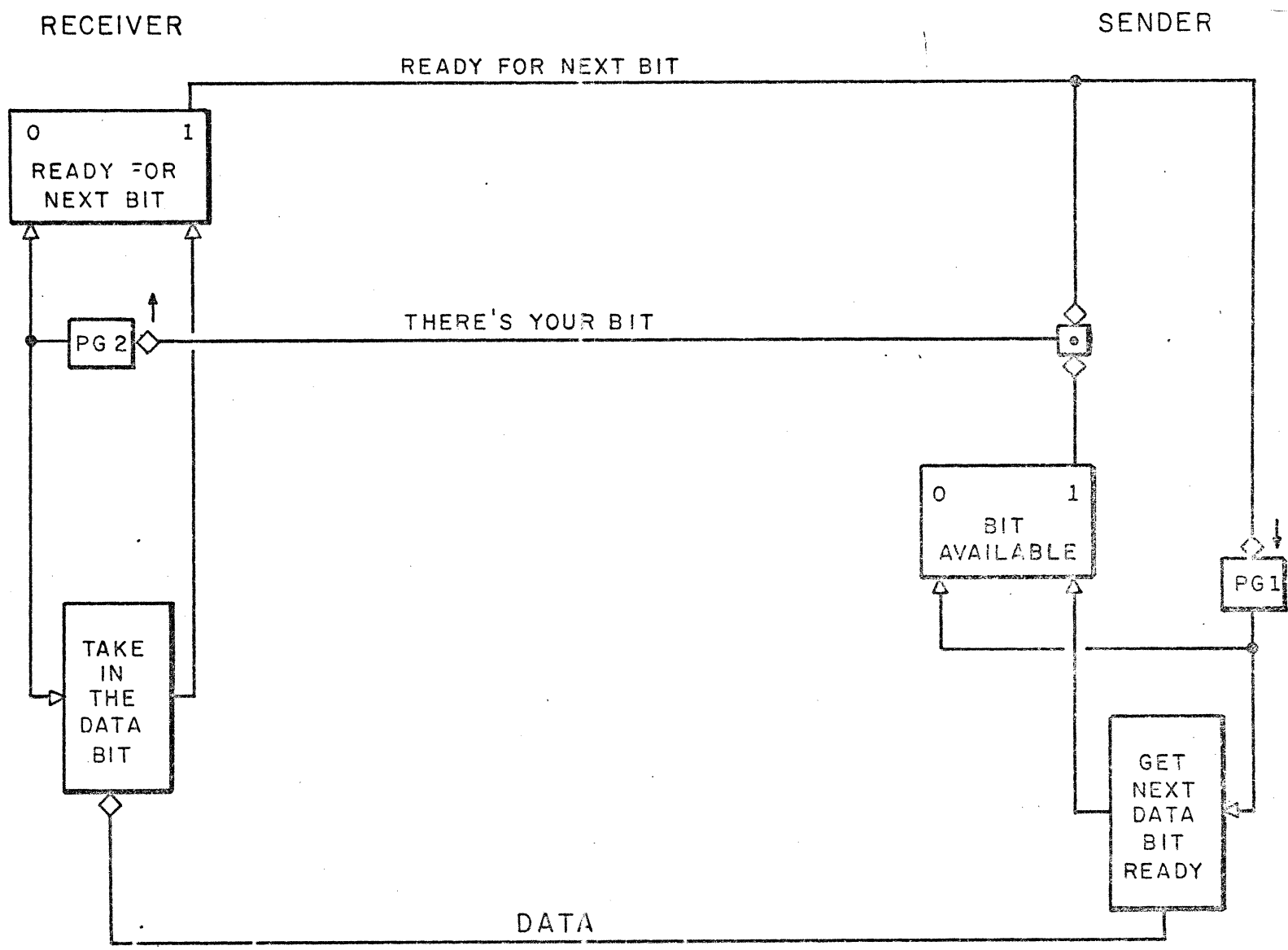


FIG.4-2 SIMPLIFIED CONTROL LOGIC FOR HOST/IMP HANDSHAKING

4-5

4/73

Each time the sender is notified that a bit has been accepted (by the *off* transition of Ready-For-Next-Bit), a word length counter is checked to see whether a new word must be fetched from memory. Similarly when a bit is accepted at the receiver, it may be necessary to tuck an assembled word into the memory before registering readiness to receive another bit. In addition to these obvious requirements, the simplified picture contains critical race problems*, which have been carefully resolved in the IMP's interface and must be similarly resolved in the Host's special interface.

The receiver may choose either of two methods of handshaking, a two-way or a four-way handshake. In the four-way handshake, the receiver awaits the dropping of There's-Your-Bit before raising Ready-For-Next-Bit. A full cycle of the four-way handshake works as follows: The sender readies the next data bit and the There's-Your-Bit signal is sent to the receiver (1st cable transit). The receiver takes in the bit and notifies the sender by dropping Ready-For-Next-Bit (2nd cable transit). The sender responds by dropping the There's-Your-Bit signal (3rd cable transit) and after the receiver has noted this, the Ready-For-Next-Bit signal can be turned back on (4th cable transit), registering preparedness for a new bit.

*For example, the race in shutting off the Ready-For-Next-Bit flip-flop.

The two-way handshake works as follows: The sender readies the next data bit and the There's-Your-Bit signal is sent to the receiver (1st cable transit). The receiver takes in the bit and notifies the sender by dropping Ready-For-Next-Bit (2nd cable transit). Instead of waiting for this signal to propagate to the sender and the resultant dropping of There's-Your-Bit to return, the receiver holds Ready-For-Next-Bit off for a brief period and then turns it back on.

This method has two dangers that must be considered, both arising from the situation where Ready-For-Next-Bit is off for too short a time.

- 1) If Ready-For-Next-Bit is off for too short a period, the sender may never note that it went off and he will continue to wait for the bit to be taken. The IMP itself requires that the signal be off at the IMP end of the cable for at least 50 nanoseconds for local Hosts and for at least 1 μ sec for distant Hosts. The IMP, in fact, always uses the two-way procedure. It does not wait for the There's-Your-Host-Bit signal to go off but instead guarantees to hold the Ready-For-Next-Host-Bit signal off for at least 1 μ sec.
- 2) If the receiver turns Ready-For-Next-Bit back on before the There's-Your-Bit signal has been observed to go off at the receiver's end of the cable, then the receiver may mistakenly believe the new bit is ready to be taken in. This problem is avoided if

the receiver maintains a *There's-Your-Next-Bit* flip-flop which is turned off when *Ready-For-Next-Bit* is turned off and is turned on only by the leading edge (*on transition*) of the *There's-Your-Bit* signal from the sender.

For local Hosts, where the cable delays are insignificant, either handshake procedure may be used. For distant Hosts, where cable delays may be significant, the two-way handshake procedure is recommended, in order to avoid placing an unnecessary restriction on the maximum bit rate.

The IMP introduces some deliberate delays into this control loop, both as a sender and as a receiver. Specifically, as a sender, the IMP introduces approximately 10 μ sec of delay* between the time that the Host indicates that it has taken one bit and the time that the next bit is made available. As a receiver, the IMP shifts in the data bit and turns off the *Ready-For-Next-Bit* signal shortly after the *There's-Your-Bit* signal comes on. However, *Ready-For-Next-Bit* will not be turned on again until about 10 μ sec* after *There's-Your-Bit* comes on. By introducing these deliberate delays, the IMP slows down the rate of information flow on the Host channels, thereby controlling

*These are minimum times assuming no IMP memory reference is required. Where a memory fetch or store is required, the times will be increased by at least 4 μ sec.

the maximum amount of IMP memory bandwidth that the channels can consume. This control is essential to avoid usurping bandwidth required for the store-and-forward functioning of the IMP.

Because of the loop nature of the handshake procedure, the Host can also introduce delays. However, knowing that the IMP will limit the data rate, *the Host should, in general, not introduce further deliberate delays of its own.* The delays we have mentioned are adjustable and can be tuned so that the interface operates at much higher speeds. At the time of installation of a new IMP, the standard interface will be set to run the Host channels at a 10- μ sec-per-bit rate. Once the IMP is connected to the Host, both the input and the output channels will normally be tuned to operate at a maximum rate of 100 kilobits/second, thereby lumping together the delays in the IMP interface and the Host special interface.*

*Since the IMP as a receiver holds the Ready-For-Next-Bit signal off for 10 μ sec, there does not appear to be any real need for the Host to have a Bit-Available flip-flop go on and off on a per-bit basis. The There's-Your-Bit line will go off when Ready-For-Next-Bit goes off. However, the 10 μ sec delay is subject to shrinkage; therefore, the Host should not rely on this delay to provide time for the next bit to arrive — even if getting the bit amounts only to moving a shift register over one place.

4.3 End-of-Message Indication

A Host indicates the end of its message to the IMP by presenting a *Last-Host-Bit* signal to the IMP together with the last bit. This signal will generally occur somewhere in the middle of an IMP word, i.e., with the input shift register in the standard interface only partially loaded. Additional padding bits will then be shifted into the register, namely a single one followed by enough zeroes (perhaps none) to fill up the register. These additional bits are appended at the end of a Host message by the hardware in the input section of the standard interface. If the last data bit happens to just fill the shift register, an additional IMP word consisting of a single one followed by fifteen zeroes will be appended to the message. Alternatively, if the single one happens to just fill the shift register, the IMP padding will contain only this single one. At the destination, the IMP will indicate the end of the message to its Host by presenting a *Last-IMP-Bit* signal to the Host together with the last bit of the IMP padding. In general, this signal will occur somewhere in the middle of a Host word, i.e., with the input shift register in the special interface only partially loaded. The Host must shift enough additional zeroes (perhaps none) into this register to fill up the register.

4.4 Master Ready Lines

Whenever the IMP is ready, it holds closed a relay contact that connects two wires (the *IMP Master Ready* and the *IMP Ready Test* lines) in the Host cable. Figure 4-3 illustrates how the

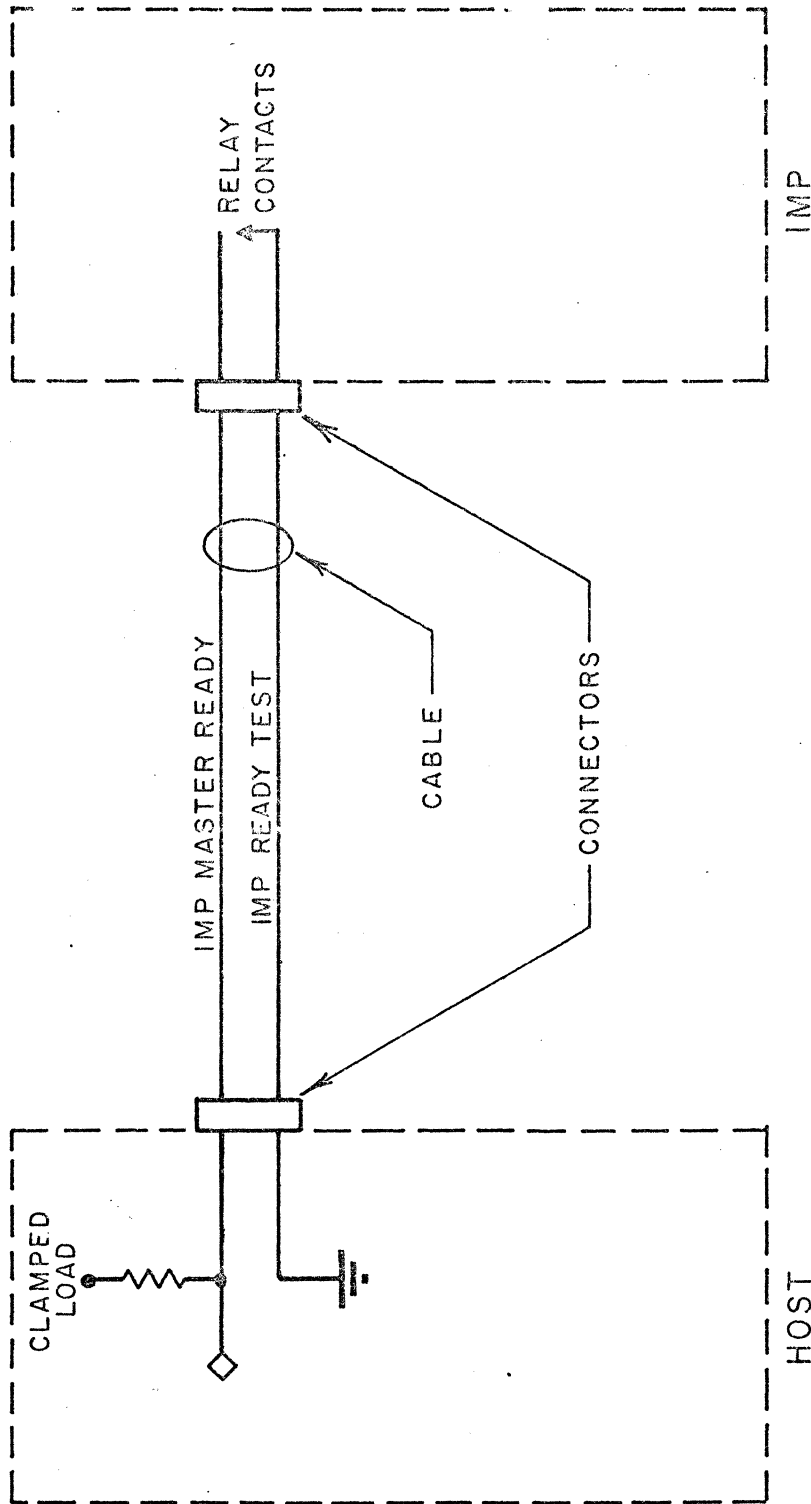


FIG. 4-3 IMP READY TEST AND IMP MASTER READY LINES

Host can employ this contact closure to ground a clamped logic line whose polarity indicates readiness of the IMP*. Note that, if the cable is removed at either end, the IMP appears to the Host not to be ready. The relay contacts are a Normally-Open pair and thus, if the IMP's power goes off, the line indicates "not ready".

The relay is kept closed by a *Watchdog Timer* in the IMP. This timer is normally held on by periodic pulses from the program. If the program fails to pulse the timer frequently enough, the relay opens and an automatic recovery procedure for the IMP is initiated. Successful recovery will eventually cause the relay to close again.

Similarly, each Host must provide for its IMP a set of contacts, which open when Host power goes off or whenever the Host does not wish to communicate with the rest of the network for an *extended* period.** The IMP will use this contact, in the specific manner suggested above, to pass a signal ground around to itself for testing Host readiness.

*The choice of ground as the interrogation level is obviously arbitrary, and the Host may use any reasonable arrangement.

**See Section 3.2 for a more complete discussion of the alternatives available to the Host for voluntarily stopping communication with the rest of the network.

The special Host interface should gate all incoming signals with the signal (or its inverse) on the IMP Master Ready line in order to avoid responding to meaningless transitions. Since the Master Ready signal passes through a relay, it will, in general, show contact bounce. When the IMP becomes ready (i.e., closes its relay), it executes a programmed delay before either the Ready-For-Next-Host-Bit or the There's-Your-IMP-Bit lines become true. This delay covers the contact bounce period and thus the Host need not worry about bounce on the gated versions of these signals.

The Host should provide similar protection by not permitting the Ready-For-Next-IMP-Bit or There's-Your-Host-Bit signals to become true until after its relay contacts have solidly finished closing.

4.5 Host Cable Connections

Following is a summary of the signals on the Host cable:

1. *IMP Master Ready* - The return for the IMP Ready Test signal through the IMP's relay contact.
2. *IMP Ready Test* - The test signal sent to the IMP to interrogate its ready status through the IMP's relay contacts. No more than 100 mamp should flow in this wire and the IMP Master Ready wire.
3. *Host Master Ready* - The return for the Host-Ready-Test signal through the Host's relay contact

4. *Host Ready Test* - The ground signal sent to the Host to interrogate its ready status through the Host's relay contacts. No more than 100 mamp should flow in this wire and the Host Master Ready wire.
5. *Host-to-IMP Data Line* - The data from the Host should be changed for successive bits only after the IMP's Ready-For-Next-Host-Bit signal goes off indicating that the previous bit has been accepted.
6. *There's-Your-Host-Bit* - This signal should be presented to the IMP by the Host as soon as the Host has a bit available to transmit *and* the IMP is indicating that it is Ready For Next Host Bit. When the Ready-For-Next-Host-Bit signal goes off, the There's-Your-Host-Bit signal should be removed. This must be done in two ways, as shown in Figure 4-2 — first by the AND gate between the Bit Available flip-flop and the Ready-For-Next-Bit signal, and second by immediately turning off the Bit Available flip-flop itself.*

*At first glance this seems like duplication. However, when the next bit becomes available, the Bit Available flip-flop will be turned back on and yet the There's-Your-Bit signal should not be sent unless the Ready-For-Next-Bit signal is on. Thus, the need for the AND gate. Shutting off Bit Available is required to avoid confusing the receiver with an old bit when a new Ready-For-Next-Bit signal comes on.

7. *Ready-For-Next-Host-Bit* - This signal will be presented to the Host whenever the IMP is waiting for a transmission by the Host. Each time that the Host gives the IMP a bit (via *There's-Your-Host-Bit*), the *Ready-For-Next-Host-Bit* will go off after the bit has been taken in. It will go back on again within 10 μ sec unless a memory access is required (once every 16 bits). A much longer off period will result when an IMP memory buffer region fills, and an interrupt service routine must operate before the IMP is ready for another bit.
8. *Last-Host-Bit* - When the Host transmits the last bit of a message, the *Last-Host-Bit* signal should be sent to the IMP in conjunction with the *There's-Your-Host-Bit* signal. Specifically, the *Last-Host-Bit* signal must come on no later than the *There's-Your-Host-Bit* signal comes on, and should remain on at least until *Ready-For-Next-Host-Bit* goes off. The IMP will pad the message with a one followed by enough zeroes (perhaps none) to fill the current IMP word.
9. *IMP-to-Host Data Line* - The data for the Host will be changed for successive bits only after the Host's *Ready-For-Next-IMP-Bit* signal goes off, indicating that the previous bit has been accepted.
10. *There's-Your-IMP-Bit* - This signal will be presented to the Host by the IMP as soon as the IMP has a bit available to transmit and the Host presents the

Ready-For-Next-IMP-Bit signal. When the Ready-For-Next-IMP-Bit goes off, the There's-Your-IMP-Bit signal will be removed. It will not be renewed until a new Ready-For-Next-IMP-Bit signal arrives.

11. *Ready-For-Next-IMP-Bit* - This signal should be presented to the IMP whenever the Host is ready to receive information. Each time that the IMP gives the Host a bit (via the There's-Your-IMP-Bit line), the Ready-For-Next-IMP-Bit signal should go off after the bit has been taken in. This notifies the IMP that the bit has been taken and that a new bit can be moved into position and made available. Ready-For-Next-IMP-Bit should be off for at least 50 nanoseconds (1 μ sec for distant Hosts) as seen at the IMP before it goes back on again. It may, of course, be off for as long as it takes the Host to ready itself to receive the next bit.
12. *Last-IMP-Bit* - When the IMP transmits the last bit of the source IMP's padding, the Last-IMP-Bit signal will be sent to the Host in conjunction with the There's-Your-IMP-Bit signal. Specifically, the Last-IMP-Bit signal will come on no later than the There's-Your-IMP-Bit signal. Last-IMP-Bit will stay on for some *arbitrary* short time after There's-Your-IMP-Bit goes off. The Host's interface must not interrogate this line after the Ready-For-Next-IMP-Bit signal has been turned off. The Host's special interface should round out the last memory word with zeroes, as required.

The asynchronous (i.e., sequential) nature of the interface causes stress to be laid on the *order* in which operations occur rather than on their *timing*. Minimum on or off times for the circuits in the IMP are 50 nanoseconds for a local Host and 1 μ sec for a distant Host. Thus, for example, the Host's Ready-For-Next-IMP-Bit line must be visibly down at the IMP for at least this length of time before it is brought back up even if the Host takes the bit more quickly than that. Similarly, the Host's Bit Available flip-flop must appear off to the IMP (via the There's-Your-Host-Bit line) for at least 50 nanoseconds for local Hosts and 1 μ sec for distant Hosts. We expect that, in general, much slower circuitry will be used, so that these minimum times will present no problems. The IMP delays at least 500 nanoseconds from the arrival of There's-Your-Host-Bit before taking the Host's data bit or checking the Last-Host-Bit line. Similarly, for IMP-to-Host transmission, the IMP will guarantee that the IMP data bit is on the line and the Last-IMP-Bit level is correct at least 500 nanoseconds before turning on the There's Your-IMP-Bit signal. Thus, skews of under 500 nanoseconds in the signals at the IMP end of the cable will be removed by the IMP. Any remaining skew must be removed by the Host.

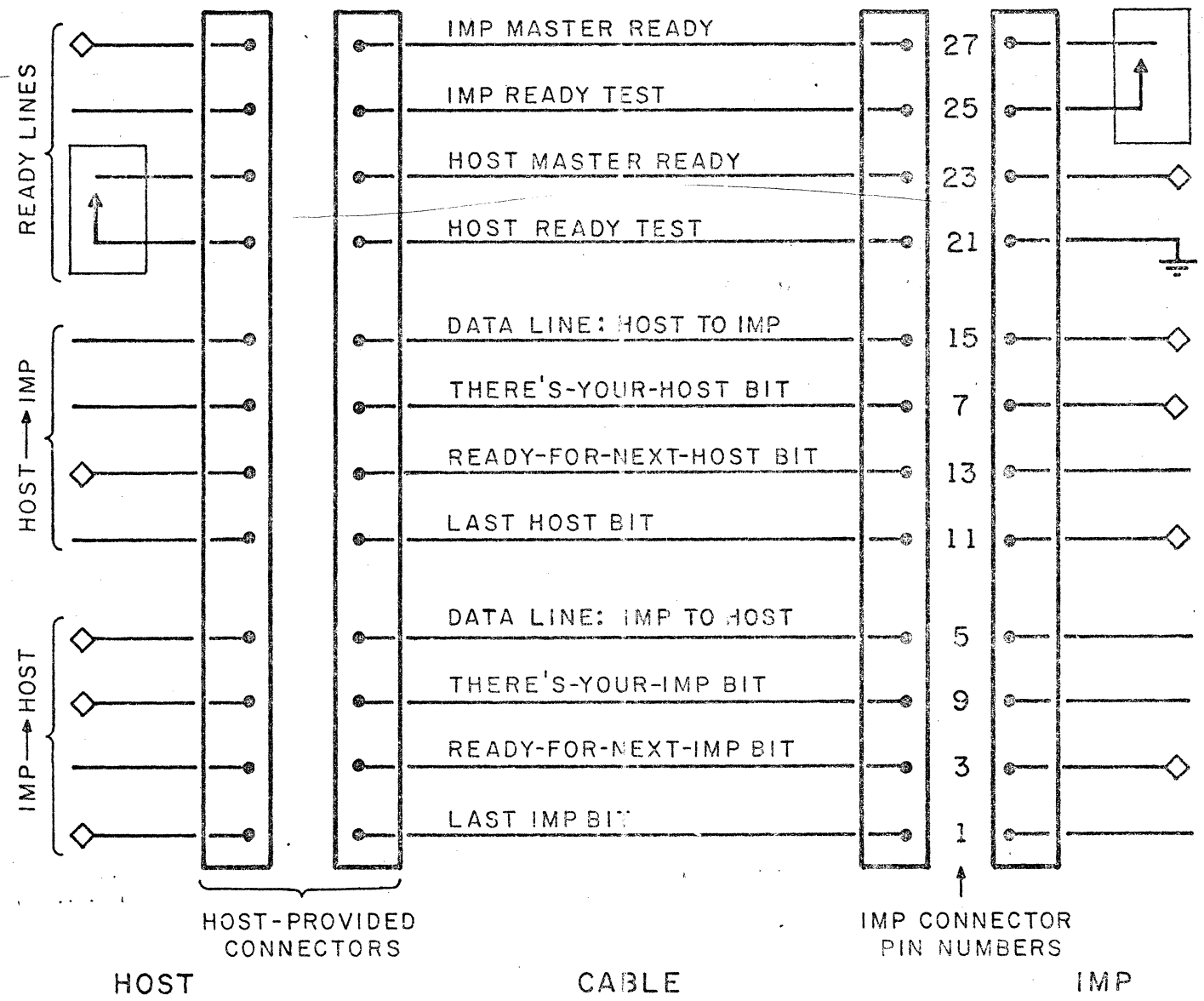
4.5.1 Connection to a Local Host

The asserted level for all logic lines (Data, Ready-For-Next-Bit, There's-Your-Bit, Last Bit) is +6 volts and the unasserted level is ground (these are with respect to the IMP signal ground). The driving and receiving circuits and specifications are shown in Appendix C.

The IMP will properly receive 5-volt logic signals; however, signals from the IMP go to 6 volts. Therefore, the Host must provide a voltage divider, if these signals are to be received by normal 5-volt logic, to prevent destruction of the receiving circuit.

The Host cable supplied with the 516 IMP is 30 feet long and contains 12 RG 174/U coaxial conductors with grounded shields. *Host personnel must provide an appropriate connector for the Host end of the cable.* The shield of each conductor is connected to signal ground at the IMP connector. Each cable is labelled with the IMP connector pin number corresponding to the center lead of the coaxial conductor. These wires are assigned as indicated in Figure 4-4; that is, the number in the figure corresponds to the number on the label attached to each coaxial conductor. All shields should be connected to signal ground in the Host. DC amplifiers are used for line driving and, by this means, we expect to couple the signal ground systems as tightly as possible.

The Host cable supplied with the 316 IMP is 30 feet long and contains 32 twisted pairs. The cable is terminated at the IMP end with a paddle card which plugs directly into the 316 Host interface. Each pair of the cable consists of a colored wire and a black wire numbered with the pin number of the paddle card to which the colored wire is connected. All black wires connect to the paddle card signal ground. *Host personnel must provide an appropriate connector for the Host end of the cable.* The wires are assigned as in Figure 4-5. All twisted pair grounds should be connected to signal ground in the Host. DC amplifiers are used for line drivers and the signal ground systems of the Host and IMP should be as highly coupled as possible.



4-19

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FIG. 4-4 516 HOST CABLE SIGNALS (LOCAL HOST)

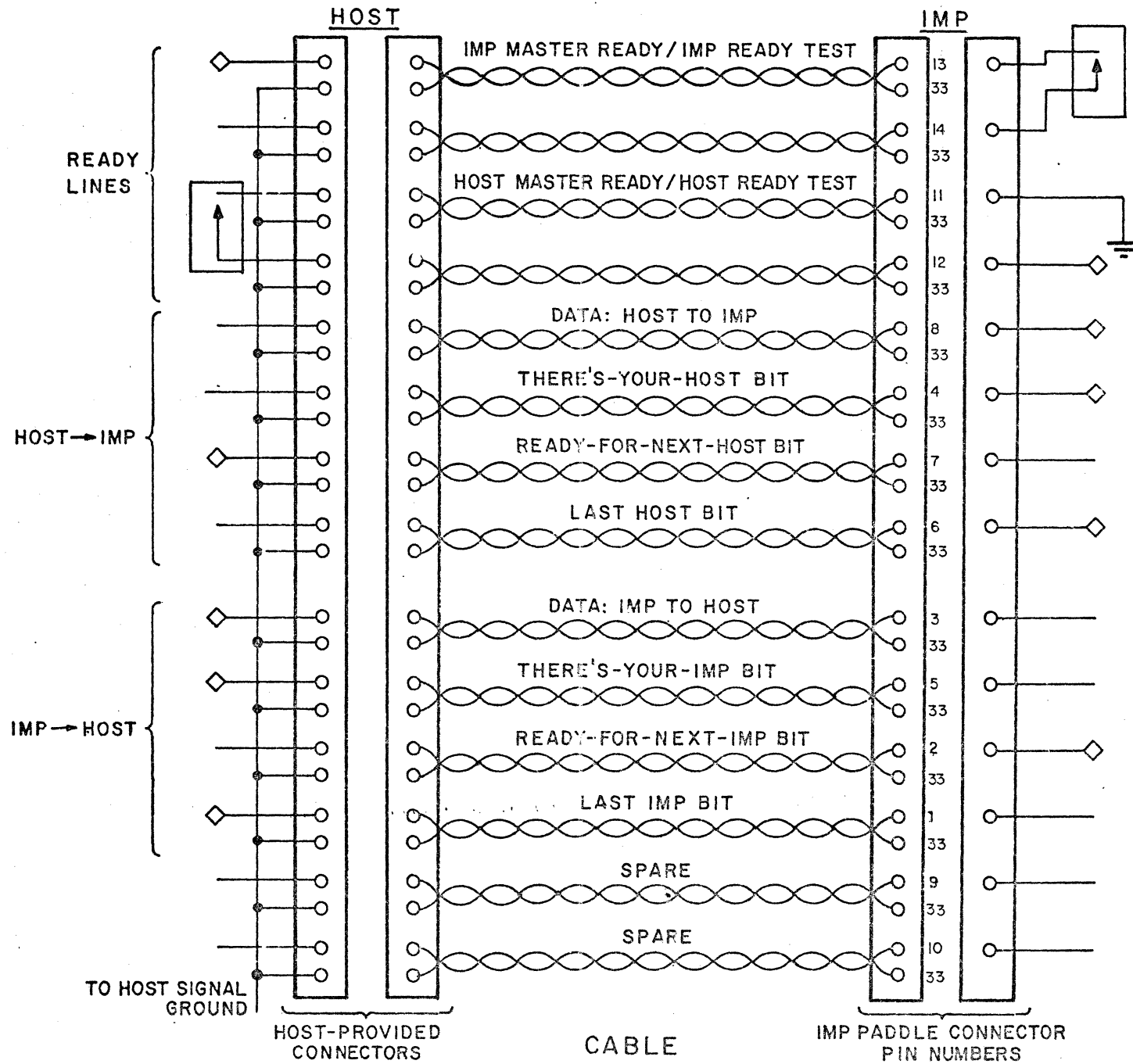


FIG. 4-5 316 HOST CABLE SIGNALS (LOCAL HOST)

4.5.2 Connection to a Distant Host

Connection to a distant Host necessitates the use of balanced lines and requires that a Host pay careful attention to differentials in ground potential. The distant Host's special interface must provide balanced drivers and receivers. *Ground isolation is provided by the IMP.*

The Host must supply a shielded cable containing multiple twisted pairs of #20 (or heavier) gauge wire. The characteristic impedance (Z_0) must be approximately 120 ohms. The wires may be either individually shielded or may have a single shield covering all pairs. The shield is used to carry the Host's ground reference and should have very low resistance. There must be at least 10 pairs in the cable, and we strongly recommend that at least two spare pairs be carried (see Figure 4-6). A suitable cable is Direct Burial Cable, REA Specification PE-23, 19AWG conductors, 12 pairs.

At the IMP side the cable must be terminated in a MS24266R18B31PN (Amphenol 48-16R18-31P) plug with a MS27291-5 clamp and MS24254-20P contacts. Pair and Pin assignments are shown in Figure 4-6. Note that the cable shield(s) should be connected to pin 31 and *not* to the connector shell.

The cable shields should be very solidly connected to the Host's signal ground, which should be connected to the third-wire power ground at the Host computer. DC isolation is done at the IMP end of the cable to prevent significant currents from

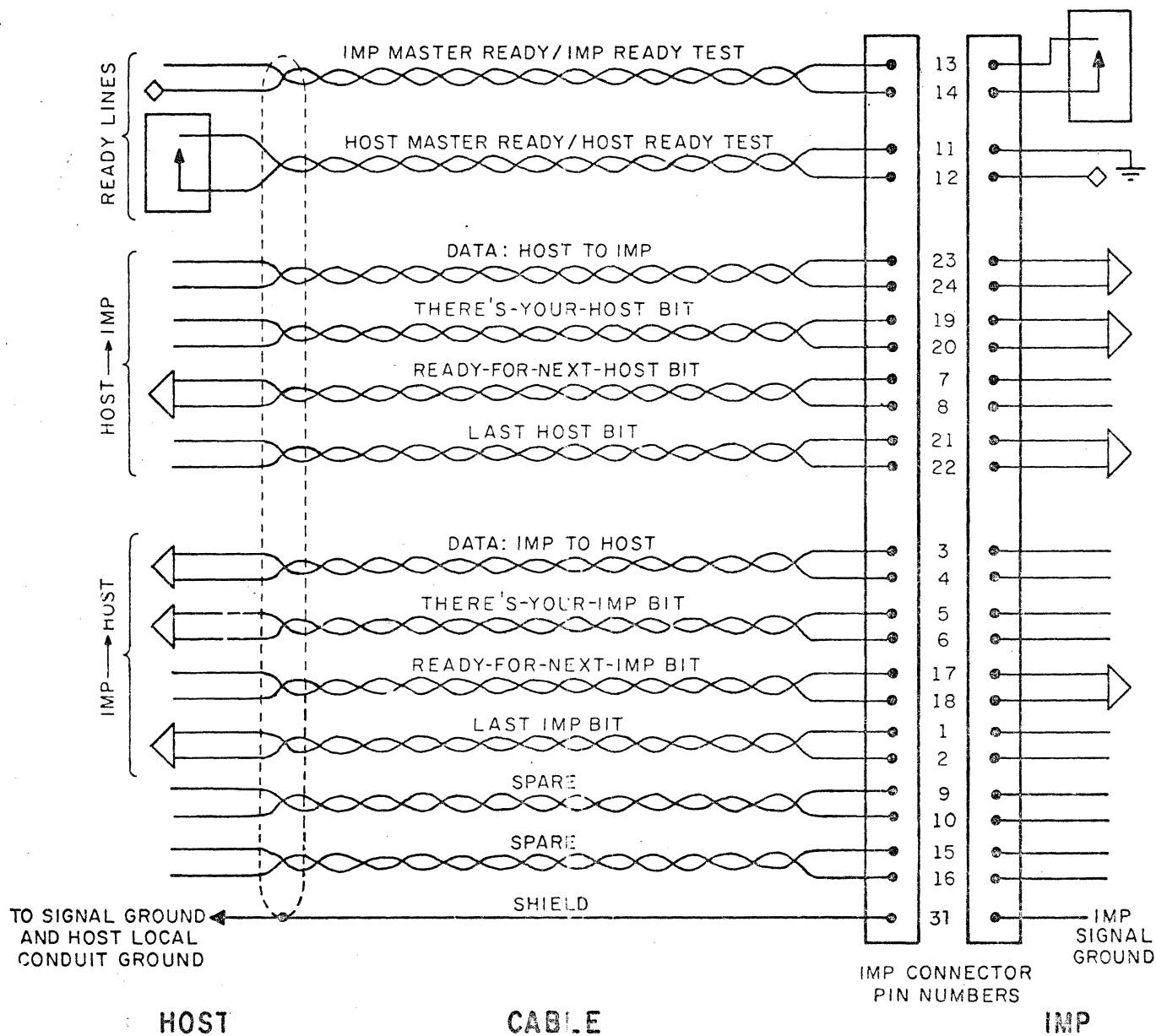


FIG. 4-6 HOST CABLE SIGNALS (DISTANT HOST)

flowing through the shields. This isolation is accomplished by transformer coupling the signals. All signals from the distant Host must therefore have transition times of less than 100 nanoseconds, and must remain in each state for at least 1 μ sec between transitions.

The logic signals on the pairs of the cable (Data, Ready-For-Next-Bit, There's-Your-Bit, Last-Bit) are balanced voltage signals with each side terminated at the driver in 62 ohms to ground. Thus, the terminating impedance is 124 ohms, and matches the cable impedance. The asserted logic signal drives the odd-numbered connector pin of each pair to +0.5 volts, and the other pin to -0.5 volts, producing a differential signal of 1.0 volt. The unasserted signal switches the polarity of this pair. There is no voltage drop across the cable since the receiver is unterminated. This produces a step reflection at the receiver which is absorbed at the transmitter. At the Host end, the transmitters should terminate the cable in 120 ohms across each signal pair.

Standard 6-volt IMP logic signals are converted to differential signals by the line drivers and from differential signals to 6-volt logical signals by the receivers. Drawings for the drivers and receivers used in the IMP are shown in Appendix D.

The Host should provide drivers and receivers similar to those used in the IMP. Use of these exact circuits is acceptable, as is use of any other circuits capable of driving and receiving a differential signal of 1.0 volts centered around ground. Care should be taken to preserve proper signal polarity in the cable.

APPENDIX B
DEVICE CODE AND JUMPERING

The Device Code for the SRI-AI IMP-10 Interface is
550 octal, or 101 101 0 binary.

The jumpering is therefore as follows:

On card D6,

E to D

J to K

M to L

On card D7,

E to D

J to K

M to L

~~S~~ to R

APPENDIX C
CARD LAYOUT, SPECIAL CARDS, DELAY SETTINGS

1. Card Layout
2. Discrete component wiring
3. Display driver card
4. Display panel
5. IMP cable cards (D1, D2)
6. Delay settings
7. Display driver wire list

CARD LAYOUT IMP-10D

SLOT	A	B	C	D
1	R205	R113	R202	IMP
2	R002	R107	R202	IMP
3	W520	R002	R202	W602
4	W520	R001	R202	W602
5	R107	R302	R202	W800
6	R302	R302	R202	W990
7	R001	R603	R202	W990
8	R113	R603	R202	R603
9	R107	R204	R202	R603
10	R204	R113	R202	B163
11	R603	R111	R202	B163
12	R603	R111	R202	B163
13	R205	R107	R202	B168
14	R205	R111	R202	B168
15	R205	R001	R202	B168
16	R205	R111	R202	B168
17	R205	R203	R202	B168
18	R205	B152	R202	B168
19	R205	R002	R202	R001
20	R205	R002	R001	R111
21	R205	R107	R001	R203
22	R205	R002	R111	B152
23	R205	R002	R203	R107
24	R205	W107	B152	R111
25	R205	W107	IOBUS	IOBUS
26	R205	W107	IOBUS	IOBUS
27	R205	W107	IOBUS	IOBUS
28	R205	W107	IOBUS	IOBUS
29	R205	W107	IOBUS	IOBUS
30	R205	B165	IOBUS	IOBUS
31	R205	R113	IOBUS	IOBUS
32	W602	R113	IOBUS	IOBUS

DISCRETE COMPONENT WIRING

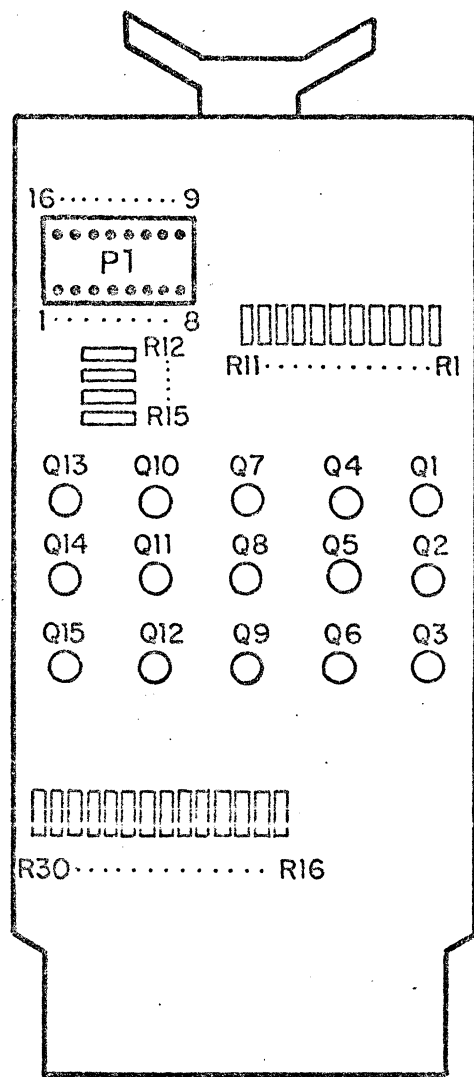
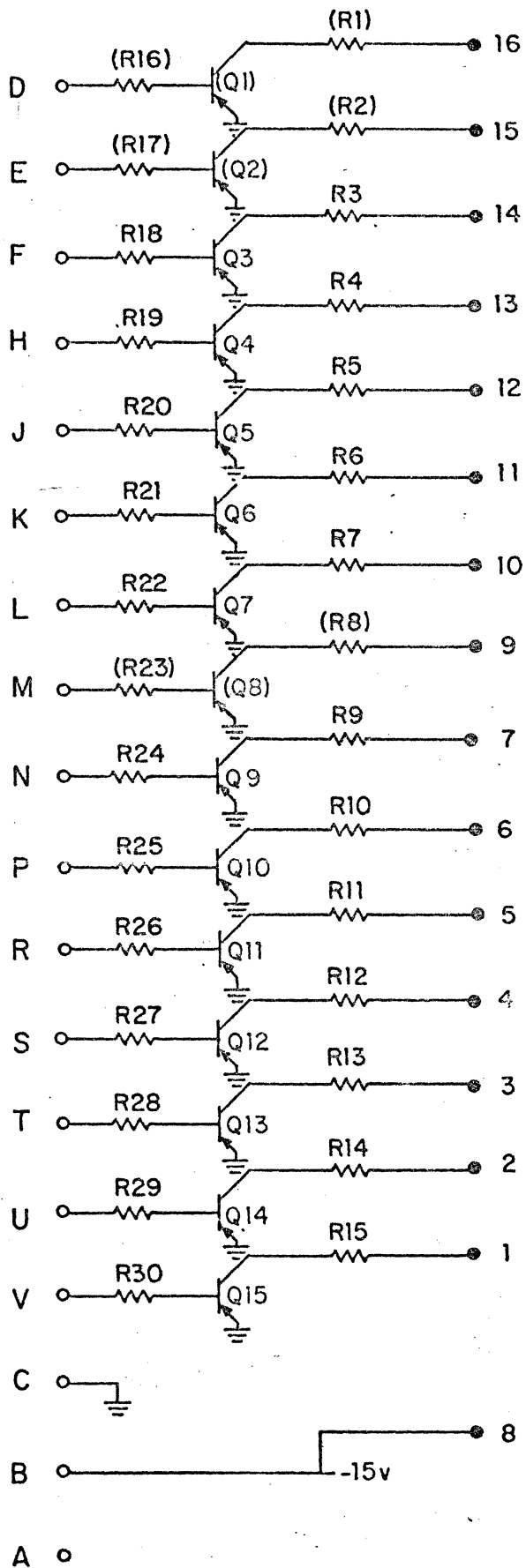
120 Ω 1/4 watt resistors

FROM	TO
A32F	D1R
A32K	D1S
D1R	D1C
D1S	D1C
D3F	D2J
D3K	D2K
D2J	D2C
D2K	D2C
D3N	D1J
D1J	D3C
D4F	D1K
D1K	D3C
D4K	D1L
D4N	D1M
D1L	D4C
D1M	D4C

22 μ fd 15 V electrolytic capacitor

+ end to A6S

- end to A6R



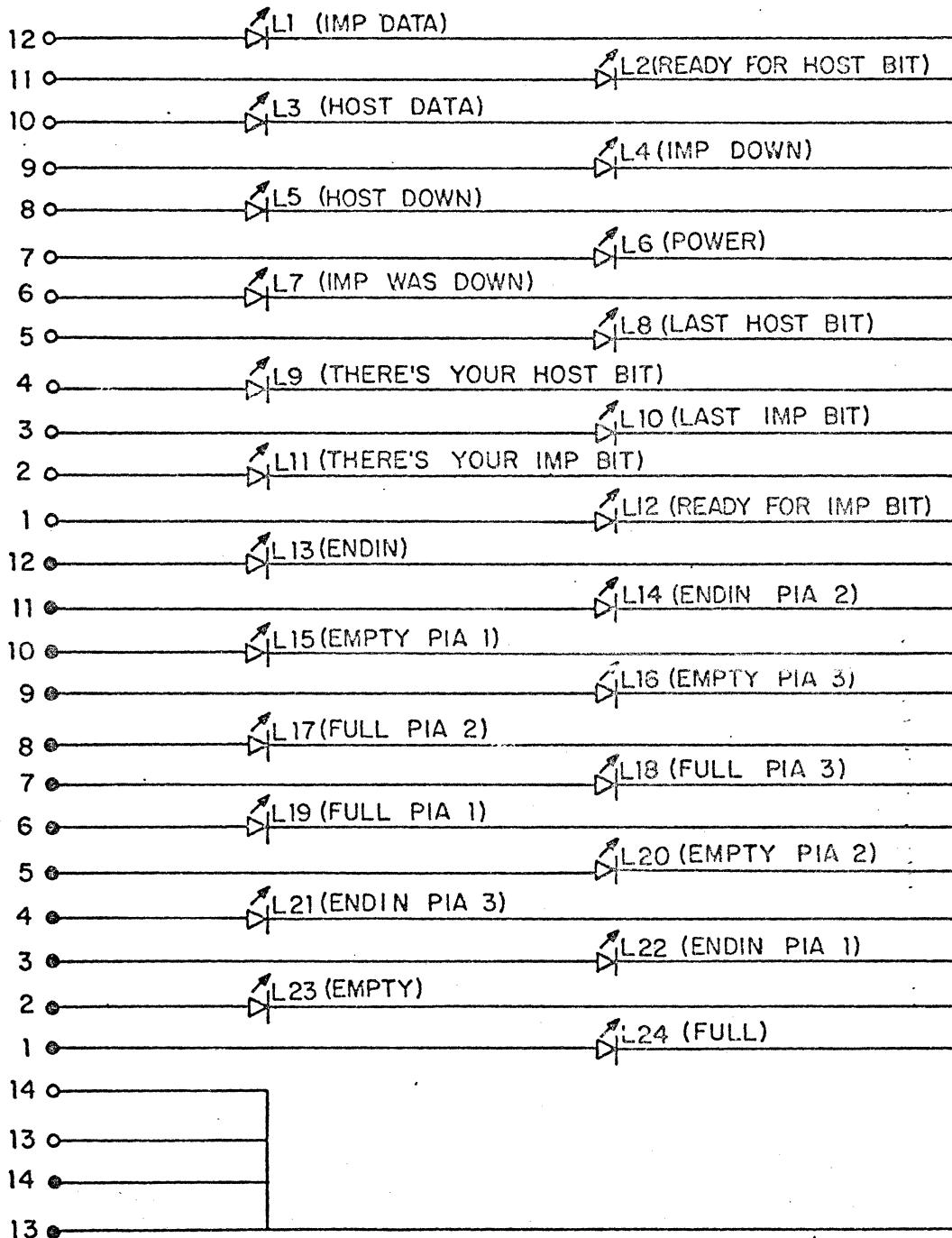
VIEW FROM COMPONENT SIDE

- R1-R15 750 1/4W
- R16-R30 3K 1/4W
- Q1-Q15 Motorola MPS6534.
- P1 16 pin DIP socket
- () component not implemented

Note: R1, R2 replaced by jumpers from pins 15 and 16 to -15V.

DISPLAY DRIVER CARD

DISPLAY PANEL



L1-L24 Dialco 521-9165

- S1 14 pin DIP plug to X1
- S2 14 pin DIP plug to X2

Note: S1 and S2 are inserted in pins 1-7 and 10-16 of the corresponding plug.

IMP CABLE CARDS (D1, D2)

<u>Signal</u>	<u>Card</u>	<u>Pin</u>	<u>Function</u>
IMRDY	D1	D ^{BR}	IMP Master Ready
GDDØ1	D1	E ^{BL}	IMP Ready Test
HMRDY	D1	F ^{BL}	Host Master Ready
HRDYT	D1	H ^Y	Host Ready Test
DHSTD	D1	J ^R	+ } Data: Host to IMP
DHSTD-	D1	K	- }
DTYHB	D1	L	+ }
DTYHB-	D1	M	- } There's Your Host Bit
DRFNH	D1	N	+ }
DRFNH-	D1	P	- } Ready For Next Host Bit
DLHBT	D1	R	+ }
DLHBT-	D1	S	- } Last Host Bit
DIDAT	D2	D	+ }
DIDAT-	D2	E	- } Data: IMP to Host
DTYIB	D2	F	+ }
DTYIB-	D2	H	- } There's Your IMP Bit
DRFNB	D2	J	+ }
DRFNB-	D2	K	- } Ready for Next IMP Bit
DLIBT	D2	L	+ }
DLIBT-	D2	M	- } Last IMP Bit

Note: IMP cable ground connects to D1C or D2C.

To loop the IMP cable for test purposes (either toward the IMP or toward the Host), make the following connections.

<u>Card</u>	<u>Pin</u>	<u>to</u>	<u>Card</u>	<u>Pin</u>	<u>Function</u>
D1	D	①	D1	F	Master Ready / Host
D1	E	②	D1	H	Ready Test / Host
D1	J	③	D2	D	+ } Data
D1	K	④	D2	E	- }
D1	L	⑤	D2	F	+ }
D1	M	⑥	D2	H	- } There's Your Bit
D1	N	⑦	D2	J	+ }
D1	P	⑧	D2	K	- } Ready for Next Bit
D1	R	⑨	D2	L	+ }
D1	S	⑩	D2	M	- } Last Bit

DELAY SETTINGS

<u>Pin</u>	<u>Signal Name</u>	<u>Timing</u>
A6M	TYIND	1 μ s
A6V	RSDLY	100 ms
B5M	DISPU	1 μ s
B5V	RFNBD	1 μ s
B6M	AAPAD	450 ns
B6V	APADP	450 ns

All are R302 adjustable one-shots.

DISPLAY DRIVER WIRE LIST

Note: Slot X1 and X2 are external to the interface and are specified by the Host. Each has -15 volts on pin B and ground on pin C.

<u>From</u>	<u>To</u>	<u>Signal</u>
X1F	A3U	IMPDA
X1H	A2D	RFNNB
X1J	A13J	HIBØØ
X1K	A5F	IMRDY
X1L	A10E	SHRDY
X1N	A5D	PWRUP
X1P	A10L	IMHBD
X1R	A32D	LHBIN
X1S	D4H	TYHBN
X1T	A3H	LIBIN
X1U	A3N	TYINN
X1V	B2N	ARFNB-
X2F	B9R	ENDIN
X2H	B4U	PIE26
X2J	A7H	PIE29
X2K	A7M	PIE31
X2L	A7S	PIE34
X2N	A7U	PIE35
X2P	A7P	PIE33
X2R	A7K	PIE30
X2S	A7E	PIE27
X2T	B4S	PIE25
X2U	B3F	PIOUT
X2V	A8H	FULL1



102724060