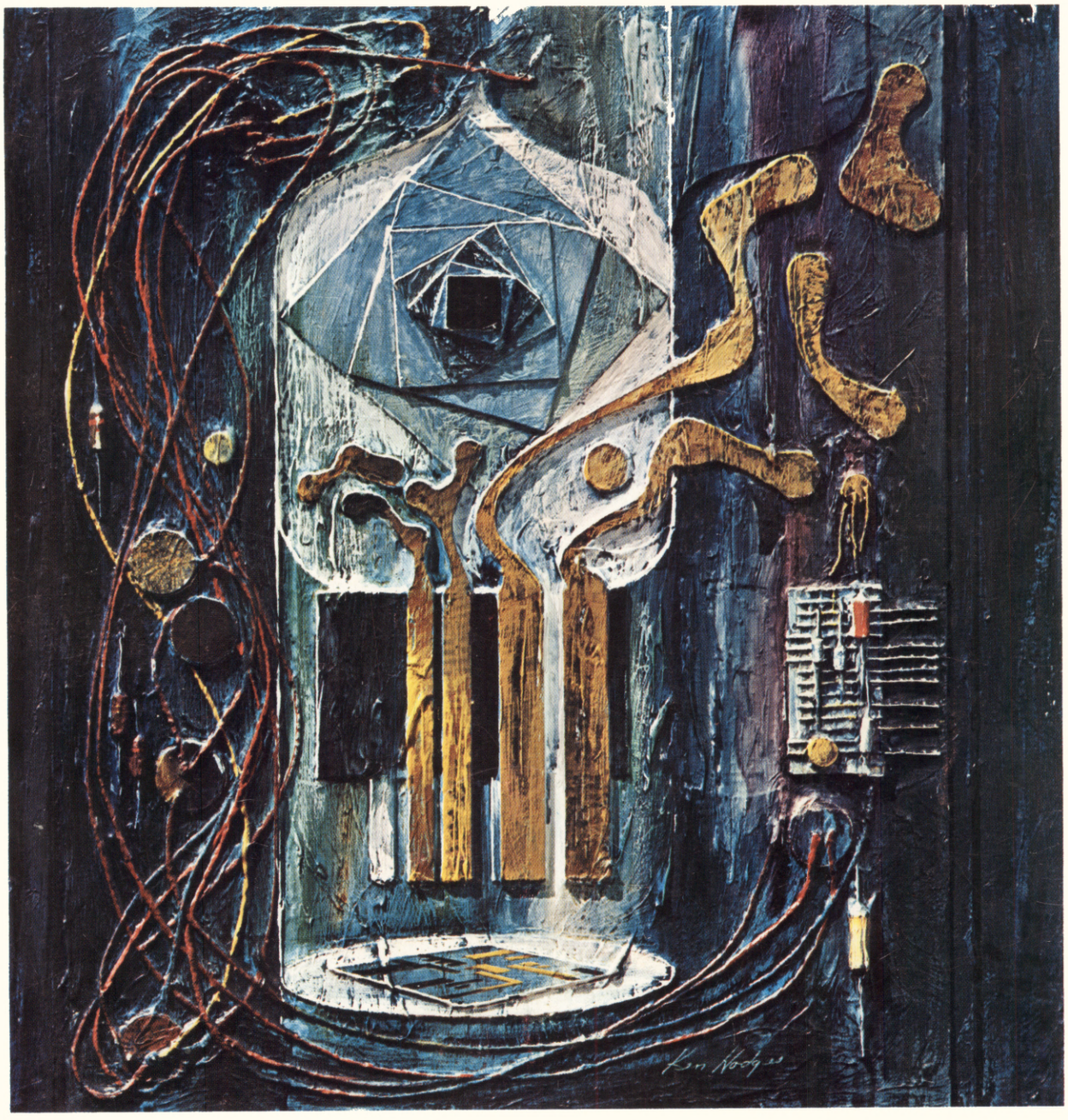
THE STORY OF

microelectronics

FIRST, SECOND, AND FUTURE GENERATIONS



North American Aviation Autonetics Division

THE STORY OF microelectronics FIRST, SECOND, AND FUTURE GENERATIONS

The Story of Microelectronics...

First, second, and future generations

by M. S. Parks

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Credits

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The Story of Microelectronics...

First, second, and future generations

Microelectronics is looked upon as a revolutionary technology that has literally exploded on the scientific horizon. Actually, microelectronics' history has been one of evolution, rather than revolution, and this "sudden" technology has been increasingly with us over a period of more than 30 years . . . presently acknowledged benefits to systems reliability, performance, and economy are the hard-won culmination of three decades of effort by dedicated scientists and engineers.

Evolution of microelectronics, from its early beginnings to the present, makes a stimulating story. Developments and improvements still evolving from the laboratories are even more exciting. Projection of the continuing evolution into the future promises startling and profitable new marvels.

☐ Microelectronics is generally hailed as answer to all electronic users' prayers. Galloping in on its attractive white stallion — cost effectiveness — this technological prodigy promises everything to everybody. But the question is, does it keep its promises?

☐ Whether or not it does in each case, depends upon many interrelated factors. But for the majority of applications — for defense, industry, and space — microelectronics deserves all the praise and consideration one can give it.

☐ In modern military avionics, for example, microelectronics is increasingly indispensable. A prime instance is its contribution to the control center of most airborne systems — the digital computer — with its numerous functions, such as navigation, fire control, display control, performance monitoring, autopilot steering, automatic radar control, air data processing, pre-mission checkout, communications control, and fuel management. This functional complexity, ever on the increase, *demands* smaller, lighter-weight, vastly more reliable means of systems implementation — in other words, microelectronics, unrivalled in all these respects.

☐ For commercial aircraft applications, benefits of microelectronics are fast becoming equally essential. In this area, advantages stem from two trends:

1. The first trend is higher speeds, and greater traffic variety and density, requiring much more accurate and responsive air traffic control both by equipment in the aircraft and by equipment on the ground.
   In the speed regime of the supersonic transport, both flight-management functions and ground control operations will require an ability to process data at a much higher rate.
2. The second significant trend is toward cheaper and much more reliable electronic equipment — cheaper to produce and cheaper to maintain.

☐ Benefits will be compounded for commercial applications, in that reduced costs and increased reliability of the electronic equipment will permit it to be used in places not previously feasible for economic or flight-safety reasons. (For example, it is now practical to consider microelectronics for performance monitoring of most aircraft subsystems, so that more economical maintenance programs can be devised. Correspondingly, increased reliability and reduced size make feasible the use of microelectronic radar, communications equipment, flight controls, and navigation devices coordinated through a central microelectronic computer—which also maintains a continuous check on performance of other elements of the aircraft, *as well as of itself.*)

☐ For the long voyages of space, microelectronics' appropriateness is obvious. In space, there is no second chance — no turning around midcourse when an electronic circuit goes bad, no convenient wayside service stations. For space, *reliability must be reliable* — and no other technique offers the inherent reliability of microelectronics. To this vital benefit add the reliability-enhancing potential for redundancy offered by microelectronics, plus the payload- and range-increasing advantages of its light weight, small size, and low power—and the attractiveness of microelectronics for space electronics is assured.

The best compromise for the best system

☐ To plan, or to buy, the best-performing, most reliable system — for the least amount of money — the system designer or purchaser must compromise or "trade off" some degree of one desirable feature to arrive at the essential degree of another. The most effective system is eventually reached through a sequence and combination of such "tradeoffs."

☐ In making the important decision of whether or not microelectronics has anything to offer this combination, it is necessary to consider its effect on and by a number of urgent factors:

Objective — How long, how often, in what environment will the system be used?

Budget and Schedule — How much money can you spend, and when do you need the system "ready to run"?

Reliability — If something goes wrong, can you replace it? If something goes wrong, will it be catastrophic to your "Objective"? (The obvious interdependence of this factor with those of "Objective" and "Logistics" dramatically point up the necessity for tradeoff.)

Logistics — How skilled will the available maintenance people be? How much room will you have for spares? How far do spares have to come to reach you from "home base"?

Physical Requirements – How much room will you have for the system? How heavy can you allow it to be? How much power supply will you be able to carry aboard for it? How much heat can you dissipate?

☐ With microelectronics, as with any other system parameter, great care must be taken during tradeoffs, not only to *keep the necessary levels* of performance, accuracy, reliability, etc, but equally to *avoid "over-specifying"* too-excellent performance, too-high reliability, or greater accuracy than is actually required for the application. These things all demand the spending of money and, because of tradeoff interdependence, their "over-specification" can make required, interrelated parameters suffer needlessly.

☐ For space, for defense, and for commerce and industry, microelectronics does, indeed, have much to offer. In every case, however, careful thought must be given to whether its benefits outweigh its cost penalty to the program involved. To be truly meaningful, any evaluation of cost effectiveness must include consideration not only of the initial purchase price, but of all the related and subsequent costs . . . for reliability improvement, personnel training, maintenance operations, and spares.

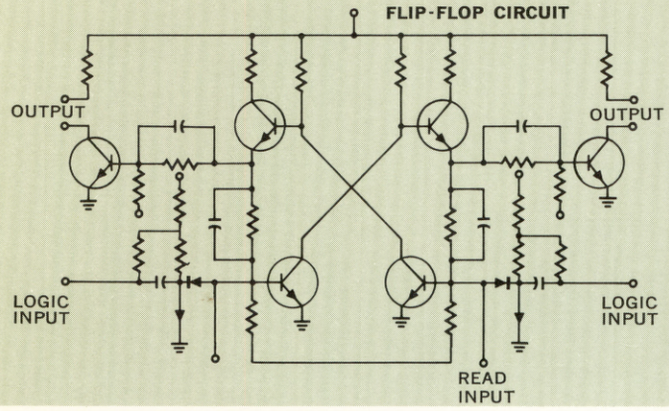
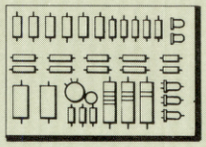
Reliability, maintainability, availability

☐ Reliability, maintainability, and availability are so closely interrelated that it is almost impossible to consider them as separate tradeoff factors.

☐ By definition, if a system is *reliable*, it can be relied upon for satisfactory performance and it is, therefore, *available* – when, as often, and for as long as needed. By the same token, if equipment is highly *maintainable*, it is easily and economically kept reliable and available. All three of these interrelated factors of reliability, maintainability, and availability are, in turn, as already stated, closely tied in with total cost effectiveness – compounded not of initial expenditures alone, but of costs throughout the program.

☐ In reliable systems, less maintenance is required. Consequently, logistics costs are greatly reduced. Fewer spares are needed, less elaborate maintenance facilities and equipment are demanded, fewer and less skilled maintenance personnel are required, and less maintenance training is necessary. Again, the result is – increased cost effectiveness.

☐ In making the systems tradeoff decision for microelectronics, these factors are all of prime importance, because microelectronics is of uniquely high reliability.

SCHEMATIC	DISCRETE PARTS	INTEGRATED CIRCUIT
	 2 X 3 INCHES	¼ X ⅛ INCH
PARTS REDUCED BY A FACTOR OF 36	36	1
CONNECTIONS REDUCED BY A FACTOR OF 8.5	234	28
CASE SEALS REDUCED BY A FACTOR OF 36	36	1
LEAD SEALS REDUCED BY A FACTOR OF 5.5	78	14

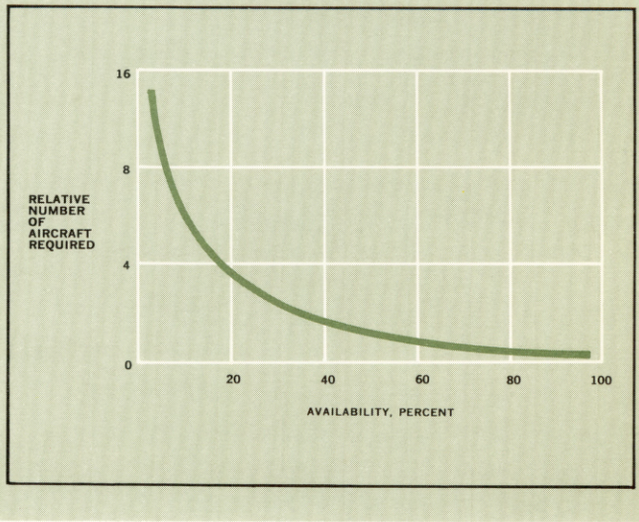
Principal Failure-Mode Reduction with Integrated Circuits

☐ First of all, its inherent reliability is not matched even remotely by that of any other type of circuitry. This fact is graphically illustrated by the accompanying chart, which compares a computer circuit using discrete components, and a functionally identical one using semiconductor integrated circuits (IC's). The chart points up the drastic reduction in failure modes achievable with this particular type of microelectronics; the reliability improvement illustrated is not limited to IC's, however, but is one of the chief advantages of microelectronics, in general. The significant buildup of reliability is reflected in equally significant lowering of maintenance and logistics requirements, with heightened overall system cost effectiveness.

☐ Primary factors in microelectronics' inherent reliability advantage are the smaller number of interconnections it requires, innate resistance to shock and vibration, and often reduced thermal stress.

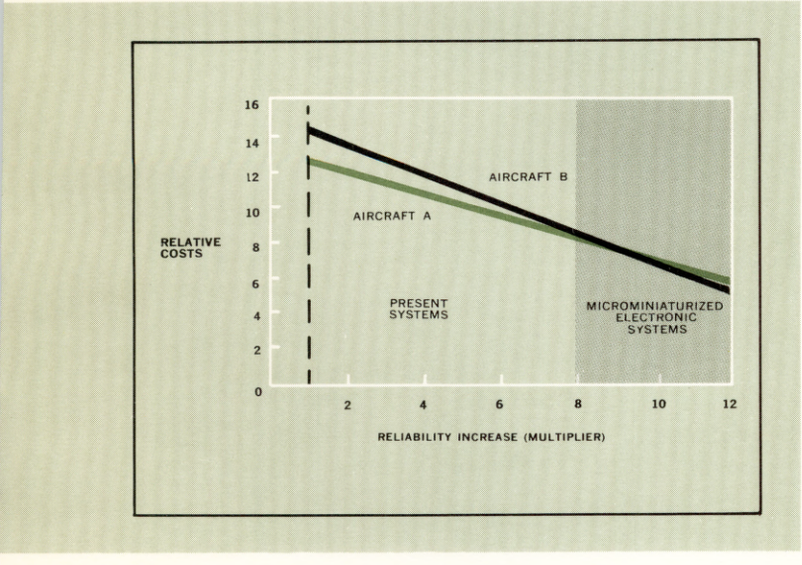
☐ Maintenance is simplified and maintenance costs are lowered by microelectronics' potential for throwaway and replacement of faulty units to the individual circuit level (with promising new developments, even to the subsystem level).

☐ Availability is also enhanced by microelectronics. (Military aircraft are taken as an example here, although the same kind of thinking applies to any major air- or space-borne system operation.) The fewer aircraft required for a given mission, the lower the total cost-of-ownership. Microelectronics can lower the number of aircraft required per mission and, thus, the total cost-of-ownership, in two ways:



Aircraft Availability

☐ First, microelectronics can permit on-board self-check and almost immediate replacement of faulty units upon return to base. From an avionics standpoint, this should increase availability of aircraft from present-day figures of 40 to 50 percent to approximately 95 percent; should cut number of aircraft required per mission by approximately one-half; and should bring about savings of billions of defense budget dollars.



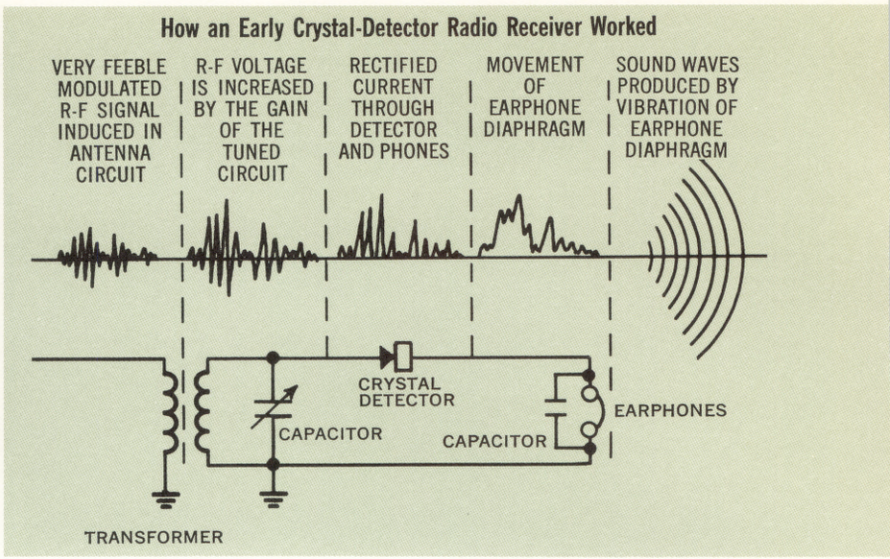
Tactical Aircraft Avionics Maintenance and Operating Costs

☐ Second, microelectronics' benefit of reduced size permits redundancy — with resulting increased reliability and, consequently, reduced number of aircraft required per mission. (Detailed studies of tactical avionic systems indicate probabilities of reliable system operation as high as 0.98 obtainable in future systems with microelectronic equipment.)

☐ Two studies of typical aircraft (conducted by the Autonetics Division of North American Aviation, Inc.) have demonstrated how significantly microelectronics can reduce total cost-of-ownership by increasing reliability of mission success. Results of the studies are plotted in the chart at left, which shows reliability increase vs relative costs of systems maintenance and operation for the two types of aircraft.

☐ As the chart indicates, the two studies revealed a common trend, with an approximately 2-to-1 reduction in maintenance and operating costs, and an order-of-magnitude or better increase in reliability with state-of-the-art microelectronics. Cost comparisons are relative numbers on the chart, and data from each study are normalized to cover the same number of aircraft for approximately 10 years.

ANCIENT INFANT—THE CRYSTAL DIODE



Batch production processes for high-device-density microelectronics promise lower component costs, with resulting lowered production costs and heightened reliability. These developments will be reflected in less demanding logistics requirements and even greater overall cost effectiveness.

Physical advantages of microelectronics

☐ The most obvious offerings of microelectronics are the "physical" ones of small size and light weight. Because of these characteristics, more room is left for fuel and payload. Equipment can be more complex, yielding greater accuracy and/or flexibility for contact with target or achievement of destination. Lighter weight and increased fuel allowance permit significantly longer range. Redundancy made possible through microelectronics' weight and space savings increases reliability, cuts maintenance, raises availability—reduces program costs.

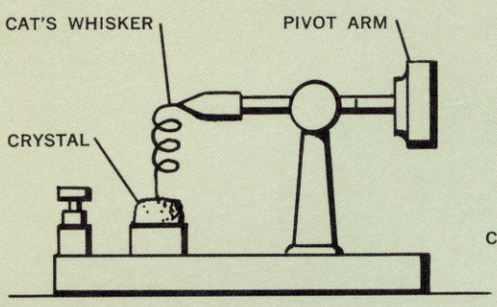
☐ Other physical advantages of microelectronics include reduced power and heat-dissipation requirements, with a resulting elimination of the need for heavy, cumbersome cooling systems and power supplies.

How it all began: the search for increasing smallness

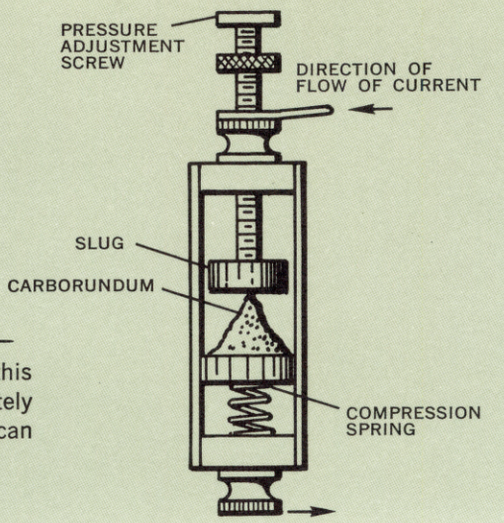
☐ The wonders of microelectronics did not happen overnight, and the story of how these wonders evolved is not only interesting, but provides a background for full understanding of their behavior today and tomorrow.

☐ Before World War II and the debut of the airplane as a major defense machine, electronic hardware was mostly land-based, big, and heavy . . . and its chief requirement, next to meeting wide-tolerance specs for performance, was for all-weather ruggedness.

☐ The most sophisticated airborne electronics was limited to intercoms, communications radio, the simplest of radio compasses, and power supplies for these. To meet the scientific advances of the enemy, however, our Government soon realized the urgent need for electronics progress—and, almost overnight it seemed, there poured from Government and industry laboratories a stream of electronic marvels . . . target search-and-track radar, airborne television, missile and drone radio control, radio and radar guidance systems, radio and radar altimeters, and bomb laying and armament control systems.



One of the Earliest Crystal Detectors. All of this early detector was out in the open, completely exposed to view. The light "cat's whisker" can be seen resting against a galena crystal.



A Later, "More Sophisticated" Crystal Detector. A form of carborundum crystal detector (vintage circa 1932) is cut open to reveal its parts. The carborundum crystal was held in contact with a metal slug under about 5 pounds pressure, exerted by a spring. Screw adjustment of the spring tension was made for best contact. The combination's efficiency as a rectifier arose from low resistance to current flow from slug to crystal, but high resistance from crystal to slug.

Billy Mitchell's predictions paled beside the actual burgeoning use of the airplane — and with this acceleration came the need for smaller, lighter electronics — and the need for "miniaturization."

☐ First to feel the impact of miniaturization was the vacuum tube — at the time (early 1940's), the heart, brains, and soul of electronics. Although tubes of consistent performance and versatility had been developed — no vacuum tube was, at the beginning of World War II, sufficiently uncumbersome to meet the new requirements. Manufacturers responded to the new requirements by developing smaller and smaller glass and metal tubes — at first, simply smaller vertical replicas of their predecessors called "miniature" tubes . . . later, "subminiature" devices departing from conventional configurations, as with the so-called "acorn tubes," sized and shaped just as their name would indicate. Always, the new tubes were, in function and in basic structure, simply smaller and smaller duplicates of the big tubes they were to replace. Definite limits of design and manufacture obviously restricted the eventual reduction in size achievable by this method.

☐ Parallel with the race to shrink vacuum tubes, other components were miniaturized and subminiaturized — including resistors, capacitors, connectors, inductors, and transformers. Fortunately, frequencies at which the wartime radar, television, and pulse circuits operated were extremely high, and components for these applications were readily compatible with the small-size, low-weight demands of airborne usage.

☐ Research went on apace. And, with all the concentrated effort and talent poured into the search for increasing smallness, the embryonic beginnings of true microelectronics were bound to take place and did — with the development of "semiconductor" devices—first, germanium and silicon diodes, soon followed by the transistor.

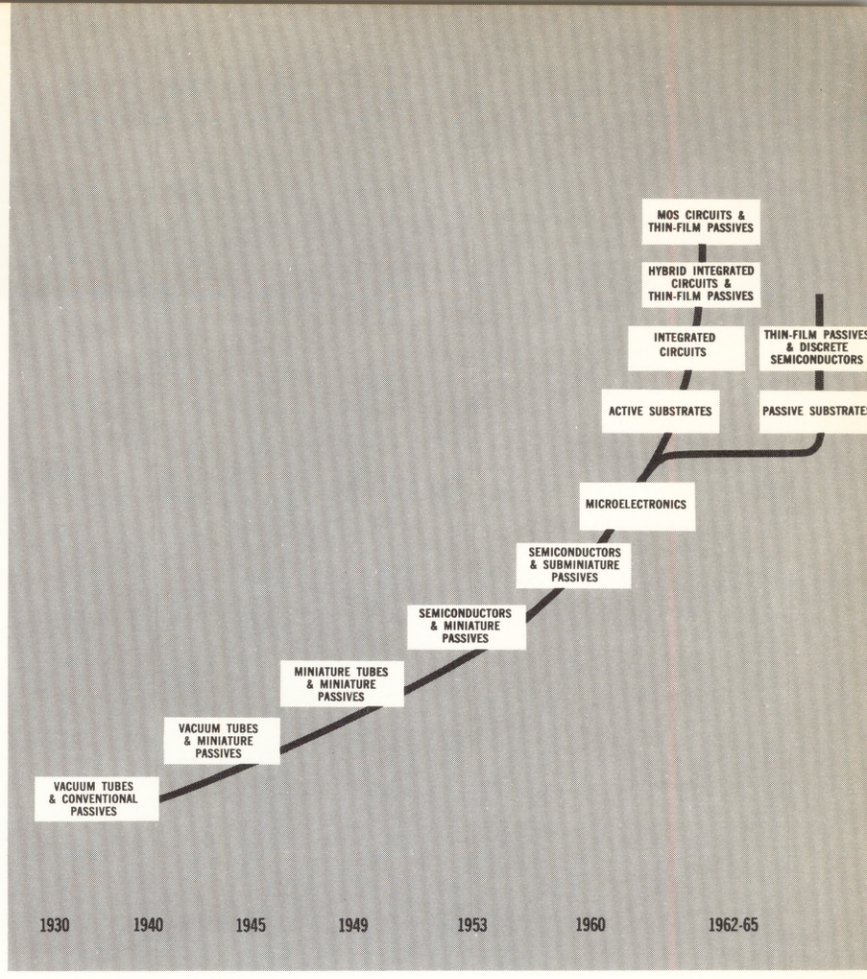
☐ Actually, use of semiconductor devices is as old as radio. The "crystal detector" in early wireless sets was a semiconductor unit. The thin wire "cat's whisker" was moved over the semiconductor (carborundum or galena) crystal's surface until it located a "sensitive" spot (i.e., a spot where the conducting and rectifying properties of the crystal were best). A current then flowed through the earphones in proportion to the audio modulation of the signal's radio-frequency carrier, and the operator "heard music."

☐ The "rectifying" property of semiconductors — that is, their ability to conduct current better in one direction than in the other — was first extensively exploited in germanium and silicon diodes during the 1940's. Long before that, though — between 1920 and 1930 — copper oxide and selenium rectifiers had come into general use in power supplies, to convert a-c line voltage into d-c voltage to operate vacuum tubes; they were high-power, low-frequency devices, however, and had little or no potentiality for miniaturization. The devices needed were low-power, high-frequency units that could be small in size and low in weight, and that had characteristics compatible with the operating parameters of the pulse and microwave circuitry in widespread use in airborne equipment.

☐ Germanium and silicon diodes were the first practical replacements for vacuum tubes to meet these requirements that were not simply miniature or subminiature replicas of tubes. Capable of being made many times smaller than the smallest vacuum tube, the semiconductor diodes were just as effective, and were inherently more rugged and reliable since they had fewer parts. They had generally a higher ratio of forward to back conductance (and, thus, were better rectifiers), needed no heater (filament) power, operated on lower voltages and so required smaller power supplies, and had longer life than vacuum tube diodes.

☐ No matter how far reduced in size, vacuum tubes continued to be measured in inches — semiconductor diodes could be fabricated to perform the same functions as vacuum tubes, better and more dependably than vacuum tubes and, at the same time, were no bigger than match heads!

☐ When semiconductor triodes—"transistors"—were added to the semiconductor family in the late '40's, they were eagerly welcomed. Transistors offered all the advantages of crystal diodes compared to vacuum tubes. Like the diodes, they were small, compact, and robust; operated with extremely low voltages; needed no cathode or filament heating power; and



Microelectronics Evolution

were capable of performing all the functions hitherto performed only by vacuum triodes — except more reliably than the latter.

☐ Certain problems had to be overcome in designing transistor circuits without inherent instability, and in eliminating spurious noise signals which existed in the transistor at a much higher level than in the vacuum tube. Trouble was encountered, too, in producing transistors with uniform characteristics from sample to sample. With time, these problems were all solved to a satisfactory extent, however, and today the transistor replaces all but the highest-power or special-purpose vacuum tubes in airborne applications.

☐ With transistors and crystal diodes supplanting their large vacuum tube counterparts, and with the miniaturization of their companions—resistors, capacitors, reactors, transformers, and potentiometers —circuit devices actually took up less space than the wires and cables to interconnect them!

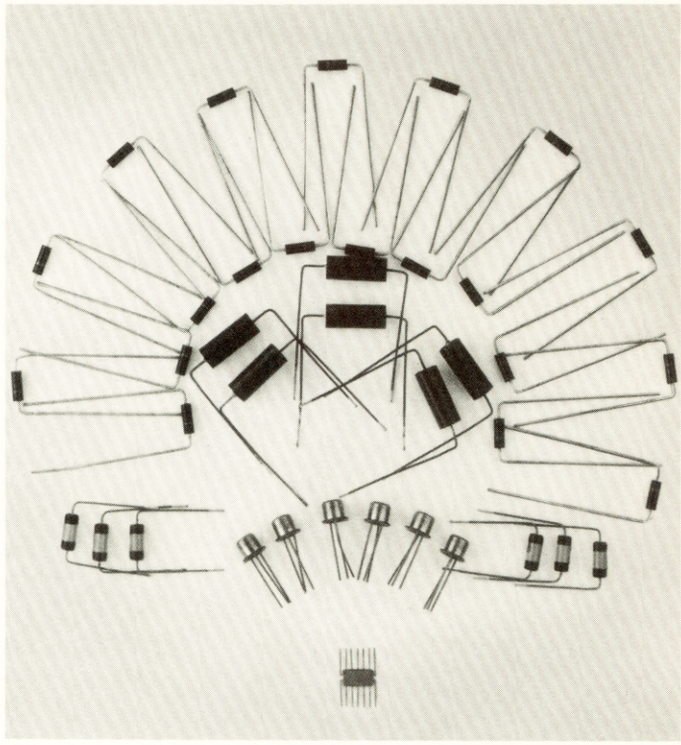
☐ The next innovation was naturally, then, the printed or etched circuit — with all wiring, except the highest-power leads and cabling, consisting of lines of a conducting metal (copper, gold, silver) deposited on the surface of a "circuit board" fabricated of an insulating material. The terms "printed circuit" and "etched circuit" came from the chemical process used to transfer the interconnecting conductors onto the board. Special miniature connectors were designed for mounting on the boards and for cable terminations, and special flat multiconductor cables were developed for space-saving interconnection between boards. As skill in design and fabrication grew with experience, techniques were developed for depositing, not only wiring between circuit devices, but some of the "passive" devices themselves as integral parts of the circuit—first, resistors and capacitors, then reactors and transformers. Later, "active" elements like transistors were fabricated as integral parts of the monolithic "integrated circuit."

These techniques became "first-generation microelectronics" . . .

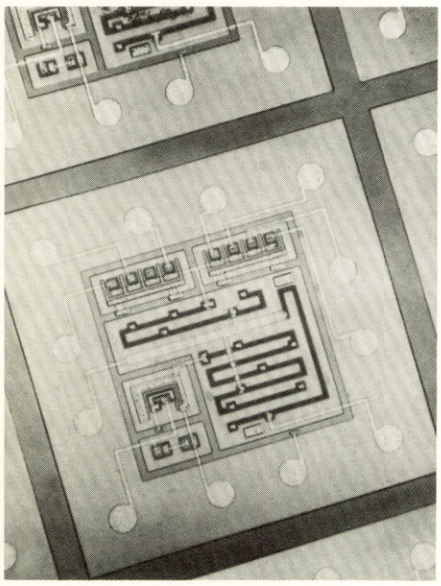
First-generation microelectronics

☐ "Birth" is usually described as the occasion upon which an entity makes its first appearance in the big, outside world, and actually begins to live. Microelectronics first saw the light of day in many areas of application. For all practical purposes, however, the birth of microelectronics took place with its use throughout Minuteman II in 1962 — for this was the first time microelectronics began to "live" — in its overall mechanization of an entire defense weapon system.

☐ The microelectronics picture changes daily and, today, portions of so-called "second-generation microelectronics" are already fast reaching the operational stage — or birth into the big world outside the laboratory — but first-generation techniques are far from becoming obsolete. Indeed, first-generation technology possesses advantages for some applications that will probably never be offset by anything offered by later developments. First-generation microelectronics is in daily, world-wide use for heightened reliability, enhanced performance, lowered cost, smaller volume and weight, and increased range and payload . . . in the electronic guidance, control, communication, and data-processing systems of industry, science, NASA, the Army, Navy, and Air Force . . . and will continue to be for quite some time.



Integrated Circuit (Bottom of Photo) Performs the Same Circuit Function as the 38 Discrete Components Shown Above It



1960:
2000 TRANSISTORS PLUS RESISTORS AND CONDUCTORS ON EACH WAFER TO FORM MANY CIRCUITS LIKE THE ONE SHOWN, CENTER, HERE

Microelectronics economy has been steadily improved through advances in batch fabrication. Costs are just about the same to process an area of silicon regardless of what kind of, or how many, elements are put on it. One of the first steps in microelectronics cost cutting was taken in the early '60's, when astute manufacturers began to deposit passive elements (conductors and resistors) on the same silicon wafer along with the active diodes and transistors.

☐ First-generation microelectronics includes — in addition to discrete transistors and diodes, potentiometers, transformers and inductors, subminiature cables and cable connectors, and boards for mounting these and other devices — three basic types of microcircuit technology, classifiable by physical structure and method of fabrication. These are the ceramic printed circuit (CPC) or "thick-film" circuitry; "thin-film" circuitry; and semiconductor integrated circuits (IC's) or, as they are sometimes called, microelectronic integrated circuits (MIC's). These three types are still in widespread use in their original forms and are, also, being brought forth from the laboratories in vastly improved "1½-generation" versions for revamping of present, and development of new, systems.

THE TYPES OF FIRST-GENERATION MICROELECTRONICS CLASSIFIED BY "STRUCTURAL" DIFFERENCES

According to basic structure, first-generation microelectronics circuitry is of three types. In one of these — the "integrated" circuit—both active and passive devices are formed by diffusing small amounts of chemicals with certain electrical characteristics down *into* a block of "host" material. In a second type — resistors, capacitors, and conductors are formed by depositing chemical materials *onto the surface* of a substrate to form a "thin-film" circuit. The third type also employs a substrate, but resistors and conductors only are screened onto its surface, and all other devices are discrete; this type of microelectronics is the "thick-film" or "ceramic printed" circuit.

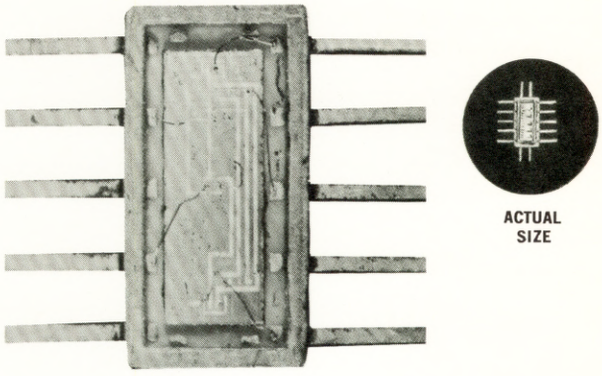
Semiconductor Integrated Circuits

In the fabrication of integrated circuits (IC's) — transistors, resistors, diodes and other devices are diffused into a minute block of semiconductor material.

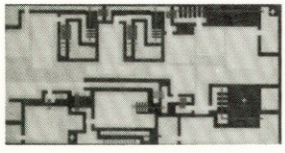
Interconnections of the diffused electronic component parts are made by vacuum depositing metal on an insulating oxide coating over the semiconductor surface. Then, by etching, the metal layer is formed into a pattern of conductors as required, to complete the circuit.

Many identical and separate circuits are formed in a single IC semiconductor wafer. The wafer is cut into individual chips—one circuit per chip—and each chip is mounted in a package. Terminals leading outside the package are attached, and the package is sealed.

The technology of "hybrid" integrated circuit packaging is also important in microelectronics. With this technique, individual chips of silicon are attached to a single header and interconnected by wire bonding, as opposed to the monolithic structure in which all of the devices are diffused into a single chip of silicon and interconnected by vapor-deposited metal. The hybrid technique occasionally employs vapor-deposited resistors, but primarily makes use of separate chips of silicon into which are diffused the active and passive devices.



ACTUAL SIZE

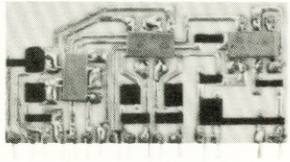


ACTUAL SIZE

Thin-Film Circuits

In one of the two major types of "thin-film" process — the "photo-etch" process — thin layers of resistive and conductive materials are chemically deposited on a ceramic or glass substrate. Unwanted portions of the overlays are then etched away by a photo process, leaving a film which forms a complex network of resistors and conductors. More than 70 resistors — ranging in individual value from 10 ohms to 1 megohm, and with a precision of 0.01% — can be deposited on a single substrate little more than an inch square.

With the "vacuum deposition" thin-film process, resistive and conductive materials are vaporized in a vacuum, then deposited on the substrate through a mask. The resulting pattern forms the conductors and passive components in the circuit. In subsequent operations, insulating layers are deposited on the substrate and covered by additional film to form an interconnected resistor-capacitor network.



ACTUAL SIZE

Ceramic Printed (Thick-Film) Circuits

One of the earliest forms of microelectronics was the screened or ceramic printed circuit process. With this method, microcircuits are made by a technique adapted from silk screening.

In ceramic printed circuit (CPC) fabrication, the circuit pattern is printed on a high-resolution metal screen. In separate operations, the conductor and resistor materials are pressed through the screen onto a tiny (as small as ¼-inch square), wafer-thin substrate of alumina or other ceramic.

When both conductor and resistor patterns have been printed, the wafer is placed, first, in a low-temperature oven which dries the pattern, and, then, in a high-temperature furnace which fires the resistor and conductor patterns in place on the substrate. Next, the conductors are dip-soldered, and additional components, such as transistors, diodes, and capacitors, are soldered, welded, or bonded to the substrate. In a final step, the substrate is placed in a special jig and encapsulated.

Typical Micro-Resistor Characteristics

PARAMETER	MONOLITHIC SILICON DIFFUSED	SILICON ON SAPPHIRE	CHROMIUM	NICHROME	TANTALUM	TIN OXIDE	CERMET	TITANIUM
Sheet resistance, ohms/square	2.5–300 [4]	2.5–300	300–800 [7]	20–1200 [5]	25–1000 [16]	80–4000 [6]	100–50,000 [13]	5–100 [10, 9, 15]
Temperature coefficient of resistance, ppm/degree Centigrade	500–2000 [4]	500–2000	100–600 [1]	±100 [5]	0–1000 [3]	0 to–1500 [6]	±300 [13]	±150 [15]
Power dissipation, milliwatts/mil	0.01	0.02	0.01	0.01	0.01	0.02	0.03 [13]	0.01 [15]
Resistance tolerance, percent: As fabricated After trimming	±10 [4]	±10	5 0.1	5 < 0.1	±10 [16] < 0.1 [17]	5 [6] 0.1	±15 [13] 0.1 [13]	±10 0.1
Resistance ratio tolerance, % before trimming	±3 [4]	±3	1	1	5	1	5	5
Distributed capacitance, picofarads/square mil	0.1	None	None	None	None	None	None	None

Typical Micro-Capacitor Characteristics

PARAMETER	MONOLITHIC SILICON		THIN-FILM		
	DIFFUSED	THERMALLY GROWN SILICON DIOXIDE	SILICON MONOXIDE	TANTALUM PENTOXIDE	TITANIUM DIOXIDE
Capacitance (C), picofarads/square mil	0.2–0.1 [4]	0.25–0.4 [4]	0.1 [4]	0.7 [17]	0.5 [15]
Working voltage, d-c volts	6–20 [4]	50 [4]	50 [14]	50 [17]	25
Dissipation factor: @ 1 kilocycle/sec @ 1 megacycle/sec	0.001–0.010 [4]	0.001 0.7 [4]	0.015 [12] 0.8 [12]	0.01 [17] [12] 0.25 [12]	0.005 [15] > 0.2 [10]
Temperature coefficient of capacitance, ppm/degree Centigrade	100 [16]	30	110 [14]	250 [17]	400 [10]
Voltage dependence	$V^{-1/2}$ [4]	None	None	None	None
Polarization	Yes	None	None	None	None
Shunt capacitance, percent of (C)	10–80 [4]	10–50 [4]	INTRACONNECTION ONLY		
Leakage current @ 5 volts, amperes/picofarad	10^{-9}	10^{-9}	10^{-8} [5]	10^{-10} [5] [12]	10^{-8} [15]

References (parenthetical superscripts in table refer to reference numbers in following list):

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☐ A question often asked of the large-scale aerospace systems designer is: "Why do you use *different types* of microelectronics in your various equipments? Would it not be much more economical, as well as give the best performance, to decide upon *one best type,* and then to use that type throughout all your systems and subsystems?" The answer is straightforward: No single type of first—*or* second—generation microelectronics *is* best for all types of applications. Each offers certain advantages, and each has certain limitations, for the various kinds of using systems. Different microelectronics techniques are employed singly or in combination, to best fulfill the performance, reliability, and cost requirements of each application.

☐ From this standpoint, microelectronics falls, again, into three classifications: digital, radio-frequency, and linear.

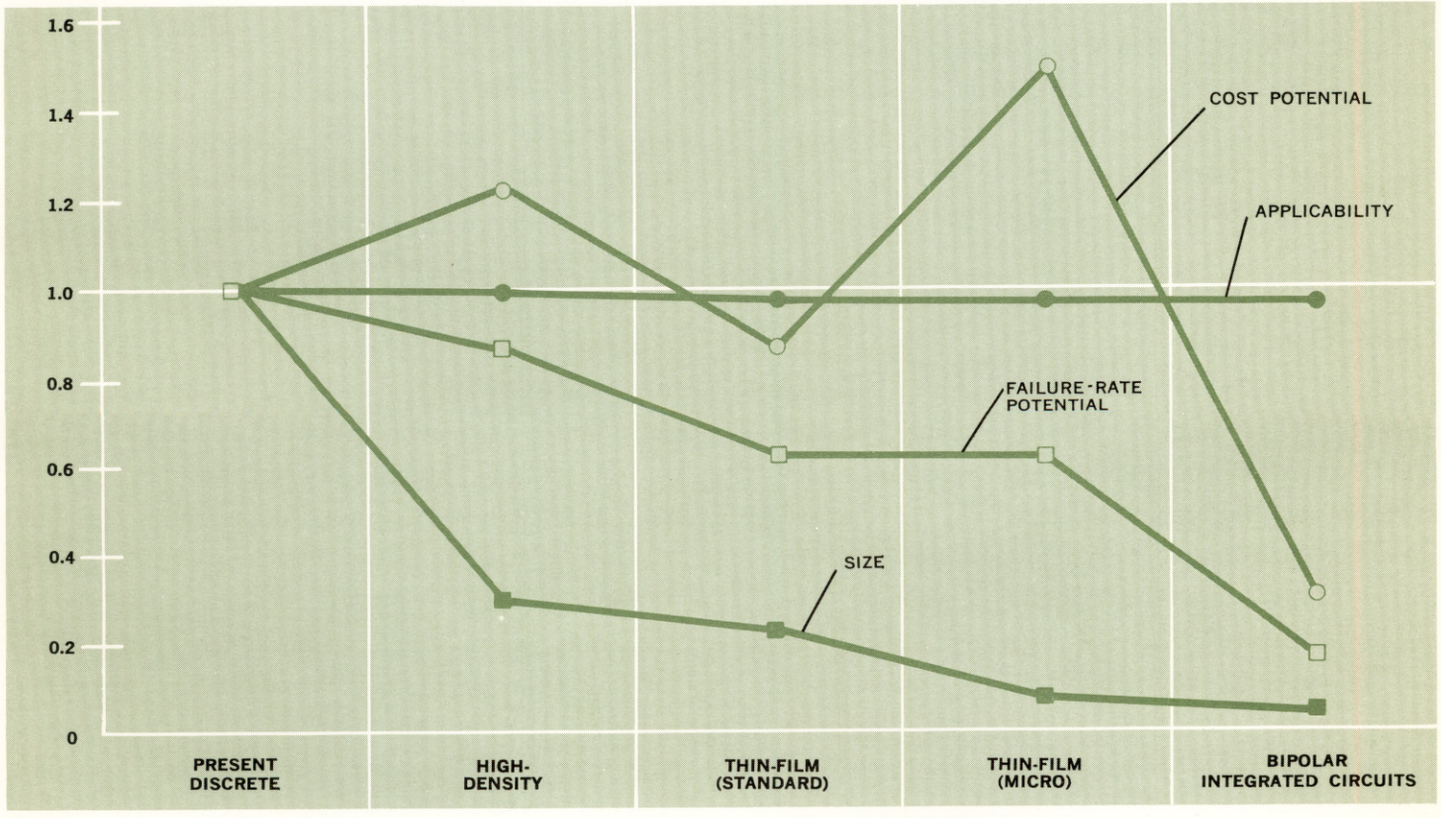
Digital Applications

☐ Digital systems include computers and other data processors. Circuit functions in these systems are pulse-driven, on-off operations, and are largely repetitive and low-power. Few capacitors are used, and those employed are small in both electronic (mostly below 2000 picofarads) and physical size. Semiconductor integrated circuits prove ideal for most digital applications.

☐ The major challenge to microelectronics in digital systems has been to devise a method for interconnecting the logic functions. In this type of circuitry, it is typically necessary for each logic element to "look at" a number of other logic elements, with the result that an enormous quantity of interconnecting leads must be provided between elements. The determining factor on the "smallness" of digital microelectronics thus becomes the ability to interconnect in as small a volume as possible. The volume is not limited by the volume of the microelectronic devices themselves—which, in digital circuitry, are generally low-profile units—but by the board area required to interconnect them adequately. Techniques developed to solve this problem of device interconnection are as ingenious as the microelectronic devices themselves, and require the solving of three-dimensional problems in design. (See "The *Big* Problem of *Little* Room—for Interconnections," page 15.)

Radio-Frequency Applications

☐ In r-f applications (radio, television, and radar systems), capacitors are still mostly less than 2000 picofarads in value and, thus, physically small, but a much larger number of them is needed than in digital applications. Also in contrast to digital systems, r-f microelectronics requires transformers and inductors and, for gain adjustment of the amplifier-type circuitry common to r-f applications, must have provisions for high-precision resistors. Distributed and stray capacitances must be kept to a minimum. To satisfy all these prerequisites, thin-film techniques



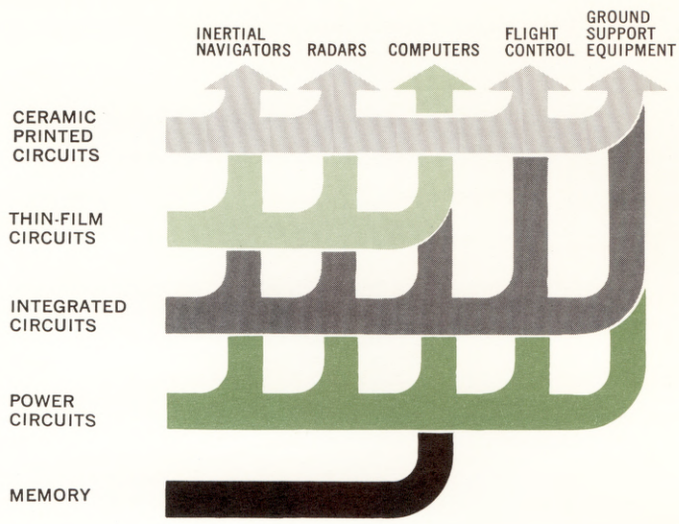
A Typical Appraisal of First-Generation Microelectronics Techniques for a 1-Megacycle Computer

IS THERE A "BEST" TYPE OF MICROELECTRONICS?

Not only must microelectronics be traded off as an entity with other *system* design factors — but, within the technology, tradeoffs must be made with regard to choice of the *type* of microelectronics best suited for a particular application. In this *microelectronics type tradeoff*, as in *system parameter tradeoff*, the factors of performance, cost, producibility, etc, must be weighed to make a final decision.

The Autonetics division of North American Aviation, Inc. recognized the feasibility of combining various microelectronics techniques and devices as far back as the late '50's. Continuing development work and actual application since that time has reinforced the conviction that no single approach is best for all kinds of systems. Various techniques are employed, depending upon the performance, reliability, and cost requirements of the system involved. As a multiproduct manufacturer, Autonetics finds applications for all types of microelectronics, using them in a variety of circuitry — both analog and digital — for inertial navigators, radars, computers, flight control, and ground support equipment.

Autonetics' Systems Usage of Various Microelectronics Techniques:



now offer the best solution. To date, integrated circuit technology has not progressed as rapidly in the r-f field as in the digital, because of the difficulty of fabricating high-speed transistors; however, second-generation semiconductor materials, a novel technique for device isolation, and new economical batch-production processes for field-effect devices are solving this problem, and future r-f systems will be able to exploit the many benefits of integrated circuitry.

Linear Applications

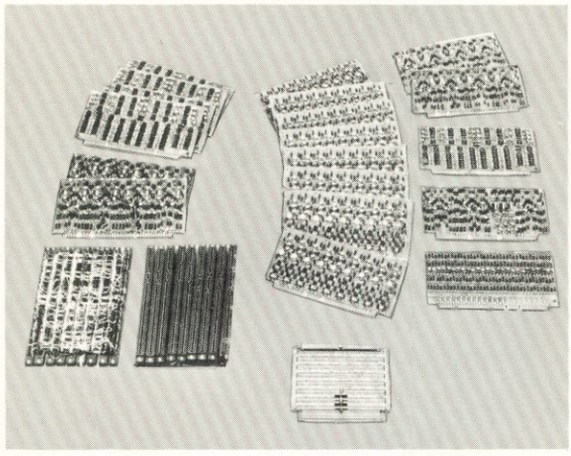
☐ Linear circuits are used in those electromechanical control systems (such as systems for navigation and flight control) which interface with transducers such as gyro pickoffs, accelerometers, velocity meters, servo motors, torquing coils, and voice coils. The circuitry often consists of amplifier circuits; frequency of operation covers the range from dc to 100 kc, with 5 kc being typically the highest frequency.

☐ Because of the low frequencies used in linear electronics, capacitors are big both electrically and physically. (Most of the capacitors in a typical set of linear microelectronics are greater than 1000 picofarads.) This electrical size "difficulty" is compounded by the fact that large numbers of the capacitors are required for coupling and bypass functions.

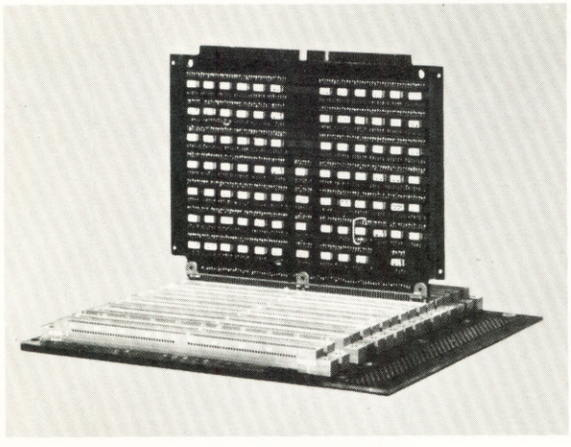
☐ The necessity for linear microelectronics to interface with electromechanical transducers requires power levels to be relatively high, and the microelectronics technology employed must provide compatible mounting methods for power-dissipating transistors and resistors.

☐ Despite these problems, semiconductor IC's have been effectively applied to fill about 70 percent of the circuit requirements in typical electromechanical control systems. Standardized semiconductor IC's have been designed for use with adapting circuits employing discrete and thin-film components. Through revisions in system techniques relating to grounding, power supplies, impedance level, and information format, the need for large capacitors and inductive elements has been greatly reduced. The power-dissipation problem is lessened by operating power amplifiers in the highly efficient switching mode.

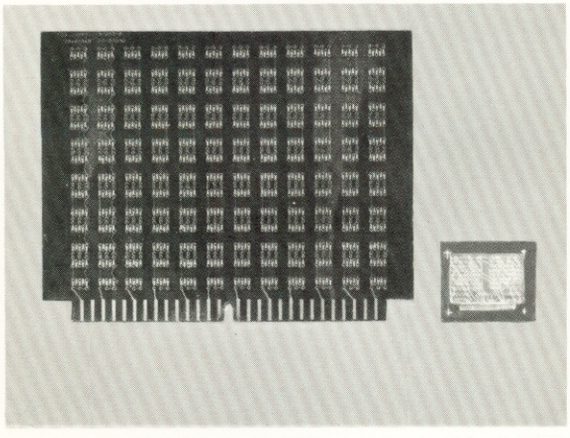
THE *BIG* PROBLEM OF *LITTLE* ROOM—FOR INTERCONNECTIONS



A single Minuteman II MLB (bottom) is the equivalent of as many as 19 conventional circuit boards, plus 19 connectors, and a substantial amount of wire harness



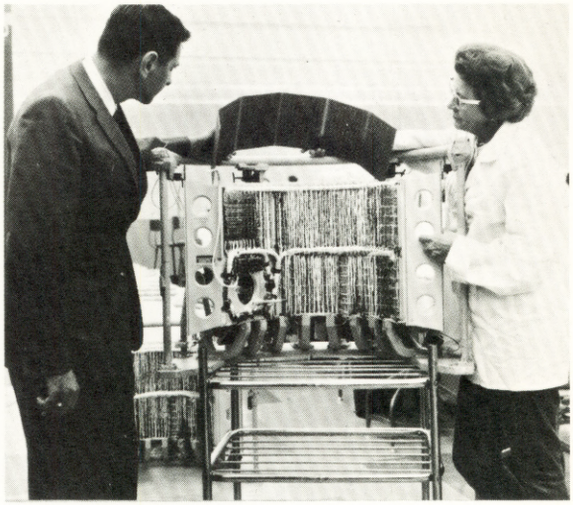
Minuteman II MLB and MIB



High-density Minuteman II MLB compared with thin-film microconductor MLB under development

With microelectronic devices becoming ever smaller and smaller, the interconnecting leads and cabling for the devices soon became actually heavier and bigger than the devices themselves. In answer to the practical impossibility of jamming the required number of leads onto a single layer of etched circuitry Autonetics took the logical step of designing a multilayer board consisting of a number of layers laminated together.

Interconnection techniques developed for early and late models of Minuteman I's N10 computer electronics are contrasted in the photograph below. The conventional wire harness involved complex hand wiring and soldering operations requiring approximately 3000 hours of assembly time. The contoured multilayer "master interconnect" board (MIB) was designed to curve around the N10 toroid and to replace the bulky harness. The pioneering multilayer board—into which were "plugged" the computer's individual etched circuit boards containing discrete electronic components—was made up of 13 layers of standard-size printed wiring and used the inherently reliable plated through-hole interconnection method.

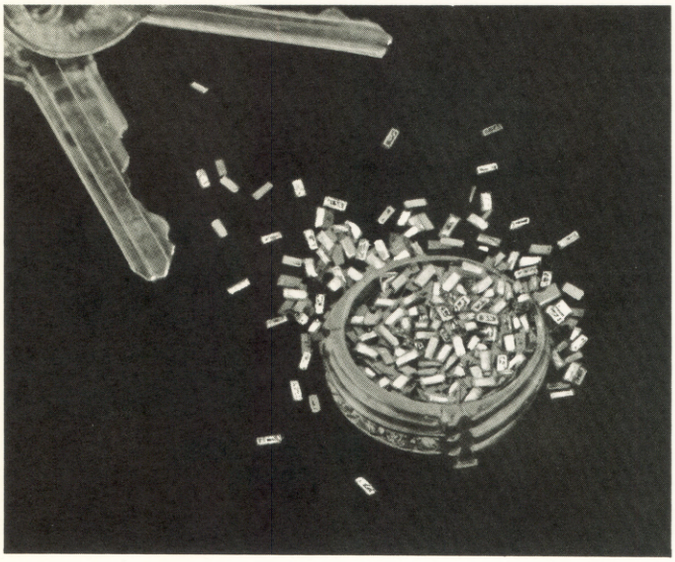


Comparison of contoured MIB designed for Minuteman I with conventional wire harness used in the missile

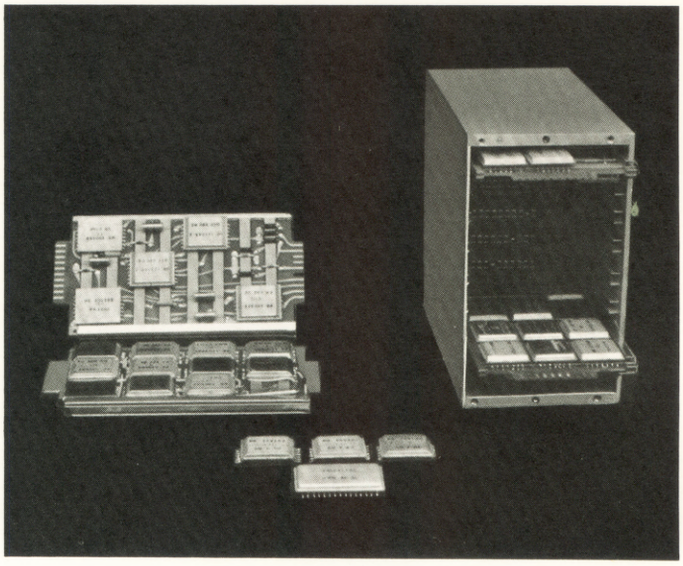
For Minuteman II's D37 computer a 10-layer high-density circuit board has been developed to take care of such new microelectronic devices as semiconductor integrated circuits; interconnections between planes in the board are made through 30-mil-diameter plated through-holes. A master-interconnect board to accommodate the high-density multilayer circuit boards (MLB's) has been developed concurrently.

Even the high-density MLB's for Minuteman II will be out-paced by the thin-film multilayer boards now in the advanced development stage at Autonetics. Conductor patterns for these boards are obtained by photolithographic and etching techniques. The thin-film conductor and insulation networks are applied by vacuum deposition of conductive and insulating materials in accordance with a master pattern. Circuitry line-widths as small as 2 mils have been achieved.

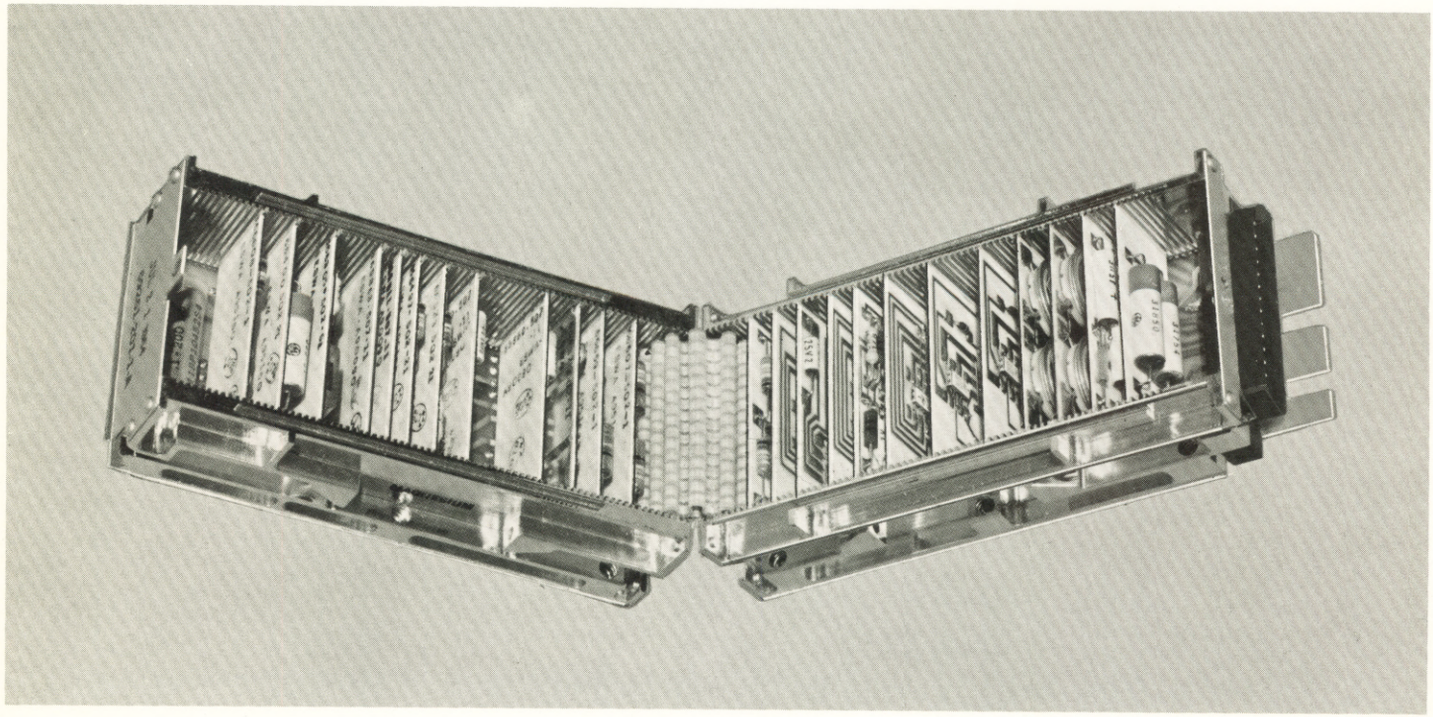
DIFFERENT APPLICATIONS — DIFFERENT MICROELECTRONICS



The quantity of semiconductor integrated circuits (IC's) in this wedding ring can form as much as 95% of the electronics for advanced computers.



Thin-film circuits—mounted on interconnection boards—yield low-profile microelectronics packaging for radars.



Individual ceramic printed circuits (CPC's) fit into tracks on the inner walls of this inertial autonavigator module.

Second-generation microelectronics

☐ The evolution of microelectronics has been given impetus by a changing motivation. At first, major emphasis was placed on size reduction; later, reliability was the chief selling-point, followed then by the suitability of microelectronics for digitalization. Today, new materials and processes are bringing cost reduction to take its place among significant microelectronics benefits — along with even higher reliability and lower weight, cube, and power.

☐ The first-generation step that integrated separate circuit elements into a complete-circuit unit is now being followed by the second-generation step of integrating hundreds of circuits into a single monolithic unit. Economical ways have been found to quantity-develop low-usage semiconductor integrated circuits for linear systems. More efficient and reliable methods of microelectronics joining are cutting production hours and dollars. At the same time, still widely applicable first-generation devices are undergoing constant second-generation evolution, improving both physically and functionally.

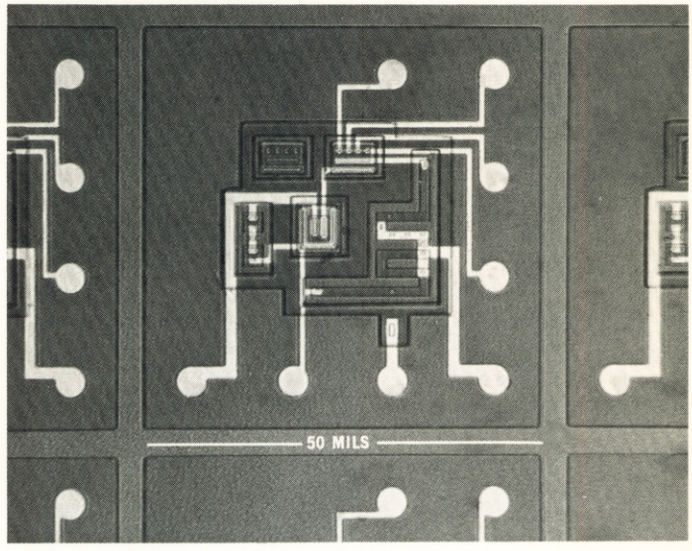
MOS Technology

☐ One of the most dramatic second-generation achievements is the transformation of metal-oxide-semiconductor (MOS) technology from a laboratory curiosity into usable microelectronic devices.

☐ Looking through a microscope at a "conventional" integrated circuit, it seems almost impossible to imagine being able to get a greater number of separate individual devices into a single monolithic chip. But the proud ability of the bipolar IC to carry up to 2000 separate elements promises to become "old hat," with the laboratory emergence of field-effect MOS and its potential device density of as high as 100,000 elements in the same area.

1960

200 Logic Gates
2000 Active Elements

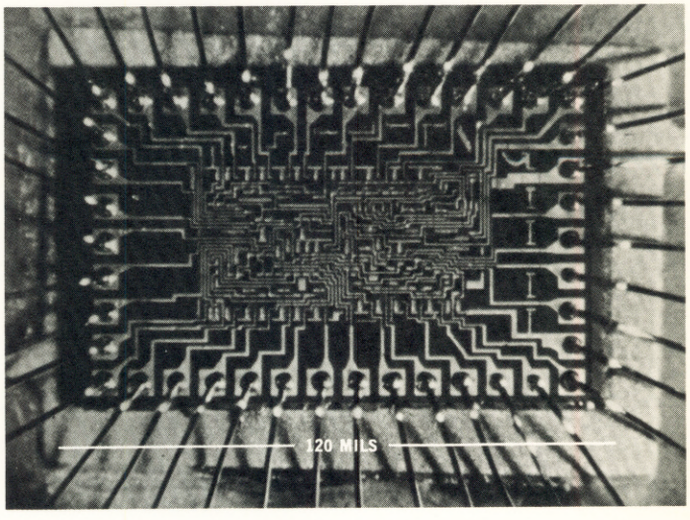


Yield: 2% To 5%

CONVENTIONAL IC

1965

100 Functional Circuits
50,000 Active Elements



Yield: Up To 50%

MOS DEVICE

☐ With MOS, functional complexity of circuitry can be increased as much as 30 to 50 times over that of the most complex double-diffused IC—either without increasing, or often actually decreasing, the space required and, at the same time, with an increase in yield.

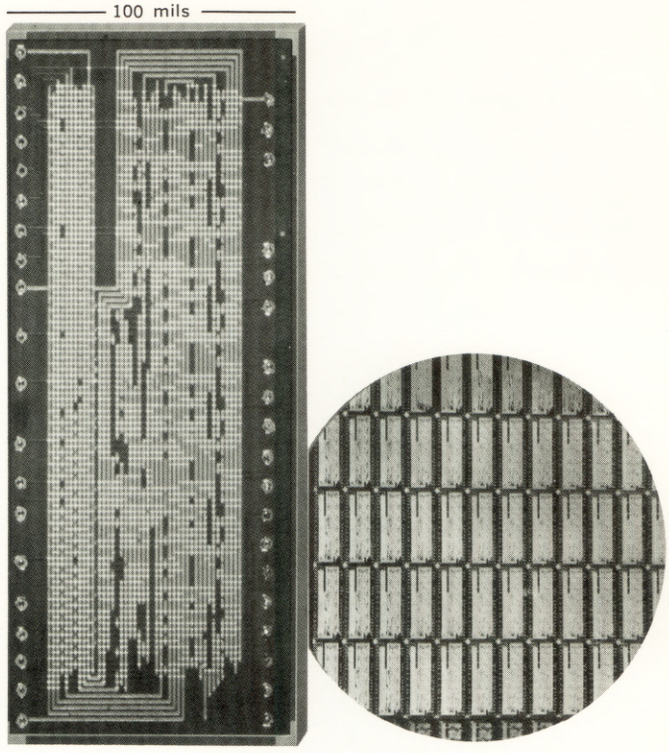
☐ *Specific examples of MOS "magic": A typical MOS logic NAND occupies only 9 sq mils, in contrast to 300 sq mils for a double-diffused integrated circuit NAND. A single MOS chip can replace as many as 100 functions of conventional double-diffused IC's, or as many as 1000 discrete components.*

☐ What exactly *is* a "MOS" device? Actually, it is a new type of semiconductor IC. Like the conventional IC, the MOS unit uses silicon as a substrate, into which its circuits are "written" by diffusion. MOS devices, however, furnish their own natural inter-element insulation. There is, thus, no need for elaborate isolation schemes, and the circuit complexity and number of circuits possible per chip are promising by-products.

☐ Unlike conventional IC's, a MOS device operates through the control of an electric field, rather than of a biased junction between portions of the device. (See Appendix I.)

☐ Although patents for field-effect devices were issued as long ago as 1930, MOS FET's (metal-oxide-semiconductor field-effect transistors) were not manufactured until the middle 1960's, due chiefly to the difficulty of developing silicon of sufficient purity for the field effect to "work." Even when, around 1955, techniques were perfected for producing silicon of the necessary quality, MOS FET's still had to await the later development of planar techniques and improvement of material-processing skills.

☐ The promise of MOS FET is not simply for reduced size and increased device density; systems designers have been and can certainly continue living happily with the density limits of conventional IC's. MOS' main offering is cost reduction, which it brings about in a number of ways. First of all, increased yield of MOS batch-fabrication processes—teamed with the enormously increased device density per chip — add up to a potential 10-fold cut in production costs. Going beyond production to actual operation "in the field," cost savings are many times multiplied by logistics economies. Permissible density and complexity of MOS chips make the new technology suitable to perform subsystem*—indeed,



MOS Digital Circuitry

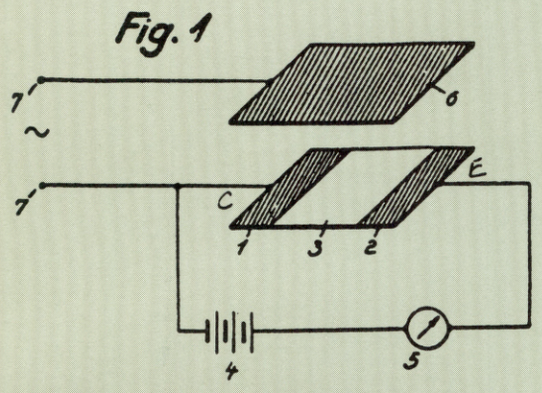
Autonetics' logic designers have decreased the size of a functioning group of circuits by a factor of 50, while increasing the effective parts count by a factor of 2, to give an overall two-order-of-magnitude increase in component density. On the 100-by-200-mil silicon chip shown here are approximately 800 effective discrete components. With computerized layout, the period from start of logical design and layout to the time of first unit availability for test is greatly reduced. *(Note the regularity of the MOS shown here, resulting from computerized layout, in contrast to the manually designed MOS on page 17.)*

*A "subsystem" as used here would be a full arithmetic unit, for example, while "system" would denote an entire computer made up of a number of subsystems."

even entire system—functions. Future logistics engineers will be able to isolate and replace malfunctioning elements to at least the subsystem level, and requirements for maintenance personnel skill and training, for handbook documentation, and for amount and complexity of ground checkout equipment will all be lowered accordingly. All of these logistics simplifications will underline the cost effectiveness of the MOS-mechanized hardware.

□ In addition to these primary economic advantages, MOS offers the already mentioned extremely small geometry, plus the characteristics of high input impedance and self-isolation of individual devices (no separate diffusion step is required for isolation). Furthermore, its principle of operation (as a majority-carrier device) makes MOS potentially more tolerant of the effects of radiation than other forms of microelectronic circuitry.

FIELD-EFFECT TRANSISTORS GO BACK TO THE 1930'S



Legend:

1 and 2 Ohmic contacts to the semiconductor

3 Thin layer of semiconductor (such as tellurium, iodine, cuprous oxide, or vanadium pentoxide)

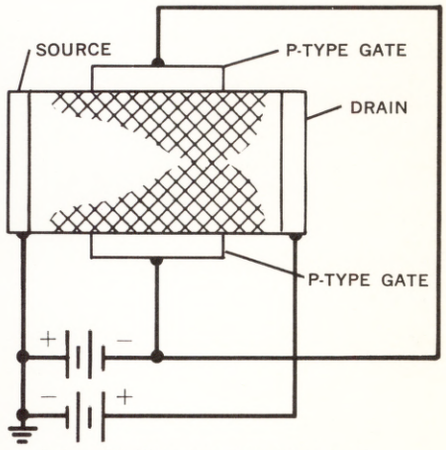
4 Battery

5 Current meter

6 Thin metallic layer adjacent to, but insulated from semiconductor layer — serves as control electrode

Operation: Signal on control electrode modulates resistance of semiconductor layer, so that amplified signal is produced, as is observable with meter.

Drawing from British Patent No. 439,457, showing early field-effect structure; inventor, O. Heil, 1935.



Schematic Diagram of W. Shockley's Unipolar Field-Effect Transistor, 1952

First attempts to develop active field-effect devices are revealed by an amazingly early series of patents granted to J. E. Lilienfeld, including U. S. Patent No. 1745175, issued in 1930, and No. 1877140 and 1900018, both issued in 1932.

In 1935, a British patent was granted to Oskar Heil of Berlin, Germany, for "Improvements in or Relating to Electrical Amplifiers and Other Control Arrangements and Devices." Study of the inventor's original patent reveals the device to be describable in today's microelectronics language as a "unipolar field-effect transistor with insulated gate."

Following World War II, studies were carried out at Bell Telephone Laboratories under the direction of W. Shockley, leading to the discovery of the transistor effect by Bardeen and Brattain in 1948. In 1952, a paper was published by Shockley describing a unipolar field-effect transistor; this paper has become a basic reference for subsequent FET development. In the paper, Shockley described a unipolar field-effect transistor with a control electrode consisting of a reverse-biased junction. Later, C. Dacey and I. M. Ross actually built and tested such transistors, and, in 1955, made a detailed analysis of their performance limits.

Manufacture of MOS FET's has only recently become economically feasible, since only recently has there been devised a practical method of reducing surface impurities to a sufficient degree for the field-effect principle to be usable. Until as late as 1954, it was impossible to develop silicon of sufficient purity for even the conventional "non-field-effect" transistors, except by a complicated 20- to 30-step refining procedure. The MOS field-effect transistor was impossible to make until planar techniques became practical, and even then stability was still a problem not to be solved until the mid-1960's, with development of a controllable process for batch-fabrication of stable, producible, uniform MOS devices.

Improvements to First-Generation Devices and Their Packaging

☐ Less dramatic than MOS, but extremely important to growth of the microelectronics art, are such second-generation improvements to first-generation devices and their packaging as dielectric isolation in integrated circuitry, conductive through-holes for ceramic printed circuits, a thin-film hybrid approach to high-density interconnection, compound semiconductor devices, and volume-development of IC's for linear system applications.

Dielectric Isolation

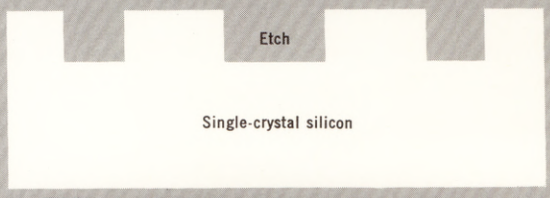
☐ First-generation semiconductor IC's insulate between active elements by means of voltages on the elements that cause them to act, relative to one another, like reverse-biased diodes. Current cannot flow between the "diodes" due to this back-biasing, and the practical result is that each active element is isolated from all others on the substrate—within limits. The "diodes" have breakdown voltages just as capacitors do, and these voltages are quite low. Also, when subjected to some types of radiation, the IC semiconductor materials can exhibit changes which completely nullify the ability of the device to perform as an integrated circuit, and this effect is irreversible. Finally, stray capacitances in the device seriously stunt the frequency range over which it can operate.

☐ The so-called "Poly" * or "dielectric isolation" technique actually coats each active element with a completely-surrounding layer of glass insulation. Between each two of these glass-coated islands, insulation strength is in the neighborhood of 1000 volts.

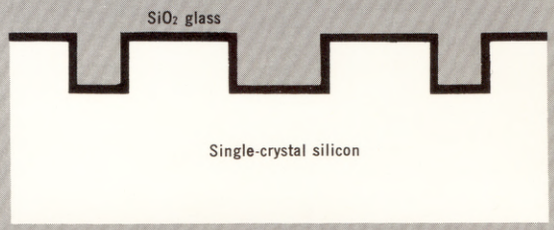
**The glass-insulated elements are mechanically supported in a polycrystalline silicon wafer—hence, the term "Poly process" for this Autonetics invention.*

DIELECTRIC ISOLATION

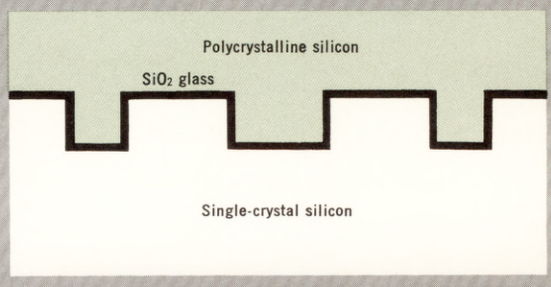
Autonetics is one of the few organizations that have developed a controllable, repeatable, economical process for growing crystalline material required for dielectric isolation. Steps in the Autonetics process are simplified here for clarity.



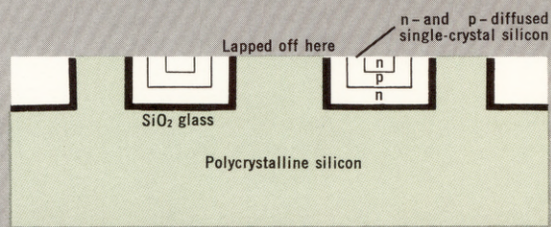
1 FIRST, A "CHUNK" OF SINGLE-CRYSTAL SILICON IS ETCHED TO THE PROPER DEPTHS AND WIDTHS TO FORM SLOTS THAT WILL CONTAIN THE INDIVIDUAL TRANSISTORS AND OTHER ACTIVE ELEMENTS MAKING UP THE CIRCUIT.



2 OVER THE SURFACE OF THE SINGLE-CRYSTAL SILICON SUBSTRATE, INCLUDING THE SURFACES OF THE ETCHED SLOTS, A LAYER OF GLASS (SILICON DIOXIDE) IS THERMALLY GROWN ONLY 10,000 ANGSTROMS THICK. (TEN THOUSAND ANGSTROMS IS ONLY 0.04 MIL, OR FOUR ONE-HUNDRED THOUSANDTHS OF AN INCH.)



3 OVER THE ENTIRE DEVICE, THERE IS THEN DEPOSITED POLYCRYSTALLINE SILICON. (THIS ACTS LIKE CEMENT, TO HOLD EVERYTHING TOGETHER.)

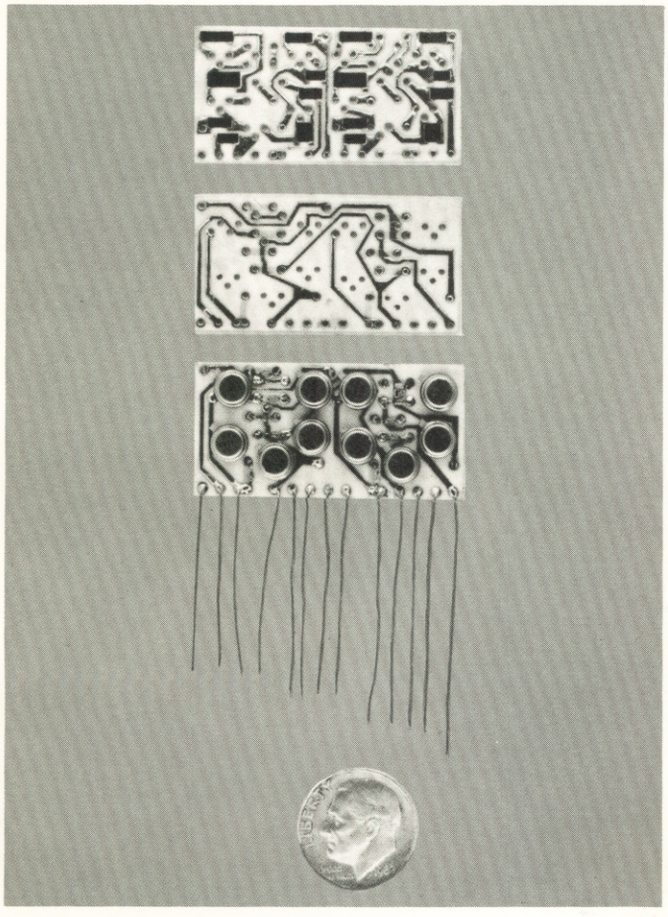


4 FINALLY, THEN, THE SURPLUS OF THE ORIGINAL SINGLE-CRYSTAL SILICON IS GROUND OFF, AND THE N AND P DIFFUSIONS ARE MADE TO FORM A FINISHED DEVICE, WITH ALL ACTIVE ELEMENTS ISOLATED FROM ONE ANOTHER BY SILICON DIOXIDE GLASS.

Ceramic Printed Circuit Advances

☐ Recent enhancement of the CPC technology has resulted in techniques for drilling holes in the substrate and screening conductive material *through* the hole to form a conductive "through-hole." This provides a greater degree of design freedom, since both sides of the substrate can be utilized and interconnected, and crossovers can be easily provided.

☐ The through-hole method permits the use of axial-lead micro parts, as well as radial-lead devices. The CPC or "thick-film" technology was originally developed as a *circuit* package technique, but the advent of the through-hole broadens its application into the *module* area.

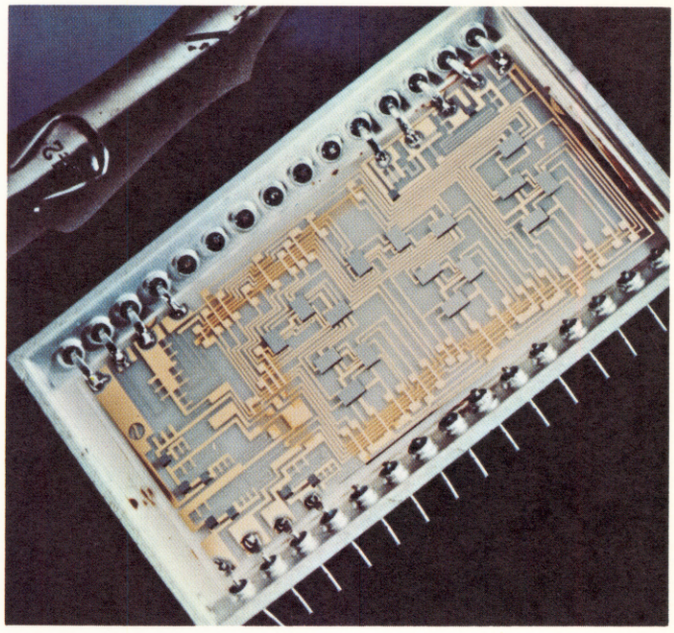


Through-Hole Ceramic Printed Circuits

Thin-Film Hybrid Packaging

☐ Interconnection density is vastly multiplied by a thin-film hybrid approach, in which solid-state active devices are bonded to thin-film passive circuitry.

☐ In the advanced thin-film hybrid "interconnection board" shown in the next illustration, uncased semiconductor integrated circuits are bonded to a thin-film conductor network. The unit shown contains 23 solid-state devices, which, because they are uncased, require only 265 bonds in contrast to the 795 bonds that would be needed for individually cased devices. Also, since all 23 devices are enclosed in the single interconnection board package, only one hermetic seal is required, in contrast to the 23 separate ones demanded by conventional, individually packaged IC's.



Thin-film hybrid interconnection board containing uncased active devices bonded to passive thin-film circuitry. Unit shown is a 7-bit counter.

Compound Semiconductor Devices

☐ Numbers of required interconnections and separate bonds are vastly diminished by the containment of as many as six different bipolar integrated circuits on a single silicon chip. Bond and interconnection requirements are reduced, and only one hermetic seal is necessary for the multifunction package. Furthermore, the simplified fabrication process, with its smaller number of steps, smaller amount of bonding and interconnection, and reduced human handling, promotes reliability and lowers costs.

Volume Development of Custom Designs

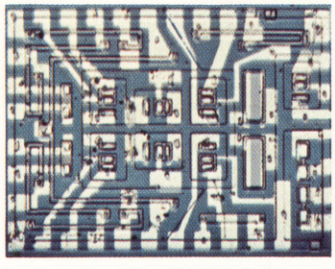
☐ Thanks to such developments as the "master dice" technique, the seemingly mutually exclusive operations of quantity production and low linear-circuit usage are becoming as compatible as the proverbial thieves.

☐ In linear systems, many different kinds of circuits are required, but, as mentioned above, usage of each of the individual kinds is extremely low. In contrast to the circuit-type-repetition characterizing a digital computer, "high usage" in a linear system is on the order of 20 of the same kind of circuit, and "average usage" is more like from two to ten. The spending of large amounts of development money on each type of these low-usage circuits would be hard to justify, but batch methods like "master dice" processing provide low-cost, fast-turnaround means for developing *many varieties* of low-usage linear circuits *simultaneously*.

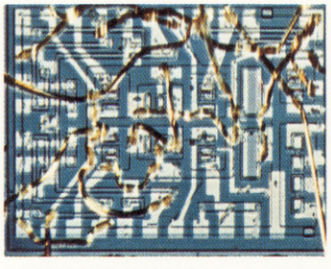
☐ With master dice, for example, "custom" circuits can actually be "volume developed." A number of basic bipolar semiconductor integrated circuits are built to make up a set of "standard dice," each die containing transistors, diodes, and resistors, but no interconnections between these elements. During development, the active elements can be interconnected in various ways to form custom circuits. When the circuit design thus achieved is finalized, identical master dice are used by suppliers to produce the IC in the necessary quantity, the only difference being that, in the production model, interconnections are *deposited* on the substrate rather than being made up of actual wires.

"MASTER DICE" TECHNIQUE

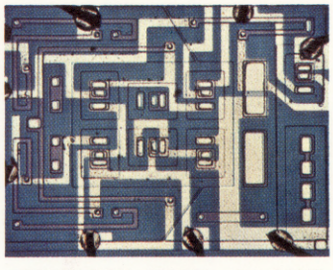
The "master dice" technique is an engineering tool for breadboarding and developing custom semiconductor integrated circuits. The process is the brainchild of Autonetics' linear system design engineers and serves as an answer to the high cost of IC development for their kinds of applications.



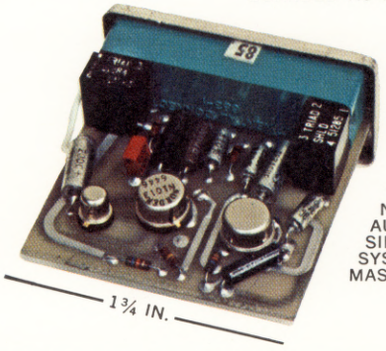
UNWIRED MASTER DIE



THE SAME MASTER DIE BREADBOARDED AS A PREAMPLIFIER



PRODUCTION MODEL OF SAME MASTER DIE WITH DEPOSITED INTERCONNECTIONS AND WITH BONDED LEADS FOR ATTACHMENT TO PACKAGE TERMINALS



THE AMPLIFIER SHOWN HERE—NOW IN PRODUCTION AT AUTONETICS FOR THE U.S. NAVY'S SINS (SHIP'S INERTIAL NAVIGATION SYSTEM)—WAS DEVELOPED BY MASTER DICE METHODS.

Joining

☐ Since the advent of true microelectronics on the Minuteman II Program, the joining technology has undergone a burgeoning growth. New packaging concepts have required the development of new inter/intraconnection techniques. Increasing circuit densities have required "high-resolution" joining methods. Working tools have grown ever smaller, and working areas have become truly microscopic.

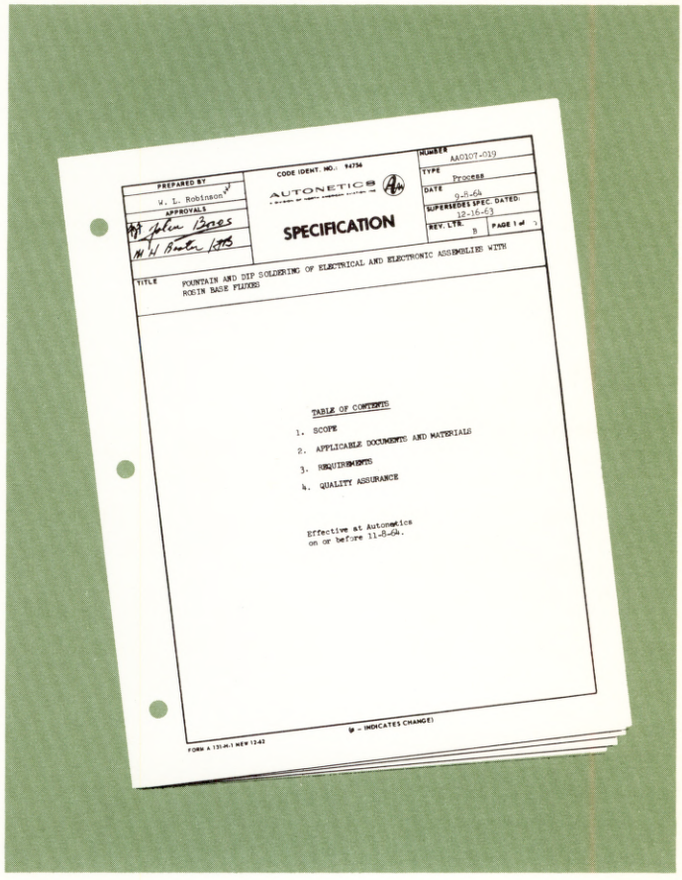
☐ Just as there is no universally best type of microcircuitry, there is no universally best type of joining, and many techniques have been developed, and are still being developed, to interconnect the devices into systems. All of these techniques have the estimable aim of avoiding degradation of the circuits, devices, and subsystems which they connect—by being reliable, producible, inspectable, and repairable. Some of the techniques are in everyday use—others require further development before attaining the degree of perfection and resulting reliability necessary for widespread application outside the laboratory.

☐ One method deserving special note here is registrative or "flip-chip" bonding, because of its marked potential for improving reliability, reducing assembly time, and lowering production costs.

☐ "Flip-chip" bonding is a technique for *inverted* joining of a device chip to a matching substrate conductor pattern. The device chip is fabricated to contain, in addition to active, passive, or other "working" networks, a pattern of metal contact pads; the pad pattern on the substrate is an exact mirror image of the pattern on the device chip.

☐ To interconnect the device chip to the substrate, the chip is *flipped* (hence, the name of the process) and, while it is face down on the substrate, its contact pads, projecting slightly from the surface, are brought into precise register with the mating contacts on the device chip. Heat and pressure (or other forms of energy) are then applied, and the pad areas are joined together. The joining techniques which can be used are many—including microsoldering, ultrasonic bonding, and thermocompression bonding. Each has advantages in certain areas requiring cost and reliability tradeoffs.

☐ For mounting integrated circuits within conventional packages, flip-chip bonding eliminates individual wire connections from the IC to the outgoing leads of the package and greatly heightens reliability of the device. It is also used to bond uncased microelectronic devices to microminiature interconnection boards such as the ones described on page 94.



An Autonetics document-controlled assembly-line soldering process has produced more than 250 billion solder-joint-hours of performance for missile systems without a single reported failure of a solder joint.

MICROELECTRONICS JOINING

JOINING TECHNIQUES

SOLDERING

Hand-bit — Manual operation in which a miniature soldering iron is used in fabrication of printed circuit boards, "cord-wood" modules, etc.

Dip — Automatic operation in which circuit boards are dipped into molten solder. Basic processes have been modified to allow use with CPC's.

Resistance — Semiautomatic or automatic operation in which components are individually soldered by direct or indirect I^2R heating between two electrodes. Automated version has been used to fabricate ceramic printed circuits for Minuteman.

Flow or Wave — Automatic operation in which printed circuit boards with discrete components are passed on a conveyor belt through a "wave" of molten solder.

WELDING

Cross-wire — Welding by discharge of a capacitor bank through the materials to be joined. Semiautomatic equipment has been developed.

Series (parallel gap) — Use of resistance welding techniques to attach IC and discrete microcomponent leads to various other circuitry.

Electron beam — Welding by impingement of a high-energy electron beam onto joining area to produce a microfusion weld. Small beam diameter (0.0005 to 0.001 inch) permits high weld density.

Laser — Use of heat produced by focused beam of coherent light to melt the joining members and form a weld. Now limited to pulse-type operation at low repetition rate.

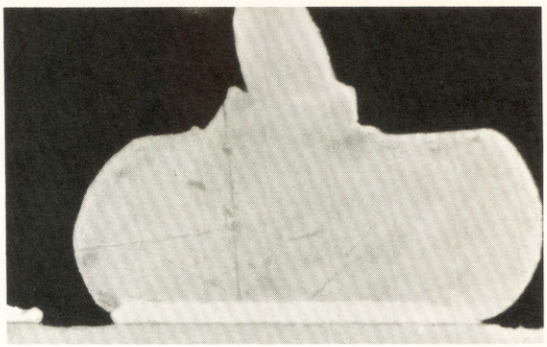
THERMOCOMPRESSION (TC) BONDING — Coalescence of two materials, of which at least one is ductile, by diffusion between the members being joined. Small gold, copper, silver, aluminum, platinum, and tin lead wires and ribbons have been successfully TC-bonded directly to various semiconductor materials or to an intermediate vapor-deposited metallic conductor film. The gold wire-to-aluminum vapor-deposited circuitry combination is most predominantly used for bonding to surfaces of IC's and many transistor devices. Two basic types of TC bonding are "wedge" and "nailhead."

Wedge — Process in which a wedge-shaped tool is used to plastically deform a small-diameter wire into intimate contact with the semiconductor or metallic conductor.

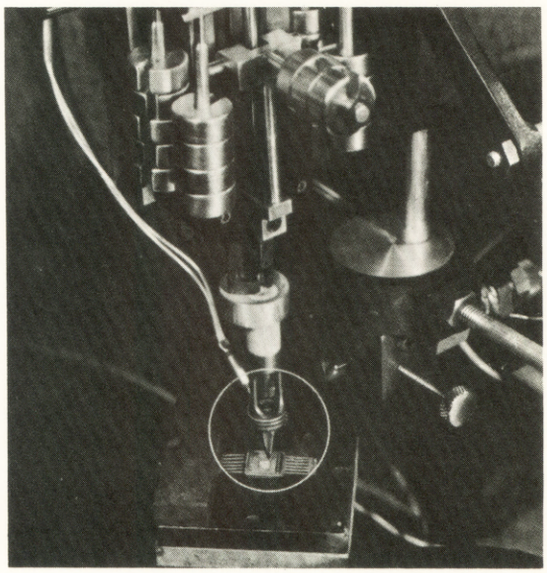
Nailhead — Process in which a ball is formed in a hydrogen flame at the end of a small-diameter wire. The ball is then deformed into intimate contact with the bonding surface.

ULTRASONIC BONDING — Process in which ultrasonic energy is used to break up surface oxides, bringing the bonding surfaces into intimate contact and producing a metallurgical joint.

SERIES (MICRO-GAP) BONDING — Process in which bonding is accomplished by an electrical pulse passed between two electrodes which are shorted by one of the joining members.



a.

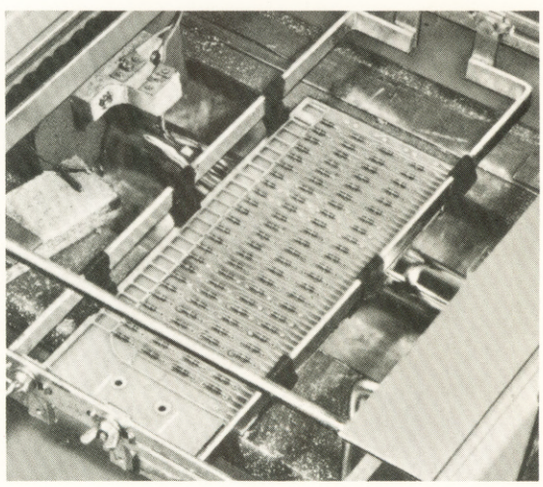


b.

NAILHEAD THERMOCOMPRESSION BONDING EQUIPMENT AND BOND

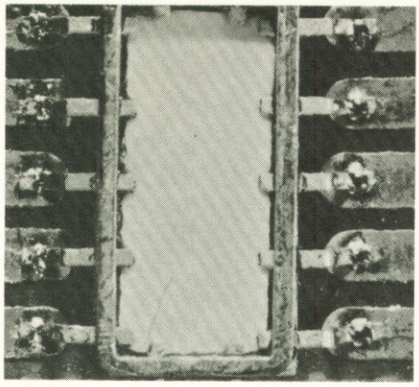
a. Cross-section of bond between 1-mil gold wire and vapor-deposited aluminum on silicon.

b. Example of a nailhead thermocompression bonding attachment. Circled area includes the heated tungsten carbide bonding capillary, flame-off nozzle, and a flat package containing a semiconductor integrated circuit.

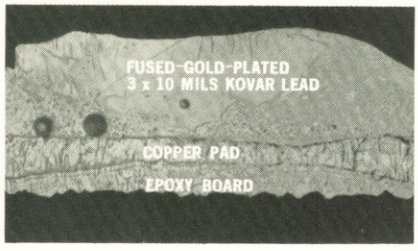


FLOW SOLDERING

Conveyor system moves board through a wave of solder.



a.



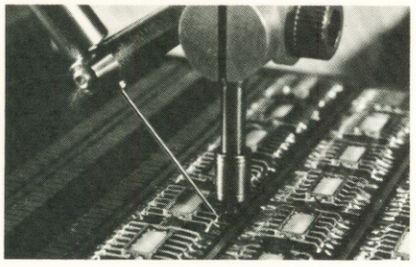
b.

LASER WELDS

a. Leads of a dummy IC package have been welded to conductor pads on a glass epoxy circuit board, using a 1-joule ruby laser.

b. Microsection of the 3 by 10 mils Kovar lead welded to copper circuitry.

a.

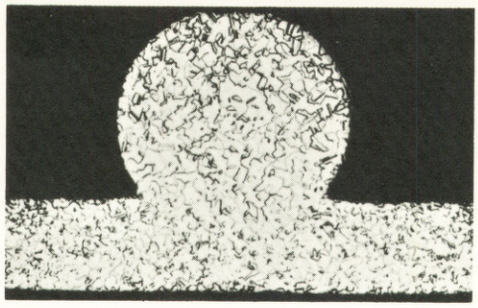


b.

RESISTANCE SOLDERING

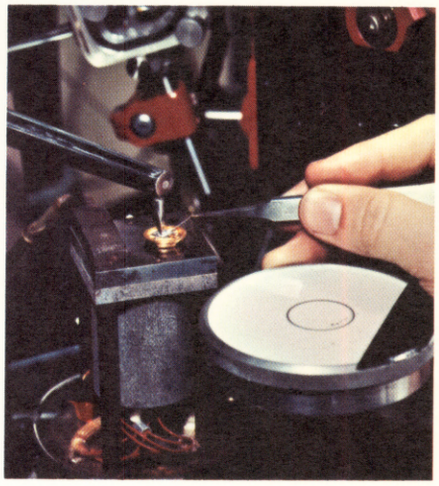
a. Resistance soldering equipment.

b. Resistance soldering of integrated circuits on multilayer board.



CROSS-WIRE WELD

Microphotograph shows nickel wire (20-mils diameter) welded to a nickel ribbon (10 by 30 mils).

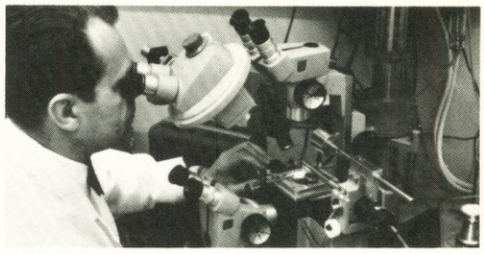


ULTRASONIC BONDING

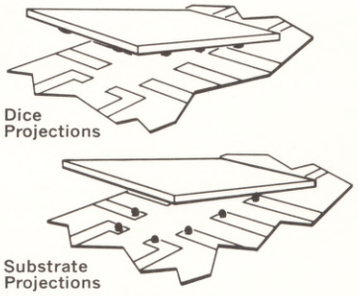
Ten-mil aluminum wire is being bonded to a power transistor.

REGISTRATIVE (FLIP-CHIP) BONDING

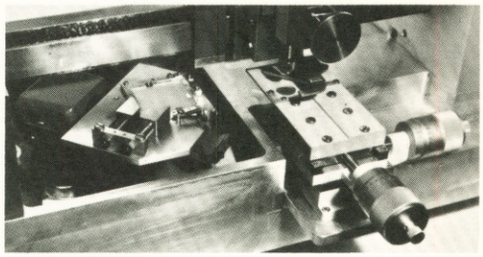
Packaging and assembly costs discovered during a microelectronics cost analysis at Autonetics have led to development of a semiautomatic flip-chip bonding machine. It was found during the analysis that the greater part of microelectronics production costs were those of packaging and assembly. Rapid handling of bonding operations by the machine have cut costs by 90%.



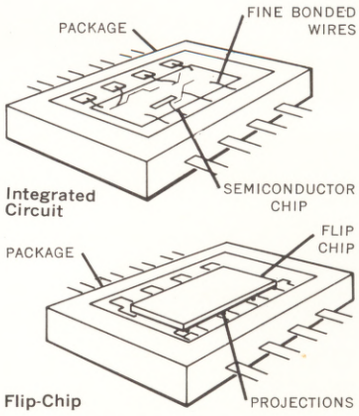
LABORATORY FLIP-CHIP BONDER



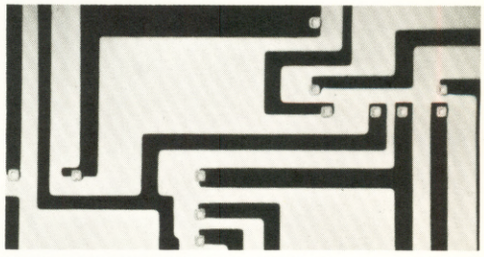
PROJECTION LOCATIONS



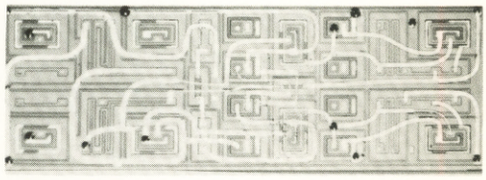
SEMIAUTOMATIC FLIP-CHIP BONDING MACHINE DEVELOPED BY AUTONETICS



COMPARISON OF THE CONVENTIONAL METHOD FOR CONNECTING IC TO PACKAGE AND THE FLIP-CHIP TECHNIQUE



ELECTRO-DEPOSITED PROJECTIONS



CONICAL GOLD PROJECTIONS FLIP-CHIP BONDED BY THERMOCOMPRESSION TO GOLD THIN-FILM IC INTRACONNECTS

A major microelectronic systems organization and what it is doing today

☐ To the visitor from "outside," the microelectronics shops and laboratories of North American Aviation's Autonetics Division seem a bewildering mixture of alphabet soup and technological complexity. The Division is one of this nation's largest and most experienced aerospace systems designers and manufacturers—as well as the most extensive systems user of microelectronics. Its scientists have brought forth an impressive number of microelectronics breakthroughs, including (alphabetically speaking): POLY, SOS, YIG, and many others. It would be strange if Autonetics' scientific staff did not produce such progeny—having at their immediate disposal, as they do, one of the most complete facilities in the world for microelectronics research, development, and pilot-line production.

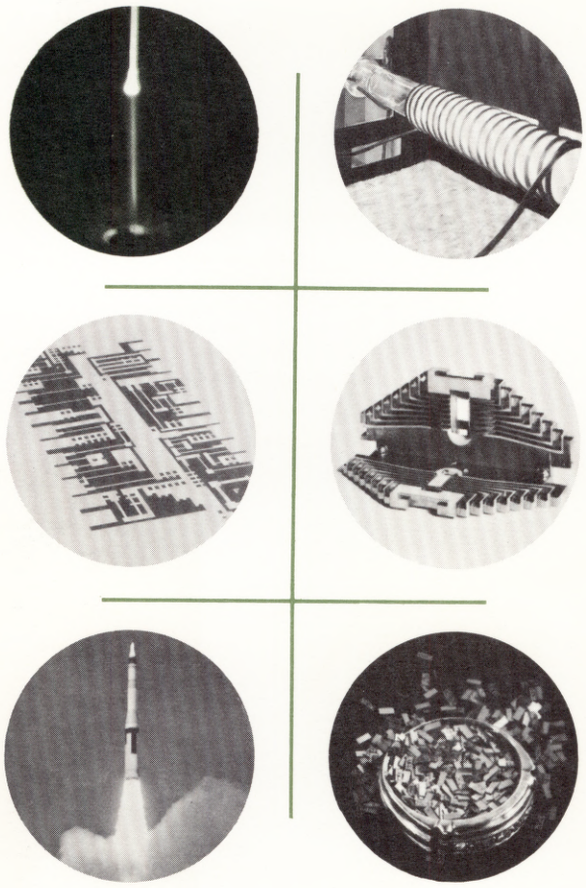
☐ To a degree unparalleled by any other technology, microelectronics is an interdisciplinary blend of sciences—physics, chemistry, and electronics. Autonetics is uniquely qualified for microelectronics by impressive strength in materials research, plus the complementary capability to translate research findings into equipment performance.

☐ One of the things that make Autonetics remarkable in the microelectronics industry, and noted by visitors to the 290-acre complex in Anaheim, California, is the diffusion of microelectronics activities throughout the Company.

☐ Coordinated purpose and focus are given by an Advanced Electronics Department comprised of three sections — Microelectronics Engineering, Materials and Processes Laboratories, and the Central Microelectronics Laboratory. Advanced Electronics has its own assigned research and development tasks in the areas of microelectronics interconnection techniques, joining methods, semiconductor diffusion processes, and microelectronic circuitry and memory design. At the same time, the department has the responsibility for making producible any promising microelectronics development of Autonetics' product divisions and Research Center, designing a pilot-line production process for it, and writing detailed specifications for its manufacture by the Company or its suppliers.

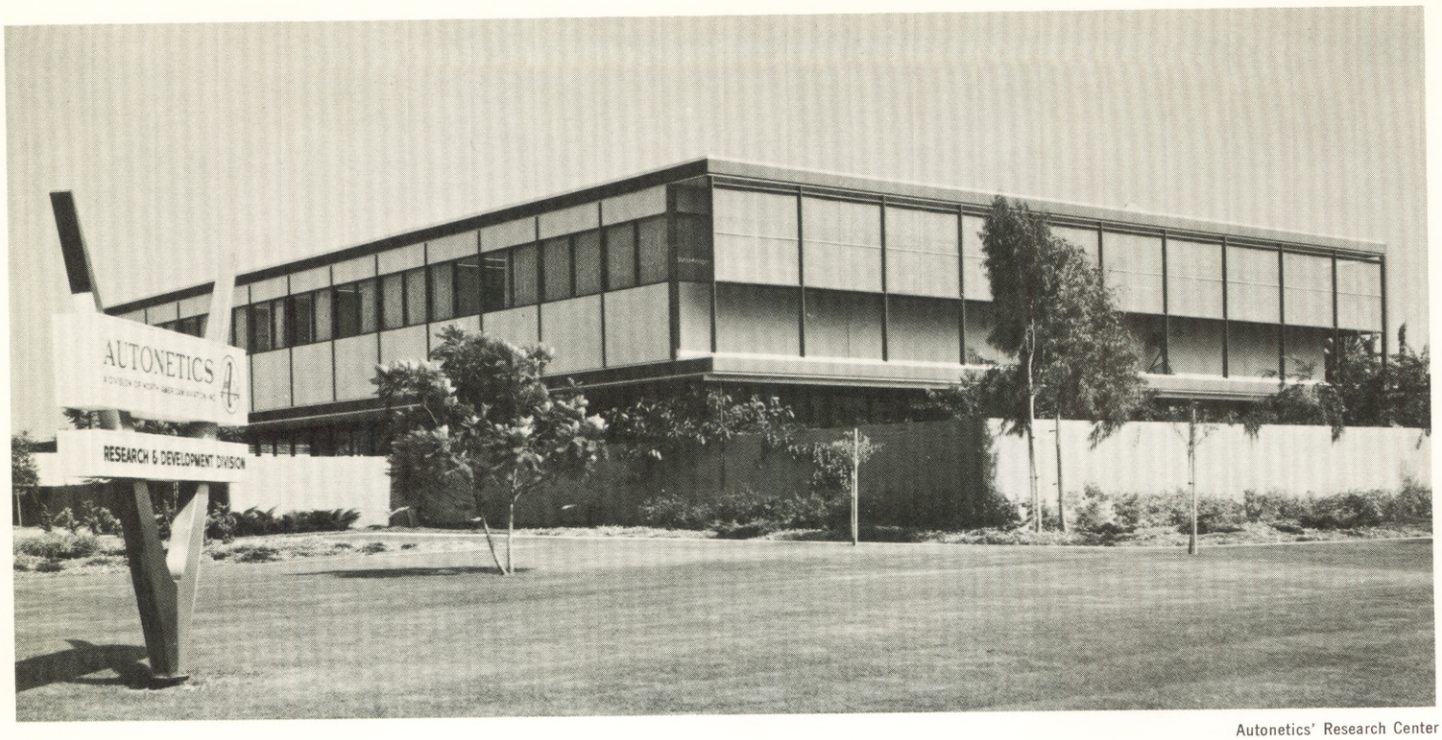
☐ While held within the reasonable boundaries of Company objectives by the firm yet flexible reins of the centralized Advanced Electronics Department, the product divisions are free to pursue the intriguing lines of development indicated by their product lines' special requirements. To this "directly applicable" research of the product divisions, is added the "purer" research of the Research Center in its own superbly equipped building near the Company's headquarters. The parent NAA Kindelberger Science Center stands ready for consultation and guidance in the conduct of any of Autonetics' research projects.

☐ Autonetics' leadership in microelectronics stems from the multiplicity of its roles in this technology—as researcher, developer, designer, producer, purchaser, and user in systems. This multiplicity of roles is borne out by the collection of words and pictures presented in the next section of this book.



Researcher...

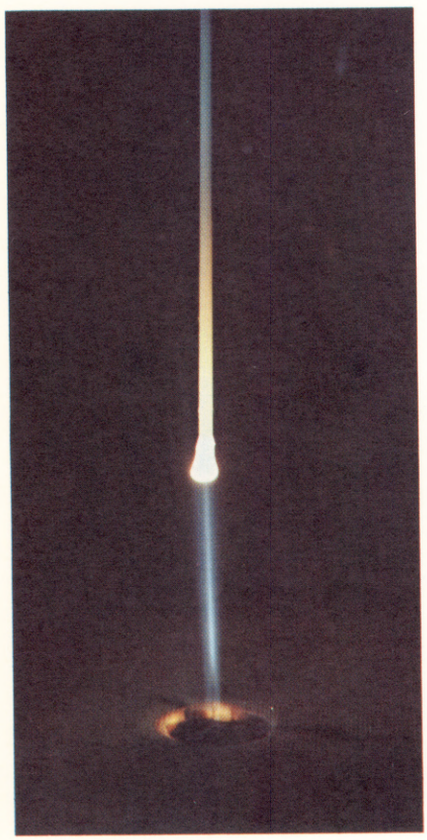
All of Autonetics' systems hardware achievements are born from the solid background of a comprehensive research program. In no technological area is this more meaningful than in the area of microelectronics. The materials, processes, and devices of microelectronics all have their origins in research—and it is from the brilliant conceptions of research that the improved systems for defense, industry, and exploration are ultimately begotten.



Autonetics' Research Center

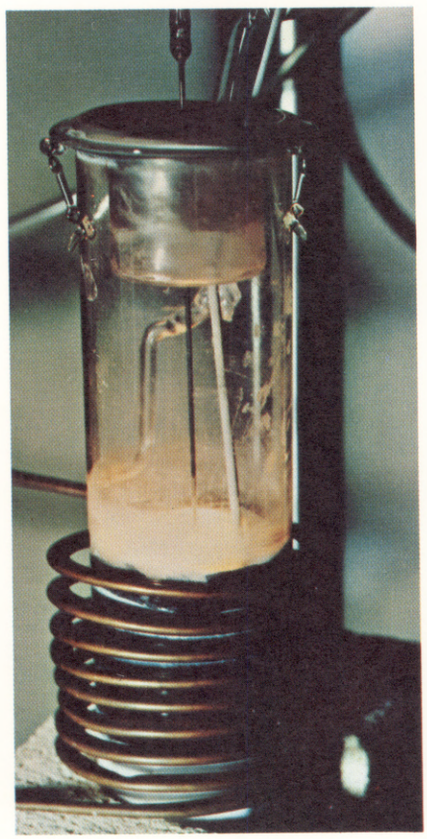
Crystal Growth Facilities

Facilities exist in the Research Center for growing a wide range of crystals from many different materials and in a variety of forms. The facilities include those for the following crystal-growth techniques: Verneuil, hydrothermal, Czochralski, Bridgman, and chemical vapor-deposition. A variety of techniques is required because of individual technique limitations with respect to crystal form and tolerable temperature. Each technique is able to produce crystals only of certain structure (thin-film, long-rod, bulk or large-crystal), and melting temperatures of raw materials are prohibitive for some processes.



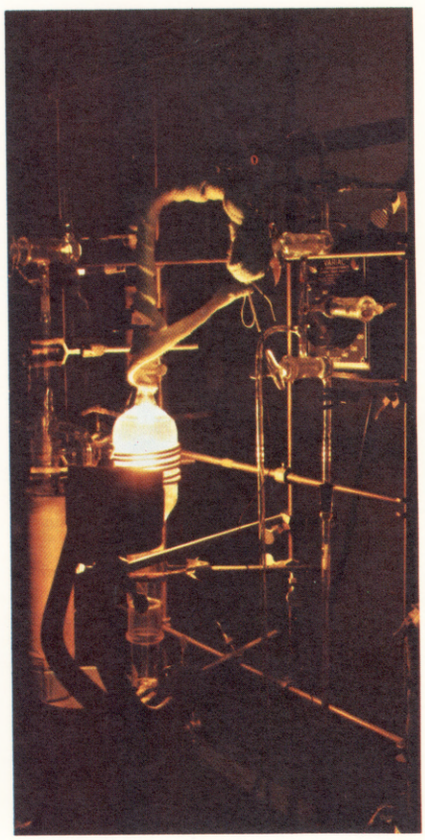
Verneuil

Source powder is fed down through an oxyhydrogen flame and onto a growing ruby boule in a flame fusion (Verneuil process) furnace.



Czochralski

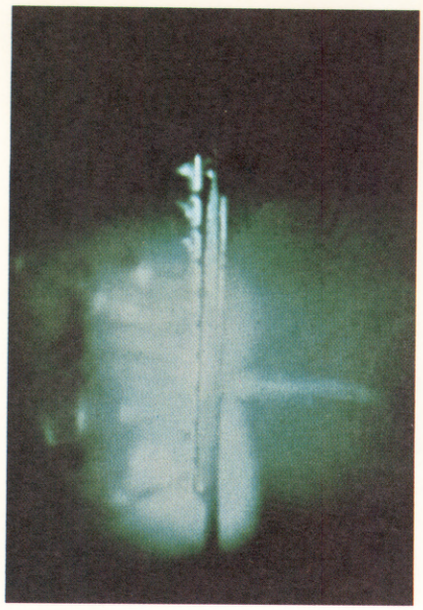
In an inert atmosphere, a rare-earth fluoride crystal is pulled from Czochralski melt. The crucible is radio-frequency heated.



Chemical Vapor-Deposition

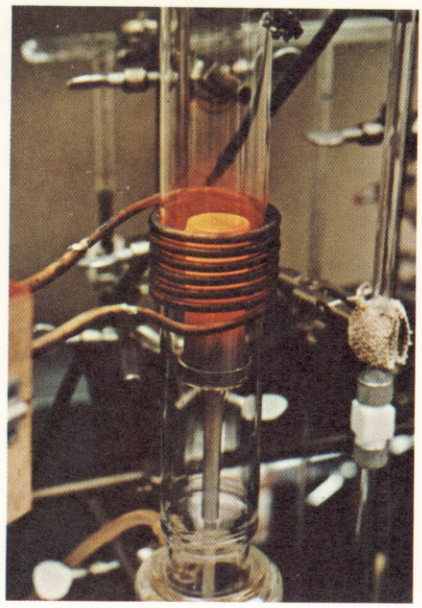
Chemical vapor-deposition is used for homoepitaxial growth of single-crystal magnesium oxide on a substrate of magnesium oxide.

Some Epitaxial Achievements



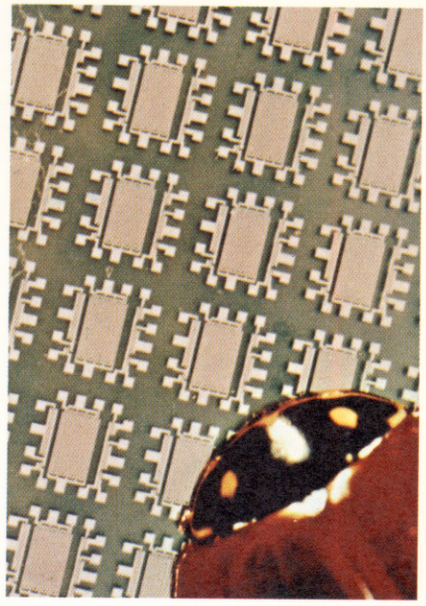
Laser Implications

Chemical vapor-deposition of single-crystal germanium on gallium arsenide, and also of single-crystal gallium phosphide on gallium arsenide, has been accomplished in the Research Center's epitaxial laboratory. Such heterojunctions are of interest because of their injection laser possibilities, as well as their photo-responsive properties. Viewed here through an infrared snooperscope, is an array of ten gallium arsenide injection lasers operating in liquid nitrogen. The array is fabricated from a single-crystal slice of gallium arsenide, grooved to allow independent operation of the ten devices.



Deposition Breakthrough

With chemical vapor-deposition, the Research Center has achieved the first reported instance of single-crystal silicon deposition upon an insulating surface (sapphire). The deposited silicon is greater than three-quarters of an inch in diameter, and is of the quality required for fabrication of diodes and transistors.



Thin-Film Transistors

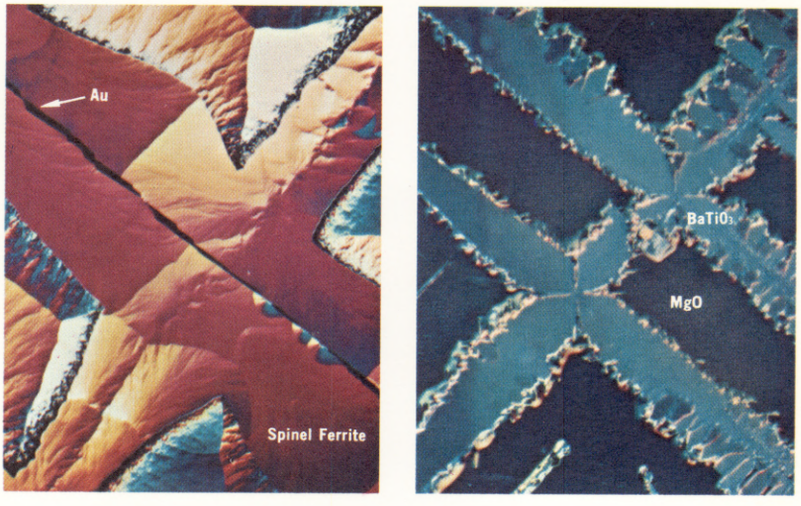
A ladybug examines an array of insulated-gate, field-effect transistors arranged in a grid on single-crystal silicon-on-sapphire. Each of these majority-carrier triodes is less than a micron thick, is completely compatible with passive thin-film elements, has excellent amplification ability, and is highly radiation-resistant.

Silicon-on-Sapphire Memories

Bit density of over 25,000 bits per square inch characterizes a fixed-program memory fabricated from a silicon-on-sapphire diode array. (See page 92 for description of the memory.)

Single-Crystal Magnetic Materials

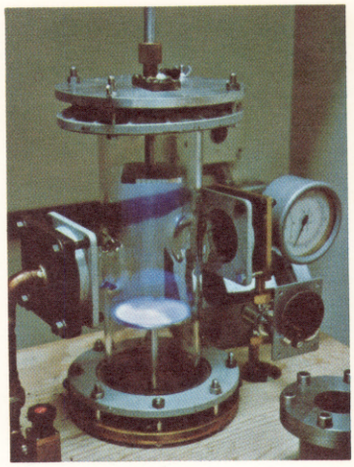
Autonetics' interest in computer application of magnetic effects goes back to 1960. Both metallic and oxide thin-film studies have been performed. It has been demonstrated that epitaxial single-crystal films of magnetic oxides that are particularly well suited for memory elements may be grown. Elementary bit capability of epitaxial ferrites and yttrium iron garnet on magnesium oxide has been demonstrated.



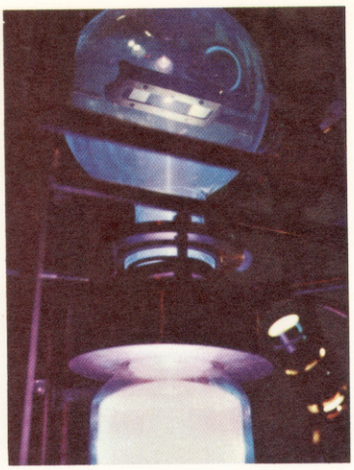
FERROELECTRIC (LEFT) AND FERROMAGNETIC (RIGHT) EPITAXY ON MAGNESIUM OXIDE

Thin-Film Deposition

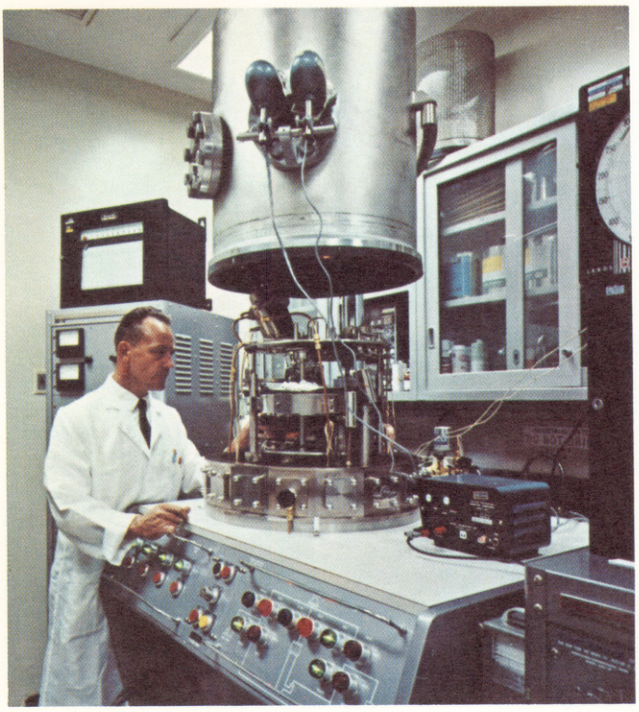
Autonetics' laboratories have for several years employed both plasma techniques (glow discharge) and electron-beam techniques (both plasma and filament cathodes) to achieve organic and inorganic thin films which are pinhole-free, continuous, controllable in thickness, and either insulating or semiconducting. The films may be extremely thin (around 50 angstroms), and are ideally suited for fabrication of high-value capacitors, as well as protective oxide coatings.



Glow-Discharge Method

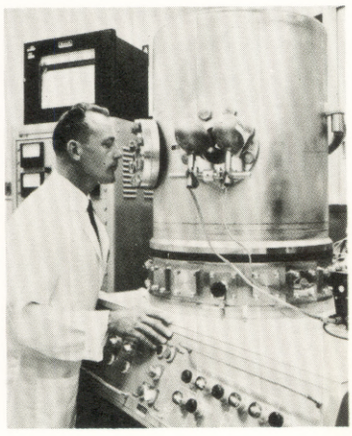


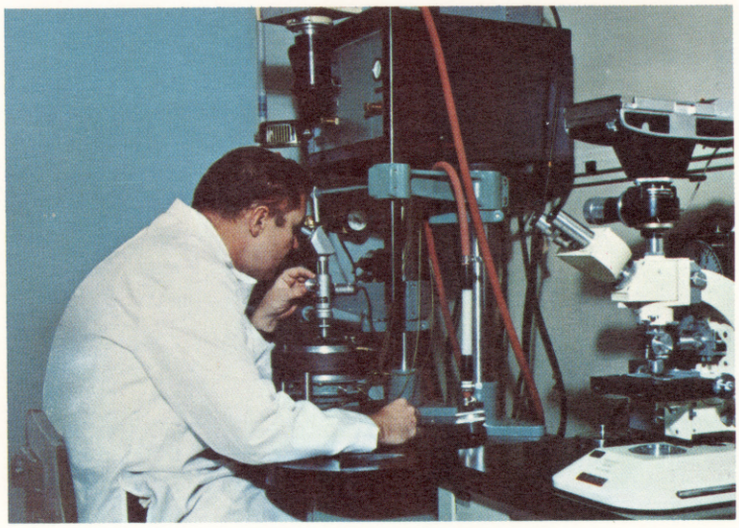
Electron-Beam Method



Thin Films as Optical Interconnections

Complex equipment is used to investigate application of thin-film dielectric structures as waveguides to transmit optical signals between light-emitting and light-detecting devices. (Such high-speed coupling is of particular interest for digital computer circuitry.) The equipment includes a vacuum system, complete with microcircuit jig; an electron-beam gun; an electrobalance; a thin-film monitor; and an optical pyrometer.



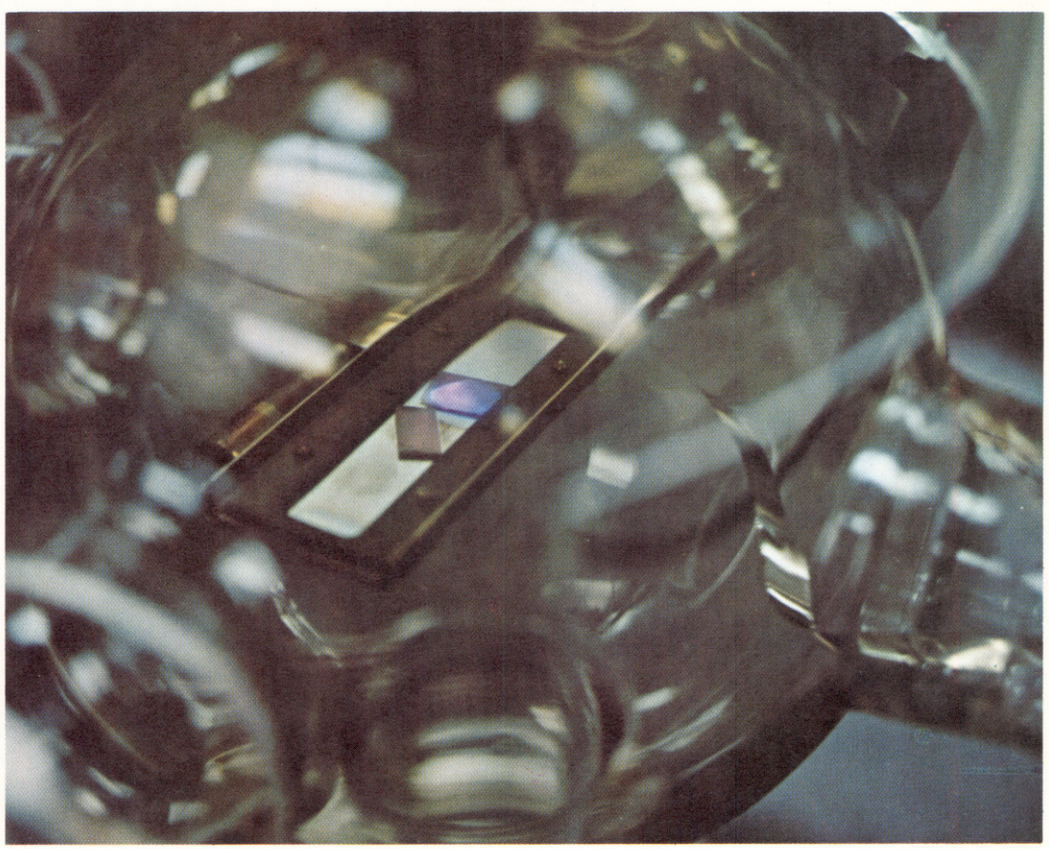


Microphotolithography

With this optical mask alinement equipment, the image of an entire pattern can be alined, projected, and printed on a photosensitized material with ultra-high precision (± 1 micron), to help achieve such devices as the planar annular varactor.

Planar Annular Varactors

Skill in microphotolithography makes this new Autonetics achievement possible. Extremely small dimensions of the varactor greatly reduce circuit losses by taking actual advantage of the skin-effect phenomenon. The varactor structure is equally applicable to varactors, tunnel diodes, and plasma diodes. (The varactor is the tiny black ring in the center of the gold disk in above photograph of the head of the eagle on a U.S. 25-cent piece. Additional idea of varactor size is gained by observing the varactor in the center of the gold disk, right, inside the loop of the figure "9" in the date on a U.S. copper penny.) Parametric amplifiers and pump harmonic generators with superior sensitivity and bandwidth are realizable with the planar annular varactor. Cutoff and resonant frequencies are raised by an order-of-magnitude over previous device capabilities.

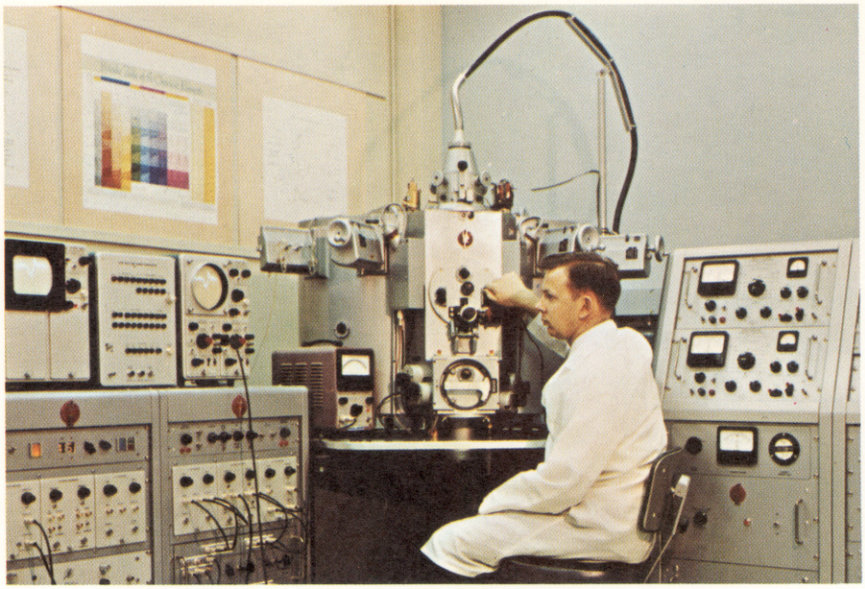


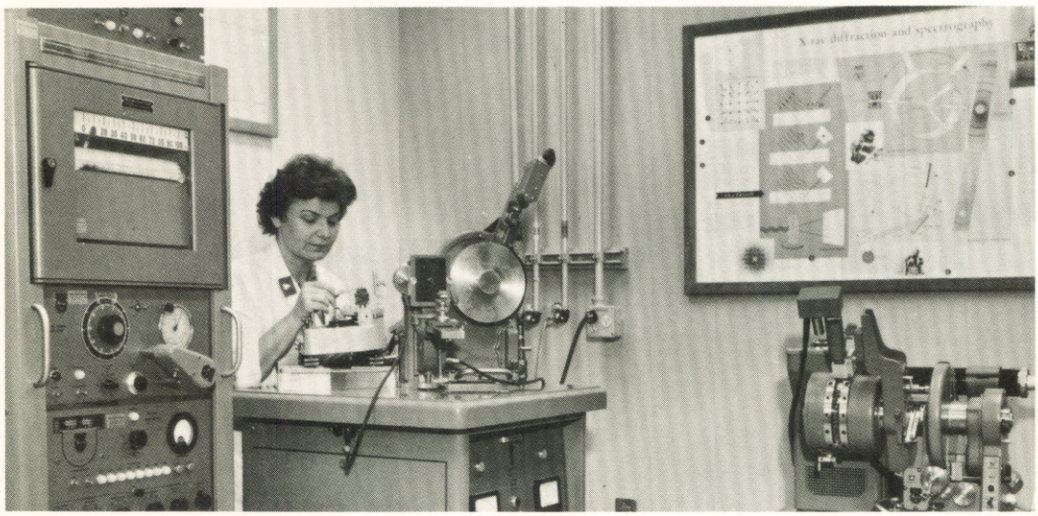
Electroluminescent Diodes

The novel characteristic of cadmium telluride for high-efficiency conversion of electricity to light is being studied as a means of information transfer in microcircuits. Other possible applications are for high-speed transistors and as laser pump sources.

Electron Microprobe Reliability Studies

Causes of failure in microelectronic components are investigated by means of electron microprobe testing. Unwanted effects in semiconductor elements are correlated with fabrication parameters, so that the effects can be eliminated. The nondestructive analysis helps determine surface, bulk, and device characteristics; foreign element and material defects; and dynamic and static junction performance parameters. Many of the common defects encountered in surface and subsurface regions of integrated circuits quickly show up by photograph with this method. Among the wide variety of investigations completed with the electron microprobe are analyses of laser materials, braze joints, welds, diffusion profiles, and oxide formations, as well as semiconductor materials and devices.



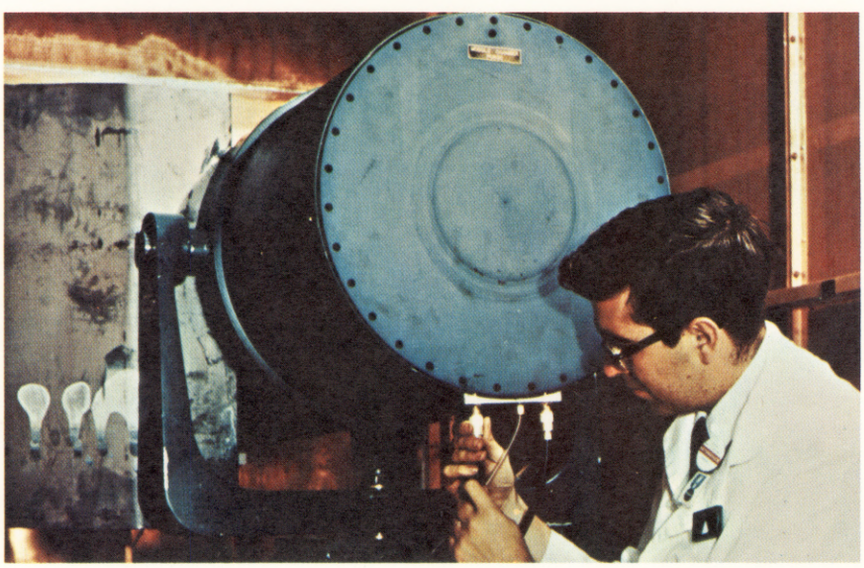


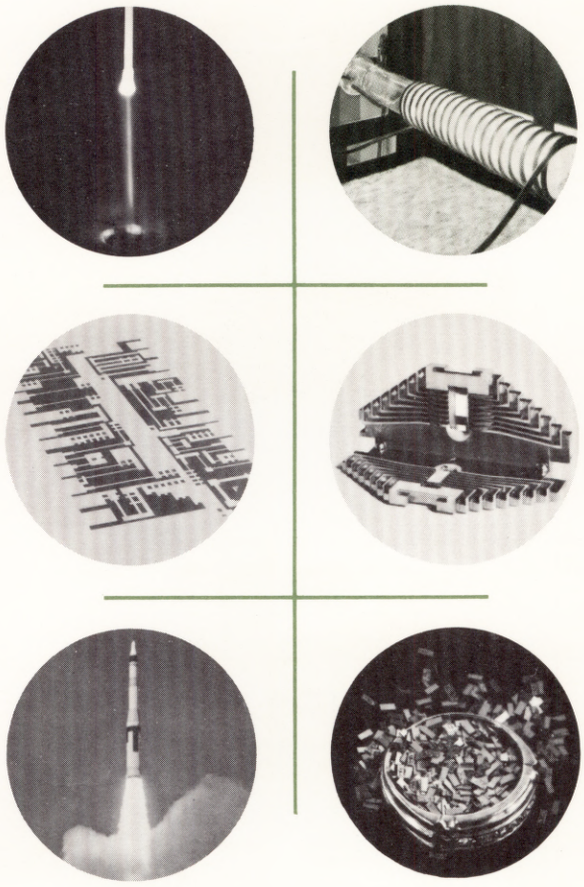
X-Ray Laboratory

This laboratory conducts all the varied X-ray analyses for the diversified programs within the Research Center. The vacuum X-ray spectrograph provides rapid and accurate analyses of all elements in the periodic table down to magnesium (atomic number 12). An additional capacity is the determination of crystal orientation to within one degree.

Radiation-Resistant Microelectronics

Both in research efforts and in practical application, Autonetics is concerned with the resistance of microelectronics to effects of nuclear radiation. The major direct application is for the Minuteman Program, and consists of the development of a guidance system for Minuteman II using microelectronic semiconductor integrated circuits, hardened against radiation. Research is carried out under a Company-sponsored program, and utilizes on-site 600,000-electron volt and 2,000,000-electron volt facilities to study transient radiation effects on microelectronics, and the mechanisms and parameters involved in these effects.





Developer...

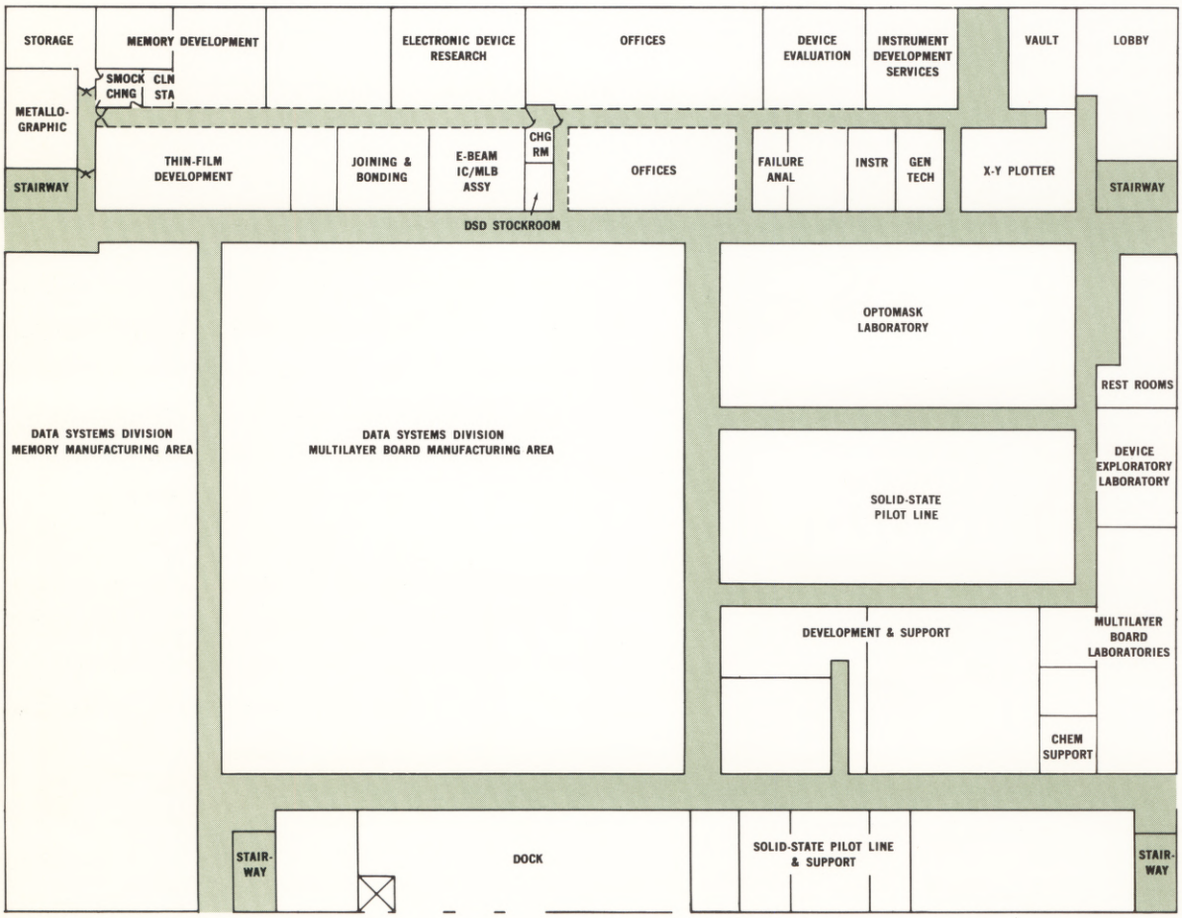
Research findings are translated into usable processes and producible materials and devices by Autonetics' Central Microelectronics Laboratory (CML), Materials and Processes (M&P) Laboratories, or the product divisions, as appropriate. In general, developments of a product division are oriented specifically toward the requirements of that division's systems. CML or M&P Laboratories developments are more universally applicable, or require facilities beyond product division capabilities.

Central Microelectronics Laboratory

CML occupies an entire 66,000-sq ft building. Created to provide Autonetics with a concentrated, coordinated facility to exploit all aspects of microelectronics, CML consists of a "host" Microelectronics Laboratory, and a grouping of "satellite" product division laboratories for conducting the specialized development required by products, without duplication of equipment and effort.

CML contains a solid-state device pilot-line, complete facilities for thin-film microelectronics development, facilities for micromemory experimentation and pilot production, and appropriate engineering evaluation and test laboratories. It is fully equipped for micro-packaging of electronic systems, having both development and small-manufacturing capability for multilayer boards, and assembly areas for prototype or breadboard system development.

Outstanding among CML capabilities are those afforded by: a computer-driven, high-precision X-Y plotter for automatic design and layout of complex multilayer boards, and of integrated microcircuit functions for solid-state or thin-film production; electron-beam machining equipment, capable of extreme precision and control in fabrication of microcircuits; and a photographic mask-making facility for producing the masks basic to the major portion of microelectronics activities.



CML's Host Laboratory

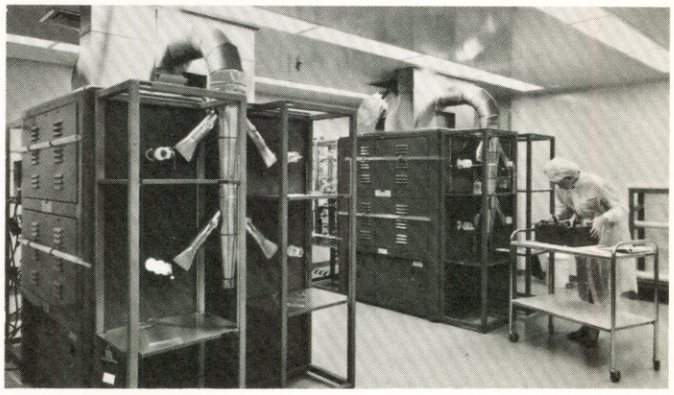
CML's host Microelectronics Laboratory is staffed by technical personnel with highly specialized training and experience in microelectronics. It is housed in a modern 22,500-sq ft facility, especially designed for solid-state activities.

A "white room" for semiconductor processing contains 13,875 sq ft of floor space, and employs the latest concepts of working space, lighting, control of airborne contaminants, air interlocks and pass-through boxes, individual rooms separated according to function, and diffusion areas completely isolated to prevent interaction with preceding or subsequent operations.

Laboratory equipment includes diffusion and oxidation furnaces; epitaxial reactors; complete photomasking, metallization, and packaging equipment; and an infrared spectrophotometer.

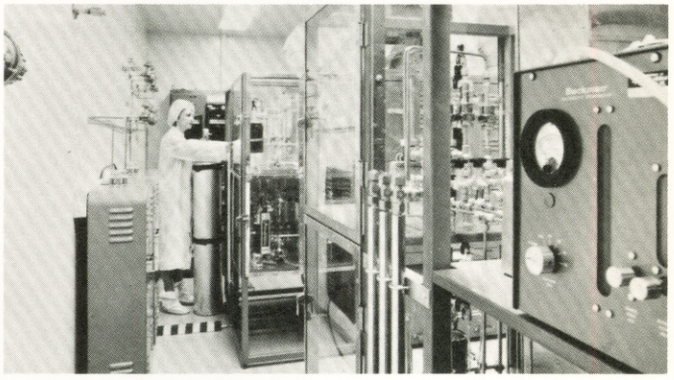
Solid-State Circuits

CML's Solid-State Devices Laboratory has complete state-of-the-art capability in semiconductor-integrated-circuits processing technology. Single-layer and multilayer silicon films (both n and p types) can be epitaxially grown over the resistivity range from 0.01 to 5.0 ohm-centimeters. Solid, liquid, and/or gaseous diffusion systems for boron, phosphorus, arsenic, gold, and other dopants permit n- and p-type diffusions over wide ranges of impurity concentration (approximately 10^{18} to 10^{21} atoms per cubic centimeter). Additional technological capabilities include photomask fabrication, microlithography, metallization, etc.



Diffusion Temperature Check

Temperature of tube diffusion zone is spot-checked before loading with wafers.



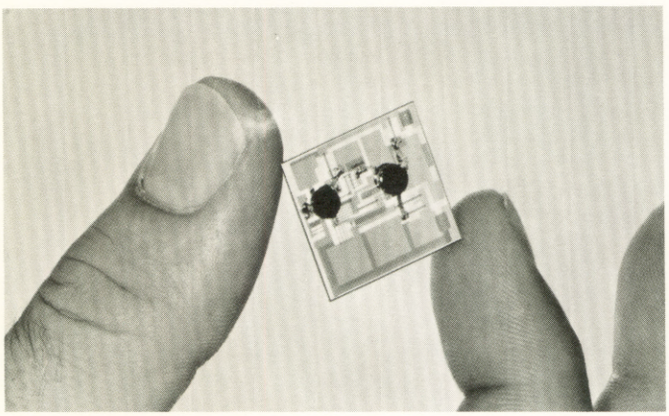
Diffusion Flow-Rate Regulation

Flow rate of carrier gas and dopant is regulated before processing run.

Epitaxial Deposition Temperature Check

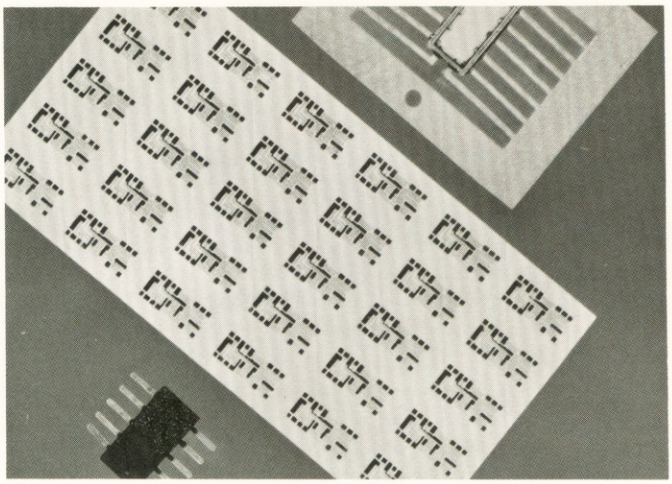
Wafer temperature is checked by means of an optical pyrometer.

Thick- and Thin-Film Circuitry



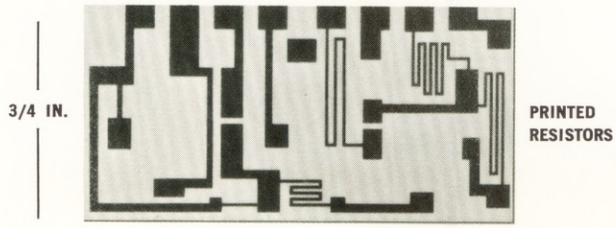
Thin-Film Circuits

Thin-film circuits have been developed by Autonetics' Electro Sensor Systems Division for operation over the frequency range of dc to 60 megacycles. Both analog and digital circuits have been developed for the R45 and R47 radars.



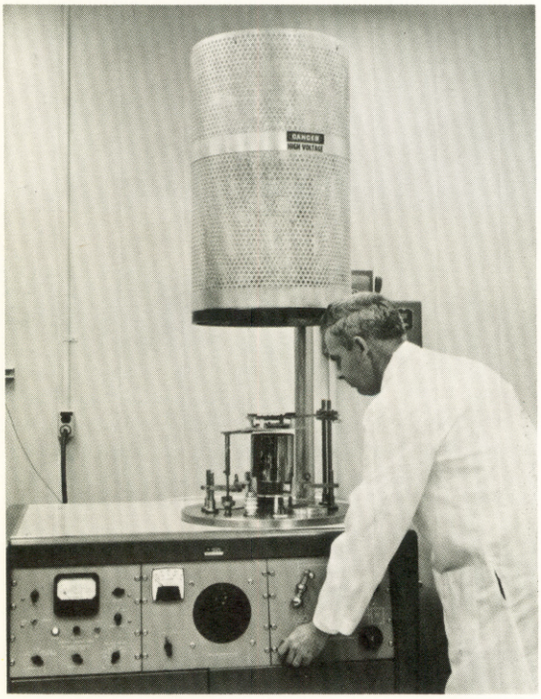
Thin-Film Photo-Etch Process

Thin-film hybrid resistor-conductor circuits are fabricated by a unique photo-etch process developed by Autonetics' Materials and Processes Laboratories. This method has proven to be much more reliable and economical than evaporation of thin-film circuit geometries through precision masks. With the new process, resistor and conductor films are consecutively deposited in a single vacuum-evaporation operation; the circuit pattern is then produced by a series of etches.



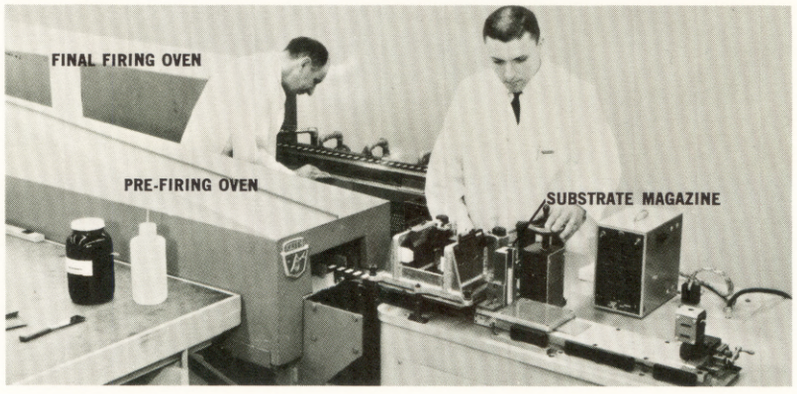
Thick-Film Resistors

Autonetics' Navigation Systems Division has developed an etching technique for producing ceramic printed circuit thick-film resistor line widths as low as 0.005 inch—as compared to a 0.020-inch minimum width obtainable with surface screen printing. The thinner lines permit higher-value resistors in less area. Individual resistors—ranging in value from 10 ohms to 1.5 megohms—can be produced from one resistance composition on a single substrate. The labyrinthine patterns of lines in upper photograph are the resistors; the maze-like patterns allow greater lengths of resistive material (higher-value resistors) in a small area.



Thin-Film Components

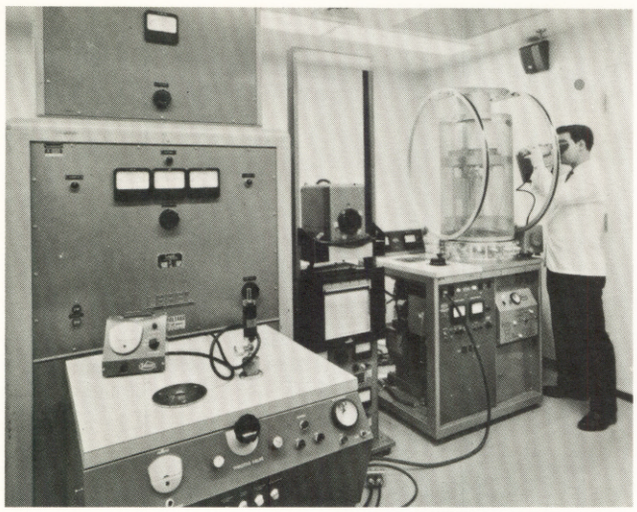
CML's Thin-Film Components Laboratory is now developing techniques for fabricating thin-film resistors compatible with integrated-circuit structures. It is also investigating techniques, materials, and processes to form thin-film resistors, capacitors, and interconnections on ceramic substrates containing several IC units, and, thus, to provide an advanced interconnected-packaging technique. The vacuum chamber shown here is used to deposit the metal or oxide films.



Resistor Experimental Printing Equipment

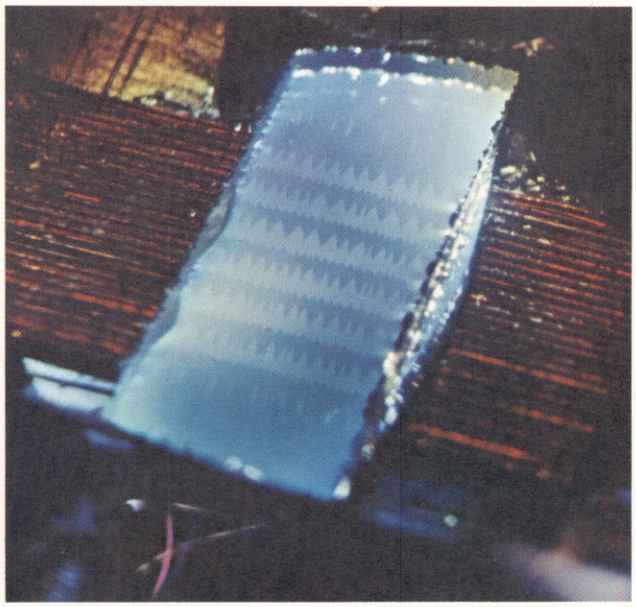
Magnetic Thin Films

CML's work in this area is directed toward research and development of magnetic thin films for memory planes. The laboratory is completely equipped to produce and evaluate the films.



Film Deposition

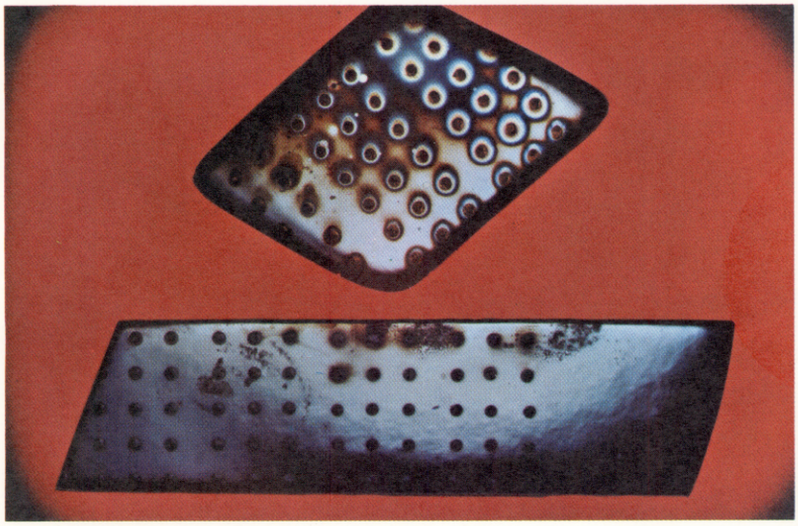
Film deposition is done in precisely controlled high-vacuum evaporators.



Film Analysis and Evaluation

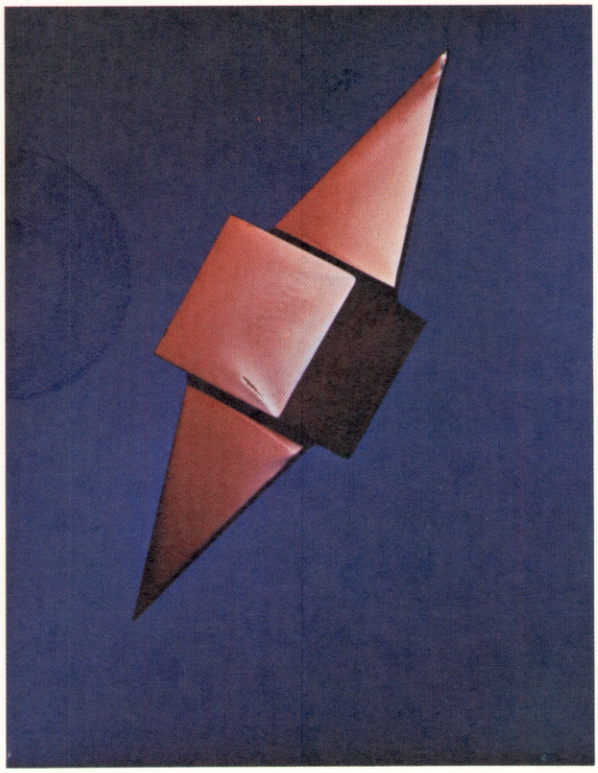
Techniques for analysis and evaluation of magnetic thin films include X ray, X-ray fluorescence, hysteresis, and (see photograph) domain orientation by the Kerr magneto-optic effect.

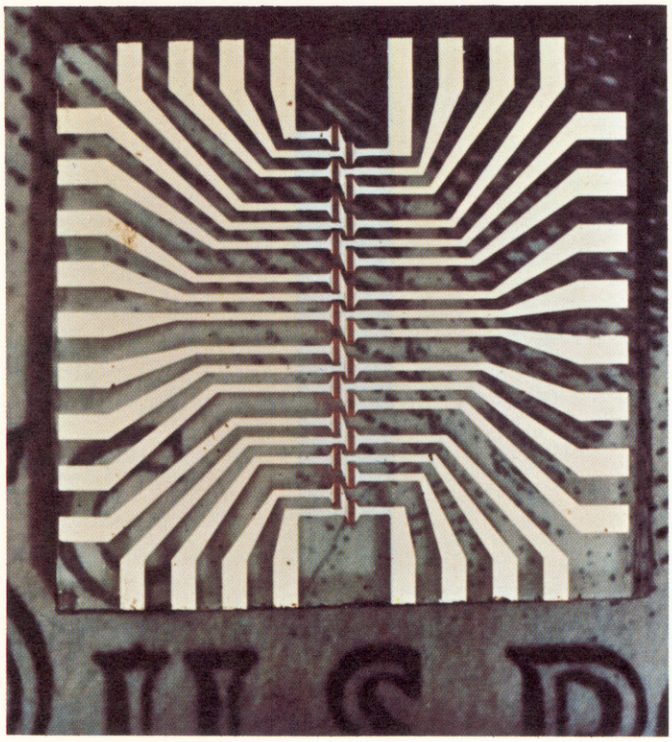
Special Devices



Solid-State Strain Sensors

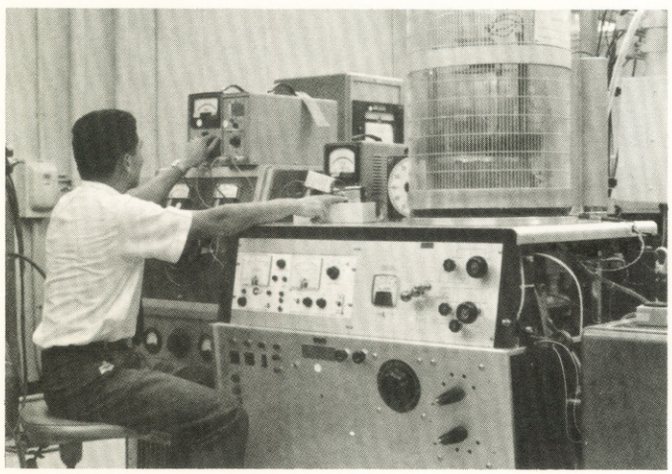
Strain sensors being developed by Autonetics' Navigation Systems Division utilize the properties of semiconductors to detect strain in materials. The small-size, low-power, long-life devices offer extremely high sensitivity, plus direct digital output. Potential applications include microminiature strain gauges, linear accelerometers, angular accelerometers, etc. At left is a magnified view of two Autonetics-fabricated arrays of tunnel diodes used as sensing elements in a microminiature accelerometer; at right is the structure for mounting and structurally supporting the diodes.





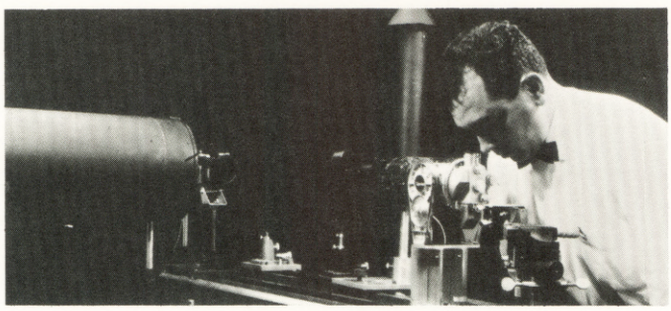
Photoconductive Cells

The Navigation Systems Division has developed a microminiature photodetector for use in star-trackers. The high gain of the device (as much as one million times) permits tracking of objects as dim as a third-magnitude star. The devices are now being used in the N16S navigation systems' star-trackers. Other applications—for example, star tracking without mechanical scanning, and tracking of objects other than stars, such as landmarks, the moon, and planets—are being investigated.



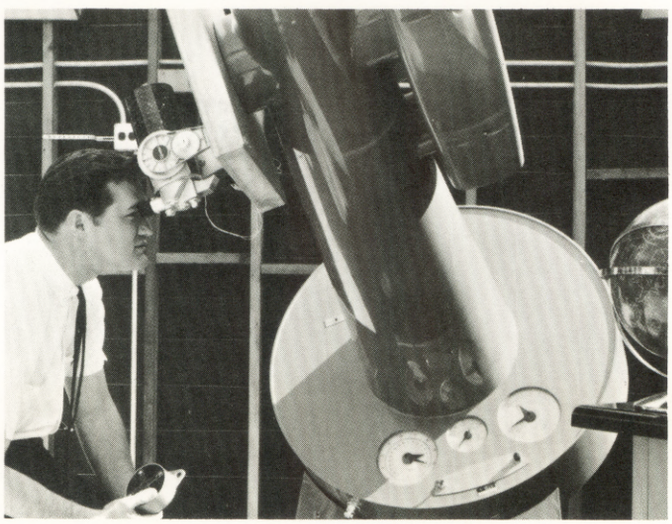
Vacuum Evaporation Chamber

In this chamber, cadmium sulfide and impurity dopants are simultaneously evaporated onto glass substrate during fabrication of experimental photodetectors. The evaporation rate and substrate temperature are closely monitored to control stoichiometry and impurity concentration.



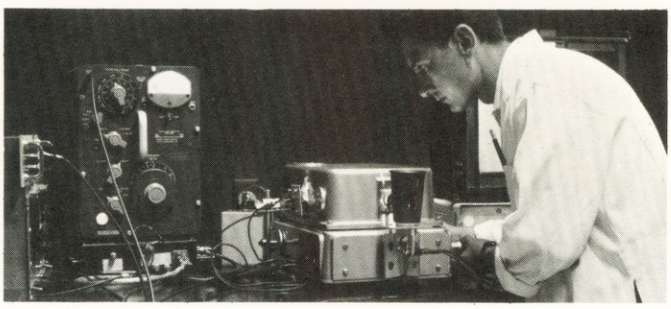
Star and Sky Simulator

This simulator presents to a telescope a variable-magnitude star, superimposed on a blue-sky background of variable brightness. Sensitivity of microelectronic photodetectors, for daylight tracking applications, can be tested here under controllable conditions.



Telescope and Star Mount

Photocell performance is evaluated in actual daylight star detection on a mount capable of supporting a complete gimballed tracker system, and of maintaining its orientation in celestial coordinates. Electronic equipment processes and records the star-presence signal for cell-sensitivity testing.

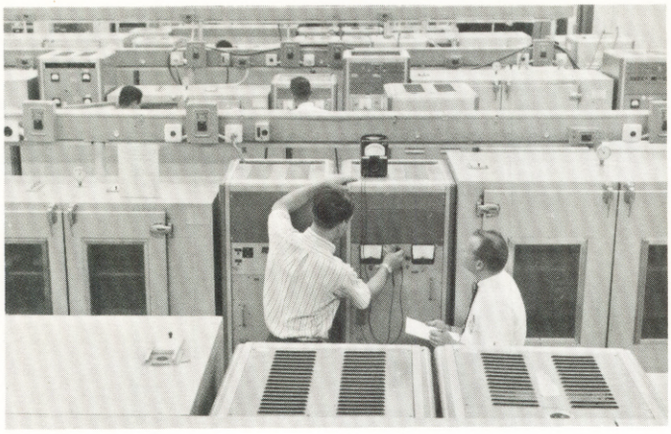


Spectral Response Measurement

A monochrometer and associated equipment determine the relative sensitivities of photocells to different star classes. Spectral response of the photocells is controlled by varying the type and concentration of impurities in the crystalline materials of which the cells are made.

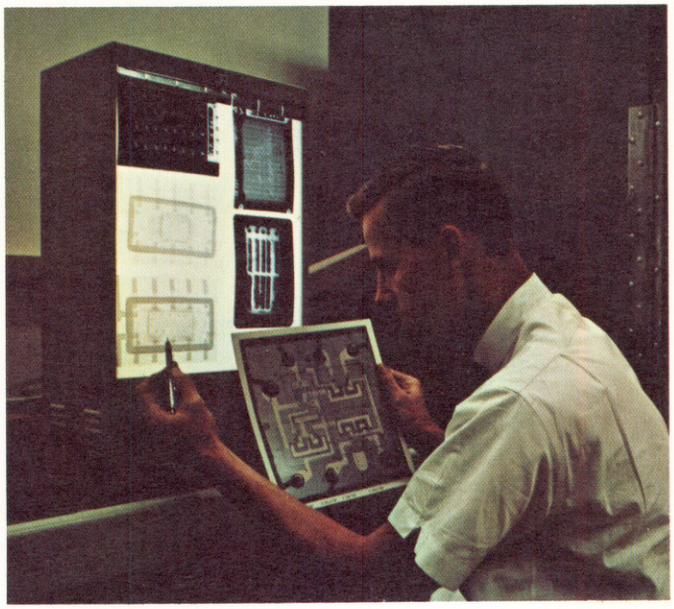
Analysis, Test and Evaluation

The Microelectronics Engineering Section of Autonetics' Advanced Electronics Department supports microelectronics activities with complete test and analysis facilities. Investigations range from performance tests at high temperature, to material structural analysis by X-ray beam and microprobe.



Accelerated Life Testing and Step-Stress Evaluation

Rows of ovens provide accelerated life testing and step-stress evaluation. Stresses are both electrical and thermal for electronic devices, and stress effects are indicated continuously or intermittently, as required.

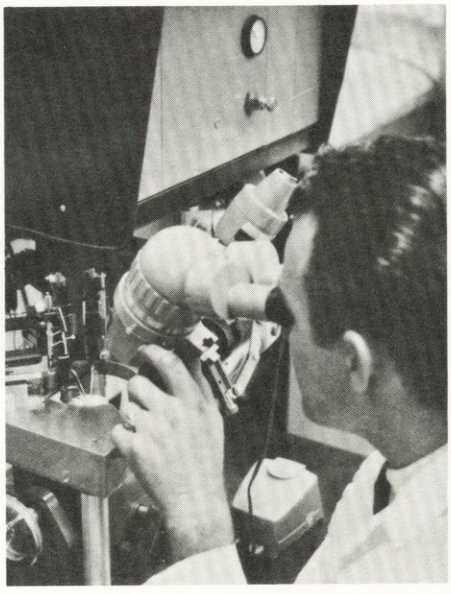


Microradiography

Radiographs of microelectronic parts are inspected on a viewer. The negatives on the left show semiconductor integrated circuits. The enlargements indicate a good device (center), and a defective device with voids in the alloy peripheral seal (lower). The negatives at right are of multilayer boards and are being examined for alinement of board layers.

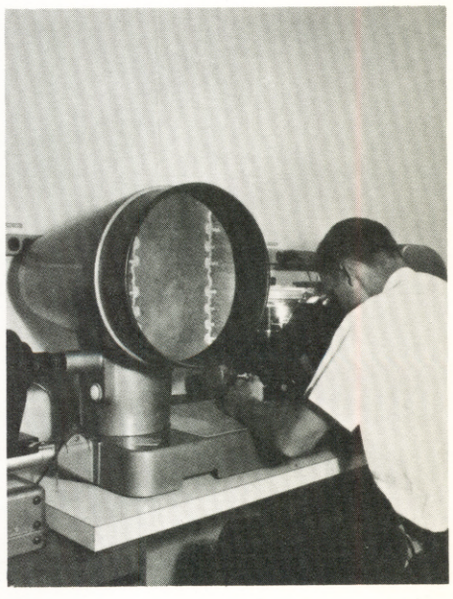
Component Life Testing

This life test chamber is one of three—each of which contains 24 trays, with power supplies for power storage of discrete parts. Each tray can mount as many as 1000 parts; heat exchangers are capable of maintaining 77 ± 2 degrees Fahrenheit over the parts, up to a maximum heat load of 24 kilowatts per hour.



Precision Probe

Examination of device details invisible to the naked eye requires specialized equipment such as the precision microprobe which measures characteristics of microscopic areas of discrete electronic devices, and gauges the performance of specific junctions or elements of a semiconductor integrated circuit.

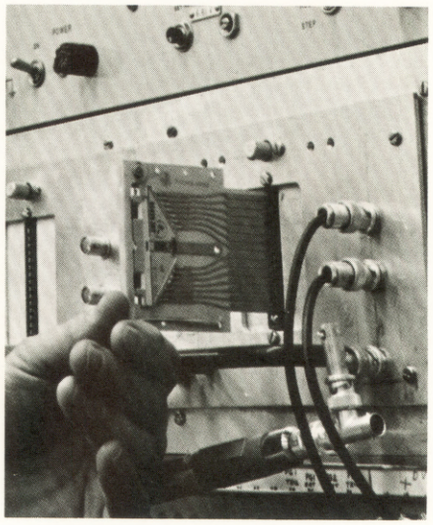


Evaluation at High Magnification

A materials engineer examines a cross section of a through-hole connection in a multilayer board. The Leitz metallograph with which he performs the inspection is equipped with flat field objectives and a xenon light source, and can be employed to study microelectronic devices at magnifications to 1600X.

Automated Testing of Integrated Circuits

All dynamic and static characteristics of integrated circuits are measured by automated test equipment. Repeatable, precision measurement is made of as many as 100 different dynamic, static, or intermixed characteristics. Printed-tape readout permits on-the-spot examination of test results, and punched-card output provides data for subsequent computerized analysis and evaluation, and for permanent filing of valuable design data. Simultaneous visual displays of test number, parameter values (shown on a digital meter), and oscilloscope patterns keep the operator informed of test progress. With the automated equipment, test time is reduced over manual by a factor of 40.

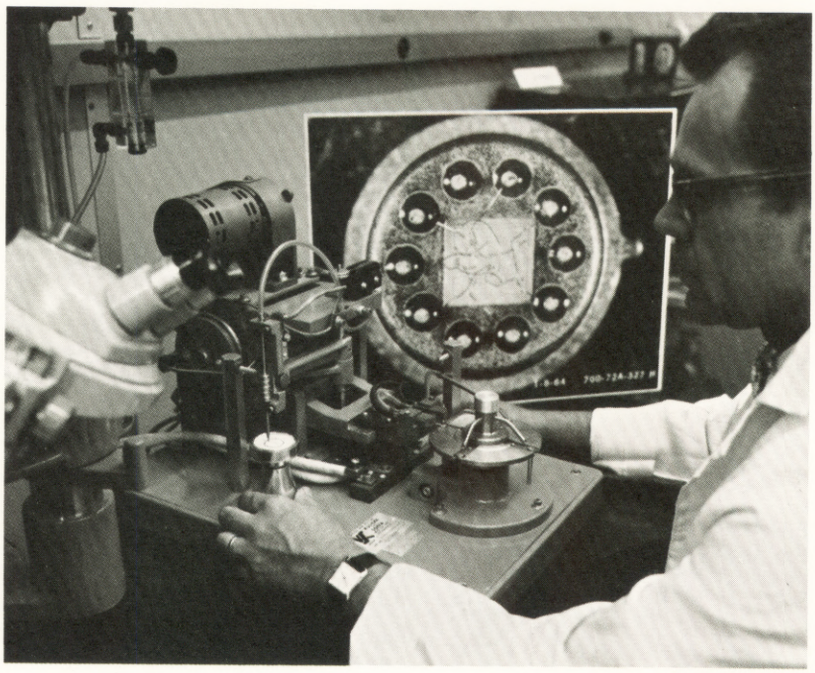


Handy "Clam-Shell" Mounting Fixture

The unique mounting fixture for the automated IC tester is also used to mount IC's for electrical and environmental stressing. A number of "clam-shells" can be inserted in a special container called a "stick," allowing simultaneous testing of many IC's.

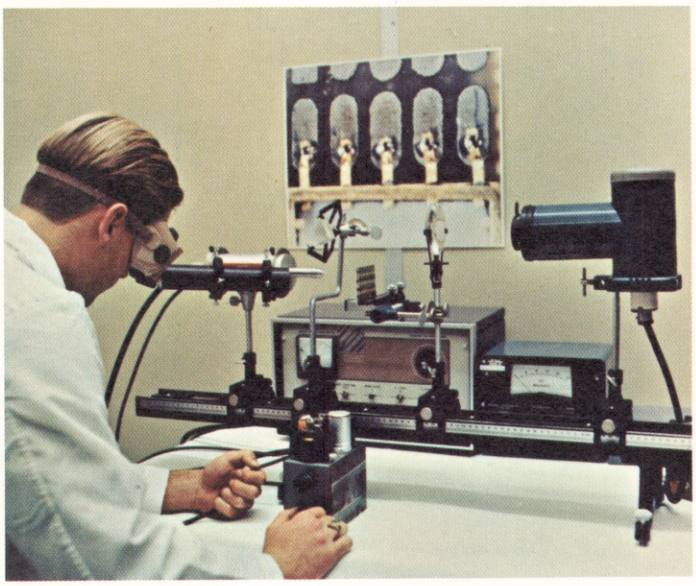
Joining

One of the ways in which the Materials and Processing Section of Advanced Electronics supports Autonetics' microelectronics activities is by development and evaluation of new methods for joining.



Die Bonding

At this automatic dice-bonding station, semiconductor device chips are picked up from a small loading platform and are eutectic-bonded to the resistance-heated, gold-plated header surface. The unit is capable of die bonding 2000 units in 8 hours.



Laser Welding

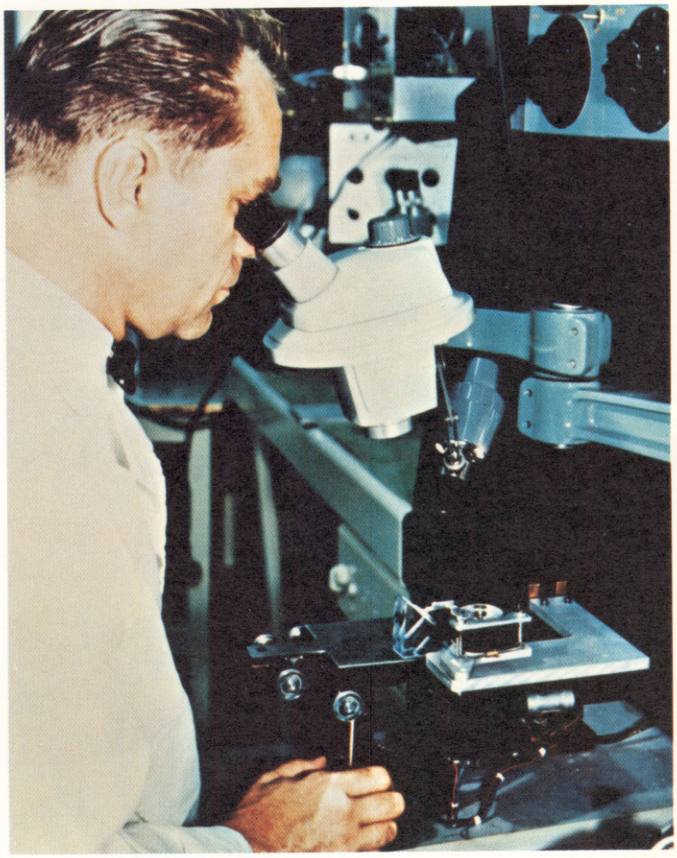
The feasibility of connecting integrated circuits to multilayer circuit boards has been demonstrated by the use of a 1-joule ruby laser. Present development has the objective of defining critical parameters for this advanced joining process.

Process Evaluation

A versatile machine for assembly of semiconductor or thin-film devices permits evaluation and development of new microelectronics joining processes. Various attachments, mounted on the hexagonal turrets on each side of the operator, enable him to select different types of joining, such as resistance welding, thermocompression bonding, soldering, etc; both turrets are controllable to 20 millionths of an inch.

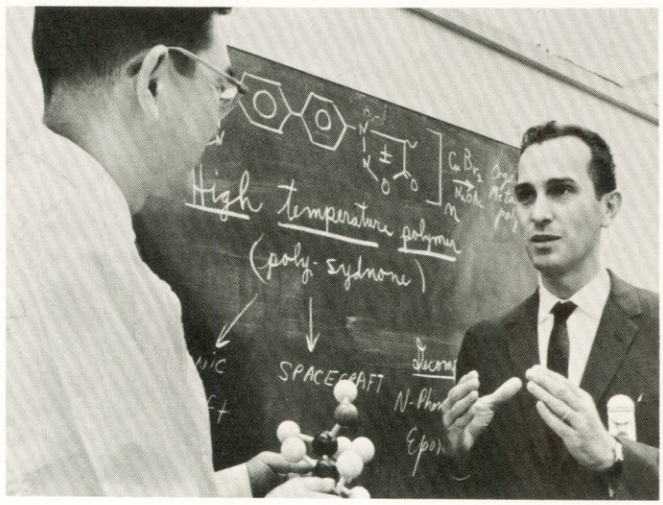
Bond Testing

A microtensile tester—designed and built by Autonetics' Materials and Processes Laboratories, since no commercial equipment was available with the required capability—tests strength of small-diameter wires or ribbons bonded to thin films or semiconductor integrated circuits. Test results help determine optimum joining techniques.



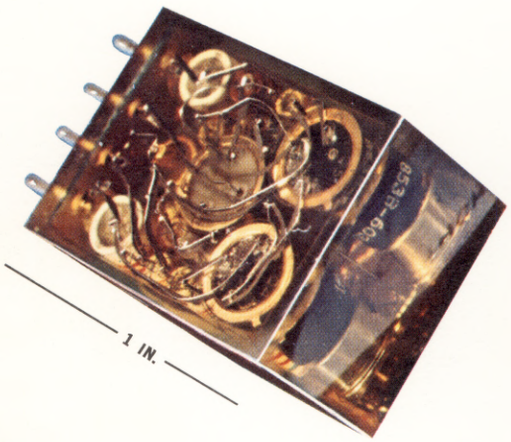
Materials

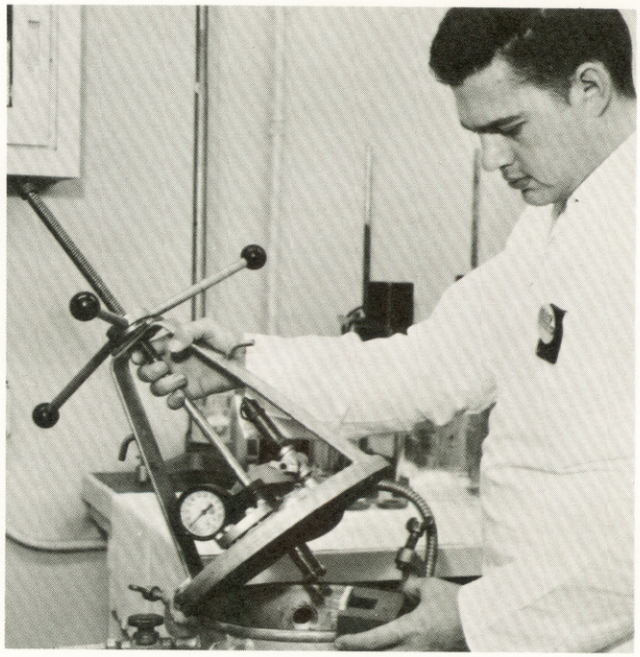
Another area of Materials and Processes Laboratories support to microelectronics is concerned with development and evaluation of materials and processes for encapsulation, embedment, and plating.



Polymer Synthesis

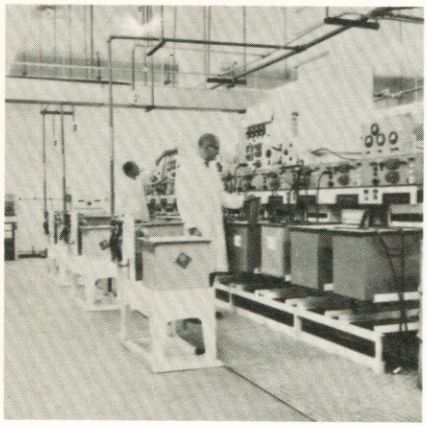
Autonetics develops new improved polymers when state-of-the-art materials do not meet stringent requirements. Organic and polymer chemists vary the molecular structure of resins to improve moisture impermeability, temperature resistance, and nuclear-radiation resistance.





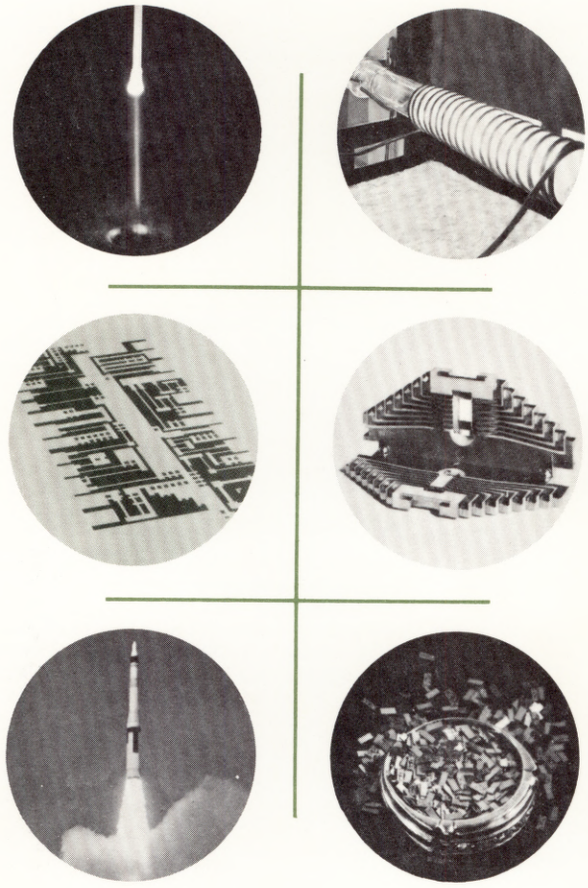
Plastic Coatings and Embedment

Considerable effort is exerted by Autonetics in selecting the optimum plastic for each application. Plastics range from thin coatings for circuit boards and microelectronic ceramic wafers, to embedment of welded modules and transformers.



Plating

A pilot line is maintained for plating-process development and evaluation. Power and utilities are supplied to each operator station from a remotely located instrument console which also contains monitoring instruments. Complete facilities are maintained here for specialized cleaning and surface preparation, precision electrolytic and electroless metal deposition, anodizing, and other surface finishing.

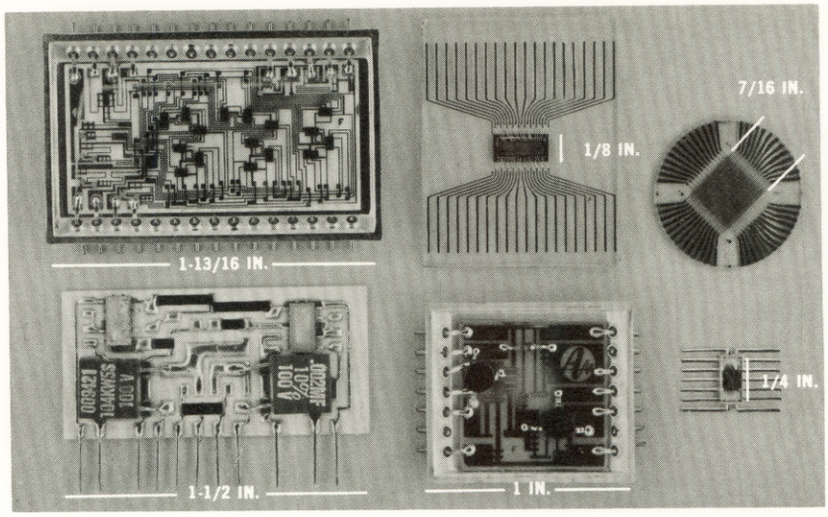


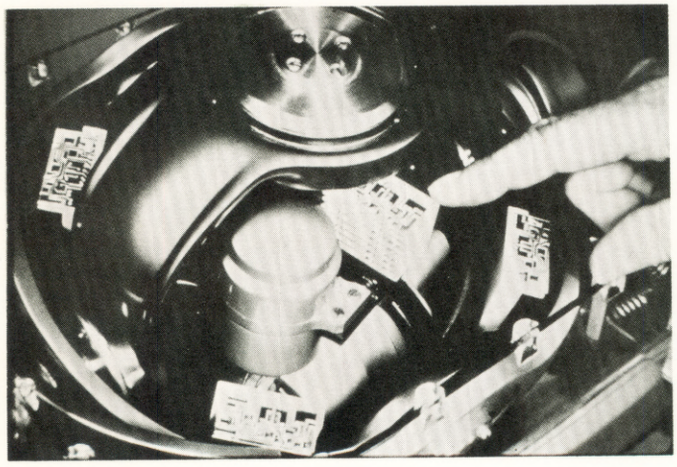
Designer...

General developments in materials and devices are specialized by Autonetics' design engineers to meet requirements of specific applications. Among the everyday tools of the designers in carrying out this task are such advanced techniques as standardized circuitry, master dice, computerized layout, and computer-assisted circuit analysis.

Which Type of Microelectronics?

The first design question to be answered is, of course, which type of microelectronics should be used in which functions of the system? Should the decision be for IC's, for CPC's, or for a combination of the two in the navigation portion of the system? Should the radar employ thin films or hybrid devices? What about MOS for the computer? What about subsystem interfaces, and what about procurability of the preferred types? Must a compromise be made between desired performance and available budget?



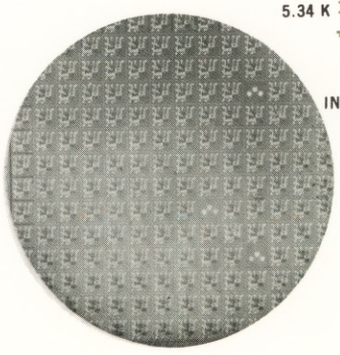


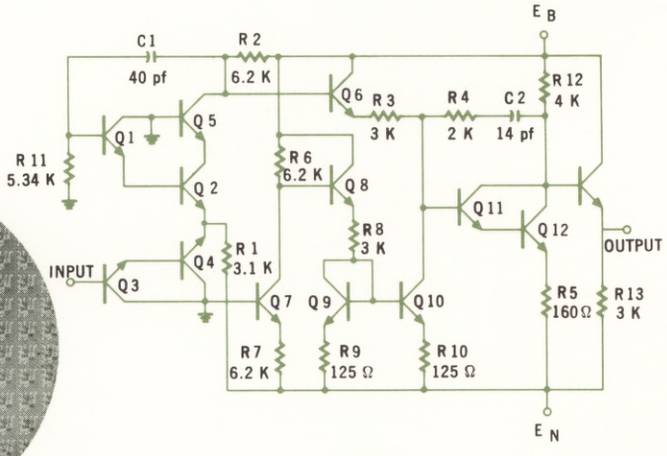
Total System Approach

Typical of Autonetics' total system approach is the design of the N16 inertial navigator family. Careful consideration has been given to the functional requirements of all elements in the total system—inertial elements, platform electronics, computers, power supplies—and their ability to work effectively together. A cost-cutting result of such analysis has been use of standard circuits throughout the N16.

Standard Integrated Circuits

Fifteen semiconductor IC's have been designed by Autonetics under USAF contract for a low-cost inertial navigation system. They are applicable to about 70 percent of the circuit requirements in typical electromechanical control systems.



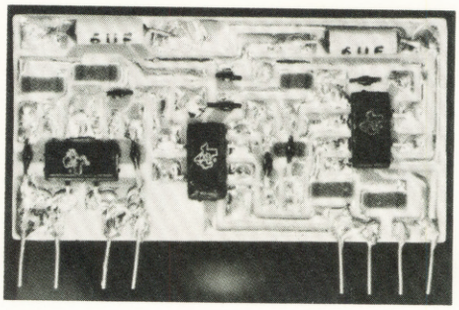


Standard Ceramic Printed Circuit / Integrated Circuit Alternates

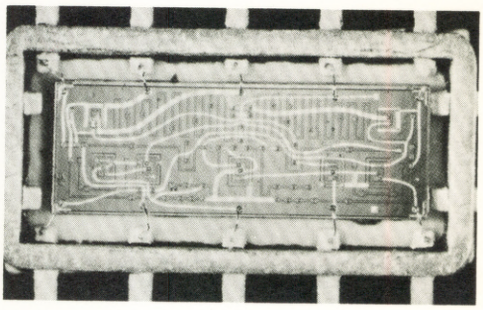
Four standard circuits are available in both ceramic-printed-circuit (CPC) and integrated-circuit (IC) form for linear applications. Functionally classified, the four are: general-purpose amplifier, demodulator-chopper, driver switch, and power switch. Versatility of these Autonetics-designed standards can be extended through adapting circuits. For example, connected to the proper adapter, a standard general-purpose amplifier can serve not only as a signal amplifier, but also as a flip-flop, multiplier, switch, or pulsewidth modulator. Development and production costs are significantly reduced by these techniques.

General-Purpose Amplifier

Four basic versions of this differential dc amplifier, with strong common-mode feedback, are made by changing resistor values.



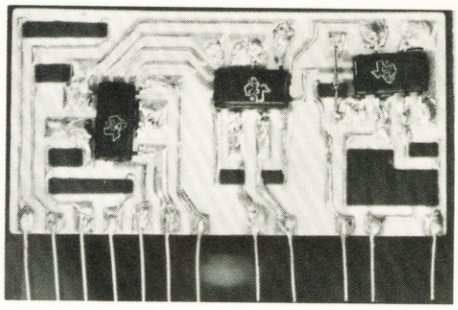
1-1/2 IN.



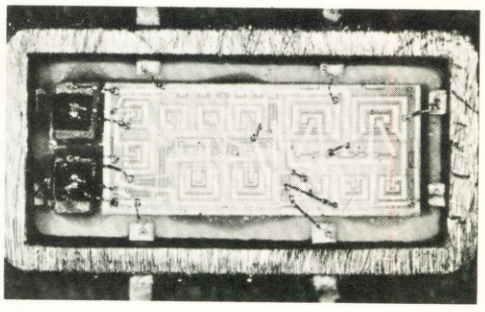
1/4 IN.

Demodulator-Chopper

This is a conventional Bright chopper circuit connected to the reference supply through a transformerless coupler circuit. (In IC version, note 3-chip construction and two p-n-p transistors, left.)



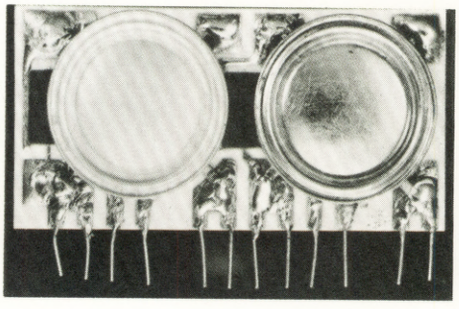
1-1/2 IN.



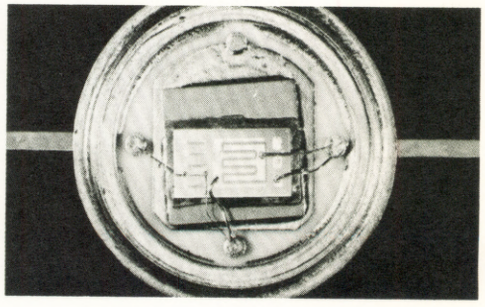
1/4 IN.

Power Switch

The power switch is a high-power, 2-ampere output, Darlington-connected pair of transistors, with an inductive-load protection diode built in. The CPC version of the power switch is actually a hybrid consisting of a pair of IC power switches mounted on a single ceramic wafer. In the IC version, shown at right, note "spare" transistors and diodes.



1-1/2 IN.

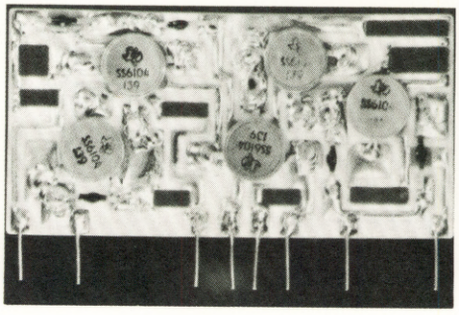


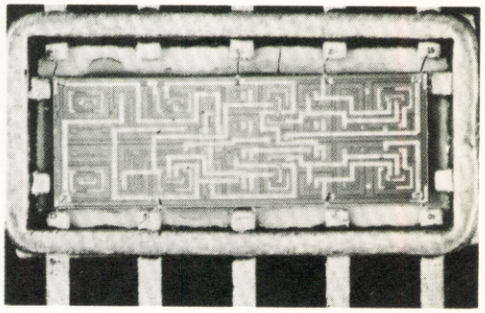
5/8 IN.

1/4 IN.

Driver Switch

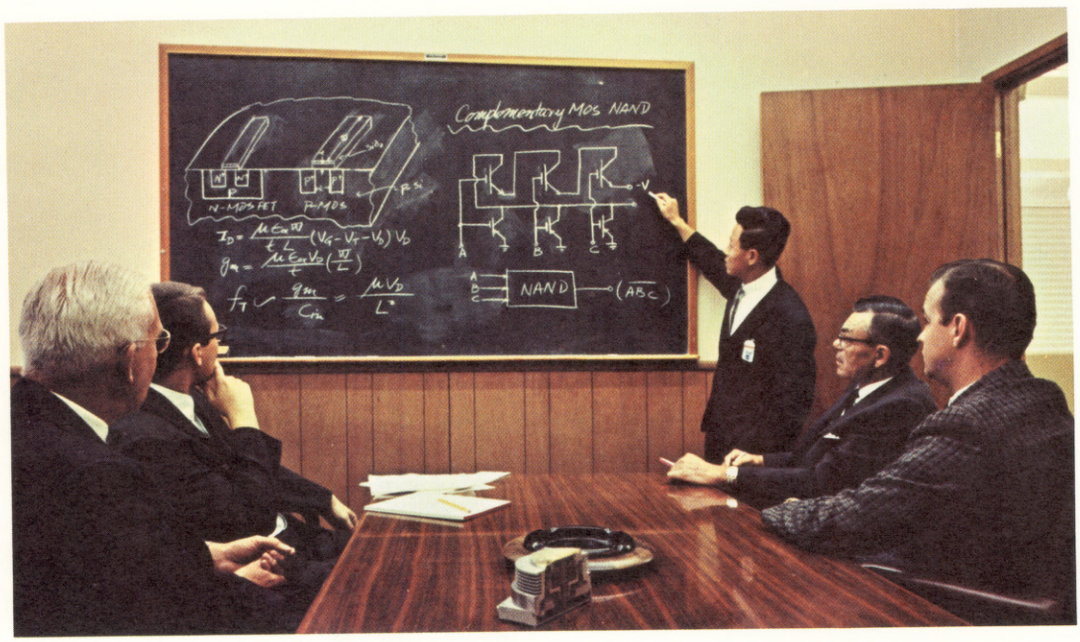
This standard circuit is employed primarily to drive the power switch.





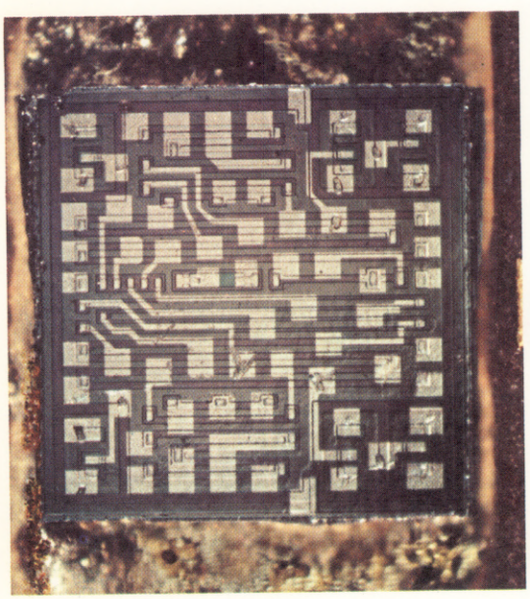
Integrated Circuit Design Approach

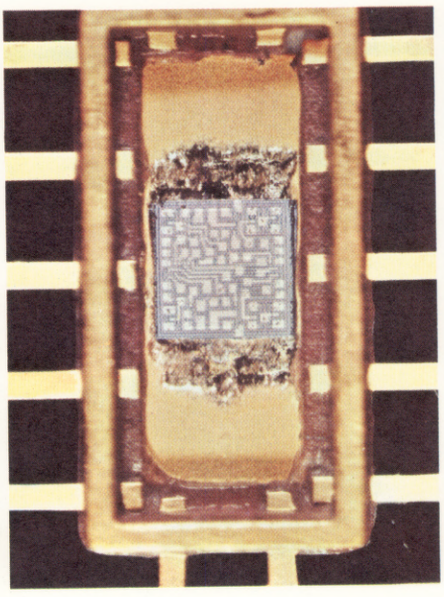
The Circuits Design Group in the Central Microelectronics Laboratory analyzes preliminary specifications from the product divisions, and recommends design approaches. The group also develops and fabricates new integrated circuits and extends the state-of-the-art in computer circuitry by investigating semiconductor networks and batch processing of semiconductor memories.

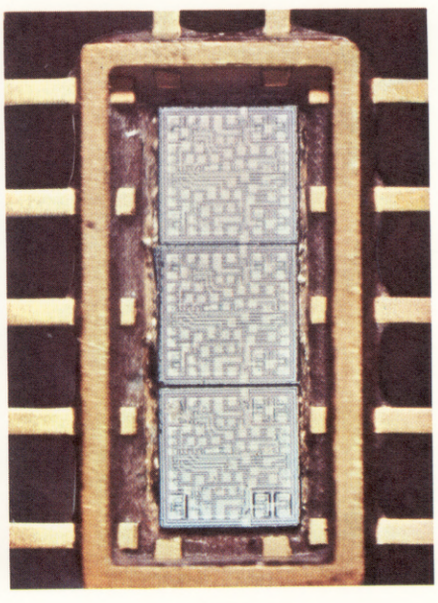


Master Dice Technique

Standard integrated circuits (left, below) are stocked in unwired dice form at Autonetics, and are breadboarded and functionally tested without the added cost of expensive intra-connect deposition masks and associated procurement delays. Circuit changes required by design revisions can be readily evaluated. Ultimately, the proven IC's can be procured from the supplier, who uses identical master dice to manufacture the "production models" (center and right, below).

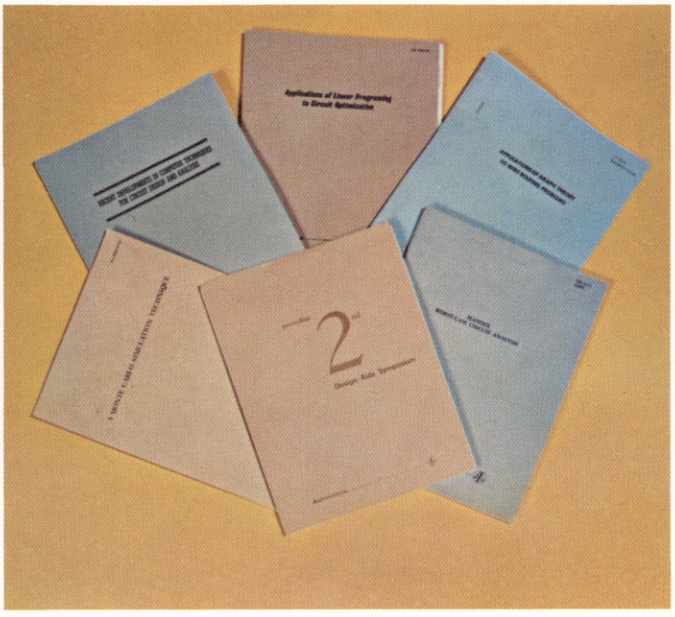






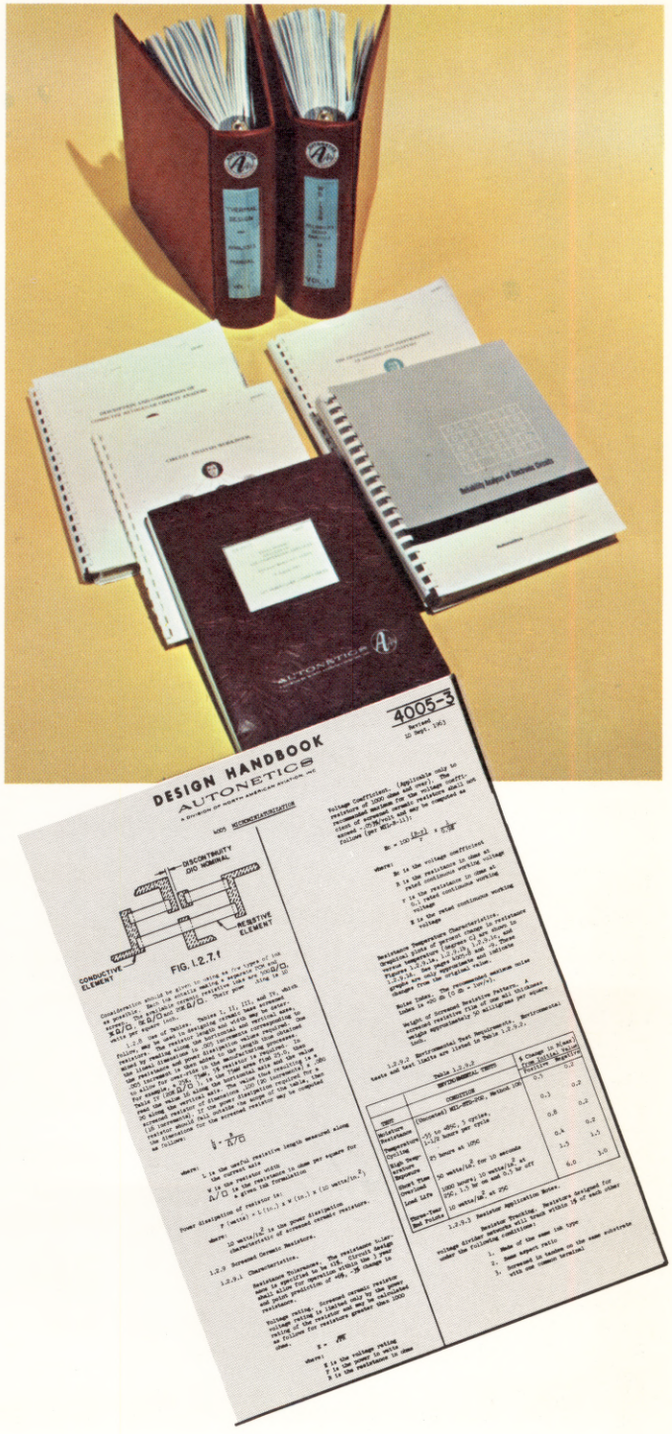
Computer-Assisted Circuit Analysis

Computer methods of circuit analysis are applied throughout Autonetics to determine optimum circuit parameters for such high-microelectronics-usage programs as Minuteman. In design of fifteen standard IC's for USAF, for example, both statistical and worst-case analysis were performed with a high-speed digital computer. Detailed statistical properties of the circuit characteristics were analyzed with computer programs developed by Autonetics.



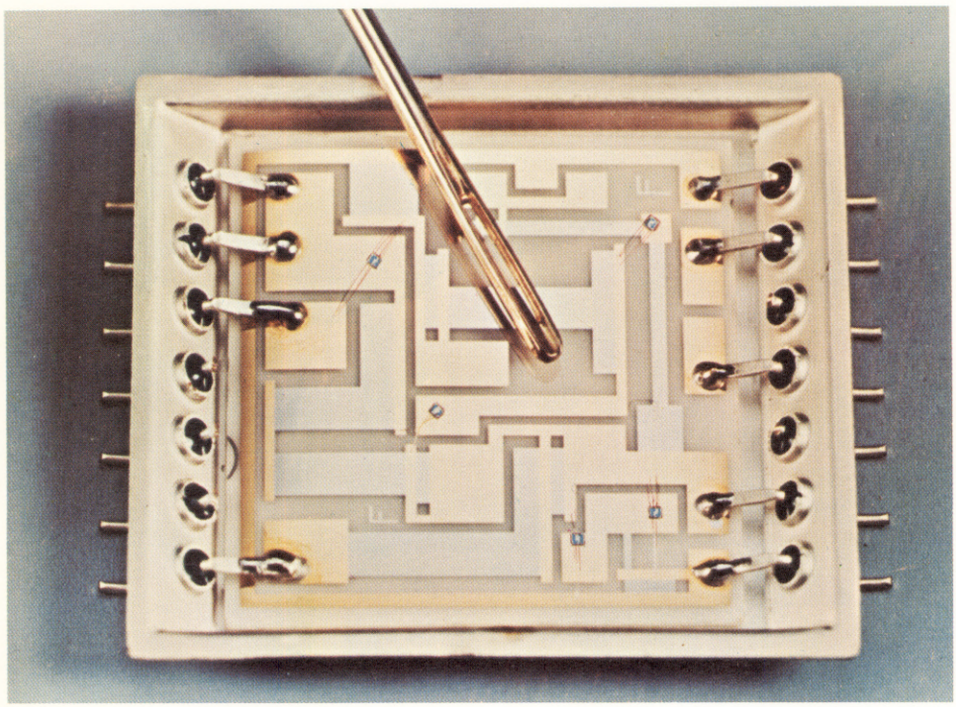
Reliability as a Design Parameter

In selecting each part or material for a new design, the engineer has available all the data derived from extensive reliability testing and failure analyses. The data (contained in Autonetics' **Reliability Handbook, Design Handbook, Standard Parts List,** and other documents) tell him how the items he is considering act under stress—both electrical and environmental—and help him select the best microelectronic performer for his application.



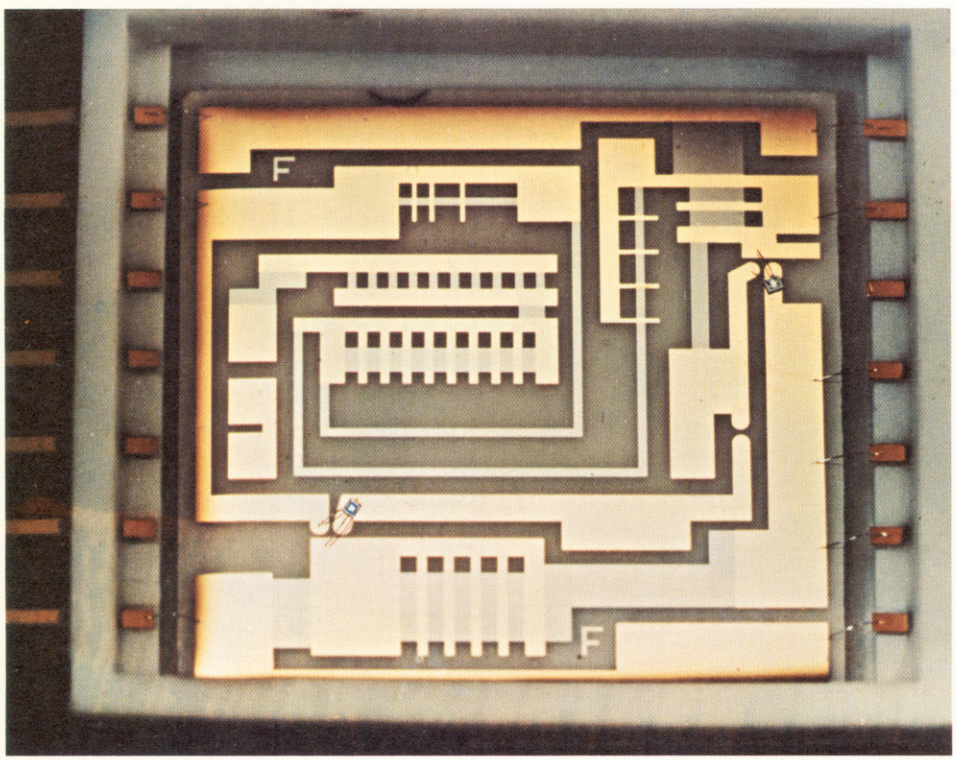
Thin-Film Design Challenges

Many factors enter into layout of a thin-film circuit—such as power dissipation, crossovers, trimming capability, grounding, size, and terminations. All of these factors are taken into consideration by Autonetics' designers in planning circuitry for such systems as the R45 and R47 radars.



Renegade Capacitors

Autonetics' thin-film circuit designers are like jigsaw puzzlers. Complete avoidance of crossovers is a real design challenge. With film thicknesses normally in the neighborhood of only 5000 angstroms, crossing conductors and insulation between them would act like a capacitor and shunt signals to "ground."



Bootleg Resistors

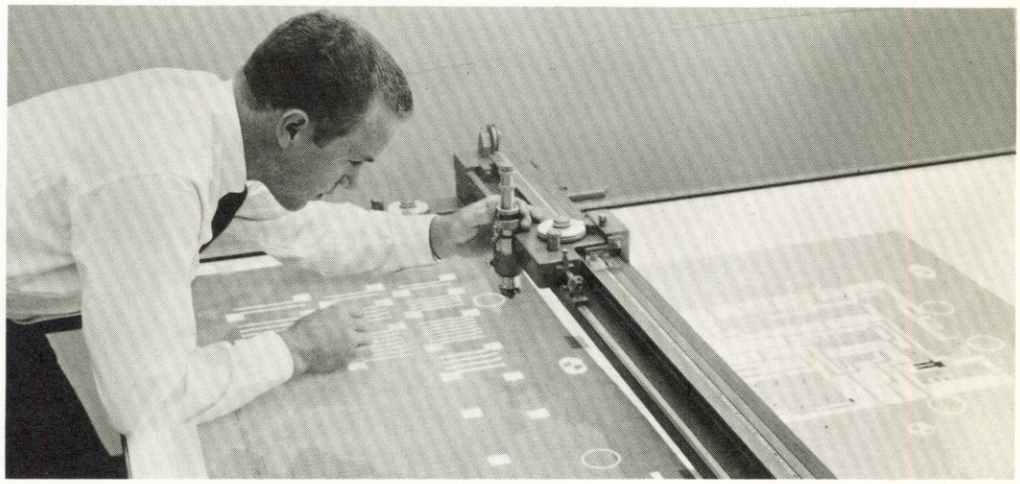
Autonetics designers are exceedingly careful to keep connections to "ground" as short as possible. Conductor lengths behave like small resistors and, unless ground connections are kept short and confined to as concentrated a "ground center" as possible, circuit performance can be badly degraded. In the accompanying photograph, note the directness of the deposited thin-film leads, as well as the brevity of the wire leads from the discrete transistor to the conductor network.

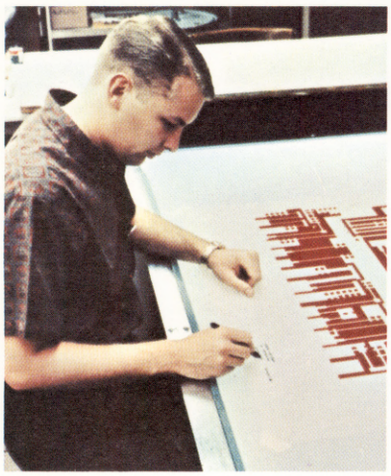
Thin-Film Microcircuit Artwork

The process involved in making a thin-film microcircuit requires a master layout drawing that is from 10 to 40 times the required eventual size of the microcircuit. From this master layout are made a resistor layout, a conductor layout, a dielectric layout, and another conductor layout of top electrodes for the capacitors. All of these layouts are eventually reduced by photographic techniques to their ultimate sizes, for use in fabricating the thin-film circuit.

Making the Master Thin-Film Layout

The thin-film circuit designer follows a circuit schematic to make the master layout drawing for placement of resistors, capacitors, inductors, diodes, and transistors. The designer is guided by his knowledge of the process limitations for fabricating all the passive components and is aware of the electronic functions of the circuit.





Printed-Circuit Originals

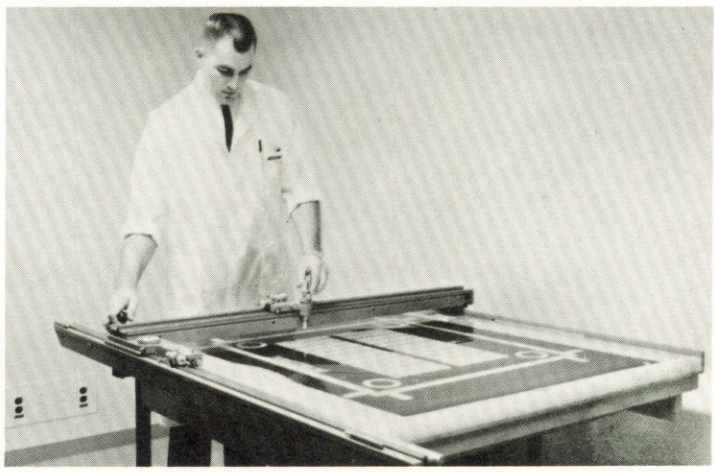
Consulting the master layout drawing, a draftsman makes printed-circuit originals for all passive components—resistors, conductors, dielectrics, and capacitor plates.

Construction Schematic

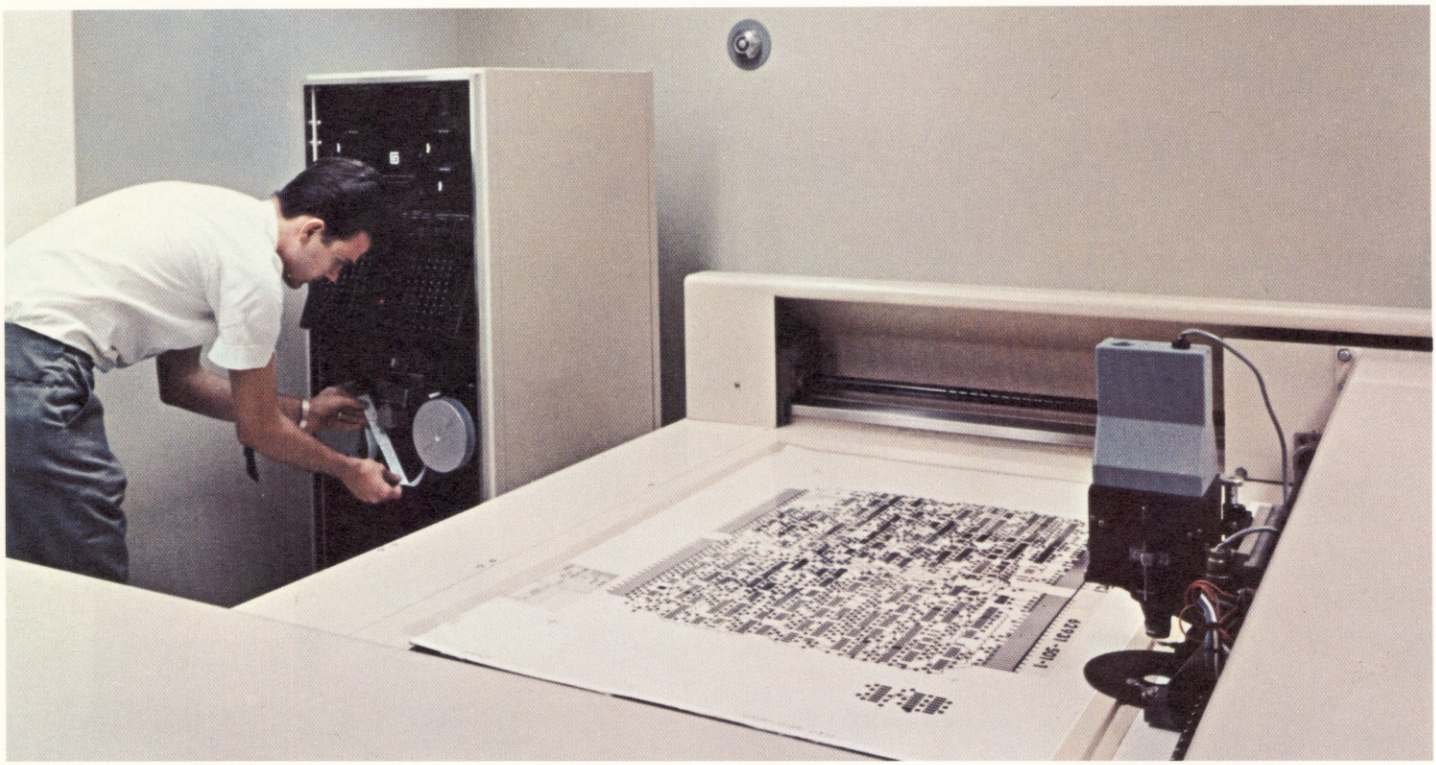
A schematic is made to guide technicians who do the actual fabrication. It keys the various printed-circuit originals to one another so that resistors, capacitors, etc, are correctly located. It also specifies processes for constructing the thin-film circuit.

Circuit Design Changes or Variations

Standard functions can often be revised or varied for a specific operation, just by changing scale factors on the thin-film circuit master layout drawing.

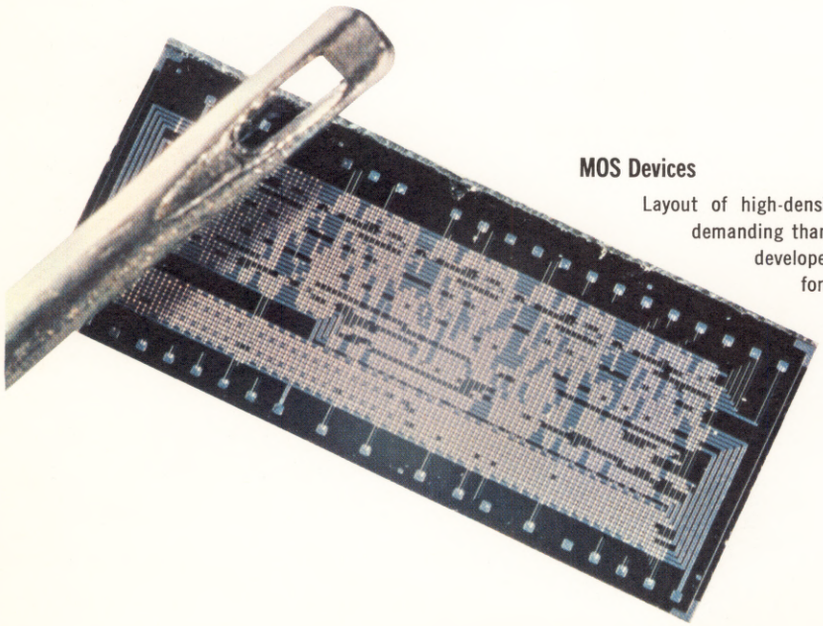


Computerized Layout



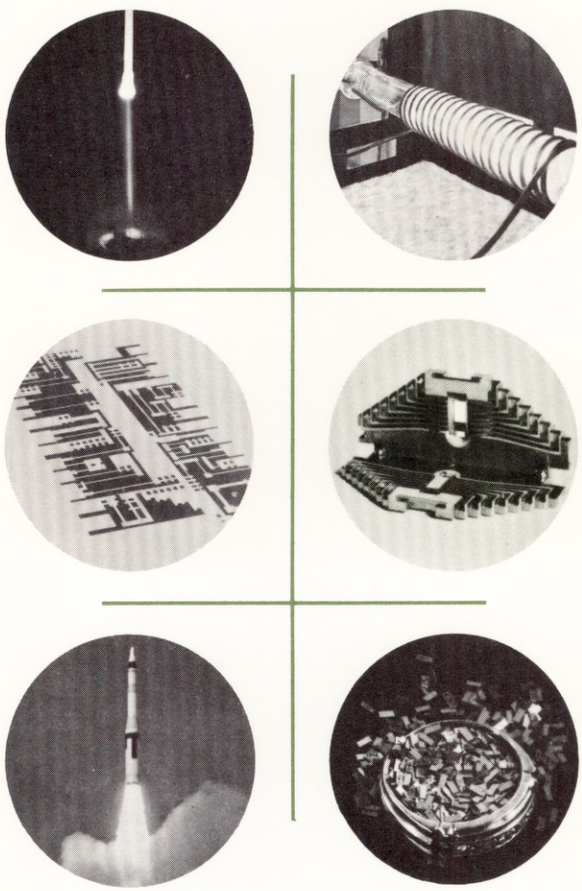
Multilayer Boards

Microelectronics has drastically lessened the number of device **intraconnections.** At the same time, it has called for volume-minimizing methods to prevent device **interconnections** from overcoming the size reduction gained within the devices themselves. One solution has been Autonetics' use of multilayer boards, as described on pages 15 and 94. Interconnection paths for the three-dimensional boards can become extremely complicated, but computerized methods of designing the paths have been developed by Autonetics, and the new techniques have cut design time from a former requirement of 6 man-months to only 1 computer-hour!



MOS Devices

Layout of high-density MOS (metal-oxide-semiconductor) circuitry devices is even more demanding than layout of three-dimensional multilayer boards. Computerized methods developed at Autonetics for MOS layout give better circuit resolution and uniformity, and eliminate chances for human miscalculations. (Details of computerized MOS layout are discussed in Appendix II.)



Producer...

Autonetics is a producer of *systems*—rather than devices or components. Its microelectronic components manufacturing role is, thus, limited to that of *pilot producer*. In this capacity, operations include making research and development microelectronic units available for evaluation in systems, assuring that the devices are uniformly and economically producible, proving their performance capability through rigorous testing, and writing specifications to guide outside suppliers in actual volume-production. When the needed microelectronic devices can be procured economically and in the quantities required, Autonetics procures them. Only when the devices are not commercially available, does the Company step beyond its pilot role and go into components production.

Volume manufacture of systems using microelectronics *is* Autonetics' business. Both microelectronic systems production, and the pilot production of microelectronic components for mechanizing the system, are illustrated in the following pages.

Precision Layout

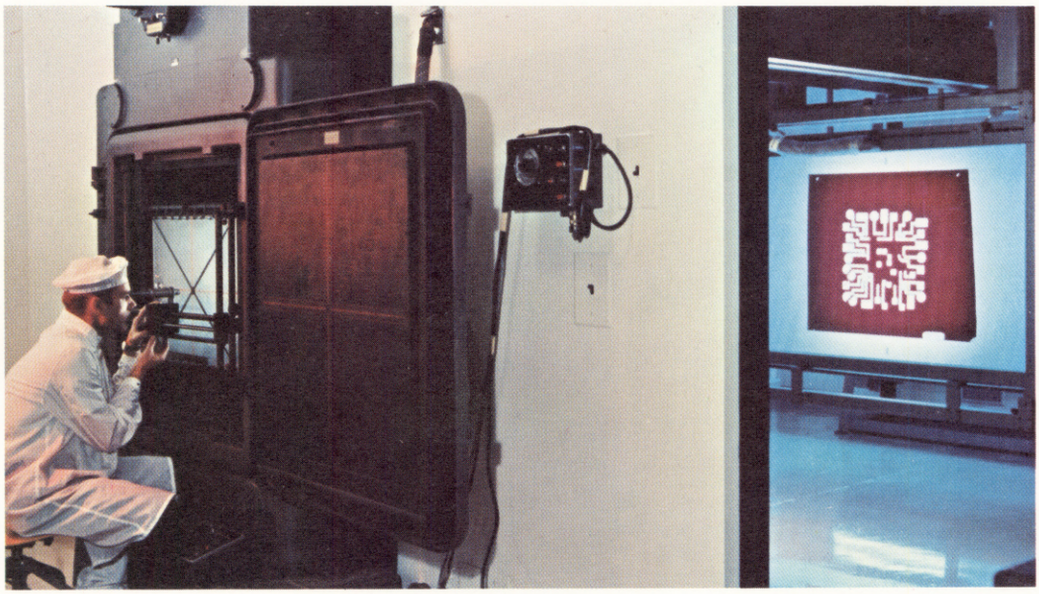
Tape- and card-controlled digital plotters produce artwork for multilayer circuit boards in as little as one-tenth the time required manually. An optical projector, mounted on the plotter carriage, projects circuit images onto stable-base photogaphic material, at predetermined points, to produce an entire complex-circuit layer.

Pattern Cutting

Precision microelectronic patterns are cut on studnite strip-and-peel material. (Here, the pattern being cut is for an integrated-circuit mask pattern original at 400X eventual device pattern size.)

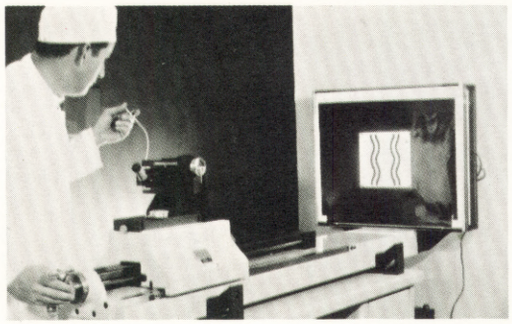
Precision Photography

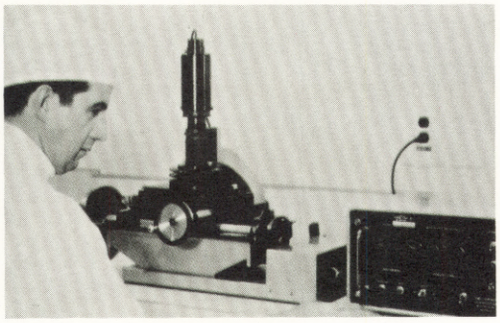
CML's Precision Photographic Laboratory prepares and processes all the masks required to fabricate multilayer boards, thin-film circuits, and semiconductor integrated circuits.



Mask Photo-Reduction

With a Robertson copy camera, an operator reduces a 400X size mask pattern to 200X size. To assure pattern precision, the camera is mounted on a floated platform, isolated from earth and building vibrations. Film artwork as large as 40 in. by 60 in., and glass artwork as large as 40 in. by 48 in., can be handled by the camera. Tolerances of ± 0.001 in. can be maintained over 24 in. of glass plate. The copy and lens board can be mechanically adjusted to within 0.001 in. of the film plane.





Multiple Imaging

An operator programs a photo-repeater to reduce a 10X size mask pattern to 1X size on a glass plate—making precise multiple images during the process. These multiple images of the integrated circuit (or other device) pattern are microphotographically transferred to semiconductor wafers for integrated circuit fabrication.

Mask Micro-Reduction

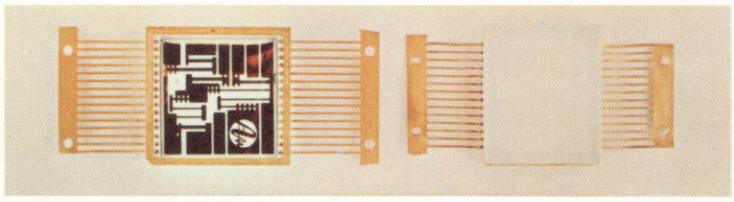
With a Mann micro-reduction camera, a 200X size mask (in the illustration, the mask shown is for an integrated circuit) is further reduced to 10X size. The Mann camera has a variable reduction capability of 10X scale to 20X scale, and a maximum format size of 20 in. by 20 in.

Pattern Precision Check

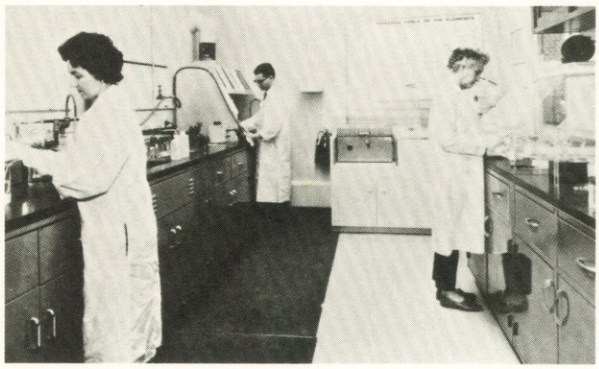
An operator measures multilayer board holes and conductor lines for width and diameter.

Thin-Film Circuits

Thin-film circuits are fabricated in a 3300-sq. ft, temperature- and humidity-controlled area, 900 sq ft of which is also dust-controlled. Facilities include those for photo processing, chemical processing, vacuum processing, and testing. Equipment is provided for cleaning, plating, precision etching, assembly, deposition, and testing. For deposition, there are four vacuum chambers, capable of attaining vacuums of 2×10^{-6} Torr.



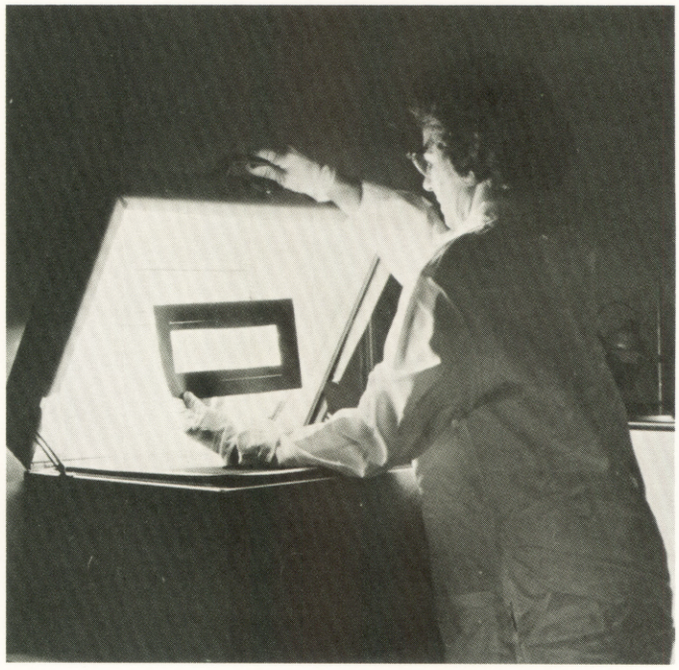
Thin-Film Microcircuit



Chemical Processing Area

Photolithography

With standard photolithographic techniques, the microcircuit print is transferred to the substrate. A multiple selective etch produces the microcircuit.



Master Artwork

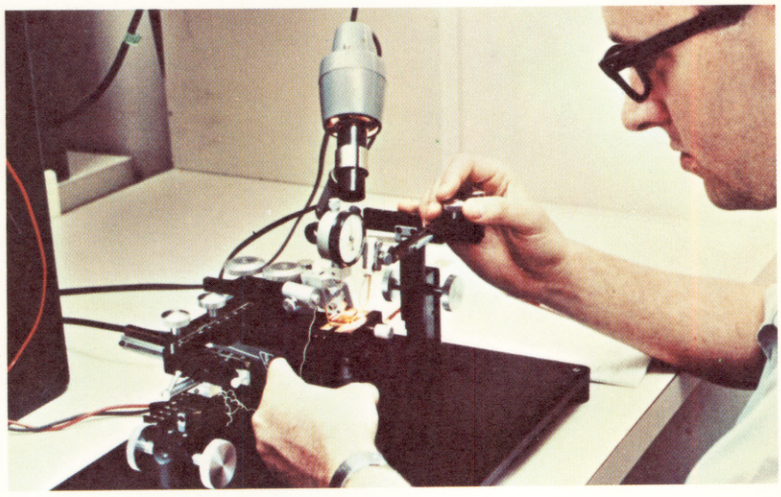
The master artwork defining circuit elements is made with a precision coordinatograph. The layout is then sent to the photo processor for reduction to microcircuit actual size.

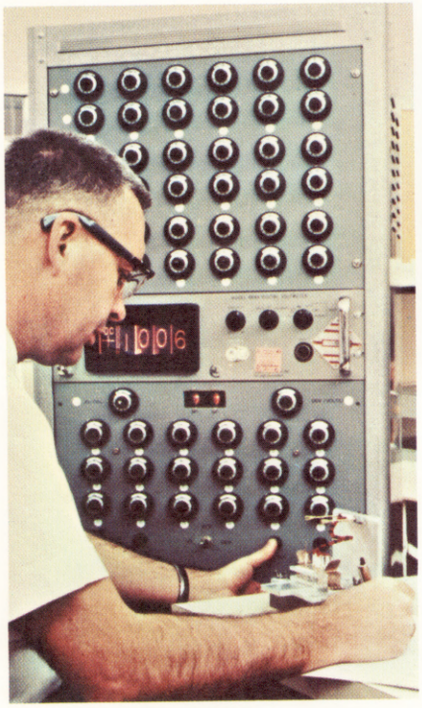
Processing the Substrates

Substrates are processed in a 6-position, lazy-Susan type of evaporation chamber. Resistive material is evaporated onto the substrate from a multiple-position electron-beam gun in the chamber.

Resistance "Trimming"

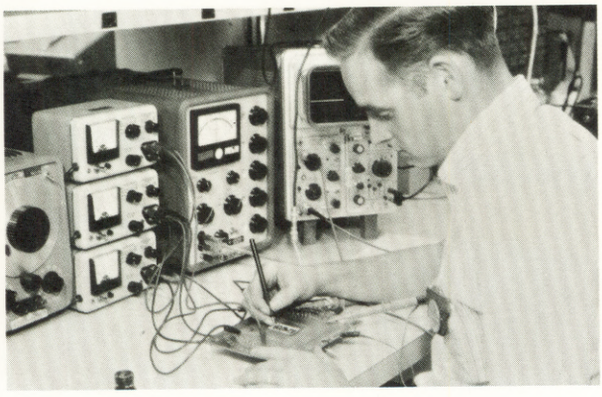
Resistor values are trimmed to specified tolerances. One-percent tolerances are commonplace, and one-tenth percent values can be achieved. Trimming is accomplished by using a diamond scribe to remove conductive shorting bars from the resistors. (Both the resistors and the shorting bars are thin films.)





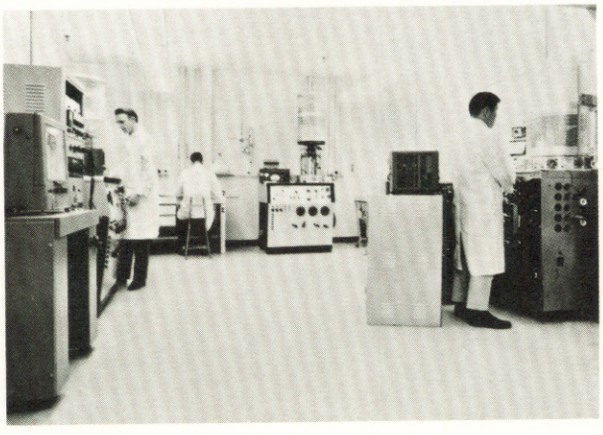
Initial Testing of Components

Resistance and capacitance of individual thin-film "components" are measured by a semiautomatic testing machine.



Final Microcircuit Test

Any need for potentiometers in the circuit is precluded by "dynamic trimming" (that is, trimming during actual circuit operation) of resistance values to the precise values for best performance of the particular circuit involved.



Assembly

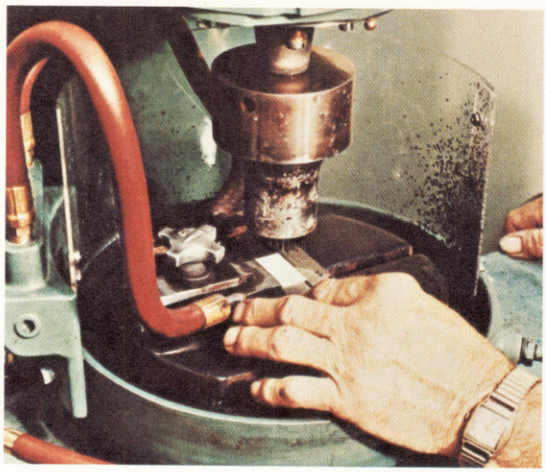
In the thin-film microcircuit assembly area: Discrete components are soldered to the microcircuits; leads from cans are soldered to conductor pads on circuits (for interconnection); a conformal coating is applied to circuits and components; lids are placed on cans and the cans are sealed; and cans are stamped to identify the circuits they contain.

Ceramic Printed (Thick-Film) Circuits

Thick-film or ceramic printed circuits are fabricated in a 13,000-sq ft, air-conditioned, dust-controlled area. Facilities and personnel are provided for producing screens, adjusting screened resistors, attaching discrete components, and functionally testing the circuits.

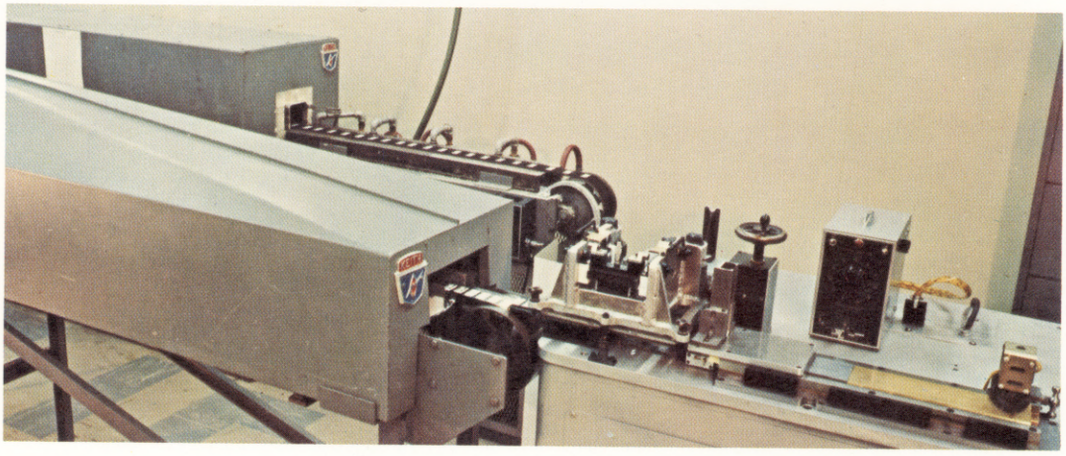
Conductive Through-Holes

A method of effecting through-hole continuity to allow mounting of components on both sides of ceramic-printed-circuit substrates uses a vacuum during conductor screening to draw gold-platinum ink through the holes. The technique permits dense circuit designs, with screened resistors on one side and discrete components on the other.



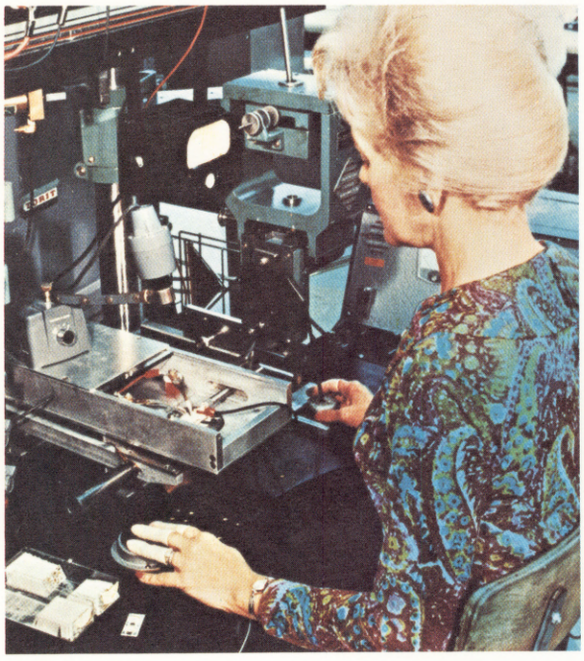
Ultrasonic Impact Drilling

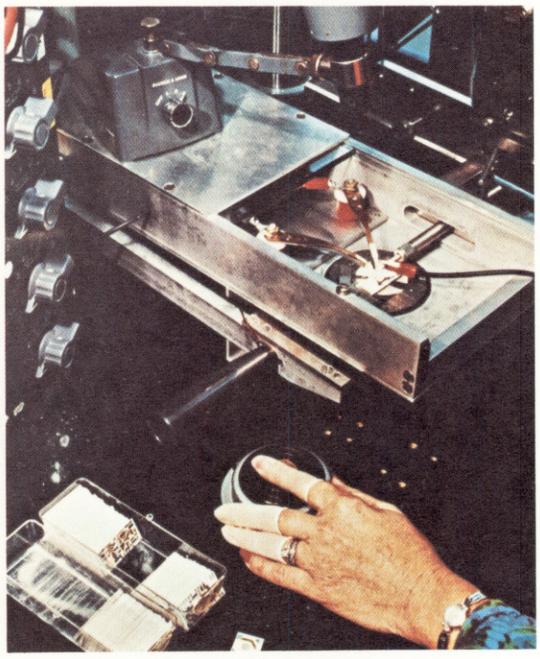
Holes are drilled in the ceramic substrates to allow attachment of discrete devices to ceramic printed circuitry later screened onto the substrates. Holes within the 0.020- to 0.500-inch diameter range can be drilled with this technique.



Automatic Screening

Conductor/resistor patterns are printed by an automatic screening machine, with belt feed into a pre-firing kiln.



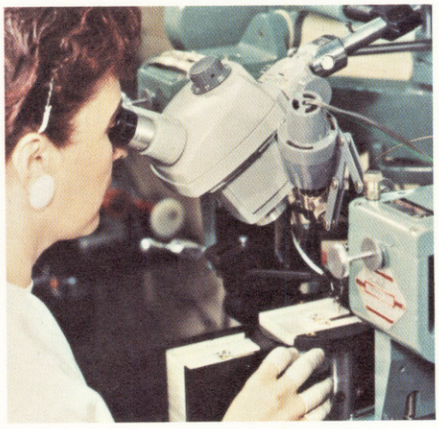


Screened-Resistor Adjustment

Individual printed resistors are adjusted in value to required tolerances. One-percent tolerances are achievable by removal of noble metals embedded in the resistor deposit following the firing cycle. Removal of these metals from the edge of the resistor by an air-operated abrasion unit gives positive control of precision resistance values, and increases reliability by eliminating the possibility of "hot spots."

Preparation for Receiving Discrete Components

The ceramic printed circuits are subjected to automatic dip soldering. Subsequently, the discrete components are connected to the circuitry by means of resistance soldering.

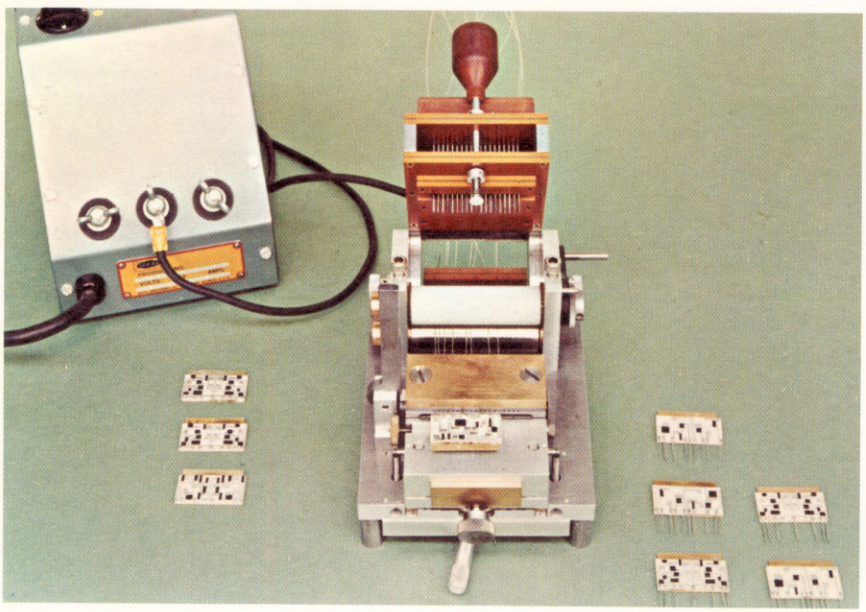


Attachment of Discrete Components

Discrete components are resistance-soldered to the ceramic-printed-circuit chips.

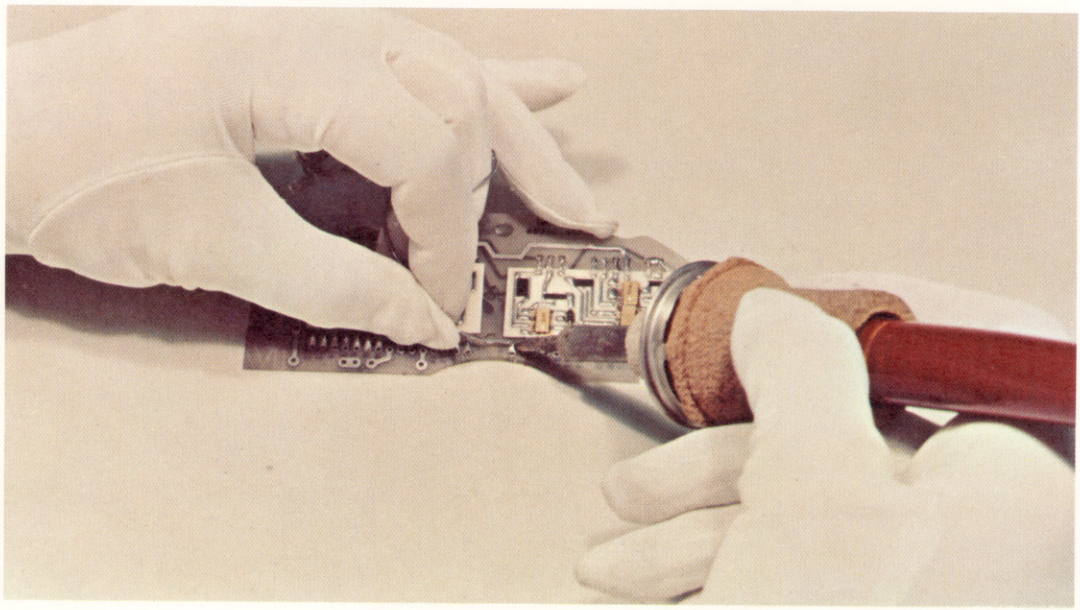
Protective Coating of Microcircuitry

Following component soldering, ceramic printed circuits are given a protective coating and then dried in a vacuum chamber. Former methods often entrapped air in the coating and formed bubbles, pinholes, and voids. The new method virtually eliminates these defects, with no degradation of hermetically sealed components.



Lead Attachment

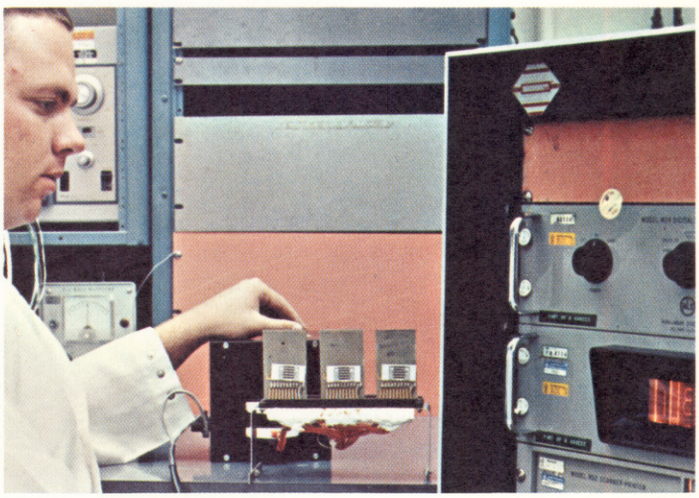
Ceramic-printed circuit leads to the "outside world" are connected to the devices with a lead-attach jig.



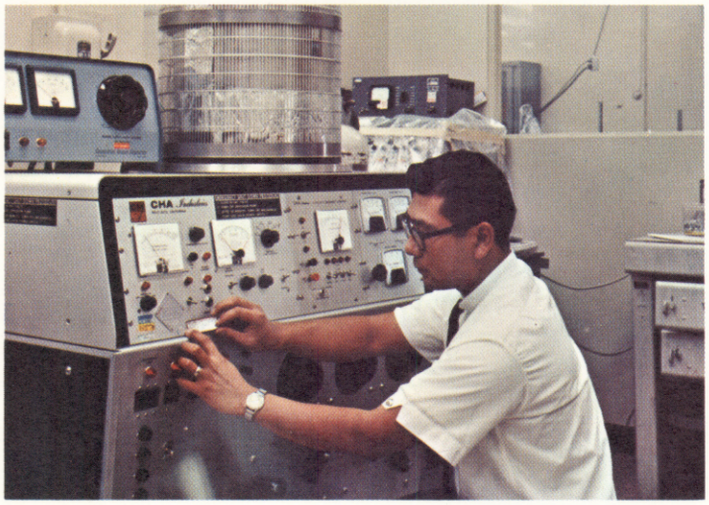
Interconnection with Other Circuits

A ceramic-printed-circuit is interconnected with other circuits on an etched-circuit board by soldering.

Chemical Analysis of Processing Solutions



Resistor Test Pattern Measurement

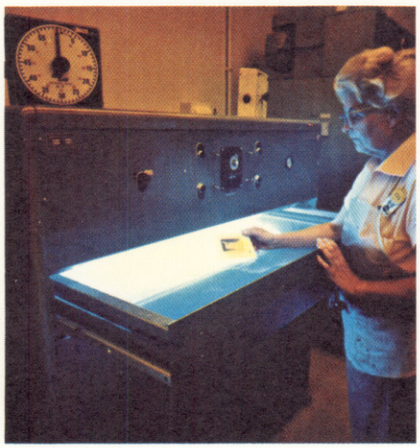


Vapor-Deposition Equipment Qualification

Ceramic-Printed-Circuit Process Control

Tight process control is assured for ceramic printed circuits by intensive chemical analysis, test pattern measurement, equipment qualification, and rigid materials and packaging inspection procedures.

Ultraviolet Inspection of Substrates

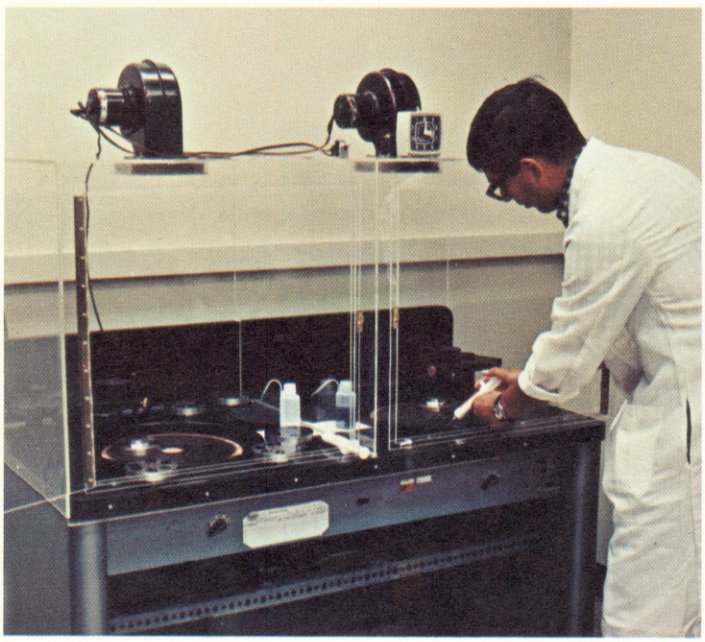


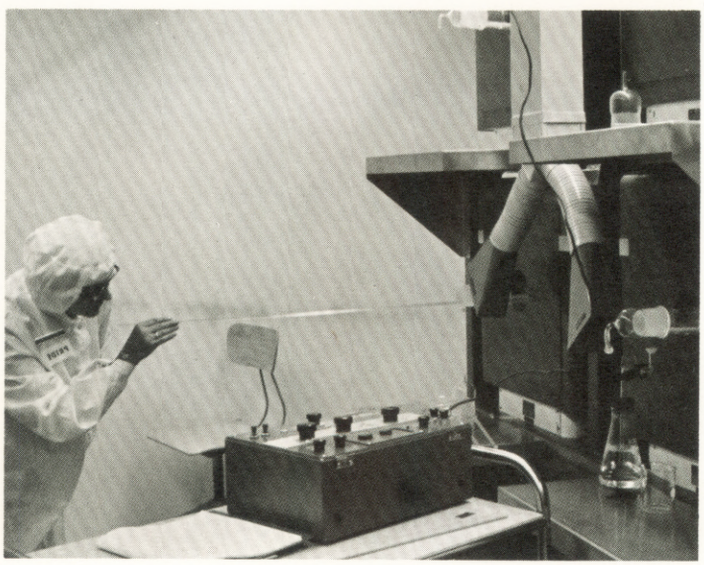
Process Control of Photo Resists

Semiconductor Integrated Circuits

Surface Preparation of Bulk Silicon Wafers

Silicon wafers for integrated circuit diffusion are prepared by means of a polishing table with two 12-inch wheels for 1-micron and ½-micron diamond paste finish, a lapping machine to lap slices to thickness of 0.005 inch and less, and a Lapmaster machine modified to carry out lapping operations or mechanical polishing.





Epitaxial Growth and Oxide Coating

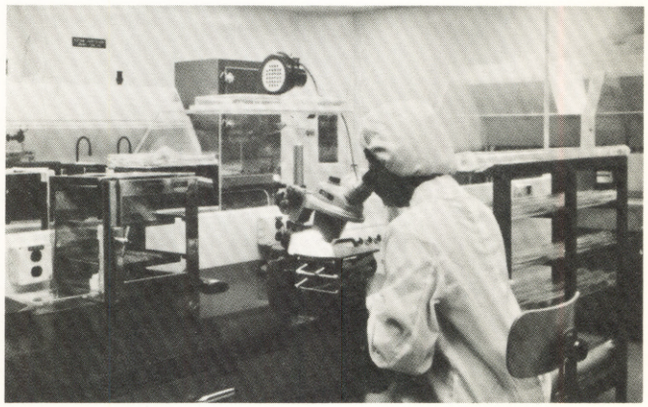
Polished silicon wafers are exposed to gaseous silicon to continue the crystal epitaxial growth with an impurity of opposite type (n or p) from the base silicon. The resulting surface is coated with silicon oxide in a high-temperature furnace.

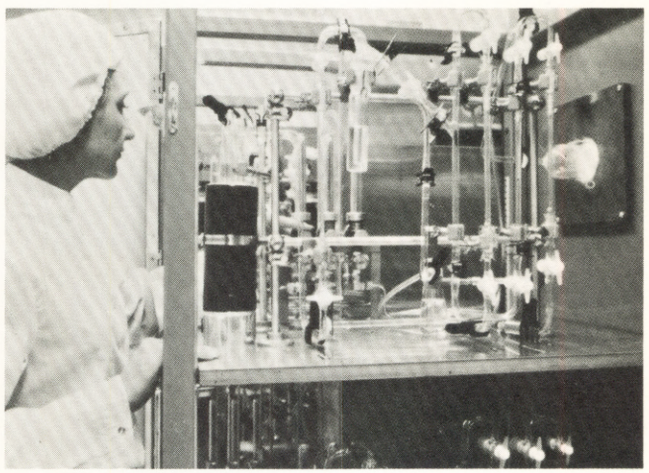
Masking the Wafer

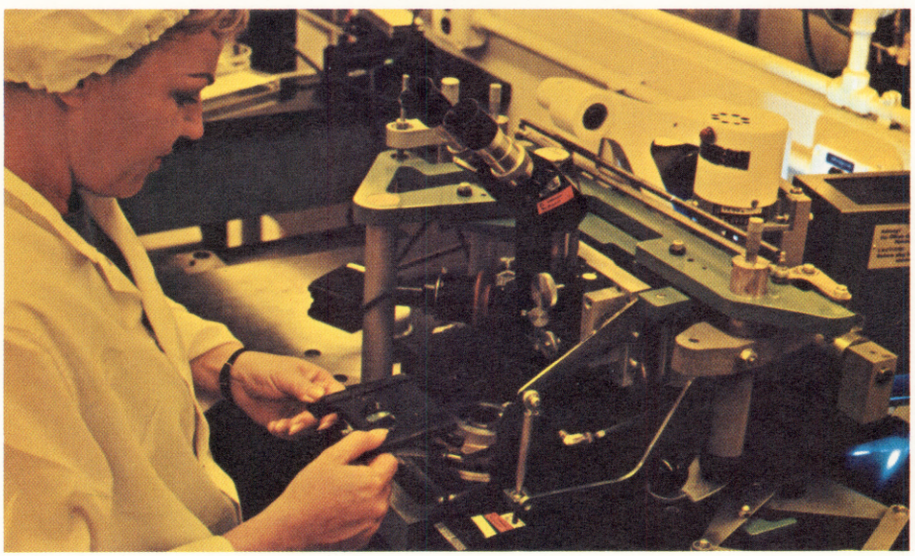
The patterns for circuit processing are applied to the semiconductor wafer by photolithography. As a first step, photo resist is applied to the entire surface.

Etching the Diffusion Pattern

The silicon oxide coating is etched away along the lines of the desired diffusion pattern.







Impurity Diffusion

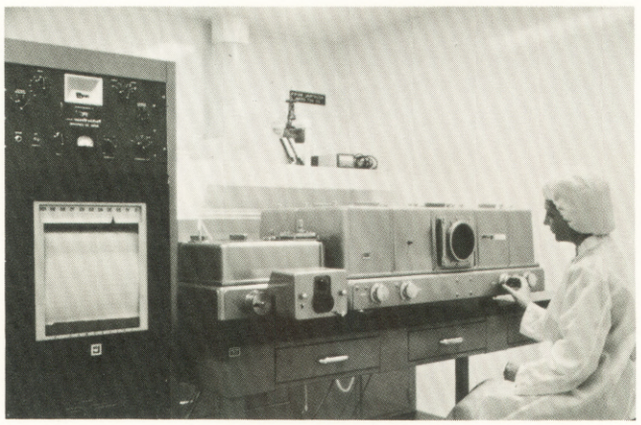
The etched silicon is inserted into a gaseous diffusion system. There, the desired n- or p-type impurities are diffused into the silicon only where the oxide has been etched away. Temperature and pressure are tightly controlled to assure the proper diffusion.

Mask Alinement and Exposure

A vacuum holds the photo-resist-coated wafer in place on an anvil. When the circuit pattern mask and fixture are precisely alined with the aid of a microscope, the photo resist is "fixed" on the silicon wafer by exposure to ultraviolet light.

Dopant Analysis

Technician operates an infrared spectrophotometer to analyze the dopant diffused into the wafer.

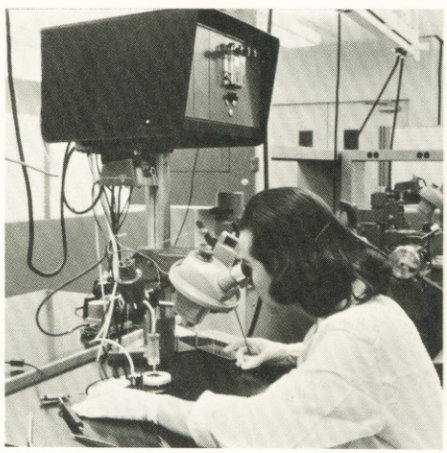


Applying the Conductors

To make interconnections between diffused devices, the wafer is metallized in a vacuum chamber. The excess metal is then etched away to leave the desired pattern of conducting lines.

Scribing into Separate Dice

Each wafer contains many identical integrated circuits. To separate these, the wafer is first marked on a scriber. It is then turned over and subjected to pressure, which causes it to break along the scribed lines into "dice," each die containing a single circuit.

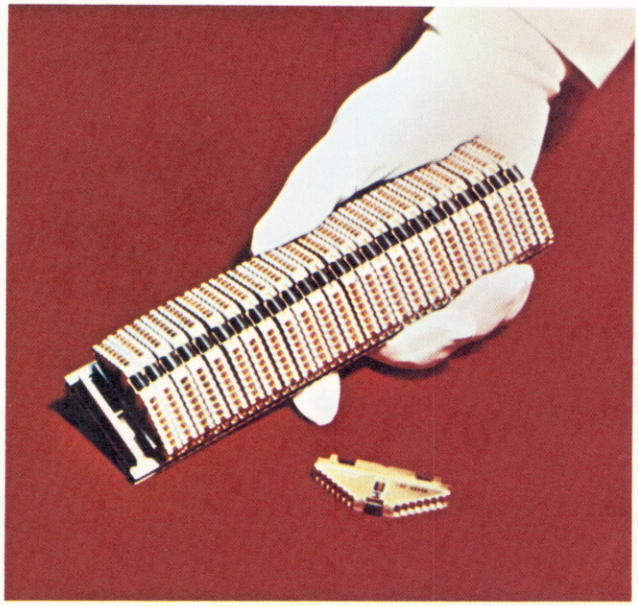


Mounting the Individual Circuit

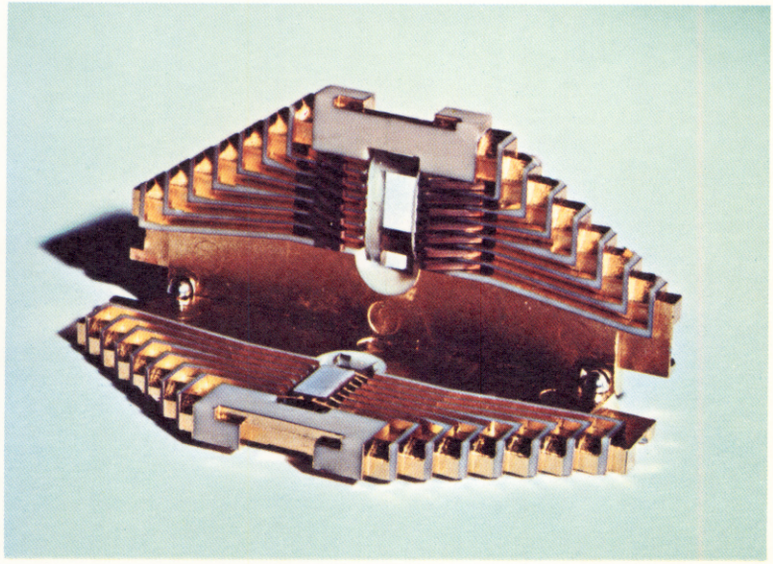
Each circuit die is mounted in the appropriate package.

Connecting the Leads

After the die is mounted in the package, 1-mil gold-wire connections are "nail-head-bonded" between the die and the package terminal posts.



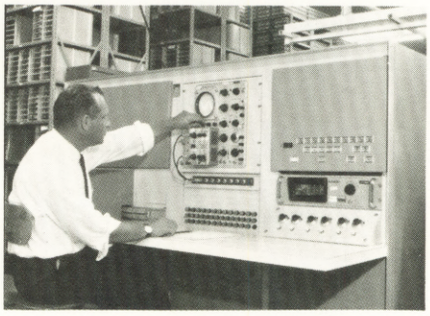
"Stick" Full of "Clam-Shells"



"Clam-Shell" Carrier
(Note IC within Clam-Shell)

Production Testing

An automatic production test console performs electrical testing of Minuteman IC's. Each IC is inserted into a "clam-shell" carrier. The clam-shells are then inserted into a "stick," capable of carrying up to 100 integrated circuits without solder connections, and with either straight- or bent-lead mounting. The clam-shell/stick combination permits complete performance measurement and electrical evaluation of integrated circuits by automatic test equipment, without the necessity for human handling of the microelectronic device itself.



Production Test Console

Assembly and Inspection

Integrated circuits are assembled in a 20,500-sq ft environmentally controlled area. A semiautomatic insertion line in the area provides an efficient method for assembling packaged IC's and discrete components. In this process, an Autonetics-developed placement and bonding machine is employed to position and attach the components on multilayer and printed circuit boards. Discrete components are soldered to the boards by operators using 30X microscopes. A 3900-sq ft area is available for application of protective coatings.

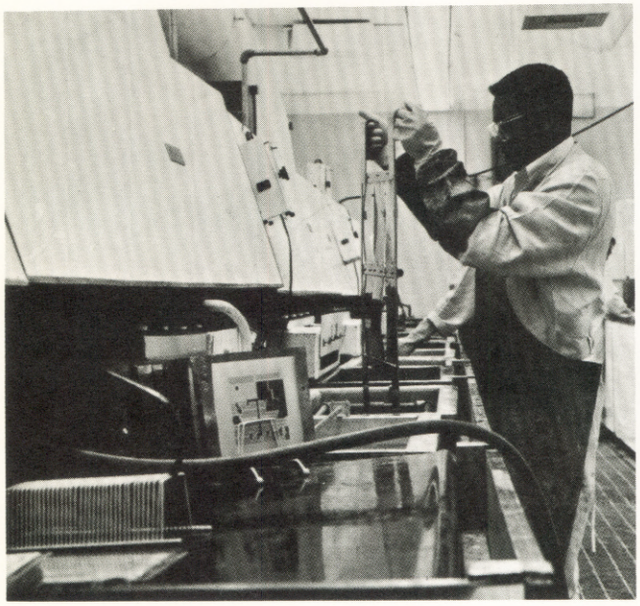
Integrated
Circuit Inspection

Integrated Circuit Placement and Bonding Machine

Circuit Boards

Multilayer Board Production Facility

The 10,000-sq ft multilayer board production facility is made up of eight environmentally controlled areas equipped for precision photography, ultrasonic cleaning and etching, plating, laminating, and testing. Production capacity of the facility is 1000 eight-layer boards per month, with expansion potential for 1800 boards per month. The accompanying three photographs show chemical processing of the boards.

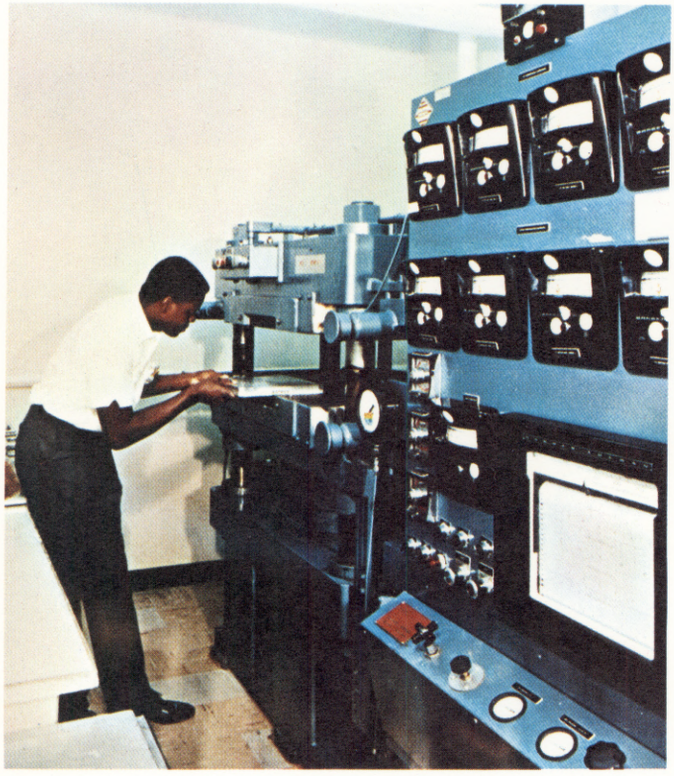


Multilayer Board Layout

Ten of these long, slender layouts are prepared for each multilayer circuit board for the D26C computer. An average board and the microcircuits it carries are equivalent to some 10,000 discrete components.

Multilayer Board Laminating Press

A 100-ton laminating press provides complete plated through-hole multilayer board fabrication. Each of the boards consists of several layers of circuitry, laminated and interconnected by plated through-holes to form a compact circuit network.



Multilayer Board Quality Check

Multilayer board plating thickness is measured with a precision metallograph.

Printed-Circuit Board Production Facility

All types of printed-circuit boards—flexible or rigid laminates, single- or double-sided, with or without plated through-holes, plated with copper, solder, or gold—are produced in a 10,000-sq ft, air-conditioned facility. Production capacity is more than 5500 boards per week. Boards range in size from 1 inch to 30 inches square.

Computers and Flight Control

Computer and Flight Control Assembly and Test

The computer assembly department, capable of assembly and test of as many as 81 computers per month, occupies 18,170 sq ft, of which 12,900 sq ft is environmentally controlled. Three vibration systems, of 5000-lb capacity each, test the computers following final assembly. A peak production rate of 67 flight control assemblies per month has been attained in another area of similar environmental control and size. An additional 2800-sq ft area is dust- and temperature-controlled for assembly and test of hydraulic flight-control components.

Microeletronics Assembly for Minuteman

Minuteman II flight control and computer electronics are assembled in a special, separate area.

Static Module Tester

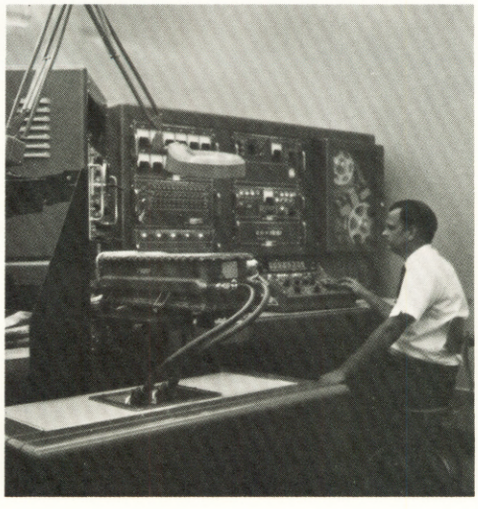
This machine for testing D26C multilayer boards and modules has the capability for simulating all inputs. With its 320 input/output pins and 220 test points, it can provide or measure signals at all 540 points.

D37 Production Line

D37 computers for Minuteman II are completely micro-electronics-mechanized for reliablity and performance.

Power Load Test of D37 Computer in Final Test Area

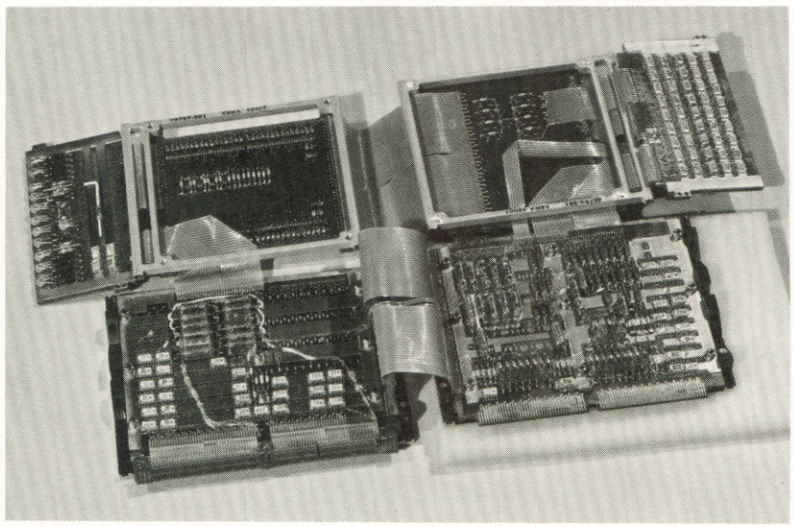
Mode boards have been inserted into the computer to test the power supplies. In this test, scope measurements must be made, and certain tolerances must be met. Following this point, the memory subsystem is installed, and the logic boards which, together with the power supplies just checked out, make up a complete unit. Next, the computer undergoes dynamic functional test.



Final Functional Test of D37 Computer

A final test program is fed into the memory, and the computer is then switched to the "compute" mode; from this moment on, the computer does all the work. Arithmetical instructions are entered, and the computer checks them out. Many tapes are put in, checking every complete function of the computer. After the computer leaves this final test area, it is connected with the inertial navigation set to become part of an actual, working system.

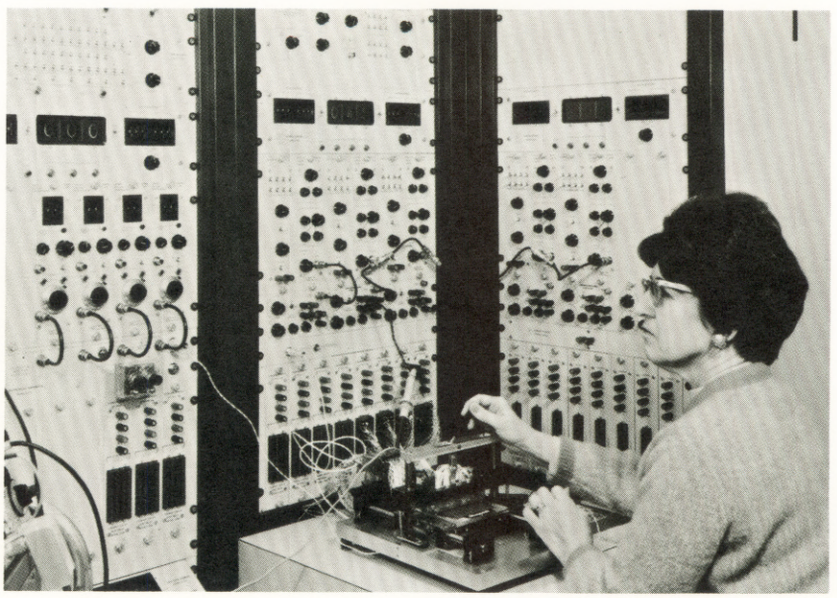
Core Memory



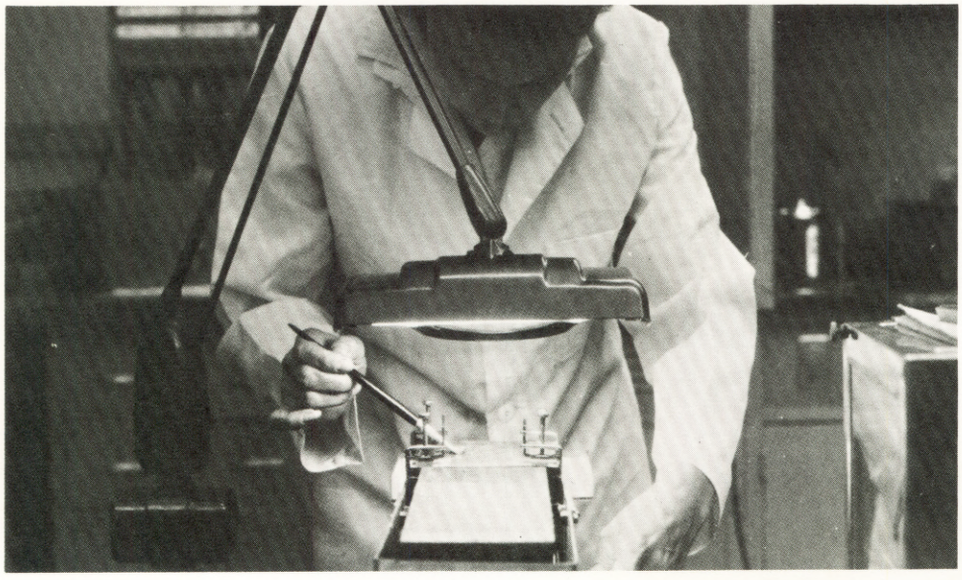
Automatic Core Tester and Handler

Core Memory Capability

The 2000-sq ft, environmentally controlled core memory production facility is capable of producing 500 memory planes (4096 cores/plane) per month. Equipment includes an automatic core tester and core handler for testing individual cores, and an automatic plane and stack tester for testing individual planes and entire stacks of planes.



Automatic Plane and Stack Tester



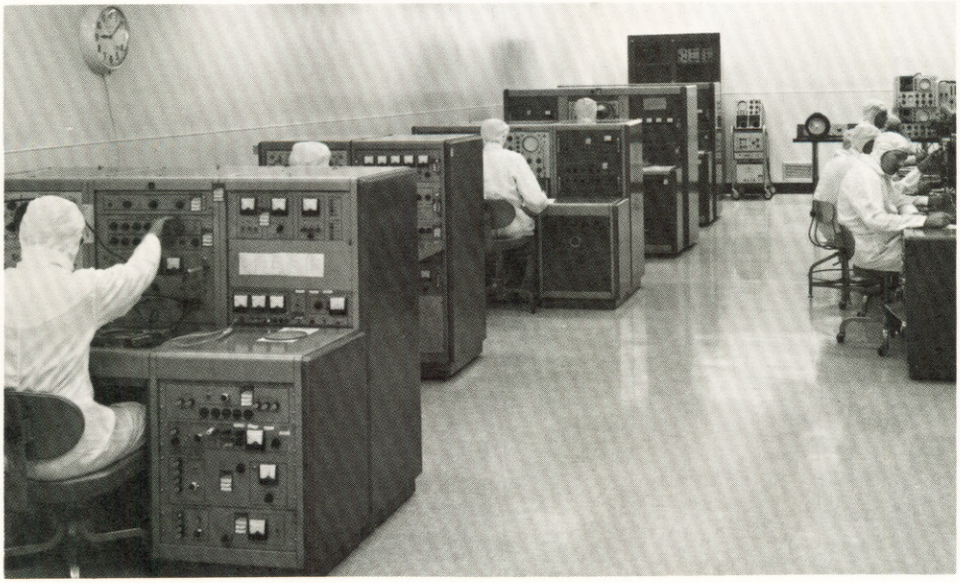
Filling the Memory Plane

Cores are poured across the top of the plane. Vibration then causes them to move down the plane until they fall into core holes—thus eliminating manual handling. After the plane is loaded in this manner, the cores are positioned by means of a rubber pressure plate which pushes them down into the holes while the plane is heated in a curing oven.

Disk Memory Assembly and Test

The 5500-sq ft, environmentally controlled disk-memory assembly shop has produced memories at a peak rate of 85 per month.

Disk Memory Assembly

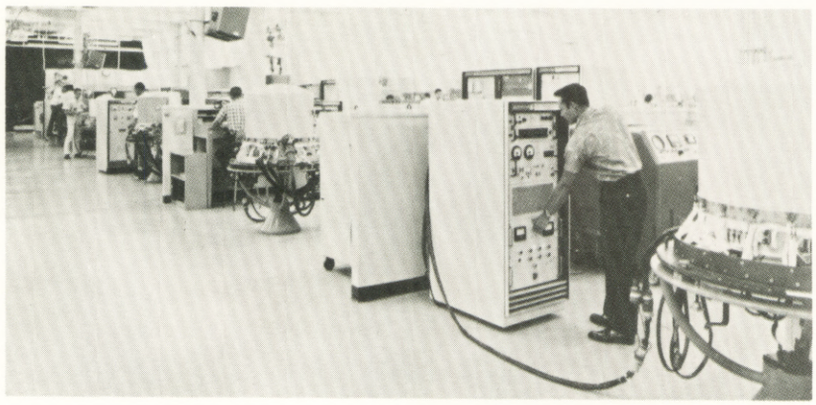


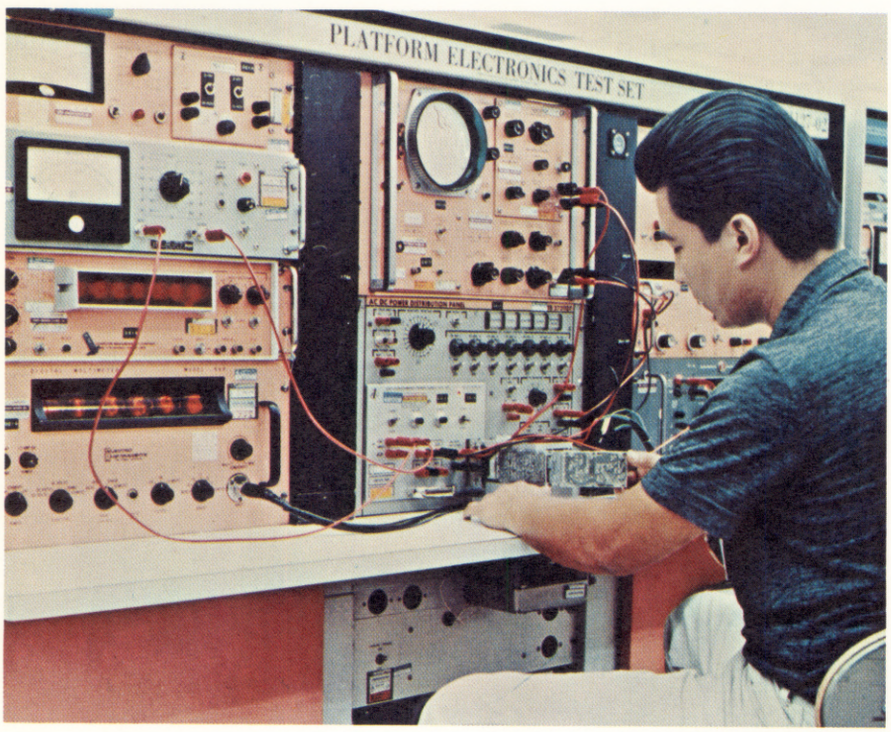
Disk Memory Functional Test

Navigation Equipment

Guidance System Assembly and Test

Guidance systems are assembled and tested in an 18,000-sq ft, environmentally controlled area, with a production capacity of more than 60 systems/month.





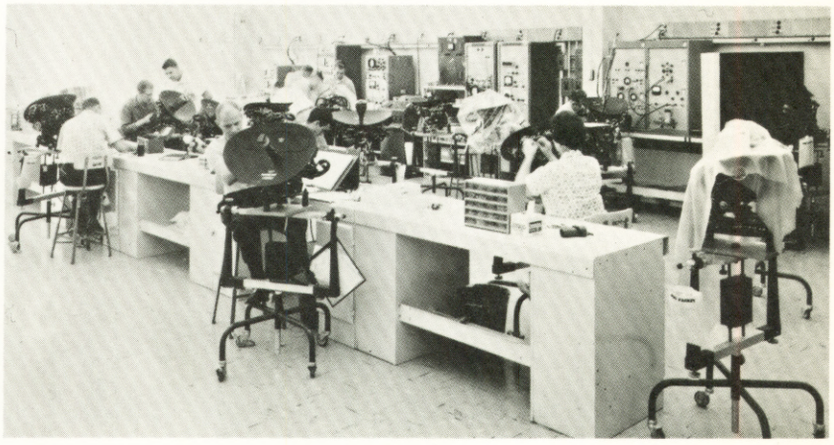
Inertial Instrument Assembly

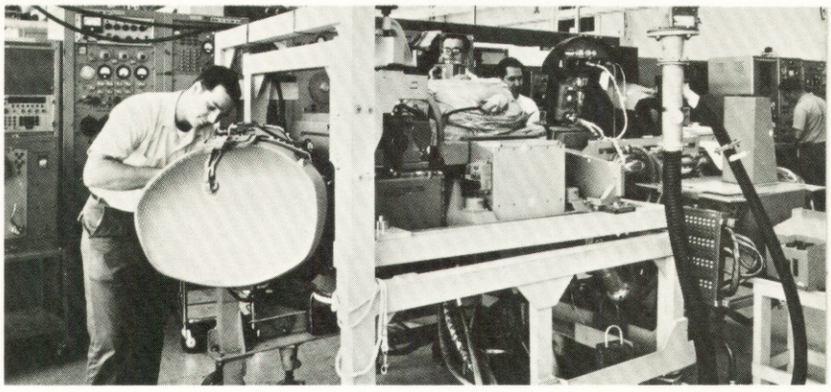
A total of 30,000 sq ft of temperature- and dust-controlled area is used for production of inertial instruments (such as the electromagnetic accelerometer described on page 85). Maximum dust count of particles as big as 5 microns (5 millionths of an inch) in diameter is limited to 500 particles per cubic foot. Work stations are individually equipped with microscopes, dry nitrogen, vacuum lines, and a variety of electrical utilities. For even more exacting dust control than that in the general controlled areas, thirty-five special, individual, dust-controlled work stations are maintained. Twenty types of instruments (gyroscopes, velocity meters, and accelerometers) have been produced at a peak rate of 600/month, with area maximum capacity being 1000/month.

Electro Sensor Systems

Radar Antenna Assembly and Test

Antenna assembly and test facilities at Autonetics have supported the production of nearly 2000 airborne radar systems. Precision mechanical and electronic subassemblies are mated and tested as subsystems within this facility. Testing capabilities include: waveguide pressure testing and checkout; precision boresight alinements on specially designed test towers; radiation pattern tests on another special tower; and life, wave ratio, power, and final functional testing.





Radar/Sensor System Assembly and Test

The operations of radar/sensor subassembly and test, and integration of these units into complete systems, are performed in adjacent areas. Tests include subjection of the equipment to simulated operational problems and situations encountered in actual use. Complex company-designed consoles provide the system stimuli for these tests and measure operating characteristics of the equipment being tested.

Special Support

Module Assembly and Test

The module assembly and test department is responsible for the production and functional testing of circuit board modules for all Autonetics radar, navigation systems, computers, flight control, and ground equipment. Production capacity is more than 2500 modular subassemblies per week.

Welded Modules

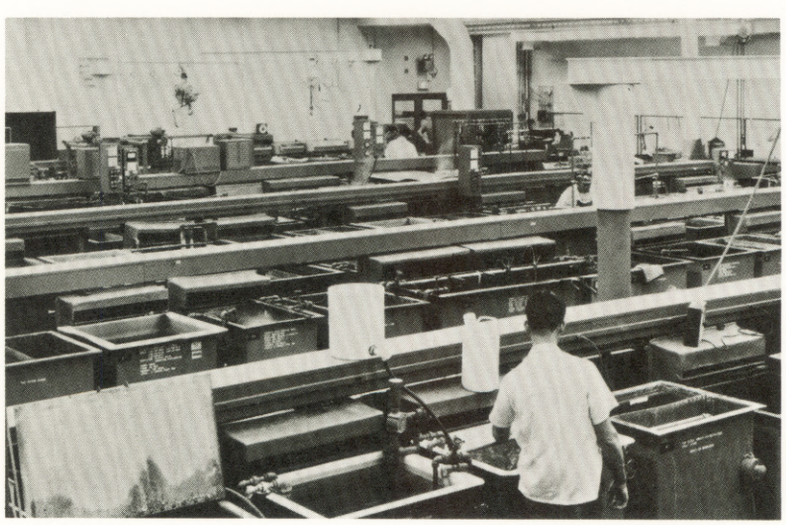
Welding of "cordwood" modules is performed in a 1200-sq ft temperature- and humidity-controlled area containing 23 precision resistance-weld stations.

Optics

A specialized facility shapes, laps, and polishes to optical specifications any size optics up to 24 inches in diameter. It has the capacity to produce as many as 500 optical parts per week, utilizing glass, fused silica, ceramics, and metal.

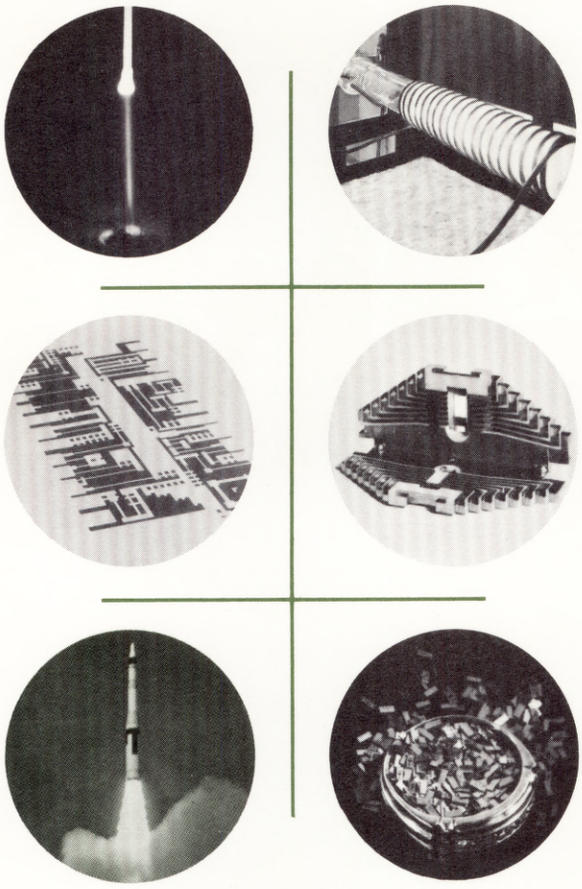
Mechanical Assembly and Test

Approximately 22,500 sq ft is devoted to precision mechanical assembly of hardware – from small gear trains to complex large equipment such as SINS (Ship's Inertial Navigation System) for the Polaris-carrying submarines of the U. S. Navy and the United Kingdom.



Precision Plating

The 5600-sq ft precision plating area contains 196 separate plating and processing tanks. Capacity of the facility is 200,000 instruments per month, with plating tolerances held to as little as ± 0.0001 inch.

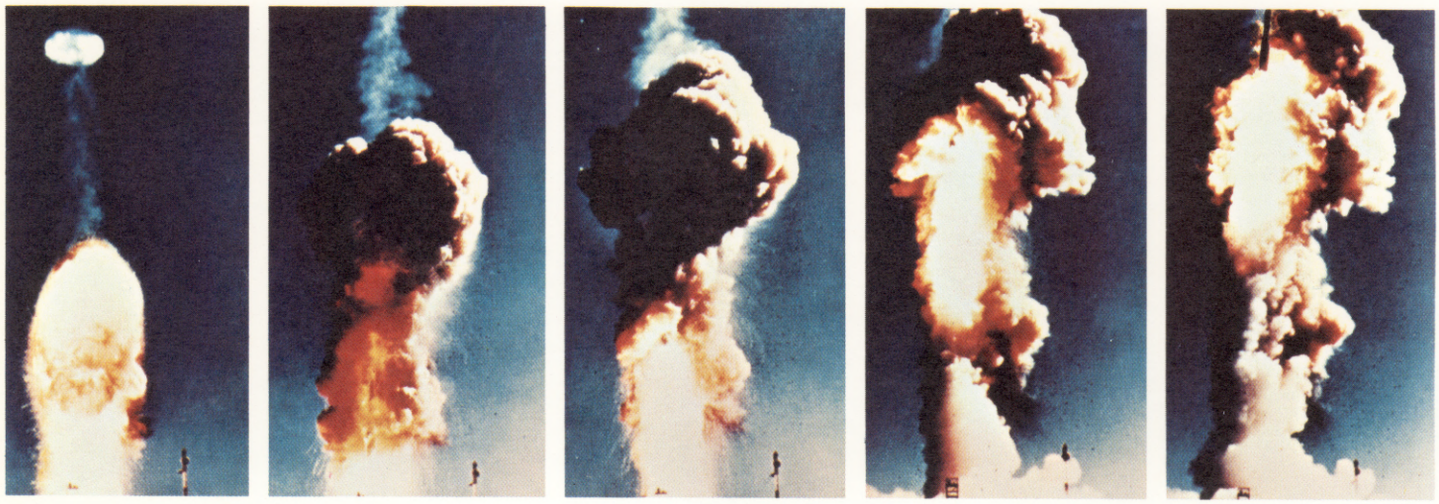


Purchaser...

Under the Company's Make-or-Buy policies, Autonetics selects those subsystems and components which produce an end item representing the best possible tradeoff for meeting requirements—whether the product is manufactured within the Company or is obtained from an outside source. Final decision is made by representatives of Quality Assurance, Engineering, Manufacturing, Purchasing, Plant Engineering, Contracts and Pricing, and Program/Project management. The Make-or-Buy Policy Board, consisting of high-level management appointed by the Executive Office, provides overall policies and objectives; and Make-or-Buy Committees in each product division implement and administer the policies and goals of the Board. The Make-or-Buy policies broaden the base of business competition and contribute substantially to product reliability and performance, as well as to fair prices to the customer, and on-schedule delivery.

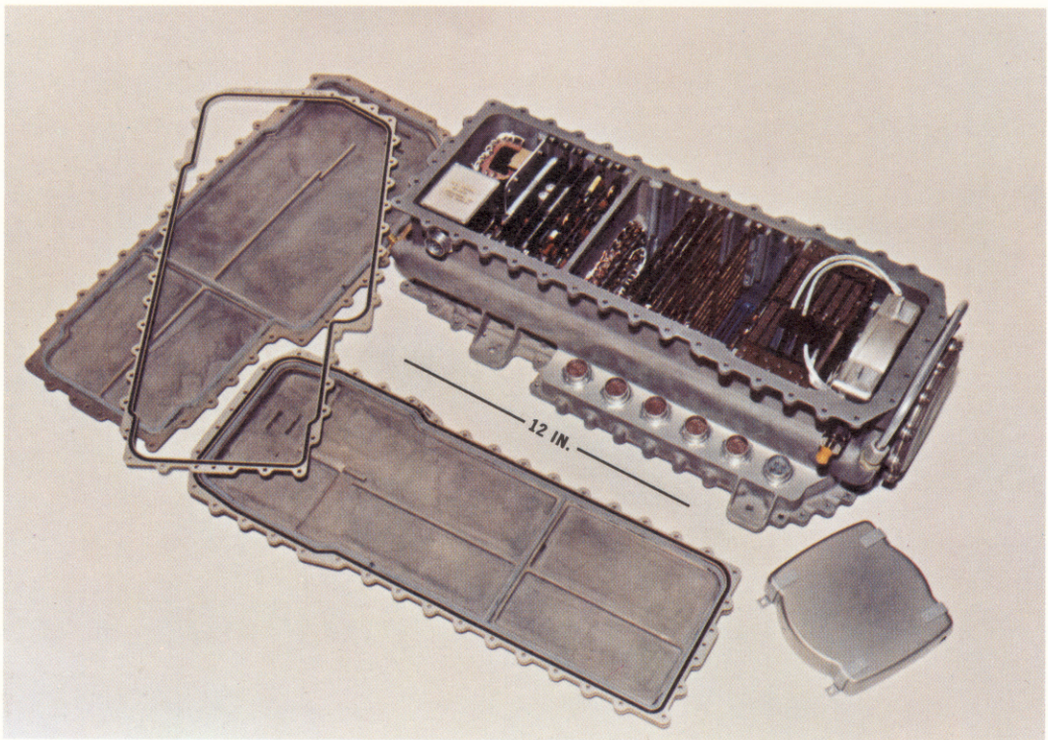
Minuteman II Is World's Largest User of Microelectronics

Minuteman II has become the largest consumer of semiconductor integrated circuits, as deliveries of this type of microelectronics in mid-1965 climbed past the half-million mark for the missile's guidance and control. Each missile uses about 2400 semiconductor microcircuits, plus another 600 for associated ground support equipment and test quantities. Dollar volume of Minuteman microcircuit purchases in 1965 accounted for about 20% of total industry sales.



Radiation Resistance

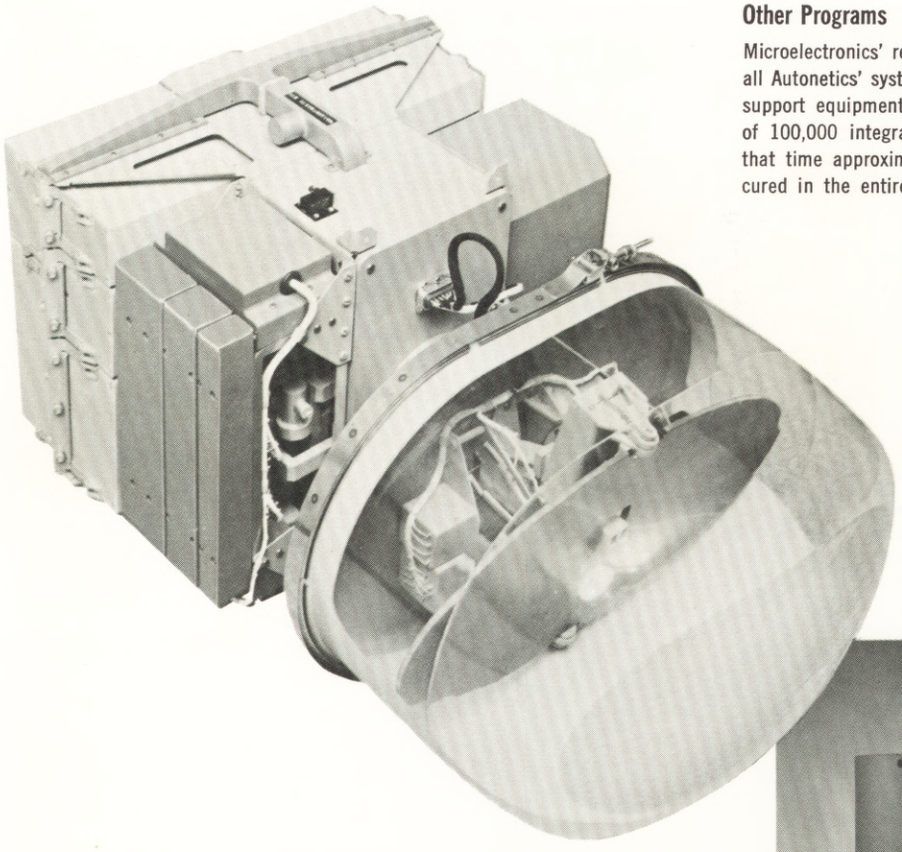
All operational Minuteman II microelectronic guidance and control systems are designed to withstand nuclear radiation.

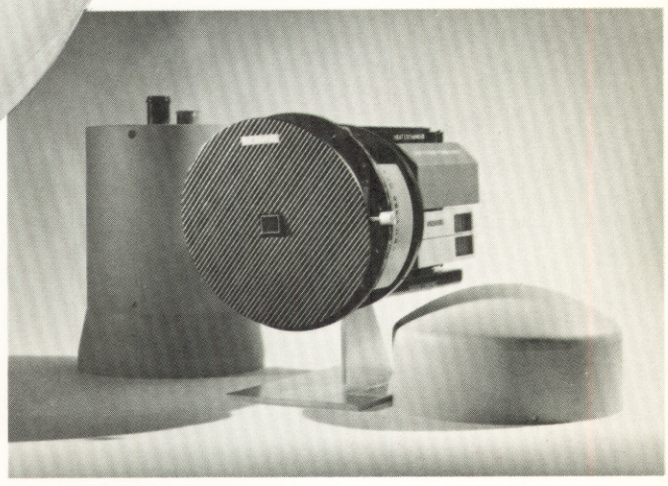


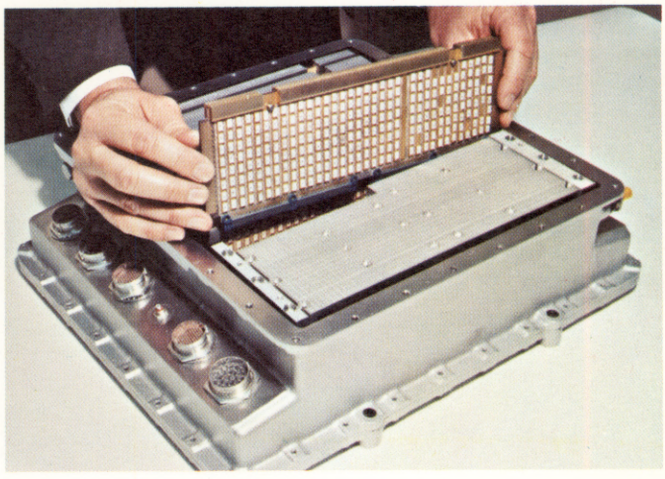
Other Programs

Microelectronics' record-breaking report card on Minuteman has led to its use in all Autonetics' systems—computing, navigation, flight control, radar, and ground support equipment. The Company approached, as 1966 started, a requirement of 100,000 integrated circuits per month. Dollar-wise, Autonetics procured at that time approximately 25% of all the semiconductor integrated circuits procured in the entire U.S.A.

As of late 1965, Autonetics had: over 800,000 semiconductor IC's in use . . . approximately 850,000 additional IC's on order . . . over 177,000,000 IC/hours of operation.







Autonetics/Supplier Teamwork

When the decision is to "buy" rather than to "make," Autonetics works hand-in-hand with its suppliers. Considering that the system being produced may contain hundreds of thousands of parts, tight teamwork between Autonetics and suppliers becomes a critical factor in contract performance.

How the Teamwork "Worked" for Minuteman I

For Minuteman I, 13 suppliers from 10 different states were selected to participate in a components reliability-improvement program. All of the subcontractors worked within a common framework and Autonetics worked with them as a team throughout planning and production to coordinate report systems and monitor operations and progress. Proof of the soundness of this setup was the record achieved with it: Of the 25,000 parts involved, 98% of those procured for Minuteman I met or surpassed the program's specified (and unprecedented) goal of 100-to-1 reliability improvement.

How the Teamwork "Works" for Minuteman II

The team concept of Autonetics and its suppliers demonstrated so successfully on Minuteman I was adapted to procurement of microelectronic circuitry and components for Minuteman II. In cooperation with suppliers, Autonetics designed solid-state microcircuits to give Minuteman II longer range, increased payload, higher reliability, reduced logistics costs—and then worked closely with suppliers to put microcircuits into production without degrading the design goals.

Suppliers' IC Reliability Data

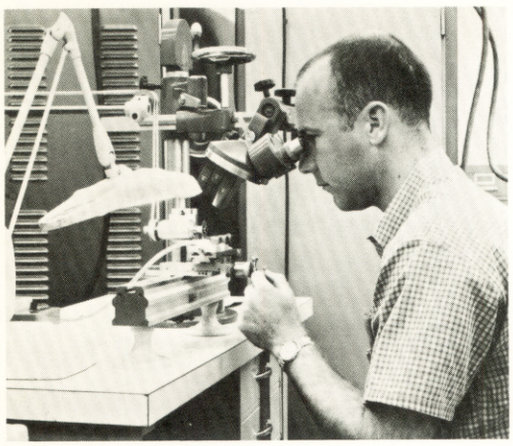
Autonetics' suppliers have accumulated (as of December 1965) more than 27,000,000 part operating hours on various types of integrated circuits. Test data from these manufacturers point to the increased inherent reliability of integrated circuits. For circuits produced in 1965, the data from one source establish an operational failure rate of 0.001 percent/1000 hours, with 90 percent confidence. Another manufacturer, by temperature step-stressing, calculates a rate less than 0.005 percent/1000 hours.

Continuing Quality Service

On Autonetics' Components Quality Assurance Program (CQAP), each supplier step-stresses his product for a selected stress—shock, temperature, vibration, etc—until it fails. The vendor then looks into his processes to see if he is inadvertently applying such failure-causing stress. If necessary, he performs corrective action. He sends samples of the failed parts to Autonetics for intensive study in Autonetics' physics-of-failure laboratories. In this way, the CQAP determines failure mechanisms so that real remedial action can be taken and maintained to assure that parts procured from suppliers continue to meet the stringent requirements specified by Autonetics for its systems components. (The methodology of the CQAP and Physics of Failure Program is described in detail in Appendix III.)

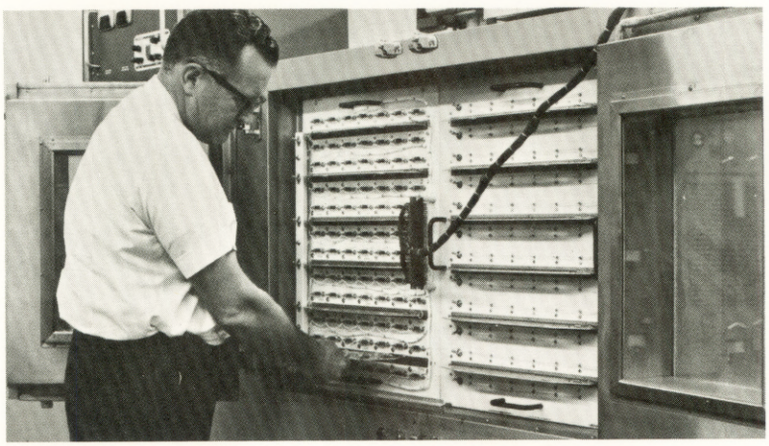
Tests of Suppliers' Components at Autonetics

Analysis of suppliers' microcircuits is performed at Autonetics by Microelectronics Engineering Section of the Advanced Electronics Department, with laboratory assistance from the Materials and Processes Laboratories of that department. Equipment is available to test the static and dynamic functions of microelectronic devices ranging from +500 C to the temperature of liquid nitrogen. In addition, the effects of vacuum, pressure, mechanical shock, vibration, thermal shock, and electrical overstress can be evaluated. Life testing can be performed under accelerated conditions to aggravate the various failure mechanisms being investigated.



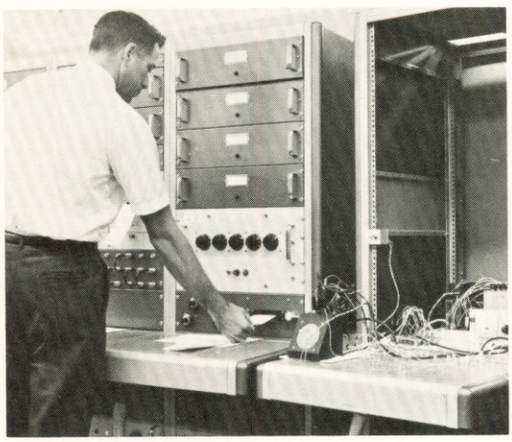
Component Decapping Lathe

A miniature lathe is used to decap suppliers' components, such as cased IC's and other microelectronic devices, to permit microscopic examination of internal construction.



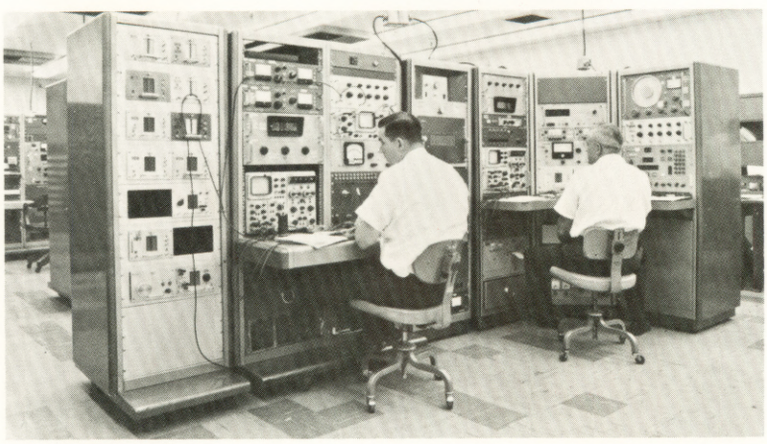
Thin-Film Device Testing

Thin-film passive devices are step-stressed for as long as 1750 hours, at various levels of power and temperature. Analysis of test results yields data on component failure modes and failure rates for use by Autonetics' microelectronic radar engineers.



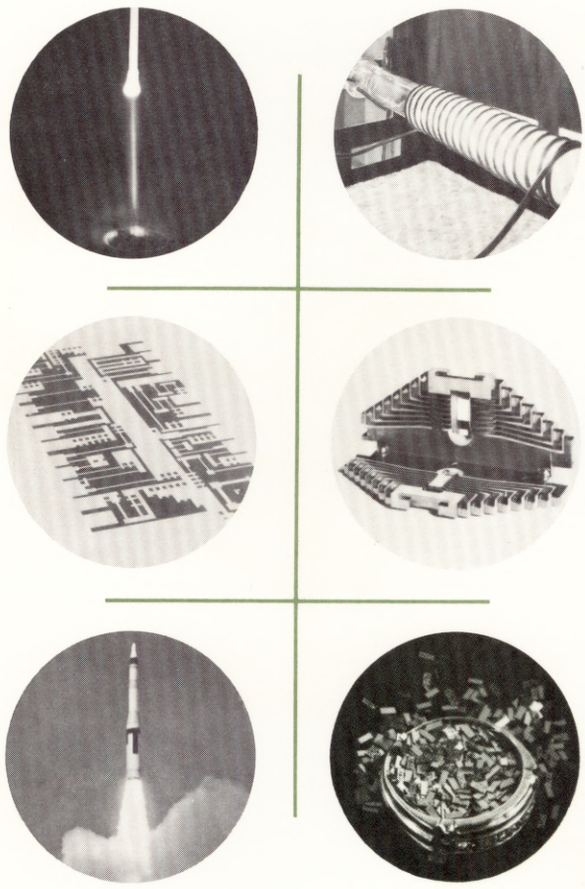
Device Evaluation for Preferred Parts List

A supplier's discrete MOS device undergoes investigation and evaluation by a punched-card-programmed automatic tester to provide engineering data for the Preferred Parts List which all Autonetics design engineers must follow.



Automated IC Tester

This automated performance test equipment for semiconductor integrated circuits is an improvement over manual testing by a factor of 40. Only 2 minutes' time is required to perform thirty separate checks on the microcircuits. Main application of the equipment is that of testing procured IC's for Minuteman II.



User...

All of Autonetics' other roles in microelectronics — researcher, developer, designer, producer, and purchaser — have as ultimate objective the role of **user in electronic and electromechanical systems.** For Autonetics is a systems company, and its *raison d'être* for fifteen years has been its service as supplier of reliable systems to our own nation and the rest of the Free World for promoting progress and maintaining defense.

Autonetics' systems talents and achievements cover a broad gamut—computers, autonavigators, radars, armament and flight controls, and ground support equipment. **All of these systems use microelectronics to assure high-calibre performance and cost-effectiveness of the programs on which they serve.**

Autonetics Systems Using Microelectronics

Autonetics has learned well the microelectronics "lessons" to be gathered from Minuteman—cost improvement, heightened reliability, space and weight reduction, and reduced requirements for power—and has applied microelectronics to enhance the value of all types of its systems. For example . . .

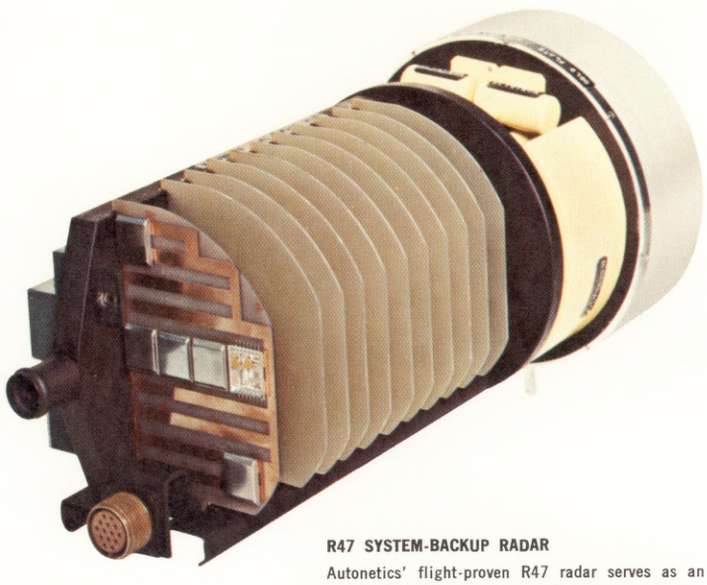
Radars

Through microelectronics and computer-assisted design, Autonetics is developing radar systems with smaller volume, lower weight, and higher reliability for space, air, and surface applications.

For space, the variety of configurations being developed include lightweight, high-reliability, cooperative rendezvous systems—as well as high-powered radars for several classified applications. The redundant-type design which microelectronics makes practical for Autonetics' space radars offers the extremely high reliability necessary for space, and also provides both the long-range search and track, and the short-range, high-accuracy performance required for space rendezvous, docking, and landing.

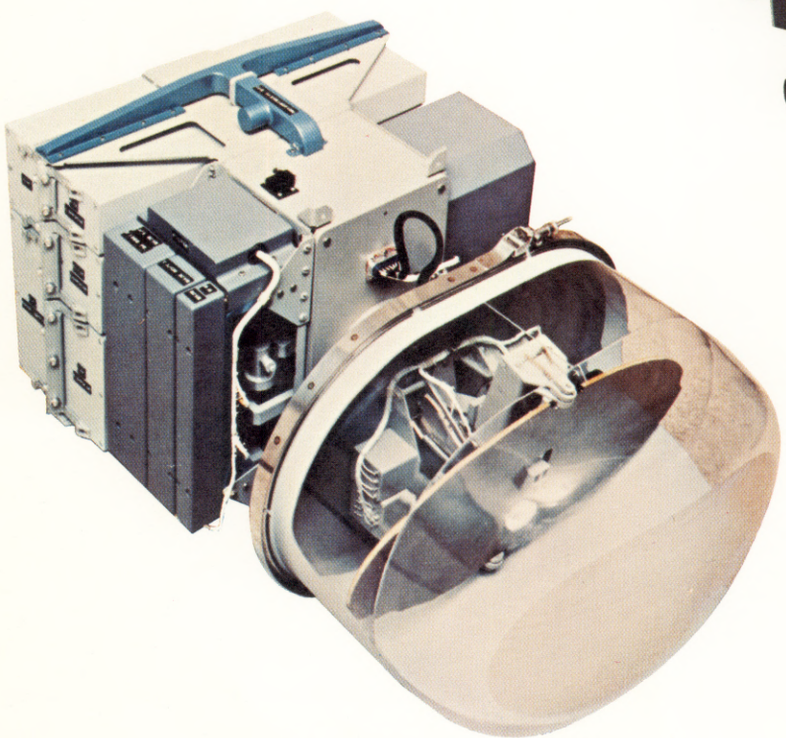
For airborne applications, modularity of Autonetics' flight-tested microelectronic radars allows system configurations to be adapted to a multiplicity of installations in both fixed- and rotary-winged aircraft, and permits their capability to be tailored to specific mission requirements.

For a highly maneuverable ground force structure, Autonetics is developing a portable microelectronic system weighing orders-of-magnitude less than contemporary systems, and providing significantly greater reliability.



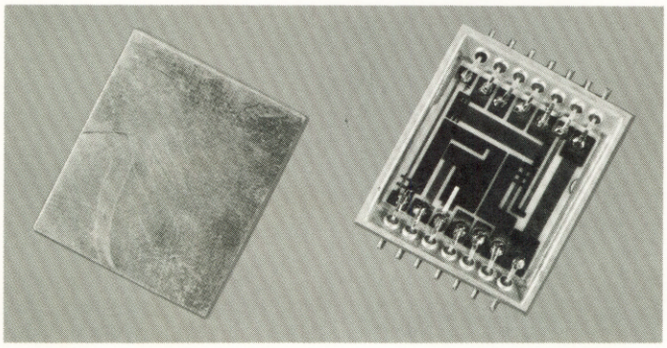
R47 SYSTEM-BACKUP RADAR

Autonetics' flight-proven R47 radar serves as an auxiliary radar to provide automatic terrain following to radar systems not having this function. Microelectronics limits R47 weight to only 24 lb, and gives failure-free operation capability in excess of 2000 hours.

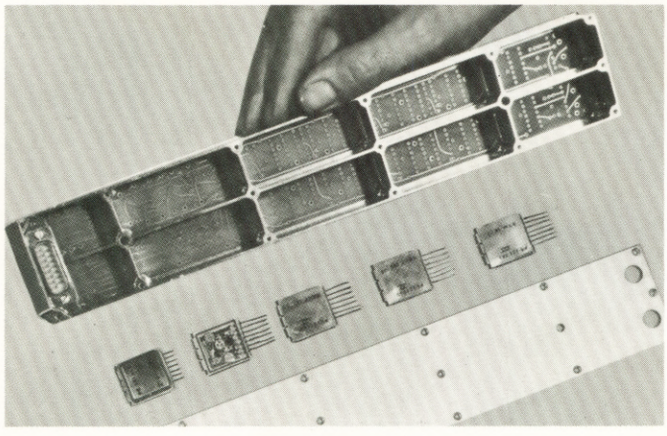


R45 MULTIMODE AIRBORNE RADAR SYSTEM

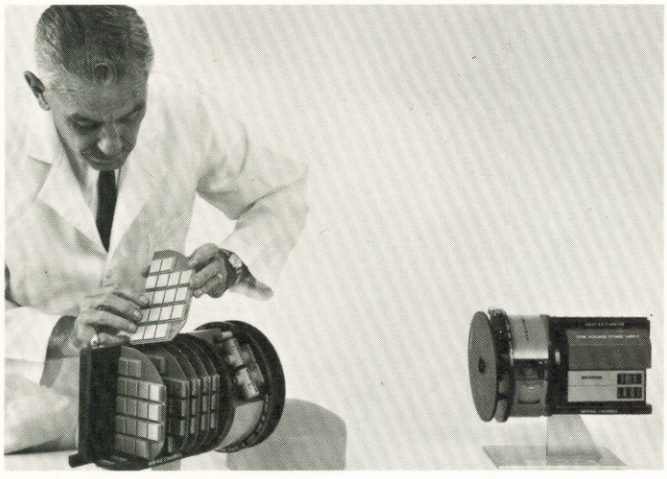
Autonetics' R45 radar system is the nation's first multimode airborne radar to employ microelectronics. The system performs the functions of ground and contour mapping; terrain avoidance; air-to-ground ranging; and air-to-air search, acquisition, and tracking. In addition, a specially designed antenna permits attainment of adequate scan rates to meet aircraft performance requirements through nominal Mach 1.2 and, thus, makes possible a mode of simultaneous automatic terrain following with ground or contour mapping. Microelectronics reduces maintenance level and logistic support needs for the system. In the flight environment, reliability of the R45 has proven to be significantly higher than that of conventional multimode radars.



LOGIC CIRCUIT FOR RADAR SYSTEMS
This microelectronic logic circuit is made by thin-film technique for both the R45 and the R47 radars.



MICROELECTRONIC RADAR RECEIVER PACKAGING
Microcircuits are edge-mounted to maintain an in-line signal flow and, at the same time, to keep the receiver's overall length limited to a reasonable value.



LOW-PROFILE THIN-FILM CIRCUITRY
Low profile of the mounted thin-film circuits for the R47 radar is clearly visible here.

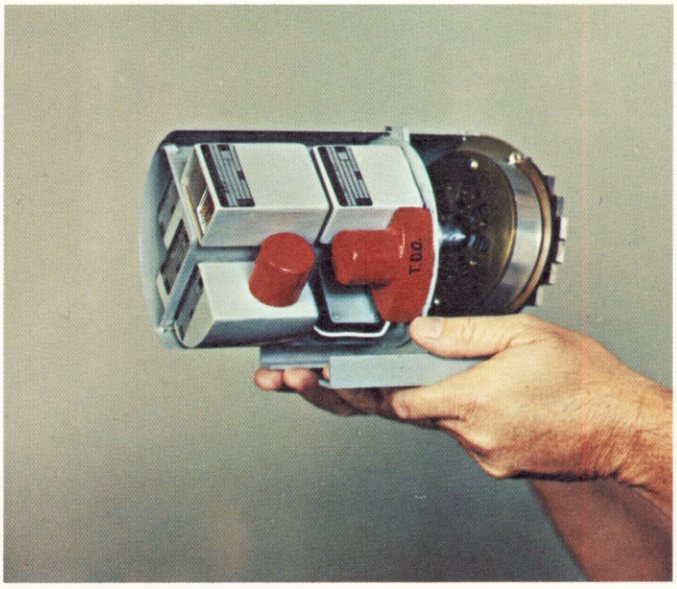
SAGS — Semiactive Guidance System

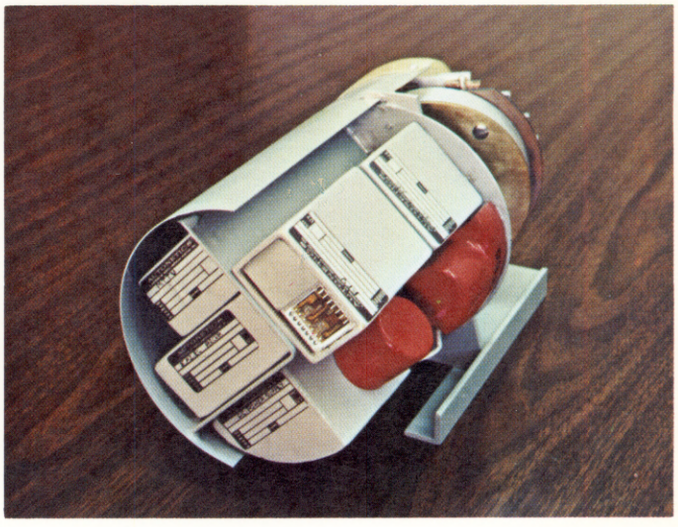
Autonetics has designed and is now testing SAGS—a semiactive guidance system based on the Doppler characteristics of moving targets.

SAGS utilizes a noncoherent, clutter-referenced, pulsed Doppler frequency technique to provide a capability for tracking moving targets in any environment, ranging from clutter-free to clutter level well above the amplitude of the radar return from the targets themselves.

In designing SAGS, Autonetics' engineers have used the latest computer techniques to establish "black box" requirements based upon actual operational environments, and to compare, evaluate, and select circuit designs for the system.

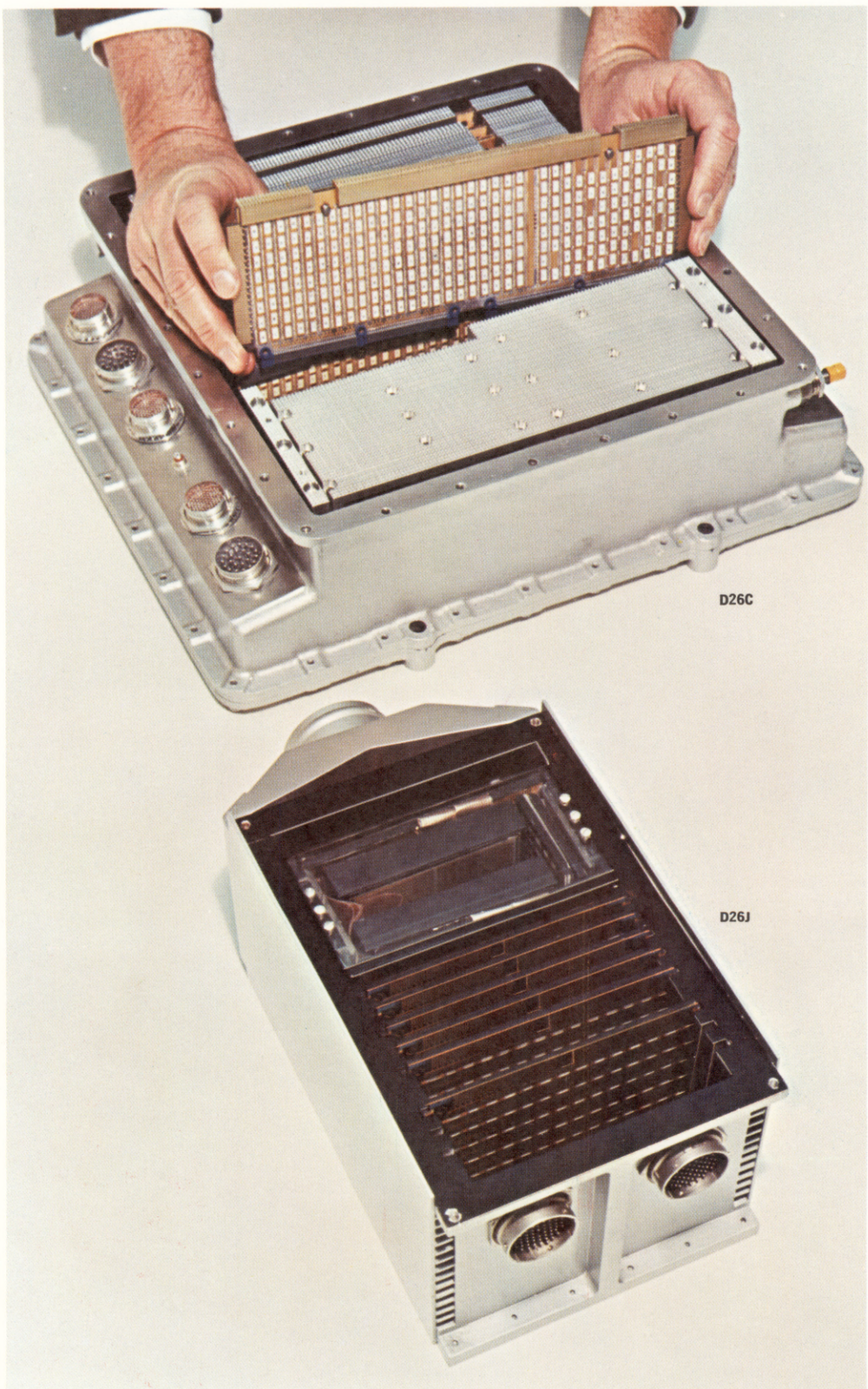
Microwave stripline and a solid-state local oscillator, along with thin-film circuitry, are used to mechanize the system. (In photographs, note thin-film device at rear of uppermost subassembly package.)





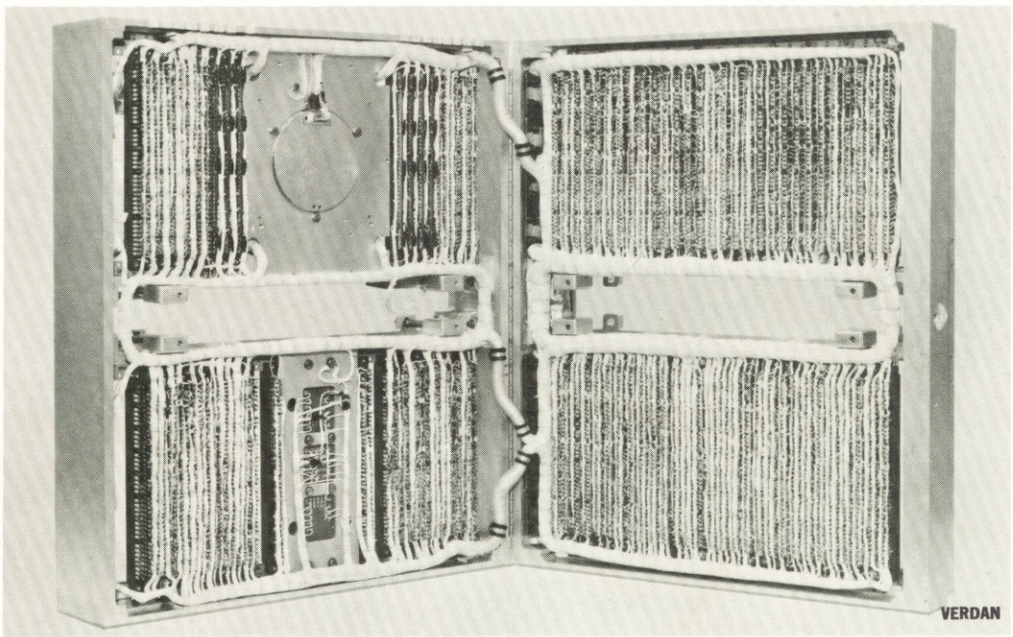
Computers

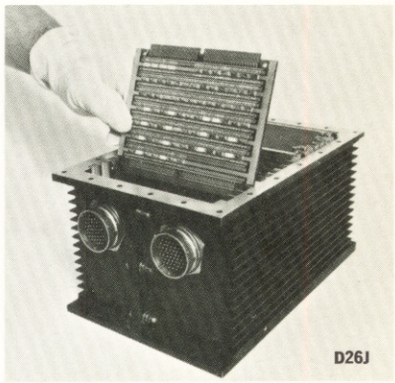
The D26 family of microminiaturized, real-time data processors is designed to fill present and future requirements for guidance, flight control, and automatic checkout systems for missiles, space vehicles, and advanced aircraft; detection systems for submarines; and command and control data-processing systems. Extensive use of integrated circuits helps make all D26 models highly reliable, lightweight, and small in volume —one version only 0.15 cubic foot overall.



The D26C (top) is designed as a central computer for advanced weapon systems. Ninety-five percent of its electronics are IC's. Also part of the computer are a rugged core memory, multilayer circuit boards, and microminiature power elements. The combination gives compact, lightweight, low-power, highly reliable computers requiring no adjustments and minimum maintenance, for airborne, ground, marine, and space applications.

Modular building-block flexibility of the D26J (bottom) provides variable word length and memory, as well as essentially unlimited input/output options. Semiconductor IC's contribute to the D26J's high reliability, low weight, and small size. Weight is only 13 lb, and volume only 0.15 cu ft.



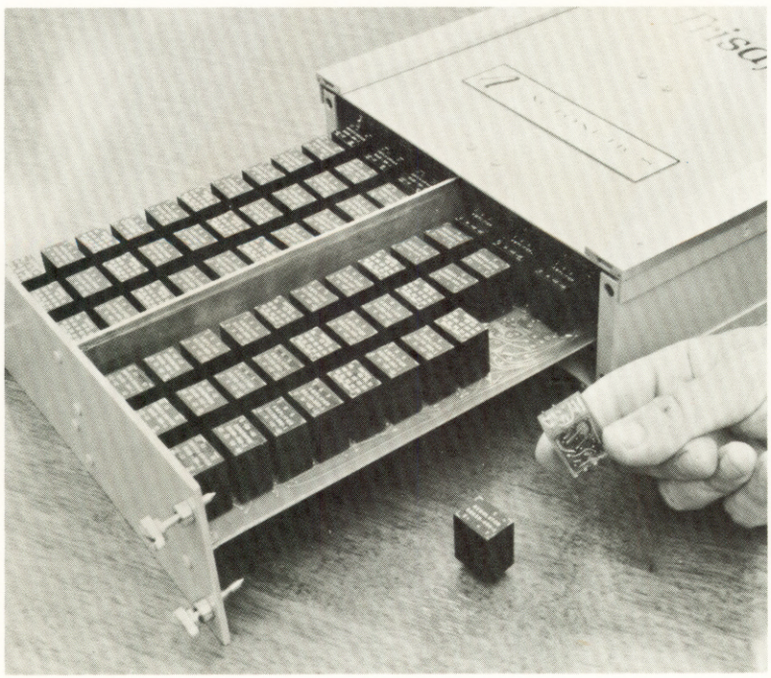


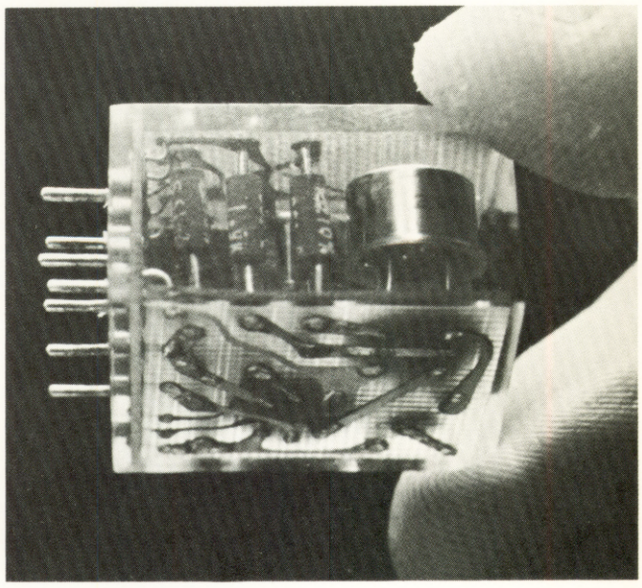
Multiple Benefits from Microelectronics

Decrease in size with microelectronics is evident by comparison of a Verdan computer utilizing discrete components, and a D26J employing IC's. Computational speed and reliability of the D26J are increased over those of Verdan by factors of 100.

Flight Control

Triply reliable because of triply redundant circuitry, is Autonetics' 9-pound automatic stability augmentation system—Trisafe. The multiple redundancy is made possible through the small size and weight of microelectronic circuits with which Trisafe is constructed. A single-axis evaluation system has been delivered to the Flight Dynamics Laboratory, Research and Technology Division, Air Force Systems Command; a three-axis system has been built on Company funds.



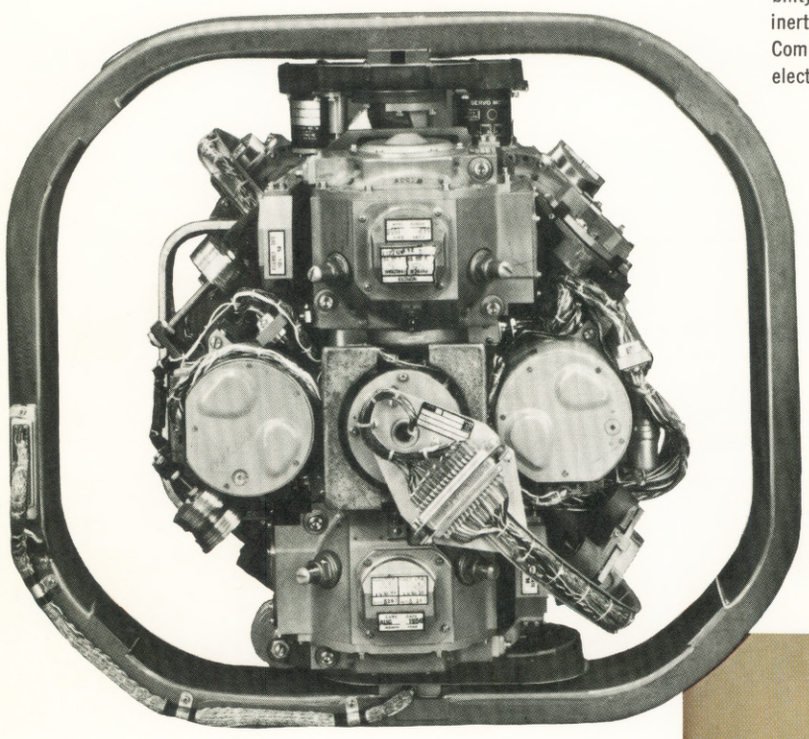


Seventy-six plug-in modules are employed in the control unit for Trisafe (left). A high-gain amplifier (above) is one of five basic types of the epoxy-encased modules. The amplifier, used 33 times, contains an integrated circuit, plus discrete resistors and capacitors.

Inertial Navigation Systems and Instruments

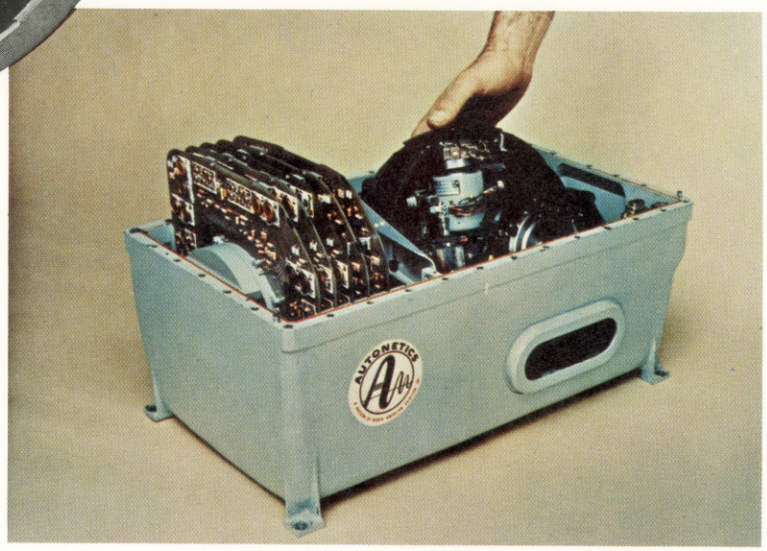
Autonetics' advanced inertial navigation systems make use of microelectronics to increase reliability, and to reduce cost, weight, volume, and power requirements. The N16 autonavigator is a compact, accurate, self-contained navigation system, designed for a wide variety of strategic, tactical, and transport aircraft. It has demonstrated excellent accuracy during tests in a highway van, in a C-131 aircraft, on a Scorsby Table at the Naval Applied Science Laboratory, and in KC-135 and T-39 aircraft. Other versions—the N16M for marine applications and the stellar-supervised N16S for extended missions—incorporate the same semiconductor integrated and ceramic printed circuits that contribute to the high accuracy and reliability of the N16.

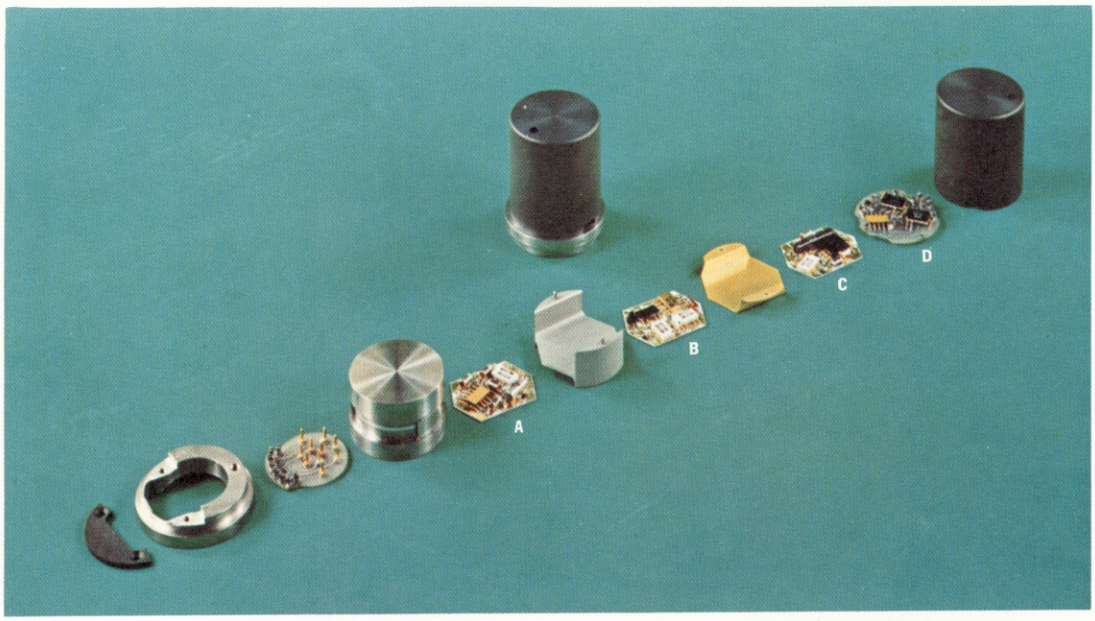
In addition to inertial and stellar-inertial navigation systems for ships, submarines, missiles and aircraft, Autonetics designs and produces alinement devices and attitude-reference systems for missile launchers, artillery orientation, land survey, aircraft, and missile-range ships. Contributing to the reliability and performance of all Autonetics navigation and guidance systems are inertial and stellar-inertial components and instruments developed by the Company—stabilizing gyroscopes, precision velocity meters, special-purpose electronic devices, and optical alinement units.

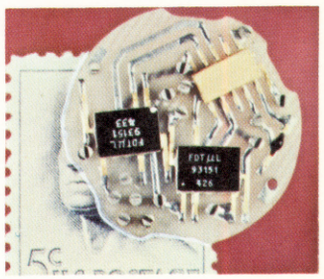


Effects of Microelectronics on Navigation Systems

The effects of microelectronics on size and weight are clearly visible in this comparison of the N5 autonavigator for the RA-5C vigilante aircraft and the AGM-28A/B Hound Dog missile, with the N16 autonavigator, Autonetics' latest generation of equipment for similar applications. Size and weight of the N16 are reduced by factors of approximately 10 and 6, and power consumption approximately 4 times, while reliability is improved ten-fold.







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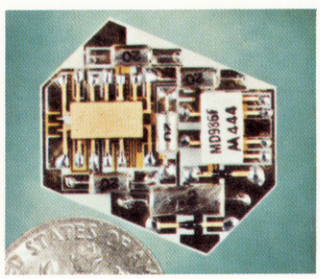

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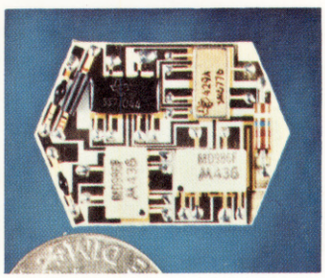

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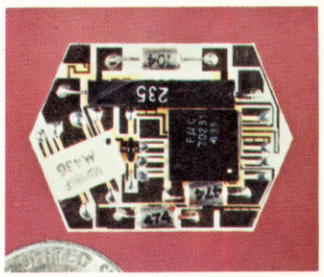

C

Electromagnetic Accelerometer

The electromagnetic accelerometer is an example of the precision inertial instruments contributing to performance and accuracy of Autonetics' navigation and guidance systems. Developed to meet system requirements for small size and low power, the 1-inch-diameter by 1.375-inch-long unit uses microelectronics throughout.

The servo and digitizer electronics which provide a digital output with respect to velocity are contained within the housing. Commercially available integrated circuits are employed where possible; for functions not available commercially, custom semiconductor integrated circuits (master dice) and commercial discrete components are used. Thin-film nichrome resistors are mounted with discrete components on ceramic substrates along with the integrated circuits, thus providing high package density and low profile.

A glimpse at the future

☐ Marvelous things have been accomplished with microelectronics, yet its potentialities are only beginning to be approached. The vigorous technology advances so constantly and so rapidly that hardly is a microelectronics technique put into use, before new techniques emerge from the laboratories to surpass it in terms of smaller size, higher reliability, and lower cost.

☐ Autonetics is an active partaker in microelectronics' progress and a confident investor in its future. An entire book could be written about the new developments being tackled in the Research Center alone, or in the Centralized Microelectronics Laboratory, the Materials and Processes Laboratories, or in any one of the product divisions. Since that much space is not available in this document, certain outstanding areas have been selected for discussion—including developments that can lead to solid-state devices for microwave applications, solid-state micromemories and displays, deposited waveguides and high-resolution conductors, microlayer boards compatible in size with the integrated circuitry they will carry, and new microelectronics packaging techniques.

Some Autonetics Breakthroughs

Single Crystals

☐ To be usable in microelectronic circuit devices, semiconductor materials must have consistent and predictable properties. One of the most stubborn obstacles to device production has been the development of a practical process for growing single-crystal* films of controlled structure, composition, and perfection on a dissimilar material.

☐ Epitaxial** growth of crystals on a substrate of the *same* material (homoepitaxy) is a technology that has existed for some time, but the capability for epitaxial growth of crystals on a *dissimilar* material (heteroepitaxy) is not widely available. At the same time, skill in heteroepitaxy is highly desirable because of the improved yields of the resulting devices, and because of the greater flexibility offered by the ability to combine in one device the electronic properties of one material with the differing properties of another.

☐ Autonetics began an intensive research program for the epitaxial growth of crystals on insulating substrates several years ago. During the ensuing period, investigations have been made of both homoepitaxial and heteroepitaxial processes, and materials studied have included ferromagnetic, antiferromagnetic, and ferroelectric substances; conductors, semiconductors, and insulators.

☐ Major emphasis in the program has been placed on the many facets of chemical vapor-deposition techniques, with complementary efforts in vacuum deposition methods, for growing single crystals. More recently, work has been initiated on glow-discharge methods for synthesizing thin films and controlling their electrical properties.

☐ Among material combinations investigated are tungsten-on-sapphire, silicon-on-silicon, silicon-on-sapphire, ferrites on magnesium oxide, yttrium iron garnet-on-magnesium oxide, barium titanate-on-magnesium oxide, gallium phosphide-on-gallium arsenide, and germanium-on-gallium arsenide. Of particular interest among these combinations are the ferrites and garnet on magnesium oxide, and silicon-on-sapphire developments; practical-device potential from these materials is enormous.

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*"*Single-crystal" describes a crystalline substance whose structural pattern on a molecular scale consists of a repeated* single *type of three-dimensional building block.*

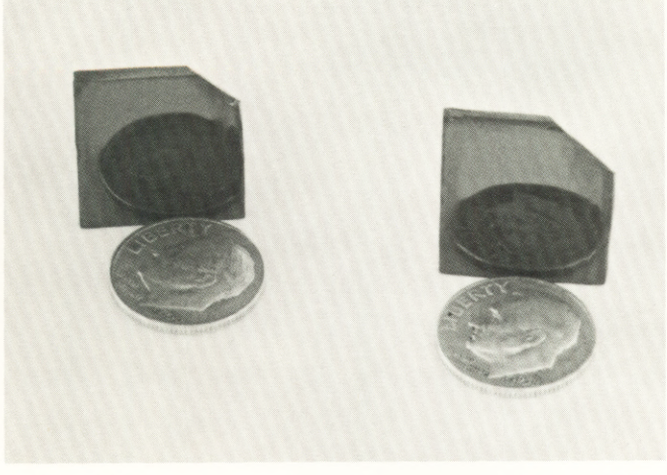
**"*Epitaxy" comes from Greek "epi" meaning "upon," and "taxis" meaning "arrange." Thus, an epitaxial growth of crystals is one which results in an arrangement of crystals upon the surface of a piece of host material. "Silicon-on-silicon" is an example of* homoepitaxy, *when host and grown materials are the same, and "silicon-on-sapphire" is an example of* heteroepitaxy, *when host and grown materials are dissimilar.*

Ferrites and YIG

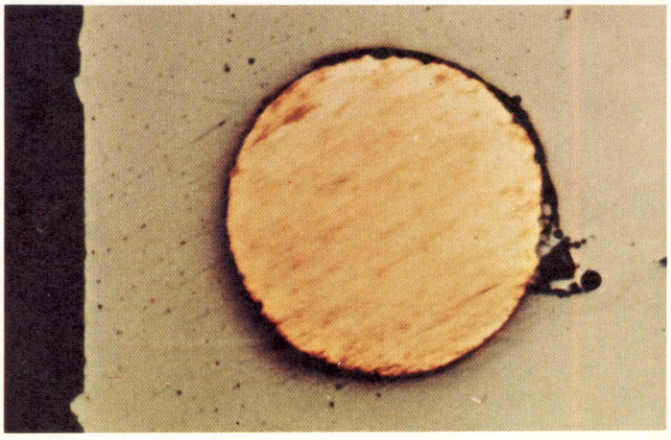
☐ Autonetics has succeeded in growing a whole family of ferrites epitaxially on magnesium oxide and, with the recent successful growth of ytrrium iron garnet (YIG) on the same substrate material, has opened up an entire new portion of the electromagnetic spectrum to solid-state microelectronics.

☐ The small geometries attainable with epitaxial ferrites and YIG especially suit them for use in microwave devices for high-power frequency conversion and harmonic generation. Since it is the lowest-loss microwave acoustical material known, YIG is particularly attractive for application in delay lines, resonators, amplifiers, and phased arrays for solid-state radar systems.

☐ Electrical properties of YIG and the ferrites have always been uniquely suitable for microwave applications, but techniques for fabricating them with the small dimensions compatible with solid-state microelectronics have been sadly lacking. Autonetics' new epitaxial growth capability for these materials changes all this—and the minimum ferrite and garnet thickness of 0.008 inch achievable with conventional manufacturing methods now appears downright monstrous, compared with the 1-micron thickness of the epitaxial films.



Epitaxial Ferrite on Magnesium Oxide Grown in Laboratory



Epitaxially Grown Single-Crystal Ferrite on Magnesium Oxide, with 50-Micron Embedded Gold Wire.

☐ YIG films' ability to rotate polarized light makes them potentially useful for displays. Their light-rotation effect also holds promise for application in extremely fast, electrically alterable, optical readout memory planes.

☐ Epitaxial ferrite can be used to make high-speed, high-density micromemories for computers. Gold conductors for forming the write and sense lines are embedded in the ferrite as described in detail on page 92.

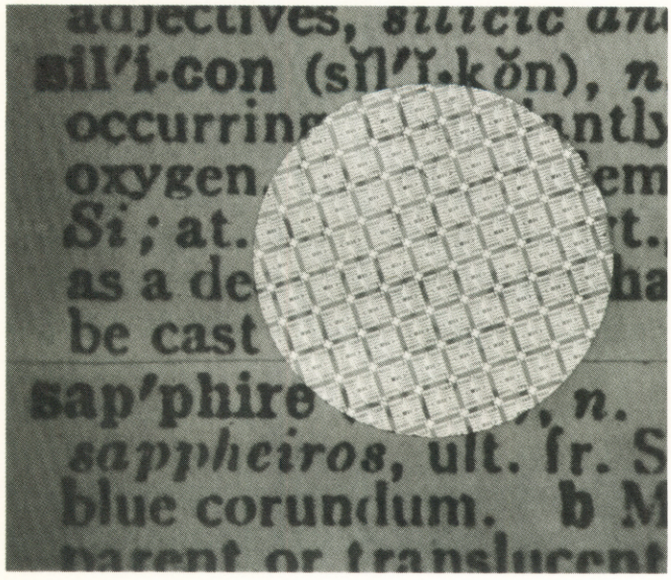
Silicon-on-Sapphire

☐ A breakthrough in its own right is the development of a controllable, repeatable process for epitaxially growing high-quality silicon crystals on a sapphire substrate. The original "pure" research that led to this Autonetics development is fanning out into a great variety of exciting new microelectronic devices.

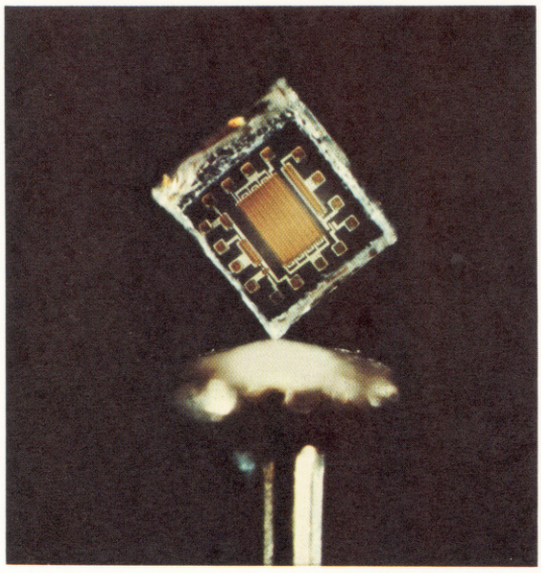
☐ Chief advantage of sapphire as a substrate lies in its much more uniform crystalline structure, in contrast to that of the commoner substrate material, silicon. Because of this uniformity, sapphire's yield of required-quality single-crystal material and, thus, the economy of producing it are much better than for silicon.

☐ Silicon-on-sapphire (SOS) is, furthermore, compatible with all other state-of-the-art microelectronics techniques; it is possible, for example, to lay down on a single slice of sapphire, all three types of device—thin-film, MOS, and "conventional" bipolar integrated circuits. A high degree of isolation is obtainable between devices, simply by etching away silicon. SOS devices are extremely radiation-resistant, and, since distributed capacitance is low, cutoff frequencies of the devices are higher than with silicon-on-silicon circuits.

☐ With SOS, solid-state devices and microcircuits can be fabricated which are unattainable with other techniques. It is possible, for instance, to fabricate extremely small-area (in the order of 1 square micron) p-n junction devices. The small diodes thus made available have storage times of less than 0.5 nanosecond (five-tenths of a thousandth of a millionth of a second)—the capability limit of the measuring equipment—and show great promise for application in large diode arrays used as high-speed, high-bit-density memories.



This 0.5-inch-diameter silicon-on-sapphire substrate accommodates 66 micropower integrated circuits with complete electrical isolation—an Autonetics breakthrough.



Putting the equivalent of a 6-transistor radio on the head of an ordinary pin is a microelectronics balancing act made possible by research achievements with silicon-on-sapphire.

☐ The thin-film character of SOS material also permits fabrication of an insulated-gate, field-effect transistor, similar in structure to the vacuum-deposited device, but employing single-crystal material. The transistor offers a high degree of electrical isolation, improved radiation tolerance, and high-frequency operation capability.

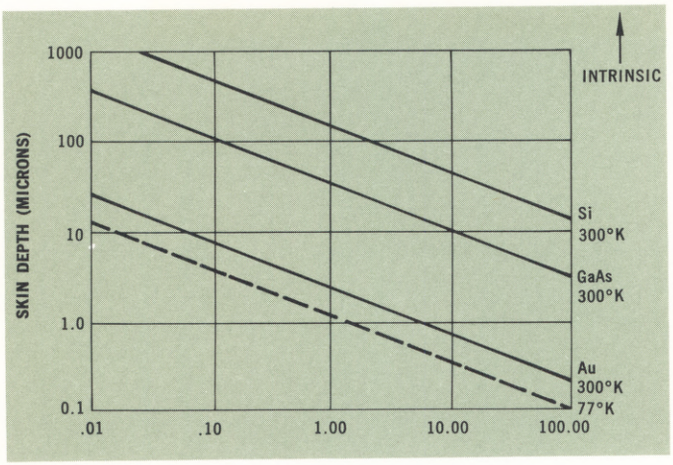
☐ The insulating properties of sapphire permit fabrication and operation of complementary metal-oxide-semiconductor devices on a common sapphire substrate, with complete absence of parasitic electrical paths or coupling between devices. Because of their proximity, the complementary devices can be cascaded or paralleled to form extremely low-power digital circuit combinations.

☐ New materials such as sapphire are expanding horizons in both device electrical performance and packaging. Whereas in the past designers have been dependent on silicon, with its often limiting thermal, strength, and dielectric properties—sapphire offers excellent dielectric and strength properties, with improved thermal properties.

Planar Annular Varactor

☐ Another door-opener to the solid-state invasion of the microwaves is the planar annular varactor—a device made possible through new know-how in the microphotolithographic art.

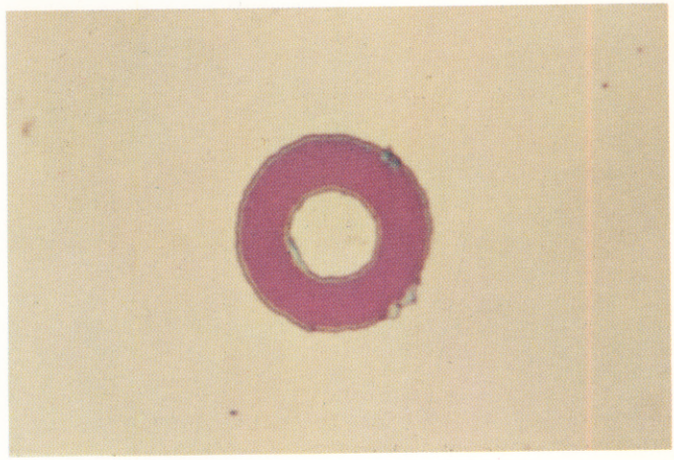
☐ In contrast to commercially available varactors with operating and cutoff frequencies of around 10 and 150 gigacycles/second, respectively, Autonetics' planar annual varactor operates well beyond 100 gigacycles/second, with cutoff occurring around 1500 gigacycles/second, and is able to amplify—distortion-free—signals as short as two millimeters in wavelength.



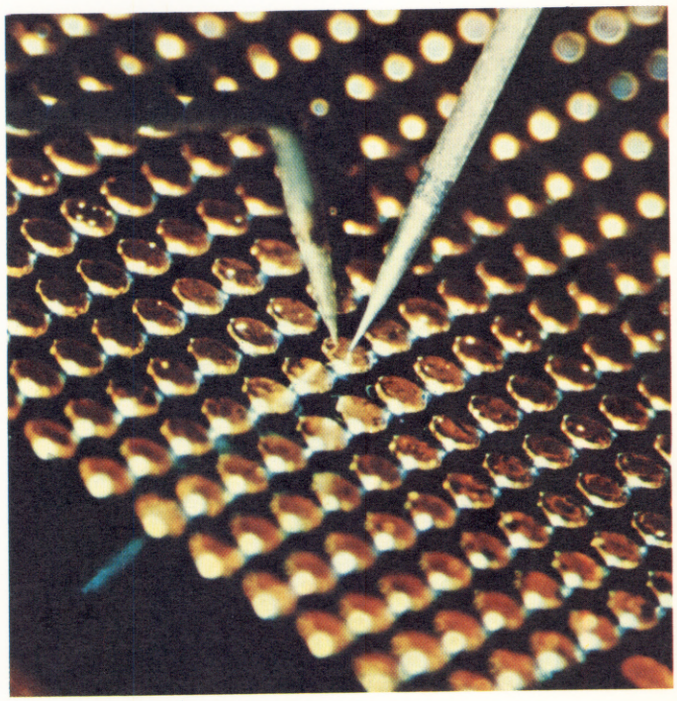
Frequency Dependence of Skin Depth

☐ Conventional semiconductor devices are locked out of the microwave part of the spectrum because of so-called "skin effect."* In these devices, the current at microwave frequencies is confined to the chip surface and never reaches the "working region" within the bulk of the semiconductor. Recent microphotolithographic refinements at Autonetics, however, permit definition of device structural details comparable to effective "skin depth" at millimeter wavelengths. In the planar annular varactor, the conduction path is only three microns — approximately six wavelengths of green light — or one hundred times less than that of conventional devices.

☐ Planar annual varactors have been fabricated at Autonetics from both silicon and gallium arsenide.



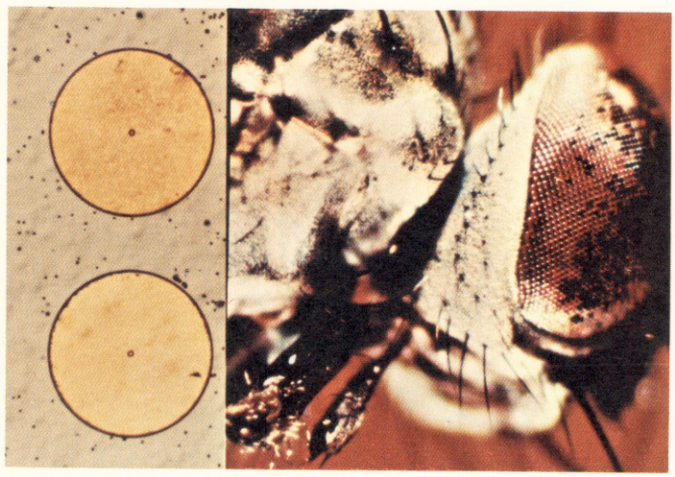
Planar Annular Varactor (Magnification 3000X)



Varactor Testing

Right-hand test probe indicates location of varactor at center of one of the gold disks in this planar annular varactor array. The two tungsten test probes (electrically etched to a diameter of 2 microns from an original diameter of 10 mils) are used to measure varactor capacitance and voltage/current characteristics.

At high frequencies, the path of electrical current flow tends to move away from the center of the conductor and toward the surface. The higher the frequency, the more pronounced is this "skin effect." Both the small dimensions and the ring shape of the planar annular varactor combat this phenomenon.

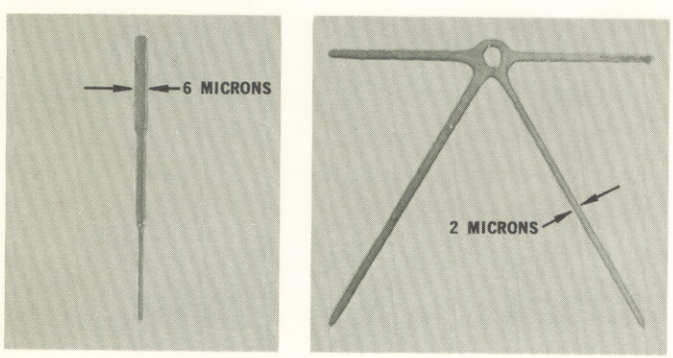


Comparison of Planar Annular Varactor with a Common Housefly's Eye

The varactors shown here could be mistaken for a fly's contact lens—except they are too little. The small rings in the centers of the circles, left, are the varactors. Right is eye of fly.

Optical Waveguide

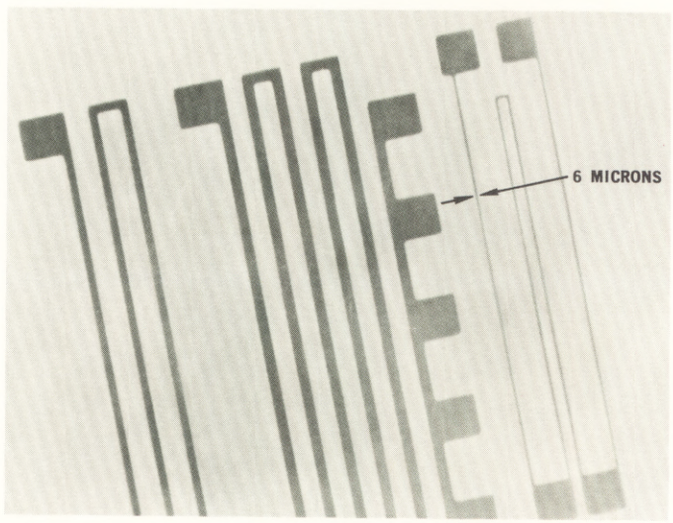
☐ A second demonstration of Autonetics' microphotolithographic sophistication is found in the achievement of optical waveguides — including such complex devices as H-plane bends, straight sections with inductive offset, and the waveguide width-transformer and "rat-race" shown below. The waveguides have been etched into silicon dioxide films thermally grown on a highly doped silicon substrate. They plainly reveal the microphotolithographic capability for accurate definition of patterns with dimensions approaching 2 microns.



Examples of Microphotolithographically Formed Optical Waveguides

Stripline

☐ One final example of the practical microphotolithographic achievements current at Autonetics is the process developed for high-resolution, metallic-deposition, thin-film conductors made by vacuum deposition through a mask. With the "old" method, it is difficult to obtain high-resolution patterns. Autonetics' microphotolithographic process defines conductor patterns with a precision equivalent to that found in monolithic integrated circuits. The photograph illustrates the definition quality of a 6-micron gold conductor with the new technique.



Example of Microphotolithographically Formed Stripline

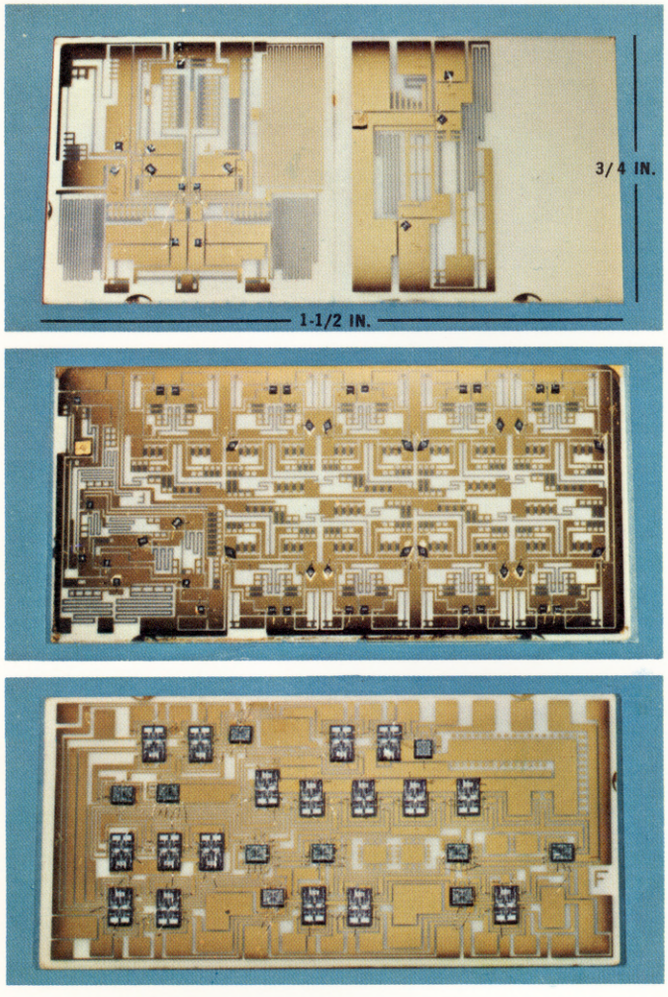
Special Devices

☐ Any glimpse at Autonetics' microelectronics future must include not only *processes* — such as the microphotolithographic process for fabricating varactors, optical waveguides, and stripline conductors; and *materials*—such as the remarkable epitaxial silicon-on-sapphire, and garnets and ferrites on magnesium oxide; but, also, special *devices*—such as the analog-to-digital converter Autonetics is now developing under contract from the Jet Propulsion Laboratory/NASA, and high-speed, high-density micromemories for microelectronic digital computers.

Analog-to-Digital Converter

☐ One-tenth the size of previous converters, a new rugged, high-speed analog-to-digital converter for NASA offers reliability and reduced cost, in addition to satisfying spacecraft requirements for ultra-small size and weight.

☐ The converter is designed to meet stringent environmental specifications, including sterilization by high-temperature cycling. It serves as a spacecraft sensor-transmitter link, by converting analog output from the sensors to digital input for the transmitter.



Three Ceramic Substrates for Autonetics' Microelectronic Analog-to-Digital Converter

Thin-film deposited conductors and microelectronic components are interconnected by registrative ultrasonic bonding. Top two substrates contain thin-film transistors and diodes for linear functions; bottom, integrated circuits for digital functions of the converter.

☐ The converter weighs less than 3 ounces and occupies only 1.2 cubic inches. It includes in its electronics a total of eighty "components"—semiconductor integrated circuits for digital functions, and thin-film passive components and discrete active components for precision linear functions. Circuitry is contained on three ceramic substrates—packaged as a unit in a hermetically sealed, encapsulated case. Leads are formed to the substrate, or from die to die, by registrative ultrasonic bonding.

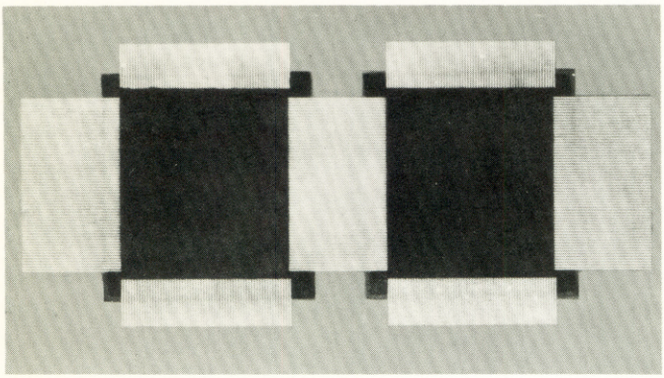
Micromemories

☐ As the computer is the brain and heart of the electromechanical control system, the memory is the brain and heart of the computer. An area of intense research and development effort at Autonetics is the area involved with microelectronic memories, or "micromemories."

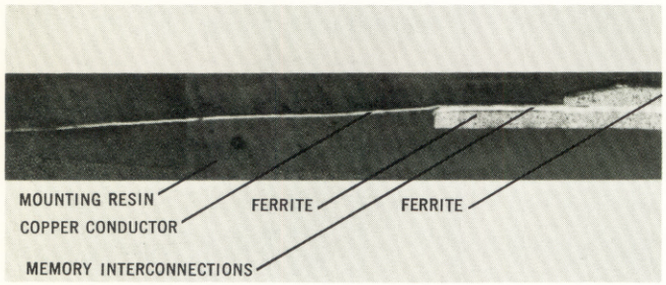
☐ Autonetics' R&D effort on memories covers a broad spectrum of approaches, including two types of ferrite nondestuctive readout (NDRO)* device: a *laminated* ferrite memory, and an *epitaxial* ferrite memory. In the *laminated* type, two mutually perpendicular layers of deposited conductors are separated by layers of insulating ferrite, with each conductor crossover constituting a memory bit. The 64-by-64-conductor matrix has 4096 crossovers, or a bit density of 4096 bits per square inch. Advantages of this type of memory are its low current requirements, its high speed of operation, its ability to operate in the NDRO mode, and the fact that it can be batch-fabricated at low cost.

☐ The *epitaxial* ferrite memory makes use of Autonetics' unique method for growing a layer of single-crystal material on a substrate of dissimilar material.

**When a memory is said to be a "nondestructive readout" type, it simply means that the same bit of information can be taken from the memory again and again, and yet, like Baukis and Philemon's unemptyable magic pitcher, the memory will always be "full" the next time. When a bit of information is taken from a "destructive readout" memory, however, that information is gone forever and never to be recalled unless it is rewritten (as it normally is).*



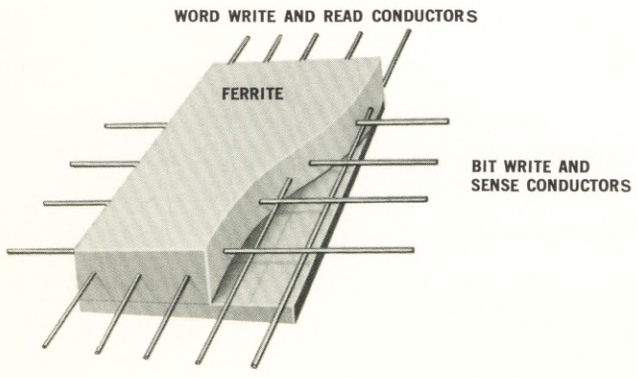
Laminated Ferrite Micromemory



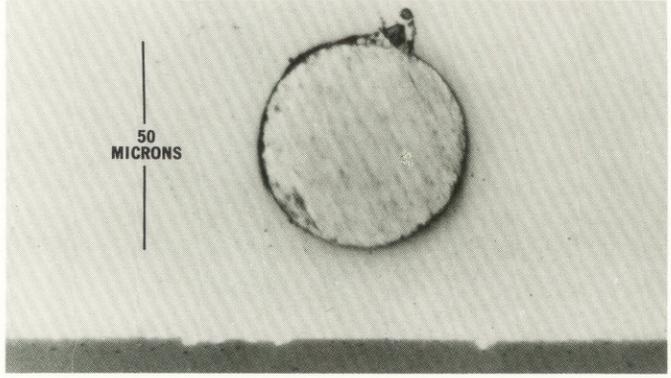
Cross Section of Layer of Laminated Ferrite Micromemory

To fabricate the memory, a single-crystal ferrite is epitaxially grown upon a substrate and surrounding a vacuum-deposited conductor array (see picture at lower right, below). Two mutually perpendicular sets of the ferrite-encased conductors form the memory; as in the laminated memory described above, each crossover constitutes a bit location. With the epitaxial technique, it is possible to have as many as 10,000 conductor intersections—and, thus, memory bits—per square inch. Furthermore, due to the magnetic properties of the ferrite, each intersection has the potential capability for storing *two* bits, thus effectively doubling the memory capacity to 20,000 bits per square inch!

☐ Another interesting NDRO approach is Autonetics' silicon-on-sapphire diode array memory; unique SOS technology developments make this device particularly attractive for program and constant data-storage. The memory is fabricated by laying down on sapphire a matrix of silicon diodes, conductors, and interconnection paths—one path for each diode. To enter information into the memory, the path is broken to open up a diode. Once opened, the path cannot be reclosed, and the memory is, thus, a permanent one. It is probably the cheapest memory possible to build—cheap enough, in fact, to be a "throwaway item" in case of failure "in the field." Another money-saving, as well as space-saving, feature is the ability to include most of the selection logic in the array itself—using diodes already present for writing-in the address, as well as the information.



Epitaxial Ferrite Micromemory



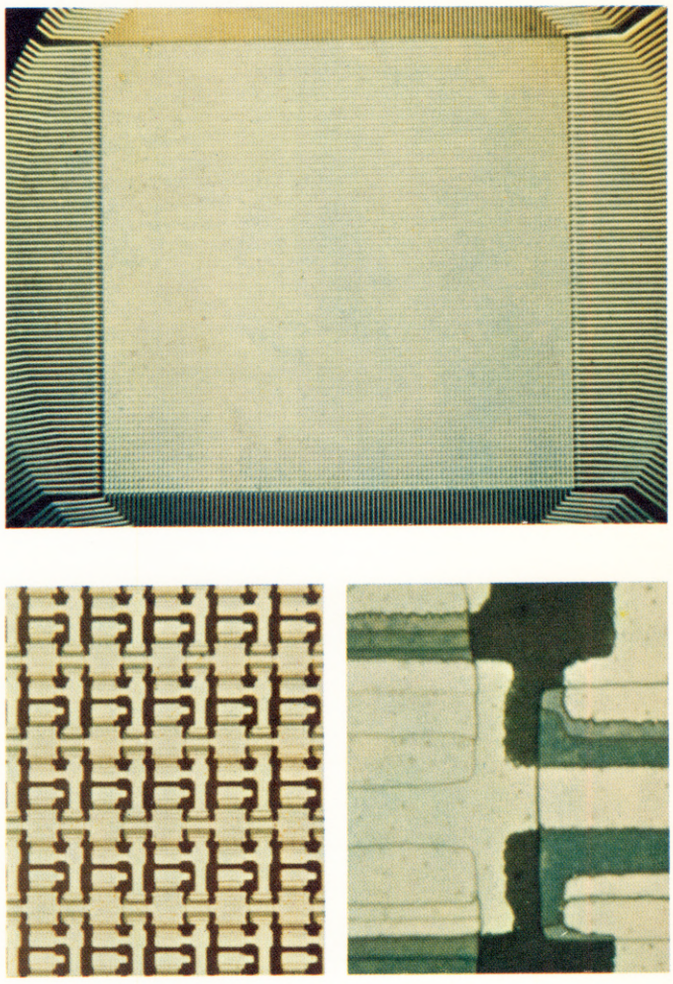
Encapsulated Gold Conductor Wire in Single-Crystal Ferrite-on-Magnesia

☐ The diode array is laid out in 96 columns by 70 rows, with each intersection containing two diodes (one for redundancy). The redundancy of two is sufficient to give an array yield of greater than 70 percent, assuming the failure mechanism to be random over the wafer and the individual diode yield to be in the order of 99 percent. (The figure of 99 percent has been proven on the pilot line.) The diode array is sufficiently flexible that the redundancy level may be increased to any desired value, simply by having several vertical columns serve as the functional equivalent of one column.

☐ Diodes in the array are initially tested to determine whether electrical characteristics are satisfactory, and all diodes are then connected to the vertical and horizontal lines by standard metallization. Data on distribution of bad diodes in the array, information to be stored, and organization of the memory are fed into a computer which generates a 20-times-size film mask. This large mask is photographically reduced to produce a 2-times-size glass mask, which is then used to disconnect the unwanted diode at each intersection of the array. Several other variations of producing a custom mask per wafer (e.g., a fuse in each path) are also being investigated to determine optimum approach in terms of cost and reliability, but the method described here has been proven and its cost is low.

☐ Still another micromemory being researched by Autonetics' scientists employs a matrix of complementary MOS devices operating as bistable digital circuits (flip-flops). This memory requires very low power and has the potential for extremely high bit density.

☐ Proven ability to produce silicon-on-sapphire device arrays can be expanded from memories to other computer electronics. The concept of a "computer on a slice" is rapidly approaching realization.



Diode Array Memory

The diode array shown at top is only about 7/16 inch on a side, but contains 13,440 thin-film diodes to make up a silicon-on-sapphire fixed-memory plane. Magnifications reveal details of the individual diodes.

Interconnection and Packaging

☐ The most excellently performing, reliable microelectronic circuits and devices are of no avail if they cannot be interconnected into modules, subsystems, and systems—*and used*. A prime area of research and development at Autonetics is, thus, concerned with devising new and improved methods for interconnection, and for the closely related technology of packaging.

☐ Elsewhere in this book is related the story of how, on the Minuteman Program, Autonetics answered

the problem of interconnecting large quantities of semiconductor integrated circuits on *single-layer* (conventional back-and-front-wired) boards, by going into three dimensions and developing *multilayer* boards.

☐ Microelectronic devices are constantly changing, however—in complexity, in function, in requirements for connections to the outside world, and in physical dimensions and configuration — and the means of device intraconnection and interconnection must change, too.

☐ Among the techniques and processes now being evaluated by Autonetics are improved multilayer and "microlayer" boards, and new methods of microelectronics joining, sealing, and protection.

Interconnection Boards

☐ Recapping the past evolution of multilayer boards (MLB's), and adding to it the new techniques now being developed in Autonetics' laboratories, we come up with the following chronological sequence:

1960 Contoured, 13-layer master interconnection board was developed for Minuteman's D17 computer.

1962 Laminated epoxy glass MLB was first put into an actual Autonetics specification. These 10-layer MLB's, and master interconnection boards to accommodate them, were first used on the Minuteman II Program.

1963 Ceramic MLB development was begun in late 1963. Laboratory samples of these radiation-resistant boards were fabricated.

1964 (a) Development was begun in early 1964 of photosensitive epoxy MLB's. Laboratory samples were fabricated.

(b) Development of microminiature MLB's began in early 1964 with units employing aluminum conductors and anodized aluminum insulation. Laboratory samples were fabricated.

(c) Around mid-1964, development was undertaken of boards that could justifiably be called "microlayer." These boards are composed of alternate layers of thin-film deposited gold conductors interleaved with silicon monoxide glass insulation. Their dimensions are truly compatible with those of the active devices they are designed to carry. "Vital statistics" of the microlayer boards are:

Thickness of conducting layers—approximately 2 microns (about 4 wavelengths of green light)

Thickness of insulation—approximately 2 microns

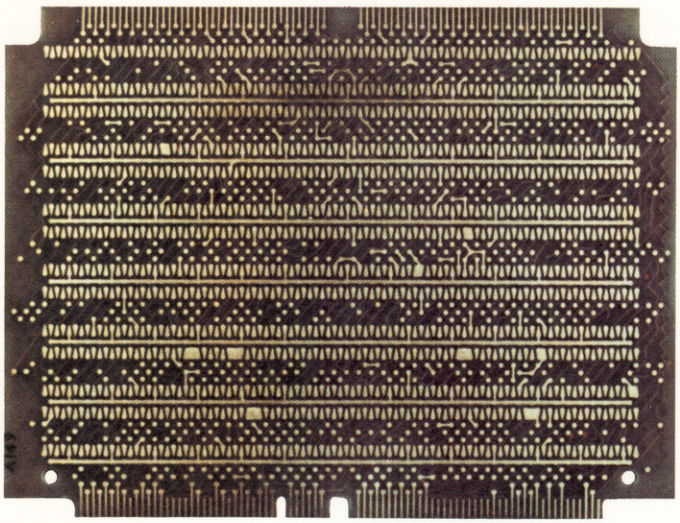
Conducting line widths—approximately 2 mils

Separation between conducting lines—approximately 2 mils

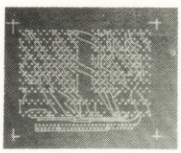
As of late 1965, the silicon monoxide microlayer board was in an advanced stage of development.

1965 Development of screened epoxy, additively plated MLB's was begun in early 1965. These economical-to-fabricate boards are designed for application in operational systems.

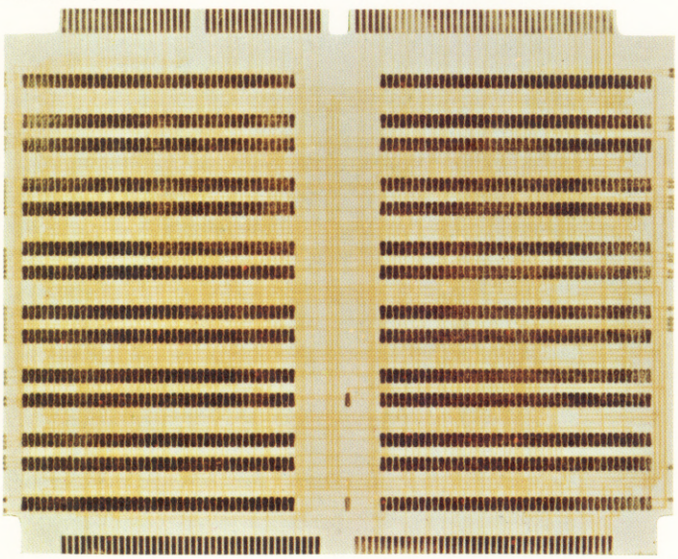
Interconnection Board Evolution



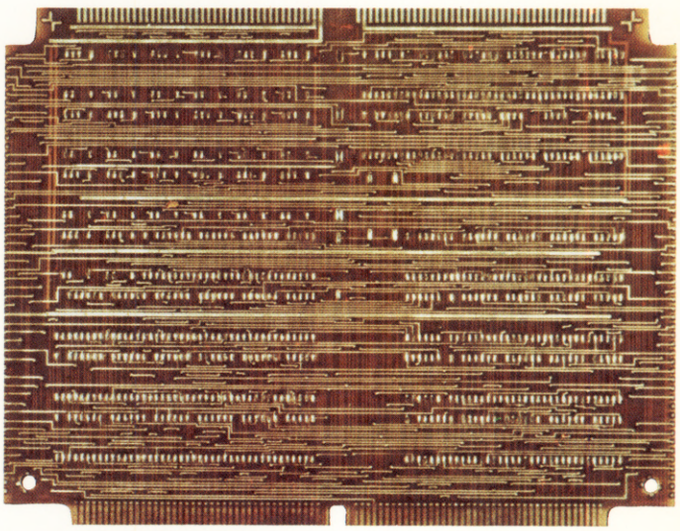
Laminated epoxy glass



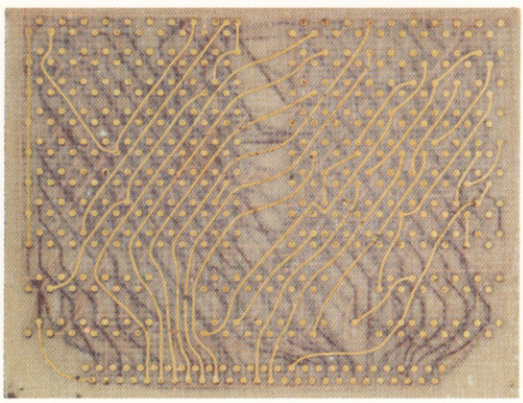
Aluminum/anodized aluminum



Ceramic



Screened epoxy, additively plated



Photosensitive epoxy

Related Research and Development

☐ Along with advanced interconnection-board developments, Autonetics is investigating new ways for using high-energy beams (electron and laser) for microelectronics joining, scribing, machining, and isolating. Photocuring epoxies for producing dielectric films for microlayer boards, and new encapsulation materials and protective coatings for hermetic sealing, are also being studied.

Conclusion...

Actually, our book—"The Story of Microelectronics"—has no conclusion, for the tale it tells is an endless and continuing one. Each day that passes brings new breakthroughs, new wonders—in processes, materials, devices, and applications. It is to be hoped that the chapters presented here as part of the continuing microelectronics saga will contribute to better understanding of, and more ready familiarity with, the future marvels yet to evolve from present-day technology.

Appendix I

HOW SEMICONDUCTORS AND SEMICONDUCTOR DEVICES "WORK"

by

M. S. Parks

Semiconductors

The electrons in a "conductor" such as an ordinary copper wire are free to move from atom to atom and form an electrical current. A "semiconductor" material, on the other hand, at room temperature normally has only a small number of free electrons, but, if slight amounts of certain other materials are intermixed with the semiconductor, the atoms of these "impurities" or "dopants" can provide the free (mobile) current carriers to make the semiconductor act like a conductor.

Impurities which *contribute* free electrons to semiconductors are called "n-type" impurities ("n" for the "negative" charge of the electron), and semiconductors doped with such electron *donors* are called "n-type" semiconductors. Operation of the other category of semiconductor—the "p-type"—depends on the addition of materials whose atoms *accept* electrons from the semiconductor atoms, resulting in the *absence* of electrons (the absence is called a "hole") from the semiconductor atoms. Each hole can be considered as having a charge opposite in sign to that of the missing electron or, in other words, positive—and the "p" in "p-type" stands for "positive." Holes can flow from atom to atom in a block of p-type semiconductor, just as electrons do in a block of n-type semiconductor, and moving holes can also be said to constitute a current, but of opposite direction from the flow of an electron current.

In order for a semiconductor to be usable as a device in an electronic circuit, its electrical characteristics must be predictable; thus, the amounts and types of impurities with which it is doped must be precisely controlled.

Common n-type impurities are phosphorus, antimony, and arsenic. Common p-type impurities are boron, aluminum, and gallium.

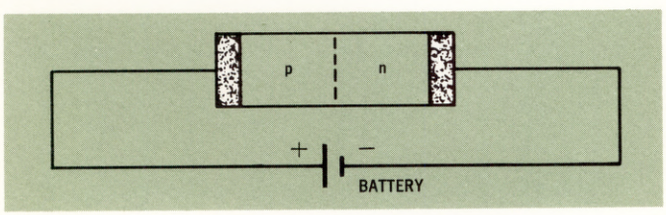
Semiconductor devices

Junction devices

P- and n-type sections of semiconductor materials can be combined to form active electronic circuit devices—diodes and transistors. Operation of these devices depends upon the behavior of holes and electrons about and across the p-n junction, and the diodes are thus called "p-n" diodes, while the transistors are called "p-n-p" or "n-p-n," depending on the physical arrangement of the materials of which the devices are fabricated.

Diodes and rectification

To help us understand the operation of such devices, we can consider the accompanying diagram of a p-n junction diode.



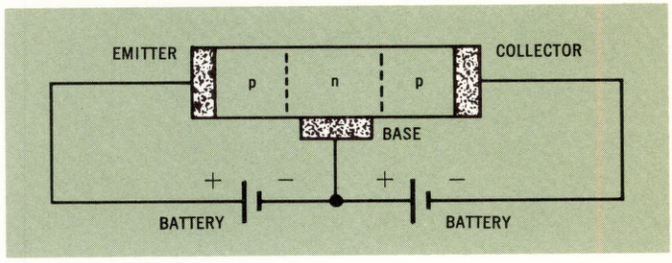
P-n junction diode

The diode shown here is made from a slab of n silicon, one-half of which has been diffused with p-type impurities. When a battery is connected to the diode in such a way that the p portion of the semiconductor is biased positively, and the n portion is biased negatively, then the p-type attracts electrons from the n-type, and the n-type attracts holes from the p-type—and the resulting movements of holes and electrons make up flows of current. If the battery is connected so that the diode is biased in the other direction, essentially no current will flow. Now, if instead of alternately connecting a battery first one way and then the other, we apply an alternating voltage to the device, it will first conduct current, and then not conduct current, as the polarity of the applied signal changes with each half cycle. In other words, the semiconductor combination acts as a "rectifier"—a one-way valve for current flow.

Performance of semiconductor devices as "amplifiers" is somewhat more complicated.

Transistors and amplification

Take, for purposes of explanation, the p-n-p transistor diagrammed below. With the two batteries connected as shown, the left-hand p section is biased positively with respect to the central n section, and the right-hand p section is biased negatively with respect to the central n section. Both hole and electron currents are encouraged to flow between the left and central sections, but between the right and central sections the effective impedance to any current flow is extremely high.



P-n-p junction transistor

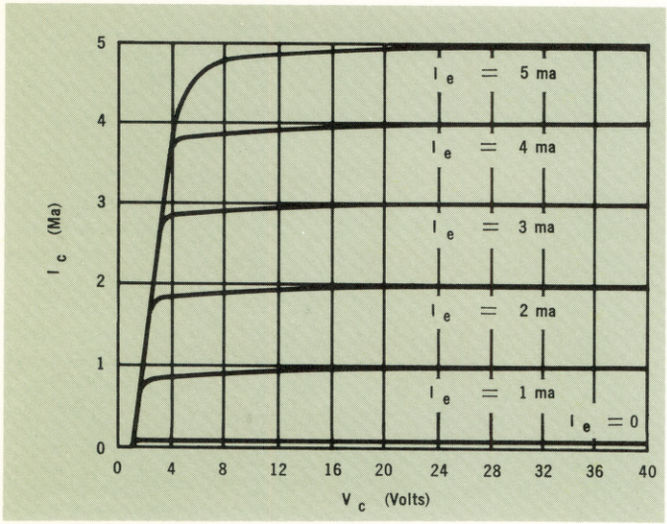
For ease of discussion, let us now refer to the various sections of the transistor as they are labeled in the diagram—emitter, base, and collector.

When the p-n-p transistor is biased as shown here, the emitter is said to be biased in the "forward" direction with respect to the base, and the collector is said to be biased in the "reverse" direction with respect to the base. Unless so biased, this transistor will not operate efficiently as an amplifier. With no voltage applied to any of the transistor elements, no current—either hole or electron—flows. With the emitter biased as shown, however, holes move into the base region as they do in the simple diode discussed above, and these "injected" holes tend to progress further into the base region as a result of mutual repulsion (diffusion forces). If the base region is thin enough, the holes reach the collector junction, from which they are then attracted into the negatively biased collector.

If an alternating signal is superimposed on the emitter bias, the flow of holes through the transistor is modulated, and a

load resistor can be connected between collector and base for development of a similarly modulated output voltage. Since the output impedance to current flow is higher than the input impedance, the output voltage is a magnification of the input signal on the emitter.

It is helpful in understanding the amplification action of a transistor to examine a set of transistor collector characteristic curves. In the next diagram, the collector current I_c of an actual transistor is plotted for a number of values of collector bias voltage V_c, for the particular form of connection shown in the previous diagram of a junction transistor – the common-base connection.



Common-base transistor collector characteristic. Collector current I_c is plotted vs collector voltage V_c for various values of emitter current I_e.

Collector output impedance can be defined as the change in collector voltage due to a change in collector current with the emitter current constant. Similarly, the emitter (input) impedance is defined as the change in emitter voltage due to a change in emitter current, with collector current constant. Emitter impedance is very low for the transistor considered here–only about 100 ohms–because the emitter is biased in a forward direction, and large emitter current changes thus result from small signal voltage changes.

Since voltage amplification is equal to the ratio of output impedance to input impedance, the voltage amplification factor of the transistor used in this way is very high.

The transistor which we have discussed here is called a "p-n-p junction" transistor, because it is composed of alternate p-, n-, and p-type materials, and because its functioning depends on the application of bias voltages across junctions between these materials. There are, also, "n-p-n junction" transistors, consisting of an n-type emitter, a p-type base, and an n-type collector, with bias polarities or directions just opposite to those for the p-n-p device. Instead of hole emission, electron emission from the n-type emitter is of importance; otherwise, the principles of the two transistor types are the same. Semiconductor junction devices that correspond functionally to tetrodes and other multi-element vacuum tubes are fabricated by varying the n- and p-type arrangement of the elements, and the relative biasing of the elements with respect to one another.

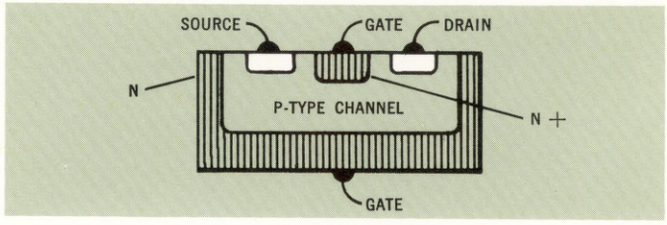
Field-effect transistors

The kind of transistor presently receiving greatest attention is the "field-effect transistor" or FET, of which there are two basic functional types–the "depletion" type and the "enhancement" type.

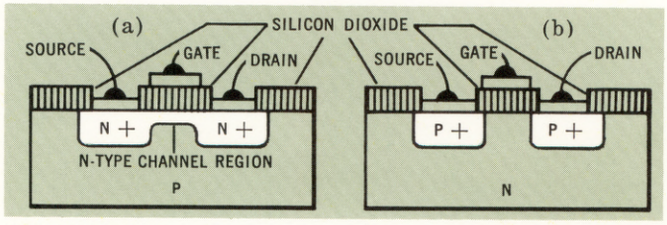
Operation of both the depletion FET and the enhancement FET depends upon current flow in a channel through a block of semiconductor material, with the current flow's magnitude being controllable by an external voltage applied to a control element of the transistor called a "gate."

In the depletion FET, the presence of a reverse-bias voltage on the gate causes an electrical field or space charge to exist in the region immediately beneath the gate. The other two elements of the transistor – "drain" and "source" – are so biased that, without the gate's reverse bias, a current would flow between them; with the gate reverse-biased, however, this current flow is inhibited. The greater the magnitude of the reverse bias on the gate, the further the space charge beneath the gate extends into the bulk of the transistor, and the less volume is left for current flow. When a signal is applied to the gate, it modulates the magnitude of the reverse bias, and, thus, modulates the effective width of the channel for greater or less current conduction.

There are two kinds of depletion FET's – junction type and MOS (metal-oxide-semiconductor). In the junction type, a p-n junction is used as the gate, while, in the MOS, the gate consists of a metal electrode separated from the semiconductor by an insulator. Like the p-n junction *depletion* type, the MOS FET *depletes* the channel of carriers when appropriate gate voltages are applied. Unlike the p-n junction device, however, MOS FET's can operate in what is called the "enhancement" mode when the gate polarity is changed.



Junction FET



MOS FET's: (a) depletion or normally "on"; (b) enhancement or normally "off"

To understand the operation of an enhancement-type transistor, let us consider a "p-channel" device.* A p-channel field-effect enhancement-type transistor consists of a block of n-type semiconductor into which are diffused two heavily doped p-type islands. The source and drain of this transistor are actually two separate diodes, with the gate spanning the region separating them. When a negative bias is applied to the gate, electrons are repelled from, and holes are attracted to, this region; if the bias is large enough, the material in this region will actually convert to p-type, and the source and drain will be separated only by a very low-impedance path. A heavy hole current then flows between the drain and the source, and, if a load resistor is connected between these two elements, a voltage proportional to the gate voltage will appear across it. If an alternating voltage is applied to the gate, an amplified version will appear across the load resistor. This type of transistor is called an *enhancement* type, because the flow of current between source and drain is *enhanced* by the gate voltage.

Probably the simplest way to think of the difference between the two basic kinds of FET's is to consider the depletion type as being a normally "on" unit, while the enhancement type is normally "off" to current flow.

Field-effect transistors are often spoken of as being "unipolar"§ in contrast to the "bipolar" character of conventional integrated circuit devices. This is due to the fact that, in junction and point-contact units, minority carriers† are injected into heavily doped regions. Since carriers of both types – holes and electrons – are involved in the process of maintaining space-charge neutrality in the injection region, the devices are said to be "bipolar." In FET's, however, current flow between input and output conists of one type of carrier only – *either* holes *or* electrons – and the size of the current, and, thus, the amplification, is controlled by changing the number of carriers of this one type. For this reason, FET's are said to be "unipolar."

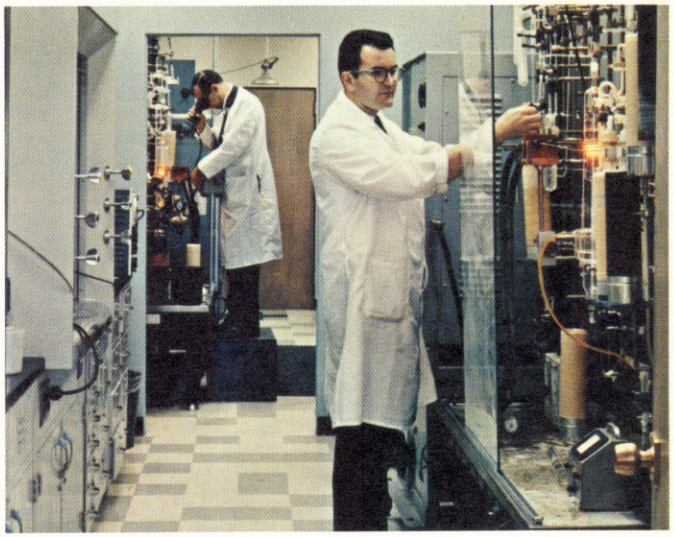
Device fabrication

Grown junctions

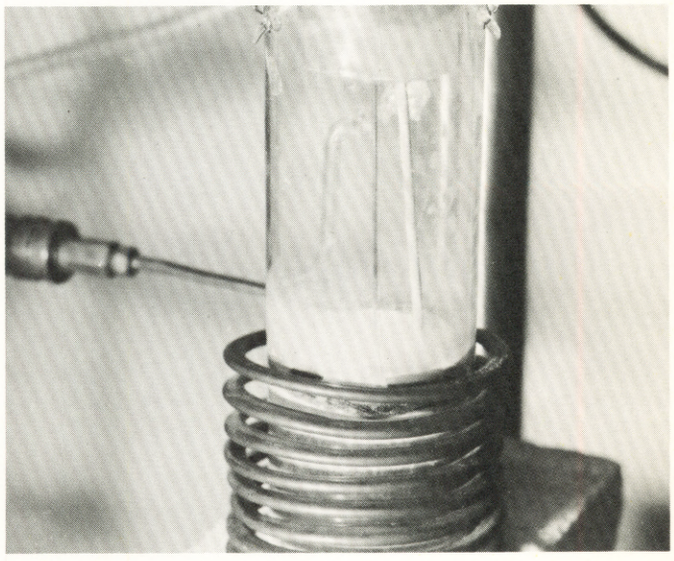
One of the greatest door-openers to present-day semiconductor technological accomplishments has been the development of methods for growing high-quality single crystals (by "single crystal" is meant a material all parts of which are arranged on a molecular scale in the same repeating three-dimensional pattern). Until controllable, repeatable, economical processes were developed for growing crystals of this quality, it was impossible to fabricate active circuit devices with predictable performance.

There are many techniques for growing crystals – including Verneuil, hydrothermal, Czochralski, Bridgman, and chemical vapor-deposition. When the crystals and the material upon which they are grown are the same, the process is called "homoepitaxy"; when the crystal and the underlying material are different, the process is called "heteroepitaxy."

One of the commonest methods of growing crystals is the Czochralski method, often called "pulling" a crystal. In this method, a crucible of purified germanium, silicon, or whatever



Crystals are grown heteroepitaxially by the chemical vapor-deposition process in this laboratory, which is a part of the Research Center, North American Aviation /Autonetics.



Close-up view of a rare earth fluoride crystal being pulled from a Czochralski melt at Autonetics' Research Center

*Although a p-channel enhancement type is described here, a similar n-type device is possible, in which conductivity types and voltages are simply interchanged from those described.

§*This terminology was proposed by W. Shockley in his article, "A Unipolar 'Field-Effect' Transistor," Proc. IRE, November 1952, pp 1365-1366.*

†*"Minority carriers" is the name given to the current-carrying media (holes or electrons) in a semiconductor material, when the carriers have the opposite type of conductivity (p or n) to that of the "host" material, e.g., p-type carriers (holes) in an n-type semiconductor. So-called "majority carriers," on the other hand, have the same kind of conductivity as the region through which they flow, e.g., n-type carriers (free electrons) in an n-type semiconductor region.*

basic material is being processed, is placed in an inert gas atmosphere and heated to the melting point. The inert atmosphere prevents oxidation and contamination of the semiconductor. With just the right temperature, a single-crystal "seed"-bearing rod, lowered into the melted material and withdrawn at just the right speed, will "pull" a crystal (i.e., cause it to grow) at the end of the seed. By carefully controlled methods of adding impurities to the basic "melt" during the growth process, the crystal can be made to consist of alternating p and n concentrations. Afterwards, the crystal can be cut into p-n junction devices as required.

Zone refining

Before it can be used for single-crystal growth, raw material such as germanium or silicon must be highly purified. A chief method for accomplishing the purification is called "zone refining." This process makes use of the fact that most impurities found in the raw materials involved have higher solubility in the molten raw materials than they do in these materials in the solid state. To purify an ingot of germanium, for example, by this process, the ingot is slowly drawn, in an inert atmosphere, through a set of r-f heating coils. As the ingot moves through the coils, the portion of its length enclosed by the coils is molten; as the ingot emerges from the coils, the emerged portion "freezes," leaving the impurities concentrated in the last end of the ingot to emerge. This process, repeated as many times as necessary, is capable of producing extremely pure semiconductor materials in the central portion of zone-refined ingots.

Rate-grown junctions

The principle employed in zone refining can be used to create p-n junctions. Removal of p-type impurities, such as gallium and indium, by zone refining, is relatively independent of the speed with which the semiconductor ingot is moved through the r-f heating coils. Thoroughness of removal of n-types, however, such as antimony, increases with increased speed (the faster the ingot moves along, the more antimony is removed). It can be seen that this process can be utilized to create junctions by modifying ingot speed to modify impurity concentration. This method requires precise control of both velocity and temperature.

Alloyed or fused junctions

Single-impurity-type ingots can be grown comparatively cheaply, and then alloyed or fused to form diodes and transistors. With this method, a sheet of metal having the same rate of expansion with temperature as the germanium or other semiconductor being processed, is covered with a layer of antimony solder, which, in turn, is covered by the germanium. Small beads of indium are held in contact with the germanium, and the whole assembly is heated to a temperature high enough for the indium and antimony solder to alloy with the germanium. The indium diffuses into the n-type germanium to form p regions – with the final product being a p-n-p transistor. Diodes can be made by this same method, only even more simply than transistors, of course. Alloyed junction transistors are not usable above megacycle frequencies, because of the control limitations of this process.

Point-contact devices

Both the cat's whisker detector in early radios and the first commercial transistor were point-contact devices. Point-contact diodes are still in use, but the transistors are largely replaced by less noisy, higher-amplification-factor diffused types. In point-contact devices, one side of a small slab of semiconductor is soldered over a broad area to a suitable base. A fine wire (the cat's whisker), sharpened at one end, is brought into contact with the other side of the semiconductor and is moved about until a spot is found that shows good rectifying properties. The cat's whisker is then welded to the semiconductor at that spot, and the device is packaged and sealed.

Diffused junctions

In the diffusion method, n- and p-type impurities are added to semiconductors either by evaporation or gaseous diffusion. In the evaporation process, a layer of donor or acceptor material is evaporated or plated onto the semiconductor surface; in the gaseous diffusion method, the semiconductor slab is placed in a furnace filled with the desired impurity or dopant in hot gaseous form. In both processes, the impurity diffuses over the surface and into the slab. Diffused regions can be developed in exactly defined areas on a semiconductor by protecting the surrounding surface with a thermally grown oxide, through which the dopant will not diffuse, leaving unprotected etched "windows" where diffusion is desired.

"Mesa" diodes are produced from the diffusion process, simply by etching the impurity away from all surfaces except small "dot" areas on the diffused slab. Transistors can be fabricated by alloying contacts of the proper impurity type onto one side of diffused-junction diodes. More often, however, device structures are made by utilizing the masking properties of oxides as mentioned above. The oxide can be removed in desired patterns by means of photosensitive coatings (called "photo resists"), exposed to light through master patterns.

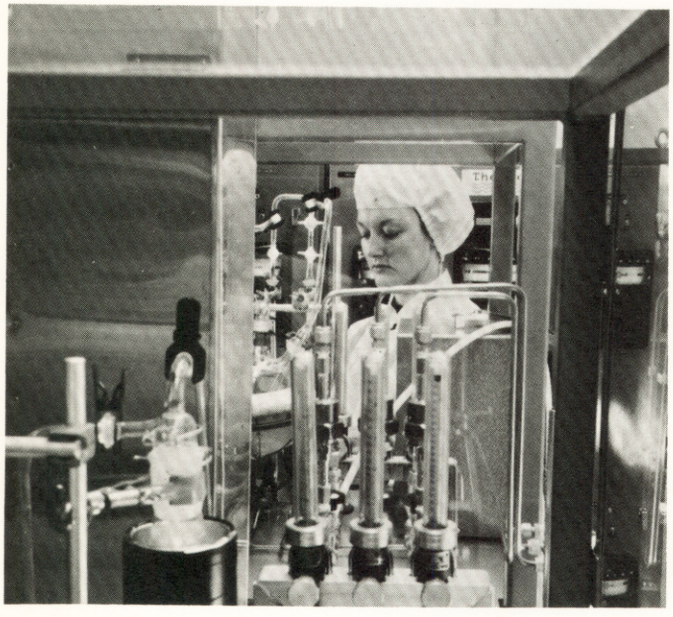
Double diffusion

Bipolar transistors are most often fabricated by a double-diffusion process. A first diffusion is used to obtain the base region, where an appropriate impurity is applied according to the desired type; phosphorus is most frequently employed for n-type, and boron for p-type regions. After the emitter region has been outlined photolithographically, a second diffusion of an opposite-type impurity is carried out. In this way, n-p-n or p-n-p structures are formed in combination with the n or p character of the original "parent" material.

Metal-oxide-semiconductor field-effect transistors

In the fabrication of metal-oxide-semiconductor field-effect transistors (MOS FET's), impurity diffusion techniques are employed, and geometry is controlled by masking and photolithography. To make a MOS FET, a lightly doped wafer of silicon is highly polished, then covered with an oxide coating by insertion into an oxidizing atmosphere. The oxide is then etched away in accordance with a pattern applied by photolithography, and the wafer is placed in a furnace containing the desired impurity in gaseous form for diffusion forming of the source and drain "diodes." To diffuse a "channel" (see page 100) into the wafer, steps of oxidation, photolithographic pattern transfer, etching, and diffusion are repeated.

Loading diffusion furnace with "boat-load" of silicon wafers



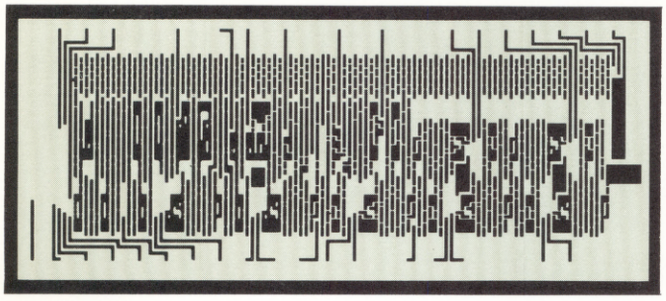
"Glass jungle"—valves, metering devices, heating elements—for mixing and distributing furnace carrier and dopant gases

Inserting a thermocouple to run furnace temperature profile

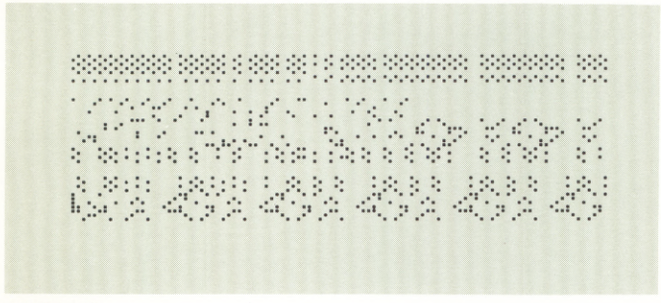
Appendix II

AUTOMATED MOS MASK PREPARATION

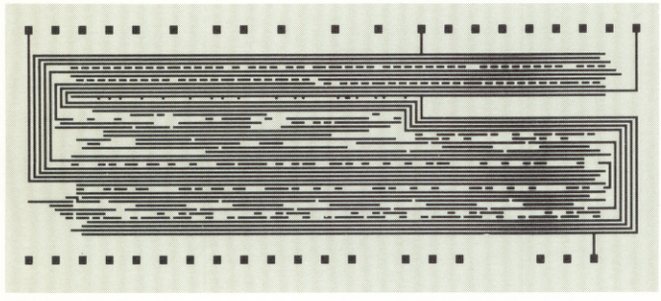
The steps involved in the transition from a rough sketch of a MOS layout to a finished optical mask are normally very laborious and usually extremely time-consuming. Such steps include preparation of an exceptionally precise scale drawing of the layout and a slow manual graph-following procedure. Thus, at a comparatively early phase of Autonetics' MOS development work, a decision was made to attempt to automate this process.



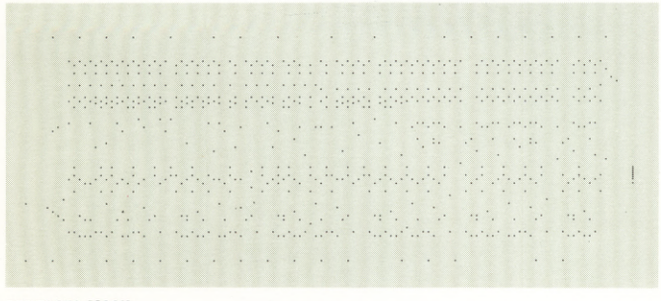
P-REGION MASK



GATES MASK



METALLIZATION MASK



CONTACTS MASK

Figure 1. Computer-Generated Masks for DDA Integrator

Masks are made many-times actual size and are photographically reduced to true circuit dimensions. Each mask is precisely alined relative to other masks, to assure correct location of diffused regions, conductors, contacts, etc. in the MOS circuitry being fabricated.

The initial result was a series of computer programs written for the Recomp III computer, which accepts as input a simplified coded description of the MOS layout, and produces as output a Flexowriter printed geometrical layout for making corrections and modifications, and a punched paper tape for driving an automated coordinatograph which produces the actual optical mask. An additional computer program generates printed listings of the X-Y coordinates for each optical exposure from the output tapes.

For a digital differential analyzer (DDA) integrator, a set of four masks and output tapes was prepared with this program. Figure 1 shows the optical masks produced by the coordinatograph for the p-region, logic gates, metallization, and contacts. The complete, bonded MOS integrator appears in Figure 2.

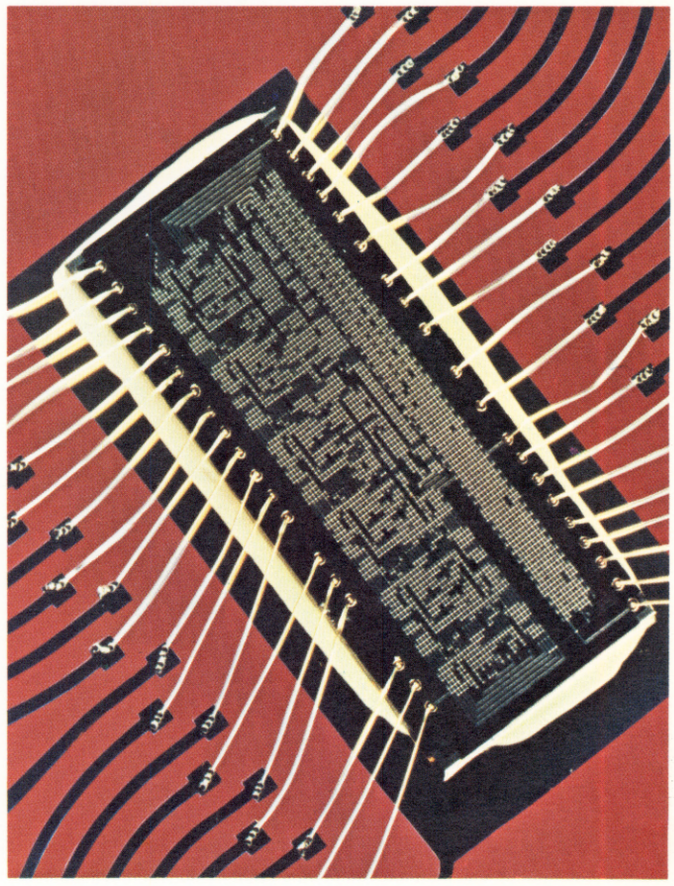


Figure 2. An Array of MOS Devices Which Mechanize a DDA Integrator (Magnification Approximately 11.5X)

To illustrate the coding technique, part of the input code for the p-region mask is presented here:

X + 000024 Y + 000030 2611111113 A 2693A2611
191316 A A A A 0419041316 A A . . .

The letter X indicates that an origin is to be set with X having the value indicated by the next six digits (000024), with the + sign ahead of these indicating the direction of the X movement. Similarly, a Y origin is set at 000030, with Y motion in the positive direction as indicated, again, by a + sign.

The layout is generated by marking off alternate areas of non-exposure and exposure in the Y direction (vertical) by means of the digit pairs following the origin coding. Thus, the digits 26 indicate 2 units (mils) of non-exposure in the positive Y direction, followed by 6 units (mils) of exposure in the positive Y direction, and similarly for the succeeding digit pairs. The letter A indicates a 1-unit (mil) advance in the positive X direction and simultaneous resetting of Y back to its origin of 000030.

For the metallization layout, two additions to the program have been found particularly useful. In the first of these, because of predominance of horizontal metallic lines, a 90-degree rotation of the coordinates is made, so that the roles of X and Y, as described by the coding, are reversed. A second improvement facilitates coding of long lines, by permitting increments greater than 9 to be coded by the letters "d" or "t" followed by a two- or three-digit number, respectively.

Experience gained from the use of the described program has initiated writing of a new improved program. The first program's use of punched paper tape for the coded inputs makes the correction process relatively inconvenient; with the new program, however, Hollerith punched-card inputs are acceptable, and corrections and modifications are much simplified. The new layout is a composite printing in which six different typing symbols represent all possible combinations of diffusions on a single sheet of paper. Letters "p," "m," and "c" identify the input codes that follow – as p-region, metallization, and contacts or gates. Also, letters "v" and "h" indicate whether the direction of propagation is vertical or horizontal. An extremely useful feature of the new program is its capability for storing and subsequently recalling a repetitive coding sequence as many times as desired. Such sequences may be contained within other sequences with as many as eight levels of nesting. Thus, patterns which recur frequently in the geometry of the layout need be coded as input only once, and thereafter may be called out by a single letter whenever and in whatever geometric orientation subsequently desired. Provision is also made for convenient alteration of the layout in the computer's internal memory just prior to printing.

A logical extension of the program for future use is the inclusion of a digital graph plotter to generate a layout more closely resembling the actual MOS configuration.

Appendix III

COMPONENTS RELIABILITY ASSURANCE

Organization, direction, purpose

Reliability efforts for Minuteman have more than paid off for that program and have yielded information of benefit to the electronic components industry in general.

For Minuteman I, all components met or surpassed the reliability goals established by the United States Air Force. The reliability of more than 98 percent of the components was increased by a factor of 100 to 1.

For Minuteman II, the same tight process controls and down-to-the-roots failure analysis were continued as had been used for Minuteman I. But the massive life testing that had been one of Minuteman I's chief reliability tools was no longer practical. To reach failure rate goals of this advanced missile, it would be necessary to test astronomically large samples of each component. On the specified schedule, there simply was not enough time.

Solution was the Component Quality Assurance Program (CQAP) carried out by Minuteman II component suppliers, as part of contract AF 04(694)-247 between Ballistic Systems Division, United States Air Force, and the Autonetics Division of North American Aviation, Inc.

Under the stipulations of the CQAP, each supplier applies high-stress testing to representative samples of his products, with the objective of producing large numbers of failures – many more than would occur in the same amount of time during "normal" use. Failures are then analyzed for cause, and components undergo corrective action to eliminate design weakness or inadequate manufacturing technique, as indicated.

The "correctiveness" of each corrective action is doubly ensured by several replicate test series, with findings from each series pointing to further correction on the components before they are subjected to the next series. A positive measure of reliability improvement is obtained from the decrease in the number of failures with each successive series.

By means of the CQAP, the supplier uncovers "failure modes" – that is, he discovers *symptoms*, such as cracks, open bonds, etc. But to identify "failure mechanisms," or *causes* of the failures requires personnel, equipment, and facilities that are often beyond his capability. To accomplish the necessary analysis-in-depth, a program complementary to the CQAP – the Physics of Failure Program – has been established at Autonetics. Under the overall direction of Ballistic Systems Division, United States Air Force, and technical monitoring of Rome Air Development Center, the two programs act together to identify underlying causes of Minuteman II component failures, and to apply timely corrective action to increase Minuteman II component reliability and to accelerate component reliability growth.

Methodology

Autonetics' Materials and Processes laboratories are among the nation's best equipped, and, in carrying out the exhaustive failure analysis and testing required in Physics of Failure studies, employ such advanced instruments and systems as the electron microprobe, gas chromatograph, mass spectrophotometer, and X-ray analyzer. Forty-five scientists, engineers, and technicians are assigned to the program, and of these 15 are PhD's.

Failed components discovered during the CQAP are sent back to Autonetics from suppliers for extensive physical, chemical, and metallurgical tests and analyses – often to the atomic level. As of late 1965, around 200,000 Minuteman II microminiature components had undergone high-stress testing on the CQAP, and resulting failures from the testing had been analyzed and corrective actions had been prescribed on Autonetics' Physics of Failure Program.

Types of devices to be investigated by the CQAP and the Physics of Failure Program were selected on the basis of their projected impact on Minuteman II reliability. An example of the charts used to compare the various devices and their failure modes, and to determine the part which each device played in Minuteman II's overall reliability is presented in Table 1. (Numerical references in the table are not actual values, but do serve to demonstrate the method used.) Components tested and analyzed have included signal and power transistors, computer and power diodes, ceramic and both solid and liquid tantalum capacitors, metal-film and wire-wound resistors, and semiconductor integrated circuits.

Table 2 summarizes Physics of Failure Program analyses of failure modes/mechanisms and corrective actions for Minuteman II semiconductor integrated circuits. The data in Table 2 are indicative of the thoroughness of the chemical, metallurgical, and physical analyses which components must undergo on the Physics of Failure Program. The test regimen for other components is equally as rigorous.

Several case histories of Physics of Failure Program investigations follow Table 2. These cases are, because of space limitations, greatly simplified, and are included here only to indicate the breadth and depth of Physics of Failure analyses.

Table 1. Systems Impact vs Failure Modes for Minuteman CQAP Devices

FAILURE MODES		OPEN INTERCONNECT	PREFORM INTERFACE FAILURE	DIELECTRIC BREAKDOWN	TANTALUM CRYSTALLIZATION	CRACKED SILICON DIE	BOND OFF INTERCONNECT	WIRE OFF POST OR LEAD	UNSTABLE RESISTOR WIRE	PLASTIC PACKAGE FAILURE	INVERSION LAYER FORMATION	CURRENT CONCENTRATION	CONTAMINATION INDUCED FAILURE	PACKAGE HERMETICITY FAILURE	BROKEN RESISTOR WIRE	SHORTED RESISTOR TURNS	Δ FR
TRANSISTOR I		5	10	X	X	20	5	0	X	X	40	10	5	5	X	X	2.95
TRANSISTOR II		0	5	X	X	5	5	0	X	X	60	10	5	10	X	X	1.58
TRANSISTOR III		0	5	X	X	5	10	0	X	X	60	5	5	10	X	X	2.51
RESISTOR		X	X	X	X	X	X	5	65	X	X	X	10	5	10	5	0.27
DIODE		X	10	X	X	15	X	0	X	30	25	15	5	0	X	X	0.60
CAPACITOR		X	0	40	25	X	X	10	X	0	X	X	15	10	X	X	0.29
INTEGRATED CIRCUIT I		20	5	X	X	5	15	0	X	X	30	0	15	10	X	X	0.25
INTEGRATED CIRCUIT II		15	10	X	X	5	15	0	X	X	35	0	10	10	X	X	0.55
	FR	.28	.62	.12	.07	.92	.60	.04	.18	.18	4.05	.67	.54	.68	.03	.01	9.00
	%	3	7	1	1	10	6	0	2	2	44	7	6	7	3	1	100

FR = FAILURE RATE; Δ FR = ACTUAL FR – GOAL FR

Table 2. Failure Modes/Mechanisms and Corrections for Integrated Circuits

FAILURE MODE/MECHANISM	MAJOR CONTRIBUTING FACTORS	METHODS TO MINIMIZE EFFECT OF MAJOR CONTRIBUTING FACTORS			
		DESIGN	PROCESS	SCREEN	INSPECTION
Inversion/channeling Contamination in, on, and under oxide layer	Impurities Non-homogeneity Adhesion of aluminum Open at oxide step Purity of oxides Pinhole in oxide	Aluminum deposition between input diodes; acts as depletion barrier	TEOS layer PbO layer Silane layer Oxide thickness control Aluminum evaporation time and temperature Double KMER Double/multiple masking/separate masks Improved mask tolerance Optimized stabilization bake Mechanized diffusion New die carrier Automatic gas cycling		Inspection for oxide tears 400X inspection Tightening of criteria on aluminum width Pre-aluminum clean inspection
Inadequate die attachment caused by incompatible materials and surfaces	Poor processes and material selection		More uniform gold plating, control Au salts in solution, post-gold deposition cleaning Thickened gold plate 100 to 200 micro-inches Removed KMER from wafer-back prior to bake Reduced die mounting temperature	In-process temperature cycle	
Contamination (surface)			Increased stabilization bake temperature Increased D.I. wash time Automated handling Vacuum pick up Dry scribe water Automatic gas cycling		
Die bond intermetallic formations Material compatibility	Uncontrolled bond size; temperature material purity	Au-Au systems Larger bonding areas Increased lead diameters Rerouted interconnections and pad locations New package gives more room to bond	Lowered bonding temperature Lower-stabilization bake temperatures One bond for contact, second bond for tail-pull Automatic tail-pull Controlled die-bonding temperature Hot capillary bonding New bonding machines	100% centrifuge In-process temperature cycle	 Visual inspection
Silicon surface epi-spikes leading to cracking Surface treatment, handling	Crystallization methods Handling methods	Small die size when possible	Improved controls and cleaning procedure at wafer lap to reduce spikes and impurities Tweezers with blocking mechanism Reduced die mount temperature Sheet resistivity limits tightened Vacuum pencils Handling mechanized Improved die boat		
Air and moisture penetration cause leakage Material compatibility	Design and processes	Thicker walls and lids Increased gold thickness Increased oxide thickness of Kovar leads Lid overlap	Moved uniform gold plating New welding tips Vacuum bake prior to seal Pre-oxide clean Kovar parts H_2O content less 35 ppm during lidding Preform cleaning (solvent) Tension on lidding boat springs Dry box cleaning cycle Control gold salts in plating Post-gold cleaning Lidding furnace profile optimization Auto Pak handling Provision of switch-weld base to header Introduction of Mech-Pak; insulated lids		Tighter specs on piece parts Daily profile check Welder clean-up Visual inspection Material inspection
Oxide defects and contamination on surface causing shorts and leakage	Inadequate control of oxide process		Moved pump down-time to assure H_2O outgassing Added vacuum bake-completed wafer Improved pre-PbO cleaning Improved pre-lid cleaning Improved post-PbO cleaning Pre-oxide cleaning of Kovar parts Solvent cleaning preforms Dry box cleaning cycle Improved pre-aluminum cleaning using D.I. rinse New die carrier Mechanized diffusion Optimization stabilization bake		Visual inspection for pinholes Visual inspection for cleanliness

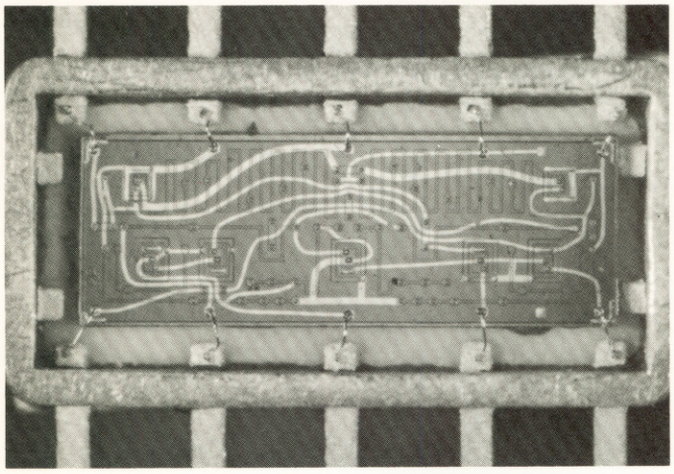
Case 1

Problem:

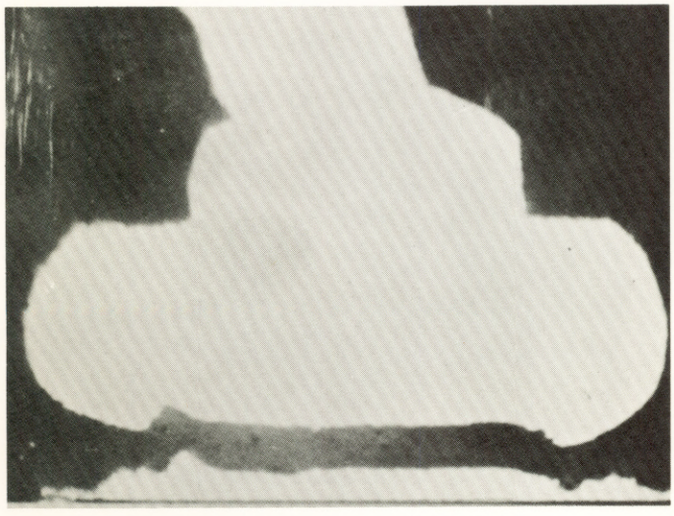
TENDENCY FOR GOLD-ALUMINUM BONDS TO OPEN

Details:

Gold-aluminum thermocompression bonds between gold wire and aluminum metallization on silicon dioxide-silicon dice in integrated circuit devices. Open bond permanent in some devices, intermittent in others.



Integrated Circuit with Lid Removed (10X)



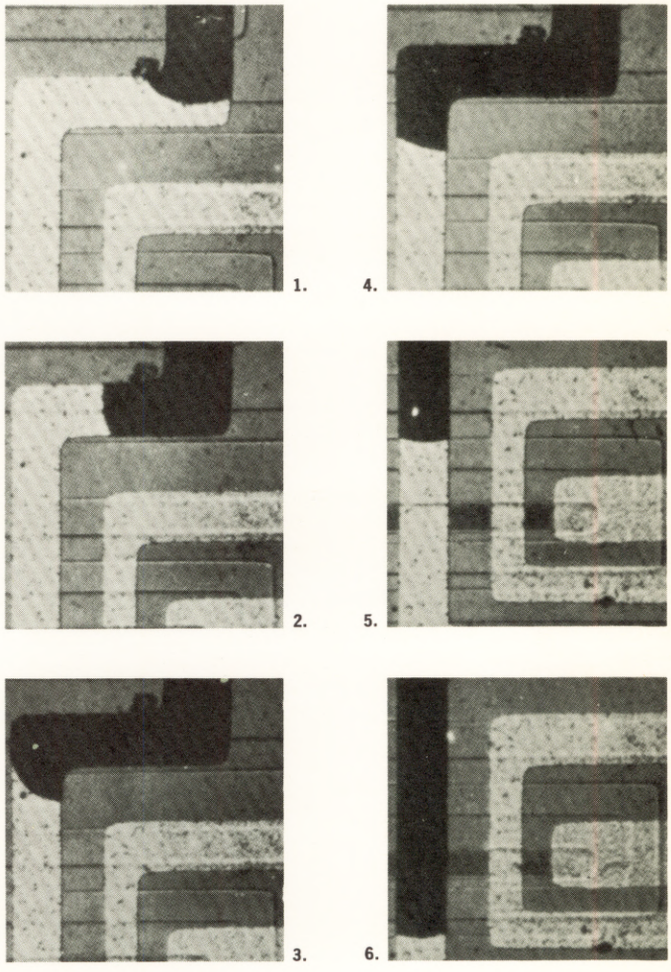
Open Thermocompression Bond (375X)

Technical approach:

Electrical testing, metallographic analysis, temperature-time study, photomicrography, X-ray diffraction and electron beam microprobe analysis, fabrication of "standard" alloys by vacuum fusion.

Observations:

Surface migration of gold away from bond; interdiffusion of gold and aluminum.



Time-Lapse Photograph Showing Surface Migration

Conclusions:

Gold-aluminum interconnects in integrated circuit devices display a time- and temperature-dependent mode of failure, resulting from interdiffusion of gold and aluminum and the tendency to form gold-rich intermetallic compounds at elevated temperatures. Temperature variation, static charges, and normal operating voltages can cause intermittent closure of open bonds.

Corrective action:

Surface oxidation; use of other metals (other than gold or aluminum) to act as diffusion barriers.

Case 2

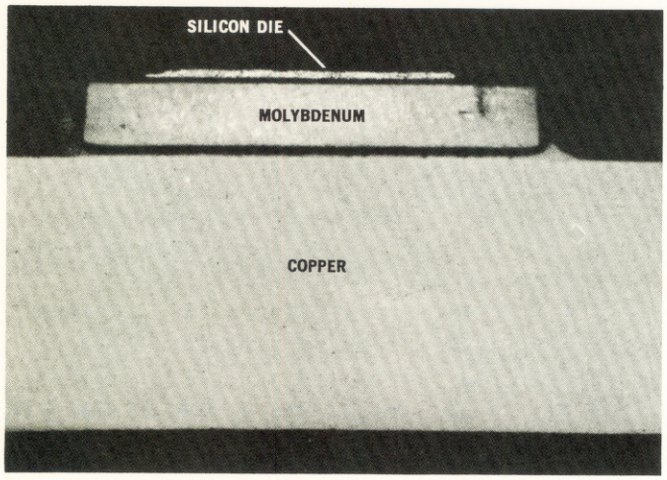
Problem:

THERMALLY INDUCED MECHANICAL STRESS IN POWER TRANSISTORS

Details:

Semiconductor devices are subjected to a considerable number of temperature changes during fabrication, screening tests, and storage. Mechanical stress results from incompatible rates of thermal expansion in adjacent materials of which the devices are composed. The stress is a function of the difference between the two materials' coefficients of thermal expansion, the change in temperature, the respective moduli of elasticity, and the thicknesses of the two materials.

To reduce stress, semiconductor devices are generally made of materials as thermally compatible as possible. Power transistors, however, require that heat generated during their operation be conducted away from the die, and materials suitable for conducting the heat away usually have a much higher coefficient of thermal expansion than the semiconducting materials of the device (especially true with silicon).



Cross Section of Power Transistor, Showing Relative Thicknesses of Copper, Molybdenum, and Silicon

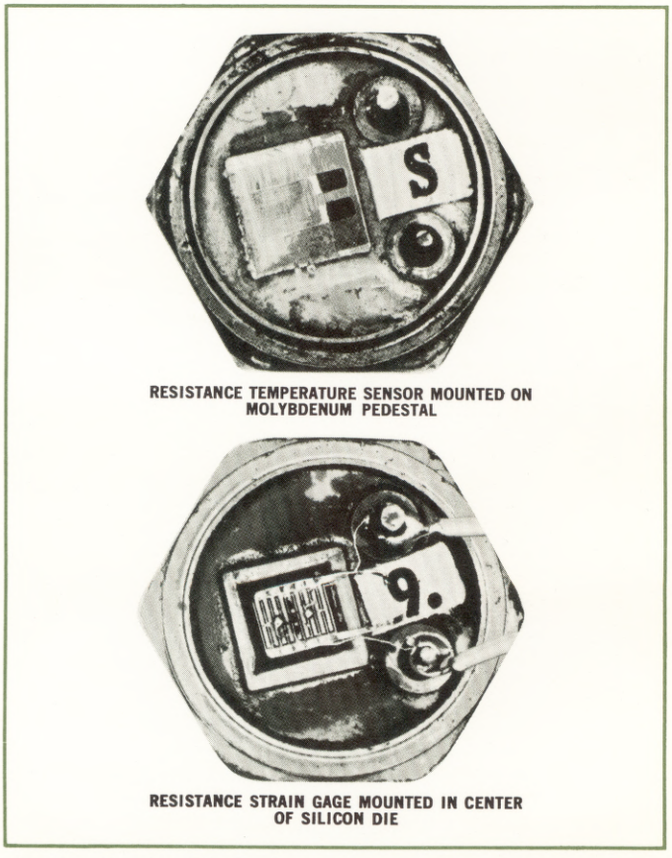
In the transistor illustrated above, the large mass of copper used to carry the heat away has a coefficient of expansion of approximately 16 ppm/degree Centigrade, while the thinner molybdenum pedestal and the silicon die have coefficients of expansion of 4.8 and 2.0 ppm/degree Centigrade, respectively. *Calculated stress in the silicon die of this device is 23,000 pounds per square inch for a 100-degree Centigrade temperature change.* This value borders on the ultimate strength of the silicon. Experimental stress analysis utilizing very small resistance strain gages measured this thermally induced mechanical stress to be less than half the calculated value. The difference was due to plastic flow in brazement between the silicon die and the header. A number of failure mechanisms were established which either reduced the plastic flow capability or weakened the power transistor brazement.

Technical approach:

Environmental chamber measurement of stress with resistance strain gages, measurement of temperature during strain, fabrication of brazements with thickness extremes, thermal induction of mechanical stress, electron microprobe analysis of temperature-cycled devices, X-ray diffraction analysis, electronmicroscopy, and microharness measurement.

Observations:

Thin brazements, which are less ductile, permit transmission of high thermally induced mechanical stress to the die. Residual stresses are also induced into the silicon die from welding, bonding, oxide growth, and lead forming. The total stress applied to the die is a combination of the applied or service stress and the composite residual stress.



Sensing Devices Mounted on Power Transistor for Accurate Measurement of Temperature and Strain

Conclusions:

Devices may be subjected to high mechanical stresses during device manufacturing and system manufacturing.

Corrective action:

Use of reduced processing temperatures, more ductile brazements, and redesigned packaging.

Case 3

Problem:

OPTIMUM PLASTIC MATERIALS FOR PACKAGING SEMICONDUCTOR DEVICES

Details:

This project was initiated by the detection of diode abnormalities consisting of excessive reverse leakage currents under stress conditions and poor lead wire-to-resin pull strength.

Technical approach:

Tests for properties, including a comparison of ionic and ionizable or gaseous contaminants contained or generated by plastics. Physiochemical property determinations were made, for the most part, on synthetically fabricated specimens, since it was difficult or impossible to directly evaluate the plastic on the diode surface.

Investigation of microdiode encapsulants from several vendors, and ascertainment by infrared spectroscopy of chemical types including silicone, phenolic, and epoxy. Comparative evaluation of fluorinated polymers to elucidate importance of relationship of polymer structure and contamination to optimum device performance.

In addition to infrared identification of plastics, property tests included measurement of water extract electrical resistivities, spectrographic analysis, thermogravimetric analysis, gas permeability, and preparation and evaluation of purified resins as protective plastics for uncased diodes. Elevated temperature and humidity testing was also performed on the components.

Observations and conclusions:

1. Ammonia was discovered to be present in a phenolic molding compound used by a diode manufacturer. Further work revealed that ammonia contamination produced increased and erratic reverse currents and was more pronounced in the presence of moisture.
2. The revelation of the presence of ammonia and other deficiencies in this molding compound induced the manufacturer to investigate other compounds and to substitute a better one.
3. The elevated temperature resistivities of coatings affected the performance of these materials as protective systems over diodes under elevated-temperature test conditions.
4. In some plastic compounds, a correlation was found between elevated-temperature resistivities and water-extract resistivities.
5. Teflon, an inert coating with a very high elevated-temperature resistivity and high water-extract resistivity, was demonstrated to have superior performance under elevated-temperature reverse bias and high-humidity reverse bias test conditions.
6. The resistivity of water extracts of evaporants was found to be an effective means of indicating the amount of ionic and other conductive impurities in plastic materials.

Case 4

Problem:

SURFACE FAILURE MECHANISMS IN SEMICONDUCTOR DEVICES

Details:

Routine failure analysis indicated that a large percentage of devices with surface-associated failure modes (e.g., I_R in diodes and I_{CBO} in transistors) could be returned to original operating level by opening the device package and releasing the enclosed gas ambient. Such a recovery indicated that the composition of the ambient encapsulated in a semiconductor device package could have an important effect on the stability of the electrical parameters of the device.

Technical approach:

A method was developed to analyze the gas ambient of good and failed devices by use of a mass spectrometer without destroying the device junction when the package was opened. Electrical measurements were made before, during, and after removal of the ambient, and after backfilling with selected ambients. Other techniques were developed which employed the gas chromatograph.

Observations:

The accompanying table shows correlation between gas ambient and the frequency of each type of failure.

AVERAGE PERCENT OF	GOOD DEVICES	I_{CBO} FAILURES	h_{FE} FAILURES	BETA RATIO FAILURES	EMPTY PACKAGES
H_2	3.2	2.4	1.5	1.4	—
CH_4	0.6	0.2	0.6	0.5	—
A	0.7	0.7	0.9	0.8	0.5
N_2	90.0	80.7	91.0	90.3	89.5
O_2	1.8	1.5	3.3	4.2	8.8
CO_2	1.9	2.6	1.2	2.3	0.4
CO	1.8	3.4	1.2	0.5	0.8
H_2O	—	8.5	0.3	—	—
Average volume (μ-cc)	4,300	4,000	3,400	3,900	4,000

Conclusions:

Composition of the ambient encapsulated in a semiconductor device can have an important effect on the stability of the device electrical parameters.

Corrective action:

Better seals, redesign of packaging, tightened specifications.

Appendix IV

AVAILABLE
AUTONETICS TECHNICAL PUBLICATIONS
ON MICROELECTRONICS

For further detail and expanded coverage of the topics discussed in this book, you may obtain copies of any of the publications listed below by submitting a written request to:

North American Aviation
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PUBLICATION NUMBER	PUBLICATION TITLE
X4-1455/3111	An Advanced Microelectronics Interconnection Technique. *C. F. O'Donnell.* October 1964.
X4-1456/3111	Advances in Electronic Systems through Use of Microelectronics. *G. V. Browning.* December 1964.
–	Application of Integrated Circuits: An Evolutionary Approach. *D. D. Robinson.* 1964.
X4-1852/3111	Application of Semiconductor Technology to Coherent Optical Transducers and Spatial Filters. *D. B. Anderson.* November 1964.
X5-1793/3111	Applications of Microphotolithography to Millimeter and Infrared Devices. *D. B. Anderson and R. R. August.* 1965.
–	Better Bonding Methods Improve Hybrid Circuits. *J. R. Howell and J. W. Slemmons.* 1965.
X4-1746/3111	Cadmium Telluride Light-Emitting Diode. *C. G. Kirkpatrick and R. G. Warren.* October 1964.
X4-1809/32	Charge Control Considerations of High-Speed Integrated Circuits. *O. S. Goda.* November 1965.
–	Chemical Vapor-Deposition of Single-Crystal Tungsten Films on Sapphire. *G. D. Barnett, A. Miller, G. R. Pulliam and R. G. Warren.*
–	Circuit-Analysis Techniques Utilizing Digital Computers. *J. J. Duffy, H. S. Scheffler and L. H. Stember.*
–	On the Coercive Force and Its Connection to the Impurities in Ferromagnetic Thin Films. *K. H. Behrndt.* 1961.
X4-1534/33	Component Quality Assurance Program for Microminiature Electronic Components for Minuteman II. *A. Borofsky.* September 1964.
X5-1159/3111	Cost Reduction Through Application of Microelectronics. *W. F. DeBoice.* June 1965.
X5-118/33	Data Analysis in Physics-of-Failure Studies. *J. R. King.* January 1965.
–	Decorated Dislocations in Magnesia Crystals. *G. R. Pulliam.* 1961.
X5-767/3111	Deposition of Films from Plasmas. *A. Miller, F. L. Morritz, D. E. Rees and R. Shima.* May 1965.
–	Derating Philosophy of Minuteman Transistors. *G. K. Cullers.*
–	Description and Comparison of Five Computer Methods of Circuit Analysis. *H. S. Scheffler and F. R. Terry.*

PUBLICATION NUMBER	PUBLICATION TITLE
X5-2024/33	Design and Process Contribution to Inherent Failure Mechanisms of Microminiature Electronic Components for Minuteman II. *A. J. Borofsky.* November 1965.
X4-1043/32	Design of Semiconductor Integrated Circuits for Low-Cost Electromechanical Control Systems. *W. F. DeBoice and N. D. Salman.* September 1964.
X5-636/3111	Development of a Flexible Epoxy Copper Clad Insulation for Etched Circuit Boards. *G. M. Knaus.* January 1965.
T4-779/34	The Development of a High-Voltage High-Yield Thin-Film Capacitor for Microcircuit Production. *L. T. Harris and G. D. Robinson.* May 1964.
T4-761/34	Development of a Thin-Film Microcircuit Facility. *F. Iles.* May 1964.
X5-1432/32	Device Coupling in Integrated Circuits: Its Cause and Prevention. *D. H. Reeder and D. D. Robinson.* October 1965.
T-168/33-3	Digital Computer Aspects of Integrated Circuit Applications. *H. C. Goodman and R. C. Platzek.* 1964.
T4-653/3111	Electron Beam Initiated Reaction Deposition of Silicon Dioxide. *A. Miller, F. L. Morritz and R. Shima.* April 1964.
–	The Electron Microprobe. *P. Pietrokowsky.* October 1964.
X5-1068/33	Electronic Components for Minuteman II. *A. J. Borofsky.*
X4-881/33	Electroplating of Plated Through-Hole Interconnection Circuit Boards. *L. J. Quintana.* 1964.
–	Epitaxial Ferrite Memory Planes. *J. L. Archer, J. E. Mee, and G. R. Pulliam.* 1965.
X5-562/33	Fabrication of Multilayer Boards at Autonetics for Minuteman II Program. *E. F. Harmon.* March 1965.
514L-1	General Purpose D-C Analog Computer with Transistor Circuitry. *H. L. Ehlers.* 1958.
552-A-15	A General Purpose Microelectronic Differential Amplifier. *J. F. Bowker and W. F. DeBoice.* 1962.
–	Gold in Silicon: Effect of Resistivity and Diffusion in Heavily Doped Layers. *D. H. Forbes, T. J. LaChapelle and W. R. Wilcox.* December 1964.
–	Growth Structure in Thin Tungsten Films. *G. D. Barnett, J. I. Medoff and A. Miller.* 1962.

PUBLICATION NUMBER	PUBLICATION TITLE
X4-1593/3111	Heteroepitaxial Silicon-Aluminum Oxide Interface: Part I. Experimental Evidence for Epitaxial Relationships of Single-Crystal Silicon. *H. M. Manasevit, A. Miller, F. L. Morritz and R. Nolder.* September 1964.
X4-1593/3111	Heteroepitaxial Silicon-Aluminum Oxide Interface: Part II. Orientation Relations of Single-Crystal Silicon. *I. B. Cadoff and R. Nolder.* 1964.
X5-848/34	I. F. Packaging Using Thin-Film Techniques. *A. T. Doyel.* June 1965.
550-A-16	The Impact of Microelectronics and Solid-State Technology on Electromechanical Control Systems. *T. Mitsutomi.* 1962.
X5-700/34	Impact of Microminiaturization on Printed Circuit Boards. *R. J. Hebert.* April 1965.
–	An Integrated Program for Procurement of High-Reliability Electronic Parts. *E. E. Valiton.* 1963.
T4-358/33	Interconnection of Integrated Circuit Flat Packs in Autonetics Improved Minuteman Program. *E. F. Harmon.* 1964.
–	An Introduction to Ferromagnetic Thin Films. *K. H. Behrndt.*
–	Investigation of the Coercive Forces of Ni, Fe and NiFe Films during and after Evaporation. *K. H. Behrndt.*
–	Linear Microcircuits Scarce? Now You Can Breadboard Your Own. *D. D. Robinson.* October 1964.
T4-353/33	The Logical Design of the D26C: A Microminiature Real-Time Processing System. *S. E. Githens, L. Miller, S. Z. Rubenstein and H. Wyle.* March 1964.
550-A-20	MANDEX, A Worst-Case Circuit Analysis Computer Program. *J. J. Duffy, H. S. Scheffler and B. Spradlin.* 1962.
X5-903/3111	Master Dice: A Low-Cost Approach to Microminiaturization. *C. D. Slaughter and J. W. Slemmons.* April 1965.
–	The Mathematical Basis of the Autonetics Etched Interconnection Design Program. *J. Weissman.*
–	Mechanisms of Gold Diffusion into Silicon. *T. J. LaChapelle and W. R. Wilcox.*
X5-642/3111	Metallurgical Failure Mechanisms in Semiconductor Devices. *G. V. Brandewie, P. H. Eisenberg and W. M. Rowe.* 1965.
–	A Method of Packaging Transistorized Printed-Circuit Board Assemblies for Efficient Use of Refrigerated Air. *H. Kamei and A. R. Tice.* 1957.
550-A-79	Microelectronics and Minuteman. *R. C. Platzek.*
552-B	Microelectronics Applications to Inertial Navigation. *W. F. DeBoice.* 1963.
T4-185/3111	Microelectronics for Future Commercial Aircraft. *J. R. Moore and R. M. Ashby.* 1964.
X5-945/319	A Microelectronics Interconnection Method. *H. T. Mortimer and J. S. Schiavo.* June 1965.
X4-1706/32	Microjoining Processes for Hybrid Thin-Film Circuits. *J. R. Howell and J. W. Slemmons.* October 1964.
–	Microminiaturization in Missiles. *J. R. Moore.* 1957.
–	Microminiaturized Autopilot Design. *E. W. Velander.* 1963.
–	Minuteman Integrated Circuits, A Study in Combined Operations. *R. C. Platzek.* December 1964.
X5-18/33	Minuteman Microelectronic Reliability Concepts. *D. G. Cummings.* January 1965.
X5-2/32	Monolithic Integrated Circuits with Wide-Band Characteristics. *C. H. Fa, G. Larchian, G. P. LeBlanc, O. Maxwell and D. McWilliams.* June 1964.
X4-2098/32	Multilayer Boards for Electrical Interconnection Density, Evolution, Design Applications, Costs, Future. *S. A. Hays.* February 1965.
X4-324/3111	New Interconnection Methods for Microcircuits. *J. B. Northrup and C. L. Zachry.* March 1964.
X5-1756/3111	Orientation Relationships in the Heteroepitaxial Tungsten on Sapphire System. *I. B. Cadoff, D. H. Forbes, A. Miller and H. M. Manasevit.* October 1965.
–	Oriented Tungsten Deposition. *G. D. Barnett and A. Miller.* 1962.
X5-1977/3111	Physics of Failure in Electronics 4th Annual Symposium Papers. November 1965.
X4-1755/3111	Planar Annular Varactor and Its Applications to Millimeter Wave Parametric Transducers. *D. B. Anderson.* October 1964.
X4-1628/3111	Planar Silicon Device Analysis with Electron Probe Microanalyzer. *P. Hagon, C. W. Laasko and C. C. Nealey.* October 1964.
X4-1493/3111	Planar Silicon Device Failure Mechanism Studies with the Microanalyzer Electron Probe. *C. W. Laasko and C. C. Nealey.* August 1964.

PUBLICATION NUMBER	PUBLICATION TITLE
X4-998/34	Predicting Performance of Integrated Circuits by a Digital Computer Technique. *C. T. Kleiner and R. D. McNair.* 1964.
X5-575/32	Predicting the Effect of an Ionizing Pulse of Radiation on Semiconductor Electronics. *C. T. Kleiner.* April 1965.
X4-890/319	Printed Cermet Resistors—Their Freedom and Constraints. *S. J. Griffin.* 1964.
–	Procurement of Extremely Reliable Semiconductor Devices for Space Applications. *H. R. Lambert.*
–	Quality Assurance for Microminiature Circuits. *J. I. Black.*
T4-710/3111	Quality Management of Supplier-Furnished Material. *H. D. Hill.* March 1964.
X5-822/32	Radiation Induced Regeneration Through P-N Junction in Monolithic I/C's. *E. D. Johnson, G. Kinoshita and C. T. Kleiner.*
X4-1055/34	R-C Active Filter Circuit Using Annular Transistors. *D. G. Edlund and D. Pruett.* 1964.
558-D-5	Recent Developments in Computer Techniques for Circuit Design and Analysis. *Scientific Computing and Analysis Group, QRS Division.* February 1962.
X5-1828/33	Reliability of Integrated Circuits for Minuteman. *T. J. Nowak.* January 1965.
X5-1255/3111	Residual Stress in Epitaxial Silicon Film on Sapphire. *C. Y. Ang and H. M. Manasevit.* June 1965.
–	Resistance of Silicon Transistors to Neutron Bombardment. *R. C. Gillis and J. W. Tarzwell.* 1957.
X4-847/32	Simulation and Verification of Transient Nuclear Radiation Effects on Semiconductor Electronics. *E. D. Johnson and C. T. Kleiner.* 1964.
X5-709/3111	Single-Crystal Silicon Epitaxy on Foreign Substrates. *H. M. Manasevit and A. Miller.* April 1965.
550-D-1	Single-Crystal Silicon on a Sapphire Substrate. *H. M. Manasevit and W. I. Simpson.*
X5-1548/3111	Single-Crystal Silicon on Beryllium Oxide. *I. B. Cadoff, D. H. Forbes and H. M. Manasevit.* September 1965.
X5-537/3111	Single-Crystal Silicon on Spinel. *D. H. Forbes and H. M. Manasevit.* March 1965.
–	Some Aspects of Applying Microminiaturized Electronics to an Electromechanical Control System. *T. Mitsutomi.*
–	Some Aspects of Microwave Phase Shifters Using Varactors. *A. E. Cohen.*
–	Some Observations of Electron Beam-Induced Recrystallization of Silicon Iron. *J. I. Medoff and A. Miller.*
T4-475/32	Strain Effects in P-N Junctions and Piezoresistance Materials. *N. E. Farb, W. G. Rogers and A. F. Rosevear.* May 1964.
–	Summary of Paper No. 7—The Mathematical Basis of the Autonetics Etched Interconnection Design Program. *J. Weissman.*
–	The System Approach to Microminiaturization. *D. D. Robinson.* February 1964.
X5-1607/32	A Technique for Low-Cost Development of Custom Linear Integrated Circuits. *D. D. Robinson.* September 1965.
–	Thermal Analysis of Integrated Circuits. *E. V. Carter.*
X4-1947/3111	Thin-Film Laser Materials. *A. Miller, F. L. Morritz and G. R. Pulliam.* December 1964.
X4-836/3111	Transient Radiation Effects on Common Microelectronics Resistor Types. *E. M. Coffin, T. C. Getten, E. E. Griffin and A. S. Hoffman.* 1964.
X5-1608/3111	Transient Radiation Effects on Insulated-Gate Field-Effect Transistors. *E. E. Griffin, Jr. and A. F. Krueger.*
X4-1662/33	Transient Radiation Effects on Semiconductor Diffused Integrated Circuits. *J. G. Doidge, T. C. Getten and A. S. Hoffman.* October 1964.
–	Tunnel Rectifier-Transistor-Logic Circuits with Transmission Line Interconnections. *O. S. Goda.*
X5-1135/3111	Twinning in Epitaxially Deposited Silicon on Sapphire. *D. H. Forbes, D. J. Klein and R. L. Nolder.* June 1965.
X4-1814/32	Utilization of Light Emission from GaAs Tunnel Diodes to Perform Computer Functions. *B. T. French.* October 1964.
–	Varactor Diode Cuts Millimeter Losses. *B. Miller.* December 1964.
T4-262/33	A Variable Junction Magnetic Effect. *Y. Yamamoto.* 1964.

Appendix V

MICROELECTRONICS GLOSSARY

Terms and Definitions

JANUARY 1966

Foreword

This glossary lists and defines many terms that are in general use within the field of microelectronics.

The terms included are those used by electronics and reliability engineers for the identification, application, electrical characterization, circuit design, and failure analysis of microelectronic devices. Basic terms defining the fundamental physics of solid-state theory are not included.

Definitions are derived from:

1. Government Section No. 20, Microelectronics Application Committee, EIA
2. IRE Standards on Electronic Devices; Definitions of Semiconductor Terms, 1954, Standard, 54 IRE 7.S2
3. Engineering Assurance Department, Components Engineering Group, Autonetics
4. New Unified List of Terms and Definitions, MCA Committee, EIA, 8 May 1964
5. MIL-STD-429A, Printed-Circuit Terms and Definitions, 19 December 1960
6. Microminiature Circuit Glossary, Terms and Definitions, Autonetics Publication No. 558-D-4 (Rev 3/63), December 1962

A

ACCEPTOR (SEMICONDUCTOR): See IMPURITY, ACCEPTOR.

ACCUMULATION LAYER: A region of a semiconductor device, usually at the surface, in which the concentration level of majority carriers has been increased beyond its original level. This increase or accumulation of carriers may be due to actual impurity diffusion or to charge separation by surface contamination. This is the opposite of INVERSION LAYER.

ACTIVATION ENERGY: The quantity of energy required to initiate a specific change, such as to ionize a donor impurity or to break a valence bond.

ACTIVE ELEMENT: An electronic circuit element which exhibits power gain or transistance. Examples: transistor and varactor diode.

ACTIVE SUBSTRATE: A substrate which contributes to at least one active element.

AGGLOMERATION: The deposition of the evaporant on the substrate in the form of balls or globules instead of as a continuous film.

ALLOYED-JUNCTION FIELD-EFFECT TRANSISTOR: A field-effect transistor in which the gate-to-channel p-n junctions are formed by an alloying process during device fabrication. This device is not of common usage.

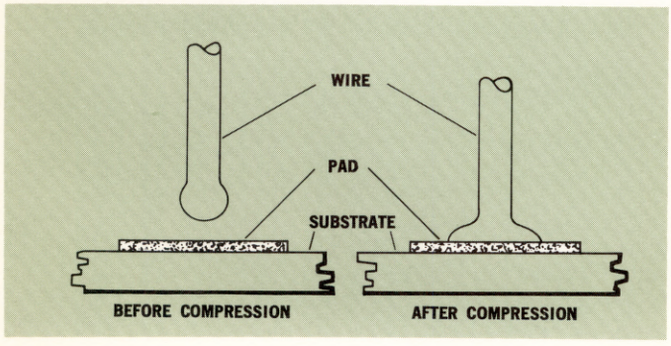
ALLOY PROCESS: A fabrication technique in which a small part of the semiconductor material is melted together with the desired metal and allowed to recrystallize. The alloy developed is usually intended to form a p-n junction or an ohmic contact.

ASPECT RATIO: The ratio of the length of a microelectronic element divided by the width. Example: The resistance of a thin-film resistor is the product of the sheet resistivity and the aspect ratio.

ARRAY DEVICE: A group of regular, repetitive, electrical elements.

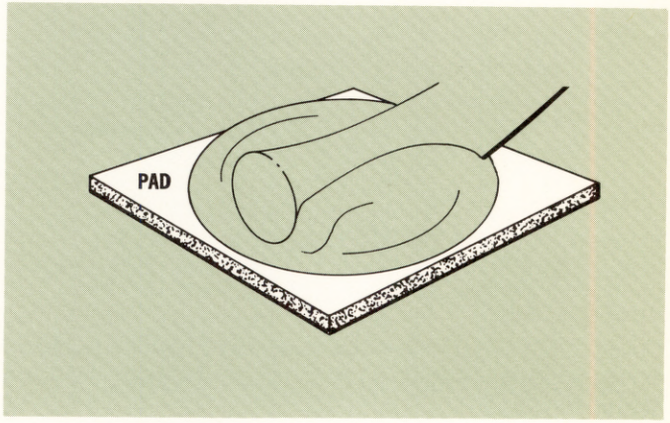
B

BALL BOND: A thermocompression bond in which a gold wire is flame-cut to produce a ball-shaped end which is then bonded to a metal pad. It is also referred to as a "nail-head bond." See the following illustration.



BIPOLAR TRANSISTOR: An injection-type transistor ("conventional" transistor).

BIRD-BEAK BOND: A thermocompression bond in which a small wire is attached to a pad. The bond is called "bird-beak" because it resembles the beak of a bird. This configuration results from a compression tool designed to allow a relatively thick section of wire along the center of the bond. See the following illustration.



BONDING ISLAND: See PADS.

BREAKDOWN VOLTAGE: The value of voltage whose application to a p-n junction or dielectric causes voltage breakdown. When applied to a p-n junction, the breakdown voltage causes current flow to increase rapidly from a relatively low value to a relatively high value. When applied to a dielectric, the breakdown voltage causes the dielectric to act as a conductor rather than as an insulator.

BUMP CONTACT: A method of providing connections to the various terminal areas of a device. The term "bump" is due to the small mound of material formed on the device surface or substrate and utilized as a contact.

BURIED-LAYER TECHNIQUE: A technique for fabricating monolithic transistors in which a low-resistivity material is introduced into the substrate under the transistor collector to reduce the effective collector resistance.

C

CARRIERS: Electrons (n-type carriers) or holes (p-type carriers) in a semiconductor material which are available (free) for the conduction of electric current.

CERAMIC: A product composed of inorganic, non-metallic compounds formed through heat-processing. Example: alumina.

CERAMIC-BASED CIRCUITRY: A circuit printed on a ceramic substrate. Usually consists of combinations of resistive, capacitive, or conductive elements fired on a wafer-like piece of ceramic.

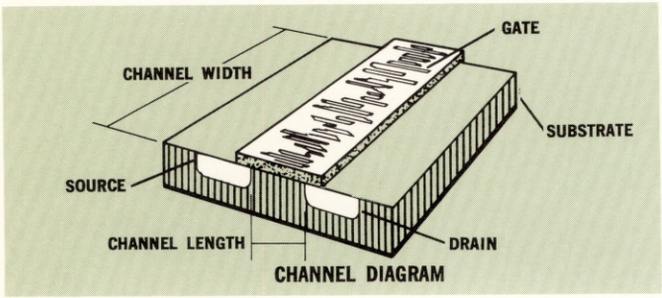
CHANNEL: An electrically-conductive path between two separated regions of a semiconductor material. In a field-effect transistor, it is the fabricated or induced path between the source and drain. In a bipolar transistor, the term is generally

used to describe an undesirable localized, severely-inverted region of the surface.

CHANNEL DEPTH: The depth of a conducting channel, usually between the source and drain of a metal-oxide-semiconductor field-effect transistor.

CHANNEL LENGTH: See next illustration.

CHANNEL WIDTH: See next illustration.



CHANNEL DIAGRAM

CHIP: See DIE.

CIRCUIT: The interconnected combination of a number of microelectronic elements or electronic parts to accomplish a desired function.

CML (CURRENT MODE LOGIC): A logic gate consisting of an n-p-n current mode switch with emitter followers coupling the signal from the collectors of the gate to the output. See also MECL.

COLD WELD: The joining of two metals by the application of pressure only.

COMPONENT: See ELEMENT and PART.

CONDUCTIVE PATTERN: A network of conductive material distributed over the surface of a substrate for the purpose of interconnecting the circuit elements.

CONDUCTIVITY, N-TYPE: The conductivity associated with free electrons in a semiconductor material.

CONDUCTIVITY, P-TYPE: The conductivity associated with hole carriers in a semiconductor material.

CONDUCTOR: A circuit element, such as metal or low resistivity semiconductor material, whose function is to conduct electrical current.

CONFORMAL COATING: An organic protective coating applied over circuit elements and conforming to contours and configurations.

CONTAMINANT: A foreign material present in a device which may change the device parameters. Examples: moisture and chemical ions.

CORDWOOD: The technique of producing modules by bundling parts as closely as possible and interconnecting them into circuits by welding or soldering leads together.

COUNTERELECTRODE: The top plate of a non-polar thin-film capacitor, or the cathode plate of a polarized capacitor.

CPC (CERAMIC PRINTED CIRCUIT): A circuit formed by sequentially screening combinations of resistive, conductive, and insulating inks on a ceramic substrate.

CROSSOVER: A method used to connect two elements of a circuit by depositing an interconnecting material across the insulated upper surface of another interconnect or element.

CROSSUNDER: A method used to connect two elements of a circuit by depositing or diffusing a conductive path into a substrate.

CROW'S-FOOT DISLOCATION: A crystalline imperfection resembling a crow's foot. This dislocation is often caused by applying excessive test probe pressure to a wafer or die. See also DISLOCATIONS, CRYSTAL.

CZOCHRALSKI CRYSTAL: A crystal grown by slowly withdrawing a seed crystal from a melt, while the melt is held slightly above the melting point of the material. High-quality, low-dislocation-density crystals of germanium and silicon are grown in this manner.

D

DANGLING BONDS: Incomplete covalent bonds at a surface of a material.

DENSITY, CARRIER: The number of hole and free-electron carriers per unit volume in a semiconductor material.

DENSITY, EXCESS CARRIER: The number of excess carriers per unit volume in a semiconductor material. Generally, it is the number of existing minority carriers, less the number of equilibrium majority carriers.

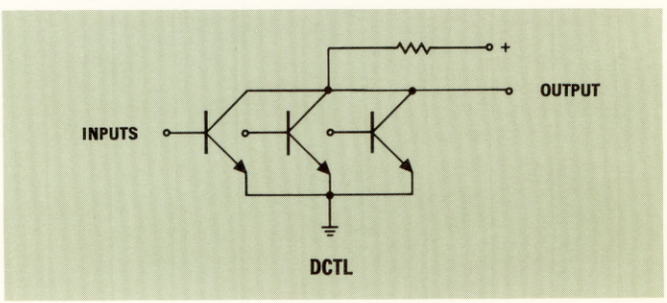
DEPLETION REGION: A region in a semiconductor material, usually at the surface, in which the majority carrier density is reduced from the bulk density.

DEPLETION REGION (JUNCTION): A space-charged region in which essentially neither holes nor electrons are available for conduction. Example: the reverse-biased region of a p-n junction.

DEPLETION-TYPE MOS FET: A field-effect transistor in which a shallow, electrically-conductive channel connecting the source and drain is diffused into the device during fabrication. This channel, of the same conductivity type as the source and drain, can be made more resistive by voltage-biasing the gate.

DEVICE: An electronic part consisting of one or more discrete active or passive elements.

DCTL (DIRECT-COUPLED TRANSISTOR LOGIC): A standard, common-emitter circuit in which all collectors are tied together and returned to the collector voltage supply through a common mode resistor as illustrated below.



DCTL

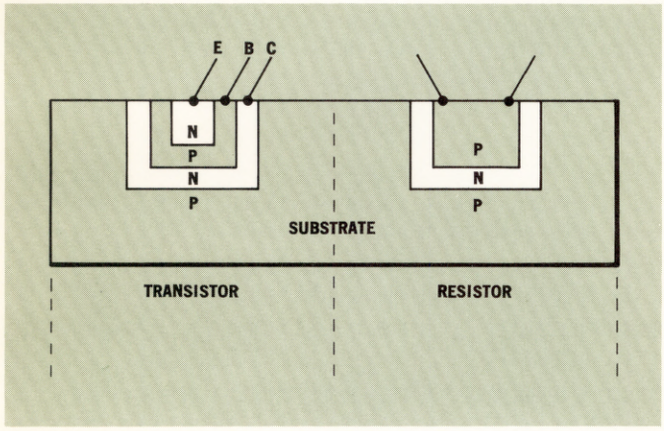
DIE (DICE): A smallest portion of a wafer which is to be bonded to a device header or package.

DIE BONDING: The attachment of a die to a header or to a device package.

DIELECTRIC: An insulating or non-conductive material used in microelectronic devices to fabricate capacitors and to insulate conductors.

DIELECTRIC ISOLATION: The achieving of electrical isolation of the monolithic integrated circuit elements from each other by dielectric material rather than by reverse-biased p-n junctions. Example: Autonetics "Poly" process.

DIFFUSED-COLLECTOR TECHNIQUE: The fabrication technique for monolithic circuits which employs three sequential diffusion cycles to form three (or less) stacked junctions as illustrated below.



DIFFUSED-JUNCTION FIELD-EFFECT TRANSISTOR: A common type of field-effect transistor in which the gate p-n junctions are fabricated by a diffusion process.

DIFFUSION CONSTANT (CARRIER): A constant to describe the migration of carriers in a semiconductor material resulting from a concentration gradient of the carriers.

DIFFUSION CONSTANT (D): A temperature-dependent constant to describe the migration of a dopant material during diffusion. Units are generally expressed in cm^2/sec.

DIFFUSION DEPTH: The depth within a material to which a specified diffusant concentration is obtained as a result of diffusion. Often, diffusion depth is specified at the depth where total compensation exists.

DIFFUSION LENGTH: The average distance to which minority carriers diffuse between generation and recombination in an operating semiconductor device.

DIFFUSION PROCESS: The process of doping semiconductor materials by injecting an impurity into the crystal lattice at an elevated temperature. This process is usually performed by exposing the semiconductor crystal to a controlled surface concentration of dopants.

DIP SOLDERING: A process whereby a printed wiring board or substrate is brought into contact with the surface of molten solder by immersing the board for the purpose of simultaneously depositing solder onto the conductive surface or for soldering parts to the printed wiring.

DISCRETE ELEMENT: An electronic element, such as a resistor or transistor, manufactured in such a manner that it can be individually measured and transported.

DISLOCATIONS, CRYSTAL: Imperfections in the idealized crystal structure.

DISLOCATION DENSITY: The quantity of dislocations observed per unit surface area.

DONOR: A semiconductor impurity that provides (donates) an electron not required for crystal-lattice bonding. The electron may be free to conduct electric current.

DONOR, SEMICONDUCTOR: See IMPURITY, DONOR.

DOPANT: See IMPURITY, DONOR; and IMPURITY, ACCEPTOR.

DOPANT CONCENTRATION: The acceptors per unit volume less the donors per unit volume in a p-type semiconductor material, or the donors per unit volume less the acceptors per unit volume in an n-type semiconductor material.

DOPANT-CONCENTRATION GRADIENT: The rate of change of the dopant concentration in a given direction, usually in a direction parallel to the alloying or diffusion direction.

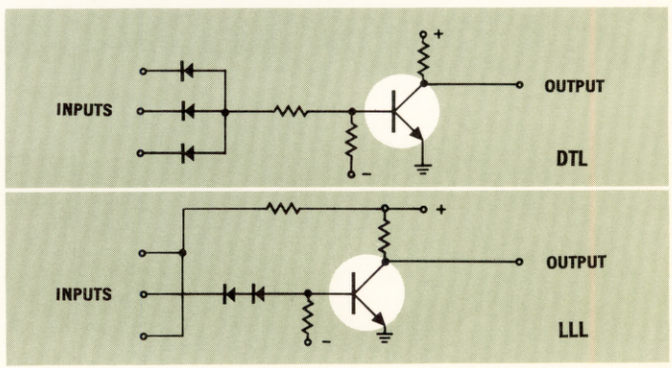
DOPING-COMPENSATED (SEMICONDUCTOR MATERIAL): A semiconductor material which contains both donors and acceptors.

DOUBLE PHOTO-RESIST: A technique developed to eliminate pinholes in the photo-resist coating during fabrication of microelectronic integrated circuits. It may consist of two separate applications and exposures of the same or different types of photo-resist emulsions.

DRAIN: The section of a field-effect transistor in which the flow of majority carriers terminates. The drain corresponds to the collector of a conventional transistor or the plate of a vacuum tube.

DRIFT MOBILITY: The average drift velocity of carriers per unit electric field in an homogeneous semiconductor.

DTL (DIODE TRANSISTOR LOGIC): A logic circuit using input coupling diodes to the base of a grounded-emitter circuit. A modified form of DTL is known as low-level logic (LLL). Both circuits are illustrated below.



E

ECL (EMITTER-COUPLED LOGIC): See CML.

ELECTRICAL FIELD (VOLTAGE GRADIENT): The voltage between two points in a material, divided by the dielectric constant of that material. The MOS transistor is controlled by an electrical field.

ELECTRICAL OVERSTRESS (EOS): The application of electrical current, voltage, or power of a level greater than that for which the device is rated, which may result in device degradation or destruction.

ELECTRON-BEAM EVAPORATION: An evaporation technique in which the heating of the evaporant is achieved by electron bombardment.

ELECTRONICS, INTEGRATED: That branch of the electronics art concerned with the electronic circuits that form an integral unit which cannot be broken down into smaller segments without destroying the entire unit. Also known as "integral electronics."

ELECTRONICS, MOLECULAR: That branch of the electronics art concerned with the electronic functions performed by the action of electrochemical states within a region of quasi-molecular dimensions residing in one single unit, a further reduction of which would destroy the electronic function of that unit.

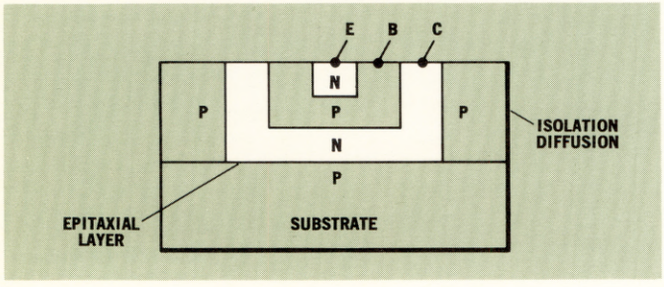
ELEMENT (ELECTRONIC): An increment of volume of a part that performs an elementary electrical function. Example: resistor, transistor, or diode.

ENHANCEMENT-TYPE METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR: A common type of metal-oxide-semiconductor field-effect transistor. Its source-to-drain conduction is dependent upon a channel which is electrostatically induced by the gate potential.

EPIC PROCESS: The registered trade name for the dielectric isolation technique used by Motorola. See also POLY PROCESS.

EPITAXIAL DEPOSITION: The growth of additional material on a substrate, usually a thin film and often having a crystal structure and orientation controlled by matching that of the substrate.

EPITAXIAL TRIPLE-DIFFUSED TECHNIQUE: The technique in the fabrication of a monolithic circuit which involves three sequential diffusion cycles to form the three (or less) stacked junctions. The diffusions are made into a high-resistivity, thin, epitaxial layer which is deposited on a silicon substrate as illustrated below.



ESTERIFICATION: The chemical reaction between an acid and an organic base (alcohol) resulting in an organic salt (ester). This term is applied to a passivation technique whereby an organic material is reacted with the silicon oxide grown over the surface of a silicon integrated circuit.

ETCHANT: A solution used, by chemical reaction, to remove the unwanted portion of a material bonded to a substrate or circuit board.

ETCHED WIRING SUBSTRATE: See PRINTED WIRING.

EVAPORANT: The material deposited on a substrate by evaporation.

EVAPORATIVE DEPOSITION: The technique of condensing a thin film of evaporated material upon a substrate. The source of the evaporant is a material usually heated in a high vacuum.

EXTRINSIC PROPERTIES (SEMICONDUCTOR): The resultant properties of a semiconductor material after modification by dopants, traps, dislocations, mechanical stress, and electrical fields.

F

FAN-IN: The number of similar type inputs connected into a microelectronic device. Example: Six logic inputs connected to one AND gate would have a fan-in of six.

FAN-OUT: The number of inputs (loads) which are driven by the output of a microelectronic device.

FEB (FUNCTIONAL ELECTRONIC BLOCK): See MONOLITHIC CIRCUIT.

FIELD-EFFECT TRANSISTOR (FET): A semiconductor device in which the output current is controlled by an electrical field. (See also JUNCTION FIELD-EFFECT TRANSISTOR and INSULATED-GATE FIELD-EFFECT TRANSISTOR.)

FLASH EVAPORATION: See EVAPORATIVE DEPOSITION.

FLIP-CHIP: See REGISTRATIVE BONDING.

FLIP-FLOP: A circuit which has two stable states; commonly called a bistable multivibrator.

FLIP-FLOP, JK: A bistable multivibrator circuit in which the simultaneous applications of set and reset inputs cause the output state to switch (complement).

FLIP-FLOP, RS: A bistable multivibrator circuit in which the simultaneous applications of set and reset inputs do not cause the output state to switch.

FLOAT-ZONE CRYSTAL: A crystal grown by passing a molten zone through a cylinder of material. No other material, except possibly a gas, is in contact with the molten zone. When the crystal is grown in a vacuum, the term "vacuum float-zone crystal" is often used.

FLY'S-EYE LENS: A multiple lens consisting of hundreds of small, closely spaced lenses; it is used to form many images of the same objective and eliminates the need for step and repeat techniques in fabricating microelectronic circuits.

FOUR-LAYER DIODE (P-N-P-N): A diode consisting of four alternate layers of n-type and p-type material forming

three p-n junctions which can exhibit silicon-controlled rectifier-like characteristics. Monolithic microelectronic parasitic elements can in effect form a p-n-p-n element.

FREE ELECTRONS: Electrons in a semiconductor material which are available to conduct electric current. These are valence electrons, not actively involved in forming covalent bonds between adjacent atoms of the crystal lattice.

FRIT (GLASS): Finely ground glass, suspended in an organic vehicle and fired to form package parts such as headers. It is also used in glass-ambient technology. See also GLASS-AMBIENT TECHNOLOGY.

FULL GATE: A MOS FET gate which extends the entire distance between and overlaps the source and drain regions.

FUNCTION: A fixed relationship between two or more variables. As applied to microelectronics, typical variables are analog input signals, output power, and digital inputs. Examples of microelectronic functions include amplification and gating.

G

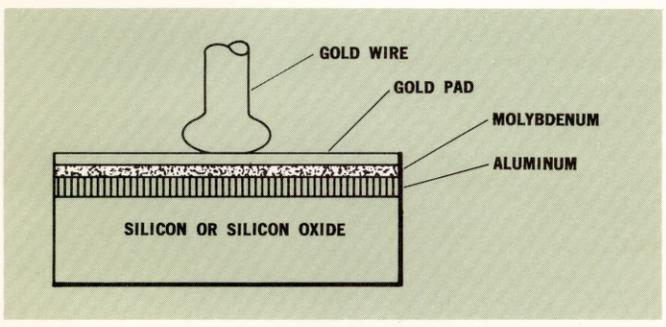
GAIN BANDWIDTH PRODUCT: A figure of merit often applied to microelectronic devices. Usually, it is the product of the midfrequency band gain and the upper radian frequency at which the gain is down 3 db from its mid-frequency value.

GLASS-AMBIENT TECHNOLOGY: The technique of applying glass directly to the surface of a semiconductor material. Typically, glass is applied to the surface of a microelectronic device by pyrolytic deposition, vapor-deposition, or by firing a glass frit to the surface at elevated temperatures.

GATE: The region of a field-effect transistor which controls the output current. The gate corresponds to the control grid of a vacuum tube and to the base of a conventional transistor.

GLAZED SURFACE: See GLASS-AMBIENT TECHNOLOGY.

GOLD MOLY BOND: A type of thermocompression ball bond. A gold wire is flame-cut to produce a ball-shaped end which is bonded to a gold surface and is, in turn, metallurgically isolated from an aluminum metallization by a thin layer of molybdenum. Other materials, such as titanium or zirconium, may be used in place of molybdenum. See illustration below.



GUARD BAND: A physical spacing between the basic elements in a device for the purpose of reducing electrical coupling between basic elements. Often the coupling results from moisture and contaminants.

GUARD ELECTRODE: A metal layer placed over a device junction and insulated from the junction by silicon oxide. The layer inhibits the formation of surface inversions and channels by constraining the junction surface electrical field.

GUARD RING: A low sheet-resistivity diffusion encircling a region of a transistor to minimize the undesirable effects of channeling which result from surface inversions. It is also known by various trade names such as "Annular Ring," "Annular Process," and "Channel Stopper."

H

HALL MOBILITY: Carrier mobility determined by measuring the "Hall effect" voltage. Hall measurements allow the determination of both carrier density and mobility.

HEADER: The portion of a device package to which the die is attached and from which the external leads extend. Examples: TO-5 case header and flat-pack base.

HEAT SINK: A mechanical device used to absorb or transfer heat away from an element or part.

HOLE CONDUCTION: A mode of electron flow within a semiconductor material. As an electron ionizes and moves (under the influence of an electric field), it leaves a hole (vacancy) in its original position. The holes appear to flow in a direction opposite to the direction of the electron flow.

HYBRID INTEGRATED CIRCUIT: An integrated circuit utilizing a combination of techniques such as diffused monolithic, thin-film elements, and discrete devices.

I

IMPURITY, ACCEPTOR (SEMICONDUCTOR): An impurity such as boron, aluminum, or gallium which may induce holes in a semiconductor material. Also referred to as "p-type dopant."

IMPURITY, DONOR (SEMICONDUCTOR): An impurity such as antimony, arsenic, or phosphorus which may induce free electrons in semiconductor material. Also referred to as "n-type dopant."

INERT GAS SPUTTERING: See SPUTTERING, CATHODIC.

INJECTION, CARRIER: An increase in the concentration of minority carriers in a semiconductor material as a result of the application of voltage or radiation. Example: the introduction of minority carriers into the base region of a conventional (injection-type) transistor from the emitter.

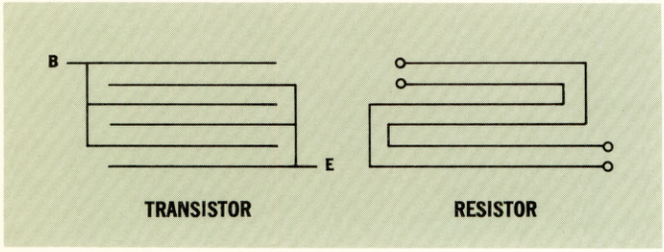
INSULATED-GATE FIELD-EFFECT TRANSISTOR (IGFET): A field-effect transistor in which the gate is insulated from the source-to-drain channel by a dielectric material. Example: MOS FET device with an oxide serving as the insulating dielectric.

INSULATOR: A material which essentially does not conduct current.

INTEGRATED CIRCUIT: An electronic device containing several integral active or passive elements which perform all

or part of a circuit function. Example: a monolithic silicon diffused circuit.

INTERDIGITATED: A topology technique used to minimize device size, optimize characteristics, or improve element matching and tracking as illustrated below.



INTERCONNECTION: The joining of one individual device with another.

INTRACONNECTION: The joining of elements within devices.

INTRINSIC PROPERTIES (SEMICONDUCTOR): The properties of a semiconductor which are characteristic of the pure, ideal crystal.

INVERSION LAYER: A surface layer of a semiconductor material which has been inverted from its original conductivity type to the opposite conductivity type.

ISLAND: An isolated region diffused or alloyed into a semiconductor substrate.

ISOLATION DIFFUSION: A diffusion process which provides a junction to electrically isolate the various elements in the monolithic circuit.

ISOLATION DIODE: A diode providing electrical isolation between circuit elements in a monolithic die. This is achieved by forming a reverse-biased p-n junction (diode) around each component.

J

JUNCTION DEPTH: See DIFFUSION DEPTH.

JUNCTION FIELD-EFFECT TRANSISTOR: A common type of field-effect transistor in which the drain-to-source conduction is controlled by a p-n junction located between the source and the drain. The voltage applied to the p-n junction varies the width of its depletion region which, in turn, controls the source-to-drain conduction.

JUNCTION, P-N (SEMICONDUCTOR): A region of transition between p- and n-type semiconductor material which exhibits an asymmetrical conduction.

K

KMER: Kodak Metal Etch Resist, a trade name. See PHOTO RESIST.

KPR: Kodak Photo Resist, a trade name. See PHOTO RESIST.

KTFR: Kodak Thin-Film Resist, a trade name. See PHOTO RESIST.

L

LANDS: See PADS.

LATCH UP: The switching of an electronic circuit mode to an unintended mode under stimulation by radiation, electronic signals, improper voltage application, or power sequencing. This effect, which usually involves parasitic elements, causes circuit malfunction and may cause device destruction.

LIFETIME, MINORITY CARRIER: A parameter which indicates the time required for minority excess carriers to recombine with majority carriers.

LLL (Low-Level Logic Circuitry): See DTL.

M

MAJORITY-CARRIER DEVICE: A semiconductor device which depends for its operation on the action of majority carriers. Example: MOS FET.

MAJORITY CARRIERS: Carriers of the same polarity as the host semiconductor material (holes in p-type material or electrons in n-type material).

MASK: An implement used to shield selected portions of a wafer or substrate during a deposition process; also, to shield selected portions of photosensitized material during photo processing.

MASTER DIE (DICE): A substrate containing unconnected active and passive elements located in a predetermined pattern. Connection pads exist for each element and sub-element. A variety of circuits may be achieved by using various intraconnection patterns.

MASTER SLICE: A registered trade name by Texas Instruments, Inc. See MASTER WAFER.

MASTER WAFER: A technique of using one basic, unconnected, diffused wafer containing a repetitive grouping of elements necessary to fabricate different circuits by employing various interconnection patterns.

MECL: Motorola Emitter Coupled Logic. The registered trade name for current mode logic. See CML.

METAL: As contrasted to semiconductor material, the conduction band of metal extends into the valence band and no energy gap exists. Metal conducts by free-electron movement and usually exhibits a positive resistivity-temperature coefficient.

METALLIZATION: The deposition of a metal film on a substrate by evaporative deposition, cathodic sputtering, vapor plating, or electroplating.

METAL-OXIDE-SEMICONDUCTOR (MOS): A term employed with other nomenclature to describe the technique of insulating a metallized electrode from a semiconductor material, using an oxide dielectric.

METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR (MOS FET): A common type of insulated-gate field-effect transistor (IGFET) employing the metal-oxide-semicondutor (MOS) technique. The metallized gate is isolated from the drain-to-source channel by an oxide of silicon.

METAL-OXIDE-SILICON: An uncommon term used synonymously with metal-oxide-semiconductor (MOS). The use of the abbreviation MOS for metal-oxide-silicon is to be discouraged.

METATHESIS: The deposition of material resulting from the reaction between two gaseous materials which precipitates a reaction product on the substrate.

MICROELECTRONICS: That branch of electronics art which is associated with extremely small electronic parts, assemblies, or systems.

MICROMINIATURIZATION: The utilization of the microelectronics art to fabricate microelectronic systems and functions.

MICROSYSTEM ELECTRONICS: That branch of the electronics art which applies to the realization of extremely small systems.

MINORITY-CARRIER DEVICE: A semiconductor device which depends for its operation on the action of minority carriers. Example: a conventional bipolar transistor.

MINORITY CARRIERS: Carriers of opposite polarity to the host semiconductor material (holes in n-type material, or electrons in p-type material).

MIS: An abbreviation for metal-insulator-semiconductor. The MOS is a subclassification of the MIS. The insulator (I) in the MIS corresponds to the oxide (O) in the MOS.

MIS CIRCUIT: An abbreviation for metal-insulator-semiconductor circuit. A circuit fabricated using the metal-insulator-semiconductor techniques. Example: a MOS circuit.

MOBILITY (DRIFT AVERAGE): The measure of the average velocity of a carrier movement under the influence of an electronic field.

MODULAR: Describes a method of microelectronic device fabrication in accordance with a set of design rules which enhances compatibility and interchangeability between components.

MODULE: An electronic component which has been designed using modular concepts.

MOLECULAR INTEGRATED CIRCUIT: An integrated circuit in which the identity and location of specific electrical elements is indeterminable even upon microscopic disassembly of the material of which the circuit is formed. As opposed to conventional and microelectronic circuitry, the molecular integrated circuit can be defined only by function. The function can be described only by mathematical models and incremental circuit representation.

MONOLITHIC CIRCUIT: A circuit fabricated within a single block of material.

MOS CIRCUIT: Metal-oxide-semiconductor circuit. A circuit fabricated utilizing MOS devices. Such a circuit consists entirely or almost entirely of metal-oxide-semiconductor field-effect transistors, some of which are used as transistors, and others as resistors (due to the transistor "on" resistance). MOS circuits are generally characterized by the large number of closely-packed field-effect transistors.

MULTIPLE-GATE DEVICE: A field-effect transistor (generally of the metal-oxide-semiconductor type) which has several gates. These gates may be arranged in series or in parallel between the source and drain of the transistor.

N

NAIL-HEAD BOND: See BALL BOND.

N-CHANNEL: A thin conductive path in a semiconductor device in which conduction occurs primarily by majority-type free electrons.

N-CHANNEL FIELD-EFFECT TRANSISTOR: A field-effect transistor in which the source, drain, and the conductive channel between them are of n-type conductivity material.

N-DIFFUSION: A semiconductor diffusion operation which results in an increase of the relative number of n-type carriers available. This is usually an in-diffusion of donor impurities.

N-TYPE CARRIERS: Free electrons in a semiconductor material. Example: electrons that are available for conduction of current.

N-MOST: An abbreviation for "n-channel metal-oxide-semiconductor transistor." The "n" implies that in the MOS FET, drain-to-source conduction is by free electrons (not hole conduction).

N-TYPE SEMICONDUCTOR: A semiconductor material in which free electrons are present in excess of free holes, in the electrically quiescent condition.

O

OFFSET-GATE DEVICE: See PARTIAL GATE DEVICE.

OHMIC CONTACT: A contact between two materials in which the potential difference across them is proportional to the current passing through, and in which the voltage drop is the same for current flow in either direction.

OHMIC (OPTIMIZED MICROCIRCUITS): A trade name registered by Amelco. A type of integrated circuit with a collector having two contacts, one for the power supply and one for the device output. It is similar to diode transistor logic (DTL) circuits.

OHMS PER SQUARE: The unit of sheet resistivity. See SHEET RESISTIVITY.

OXIDATION (CHEMICAL): A chemical reaction resulting in an increase in the proportion of oxygen- or acid-forming element or radical in a given compound. In microelectronics, silicon oxide passivations are sometimes formed by chemical oxidation of the silicon surface.

OXIDATION (THERMAL): Chemical oxidation accelerated by the application of heat. Silicon oxide layers of monolithic integrated circuits are usually formed by thermal oxidation.

OXIDE STEPS: A sharp variation in thickness of the silicon oxide on the surface of an integrated circuit due to the selective removal of the oxide at various fabrication steps.

P

PADS: Metallized areas on the surface of a device wafer or

die to which bonds, interconnects, or test probes may be applied.

PARALLEL-GATE DEVICE: A field-effect transistor having multiple gates in parallel between the source and drain.

PARASITIC ELEMENT: An extraneous or undesirable circuit element existing in a microelectronic circuit as a result of the inherent nature of the particular fabrication process and circuit element layout involved. Examples: stray capacitances or substrate transistor actions.

PARASITIC SHUNT CAPACITANCE: An undesirable parasitic capacitance in a monolithic integrated circuit often resulting from a reverse-biased isolation diode ("tub").

PART: One device, or two or more devices joined together, not normally subject to disassembly without destruction of the intended function.

PARTIAL-GATE DEVICE: A field-effect transistor in which the gate element does not extend the entire distance between the source and drain.

PARTICLE: A piece of foreign material within the microelectronic device package which may cause mechanically induced damage or electrical shorts.

PASSIVATION: The surface treatment of a semiconductor material to protect the device from the effects of moisture and contaminants. Examples: oxidation, glazing, and esterification.

PASSIVE ELEMENT: An electronic circuit element which exhibits neither power gain nor transistance. Examples: capacitors, resistors, and transformers.

PASSIVE SUBSTRATE: A substrate which does not contribute to an active electrical element. Examples: glass and alumina.

PATTERN DEFINITION: The accuracy of the reproduction of pattern edges in the integrated circuit elements, relative to the original artwork.

P-CHANNEL: A thin conductive path in a semiconductor device in which conduction occurs primarily by majority hole carriers.

P-CHANNEL FIELD-EFFECT TRANSISTOR: A field-effect transistor in which the source, drain, and conducting channel between them are of p-type conductivity material.

P-DIFFUSION: A semiconductor diffusion operation which results in an increase of the relative number of p-type carriers available. This is usually an in-diffusion of acceptor impurities.

PHOTO RESIST: A material which is photographically fixed in position to selectively mask against etching or plating. Typical photo resists include Kodak Photo Resist (KPR), Kodak Metal-Etch Resist (KMER), and Kodak Thin-Film Resist (KTFR).

PINCH-OFF VOLTAGE: The drain-to-source voltage of a field-effect transistor, beyond which an increase in voltage does not appreciably increase the drain-to-source current, for a given gate-to-source voltage.

PINHOLE: A very small hole extending through a layer of material.

PIPES, DIFFUSED: A thin, column-like diffused structure extending between the diffused layers of a device, usually resulting from imperfect oxide masking or oxide removal during fabrication.

PITS: Small holes occurring as imperfections which do not penetrate entirely through the material.

PLANAR DEVICE: A registered trade name by Fairchild Semiconductor Division. A type of semiconductor device in which all p-n junctions terminate in the same geometric plane.

P-MOST: An abbreviation for "p-channel metal-oxide-semiconductor transistor." The "p" implies that in the MOS FET, drain-to-source conduction is by hole carriers.

POLYCRYSTALLINE MATERIAL: A monolithic material containing more than one crystal. "Polycrystalline" can apply to a twin crystal as well as to a heterogeneous growth of many crystals.

POLY PROCESS: The term for Autonetics' inverted dielectric isolation technique whereby individual circuit elements are surrounded by an insulating layer of glass, and are mechanically supported in a substrate of polycrystalline silicon. See DIELECTRIC ISOLATION.

PRINTED CIRCUIT: A pattern comprising printed wiring and printed elements, all formed in a predetermined design in, or attached to, the surface or surfaces of a substrate.

PRINTED-CIRCUIT ASSEMBLY: A printed-circuit board on which separately manufactured parts have been added. Example: a ceramic substrate with screened conductors, screened resistors, screened inductors, and separate miniaturized capacitors.

PRINTED-CIRCUIT BOARD: A metallized conductor pattern deposited on a non-conductive board (substrate) to which printed-circuit elements may be deposited and discrete components may be attached to perform a circuit function.

PRINTED CONTACT: The portion of a printed circuit used to connect the circuit to a plug-in receptacle and to perform the function of a male pin of a connector.

PRINTED ELEMENT: An electrical element deposited on a printed-circuit board (substrate).

PRINTED WIRING: A pattern of conductors printed (screened) onto the surface of an insulating base in order to interconnect active and passive electronic devices to form an electronic circuit.

PRINTED-WIRING BOARD: A stiff, flat insulating base such as epoxy glass. A conductor pattern on the surface of one or two sides of the base is used to interconnect active and passive electronic devices to form an electronic circuit.

PRINTED-WIRING SUBSTRATE: A substrate on which the conductor pattern is printed.

P-TYPE CARRIERS: See HOLE CONDUCTION.

P-TYPE SEMICONDUCTOR: A semiconductor material which, in the electrically quiescent condition, contains hole carriers in excess of free electrons.

PURPLE PLAGUE: An expansive and brittle gold-aluminum intermetallic ($AuAl_2$) which often forms at an interface of a gold-aluminum thermocompression bond. This intermetallic

appears purple in the crystalline form.

PYROCERAM: A registered trade name by the Corning Glass Co. A devitrified solder glass used for fabricating glass seals and for die bonding.

PYROLITIC DEPOSITION: A type of thin-film deposition catalyzed by a heated substrate and resulting from the reaction of gaseous chemicals.

Q

QUADRUPLE-DIFFUSED TECHNIQUE: A technique used in fabrication of a monolithic integrated circuit. A fourth diffusion cycle is employed to yield both p-n-p and n-p-n types of transistors. See EPITAXIAL TRIPLE-DIFFUSED TECHNIQUE, DIFFUSED COLLECTOR TECHNIQUE, and ISOLATION DIFFUSION.

R

REACTIVE SPUTTERING: A sputtering technique in which reactive gasses such as oxygen, nitrogen, and hydrogen are purposely introduced into the glow discharge; and oxides, nitrides, and hydrides of the evaporant are consequently deposited on the substrate.

RECOMBINATION RATE (CARRIER): The time-rate at which free electrons and holes recombine.

RECOMBINATION RATE (BULK): The carrier recombination rate in the semiconductor bulk material. See RECOMBINATION RATE, CARRIER.

RECOMBINATION RATE (EFFECTIVE): The total apparent carrier recombination rate in a device, resulting from both surface and bulk recombination rate and the device geometry. See RECOMBINATION RATE, CARRIER.

RECOMBINATION RATE (SURFACE): The carrier recombination rate at the surface of a semiconductor material. See RECOMBINATION RATE, CARRIER.

REGISTER MARK: An alinement mark used to establish the relative positions of superimposed masks during device fabrication.

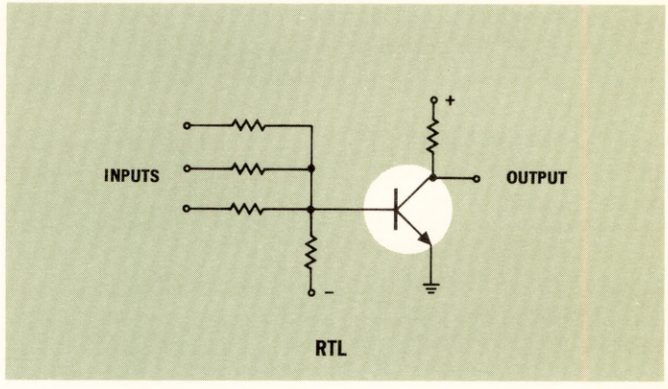
RESIST: A material used to selectively mask against etching or plating.

RESISTIVE PATTERN: An array of resistive elements on a substrate.

RESISTIVITY: The electrical resistance across the opposite faces of a cube of material.

REGISTRATIVE BONDING: A method of attaching a component die to a substrate by inverting the die and bonding the die contacts to the thin-film pads of the substrate. The term "flip-chip" is sometimes used synonymously with registrative bonding.

RTL (RESISTOR-TRANSISTOR LOGIC): A logic circuit using resistors for the input coupling to the base of a grounded-emitter transistor amplifier. See the following diagram.



S

SCRUBBED BOND: The attachment technique involving mechanical movement between the parts being bonded. Examples: sliding a tinned die with a tweezer, or ultrasonic movement of a die during use of an ultrasonic transducer.

SEMICONDUCTOR MATERIAL: A material in which the conductivity ranges between that of a conductor and an insulator. Semiconductor material has a negative resistance temperature coefficient over a given temperature range. The electrical characteristics of semiconductor materials (e.g., silicon, gallium arsenide, and cadmium sulphide) are dependent upon the small amounts of impurities (dopants) added.

SERIES-GATE DEVICE: A field-effect transistor in which the gates are placed in series between the source and drain.

SHEET RESISTIVITY: The electrical resistance measured across the opposite sides of a square of deposited thin-film material. Expressed in ohms per square.

SILICON MONOXIDE: A dielectric material often used in the fabrication of a microelectronic device to form an insulator, substrate, or a thin-film-capacitor dielectric.

SILICON OXIDE: A dielectric material commonly used in the surface passivation of microelectronic circuits. Silicon oxide contains various combinations of silicon monoxide and silicon dioxide.

SINGLE CRYSTAL: A monolithic material grown in such a manner that a regular molecular pattern is repetitive in three dimensions.

SLICE: See WAFER.

SOURCE: The region of a field-effect transistor in which the flow of majority carriers originates. The source corresponds to the emitter of a conventional transistor or the cathode of a vacuum tube.

SPIKE, DEVICE: A localized irregularity in an ohmic contact or junction, which may cause undesirable effects such as localized heating and secondary breakdown.

SPUTTERING: The ejection of atoms or molecules from the surface of a material, resulting from bombardment by atoms or ions and utilized as a source of material for thin-film deposition.

SPUTTERING, ANODIC: Sputtering in which the material

to be sputtered is the anode in a low-pressure glow discharge.

SPUTTERING, CATHODIC: Sputtering in which the material to be sputtered is the cathode in a low-pressure glow discharge.

STATES, SURFACE: Discontinuities and contaminants at the surface of a semiconductor device which tend to change the surface resistivity or the carrier mobility and lifetime. Surface states may cause inversion layers, accumulation layers, or device parameter instability.

STEP-AND-REPEAT TECHNIQUE: A mechanical technique providing for linear indexing of a movable platform to which a wafer or photographic plate is attached. This technique is utilized in the testing of a device wafer, or in the masking operation associated with the fabrication of microelectronic devices.

SUB-ELEMENT: A distinguishable portion of an element. Example: The base, collector, and emitter are sub-elements of a transistor.

SUBMINIATURIZATION: The technique of packaging miniaturized parts using unusual assembly techniques for increased volumetric efficiency. Example: cordwood.

SUBSTRATE: A material upon which epitaxial layers, thick-film depositions, or thin-film deposition are made, or within which diffusions are made. Examples: sapphire and glazed alumina.

SUHL (Sylvania Universal High-Level Logic): A trade name registered by the Sylvania Corporation. See TTL.

SURFACE INVERSION: See INVERSION LAYER.

SURFACE MOBILITY: Carrier mobility at the semiconductor surface. See MOBILITY, DRIFT.

SURFACE STABILIZATION: See PASSIVATION.

T

THERMOCOMPRESSION BONDING: The joining of materials by the combined effects of temperature and pressure.

THERMAL RESISTANCE (DEVICE): The ratio of the rise of the internal temperature of the device above its ambient or case temperature to the power dissipated within the device. Usually expressed as °C/W.

THICK-FILM CIRCUIT: Circuits fabricated utilizing the deposition of material having an approximate 0.5-mil thickness. Examples: stainless steel-screened circuits or etched Cermet circuits.

THIN-FILM CIRCUIT: A circuit fabricated by the deposition of material of several thousand Angstroms in thickness. Example: a circuit fabricated by vapor-deposition.

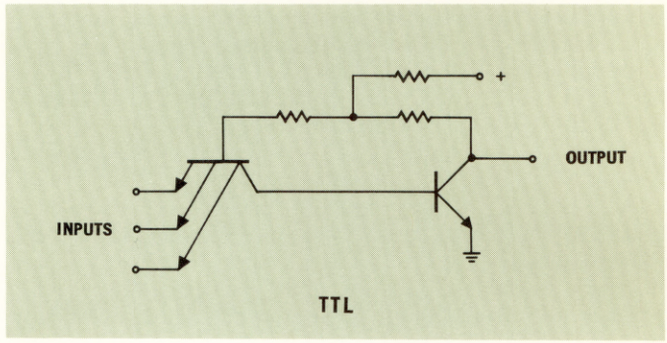
THIN-FILM FLIP-CHIP NETWORK: See REGISTRATIVE BONDING.

THRESHOLD VOLTAGE: The voltage which must be applied to the gate of a metal-oxide-semiconductor field-effect transistor to create a source-to-drain conduction path (channel).

TRANSCONDUCTANCE (FET): The ratio of the variation of the source-to-drain current to the corresponding variation of the gate-to-source voltage, with the output voltage held constant.

TRANSISTANCE: An electronic characteristic exhibited in the form of voltage or current gain, or in the ability to control voltages or currents in a precise manner.

TTL (TRANSISTOR-TRANSISTOR LOGIC): A logic circuit having all inputs connected to the multiple emitters of a single, common-base-connected transistor. The associated output transistor is used as an inverter amplifier as illustrated below.



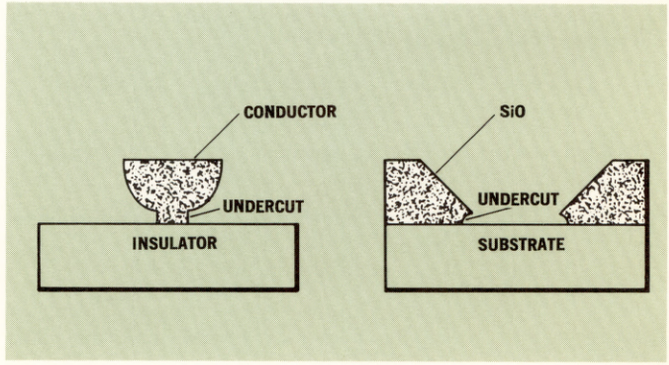
TUB: The region of a monolithic integrated circuit providing electrical isolation of the circuit elements by means of the high impedance of a reverse-biased p-n junction or dielectric material.

TURN-ON VOLTAGE: See THRESHOLD VOLTAGE.

U

ULTRASONIC ATTACHMENT: Die and lead attachments which utilize ultrasonic vibrations during the attachment operation.

UNDERCUT: The accentuation of etching at a material interface. This occurs during the etching of conductors and windows in a microelectronic device and is often due to residual etchants. See the following illustration.



UNDERPASS: See CROSSUNDER.

UNIPOLAR TRANSISTOR: A term occasionally applied to field-effect transistors, and used to differentiate between a field-effect transistor and a bipolar or conventional injection transistor.

V

VACUUM ALLOY PROCESS: An alloying process effected in a vacuum to reduce voids or prevent certain types of contaminants from entering the device.

VACUUM-DEPOSITION: See EVAPORATIVE DEPOSITION.

VAPOR-DEPOSITION: See VAPOR-PLATING.

VAPOR-PLATING: Deposition of a thin-film material precipitated from a chemical reaction between gaseous materials with the chemical reaction occurring in the vapor.

VOLTAGE BREAKDOWN: Rapid increase of current flow, from a relatively low value to a relatively high value, upon application of voltage to a p-n junction or dielectric.

VOLTAGE BREAKDOWN, AVALANCHE: A voltage breakdown that is due to the multiplication of carriers resulting from an accelerating field in a reverse-biased junction. This effect is similar to the "Townsend discharge" in vacuum tubes.

VOLTAGE BREAKDOWN (SECONDARY): A sudden reduction in the p-n junction breakdown voltage due to localized heating or imperfections in the device structure.

VOLTAGE BREAKDOWN (ZENER): A voltage breakdown resulting from the field emission of electrons when a material is exposed to a high-voltage field. Zener breakdown can occur in insulators and in low-resistivity, high-dopant-gradient semiconductor junctions.

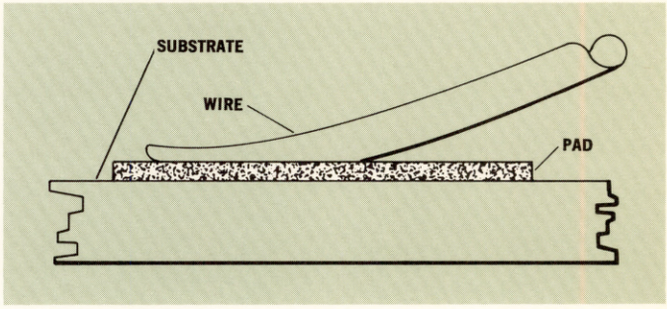
VOLTAGE, BREAKDOWN: See BREAKDOWN VOLTAGE.

W

WAFER: A piece of substrate or semiconductor material that is wafer-like. Example: a thin silicon slice whose large surface areas are essentially parallel. See DIE.

WAVE SOLDERING: A soldering process whereby a mechanically induced wave of molten solder is brought into contact with the conductive surface of a printed-wiring board or a substrate. The process also provides for the soldering of parts to the printed-wiring board or substrate.

WEDGE BOND: A type of lead bond which is bonded with a wedge-shaped tool. A wedge bond may be a cold-weld, an ultrasonic, or a thermocompression bond. See the following illustration.



about the author . . .

Martha Smith Parks was graduated from Stephens College and the University of Mississippi with majors in English and journalism. She studied electronics at the American Defense School, Memphis, Tennessee; the University of Cincinnati; and the Aircraft Radio Engineering School, Dayton, Ohio. Following graduation from the latter, she was retained by that Signal Corps-sponsored institution as an instructor in theory, operation, and maintenance of airborne radio and radar, and was subsequently made head instructor of the school's training program for radio engineering aides. During this same period, she was chief editor of the airborne radio maintenance manual prescribed for use in Federal depots throughout the United States. Upon completion of her assignment as head instructor at the Aircraft Radio Engineering School, she worked as a radio engineer, engaged in airborne electronics development at Wright Field, Ohio; as a nuclear research instrument design engineer at Oak Ridge National Laboratories, Oak Ridge, Tennessee; and as a missile test equipment development engineer at Capehart-Farnsworth, Ft. Wayne, Indiana. In 1955, she was brought to California by Hughes Aircraft Company to assist in development of test specifications for electronic components. Coming to the Autonetics Division of North American Aviation, Inc., in 1956, she has been able to combine journalism training with electronics engineering experience, as writer and writing supervisor for this technological organization.

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