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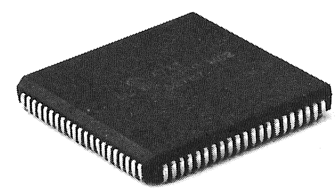
WE® DSP16A Digital Signal Processor

Description

The *WE* DSP16A Digital Signal Processor is a 16-bit high-speed programmable integrated circuit. The device is fabricated in low-power CMOS technology and is packaged in an 84-pin plastic leaded chip carrier. The DSP16A device is a general-purpose building block that can be programmed to perform a wide variety of signal processing functions. It achieves high throughput without programming restrictions or latencies due to its parallel pipelined architecture. The processor has an arithmetic unit capable of a 16- × 16-bit multiplication and 36-bit accumulation or a 32-bit ALU operation in one instruction cycle. Data is supplied by two independent addressing units. The DSP16A device can function in a stand-alone manner, requiring only an external clock.

The DSP16A contains twice the amount of ROM and four times the the amount of RAM as the DSP16 device, while maintaining pin, source code, and object code compatibility with the DSP16 device.



***WE* DSP16A Digital Signal Processor**
84-Pin Plastic Leaded Chip Carrier

Features

- Pin and instruction compatible with the *WE* DSP16 Digital Signal Processor
- Low-power CMOS technology
- 33-ns instruction cycle
- 16- × 16-bit multiplication and 36-bit accumulation in one instruction cycle
- Two 36-bit accumulators
- Instruction cache for high-speed, ROM-efficient, repetitive operations
- 4096-word ROM, 2048-word RAM (on-chip)
- Off-chip ROM expansion to 64K-word
- Serial and parallel I/O ports with multi-processor capability
- Maskable interrupts
- Single 5 V power supply
- Supported by *WE* DSP16A-SL Support Software Library and *WE* DSP16A-DS Digital Signal Processor Development System

User Information

Architectural Summary

The DSP16A device contains a data arithmetic unit (DAU) that performs signal processing arithmetic, a ROM address arithmetic unit (XAAU), a RAM address arithmetic unit (YAAU), a 4096 × 16-bit ROM that contains program instructions and fixed data, a 2048 × 16-bit RAM for variable data, an instruction cache (CACHE), a serial I/O unit (SIO), and a 16-bit parallel I/O unit (PIO).

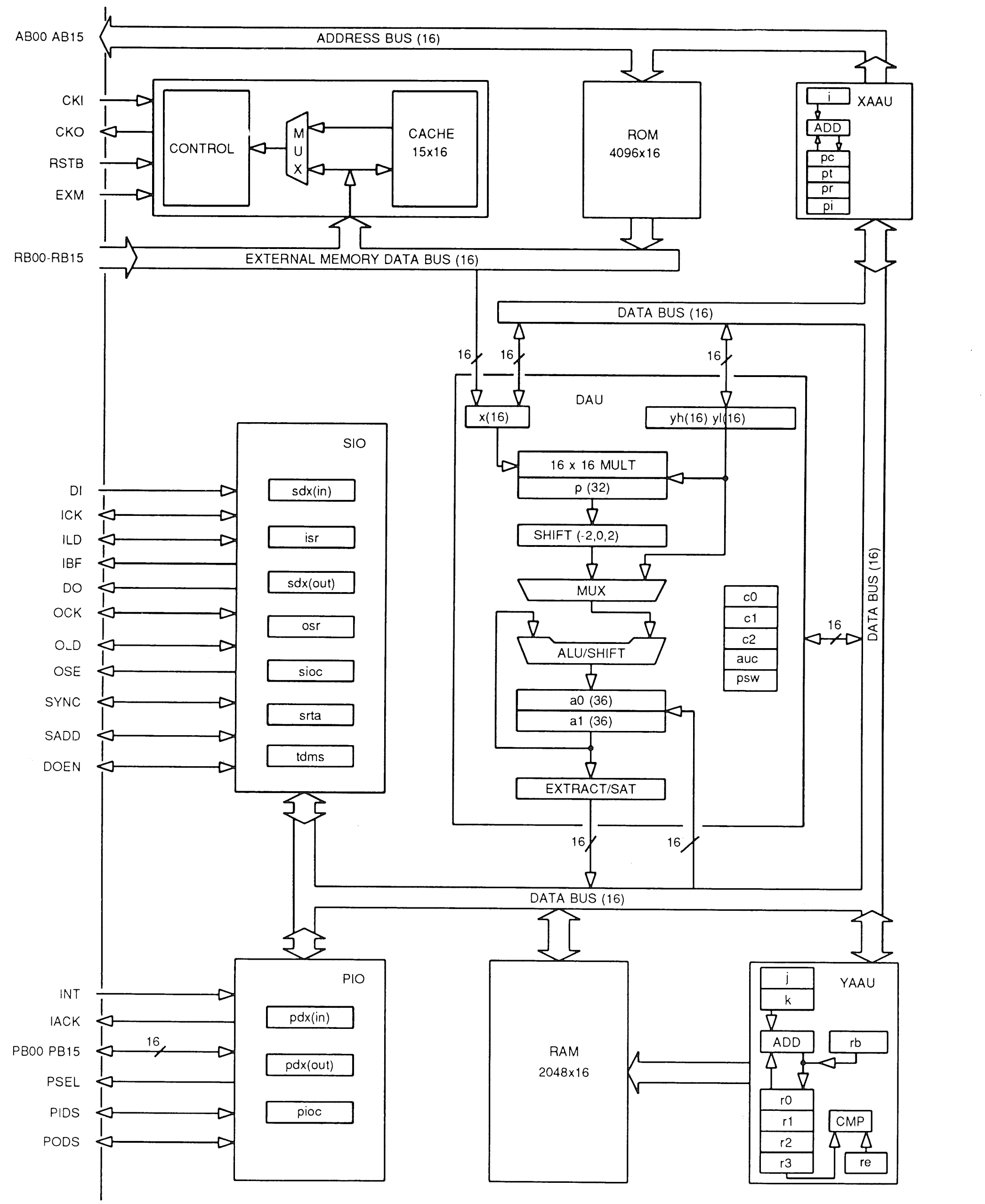
The arithmetic unit contains a 16- × 16-bit parallel multiplier that generates a full 32-bit product in one instruction cycle. The product can be accumulated with one of two 36-bit accumulators. The data in these accumulators can be directly loaded from or stored to memory in two 16-bit words with automatic saturation on overflow. The ALU supports a full set of arithmetic and logical operations on either 16- or 32-bit data. A standard set of ALU conditions can be tested for conditional ALU operations, branches, and subroutine calls. This procedure allows the processor to perform as a powerful 16- or 32-bit microprocessor for logical and control applications.

Two addressing units support high-speed, register-indirect, memory addressing with postmodification of the register. Direct and immediate addressing is supported at the cost of only one additional instruction cycle and ROM location. Four address registers in the YAAU (r0—r3) can be used for either read or write addresses to the RAM without restrictions. Registers j and k provide user-defined post-increments for the addresses. Fixed increments of +1, −1, and +2 are also available. The YAAU also supports a flexible modulo addressing mode for efficient filter implementations. Registers rb and re are used to define the beginning and end of the modulo. Four compound addressing modes are provided to make read/write operations more efficient. In the XAAU, the register pt is used for ROM table look-up, and register i is used to hold a user-defined post-increment. A fixed post-increment of +1 is also available. Register pc is the program counter. Registers pr and pi hold the return address for subroutine calls and interrupts, respectively.

The on-chip memory includes 4096 × 16-bit words of ROM and 2048 × 16-bit words of RAM. The on-chip ROM can be augmented with up to 60K words of external memory or can be replaced by up to 64K words of external memory for prototyping or for applications that require a large program space or frequent modification. When the internal ROM is selected by the EXM pin and a memory location outside the 4K of internal ROM is accessed, the external memory interface is automatically selected.

An on-chip memory cache can be selectively used to store such repetitive operations as those found in a filter section. Up to 15 words in the cache can be repeated up to 127 times with no looping overhead. In addition, operations in the cache that require a ROM access (for example, reading fixed coefficients) execute at twice the normal rate. The cache greatly reduces the need for writing repetitive code in-line and, therefore, conserves ROM storage.

The DSP16A device has both serial and parallel I/O ports. The serial I/O unit is an asynchronous, full duplex, double-buffered channel operating at up to 10 Mbits/s that easily interfaces with other DSP16A devices in a multiple DSP16A environment. Commercially available codecs and time division multiplex (TDM) channels can be interfaced to the DSP16A device with few (if any) additional components. The parallel I/O unit is capable of interfacing to a 16-bit bus containing other DSP16A devices, microprocessors, or peripheral I/O devices. Data rates of up to 30 Mbytes/s are obtainable through this port.



Note: See Table 15 for signal name definitions.

Legend:

16 x 16 Mult	16-bit by 16-bit Multiplier
a0—a1	Accumulators 0–1
ADD	Adder
ALU/SHIFT	Arithmetic Logic Unit/Shifter
auc	Arithmetic Unit Control
c0—c2	Counters 0–2
CMP	Comparator
DAU	Data Arithmetic Unit
i	Increment Register
isr	Input Shift Register
j	Increment Register
k	Increment Register
MUX	Multiplexer
osr	Output Shift Register
p	Product Register
pc	Program Counter
pdx(in)	Parallel I/O Data Transmit Input Register
pdx(out)	Parallel I/O Data Transmit Output Register
pi	Program Interrupt Register
PIO	Parallel I/O Unit
pioc	Parallel I/O Control Register
pr	Program Return Register
psw	Processor Status Word
pt	ROM Table Pointer
r0—r3	RAM Pointer Registers 0—3
RAM	Read/Write Memory
rb	Modulo Addressing Register
re	Modulo Addressing Register
ROM	Read-Only Memory
sdx(in)	Serial Data Transmit Input Register
sdx(out)	Serial Data Transmit Output Register
SIO	Serial I/O Unit
sioc	Serial I/O Control Register
srta	Serial Receive/Transmit Address Register
tdms	Serial I/O Time-Division Multiplex Signal Control Register
x	Multiplier Input Register
XAAU	ROM Address Arithmetic Unit
YAAU	Ram Address Arithmetic Unit
yh	y(High) DAU Register
yl	y(Low) DAU Register

Figure 1. Block Diagram

The DSP16A device has a maskable interrupt that can be generated by the user or by any of four I/O conditions: input buffer full (IBF), output buffer empty (OBE), parallel input data strobe (PIDS), and parallel output data strobe (PODS).

Note: Branch instructions and cache operations are protected from interrupts.

Instruction Set

The DSP16A processor has five types of instructions: multiply/ALU, special function, control, cache, and data move. The multiply/ALU instructions are the primary instructions used to implement signal processing algorithms. Statements from this group can be combined to generate multiply/accumulate, logical, and other ALU functions and to transfer data between memory and registers in the data arithmetic unit. The special function instructions can be conditionally executed based on flags from the previous ALU operation, the condition of one of the counters, or the value of a randomly set bit in the DSP16A device. The control instructions implement the goto and call commands. Control instructions can also be executed conditionally. Cache instructions are used to implement low-overhead loops, conserve program memory, and decrease the execution time of certain multiply/ALU instructions. Data move instructions are used to transfer data between memory and registers or between accumulators and registers.

The following operators are used in describing the instruction set:

*	16- × 16-bit → 32-bit multiplication (Denotes register-indirect addressing when used as a prefix to an address register)
+	36-bit addition
-	36-bit subtraction
>>	Arithmetic right shift
<<	Logical left shift
|	32-bit bitwise OR
&	32-bit bitwise AND
^	32-bit bitwise EXCLUSIVE OR
:	Compound address swapping

Multiply/ALU Instructions

Note that the function statements and transfer statements in Table 1 are chosen independently. Any function statement may be combined with any transfer statement to form a valid muliply/ALU instruction. If either statement is not required, a single statement from either column constitutes a valid instruction. The number of cycles to execute the instruction is a function of the transfer column. (An instruction with no transfer statement executes in one instruction cycle.) All multiply/ALU instructions require 1 word of program memory.

Table 1. Multiply/ALU Instructions

Function Statements		Transfer Statements†		Transfer Cycles Out/In Cache
	p=x*y	y=Y	x=X	2/1
aD=p	p=x*y	y=aT	x=X	2/1
aD=aS+p	p=x*y	y[l]=Y		1/1
aD=aS−p	p=x*y	aT[l]=Y		1/1
aD=p		x=Y		1/1
aD=aS+p		Y		1/1
aD=aS−p		Y=y[l]		2/2
aD=y		Y=aT[l]		2/2
aD=aS+y		Z: y	x=X	2/2
aD=aS−y		Z: y[l]		2/2
aD=aS&y		Z: aT[l]		2/2
aD=aS|y				
aD=aS^y				
aS−y				
aS&y				

† Brackets, [ ], indicate an optional argument and are not part of the instruction syntax. The l argument designates the low 16-bits of aT or y.

Table 2. Replacement Table for Multiply/ALU Instructions

Replace	Value†	Meaning
aD aS aT	a0, a1	One of two DAU accumulators.
X	*pt++,*pt++i	ROM location pointed to by pt. pt is postmodified by +1 and i, respectively.
Y	*rM, *rM++, *rM−−, *rM++j	RAM location pointed to by rM (M = 0, 1, 2, 3). rM is postmodified by 0,+1,−1, or j, respectively.
Z	*rMzp, *rMpz, *rMm2, *rMjk	Read/write compound addressing. rM (M = 0, 1, 2, 3) is used twice. First, post-modified by 0, +1, −1, or j, respectively and, second, postmodified by +1, 0, +2, or k, respectively.

† When loading the upper half of a0, a1, or y, the lower half of the register is cleared if the corresponding CLR bit in the AUC register is zero. See the Register Settings section.

Special Function Instructions

All forms of the special function instructions execute in one instruction cycle:

aD=aS>>1 aD=aS>>4 aD=aS>>8 aD=aS>>16	Arithmetic right shift (sign preserved) of 36-bit accumulators
aD=aS	
aD=–aS	
aD=rnd(aS)	– Round upper 20-bits of accumulator
aDh=aSh+1	– Increment upper half of accumulator (lower half cleared)
aD=aS+1	– Increment accumulator
aD=y	
aD=p	
aD=aS<<1 aD=aS<<4 aD=aS<<8 aD=aS<<16	Logical left shift (sign not preserved) of the lower 32 bits of accumulators (upper 4-bits are sign-bit-extended from bit 31 at the completion of the shift)

The above special functions can be conditionally executed

    if CON instruction

and with an event counter

    ifc CON instruction

which means:

```
if CON is true then
        c1=c1+1
        instruction
        c2=c1
else
        c1=c1+1
```

Table 3. Replacement Table for Special Function Instructions

Replace	Value	Meaning
aD aS	a0, a1	One of two DAU accumulators
CON	mi, pl, eq, ne, gt, le, lvs, mvs, mvc, c0ge, c0lt, c1ge, c1lt, heads, tails, true, false	See Table 7 for definitions of mnemonics

Control Instructions

All unconditional control instructions execute in 2 instruction cycles and require one word of program memory; conditional control instructions execute in 3 instruction cycles and require two words of program memory.

```
goto JA
goto pt
call JA
call pt
icall
return     (goto  pr)
ireturn    (goto  pi)
```

The above control instructions, with the exception of ireturn and icall can be conditionally executed. For example:

```
If CON goto JA
```

Table 4. Replacement Table for Control Instructions

Replace	Value	Meaning
CON	mi, pl, eq, ne, gt, le, lvs, mvs, mvc, c0ge, c0lt, c1ge, c1lt, heads, tails, true, false	See Table 7 for definitions of mnemonics
JA	12-bit value	Least significant 12 bits of absolute address within the same 4 K-word memory section

Cache Instructions

Cahce instructions require one word of program memory. The do instruction executes in one instruction cycle; the redo instruction executes in two instruction cycles. The instruction formats are:

```
do K {inst1, instr2, ..., instrNI}
redo K
```

Table 5. Replacement Table for Cache Instructions

Replace	Value	Meaning
K	$2 \leq K \leq 127$	Number of times the instructions are to be executed
NI	$1 \leq N \leq 15$	1 to 15 instructions may be included

Data Move Instructions

Data move instructions execute in two instruction cycles. Immediate data move instructions require two words of program memory; all other data move instructions require only one word. The only exception to these statements is a special case immediate load (short immediate) instruction. If a YAAU register is loaded with a 9 bit or smaller value, the instruction requires only one word of memory and executes in one instruction cycle. The data move instructions are:

R = N	aT = R
R = M	Y = R
R = Y	Z : R
R = aS	

Table 6. Replacement Table for Data Move Instructions

Replace	Value*	Meaning**, †
R	x, y yl auc c0, c1, c2	DAU registers – signed, 16 bits DAU register – unsigned, 16 bits DAU control register – unsigned, 7 bits DAU counters – signed, 8 bits
	r0, r1, r2, r3 rb, re j, k	YAAU pointer registers – unsigned, 16 bits YAAU modulo addressing registers – unsigned, 16 bits YAAU increment registers – signed, 16 bits
	pt, pr, pi i	XAAU pointer registers – unsigned, 16 bits XAAU increment register – signed, 12 bits
	psw	Processor status word
	sioc sdx tdms srta	Serial I/O control register Serial I/O data register Serial I/O TDMS control register Serial receive/transmit address
	pioc pdx0 pdx1	Parallel I/O control register Parallel I/O data register with PSEL = 0 (pin 72) Parallel I/O data register with PSEL = 1 (pin 72)
aD, aS, aT	a0, a1	High half of accumulator
Y	*rM,*rM++, *rM––,*rM++j	Same as in multiply/ALU instructions
Z	*rmZp,*rMpz, *rMm2,*rMjk	Same as in multiply/ALU instructions
N	16-bit value	Immediate data
M	9-bit value	Immediate data for YAAU registers

* sioc, tdms, and srta registers are not readable.
** When signed registers less than 16 bits wide are read, their contents are sign-extended to 16 bits. When unsigned registers less than 16 bits wide are read, their contents are zero-extended to 16 bits.
† Loading an accumulator with a data move instruction does not effect the flags.

Conditional Mnemonics

Table 7 lists mnemonics used in conditional execution of special function and control instructions.

Table 7. DSP16A Conditional Mnemonics

Test	Meaning	Test	Meaning
pl	Result is nonnegative (sign bit is bit 35)	mi	Result is negative
eq	Result is equal to zero	ne	Result is not equal to zero
gt	Result is greater than zero	le	Result is less than or equal to zero
lvs	Logical overflow set*	lvc	Logical overflow clear
mvs	Mathematical overflow set**	mvc	Mathematical overflow clear
c0ge	Counter 0 greater than or equal to zero	c0lt	Counter 0 less than zero
c1ge	Counter 1 greater than or equal to zero	c1lt	Counter 1 less than zero
heads	Pseudorandom sequence bit set	tails	Pseudorandom sequence bit clear
true	The condition is always satisfied in an if instruction	false	The condition is never satisfied in an if instruction

* Result is not representable in the 36-bit accumulators.
** Bits 35—31 are not the same.

Register Settings

Tables 8 through 13 show how to set various operating conditions for the DSP16A device.

Note that the following abbreviations are used in the tables:

x = don't care
R = read only
W = read/write

Table 8. Serial I/O Control (SIOC) Register

Bit	9	8	7	6	5	4	3	2	1	0
Field	LD	CLK		MSB	OLD	ILD	OCK	ICK	OLEN	ILEN

Field	Value	Description
LD	0	Active ILD/OLD = ICK ÷ 16, active SYNC = ICK ÷ 128/256*
	1	Active ILD/OLD = OCK ÷ 16, active SYNC = OCK ÷ 128/256*
CLK	0 0	Active clock = CKI ÷ 4
	0 1	Active clock = CKI ÷ 12
	1 0	Active clock = CKI ÷ 16
	1 1	Active clock = CKI ÷ 20
MSB	0	LSB first
	1	MSB first
OLD	0	OLD is an input (passive mode)
	1	OLD is an output (active mode)
ILD	0	ILD is an input (passive mode)
	1	ILD is an output (active mode)
OCK	0	OCK is an input (passive mode)
	1	OCK is an output (active mode)
ICK	0	ICK is an input (passive mode)
	1	ICK is an output (active mode)
OLEN	0	16-bit output
	1	8-bit output
ILEN	0	16-bit input
	1	8-bit input

* See tdms register, SYNC field.

Table 9. Time-Division Multiplex Slot (TDMS) Register

Bit	9	8	7	6	5	4	3	2	1	0
Field	SYNCSP	MODE	TRANSMIT SLOT							SYNC

Field	Value	Description
SYNCSP	0	SYNC = ICK/OCK* ÷ 128**
	1	SYNC = ICK/OCK* ÷ 256
MODE	0	Multiprocessor mode off, DOEN is an input (passive mode)
	1	Multiprocessor mode on, DOEN is an output (active mode)
TRANSMIT SLOT	1xxxxxx	Transmit slot 7
	x1xxxxx	Transmit slot 6
	xx1xxxx	Transmit slot 5
	xxx1xxx	Transmit slot 4
	xxxx1xx	Transmit slot 3
	xxxxx1x	Transmit slot 2
	xxxxxx1	Transmit slot 1
SYNC	1	Transmit slot 0, SYNC is an output (active mode)
	0	SYNC is an input (passive mode)

* See sioc register, LD field.
** Select this mode when in multiprocessor mode.

Table 10. Serial Receive/Transmit Address (SRTA) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	RECEIVE ADDRESS								TRANSMIT ADDRESS							

Field	Value	Description
RECEIVE ADDRESS	1xxxxxxx	Receive address 7
	x1xxxxxx	Receive address 6
	xx1xxxxx	Receive address 5
	xxx1xxxx	Receive address 4
	xxxx1xxx	Receive address 3
	xxxxx1xx	Receive address 2
	xxxxxx1x	Receive address 1
	xxxxxxx1	Receive address 0
TRANSMIT ADDRESS	1xxxxxxx	Transmit address 7
	x1xxxxxx	Transmit address 6
	xx1xxxxx	Transmit address 5
	xxx1xxxx	Transmit address 4
	xxxx1xxx	Transmit address 3
	xxxxx1xx	Transmit address 2
	xxxxxx1x	Transmit address 1
	xxxxxxx1	Transmit address 0

Table 11. Processor Status Word (PSW) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	DAU Flags				X	X	a1[V]	a1[35—32]				a0[V]	a0[35—32]			

Field	Value	Description
DAU Flags	Wxxx	LMI – logical minus when set
	xWxx	LEQ – logical equal when set
	xxWx	LLV – logical overflow when set
	xxxW	LMV – mathematical overflow when set
a1[V]	W	Accumulator 1 (a1) overflow when set
a1[35—32]	Wxxx	Accumulator 1 (a1) bit 35
	xWxx	Accumulator 1 (a1) bit 34
	xxWx	Accumulator 1 (a1) bit 33
	xxxW	Accumulator 1 (a1) bit 32
a0[V]	W	Accumulator 0 (a0) overflow when set
a0[35—32]	Wxxx	Accumulator 0 (a0) bit 35
	xWxx	Accumulator 0 (a0) bit 34
	xxWx	Accumulator 0 (a0) bit 33
	xxxW	Accumulator 0 (a0) bit 32

Table 12. Arithmetic Unit Control (AUC) Register

Bit	6	5	4	3	2	1	0
Field	CLR			SAT		ALIGN	

Field	Value	Description
CLR	1xx	Clearing yl is disabled (enabled when 0)
	x1x	Clearing a1l is disabled (enabled when 0)
	xx1	Clearing a0l is disabled (enabled when 0)
SAT	1x	a1 saturation on overflow is disabled (enabled when 0)
	x1	a0 saturation on overflow is disabled (enabled when 0)
ALIGN	00	$p \leftarrow (x \times y)$
	01	$p \leftarrow (x \times y) \div 4$
	10	$p \leftarrow (x \times y) \times 4$
	11	Reserved

Table 13. Parallel I/O Control (PIOC) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	IBF	STROBE		PODS	PIDS	S/C	INTERRUPTS					STATUS				

Field	Value	Description
IBF	R	IBF interrupt status bit (same as bit 4)
STROBE		Strobe width of:
		PODS **PIDS**
	00	T* T
	01	2T 2T
	10	3T 3T
	11	4T 4T
PODS	0	PODS is an input (passive mode)
	1	PODS is an output (active mode)
PIDS	0	PIDS is an input (passive mode)
	1	PIDS is an output (active mode)
S/C	0	Not status/control mode
	1	Status/control mode
INTERRUPTS	1xxxx	IBF interrupt enabled (disabled when 0)
	x1xxx	OBE interrupt enabled (disabled when 0)
	xx1xx	PIDS interrupt enabled (disabled when 0)
	xxx1x	PODS interrupt enabled (disabled when 0)
	xxxx1	INT interrupt enabled (disabled when 0)
STATUS	Rxxxx	IBF status bit
	xRxxx	OBE status bit
	xxRxx	PIDS status bit
	xxxRx	PODS status bit
	xxxxR	INT status bit

* T = 2 × tCKIHCKIH. See Figure 3.

Instruction Set Formats

This section defines the hardware-level encoding of the DSP16A device instructions.

Multiply/ALU Instructions

Format 1: Multiply/ALU Read/Write Group:

Field	T					D	S	F1				X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 1a: Multiply/ALU Read/Write Group:

Field	T					a$\overline{T}$	S	F1				X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 2: Multiply/ALU Read/Write Group:

Field	T					D	S	F1				X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 2a: Multiply/ALU Read/Write Group:

Field	T					a$\overline{T}$	S	F1				X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Special Function Instructions

Format 3: Special Functions

Field	T					D	S	F2				CON				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Control Instructions

Format 4: Branch Direct Group:

Field	T1				JA											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 5: Branch Indirect Group:

Field	T					B										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 6: Conditional Branch Qualifier/Software Interrupt (icall):
Note that a branch instruction immediately follows except for a software interrupt (icall).

Field	T					SI						C				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Data Move Instructions

Format 7: Data Move Group:

Field	T					$\overline{aT}$	R						Y/Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 8: Data Move (immediate operand - 2 words)

Field	T					D	R						Y			
	Immediate Operand															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 9: Short Immediate Group:

Field	T					I		Short Immediate Operand								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Cache Instructions

Format 10: D0 — Redo

Field	T					NI				K						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Field Descriptions

T Field. Specifies the type of instruction.

T	Operation	Format
0000x	goto JA	4
00010	Short imm j, k, rb, re	9
00011	Short imm r0, r1, r2, r3	9
00100	Y=a1 F1	1
00101	Z : aT F1	2a
00110	Y F1	1
00111	aT=Y F1	1a
01000	aT=R	7
01001	R=a0	7
01010	R=imm	8
01011	R=a1	7
01100	Y=R	7
01101	Z : R	7
01110	Do, redo	10
01111	R=Y	7
1000x	call JA	4
10010	ifc CON F2	3
10011	if CON F2	3
10100	Y=y F1	1
10101	Z : y F1	2
10110	x=Y F1	1
10111	y=Y F1	1
11000	Branch indirect	5
11001	y=a0 x=X F1	1
11010	Cond. branch qualifier	6
11011	y=a1 x=X F1	1
11100	Y=a0 F1	1
11101	Z : y x=X F1	2
11110	Reserved	—
11111	y=Y x=X F1	1

* imm = immediate.

D Field. Specifies a destination accumulator.

D	Register
0	Accumulator 0
1	Accumulator 1

$\overline{aT}$ Field. Specifies transfer accumulator.

$\overline{aT}$	Register
0	Accumulator 1
1	Accumulator 0

S Field. Specifies a source accumulator.

S	Register
0	Accumulator 0
1	Accumulator 1

F1 Field. Specifies the multiply/ALU function.

F1	Operation	
0000	aD=p	p=x*y
0001	aD=aS+p	p=x*y
0010		p=x*y
0011	aD=aS–p	p=x*y
0100	aD=p	
0101	aD=aS+p	
0110	NOP	
0111	aD=aS–p	
1000	aD=aS|y	
1001	aD=aS^y	
1010	aS&y	
1011	aS–y	
1100	aD=y	
1101	aD=aS+y	
1110	aD=aS&y	
1111	aD=aS–y	

X Field. Specifies the addressing of ROM data in two-operand multiply/ALU instructions. Specifies the high or low half of an accumulator or the y register in one-operand multiply/ALU instructions.

X	Operation
Two-Operand Multiply/ALU	
0	*pt++
1	*pt++i
One-Operand Multiply/ALU	
0	aTl, yl
1	aTh, yh

Y Field. Specifies the form of register indirect addressing with postmodification.

Y	Operation
0000	*r0
0001	*r0++
0010	*r0––
0011	*r0++j
0100	*r1
0101	*r1++
0110	*r1––
0111	*r1++j
1000	*r2
1001	*r2++
1010	*r2––
1011	*r2++j
1100	*r3
1101	*r3++
1110	*r3––
1111	*r3++j

Z Field. Specifies the form of register indirect compound addressing with postmodification.

Z	Operation
0000	*r0zp
0001	*r0pz
0010	*r0m2
0011	*r0jk
0100	*r1zp
0101	*r1pz
0110	*r1m2
0111	*r1jk
1000	*r2zp
1001	*r2pz
1010	*r2m2
1011	*r2jk
1100	*r3zp
1101	*r3pz
1110	*r3m2
1111	*r3jk

F2 Field. Specifies the special function to be performed.

F2	Operation
0000	aD=aS>>1
0001	aD=aS<<1
0010	aD=aS>>4
0011	aD=aS<<4
0100	aD=aS>>8
0110	aD=aS>>16
0111	aD=aS<<16
1000	aD=p
1001	aDh=aSh+1
1010	Reserved
1011	aD=rnd(aS)
1100	aD=y
1101	aD=aS+1
1110	aD=aS
1111	aD=–aS

C Field. Specifies the condition for special functions and conditional control instructions.

CON	Condition
00000	mi
00001	pl
00010	eq
00011	ne
00100	lvs
00101	lvc
00110	mvs
00111	mvc
01000	heads
01001	tails
01010	c0ge
01011	c0lt
01100	c1ge
01101	c1lt
01110	true
01111	false
10000	gt
10001	le
Other codes	Reserved

B Field. Specifies the type of branch instruction (except software interrupt).

B	Operation
000	return
001	ireturn
010	goto pt
011	call pt
1xx	Reserved

R Field. Specifies the register for data move instructions.

R	Register
000000	r0
000001	r1
000010	r2
000011	r3
000100	j
000101	k
000110	rb
000111	re
001000	pt
001001	pr
001010	pi
001011	i
010000	x
010001	y
010010	yl
010011	auc
010100	psw
010101	c0
010110	c1
010111	c2
011000	sioc
011001	srta
011010	sdx
011011	tdms
011100	pioc
011101	pdx0
011110	pdx1
Other codes	Reserved

I Field. Specifies a register for short immediate data move instructions.

I	Register
00	r0/j
01	r1/k
10	r2/rb
11	r3/re

SI Field. Specifies when the conditional branch qualifier instruction should be interpreted as a software interrupt instruction.

SI	Operation
0	Not a software interrupt
1	Software interrupt

NI Field. Number of instructions to be loaded into the cache. Zero implies redo operation.

K Field. Number of times the NI instructions in cache are to be executed.

JA Field. 12-bit jump address.

Pin Descriptions

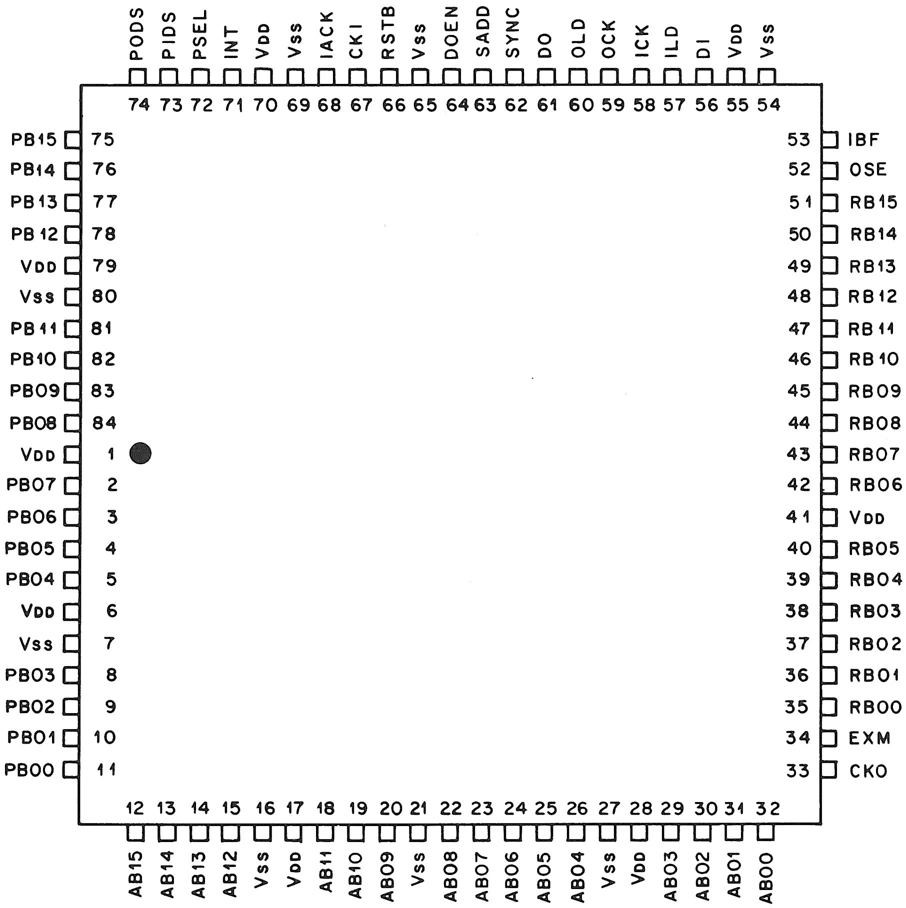


Figure 2. Pin Diagram

Table 14. Pin Names

Symbol	Pin	Symbol	Pin
AB00—AB15	32—29, 26—22, 20—18, 15—12	OLD	60
		OSE	52
CKI	67	PB00—PB15	11—8, 5—2, 84—81, 78—75
CKO	33		
DI	56		
DO	61	PIDS	73
DOEN	64	PODS	74
EXM	34	PSEL	72
IACK	68	RB00—RB15	35—40, 42—51
IBF	53	RSTB	66
ICK	58	SADD	63
ILD	57	SYNC	62
INT	71	VDD	1, 6, 17, 28, 41, 55, 70, 79
OCK	59	Vss	7, 16, 21, 27, 54, 65, 69, 80

In the following table, I = input, 0 = output, and P = power

Table 15. Pin Descriptions

Pin	Symbol	Type	Name/Description
1	VDD	P	**5 V Supply.**
2	PB07	I/O*	**Parallel I/O Data Bus — Bit 7.**
3	PB06	I/O*	**Parallel I/O Data Bus — Bit 6.**
4	PB05	I/O*	**Parallel I/O Data Bus — Bit 5.**
5	PB04	I/O*	**Parallel I/O Data Bus — Bit 4.**
6	VDD	P	**5 V Supply.**
7	VSS	P	**Ground.**
8	PB03	I/O*	**Parallel I/O Data Bus — Bit 3.**
9	PB02	I/O*	**Parallel I/O Data Bus — Bit 2.**
10	PB01	I/O*	**Parallel I/O Data Bus — Bit 1.**
11	PB00	I/O*	**Parallel I/O Data Bus — Bit 0.**
12	AB15	O*	**ROM Address Bus — Bit 15.**
13	AB14	O*	**ROM Address Bus — Bit 14.**
14	AB13	O*	**ROM Address Bus — Bit 13.**
15	AB12	O*	**ROM Address Bus — Bit 12.**
16	VSS	P	**Ground.**
17	VDD	P	**5 V Supply.**
18	AB11	O*	**ROM Address Bus — Bit 11.**
19	AB10	O*	**ROM Address Bus — Bit 10.**
20	AB09	O*	**ROM Address Bus — Bit 9.**
21	VSS	P	**Ground.**
22	AB08	O*	**ROM Address Bus — Bit 8.**
23	AB07	O*	**ROM Address Bus — Bit 7.**
24	AB06	O*	**ROM Address Bus — Bit 6.**
25	AB05	O*	**ROM Address Bus — Bit 5.**
26	AB04	O*	**ROM Address Bus — Bit 4.**
27	VSS	P	**Ground.**
28	VDD	P	**5 V Supply.**
29	AB03	O*	**ROM Address Bus — Bit 3.**
30	AB02	O*	**ROM Address Bus — Bit 2.**
31	AB01	O*	**ROM Address Bus — Bit 1.**
32	AB00	O*	**ROM Address Bus — Bit 0.**
33	CKO	O*	**Clock Out.** Buffered clock at half the frequency of CKI.
34	EXM	I	**External Memory.** When low, internal ROM is accessed for addresses 0x0000—0x0FFF and external ROM is accessed for addresses 0x1000—0xFFFF. If EXM is high, instructions and coefficients are fetched from external ROM (internal ROM disabled).

* Indicates 3-state condition.

Table 15. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Description
35	RB00	I	**ROM Data Bus — Bit 0.**
36	RB01	I	**ROM Data Bus — Bit 1.**
37	RB02	I	**ROM Data Bus — Bit 2.**
38	RB03	I	**ROM Data Bus — Bit 3.**
39	RB04	I	**ROM Data Bus — Bit 4.**
40	RB05	I	**ROM Data Bus — Bit 5.**
41	VDD	P	**5 V Supply.**
42	RB06	I	**ROM Data Bus — Bit 6.**
43	RB07	I	**ROM Data Bus — Bit 7.**
44	RB08	I	**ROM Data Bus — Bit 8.**
45	RB09	I	**ROM Data Bus — Bit 9.**
46	RB10	I	**ROM Data Bus — Bit 10.**
47	RB11	I	**ROM Data Bus — Bit 11.**
48	RB12	I	**ROM Data Bus — Bit 12.**
49	RB13	I	**ROM Data Bus — Bit 13.**
50	RB14	I	**ROM Data Bus — Bit 14.**
51	RB15	I	**ROM Data Bus — Bit 15.**
52	OSE	O*	**Output Shift Register Empty.** Indicates the end of a serial transmission. OSE is set either by the emptying of the output shift register or by asserting RSTB. OSE is reset by the DSP16A writing a word (two clock cycles after the falling edge of OLD) to the output shift register. If no new word is written by the DSP16A, OSE remains high regardless of activity on OLD.
53	IBF	O*	**Input Buffer Full.** IBF is asserted when the input buffer is filled and negated by a read of the buffer. IBF is also negated by asserting RSTB.
54	VSS	P	**Ground.**
55	VDD	P	**5 V Supply.**
56	DI	I	**Data Input.** Serial PCM data latched on rising edge of ICK, either LSB or MSB first, according to the sioc register MSB field.
57	ILD	I/O*	**Input Load.** Falling edge of ILD indicates the beginning of a serial input word. In active mode, ILD is an output; in passive mode, ILD is an input, according to the sioc register ILD field.
58	ICK	I/O*	**Input Clock.** Clock for serial PCM input data. In active mode, ICK is an output; in passive mode, ICK is an input, according to the sioc ICK field.
59	OCK	I/O*	**Output Clock.** Clock for serial PCM output data. In active mode, OCK is an output; in passive mode, OCK is an input, according to the sioc register OCK field.

* Indicates 3-state condition.

Table 15. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Description
60	OLD	I/O*	**Output Load.** Clock for loading the parallel-to-serial converter from the output buffer (obuf). A falling edge of OLD indicates the beginning of a serial output word. In active mode, OLD is an output; in passive mode, OLD is an input, according to the sioc register OLD field.
61	DO	O*	**Data Output.** Serial PCM data output from the output shift register (osr), either LSB or MSB first, according to the sioc register MSB field. DO changes on the rising edges of OCK. DO is 3-stated when DOEN is high.
62	SYNC	I/O*	**Multiprocessor Synchronization.** Typically used in the multiprocessor mode. A falling edge of SYNC indicates the first word of a TDM I/O stream and causes the resynchronization of the active ILD and OLD generators. SYNC is an output when the tdms register SYNC field is set; otherwise, it is an input. SYNC must be tied low if it is not used as an output. When used as an output, SYNC = ILD/OLD ÷ 8 or 16, depending on the setting of the SYNCSP field of the tdms register. This procedure can be used to generate a slow clock for SIO operation.
63	SADD	I/O*	**Serial Address.** An 8-bit serial bit stream typically used for addressing during multiprocessor communication between multiple DSP16A devices. In multiprocessor mode, SADD is an output when the tdms time slot dictates a serial transmission; otherwise, it is an input. SADD is always an output when not in multiprocessor mode. SADD is 3-stated when DOEN is high.
64	DOEN	I/O*	**Data Output Enable (Active Low).** An input when not in the multiprocessor mode. DO and SADD are enabled only if DOEN is low. DOEN is an output when in the multiprocessor mode (tdms register MODE field set). In the multiprocessor mode, DOEN indicates a valid time slot for a serial output.
65	Vss	P	**Ground.**
66	RSTB	I	**Reset.** A high-to-low transition causes entry into the reset state. The sioc, pioc, tdms, rb, and re register bits are cleared. Reset clears external flags IACK and IBF and sets external flag OSE. DAU condition flags and the DAUC register are not affected by reset. All output and bidirectional pins are 3-stated during reset. A low-to-high transition causes execution to begin at ROM location 0.

* Indicates 3-state condition.

Table 15. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Description
67	CKI	I	**Clock In.** Input clock at twice the frequency of internal operations.
68	IACK	O*	**Interrupt Acknowledge.** Interrupt acknowledge signals when an interrupt is being serviced by the DSP16A. The IACK remains high until normal instruction operation resumes.
69	VSS	P	**Ground.**
70	VDD	P	**5 V Supply.**
71	INT	I	**Processor Interrupt.** Interrupt to DSP16A. INT is acknowledged when the interrupt is enabled by the PIOC register.
72	PSEL	O*	**Peripheral Select.** PSEL is used to specify the logical port to/from which data is to be conveyed. In active mode, PSEL is high (logic 1) when pdx1 is the register specified in the I/O instruction and low when pdx0 is the register specified. PSEL has no meaning when the device is in passive mode.
73	PIDS	I/O*	**Parallel Input Data Strobe (Active low).** In active mode, PIDS is an output. When PIDS is asserted, data may be placed onto the PDB. Upon negation of PIDS, data should be removed from the PDB. PIDS is asserted by the DSP16A device during an active mode read transaction. In passive mode, PIDS is an input. When asserted by an external device, this signal indicates that data is available on the PDB. In both active and passive modes, the trailing edge (low-to-high transition) of PIDS is the sampling point.
74	PODS	I/O*	**Parallel Output Data Strobe (Active low).** In active mode, PODS is an output. When PODS is asserted, data is available on the PDB. PODS is asserted by the DSP16A device during an active mode write transaction. In passive mode, PODS is an input. When PODS is asserted by an external device, the DSP16A device places the contents of its parallel output register (pdx0 or pdx1) onto the PDB.
75 76 77 78	PB15 PB14 PB13 PB12	I/O* I/O* I/O* I/O*	**Parallel I/O Data Bus — Bit 15.** **Parallel I/O Data Bus — Bit 14.** **Parallel I/O Data Bus — Bit 13.** **Parallel I/O Data Bus — Bit 12.**
79	VDD	P	**5 V Supply.**
80	VSS	P	**Ground.**
81 82 83 84	PB11 PB10 PB09 PB08	I/O* I/O* I/O* I/O*	**Parallel I/O Data Bus — Bit 11.** **Parallel I/O Data Bus — Bit 10.** **Parallel I/O Data Bus — Bit 9.** **Parallel I/O Data Bus — Bit 8.**

* Indicates 3-state condition.

Characteristics

The following electrical and timing characteristics are advance information, and are subject to change.

Electrical Characteristics

The parameters below are valid for the following conditions: T_C = 0 to 85 °C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T = 2 X tCKIHCKIH (see Figure 3).

Parameter	Sym	Min	Max	Unit
Input voltage:				
low	V_{IL}	—	0.8	V
high	V_{IH}	2.0	—	V
Output voltage:				
low (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	V
high (I_{OH} = –2.0 mA)	V_{OH}	2.4	—	V
Output current:				
low (V_{OL} = 0.4 V)	I_{OL}	—	2.0	mA
high (V_{OH} = 2.4 V)	I_{OH}	—	–2.0	mA
Output short circuit current V_{OH} = 0 V	I_{OS}	—	–200	mA
Output 3-state current:				
high (V_{IH} = 2.0)	I_{OZH}	–75	75	μA
low (V_{IL} = 0.8)	I_{OZL}	–75	75	μA
Input current:				
high (V_{IH} = 5.5; V_{DD} = 5.5)	I_{IH}	—	25	μA
low (V_{IL} = 0, V_{SS} = 0)	I_{IL}	—	–25	μA
Power supply current V_{DD} = 5.5 V	I_{DD}	—	82	mA
Power dissipation V_{DD} = 5.5 V	PD	—	450	mW
Input capacitance	C_I	—	15	pF

Maximum Ratings

Voltage range on any pin with respect to ground .... –0.5 to +6 V
Power dissipation .... 1 W
Ambient temperature range .... –40 to +120 °C
Storage temperature range .... –65 to +150 °C

Maximum ratings are the limiting conditions that can be applied to all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded and soldered safely at temperatures of up to 300 °C.

Chip current in the input buffers is highly dependent on input voltage level. At full CMOS levels essentially no DC current is drawn but, for levels near the threshold of 1.4 V, high and unstable levels can flow. The table below gives the I_{DD} input buffer current for 43 inputs biased at DC level, V_{IN}. The worst case power assumes 100 mW dissipated by the input buffers. Inputs are protected against electrostatic discharge (ESD) damage with diodes connected to V_{DD} and V_{SS}. Input voltage should not be greater than V_{DD} + 0.5 V or less than V_{SS} – 0.5 V. The power dissipation listed is for unloaded outputs. Total power dissipation can be calculated on the basis of the application by adding $C \cdot V_{DD}^2 \cdot f$ for each output, where C is the load capacitance and f is the output frequency.

I_{DD} Input Buffer Current Versus V_{IN}

V_{IN} (V)	5.0	3.6	2.8	2.4	2.0	1.4	0.8	0.4	0
I_{DD} (ma)	<.2	2.7	28.	36.	36.	*	16.	1.3	<.2

* High and unstable.

Timing Characteristics and Requirements

Timing characteristics refer to the behavior of the device under specified conditions. Timing requirements refer to conditions imposed on the user for proper operation of the device. All timing data is valid for the following conditions unless otherwise specified: T_C = 0 to 85 °C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T = 2 × tCKIHCKIH, capacitance load on outputs = 50 pF.

External Memory and Clocks

Timing Requirements for External ROM and Clocks (See Figure 3)

Description	Symbol	Min	Max	Unit
Clock in period	tCKIHCKIH	16.5	1000	ns
Clock in low time	tCKILCKIH	5	—	ns
Clock in high time	tCKIHCKIL	5	—	ns
External memory set-up	tRBVCKOL	13	—	ns
External memory hold	tCKOLRBX	0	—	ns

Timing Characteristics for External ROM and Clocks (See Figure 3)

Description	Symbol	Min	Max	Unit
Clock out high delay	tCKIHCKOH	—	17	ns
Clock out low delay	tCKIHCKOL	—	17	ns
Address delay time	tCKOLABV	—	5	ns
Address hold time	tCKOLABX	0	—	ns

Reset and Interrupts

Timing Requirements for Reset and Interrupts (See Figure 4)

Description	Symbol	Min	Max	Unit
RSTB low time	tRSTBLRSTBH	6T	—	ns
INT hold time	tIACKHINTL	0	2T	ns
INT assertion time	tINTHINTL	2T	—	ns

Timing Characteristics for Reset and Interrupts (See Figure 4)

Description	Symbol	Min	Max	Unit
RSTB disable time	tRSTBHOUTZ	—	100	ns
RSTB enable time	tRSTBHOUTV	—	100	ns

Serial I/O (SIO)

Timing Requirements for Serial Inputs (See Figure 5)

Description	Symbol	Min	Max	Unit
Clock period	tICKHICKH	66	—	ns
Clock low time	tICKLICKH	30	—	ns
Clock high time	tICKHICKL	30	—	ns
Load high set-up	tILDHICKH	15	—	ns
Load low set-up	tILDLICKH	15	—	ns
Load high hold	tICKHILDH	0	—	ns
Load low hold	tICKHILDL	0	—	ns
Data set-up	tDIVICKH	12	—	ns
Data hold	tICKHDIX	0	—	ns

Timing Characteristics for Serial Input (See Figure 5)

Description	Symbol	Min	Max	Unit
IBF delay	tICKHIBFH	—	45	ns

Timing Requirements for Serial Output (See Figures 6 and 7)

Description	Symbol	Min	Max	Unit
Clock period	tOCKHOCKH	66	—	ns
Clock low time	tOCKLOCKH	30	—	ns
Clock high time	tOCKHOCKL	30	—	ns
Load high set-up	tOLDHOCKH	15	—	ns
Load low set-up	tOLDLOCKH	15	—	ns
Load high hold	tOCKHOLDH	0	—	ns
Load low hold	tOCKHOLDL	0	—	ns

Timing Characteristics for Serial Output* (See Figures 6 and 7)

Description	Symbol	Min	Max	Unit
Data delay	tOCKHDOV	—	35	ns
Enable data delay	tDOENLDOV	—	35	ns
Disable data delay	tDOENHDOZ	—	35	ns
Data hold	tOCKHDOX	5	—	ns
OSE delay	tOCKHOSEH	—	45	ns
Address delay	tOCKHSADDV	—	35	ns
Address hold	tOCKHSADDX	5	—	ns
Enable delay	tDOENLSADDV	—	35	ns
Disable delay	tDOENHSADDZ	—	35	ns

* Capacitance load on OCK and DO: 100 pF.

Clock Generation (Active Mode)

Timing Characteristics for Clock Generation (See Figures 5—7)

Description	Symbol	Min	Max	Unit
ICK duty cycle	tICKDC	45	55	%
OCK duty cycle	tOCKDC	45	55	%
ILD duty cycle	tILDDC	49.9	50.1	%
OLD duty cycle	tOLDDC	49.9	50.1	%
ILD delay	tICKHILDH tICKHILDL	—	45	ns
OLD delay	tOCKHOLDH tOCKHOLDL	—	45	ns
SYNC duty cycle	tSYNCDC	49.98	50.02	%
SYNC delay	tOCKHSYNCL tOCKHSYNCH	—	35	ns

Multiprocessor Communication

All serial I/O timing requirements and characteristics (except DOEN characteristics) still apply.

Timing Requirements for Multiprocessor Communication
(See Figure 8)

Description	Symbol	Min	Max	Unit
SYNC set-up	tSYNCHOCKH tSYNCLOCKH	40	—	ns
SYNC hold	tOCKHSYNCH tOCKHSYNCL	0	—	ns
Address set-up	tSADDVOCKH	12	—	ns
Address hold	tOCKHSADDX	0	—	ns

Timing Characteristics for Multiprocessor Communication (See Figure 8)

Description	Symbol*	Min	Max	Unit
Data delay (bit 0 only)	tOCKLDOV	—	33	ns
Data disable delay	tOCKHDOZ	—	40	ns
Data hold	tOCKHDOX	5	—	ns
Data delay	tOCKHDOV	—	35	ns
DO valid delay	tOCKHDOENL	—	35	ns
Address delay (bit 0 only)	tOCKLSADDV	—	33	ns
Address disable delay	tOCKHSADDZ	—	40	ns
Address delay	tOCKHSADDV	—	35	ns
Address hold	tOCKHSADDX	5	—	ns
SYNC delay	tOCKHSYNCL tOCKHSYNCH	—	35	ns
SYNC duty cycle	tSYNCDC	49.98	50.02	%

* Capacitance load on ICK, OCK, DO, SYNC, and SADD: 100 pF.
tICKHICKH and tOCKHOCKH are tCKIHCKIH X 4, 12, 16, or 20. See sioc register.
tILDHILDH and tOLDHOLDH are (tICKHICKH or tOCKHOCKH) X 16. See sioc register.
tSYNCHSYNCH is (tICKHICKH or tOCKHOCKH) X (128 or 256). See tdms register.

Parallel I/O (PIO)

Timing Requirements for PIO (See Figures 9—13)

Description	Symbol	Min	Max	Unit
PB set-up time	tPDBVPIDSH	15	—	ns
PB hold time	tPIDSHPDBX	0	—	ns
Passive strobe width (read)	tPIDSLPIDSH	T	—	ns
Passive strobe width (write)	tPODSLPODSH	T	—	ns
PODS high between writes	tPODSHPODSL	T	—	ns

Timing Characteristics for PIO (See Figures 9—13)

Description	Symbol	Min* 00	Min* 01	Min* 10	Min* 11	Max	Unit
PIDS pulse width	tPIDSLPIDSH	T	2T	3T	4T	—	ns
PODS pulse width	tPODSLPODSH	T	2T	3T	4T	—	ns
PSEL hold time PODS	tPODSHPSELX	0	T/2	T/2	T/2	—	ns
PODS high to PIDS low	tPODSHPODSL	20				—	ns
PIDS high to PODS low	tPIDSHPODSL	T				—	ns
PSEL valid before PODS	tPSELVPODSL	T/2 − 10				—	ns
PB hold time	tPODSHPDBX	10				—	ns
PIDS low to PSEL valid	tPIDSLPSELV	—				10	ns
PSEL hold time PIDS	tPIDSHPSELX	25				—	ns
PIDS high (interaccess)	tPIDSHPIDSL	20				—	ns
Data valid after PODS	tPODSLPDBV	—				25	ns

* The pulse widths of PIDS and PODS for those timing specifications having multiple entries under the minimum value column are determined by bits 14 and 13 of the pioc register. See Table 13.

Timing Diagrams

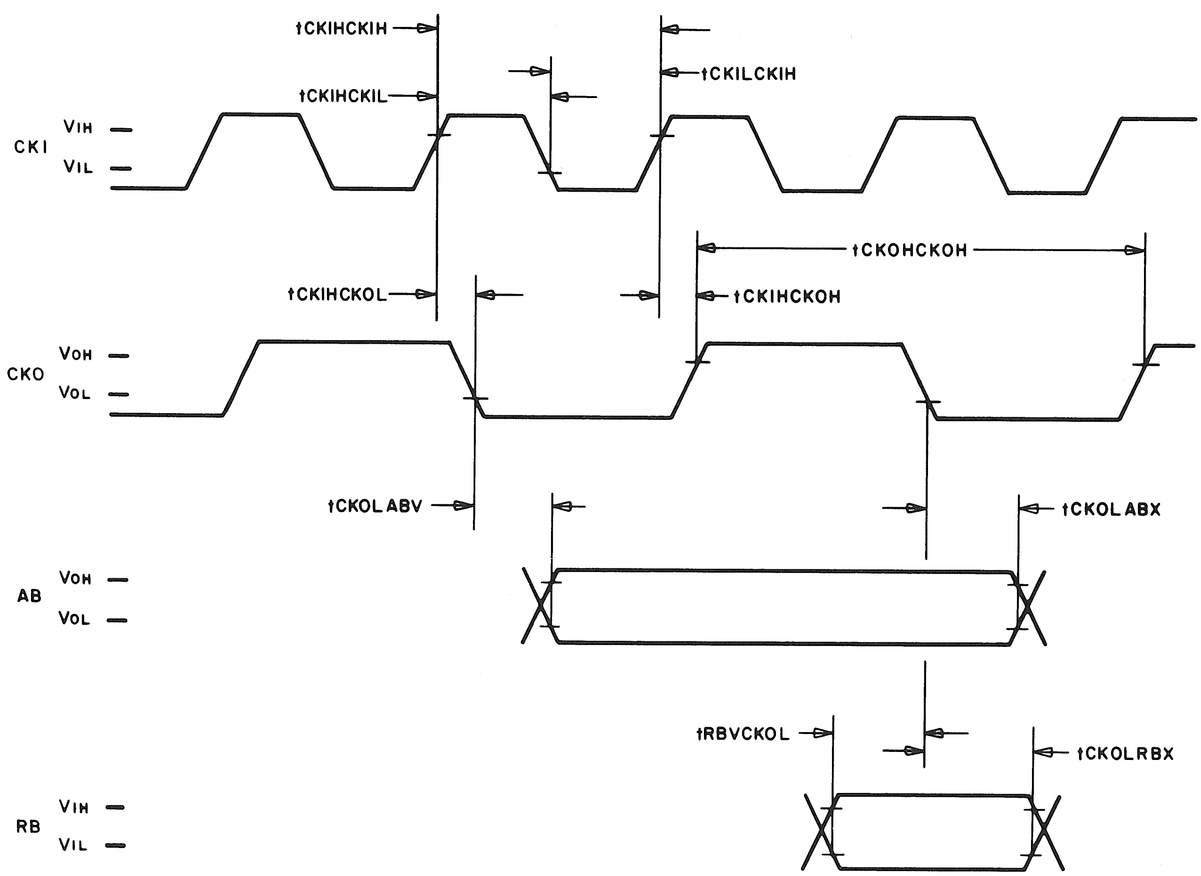
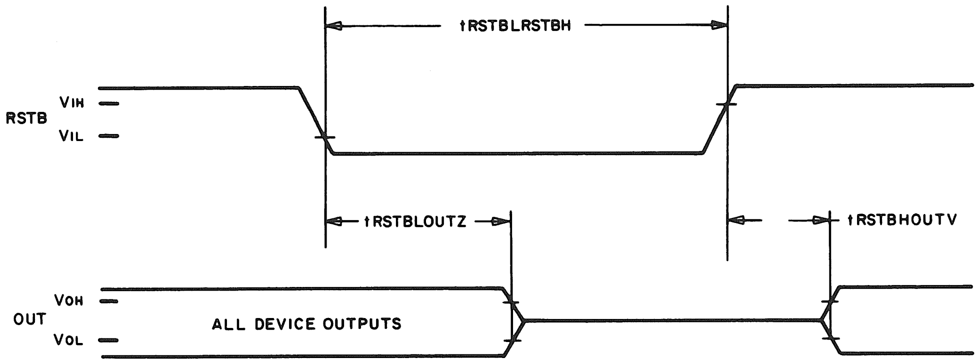
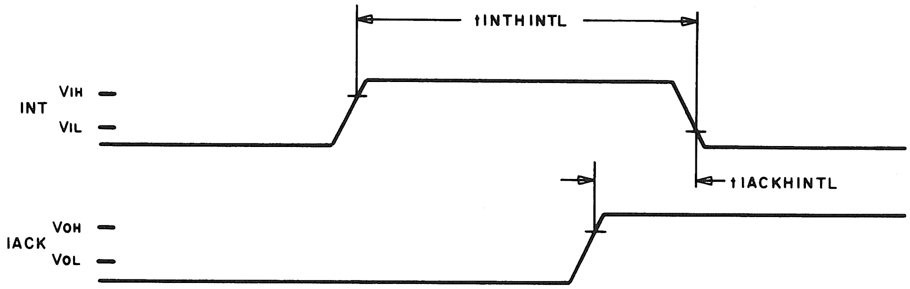


Figure 3. External Memory Interface



A. Reset Timing



B. Interrupt Timing

Figure 4. Reset and Interrupt Timing

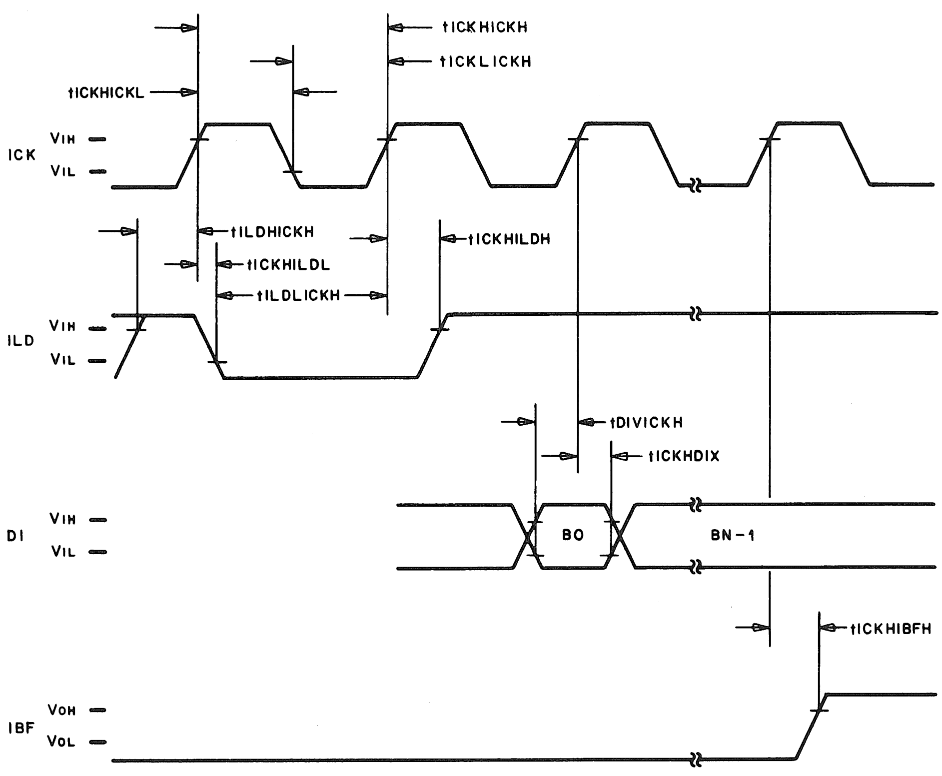


Figure 5. Serial Input Timing

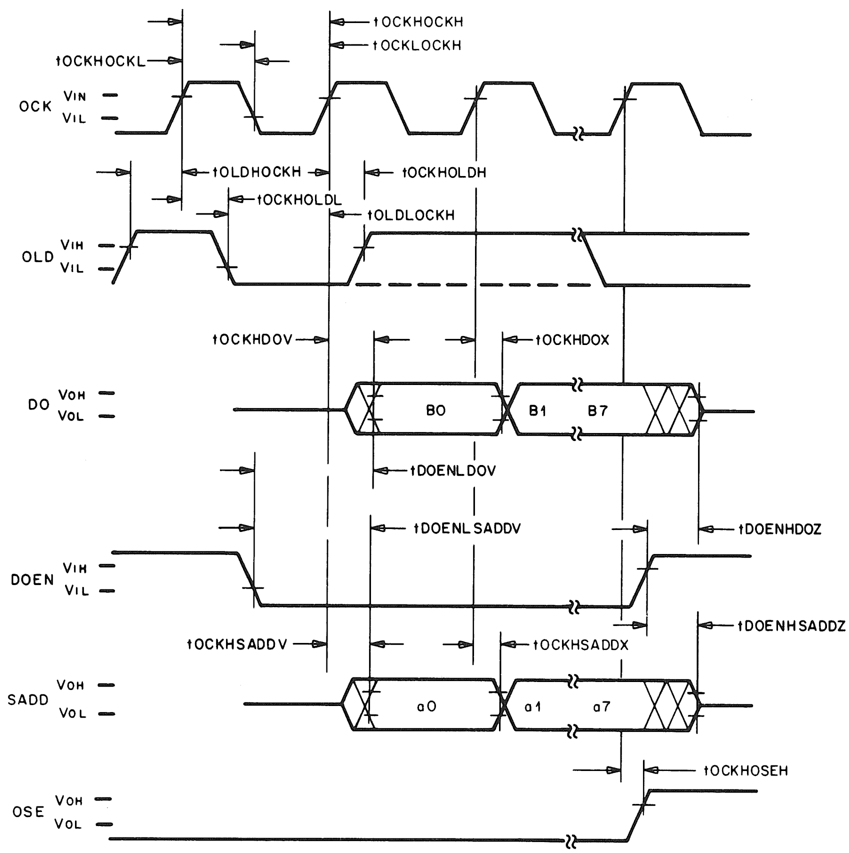


Figure 6. Serial Output Timing — 8 Bits

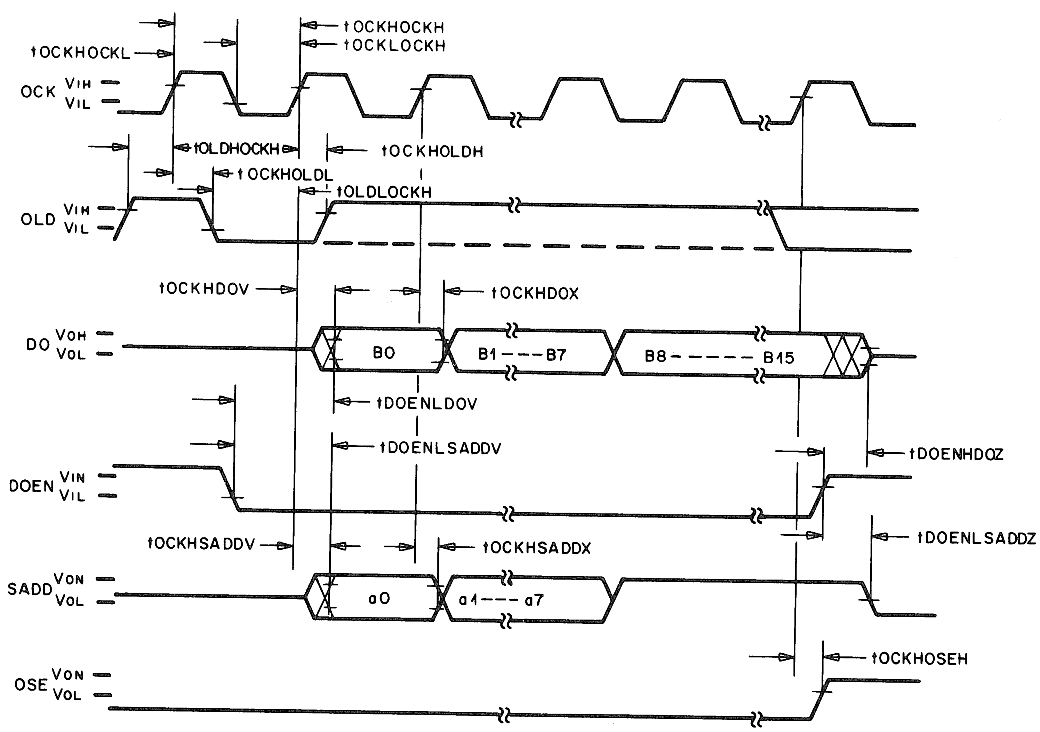
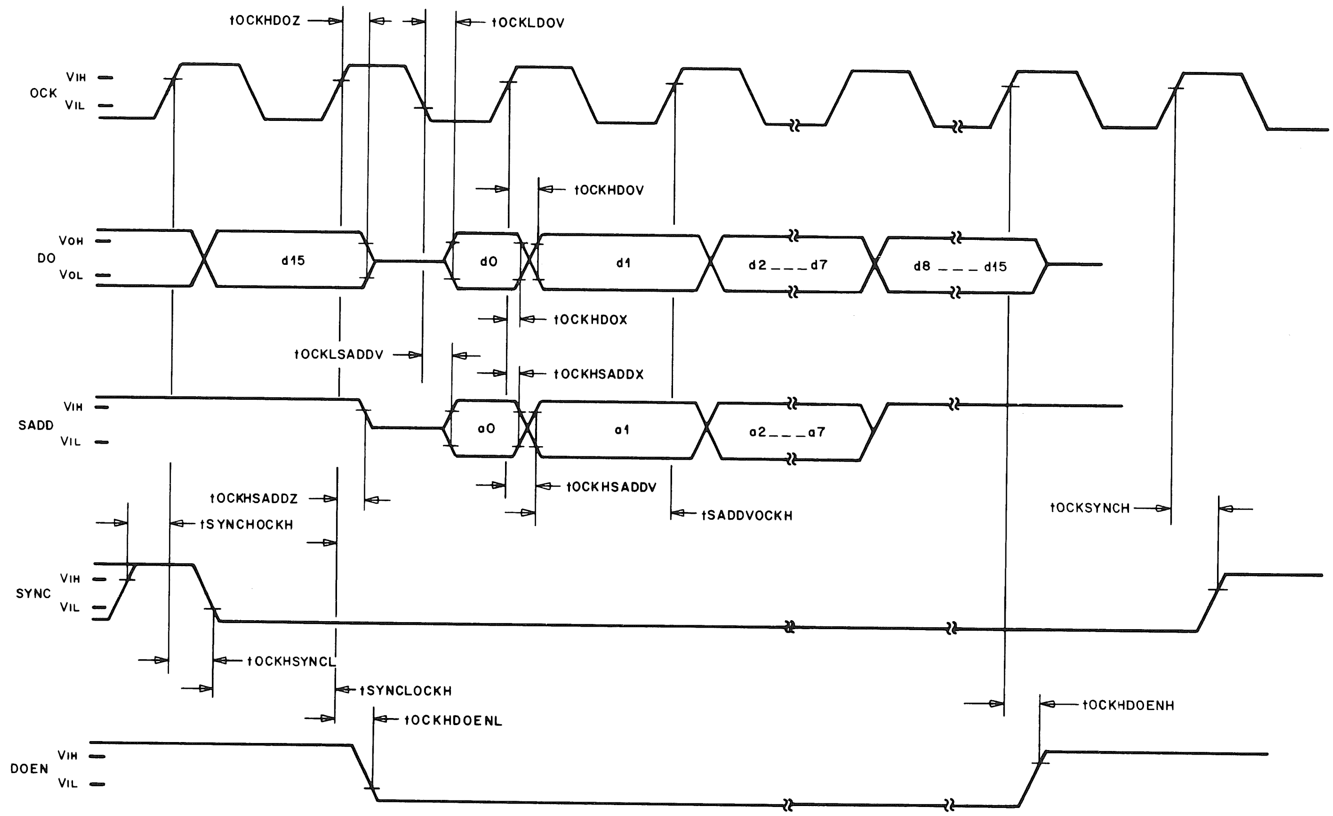


Figure 7. Serial Output Timing — 16 Bits



Note: Sioc register, LD field must be set for multiprocessor operation

Figure 8. Multiprocessor Timing

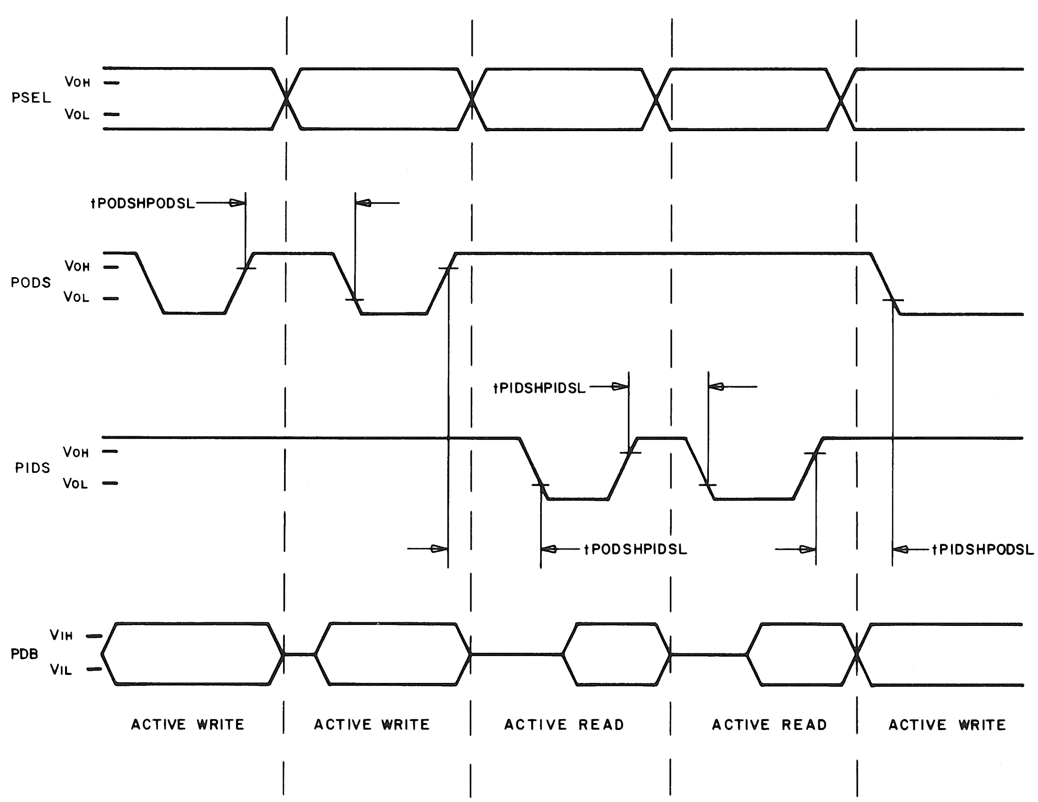


Figure 9. Parallel I/O Interaccess Timing

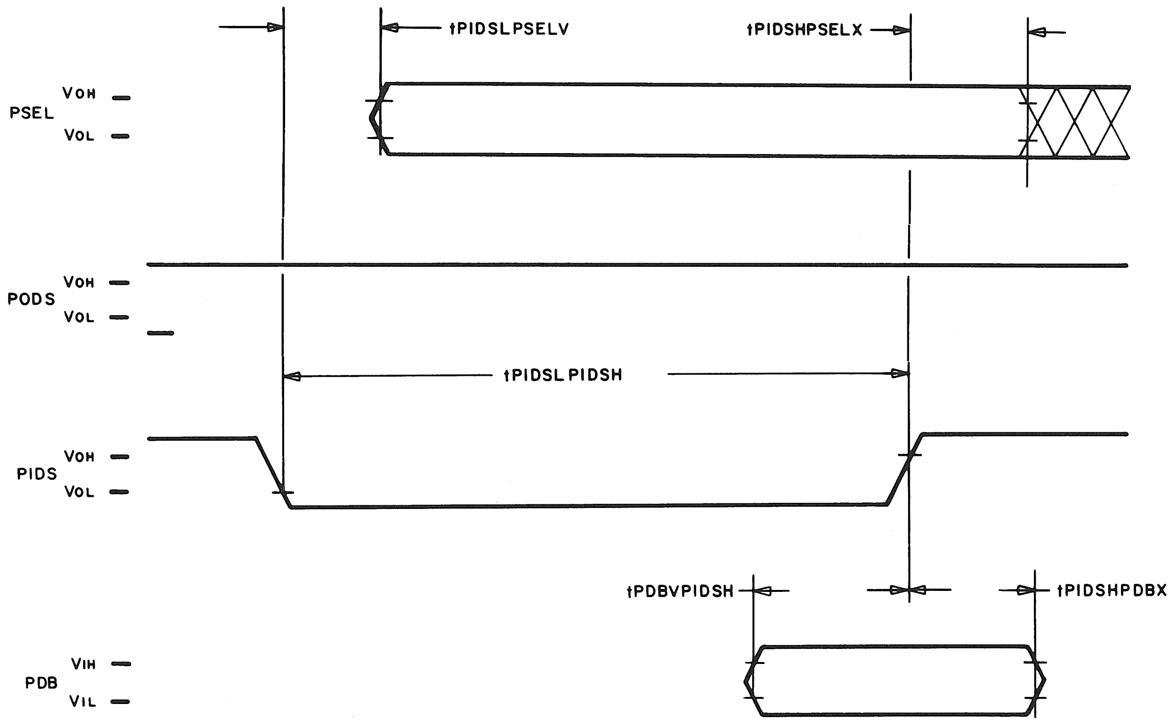


Figure 10. Parallel Active Input Timing

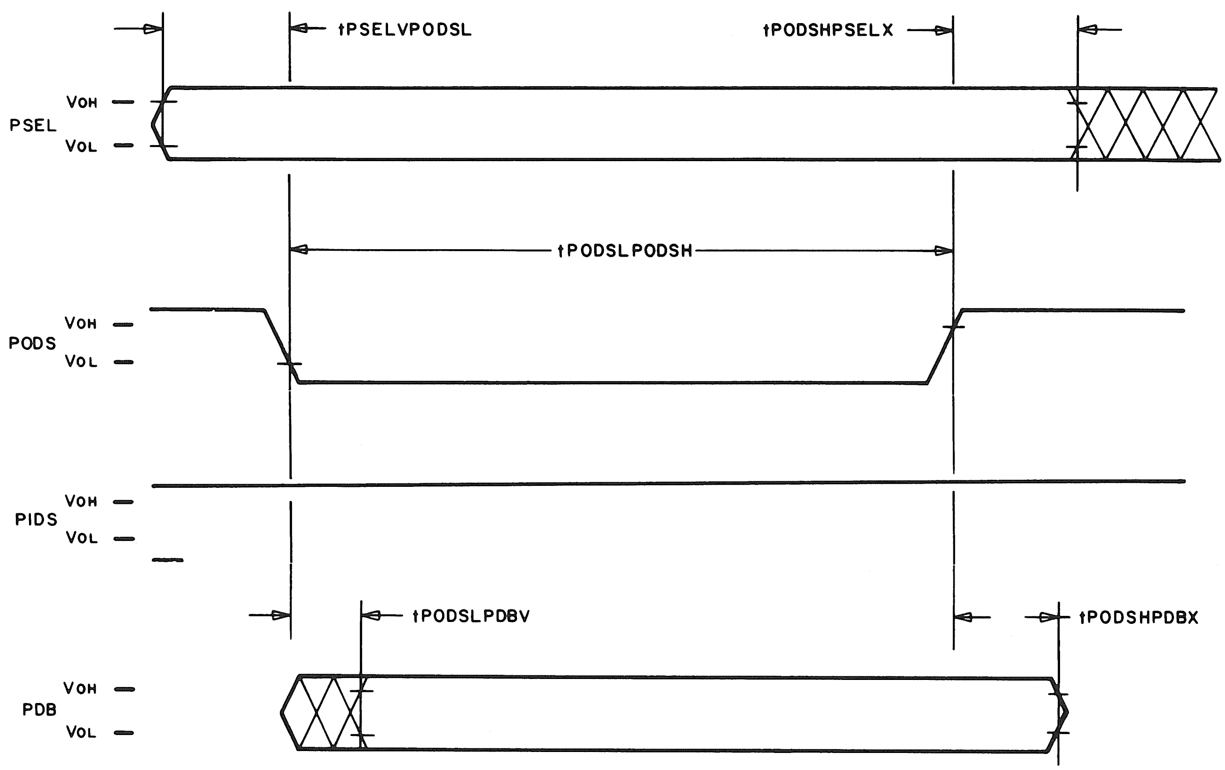


Figure 11. Parallel Active Output Timing

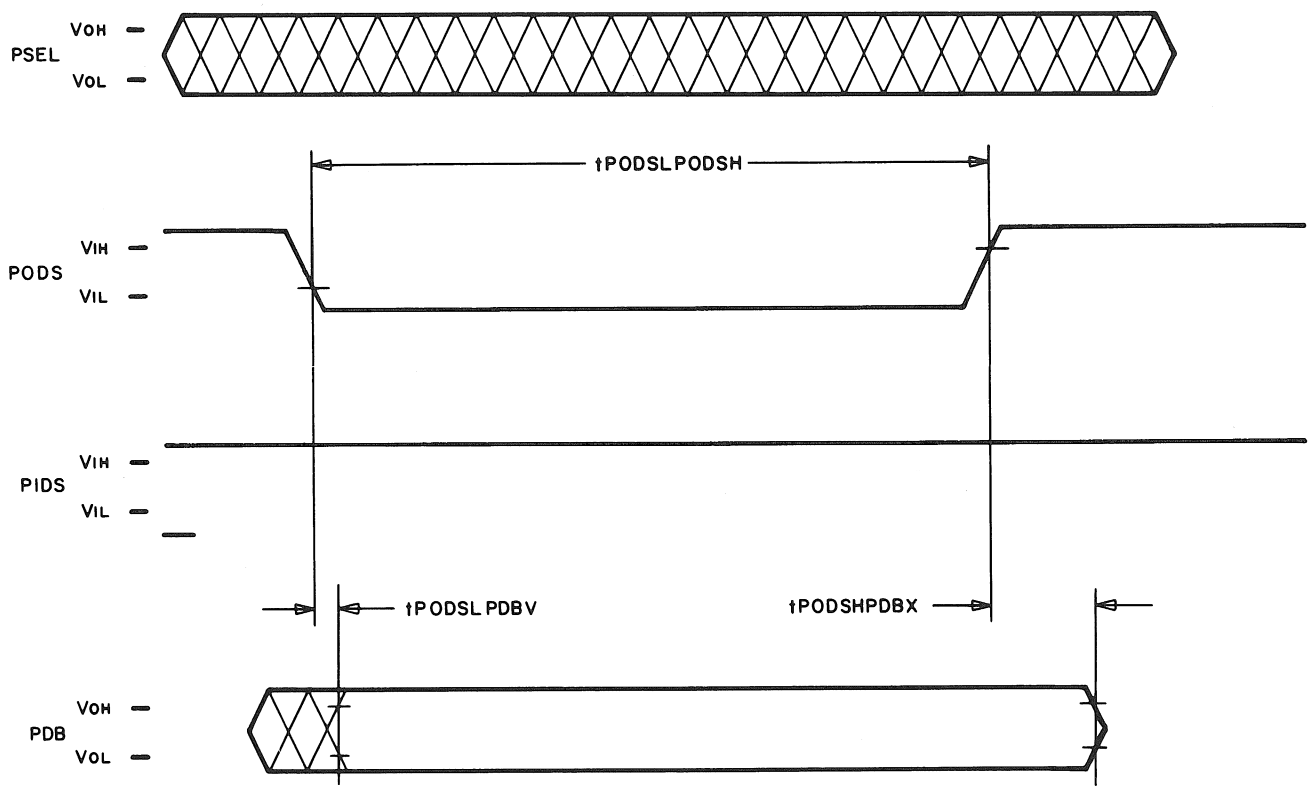


Figure 12. Parallel Passive Output Timing

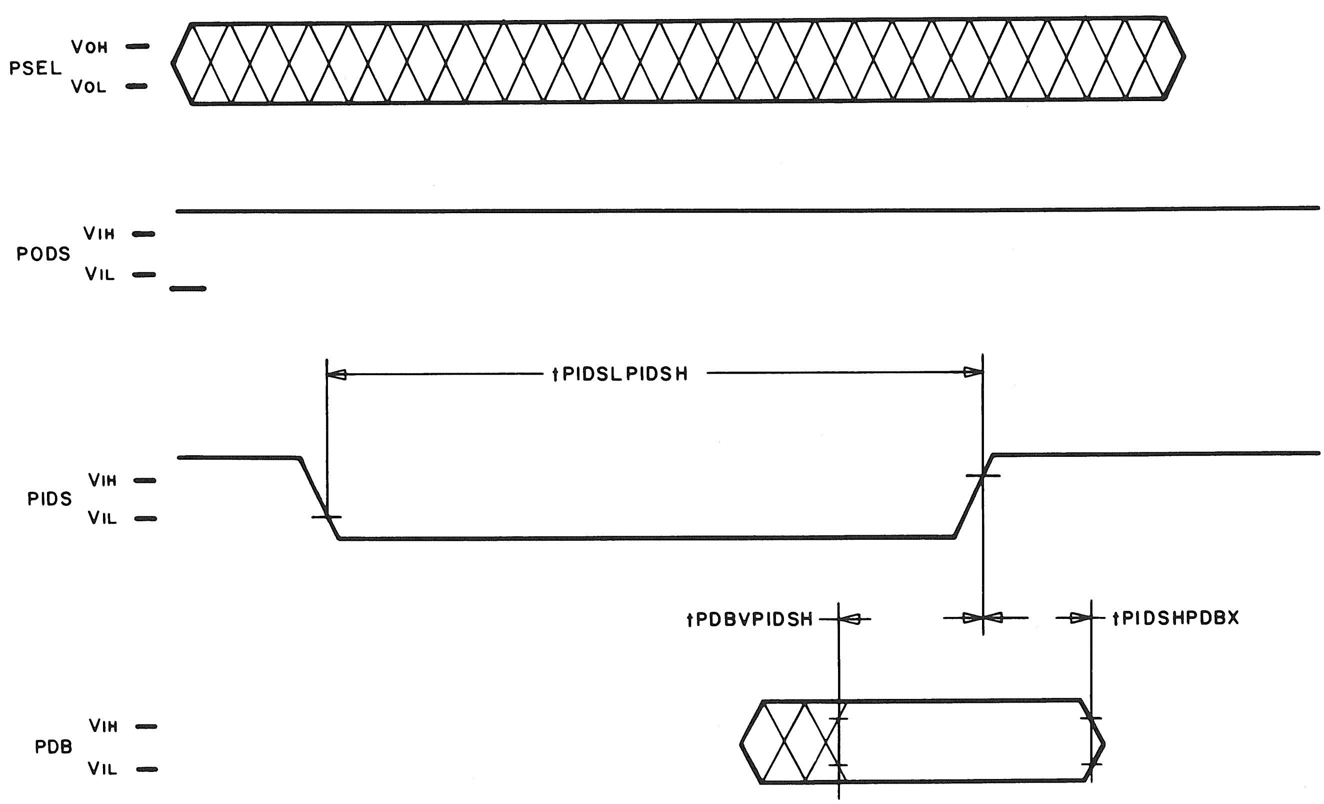
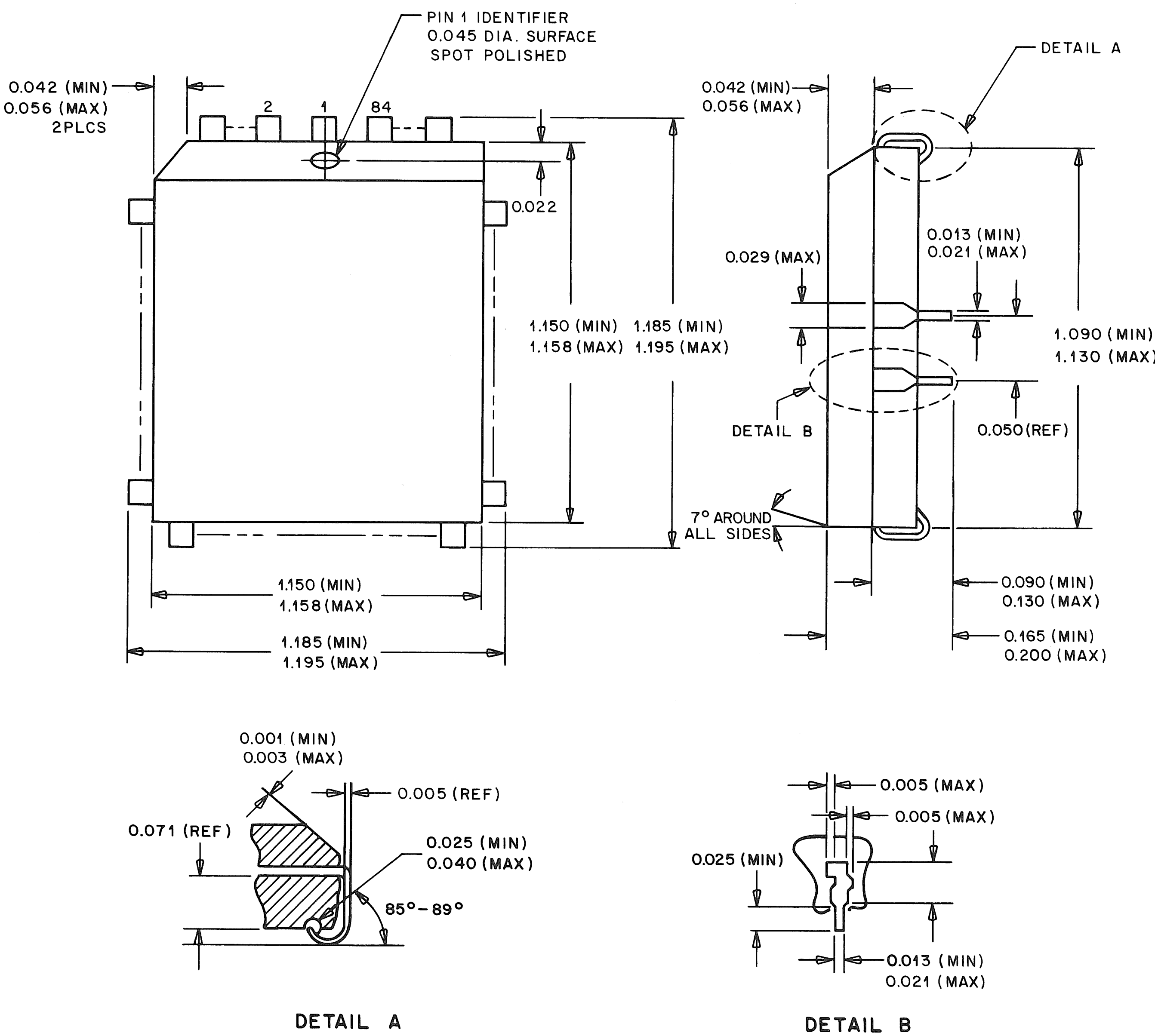


Figure 13. Parallel Passive Input Timing

Outlines

84-Pin Plastic Leaded Chip Carrier



Notes:
Holding flash is permitted around periphery of body. Flash must not extend more than .010 beyond body.
All dimensions are in inches.

Notes

Notes

Notes

WE DSP16A Digital Signal Processor

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