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Floppy Tape Interface Theory of Operation

This overview summarizes the major functions performed by the Floppy Tape Interface hardware. The Floppy Tape interface hardware description includes:

- Interface I/O Description
- Interface Operations
- DMA Circuitry
- Floppy Tape Controller

In addition, some brief adjustment procedures are provided at the end of this chapter. These procedures are for adjusting the read and write pulsewidth of the floppy tape controller IC, and its nominal VCO frequency.

Floppy Tape Interface

The Floppy Tape Interface performs all read/write operations through a DMA channel containing two proprietary ICs. Besides the I/O registers for the DMA ICs and the floppy tape controller IC, several other I/O addresses can be accessed on the card. The "Block Diagram Description" discusses the hardware contained in the Floppy Tape Interface. The circuitry is divided into four parts: the expansion bus interface to the **UNIX** PC, the DMA Circuits, the address decoding logic, and the floppy tape controller itself.

Floppy Tape Cartridge Tape Drive Specifications

Specifications for the Floppy Tape Cartridge Tape Drive are as follows:

Manufacturer	Specification	
Cipher	Capacity	1/4 inch tape cartrige Unformatted Per Drive 32MBytes Formatted 26.6MB 1024 Byte sectors 25.1MB 512 Byte sectors 21.2MB 256 Byte sectors
	Functional	Total Data Tracks - 6 Recording Mode Single track, serpentine Recording Time up to 3.4 min Write/Read full Cartridge 9.3 min. Transfer Rate (Read/Write) 500 kbits/sec 250 kbits/sec (optional) Tape Motion 78 ips streaming 39 ips optional
	Interface	Standard Floppy Disk SA450 or SA850
	Error Rates Read Error 1 per 10^9 bits recoverable Read Error 1 per 10^{11} bits non-recoverable Error Detection CRC or read verify pass	
	DC Power Requirements +5V DC +/- 5%, 0.8 amps maximum +12V DC +/-5%, 1.8 amps nominal 2.5 amps surge maximum	
	Power Dissipation	25.6 watts nominal 35 watts surge

Floppy Tape Interface I/O Description

I/O addressing and register descriptions are given below. Also, there is a discussion of offest addresses as used in the UNIX PC Expansion Slots, and a listing of steps required to perform read/write operations using the Floppy Tape Interface.

The Expansion Slot

The expansion cards in the UNIX PC are each assigned 256K bytes of address space. Since all addressing is done on word boundaries, there is 128K words of address space. Expansion Bus address bits XA1 - XA17 define this space. Each expansion slot contains hardwired identification bits XID0 - XID2 to define eight unique slot addresses. Bits XA18 - XA20 are compared against the slot identification bits to validate the address. Also, address bit XA21 is always zero; similarly, expansion addresses have XA22 and XA23 as always ones. Therefore, once the expansion card is plugged into its slot, the predetermined XA18 - XA23 bits generate the offset address, while XA1 - XA17 bits are the base address used to access I/O devices. The offset addresses used in the UNIX PC are listed below.

Expansion Slot Offset Addresses

Slot Number	Offset Address (h)
0	0C00000
1	0C40000
2	0C80000
3	0CC0000
4	0D00000
5	0D40000
6	0D80000
7	0DC0000

Interface Registers and Command Descriptions

The following paragraphs list the registers used in floppy tape interface operations and the command descriptions that select the I/O functions.

ID Register (Base Address 03FFFEh - 03FFF8h)

When the **UNIX** PC is first powered up, the UNIX kernel reads the ID register into memory. The content of the register is used to identify which expansion card is present and in which slot it resides. The kernel then refers to the appropriate driver, which knows the proper offset it must apply to access registers on the card. Also, a write operation to the ID Register resets the card.

Base Addr. (h)	R/W	Data	Description
03FFFE	R	XXEF	MSB of ID checksum (0F0)
03FFFC	R	XXFF	LSB of ID checksum (0FF)
03FFFA	R	XX10	MSB of ID checksum (010)
03FFF8	R	XX01	LSB of ID checksum (001)
03FFFE	W	XXXX	A write to any of these
03FFFC	W	XXXX	four locations resets
03FFFA	W	XXXX	the card.
03FFF8	W	XXXX	

DMA Address Register (Base Address 02XXXXh)

A write to this register specifies the starting logical address for the DMA operation. During a DMA transfer, the addresses are incremented from low to high. The data bus is not used to transfer address data. Instead, certain address bits are assigned to contain the data. This address cannot be read during DMA or else DMA data is destroyed (see DMA Operations below).

Base Addr. (h)	R/W	Data	Description
02[x1dd]DDD	W	XXXX	

Transfers upper bits of the DMA address. The data bus is not used. Instead, address bits XA1 - XA13 contain the value of bits DA9 - DA21 of the DMA address to be loaded into the DMA Address Register. Note that XA15 is don't care, while XA14 = 1 signifies upper bits.

Base Addr. (h)	R/W	Data	Description
02[x0xxxxx]DD	W	XXXX	

Transfers lower bits of the DMA address. The data bus is not used. Here, address bits XA1 - XA8 contain the value of bits DA1 - DA8 of the DMA address to be loaded into the DMA Address Register. Note that XA15 and XA13 - XA19 are don't care, while XA14 = 0 signifies lower bits.

DMA Count Register (Base Address 003FFEh)

When this address is read, bits D0 - D13 contain the current contents of the register. Bits D14 and D15 are not valid. For a write to this register, bits D0 - D13 must be set to the complement of the number of words to be transferred. D14 is set to 1 if the DMA operation is to be a memory-read operation; that is, data flows from memory to tape, or to 0 if the operation is a memory write. When no DMA operation is being done, this bit would normally be left as 0. Data bit D15 is set to 1 to enable DMA; otherwise, it should be set to 0. These two bits are used as signals in the proprietary DMA IC set. Similar, but not identical, signals exist in the Tape Control Register as shown below.

Base Addr. (h)	R/W	Data	Description
003FFE	R	DDDD	

Bits D0 - D13 contain the value of the DMA Count Register contents. Data bits D14 and D15 are not used.

Base Address	R/W	Data	Description
003FFE	W	DDDD	

Bits D0 - D13 are to contain the value loaded into the DMA Count Register. This value is the complement of the number of words to be transferred. When D14 is 1, the DMA controller operation is a read (memory to tape). When D14 is 0, the operation is a write (tape to memory). When D15 is 1, the DMA controller is enabled.

WD2797 Floppy Disk Controller Registers (Base Addresses)

007FF8h -- Status/Command Register
007FFAh -- Track Register
007FFCh -- Sector Register
007FFEh -- Data Register

During a read operation, bits D0 - D7 contain status information read from the WD2797. The format of data on the tape is similar to a floppy disk drive. Bits D8 - D15 are not valid. During a write operation, Bits D0 - D7 contain commands or data for the WD2797. Bits D8 - D15 are not used. For more information, see the WD2797 data sheet in the latest edition of the Storage Management Products Handbook, published by the Western Digital Corporation.

Tape Control Register (00BFFEh)

The Tape Control Register contains control bits used to select the tape stream on which data is to be read or written. It also contains reset bits and enable bits. After power-up, all bits in this register are set to 0; that is, resets are active and interrupts are disabled. The card is enabled when D0 and D1 are set to 1 and one of the interrupt levels is enabled.

When read, only two bits (D8 and D9) of the most significant byte are used. All other bits are not used.

Bit	Meaning (Read Mode)
D8	If this bit is 1, the tape cartridge is present.
D9	If this bit is 1, an interrupt request from the WD2797 is pending.

Bit	Meaning (Write Mode)
D0	If 0, the DMA Data IC is reset.
D1	If 0, the WD2797 is reset.
D2 - D5	Not Used.
D6	If 1, the DMA direction is read (memory to tape). If 0, the DMA direction is write (tape to memory).
D7	If 1, Interrupt level 1 is enabled (normal).
D8	If 1, Interrupt level 5 is enabled.
D9	If 1, the floppy tape drive motor is on.
D10	If 1, the cartridge is locked in the drive and cannot be removed.
D11 - D14	Drive Select lines 1 - 4, respectively.
D15	Side Select line.

Floppy Tape Interface Operations

This is a list of the steps required to write data to the floppy tape or read information from it. A read operation is one in which data is read from memory and written onto the tape. A write operation is just the opposite. In the following sequences, it is assumed that whenever the Tape Control Register is written to, data bits D0 - D15 are the same as they were for a previous write operation unless they are specifically required to be different. Also, once a DMA operation has begun, no I/O read or writes can be performed until the DMA operation has completed or an interrupt has occurred.

The sequence of operations necessary to do a DMA read operation is the following:

1 Any required prerequisite operations are performed, such as selection of the tape stream or preparation of memory.

2 The D6 direction bit in the Tape Control Register is set to 1.

3 The DMA Address Register is loaded with the starting logical address.

4 The DMA Count Register is loaded with all 0s. It is then loaded with the following:

D15 and D14 = 1
D0 - D13 = the complement of the number of words to be transferred.

5 A Write Data Command is written to the WD2797.

6 When the command is complete, an interrupt is generated to indicate the end of DMA.

The sequence of operations necessary to do a DMA write operation is the following:

1 Any required prerequisite operations are performed, such as selection of the tape stream or preparation of memory.

2 The D6 direction bit in the Tape Control Register is set to 0.

3 The DMA Address Register is loaded with the starting logical address.

4 The DMA Count Register is loaded with all 0s.

5 The DMA Count Register is now loaded with the following: D15 and D14 = 1, and D0 - D13 = the complement of the number of words to be transferred.

6 The DMA Count Register is read until the count has incremented.

7 The DMA Address and DMA Count Registers are reloaded with the values in steps 3 and 5.

8 A Read Data Command is written to the WD2797.

9 When the command has completed, an interrupt is generated to indicate the end of DMA.

Block Diagram Description

The Floppy Tape Interface can be divided into four major functional blocks as shown in Figure C-1:

- The Expansion Bus Interface contains buffers and drivers to connect the floppy tape controller circuitry to the **UNIX** PC.
- DMA Control Logic controls and performs data transfers between the floppy tape controller and the Expansion Bus Interface.
- Address Decoding Logic decodes the addresses of the command and status registers on the controller.
- The Floppy Tape Controller Interface consists of a Western Digital 2797 floppy controller and associated logic for control of the floppy tape drive.

Also refer to Figure C-2, PC 7300 Floppy Tape Interface Schematic.

Expansion Bus Interface

On Sheet 4 of Figure A-2, the Expansion Bus Interface buffers address and data between the UNIX PC Expansion Bus and the circuitry on the Floppy Tape Interface. The Interface is composed of address and data buffers, control buffers, and some logic used during DMA transfers. Two kinds of Expansion Bus Interface operations are performed: I/O transfers and DMA transfers. The **UNIX** PC performs I/O transfers through the transfers, the **UNIX** PC loads the DMA ICs with a starting address and a byte count for the transfer. Once the DMA channel is initialized, the DMA circuits supply the address to transfer data either to or from system memory.

Expansion address lines XA1 - XA21 and data lines XD0 - XD15 provide address and data for the board, while control lines from the **UNIX** PC, such as lower and upper data strobe signals (XLDS* and XUDS*), the expansion request line (EXPRQ*), the I/O enable (XI/OEN*), and the read/write direction line (XR/W*) control the data flow. The address lines are sent to address transceivers 1E - 1G and then onto the inputs of DMA Address IC 3G. Similarly, data is transferred using data transceivers 1C and 1D for I/O operations, or transparent latches 2C and 2D sending data to the DMA channel.

During an I/O operation involving the floppy tape controller 7A, I/OEN* is low. This causes address lines XA18 - XA20 to be compared at 3E against expansion slot identification lines XID0 - XID2. If the two addresses compare favorably, a gated I/O request, GI/ORQ* is generated to enable the two data transceivers and the pair of buffers on the register-select lines of 7A. During operations involving the Tape Control Register or the ID Register, the address is decoded using the XA14 - XA20 lines at decoders 4E.

During DMA cycles, the two data transceivers are disabled and two latches at 2C and 2D are used to write data to the DMA Data IC during memory-to-tape DMA operations. In either direction of a DMA transfer, the DMA Address IC supplies the memory address once it has been initialized. Since the DMA logic takes over control of the UNIX PC during a DMA transfer, logic in the Expansion Bus Interface also simulates the control signals necessary for operation of the bus. The Expansion Bus Interface is composed of counter 3C and several gates. The high XLDS* and XUDS* data strobes are gated by buffer 1A back to the address buffers. The XR/W* read/write direction line is provided by a bit in the Tape Control Register, MTTDIR.

Address Decoding Logic

On Sheet 3 of Figure C-2, the Address Decoding Logic decodes the addresses of the command and status registers on the controller. Two address decoders at 4E perform the decoding.

The first decoder is enabled by LOC I/O* from the DMA Address IC. LOC I/O* is actually a delayed version of the I/O enable signal I/OEN+ from the Expansion Bus Interface. At the first decoder, address lines XA16 and XA17 select one of three outputs. Output Y0 enables the second half of decoder 4E. Y2 is gated with other signals to generate the DMA address ICs DADOWR* address write-enable. Y3 is gated with the R/W (from Sheet 4 of Figure C-2) to generate the read enable for the ID register, READ ID*.

The second decoder uses the XA14 and XA15 address lines to decode three enables. The first, Y0, is gated with R/W* and the processor clock, PCK*, to generate a gated processor clock used to run the DMA Data IC at 3A. The Y1 output is the chip-select line for 3A. Finally the Y2 output is gated with R/W* to latch data from the D0 - D15 data lines into the Tape Control Register.

DMA Circuits

The DMA circuits are used only for data transfers between the Floppy Tape Controller and the Expansion Bus Interface. The DMA channel is contained on two proprietary ICs: the DMA Data IC at 3A and the DMA Address IC at 3G. The DMA Data IC makes the conversion between the 8-bit data bus of the WD2797 and the 16-bit bus used at the Expansion Bus Interface. It is programmed with the byte count. The DMA Address IC is programmed with the initial address of the transfer before the DMA transfer begins. For each word of data transferred during a DMA operation, the DMA Address IC issues an address in memory where the 16-bit word of data is to be found or stored. Up to 16,384 bytes of data can be transferred during one operation. If the transfer is from memory to tape, the data is transferred through data latches 2C. If the transfer is from memory to tape, the data is transferred through data latches 2C and 2D to the DMA Data IC. That IC then transfers each of the two bytes of the transfer to the WD2797 when the data request line TFER* from the Floppy Tape Controller logic goes low. If the transfer is from tape to memory, the DMA Data IC gets two bytes of data from the WD2797 before it sends one 16-bit word to memory through the two data transceivers 1C and 1D. During this time, the DMA logic is also generating the bus control signals necessary for the transfer.

The DMA cycle timing is shown in Figure C-3. The logic relating to the timing diagram is shown on Sheets 3 and 4 of Figure C-2. When the Data DMA IC asserts the expansion bus request signal, EXPxRQ*, through flip-flop 2B, the UNIX PC responds with an expansion bus grant signal, EXPxBG*. Signals Q1 - Q4 represent the outputs of serial timing register 3C. Generated from the Q1 output of 3C is LATCH EN+ at pin 8 of flip-flop 2B, which latches data for the DMA Data IC at 2C and 2D. The DMA bus grant acknowledge signal, DMABGA*, resets 3C to start the timing cycle and is the OR of the bus request and bus acknowledge signals. The remaining data and address waveforms show the timing of the external data bus, XD0 - XD15, the internal data bus used by the DMA Address IC, D0 - D15, and the internal address bus, A0 - A21. For reference, the 10-MHz processor clock, PCK+, is shown.

Floppy Tape Controller

The floppy tape controller is based on a Western Digital WD2797 Floppy Disk Formatter/Controller at 7A. In this application, the WD2797 is adapted to operate a cartridge tape drive designed for such a controller. The drive has a standard floppy disk interface with a 37-pin connector at J2. The WD2797 contains most of the circuitry required to operate a floppy drive, including a phase-locked loop data separator, address mark generation and detection circuitry, and CRC circuitry. For detailed information about the WD2797, including I/O read/write timing diagrams, tape format, and pinouts, refer to the WD2797 data sheet in the latest edition of the Storage Management Products Handbook, published by the Western Digital Corporation.

The WD2797's data bus is connected to DMA Data IC 3A. During I/O operations, command and status information is passed through 3A without invoking a DMA cycle. When the WD2797 is initialized for an actual data transfer, the DMA channel is also set up for the transfer. Before a data transfer, several bytes of data must be written into the WD2797. The data indicates the track and sector to be operated on and the actual command to be executed, such as a data write, format, or status-read command. Immediately after the command is issued, the data transfer between the WD2797 and the floppy tape drive is started. The D0 - D7 data lines into 7A are connected to the DMA Data IC at 3A as DD0 - DD7. The different registers of 7A are selected by the expansion bus XA1 and XA2 address lines as enabled by a gated I/O request signal GI/ORQ*. The status of the read-enable (RE) and write-enable (WE) inputs to the WD2797 are determined by the outputs of gates at 6E, that condition signals from the Expansion Bus Interface and DMA logic.

The circuits surrounding the WD2797 buffer or condition control signals and data between it, the floppy tape drive, and the other circuits on the Floppy Tape Interface. As is usual with this type of interface, the control signals and serial data lines to and from the drive on the 37-pin cable are buffered and inverted. Many of the conventional floppy disk interface signals are used, but some have slightly different meanings with a tape drive.

A group of control lines for the floppy tape drive is provided by the Tape Control Register. Side select signals (SS) and four drive select lines (DS1 - DS4) specify the stream address for the tape drive. A LOCK signal is provided to lock the floppy tape cartridge in place when the drive is operating. Finally, a motor control line, MOTOR, is provided to turn the drive motor on or off.

The Tape Control Register also contains two bits of status information that can be read anytime a DMA transfer is not in progress. The presence of the tape cartridge is sensed at data line D8. Similarly, if an interrupt request from the WD2797 is pending, it can be sensed at D9.

For a discussion of the interface signals and tape format, refer to the document included in this appendix, Series 525 FloppyTape Cartridge Tape Drive Product Description, by Cipher Data Products, Inc.

When the WD2797 has completed a data transfer or I/O operation, it requests service from the host by asserting an interrupt request line at pin 39, INTRQ. On the Floppy Tape Interface board, the interrupt can be selected as one of two levels, INTQ1* or INTQ5*. Gates at 5C determine the interrupt level as directed by two bits in the Tape Control Register. The data request line, DRQ at pin 38 of the WD2797, is asserted during a data transfer when the WD2797 is ready for another byte of data or has a byte of data to transfer. The request is sent through flip-flop at 7C where it is synchronized to the 2-MHz clock driving the WD2797. The output of 7A is sent to DMA Data IC 3A as TFER*. The clock itself is derived from the 10-MHz processor clock, PCK+. The clock is divided by counter 6D and half of flip-flop 7C to generate a 2-MHz square wave clock required by the WD2797.

Adjustments

Several adjustments can be performed to control the WD2797's read and write pulsewidth, and VCO frequency. The adjustments should not be performed until the Floppy Tape Controller has warmed up for two minutes and the preadjustment preparations (steps 1 through 4) have been made.

1 With power off, remove the Floppy Tape Controller board and insert an extender board in its place.

2 Remove the cable connecting the back of the floppy tape controller board to the floppy tape drive.

3 Power the **UNIX** PC on and temporarily ground pin 19 of 7A. This is the master reset line of the WD2797.

4 Connect TP3 and TP4. This activates the test mode for the WD2797.

The VCO and Pulsewidth Adjustments are as follows:

5 The VCO frequency is adjusted to 500 kHz. To adjust the VCO, monitor its frequency at TP5 (pin 16 of 7A). Adjust C7 until 500 kHz is obtained.

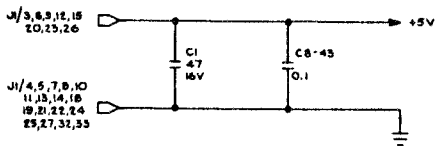
6 The write pulsewidth is set to 200 nanoseconds. Monitor the pulse at TP1 while adjusting R5.

7 Similarly, the read pulsewidth is set to 250 nanoseconds. Monitor the pulse at TP2 while adjusting R6.

8 With the adjustments made, remove the jumper from TP3 and TP4, and reinstall the Floppy Tape Controller in the appropriate **UNIX** PC expansion slot.

I.C. DEVICE CHART

I.C TYPE	REFERENCE DESIGNATIONS	+5V	GND	UNUSED GATES ④
74F04	1B	14	7	8,9/10,11/12,13
74F08	2F	14	7	11,12,13
74F32	4D	14	7	8,9,10/11,12,13
74F74	2B	14	7	
74F175	3C	16	8	
74F240	1A	20	10	
74F245	1C,1D,1E,1F,1G	20	10	
74F373	2C,2D	20	10	
74LS00	2G	14	7	1,2,3/4,5,6/11,12,13
74LS02	6C	14	7	4,5,6 / 8,9,10
74LS04	3D,7E	14	7	
74LS08	2A	14	7	
74LS14	8E	14	7	
74LS32	5E,5F	14	7	5F : 11,12,13
74LS51	6E	4	11	
74LS74	7C	14	7	
74LS86	5D	14	7	8,9,10
74LS125	4C	14	7	
74LS139	4E	16	8	
74LS273	8A,8B	20	10	
74LS290	6D	14	7	
74S86	3E	16	8	
74S288	2E			
7406	8C,8D	14	7	8C : 10,11
7438	5C	14	7	8,9,10 11,12,13
WD 2797-02	7A	21	20	
DMA ADDRESS	3G	20	40	
DMA DATA	3A	20	40	



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. PAGE REFERENCE SHOWN AS :

   SHEET NO.
   ZONE

④ UNUSED INPUTS OF GATES ARE AS A RULE TIED TO +5V OR GND THRU. A RESISTOR FOR IMPROVED NOISE IMMUNITY.

REFERENCE DESIGNATIONS		
LAST USED	NOT USED	
C43		
CR1		
J2		
R6		
RN6		
TP1		

SPARES (EXCL. IC'S)	
PART	UNUSED PINS
RN1	4,6,7,8
RN3	6,7,8,9,10
RN4	8,9,10
RN5	6,7
J1	31,34,36,37,41,42,43,44,45
	71,72,73,74,83,84,85,86,87
	88,89,90,91
J2	1,2,20

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	RELEASE TO CONTROL	9/27	
	B	REVISED PER C.O. # 5389	1/2	
	C	REVISED PER C.O. # 5459		

INCHES

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
.XX ±
.XXX ±
.XXXX ±
ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

QTY REQD | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | MATERIAL SPECIFICATION

PARTS LIST

This drawing contains information which is the proprietary property of Convergent Technologies. This drawing is received in confidence and its contents may not be disclosed without the prior written consent of Convergent Technologies.

APPROVALS | DATE

DRAWN H. NGUYEN 9-85

CHECKED 9/25

APVD 9/25

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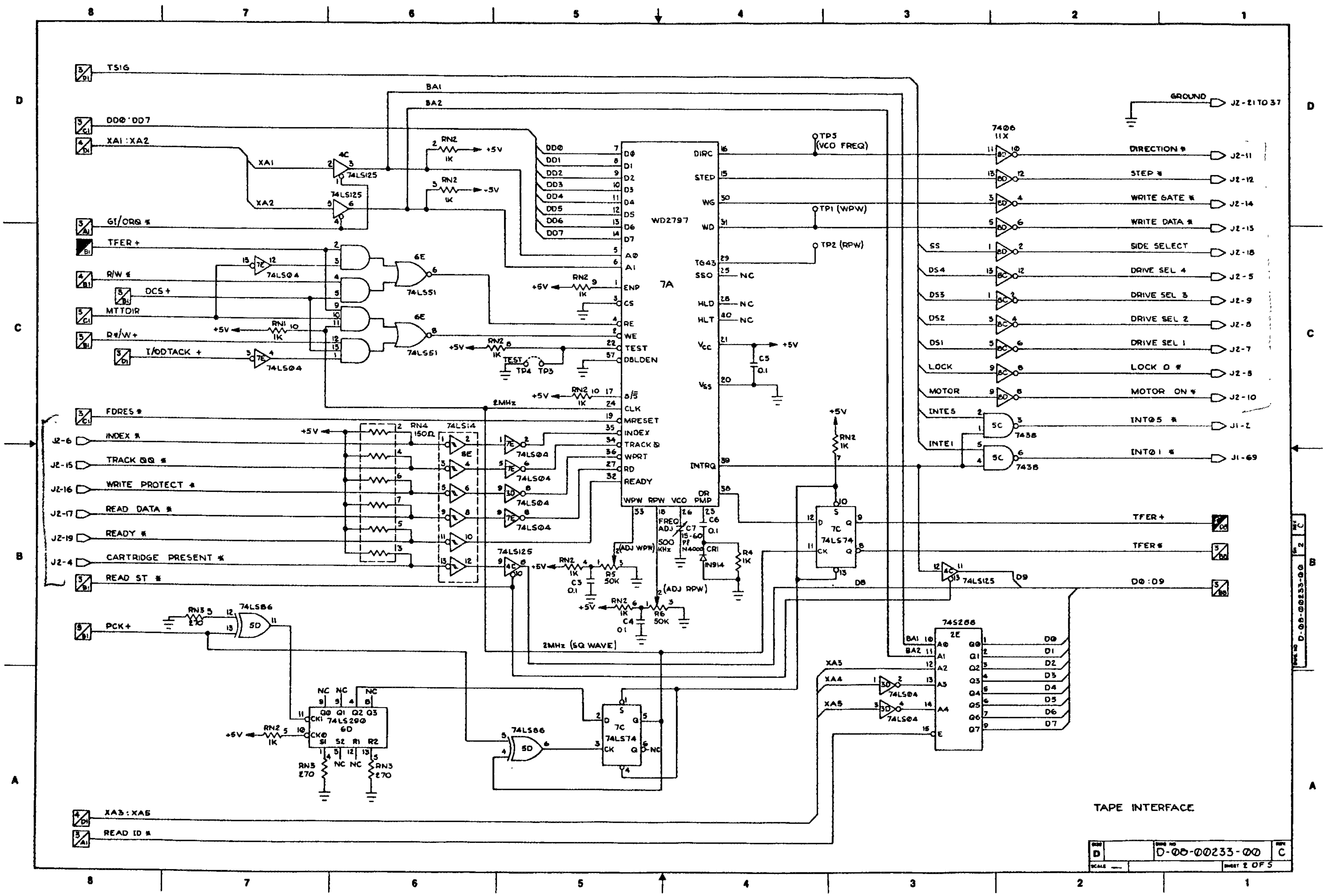
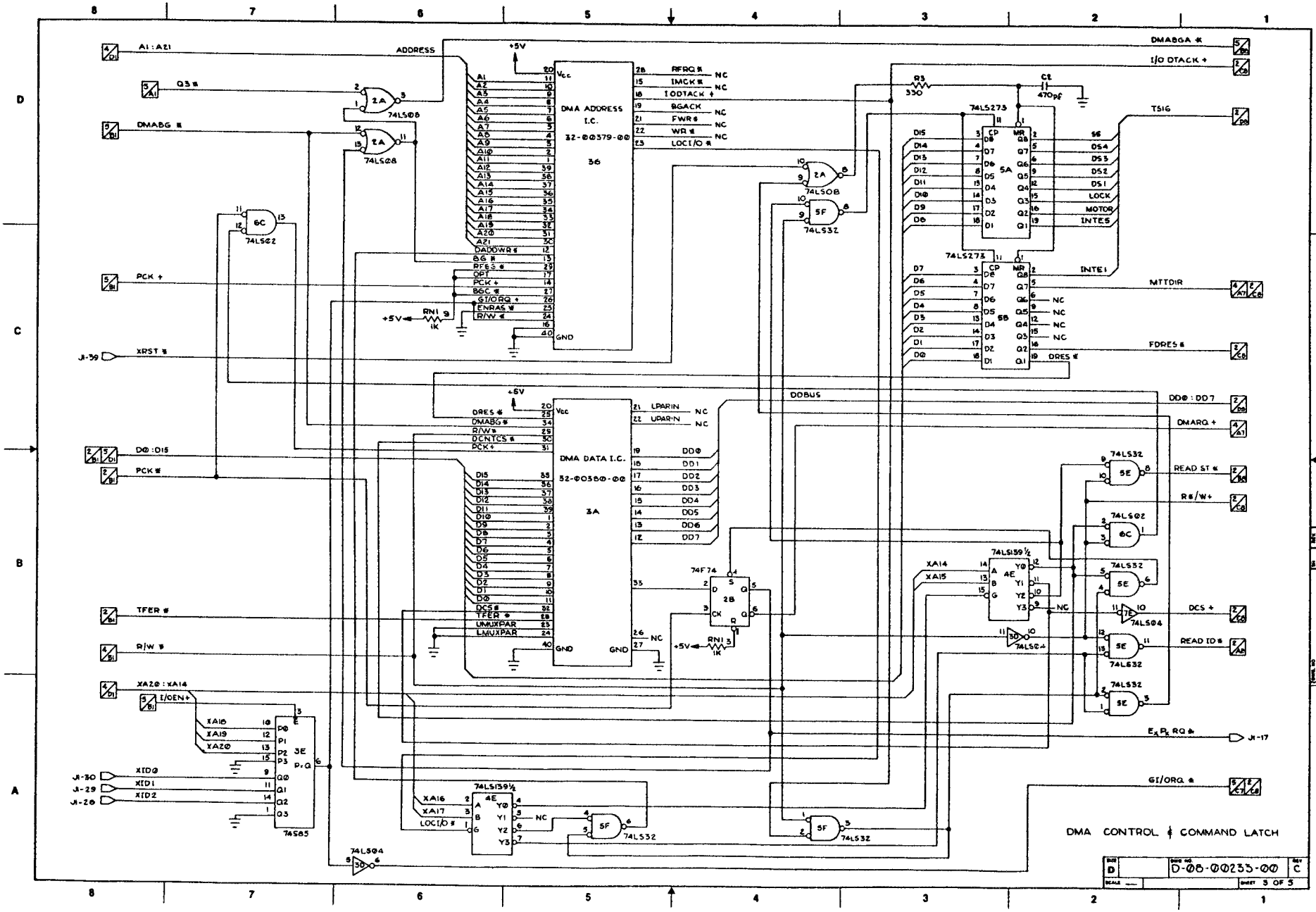
TITLE
SCHEMATIC,
S4 FLOPPY TAPE
INTERFACE MODULE

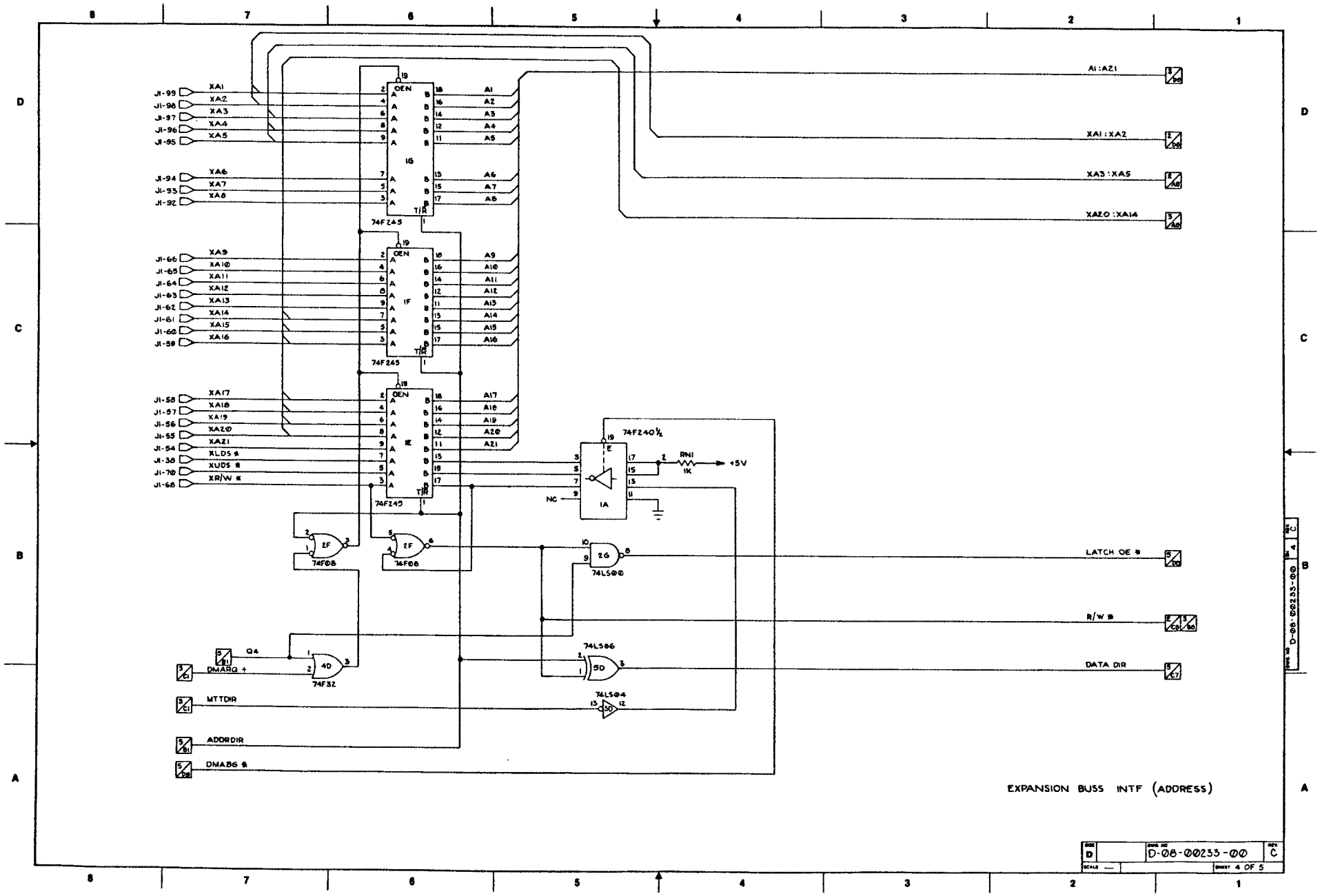
SIZE D | DWG NO D-08-00233-00 | REV C

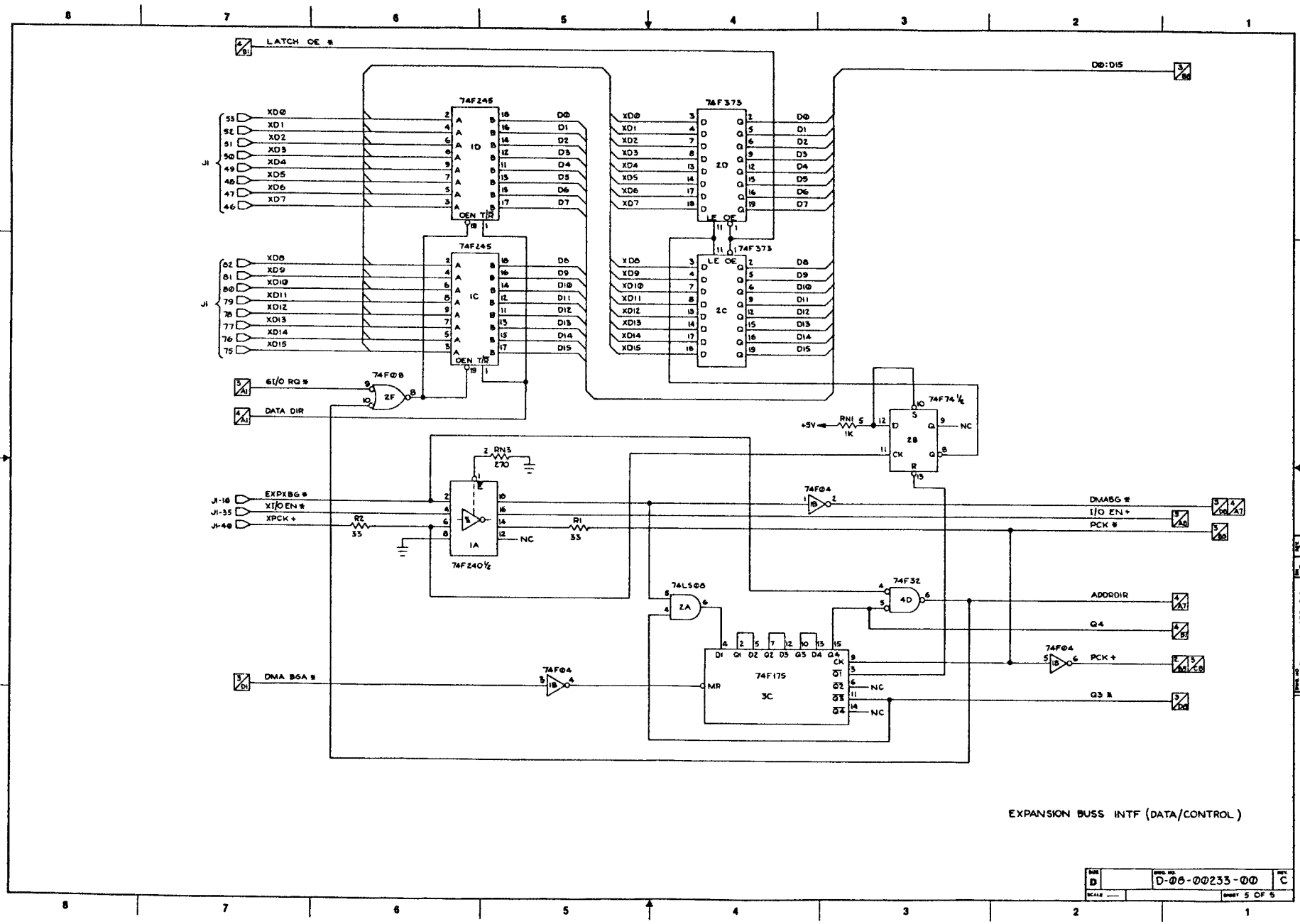
SCALE — | SHEET 1 OF 5

D-00-00233-00 REV C


TSIG
DD0 · DD7
XA1 : XA2
G1/ORQ *
TFER +
R/W *
DCS +
MTTDIR
R*/W +
I/ODTACK +
FDRES *
INDEX *
TRACK 00 *
WRITE PROTECT *
READ DATA *
READY *
CARTRIDGE PRESENT *
READ ST *
PCK +
XA3 : XA5
READ ID *
WD2797
7A
DIRECTION *
STEP *
WRITE GATE *
WRITE DATA *
SIDE SELECT
DRIVE SEL 4
DRIVE SEL 3
DRIVE SEL 2
DRIVE SEL 1
LOCK 0 *
MOTOR ON *
INT05 *
INT01 *
GROUND
J2-21 TO 37
TFER +
TFER *
D0 : D9
TP5 (VCO FREQ)
TP1 (WPW)
TP2 (RPW)
2MHz (SQ WAVE)
(ADJ WPW)
(ADJ RPW)
74S288
74LS290
74LS74
74LS86
74LS125
74LS04
74LS14
74LS51
7406
7438
TAPE INTERFACE
D-00-00233-00
C
SHEET 2 OF 5


DMA ADDRESS I.C. 32-00379-00
DMA DATA I.C. 52-00360-00
DMA CONTROL & COMMAND LATCH
D-00-00233-00
C
3 OF 5
ADDRESS
DDBUS
+5V
GND
74LS08
74LS02
74LS32
74LS273
74LS139½
74F74
74LS04
74S85
RN1 1K
330
470pf
XRST #
TFER #
R/W #
PCK +
PCK #
DMABG #
Q3 #
I/OEN+
XID0
XID1
XID2
DMABGA #
I/O DTACK +
TSIG
MTTDIR
FDRES #
DCS +
READ ID #
READ ST #
R#/W+
DMARQ +
DD0 : DD7
EXPRQ #
GI/ORQ #
INTE1
MOTOR
LOCK
INTES
DS1
DS2
DS3
DS4
DS5
DS6


J1-99 XA1
J1-98 XA2
J1-97 XA3
J1-96 XA4
J1-95 XA5
J1-94 XA6
J1-93 XA7
J1-92 XA8
J1-66 XA9
J1-65 XA10
J1-64 XA11
J1-63 XA12
J1-62 XA13
J1-61 XA14
J1-60 XA15
J1-59 XA16
J1-58 XA17
J1-57 XA18
J1-56 XA19
J1-55 XA20
J1-54 XA21
J1-36 XLDS #
J1-70 XUDS #
J1-68 XR/W #
74F245
74F240 1/2
74F08
74LS00
74F32
74LS86
74LS04
RN1
1K
+5V
NC
A1:A21
XA1:XA2
XA3:XA5
XA20:XA14
LATCH OE #
R/W #
DATA DIR
Q4
DMARQ +
MTTDIR
ADDRDIR
DMABS #
EXPANSION BUSS INTF (ADDRESS)
D-08-00233-00
SHEET 4 OF 5


LATCH OE *
D0:D15
74F245
1D
2D
74F373
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
XD8
XD9
XD10
XD11
XD12
XD13
XD14
XD15
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
OEN T/R
LE OE
1C
2C
61/O RQ *
DATA DIR
74F08
2F
74F74 1/2
2B
+5V
RN1 5
1K
NC
Z RN3
270
J1-16 EXPXBG *
J1-35 XIOEN *
J1-49 XPCK +
R2
33
R1
33
1A
74FZ240 1/2
74F04
DMABG *
I/O EN +
PCK *
74LS08
2A
74F32
4D
ADDRDIR
Q4
74F175
3C
MR
Q3 *
DMA BGA *
PCK +
EXPANSION BUSS INTF (DATA/CONTROL)
D-00-00233-00
C
SHEET 5 OF 5