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# 80C186/C188
# Addendum

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# SECTION 1

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## Introduction

This addendum describes the new features available with the ES 1800 for CMOS 80C186/C188 microprocessors. It is meant to be used in conjunction with the *ES 1800 Reference Manual for 80186/188 Microprocessors.*

All of the information and commands in the *ES 1800 Reference Manual for 80186/188 Microprocessors* work as described, except the **ON TE** and **DME** commands, which now operate as described in this addendum. In addition, the ES 1800 for the 80C186/C188 includes commands to work with the additional 80C186/C188 PCB features. The PCB contains a dynamic RAM refresh controller and a power save mode controller. Two new ON/OFF switches have been added, **IDP** and **PRE**, and there are 4 additional registers.

For the 80C18X processors, on the run-to-pause transition all interrupts are disabled unless the **IDP** switch is set to ON. Overlay memory speed is controlled by the **OVS** command. The dynamic RAM refresh registers are controlled by the **PRE** switch, and can be used to enable continuous refresh or target RAM during pause mode.

The 80C18X pod differs from the 8018X pods; with the new design, you can hang the pod from the wall or from a office cubicle divider to save desk space. A description of the hanging process is included in this addendum.

This addendum contains four major sections: a description of the new capabilities of the emulator, an alphabetical command reference for new 80C186/C188 commands, a definition of 80C18X pod jumpers used to specify choices in clock and chip select circuitry, and the pod hanging instructions.

**PCB Registers Used in Enhanced Mode (80C18X Only)**

| | *Name* |
|---|---|
| MDR | DRAM memory partition register |
| CDR | DRAM clock pre-scalar register |
| EDR | DRAM enable RCU register |
| PDC | Power save control register |

## Alphabetic Command Reference

This section includes the following commands:

| | |
|---|---|
| IDP | Interrupts During Pause |
| DME | Enable Data |
| OVS | Overlay Memory Speed |
| PRE | Refresh During Pause |
| TE | Timers |

If it becomes necessary for you to reset the emulator (<ctrl-z> by default), remember that some switch settings are set to a default state. If you do not want them in their default state, you must reset them after resetting the emulator. You can conveniently do this with a macro or you may wish to save the switch values to EEPROM and execute a LD 5 command after resetting the emulator. A typical macro example is: **_3=ON IDP+DME.**

## IDP: Interrupts During Pause (80C18X only)

| Command | Result |
|---|---|
| **ON IDP** | Honor interrupts from the target system during pause mode. The associated interrupt routine will be executed. |
| **OFF IDP** | Ignore interrupts from the target system during pause mode.<br>Default: OFF |

### Comments

The following requirements must be met in order to execute target interrupts during pause mode.

- For this mode to operate correctly, the ESL variable **PIA** must be set to the address of a block of 16 bytes of unused memory. This block may be located in overlay, but it *MUST BE UNUSED!* You can explicitly map a block of memory for this purpose.
- The interrupt service routine must return execution to the location where the interrupt occurred.
- The interrupt service routine may not execute a halt (HLT) instruction.

If the above requirements are not met, proper operation of your emulator cannot be guaranteed.

Enabling the **IDP** switch will slow the response time to some commands, such as memory reads. In order to speed command response time, interrupt service routines should not take excessive time because ESL cannot communicate with the pod while a target interrupt is being serviced.

The average interrupt latency time in the target will be increased by approximately 50 clock cycles when **IDP** is enabled.

Interrupt service routines executed while the emulator is in pause mode will not appear in the trace memory.

If you enter the reset character (default is <ctrl-z>), the **IDP** switch is automatically reset to the OFF state. You must enter the **ON IDP** command after resetting the emulator if you wish to honor target interrupts during pause mode.

## DME: Enable Data (different operation with 80C18X)

| Command | Result |
|---|---|
| **ON DME** | The DMA controllers are active during pause. The values in the DMA0 and DMA1 registers are not reloaded to the physical PCB upon pause-to-run. The following also occurs:<br><br>On a run-to-pause transition the IST register is copied to the internal RAM table. The DHLT bit is then cleared, causing DMA cycles to resume. All DMA cycles are directed to the target system. |
| **OFF DME** | The DMA controllers are not active during pause mode.<br><br>Default: OFF |

### Comments

All DMA cycles are disabled immediately upon a run-to-pause transition.

If the target system uses an external dynamic memory controller for refresh, DME must be set to OFF. This prevents memory read signals from going out to the target in pause mode.

If internal DMA is used, then DME should be ON.

If you enter the reset character (default is <ctrl-z>), the **DME** switch is automatically reset to the OFF state. You must enter the **ON DME** command after resetting the emulator if you wish to honor target interrupts during pause mode.

## OVS: Overlay Memory Speed (80C18x only)

| Command | Result |
|---|---|
| **OVS** | Display the current value of the overlay memory speed register. |
| **OVS** = *<0-15>* | Specify the number of wait states inserted before the overlay memory supplies a **RDY** signal to terminate the cycle. No wait states are inserted if **OVS** is zero. |

### Comments

The value of **OVS** determines how many cycles occur before a **RDY** signal is returned by the overlay memory. The wait state generator is only active when the **RDY** softswitch is on (ON RDY).

Assigning **OVS** a value of zero indicates that no wait states are inserted and the processor runs at full speed. A value of one inserts a single wait state, a value of two inserts two wait states, etc. The maximum number of wait states is fifteen.

### 16 MHz Overlay Operation

The overlay memory cannot operate at 16 MHz without wait states. If you are running your target system at 16 MHz and you wish to access overlay memory, one of the following statements *must* be true.

**OVS** is set to a value between one and fifteen, and the **RDY** switch is turned on.

- or -

Your target system is running with at least one wait state per memory access.

## PRE: DRAM Refresh During Pause (80C18X only)

| Command | Result |
|---|---|
| **ON PRE** | The DRAM refresh controller is active during pause mode. |
| **OFF PRE** | The DRAM refresh controller is *not* active during pause mode.<br>Default: OFF |

### Comments

When the emulator transitions between pause and run modes, the setting of the **PRE** switch determines whether the refresh register values are read from or written to the physical PCB and whether the refresh controller continues to run while the emulator is paused. The refresh control registers MDR, CDR and EDR are affected by the switch setting.

**Pause to Run Transition**

When the emulator transitions from pause to run mode, the **PRE** switch setting determines if the values of the MDR, CDR and EDR registers in the emulator's RAM image are loaded to the physical PCB.

If the **PRE** switch is OFF, the registers are loaded to the physical PCB.

If the **PRE** switch is ON, the registers are *not* loaded to the physical PCB. This prevents the currently active register values being overwritten with values from a previous run state.

**Run to Pause Transition**

When the emulator transitions from run to pause mode, the current values of the MDR, CDR and EDR registers are loaded from the physical PCB to the emulator's RAM image of the CPU registers.

If the **PRE** switch is ON, no other action occurs and the refresh controller continues to run while the emulator is paused.

If the **PRE** switch is OFF, the refresh controller is disabled immediately after the transition to pause mode by clearing bit 15 of the EDR register in the physical PCB.

If you enter the reset character (default is <ctrl-z>), the **PRE** switch is automatically reset to the OFF state. You must enter the **ON PRE** command after resetting the emulator if you wish to honor target interrupts during pause mode.

You can modify refresh registers while you are in pause mode, and, if **PRE** is off, those values continue to be active when run mode is entered. Registers are modified using a **<register> = <value>** command.

For this mode to operate correctly, the ESL variable **PIA** must be set to the address of a block of 16 bytes of unused memory. This block may be located in overlay, but it *MUST BE UNUSED!* You can explicitly map a block of memory for this purpose.

The table below summarizes the effect of the refresh switch.

*Effect of* **PRE** *switch on Run/Pause Transitions*

| Switch Setting | Pause to Run Transition | Run to Pause Transition |
|---|---|---|
| ON | The emulator's RAM image of the refresh registers are *not* loaded to the physical PCB before entering run mode. | The values in the refresh registers are loaded into the emulator's RAM image of the CPU registers. |
| OFF | The emulator's RAM image of the refresh registers are loaded to the physical PCB just before running the target code. | The values in the refresh registers are loaded into the emulator's RAM image of the CPU registers. The refresh controller is then disabled by clearing bit 15 of the EDR register. |

## TE: Timers (different operation with 80C18X)

| Command | Result |
|---|---|
| **ON TE**<*0,1,2*> | The specified PCB timer (0,1 or 2) is active during pause mode. |
| **OFF TE**<*0,1,2*> | The specified PCB timer (0,1 or 2) is not active during pause mode.<br>Default: OFF |

### Comments

When the emulator transitions between pause and run modes, the settings of the TE switches determine whether the timer register values are read from or written to the physical PCB and whether the timer continues to run while the emulator is paused. The mode control word registers (MCW0, MCW1 and MCW2) and the timer count registers (TC0, TC1 and TC2) are affected by the switch setting.

**Pause to Run Transition**

When the emulator transitions from pause to run mode, the **TE** switch setting determines if the values of the MCW and TC registers in the emulator's RAM image are loaded to the physical PCB.

If the **TE** switch is OFF, the registers are loaded to the physical PCB. The value loaded into the MCW register determines whether or not the timer becomes active during run mode.

If the **TE** switch is ON, the registers are *not* loaded to the physical PCB. This prevents the timer count register being overwritten by the old count value (this is undesirable if the timer was counting while the emulator was paused).

**Run to Pause Transition**

When the emulator transitions from run to pause mode, the current value of the MCW and TC registers are loaded from the physical PCB to the emulator's RAM image of the CPU registers.

If the **TE** switch is ON, no other action occurs and the timer continues to run while the emulator is paused.

If the **TE** switch is OFF, the timer is disabled immediately after the transition to pause mode by clearing bit 15 of the mode control word register in the physical PCB.

You can modify timer registers while you are in pause mode, and, if **OFF TE** is specified, those values continue to be active when run mode is entered. Registers are modified using a **<register>** = **<value>** command.

The table below summarizes the effect of the timer switches.

| *Effect of* **TE** switches on Run/Pause Transitions | | |
|---|---|---|
| Switch Setting | Pause to Run Transition | Run to Pause Transition |
| ON | The emulator's RAM image of the specified timer register is *not* loaded to the physical PCB before entering run mode. | The value in the specified timer register is loaded into the emulator's RAM image of the CPU registers. |
| OFF | The emulator's RAM image of the specified timer register is loaded to the physical PCB just before running the target code. | The value in the specified timer register is loaded into the emulator's RAM image of the CPU registers. The timer is then disabled by clearing bit 15 of the appropriate mode control word register. |

# Pod Jumper Definitions

There are two jumpers in the 80C18X pod which can be changed to specify choices in clock and chip select circuitry.

## 80C18X Pod Jumpers

The 80C18X probe is shipped configured for 3rd harmonic crystal clock generation using the circuit layout described in the Intel manual for the 80C186/C188. Jumpers JP1 and JP2 may be reconfigured to allow slower clocks (XTAL fundamental) or target system generated clock input.

### Accessing the Jumpers

To access the jumpers, remove the snap-on pod cover. and then remove the pod cover. The jumper numbers are written on the board. Place the shunt on the appropriate jumper setting.

### Setting the Jumpers

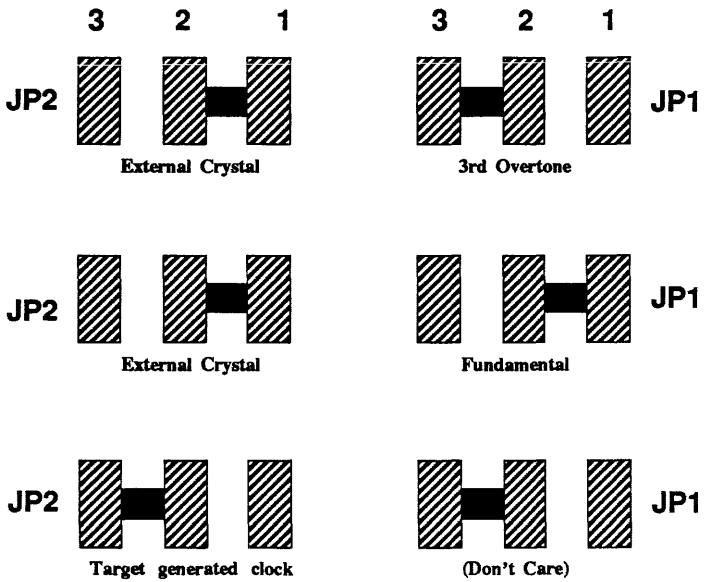
JP2 Used to select external crystal or target system generated clock.

JP1 Significant only when external crystal is selected by JP2 - selects between fundamental and 3rd-overtone crystal configurations.

| | |
|---|---|
| Target system generated clock: | JP2 2-3 |
| External crystal: | JP2 1-2<br>JP1 2-3 (3rd-overtone)<br>JP1 1-2 (fundamental) |

Figure 1-1 shows the pin positions for these jumpers.

*Figure 1-1. Jumper 1 and 2 Pin Positions*



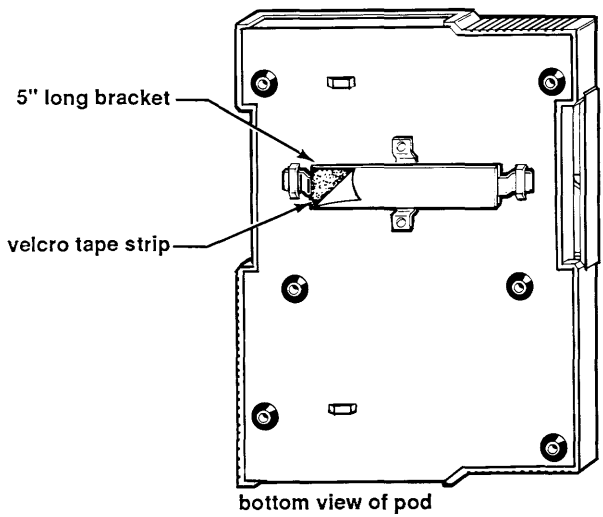
## Saving Desk Space

To save limited desk or table space, the 80C186/C88 pods can be supported from walls, an overhead hook, or other non-horizontal surfaces either by velcro tape or by a hanging strap.

### Velcro Tape

To support the pod using velcro tape, you must first attach the 5" long bracket to the bottom sheet metal of the pod (you may need to bend the bracket slightly). Figure 1-2 shows bracket placement. When the bracket is in place, simply peel off the adhesive backing on the velcro tape strip and firmly press the tape onto the bracket as shown in Figure 1-2. You can now attach the 80C86/C88 pod to any surface that adheres to velcro, such as many types of office partitions.

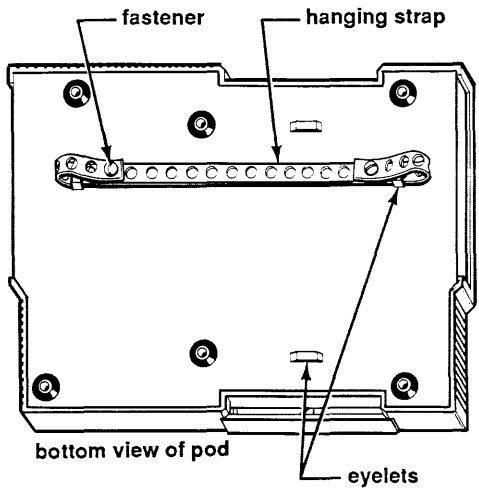
*Figure 1-2. Velcro Tape Support*



## Hanging Strap

The hanging strap can be threaded through either set of eyelets on the bottom sheet metal of the pod. The 5" long bracket is not needed when using the hanging strap. Figure 1-3 shows both of these configurations. After threading the strap through the eyelet, bend the strap back on itself and fasten it with the enclosed fasteners. Make sure the fasteners on both sides are firmly closed before hanging the pod from the strap.

*Figure 1-3. Hanging Strap Support*



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