July 10, 1986

CONTENTS

PART 1

Freeport

Product Description

PART 1

Freeport
Product Description

General

Freeport is an enhanced Macintosh Plus that supports internal and external customized expansion options including:

from Apple Computer,Inc.

* Internal 20MB Hard Disk or a Second Internal Sony Floppy Disk Drive

and from third party vendors

* External Video Board
* Ethernet/Token Ring Interface Board
* Modem Board
* Accelerator/Coprocessor Boards
* Etc.(This list is suggestive only, not limiting)

Freeport supports the same peripherals as Macintosh Plus except that the keyboard and mouse follow the new corporate Apple DeskTop Bus design.

Product Design

External Features

* Same overall form factor as Macintosh Plus
* Apple DeskTop Bus keyboard and mouse (two connectors at rear)
* Floppy disk slot streamlined, compatible with new Frog styling
* Restyled front bezel and rear housing, ventilation slots added for better cooling
* Optional pluggable slot in front housing, for a second internal floppy disk drive
* Plastic snap-out door at rear to support out-of-box I/O

Internal Features

* Optional hard disk or optional second Sony, above the standard Sony disk drive
* Higher capacity power supply to support the optional floppy or hard disks
* Connectors for the optional floppy, optional SCSI hard disk, and expansion hardware (daughterboard or external)
* Fan for cooling
* New swing-away logic board mounting to allow insertion with third-party daughterboard present

Hardware

Logic Board

* 8 MHz 68000 CPU
* Enhanced memory access yields 16.8% increased speed when operating from RAM
* Gate array implementation of PAL and discrete logic devices
* Seven year lithium battery for clock and calendar
* Internal-- two Floppy Disk and SCSI connectors
* External--two Serial, two Apple DeskTop Bus, SCSI, Floppy Disk, and Sound port connectors

Analog Section

* New 80 Watt, wide input range power supply
* Improved display sweep section
* Fan

Software

System

* New ROM with minimum changes from Macintosh Plus
* Changes include new SCSI manager, support for Apple DeskTop Bus, and modifications to the AppleTalk drivers to support the new Apple serial port architecture

Application

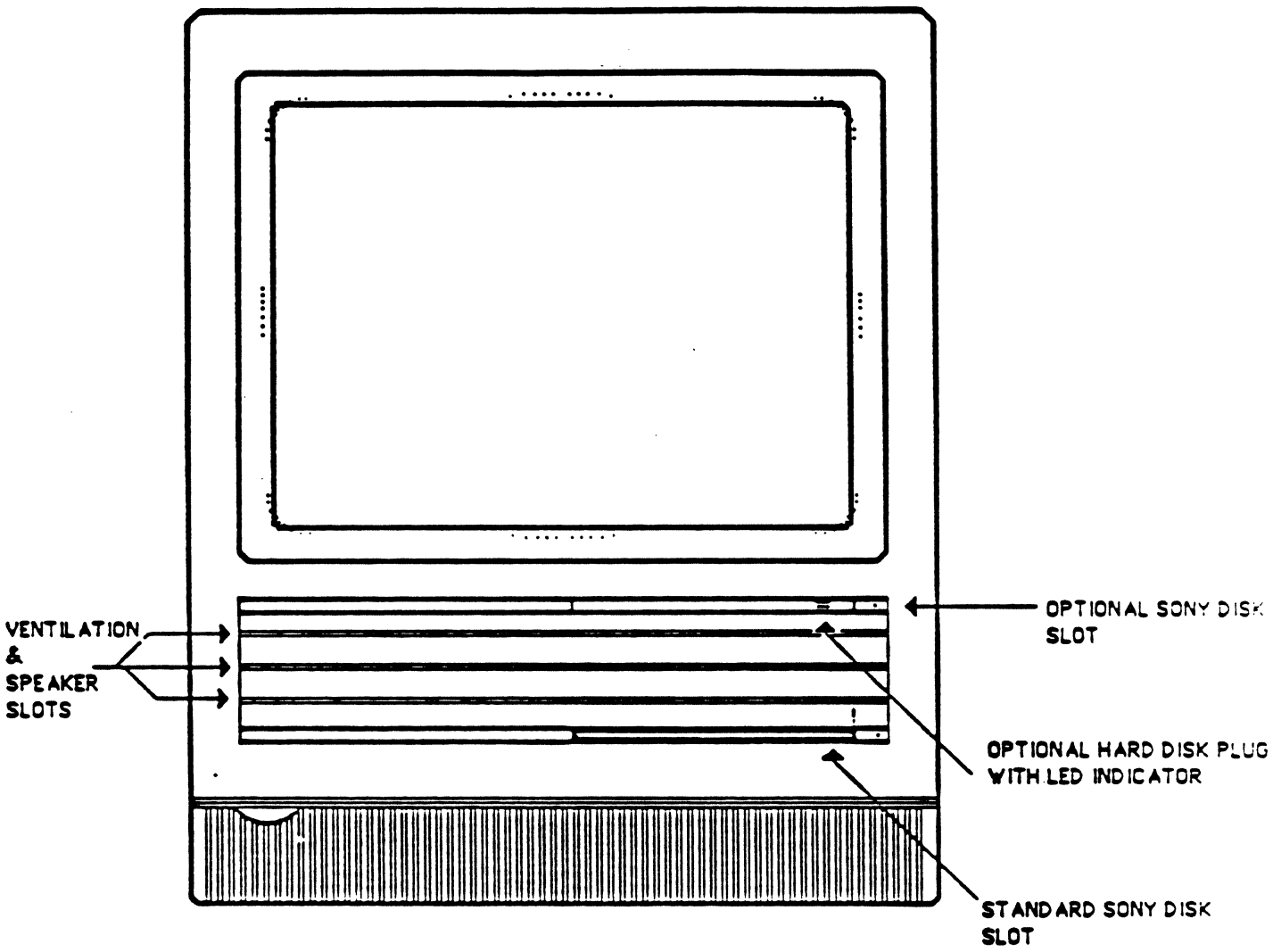
* Boot chooser to allow start-up drive selection
* Compatible with Macintosh Plus

Options

* Internal 20 Megabyte SCSI hard disk compatible with SCSI HD-20, or a second 800K internal floppy disk drive

Freeport

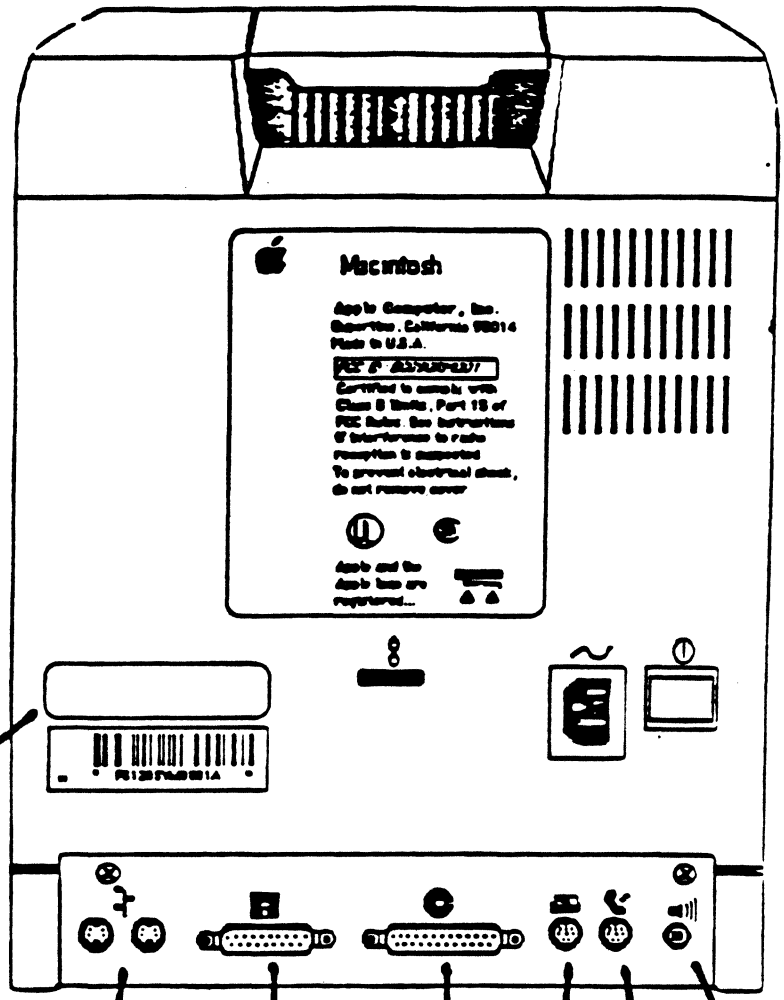
FRONT BEZEL



Freeport INCORPORATES LATEST
"FROG" DESIGN WORK

3-19-86

Freeport
REAR
HOUSING



Optional, Third Party Expansion Port

Snap-In/Out Door, Removable only from inside the housing.

Apple DeskTop Bus (2)

External Floppy

SCSI Port

Printer

Modem

Sound

CONNECTORS

PART 2

Freeport System: Comparison with MacPlus

Macintosh Plus vs Freeport
Hardware Comparison
7-17-86

FEATURE	MACINTOSH	FREEPORT
PROCESSOR:	68000 CPU (16 bit)	68000 CPU (16 bit), Increased speed
CLOCK FREQUENCY:	7.8336 MHZ	7.8336 MHZ
FLOPPY DISK DRIVE:	800K Internal Floppy Drive, Optional 800K External Drive	800K Internal Floppy Drive, Optional 2nd 800K Internal Drive, Optional 800K External Drive
HI SPEED PERIPH.:	SCSI Port	SCSI Port
HARD DISK:	Optional HD20, Optional SCSI HD (External)	Optional HD20, Optional SCSI HD20 (External) Optional SCSI HD20 (Internal)
SERIAL PORTS:	2 Mini-8 Built-In Serial Ports	2 Mini-8 Built-In Serial Ports, with extended input handshake capability
HARDWARE EXPANSION:	No Provision	Access to 68000 pins Customizable I/O Port in removable door at rear
SOUND:	Mac Sound	Mac Sound
RAM EXPANSION:	1MB Expandable to 4MB RAM (SLANTED SIMM)	1 MB Expandable to 4MB RAM (SIMM)
ROM EXPANSION:	New 128 KB ROM with Hierarchical File System	New 256 KB ROM with Hierarchical File System - ROM modified to support SCSI, ADTB, AppleTalk

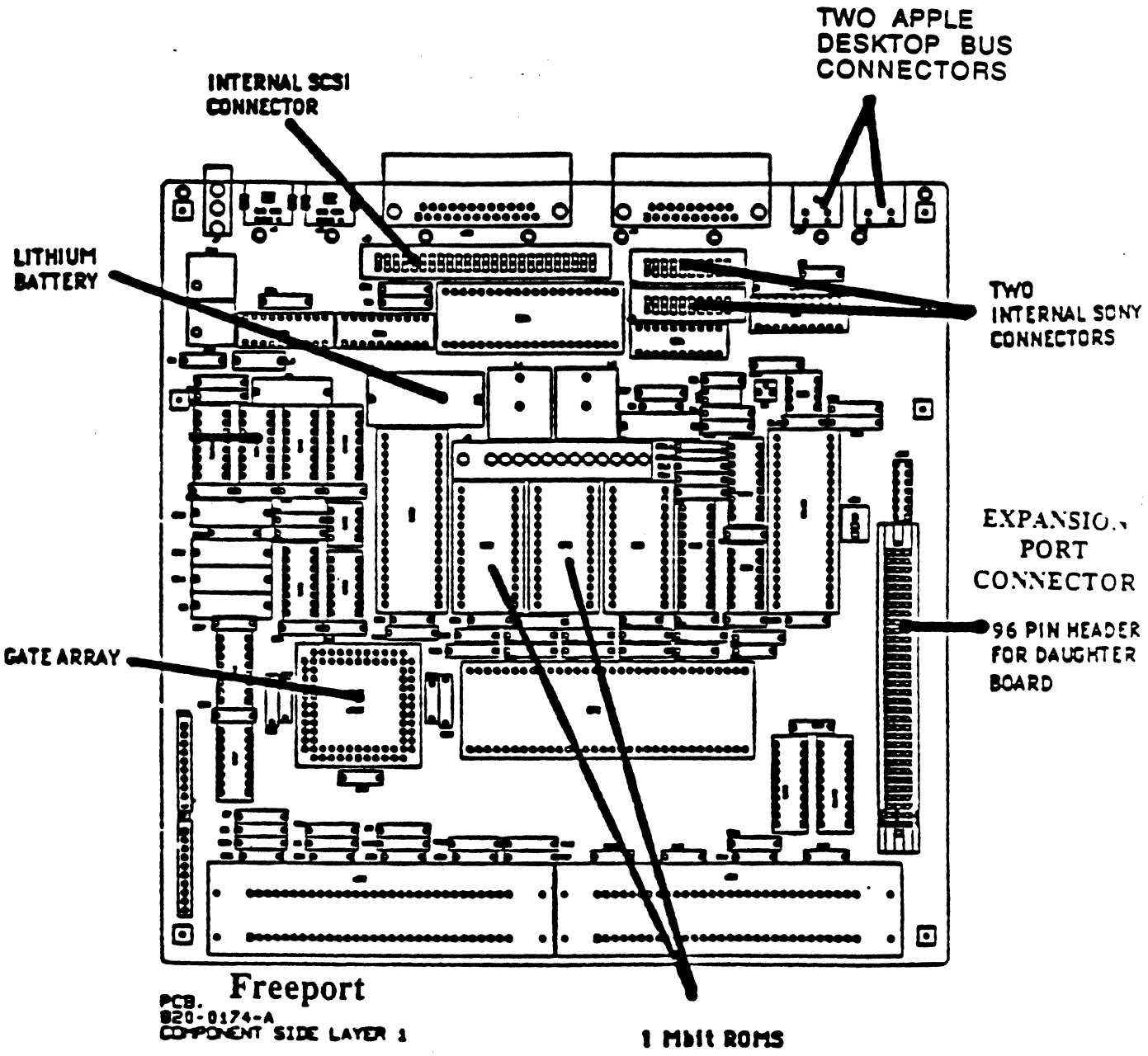
Mac Plus vs Freeport
Hardware Comparison, page 2

KEYBOARD:	Cursor and Numeric Keyboard	Cursor and Numeric Keyboard via Apple DeskTop Bus, Allows additional input devices e.g., Graphics Tablet
VIDEO DISPLAY:	Built-In Monitor 9", 512 X 342 B/W	Built-In Monitor 9", 512 x 342 B/W

PART 3

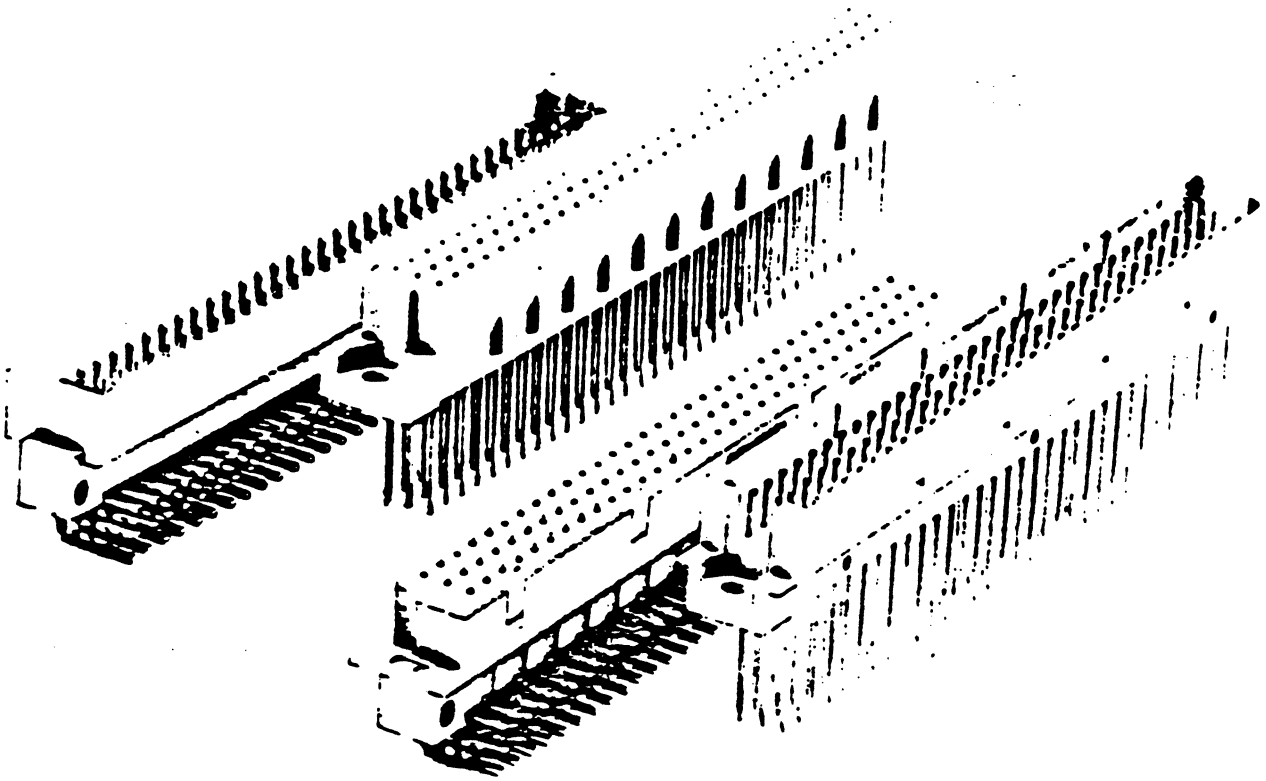
Main Logic Board (Mother Board)

Freeport MAIN LOGIC BOARD



PART 4

High Performance Expansion Slot

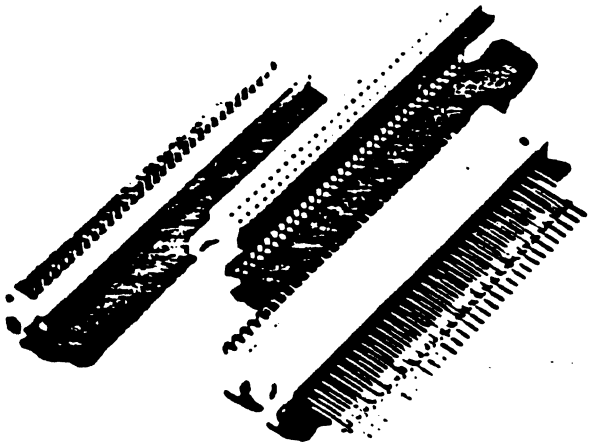


PC Connectors G06/G60

Two piece, high density pcb connectors per MIL-C-55302/DIN 41612

G06-4/483

CANNON ITT
The Global Connector



G06 connectors are designed for printed circuit boards size 3.93" x 6.30" (100 x 160). They also can be used for multilayer boards as for flat ribbon cable. They comply with the requirements of the MIL-C-55302 and European specifications DIN 41612, VG 95324 and IEC.

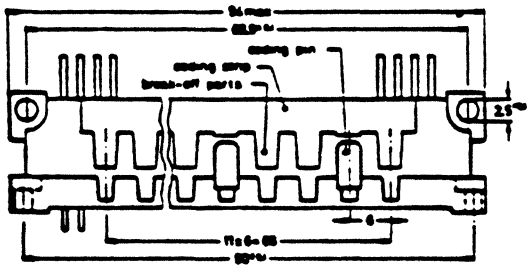
Contacts
32/64/96 contacts are spaced at .100" (2.54 mm) centers in the male and female connectors giving a high contact density and a space saving construction. The 64/96 contact connectors G06 are also available partially equipped with 32 contacts. (See the modification codes shown in the Ordering Information on page 4.)

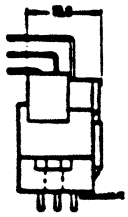
Three different contact arrangements with cavities for coaxial, HP and/or HV-contacts are also available.

An extraction tool for these special contacts is designated CET-C6B.

Mounting
Mounting is by screws for both the male and female connectors. Furthermore, a version of the female connector with short solder posts can be soldered directly into PC boards.

Coding
Coding is possible without loss of contact.
Coding key part no.: 201-8518-000

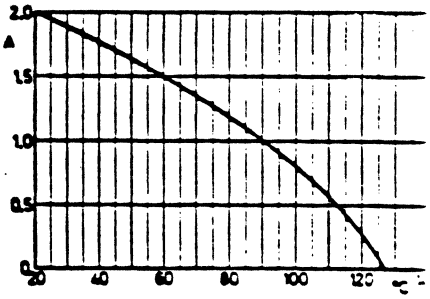




Standard Data

Materials	
Contacts	Female: Copper alloy CuNiSn (Male: Copper alloy CuZn
Contact finish	Selective gold plate over nickel at contact area
Contact terminations	tin plated
Insulator material	Polyester GF, not pigmented. UL94 V-0 rated
Mechanical features	
Number of contacts	32, 64, 96
Contact spacing	.100"/2,54 mm
Contact terminations	Female: Mini Wire Wrap post, short solder pins Male: short solder pins 90°
Temperature range (climatic category)	–55/125°C (–67/257°F)
Operating temperature (long term)	–55/105°C (–67/221°F)
Insertion force	35 N max. for 32 contacts 65 N max. for 64 contacts 95 N max. for 96 contacts
Gauge retention force per contact	0,15 N max.
Durability	500 mating cycles min.

Electrical Data
Rated current per contact

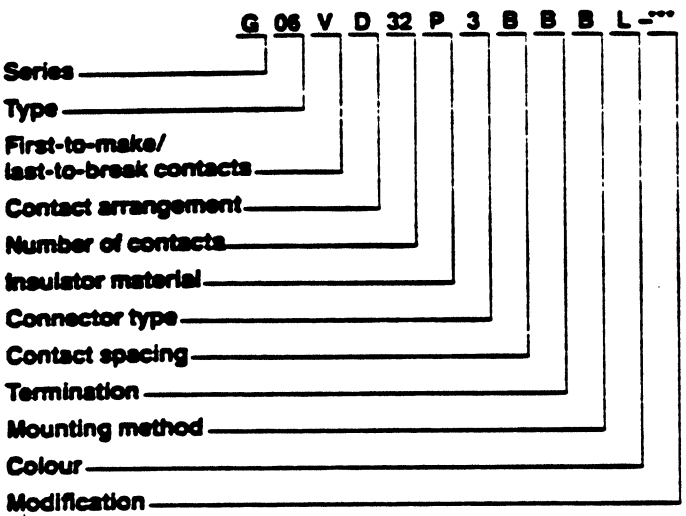


Operating voltage	300 V_{rms}
Test voltage	1000 V_{rms}
Insulator resistance	1 teraohm (10^{12}) min.
Contact resistance	15 milliohms max.

Wire and Tools

Wire		Recommended Gardner-Denver Tools			
AWG	Dia. mm	Standard Wrapping Bit	Modified Wrapping Bit	Sleeve	Number of Turns Bare Wire
30	0.25	–	507063	507100	
28	0.32	–	609278	507100	
26	0.40	–	606445	507100	6

Ordering Information



Series	G	– ITT Cannon designation
Type	06	– PC connector per MIL-C-55302, DIN 41612 and VG 95324
First-to-make/ last-to-break contacts	V*	– first-to-make/ last-to-break contacts [4] three rows: a1 and c32, two rows: a1 and b32 (standard, other upon request).
Contact arrangements	D	– double read-out [1]
	M	– three contact rows [2]
Number of contacts	32	– 64 – 96 [3]
Insulator material	P	– Polyester GF
Connector type	3	– female [5]
	4	– male
	5	– male, with coding part
Contact spacing	B	– 2.54 mm (.100")
Termination	B	– short solder post (female and male)
	D	– Mini wire wrap (female only) [6]
	E	– 90° solder post (male only)
	K	– for ribbon cable (Speedy only)
	L	– for daisy-chain (Speedy only)
Mounting method	A	– no mounting (Speedy only)
	B	– two through-holes
Colour	L	– not pigmented
Modification	004	– 64 contacts, row a and c, in 96 contact insulator
	005	– 32 contacts, in row a only, in 64 contact insulator
	006	– 32 contacts, staggered, beginning at a1, in 64 contact insulator
	019	– 32 contacts, row a and c, cavities with even numbers only,
	028	– Wire Wrap post 17 mm, female only (consult factory)
	029	– VG-version
	034	– Short solder post length for female: 4 mm (standard) Without modification code length 3 mm
	067	– 32 contacts, row b, in 96 contact insulator
	081	– 64 contacts, row a and b in 96 contact insulator
	090	– gold flash on contact tail
	107	– MIL version
	702	– industrial version

* Indicate V only, if first-to-make/ last-to-break contact is required

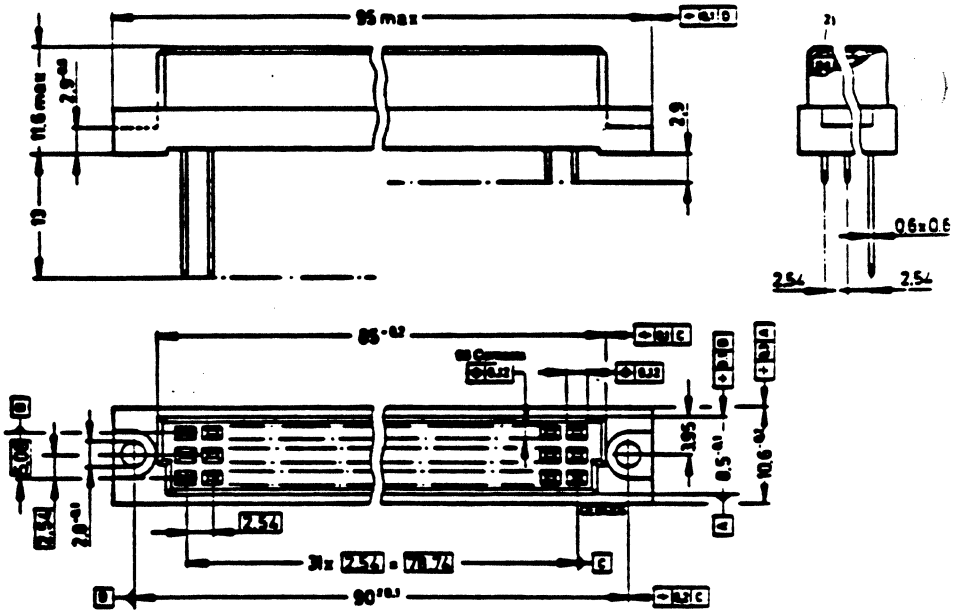
1) 32 and 64 contacts
2) 96 contacts
3) For "Number of contacts" indicate all contacts incl. empty cavities
4) male only
0.5 mm ±0.3 mm tolerance (standard),
1.0 mm ±0.4 mm tolerance (modification –103)
5) coding key for female only. Part Nr. 201-6518-000
6) different lengths are possible. Please consult factory

Cross Reference List

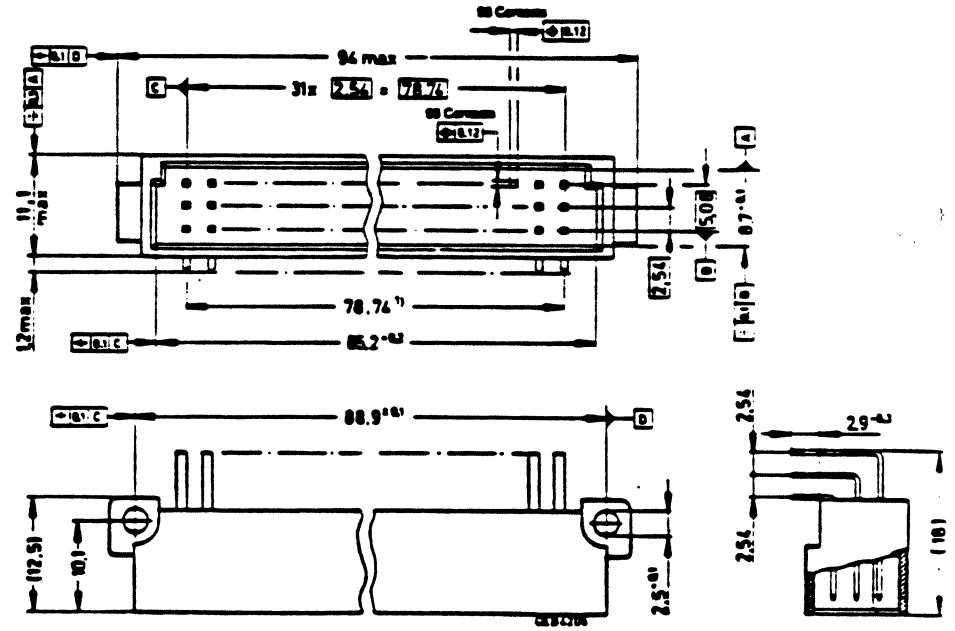
Government Designation	ITT Cannon-Designation
M55302/131-01	G06M96P4BEBL-107
M55302/131-02	G06M96P4BEBL-004-107
M55302/132-01	G06M96P3BBBL-107
M55302/132-02	G06M96P3BDBL-107
M55302/132-03	G06M96P3BDBL-028
M55302/132-04	G06M96P3BBBL-004-107
M55302/132-05	G06M96P3BDBL-004-107
M55302/132-06	G06M96P3BDBL-004-028
M55302/133-01	G06D64P4BEBL-107
M55302/133-02	G06D64P4BEBL-067-107

Government Designation	ITT Cannon-Designation
M55302/133-03	G06D64P4BEBL-005-107
M55302/134-01	G06D64P3BBBL-107
M55302/134-02	G06D64P3BDBL-107
M55302/134-03	G06D64P3BDBL-028
M55302/134-04	G06D64P3BBBL-005-107
M55302/134-05	G06D64P3BDBL-005-107
M55302/134-06	G06D64P3BDBL-005-028
M55302/134-07	G06D64P3BBBL-067-107
M55302/134-08	G06D64P3BDBL-067-107
M55302/134-09	G06D64P3BDBL-067-028

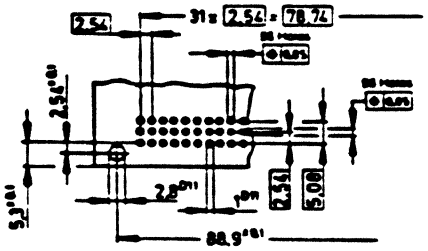
Female Connector, 96 contacts
Part No. G06M96P3B* BL**



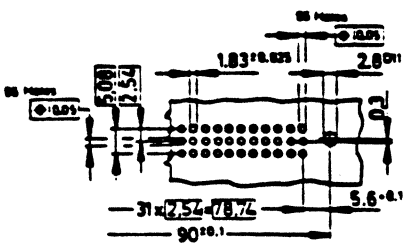
Male Connector 96 contacts
Part No. G06M96P4B* BL**



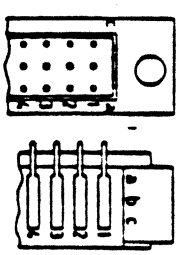
PC Board . . . BEBL



. . . BBBL



Contact Identification

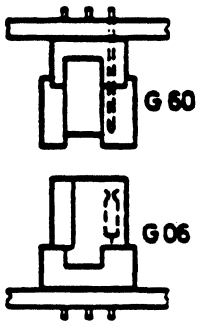


* Please add termination type
** Please add modification

(1) Termination suitable to PC board holes
(2) Contact mating face selectively gold plated

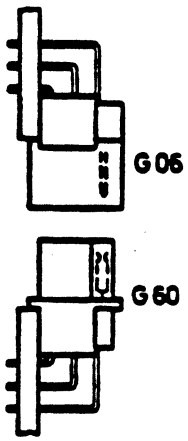
Application examples

Sandwich-connection



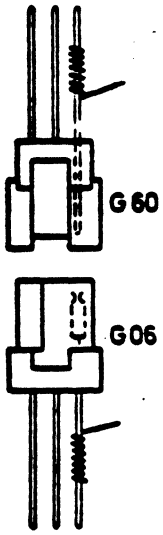
G06M96P3BBBL
G60M096P4BBBM...

Continuing connection

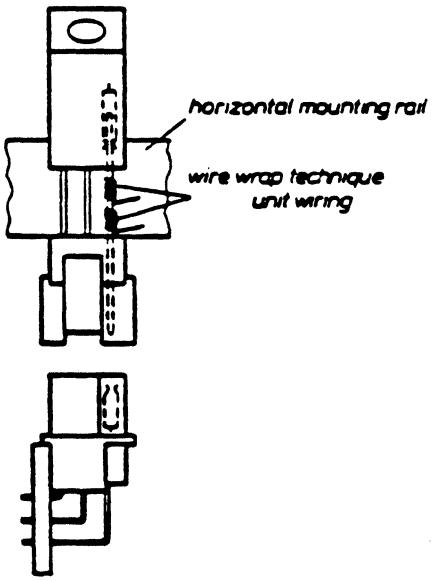


G06M96P4BEBL
G60M096P3BEBM...D...

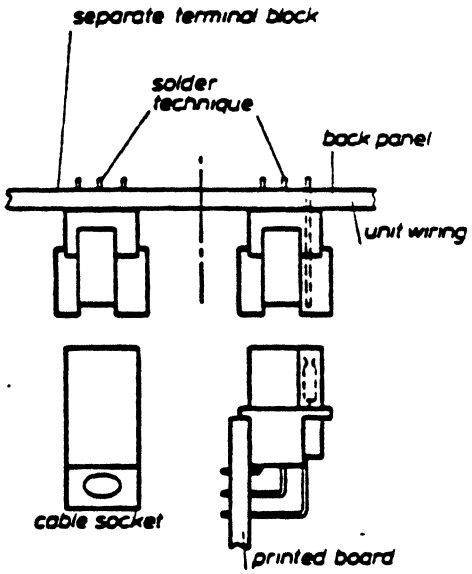
Termination block



G06M96P3BDBL
G60M096P4BDBM...



G60...096P...BDBM...
G60M096P...BEBM...D...



G60...096P...BBBM...
G60M096P...BEBM...D...

PART 5

Apple DeskTop Bus and

Human Interface Peripherals

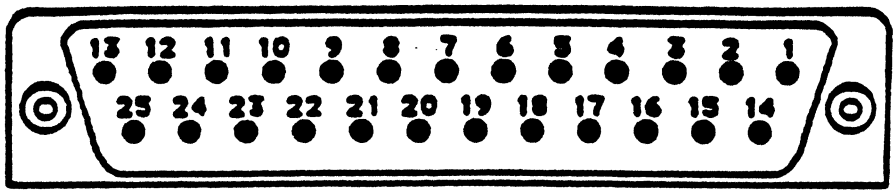
KEY NO.	KEY CODE	LEGEND	KEY NO.	KEY CODE	LEGEND	KEY NO.	KEY CODE	LEGEND
81	7F7FH	Reset (Δ)	28	1FH	O	56	08H	C
1	35H	Esc	29	23H	P	57	09H	V
2	12H	1	30	21H	[	58	0BH	B
3	13H	2	31	1EH	]	59	2DH	N
4	14H	3	32	24H	Return	60	2EH	M
5	15H	4	33	59H	7	61	2BH	,
6	17H	5	34	5BH	8	62	2FH	.
7	16H	6	35	5CH	9	63	2CH	/
8	1AH	7	36	4EH	-	64	38H	Shift
9	1CH	8	37	36H	Control	65	3EH	UP ARROW
10	19H	9	38	00H	A	66	53H	1
11	1DH	0	39	01H	S	67	54H	2
12	1BH	-	40	02H	D	68	55H	3
13	18H	=	41	03H	F	69	4CH	ENTER
14	33H	Delete	42	05H	G	70	39H	Caps Lock
15	47H	Clear	43	04H	H	71	3AH	Option
16	51H	=	44	26H	J	72	37H	APPLE
17	4BH	/	45	28H	K	73	31H	(SPACE)
18	43H	*	46	25H	L	74	32H	`
19	30H	Tab	47	29H	;	75	2AH	\
20	0CH	Q	48	27H	'	76	3BH	L. ARROW
21	0DH	W	49	56H	4	77	3CH	R. ARROW
22	0EH	E	50	57H	5	78	3DH	DOWN ARROW
23	0FH	R	51	58H	6	79	52H	0
24	11H	T	52	45H	+	80	41H	.
25	10H	Y	53	38H	Shift			
26	20H	U	54	06H	Z			
27	22H	I	55	07H	X			

TABLE 2 KEY CODES AND LEGENDS

PART 6

SCSI Interface to Hard Disk

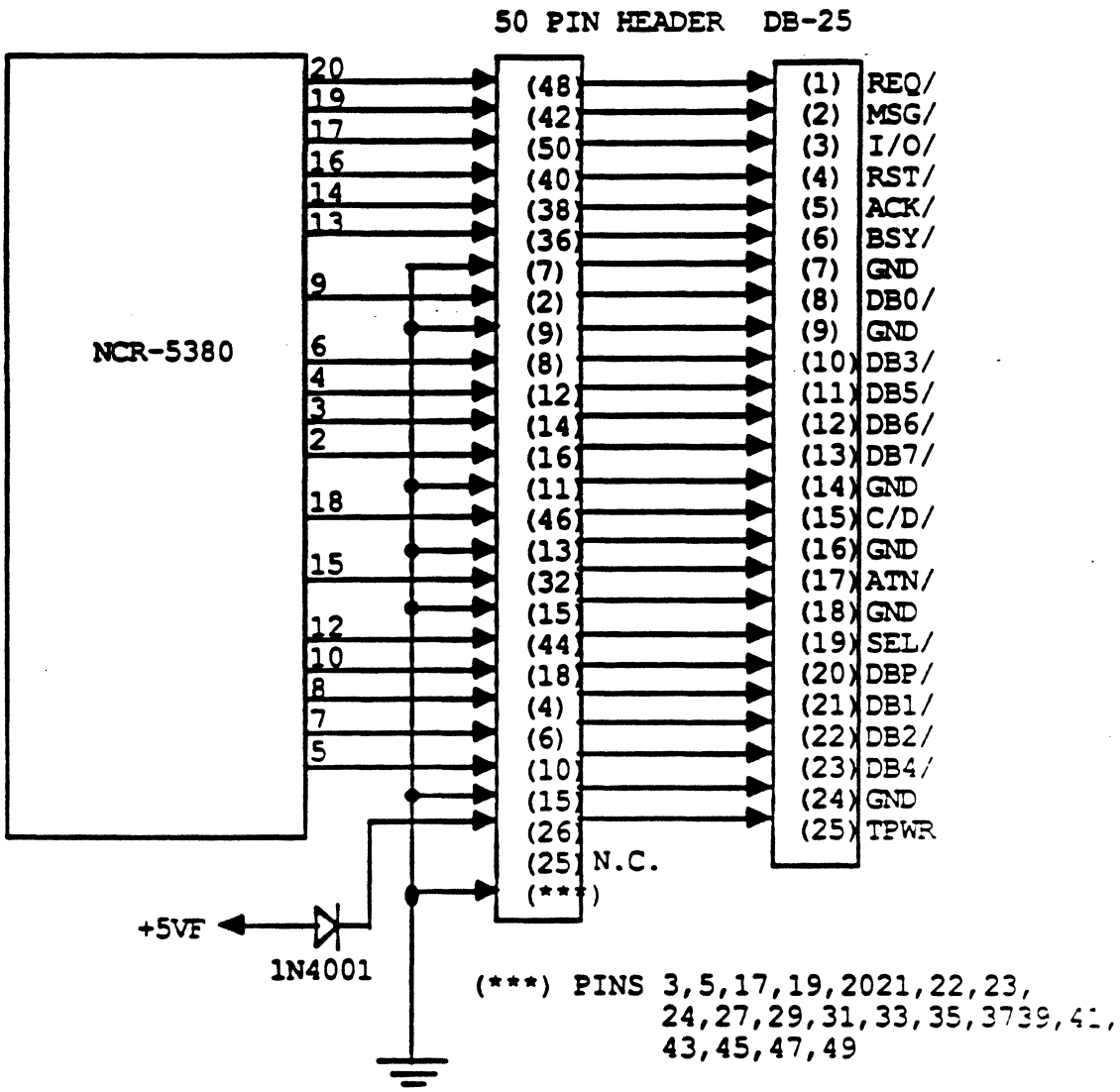
Figure 6 shows the DB-25 pinout for the SCSI connector at the back of the Freeport .



1	REQ	14	Ground
2	MSG	15	C/D
3	I/O	16	Ground
4	RST	17	ATN
5	ACK	18	Ground
6	BSY	19	SEL
7	Ground	20	DBP
8	DB0	21	DB1
9	Ground	22	DB2
10	DB3	23	DB4
11	DB5	24	Ground
12	DB6	25	TPWR
13	DB7		

Figure 6. Pinout for SCSI Connector

Freeport SCSI CONNECTOR PINOUT



(***) PINS 3,5,17,19,2021,22,23,
24,27,29,31,33,35,3739,41,
43,45,47,49

JLM 4/16/86

APPLE COMPUTER, INC.
20525 Mariani Avenue
Cupertino, CA 95014

1.0 INTRODUCTION

This specification describes the electrical characteristics of the APPLE SCSI BUS system.

2.0 APPLE REFERENCE DOCUMENTS

2.1 SCSI CABLE SPECIFICATION : 569-0407
2.2 APPLE SCSI COMMAND PROTOCOL : 062-2075
2.3 SCSI TERMINATOR ASSEMBLY : 590-0348
2.4 SCSI CONNECTORS :

DB25 MALE	520-0030
PLUG 50 PIN MICRORIBBON D MALE	519-0400 & 519-0401
PLUG 50 PIN MICRORIBBON D FEMALE	519-0410 & 519-0411

2.5 ESD: 062-0302

3.0 PHYSICAL CHARACTERISTICS

This section contains the physical definition of the APPLE SCSI BUS. The connectors, cables, signals, terminators, and bus timing needed to implement SCSI are specified.

3.1 Physical Description. APPLE SCSI BUS is used to daisy-chain SCSI devices to APPLE personal computers. An APPLE computer connects the SCSI bus through its female DB25 connector.

APPLE SCSI BUS cable accessories consist of an 18 inch System Cable, 1.0 meter long Peripheral Interface Cable with 50 pin male connectors at both ends, 1.0 meter long Cable Extender with one 50 pin female connector at one end and one 50 pin male connector at the other end; and lastly, a terminator block with a 50 pin female connector at one end and a 50 pin male connector at the other end. The 50 pin connectors used in APPLE SCSI BUS are the alternative 2, shielded connectors described in the ANSI X3T9.2 document rev. 17B and are commonly called "blue ribbon connectors".

An 18 inch long System Cable, Assembly 590-0345, is used to connect an APPLE computer to a SCSI device.It has a male DB25 connector for the APPLE personal computer and a 50 pin male blue ribbon connector to attach the first SCSI bus device.

APPLE SCSI BUS should be terminated at both ends with termination resisters. APPLE Macintosh computer does not have internal bus terminator. All APPLE SCSI devices should not have an internal terminator. The first SCSI device requires a terminator plugged to its output female connector if it is the only bus device in the SCSI bus. Otherwise, a terminator block shall be connected between the male blue ribbon connector of the System Cable and the device's input female connector. The last SCSI bus device should have a terminator block plugged to its output connector. For further information on APPLE SCSI terminator block, refer to APPLE TERMINATOR ASSEMBLY, specification 590-0348.

A SCSI device shall provide two female 50 pin blue ribbon connectors. The output connector is used to daisy-chain the next SCSI device if it is not the last device in the bus, or to connect to the terminator if it is the last device in the bus.

A 38 wire, 1.0 meter long PERIPHERAL INTERFACE CABLE, Assembly 590-0346 with 50 pin male blue ribbon connectors at both ends is used to daisy-chain SCSI bus devices. A 38 wire, 1.0 meter long EXTENDER CABLE, Assembly 590-0347, with one male 50 pin blue ribbon connector at one end and one female 50 pin blue ribbon connector at the other end, is used to extend the former cable to more than 1.0 meter.

APPLE SCSI BUS uses single-ended drivers and receivers. The maximum total end-to-end cable length is six meters.

3.2 Cable. All cables shall be shielded round cable with 38 conductors to form 19 twisted pairs within a shield and use a stranded conductor size of 26 AWG to minimize noise effect and ensure proper distribution of terminator power. The cable and connector shall conform APPLE SCSI cable and connector specification 569-0407. The cable shall have a characteristic impedance of 100 +/-10 ohms.

A stub length of no more than 0.1 meters is allowed off the mainline interconnection within any connected equipment.

SCSI bus termination shall be external to the SCSI device that is at the end of the cable. A terminator block, APPLE TERMINATOR ASSEMBLY, specification 590-0348, shall be used for bus termination.

3.3 Connector Requirements. Shielded connector shall be used. The cable and connector combination shall pass FCC class B and APPLE corporate ESD specification 062-0302 .

3.3.1 Shielded Connectors. Alternative 2 of the Shielded SCSI Device Connector specified in ANSI X3T9.2 document rev. 16 is used. The specification of the shielded connector is described in APPLE specification 519-0410 & 519-0411. The connector shielding system shall provide a dc resistance of less than

10 milliohms from the cable shield at its termination point to the SCSI device enclosure.

The cable shield shall be soldered 360 degree to the connector shield. The shield shall not connect to the signal ground at the connector. It shall be tied to device chassis ground.

3.3.2 Pin assignment:

50 Pin Connector			DB25 Connector
Signal	Pin#		Pin#
DBØ-GND	1	connected to	14
DB1-GND	2		14
DB2-GND	3		14
DB3-GND	4		16
DB4-GND	5		16
DB5-GND	6		16
DB6-GND	7		18
DB7-GND	8		18
DBP-GND	9		18
DIFFSENS-GND	11		18
ATN-GND	16		7
BSY-GND	18		7
ACK-GND	19		7
RST-GND	20		9
MSG-GND	21		9
SEL-GND	22		9
C/D-GND	23		24
REQ-GND	24		24
I/O-GND	25		24
-DBØ	26		8
-DB1	27		21
-DB2	28		22
-DB3	29		10
-DB4	30		23
-DB5	31		11
-DB6	32		12
-DB7	33		13
-DBP	34		20
TERMPWR	38		25
-ATN	41		17
-BSY	43		6
-ACK	44		5
-RST	45		4
-MSG	46		2
-SEL	47		19
-C/D	48		15
-REQ	49		1
-I/O	50		3

Pin 11, which is DIFFSENS in a differential cable system, shall be grounded at the APPLE DB25 connector and to the device logical ground.

Pin 13 shall be left open and unconnected inside the device.

Pins 10, 12, 13, 14, 15 and17 of the blue ribbon 50 pin connector shall be left open. No wire is connected to these pins in the cable.

3.4 Electrical Description.

3.4.1 Single-Ended. All assigned signals shall be terminated at each end of the cable. All signals shall use open-collector or three-state drivers.

3.4.1.1 Output Characteristics. Each signal driven by an SCSI device shall have the following output characteristics when measured at the SCSI device's connector:

Signal assertion	= 0.0 volts dc to 0.4 volts dc
Minimum driver output capability	= 48 mA (sinking) at 0.5 volt dc
Signal negation	= 2.5 volts dc to 5.25 volts dc

3.4.1.2 Input Characteristics. Each signal received by an SCSI device shall have the following input characteristics when measured at the SCSI device's connector:

Signal true	= 0.0 volts dc to 0.8 volts dc
Maximum total input load	= -0.4 mA at 0.4 volts dc
Signal false	= 2.0 volts dc to 5.25 volts dc
Minimum input hysteresis	= 0.2 volts dc

3.4.1.3 Input Hysteresis. SCSI bus receivers shall have the following hysteresis characteristics:

Threshold from low to high	= 1.48 volts
Threshold from high to low	= 1.18 volts

3.4.1.4 Input clamp. The bus receiver shall have diode connected to ground to clamp any negative going input signal when the input becomes lower than -0.7 volt. This clamp will reduce ringing on the bus.

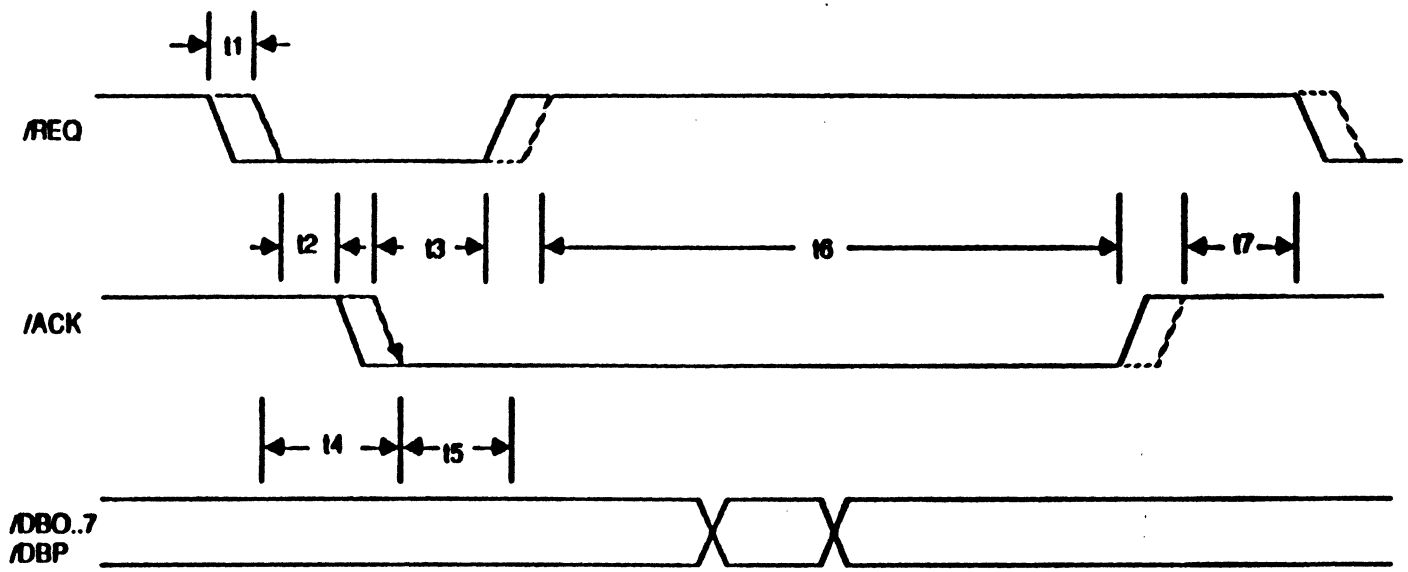
3.4.1.5 Signal transition times. The 90 to 10 % fall time for any high-to-low transition on the APPLE SCSI BUS shall be greater than 20 nanosec.

3.4.2 Terminator Power. All SCSI devices in APPLE SCSI BUS shall provide +5V terminator power (TERMPWR pin 38) through a diode or similar semi-conductor that prevents the backflow of power to the SCSI device. The terminator power shall have the following characteristics:

V term	= 4.0 volts dc to 5.25 volts dc (800 mA minimum source drive capability, 1.0 mA maximum sink capability, with 1.0 amp recommended current limiting.)

4.0 SCSI BUS TIMING

Detailed bus timing tolerances for SCSI READ: INITIATOR RECEIVES & TARGET SENDS are given in Figure 4.1. Tolerances for SCSI WRITE: INITIATOR SENDS & TARGET RECEIVES are given in Figure 4.2.



	min.	typ.	max.	unit:
t1 : Cable propagation delay	0	3		
t2 : /REQ true to /ACK true at the initiator	20	150	160	ns
t3 : /ACK true to /REQ false at the target	25	110	125	ns
t4 : Data sepup time to /ACK true at the target	20			ns
t5 : Data hold time after /ACK true	50			ns
t6 : /REQ false to /ACK false at the initiator	145			ns
t7 : /ACK false to /REQ true at the target	20	140	150	ns

Figure 4.2 SCSI WRITE : INITIATOR SENDS & TARGET RECEIVES

PART 6

SCSI Interface to Hard Disk

NOTE: The documentation of the SCSI interface, at this time, consists of information from *Inside Macintosh, Volume IV* and the interdependent referencing between two sources included in this PART 6:

1) draft proposed American National Standard for information systems- SMALL COMPUTER SYSTEM INTERFACE (SCSI), REV17B, December 16, 1985

2) Apple Engineering Specification 062-2075 Revision 3, May 19,1986

1.0 Overview

The purpose of this document is to specify all the information needed to understand Apple requirements and standards for SCSI device command protocol. The goal is to specify information here regarding Apple standards that should not change and refer to other SCSI information. In this document all SCSI defined data will be referred to with the referenced location specified. Every attempt will be made to avoid specifying duplicate information to that specified in the ANSI SCSI documents to reduce confusion and maintenance. Only clarifications, extensions to and differences from the ANSI SCSI documents will be specified.

1.1 Logical Characteristics

The following section of this SCSI document defines the logical characteristics of the Apple implementation of a SCSI bus and its attached devices. In general the logical characteristics set forth in ANSI X3T9.2/82-2 Rev. 17B apply with the following clarifications, options and additions.

1.1.1 SCSI Bus

An Apple SCSI Bus uses five phases. The SCSI bus can never be in more than one phase at any given time. The phases are:
BUS FREE
ARBITRATION
SELECTION
RESELECTION
Information Transfer

Information transfer can be further defined to be:
COMMAND Phase
DATA Phase
STATUS Phase
MESSAGE Phase

BUS FREE - The BUS FREE phase is used to indicate that no SCSI device is actively using the SCSI bus and that it is available for users. See ANSI X3T9.2/82-2 Rev. 17B SCSI Specification 5.1.1 for accurate detailing.

ARBITRATION - The ARBITRATION phase allows one SCSI device to gain control of the SCSI bus so that it can assume the role of an initiator or target. See ANSI X3T9.2/82-2 Rev.17B SCSI Specification 5.1.2 for accurate detailing.

SELECTION - The SELECTION phase allows an initiator to select a target for the purpose of initiating a target function (Example - READ or WRITE command). The SCSI device that won ARBITRATION becomes an initiator by releasing I/O. See ANSI X3T9.2/82-2 Rev. 17B Specification 5.1.3 for accurate detailing.

RESELECTION - The RESELECTION phase allows a target to reconnect to an initiator for the purpose of continuing a previously started operation that was suspended by the target (Target allowed a BUS FREE phase to occur before the operation was complete.) See ANSI X3T9.2/82-2 Rev.,17B SCSI Specification 5.1.4 for accurate detailing.

Information Transfer - The Information Transfer phases are grouped because they use the DATA bus to transfer data or control information. The COMMAND, STATUS, DATA, and MESSAGE phases are controlled by the C/D, I/O, and MSG signals. Information Transfer phases accomplish the actual data transfer of the SCSI bus.
See ANSI X3T9.2/82-2 Rev.17B SCSI Specification 5.1.5 for detailing.

1.1.2 SCSI Bus Conditions - RESET

As defined in ANSI X3T9.2/82-2 Rev. 17B Section 5.2.2, Initiators will implement the *Soft* RESET Option and Targets will implement the *Hard* RESET Option.

1.1.3 Arbitration, Disconnection/Reselection

The Apple SCSI bus implementation is an arbitrating, multi-initiator, multi-target bus. All Apple SCSI devices that act as initiators will be arbitrating devices and will allow disconnection/reselection. Except in specific cases, it is recommended that all target devices be capable of disconnection/reselection.

1.1.4 Message Implementation

Implementation of messages requires the Command Complete message and Apple strongly recommends the following messages. If any of the following messages are implemented, then all must be implemented.

1. Disconnect
2. Abort
3. Message Reject
4. No Operation
5. Bus Device Reset
6. Identify

These messages are not extended format messages.

2.0 Commands

2.1 Direct Access Commands

The SCSI mandatory commands and the following SCSI optional commands are Apple Mandatory.

The Apple Mandatory Command Set:
•does not substantially deviate from the proposed SCSI standard or preclude the use of additional commands.
•does not limit the performance of the products conforming to the document.

From Here to 2.2 are Apple additions, clarifications and extensions tothe ANSI SCSI Rev. 17B document:

Bold denotes Apple added text to existing SCSI Commands.

REQUIRED. Describes commands, messages, fields, bytes, bits which shall be implemented in order to conform to the Apple requirements.

Table 5-2
Message Codes

Code	Description	Type
BASIC SET		
00	COMMAND COMPLETE	REQUIRED
SYSTEMS SET		
06	ABORT	REQUIRED
07	MESSAGE REJECT	REQUIRED
08	NO OPERATION	REQUIRED
0C	BUS DEVICE RESET	REQUIRED
DISCONNECT SET		
04	DISCONNECT	REQUIRED
80-FF	IDENTIFY	REQUIRED
	It is required that the target accept the Identify message. The initiator may or may not issue this message. The initiator may or may not set bit 6 of the Identify message indicating its ability to accomodate disconnection and reconnection.	

6.1.2 Operation Code Types

Operation Code Type **Description**

REQUIRED: Commands so designated shall be implemented by the target in order to comply to this document.

V Vendor Unique, Operation codes so designated in the standard and *not used* in this document are available for Vendor defined commands.

6.2.6 Control Byte.

Bit 7	Vendor Unique. To be checked by the target.
Bit 6	Vendor Unique. To be checked by the target.
Bit 5	Reserved
Bit 4	Reserved
Bit 3	Reserved
Bit 2	Reserved
Bit 1	Flag. Optional. To be checked by the target.
Bit 0	Link. Optional. To be checked by the target.

14. STATUS

Table 14-0
Status Codes

Status	Type
GOOD	REQUIRED
CHECK CONDITION	REQUIRED
BUSY	REQUIRED
RESERVATION CONFLICT	REQUIRED

COMMAND SET for Direct-Access Devices

APPLE REQUIRED COMMANDS

Operation Code Hex	Command Name
00	TEST UNIT READY
03	REQUEST SENSE
04	FORMAT UNIT
07	REASSIGN BLOCKS
08	READ
0A	WRITE
0E	READ CNTRLER INFORMATION (Tape Only)
0F	WRITE CNTRLER INFORMATION (Tape Only)
12	INQUIRY
13	READ QIC-100 DATA(Tape Only)
14	WRITE QIC-100 DATA (Tape Only)
15	MODE SELECT
16	RESERVE UNIT
17	RELEASE UNIT
1A	MODE SENSE
1B	START/STOP UNIT{LOAD/UNLOAD (Tape Only)}
1D	SEND DIAGNOSTIC
25	READ CAPACITY
28	READ EXTENDED
2A	WRITE EXTENDED
37	READ DEFECT DATA
3B	WRITE BUFFER(5/1/86)
3C	READ BUFFER(5/1/86)

For all the following commands, no changes or comments are applied within this document. Refer to the ANSI document sections 7 and 8.

Command Name	Code
TEST UNIT READY	00
READ	08
WRITE	0A
READ EXTENDED	28
WRITE EXTENDED	2A
WRITE BUFFER	3B
READ BUFFER	3C

7.1.2 REQUEST SENSE Command (03_H)

Extended Sense Data format is Required. Non Extended Sense is optional.

If the Allocation Length of the CDB is different than zero, the target shall return the Extended Sense Format. The eight (8) first bytes of the Extended Format, as defined in the SCSI specifications, are to be supported by the target. All additional bytes are optional.

If the Allocation Length byte 4 of the CDB is set to zero, the target shall return four sense bytes of non Extended Sense data format.

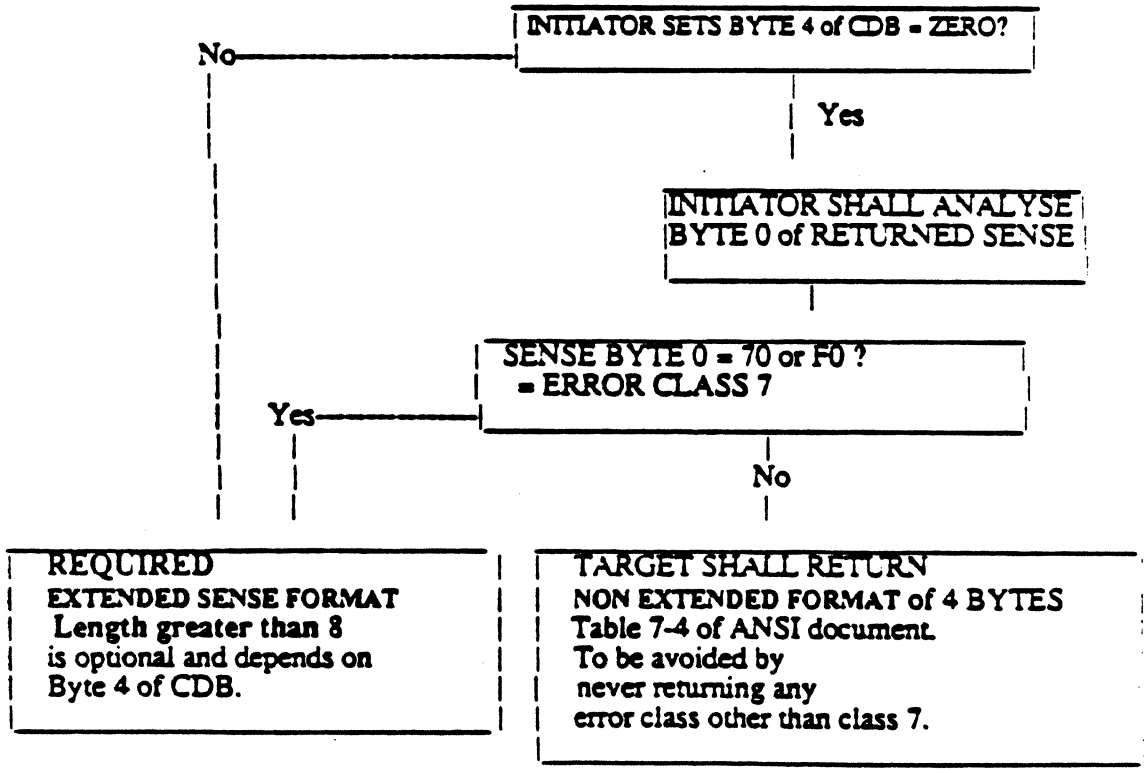
EXTENDED SENSE DATA

The following bytes are REQUIRED

Byte	Bit 7	6	5	4	3	2	1	0
0	Valid	Error Class						Error Code
1	Segment Number							
2	FileMark	EOM	ILI	R	Sense Key			
3	Information Byte (MSB)							
4	Information Byte							
5	Information Byte							
6	Information Byte(LSB)							
7	Additional Sense Length (n)							

Non-extended format may be implemented *additionally* at the option of the target as defined below.

If the Allocation Length byte 4 of the CDB is set to zero, the target shall return four sense bytes of Non-Extended Sense data format. The Initiator shall analyze the first Sense byte to determine which Sense Format, either Extended (class 7) or Non-Extended (classes 0-6) has been returned by the target. It is recommended that Non-Extended Sense Format be not implemented by the target.



EXTENDED SENSE DATA

The following bytes are optional and follow the Required Extended Sense Data byte 7.

Bit	7	6	5	4	3	2	1	0
Byte								
8 through 11	Optional, except for use with SEARCH and COPY commands as per 7.1.4.2							
12	Additional Sense Code							
13	Reserved							
14	FRU failed							
15	FPV	C/D		VU		VU	BPV	Bit Pointer
16	Field Pointer (MSB)							
17	" " (LSB)							
18-n+17	N/A							

Byte 12 Additional Sense code.
The additional Senses may be applied with the same code by the target to Extended and Non-Extended Sense Formats. The range of the Non-Extended Sense format is from 00 to $6F_H$ (Class 0 to 6), therefore all codes are within these limits.
The Additional Sense code 00_H indicates that the target does not support any additional sense code for the related Sense Key or does not have any appropriate additional sense to return for the Check Condition status that it created.

DIRECT ACCESS DEVICES ADDITIONAL SENSE CODES (byte 12)

Code		Related Sense Keys
00	No Additional Sense Information	No Sense
01	No Index/Sector signal	Hardware error
02	No Seek Complete	Hardware error
03	Write Fault	Hardware error
04	Drive Not Ready	Not Ready
05	Drive Not Selected	Not Ready
06	No Track Zero found	Hardware error
07	Multiple Drives Selected	Hardware error
08	Logical Unit Communication Failure	Hardware error
09	Track Following error	Hardware error
0A through 0F	Reserved	
10	ID CRC or ECC error	Hardware error or Medium error
11	Unrecovered Read error of data blocks	Medium error
12	No Address Mark found in ID field	Medium error
13	No Address Mark found in Data field	Medium error
14	No record found	Medium error
15	Seek Positioning error	Hardware error or Medium error
16	Data Synchronizing Mark error	Medium error or Recovered error
17	Recovered Read data with target's Read retries(not with ECC)	Recovered error
18	Recovered Read data with target's ECC correction(not with retries)	Recovered error
19	Defect List error	Medium error or Recovered error
1A	Parameter Overrun	Illegal Request
1B	Synchronous Transfer error	Hardware error
1C	Primary Defect List not found	Medium error or Illegal Request
1D	Compare error	Miscompare
1E	Recovered ID with target's ECC correction	Medium error or Recovered error
1F	Reserved	
20	Invalid Command Operation Code	Illegal Request
21	Illegal Logical Block Address, Address greater than the LBA returned by the READ CAPACITY data with PMI not set	Illegal Request
22	Illegal function for device type	Illegal Request
23	Reserved	
24	Illegal field in CDB	Illegal Request
25	Invalid LUN	Illegal Request
26	Invalid field in Parameter List	Illegal Request
27	Write Protected	Hardware error
28	Medium Changed	Unit Attention
29	Power On or Reset or Bus Device Reset occured	Unit Attention
2A	Mode Select Parameters changed	Unit Attention
2B through 2F	Reserved	

30	Incompatible Cartridge	Medium error
31	Medium Format corrupted	Medium error
32	No Defect Spare Location Available	Medium error
33 through 3F Reserved		
40	RAM failure	Hardware error
41	Data Path Diagnostic Failure	Hardware error
42	Power On Diagnostic Failure	Hardware error
43	Message Reject Error (see 5.6.1.5)	
44	Internal Controller Error (see 5.6.1.8)	Hardware error
45	Select/Reselect failed (see 5.6.1.7.)	Hardware error
46	Unsuccessful Soft Reset	
47	SCSI Interface Parity Error (see 5.6.1.)	Hardware error
48	Initiator Detected Error (see 5.6.1.4)	
49	Inappropriate/Illegal Message	
4A through 4F Reserved		
50 through 5F Reserved		
60 through 6F Reserved		
70 through 7F Reserved		
80 through 9F Vendor Unique		
A0	Backgound Noise Error	Hardware Error
A1 through A6 Vendor Unique		
A7	Logical Load Error	Hardware Error
A8	Cartridge is Currently Autoloading	Hardware Status
A9 through AF Vendor Unique		
B0	No Cartridge in Drive	Hardware Status
B1 through FF Vendor Unique		

Byte 14 Field Replaceable Unit (FRU) failed. A non zero value indicates failure. A value of zero means that no FRU is to be reported.

Byte 15 definition:
-FPV (Field Pointer Value) Bit 7 of zero indicates that the target does not implement the functions supported by C/D & BPV bits and bytes 16 and 17, therefore these bits and fields are not valid. Bit FPV of one indicates that the Field Pointer bytes 16 and 17, the C/D and BPv bits are significant.
-C/D bit of one indicates that the value reported in the Field Pointer is the CDB's byte number for which an ILLEGAL REQUEST Sense Key was issued. C/D bit of zero indicates that the value reported in the Field Pointer is the byte number of the DATA phase for which an ILLEGAL REQUEST Sense Key was issued.
-Bits 5 and 4 are vendor unique.
-BPV bit of zero indicates that the target does not implement this function, therefore the Bit Pointer field is not valid. BPV bit of one indicates that the Bit Pointer field (bits 0 through 2) is significant.
-Bits 0 through 2, Bit Pointer, indicates which bit of the byte number reported in bytes 16 and 17 is the bit for which the ILLEGAL REQUEST Sense Key was issued.

7.1.3 INQUIRY Command (12_H)

Bytes 0 through 48 of the Inquiry data are Required.
(Parameters not used by Tape are noted by Δ)

INQUIRY DATA

Bit	7	6	5	4	3	2	1	0
BYTE 0	Peripheral Device Type							
BYTE 1	RMB	Device Type Qualifier						
BYTE 2	Version							
BYTE 3	Reserved						Response Data Format	

Response Data Format:

Code	Description
0_H	Vendor Unique
1_H	Common Command Set (CCS)
2_H through F_H	Reserved

Targets conforming to at least conformance level 2 as defined in Table E1, Appendix E, of the standard, and conforming to this document shall set the Common Command Set code (1_H) in the Response Data Format field.

BYTE 4	Additional Length (n)
BYTE 5	Vendor Unique
BYTE 6 and 7	Reserved
BYTE 8 through BYTE 15	Vendor Identification (in ASCII)
BYTE 16 through BYTE 31	Product Identification (in ASCII)
BYTE 32 through BYTE 35	Revision Level (in ASCII)

Beginning at byte 36 in the VENDOR UNIQUE area of the response are extension bytes to specify the number of extents supported by the RESERVE (command $16) and RELEASE (command $17) commands. Following this is a list of SCSI commands supported by this device. Commands map into this list by their group code and command code values. Values are returned by first specifying a Group Code Specifier (a byte for the Group Code value: 0 for Goup 0, 1 for Group 1, etc), then specifying a 4 byte Command Bit Map representing the commands implemented within that group. The bit map is constructed by setting a bit for an implemented command according to that command's value, and clearing a bit otherwise. Bits within the bit map are numbered in ascending order beginning with the first bit following the Group Code Specifier. This list is terminated by specifing a $FF for the Group Code (no additional command bit map bytes are necessary).

Example: A device that implements the mandatory commands specified by this document would have the form:

Byte 36:$00	[Hi Order byte - number of Extents]
Byte 37:$08	[Low Order byte -number of Extents]
Byte 38:$00	[Group 0 commands]
Byte 39:$99	[Commands 0,3,4,7]
Byte 40:$A0	[Commands 8,10]
Byte 41:$27	[Commands 18,21,22,23]
Byte 42:$24	[Commands 26,29]
Byte 43:$01	[Group 01 commands]
Byte 44:$04	[Command 5]
Byte 45:$A0	[Commands 8,10
Byte 46:$01	[Command 23]
Byte 47:$00	[No commands implemented in this range]
Byte 48:$FF	[End of list]

7.1.6 SEND DIAGNOSTIC Command ($1D_H$)

SelfTest bit 2 byte 1 is the only Required function.

8.1.2 FORMAT UNIT Command (04_H)

Non-bold text is the regular text of the ANSI document.

Peripheral Device Type: Direct Access
Operation Code Type: Required
Operation Code: 04_H

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code							
1	LUN				FmtData	CmpLst	Defect List Format	
2	Vendor Unique							
3	Interleave (MSB)							
4	Interleave (LSB)							
5	VU	VU	Reserved				Flag	Link

The FORMAT UNIT command (Table 8-3) ensures that the medium is formatted so that all of the initiator addressable data blocks can be accessed. There is no guarantee that the medium has or has not been altered. In addition, the medium may be certified and control structures be created for the management of the medium and defects.

The FORMAT UNIT command shall be rejected with RESERVATION CONFLICT status if any extent (see 8.1.8.2) in the specified logical unit is reserved.

It is recommended that the MODE SELECT Parameters (if any) are set properly prior to issuing the FORMAT UNIT command.

The FORMAT UNIT command is both a Required and an Extended command. Bits 0 through 4, byte 1 of the CDB, include three Required and multiple optional implementations of the command.

During the execution of the FORMAT UNIT command, the target may perform a medium flaw management scheme which can be selected by the initiator. Four schemes of flaws P, C, D and G are defined as follows:

P = PRIMARY DEFECT LIST : This list refers to the list of defects supplied by the original manufacturer of the device considered as permanent flaws. It is recommended that the device manufacturer record the P list on a specific location on the device and that writing access be prevented by the initiators to this location. During the FORMAT UNIT command the target intelligence shall have access to this list in order to remove the P list flaws from the initiator addressable data blocks. This list shall not be subject to additions.

C = TARGET CERTIFICATION : Includes defects detected by the target during an optional verify process executed during the FORMAT UNIT command. The C scheme includes flaw areas to be removed from the initiator addressable data blocks. The target certification flaws may or may not be saved or recorded as a list by the target.

D = DATA DEFECT LIST : This list is supplied to the target by the initiator in the Data Out phase of the FORMAT UNIT command as shown in tables 8-5, 8-6, and 8-7. The defect list length (Byte 2 and 3) of the Defect List Header may be null. The Data Defect list may or may not be saved or recorded by the target.

G = GROWN DEFECT LIST : This list includes defects identified to or by the target. This list does not include the Primary list of defects. The defects classified as grown are medium flaws identified by or to the target other than the PRIMARY list of defects. Entries to this Grown list may include (at the option of the target) :

- Defects provided to the target in Data Defect lists (D list) during previous FORMAT UNIT commands.

- The target certification defects (C list) detected during the previous FORMAT UNIT commands or vendor unique utilities.

- Defects appended by the result of successful completion of the REASSIGN BLOCKS commands.

- Defects identified by the target and automatically handled by the target. The defective blocks classified in this grown list are automatically reassigned to an area on the logical unit reserved for this purpose. The implementation of this automatic handling of defects is target specific.

A format data (FmtData) bit of one indicates that a DATA OUT PHASE takes place during the command execution. The defect list included with this data(if Defect List Length is different than zero) specifies the defect list that shall be entered into the defect map. The flaw areas of this map shall be removed by the target from the initiator addressable blocks. The format of the defect list is determined by the Defect List Format defined by bits 0 through 2. A FmtData bit of zero indicates that the DATA OUT phase shall not occur (no defect list header and no defect data shall be supplied by the initiator).

A complete list (CmpLst) bit of one indicates that the data supplied by the initiator during the DATA OUT phase of the command execution is the complete list of known defects. Any previous initiator-specified defect map or defect data shall be erased by the target. The result is to purge any previous initiator-specified defect list and to build a new defect list. Any previous C, D or G lists (if any) shall be erased or removed by the target.

The target may add to this complete list as it formats the medium, when performing a target certification process (or a new C list).A CmpLst bit of zero indicates that the data supplied by the initiator during the DATA OUT phase is in addition to existing defect data already removed from initiator addressable blocks and using the current format.

When using the block format, the defect list refers to the current block length (and not to the new block length, if it is different) and the defect list refers to current logical block addresses (not physical addresses).

The defect list format field (bits 0 through 2 of byte 1) specifies additional information related to the defect list. (See Table 8-4 for further information.)

The interleave field requests that the logical blocks be related in a specific fashion to the physical blocks to facilitate speed matching between the host bus data transfer rate and the block data transfer rate from the device. An interleave value of zero requests that the target use its default interleave. An interleave value of one requests that consecutive logical blocks be placed in consecutive physical order. Values of two or greater are vendor unique.

Table 8-4

Bit Reference 4 3 2 1 0	List Type	Flaw Length	Defect Management with (1) or without (0) P	C	G	D	Comments
0 x x x x	REQUIRED	N/A	0	0	0	0	No Data Out phase(no defect list
			0	0	1	0	header, no defect descriptors).
			0	1	0	0	The target optionally defines
			0	1	1	0	what combination of P,C,G to
			1	0	0	0	use if flaw management is
			1	0	1	0	performed.
			1	1	0	0	
			1	1	1	0	
1 0 0 x x	REQUIRED	Zero	0	0	1	0	Reformat using G list
			0	1	1	0	Defect List Length of zero
			1	0	1	0	
			1	1	1	0	
1 1 0 x x	REQUIRED	Zero	0	0	0	0	With CmpLst bit set to one.
			0	1	0	0	Target erases and/or removes
			1	0	0	0	current G list.
			1	1	0	0	Defect List Length of zero.

P,C,G, and D refer to the various lists of defects

Implementation of the Required variations :
The following refers to the configuration of the bits 4 through 0 in the table 8-4.

0 x x x x REQUIRED :
With this variation, the initiator requests to have no control on how the format process is executed by the target. This is the case when the initiator is confident in the target's intelligence to perform the format accordingly.
The target determines if flaw management shall be performed or not during the format process of this variation. If flaw management is performed, the target shall define what combination of P,C,G defects scheme be performed. The target may remove or erase previous lists of flaws, except the P list. No DATA OUT phase shall take place with this variation (no Defect list Header and no D list).

In the following two variations, bit 2 is set to zero to preserve the bit combinations of the vendor unique and the reserved variations(1x110 and 1x111). Otherwise with Defect List length set to zero, bit 2 has no other meaning with these two variations for which no defect descriptors are involved.

1 0 0 x x REQUIRED :
The target shall perform the format process with flaw management. This variation allows the initiator to request the target to use the G list of medium grown defects as defects to be removed from the initiator addressable blocks. This variation is available for a reformat process ensuring that all previously detected flaws be managed. DATA OUT phase with the Defect List Header shall take place during this variation, with the Defect List length of zero.
The target shall determine whether or not to implement the certification process (C scheme).

1 1 0 x x REQUIRED :
The target shall perform the format process with flaw management. This variation allows the initiator not to consider the G list of medium grown defects but return to the "as shipped" condition from the original manufacturer of the device. This assumes that the list of defects had grown during the lifetime of the medium either with a C, D, or G lists as defined below. DATA OUT phase with the Defect List Header shall take place during this variation, with the Defect List length of zero. The target shall determine whether or not to implement the certification process (C scheme).

Notes
- X bits are not analysed by the target. *x* value may be 1 or 0, but recommended to be set to zero by the initiator.

-With all the above variations, at completion of the FORMAT UNIT command, some initiator addressable blocks may include flaws. The target may require a Vendor Unique certification utility to identify defects as an alternative source to remove known flaws from initiator addressable blocks. It is recommended that this utility, in form of either a vendor unique command, or use of the REASSIGN BLOCKS command or a vendor unique process be implemented immediately upon completion of the FORMAT UNIT command.

8.1.7 MODE SELECT Command (15_H)

(Parameters not used by Tape are noted by Δ)

The Mode Select command (and Mode Sense) are mandatory commands. Within the Mode Select command it is possible to have functions that are not applicable to a specific device (i.e., page code 5: flexible disk drive parameters are not applicable to a hard disk drive); the intent of this command is for each device to implement those functions that make sense for that specific device, although there are several functions that are mandatory.

Mandatory Page Codes for Mode Select and Mode Sense

1. Page Code:$0: Unit Attention
1. Page Code $1: Error Recovery Parameters
2. Page Code $2: Disconnect/Reconnect Control Parameters
3. Page Code $3: Direct Access Device Format Parameters
4. Page Code $4: Rigid Disk Drive Geometry Parameters
5. Page Code $6: Certification Pattern
6. Page Code $20: Serial Number
7. Page Code $3F: Report Values (Mode Sense only)

Table 8-13
Mode Select Command

Bit / Byte	7	6	5	4	3	2	1	0
0				Operation				
1		LUN			Reserved			SP
2				Reserved				
3				Reserved\				
4				Parameter List Length				
5	VU	VU		Reserve			Flag	Link

The MODE SELECT command (Table 8-13) provides a means for the initiator to specify or change medium, logical unit, target or peripheral device parameters to the target. Absolutely necessary to some targets, this command is Required within the Apple Common Command Set.

SP (Save Mode Parameters) bit 0 byte 1 set to *one* indicates that the target shall update the Current mode values with the values defined in the following Pages; shall save all Saveable Pages except the Pages defined by the Page Codes 3, 4 and 5. Then the target shall report command complete with no Check Condition status when successfully completing the above. Saveable Pages are Pages for which preceding MODE SENSE commands returned the PS bit (bit 7 byte 0) of the Page Header set to one.

SP (Save Mode Parameters) bit 0 byte 1 set to *zero* indicates that the target shall update the Current mode values with the values defined in the following Pages; shall not save the Saveable Pages; shall not modify the saved parameters of the Pages defined by the Page Codes 3, 4 and 5. Then the target shall report command complete with no Check Condition status when successfully completing the above.

The parameter list length specifies the length in bytes of the MODE SELECT parameter list that shall be transferred during the DATA OUT phase. A parameter list length of zero indicates that no

data shall be transferred. This condition shall not be considered an error.

The MODE SELECT parameter list (TABLE 8-14) contains a four-byte header, followed by zero or more block descriptors, followed by zero or more Pages.

Table 8-14
Mode Select Parameter List
MODE SELECT Header

Bit / Byte	7	6	5	4	3	2	1	0
0	Reserved							
1	Medium Type							
2	Reserved							
3	Block Descriptor Length							

Block Descriptor(s)

Bit / Byte	7	6	5	4	3	2	1	0
0	Density Code							
1	Number of Blocks (MSB)							
2	Number of Blocks							
3	Number of Blocks (LSB)							
4	Reserved							
5	Block Length (MSB)							
6	Block Length							
7	Block Length (LSB)							

Page Descriptor(s)

Bit / Byte	7	6	5	4	3	2	1	0
0	R	R	Page Code					
1	Page Length (in bytes)							
2 to n	Refer to each page							

Optional additional blocks of parameters called *Pages* may be sent to the target in the Data Out phase of the MODE SELECT command, following either:
- the MODE SELECT Header, if the Block Descriptor length is set to zero.
- or all Block Descriptors, if the Block Descriptor length is different from zero.
The Block Descriptor Length shall not include the length of the Pages.

Block lengths of 512 and 532 bytes in the Block Descriptor must be supported for Disk products.

Each defined Page is preceded by a Header of two bytes defining the Page Code and the length of the page. Following the Header the Pages are separated into sub-blocks containing a list of related flags and/or values.

Bits 7 and 6 of byte 0 are reserved.

The Page Code identifies the meaning of the following bytes in the Page. The Page Code is either defined, reserved or vendor unique. The parameters in the defined Pages are classified in priority sequence to ease implementation by the target.

The Page Length value of each defined page, shall not include the Page Length byte. The Page Length represents the number of bytes that the target supports in each Page. The target may return in the Pages of the MODE SENSE commands as many consecutive bytes that it supports, for each Page that it supports, without splitting fields of multiple bytes. The Page Length shall be set in the pages of the MODE SELECT commands to the exact same value (zero value included) returned by the target in the MODE SENSE Page Length bytes. Otherwise, the target shall create Check Condition status with the Sense Key of ILLEGAL REQUEST. The initiator shall issue a MODE SENSE command requesting the target to return all Changeable values (see PCF field configuration 0 1 in byte 2 of the MODE SENSE CDB) prior to issuing any MODE SELECT commands, in order to find out which Pages are implemented by the target and the length of each Page for that particular LUN(Logical Unit Number).

Initiator Implementor Notes:
- Those Pages, supported by the target, in which the initiator requests parameters to be changed shall be sent to the target.
- The initiator may send in MODE SELECT commands all Pages supported by the target.
- The Pages are not required to be sent in ascending order.
- Intelligent targets, versus targets supporting multiple LUNs, may authorize limited number of parameters to be changed. Those parameters have been classified as the first sub blocks in the Pages.

In the event of a *Hard Reset*, the target shall first attempt to restore the Saved Parameters. If Saved Parameters are not available, the target shall restore to Default Parameters.

Page Code	Meaning
0_H	Unit Attention
1_H	Error Recovery parameters
2_H	Disconnect/Reconnect Control parameters
3_H	Direct Access Device Format parameters
4_H	Rigid Disk Drive Geometry parameters
5_H	Flexible Disk Drive parameters
6_H	Certification Pattern
7_H through $1F_H$	Reserved
20_H	Serial Number
21_H	Format Limits(tape only)
22_H through 39_H	Vendor Unique Page formats
$3A_H$ through $3B_H$	Reserved
$3C_H$ through $3E_H$	Vendor Unique
$3F_H$	Defined in MODE SENSE only.

It is recommended that the initiator issue the RESERVE UNIT command prior to executing the MODE SELECT command, then issue the RELEASE UNIT command after completion of the FORMAT UNIT command. This procedure will prevent any other initiator from issuing different MODE SELECT parameters to the unit prior to execution of the FORMAT UNIT command. The initiator may request that the parameters of Pages 1 and 2 be changed at any time.

The target may or may not save the block descriptors and Pages for each LUN and for each initiator. If the target supports 8 LUNs and the bus configuration includes 7 hosts, the target would have to save 56 sets of MODE SELECT/ MODE SENSE data. The data for each LUN for each host could be different.

A target shall create the Check Condition Status with Sense Key of UNIT ATTENTION to the first command received from other initiators, when the target has changed Mode Select parameters for that LUN. The change may be due to a MODE SELECT command issued from a different or from the same initiator. Initiators are recommended to save MODE SELCT parameters for each LUN. Targets are recommended to record on disk those MODE SELECT parameters that are necessary to be issued prior to the FORMAT UNIT command. The recording on the LUN disk may or may not include Pages 3 and 4 or 5, depending on the drive type. Parameters of Pages 1 and 2 that the target implements may or may not be recorded on the device, may or may not be saved by the target, for each LUN, and for all initiators.

UNIT ATTENTION PARAMETERS. Page code 0_H.

Bit / Byte	7	6	5	4	3	2	1	0
0	R	R	Page Code=0_H					
1	Page Length (in bytes)							
2	V.U.	V.U.	V.U.	UnitAtn	Rsvd.	Rsvd	Rsvd	Rsvd
3	Reserved							

When bit 4 of byte 2 is SET (1), then Unit Attention is logged in sense only; no Check Condition Status will be presented following any *reset*. When this bit is RESET (0), then Check Condition is presented for all affected Initiators following a *reset* until Request Sense is issued by each Initiator (as per current operation).

Page Zero is stored on the drive and is not changed by power off/on cycles or Mode Select commands that do not access page zero. The default state of UnitAttn is Reset.

ERROR RECOVERY PARAMETERS. Page code 1_H.

Bit / Byte	7	6	5	4	3	2	1	0
0	R	R	Page Code=1_H					
1	Page Length (in bytes)							
2	AWRE	ARRE	TB	RC Δ	EEC Δ	PER	DTE Δ	DCR Δ
3	Retry Count							
4	Correction Span(Opt.)							
5	Head Offset Count (Opt.)							
6	Data Strobe Offset Count (Opt.)							
7	Recovery Time Limit (Opt.)							

A DCR (Disable Correction) bit 0 set to one indicates that the data shall be transferred without applying correction. A DCR bit set to zero enables error correction.

A DTE (Disable Transfer on Error) bit 1 set to one and if the PER bit is set to one, indicates that the target shall create the Check Condition status and terminate the data transfer to the initiator immediately upon detection of an error. The Transfer Length is then not exhausted. The data of the block in error, which is the first erring block encountered, may or may not be transferred to the initiator depending upon the setting of the TB bit. The DTE bit can only be set to one by the initiator if the PER bit is set to one. The target shall create the Check Condition status with Illegal Request Sense Key, if it receives PER bit of zero and DTE bit set to one.

A DTE bit set to zero enables data transfer for any data which can be recovered within the limits of the Error Recovery Flags. Any erring block that would be posted, which is the last recovered block encountered, is not posted until the Transfer Length is exhausted.

A PER (Post Error) bit 2 set to one indicates that the target shall enable the reporting of the Check Condition status for recovered errors, with the appropriate Sense Key. The Check Condition shall happen during the data transfer depending either on the DTE bit value or if an unrecoverable error occured. If multiple errors occur, the REQUEST SENSE data shall report the block address of either the last block on which recovered error occured or of the first unrecoverable error.

A **PER** bit set to zero indicates that the target shall not create the Check Condition status for errors recovered within the limits established by the other Error Recovery Flags. Recovery procedures exceeding the limits established by the other Error Recovery Flags shall be posted accordingly by the target. The transfer of data may terminate prior to exhausting the Transfer Length depending on the error and the state of the other Error Recovery Flags.

An **EEC (Enable Early Correction)** bit 3 set to one indicates that the target shall enable the use of the most expedient form of error recovery, such as error correction, before applying retries. Seek or positioning retries and the recovery procedure retries of the message system are not affected by the value of this bit. Targets implementing error correction schemes that do not provide the most expedient form of error recovery should default to zero and report the EEC bit as not changeable in the MODE SENSE Page code 3. EEC and DCR both of one is an invalid request, for which the target shall create the Check Condition status with Illegal Request Sense Key.
An **EEC** bit set to zero, indicates that the target shall exhaust the defined retry limit prior to enabling error correction. If DCR bit is set to one, the defined retry limit only is to be performed.

A **RC (Read Continuous)**bit 4 set to one requests the target to transfer the entire requested length of data without adding delays that would increase or ensure data integrity (ie. delays caused by the target's error recovery schemes). This implies that the target may send data which may be erroneous or fabricated in order to maintain a coutinuous flow of data and avoid delays.
The target shall assign priority to this bit over conflicting error control bits (EEC, DCR, DTE, PER) within this byte.
Implementors note: Fabricated data may be data already in the buffer or any other target scheme. This bit is typically to be used in Image Processing, Audio or Video applications.

A **RC** bit set to zero, indicates that error recovery operations which cause reasonable delays are acceptable during the data transfer. Data shall not be fabricated.

A **TB(Transfer Block)** bit 5 set to one indicates that the failing data block (recovered or unrecoverable) data shall be transferred to the initiator. A **TB** bit set to zero indicates that the failing data block (recovered or unrecoverable) data shall not be transferred to the initiator.
Implementor Note: In both cases, but particularly when TB is zero, the block address reported in the REQUEST SENSE data shall be of the erring block, not of the preceding block.

An **ARRE (Automatic Read Reallocation of defective data blocks Enabled)** bit 6 of one indicates that the target shall enable automatic reallocation of defective data blocks during READ operations. The execution of the automatic reallocation is similar to the function of the REASSIGN BLOCKS command, but is initiated at the discretion of the target. The implementation is device specific.

An **ARRE** bit set to zero indicates that the target shall not perform automatic reallocation of defective data blocks during READ operations, but instead shall create the Check Condition Status with Sense Key of Medium Error upon encountering such defective data blocks.

An **AWRE (Automatic Write Reallocation of defective data blocks Enabled)** bit 7 set to one indicates that the target shall enable automatic reallocation of defective data blocks during WRITE operations. The execution of the automatic reallocation is similar to the function of the REASSIGN BLOCKS command, but is initiated at the discretion of the target. The implementation is device specific.

An **AWRE** bit set to zero indicates that the target shall not perform automatic reallocation of defective data blocks during WRITE operations, but instead shall create the Check Condition Status with Sense Key of Medium Error upon encountering such defective data blocks.

The following table summarizes all valid modes of operation.

EEC	PER	DTE	DCR	Description
0	0	0	0	Retries then Correction are attempted (EC & DCR off). Recovered and/or corrected data (if any) is transferred with no Check Condition Status (PER off) at the end of the transfer. - Transfer Length is exhausted. Data transfer stops only if an unrecoverable error is encountered. The target shall then create Check Condition status with the appropriate Sense Key. - The data of the unrecoverable Block (if any), may or may not be transferred to the initiator depending on the setting of the TB bit.
0	0	0	1	Same as (0000) above but No Correction Applied(EEC off,DCR on)
0	0	1	0	Invalid Request (DTE on, PER off)
0	0	1	1	Invalid Request (DTE on, PER off)

EEC	PER	DTE	DCR	Description
0	1	0	0	Report Last Data Block in error at the end of transfer. Retries then Correction (EEC off, DCR off) are attempted and recovered data (if any) is transferred corrected. - The Transfer Length is exhausted if no unrecoverable error occured (DTE off). - The target creates Check Condition status with RECOVERED ERROR Sense Key and reports (in the information bytes field of the Extended Sense data) the last block for which recovered error occured, if any. (PER on). - The data of the unrecoverable Block (if any), may or may not be transferred to the initiator depending on the setting of the TB bit.
0	1	0	1	Same as (0 1 0 0) above but No Correction Applied (EEC off, DCR on).
0	1	1	0	Stop Transfer on First Recovered Error Encountered. Retries then Correction (EEC off, DCR off) are attempted and recovered data (if any) is transferred corrected, but transfer stops (DTE on) after the first recovered or unrecoverable error is detected. - The target creates Check Condition status (PER on) with RECOVERED ERROR Sense Key on the first block for which a recovered error occured, if any. Implementor Note: This mode is not recommended for use if TB is set to zero. It is suggested that mode 0111 be used instead if TB is set to zero.
0	1	1	1	Same as (0 1 1 0) above but no Correction Applied (EEC off, DCR on). The data of the erring Block (if any), may or may not be transferred to the initiator depending on the setting of the TB bit.

1	0	0	0	Correction then Limited Retries (DCR off, EEC on). Same as (0 0 0 0) except apply ECC Correction first.
1	0	0	1	Invalid Request (EEC on, DCR on).
1	0	1	0	Invalid Request (DTE on, PER on).
1	0	1	1	Invalid Request (DTE on, PER off).
1	1	0	0	Report Last Data Block in error at the end of transfer. Same as (0 1 0 0) except apply ECC Correction first.
1	1	0	1	Invalid Request (EEC on, DCR on).
1	1	1	0	Stop Transfer on First Recovered Error Encountered. Same as 0110 except Correction then Limited retries are attempted.
1	1	1	1	Invalid Request (EEC on, DCR on).

Retry Count is the number of times that the target should attempt its read recovery algorithm. Typically, this is performed before applying correction. If both Retry Count and Recovery Time Limit are specified in a MODE SELECT command, the field which specifies the shorter time period of recovery actions shall dominate. In this case, the non dominant field shall be returned as zero in subsequent MODE SENSE commands requested with current values. If the target does not support this field, it shall return a zero value in the MODE SENSE command.

Correction Span is the size of the largest read data error, in bits, on which correction may be attempted. If the target does not support this field, it shall return a zero value in the MODE SENSE command.

Head Offset Count is a two's complement value that specifies some incremental offset position from the center of the track that indicates where shall the disk heads move. The effect of this field to WRITE operations is unspecified. The value shall be applied and be maintained until another MODE SELECT command is successfully completed with a different value. If the target does not support this field, it shall return a zero value in the MODE SENSE command.
- A value of zero indicates that no offset is to be applied.
- A positive value (i.e. 1, 2, ...) indicates an increasing distance in the direction of the next (+1) physical track. This next physical track could be towards the innermost track or towards the outermost track, depending upon whether track zero was on the outermost or the innermost track of the drive.
- A two's complemented (i.e., FF, FE, ...) value indicates an increasing distance in the opposite direction from a positive value. This is in the direction of the previous (-1) physical track.
The degree of offset for each incremental value and the number of valid steps are device specific. It is recommended that devices support equal incremental positive and negative values. The target shall create the Check Condition Status with Illegal Request Sense Key if it receives an invalid (larger or smaller) offset value than that supported by the device. In this case, the Information bytes of the Extended Sense shall return the positive value of the maximum count that the device supports.

Data Strobe Offset Count is a two's complement value that specifies an incremental position the recovered data strobe shall be adjusted from nominal. This field applies to READ operations only. The value shall be applied and be maintained until another MODE SELECT command is successfully completed with a different value. If the target does not support this field, it shall return a zero value in the MODE SENSE command.
- A value of zero indicates the nominal position.
- A positive value (i.e. 1, 2, ...) indicates an increasing adjustment in the positive direction as defined by the device (such as moving the data strobe out in time by some number of nanoseconds).
- A two's complemented (i.e., Ff, FE, ...) value indicates an increasing adjustment in the negative direction.

The degree of adjustment for each incremental value and the number of valid steps are device specific. It is recommended that devices support equal incremental positive and negative values. The target shall create the Check Condition Status with Illegal Request Sense Key if it receives an invalid (larger or smaller) strobe offset count value than that supported by the device. In this case, the Information bytes of the Extended Sense may return the positive value of the maximum valid count that the device supports. The target shall return a zero value in the Information bytes if it does not have the capability to return a defined value.

Recovery Time Limit is the maximum time that the target shall attempt error recovery actions to correctly recover data, if such recovery is allowed in other fields of this page. The field is defined in 10 milliseconds increments. The target may round the value to its nearest convenient value. Subsequest MODE SENSE commands requested with current values shall return the rounded value. A zero value indicates that the time is unlimited. If both Retry Count and Recovery Time Limit are specified in a MODE SELECT command, the field that specifies the shorter time period of recovery actions shall dominate. In this case, the nondominant field shall be returned as zero in subsequent MODE SENSE commands requested with current values.

DISCONNECT/RECONNECT CONTROL PARAMETERS. Page code 2_H

(Parameters not used by Tape are noted by Δ)

Bit / Byte	7	6	5	4	3	2	1	0
0	R	R	Page Code = 2_H					
1	Page Length (in bytes)							
2	Buffer Full RatioΔ							
3	Buffer Empty RatioΔ							
4	Bus Inactivity Limit (MSB)							
5	Bus Inactivity Limit (LSB)							
6	Disconnect Time Limit (MSB)							
7	Disconnect Time Limit (LSB)							
8	Connect Time Limit (MSB)							
9	Connect Time Limit (LSB)							
10	Reserved							
11	Reserved							

Each ratio parameter is the numerator of a fractional multiplier that has 256 as its denominator.

Buffer Full Ratio indicates to the target, on READ commands, how full the buffer shall be prior to reconnecting. Targets that include a larger granular buffer block size shall round down to the nearest whole buffer block. **(Field not used for Tape) (0 equals Not Implemented)**

Buffer Empty Ratio indicates to the target, on WRITE commands, how empty the buffer shall be prior to reconnecting to fetch more data. Targets that include a larger granular buffer block size shall round up to the nearest whole buffer block. **(Field not used for Tape) (0 equals Not Implemented)**

Bus Inactivity Limit field (bytes 4 and 5) indicates the maximum time in 100 microseconds increments that the target is allowed to maintain the bus busy without handshakes until it shall disconnect. The target may round to its nearest capable value. A setting value of zero indicates that the target is allowed to maintain the bus busy indefinitely without handshakes until it determines to disconnect.

Disconnect Time Limit field (bytes 6 and 7) indicates the minimum time in 100 microseconds increments that the target should remain disconnected until it attempts to reconnect. The target may round to its nearest capable value. A setting value of zero indicates that the target is allowed to reconnect immediately.

Connect Time Limit field (bytes 8 and 9) indicates the maximum time in 100 microseconds increments that the target should remain connected until it attempts to disconnect. The target may round to its nearest capable value. A setting value of zero indicates that the target is allowed to remain connected indefinitely until it determines to attempt disconnection.

DIRECT ACCESS DEVICE FORMAT PARAMETERS. Page code 3_H.
(Parameters not used by Tape are noted by Δ)

Bit / Byte	7	6	5	4	3	2	1	0
0	R	R	Page Code = 3_H					
1	Page Length (in bytes)							
	HANDLING OF DEFECTS FIELDS							
2	Tracks per Zone (MSB) Δ							
3	Tracks per Zone (LSB) Δ							
4	Alternate Sectors per Zone (MSB) Δ							
5	Alternate Sectors per Zone (LSB) Δ							
6	Alternate Tracks per Zone (MSB) Δ							
7	Alternate Tracks per Zone (LSB) Δ							
8	Alternate Tracks per volume (MSB) Δ							
9	Alternate Tracks per volume (LSB) Δ							
	TRACK FORMAT FIELD							
10	Sectors per Track (MSB) Δ							
11	Sectors per Track (LSB) Δ							
	SECTOR FORMAT FIELDS							
12	Data Bytes per Physical Sector (MSB)							
13	Data Bytes per Physical Sector (LSB)							
14	Interleave (MSB)							
15	Interleave (LSB)							
16	Track Skew Factor (MSB) Δ							
17	Track Skew Factor (LSB) Δ							
18	Cylinder Skew Factor (MSB) Δ							
19	Cylinder Skew Factor (LSB) Δ							
	DRIVE TYPE FIELD							
Bit	7	6	5	4	3	2	1	0
20	SSEC	HSEC	RMB	SURF Δ	INS	Reserved		
21	Reserved							
22	Reserved							
23	Reserved							

The following information is only valid to be sent to the target prior to the execution of the FORMAT UNIT command.

Handling of Defects Fields :
The target may or may not accept the exact value requested by the initiator in these fields, but may round to its nearest most convenient value (which value may be zero). In this case, the target shall create the Check Condition status with ILLEGAL REQUEST Sense Key. The initiator may issue a MODE SENSE command requesting the current Format Parameters Page to be returned, in order to be informed about which value has been set by the target in response to the initially requested value of the MODE SELECT command.

Tracks per Zone indicates that the target shall divide the capacity of the device, prior to format, in equal number of tracks for the purpose of allocating with the next four bytes, an equal number of alternate sectors or tracks per zone for handling defects. The last zone of the device may or may not include the same number of tracks as the previous zone(s). A value of zero means that the sole zone is defined as the whole unit. The capacity of the device is represented by the number of cylinders and number of heads returned in the Page 4 or 5 depending on the device type.

Alternate Sectors per Zone indicates the number of sectors that the target shall deallocate from the initiator addressable blocks during the FORMAT UNIT command. These sectors will be available to the target as replaceable sectors for defective sectors. The method used by the target to access alternate sectors when encountering a defective sector is device specific. A value of zero indicates that no alternate sectors are to be deallocated or that the MODE SENSE command indicated that the target does not support this field or does not authorize this field to be changeable.

Alternate Tracks per Zone indicates the number of tracks that the target shall deallocate from the initiator addressable blocks during the FORMAT UNIT command. These tracks will be available to the target as replaceable tracks for defective tracks. The method used by the target to access alternate tracks when encountering a defective track is vendor unique. A value of zero indicates that no alternate tracks are to be deallocated or that the MODE SENSE command indicated that the target does not support this field or does not authorize this field to be changeable.

Alternate Tracks per Volume indicates the number of tracks that the target shall deallocate from the initiator addressable blocks during the FORMAT UNIT command. These tracks will be available to the target as replaceable locations (tracks or sectors) for defect handling. The method used by the target to access these alternate tracks when encountering a defect is vendor unique. A value of zero indicates that no alternate tracks are to be deallocated or that the MODE SENSE command indicated that the target does not support this field or does not authorize this field to be changeable.

When the initiator sets the three fields (Alternate Sectors per Zone, Alternate Tracks per Zone, Alternate Tracks per Volume) to zero, it may rerquest the target to set its own default scheme for handling defects or may request the target not to perform any defect handling. The target may or may not return Check Condition status to this condition.

Track Format Field:

Sectors per Track indicates the number of physical sectors that the target shall allocate per disk track. This implies that the target set an equal data sector size to all sectors accordingly. The value of zero indicates that either the number of Sector per Track varies or that the MODE SENSE command reported that the target does not authorize this field to be changeable or that other mechanism implemented is not specified.

Sector Format Field:

Data Bytes per Physical Sector indicates the number of data bytes that the target shall allocate per physical sector. This value may be different from the logical block size in the Block Descriptor section of the MODE SELECT data. This implies that the target set an equal number of sectors per track accordingly. The target shall create the Check Condition status if it determines that the combination of this field and the sectors per track values exceed the physical abilities of the medium. The value of zero indicates that either the number of Data Bytes per Physical sector varies or that the MODE SENSE command rerported that the target does not authorize this field to be changeable or that other mechanism implemented is not specified.

Interleave is the same parameter passed in the FORMAT UNIT command, and is only returned by the MODE SENSE command. The target shall report this field as nonchangeable in the corresponding MODE SENSE command. The target shall ignore this field in MODE SELECT commands.

Track Skew Factor indicates the number of physical sectors between the last logical block of one track and the first logical block on the next sequential track of the same cylinder.

Cylinder Skew Factor indicates the number of physical sectors between the last logical block of one cylinder and the first logical block on the next sequential cylinder.

Drive Type Field:

A **SSEC** bit set to one indicates that the target shall use *soft* sector formatting. Δ

A **HSEC** bit set to one indicates that the target shall use *hard* sector formatting. The **HSEC** bit and the **SSEC** bit are mutually exclusive in MODE SELECT commands.

Possible combinations of MODE SENSE Report Default Values

SSEC	HSEC	
0	0	Target not allowed to return this combination
1	0	Target supports Soft sector formatting only Δ
0	1	Target supports Hard sector formatting only
1	1	Target supports both Soft and Hard sector formatting Δ

Possible combinations of MODE SENSE Report Changeable Values

SSEC	HSEC	
0	0	Sector formatting Not changeable
1	0	Target not allowed to return this combination
0	1	Target not allowed to return this combination
1	1	Target supports both Soft and Hard sector formatting Δ

A **RMB** (Removable) bit set to one indicates that the logical unit is removable. A **RMB** bit set to zero indicates that the logical unit is not removable.

The **SURF** (Surface) bit indicates how the target shall map the logical block addressing into physical block addressing. A **SURF** bit set to zero indicates that the target shall allocate progressive addresses to all sectors within a cylinder prior to allocating sector addresses to the next cylinder. A **SURF** bit set to one indicates that the target shall allocate progressive addresses to all sectors on a surface prior to allocating sector addresses to the next surface.

The **INS** (Inhibit Save) bit 3 byte 20 *set to one* in MODE SELECT commands indicates that the target shall inhibit the saving of any parameters during the successfull completion of the next FORMAT UNIT command. The **INS** bit *set to zero* indicates that the parameters of the Pages defined by the Page Codes 3, 4 and 5 shall be saved by the target if such pages were indicated to be saveable (by PS bit 7 byte 0 set to one in Page Headers) in preceding MODE SENSE commands.

As a reminder:
- The Pages defined by Page Codes 3, 4 and 5, depending on device type, include all parameters necessary to be indicated to the target prior to the FORMAT UNIT command. The saving, if implemented, shall therefore be performed only during the FORMAT UNIT command and not at any other time.
- All other Saveable Pages not affecting the format may be saved in following MODE SELECT commands if the SMP bit is set to one in the CDB of these MODE SELECT commands.

RIGID DISK DRIVE GEOMETRY PARAMETERS. Page Code 4_H. Δ

This Page is mainly intended for defining parameters of rigid disk drives, but may be used for flexible disk drives if deemed applicable.

Bit / Byte	7	6	5	4	3	2	1	0
0	R	R	Page Code = 4_H					
1	Page Length (in bytes)							
2	Number of Cylinders (MSB)							
3	Number of Cylinders							
4	Number of Cylinders (LSB)							
5	Number of Heads							
6	Starting Cylinder-Write Precompensation (MSB)							
7	Starting Cylinder-Write Precompensation							
8	Starting Cylinder-Write Precompensation (LSB)							
9	Starting Cylinder-Reduced Write Current (MSB)							
10	Starting Cylinder-Reduced Write Current							
11	Starting Cylinder-Reduced Write Current (LSB)							
12	Drive Step Rate (MSB)							
13	Drive Step Rate (LSB)							
14	Landing Zone Cylinder (MSB)							
15	Landing Zone Cylinder							
16	Landing Zone Cylinder (LSB)							
17	Reserved							
18	Reserved							
19	Reserved							

The target shall create the Check Condition Status with ILLEGAL REQUEST Sense Key if it receives values in Number of Cylinders and Number of Heads fields that are greater than the defaults values returned by the MODE SENSE command or greater than the actual values.

The target shall create the Check Condition Status with ILLEGAL REQUEST Sense Key if it receives values in Starting Cylinder-Write Precompensation or Reduced Write Current fields that are greater than the Number of Cylinders field.

Drive Step Rate is expressed in units of 100 nanosecoinds. The target shall use the lowest step rate, greater than or equal to the step rate required,that it is capable of implementing. A value of zero indicates that the target is required to set its default value.

The **Landing Zone Cylinder** field indicates two's complement location where the target shall position the disk heads prior to stop the spindle with the START/STOP command. This field is only meaningful with drives that do not automaticaly seek to the Landing Zone before stopping the spindle. A negative value steps the device outside the recorded cylinders. A value greater than the number of cylinders steps the device beyond the recorded cylinders toward the spindle.

FLEXIBLE DISK DRIVE PARAMETERS. Page Code 5_H. Δ

This Page is intended for defining parameters of flexible disk drives.

Bit / Byte	7	6	5	4	3	2	1	0
0	SDP	R	Page Code = 5_H					
1	Page Length (in bytes)							
2	Transfer rate (MSB)							
3	Transfer rate (LSB)							
	TRACK FORMAT FIELD							
4	Number of Heads							
5	Sectors per Track							
	SECTOR FORMAT FIELDS							
6	Data Bytes per Physical Sector (MSB)							
7	Data Bytes per Physical Sector (LSB)							
8	Number of Cylinders (MSB)							
9	Number of Cylinders (LSB)							
10	Starting Cylinder-Write Precompensation (MSB)							
11	Starting Cylinder-Write Precompensation (LSB)							
12	Starting Cylinder-Reduced Write Current (MSB)							
13	Starting Cylinder-Reduced Write Current (LSB)							
14	Drive Step Rate (MSB)							
15	Drive Step Rate (LSB)							
16	Drive Step Pulse Width							
17	Head Settle Delay							
18	Motor On Delay							
19	Motor Off Delay							
20	TRDY	Reserved						
21	Head Load Delay							
22	Starting Sector Number, Side Zero							
23	Starting Sector Number, Side One							

Transfer Rate (byte 2 and 3) is expressed in kilobits per second. As typical examples, the value in byte 2 and 3 shall be:

-$00FA_H$ to select 250 kbit/second transfer rate
-$012C_H$ to select 300 kbit/second transfer rate
-$01F4_H$ to select 500 kbit/second transfer rate
-$03E8_H$ to select 1 megabit/second transfer rate
-$07D0_H$ to select 2 megabit/second transfer rate
-1388_H to select 5 megabit/second transfer rate

Motor On Delay depends on the state of the TRDY bit. If TRDY is not set, the Motor On Delay indicates the amount of time in 1/10 second that the target will delay, before trying to access data after asserting the motor-on signal to the drive. If TRDY is set, the Motor On Delay indicates the amount of time that the target will delay for drive ready status before aborting a disk access.

Motor Off Delay indicates the amount of time in 1/10 second that the target will delay before deasserting the motor on signal to the drive after the target has become idle. A value of FF_H indicates that the motors are to be left on. In this case, the motors can still be controlled by the START/STOP UNIT command.

A TRDY (True Ready) bit of one indicates that the drive provides a ready signal which indicates that the spindle motor is up to speed and the drive and medium are ready to transmit and receive data. In this case, the target may attempt to access the disk immediately upon sensing drive ready.

Drive Step Rate and Step Pulse Width are expressed in units of 1 microsecond. The target shall round up to its next supported value.

CERTIFICATION PATTERN. Page code 6_H.

Bit / Byte	7	6	5	4	3	2	1	0
0	R	R	Page Code = 6_H					
1	Page Length (in bytes)							
2	Reserved							
3	Reserved							
4 through n	Vendor Unique							

This Page is intended to provide the pattern to be used by the target to fill out the data blocks during the FORMAT UNIT command.

Various schemes may be requested, all are vendor unique. Some examples may be:
- Fixed pattern of zero
- Fixed pattern of one
- Fixed and repetitive pattern of a defined value and of a defined length
- Pattern becoming variable starting with a fixed value and increasing by a defined value for a defined length
- Pattern becoming variable starting with a fixed value and shifting by a certain number of bits for a defined length
- Blocks filled with their Logical block address repeated
- Blocks filled with their Physical block address (cylinder, head, sector) repeated

SERIAL NUMBER. Page Code 20_H.

Bit / Byte	7	6	5	4	3	2	1	0
0	R	R	Page Code = 20_H					
1	Page Length (in bytes)							
2 through 9	Drive Serial Number in ASCII							

Initiators will not attempt to modify this page.

FORMAT LIMITS. Page Code 21_H (Tape Only)

Bit / Byte	7	6	5	4	3	2	1	0
0	R	R	Page Code = 21_H					
1	Page Length (in bytes)							
2	Starting Track for Format							
3	Ending Track for Format							

8.1.8 RESERVE UNIT Command (16_H)

Third party and Extent Reservation is Required.

The RESERVE and RELEASE commands are defined to be mandatory commands. In addition to the protocol defined in the ANSI X3T9.2 /82-2 Revision 17B document, these commands are to be implemented using EXTENTS (extent reservation and extent release). Apple requires a minimum of 8 extents to be supported on devices where extents are possible (Hard disk, Floppy disk, Direct Access Tape, CD Rom, M/O disk, ...). All four reservation types must be supported (Read Exclusive, Write Exclusive, Exclusive Access, Read Shared). The command format is shown in Tables 8-15 and 8-16 of X3T9.2, Rev. 17B.

8.1.9 RELEASE UNIT Command (17_H)

Third party and Extent Release is Required. The command format is shown in Tables 8-17 and 8-16 of X3T9.2, Rev. 17B.

8.1.10 MODE SENSE Command ($1A_H$)

Table 8-18
Mode Sense Command

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code							
1	LUN		Reserved					
2	PCF		Page Code					
3	Reserved							
4	Allocation Length							
5	VU	VU	Reserved				Flag	Link

The MODE SENSE command (Table 8-18) provides a means for a target to report its medium, logical unit, target or peripheral device parameters to the initiator. It is a complementary command to the MODE SELECT command.

It is Required that targets implement this command. It is recommended that the MODE SENSE command be issued prior to the MODE SELECT command.

The Allocation Length specifies the number of bytes that the initiator has allocated for returned MODE SENSE data. An Allocation Length of zero indicates that no MODE SENSE data shall be transferred. This condition shall not be considered an error. Any other value indicates the maximum number of bytes that shall be transferred. The target shall terminate the DATA IN phase when the Allocation Length have been transferred or when all available MODE SENSE data have been transferred to the initiator, whichever is less.

The MODE SENSE data (TABLE 8-19) contains a four-byte header, followed by one or more eight-byte block descriptors, followed by zero or more Pages.

Table 8-19
MODE SENSE DATA
MODE SENSE Header

Bit / Byte	7	6	5	4	3	2	1	0
0				Sense Data Length				
1				Medium Type				
2	WP			Reserved				
3				Block Descriptor Length				
				Block Descriptor(s)				

Bit / Byte	7	6	5	4	3	2	1	0
0	Density Code							
1	Number of Blocks (MSB)							
2	Number of Blocks							
3	Number of Blocks (LSB)							
4	Reserved							
5	Block Length (MSB)							
6	Block Length							
7	Block Length (LSB)							
	Page Descriptor(s)							

Bit / Byte	7	6	5	4	3	2	1	0
0	PS	R	Page Code					
1	Page Length (in bytes)							
2 to n	Refer to Page definition in MODE SELECT							

The Sense Data Length byte specifies the length in bytes of the following MODE SENSE data that is available to be transferred during the DATA IN phase. The Sense Data Length byte shall not include itself. If the Allocation Length of the CDB is too small to transfer all the sense data, the Sense Data Length shall not be adjusted to reflect the truncation.

Refer to the SCSI standard for the code values of the Medium Type field and of the Density Code field.

Optional additional blocks of parameters called *Pages* may be sent to the target in the Data Out phase of the MODE SELECT command, following either :
- the MODE SELECT Header, if the Block Descriptor length is set to zero.
- all Block Descriptors, if the Block Descriptor length is different than zero.

The Block Descriptor Length shall not include the length of the Pages.
Each defined Page is preceded by a Header of two bytes defining the Page Code and the length of the page. Following the Header the Pages are separated into subblocks containing a list of related flags and/or values.

Bits 7 and 6 of byte 0 are reserved.
The Page Code identifies the meaning of the following bytes in the Page. The

Page Code is either defined, reserved or vendor unique. The parameters in the defined Pages are classified in priority to ease implementation by the target.

The Page Length value of each defined page, shall not include the Page Length byte. The Page Length represents the number of bytes that the target supports in each Page. The target may return in the Pages of the MODE SENSE commands as many consecutive bytes that it supports, for each Page that it supports, without splitting fields of multiple bytes. The Page Length shall be set in the pages of the MODE SELECT commands to the exact same value (zero value included) returned by the target in the MODE SENSE Page Length bytes. Otherwise, the target shall create Check Condition status with the Sense Key of ILLEGAL REQUEST.

The initiator shall issue a MODE SENSE command requesting the target to return all Changeable values (PCF field configuration 0 1 and Page Code $3E_H$ in byte 2 of the MODE SENSE CDB) prior to issuing any MODE SELECT commands, in order to find out which Pages are implemented by the target and the length of each Pages for that particular LUN.

An initiator may request a particular Page to be returned by the target by selecting its code in byte one of the CDB.

Bit 7 byte 0 of each Page is reserved.

Vendor Unique fields shall be addressed in Vendor Unique Pages 20_H through 39_H, but not within the defined Pages.

PS (Parameters Saveable) bit 7 byte 0 of each Page Header set to one by the target indicates that the supported parameters will be saved by the target. PS set to zero indicates that the supported parameters cannot be saved by the target.

Page Code Field bits 7 and 6 byte 0 of the CDB.

7 6

0 0 Report Current Values

- If the Page Code is equal to $3F_H$, all Pages implemented by the target are to be returned to the initiator with fields and bits set to Current values.
- If the Page Code is different than $3F_H$, the Page defined by the Page Code, if supported by the target is to be returned to the initiator with fields and bits set to Current values.

The Current values are one of the following:

- as set in the last successfully completed MODE SELECT command.
- identical to the Saved values if saving is available and if no MODE SELECT command were yet issued since the last power on.
- identical to the Default values if no saving is available or if no Saved values are available.

Fields and bits not supported by the target shall be set to zero. The Page Length byte value of each Page returned by the target indicates the last field supported within the particular Page.

0 1 Report Changeable Values

- If the Page Code is equal to $3F_H$, all Pages implemented by the target are to be returned to the initiator with bits and fields that are allowed to be changed by the initiator set to one. Fields and bits not allowed to be changed by the initiator shall be set to zero.
- If the Page Code is other than $3F_H$, the Page defined by the

Page Code, if supported by the target, is to be returned to the initiator with bits and fields that are allowed to be changed by the initiator set to one. Fields and bits not allowed to be changed by the initiator shall be set to zero.

If no bits or fields are changeable within a Page, the target may or may not return bytes 0 and 1 of the Page. If the target returns these two bytes, the Page Length byte value shall be set to zero by the target. The Page Length byte value of each Page returned by the target indicates the last field supported within the particular page.

1 0 Report Default Values.
- If the Page Code is equal to $3F_H$, all Pages implemented by the target are to be returned to the initiator with fields and bits set to the target's or device's default values.
- If the Page Code is other than $3F_H$, the Page defined by the Page Code, supported by the target, is to be returned to the initiator with fields and bits set to the target's or device's default values. Fields and bits not supported by the target shall be set to zero.

The Page Length byte value of each Page returned by the target indicates the last field supported within the particular page.
The value of the fields returned with this code is intended to avoid confusion over whether the value of zero is the default or the nonsupported value.

1 1 Report Saved Values.
- If the Page Code is equal to $3F_H$, all Pages implemented by the target are to be returned to the initiator with fields and bits set to the saved values if saving is supported by the target.
- If the Page Code is other than $3F_H$, the Page defined by the Page Code, if supported by the target, is to be returned to the initiator with fields and bits set to the saved values if saving is supported by the target.

The Saved values are one of the following:
- the values saved during the last successfully completed FORMAT UNIT or MODE SELECT commands.
- or identical to the Default values if no saving possibility is available.

The mode of saving is vendor unique, the values may either be recorded on disk or saved in another manner.
Fields and bits not supported by the target shall be set to zero.
The Page Length byte value of each Page returned by the target indicates which fields are supported within the particular page.

Current values may be modified by successfully completed MODE SELECT commands. Saved values may be updated by a successfully completed FORMAT UNIT command. A FORMAT UNIT command completing with no *Check Condition* status shall indicate that the Saved values have been successfully saved.

Page Codes (bits 0 through 5 of byte 2)

Page Code	Meaning
0_H	Unit Attention
1_H	Error Recovery parameters
2_H	Disconnect/Reconnect Control parameters
3_H	Direct Access Device Format parameters
4_H	Rigid Disk Drive Geometry parameters
5_H	Flexible Disk Drive parameters
6_H	Certification Pattern
7_H through $1F_H$	Reserved
20_H	Serial Number
21_H	Format Limits
22_H through 39_H	Vendor Unique Page formats
$3A_H$ through $3B_H$	Reserved
$3C_H$ through $3E_H$	Vendor Unique
$3F_H$	Return all Pages to the initiator. See PCF bit configuration. Page Code valid for MODE SENSE commands only.

The target shall return the same Page Length value in each Page that it supports with the $3F_H$ Page Code whatever the value of each bit of the PCF field is.

After a power-on or reset, the actions to be taken by the target following MODE SENSE commands are :

If MODE SENSE is requesting :	Target Shall:
Default Values	Report Default Values
Saved Values	Report existing valid restore of parameters, or execute a restore of parameters if not previously performed, or report *Drive Not Ready* if unable to access the specific location on the drive where the saved values have been stored.
Current Values	Report a valid set of saved parameters if available, or execute a restore of parameters if not previously performed,or report *Drive Not Ready* if unable to access the specific location on the drive where the saved values have been stored.or attempt to identify the parameters if no saving is available (such as cyl., track, sector)or if all the above are unsuccessful, legitimately report Default values.

8.1.11 Start/Stop Unit{Load/Unload} Command $1B_h$ (For Tape Only)

Table 8-20

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation code							
1	LUN		Reserved					Immed
2	Reserved							
3	Reserved							
4	Reserved					Mod	Retensn	Start/Load
5	Vendor Unique		Reserved				Flag	Link

The Load/Unload command causes the cartridge to be autoloaded(if the Start/Load bit = 1), or unloaded, to the end-of-tape (if the Start/Load bit = 0).

An Immediate(Immed) bit of one indicates that status and message bytes will be returned to the initiator before the operation starts. An Immed bit of zero indicates that status and message bytes will be returned to the Initiator after the operation has been completed.

The command function depends upon the setting of the Mod, Retension and Start/Load bits as indicated by the following table.

Mod	Retension	Start/Load	Description
0	0	0	Normal Unload
0	0	1	Normal Load
0	1	0	Retension Only
0	1	1	Normal Load
1	0	0	Unload w/o Tape Movement
1	0	1	Load w/o Condition Pass
1	1	0	Retension only
1	1	1	Reserved

READ QIC-100 DATA Command (13_h) (For Tape Only)

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation code							
1	LUN		Reserved					
2	Reserved							
3	Reserved							
4	Reserved							
5	Reserved							

This command allows the host to read QIC-100 related information from the controller.

DATA-IN LAYOUT

Byte \ Bit	7	6	5	4	3	2	1	0
0	Date MSB (Default 0)							
1	Date LSB (Default 0)							
2	Time MSB (Default 0)							
3	Time LSB (Default 0)							
4	Lot Number MSB (Default 0)							
5	Lot Number LSB (Default 0)							
6	Manufacturer MSB (Default 0)							
7	Manufacturer LSB (Default 0)							
8	Frames per Track MSB							
9	Frames per Track LSB							
A	Track Offset MSB							
B	Track Offset LSB							
C	Stop Time MSB(in number of frames)							
D	Stop Time LSB(in number of frames)							
E	Interleave							
F	Transfer Size(0=8192b,1=8320b)							
10	Number of Bad Blocks on Tape (MSB)							
11	Number of Bad Blocks on Tape (LSB)							
12	Maximum number of Bad Blocks Allowed (MSB)							
13	Maximum number of Bad Blocks Allowed (LSB)							
14	Number of Alternate Blocks Assigned (MSB)							
15	Number of Alternate Blocks Assigned (LSB)							
16	Maximum Number of Alternate Blocks Allowed (MSB)							
17	Maximum Number of Alternate Blocks Allowed (LSB)							

WRITE QIC-100 DATA Command (14_h) (For Tape Only)

Byte \ Bit	7	6	5	4	3	2	1	0
0	Operation code							
1	LUN			Reserved				
2	Reserved							
3	Reserved							
4	Reserved							
5	Reserved							

This command allows the host to write QIC-100 related information to the controller.

DATA-OUT LAYOUT

Byte \ Bit	7	6	5	4	3	2	1	0
0	Date MSB (Default 0)							
1	Date LSB (Default 0)							
2	Time MSB (Default 0)							
3	Time LSB (Default 0)							
4	Lot Number MSB (Default 0)							
5	Lot Number LSB (Default 0)							
6	Manufacturer MSB (Default 0)							
7	Manufacturer LSB (Default 0)							
8	Frames per Track MSB(default=$026A_h$)							
9	Frames per Track LSB							
A	Transfer Size(0=8192b,1=8320b)							

READ DEFECT DATA Command (37_H)

Peripheral Device Type: Direct Access
Operation Code Type: Mandatory
Operation Code: 37_H

Byte \ Bit	7	6	5	4	3	2	1	0
0	Operation Code							
1	LUN			Reserved				
2	Reserved			P	G	Defect List Format		
3	Reserved							
4	Reserved							
5	Reserved							
6	Reserved							
7	Allocation Length (MSB)							
8	Allocation Length (LSB)							
9	Control Byte							

The READ DEFECT DATA command requests that the target transfer the medium defect data to the initiator.
The meaning of bits 0 through 2 of byte 2 is similar to the bit definition of the bits 0 through 2 of the byte 1 of the FORMAT UNIT command. The initiator indicates with this field a preferred format for the defect list to be returned by the target. This Defect List Format field is intended for those targets capable of returning various formats. A target unable to return various formats may return it's default format and create the Check Condition status with RECOVERED ERROR Sense Key at the end of the Read Defect Data data transfer.
- The P set to one indicates that the initiator requests the Primary list of defects be returned. The P bit of zero indicates that the target shall not return the Primary list of defects.
- The G bit set to one indicates that the initiator requests that the Growing list of defects be returned. The target shall include the Certification list of defects, if implemented, to be returned with this selection. The G bit of zero indicates that the target shall not return the Growing list of defects.

- With bits P and G both set to one, the target is requested to return the Primary and the Growing list of defects. The target shall determine the order in which the lists are to be returned and shall determine if the lists will be merged or not.
- With bits P and G both set to zero, the Defect List Header only is to be returned.

The Allocation Length specifies the number of bytes that the initiator has allocated for returned READ DEFECT DATA. An Allocation Length of zero indicates that no READ DEFECT DATA shall be transferred. Any other value indicates the maximum number of bytes that shall be transferred.
The target shall terminate the DATA IN phase when the Allocation Length data have been transferred or when all available READ DEFECT DATA have been transferred to the initiator, whichever is less.

The READ DEFECT DATA contains a four-byte header, followed by zero or more defect descriptors.

Defect List Header

Bit / Byte	7	6	5	4	3	2	1	0
0	Reserved							
1	Reserved			P	G	Defect List Format		
2	Defect List Length (MSB)							
3	Defect List Length (LSB)							

The meanings of bits 0 through 2 of byte 1 are similar to the Defect List Format in Table 8-4 of the FORMAT UNIT command. The bits P, G, and the Defect List Format indicate which defect list is actually returned by the target.

The format of the defect descriptors, if the Defect list length is different than zero, are shown in Table 8-5, 8-6, 8-7 in the FORMAT UNIT command. The length of each defect descriptor may be four bytes or eight bytes depending upon the Defect List format code. The defect list length specifies the total length in bytes of the defect descriptors that follow. The Defect List Length is equal to four or eight times the number of defect descriptors.

If the Allocation Length of the CDB is too small to transfer all the defect descriptors, the Defect List Length shall not be adjusted to reflect the truncation. The target shall not create a Check Condition status. It is recommended that the initiator compares the Defect List Length to the Allocation Length to ensure that it did not receive a partial list due to a too small Allocation Length.
The defect descriptors may or may not be sent in ascending order.

The initiator may be informed about the exact number of defects by dividing the Defect List Length by the Defect Descriptor Length.

SCSI ERROR CONDITIONS

This section describes the various SCSI bus-related errors can occur during the execution of a command and the actions taken by the target in response to these errors. A proper handling of the SCSI bus-related errors is by the implementation of :

- most messages of the Error Recovery Set, by both target and initiator
- Bus Parity enabled in both target and initiator

5.6.1 Target Mode Error Conditions

Under several error conditions, the target may change the phase to Bus Free, without correctly terminating the command (i.e. No Disconnect or Command Complete messages sent to the initiator). The target shall then clear all information regarding the command, with the exception of Sense Data (if any), and shall not attempt to reconnect to the initiator. The initiator shall consider this a catastrophic error. The initiator may issue a REQUEST SENSE command attempting to recover further information concerning the catastrophic error.

5.6.1.1 Message Out Phase Parity Error

Parity is optional, the following does not apply to those SCSI devices communicating on the bus and are not configured with Parity enabled.
When the target detects a Parity error during the Message Out Phase, it may retry the Message Out Phase using the following sequence (see section 5.1.9.2) :

1 - Continue the REQ/ACK handshakes until the initiator negates ATN (all message bytes received).
2 - Notify the initiator to resend all previous Message Out bytes within the current phase, by not changing the phase and by asserting REQ.
3 - The initiator shall then resend all previous message bytes.

If the message is not received correctly, the target may process the error using one of the following sequences:

1 - Immediately go to Bus Free phase with no Sense Key/Sense Code information set.
2 - Terminate the present command with a *Check Condition* status and set the Sense Key/Sense Code to *Aborted Command Parity Error.* This error does not prevent the initiator from retrying the command.
Note : This method can be used only if the addressed LUN is known from an Identify message or from the LUN field in the CDB.

5.6.1.2 Command Phase Parity Error

Parity is optional, the following does not apply to those SCSI devices communicating on the bus and that are not configured with Parity enabled.
When the target detects a parity error during the Command phase, it may retry the Command Phase using the following sequence :

1 - Change the phase to Message In, send the initiator a Restore Pointers message to reset the command pointer to byte 0 of the command.
2 - Attempt to receive all command bytes again.

If the command is not received successfully, the target will abort the command using one of the following sequences :

1 - Immediately go to the Bus Free Phase with No Sense Key/Sense Code information set.

2 - Terminate the command with a *Check Condition* status and set the Sense Key/Sense Code to *Aborted Command/Parity Error*. This error does not prevent the initiator from retrying the command.
Note: This method can be used only if the addressed LUN is known from an Identify message.

5.6.1.3 Data Out Phase Parity Error

Parity is optional, the following does not apply to those SCSI devices communicating on the bus and that are not configured with Parity enabled. When the target detects a parity error during the Data Out phase, it may retry the Data Out Phase using the following sequence :

1 - Change the phase to Message In, send to the initiator the Restore Pointers message to reset the data pointer to the first byte.
2 - Change the phase to Data Out to receive the data again.

If the data is not received successfully, the target will terminate the command with a *Check Condition* status and set the Sense Key/Sense Code to *Aborted Command/Parity Error*. This error does not prevent the initiator from retrying the command.

5.6.1.4. Initiator Detected Error Message

If the target receives an *Initiator Detected Error* message, it may retry the previous operation using the following sequence :

1 - Change the phase to Message In, send to the initiator the Restore Pointers message.
2 - Return to the phase just prior to the receipt of the *Initiator Detected Error* message and retry the operation.

If the operation cannot be completed successfully, the target will abort the command using one of the following sequences :

1 - Immediately go to the Bus Free Phase with no Sense Key/Sense Code information set.
2 - Terminate the current command with a *Check Condition* status and set the Sense Key/Sense Code to *Aborted Command \Initiator Detected Error*. This error does not prevent the initiator from retrying the command.

5.6.1.5 Rejected Messages

When the target receives a *Message Reject* message from the initiator, it may retry the operation by resending the original message. If the message cannot be sent successfully, the target will take the following action, based on which message was rejected.

Command Complete : The Target shall go to Bus Free phase and not consider this an error.

Disconnect : The target shall not disconnect and shall continue the current command. This condition does not preclude the target from attempting to disconnect at a later time.
Note : The target shall not send the Disconnect message to an initiator which indicated previously in the Identify message that it does not support the disconnect/reconnect option.

Identify : Sent to reconnect. The target shall immediately go to the Bus Free

phase and abort the command. No further reconnection shall be attempted, and no Status or Message In phase with Command Complete message shall be created by the target. The target shall set the Sense Key/Sense Code to *Hardware Error/Message Reject Error.*

Linked Command Complete or Linked Command Complete with Flag : The target shall immediately go to the Bus Free phase and shall not attempt to change the phase to Command phase. The link shall be broken. The target shall set the Sense Key/Sense Code to *Hardware Error/Message Reject Error.*

Message Reject : The target shall immediately terminate the command with Check Condition status and set the Sense Key/Sense Code to *Hardware Error/Message Reject Error.*

Restore Pointers : Since the Restore Pointers message is normally used during retries or error recovery, the target shall abort the retry or recovery attempt, shall assume that the error is unrecoverable, then complete the command according to the error condition.

Save Data Pointer : The target shall assume that the initiator does not support the Save Data Pointer message, shall not attempt to disconnect from the bus, but shall complete the command.

Synchronous Data Transfer : The target shall assume that the initiator does not support the Synchronous Transfer mode, and shall continue execution using asynchronous transfer.

5.6.1.6 Initiator Message Parity Error

When the target receives a Message Parity Error message from the initiator, it may retry the operation by resending the original message once. If the message cannot be sent successfully, the target shall immediately go to the Bus Free phase and abort the current SCSI command. No further reconnection shall be attempted, no status or Command Complete message shall be returned for the command. The target shall set Sense Key/Sense Code to *Aborted Command/Parity Error.*

5.6.1.7 Reselection Timeout

When the target attempts to reselect to the initiator and the initiator does not respond within a Selection Timeout Delay, the reselection shall be aborted. The target may attempt reselection one or more times. The target shall determine after how many attempts to abort the command. No further reconnection shall be attempted and no status or Command Complete message shall be created for the command. The target shall set Sense Key/Sense Code to *Hardware Error/Select-Reselect Timeout.*

Implementors Note : The initiator shall implement an overall command timeout delay to detect this error.

5.6.1.8 Internal Target Errors

If an error occurs within the target which is related to the SCSI hardware or firmware, the target shall terminate the present command with a Check Condition status and set the Sense Key/Error Code to *Hardware Error/SCSI Hardware Error.* This error does not prevent the initiator from retrying the command.

2.2 Sequential Access Commands

T.B.S.

2.3 Printer Commands

T.B.S.

2.4 Scanner Commands

T.B.S.

3.0 Boot Procedures (For Bootable Devices)

3.1 Macintosh Boot Procedures

To allow for boot capability from any bootable SCSI device from the Macintosh 128K ROM, a data structure for logical block 0 has been defined. This data structure will allow the ROM code to locate the various drivers available for *upload* to the host. These drivers can be located anywhere on the drive and can be as large as required. Additionally, there is a data structure for logical block 1 describes the allocation of blocks on the device for different partitions and /or operating systems.

The ROM code, in order to boot properly, must be able to read blocks from the SCSI device and be able to analyze logical blocks 0,1.

A typical Macintosh boot procedure would proceed as follows:

0. Hard Reset
1. Attempt to select the device by its SCSI ID.
2. Read the first 256 bytes of logical block 0 and check for proper signature indicating a valid Driver Descriptor Map (DDM). Read the 256 bytes of Device Partition Map from logical block 1 and check for proper signature.
   <-------If error, else
3. Search the DDM for a driver for the host machine.
4. Upload the driver from the indicated logical blocks into system RAM by using standard READ commands. Check for proper driver signature.
5. Call the driver to install itself, also passing a pointer to the DPM for examination by the driver.
6. Perform these steps for all other SCSI ID's on the bus.

Once the driver is installed in the host's disk environment, the boot operation can continue normally. For example, in the Macintosh world, a *read* of *logical* blocks 0 and 1 would fetch the appropriate Macintosh boot blocks. (Macintosh *logical* or any other partition *logical* is *DPM Starting Block Address*"greater than *SCSI* logical.)

3.2 6502 Boot Procedure

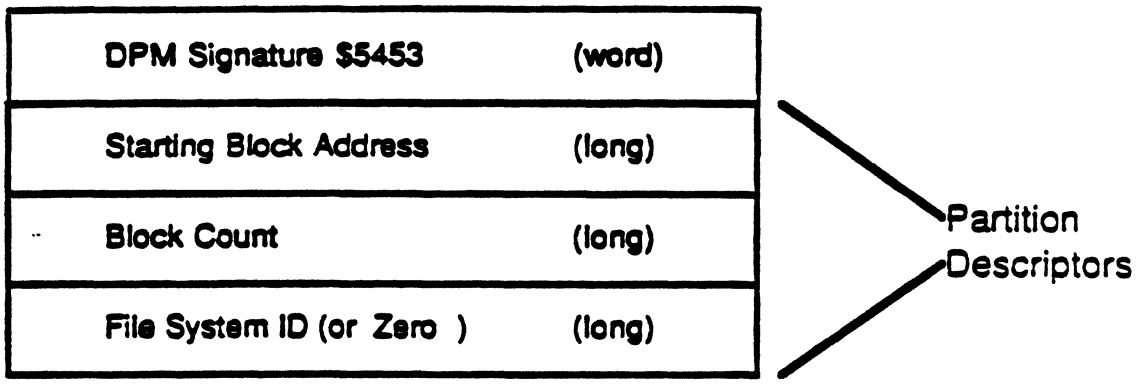
Because the ProDos Apple// operating system does not support loadable device drivers, the SCSI driver will reside, in total, in ROM on the SCSI interface board. In an effort to provide flexibility, the interface board will allow some SCSI program modules (RAM modules) to be loaded into the interface board RAM. The intention is to allow a special SCSI device the ability to provide code that was not incorporated into the interface board ROM. This code can then be executed as a module attached to the normal SCSI firmware.

The ProDos boot procedure from a SCSI device would proceed as follows:

1. Select device by SCSI ID.
2. Look for a valid Driver Descriptor Map (DDM). Read the 256 bytes of Device Partition Map (DPM) from physical block 1 and check for proper signature.
3. Look through the DDM to see if a *driver* for the host machine is present.
4. Do a mode sense of the SCSI device, using the parameters to get pertinent device information and help construct a table of device information in interface card RAM.
5. Load the *driver* RAM module into interface board RAM, filling the RAM heap from the top.
6. Repeat steps 1 through 5 for all valid SCSI ID's found on the bus.
7. Locate the ProDos Boot device.
8. Load ProDos starting at $0800 in system RAM.

Device Partition Map (DPM)

Logical Block 1



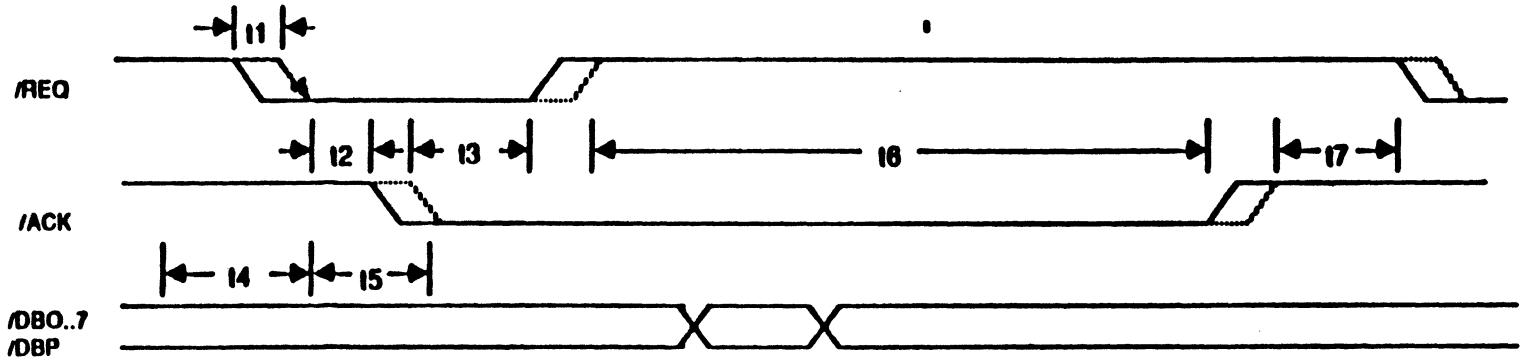
SCSI Boot Data Structures

Driver Descriptor Map (DDM)

Logical Block 0

DDM Signature $4552	(word)
Blocksize	(word)
Block Count	(long)
Device Type	(word)
Device ID	(word)
Data Area Start	(long)
Count of Driver Descriptors	(word)
Block Address of Driver	(long)
Driver Size in Blocks	(word)
Driver System Type	(word)

Driver Descriptors



	min.	typ.	max.	unit
t1 : Cable propagation delay	0	3		
t2 : /REQ true to /ACK true at the initiator	20	150	160	ns
t3 : /ACK true to /REQ false at the target	25	110	125	ns
t4 : Data setup time to /REQ true at the initiator	20			ns
t5 : Data hold time from /REQ true	50			ns
t6 : /REQ false to /ACK false at the initiator	15	120	140	ns
t7 : /ACK false to /REQ true at the target	20	140	150	ns

Figure 4.1 SCSI READ : INITIATOR RECEIVES & TARGET SENDS

Apple DeskTop Bus

INTRODUCTION

The Apple DeskTop Bus is a method and protocol for interconnecting computers with human input and other devices. This specification covers the Physical, Datalink, and Network layers of the Apple DeskTop Bus . In this specification the computer is referred to as the host. Peripherals connected to the bus are referred to as devices.

The host is the undisputed bus master. It controls the flow of data by issuing **Commands** and it is the only device permitted to issue them. **Talk** is the command used for a data transaction from a device to the host. **Listen** is the command used for a data transaction from the host to a device.

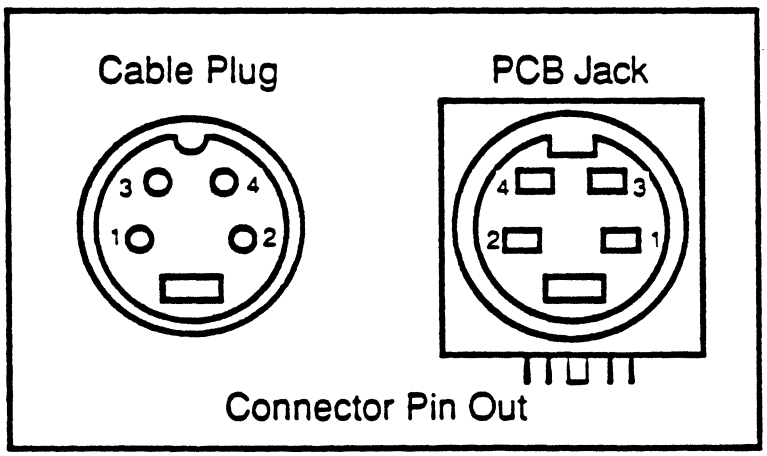
PHYSICAL LAYER

Interconnection:

All devices will communicate with the host via a four pin Mini-4 jack, as specified in Apple Specification, 519-0370., with the following connector assignments;

1. Data
2. Reserved
3. Power(V+)
4. Return

They will be connected with three conductor cables, which do not exceed 100 pf per meter, terminated with four pin Mini-4 plugs, as specified in Apple Specification, 519-0320 The maximum length of all cables shall be five meters.



Signal Levels:

Host:

Data:

The data line will be pulled up in the host with a 470 Ω ± 10% resistor and shall have the characteristics outlined in Table 1.

Power:

The Host will supply 5.0 Vdc ± 10% at .5 Amp minimum to the devices. The power line will be current limited by the host to prevent systems damage in the event of a Power to Power Return short. One **Apple DeskTop Bus Load** (ADBL) is defined as a power consumption by a device of twenty five milliamps. Each system shall clearly state in its documentation the number of **Apple DeskTop Bus Loads** it can support.

FDB Host Electrical Characteristics					
Symbol	**Parameter**	**Test Condition**	**Min.**	**Max.**	**Unit**
V_{IL}	Low-Level Input Voltage		-0.2	0.8	V
V_{IH}	High-Level Input Voltage		2.4	V+	V
V_{OL}	Low-Level Output Voltage	I_{OL} = 12 mA	—	0.45	V
V_{OH}	High-Level Output Voltage	I_{OH} = -4.0 mA	2.4	—	V

Table 1

Devices:

Data:

The data line shall have the characteristics outlined in Table 2.

Power:

Each device shall be clearly marked on the device and in its documentation with the number of **Apple DeskTop Bus Loads** it represents, which is equal to the devices maximum power consumption divided by twenty five milliamps.

FDB Device Electrical Characterist ics					
Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{IL}	L ow-Level Input Voltage		-0.2	0.8	V
V_{IH}	High-Level Input Voltage		2.4	V+	V
V_{OL}	Low-Level Output Voltage	I_{OL} = 12 mA	—	0.45	V
I_{OZ}	Off State Output Current	V_I = 0.4 V	—	-20	uA
C_{IN}	Input Capacitance		—	150	pF

Table 2

Modulation:

There are three forms of modulation on the bus; Normal modulation which transmits commands and data, High Speed modulation which transmits data, and Signals which broadcast global messages such as Service Request and Reset.

Normal Modulation:

An RZ code for modulation has been adopted for the **Apple DeskTop Bus** . Each bit cell boundary is signified by a falling edge on the bus. The period of each bit cell is the time between two falling edges on the bus. The time for a normal modulation bit cell, T_{cyc}, is 100 usec ± 30%. All devices must support, initialize, and reset in normal modulation.

The data is encoded as the ratio of low to high time of each bit cell. Thus a "0" is encoded as a bit cell in which the low time is greater than the high time. Conversely, a "1" is encoded as a bit cell in which the low time is less than the high time. A **Start** is defined as a "1".A **Stop** is similar to a "0", in that it has a low time of T0 , but it does not have another negative edge to define the bit cell time. It is used to synchronize the stopping of a transaction.

High Speed Modulation:

High speed modulation is used only for data and not commands. A device will not send data with high speed modulation unless it has been enabled to do so by the host. The time for a high speed modulation bit cell is 50 usec ± 1%.

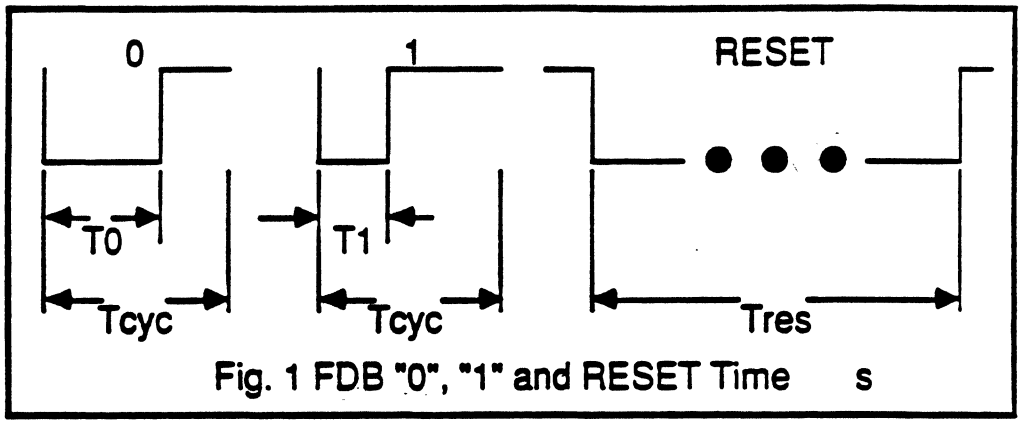


Fig. 1 FDB "0", "1" and RESET Time s

Signals:

Certain transactions fall under the category of neither commands nor data transactions. These are special transactions which globally broadcast status to devices on the bus. There are four special transactions in this group.

Attention and Sync:

To signal the start of a command, a long **attention** pulse is sent. This is followed by a **synch** pulse to give the initial bus timing. The falling edge of the **synch** pulse is used as a timing reference for the first bit of the command .

Reset:

Reset issues a break on the bus by holding the bus low for a minimum of T_{res}.

Service Request:

Service Request is a transaction that devices can use to signal the host that they require service, i.e. have data to send. Following any command transaction, a requesting device can signal by holding the bus low during the low portion of the stop bit of the **Command** transaction. The requesting device holds the bus low T_{int} beyond the bit cell boundary to signal.

Once a device has requested service by asserting a **Service Request** on the bus, it shall request service repeatedly until serviced. When the requesting device is addressed to **Talk** to any register, it will not assert **Service Request**. When the requesting device is addressed to **Talk** to the register which contains the data causing the **Service Request** condition, it will not assert **Service Request** , shall be considered serviced, and not request service again until it again needs to be serviced.

The ability for a device to assert a **Service Request** can be enabled and disabled by the host. All devices shall be initialized with the **Service Request** capability enabled.

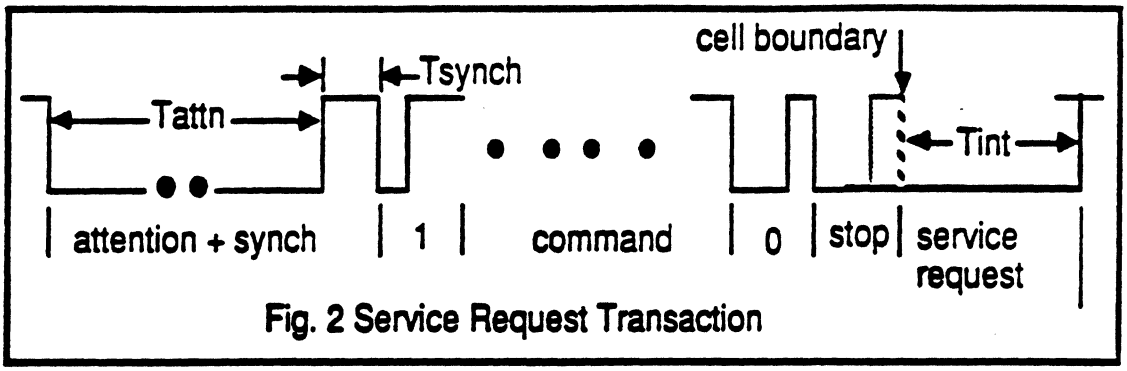


Fig. 2 Service Request Transaction

FDB Interface Characteristics						
Symbol	Parameter	Min.	Max.	Unit	Fig.	Definition
T0	"0" low time	60	70	% Tcyc	1	
T1	"1" low time	30	40	% Tcyc	1	
Tattn	ATTENTION signal	560	1040	usec	2	8 * Tcyc
Tcyc	FDB bit cell time	70	130	usec	1	
Tint	INTERRUPT signal	140	260	usec	2	2 * Tcyc
Tres	RESET signal	2.8	5.2	msec	1	40 * Tcyc
Tsynch	Synch pulse width	60	70	% Tcyc	2	
Tlt	Stop to start time	140	260	usec	3	2*Tcyc
Tstop	Stop pulse width	49	91	usec	3	

Table 3

Transactions:

Commands:

The format of a **command** is an **attention** signal, followed by a **sync** signal, then by eight data bits,and to synchronize the stopping of the transaction, a **stop** bit. Following the imaginary bit cell boundary after the **stop** bit, the transaction is complete and the host releases its active drive of the bus.

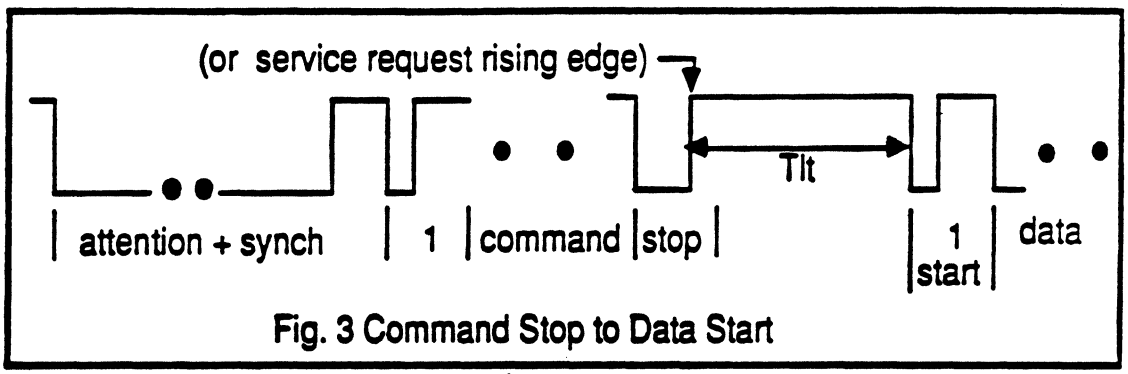


Fig. 3 Command Stop to Data Start

Data:

The format of a **data** transaction is a **start** bit ,followed by N times 8 bits of data with the most significant data bit sent first, where N may be from 2 to 8, followed by a **stop** bit. The specific length of the data transaction for a specific device is defined at a higher level of the protocol.

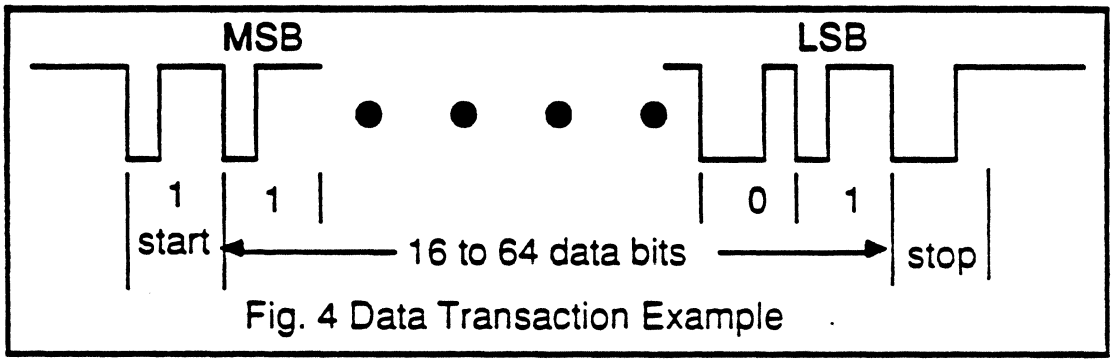


Fig. 4 Data Transaction Example

DATA LINK:

Each device on the bus has an address. There shall be only one active talker on the bus at any time, (see colision detection) this may be the host or an addressed device. A device addressed to talk, with data to send, "untalks" itself after it sends its data. If a device has no data to send, it "untalks" itself immediately and allows the bus to time-out.The host may also send data after a command.

Apple DeskTop Bus Peripherals:

Addresses:

All devices have a four bit command address which is defined by device type assignment. A device will always respond to that address on either power on or after a reset signal. The **Soft Address** locations are places were devices may be moved to by the host. The Addresses are assigned as shown in Table 4.

Device Table			
Address	Device type	Addressing	Example
0000 (0)	ADAPSO keys	extended	
0001 (1)	Appliances	extended	
0010 (2)	Encoded devices	movable	Keyboard
0011 (3)	Relative devices	movable	Mouse
0100 (4)	Absolute devices	movable	Tablet
0101 (5)	Reserved	-	
0110 (6)	Reserved	-	
0111 (7)	Reserved	-	
1000 (8)	Soft address	-	
. .	. .	. .	
1111 (15)	Soft address	-	

Table 4

Registers:

All devices have at most four locations to receive data, and at most four locations to send data. These locations are called **registers** and are referred to as **R0** to **R3**. They depend on addressing mode supported and are defined as follows:

Register 0 Talk: Data Register, Device specific as to meaning.

Register 0 Listen: Data Register, Device specific as to meaning.

Register 1 Talk: Data Register, Device specific as to meaning.

Register 1 Listen: Data Register, Device specific as to meaning.

Register 2 Talk: Data Register,Device specific as to meaning.

Register 2 Listen: Movable Devices: Device specific as to meaning.
Extended Address Devices: Enabling Extended Address

Register 3 Talk: Status information, ie: device address, handler.

Register 3 Listen: Status information, ie: device address, handler.

Commands:

Commands may be sent only by the host. There are four commands; **Talk, Listen, SendReset, and Flush.** A command is an eight bit value with the following syntax. The most significant nibble is the address which ranges from 0 - 15 (A3-A0). The next two bits form the command. The last field is a two bit register address field (RB,RA). This field, which is optional, allows a specific register, **R0** to **R3**, within an addressed device to be specified. An example of where this might be used is to differentiate a data register (in a keyboard, the specific keystroke) from a status or configuration register (in a keyboard, a response that signifies the model of the keyboard).

Command Syntax			
7654	**32**	**10**	**Command**
XXXX	00	00	SENDRESET *
A3 - A0	00	01	FLUSH
XXXX	00	10	RESERVED
XXXX	00	11	RESERVED
XXXX	01	XX	RESERVED
A3 - A0	10	RB RA	LISTEN
A3 - A0	11	RB RA	TALK
* forces RESET signal on FDB			

Table 5

To allow for future expansion of the command structure, a group of "place holder" **Reserved** instructions has been defined. These instructions shall be treated as no response and immediate bus release.

As a specific example, a **Talk** command to **Register 0** of device 5 would be encoded as "01011100". The bus would be modulated with the following:

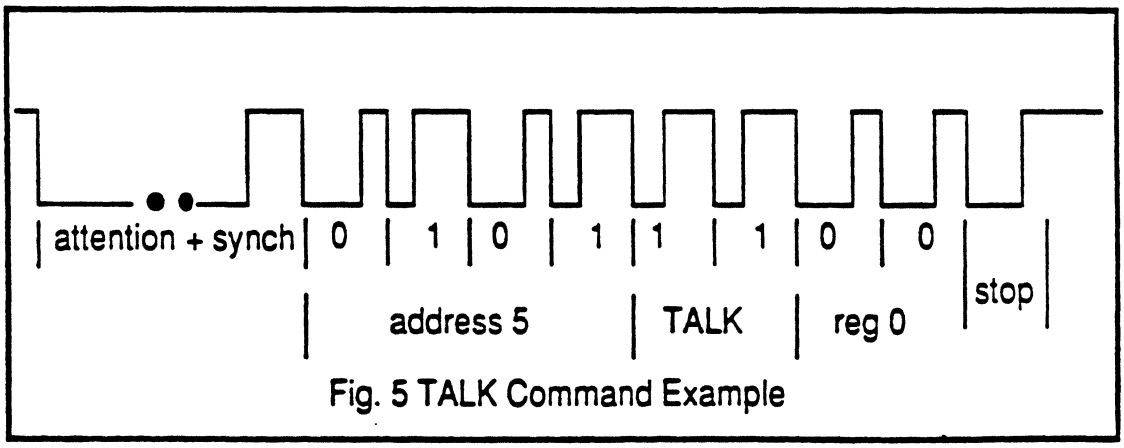


Fig. 5 TALK Command Example

Talk:

All devices on the bus must support **Talk** and **Listen** commands. When a device is addressed to **Talk**, it must respond before being timed out by the host. This timeout shall be T_{lt} max. after the rising edge of the stop bit of the **Talk** command.

The selected device, if it does not timeout, becomes active on the bus. It performs its data transaction no sooner then T_{lt} min after the rising edge of the stop bit of the **Talk** command then "untalks" itself and goes inactive on the bus.

Listen:

When a device is addressed to **Listen**, it is enabled to receive the data bits that are placed on the bus by the host. The host performs its data transaction within T_{lt} min to T_{lt} max, after the rising edge of the stop bit of the **Listen** command After the data bits are received, the transaction is complete and the device "unlistens" itself. If a device is addressed to **Listen** and it receives another command on the bus before it receives any data, then by definition the transaction is immediately complete and the device "unlistens" itself. Any "handshaking " will be handled at a higher level.

SendReset:

The **SendReset** command bit pattern does not go out on the bus. It causes a **Reset** signal to be put on the bus. The **Reset** has the effect of resetting all pending **Service Requests**; enabling the service request mode of all devices to enable; and in general puts the devices in a mode in which they will accept commands.

Flush:

The effect of the **Flush** command is defined by the device. It can be used for such functions as clearing a fifo and resetting all keys on a keyboard so they will be sent again.

Collision Detection:

All devices will detect a collision of data. If a device is trying to output a one and the data line is or goes to a zero, it has lost a collision to another device. If another device sends data before the device is able to assert its start bit, it has lost a collision. The losing device should immediately "untalk" itself and preserve the data that was being sent for retransmission. The device will set an internal flag if it loses a collision .

The device will clear the internal flag each time it is able to **Talk** without detecting a collision.

In order to aid in collision detection, devices using internal clocks that operate within ± 1% should attempt to assert their start bit at a random time within the limits of the line turn around time, T_{lt}.

Error Conditions:

If the data line gets hung low for T_{res}, all devices will reset themselves and output a one. If a command transaction is incomplete by staying high beyond the maximum bit cell time, all devices will ignore the command and seek another attention signal.

NETWORK LAYER:

Preferred Systems Implementation:

Assumptions:

The **Apple DeskTop Bus** is designed to be used primarily for human input devices. These types of devices have three characteristics which should be taken into consideration when designing systems software to use the bus. First, the rate of information coming from an input device is slow relative to the systems visual update. Second, only one device is used for input at any given time. Third, the time moving from one device to another is very long compared to the systems visual update.

Activity:

In order to allow for the use of inexpensive electronics in **Apple DeskTop Bus** devices the preferred systems inplemention minimizes activity on the bus by only polling the active device once each vertical retrace interval. If a **Service Request** is detected a polling sequence of **Register 0** is initiated to determine the device which has data and is requesting service. Once located, this device becomes the active device, it's **Service Requst Enable** is disabled, and the old active device's **Service Request Enable** is enabled. The default active device should be the relative positioning device.

Apple DeskTop Bus Peripheral Types:

Movable devices:

These devices will have the capability of being moved by the host to a Soft Address location. Movable device will optionally have a switch on them to indicate activity, which is called the activator. The activator can be a special key on a keyboard or a mouse button. In order to aid in collision detection they will also replace the address portion of the address field of Register 3 with a random number in response to a Talk R3 command.

Extended Address devices:

These devices all have the same command address as well as a unique 16 to 64 bit extended address which is stored in the device. Their command address may not be changed. On power up or after Reset they will only accept the Listen R2 command. They are enabled to talk and listen only after receiving a Listen R2 command in which the data matches their stored address. Once enabled they will respond to all commands addressed to them and have the capability to assert a Service Request. These devices become disabled after receiving a Listen R2 command in which the data does not match their stored address.

Register 3:

Register 3 contains the information which tells the device how to behave relative to the host.

Service Request and High Speed Enabling:

The Listen R3 command can be used to enable and disable Service Request and High Speed modulation. They are enabled by setting the appropriate bit in Register3 to a one and disabled by setting the appropriate bit to a zero.

Enabling the Service Request bit gives devices on the bus the ability to request service from the host. Setting the bit allows the device to signal a Service Request on the bus, or conversely, clearing the bit disables the signalling of a Service Request. This is useful in systems where the Service Request response time in a polled system is longer than desired. Or, when only specific devices are required for an application, the others could be disabled.

Enabling the High Speed bit causes the device to use High Speed modulation. Setting the bit causes the device to use High Speed modulation on the bus, or conversely, clearing the bit disables the use of High Speed modulation.

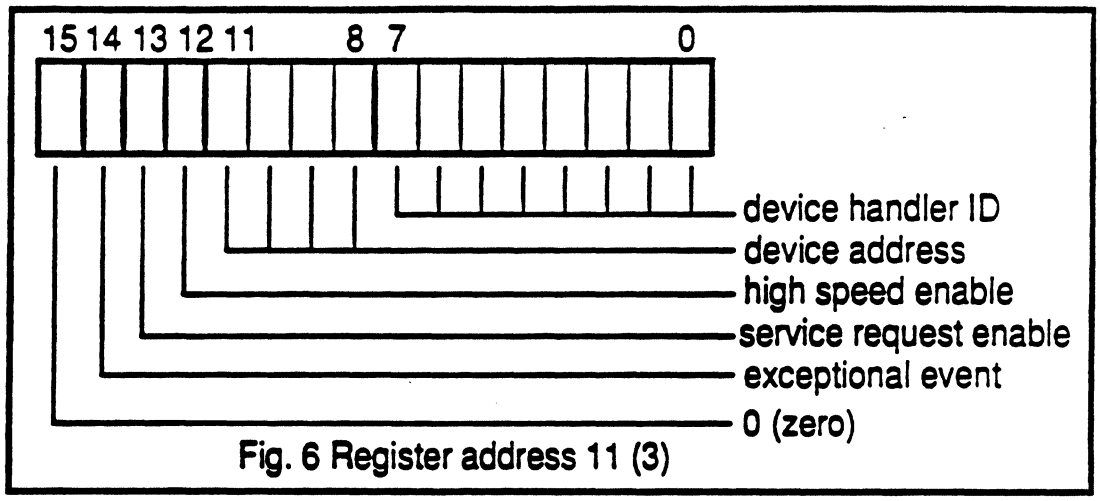


Fig. 6 Register address 11 (3)

Exceptional Event:

The **Exceptional Event** bit in **Register 3** can be cleared by a device to indicate an exceptional input condition such as reset or a failure.This bit shall be set to a one if not used. The specific application is defined at a higher level.

Handlers:

Handlers define a set of capabilities in both the host and the device such as the meaning of the data in each of the registers, the length of data transactions, ect. The host is able to interact with devices to modify thier function with a **Handler ID** which is stored by the device in **Register 3**. The host is able to change the the way a device functions by sending it a new **Handler ID** with a **Listen R3** command. If the receiving device is able to match the **Handler ID** to a function in the device, the new **Handler ID** will be stored and sent in response to a **Talk R3** command.

Reserved Handler ID's

The **Handler ID** "FF" hex is reserved for the self test mode for all devices. The ID in **Register 3** prior to command shall be perserved.

The **Handler ID** "00" hex, in response to a talk is reserved to indicate a failed self test.
The **Handler ID** "00" hex sent with a listen is reserved to indicate that the device is only to change unconditionally bits 8 to 13 of **Register 3**. The ID in **Register 3** prior to command shall be perserved.

The **Handler ID** "FE" hex sent with a listen is reserved to indicate that the device is only to change the address portion of **Register 3** if no collision has been detected. The ID in **Register 3** prior to command shall be perserved.

The **Handler ID** "FD" hex sent with a listen is reserved to indicate that the device is only to change the address portion of **Register 3** if the devices switch is depresed. The ID in **Register 3** prior to command shall be preserved.

Changing Addresses:

Systems Level:

At the systems level a host can change the address of Movable devices by forcing the collision of devices sharing the same address. By issuing a **Talk R3** command and following it with a **Listen R3** command, with a new address in bits 8 to 11 and **Handler ID "FE"** in bits 0 to 7 of the data, the device which did not detect a collision will be moved to the new address. This process can be repeated at the initialization address until the response to the **Talk R3** command is a time out. This can be used to identify and relocate multiple devices of the same type after initialization of the system.

Applications Level:

At the applications level addresses can by changed by displaying a message requesting a user to use the devices activator. The host then issues a **Listen R3** command with a **Handler ID** of **"FD"** to a new address and the device with the activator being used is moved. This can be used to identify and locate individual devices in multi-user applications.

Device Assignments				
Device	Initialization Address	Extended Address	Handler ID	Specification Number
Transciever	01	0000	01	341-0440
Keyboard	02	N/A	01	062-2068
Mouse	03	N/A	01,02	669-0152

Table 6

Excerpts from
KEYBOARD SPECIFICATION

6.0 COMMUNICATION PROTOCOL

6.1 THE KEYBOARD SHALL MEET ALL REQUIREMENTS OF THE APPLE DESKTOP BUS SPECIFICATION #062-0267.

6.2 THIS SPECIFICATION DEFINES THE REQUIREMENTS OF HANDLER I.D. 0001H FOR ENCODED DEVICES.

6.3 THE ACTIVATOR SHALL BE THE OPEN APPLE KEY (KEY #72).

6.4 ANY VALID KEY DEPRESSION OR RELEASE SHALL CAUSE DATA TO BE TRANSMITTED THROUGH REGISTER 0 PER SECTION 8. IF THERE IS DATA IN REGISTER 0, SRQ SHALL BE ASSERTED IF ENABLED.

6.5 IF THERE IS ONLY A SINGLE CHARACTER TO BE TRANSMITTED A FILL CHARACTER OF FFH WILL BE INSERTED FOR EITHER KEY CODE. THE EARLIEST KEY PRESSED SHALL ALWAYS BE IN KEY CODE 1.

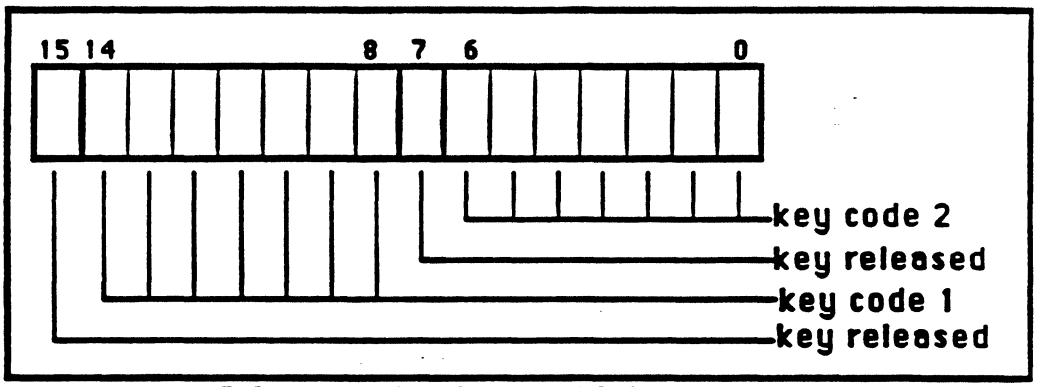


FIGURE 1 KEYBOARD REGISTER 0

6.6 THE STATUS OF THE FOLLOWING KEYS WILL BE INDICATED IN REGISTER 2 PER FIGURE 2

CAPS LOCK	(70)
OPEN APPLE	(72)
SHIFT	(53 & 64)
OPTION	(71)
RESET	(81)
CONTROL	(37)
DELETE	(14)

6.6.1 A DEPRESSED KEY WILL BE INDICATED BY A ZERO AND A RELEASED KEY WILL BE INDICATED BY A ONE.

6.6.2 THE STATUS INDICATED SHALL BE THE CURRENT STATUS OF THE KEY AND SHALL NOT BE BUFFERED.

6.7 BITS 0 TO 7 AND 15 ARE RESERVED.

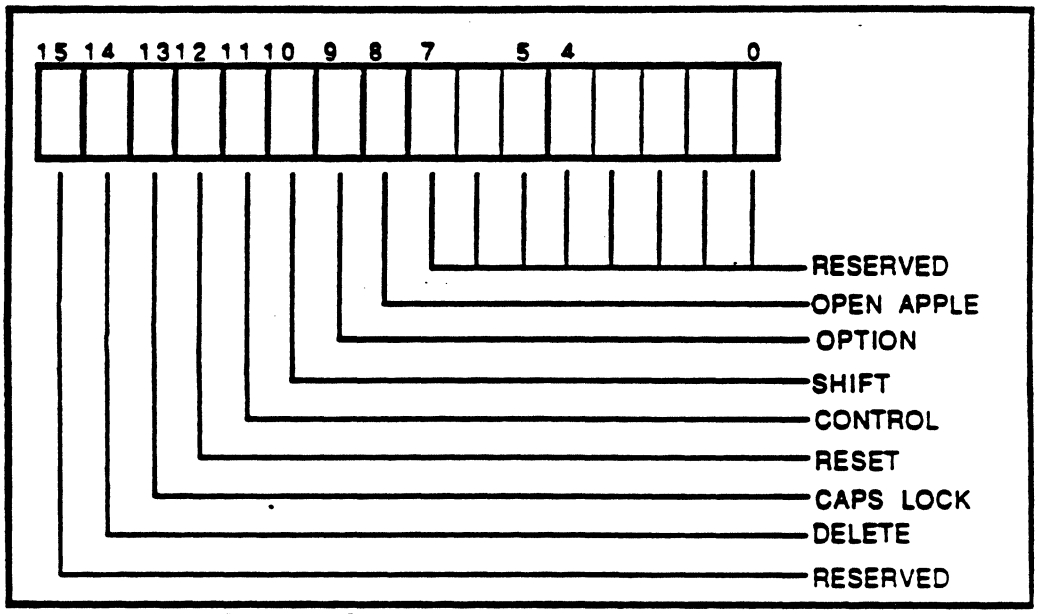


FIGURE 2 KEYBOARD REGISTER 2

6.8 A DEPRESSED RESET KEY (KEY 81) WILL BE INDICATED BY A ONE IN THE EXCEPTIONAL EVENT BIT (BIT 14) OF REGISTER 3 AND A RELEASED RESET KEY WILL BE INDICATED BY A ZERO.

6.9 IN RESPONSE TO A FLUSH COMMAND, THE KEYBOARD SHALL CLEAR ANY INTERNAL FIFO AND SET ANY INTERNAL KEY MATRIX HISTORY RECORD TO AN "ALL KEYS UP" STATE. THIS SHALL RESULT IN THE CODE FOR ANY KEYS WHICH ARE DOWN BEING TRANSMITTED AGAIN.

7.0 KEY ROLLOVER

7.1 TWO-KEY LOCKOUT: IF THERE ARE TWO SIMULTANEOUS VALID KEYS DOWN, SUBSEQUENT KEY DEPRESSIONS WILL BE IGNORED.

7.1.1 ALL KEYS EXCEPT THOSE LISTED IN 7.2 WILL HAVE TWO-KEY LOCKOUT.

7.2 N-KEY ROLLOVER: A KEY DEPRESSION WILL BE ACKNOWLEDGED REGARDLESS OF THE POSITION OF ALL OTHER KEYS.

7.2.1 THE FOLLOWING KEYS WILL HAVE N-KEY ROLLOVER:

CAPS LOCK	(70)
OPEN APPLE	(72)
SHIFT	(53 & 64)
OPTION	(71)
RESET	(81)
CONTROL	(37)

7.2.2 THE RIGHT AND LEFT SHIFT KEYS SHALL BE WIRED IN PARALLEL.

7.2.3 THE KEYBOARD SHALL BE DESIGNED SO THAT THE STATE OF THESE KEYS SHALL BE DETECTED FIRST FOLLOWING A POWER ON RESET, A RESET SIGNAL, OR A FLUSH COMMAND.

7.3 THE CAPS LOCK KEY IS A MECHANICAL ALTERNATE ACTION SWITCH.

7.4 IN ADDITION TO ITS FUNCTION CALLED OUT IN SECTION 6.6, 6.8, AND 7.2, DEPRESSION OF THE RESET SWITCH (NO 81) SHALL CONNECT THE SOFT POWER ON LINE (PIN 2 OF THE CONNECTOR) TO SIGNAL GROUND (PIN 4 OF THE CONNECTOR).

8.0 KEY CODES

8.1 ANY KEY DEPRESSION WILL GENERATE A CODE AS INDICATED IN TABLE 2. RELEASING A KEY WILL GENERATE THE SAME CODE WITH BIT 7 SET (EX. 'S' KEY: DEPRESS= 001H, RELEASE = 081H).

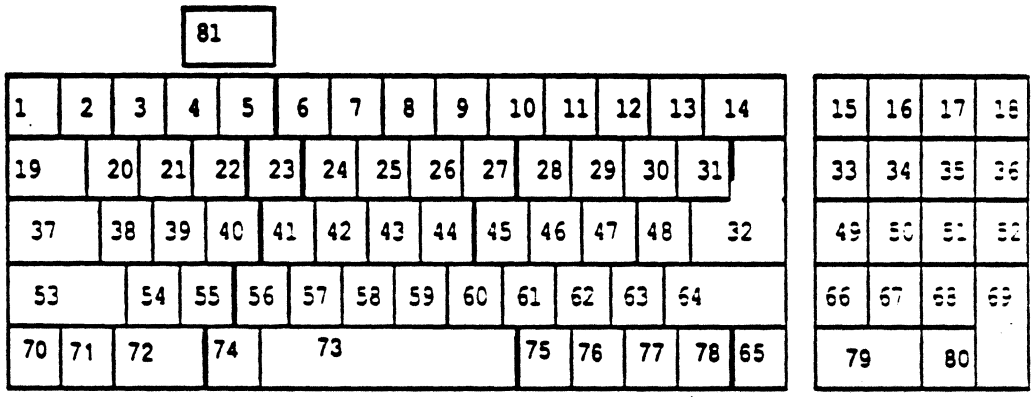


FIGURE 4 KEYSWITCH DESIGNATION

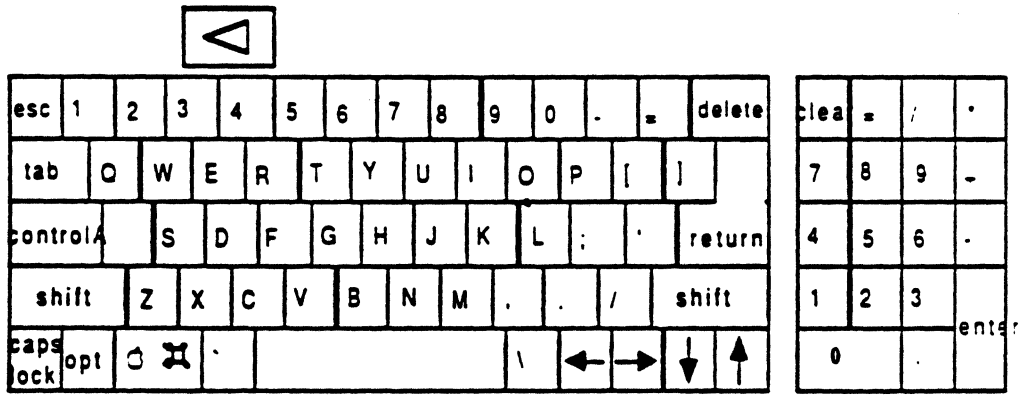


FIGURE 5 U.S. LEGENDS

Apple DeskTop Bus

Macintosh Software Architecture Specification

Revision 1.01

October 27, 1986

騎虎難下

(He who rides a tiger cannot dismount)
-Chinese Proverb

Introduction

The advent of the Apple DeskTop Bus (ADB) hardware on Macintosh machines creates the need for a standard technique for installing devices which use this bus. These devices are likely to be supplied by a third party vendor. This means that device driver software for these devices must be installed dynamically, so that the drivers can be distributed independently of the Macintosh system software.

In addition, the Apple DeskTop Bus supports the standard keyboard and mouse peripherals. To provide maximum flexibility, the ADB standard support software must allow these devices or the drivers which service them to be replaced dynamically.

This document describes the technique which will be used to meet these goals. The intended audience is the development team, management, and third party vendors with a need for early documentation.

Hardware Background

The Apple DeskTop Bus is a simple local area network. This network connects the computer system (master) with up to 16 low-speed input devices. Each device on the network has up to 4 data areas (called registers) which can be read or written over the network. Each register is 2-8 bytes long, and can have different meanings for read and write operations. (The bus can support variable length registers, from 2-8 bytes.).

The Macintosh accesses the network devices through port B of the VIA. Each byte transferred takes approximately 220 microseconds.

Command Format

The ADB uses a polling protocol. The Macintosh must initiate each operation. The network supports 4 operations, called commands. A command is an 8-bit quantity which is sent from the Macintosh to the desired device on the network. The 4

are shown in Figure 1.

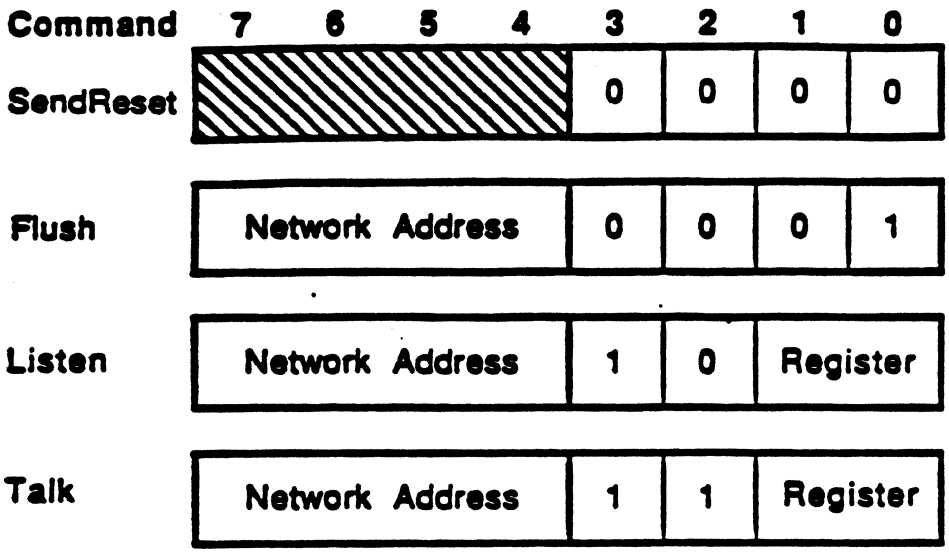


Figure 1. ADB Command Bytes

The SendReset command issues a hardware reset to all devices on the network. The hardware reset clears all pending transactions, and places all network devices in a state in which they will accept commands.

The Flush command performs a device-dependent initialization for a single device. This command is intended to be used for resetting a single device. Any user input stored by the device (such as typeahead in a keyboard device) is discarded.

The Listen command initiates a data transfer from the Macintosh to a network device register. Both the device address and the register number are encoded in the command byte.

The Talk command is the opposite of a listen. Data is transferred from a register in the device to the Macintosh.

All other bit patterns are reserved for future expansion.

Device Registers

Both the listen and talk commands transfer from 2-8 bytes of information between the Macintosh and a register on the network device. Transfers are performed one byte at a time, with the Macintosh taking an interrupt at the end of each byte transfer. Once data from an ADB device has been read by the Macintosh, the data may no longer be available.

Two of the device registers have a standardized format. Device Register 0 is used for interrupt polling. This register, if present in conjunction with an interrupt request (a

"Service Request" in ADB terminology) contains the interrupt data from the device. A talk command to Register 0 will time out if the device is not requesting service. Device Register 3 is an ID register which describes the device type. This register is 16 bits wide, and has the following format:

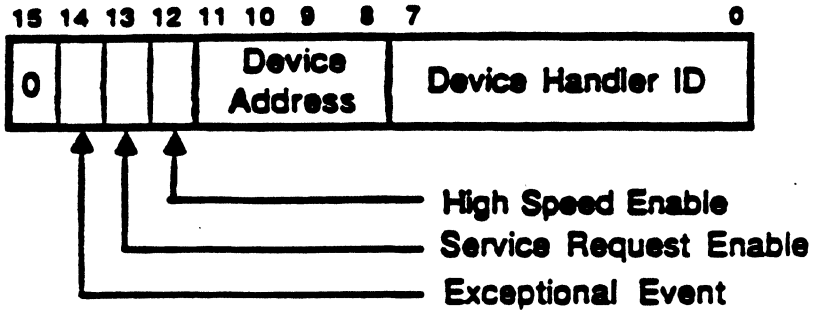


Figure 2. Layout of ADB Device Register 3.

This register may be both read and written (talk'ed and listen'ed) by Macintosh software. The Device Handler ID is basically a signature which indicates the type of device. This quantity may be changed by the host with a listen command. If the device supports the new handler ID, it will appear in subsequent talk commands. Certain values of this field have special meanings. These values have different meanings depending on the command (talk or listen) as follows:

Value	Command	Meaning
00H	Listen	Change only bits 8-13 of Register 3
00H	Talk	Self Test Failure
FEH	Listen	Change address if no collision detected
FDH	Listen	Change address if device switch depressed
FFH	Listen	Initiate device self test

The values 00H, FEH, and FDH on a listen command do not change the value of the device handler field returned by a subsequent talk command. The self-test process changes this field only on test failure.

The Device Address field may be set by the Macintosh with a listen command. This causes the device to appear at a different place on the bus. This field is set to a random pattern on a talk command, to enhance the collision detection feature.

The Exceptional Event bit is a device-dependent flag which can be used by the device and the Macintosh driver to communicate a significant event.

The Service Request Enable bit allows a device to assert the ADB service request line, which causes the Macintosh to (eventually) poll the device for service. See the "Interrupt Mechanism" section below for details on the Service Request below.

The High-Speed Enable bit enables a different (higher speed) modulation technique for the device on the ADB.

Data Transfer Mechanism

The Macintosh transfers data to and from bus devices via the shift register on the VIA . There are two other signal lines called "ST0" and "ST1" which designate to the Apple DeskTop Bus transceiver how the data in the shift register is to be used. These two lines define a state. When the Macintosh changes the value of these two bits, the transceiver initiates a bus transaction. There are four possible states, as follows:

State	Meaning
0	Start a new command
1	Transfer even data byte
2	Transfer odd data byte
3	Idle

State 3 is the initial (power up) state. To execute an ADB command, the Macintosh loads the command byte into the VIA shift register, and sets state 0. Upon getting the shift out interrupt, the Macintosh alternates between states 1 and 2 to transfer the data in or out. An interrupt occurs after each byte is transferred. After the last completion interrupt, the Macintosh sets either state 0 or 3 to complete the command. You can abort a partially executed command by setting the state to 0 at any time.

For a talk command (device to Macintosh), the end of data is indicated by the presence of the Int signal at the end of state 1 or any state 2 after the first state 2.

When in state 3, the transceiver re-executes the last talk command every 16.7 msec. This eliminates the need for the Macintosh to continuously poll the Apple DeskTop Bus to see if a device requires service. In the event that the Macintosh initiates a command while the transceiver contains data from a successful poll, the transceiver will initiate the Int signal at the end of state 0. If the Macintosh proceeds to state 1, it will receive data from the polling operation. The command which the Macintosh attempted to send is discarded, and must be re-issued at the end of the polling data.

Interrupt Mechanism

When a device on the Apple DeskTop Bus needs to present an unsolicited interrupt to the Macintosh, it asserts a System Request (SRQ) line on the bus. This shows up as the Int signal on the Macintosh VIA, at the end of the first state 2 in a command sequence. When the signal is asserted, the Macintosh must then poll each device on the bus to determine whether that device needs service.

The polling mechanism works as follows: The Macintosh will issue a talk command for register 0 on each device on the bus in turn. If a device has data to send, it will respond to the talk command. If the device has no data to send, the transceiver will assert the

Int signal at the end of state 1, indicating that no data was sent.

The presence of data after state 1 (indicated by the lack of an Int signal) means that the device did require service. The Macintosh must retrieve all data from the device before polling the next device. The transceiver will assert the Int signal between state 1 and all but the first state 2 when the data is exhausted. The Int signal will be asserted at the end of the first state 2 if a device is requesting service. A device requesting service will continue generate this signal until the Macintosh issues a talk command for the device's register 0.

Other Considerations

The devices on the Apple DeskTop Bus typically utilize inexpensive (slow) single-chip microprocessors. The same processor typically handles both the external device and the device's ADB interface. The Macintosh must leave the ADB idle at least 50% of the time to allow the external devices time to function.

The Apple DeskTop Bus also supports a feature known as extended addressing. Using this feature, a single ADB address can be used for multiple devices. These devices have a fixed address, from 16 to 64 bits. An extended address device is selected by issuing a listen command to register 2. The device whose address matches the data sent to register 2 becomes selected.

It is also possible to connect several devices to a single non-extended ADB address. The Macintosh code may separate these devices by issuing a talk command to register 3. This will force a collision. The Macintosh should then issue a listen command to register 3 with the special code FE hex in the device handler ID field. If there is more than one device connected to the address specified in the listen command byte, then there is a high probability that only one device will change its address to the value specified in the data field. When performing this operation in software, you must move all the devices from an address to other addresses. To isolate a device to a unique address, you must have moved the device at least 40 times from one address to a free address using the collision detection mechanism.

Adding a device to the Apple DeskTop Bus while the system is running can be disastrous. Connecting the device will, in all likelihood, reset all devices on the bus to their power-up addresses. Worse, there is no way for the Macintosh to tell that this has occurred. Therefore, adding a device to a "hot" system is not supported. Note that the power-on addresses for the keyboard and mouse are not changed by the initialization code to allow a graceful shutdown in this situation. There is currently no way of notifying a Macintosh application, and no plans to support this feature.

Software Overview

The software to support the Apple DeskTop Bus resides in the Macintosh ROM. This code has four components:

- Apple DeskTop Bus Initialization Code

- Apple DeskTop Bus Interrupt and Polling Code
- Universal Keyboard Driver
- Mouse Driver

This code must be designed in such a way as to permit the addition of extra devices in a minimally painful fashion. The software to handle these devices must work with new versions of the Macintosh system software (including ROM code). It must also be possible to replace the keyboard and/or mouse devices and drivers with new devices and drivers without disrupting the rest of the system.

Externally Visible Data Structures

There is only one externally-visible data structure associated with Apple DeskTop Bus support software. This is the device table, placed in the system heap by the ROM code during initialization. This table is shown in Figure 3.

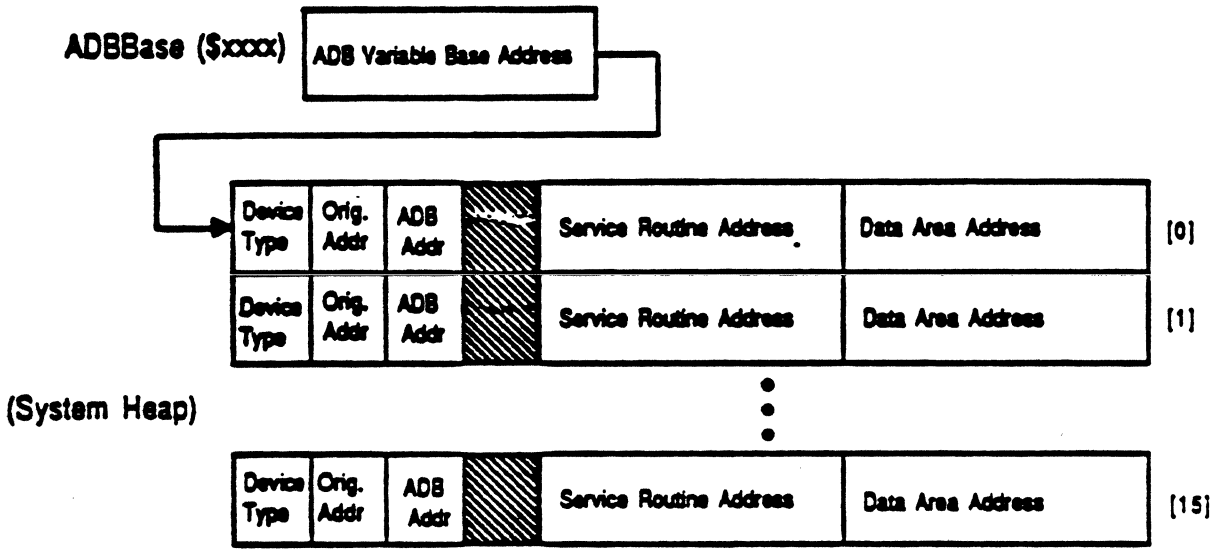


Figure 3. ADB Device Table.

Low memory location "ADBBase" contains the address of this table which is also the base address of the ADB variables. There are 16 entries in the table, corresponding to the 16 possible network addresses. Each entry consists of the Device Type (8 bits), the Original ADB Address (8 bits), the ADB Address (8 bits), one unused byte(8 bits), the Service Routine Address (32 bits), and the Data Area Address. The Device Type field is a copy of the device handler ID from the device's register 3. This field is updated by the driver to reflect any changes made to this field with a listen command to the device. The Original ADB address is the address the device first responsed to. The ADB address is the current Apple DeskTop Bus address of the device. The unused byte is reserved for future use, this byte makes the entries of even length. The Service Routine Address is the address of the code which handles a request for service from the device. See the section on Polling code for the calling sequence for this routine. The Data Area Address is passed to the service routine in

ADB Device Drivers

Two standard drivers are inside the Apple DeskTop Bus Manager. They are the mouse driver and the universal keyboard driver. The mouse driver will be able to support Apple's ADB mouse and the universal keyboard driver will be able to support all Apple's ADB keyboards. All non-Apple ADB mouse or keyboard devices may require its own device driver. All ADB device drivers are put into a new resource called 'ADBS' and it has to be installed inside the System File.

The 'ADBS' resource has two sections: a initialization code section which starts at the beginning of the resource and an optional driver code section. The Start Manager calls the initialization code to set up the driver in a fixed system heap location and update the device table with the Service Routine Address and the Data Area Address. The initialization code should first check if the device it is for is presently connected to the Macintosh by checking the Device Type and the Original ADB Address fields of the device table. If no corresponding entry is found in the table, it should just exit.

Initialization Code.

On power up, a section of code must be executed which will initialize the Apple DeskTop Bus and its associated devices. This code is called by the Start Manager, and performs the following actions:

1. Allocate memory for the ADB device table and set the low memory address to point to the first byte of this table.

2. Initialize the table to binary zeros.

3. Issue a talk command to register 3 on each network address. For all devices which do not time out, place the address and device handler ID in the next slot in the table.

4. Ensure that each address on the network has at most one (non-extended type) device, using the technique described previously. Make a mouse in the system address 3 and the keyboard address 2. If one of these devices does not exist, do not make an entry for it. Place the entries (if any) in the first slots in the table.

5. Initialize the Service routine address for the mouse and keyboard table entries (if any) to point to the proper driver code.

6. Issue a talk register 3 command for the mouse. This command is the auto-poll command until there is any activity from another device.

7. The Start Manager will then call the InitADBDrvr routine which would load the ADBS resources and execute them one by one.

Note that following initialization, the table will contain the standard mouse and keyboard devices. Any other devices connected will have the Service Routine Address field and the Data Area Address updated by the corresponding ADBS resources if they are in the system file, otherwise they will remain uninitialized.

ADB System Calls

Six new OS traps are added to support the Apple DeskTop Bus. They are ADBReInit, ADBOp, CountADBs, GetIndADB, GetADBInfo, and SetADBInfo.

ADBReInit is the call to reinitialize the whole Apple DeskTop Bus. First, the ADB device table is zeroed out, then a Reset command is issued to reset all ADB devices to their original addresses. Then the initialization sequence described above is executed. ADB address for any device cannot be count on to remain the same. No argument is required for this call.

ADBOp is the call to issue an ADB command to any device currently connected. Register D0.B contains the desired command and register A0 is the pointer to the ADBOp paarameter block as shown in figure 4. If the command can be successfully issued, it will return a zero in register D0.B, otherwise a -1 will be returned. The data buffer has to be at least 9 bytes long with the first byte as the length count.

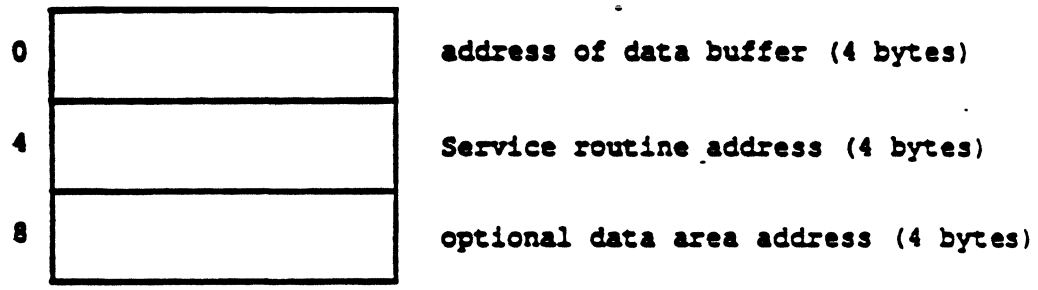


Figure 4. ADBOp Parameter Block

CountADBs is the call to count the number of entries in the device table, no argument is required and the result is returned in register Do.W.

GetIndADB is the call to return information from the device table by the entry index. Register D0.W contains the entry index of the device table, the value can be from 1 to the value returned by CountADBs. Register A0 is a pointer to the ADB Data parameter block (as shown in figure 5) containing fields for device type, original ADB address, service routine address and the data area address. On exit, register D0.B will contain the error code.

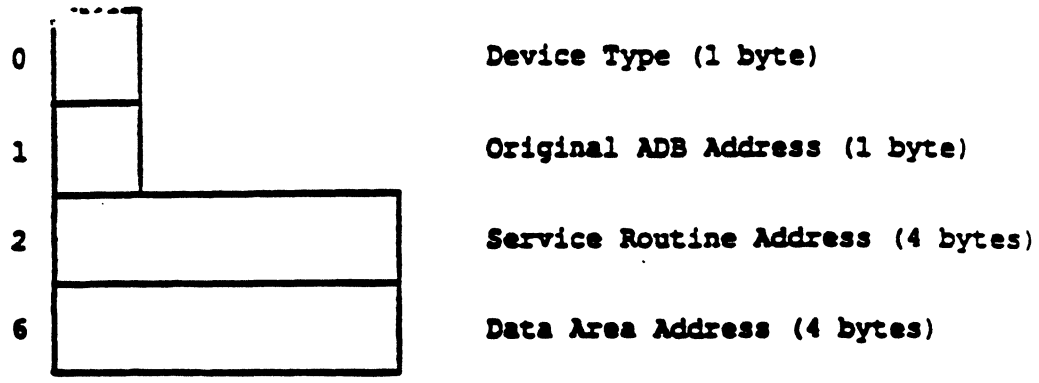


Figure 5. ADB Data Parameter Block

GetADBInfo is the call to return information from thedevice table by the ADB address. Register D0.B contains the ADB address. Register A0 is a pointer to the ADB Data parameter block (as shown in figure 5) containing fields for device type, original ADB address, service routine address and the data area address. On exit, register D0.B will contain the error code.

SetADBInfo is the call to set the service routine address and the data area address in the device table. Register D0.B contains the ADB address. Register A0 is a pointer to the SetInfo parameter block (as shown in figure 6) containing the service routine address and the data area address. On exit, register D0.B will contain the error code.

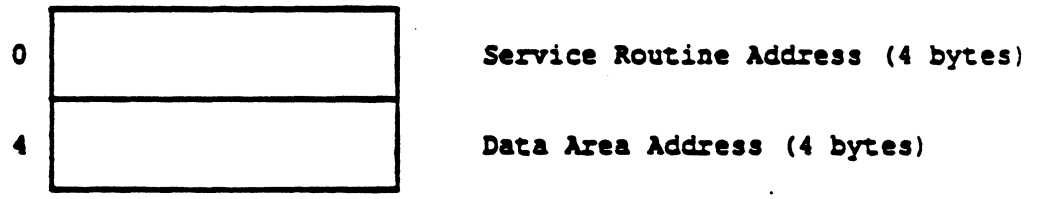


Figure 6. SetInfo Parameter Block

Flow Chart of some important routines

Flow charts for the ADBOp and Shift-Register Interrupt are shown in figures 7 and 8. They are here as a reference only, and the actual implementation is not an exact duplicate of the flow chart.

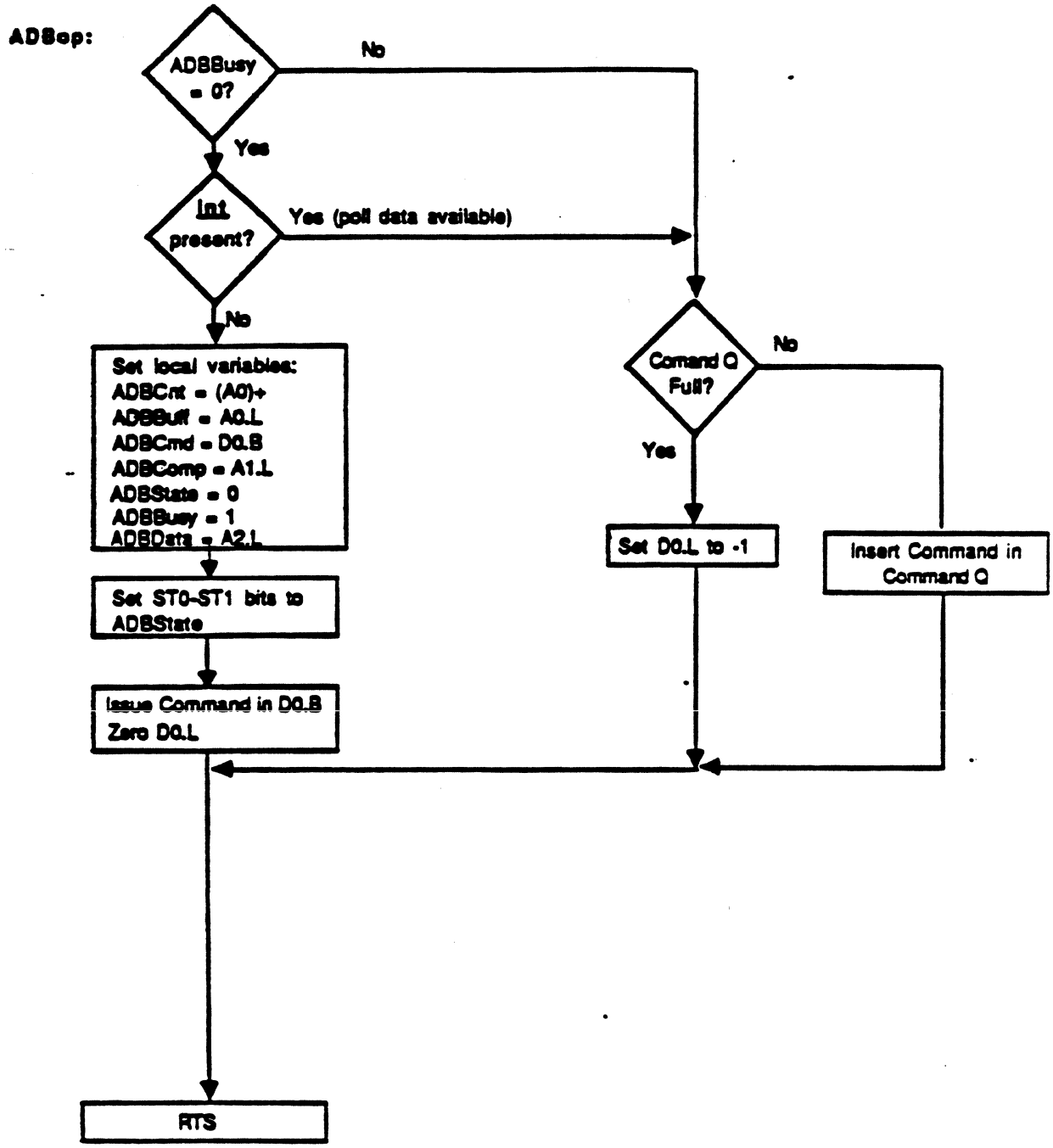


Figure 7. ADBop Flow Chart.

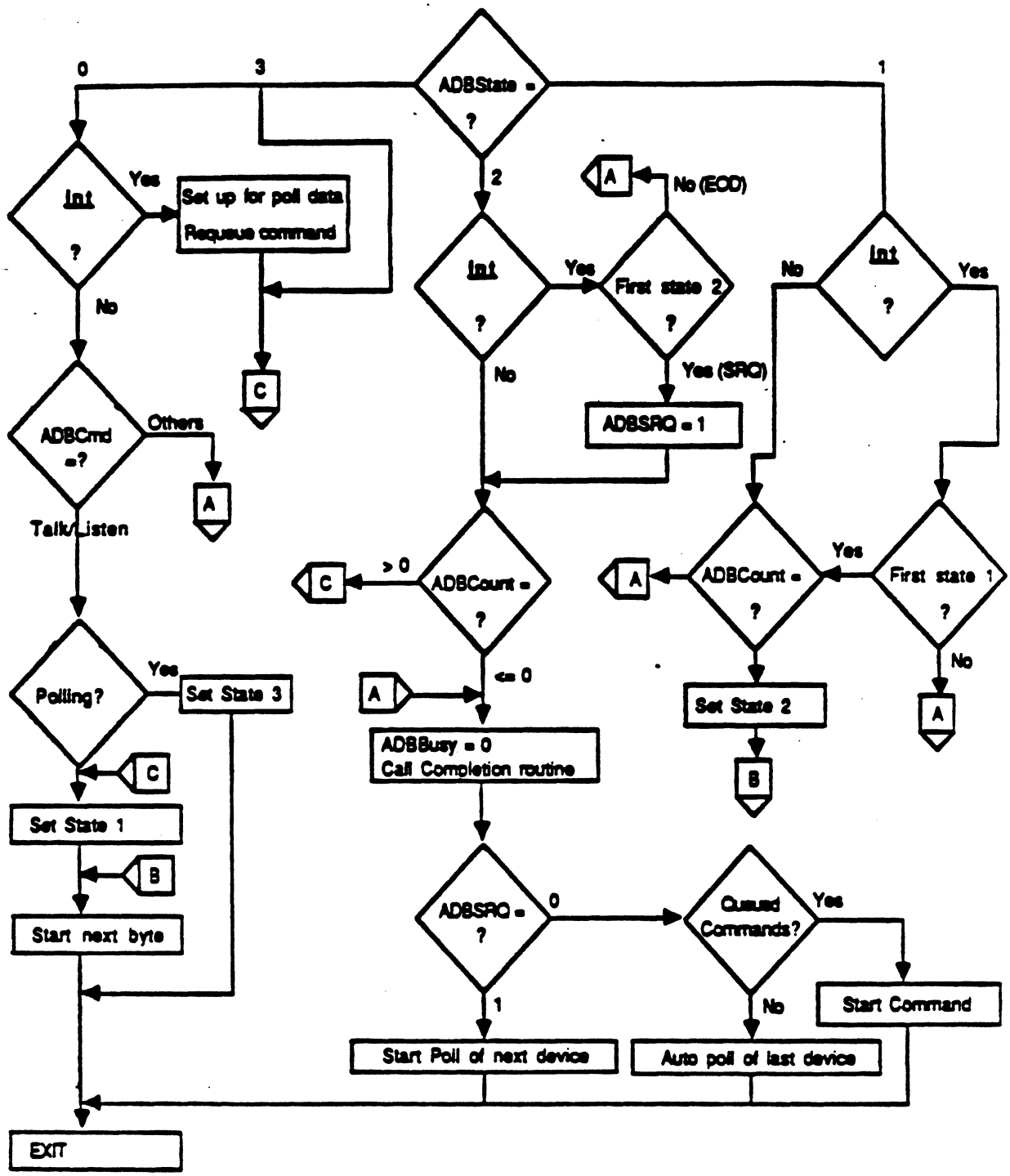


Figure 8. Shift-Register Interrupt Flowchart.

Related Documentation

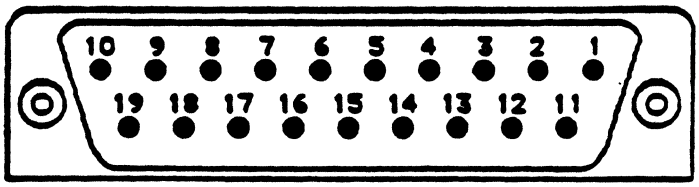
The following documents are helpful in getting a better understanding of the Apple DeskTop Bus:

- FDBDvrB.Asm sample code for Macintosh (Larry Kenyon / Mike Clark, 2/20/86)
- Front Desk Bus Specification (Mike Clark, 2/11/86)
- Macintosh to FDB Transceiver Interface (Mike Clark, 2/24/86)
- Apple DeskTop Bus Specification Rev. D-2 (Bill Marino, 8/13/86)

PART 7

Floppy Disk Interface

Floppy Disk Connector Pinout



1	Ground	11	CA0
2	Ground	12	CA1
3	Ground	13	CA2
4	Ground	14	LSTRB
5	-12 volts	15	Write request
6	+5 volts	16	SEL
7	+12 volts	17	External drive enable
8	+12 volts	18	Read data
9	(not connected)	19	Write data
10	Motor speed control		

PART 8

Serial Ports

Freeport Serial Ports

14 July 1986

The Aladdin extends the capabilities of the Macintosh serial ports, primarily for better support of synchronous modems. This serial port enhancement includes the following:

Production Hardware (DVT-2 and later)

1. Freeport provides an **additional handshake input**, GPi (General Purpose Input), on each serial port. This input is accessible at pin 7 of the mini-8 serial connectors. GPi is received, inverted, at the SCC's DCD/ (Data Carrier Detect) input. On the Macintosh Plus serial connectors, pin 7 is not connected. On the Macintosh Plus and Macintosh 512K, the SCC's DCD/ inputs are used to detect interrupts from the mouse, a function taken over by the Apple DeskTop Bus on Freeport.

2. For port A (the "modem" port) only, a software accessible switch directs either the usual 3.672 MHz clock signal or an **externally supplied clock** to the SCC's RTxCA/ (Receive/Transmit Clock - channel A) input. This switch is set by the VIA's PA3 output: when PA3 is high (1, the default) RTxCA/ receives the 3.672 MHz clock; when PA3 is low (0) RTxCA/ receives the same inverted GPiA signal that appears at the SCC's DCDA/ input. On the Macintosh Plus and Macintosh 512K, the VIA's PA3 is used as an output called SND.PG2/, which selects the alternate sound buffer when low. The alternate sound buffer is not available on Freeport.

DVT-1 Prototype Hardware

The following changes were introduced on the **first-revision Freeport prototypes only**, built in July, 1986. In the interest of backwards compatibility, it was decided to **reverse** these changes (back to the Macintosh Plus definition) for all subsequent revisions, beginning with Rev. 2 Freeport prototypes to be built in August, 1986, for DVT 2.

1. The TXD+ and TXD- (Transmit Data + & -) outputs, accessible at pins 6 and 3 of the mini-8 serial connectors, are enabled by the SCC's DTR/ (Data Terminal Ready) output: if DTR/ is low (0) the TXD outputs are enabled; if DTR/ is high (1) the TXD outputs are placed in a high-impedance state. On the final Freeport, Macintosh Plus and Macintosh 512K, the TXD outputs are enabled by the SCC's RTS/ (Request to Send) output.

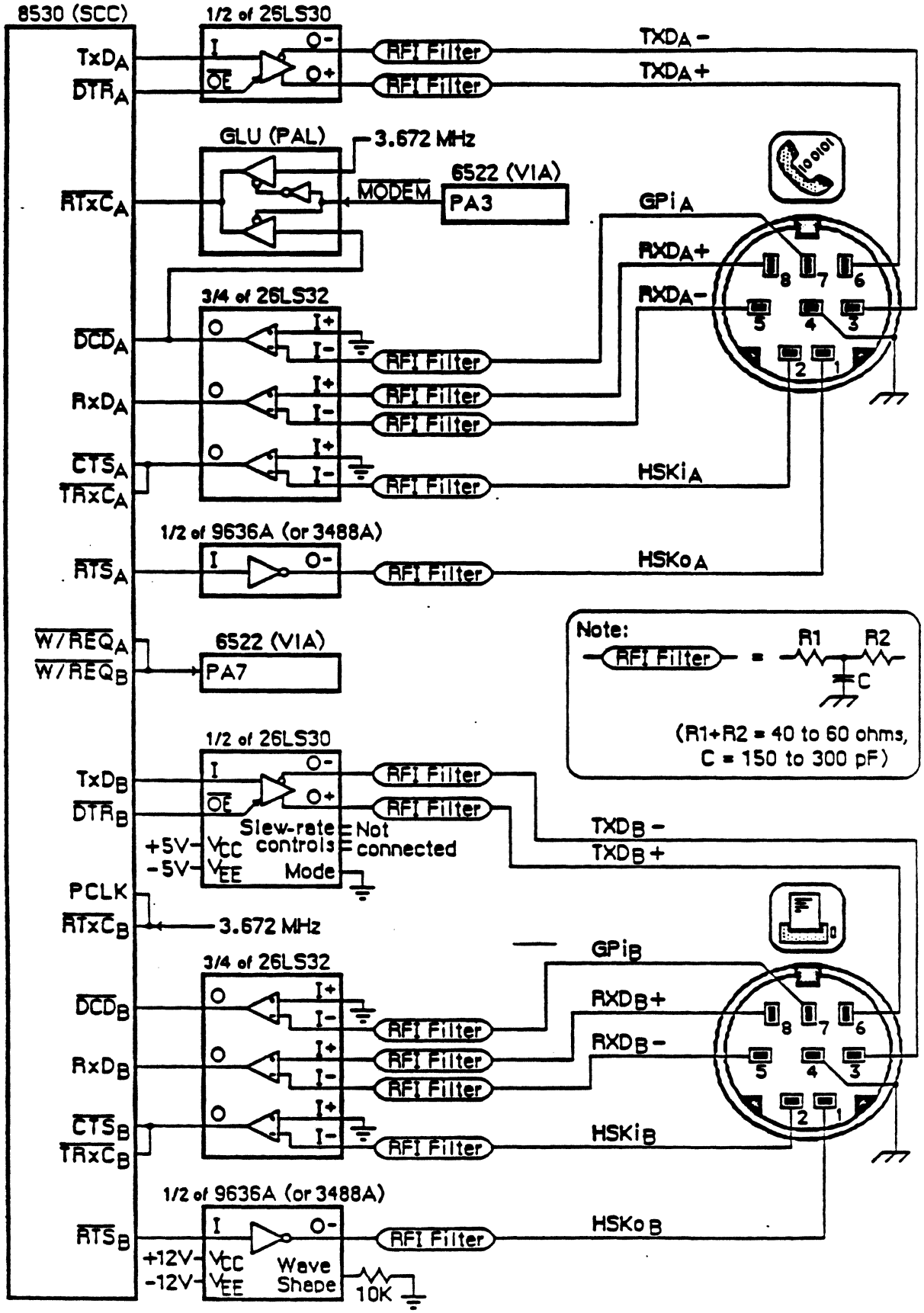
2. HSKo, the Handshake Output accessible at pin 1 of the mini-8 serial connectors, is driven inverted from the SCC's RTS/ (Request to Send) output. On the final Freeport and Macintosh Plus, the HSKo output is driven inverted from the SCC's DTR/ output.

3. HSKi, the Handshake Input accessible at pin 2 of the mini-8 serial connectors, is received **inverted** at the SCC's CTS/ (Clear to Send) and TRxC/ (Transmit/Receive Clock) inputs. On the final Freeport, Macintosh Plus and Macintosh 512K, the HSKi signal is received without inversion.

Here's a quick pin-by-pin comparison of the Freeport, Macintosh Plus,and the Macintosh 512K serial ports.

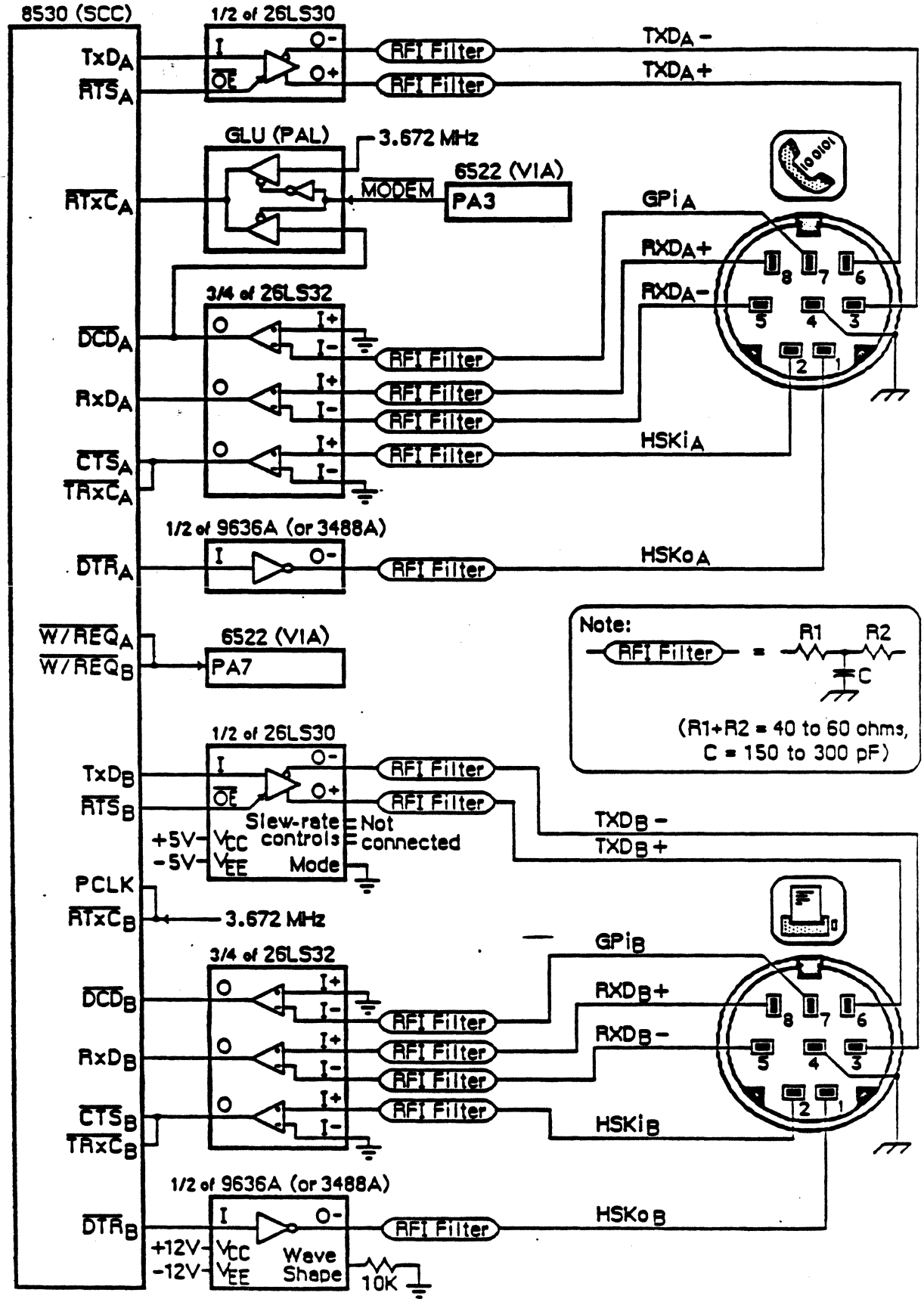
Freeport, All Rev's. Mini-8	**Macintosh Plus** Mini-8	**Macintosh128K/512K** DB-9
Pin 7: GPi, received inverted at DCD/ (on port A, also received at RTxCA/ if VIA's PA3 is set low)	**Pin 7: (Not connected)**	(No General Purpose Input)
Freeport Rev.1, Only Mini-8	**Production Freeport and Macintosh Plus** Mini-8	**Macintosh 128K/512K** DB-9
Pin 1: HSKo, driven inverted from RTS/	**Pin 1: HSKo, driven inverted from DTR/**	(No Handshake Output)
Pin 2: HSKi, received **inverted** at CTS/ and TRxC/	Pin 2: HSKi, received **un-inverted** at CTS/ and TRxC/	Pin 7: HSKi, received un-inverted at CTS/ and TRxC/
Pins 8 & 5: RXD+ & -, received differentially at RxD	Pins 8 & 5: RXD+ & -, received differentially at RxD	Pins 8 & 9: RXD+ & -, received differentially at RxD
Pins 6 & 3: TXD+ & -, driven differentially from TxD; enabled from **DTR/**	Pins 6 & 3: TXD+ & -, driven differentially from TxD; enabled from **RTS/**	Pins 4 & 5: TXD+ & -, driven differentially from TxD; enabled from RTS/
Pin 4 & Shell: Ground	Pin 4 & Shell: Ground	Pins 1, 3, & Shell: Ground
(No +5V supplied)	(No +5V supplied)	Pin 2: +5V
(No +12V supplied)	(No +12V supplied)	Pin 6: +12V

Freeport Rev. 1 Prototype Serial Ports 17 May 1986



Freeport Production Serial Ports

14 July 1986



FREEPORT SUPPLEMENTAL DOCUMENTATION

December, 1986

Introduction

The documentation contained herein will supplement the documentation that you received earlier. All duplicate information contained in this document should supercede all previous documents.

The design of the Freeport is now stable. Changes between DVT2 units (the units you received in early November) and production units will be minor and should not effect your product plans. You should have no reservations about committing to your designs from this point forward. This documentation should accompany the final pre-production prototype Freeport (Called a "PVT" unit).

Changes between the various prototype levels (DVT1, DVT2 and PVT/Production) are all detailed in this document.

Documentation Outline

Three sections are replaced (from the early package): "Differences between Freeport and Macintosh 512K , Macintosh Plus" (Information updated and redistributed to different sections), "Expansion Port Connector" diagram replaced (See amended and enhanced information below), SCSI and ADB software specifications (specifications updated).

This documentation packet includes the following sections:

I. Rom Daugtherboards
II. Changes between DVT1 and DVT2 prototypes
III. Changes between DVT2 and PVT/Production units
IV. New Expansion Features (of Freeport) - Description, Warranty Issues
V. Custom Card Expansion - Features of the 96 pin connector
VI. Disk Drive Expansion - SCSI Hard Disks, 800K Drives
VII. Apple Desktop Bus - Input Device Bus
VIII. Feature Changes From Previous Macintosh Systems
IX. General System Enhancements
X. Power Budget Considerations
XI. Heat Dissipation Guidelines
XII. Memory Map
XIII. System Timing Diagrams
XIV. Mechanical Drawings
XV. Latest SCSI Software Specification
XVI. Latest ADB Software Specification

I. ROM daughterboards

Enclosed with this documentation are a new set of ROMS. Also included is a new System Tools disk. The ROMs will work properly in your PVT units only.

The final Freeport system will ship with 256K of ROM which will plug directly into the ROM sockets on the logic board. Because EPROMs of this size are not readily available, we have provided you with a ROM daughterboard that holds four EPROMs. Taken together, the four EPROMs contain the ROM image of the final 256K Freeport ROM.

Since you may be developing expansion card products which might interfere with the ROM daughterboard, we have also provided you with a set of masked ROMs that are electrically and mechanically identical to the final ROM. However, these ROMs have many known bugs. They are provided for your convenience only.

II. Changes between first (DVT1) and second (DVT2) prototypes

- Serial Ports are now Macintosh Plus compatible (This change was previously detailed in section 8 of the "Freeport Hardware Preliminary Notes").
- 96 Pin expansion connector is reversed and several pins have been changed (See Section V. Custom Card Expansion). However, these changes should not have a major impact on your products.
- Internal SCSI connector has been turned around. Reset feature on drive is now functional.
- Hard drive firmware now supports 2:1 interleave.
- Minor mechanical revisions (See mechanical drawings).

III. Changes between DVT2 and PVT/Production Units

The PVT units you have received are functionally identical to the final production units in every detail except for some appearance changes to the housing (however mechanical size/location features will not change). These units pass FCC emissions standards. The only meaningful differences between DVT2 units and production units will be that PVT units will be the first units to include the SCSI IRQ feature and the removable Accessory Access Port door at the rear.

IV. New Expansion Features

The Freeport includes three new and powerful expansion capabilities. These are: Provisions for an internal custom expansion card, provisions for an internal 3.5 Hard Disk (or Second Internal 800K Drive), and provisions for flexible connections of input devices by way of the Apple Desktop Bus.

The internal expansion features provide logic and power connections as well as a fan for cooling. Third-party products that adhere to the recommended expansion guidelines (power dissipation, mounting, cooling, connections, etc), use the Apple supplied expansion features and do not require physical alteration of the Freeport will not void the Apple Limited Warranty.

V. Custom Card Expansion

The Freeport is the first Macintosh to provide the capability for internal hardware expansion. The Freeport supports one internal expansion card of approximately 4"x8" in size (See included drawings).

Custom card expansion of the Freeport is supported by these features:

- 96 Pin Expansion Connector (Euro-DIN type) that provides power, timing and direct access to the 68000 microprocessor bus.
- Standoff mounting features for physical card support.
- Revised logic board installation and layout features.
- Accessory Access Port for custom external connector support.

96 Pin Connector

The 96-pin Euro-DIN bus connector, on the CPU board, has all of the 68000 signals, plus the 15.6672 MHz system clock, a signal which can tri-state the CPU board's DTACK/ line, +12V, +5V, -5V, and -12V power, and ground.

The majority of the signals on the expansion connector are connected directly to the 68000 microprocessor, with no buffering. See 68000 documentation for additional detail, timing and use.

CHANGES TO 96 Pin Expansion Connector Pinout

The information below applies to DVT2 and later (including production) systems.

In order to accomodate potential future enhancements, several changes have been made to the connector pinout. The changes fall into three categories:

- Label Changed only (seven pins and connector reversed*),
- Label Changed to Reserved (Signals still intact, but could be changed, without notice to support system enhancements - six pins)
- Functional Change (2 Pins)

* While all signals are physically in the same position relative to the logic board, the connector has been physically reversed. The only effect that this has is to renumber the labeling of the pins. The charts below follow the new numbering scheme.

Functional Changes

Pin	Old Description	New Description	Impact
C31	-12V	Spare	Can't Use
C11	Spare	PMCYC/	Adds New Function

Label Changed Only, But Reserved For Possible Future Change

Pin	Old Description	New Description	Impact
B27	E	Reserved	Use Pin A27
B26	A23	Reserved	Use Pin A26
B25	A22	Reserved	Use Pin A25
B24	A21	Reserved	Use Pin A24
B23	A20	Reserved	Use Pin A23
B10	AS/	Reserved	Use Pin C10

Label Changed Only

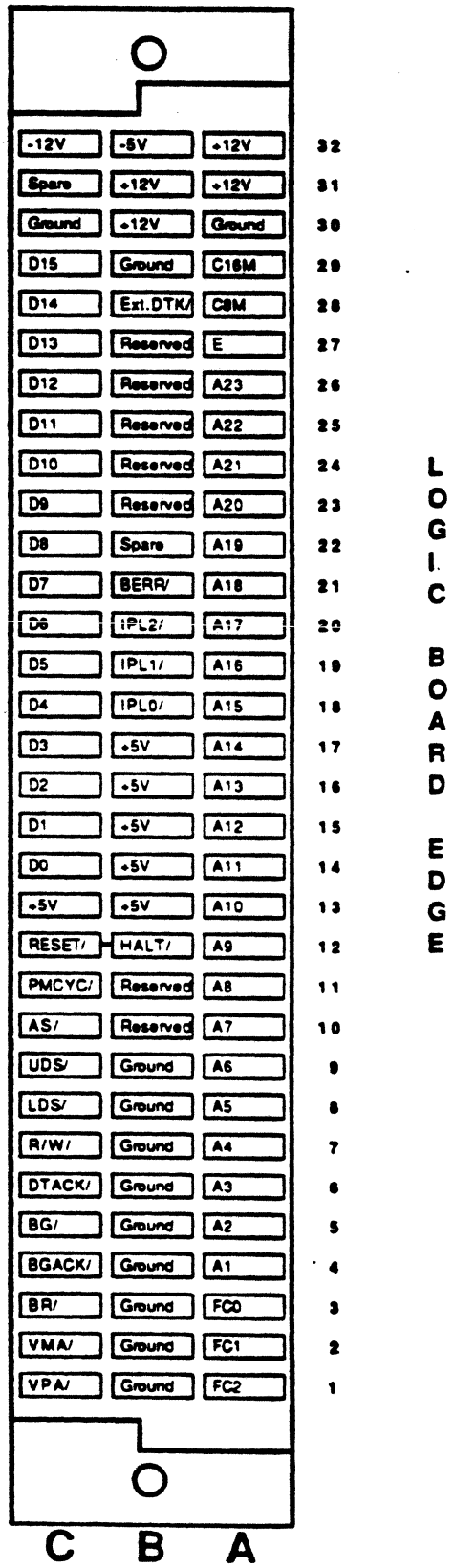
Pin	Old Description	New Description	Impact
C10	AS.CPU/	AS/	None. Labeling Change
B11	Spare	Reserved	None. Labeling Change
A27	E.CPU	E	None. Labeling Change
A26	A23.CPU	A23	None. Labeling Change
A25	A22.CPU	A22	None. Labeling Change
A24	A21.CPU	A21	None. Labeling Change
A23	A20.CPU	A20	None. Labeling Change

Signal by Signal Description

Connector Row	Connector Pin	Signal Name	Signal Description	Input or Output	Loading or Drive Capability (High/ Low)
A	1	FC2	Function Code 2	Output (Input)	Drive: 40 uA/.4 mA, 30 pF (Load: 100 uA/ 100 uA, 50 pF)
A	2	FC1	Function Code 1	Output (Input)	Drive: 40 uA/.4 mA, 30 pF (Load: 100 uA/ 100 uA, 50 pF)
A	3	FC0	Function Code 0	Output (Input)	Drive: 40 uA/.4 mA, 30 pF (Load: 100 uA/ 100 uA, 50 pF)
A	4	A1	Address 1	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	5	A2	Address 2	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	6	A3	Address 3	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	7	A4	Address 4	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	8	A5	Address 5	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	9	A6	Address 6	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	10	A7	Address 7	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	11	A8	Address 8	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	12	A9	Address 9	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	13	A10	Address 10	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	14	A11	Address 11	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	15	A12	Address 12	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	16	A13	Address 13	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	17	A14	Address 14	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	18	A15	Address 15	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	19	A16	Address 16	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	20	A17	Address 17	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF

FREEPORT 96-PIN BUS CONNECTOR

December 1986
(DVT2 and Later Systems)
J13



LOGIC BOARD EDGE

Connector Row	Pin	Signal Name	Signal Description	Input or Output	Loading or Drive Capability (High/ Low)
A	21	A18	Address 18	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	22	A19	Address 19	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	23	A20	Address 20	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	24	A21	Address 21	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	25	A22	Address 22	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	26	A23	Address 23	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
A	27	E	E clock, to main board	Output	Drive: 40 uA/.4 mA, 30 pF (Load: 100 uA/ 100 uA, 50 pF)
A	28	C8M	7.8336 MHz clock	Output	Drive: 20 uA/.2 mA, 20 pF
A	29	C16M	15.6672 MHz clock	Output	Drive: 20 uA/.2 mA, 20 pF
A	30	GND	Logic ground		
A	31	+12V	+12 volts	Output	Drive: 150 mA total, from
A	32	+12V	+12 volts	Output	all +12V pins
B	1	GND	Logic ground		
B	2	GND	Logic ground		
B	3	GND	Logic ground		
B	4	GND	Logic ground		
B	5	GND	Logic ground		
B	6	GND	Logic ground		
B	7	GND	Logic ground		
B	8	GND	Logic ground		
B	9	GND	Logic ground		
B	10	Rsrvd	Reserved		
B	11	Rsrvd	Reserved		
B	12	HALT/	68000 Halt	In/Out	Load: 300 uA/ 6 mA, 50 pF (without RESET/: 50 uA/ 50 uA) Drive: 0 uA/ 0 uA, 30 pF (without RESET/: 40 uA/ .4 mA)
B	13	+5V	+5 volts	Output	
B	14	+5V	+5 volts	Output	
B	15	+5V	+5 volts	Output	Drive:1.5 A total, from all +5V pins
B	16	+5V	+5 volts	Output	

Connector Row	Pin	Signal Name	Signal Description	Input or Output	Loading or Drive Capability (High/ Low)
B	17	+5V	+5 volts	Output	
B	18	IPL0/	Interrupt level 0 (VIA, SCSI.IRQ)	In/Out	Load: 100 uA/ 2 mA, 50 pF Drive: 40 uA/.4 mA, 30 pF (Open collector; 3.3K ohm pullup)
B	19	IPL1/	Interrupt level 1 (SCC)	In/Out	Load: 100 uA/ 2 mA, 50 pF Drive: 40 uA/.4 mA, 30 pF (Open collector; 3.3K ohm pullup)
B	20	IPL2/	Interrupt level 2 (NMI switch)	In/Out	Load: 100 uA/ 2 mA, 50 pF Drive: 40 uA/.4 mA, 30 pF (Open collector; 3.3K ohm pullup)
B	21	BERR/	Bus Error	In/Out	Load: 100 uA/ 2 mA, 50 pF Drive: 40 uA/.4 mA, 30 pF (Open collector; 3.3K ohm pullup)
B	22	Spare	Spare		
B	23	Rsrvd	Reserved		
B	24	Rsrvd	Reserved		
B	25	Rsrvd	Reserved		
B	26	Rsrvd	Reserved		
B	27	Rsrvd	Reserved		
B	28	Ext.DTK/	External DTACK/ (tri-states main board's DTACK/)	Input	Load: 100 uA/ 2 mA, 50 pF (3.3K ohm pullup)
B	29	GND	Logic ground		
B	30	+12V	+12 volts	Output	Drive: 150 mA total, from
B	31	+12V	+12 volts	Output	all +12V pins
B	32	-5V	-5 volts	Output	Drive: 100 mA
C	1	VPA/	Valid Periph. Address	Output	Drive: 40 uA/.4 mA, 30 pF
C	2	VMA/	Valid Memory Address	Output (Input)	Drive: 40 uA/.4 mA, 30 pF (Load: 100 uA/ 100 uA, 50 pF)
C	3	BR/	Bus Request	Input	Load: 100 uA/ 2 mA, 50 pF (3.3K ohm pullup)
C	4	BGACK/	Bus Grant Acknowledge	Input	Load: 100 uA/ 2 mA, 50 pF (3.3K ohm pullup)

Connector Row	Pin	Signal Name	Signal Description	Input or Output	Loading or Drive Capability (High/ Low)
C	5	BG/	Bus Grant	Output	Drive: 40 uA/.4 mA, 30 pF
C	6	DTACK/	Data Transfer Acknowledge	In/Out	Load: 100 uA/ 2 mA, 50 pF Drive: 40 uA/.4 mA, 30 pF (Ext.DTK/ low tri-states main board's DTACK/; 3.3K ohm pullup)
C	7	R/W/	Read/Write	Output (Input)	Drive: 40 uA/.4 mA, 30 pF (Load: 200 uA/ 2 mA, 50 pF)
C	8	LDS/	Lower Data Strobe	Output (Input)	Drive: 40 uA/.4 mA, 30 pF (Load: 100 uA/ 1 mA, 50 pF)
C	9	UDS/	Upper Data Strobe	Output (Input)	Drive: 40 uA/.4 mA, 30 pF (Load: 100 uA/ 1 mA, 50 pF)
C	10	AS/	Address Strobe, to main board	Output (Input)	Drive: 40 uA/.4 mA, 30 pF (Load: 200 uA/ 3.2 mA, 50 pF; 3.3K ohm pullup)
C	11	PMCYC/	Processor Memory Cycle	Output	Drive: 40 uA/.4 mA, 30 pF (High during video access to RAM)
C	12	RESET/	Reset	In/Out	Load: 300 uA/ 6 mA, 50 pF Drive: 40 uA/ .4 mA (Open collector; 1K ohm pullup)
C	13	+5V	+5 volts	Output	Drive: 1.5 A total, from all +5V pins
C	14	D0	Data bus, bit 0	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	15	D1	Data bus, bit 1	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	16	D2	Data bus, bit 2	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	17	D3	Data bus, bit 3	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	18	D4	Data bus, bit 4	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	19	D5	Data bus, bit 5	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	20	D6	Data bus, bit 6	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	21	D7	Data bus, bit 7	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF

Connector Row	Pin	Signal Name	Signal Description	Input or Output	Loading or Drive Capability (High/ Low)
C	22	D8	Data bus, bit 8	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	23	D9	Data bus, bit 9	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	24	D10	Data bus, bit 10	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	25	D11	Data bus, bit 11	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	26	D12	Data bus, bit 12	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	27	D13	Data bus, bit 13	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	28	D14	Data bus, bit 14	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	29	D15	Data bus, bit 15	In/Out	Load: 250 uA/ 1 mA, 100 pF Drive: 40 uA/.4 mA, 30 pF
C	30	GND	Logic ground		
C	31	Spare	Spare		
C	32	-12V	-12 volts	Output	Drive: 100 mA

Notes on Bus Loading/Driving:
The following lines are pulled high, using 3.3K ohms to +5V, so that they go to a known level when the lines are put in a high-impedance state: AS/, DTACK/, EXT.DTACK/, IPL0/, IPL1/, IPL2/, BR/, BGACK/, BERR/. The following lines are pulled high using 1.0K ohms to +5V: RESET/, HALT/. The DC load and drive specifications are indicated in the format "signal-high/signal-low."

The C8M and C16M clock outputs are specified to drive one 74LS input (a standard 74LS input load is 20 uA high, .2 mA low). All other outputs have been specified to drive two 74LS inputs.

The terms "Input" and "Output" are defined relative to the Freeport main logic board.

Where (Input) is in parentheses, the pin carries a signal which is usually an output driven by the 68000, but which is put in a high-impedance state by the 68000 after responding to a Bus Request. When put in a high-impedance state by the 68000, this pin may be driven as an input from the 96-pin connector.

Additional Signal Description:

FC0-FC2	- 68000 Function Code lines.
A1-A23	- 68000 Address lines.
E	- 68000 E Clock
C8M	- Microprocessor clock = 7.8336 MHz = C16M divided by 2.
C16M	- Gate Array Clock = 15.6672MHz.
HALT/	- 68000 Halt. Wired directly to RESET/.
IPL0/-IPL2/	- 68000 Interrupt Priority Level lines.
BERR/	- 68000 Bus Error. Generated by gate array due to SCSI access timeout. See "General Enhancements Section" of this document, Section 3.
Ext.DTK/	- Pull low to put the Gate Array generated DTACK/ into a high-impedance state. The expansion board is then responsible for generating the DTACK/ signal (as an output to the microprocessor, through the DTACK/ signal line).
VPA/	- 68000 Valid Peripheral Address. Supplied to 68000. For Freeport, VPA space is $E0 0000 to $FF FFFF.
VMA/	- 68000 Valid Memory Address.
BR/	- 68000 Bus Request.
BGACK/	- 68000 Bus Grant Acknowledge.
BG/	- 68000 Bus Grant.
DTACK/	- 68000 Data Transfer Acknowledge. Inserts wait states until data bus is available. Normally supplied by the gate array. Gate array generation of DTACK/ can be suppressed (put into a high-impedance state) by pulling the EXT.DTACK/ line low; this allows DTACK/ to be externally generated by an add-on device. DTACK/ is not supplied for accesses to VPA space, is held off to separate 2 successive accesses to the SCC and is held off during RAM access by video.
R/W/	- 68000 Read/Write.
LDS/	- 68000 Lower Data Strobe.
UDS/	- 68000 Upper Data Strobe.
AS/	- 68000 Address Strobe.
PMCYC/	- Processor-Memory Cycle. Used to synchronize with the gate array for RAM accesses. PMCYC/ is low when RAM is available for microprocessor accesses and is high during video accesses. PMCYC/ is always high during S0. See attached timing diagrams.
RESET/	- 68000 Reset. Wired directly to HALT/.
D0-D15	- 68000 Data Bus.

Physical Mounting Features

Two mounting holes are provided on the CPU board, for standoffs, to mechanically hold an expansion board in place. (See Mechanical Drawings and Logic Board itself)

Logic Board Installation Features

The CPU board has been altered so that it can be fastened into the chassis without sliding in from the rear, as on the Macintosh 512K and Macintosh Plus. This feature will accommodate the extra height of a CPU board with an expansion board mounted on top of it. In addition, to leave more room for mounting components on the bottom side of an expansion board, the SIMM sockets have been placed side by side, at the extreme front edge of the CPU board.

Installation and removal of the Freeport logic board is accomplished by sliding the board out, about one-half inch, along the rails. The slotted side of the logic board then swings out for removal.

Accessory Access Port

The Accessory Access Port provides connector mounting features and out-of-case connector access to external peripherals (e.g. external monitor, telephone line, disk drive, local area network, etc). Mounting features are provided by a bracket at the rear of the chassis. Out-of-case access is provided by a removable plastic door (door not included on DVT2 systems).

The Connector Bracket will shield a third-party supplied connector and physically support a Connector Mounting Card. A Connector Mounting Card is a PCB that holds the custom connector and could also contain some electronic components, if necessary. Developers should pay close attention to EMI, heat, CRT interaction and hard drive interaction when placing components on this card.

The removable plastic door is similar to the battery door on previous Macintosh systems, however it can only be removed from the inside of the case. Developers may choose to replace the plastic door with one that has a cut-out for their custom connector. It is also acceptable to have no replacement plastic insert, **provided that the entire case opening is blocked or covered, from the inside**, to prevent inadvertent access to the high voltages inside of the case.

VI. Disk Drive Expansion

The Freeport provides the capability to add an internal 3.5 SCSI hard disk or second internal 800K drive.

Add-on disk drive support of the Freeport is supported by these features:

- A standard 50-pin SCSI connector on the logic board.
- A standard 4-pin hard disk power connector.
- A front-mounted hard disk activity lens.
- IRQ line support for asynchronous transfers.
- Improved hardware handshaking.
- Second internal IWM connector.

INTERNAL HARD DISK SUPPORT

50-pin SCSI Connector

Details in SCSI documentation.

4-Pin Hard Disk Power Connection

See manufacturer's hard disk documentation.

Front-Mounted Activity Lens

See drawings.

Asynchronous Transfers

A CPU interrupt from the SCSI IRQ line has been added to support asynchronous SCSI operations. On production Freeports (not on DVT1 or DVT2), the SCSI chip's IRQ line can generate a level 1 interrupt (the same level as the VIA interrupt) when the IRQ goes high, indicating that the NCR5380 (SCSI chip) has detected one of the conditions for IRQ (see NCR5380 documentation for details). This interrupt is normally masked, but it can be enabled by setting the VIA's PB6 output low (while waiting for the first byte of a block transfer to arrive, for instance).

Hardware Handshaking

Hardware handshaking to the SCSI port has been improved. On Macintosh Plus, a data strobe (DTACK/=0) is sent to the CPU whenever the SCSI chip is addressed. On Freeport when accessing SCSI in DMA mode (address bit A9=1), DACK/ is not sent to the SCSI chip, and DTACK/ is not sent to the CPU, until the SCSI chip's DRQ line goes high, indicating that a byte of data has been received or transmitted. If DTACK/ is not set low for 265 milliseconds after AS/ goes low, a bus error (BERR/= 0) is sent to the CPU. [Actually, BERR/ may be generated at any time greater than 265 mS, and is certain to have been generated by the time DTACK/ has been held off for 284 mS.]

Second Internal 800K Drive

On Macintosh 512K and Macintosh Plus, the IWM's ENBL1/ signal enables the internal floppy disk for reading or writing. On Freeport, ENBL1/ has been further decoded to provide two enable lines: one enables the lower internal drive, which is always present, while the other enables the optional, upper internal drive. A bit in the VIA (DRIVE1B/, on PA4) selects between the two internal drives. When DRIVE1B/ is high (the default: PA4=1), ENBL1/ enables the lower drive, while setting DRIVE1B/ low (PA4=0) allows ENBL1/ to select the upper drive.

VII. Apple Desktop Bus

The Apple Desktop Bus is a flexible input bus that provides the capability for concurrent connection of multiple input devices. The Freeport includes two Apple Desktop Bus connectors that can be used interchangeably. The two connectors on the keyboard can be used to connect the keyboard to the system and to daisy-chain another device. See Apple Desktop Bus documentation for details.

VIII. Feature Changes From Previous Macintosh Systems

As with any new system, some old features have been changed to support new features. These changes are detailed below.

1. **The alternate sound/disk-speed buffer is not available on Freeport.** On Macintosh 512K and Macintosh Plus, this buffer was accessed by setting SND.PG2/ (VIA's PA3) low. On Freeport, the VIA's PA3 is used for MODEM/ (see Freeport Serial Ports document).

2. **The horizontal retrace input to the VIA is not available on Freeport.** On Macintosh 512K and Macintosh Plus, this input was called H4, and was received at the VIA's PB6 input. It allowed a program to count horizontal screen lines. On Freeport, the VIA's PB6 is used as an output, to mask SCSI IRQ interrupts (see the SCSI discussion).

3. **The OVERLAY function is handled automatically on Freeport.** OVERLAY causes ROM to appear at the bottom of memory, in addition to its usual location at $400000, when first booting the machine. Later on, RAM is re-mapped to appear at the bottom of memory. On Macintosh 512K and Macintosh Plus, this function was under software control, through the VIA's PA4. When OVERLAY was high (the default: PA4=1), ROM was at the bottom of memory. When OVERLAY was set low (PA4=0), RAM was at the bottom. On Freeport, ROM is at the bottom of memory at power-on, but the first access to the $400000-$5FFFFF space automatically re-maps RAM to the bottom of memory. The VIA's PA4 is now used for selecting between two internal floppy disk drives (see section Disk Drive Expansion, above).

4. **The positions of certain components have been changed.** Of possible interest to various hardware developers for Macintosh: the locations of the SIMM sockets have changed (they are now side by side, at the extreme front edge of the CPU board), and the ROMs and the CPU are also in slightly altered positions, compared to a Macintosh 512K or Macintosh Plus.

IX. General Enhancements

Several system enhancements have been made to Freeport. They include:

1. **Speed of operation out of RAM has been improved.** On Macintosh 512K and Macintosh Plus, during the display of a horizontal line on the video screen the CPU and the video are given alternating accesses to RAM, so that the CPU's use of RAM slows to 50% of the maximum rate. On Freeport every other video access point is given back to the CPU, and the video takes a double word at each remaining video access point, to make up. This gives the CPU three accesses to every one for video during a horizontal line, and the CPU can run at 75% of the maximum rate. This results in an average increase in overall speed of approximately 16%, more for RAM only tasks. Software timing loops written for Macintosh 512K and Macintosh Plus may have to be adjusted to work correctly on Freeport.

2. **More address ranges in the memory map are available for use by other hardware.** Through additional decoding in Freeport, memory map spaces have been recovered which were off limits in the Macintosh 512K because they were used for Phase Read or because they turned on multiple devices at once. These spaces include the ranges $800000 - $8FFFFF, $A00000 - $AFFFFF, $C00000 - $CFFFFF, $E00000 - $E7FFFF, and $F00000 - $F7FFFF.

Note: On DVT1 Freeport units (only), the address space $600000-$7FFFFF contains a duplicate image of the upper row of RAM. On Mac 512, MacPlus and on production Freeport units, that space is available for use by other hardware after startup.

3. **Hardware handshaking to the SCC has been improved.** On Macintosh 512K and Macintosh Plus, it was possible for consecutive SCC accesses to follow each other so quickly that the SCC specification was violated. This required a software delay between such accesses. On Freeport, hardware delays an SCC access if it attempts to follow the previous access in less than 2.25 microseconds.

4. **Timing phase adjustment is eliminated on Freeport.** On Macintosh 512K and Macintosh Plus, the high-frequency CPU timing was adjusted at boot time, using Phase Read and word-wide accesses to the SCC. This adjustment is not necessary on Freeport.

5. **Serial Ports.** The serial ports have been enhanced with the addition of a backwards compatible handshake line. See serial port documentaion.

6. **Battery changed.** On Mac 512 and Plus, the real-time clock and parameter RAM were powered by a rechargeable NiCad battery which could be replaced through a door on the back of the Macintosh case. On Freeport, a lithium battery provides this function; it is soldered onto the main logic board and has an estimated life of at least seven years. The Freeport case does not have a battery door.

X. Power Budget Considerations

The capacity of the power supply has been increased to support the requirements of an expansion board, internal hard disk, etc. This increased power is budgeted approximately as follows:

Freeport Device	Amps at +5V	Amps at -5V	Amps at +12V	Amps at -12V
DeskTop Bus	0.5			
Internal SCSI Hard Disk	1.5		0.9	
Expansion Board	1.5	0.1	0.15	0.1

Notes:

The supply will support a surge of an additional 2 Amps at +12V for up to 10 Seconds. This is provided to accomodate required startup currents for the internal hard disk.

XI. Heat Dissipation Guidelines

Freeport expansion cards, by their own heat dissipation, will change the overall temperature profile of the CPU product. Because excessive heat can have a detrimental effect on product performance and reliability, we recommend the following as guidelines:

1. Optimum cooling for both the logic and expansion boards can be achieved by positioning the expansion card as far above the logic board as possible (without running into the chassis - the maximum possible is 16.5mm). In addition, placing components on the top side of the expansion board is optimal.

2. Hot components should be placed away from the front bezel. This provides for better cooling by the air flow from the fan.

3. Dissipation by the expansion board of up to 7.5 watts of power provides a comfortable margin for the major product components. Dissipation of more than 7.5 watts of power may cause excessive temperature rise on certain critical components. Our studies indicate that at an ambient temperature of about 24°C, 7.5 watts of dissipated power from the expansion board will cause an acceptable rise to about 53°C on the CPU components located directly under the expansion card (Studies conducted with internal hard drive installed).

4. Components placed on a connector board mounted to the Accessory Access Port features should cool without significant impact to the rest of the product.

5. The CPU components to be most concerned with include the 68000 and the DRAM modules.

6. Disk products should not cause an inside the box ambient temperature rise of more than 15°C over external ambient air temperature.

7. Installation of an expansion board should not cause the case temperature of the hard disk to rise more than 15° C over external ambient air temperature.

Memory Map and Address Decodes

The main purpose of the address decoder is to generate chip selects for different address spaces. The address space is divided into 16 equal spaces. There are two different address space maps depending on OVERLAY. OVERLAY is a node internal to the gate array. It is set by RESET/ and cleared by addressing normal ROM space. (Specifically cleared by 400000 - 5FFFFF.) The table below shows the address mapping. axxxxx indicates the hex address. For example 3xxxxx means any address in the range 300000-3FFFFF (A23=0, A22=0, A21=1, A20=1, and A19-A0 any value).

MEMORY MAP

Address Range	Overlay=0	Overlay=1	Other Requirements	
0x xxxx	RAM	ROM	ROM if R/W=1	
1x xxxx	RAM			
2x xxxx	RAM			
3x xxxx	RAM			
4x xxxx	ROM	ROM	ROM if R/W =1	
5x xxxx	SCSI	SCSI	A19=1	note 1
6x xxxx		RAM		
7x xxxx		RAM		
8x xxxx				
9x xxxx	SCC	SCC		note 2
Ax xxxx	EXP.EN	EXP.EN	A19=1, A17=1	
Bx xxxx	SCC	SCC		note 3
Cx xxxx				
Dx xxxx	IWM	IWM		
Ex xxxx	VPA, VIA	VPA, VIA	VIA if A19=1	note 4
Fx xxxx	VPA	VPA		

Note 1: If A9=0 then the operation is a normal SCSI access:
SCSI/=0, DACK/=1, DTACK/ functions normally.
If A9=1 then the operation is a pseudo-DMA access:
SCSI/=1, DACK/= DTACK/, DTACK/ waits for SCSI.DRQ=1.

Note 2: If R/W =1 and LDS/=1, then read SCC.
If R/W =1 and LDS/=0, then reset SCC.

Note 3: If R/W =0 and LDS/=0, then write SCC.

Note 4: VIA **does not require AS/**

Address Decodes (cont)

Address space 9xxxxx with R/W =1 and LDS/=1 is for SCC Read. Address space Bxxxxx with R/W =0 and LDS/=0 is for SCC Write. Address space 9xxxxx with R/W =1 and LDS/=0 is for hardware reset of the SCC. Read modify write instructions like BCLR are not legal (also not legal in MAC) since the address space for reads is different from the address space for writes.

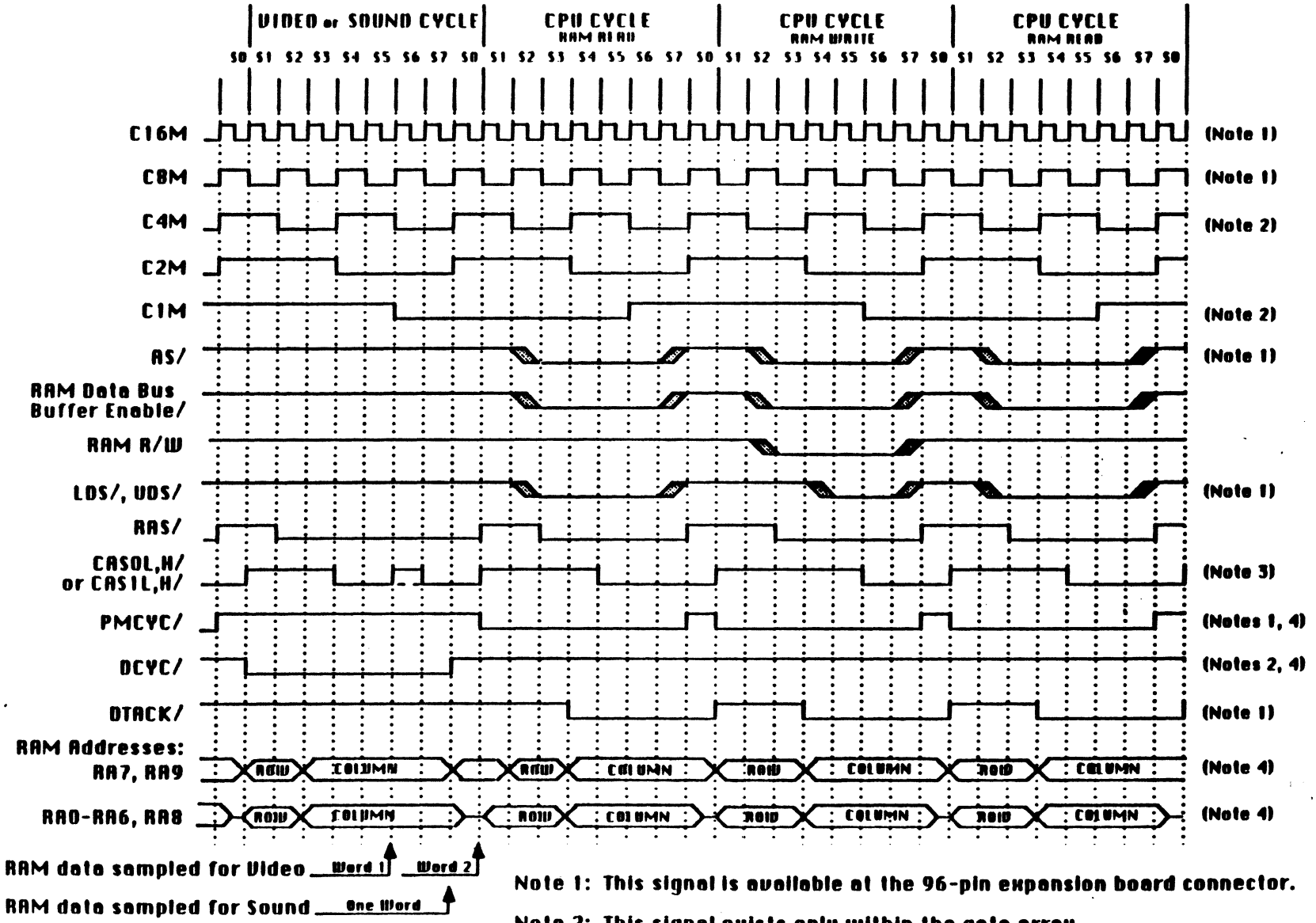
The timing for SCC decodes is complicated. DTACK/ is returned 8 clocks later than it would be normally. This additional 500 ns is required for the long access time of the SCC. If doing an SCC Read, SCCRD/ falls 125 ns after SCCEN/ (the SCC's CE/) falls. Delays in the gate array keep SCCEN/ from rising until slightly after SCCRD/ rises (due to AS/ rising). If doing an SCC Write, IOW/ (the SCC's WR/) falls 125 ns after SCCEN/ falls. Delays in the gate array keep SCCEN/ from rising until slightly after IOW/ rises (due to AS/ rising). In addition, hardware prevents two SCC accesses from being too close together. An SCCEN/ falling will be held off (and no DTACK/ returned) for 36 cycles after the first SCC operation finishes with SCCEN/ rising.

SCSI write operations require R/W =0. Read modify write instructions like BCLR are not legal (also not legal in MAC) since the data strobe for reads is different from the data strobe for writes (the SCSI's IOR/ is driven by UDS/). The timing for the SCSI write operation involves IOW/. IOW/ falls due to R/W falling (S2). IOW/ rises during S6. This early ending of the write is done to meet the data hold requirement of the SCSI chip.

DTACK/ falls on multiples of 4 clocks (S0,S4) and rises 5 clocks later. It may be held off in some address spaces. Space E00000-FFFFFF is VPA space and does not return DTACK/. SCC space (9xxxxx or Bxxxxx) holds off DTACK/ for 8 clocks longer than normal. In addition the hold off between two SCC accesses holds off DTACK/ until the time-out occurs. RAM accesses are restricted to occur on 8 clock boundries so DTACK/ falls only on (S4) and only for valid RAM operations with AS/ low. In addition, RAM accesses which occur during video or sound cycles are held off until the video or sound DMA cycle completes. For SCSI operations in pseudo-DMA mode, DTACK/ is not returned until the next occurance of the time slot (S0,S4) after SCSI.DRQ=1. DTACK/ can be tri-stated by holding EXT.DTK/ low.

EN245/ enables the tranceivers which connect the RAM data bus to the microprocessor data bus during RAM operations. Microprocessor RAM operations which are held off during video/sound cycles have EN245/ disabled during the video/sound cycle.

Timing of Video and 68000 Accesses to Freeport RAM



Note 1: This signal is available at the 96-pin expansion board connector.

Note 2: This signal exists only within the gate array.

Note 3: In a Sound cycle, CAS/ remains low during S6 (shown by dashed line).

Note 4: If DCYC/ is low, gate array supplies RA0-6,8 ; if PMCYC/ is low, F257's supply RA0-6,8. Gate array always supplies RA7,9.

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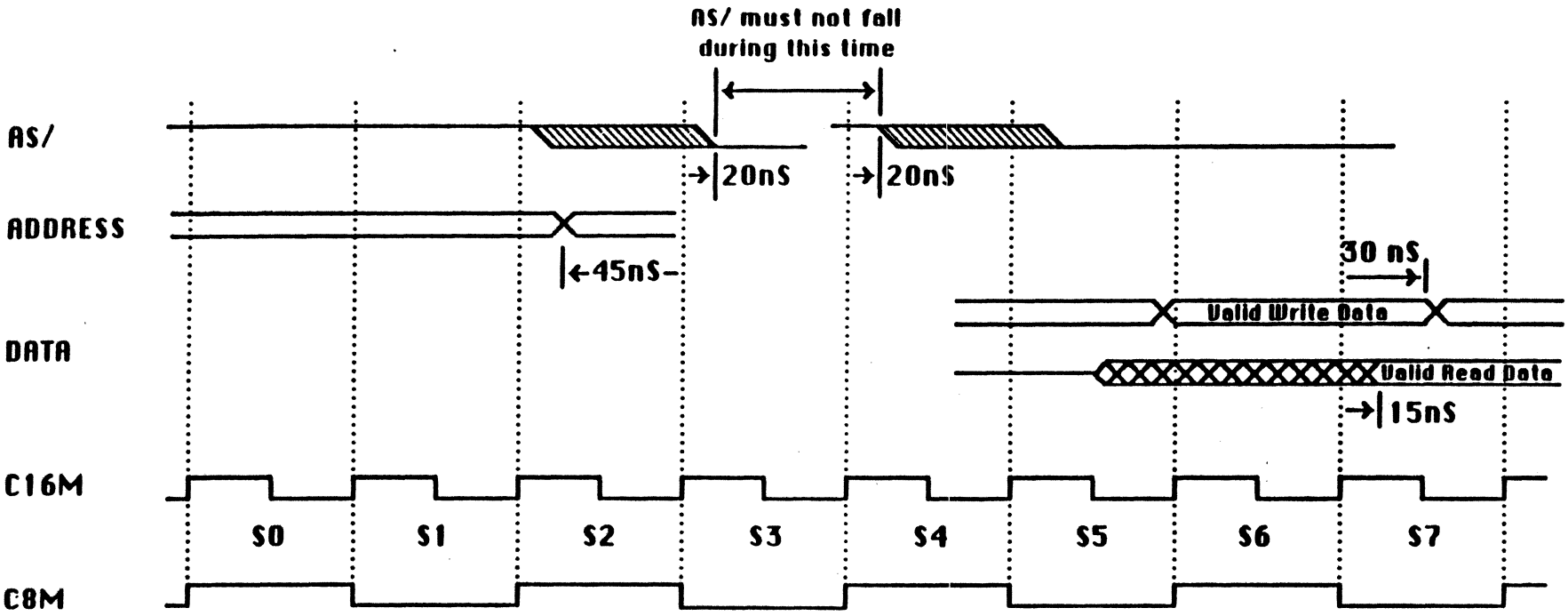
Reading and Writing Freeport RAM from an Expansion Board



(Note: C8M shown for reference to state sequence, only.
Actual C8M is delayed from C16M by up to 30 nS.)

Minimum ADDRESS setup time to AS/ is 15nS.

Minimum AS/ hold time after ADDRESS becomes valid is 15nS.

Minimum ADDRESS setup time to start of S3 is 45nS unless AS/ falls after start of S3, in which case minimum ADDRESS setup time to AS/ is 45nS.

AS/ falling must occur not later than 20nS into S3. If AS/ has not fallen by that time, AS/ must not fall until after the first 20nS of S4 (data will be read or written in the next RAM access).

DTACK/ rises 25nS maximum following start of an odd S-state after AS/ rises.

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A Note on Reading and Writing Freeport RAM from an Expansion Board

To speed up RAM access, the Freeport gate array internally generates a RAS-Enable if it sees a RAM-space address anytime during S2 or the first 20 nS of S3, without waiting for AS/ to tell it the address is valid. Then, if AS/ falls before the end of S3, and a RAM-space address is still present, RAS/ is generated.

However, the RAM-address multiplexors switch from row addresses to column addresses at the beginning of S4, regardless of when RAS/ occurred. If AS/ falls later than the first 20nS of S3, the RAM addresses will change too soon after RAS/, causing RAM errors.

Furthermore, if AS/ has not fallen by the end of S3, RAS-Enable is negated, a process that takes the first 20 nS of S4. If AS/ falls during that 20 nS, and a RAM-space address is still present, a RAS/ spike is generated which can cause RAM errors.

These restrictions mean that, to avoid problems when addressing the Freeport RAM, expansion board logic must never let AS/ fall during the period from 20 nS into S3 through 20 nS into S4.

(There is one exception to this: if it is guaranteed that the gate array did not see a RAM-space address (even on a floating address bus) during S2 or the first 20 nS of S3, no RAS-Enable is generated, so that a RAM-space address and AS/ anytime after the first 20 nS of S3 will not cause a RAS/ until the usual point in the next RAM-access cycle.)

Freeport Video

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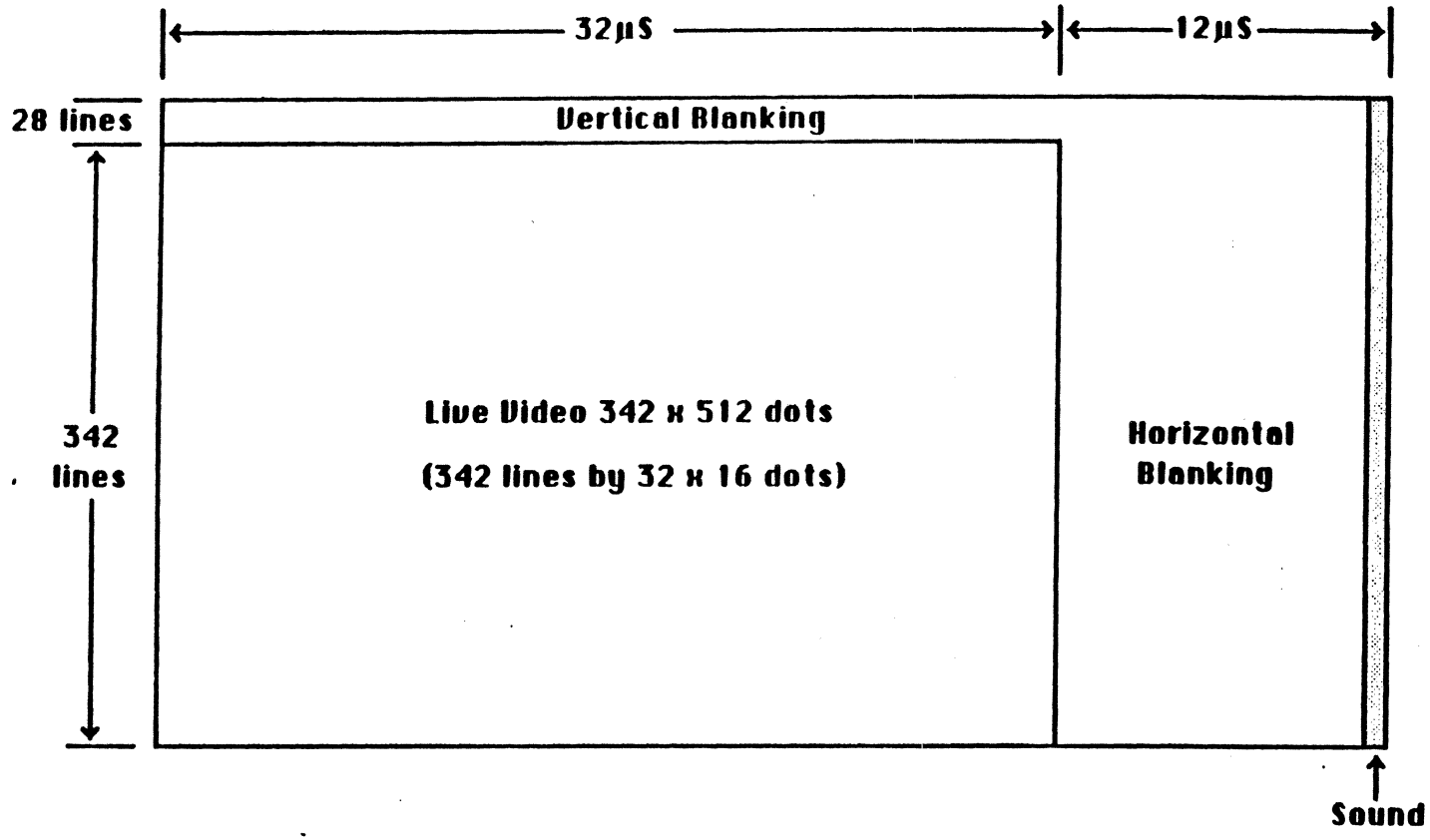

Live video: while the display is actively tracing a horizontal line of dots on the screen, video accesses to RAM (two words of data are read in each video access) alternate with three 68000 accesses.

Horizontal blanking: at the end of each horizontal screen line, while the display beam is returning from the right end of one line to begin the left end of a new line, the 68000 has uninterrupted use of RAM, except for one sound-buffer access (one word of data is read) each line.

Vertical blanking: at the end of each full screen, while the display beam is returning from the bottom of the screen to begin at the top again, the turned-off beam invisibly traces 28 more horizontal lines. During this time, the 68000 has full use of RAM, except for one sound-buffer access each invisible line.

SCC Timing for Freeport

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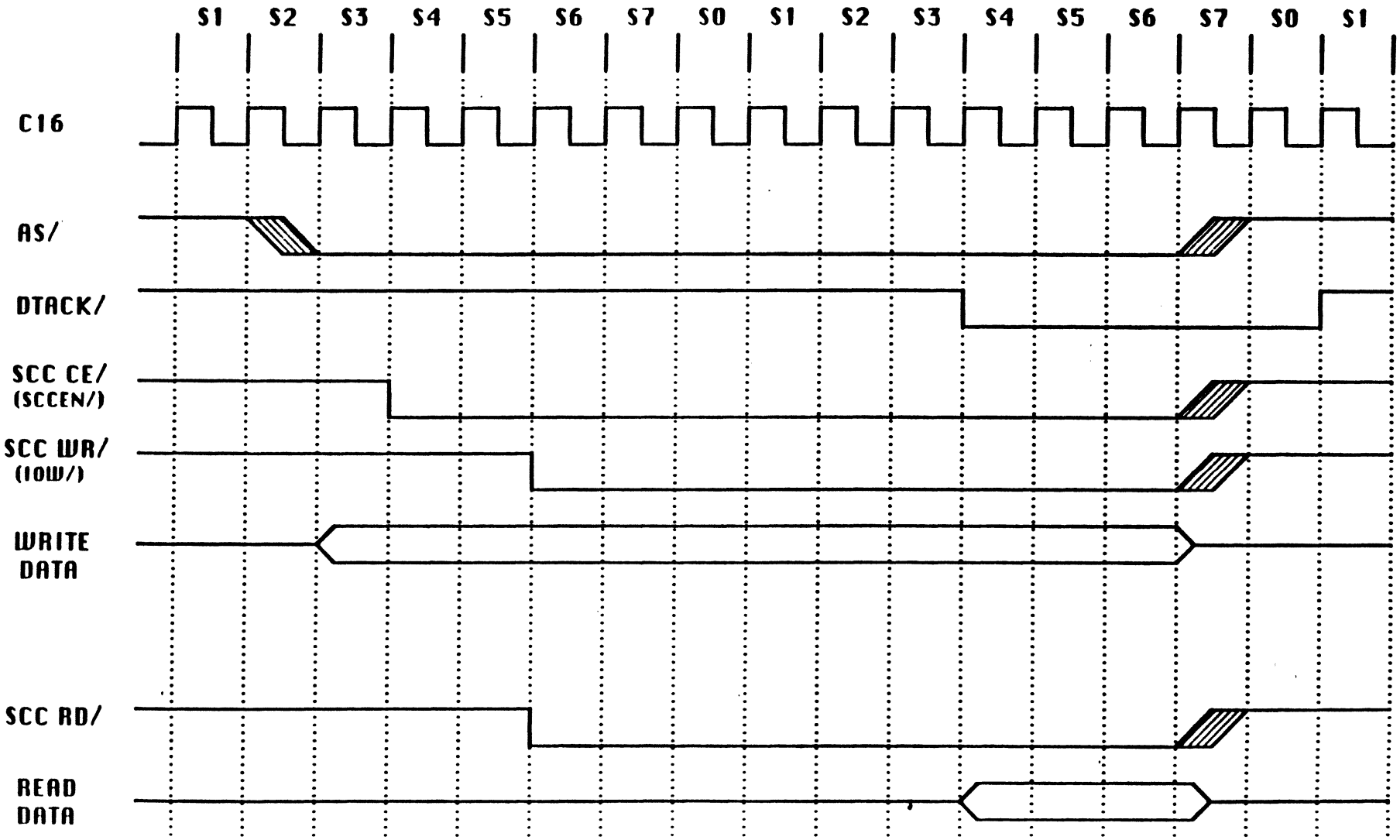

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SCSI Timing for Freeport