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AMDAHL 580
Large Scale
Integrated Circuit Manual

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REVISION NOTICE

This manual replaces the ALTA LSI Circuit Manual. Additional information has been added for clarification.

ABSTRACT

This publication provides the 580 Large Scale Integration (LSI) circuit chip wiring rules, logic design restrictions, and delay equations. The information is presented for the 580 logic designers so they may become cognizant of the configuration networks, become familiar with the wiring rules, and understand the LSI macros.

READER COMMENT FORM

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CHAPTER 1 - INTRODUCTION

Amdahl 580 LSI represents the state of the art in high speed, bipolar LSI logic. The propagation delay may be as small as 350 ps per gate. Design rules are required to fully utilize the very high performance of 580 LSI circuit chips and at the same time achieve reliable operation.

1.1 IMPEDANCE MATCHING

As a result of fast rise and fall times (less than 1 ns), the Current Switch Emitter Follower (CSEF) circuit family is designed to drive a 90 ohm matched impedance system whenever communication is done off-chip. The terminating resistor is a hybrid integrated R-pack of 90 ohms, returned to -2.0 volts.

1.2 TESTABILITY

Another important consideration for an LSI system is testability. Some logic design standardizations and restrictions are necessary to enhance testability.

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CHAPTER 2 - OFF-CHIP WIRING RULES

2.1 DEFINITIONS

Table 2-1 lists the definitions and rules that apply to off-chip terminated nets. Figure 2-1 is a typical off-chip wiring net illustration.

Table 2-1. Off-Chip Wiring Definitions

TERMS	DEFINITIONS
Network (Net)	Refers to the wire which connects a group of driving circuits and load circuits that are electrically connected together to perform some logic function.
Main Line (LM)	The longest distance in the net measured from a driver circuit output to a terminator.
Stub (LS)	When driving more than one load, short lines may be needed to connect loads on a card to the main line. These lines are called Load Stubs (LS). A stub starts at the main line and ends at the furthest load on the stub.
Loading Units (LU)	A term used to represent the capacitive loading effect of the circuit and packages. One loading unit (LU) is defined to be the capacitance of one Low Power Transistor Base and is equivalent to 0.1 pF.
Base	The base of a transistor which is the input of an ECL gate. A low power base is defined to be 1 LU, and a high power base is 2 LU.
Chip Carrier Crossing	Signals are transmitted from an LSI chip to an MCC through the chip carrier. Each chip carrier crossing consists of the following: LSI chip bonding pad, chip-to-chip carrier bonding wire, chip carrier lead frame, and one or two via hole(s) which interconnect to a multilayer MCC.
Via	A Plated Through Hole (PTH) used to interconnect layers on a MCC or sidepanel (SP).

(continued)

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Table 2-1. Off-Chip Wiring Definitions and Rules (continued)

TERMS	DEFINITIONS AND RULES
Connector Crossing	The signal path through a connector (MCC and/or Sidepanel Connector) which includes fixed traces and vias associated with that crossing.
Resistor Pack	MCC Module containing twenty-four terminating resistors.
RAM Module	Hybrid Random Access Memory module containing four (OLSO) memory chips interconnected to obtain various module organizations.
Lead Extension or Lead Frame	I/O signals pass through the lead extension. R-pack and RAM module are attached to the MCC by the lead extension.
Critical Net	A net which does not violate the design rules established in the Circuit Manual and whose performance can be predicted by the Delay Equation.
Non-Critical Net	A net whose performance is not essential to system performance. Design rules have been loosened and the delay prediction accuracy is not guaranteed.

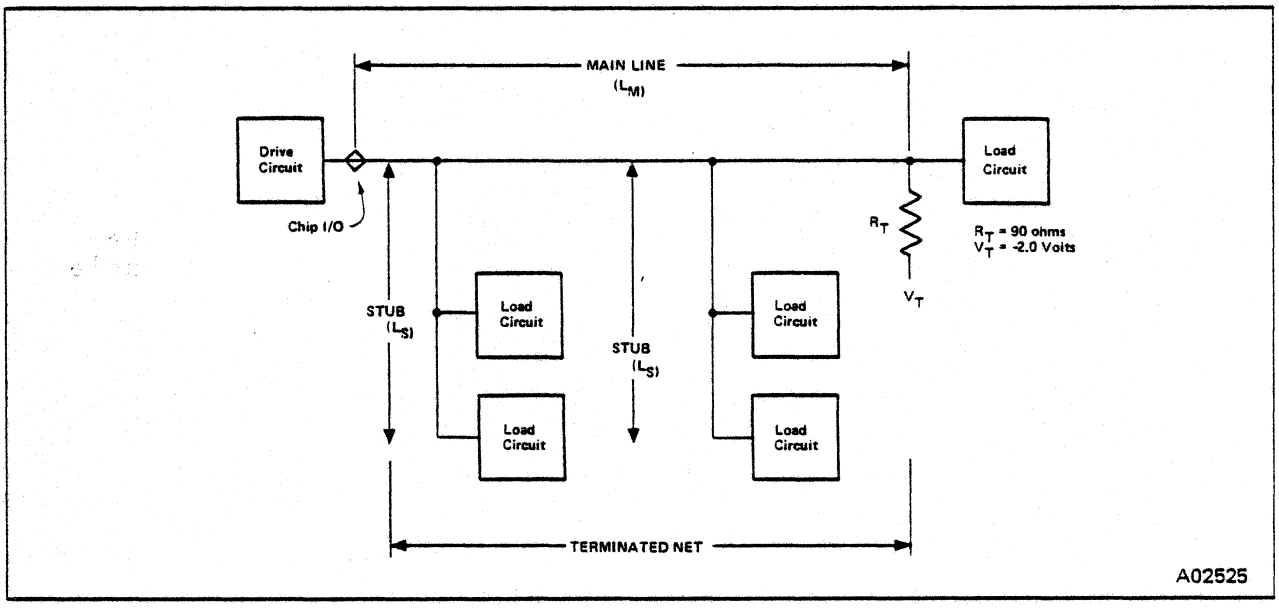

Figure 2-1. A Typical Off-Chip Wiring Net

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2.2 GENERAL WIRING RULES

As a result of fast rise and fall times of the 580 LSI, all off-chip wiring should be treated as a transmission line of definite characteristic impedance. All loads, stubs and characteristic impedance mismatches slow down the propagation of signals and/or generate noise. Noise can also be generated by crosstalk between electrically coupled lines. The following rules are established to fully utilize the 580 LSI capabilities and maintain ac and dc noise margins.

2.2.1 Wiring Principle

Although a limited length stub is allowed, in most cases it is desirable to route all external nets as a single non-branch, non-loop trace from driving gate to terminator. If stubs are used, the metal of the stub trace is a capacitive load in addition to the existing load on that stub. Refer to paragraph 5.8.2.

2.2.2 Termination

General external nets should have one termination resistor. Depending on the net, bi-directional transmission nets should have one or two termination resistors at each end. Short wiring between the last load or last stub on the main line and termination resistor is preferred. For clock nets, the wiring (from last load to terminator) should be printed wire and follow the clock distribution rules in paragraph 2.8.

2.2.3 Loop

Any single net may not contain and may not constitute a closed loop.

2.2.4 Wiring Resistance

Total dc wiring resistance from any driving circuit in a net to the last load or last stub on main line is limited to the values of table 6-2. Total dc wiring resistance is obtained as follows:

$$Rdc = R_i L_i + \sum R_{con}$$

where:

R_i : is the dc resistance per unit length for each wiring material

L_i : wiring length in corresponding wiring material

R_{con} : dc resistance of connector(s) in path

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This rule is not applicable to tie down nets.

Table 2-2. Wiring Resistance Limitations

MACRO	OUTPUT	INTRA MCC	INTER MCC	INTER STACK
Normal Macro	NOR	5 ohms	--	--
	OR	4 ohms	--	--
Macro 43 (MD)	NOR Single Gate	5 ohms	5 ohms	--
	NOR Int. Gate*	5 ohms	5 ohms	4.8 ohms
	OR	5 ohms	5 ohms	4 ohms
	OR Driving Memory	1.2 ohms	--	--
Macro 42 (BD)	OR	4 ohms	4 ohms	4 ohms
RAM		5 ohms	5 ohms	--
*A gate whose inputs are driven from a source on that same chip.				

2.2.5 Wiring Materials

Table 2-3 lists the resistance of wiring materials for external nets.

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Table 2-3. Wiring Materials Resistance Cross Reference

WIRE MATERIAL	RESISTANCE
MCC Printed Wire	0.20 ohms/inch
SP Printed Wire	0.14 ohms/inch
Single/Twin Lead Wire	0.10 ohms/inch
Coaxial Cable	0.014 ohms/inch
MCC <--> SP Connector	0.025 ohms
SP <--> Cable Connector	0.045 ohms

2.2.6 Unused Inputs

Unused inputs should be tied down to -2V through a termination resistor. Up to fifty unused inputs may be connected to the same terminator. This tie down net should be 10 inches or less in total length. Refer to paragraph 4.5 for unused RAM inputs.

2.3 WIRING RULES FOR SINGLE 90 OHM TERMINATED NETS

The designer is reminded that the fastest nets are short and lightly loaded. In order to meet the loading per unit length requirements, it is recommended to reduce loading by dividing the net into two or more nets rather than lengthening one net.

2.3.1 High Performance Terminated (Short/Lightly Loaded) Nets

The following two rules will produce the highest possible performance nets.

1. If the total length of the net is less than three inches and the loading is less than 120 LU, there are no placement rules.

2. If the total loading units on the net are less than or equal to 80 LU, there are no placement restrictions. Length restrictions must meet minimal DC resistance requirements of paragraph 2.2.4.

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2.3.2 General Terminated Net Wiring Rules

Use with most general nets except Clocks and Speed Critical nets.

1. Distributed loading should average $\leq$ 14 LU per inch of line to insure maximum propagation speed and to minimize waveform distortion.

2. Designers are encouraged to avoid large lumped loading ($\geq$ 60 LU) and to place any lumped loading at the end of a net not further than one inch from a terminator. Uniform distribution of loads will preserve waveform integrity.

3. All stub lengths must be less than or equal to one inch.

4. Maximum stub loading (including trace loading) is 60 LU.

5. The absolute maximum loading on any three-inch net segment is 120 LU.

2.3.3 Critical Net Fanout

The maximum fanout of normal LSI external emiter followers is a function of the line resistance. Figure 2-2 shows this relationship.

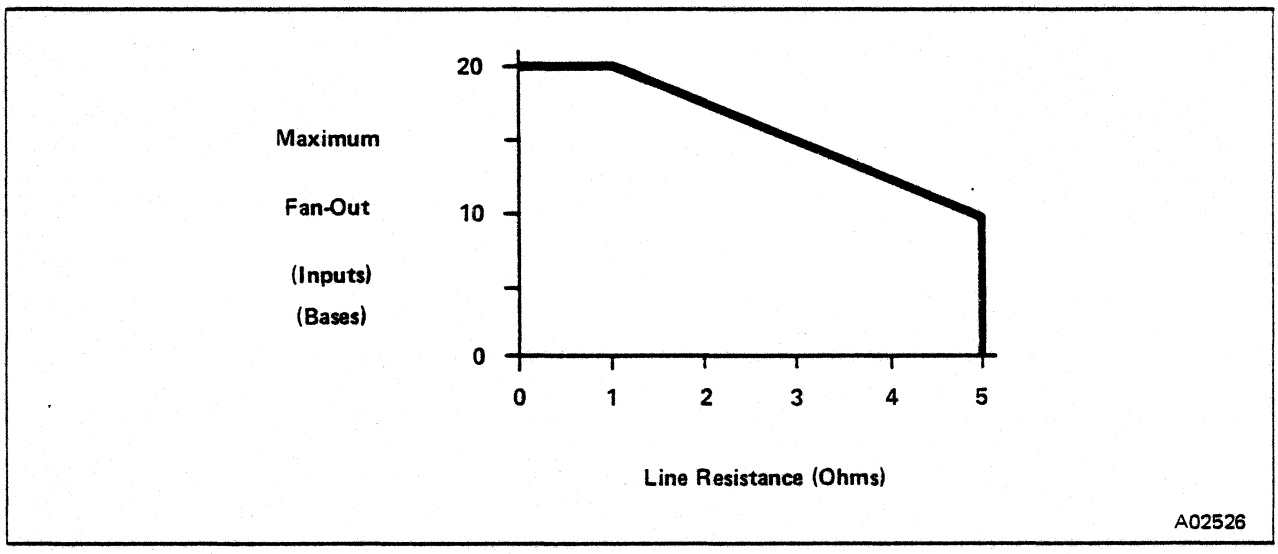

Figure 2-2. Maximum Fanout

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2.3.4 Termination Resistor

Normal nets, including RAM, are terminated with a 90 ohm terminator at the end of the net farthest from the driver.

2.3.5 Multiple Base Inputs

The following macros contain multiple bases at one or more input ports. Both inputs of macros 42 and 43 are two base inputs for fanout purposes.

Macro 2399, input port 15, must be counted as two inputs. Macros 3199 and 3399 contain two base inputs at ports 8 and 9. Macro 3299 contains two base inputs at ports 4 and 5.

2.3.6 Input Biasing

The state of an open input cannot be guaranteed. It is the designer's responsibility to ensure that unused inputs are biased properly.

- Tie Up ("V_{IH}" Input): Use the ϕout of the gate whose inputs are all forced to "V_{OL}". DO NOT GROUND ANY INPUTS.
- Tie Down ("V_{OL}" Input): Normal terminator (90 ohms to -2V).

2.3.7 Driver Choice

- Intra MCC
  - General - No restrictions
  - Driving Memories-RAMs must be driven by OR output of Memory Drivers. Refer to Chapter 4, Random Access Memory Wiring Rules.
- Inter MCC

  Use MACRO 42 or MACRO 43.
- Inter Stack

  Use MACRO 42 or MACRO 43 (OR Output)

2.3.8 Driver Location

When driving off an MCC to another MCC, another stack or to the non-stack units, the driver must be placed as follows:

- When using Macro 42 (BD), the driver must be placed within three columns of the MCC connector.

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- When using Macro 43 (MD), there are no placement restrictions between MCCs in the same stack. If the driver is between stacks, the driver must be placed within three columns of an MCC connector.

2.3.9 Driving Off Stack

When driving from an LSI chip off stack (to non-LSI or to another stack), the designer must continue to follow the wiring rules contained in this manual.

2.3.10 Basic Logic Cards with LSI

The Interface Handler and Direct Control BLC use LSI devices. For this reason, MCC wiring rules are to be used.

2.4 DOTTED EMITTER FOLLOWER WIRING RULES

Dot-OR noise results when one or more emitter followers switch state when they are dotted together to perform the OR function. Refer to T_{add} in paragraph 5.3.8 for on-chip effects.

2.4.1 Current Changing Rate

Dot-OR noise depends upon the current change on the transmission line caused by switching emitter followers and the length of the line between emitter followers. In order to calculate the maximum distance between dots, the current changing rate is defined below and in figure 2-3.

$$\frac{\Delta IEF}{IEF} = \frac{Nsw}{N1}$$

where:

ΔIEF = Net current change on the line caused by emitter followers switching at the same time.

IEF = Net current on the line just before the switching occurs.

Nsw = The number of emitter followers switching from "V_{OH}" state to "V_{OL}" state within ±1 ns.

N1 = The number of emitter followers in the "V_{OH}" state just before switching occurs.

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In the case that EF_A is of interest, $\frac{\Delta IEFA}{IEF}$ is always counted as 1;

If $t_{BA} \geq 2$ ns, then $\frac{\Delta IEFB}{IEF}$ is counted as 1;

If 1 ns $\leq t_{BA} < 2$ ns, then $\frac{\Delta IEFB}{IEF}$ is counted as 0.5;

If $t_{BA} < 1$ ns, then $\frac{\Delta IEFB}{IEF}$ is counted as 0;

If $t_{AC} \geq 0$ ns, then $\frac{\Delta IEFC}{IEF}$ is counted as 1.

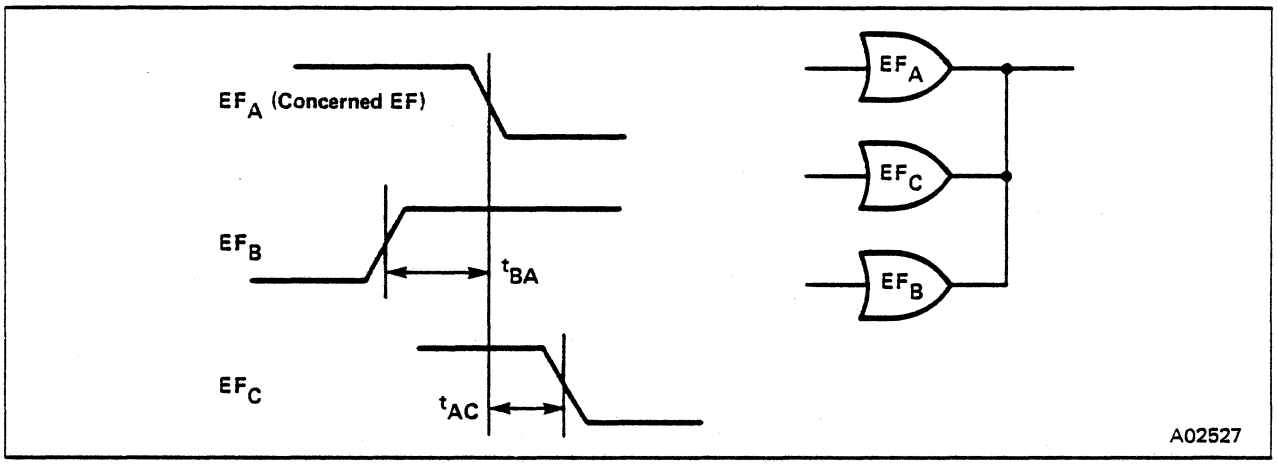

Figure 2-3. Definitions of t_{BA} and t_{BC}

2.4.2 Maximum Distance Between Dots

Maximum distance between dot-ORs (Ldot) is the maximum allowable length of trace between the two emitter followers which are furthest apart as illustrated and defined in figures 2-4 and 2-5 and table 2-4.

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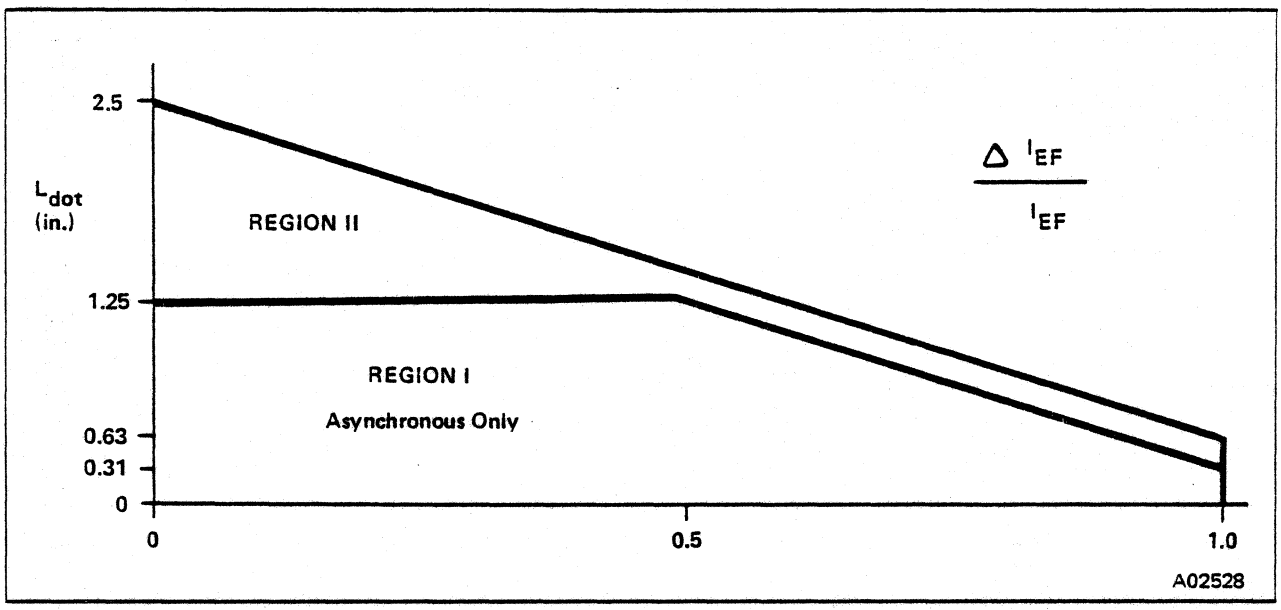

Figure 2-4. Maximum Distance Between Dots for Same Chip Outputs

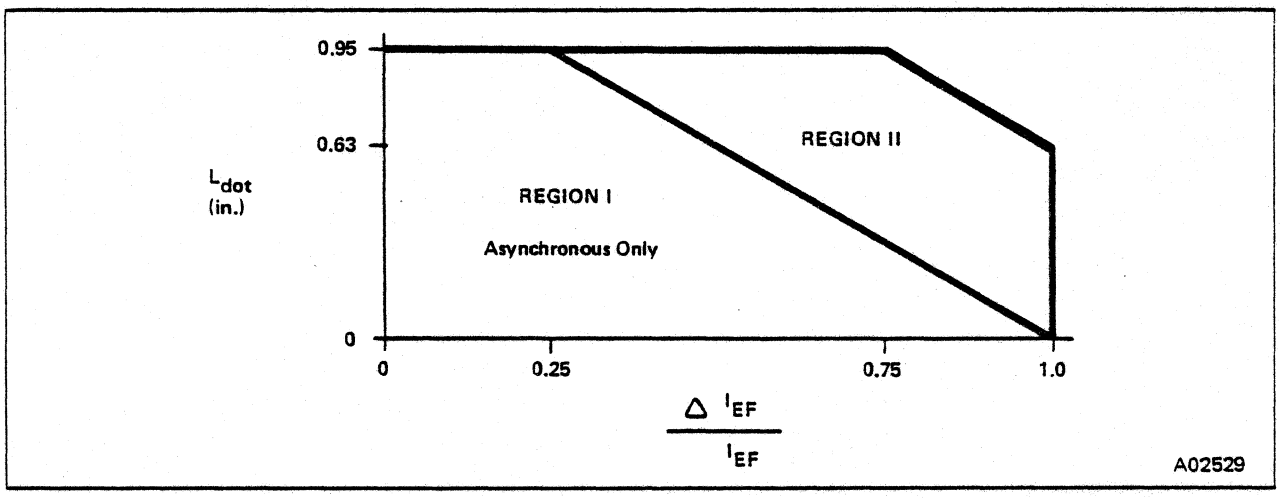

Figure 2-5. Maximum Distance Between Dots for Different Chip Outputs

Table 2-4 lists the EF Dotting restrictions.

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Table 2-4. EF Dotting Restrictions

MACRO	OUTPUT	INTRA MCC	INTER MCC	INTER STACK
Normal Macro	NOR (Single Gate)	2	--	--
	NOR (Int. Gate)*	8	--	--
	OR	8	--	--
Macro 43 (MD)	NOR (Single Gate)	--	--	--
	NOR (Int. Gate)*	2(4EF)	2(4EF)	--
	OR	4(8EF)	4(8EF)	4(8EF)
Macro 42 (BD)	OR	8(16EF)	4(8EF)	2(4EF)
*A gate whose inputs are driven from sources on the same chip.				
NOTE: 1. Non-critical net can contain up to sixteen dotted EFs. 2. When dotting to macros with outputs dotted within the macro, the total number of EFs must be counted in determining EF-dot limitations. 3. Internal EFs cannot be dotted to external EFs. 4. 2 (4EF) means two macro 42s may be dotted to make a dot of 4 Emitter followers.				

2.4.3 Maximum Distant Between Dots for Different Chip Outputs

Both Region I and Region II are allowed. For Region II, however, there are some cases that produce DOT-OR noise as shown in figure 2-6 This noise can cause faulty operation of the asynchronous circuits. Therefore, only Region I is allowed for asynchronous circuits. The outer area of Region I and Region II is allowed only in special cases. In this case, we have to allow for the extra delay which corresponds to the DOT-OR noise pulse width when we calculate off-chip delay.

The delay is defined by:

Case 1: $2 \times t_{Ldot}$ (ns) when receiver is outside Ldot.

Case 2: $5 \times t_{Ldot}$ (ns) when receiver is inside Ldot.

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where:

$^{t}Ldot$ = wiring delay which corresponds to the line length between those two emitter followers which are the furthest apart.

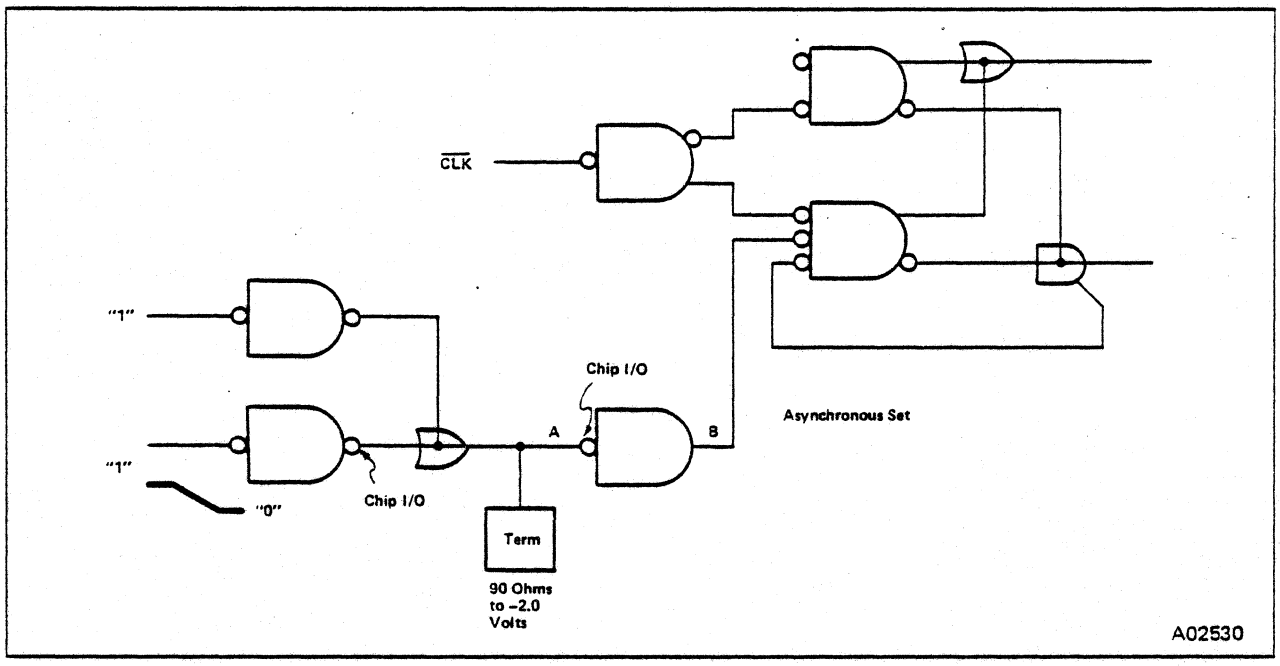

Figure 2-6. Typical Dot-OR Circuit for Calculation

2.5 NON-CRITICAL INTERCONNECTION

There are no restrictions on stub line lengths, total number of loading units in a net, and loading density in non-critical interconnections. Only two conditions 1) a maximum of fifty loads, and 2) line resistance of $\leq$ 8 ohms should be satisfied. Consequently, this interconnection is not suitable for sections where delay time is of importance.

2.5.1 Non-Critical Net Types

There are two types of non-critical nets. They are distinguished by the stub lengths. Type 1 net has stubs $\leq$ 1.18 inches, while Type 2 net has stubs $\geq$ 1.18 inches.

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2.5.2 Short Stub (Type 1) Non-Critical Net Delay Calculation

Using figure 2-7 and the following equation, we can calculate the delays.

$T_{pd\ min}$ = delay time that is calculated by the normal delay equation

$T_{pd\ max}$ = $T_{pd\ min}$ + 2 x (delay time from the output of A to the input of C)

where:

$T_{pd\ min}$ is the delay time for B to receive the first signal.

$T_{pd\ max}$ is the delay time for the noise at the input of B to settle.

$T_{pd\ min}$ and $T_{pd\ max}$ do not include the process variation of LSI delay (±30%).

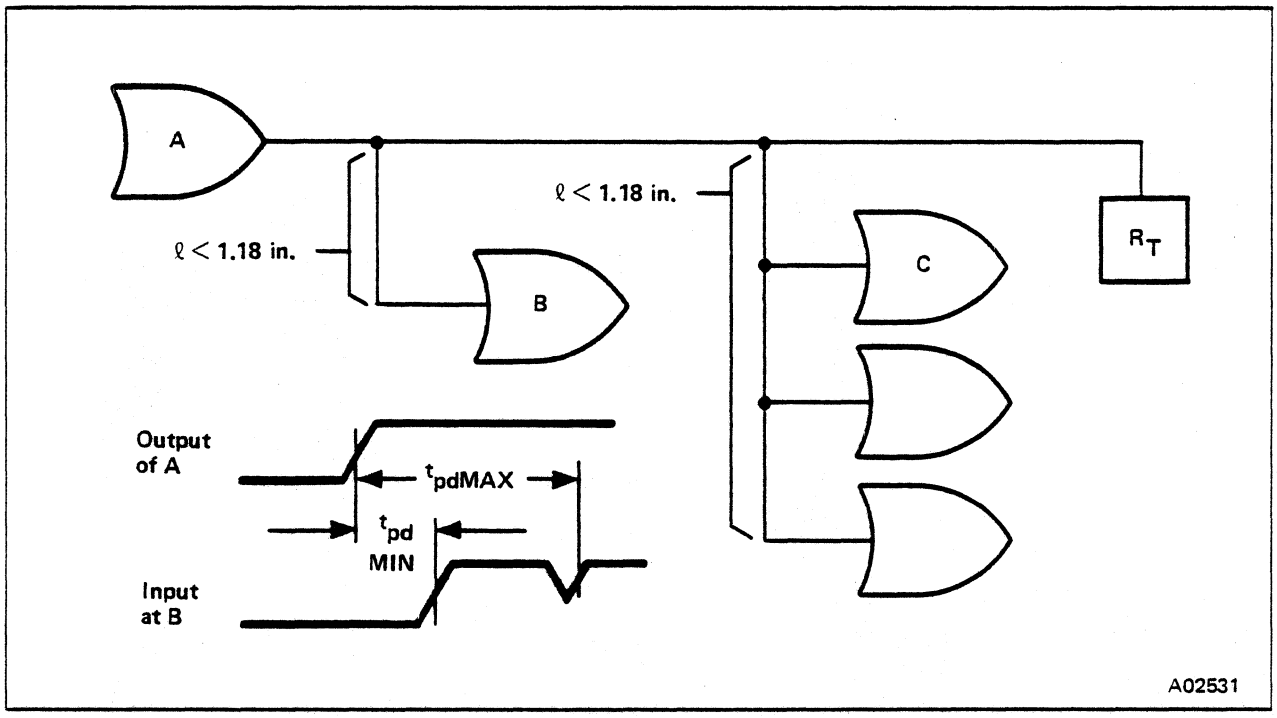

Figure 2-7. Type 1 Delay Equation

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2.5.3 Long Stub (Type 2) Non-Critical Net Delay Calculation

Using figure 2-8 and the following equation, you can calculate the delays.

$T_{pd\ min}$ = delay time that is calculated by the normal delay equation.

$T_{pd\ max}$ = 21 X (largest delay time of the stub segments that are $\geq$ 1.18 inches.

+ 3 X (delay time of the main line from the output of the driver to the turning point of the farthest receiver, not considering the said worst stub as loads.

This $T_{pd\ max}$ is defined to be the delay to all of the receivers of this net.

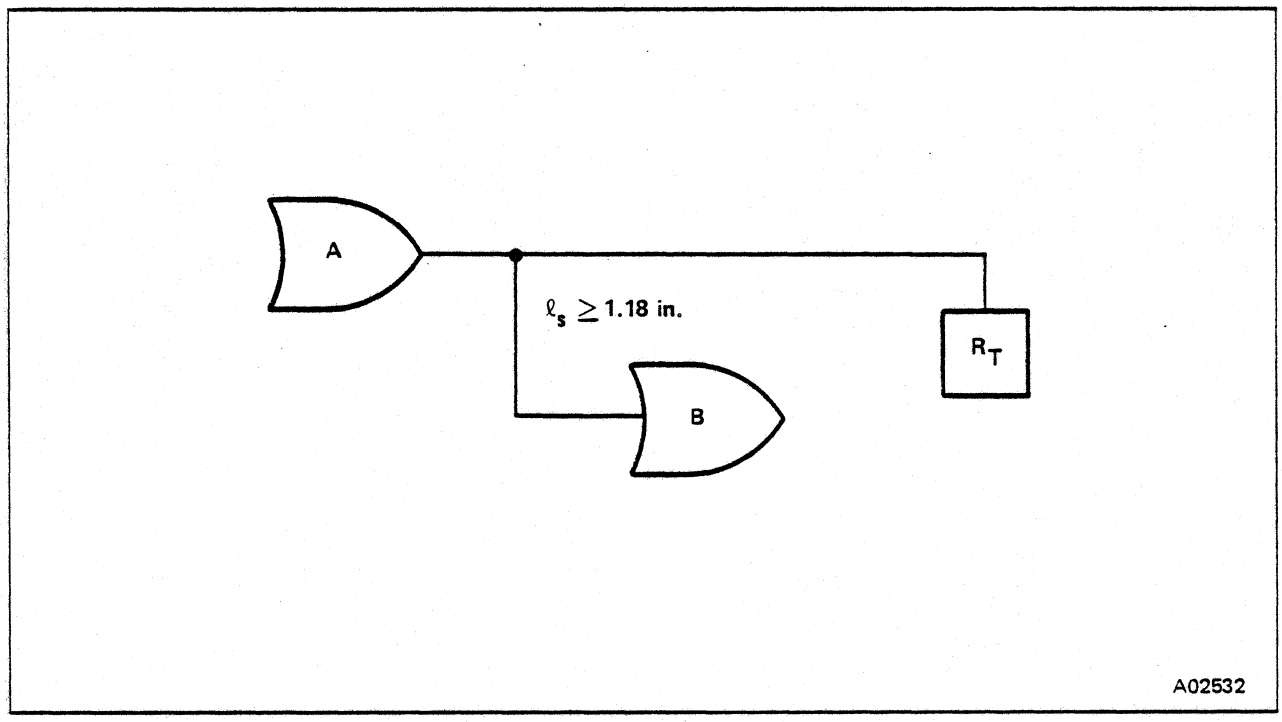

Figure 2-8. Type 2 Delay Calculation

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If you have more than one driver and they switch at the same time, refer to the following equation.

$T_{pd\ max}$ = 25 x (largest delay time of the stub segments that are $\geq$ 1.18 inches).

+ 5 X (delay time of the main line from the output of the driver to the turning point of the farthest receiver, not considering the said worst stub as loads).

Here, $T_{pd\ min}$ and $T_{pd\ max}$ mean the same as net Type 1. Each stub must be $\leq$ 29 inches in length. Refer to the example given in figure 2-9 and table 2-5 to calculate $T_{pd\ max}$.

2.5.4 Calculation Example of $T_{pd\ max}$.

Given the net of figure 2-9, calculate $T_{pd\ max}$.

Solution:

Stubs 1, 2, and 3 are type two nets. Refer to table 2-5 for the delay calculations.

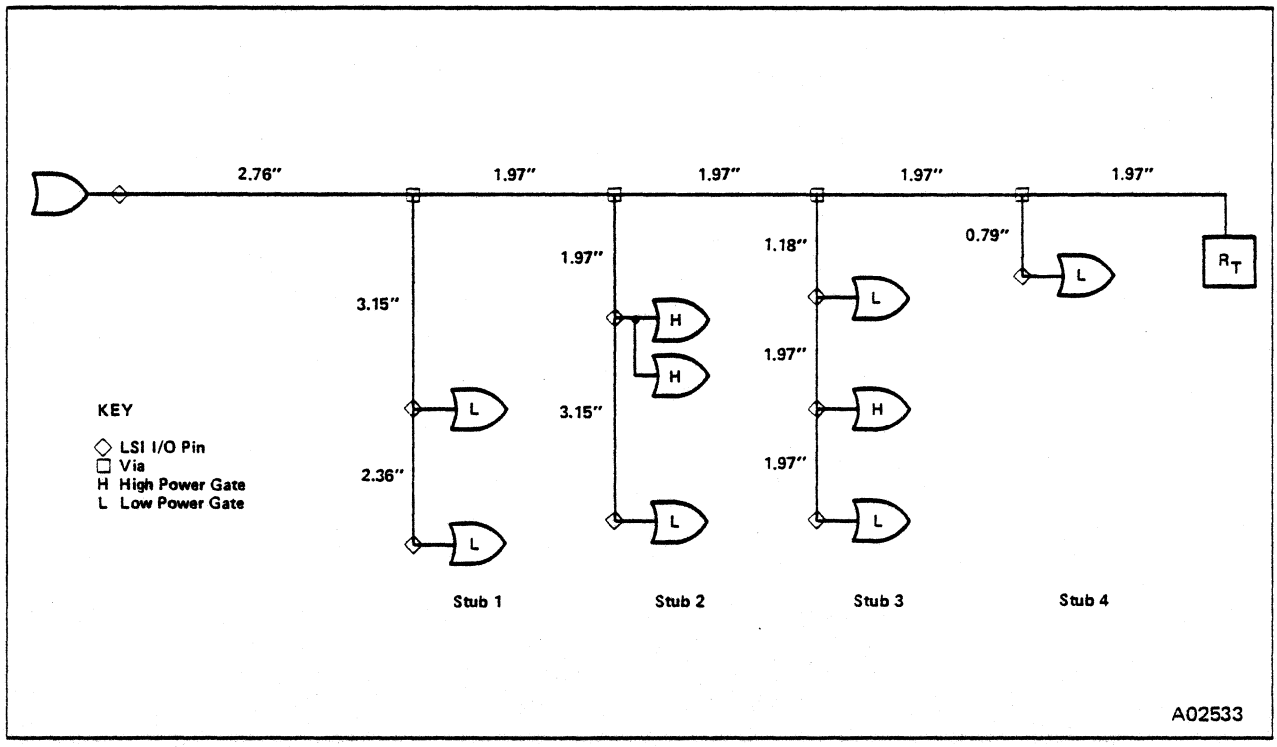

Figure 2-9. Example of Type 2 Non-Critical Net

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Table 2-5. Delay Calculation of Example in Figure 2-9

	DELAY ELEMENT	LOADING	DELAY (PS)
STUB 1:	Trace:	5.51"	980/980
	Bases: Low Power High Power	2 0	5.8/2.8
	LU: Via Chip I/O Metal on Chip	12 LU 48 LU 6 LU	323.4/349.8
STUB 2:	UP/DN Delay		1309/1333
	Pattern	5.12"	910/910
	Bases: Low Power High Power	1 2	2.9/1.4 11/5.2
	LU:	60 LU	294/318
STUB 3:	UP/DN Delay		1218/1235
	Pattern	5.12"	910/910
	Bases: Low Power High Power	2 1	5.8/2.8 5.5/2.6
	LU	93 LU	455.7/492.9

NOTE: Stub 3 has the largest delay time. The delay time of the main line without stub 3 will be as follows:

Main Line	Pattern	8.66"	1540/1540
STUB 1	Base: Low Power	2	5.8/2.8
	LU:	171 LU	839.9/906.3
STUB 2	Base: Low Power	1	2.9/1.4
	High Power	2	11/5.2
	LU:	157.5 LU	771.8/834.8
STUB 4	Base: Low Power	1	2.9/1.4
	High Power	0	
	LU:	48 LU	235.2/254.4
		UP/DN Delay	3407.5/3546.3

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Then:

$T_{pd\ max}$ (up) = 21 X 1377 + 3 X 3407.5 = 39140 ps

$T_{pd\ max}$ (dn) = 21 X 1408.3 + 3 X 3546.3 = 40213 ps

2.6 PARALLEL WIRE RULES

Parallel signal lines induce noise pulses onto each other because these lines are electrostatically and electromagnetically coupled. This induced noise is called crosstalk noise. Parallel wiring limits are established to control this crosstalk noise and to achieve reliable operation. If a net contains both MCC and sidepanel segments, they are treated separately. Refer to table 2-6 for maximum parallel net lengths.

Table 2-6. Maximum Parallel Net Length in Inches and Grid Units

LOCATION	LAYER OR TYPE OF COUPLING*	NORMAL NETS		CLOCKS AND ASYNCHRONOUS NETS		BUS	
		in.	gu	in.	gu	in.	gu
MCC	X & Y LAYERS	1.65	33	1.35	27	1.35	27
	SLANT LAYERS	2.20	98	1.84	82	1.84	82
SIDE PANEL	TYPE 1	2.60	26	2.10	21	2.10	21
	TYPE 2	1.40	14	1.10	11	1.10	11
	TYPE 3	3.20	32	2.60	26	2.60	26
*Refer to figure 2-10 for definition of coupling types.							

2.6.1 Geometric Factors

Figure 2-10 illustrates the three types of parallelism which can exist in the sidepanel (SP). Only Type 1 parallelism can exist within the MCC. Each type exhibits a different amount of crosstalk noise coupling and is therefore weighted to reflect this difference. The weakest coupling is Type 3, with a weighting factor of 1.0. The strongest coupling is Type 2 with a weighting factor of 2.0. Type 1 coupling has a weighting factor of 1.3.

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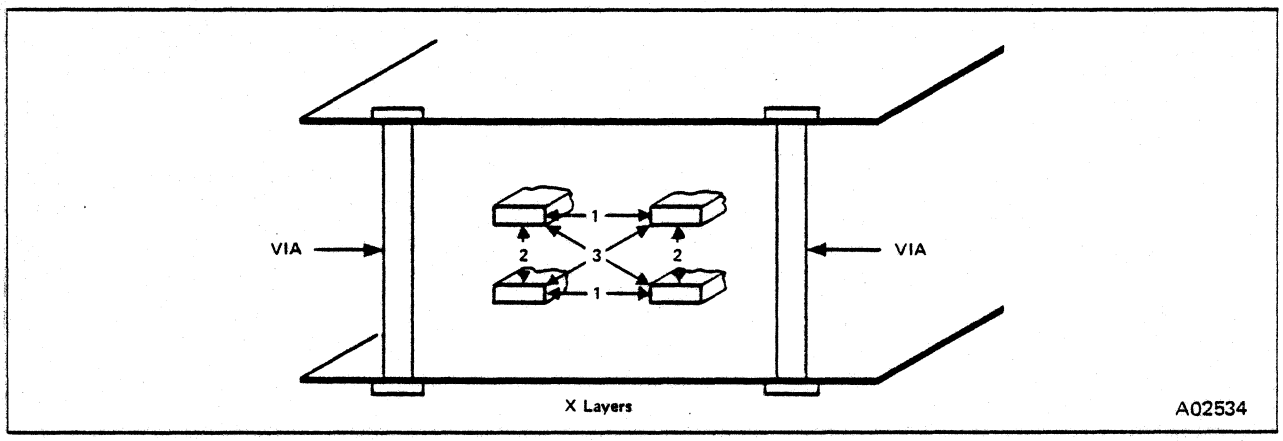

Figure 2-10. Three Types of Parallelism

2.6.2 Intra-MCC Net

Figure 2-11 is applied to intra-MCC net parallel length calculations. Nets A and B are parallel on layer X1 for a distance of x. On layer S1, nets A and B are parallel for a distance of s, and on layer YZ, they are parallel for a distance of y. In order to calculate intra-MCC nets, refer to table 2-6 and the following equation:

$$\frac{\ell_x + \ell_y}{L_{xy}} + \frac{\ell_s}{L_s} \leq 1$$

where:

- ℓ_x = the parallel distance on the X layer.
- ℓ_y = the parallel distance on the Y layer.
- ℓ_s = the parallel distance on the slant layers.
- L_{xy} = the maximum allowable parallel distance on the X and Y layers.
- L_s = the maximum allowable parallel distance on the slant layers.

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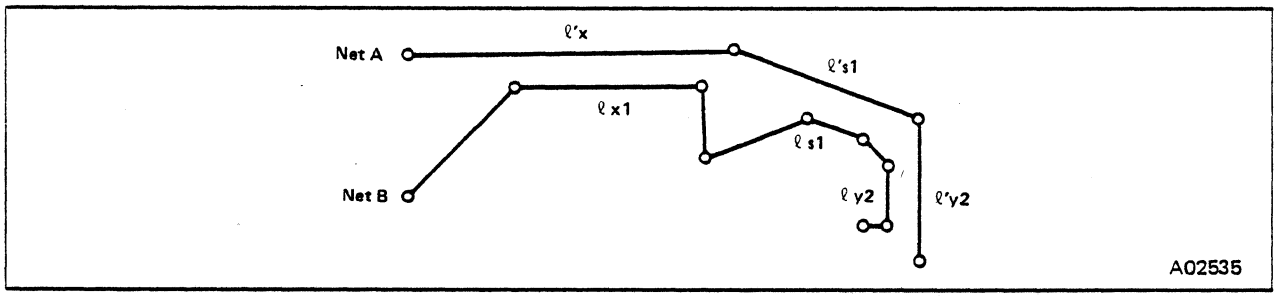

Figure 2-11. Parallel Nets on MCCs

2.6.3 Inter-MCC Net (Sidepanel)

Figure 2-12 is applied to inter-MCC net parallel length calculations. In order to calculate inter-MCC nets, refer to table 2-6 and the following equation:

$$\sum_{3}^{N=1} \frac{\ell x_N + \ell y_N + \ell s_N}{L_N} \leq 1$$

where:

$\ell x_N, \ell y_N \ell s_N$ = the lengths of wire that are parallel on the x, y, and s layers with a coupling of N.

L_N = the maximum allowable parallel length for each coupling type.

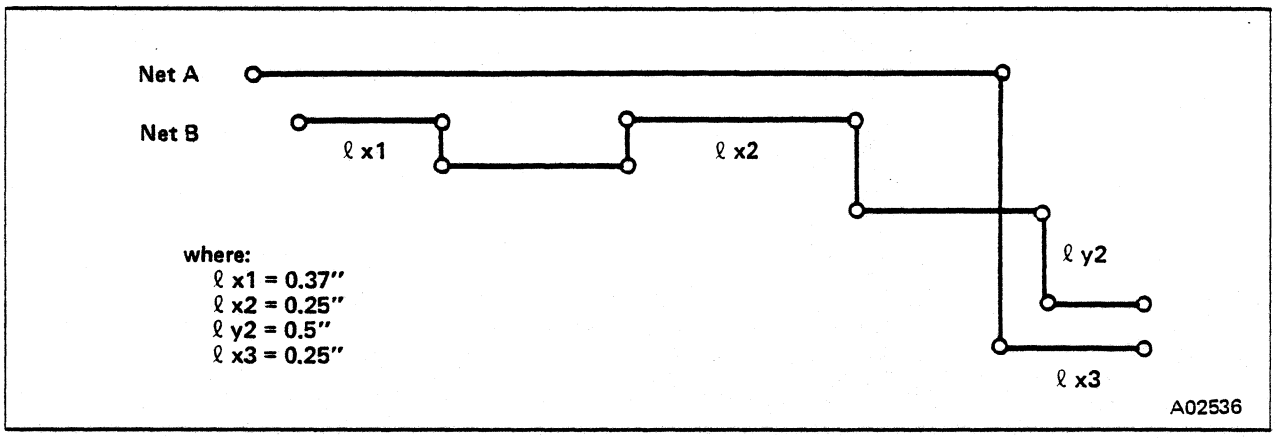

Figure 2-12. Calculation for Maximum Parallel Lengths on SP

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Nets A and B are parallel on various layers in four segments. Segment ℓ_{x1} of net B is parallel to net A over a length of 0.37 inches with coupling type 1. Segments ℓ_{x2} and ℓ_{y2} are parallel with coupling factor 2. Segment ℓ_{x3} is parallel with coupling factor 3. Using the equation on the previous page, nets A and B are parallel.

$$\frac{.37}{2.6} + \frac{.25 + .5}{1.4} + \frac{.25}{3.2} = .756$$

Note: Notations are in inches.

2.6.4 MCC I/O Pin Physical Assignment

Due to crosstalk and noise problems, the MCC I/O pin assignment must be restricted. Arbitrary units were chosen for noise coupling factors and maximum noise limits. Figure 2-13 shows the geometric coupling between MCC I/O pins. All pins with drivers on the MCC are noise sources. Pins with noise sources couple noise into horizontally and vertically adjacent pins with a weight of 1. The diagonal coupling weight is 0.5.

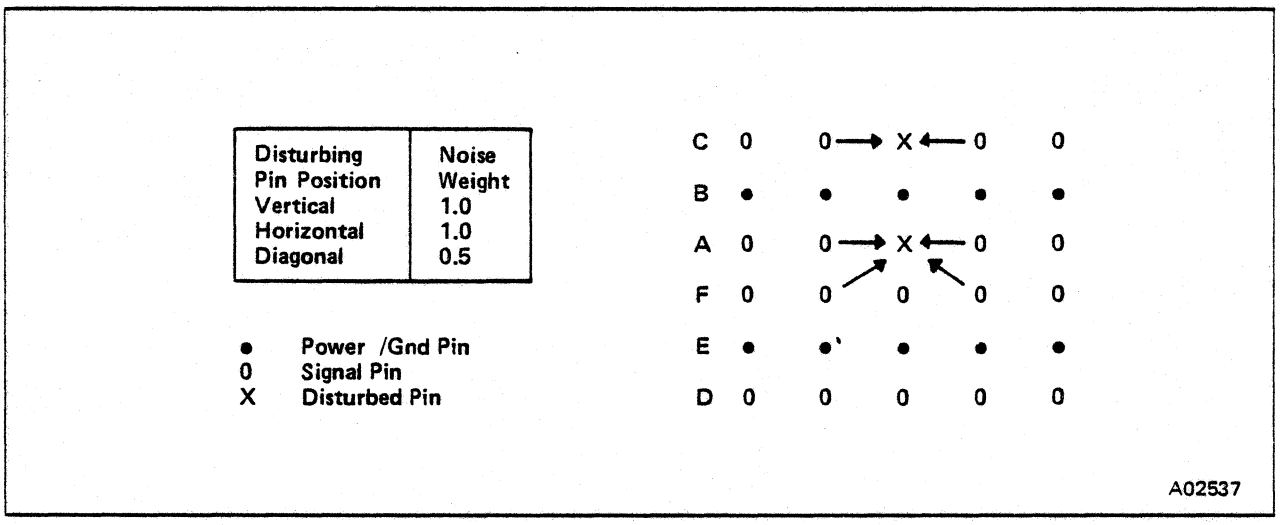

Figure 2-13. Noise Coupling Weight

Table 2-7 is a list of the maximum noise limits for the following four net types:

1. Unterminated receiver.
2. Receiver with a 90 ohm terminator.

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3. Net driving off MCC (no receiver).
4. Net with a driver and receiver.

NOTE: Net types 3 and 4 are noise sources. Terminators are "Don't Care" on net types 3 and 4.

Table 2-7. MCC I/O Noise Limits

NET TYPE	NOISE LIMIT		
	Unidirectional Net		Bi-directional Net
	On Stack	Off Stack	
1 2 3 4	2.0 3.5 No limit 3.5	1.5 3.0 No limit 3.0	1.5 2.5 No limit 2.5
NOTE: IF E/Cs are anticipated, use net 4 for net 3 types.			

2.6.5 Simplified MCC I/O Pin Physical Assignment

A simplified version of the rule in paragraph 2.6.4 has been developed by Fujitsu. Refer to figure 2-14.

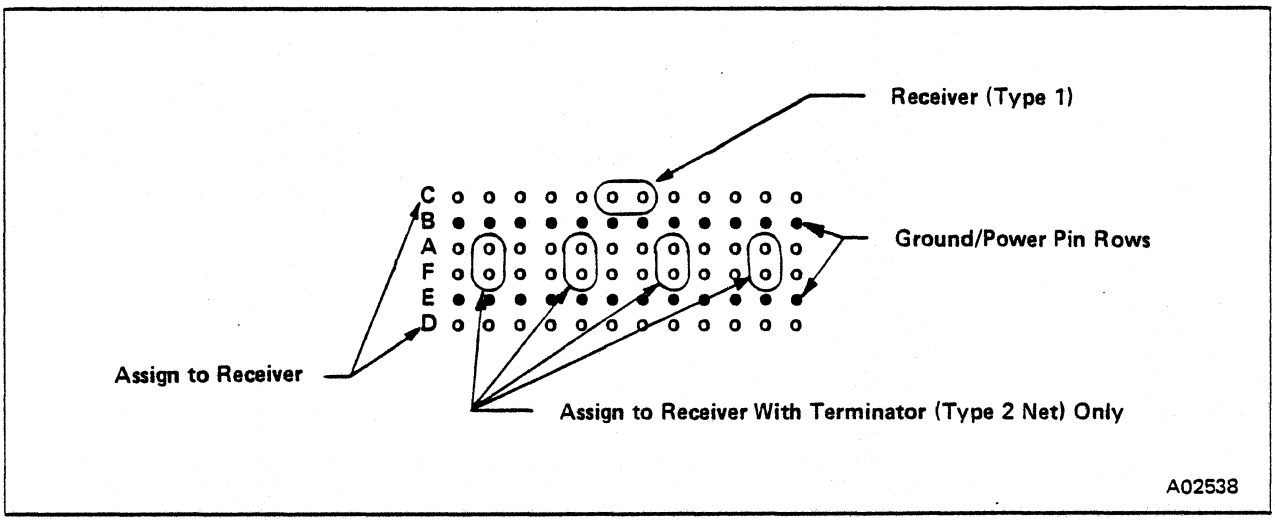

Figure 2-14. Simplified I/O Assignment

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2.7 DISCRETE WIRING RULE (MCC AND SP)

This class of wire is provided for clock tuning and future engineering changes. Due to high manufacturing costs, discrete wire should not be designed into the MCC and SP. Discrete wire should not be used to make a net faster. A better way would be to reduce loading or shorten the net length.

2.7.1 Wiring Principle

Discrete wires should be routed in minimal length paths.

2.7.2 Discrete Wire Stub

Each discrete wire stub should be 1.5 inches or less.

2.7.3 General Discrete Wire Selection Rule

1. General Wiring

   Single Lead: Less than 2 inches
   Twin Lead: 2 to 24 inches

2. Asynchronous, Set/Reset Net and Clock

   Single Lead: Less than 0.8 inch
   Twin Lead: 0.8 to 24 inches

2.7.4 Single Lead Wiring

1. Single lead wire has to be placed against the MCC surface as close as the manufacturing process allows to reduce the characteristic impedance of the wire. Single lead wire placed 0.040 to 0.080 inches above the MCC has a characteristic impedance of 200 ohms, which is more than twice the nominal system impedance.

2. Single lead wire which carries clock or set/reset signals should be placed to minimize length parallel to other discrete wires because of the large crosstalk noise coefficient.

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2.7.5 Twin Lead Wire Split

The split at both ends of twin lead wire should be 0.2 inch or less to minimize the impedance mismatch.

2.8 CLOCK DISTRIBUTION

In order to distribute clocks on an MCC with minimum skew, the two loads should have equal length stubs and the loading should be the same. Refer to figure 2-15.

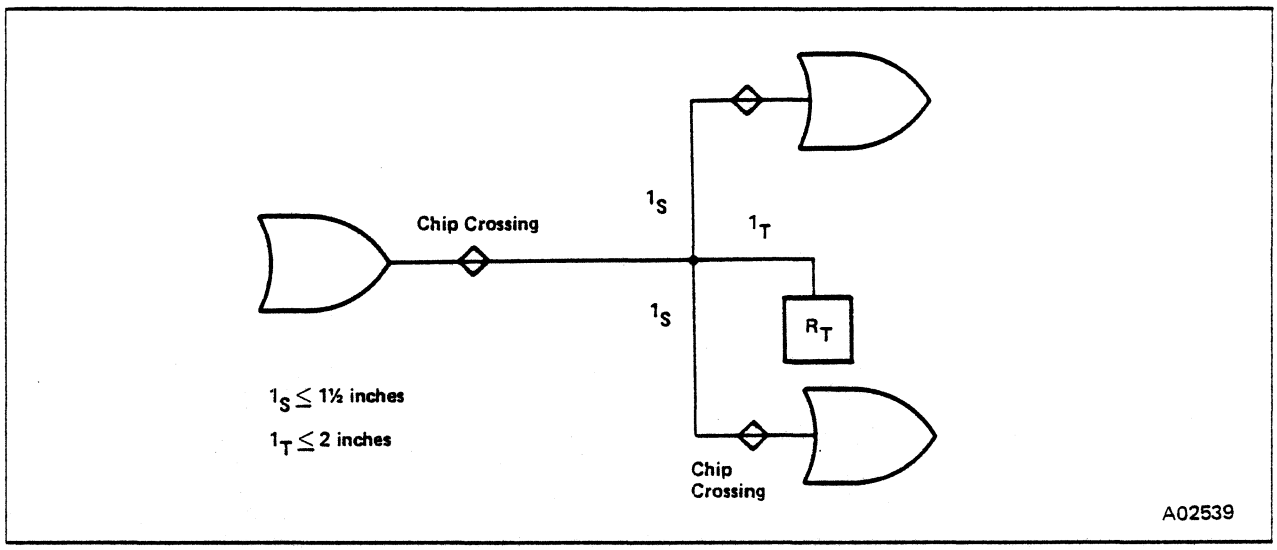

Figure 2-15. MCC Clock Distribution

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CHAPTER 3 - COMMON BUS

3.1 GENERAL

In general, data bussing involves connecting two or more driver outputs and one or more receiver inputs to the same signal line. ECL bi-directional bussing requires each end of the bus to be terminated. Only one driver emitter can be turned on at any time. If more than one driver is turned on, drivers appear as low impedance discontinuities. MACRO 42 Bus Drivers are employed which have an especially low Vol ($< V_T$). This ensures that their emitters are completely turned off and appear as a high impedance.

Figure 3-1 shows a typical bus line for the 580 system. It consists of seven stubbed loads across eight consecutive MCC positions. To begin to analyze the performance of the bus, we must know the starting impedance, delay of the unloaded bus line, total capacitive loading effect of each stubbed load, bus length, stub lengths, and the driver rise and fall times as well as overall drive capability.

Optimum performance is obtained from a bus that is uniformly loaded (that is, equally spaced stubs along the mainline of the bus each with the same loading capacitance). In addition, the electrical length of the stub spacing should not exceed one-half of the rise or fall time of the bus signal. Also, the electrical length of the stub should not exceed one-half of the rise or fall time of the bus signal.

For a discussion of the theory of modified impedance and transmission line delay, refer to the Non-LSI Circuit Manual written for 470. Paragraphs 2.9 and 3.3 were used to derive the equations used in this chapter. Refer to paragraph 3.2 of this manual for the equations and the method of analysis for a proposed bus design.

The following limitations on Bus construction are used:

- The Bus Driver (MACRO 42) rise and fall times are $\geq$ 2.0 ns.
- The physical distance between MCCs (pitch) will be 1.2 inches.

Common bus transmission systems are composed as follows:

- Only a double MACRO 42 (4 emitters) must be used for the driver.
- Any gate may be used for the receiver.

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- A maximum of 200 LU may be connected to each MCC Stub to perform a multiplex function. Stub loading consists of sidepanel and MCC Vias, Stub Printed Wire (SP and MCC), MCC connectors and all LSI Loading.
- A double termination (45 ohms) matching the Bus impedance must be connected to each end of the Bus line. Refer to figure 7-15
- The maximum mainline length between Bus Stub Loads shall be 2.5 inches.
- The maximum MCC Printed Trace Length to connect Drivers and Receivers shall be 1.5 inches.

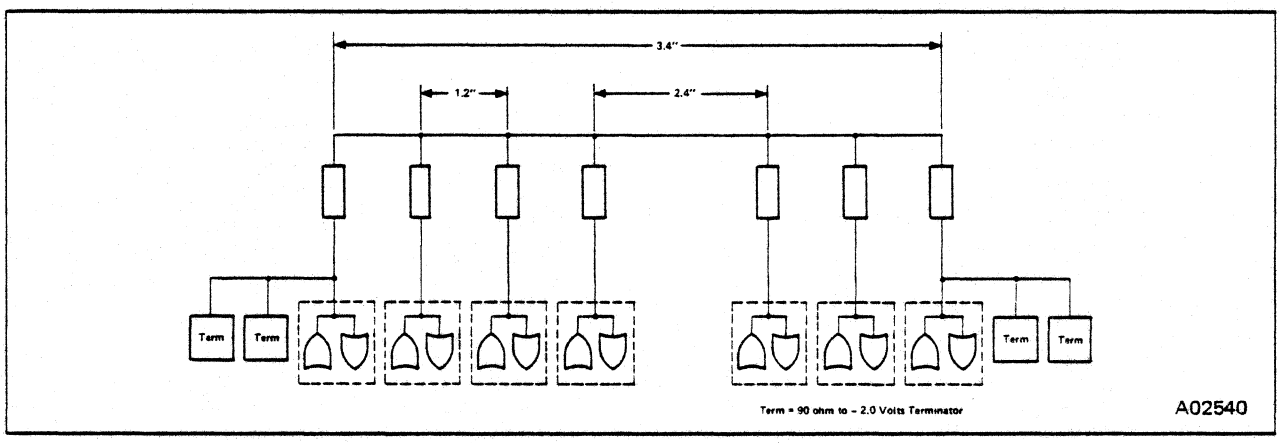

Figure 3-1. Typical 580 Bus Line

3.2 COMMON BUS SYSTEM DESIGN

3.2.1 Modified Bus Impedance and Propagation Delay

When designing a common bus structure as described in paragraph 3.1, careful attention must be paid to stub loading, especially as to the effect of lowering the overall bus impedance. As will be shown, the bus impedance will be lower than the 45 ohm termination value at each end of the bus. The major problem in the bus design is to keep the bus impedance from becoming excessively low (25 ohms) which will create large noise amplitudes due to reflections at the terminations and the driver. A secondary problem is control of the bus propagation

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delay. If this delay becomes too large, severe limitations on the locations of stubs will have to be enforced to prevent excessive ringing on the bus. The following equations allow prediction of the modified bus impedance and delay:

$$Z' = \frac{Z_o}{\sqrt{1 + (C_d/C_o)}}$$

$$\delta' = \delta_o \sqrt{1 + (C_d/C_o)}$$

where:

Z_o is the intrinsic (unloaded) impedance of the bus mainline.

C_o is the intrinsic distributed capacitance of the bus mainline.

δ_o is the intrinsic delay of the bus mainline.

C_d is the distributed loading attached to the bus mainline. This loading is from backpanel vias and printed trace, connectors, MCC fixed pattern metalization and vias, MCC printed trace, LSI packaging and LSI chip junction and metal capacitance. With uniform stub loading, the total capacitive loading of all stubs and loads is divided by the length of the mainline to derive C_d.

3.2.2 Bus Analysis

This Bus Analysis equation was developed to be used when only one chip crossing was required. Unfortunately, one chip crossing has not been developed at this time. When one chip crossing is developed, the following equation will be valid.

Figure 3-2 shows a single bus line connecting eight MCCs. Each MCC has a driver consisting of four emitters (two MACRO 42s) and a receiver gate on a single LSI chip connected internally via chip metalization which requires only one chip crossing. Let us use a value of 4.0 pF (40 LU) for this chip crossing. If each stub uses the maximum MCC printed trace allowed (1.5 inches), this represents an additional 3.0 pF per stub. Assume that in routing the MCC printed trace, two Vias were used for a capacitive load of 1.2 pF. Then each MCC connector crossing represents an additional 4.0 pF of loading. This gives a total of 12.2 pF per stub.

For MCCs with terminators, each terminator has a 1.8 pF capacitive load plus any additional trace capacitance. Let us assume 1.0 pF for trace and 3.6 pF for the double termination giving the terminated stubs a total of 16.8 pF of capacitive loading. Therefore, for the eight MCC stubs there is a total capacitive load of 6 x 12.2 + 2 x 16.8 = 106.8 pF. Since the bus mainline length is 8.4 inches, the distributed loading (C_d) is 12.7 pF/inch. Now, using the intrinsic

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bus values of Z_o = 85 ohms, δ_o = 180 ps/inch, C_o = 2.1 pF/inch, we may calculate the modified bus mainline impedance and propagation delay:

$$Z' = \frac{85 \text{ ohms}}{\sqrt{1 + (12.7/2.1)}} = 32.0 \text{ ohms}$$

and $\delta' = 180 \text{ ps/inch} \times \sqrt{1 + (12.7/2.1)} = 478 \text{ ps/inch}$

The propagation delay along the bus mainline located on the sidepanel will be 478 ps/inch x 8.4 inches equaling 4015 ps. Additional delay calculations must be performed by determining propagation delay from a driver to the mainline and from the mainline to the receiver. These delays are calculated as follows:

Driver to Mainline Delay = ℓ printed trace x 180 ps/in + t connector crossing + C_{load} (pF) x 35 ps/pF

Mainline to Receiver Delay = ℓ printed trace x 180 ps/in + t connector crossing + C_{load} (pF) x 50 ps/pF

where:

ℓ printed trace	is the MCC printed trace length from the driver output to the MCC connector.
t connector crossing	is a fixed delay from the MCC I/O to the backpanel connection to the bus mainline and has a value of 270 ps.
C_{load}	is all capacitive loading on the MCC printed trace. This includes LSI capacitance (emitters and receiver input as well as chip carrier capacitance and LSI I/O via capacitance), any stub trace to terminators at 2.0 pF/inch, terminator capacitance at 1.8 pF/90 ohm terminator, as well as any routing vias used to the MCC I/O.

For the example above, to calculate the worst case delay from one end of the bus to the other end, proceed as follows: since each stub with a terminator had a total of 16.8 pF of loading which included 4.0 pF for the connector and 3.0 pF for the 1.5 inches of MCC printed trace, the remaining capacitance of 9.8 pF is loading on the MCC printed trace. Therefore, the delay from the driver to the bus mainline is:

1.5 inch printed trace x 180 ps/inch + 270 ps (tconnector) + 9.8 pF x 35 ps/pF = 270 + 270 + 343 = 883 ps.

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The delay from the mainline to the receiver is:

1.5 inch printed trace x 180 ps/inch + 270 ps (tconnector) + 9.8 pF x 50 ps/pF = 270 + 270 + 490 = 1030 ps.

Since the mainline delay has already been calculated as 4015 ps, the total delay end-to-end for this bus is 883 + 4015 + 1030 = 5928 ps.

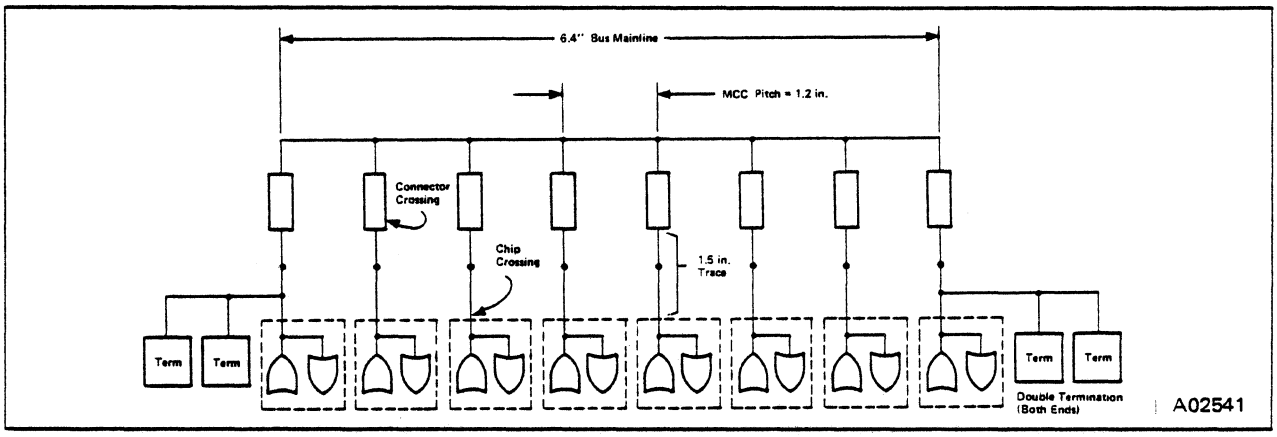

Figure 3-2. MCCs Connected by a Single Bus Line

3.2.3 Review Of Bus Analysis

A review of the previous analysis reveals several important things. First of all, the calculated delay from the bus mainline to a receiver is roughly 1 ns. As pointed out in paragraph 3.1, this delay should not exceed 50 percent of the signal rise or fall times to prevent excessive ringing. Hence, the requirement for a $\geq$ 2 ns risetime on the bus and the 1.5 inch limit on MCC printed trace on the stub is needed.

Secondly, the calculated bus mainline delay was 478 ps/inch which is a delay of 574 ps between stubs (assuming the stub pitch is 1.2 inches). Again, as pointed out in paragraph 3.1, the electrical delay between stubs should not exceed 50 percent of the signal rise or fall times. For the case just analyzed, the risetime requirement would be $\geq$ 2 x 574 ps equaling 1148 ps for stubs on 1.2 inch centers.

When skipping one MCC position, it is necessary to increase the stub pitch. The stub pitch would be 2.4 inches requiring a risetime of $\geq$ 4 x 574 ps equaling 2296 ps. This is the reason for the 2.5 inch pitch limit for stubs in paragraph 3.1. Obviously, as the stub loading increases, the modified impedance of the bus will decrease while the bus propagation delay and stub delay will increase, requiring even greater risetimes for the bus signals. Conversely, for a given rise-time, bus signal distortion and ringing will increase with increased

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bus loading. This is the reason for the 20.0 pF maximum loading limitation for stubs. Loading beyond this limit will create large impedance mismatches and cause excessive ringing and waveform distortion on the bus signals.

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CHAPTER 4 - RANDOM ACCESS MEMORY WIRING RULES

580 technology allows packaging bipolar RAM LSI (1K bits or 4K bits) mixed with logic LSI on the same MCC board. RAM wiring requires special attention because of its strict timing and noise requirements.

4.1 GENERAL RULES

RAM wiring should not have any stubs. Pulse width for write enable (WE) signal should be generated on the MCC on which it is used. When it is supplied externally, it should be buffered.

Macro 43 (OR output only) should be used for driving the RAM Modules. It terminates in 90 ohms placed 1 inch or less from the last RAM Module.

RAM Modules should not be driven by emitter dot (wire OR) logic.

Because of the very high performance of the RAMs, they will respond unpredictably to glitches or very narrow pulses. Therefore, the RAM inputs should be protected from glitches.

Different types of RAM Modules should not be driven by the same driver.

RAM input nets may contain discrete wires, but printed wires are recommended.

4.2 WIRING IN ARRAY SECTION

Wires which carry address signals, chip or block select signal(s), read/write control signals, read signals, or write signals are called array wiring (AW). Array wiring may not cross an MCC boundary, unless it has been buffered on the same MCC board. Manually routed array wiring is preferred because it has better electrical characteristics.

The maximum dc resistance of a RAM input net should be less than or equal to 1.2 ohms of line resistance. (6 inches of printed wire or 12 inches of discrete wire)

WE (Write Enable) input net should be routed on layers L5 (Y1) and L10 (X2). If necessary, layers L4 (X1) and L11 (Y2) may be used.

4.3 PARALLEL WIRING IN ARRAY SECTION

Parallel wiring restrictions defined in paragraph 2.6 are not applicable to array wiring. Array wires have to be routed to minimize crosstalk noise.

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4.3.1 Separation Between Array Wiring And Other Wiring

Array wiring and other wiring have to be completely separated in each layer of the MCC board to minimize noise coupling. For example, the address input signal before buffering, which is not an array signal, may not be routed through the array wiring area. While logic wiring allows two wires in a .05 inch channel, array wiring restricts wiring to 1 wire per .05 inch channel. Two copies of the same signal may be routed in a .05 channel.

4.3.2 Read/Write Control Signal (Write Enable)

Special attention has to be paid to the write enable signal routing to minimize crosstalk noise and skew. One grid unit (or wider) spacing is required between write enable and other array signals (address, chip select, data line, etc.). It is desirable to route all array signals in the same direction, so that the delay difference between RAM chips becomes minimal.

In figure 4-1, the address distribution designated as GOOD EXAMPLE is recommended. RAM 1 receives the earlier WE and address signals but the output signal travels the longest distance. This situation is reversed for RAM n and the total delay from WE or address to data out is almost equal to that of RAM 1.

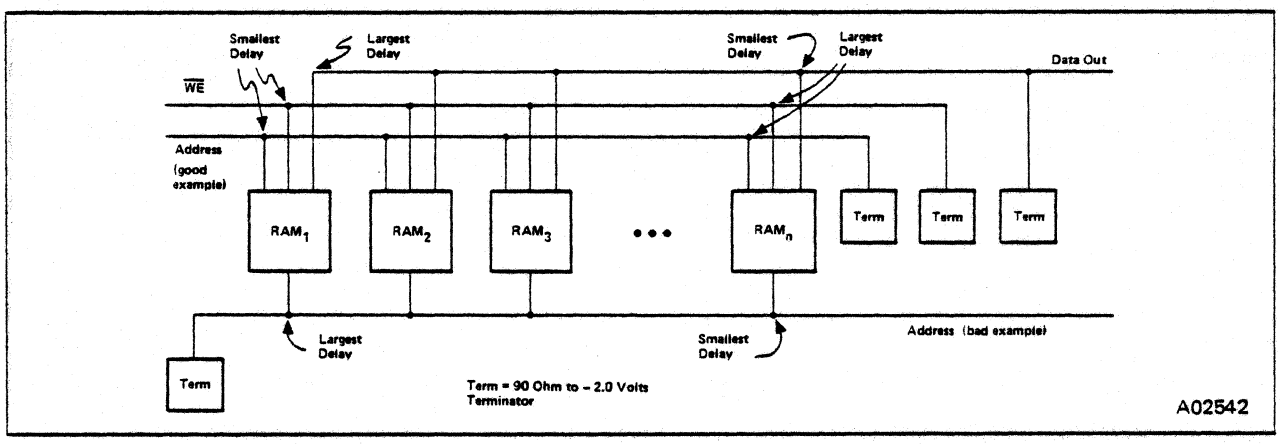

Figure 4-1. Preferred Distribution Design

Poor address distribution produces larger delay skew, faster response from RAM n but far slower response from RAM 1, and slows down memory operation as a whole.

Figures 4-2 and 4-3 illustrate the rules that should be maintained on RAM Input lines.

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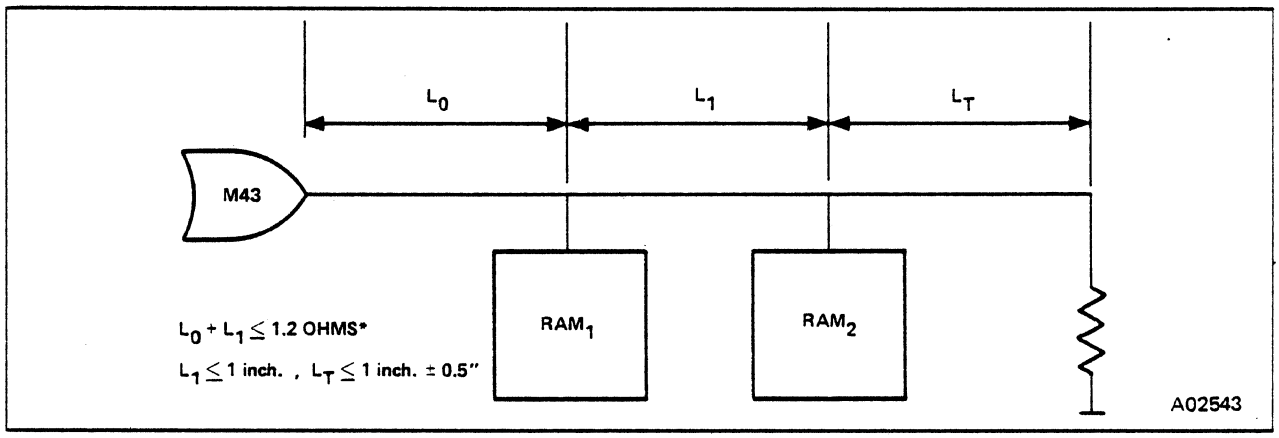

Figure 4-2. Address and Write Enable Nets

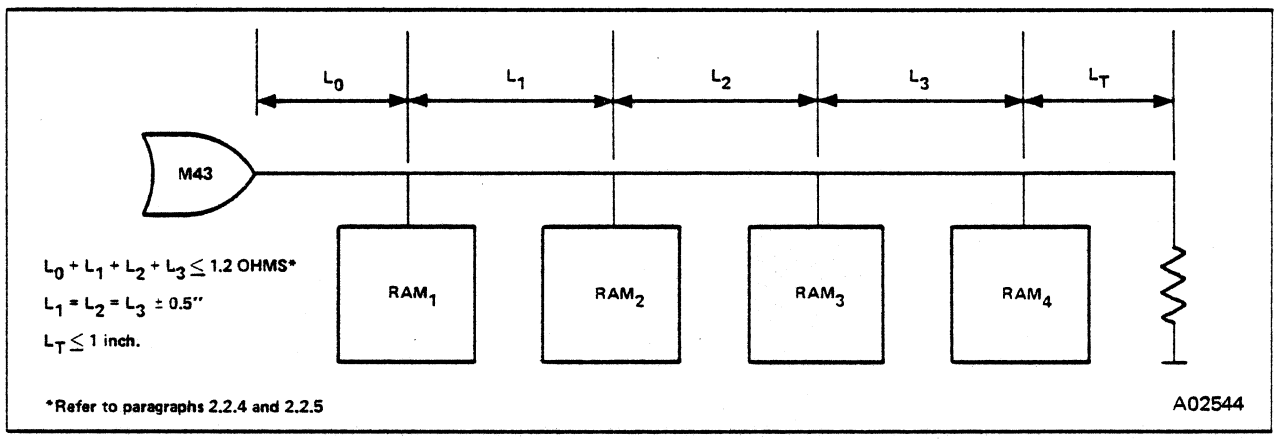

Figure 4-3. Block Select and Data-In Nets

4.4 PULL DOWN

All RAM input nets must be terminated. Note, RAM chips do not have input pull down resistors.

4.5 TIE DOWN (UNUSED INPUT)

All unused inputs should be tied down to -2V through a termination resistor. Up to fifty unused inputs may be connected to the same terminator. This tie down net should be 10 inches or shorter in total length to minimize noise pick up. Unused RAM input tie down nets should not contain any logic LSI unused inputs.

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4.6 DATA-OUT DOT-ORING

Data-out Dot-ORing (emitter dot) is a common way to expand the number of words in a memory as a unit. The following conditions have to be met when dotting is employed:

1. Maximum of eight EFs may be dotted.
2. Maximum of four Module Pins may be dotted.
3. Maximum distance between emitter followers in a dot is three inches.
4. Each stub must be $\leq$ one grid unit.

4.7 RAM DRIVER FAN-OUT

Fan-out rules are as follows:

- The fan-out of write enable and address drivers should be less than or equal to two module input pins.
- The maximum fan-out of other signals driving the memory array is eight chips on four modules. A maximum of four module input pins can then contain up to two chip inputs each.

4.8 LSI AND RAM MODULE MIX RESTRICTIONS

When LSI inputs and RAM Module inputs are mixed in the same net, only one RAM Module and one two-base LSI input are allowed. The spacing of figure 4-4 should be maintained.

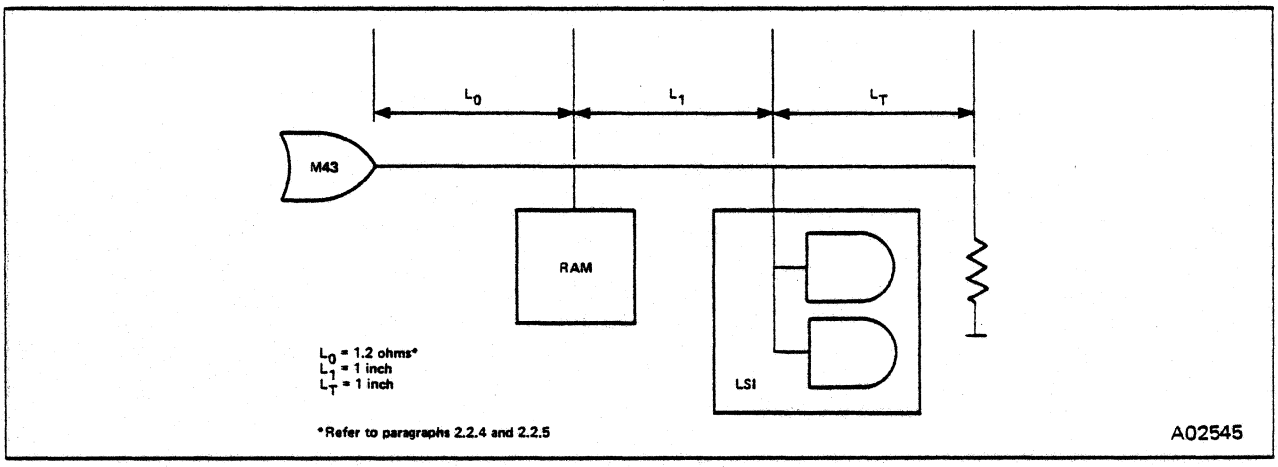

Figure 4-4. Spacing Restrictions

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4.9 RAM MODULE

The 580 RAM Module allows high speed Random Access Read-Write Memory to be packaged on an MCC. Four RAM chips are packaged in a Memory Module. Type I through Type VI Modules and Type VIII contain 4K bits of high speed RAM in various configurations. The Type VII Module contains 16K bits of a slower access time RAM. Refer to figure 4-5 for RAM Module I/O assignments. Figure 4-6 is a block diagram of the RAM Modules.

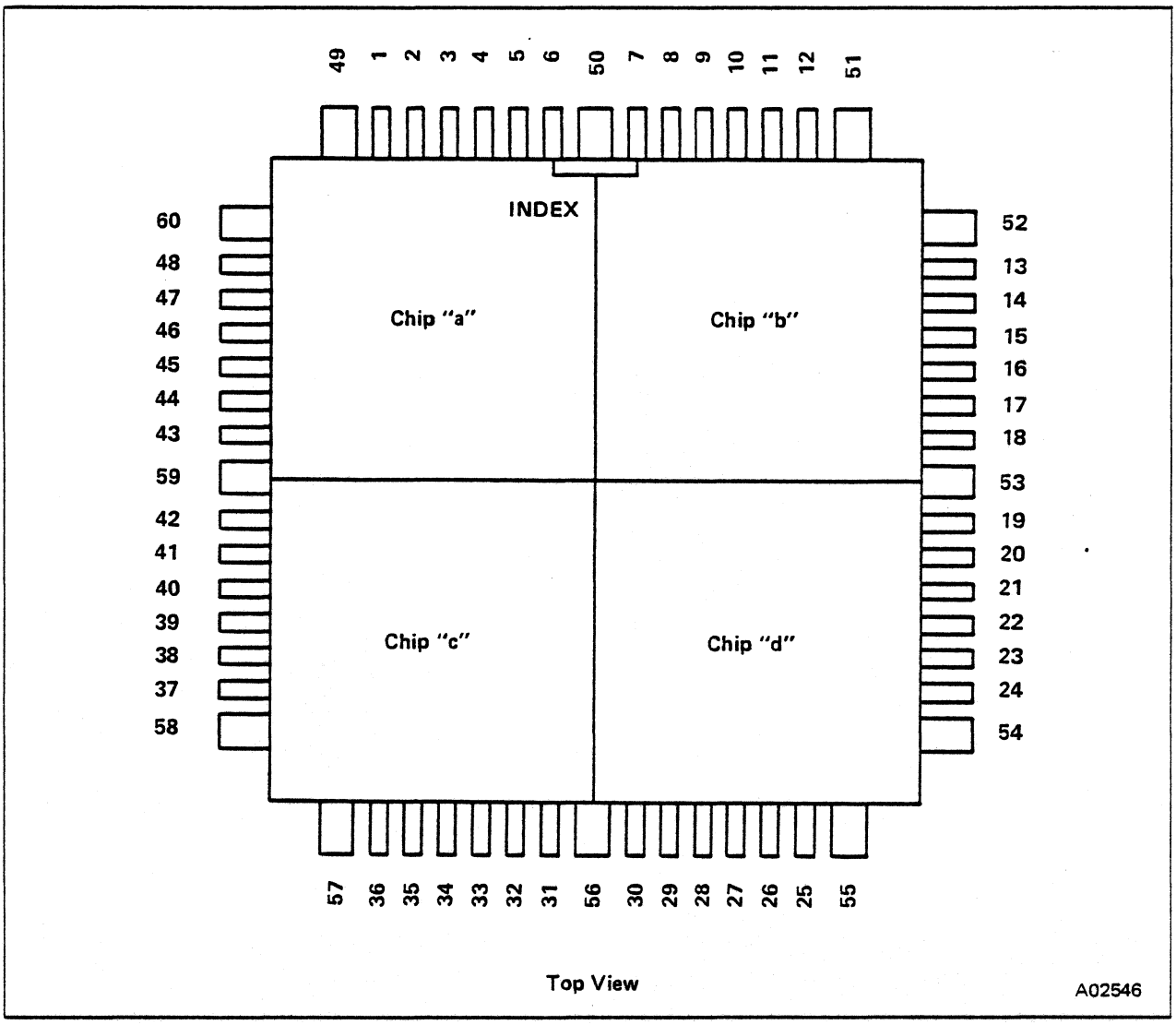

Figure 4-5. RAM Module I/O Assignments

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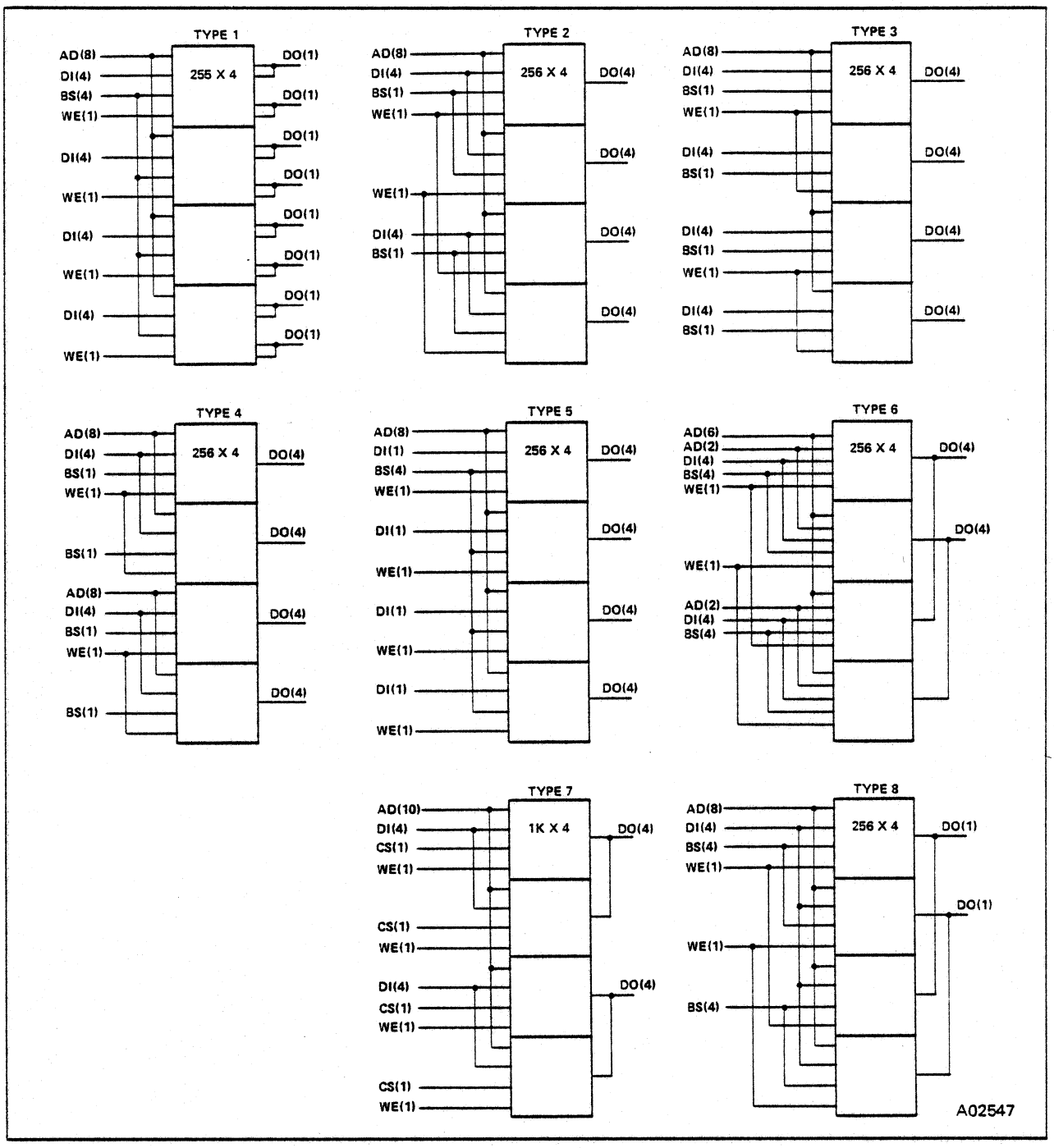

Figure 4-6. RAM Module Block Diagram

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Table 4-1 contains RAM Module I/O assignments, chip identification and the various RAM configurations. The following is a listing of RAM I/O pin names and abbreviations used in the table:

A_n	= Address input N
BS_n	= Block select n similar to chip select (CS) used on the 1K x 4 RAMs used in Type VII Module.
DI_n	= Data in n
DO_n	= Data out n
WE	= Write Enable
DO_1.ab	= Chip "a", Chip "b" Dot (between chips inside module)
DO_{12}.a	= DO1,DO2 Dot (betweeen pins on a single chip)
VCC,VCCO	= 0V
VEE_1	= -3.6V
VEE,VEE_2	= -5.2V
-----	= No connection

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Table 4-1. 580 RAM Module Pin Assignment

TYPE NO PIN NO	I MB76001	II MB76002	III MB76003	IV MB76004	V MB76005	VI MB76006	VII MB76007	VIII MB76008
1	$DO_{23.a}$	$DO_{3.a}$	$DO_{3.a}$	$DO_{3.a}$	$DO_{3.a}$	DO_{0ac}	$DO_{0.ab}$	$DO_{.ac}$
2	$DO_{01.a}$	$DO_{2.a}$	$DO_{2.a}$	$DO_{2.a}$	$DO_{2.a}$	$DO_{1.ac}$	$DO_{1.ab}$	–
3	A_0	A_0	A_0	$A_{0.ab}$	A_0	$A_{0.ab}$	$CS_{.a}$	A_0
4	A_1	A_1	A_1	$A_{1.ab}$	A_1	$A_{1.ab}$	–	A_1
5	A_2	A_2	A_2	$A_{2.ab}$	A_2	A_2	–	A_2
6	A_3	A_3	A_3	$A_{3.ab}$	A_3	A_3	–	A_3
7	$DO_{01.b}$	$DO_{0.b}$	$DO_{0.b}$	$DO_{0.b}$	$DO_{0.b}$	$DI_{0.ab}$	$DI_{0.ab}$	DI_0
8	$DO_{23.b}$	$DO_{1.b}$	$DO_{1.b}$	$DO_{1.b}$	$DO_{1.b}$	$DI_{1.ab}$	$DI_{1.ab}$	DI_1
9	$DI_{0.b}$	$DO_{2.b}$	$DO_{2.b}$	$DO_{2.b}$	$DO_{2.b}$	$DI_{2.ab}$	$CS_{.b}$	–
10	$DI_{1.b}$	$DO_{3.b}$	$DO_{3.b}$	$DO_{3.b}$	$DO_{3.b}$	$DI_{3.ab}$	–	–
11	A_4	A_4	A_4	$A_{4.ab}$	A_4	A_4	$DO_{2.ab}$	A_4
12	A_5	A_5	A_5	$A_{5.ab}$	A_5	A_5	$DO_{3.ab}$	A_5
13	A_6	A_6	A_6	$A_{6.ab}$	A_6	A_6	–	A_6
14	A_7	A_7	A_7	$A_{7.ab}$	A_7	A_7	$WE_{.b}$	A_7
15	$DI_{2.b}$	$DI_{1.ab}$	$DI_{1.b}$	$DI_{1.ab}$	$DI_{.b}$	–	A_0	–
16	$DI_{3.b}$	$DI_{0.ab}$	$DI_{0.b}$	$DI_{0.ab}$	BS_3	$BS_{0.ab}$	A_1	$BS_{0.ab}$
17	––	–	$BS_{.b}$	$BS_{.b}$	BS_2	$BS_{1.ab}$	–	$BS_{1.ab}$
18	$WE_{.b}$	$WE_{.bd}$	$WE_{.ab}$	$WE_{.ab}$	$WE_{.b}$	$WE_{.bd}$	A_2	$WE_{.bd}$
19	$WE_{.d}$	$BS_{.cd}$	$BS_{.d}$	$BS_{.d}$	$WE_{.d}$	–	$WE_{.d}$	–
20	–	–	–	–	–	$BS_{3.cd}$	A_3	$BS_{3.cd}$
21	BS_2	$DI_{3.cd}$	$DI_{3.b}$	$DI_{3.cd}$	–	$BS_{2.cd}$	A_4	$BS_{2.cd}$
22	BS_1	$DI_{2.cd}$	$DI_{2.b}$	$DI_{2.cd}$	$DI_{.d}$	–	–	–
23	–	$DO_{1.d}$	$DO_{1.d}$	$DO_{1.d}$	$DO_{1.d}$	$DO_{3.bd}$	$DI_{3.cd}$	–
24	–	$DO_{0.d}$	$DO_{0.d}$	$DO_{0.d}$	$DO_{0.d}$	$DO_{2.bd}$	$DI_{2.cd}$	–
25	$DO_{23.d}$	$DO_{3.d}$	$DO_{3.d}$	$DO_{3.d}$	$DO_{3.d}$	$DO_{0.db}$	$DO_{0.cd}$	$DO_{0.bd}$
26	$DO_{01.d}$	$DO_{2.d}$	$DO_{2.d}$	$DO_{2.d}$	$DO_{2.d}$	$DO_{1.bd}$	$DO_{1.cd}$	–
27	$DI_{3.d}$	–	$DI_{1.d}$	$A_{0.cd}$	–	$AO_{.cd}$	–	–
28	$DI_{2.d}$	–	$DI_{0.d}$	$A_{1.cd}$	–	$A_{1.cd}$	–	–
29	$DI_{1.d}$	–	$DI_{2.d}$	$A_{2.cd}$	–	–	–	–
30	$DI_{0.d}$	–	$DI_{3.d}$	$A_{3.cd}$	–	–	$CS_{.d}$	–
31	$DO_{01.c}$	$DO_{0.c}$	$DO_{0.c}$	$DO_{0.c}$	$DO_{0.c}$	$DI_{0.cd}$	$DI_{0.cd}$	–
32	$DO_{23.c}$	$DO_{1.c}$	$DO_{1.c}$	$DO_{1.c}$	$DO_{1.c}$	$DI_{1.cd}$	$DI_{1.cd}$	–
33	$DI_{0.c}$	$DO_{2.c}$	$DO_{2.c}$	$DO_{2.c}$	$DO_{2.c}$	$DI_{2.cd}$	$CS_{.c}$	DI_2
34	$DI_{1.c}$	$DO_{3.c}$	$DO_{3.c}$	$DO_{3.c}$	$DO_{3.c}$	$DI_{3.cd}$	–	DI_3
35	–	–	$DI_{2.c}$	$A_{4.cd}$	–	–	$DO_{2.cd}$	–

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Table 4—1. 580 RAM Module Pin Assignment

TYPE NO PIN NO	I MB76001	II MB76002	III MB76003	IV MB76004	V MB76005	VI MB76006	VII MB76007	VIII MB76008
36	–	–	$DI_{3.c}$	$A_{5.cd}$	–	–	$DO_{3.cd}$	–
37	$DI_{3.c}$	–	$DI_{1.c}$	$A_{6.cd}$	–	–	A_5	–
38	$DI_{2.c}$	–	$DI_{0.c}$	$A_{7.cd}$	–	–	A_6	–
39	BS_3	$DI_{1.cd}$	$DI_{3.a}$	$DI_{1.cd}$	$DI_{1.c}$	–	–	–
40	BS_0	$DI_{0.cd}$	$DI_{2.a}$	$DI_{0.cd}$	BS_0	$BS_{0.cd}$	–	$BS_{0.cd}$
41	–	–	$BS_{.c}$	$BS_{.c}$	BS_1	$BS_{1.cd}$	$WE_{.c}$	$BS_{1.cd}$
42	$WE_{.c}$	$WE_{.ac}$	$WE_{.cd}$	$WE_{.cd}$	$WE_{.c}$	$WE_{.ac}$	A_7	$WE_{.ac}$
43	$WE_{.a}$	$BS_{.ab}$	$BS_{.a}$	$BS_{.a}$	$WE_{.a}$	–	A_8	–
44	–	–	–	–	–	$BS_{3.ab}$	A_9	$BS_{3.ab}$
45	$DI_{0.a}$	$DI_{3.ab}$	$DI_{0.a}$	$DI_{3.ab}$	–	$BS_{2.ab}$	$WE_{.a}$	$BS_{2.ab}$
46	$DI_{1.a}$	$DI_{2.ab}$	$DI_{1.a}$	$DI_{2.ab}$	$DI_{.a}$	–	$DI_{3.ab}$	–
47	$DI_{2.a}$	$DO_{1.a}$	$DO_{1.a}$	$DO_{1.a}$	$DO_{1.a}$	$DO_{3.ac}$	$DI_{2.ab}$	–
48	$DI_{3.a}$	$DO_{0.a}$	$DO_{0.a}$	$DO_{0.a}$	$DO_{0.a}$	$DO_{2.ac}$	–	–
49	$VCC_{.a}$	$VCC_{.a}$	$VCC_{.a}$	$VCC_{.a}$	$VCC_{.a}$	$VCC_{.a}$	$VCC_{.a}$	$VCC_{.a}$
50	$VCC_{0.ab}$	$VCC_{0.ab}$	$VCC_{0.ab}$	$VCC_{0.ab}$	$VCC_{0.ab}$	$VCC_{0.ab}$	$VCC_{0.ab}$	$VCC_{0.ab}$
51	$VCC_{.b}$	$VCC_{.b}$	$VCC_{.b}$	$VCC_{.b}$	$VCC_{.b}$	$VCC_{.b}$	$VCC_{.b}$	$VCC_{.b}$
52	$VEE_{2.b}$	$VEE_{2.b}$	$VEE_{2.b}$	$VEE_{2.b}$	$VEE_{2.b}$	$VEE_{2.b}$	$VEE_{2.b}$	$VEE_{2.b}$
53	$VEE_{1.bd}$	$VEE_{1.bd}$	$VEE_{1.bd}$	$VEE_{1.bd}$	$VEE_{1.bd}$	$VEE_{1.bd}$	–	$VEE_{1.bd}$
54	$VEE_{2.d}$	$VEE_{2.d}$	$VEE_{2.d}$	$VEE_{2.d}$	$VEE_{2.d}$	$VEE_{2.d}$	$VEE_{.d}$	$VEE_{2.d}$
55	$VCC_{.d}$	$VCC_{.d}$	$VCC_{.d}$	$VCC_{.d}$	$VCC_{.d}$	$VCC_{.d}$	$VCC_{.d}$	$VCC_{.d}$
56	$VCC_{0.cd}$	$VCC_{0.cd}$	$VCC_{0.cd}$	$VCC_{0.cd}$	$VCC_{0.cd}$	$VCC_{0.cd}$	$VCC_{0.cd}$	$VCC_{0.cd}$
57	$VCC_{.c}$	$VCC_{.c}$	$VCC_{.c}$	$VCC_{.c}$	$VCC_{.c}$	$VCC_{.c}$	$VCC_{.c}$	$VCC_{.c}$
58	$VEE_{2.c}$	$VEE_{2.c}$	$VEE_{2.c}$	$VEE_{2.c}$	$VEE_{2.c}$	$VEE_{2.c}$	$VEE_{.c}$	$VEE_{2.c}$
59	$VEE_{1.ac}$	$VEE_{1.ac}$	$VEE_{1.ac}$	$VEE_{1.ac}$	$VEE_{1.ac}$	$VEE_{1.ac}$	–	$VEE_{1.ac}$
60	$VEE_{2.a}$	$VEE_{2.a}$	$VEE_{2.a}$	$VEE_{2.a}$	$VEE_{2.a}$	$VEE_{2.a}$	$VEE_{.a}$	$VEE_{2.a}$

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CHAPTER 5 - DELAY EQUATIONS

5.1 ON-CHIP DELAY EQUATION

Figure 5-1 illustrates the basic delay definition and measuring points. The basic section of delay is defined from the macro input pin of the driver circuit to the macro input pin of the receiver circuit of interest. The load of interest is affected by any loading within 1.6 inches of that load. Figure 5-2 shows the definition of switching types.

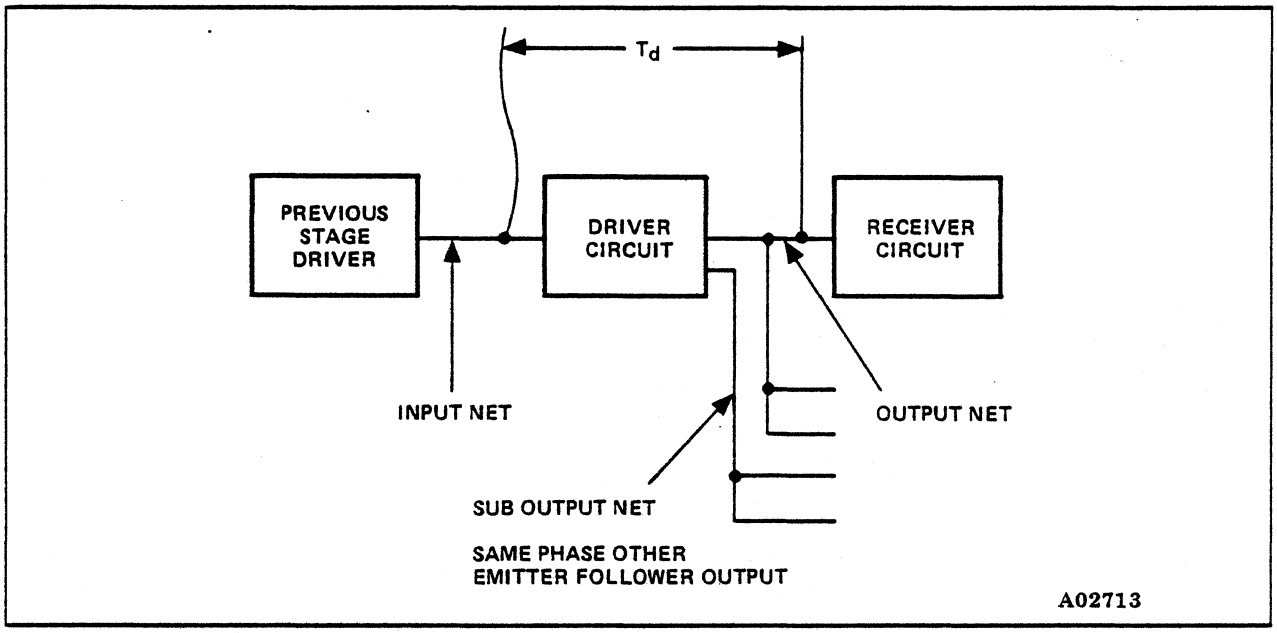

Figure 5-1. Delay Definition

Total delay time (T_d) of basic section is defined by the following equation:

$$T_d = T_{in} + T_{fanin} + T_{circuit} + T_{out} + T_{BD} + T_{EDOT} + T_{add}$$

where:

T_{in}	is the loading effect of the input net. It is actually the effect of input rise or fall time.
T_{fanin}	is the effect of the number of fan-ins.
$T_{circuit}$	is the basic circuit delay time. It is defined for each macro.

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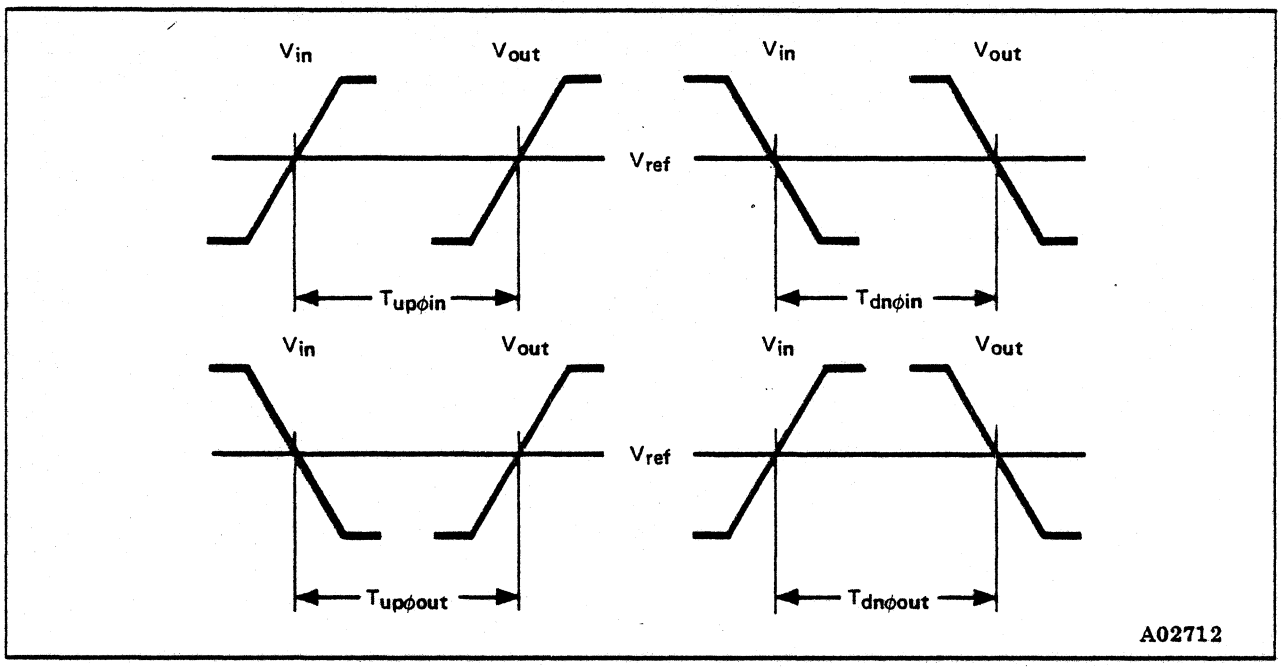

Figure 5-2. Definition of Switching Types

T_{out}	is the loading effect of the output net and sub-output net.
T_{BD}	is the effect of using the bias driver commonly. It occurs when another circuit in the same macro switches at the same time.
T_{EDOT}	is the loading effect of emitter follower dotting.
T_{add}	is the additional delay time of external emitter follower dotting, specified at the up-switching.

This Delay Equation is identical to the off-chip delay equation (paragraph 5.6) except for the T_{line} term which is omitted. Propagation delay is insignificant when on-chip.

5.2 ON-CHIP LOADING PARAMETERS

To calculate the term T_{in}, refer to paragraph 5.2.1. Loading parameters for $T_{circuit}$ and T_{out} are defined in paragraphs 5.2.2 and 5.2.3.

5.2.1 T_{in} Definitions

NINL Total number of low power bases including switching and non-switching in the input net of the circuit of interest.

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NINH Total number of high power bases including switching and non-switching in the input net of the circuit of interest.

SNINL Total number of low power switching bases in the input net of the circuit of interest.

SNINH Total number of high power switching bases in the input net of the circuit of interest.

MNIN Total loading units, except lower power and high power bases, in the input net of the circuit of interest.

5.2.2 $T_{circuit}$ Definitions

MEF The number of same phase multiple emitter follower outputs within one circuit.

M3 In the case of high power external gate, it is the total loading units in collector net from the macro output pin to the base terminal of the external emitter follower.

5.2.3 T_{out} Definitions

NONL Total number of low power bases including switching and non-switching in the output net of the circuit of interest.

NONH Total number of high power bases including switching and non-switching in the output net of the circuit of interest.

SNONL Total number of low power switching bases in the output net of the circuit of interest.

SNONH Total number of high power switching bases in the output net of the circuit of interest.

MNON Total loading units, except for low power and high power bases, of the output net of the circuit of interest.

5.3 ON-CHIP DELAY TERMS

The on-chip delay (picosecond, ps) equation is defined by the following terms.

5.3.1 T_{in} Definitions

T_{in} is a function of the power of the driver circuits, the power of the previous stage circuit, the pull down resistor of the previous one and the input transition type. It is defined by the following loading parameters (table 5-1).

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Table 5-1. T_{in} Definitions and Cross References

	T_{in} = (K1 x NINL) + (K2 x NINH) + (K3 x SNINL) + (K4 x SNINH) + (K5 x MNIN)							
DRIVER OF INTEREST	PREVIOUS STAGE	Rp	WAVEFORM*	K1	K2	K3	K4	K5
LOW POWER	Low Power	4K	UP	2	2	2	3	1
			DN	3	4	2	4	3
		2K	UP	2	2	2	3	1
			DN	2	3	2	3	2
	High Power Internal	4K	UP	2	2	2	3	1
			DN	3	4	2	4	3
		2K	UP	2	2	2	3	1
			DN	2	3	2	3	2
	High Pwr External	90	UP	6.2	8.4	3.4	4.8	1.2
			DN	7.3	9.6	0.5	0.9	1.3
HIGH POWER	Low Power	4K	UP	1	2	2	3	1
			DN	2	3	2	4	3
		2K	UP	1	2	2	3	1
			DN	2	2	2	3	2
	High Power Internal	4K	UP	1	2	2	3	1
			DN	2	3	2	4	3
		2K	UP	1	2	2	3	1
			DN	2	2	2	3	2
	High Pwr External	90	UP	6.2	8.4	3.4	4.8	1.2
			DN	7.3	9.6	0.5	0.9	1.3

*This is the phase of the waveform at the input of the driver of interest.

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5.3.2 T_{fanin} Definitions

The number for T_{fanin} is the number of inputs on the current switch connected to the input net.

T_{fanin} is a function of the power of the driver circuit and the switching type. T_{fanin} Definitions and Cross References are given in Table 5-2.

Table 5-2. T_{fanin} Definitions and Cross References

DRIVER CIRCUIT	SWITCHING TYPE	T_{fanin}(ps)							
		FANIN=1	FANIN=2	FANIN=3	FANIN=4	FANIN=5	FANIN=6	FANIN=7	FANIN=8
Low Power	$T_{up\ øin}$	0	−1	3	20	20			
	$T_{dn\ øin}$	0	−9	−1	52	42			
	$T_{up\ øout}$	0	−12	33	110	92	210	187	253
	$T_{dn\ øout}$	0	−2	67	127	128	199	196	269
High Power Int/ Ext	$T_{up\ øin}$	0	−3	−1	8	7			
	$T_{dn\ øin}$	0	−1	1	12	10			
	$T_{up\ øout}$	0	−5	17	36	30	63	56	78
	$T_{dn\ øout}$	0	−1	29	59	59	82	80	99

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5.3.3 $T_{circuit}$ Definitions

$T_{circuit}$ is the loading compensated delay of each macro. It is a function of the power of the driver circuit, pull down resistor, and the switching type. It is defined by the following formula.

$$T_{circuit} = T_B + [K6 \times (MEF-1)] + (K7 \times M3)$$

Where:

T_B is the basic delay time of each circuit.

MEF is the number of same phase emitter followers. Only more than 1 same phase emitter follower is penalized.

When determining which K6 coefficient to use with macros with multiple same phase emitter followers, the left column is for internal emitter followers and the right column is for external emitter followers. No more than 1 emitter follower per phase in any gate may drive off-chip.

5.3.4 Macro Identifications

Table 5-3 identifies the macros. Cross referenced on the table are the illustrated macro logic symbols and the associated tabularized macro characteristics described in the previous paragraphs.

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Table 5-3. Macro Identification and Description Locational Chart

MACRO ID.	MACRO DESCRIPTION	FIGURE NO.	TABLE NO.
01	Dual, 3-Input OR/NOR	5-3	5-4
02	Single, 5-Input, 2-OR/2-NOR	5-4	5-5
03	Dual, 3-Input, 2-NOR	5-5	5-6
04	Dual, 3-Input, 2-OR	5-6	5-7
05	Dual, 4-Input NOR	5-7	5-8
08	Single, 8-Input, 3-NOR	5-8	5-9
11	Two Wide,3-Input OR-AND/Dual,3-Input NOR	5-9	5-10
12	Two Wide, 3-Input NOR-AND/2-Wide, 3-Input OR-AND (Exclusive NOR)	5-10	5-11
13	Two Wide, 3-Input OR NOR-AND/2-Wide, 3-Input NOR OR-AND (Exclusive OR)	5-11	5-12
21	Three Input NOR/3-Input, 2-Sample Skewed Drive	5-12	5-13
22	Three Input, 3-Sample Skewed Driver	5-13	5-14
31	In-Phase Latch Without Scan-In/Scan-Out	5-14	5-15
32	Out-of-Phase Latch Without Scan-In/Scan-Out	5-15	5-16
42	OR Bus Driver	5-16	5-17
43	OR/NOR Memory Driver	5-17	5-18
0199	Four Wide,3-Input,2 OR-AND/Quad, 3-Input NOR	5-18	5-19
0299	Three Wide,3-Input,2 OR-AND/Quad, 3-Input NOR	5-19	5-20
2399	Clock Chopper	5-20	5-21
3199	Out-of-Phase Latch With Scan-In/Scan-Out	5-21	5-22
3299	In-Phase Latch With Scan-In/Scan-Out	5-22	5-23
3399	Out-of-Phase Latch With Scan-In/Scan-Out	5-23	5-24

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Table 5-4. Macro 01 Characteristics

INPUT PIN	OUTPUT PIN	PHASE
3, 4, 5	1	øin
3, 4, 5	2	øout
8, 9, 10	12	øin
8, 9, 10	11	øout

DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K7
Low Power	4K	Tup øin	380	
		Tdn øin	294	
		Tup øout	250	
		Tdn øout	315	
	2K	Tup øin	420	
		Tdn øin	275	
		Tup øout	280	
		Tdn øout	295	
High Power Internal	4K	Tup øin	300	
		Tdn øin	240	
		Tup øout	210	
		Tdn øout	255	
	2K	Tup øin	330	
		Tdn øin	225	
		Tup øout	230	
		Tdn øout	240	
High Power External	90	Tup øin	659	55
		Tdn øin	538	38
		Tup øout	479	40
		Tdn øout	540	35

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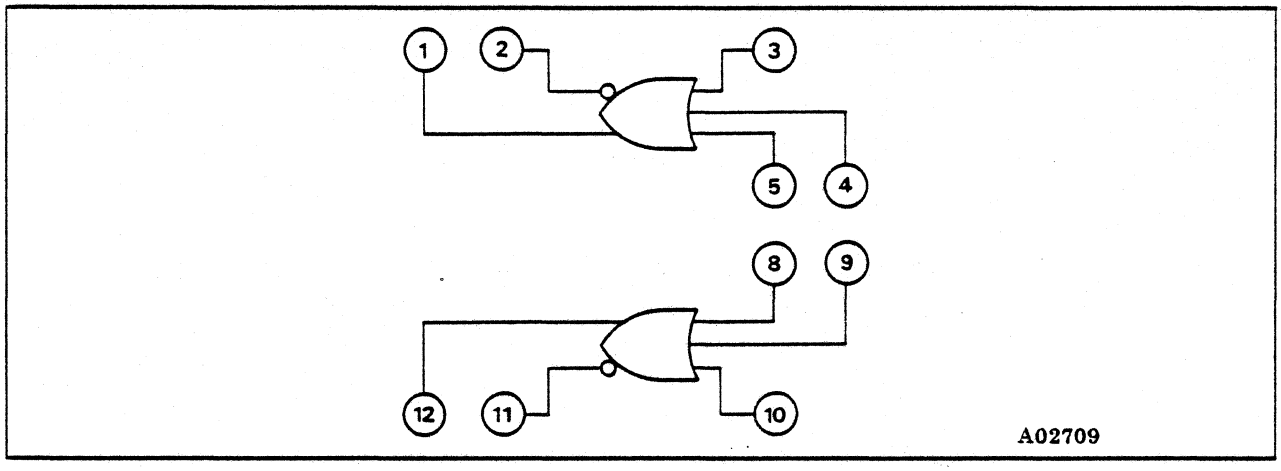

Figure 5-3. Dual, 3-Input OR/NOR Macro 01 (Half-Macro)

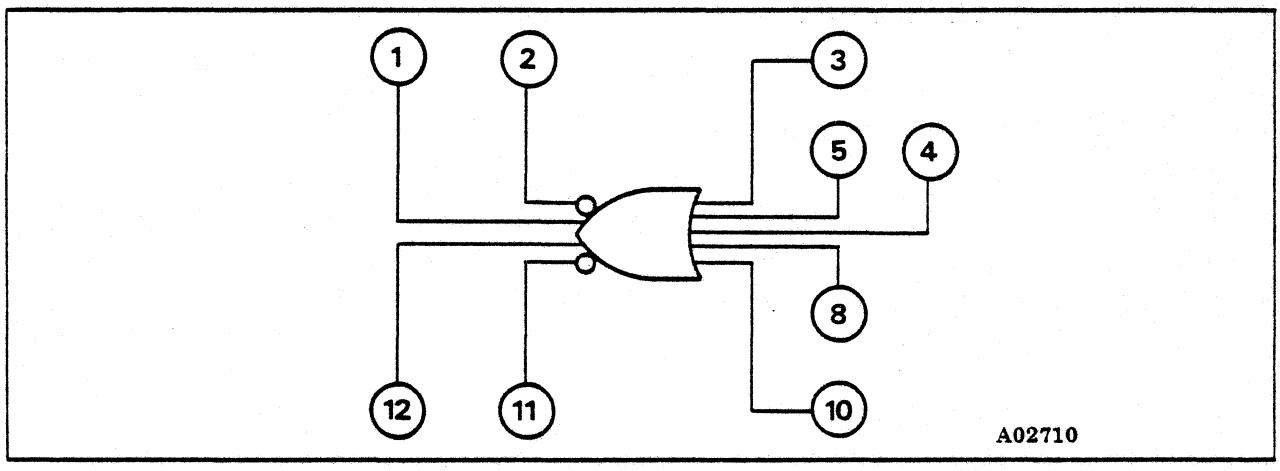

Figure 5-4. Single, 5-Input, 2 OR/2 NOR Macro 02 (Half-Macro)

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Table 5-5. Macro 02 Characteristics

INPUT PIN		OUTPUT PIN	PHASE		
3,4,5,8,10 3,4,5,8,10		1,12 2,11	øin øout		
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øin Tdn øin Tup øout Tdn øout	410 324 265 325	75 28 65 26	
	2K	Tup øin Tdn øin Tup øout Tdn øout	450 305 295 305	105 24 90 22	
High Power Internal	4K	Tup øin Tdn øin Tup øout Tdn øout	320 260 220 260	26 280 16 73 26 210 13 68	55 38 40 35
	2K	Tup øin Tdn øin Tup øout Tdn øout	350 245 240 245	30 280 16 61 30 210 13 62	55 38 40 35
High Power External	90	Tup øin Tdn øin Tup øout Tdn øout	679 558 484 545	30 16 30 16	55 38 40 35

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Table 5-6. Macro 03 Characteristics

INPUT PIN		OUTPUT PIN	PHASE		
3, 4, 5 8, 9, 10		1, 2 11, 12	øout øout		
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øout Tdn øout	250 315	65 26	
	2K	Tup øout Tdn øout	280 295	90 22	
High Power Internal	4K	Tup øout Tdn øout	210 255	26 210 13 68	40 35
	2K	Tup øout Tdn øout	230 240	30 210 13 62	40 35
High Pwr External	90	Tup øout Tdn øout	475 540	30 13	40 35

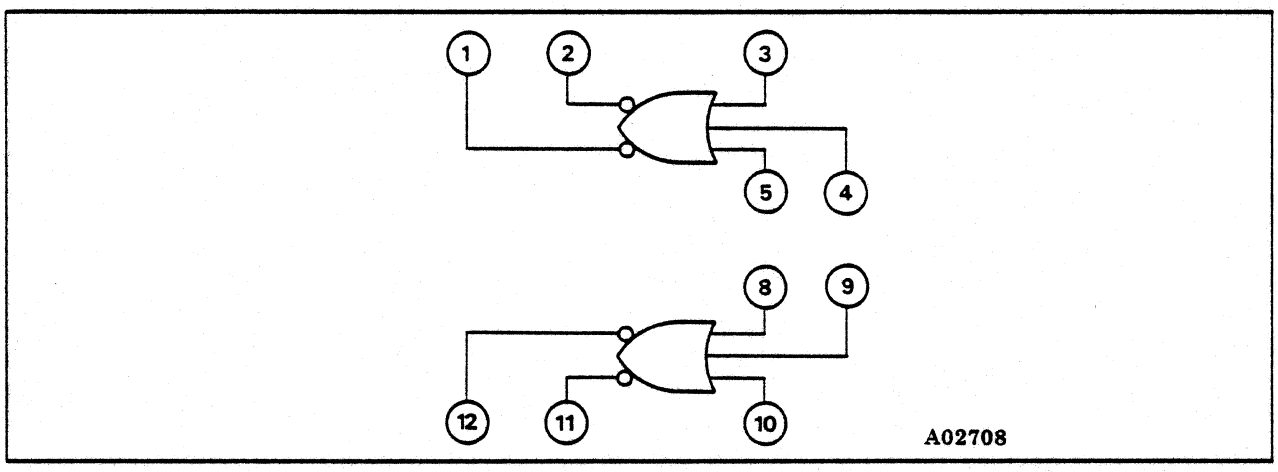

Figure 5-5. Dual, 3-Input, 2 NOR Macro 03 (Half-Macro)

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Table 5-7. Macro 04 Characteristics

INPUT PIN		OUTPUT PIN	PHASE		
3, 4, 5 8, 9, 10		1, 2 11, 12	øin øin		
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øin Tdn øin	380 294	75 28	
	2K	Tup øin Tdn øin	420 275	105 24	
High Power Internal	4K	Tup øin Tdn øin	300 240	26 280 16 73	55 38
	2K	Tup øin Tdn øin	330 225	30 280 16 61	55 38
High Pwr External	90	Tup øin Tdn øin	659 538	30 16	55 38

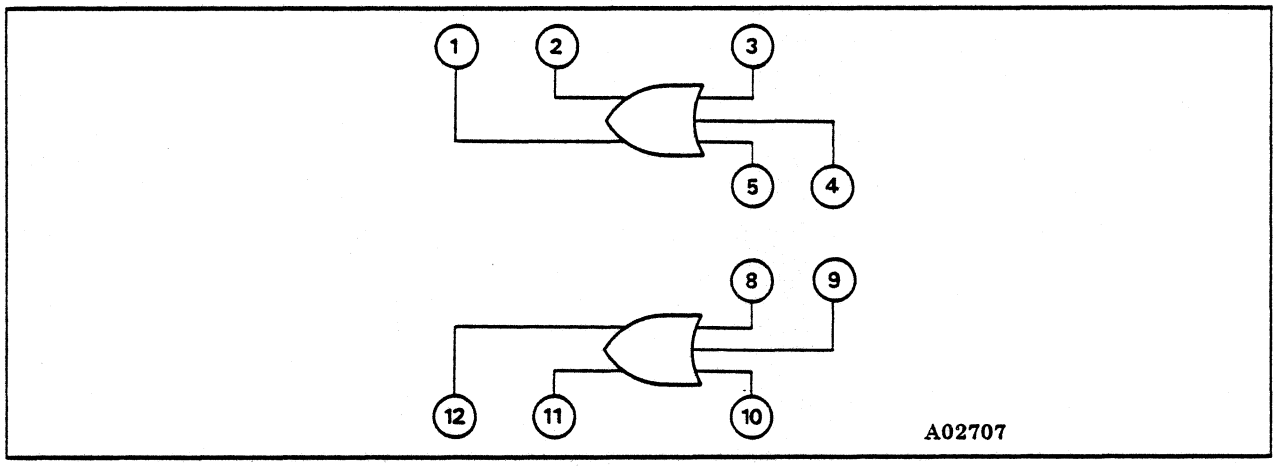

Figure 5-6. Dual, 3-Input, 2 OR Macro 04 (Half-Macro)

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Table 5-8. Macro 05 Characteristics

INPUT PIN		OUTPUT PIN	PHASE	
3, 4, 5, 6 7, 8, 9, 10		2 11	øout øout	
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K7
Low Power	4K	Tup øout Tdn øout	250 315	
	2K	Tup øout Tdn øout	280 295	
High Power Internal	4K	Tup øout Tdn øout	210 255	
	2K	Tup øout Tdn øout	230 240	
High Pwr External	90	Tup øout Tdn øout	475 540	40 35

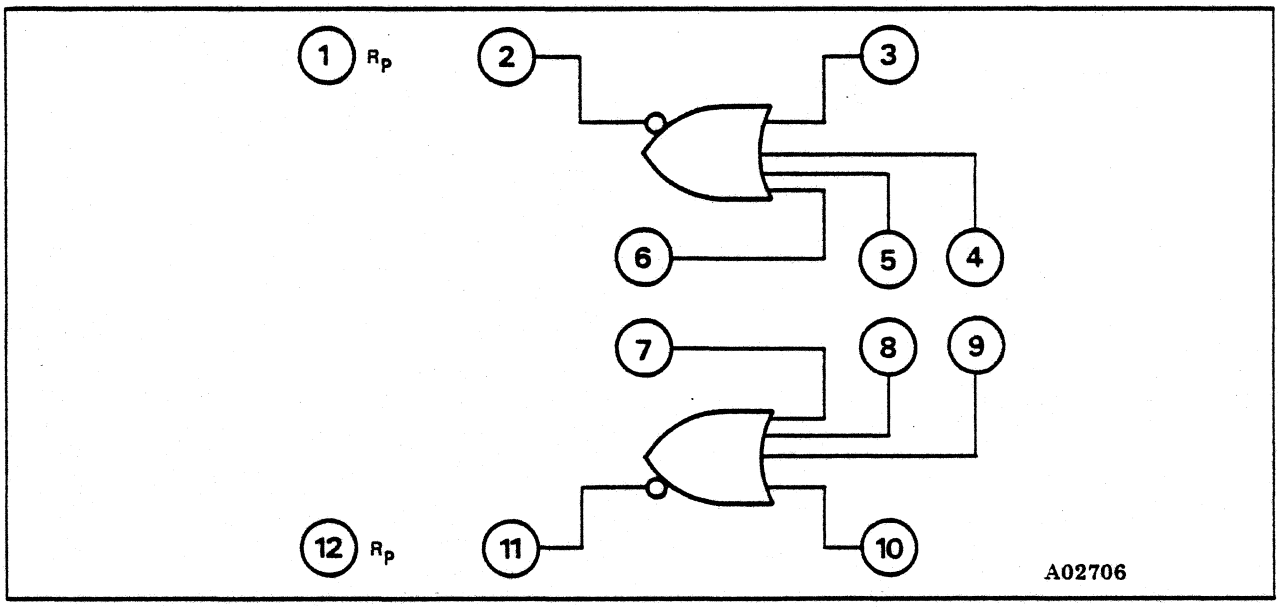

Figure 5-7. Dual, 4-Input NOR Macro 05 (Half-Macro)

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Table 5-9. Macro 08 Characteristics

INPUT PIN		OUTPUT PIN	PHASE		
3, 4, 5, 6, 7, 8, 9, 10		1, 2, 12	øout		
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øout Tdn øout	295 345	65 26	
	2K	Tup øout Tdn øout	325 325	90 22	
High Power Internal	4K	Tup øout Tdn øout	230 260	26 210 13 68	40 35
	2K	Tup øout Tdn øout	250 245	30 210 13 62	40 35
High Pwr External	90	Tup øout Tdn øout	495 545	30 13	40 35

This implementation of an 8 input NOR gate is dense but slow. It should be used only where power and space savings are desired on non-critical paths.

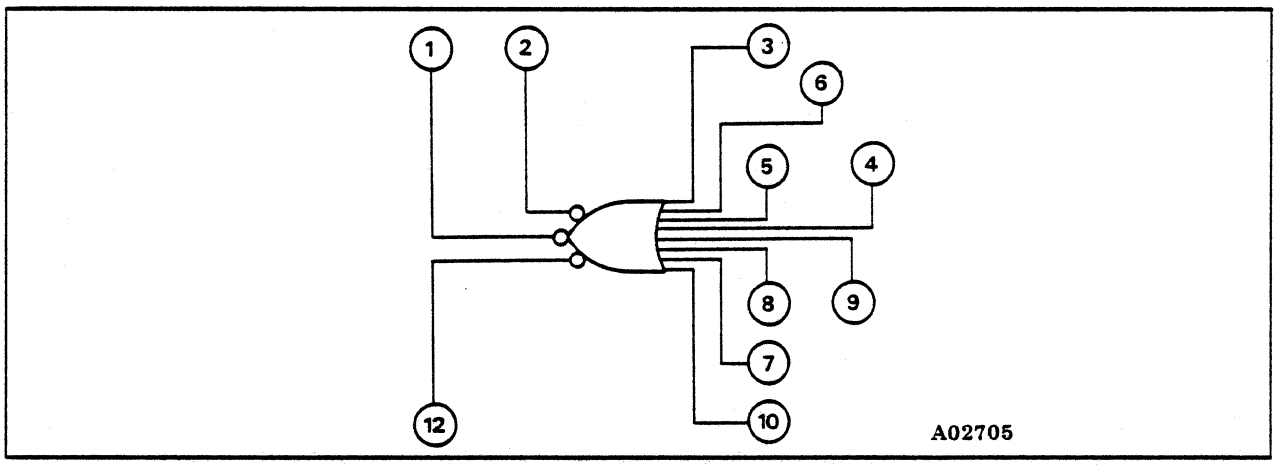

Figure 5-8. Single, 8-Input, 3 NOR Macro 08 (Half-Macro)

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Table 5-10. Macro 11 Characteristics

INPUT PIN		OUTPUT PIN	PHASE	
3, 4, 5 3, 4, 5 8, 9, 10 8, 9, 10		1 2 1 11	øin øout øin øout	
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K7
Low Power	4K	Tup øin Tdn øin	587 370	
	2K	Tup øin Tdn øin	627 350	
High Power Internal	4K	Tup øin Tdn øin	439 295	
	2K	Tup øin Tdn øin	469 280	
High Pwr External	90	Tup øin Tdn øin	800 595	55 38
$T_{up\ øout}$ and $T_{dn\ øout}$ are equal to that of Macro 01.				

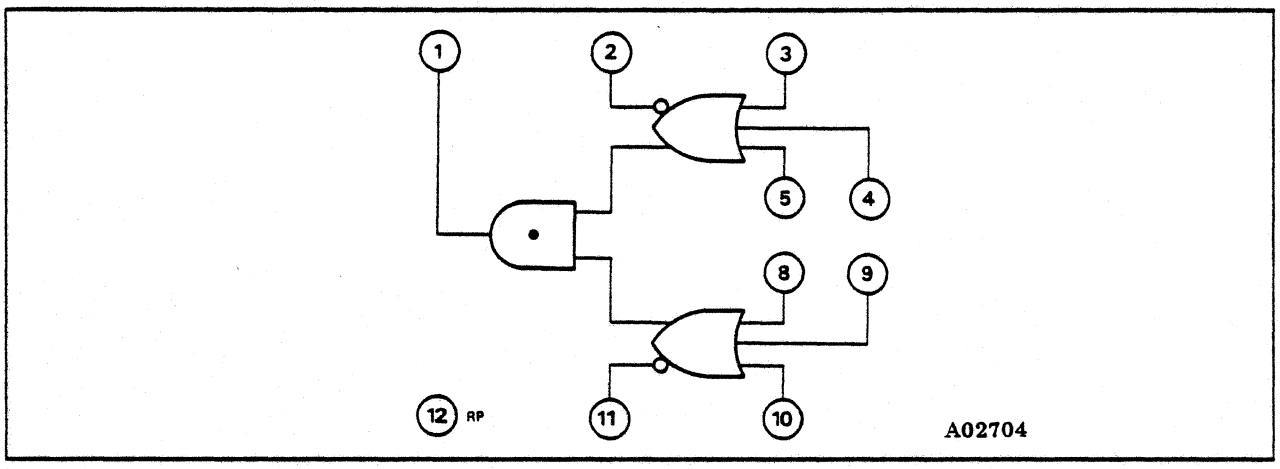

Figure 5-9. Two Wide, 3-Input OR-AND/Dual, 3-Input NOR Macro 11

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Table 5-11. Macro 12 Characteristics

INPUT PIN		OUTPUT PIN	PHASE	
3, 4, 5 3, 4, 5 8, 9, 10 8, 9, 10		1 2 1 2	ϕin ϕout ϕin ϕout	
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K7
Low Power	4K	Tup ϕin Tdn ϕin Tup ϕout Tdn ϕout	590 370 430 390	
	2K	Tup ϕin Tdn ϕin Tup ϕout Tdn ϕout	630 350 460 370	
High Power Internal	4K	Tup ϕin Tdn ϕin Tup ϕout Tdn ϕout	440 295 330 310	
	2K	Tup ϕin Tdn ϕin Tup ϕout Tdn ϕout	470 280 350 295	
High Power External	90	Tup ϕin Tdn ϕin Tup ϕout Tdn ϕout	800 595 590 595	55 38 40 35

An exclusive NOR function can be performed by optionally connecting output pins 1 and 2.

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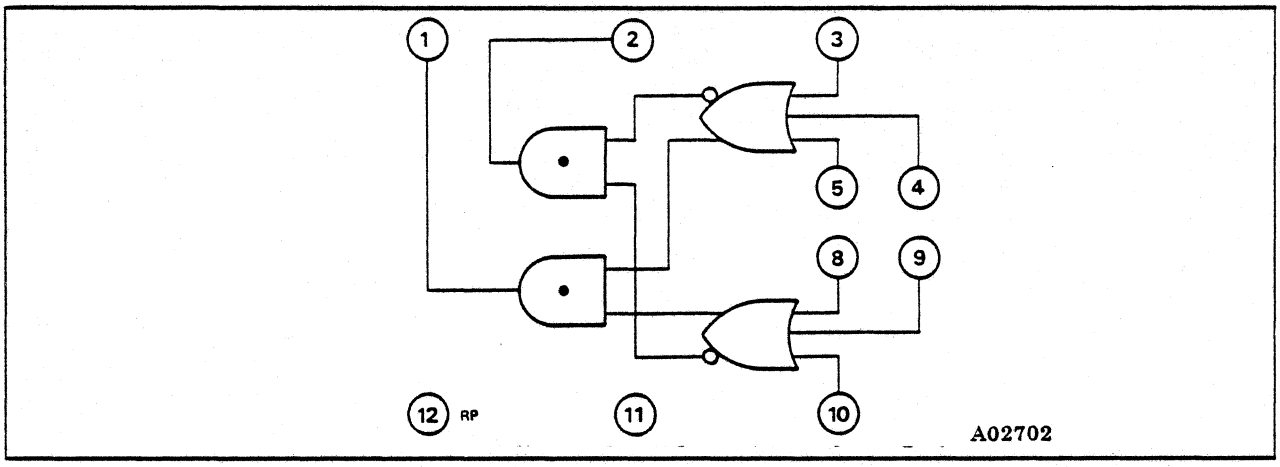

Figure 5-10. Two Wide, 3-Input NOR-AND/2-WIDE, 3-Input OR-AND Macro 12

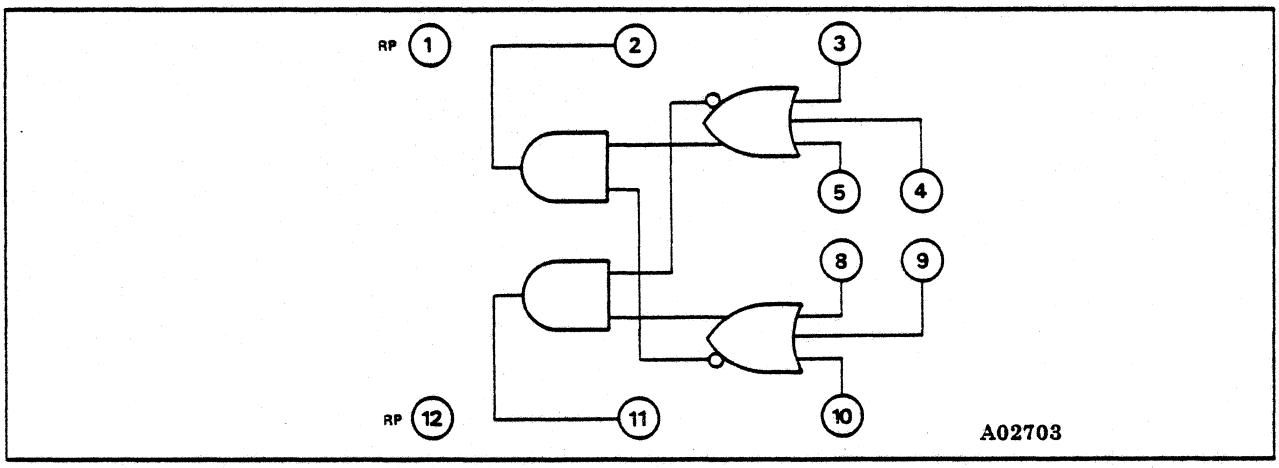

Figure 5-11. Macro 13

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Table 5-12. Macro 13 Characteristics

INPUT PIN		OUTPUT PIN	PHASE	
3, 4, 5 3, 4, 5 8, 9, 10 8, 9, 10		2 11 2 11	øin øout øout øin	
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K7
Low Power	4K	Tup øin Tdn øin Tup øout Tdn øout	550 390 430 390	
	2K	Tup øin Tdn øin Tup øout Tdn øout	590 370 460 370	
High Power Internal	4K	Tup øin Tdn øin Tup øout Tdn øout	475 320 420 300	
	2K	Tup øin Tdn øin Tup øout Tdn øout	505 305 450 285	
High Power External	90	Tup øin Tdn øin Tup øout Tdn øout	850 630 800 560	55 38 55 38

An exclusive OR function can be performed by optionally connecting output pins 1 and 2.

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Table 5-13. Macro 21 Characteristics

INPUT PIN		OUTPUT PIN	PHASE	
8, 9, 10 8, 9, 10 3, 4, 5		1, 12 11 2	ϕin ϕout ϕout	
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6
Low Power	4K	Tup ϕin Tdn ϕin	680 250	120 26
	2K	Tup ϕin Tdn ϕin	740 230	160 20
$T_{up\phi out}$ and $T_{dn\phi out}$ are equal to that of Macro 01.				

The skewed driver must be implemented by a low power cell. The skewed driver in-phase output should not drive off-chip. To preserve the skew, both outputs always have two pulldown resistors. Both types of outputs should have roughly equal loads. Skewed drivers must be used for driving the clock inputs of latches.

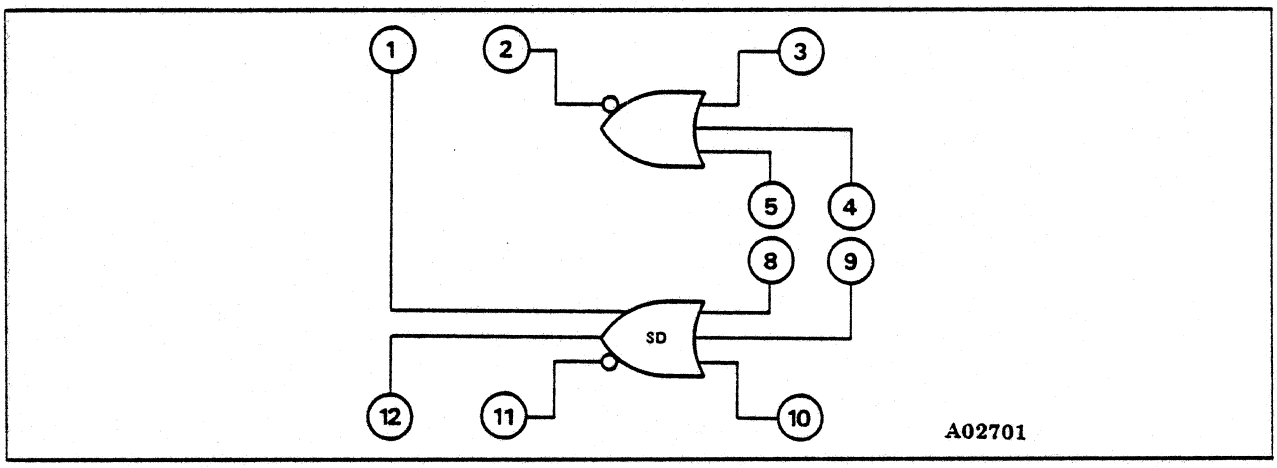

Figure 5-12. 3-Input NOR/3 Input 2 Sample Skewed Driver Macro 21

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Table 5-14. Macro 22 Characteristics

INPUT PIN		OUTPUT PIN	PHASE
8, 9, 10 8, 9, 10		1, 2, 12 11	ϕin ϕout
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B
Low Power	4K	Tup ϕin Tdn ϕin	990 310
	2K	Tup ϕin Tdn ϕin	1150 280
$T_{up\,\phi out}$ and $T_{dn\,\phi out}$ are equal to that of Macro 01. T_B in the table includes the delay time of MEF.			

Refer to Macro 21 for usage.

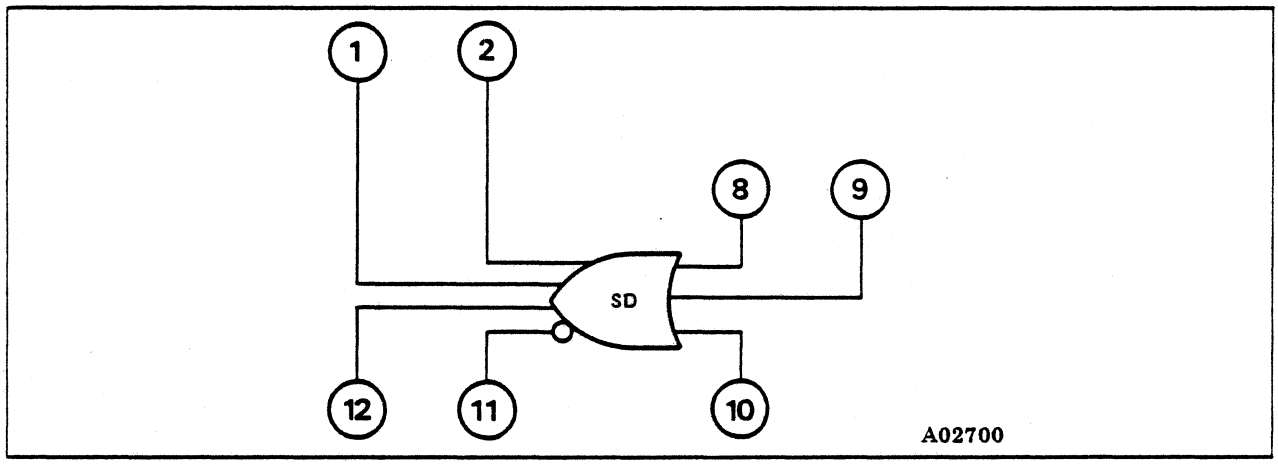

Figure 5-13. 3-Input, 3 Sample Skewed Driver Macro 22 (Half-Macro)

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Table 5-15. Macro 31 Characteristics

INPUT PIN		OUTPUT PIN	PHASE		
1, 4, 5 1, 4, 5 8, 9, 10 8, 9, 10		1, 12 2 1, 12 11	øin øout øin øout		
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øin Tdn øin	455 335	75 28	
	2K	Tup øin Tdn øin	495 315	105 24	
High Power Internal	4K	Tup øin Tdn øin	350 270	26 280 16 73	55 38
	2K	Tup øin Tdn øin	380 255	30 280 16 61	55 38
High Pwr External	90	Tup øin Tdn øin	710 570	30 16	55 38
$T_{up\ øout}$ and $T_{dn\ øout}$ are equal to that of the Macro 01.					

Macro 31 has no associated scan circuitry. For this reason, it is generally used only as a slave in a master-slave type latch. The in-phase latch is inherently faster than the out-of-phase latch and will function properly with either skewed driver macro.

Output 1 cannot be deleted nor used as a high power output for driving a line chip- off. To produce an out-of-phase output, output ports 11 and 2 must be dotted outside the macro.

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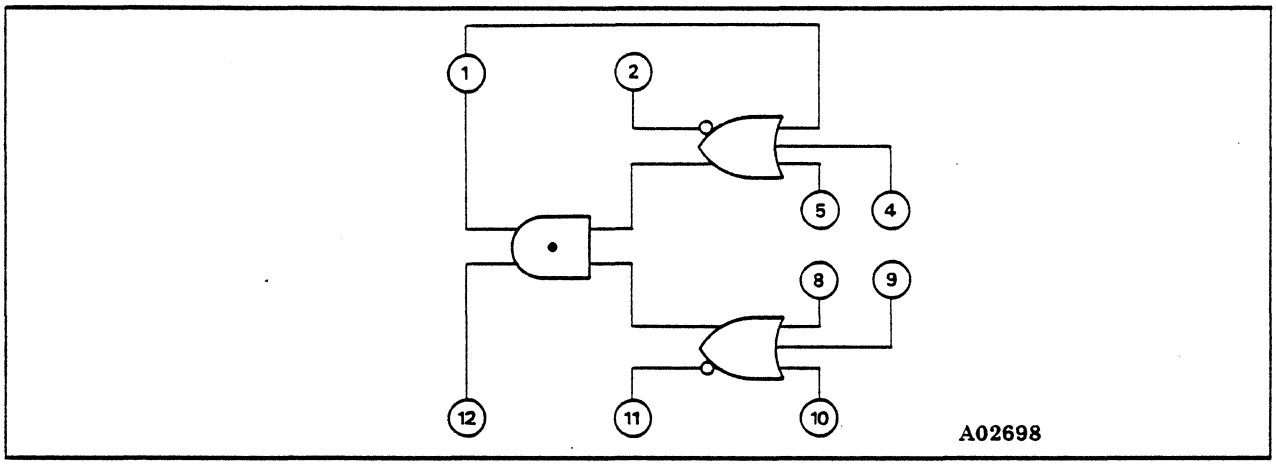

Figure 5-14. In-Phase Latch without Scan-In/Scan-Out Macro 31

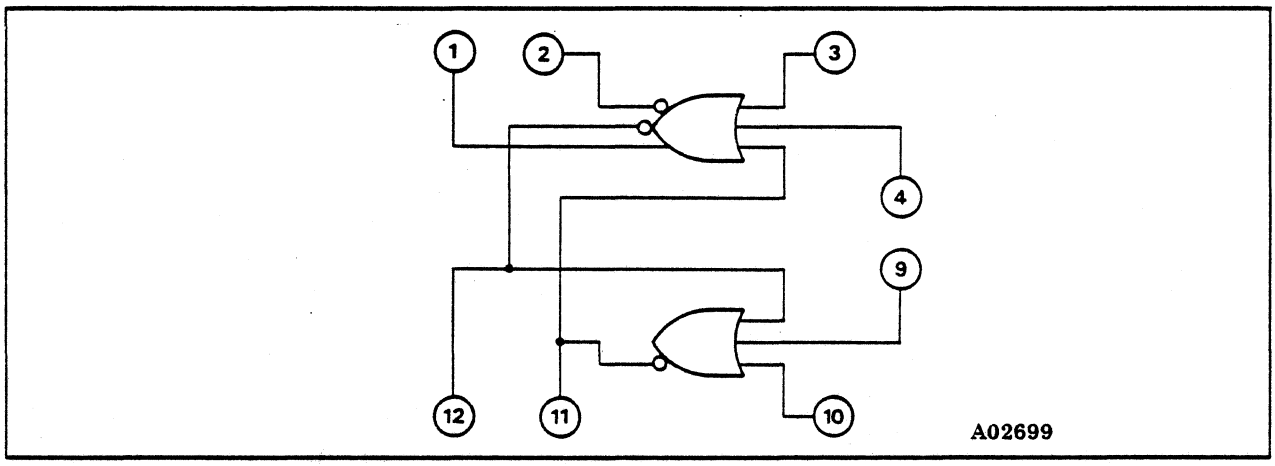

Figure 5-15. Out-of-Phase Latch without Scan-In/Scan-Out Macro 32

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Table 5-16. Macro 32 Characteristics

INPUT PIN		OUTPUT PIN	PHASE		
3, 4, 11 3, 4, 11		1 2, 12	øin øout		
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øin Tdn øin Tup øout Tdn øout	390 304 275 335	 65 26	
	2K	Tup øin Tdn øin Tup øout Tdn øout	430 285 305 315	 90 22	
High Power	4K	Tup øin Tdn øin Tup øout Tdn øout	310 250 225 265	 26 210 13 68	 40 35
Internal	2K	Tup øin Tdn øin Tup øout Tdn øout	340 235 245 250	 30 210 13 62	 40 35
High Pwr External	90	Tup øin Tdn øin Tup øout Tdn øout	669 548 490 550	 30 13	55 38 40 35
$T_{up\ øin}$ and $T_{dn\ øin}$ are equal to that of the Macro 01.					

INPUT PIN	OUTPUT PIN	PHASE
9, 10, 12	11	øout
$T_{up\ øout}$ and $T_{dn\ øout}$ are equal to that of the Macro 01.		

The latch macro has no associated scan circuitry. For this reason, it is used only as a slave in a master-slave type latch.

Output ports 11 and 12 are available for on-chip connections, but they cannot drive off-chip. Full fanout on these outputs is not available. The external data gates must be present for this latch to work. Refer to paragraph 7 for latch rules.

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Table 5-17. Macro 42 Characteristics

INPUT PIN		OUTPUT PIN	PHASE	
3, 10		1, 12	øin	
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K7
High Pwr External	90 (45)	Tup øin Tdn øout	820 (960) 440 (440)	39 11
M3 is the sum of the loading units of each collector net.				

Buses, bidirectional transmission lines, should only be driven with the bus driver macro. The bus driver macro can source enough current to drive a 50 ohm line, and has a V_{OL} which is lower than -2.0 volts. Noise generation is minimal. A bus driver macro cannot be implemented in a lower power cell nor can it drive internal outputs. Normally the bus driver macro output connects to two on-chip external emitter following transistors in parallel. Each input is counted as two bases (refer to chapter 2.3.3).

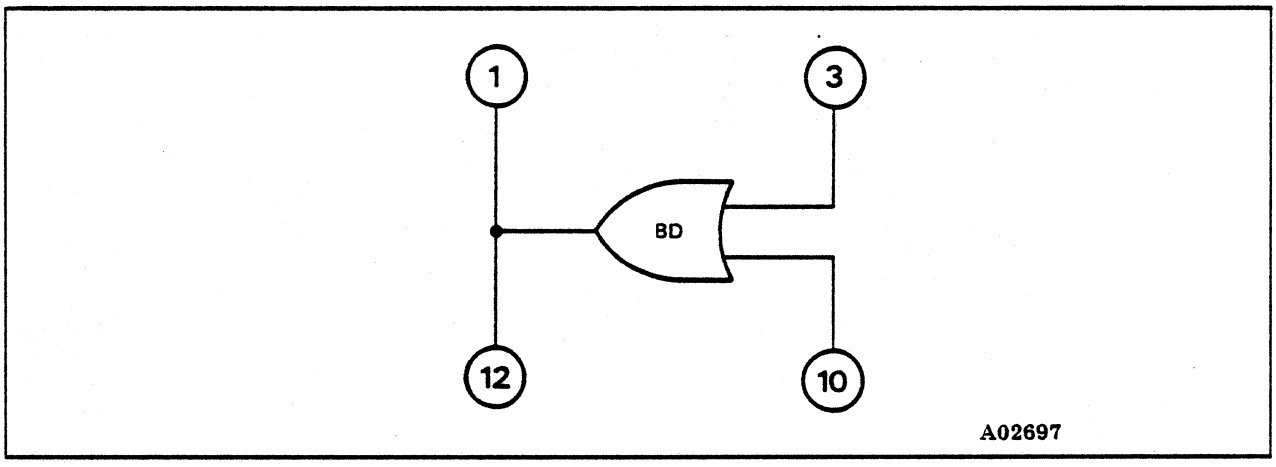

Figure 5-16. OR Bus Driver Macro 42 (Half-Macro)

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Table 5-18. Macro 43 Characteristics

INPUT PIN		OUTPUT PIN	PHASE	
3, 4, 10 3, 4, 10		1, 12 2, 11	ϕin ϕout	
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K7
High Power Internal	4K	Tup ϕin Tdn ϕin Tup ϕout Tdn ϕout	290 240 200 225	
	2K	Tup ϕin Tdn ϕin Tup ϕout Tdn ϕout	310 230 220 215	
High Power External	90 (45)	Tup ϕin Tdn ϕin Tup ϕout Tdn ϕout	570 (650) 531 (541) 410 (400) 535 (560)	28 20 20 18
M3 of the ϕin is the total loading units of the ϕin collector nets. M3 of the ϕout is the total loading units of the ϕout collector nets.				

This macro is used to drive RAM inputs and to drive off MCC loads. It has both in-phase and out-of-phase outputs which can drive heavily capacitive 50 ohm nets. Macro 43 cannot be implemented in a lower power cell (refer to chapter 4). Each input is counted as two bases.

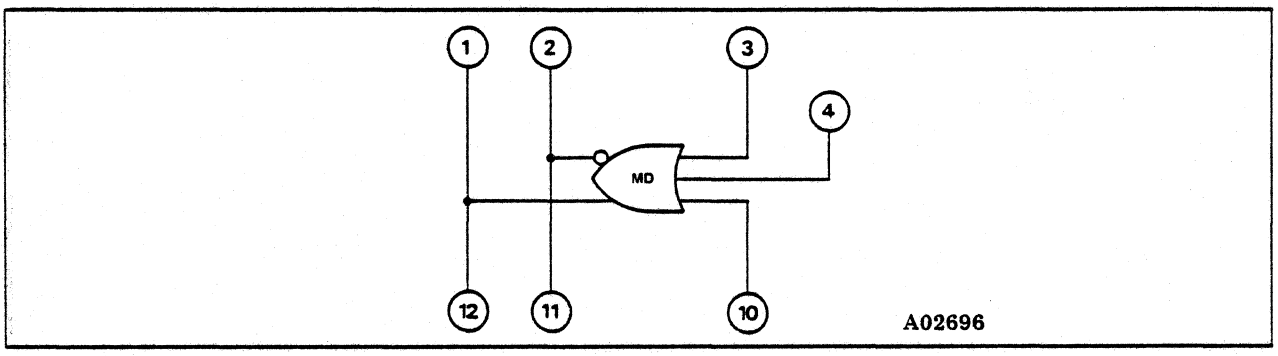

Figure 5-17. OR/NOR Memory Driver Macro 43 (Half-Macro)

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Table 5-19. Macro 0199 Characteristics

INPUT PIN	OUTPUT PIN	PHASE
3, 4, 5	1, 13	øin
3, 4, 5	2	øout
8, 9, 10	1, 13	øin
8, 9, 10	11	øout
15, 16, 17	1, 13	øin
15, 16, 17	14	øout
20, 21, 22	1, 13	øin
20, 21, 22	23	øout

DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øin	815	75	
		Tdn øin	560	28	
	2K	Tup øin	855	105	
		Tdn øin	540	24	
High Power Internal	4K	Tup øin	555	26 280	55
		Tdn øin	395	16 73	38
	2K	Tup øin	585	30 280	55
		Tdn øin	380	16 61	38
High Pwr External	90	Tup øin	905	30	55
		Tdn øin	695	16	38

$T_{up\ øout}$ and $T_{dn\ øout}$ are equal to that of the Macro 01.

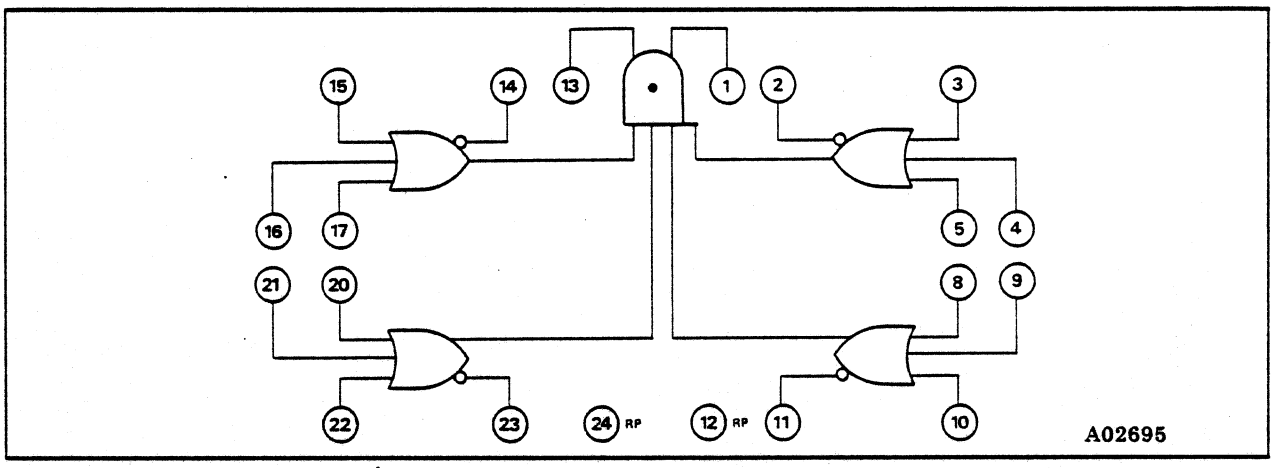

Figure 5-18. Macro 0199

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Table 5-20. Macro 0299 Characteristics

INPUT PIN	OUTPUT PIN	PHASE
3, 4, 5	1, 13	øin
3, 4, 5	2	øout
8, 9, 10	1, 13	øin
8, 9, 10	11	øout
20, 21, 22	1, 13	øin
20, 21, 22	23	øout
15, 16, 17	14	øout

DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øin	775	75	
		Tdn øin	525	28	
	2K	Tup øin	815	105	
		Tdn øin	505	24	
High Power Internal	4K	Tup øin	535	26 280	55
		Tdn øin	375	16 73	38
	2K	Tup øin	565	30 280	55
		Tdn øin	360	16 61	38
High Pwr External	90	Tup øin	885	30	55
		Tdn øin	675	16	38

$T_{up\ øout}$ and $T_{dn\ øout}$ are equal to that of the Macro 01.

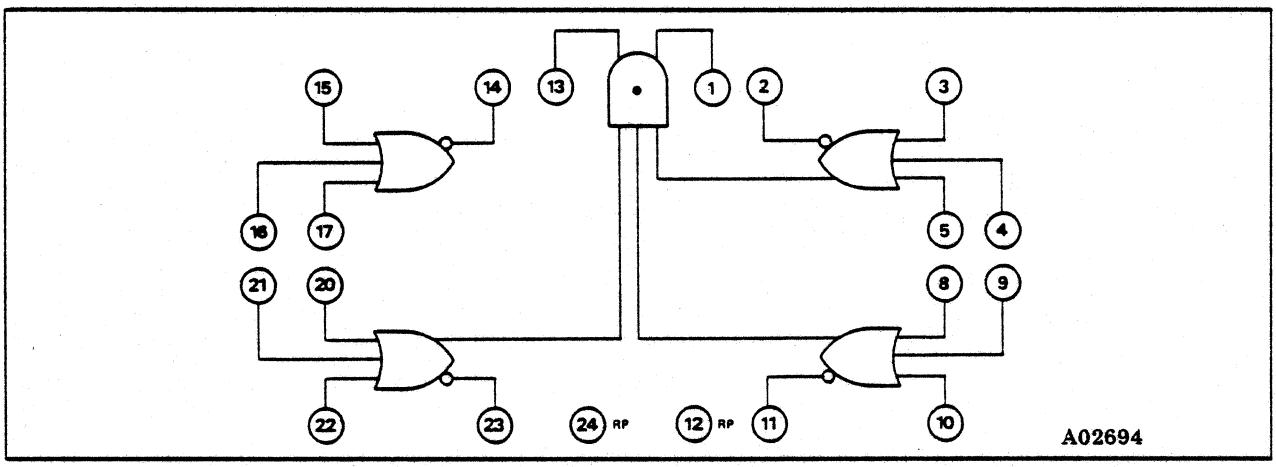

Figure 5-19. Macro 0299

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Table 5-21. Macro 2399 Characteristics

INPUT PIN		OUTPUT PIN	PHASE
15 15, 17		1, 12, 13 1, 12, 13	øin øout
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B
Low Power	2K	Tup øin Tdn øin Tup øout Tdn øout	770 330 2270 1580
T_B includes the delay time of MEF.			

INPUT PIN		OUTPUT PIN	PHASE
15 15, 17		2 2	øout øin
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B
Low Power	2K	Tup øin Tdn øin Tup øout Tdn øout	1570 1850 320 350

INPUT PIN		OUTPUT PIN	PHASE
8 8		1, 12, 13 2	øin øout
DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B
Low Power	2K	Tup øin Tdn øin Tup øout Tdn øout	1220 680 670 800
T_B includes the delay time of MEF.			

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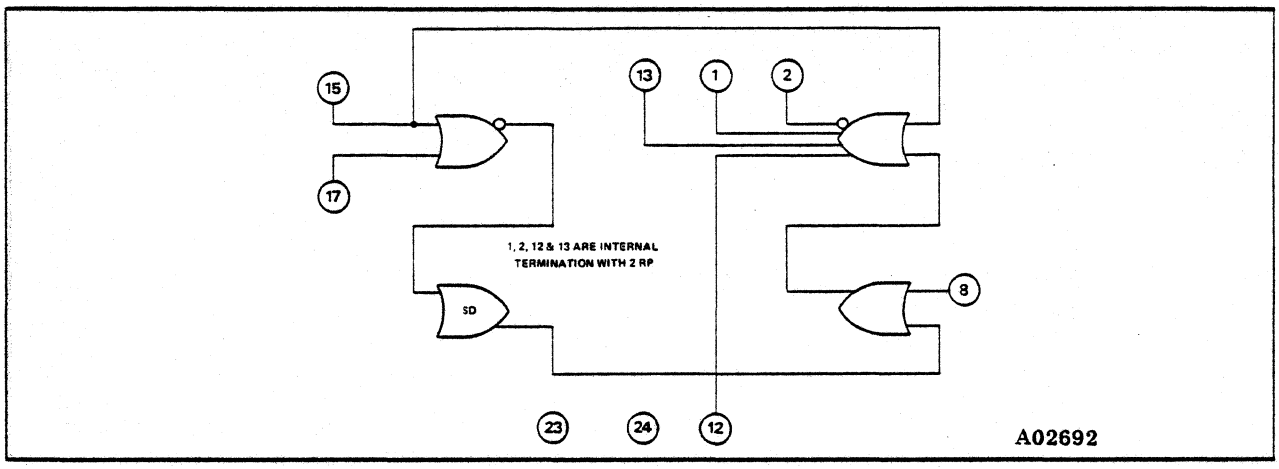

Figure 5-20. Clock Chopper Macro 2399 (Full Macro)

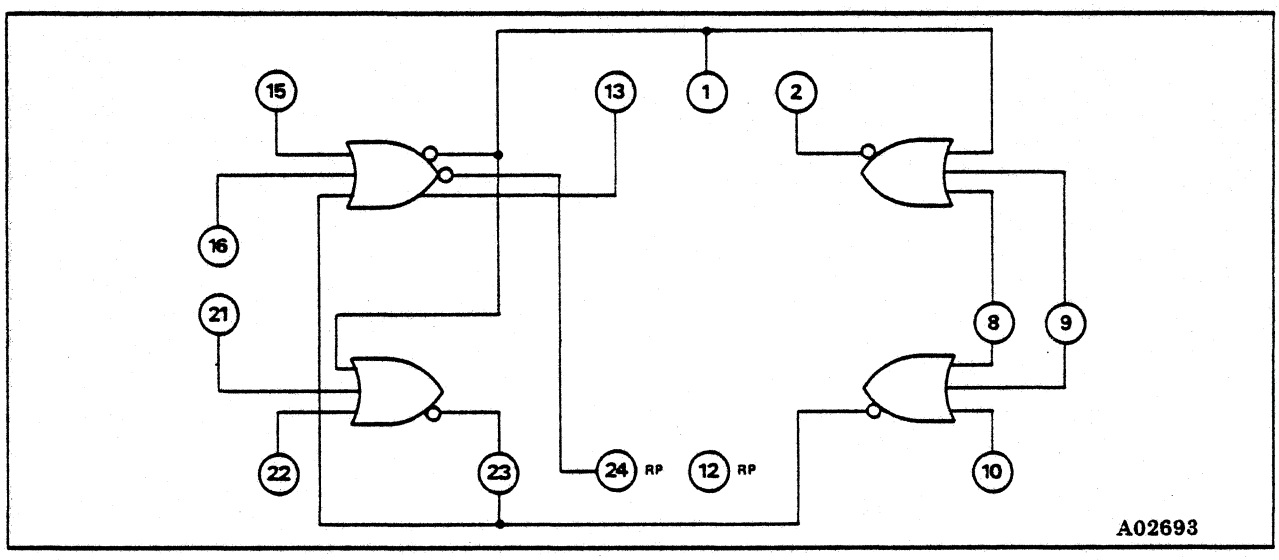

Figure 5-21. Out-of-Phase Latch with Scan-In/Scan-Out Macro 3199

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Table 5-22. Macro 3199 Characteristics

INPUT PIN	OUTPUT PIN	PHASE
15, 16, 23 15, 16, 23	13 1, 24	øin øout

DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øin	410		
		Tdn øin	324		
		Tup øout	265	65	
		Tdn øout	325	26	
	2K	Tup øin	450		
		Tdn øin	305		
		Tup øout	295	90	
		Tdn øout	305	22	
High Power Internal	4K	Tup øin	320		
		Tdn øin	260		
		Tup øout	220	26 210	40
		Tdn øout	260	13 68	35
	2K	Tup øin	350		
		Tdn øin	245		
		Tup øout	240	30 210	40
		Tdn øout	245	13 62	35
High Power External	90	Tup øin	679		55
		Tdn øin	558		38
		Tup øout	485	30	40
		Tdn øout	545	13	35

INPUT PIN	OUTPUT PIN	PHASE
1, 8, 9	2	øout
8, 9, 10	23	øout
1, 21, 22	23	øout

$T_{up\ øout}$ and $T_{dn\ øout}$ are equal to that of the Macro 01.

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Table 5-23. Macro 3299 Characteristics

INPUT PIN	OUTPUT PIN	PHASE
3, 4, 5	1, 13	øin
15, 16, 17	1, 13	øin
15, 16, 17	14	øout
1, 20, 21	1, 13	øin
1, 20, 21	23	øout

DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øin	715	75	
		Tdn øin	470	28	
	2K	Tup øin	755	105	
		Tdn øin	450	24	
High Power Internal	4K	Tup øin	500	26 280	55
		Tdn øin	345	16 73	38
	2K	Tup øin	530	30 280	55
		Tdn øin	330	16 61	38
High Pwr External	90	Tup øin	850	30	55
		Tdn øin	645	16	38

$T_{up\ øout}$ and $T_{dn\ øout}$ are equal to that of the Macro 01.

INPUT PIN	OUTPUT PIN	PHASE
1, 4, 5	11	øout

DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K7
Low Power	4K	Tup øout	250	
		Tdn øout	315	
	2K	Tup øout	280	
		Tdn øout	295	
High Power Internal	4K	Tup øout	210	
		Tdn øout	255	
	2K	Tup øout	230	
		Tdn øout	240	
High Pwr External	90	Tup øout	475	40
		Tdn øout	540	35

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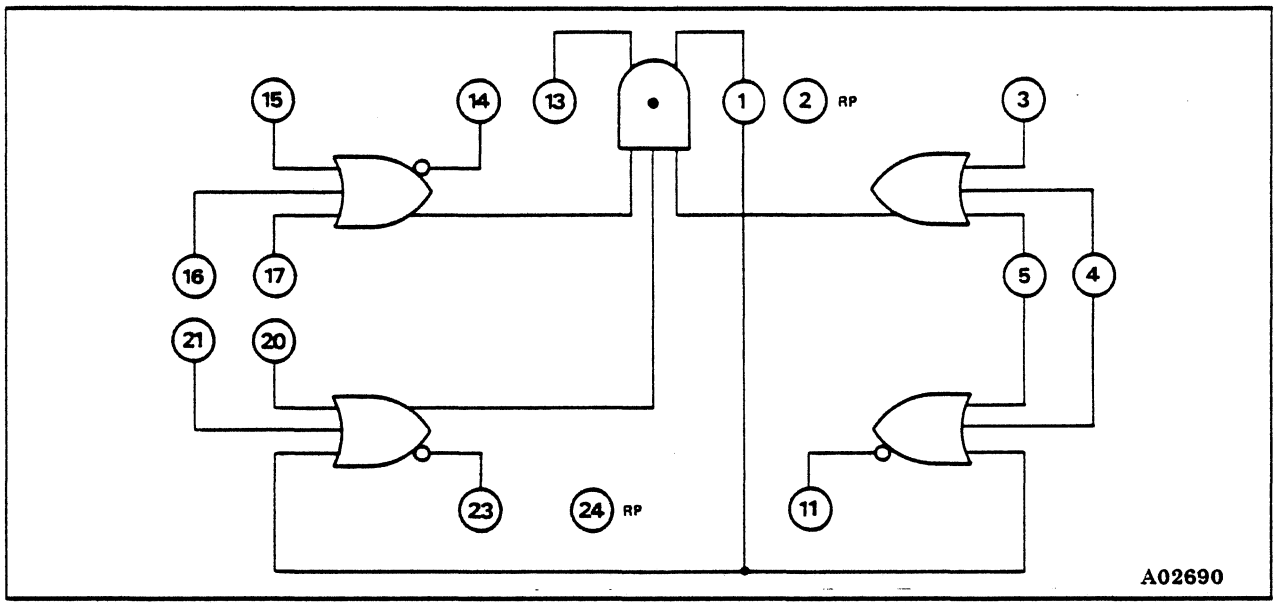

Figure 5-22. In-Phase Latch with Scan-In/Scan-Out Macro 3299

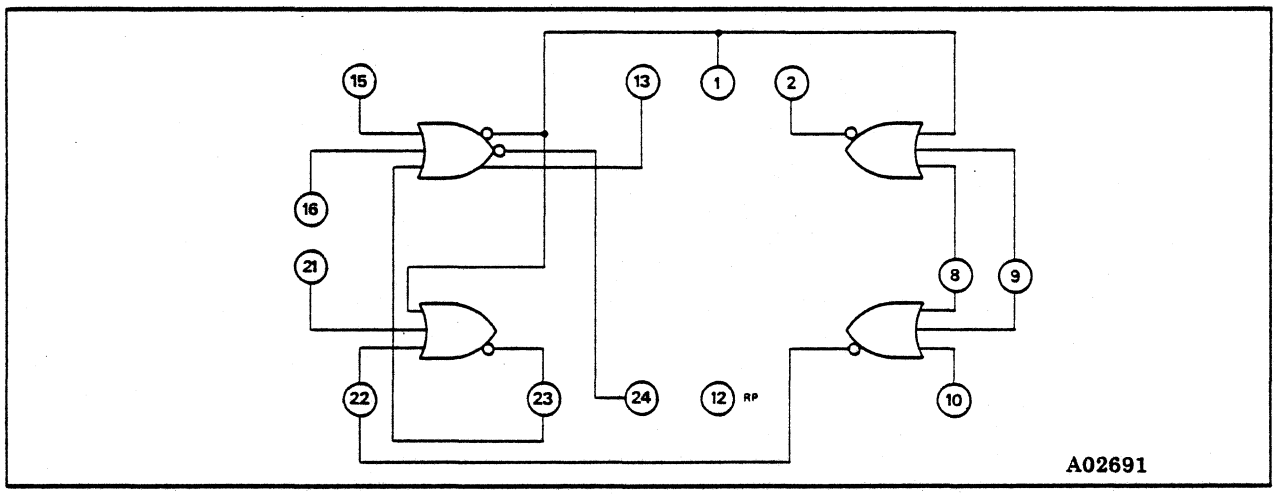

Figure 5-23. Out-of-Phase Latch with Scan-In/Scan-Out Macro 3399

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Table 5-24. Macro 3399 Characteristics

INPUT PIN	OUTPUT PIN	PHASE
15, 16, 23	13	øin
15, 16, 23	1, 24	øout

DRIVER CIRCUIT	Rp	SWITCHING TYPE	T_B	K6	K7
Low Power	4K	Tup øin	410		
		Tdn øin	324		
		Tup øout	265	65	
		Tdn øout	325	26	
	2K	Tup øin	450		
		Tdn øin	305		
		Tup øout	295	90	
		Tdn øout	305	22	
High Power Internal	4K	Tup øin	320		
		Tdn øin	260		
		Tup øout	220	26 210	40
		Tdn øout	260	13 68	35
	2K	Tup øin	350		
		Tdn øin	245		
		Tup øout	240	30 210	40
		Tdn øout	245	13 62	35
High Power External	90	Tup øin	679		55
		Tdn øin	558		38
		Tup øout	485	30	40
		Tdn øout	545	13	35

INPUT PIN	OUTPUT PIN	PHASE
1, 8, 9	2	øout
8, 9, 10	SI*	øout
1, 21, SI*	23	øout

$T_{up\ øout}$ and $T_{dn\ øout}$ are equal to that of the Macro 01.

*Here, SI is the output of the scan-in gate.

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5.3.5 T_{out} Definition

T_{out} contains the line loading factors. For this reason, it cannot be ignored. T_{out} is a function of the power of the driver circuit, the pull down resistor, and the output transition type. It is defined by the following parameters:

$$T_{out} = \sum_{1}^{MEF} [KFB \times ((K8 \times NONL) + (K9 \times NONH) + (K10 \times SNONL) + (K11 \times SNONH) + (K12 \times MNON)) + CFB]$$

If the driver circuit has a sub-output net (same phase other emitter follower output), the loading parameters of the sub-output net should be considered.

KFB is the feedback coefficient of the loading delay time (of the sub-output net) to the delay time of the main output net. KFB is equal to 1 when calculating the loading delay of the main output nets. CFB is 0 when KFB is used. CFB is considered only when the sub-output net is dotted. When this occurs, KFB is 0 and CFB is used. Refer to Table 5-25 for main coefficients and Table 5-26 for CFB and KFB.

Table 5-25. Main Coefficients

DRIVER CIRCUIT	RP	TRANSISTION	K8	K9	K10	K11	K12
Low Power	4K	UP	7.1	13.5	1.2	2.5	14.6
		DN	67.4	140.2	-36.0	-75.1	75.0
	2K	UP	7.5	14.0	1.4	3.0	15.0
		DN	29.0	60.0	-13.0	-28.0	30.0
High Power Internal	4K	UP	6.5	11.0	1.0	2.0	12.0
		DN	67.4	140.2	-36.0	-75.1	75.0
	2K	UP	6.5	11.0	1.0	2.0	12.0
		DN	29.0	60.0	-13.0	-28.0	30.0
High Pwr External	90	UP	2.0	3.8	0.4	0.7	2.7
		DN	3.0	5.5	-1.2	-2.5	4.2

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Table 5-26. Feedback Coefficient KFB (CFB)

DRIVER CIRCUIT	Rp	OUTPUT TRANSISTION	MAIN OUTPUT	SAME PHASE OTHER OUTPUTS		
				Rp 4K	Rp 2K	EXT.
Low Power	4K	UP	1	0.58(-40)	0.64(-60)	
		DN	1	0.01(0)	0.03(0)	
	2K	UP	1	0.58(-40)	0.64(-60)	
		DN	1	0.01(0)	0.03(0)	
High Power Internal	4K	UP	1	0.22(-15)	0.24(-20)	0.79(-135)
		DN	1	0.00(0)	0.01(0)	0.25(30)
	2K	UP	1	0.22(-15)	0.24(-20)	0.79(-135)
		DN	1	0.00(0)	0.01(0)	0.23(30)
High Pwr External	90	UP	1	0.22(-15)	0.24(-20)	
		DN	1	0.0(0)	0.01(0)	

5.3.6 T_{BD} Definition (Bias Driver Interference)

T_{BD} is defined by the following formula:

$$T_{BD} = K_{BD} \times (N_{SD} - N_{OD} - 1)$$

where:

K_{BD} is the coefficient of T_{BD}. It is defined for the gate power types of the driver circuit and each switching type (refer to table 5-27).

N_{SD} is the total number of switching bases having the same direction and same macro within ±200ps.

N_{OD} is the total number of switching bases going in opposite directions and using the same macro within ±200ps.

$(N_{SD} - N_{OD} - 1)$ is equal to 1 for minimum delay calculations. For maximum delay calculations assume all gates switch in the same direction (N_{SD} is maximum).

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Table 5-27. T_{BD} Coefficients

DRIVER CIRCUIT	SWITCHING TYPE	K_{BD}
Low Power	Tup ϕin	34
	Tdn ϕin	46
	Tup ϕout	16
	Tup ϕout	36
High Power Internal or High Pwr External	Tup ϕin	17
	Tdn ϕin	20
	Tup out	6
	Tdn ϕout	15

5.3.7 T_{EDOT} Definition

T_{EDOT} is defined for internal emitter follower dotting and external emitter follower dotting as shown in table 5-28.

Table 5-28. T_{EDOT} (ps)

DOT SIZE	INTERNAL DOT		EXTERNAL DOT	
	UP	DN	UP	DN
2	52	6	55	40
3	63	10	101	80
4	74	14	138	120
5	85	18	174	160
6	96	22	210	200
7	107	26	246	240
8	118	30	283	280

5.3.8 T_{add} Definition

T_{add} is defined as an additional delay to be added only to the Tup transition of an E-dot to compensate for the output switching skew (refer to figure 5-24). If used, Tadd=200 pSec.

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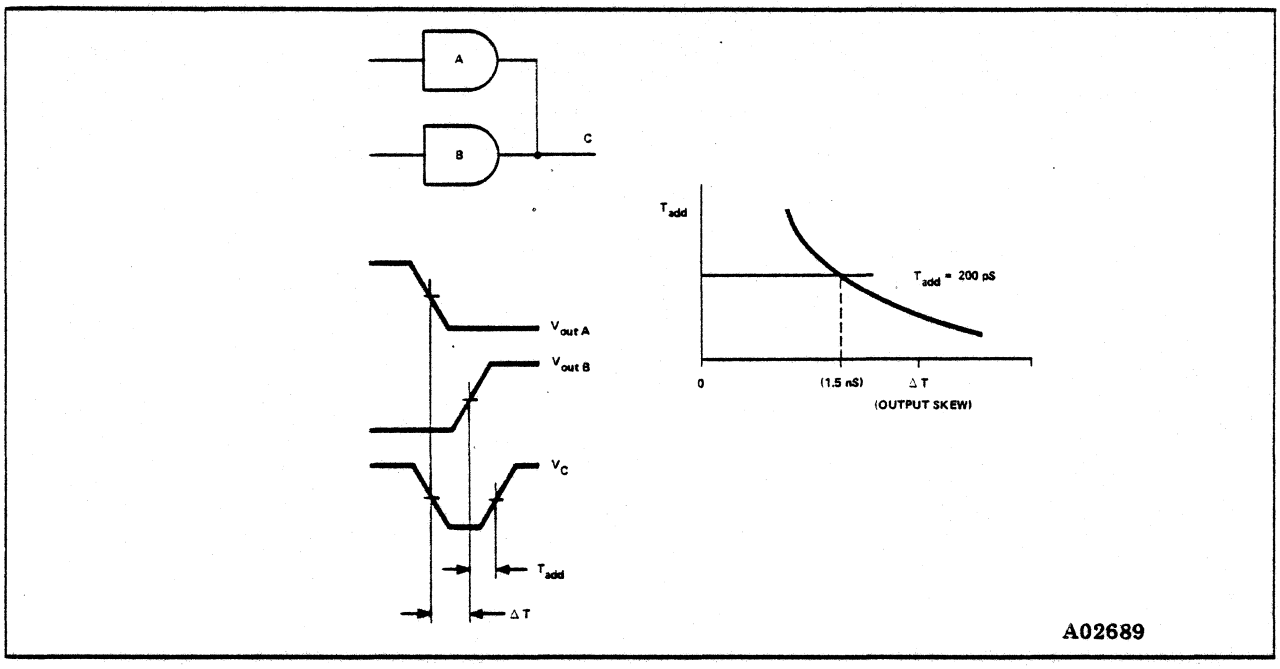

Figure 5-24. Definition of T_{add}

5.4 OFF-CHIP DELAY EQUATION

The basic section of the off-chip delay is defined (figure 5-25) from the macro input pin of the driver circuit to the macro input pin of the receiver circuit, similar to the on-chip delay.

The total delay time (T_{in}) of the basic section is defined by the following terms:

$$T_d = T_{in} + T_{fanin} + T_{circuit} + T_{out} + T_{BD} + T_{EDOT} + T_{add} + T_{line}$$

where:

T_{in}, T_{fanin}, $T_{circuit}$, T_{out}, T_{BD}, T_{EDOT}, and T_{add} have the same meanings as that of the on-chip delay equation.

T_{line} is the delay time of the printed wire, discrete wire, coaxial cable, and card connector crossing.

T_{in} and T_{out} are calculated by using the loading parameters from paragraph 5.5.

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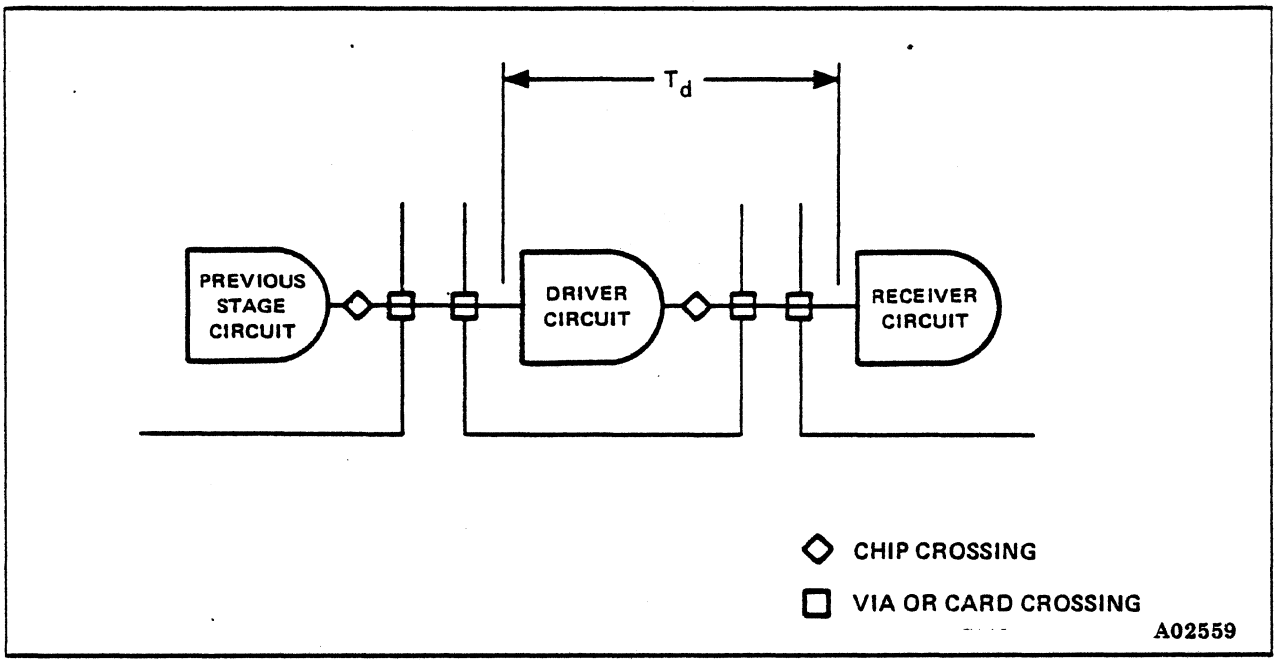

Figure 5-25. Off-Chip Delay

5.5 OFF-CHIP LOADING PARAMETERS

Figure 5-26 illustrates the off-chip loading parameters that are described below.

5.5.1 T_{in} Definitions

NINL-n Total number of low power bases including switching and non-switching in the L1 section of the input net of the circuit of interest.

NINH-n Total number of high power bases including switching and non-switching of the L1 section of the input net of the circuit of interest.

SNINL-n Total number of low power switching bases in the L1 section of the input net of the circuit of interest.

SNINH-n Total number of high power switching bases in the L1 section of the input net of the circuit of interest.

MNIN-n Total loading units, except for low power and high power bases, in the L1 section of the input net of the circuit of interest.

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NINL-f Total number of low power bases including switching and non-switching in the L2 section of the input net of the circuit of interest.

NINH-f Total number of high power bases including switching and non-switching in the L2 section of the input net of the circuit of interest.

SNINL-f Total number of low power switching bases in the L2 section of the input net of the circuit of interest.

SNINH-f Total number of high power switching bases in the L2 section of the input net of the circuit of interest.

MNIN-f Total loading units, except for low power and high power bases, in the L2 section of the input net of the circuit of interest.

5.5.2 T_{out} Definitions

NONL-n Total number of low power bases including switching and non-switching in the L3 section of the output net of the circuit of interest.

NONH-n Total number of high power bases including switching and non-switching in the L3 section of the output net of the circuit of interest.

SNONL-n Total number of low power switching bases in the L3 section of the output net of the circuit of interest.

SNONH-n Total number of high power switching bases in the L3 section of the output net of the circuit of interest.

MNON-n Total loading units, except for low power and high power bases, in the L3 section of the output net of the circuit of interest.

NONL-f Total number of low power bases including switching and non-switching in the L4 section of the output net of the circuit of interest.

NONH-f Total number of high power bases including switching and non-switching in the L4 section of the output net of the circuit of interest.

SNONL-f Total number of low power switching bases in the L4 section of the output net of the circuit of interest.

SNONH-f Total number of high power switching bases in the L4 section of the output net of the circuit of interest.

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MNON-f Total loading units, except for low power and high power bases, in the L4 section of the output net of the circuit of interest.

L1 and L3 are considered the "near" section of a net which starts with the output of the switching gate and extends 1.2" (printed wire) or 1.6" (discrete wire) towards the load of interest.

L2 and L4 are considered the "far" section of a net which begins where "near" ends and extends 1.2" (printed wire) or 1.6" (discrete wire) beyond the load of interest.

Loading outside L1, L2 or L3, L4 sections of the net do not affect the delay of the circuit of interest.

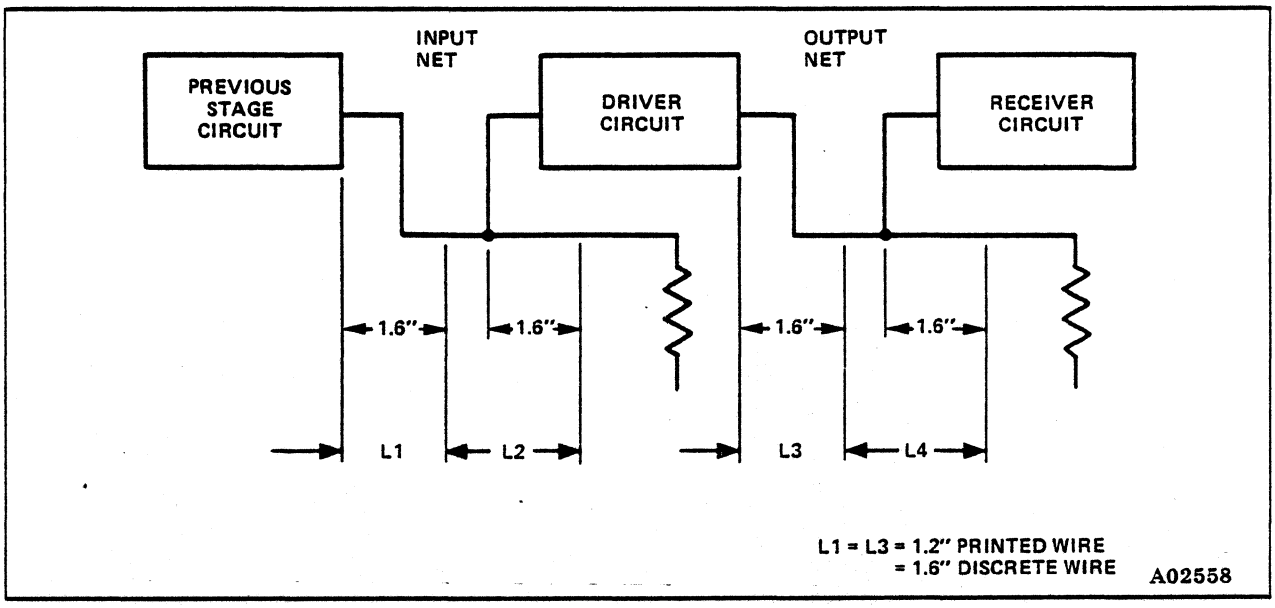

Figure 5-26. Off-Chip Loading Parameters

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5.6 OFF-CHIP DELAY TERMS

5.6.1 T_{in} Definition

Table 5-29 lists the T_{in} coefficients which are defined as follows:

$$T_{in} = (K13 \times NINL\text{-}n) + (K14 \times NINH\text{-}n) + (K15 \times SNINL\text{-}n) + (K16 \times SNINH\text{-}n) + (K17 \times MNIN\text{-}n) + (K18 \times NINL\text{-}f) + (K19 \times NINH\text{-}f) + (K20 \times SNINL\text{-}f) + (K21 \times SNINH\text{-}f) + (K22 \times MNIN\text{-}f)$$

Table 5-29. T_{in} Coefficients

DRIVER CIRCUIT	INPUT WAVEFORM	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22
Low Power	UP	6.2	8.4	3.4	4.8	1.2	6.3	8.6	3.6	5.2	1.3
	DN	7.3	9.6	0.5	0.9	1.3	7.3	9.6	0.5	0.9	1.3
High Pwr Int/Ext	UP	6.2	8.4	3.4	4.8	1.2	6.3	8.6	3.6	5.2	1.3
	DN	7.3	9.6	0.5	0.9	1.3	7.3	9.6	0.5	0.9	1.3

5.6.2 T_{out} Definition

Table 5-30 lists the T_{out} coefficients which are defined as follows:

$$T_{out} = (K23 \times NONL\text{-}n) + (K24 \times NONH\text{-}n) + (K25 \times SNONL\text{-}n) + (K26 \times SNONH\text{-}n) + (K27 \times MNON\text{-}n) + (K28 \times NONL\text{-}f) + (K29 \times NONH\text{-}f) + (K30 \times SNONL\text{-}f) + (K31 \times SNONH\text{-}f) + (K32 \times MNON\text{-}f) + KFB \times [(K8 \times NONL) + (K9 \times NONH) + (K10 \times SNONL) + (K11 \times SNONH) + (K12 \times MNON)]$$

Table 5-30. T_{out} Coefficients

DRIVER CIRCUIT	OUTPUT TRANSITION	K23	K24	K25	K26	K27	K28	K29	K30	K31	K32
High External	UP	2.0	3.8	0.4	0.7	2.7	3.0	5.8	0.6	1.0	4.5
	DN	3.0	5.5	-1.2	-2.5	4.2	3.3	6.1	-1.4	-2.7	4.8

5.6.3 T_{line} Definition

MCC Printed Wire: (X and Y layers) 191 ps/in

MCC Printed Wire: (Slant layers) 203 psec/in

SP Printed Wire: 191 psec/in

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MCC to SP Connector:	320 psec
SP to Cable Connector:	350 psec
Coaxial Cable:	102 psec/in
Discrete Wire:	114 psec/in

5.7 RAM MODULE DELAY EQUATIONS

5.7.1 Definitions of Delay Equation

Figure 5-27 illustrates the basic RAM Module delay definitions. Basic delays consist of three parts. The first part is the entry net delay, the second part is the intra-module delay, and the rest is the output net delay. Delay time of the driving logic gate is calculated on the assumption that the output loading is zero.

Delay time is defined by the following terms:

$$T_D = T_{RAM\ IN} = T_{MODULE} + T_{RAM\ OUT}$$

where:

$T_{RAM\ IN}$ = the entry net delay time.

T_{MODULE} = the intra-module delay time. (Pin to pin delay time.)

$T_{RAM\ OUT}$ = the output net delay time. (Delay equation treatment of T_{RAMOUT} is similar to the logic to logic delay equation.)

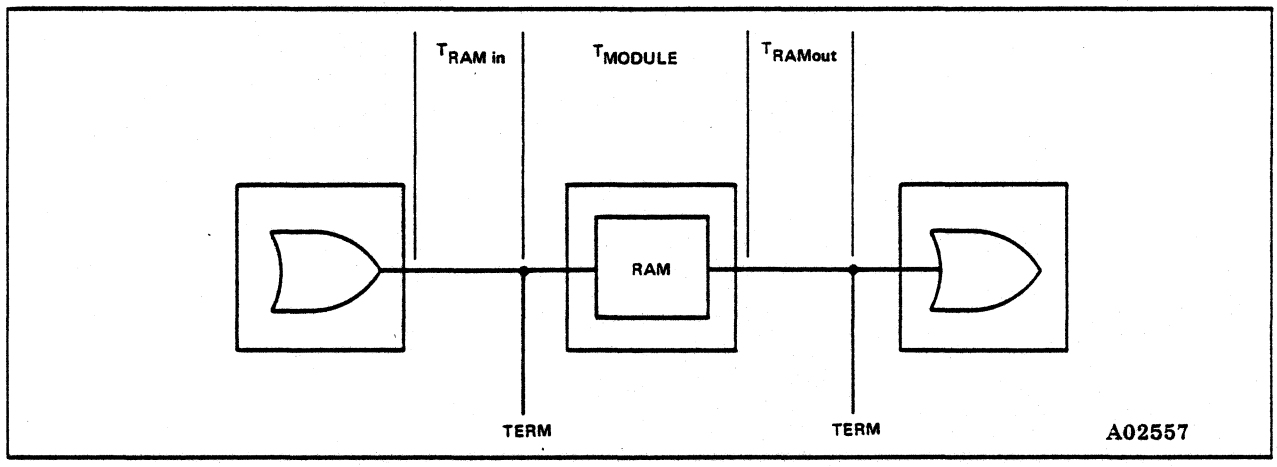

Figure 5-27. Basic RAM Module Delay Definitions

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5.7.2 Input Net Delay ($T_{RAM\ IN}$)

The RAM input net delay begins at the output pin of the driver and ends at the RAM Module input pin. The T_{RAMIN} equations are shown in table 31. The equation used is determined by the number of RAM Modules in the net and the distance between the input pins (ℓ_M). coefficients are shown in table 5-32.

Table 5-31. $T_{RAM\ IN}$ Equation Formats

Case	Number of Ram Module Input Pins	Distance Between Input Pins (ℓ_M)	Equation
A	1		$T_{RAMIN}=K_N \times C_N + K_F \times C_F + \ell t$
B1	2	$\ell_M < L_M$	$*T_{RAMIN\ 1}= K_N \times C_N + K_F \times C_F + \ell t_1$ $**T_{RAMIN\ 2}=K_N \times C_N + K_F \times C_F + \ell t_1 + K_1 \times \ell t_2$
B2	2	$\ell_M > L_M$	$*T_{RAMIN\ 1\ (max)}=K_N \times C_N + K_F \times C_F + K_R \times C_A + 2\ell t_2 + \ell t_1$ $*T_{RAMIN\ 1\ (min)}=K_N \times C_N + K_F \times C_F + \ell t_1$ $**T_{RAMIN\ 2}=K_N \times C_N + K_F \times C_F + \ell t_1 + K_1 \times \ell t_2$
C	N (N $\geq$ 3)		$T_{RAMIN}=K_N \times C_N + K_F \times C_F + \ell t_1 + \sum_{i=2}^{N} K_1 \times \ell t_i$

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*Use for first RAM
**Use for second RAM

Where:

L_M = 1.2 inches of stripline or 1.65 inches of discrete wire.
K_N (K_F) = Degradation Coefficient in the near (far) region.
K_R = Reflection Degradation Coefficient
K_L = Line Delay Coefficient
C_N (C_F) = Loading in near (far) region
C_A = Loading after first RAM
lt_N = intrinsic line delay of segment n

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Table 5-32. $T_{RAM\ IN}$ Equation Coefficients

Case	Loading of first RAM Module	Transition	K_n min	K_n max	K_f min	K_f max	K_r max	K_1 min	K_1 max
A		Tup	0.5	4.0	0.5	6.2	---	---	---
		Tdn	0.5	6.0	0.5	6.5	---	---	---
B1	$\leq$ 250LU	Tup	0.5	4.0	1.2	10.0	---	1.0	2.5
		Tdn	0.5	10.0	1.2	10.0	---	1.0	1.0
B1	>250LU	Tup	0.5	4.0	1.2	7.0	---	1.0	2.5
		Tdn	0.5	9.0	1.2	9.0	---	1.0	1.0
B2		Tup	0.5	4.0	0.5	6.2	8.0	1.0	1.0
		Tdn	0.5	6.0	0.5	6.5	8.0	1.0	1.0
C		Tup	0.3	3.0	0.3	6.2	---	1.0	2.0
		Tdn	0.3	10.0	0.3	11.5	---	1.0	1.0

5.7.3 Intra-Module Delay (T_{MODULE})

T_{MODULE} includes intra-chip delay and the delay time of mother board pattern in the module. The delay time in relation to the output emitter follower dotting is not included in T_{MODULE}. Refer to figure 5-28 and table 5-33.

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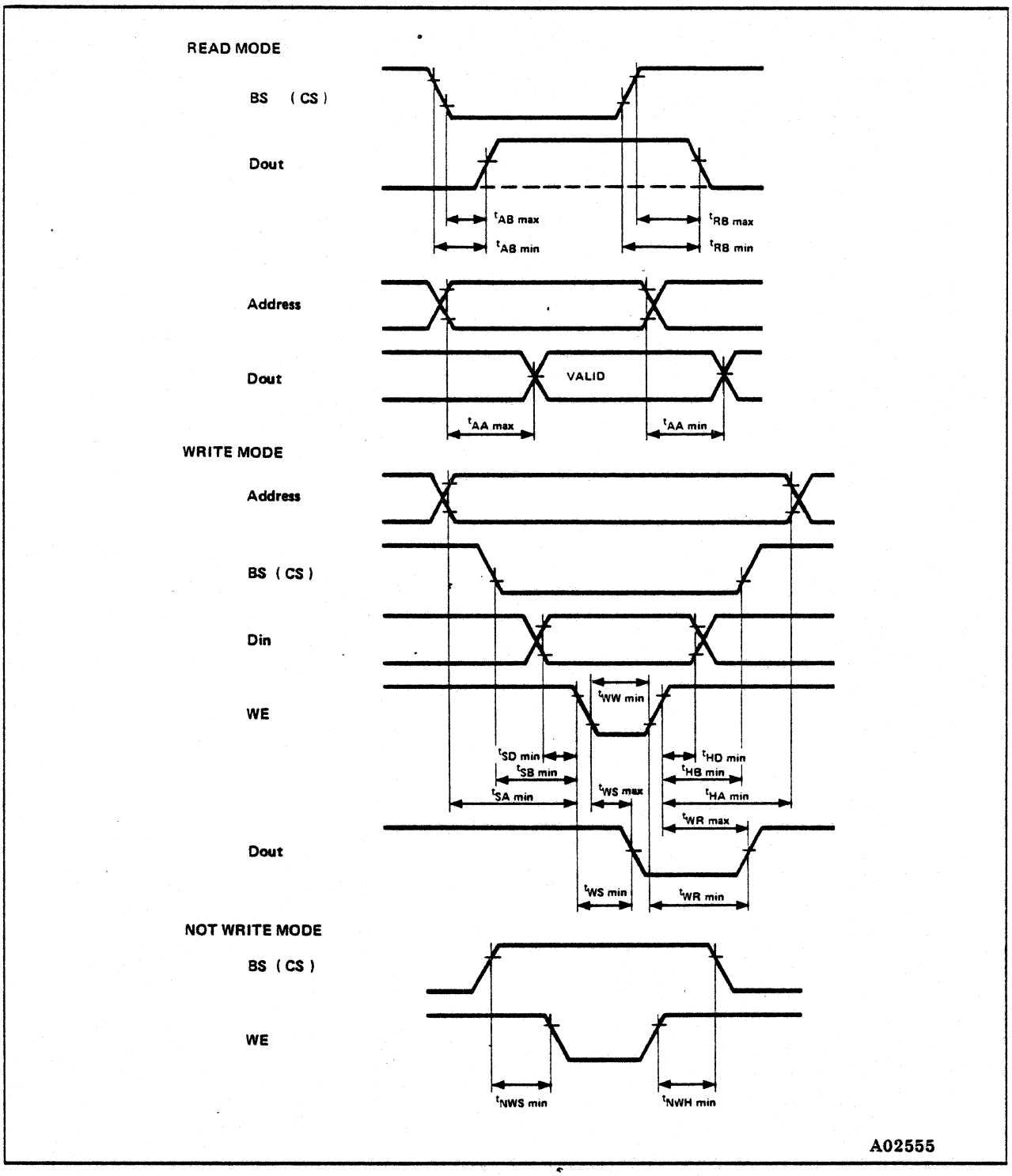

Figure 5-28. Read and Write Timing Chart

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Table 5-33. Intra-Module Delay and RAM Timing Requirements (ps)

TYPE			I	II	III	IV	V	VI	VII	VIII
	READ									
t_{AB}	Block Select Address Time	MIN	1500	1700	1400	1400	1500	1300	1200	1300
		MAX	4500	4300	4600	4600	4500	4700	10300	4700
t_{RB}	Block Select Recov. Time	MIN	1300	1500	1300	1300	1300	1200	1200	1200
		MAX	4700	4500	4700	4700	4700	4800	10300	4800
t_{AA}	Address Access time	MIN	2300	2300	2300	2200	2300	2200	2300	2300
		MAX	7200	7200	7200	7300	7200	7300	26700	7200
	WRITE									
t_{WW}	Write Pulse Width	MIN	3200	3000	2900	2900	3200	3000	12600	3000
		MAX	----	----	----	----	----	----	----	----
t_{SA}	Address Set Up Time	MIN	1500	1400	1400	1500	1500	1500	8500	1500
		MAX	----	----	----	----	----	----	----	----
t_{SB}	Block Select Set Up Time	MIN	1300	1000	1300	1300	1300	1400	5600	1400
		MAX	----	----	----	----	----	----	----	----
t_{SD}	Data Set Up Time	MIN	700	500	500	500	600	500	4600	500
		MAX	----	----	----	----	----	----	----	----
t_{HA}	Address Hold Time	MIN	1600	1500	1500	1600	1600	1600	5500	1500
		MAX	----	----	----	----	----	----	----	----
t_{HB}	Block Select Hold Time	MIN	1600	1300	1500	1500	1600	1600	5700	1600
		MAX	----	----	----	----	----	----	----	----
t_{HD}	Data Hold Time	MIN	2800	2600	2700	2600	2600	2600	5700	2500
		MAX	----	----	----	----	----	----	----	----
t_{WS}	Write Disable Time	MIN	0	0	0	0	0	0	0	0
		MAX	5800	5700	5600	5600	5800	5700	8800	5700
t_{WR}	Write Recov. Time	MIN	0	0	0	0	0	0	0	0
		MAX	5800	5800	5800	5800	5800	5800	15800	5800
t_{NWS}	Block Select Release Time	MIN	1300	1000	1300	1300	1300	1400	5600	1400
		MAX	----	----	----	----	----	----	----	----
t_{NWH}	Write Release Time	MIN	1600	1300	1500	1500	1600	1600	5700	1600
		MAX	----	----	----	----	----	----	----	----

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5.7.4 Output Net Delay ($T_{RAM\ OUT}$)

Output net delay is defined from the output pin of the RAM module to the macro input pin of the receiving circuit. The delay time is defined by the following terms and listed in table 5-34.

$$T_{RAM\ OUT} = T_{OUT} + T_{LINE} + T_{OUTDOT}$$

where:

$$T_{OUT} = (K23 \times NONL\text{-}n) + (K24 \times NONH\text{-}n) + (K25 \times SNONL\text{-}n) + (K26 \times SNONH\text{-}n) + (K27 \times MNON\text{-}n) + (K28 \times NONL\text{-}f) + (K29 \times NONH\text{-}f) + (K30 \times SNONL\text{-}f) + (K31 \times SNONH\text{-}f) + (K32 \times MNON\text{-}f)\ (ps)$$

$$T_{OUTDOT} = F01 \times (T_{EDOT} + F02 \times 2 \times (lt_{DOT} + T_{add}))$$

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NONLn = total number of low power bases including switching and non-switching in LN section.

NONHn = total number of high power bases including switching and non-switching in LN section.

SNONLn = total number of low power switching bases in LN section.

SNONHn = total number of high power switching bases in LN section.

MNONn = total loading units except for low power, high power bases and the switching output of the memory module in LN section.

NONLf, NONHf...MNONf = total loading units except for low power, high power bases and the switching output of the memory module in Lf section.

F01,F02 = Dot-OR Flag.

T_{EDOT} = delay with the output emitter follower dotting.

lt_{DOT} = wire delay with distance between dots.

T_{add} = additional delay of dotting specified at the UP switching transition only.

T_{line} = wire delay in main output net.

Table 5-34. Output Net Delay Times

OUTPUT TRANSISTION	K23	K24	K25	K26	K27	K28	K29	K30	K31	K32
UP	3.0	4.8	0.8	2.5	6.7	2.3	3.6	0.6	1.9	4.9
DN	2.9	5.4	-0.7	-1.5	7.0	1.8	3.5	-0.4	-0.9	5.3

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Output Dotting:

Flag F01: If output dotting exists, regardless of whether it is inside or outside of the RAM module, the flag is a 1. When using Type I, Type VI, or Type VII module, F01 is always a 1. In all other conditions, the flag becomes a 0.

Flag F02: Flag F02 is used only with the block-select path delay. When all four conditions listed below are satisfied simultaneously, the flag becomes a 1. In all other conditions, the flag becomes a 0.

1. Dotting is outside of the RAM module.
2. Dotting is between the outputs of different chips.
3. Distance between the dots ℓ_{DOT} is > L_{DOT} (1.2 inches of strip line or 1.65 inches of discrete wire).
4. RAM module of interest is not placed at the position farthest from the terminator.

RAM MODULE OUTPUT LOADING is given in paragraph 5.8.2. All Loading parameters are as defined in paragraph 5.5.

T_{EDOT} is defined by the following:

T_{EDOT} (Up) = (N_{DOT} - 1) x 100 in pSec.

T_{EDOT} (Down) = (N_{DOT} - 1) x 200 in pSec.

where:

N_{DOT} is the total number of emitters dotted. This includes dots both inside and outside the module.

T_{add} is used for the up transition only.

T_{add} = 200 pSec.

Refer to figure 5-25.

5.7.5 Examples of Entry Net Calculations

Refer to the example given in figure 5-29 for the calculation when a driver's fan-out is 1 input pin.

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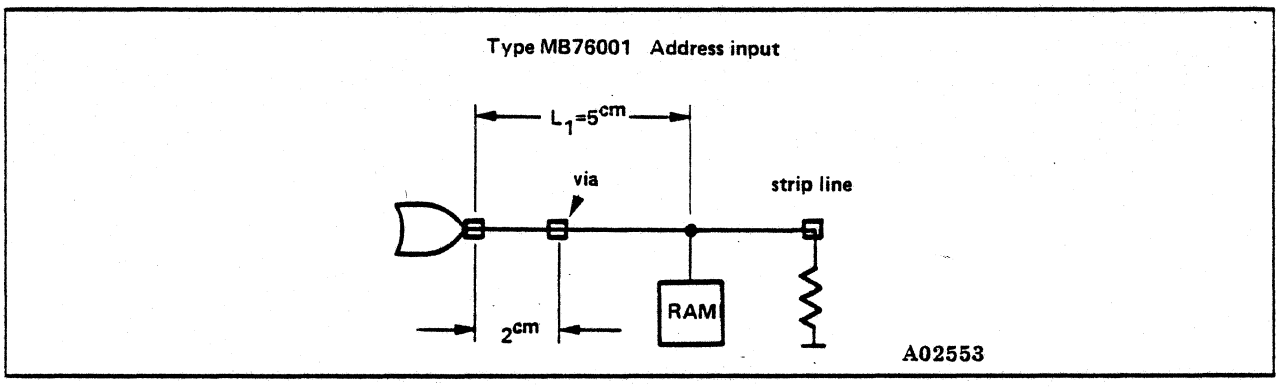

Figure 5-29. Driver Fan-out is One Input Pin

$T_{RAM.\,IN}(max) = K_N \times C_N + K_F \times C_F + Lt_1$

where:

K_N, K_F = maximum value in Down

C_N = loads at output of LSI + Via

D_F = maximum value of L_{MODULE} + lead extension of R-pack.

"Loads at output of LSI" include the lead extension, via and other output loading units (αL). "L_{MODULE}" includes the RAM input loading units, lead extension and via.

In actual value:

$$T_{RAM.\,IN}(max) = 6.0 \times (\alpha L + 6) + 6.5 \times (215 + 2.8 + 6 + 18) + 5 \times 70 = 1957.7 + 6 \times \alpha L \text{ (ps)}$$

Up-min

$T_{RAM.\,IN}(min) = K_N \times C_N + K_F \times C_F + Lt_1$

where:

K_N, K_F = minimum value in Up

C_N = loads at output of LSI + via

C_F = minimum value of L_{MODULE} + lead extension of R-pack

In actual value:

$$T_{RAM.\,IN}(min) = 0.5 \times (\alpha L + 6) + 0.5 \times (131 + 2.8 + 6 + 18) + 5 \times 70 = 431.9 + 0.5 \times \alpha L \text{ (ps)}$$

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Refer to the example given in figure 5-30 for entry net calculation when a driver's fan-out is 2 input pins.

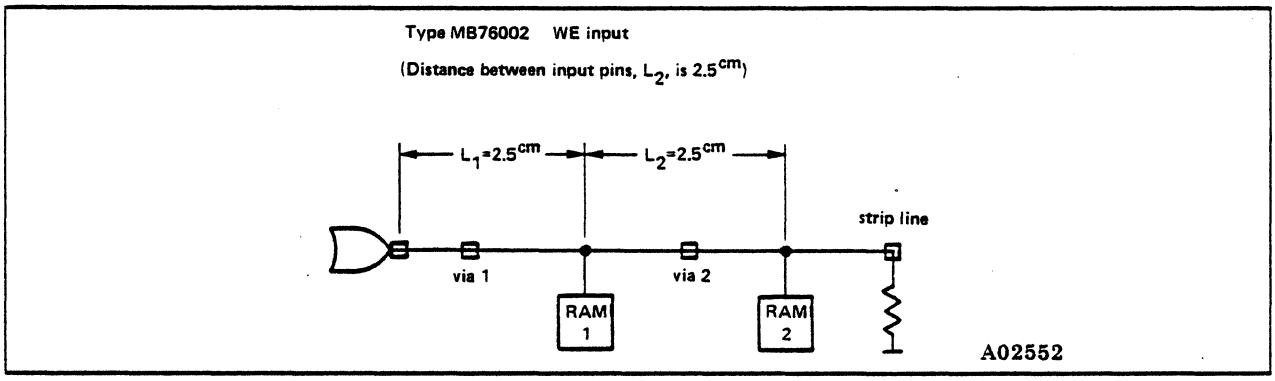

Figure 5-30. Driver Fan-out with Two Input Pins (Up-Min)

Up-max

RAM 1

$$T_{RAM.\,IN}(max) = K_N \times C_N + K_F \times C_F + Lt_1$$

where:

K_N, K_F = maximum value in Up

C_N = Loads at output of LSI + via 1 + via 2 + maximum value of L_{MODULE} x 2 + lead extension of R-pack.

C_F = 0

In actual value:

$$T_{RAM.\,IN}\ (max) = 4.0 \times (\alpha L + 6 + 6 + (113 + 2.8 + 6) \times 2 + 18) + 2.5 \times 70 = 1269.4 + 4.0 \times \alpha L\ (ps)$$

RAM 2

$$T_{RAM.\,IN}(max) = K_N \times C_N + K_F \times C_F + Lt_1 + K_L \times Lt_2$$

where:

K_N, K_F, C_N, C_F = same as RAM 1 case.

K_L = maximum value in Up

In actual value:

$$T_{RAM.\,IN}\ (max) = 4.0 \times (\alpha l + 6 + 6 + (113 + 2.8 + 6) \times 2 + 18) + 2.5 \times 70 + 2.5 \times 2.5 \times 70 = 1706.9 + 4.0 \times \alpha L\ (ps)$$

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In these cases the concept of load is "Totalized". Therefore, the same value in C_N is used in both calculations. "Near" and "far" are determined by the position of RAM 1.

Refer to the example given in figure 5-31 for the calculation when a driver's fan-out is 2 input pins.

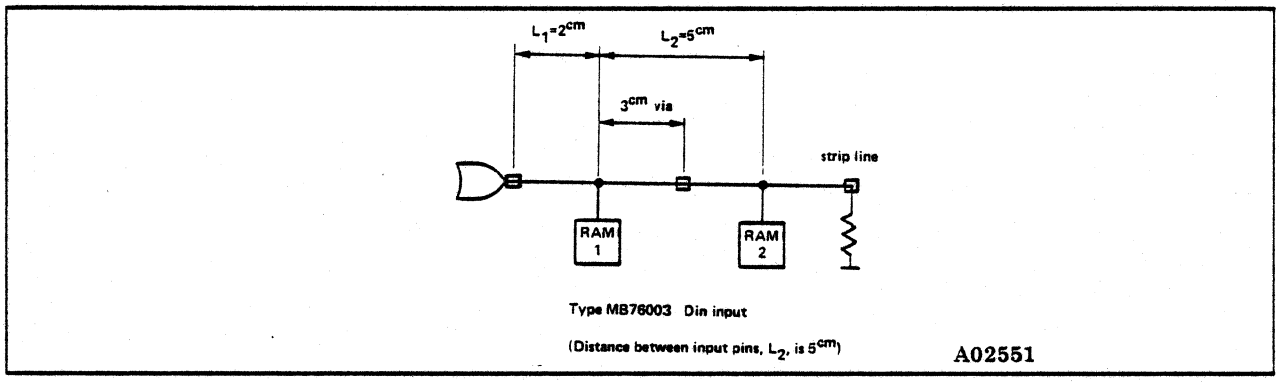

Figure 5-31. Driver Fan-out with Two Input Pins (Up-Max)

Down-Max

RAM 1

$$T_{RAM.\,IN}\,(max) = K_N \times C_N + KF \times C_F + (K_R \times C_A + 2 \times Lt_2) + Lt_1$$

where:

K_N, K_F, K_R = maximum value in Down

C_N = loads at output of LSI + maximum value of L_{MODULE} via

C_F = 0

C_A = maximum value of L_{MODULE} + lead extension of R-pack.

In actual value:

$$T_{RAM.\,IN}\,(max) = 6.0 \times (\alpha L + 70 + 2.8 + 6 + 6) + 8.0 \times (70 + 2.8 + 6 + 18) + 2 \times 5 \times 70 + 2 \times 70 = 2123.2 + 6 \times \alpha L\ (ps)$$

RAM 2

$T_{RAM.\,IN}$ $T_{RAM.\,IN}\,(max) = K_N \times C_N + K_F \times C_F + Lt_1 + K_L \times Lt_2$

where:

K_N, K_F = same as for RAM 1 case

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C_N = loads at output of LSI + maximum value of L_{MODULE}

C_F = via + maximum value of L_{MODULE} + lead extension of R-pack

K_L = maximum value in Down

In actual value:

$$T_{RAM.\,IN}\ (max) = 6.0 \times (\alpha L + 70 + 2.8 + 6) + 6.5 \times (6 + 70 + 2.8 + 6 + 18) + 2 \times 70 + 1.0 \times 5 \times 70 = 1631 + 6 \times \alpha L\ (ps)$$

Down-Mim

RAM 1

$$T_{RAM.\,IN}\,(min) - K_N \times C_N + K_F \times C_F + Lt_1$$

where:

K_N, K_F = minimum value in Down

C_N = loads at output of LSI + minimum value of L_{MODULE} + via

C_F = 0

In actual value:

$$T_{RAM.\,IN}\ (min) = 0.5 \times (\alpha L + 31 + 2.8 + 6) + 2 \times 70 = 159.9 + 0.5 \times \alpha L\ (ps)$$

RAM 2

$$T_{RAM.\,IN}\,(min) = K_N \times C_N + K_F \times C_F + Lt_1 + K_L \times Lt_2$$

where:

K_N, K_F = same as RAM 1 case

C_N = loads at output of LSI + minimum value of L_{MODULE}

C_F = via + minimum value of L_{MODULE} + lead extension of R-pack

K_L = minimum value in Down

In actual value:

$$T_{RAM.\,IN} = 0.5 \times (\alpha L + 31 + 2.8 + 6) + 0.5 \times (6 + 31 + 2.8 + 6 + 18) + 2 \times 70 + 1.0 \times 5 \times 70 = 541.8 + 0.5 \times \alpha L\ (ps)$$

The load is calculated to each RAM independently. The criteria of region ("near" or "far") is defined by the position of RAM module of interest. When the RAM 1 is of interest, the via is included in the

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load of RAM 1. However, in the case of RAM 2, it is considered to be in a "far" region.

Refer to the example given in figure 5-32 for the calculation when a driver's fan-out is 4 input pins.

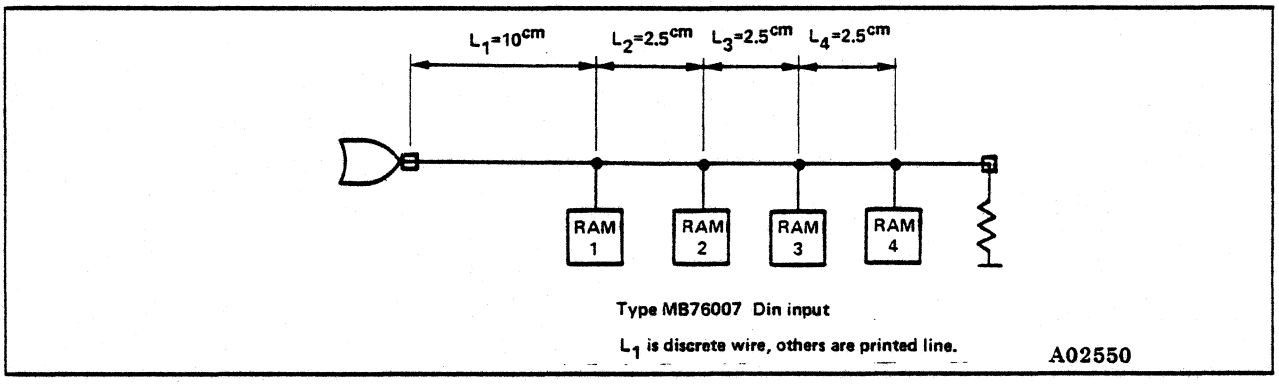

Figure 5-32. Driver Fan-out with Four Input Pins

RAM 1

$$T_{RAM.\,IN}(max) = K_N \times C_N + K_F \times C_F + Lt_1$$

where:

K_N, K_F = maximum value in Up

C_N = loads at output of LSI

C_F = maximum value of L_{MODULE} x 4 + lead extension of R-pack

In actual value:

$$T_{RAM.\,IN}\ (max) = 3.0 \times \alpha L + 6.2 \times ((137 + 2.8 + 6) \times 4 + 18) + 10 \times 50 = 4227.4 + 3.0 \times \alpha L\ (ps)$$

RAM 2

$$T_{RAM.\,IN}(max) = K_N \times C_N + K_F \times C_F + Lt_1 + K_L \times Lt_2$$

where:

K_N, K_F, C_N, C_F = same as for RAM 1 case

K_L = maximum value in Up

In actual value:

$$T_{RAM.\,IN}\ (max) = 3.0 \times \alpha L + 6.2 \times ((137 + 2.8 + 6) \times 4 + 18) + 10 \times 50 + 2.0 \times 2.5 \times 70 = 4577.4 + 3.0 \times \alpha L\ (ps)$$

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RAM 3

$$T_{RAM.\,IN}\,(max) = K_N \times C_N + K_F \times C_F + Lt_1 + K_L \times Lt_2 + K_L \times Lt_3$$

In actual value:

$$T_{RAM.\,IN}\ (max) = 4927.4 + 3.0 \times \alpha L\ (ps)$$

RAM 4

$$T_{RAM.IN}\,(max) = K_N \times C_N + K_F \times C_F + Lt_1 + K_L \times (Lt_1 + Lt_2 + Lt_3 + Lt_4)$$

In actual value:

$$T_{RAM.\,IN}\ (max) = 5277.4 + 3.0 \times \alpha L\ (ps)$$

5.8 CAPACITIVE LOADING

To normalize the loading capacitance, the loading unit (LU) is used. A loading unit is defined as the capacitance of a low power switching base which is approximately 0.1 pF.

5.8.1 On-Chip Metalization Capacitance

Tables 5-35 through 5-39 list the load units for specific calculations.

Table 5-35. Macro Multiple Base Input (Excluding Bases)

MACRO NUMBER	INPUT PIN	LU	
		LOW POWER	HIGH POWER
2399	15	0.94	
3199	8	0.20	0.16
3399	9	0.20	0.16
3299	4	0.20	0.16
	5	0.20	0.16

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Table 5-36. Macro Re-entry Pin (Excluding Bases)

MACRO NUMBER	INPUT PIN	LU	
		LOW POWER	HIGH POWER
31	1 11	0.24 0.37	0.21 0.35
32	12	0.34	0.26
3199	1 23	0.94 0.93	0.99 0.88
3299	1	0.71	0.66
3399	1 23	0.76 0.27	0.75 0.25

Table 5-37. Intra Macro Net without Pin (Excluding Bases)

MACRO NUMBER	INPUT PIN	LU	
		LOW POWER	HIGH POWER
3399	SI*	0.42	0.40
*SI = output of a scan-in gate.			

Table 5-38. Wiring Segments (MNIN, MNON)

SEGMENT	LU/GRID
First layer for the connection of Ext. EF and chip I/O pad	0.12
First layer for Ext. EF dotting	0.0594
First layer for the connection of macro I/O pins	0.0324
Second layer for the connection of Ext. EF and chip I/O pad	0.083
Second layer for Ext. EF dotting	0.034
Second layer for the connection of macro I/O pins	0.0156

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Table 5-39. Wire Loading Units

WIRE SEQ. NO. FOR CHIP I/O PIN	LU	WIRE SEQ. NO. FOR CHIP I/O PIN	LU	WIRE SEQ. NO. FOR EXT EF BASE	LU
1	1.05	41	1.05	1	0.95
2	1.28	42	1.28	2	0.90
3	1.14	43	1.14	3	1.25
4	1.40	44	1.40	4	1.08
5	1.32	45	1.32	5	1.08
6	1.50	46	1.50	6	0.99
7	1.33	47	1.33	7	1.34
8	1.60	48	1.60	8	1.22
9	1.49	49	1.49	9	1.24
10	1.77	50	1.77	10	1.11
11	1.77	51	1.77	11	1.49
12	1.49	52	1.49	12	1.32
13	1.60	53	1.60	13	1.32
14	1.33	54	1.33	14	1.22
15	1.50	55	1.50	15	1.60
16	1.32	56	1.32	16	1.44
17	1.40	57	1.40	17	1.45
18	1.14	58	1.14	18	1.32
19	1.28	59	1.28	19	1.78
20	1.05	60	1.05	20	1.78
21	1.43	61	1.43	21	1.32
22	1.25	62	1.25	22	1.45
23	--	63	--	23	1.44
24	1.14	64	1.14	24	1.60
25	1.20	65	1.20	25	1.22
26	1.05	66	1.05	26	1.32
27	1.12	67	1.12	27	1.32
28	0.99	68	0.99	28	1.49
29	1.05	69	1.05	29	1.11
30	1.06	70	1.06	30	1.24
31	1.06	71	1.06	31	1.22
32	1.05	72	1.05	32	1.34
33	0.99	73	0.99	33	0.99
34	1.12	74	1.12	34	1.08
35	1.05	75	1.05	35	1.08
36	1.20	76	1.20	36	1.25
37	1.14	77	1.14	37	0.90
38	--	78	--	38	0.95
39	1.25	79	1.25	39	1.49
40	1.43	80	1.43	40	1.27

(continued)

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Table 5-39. Wire Loading Units (continued)

WIRE SEQ. NO. FOR EXT EF BASE	LU	WIRE SEQ. NO. FOR EXT EF BASE	LU	WIRE SEQ. NO. FOR EXT EF BASE	LU
41	1.63	81	1.08	121	0.99
42	1.40	82	0.99	122	0.77
43	--	83	1.34	123	1.06
44	0.79	84	1.22	124	0.83
45	0.99	85	1.24	125	0.93
46	0.77	86	1.11	126	0.81
47	1.06	87	1.49	127	1.01
48	0.83	88	1.32	128	0.77
49	0.93	89	1.32	129	0.86
50	0.81	90	1.22	130	0.82
51	1.01	91	1.60	131	0.94
52	0.77	92	1.44	132	0.81
53	0.86	93	1.45	133	0.93
54	0.82	94	1.32	134	0.93
55	0.94	95	1.78	135	0.81
56	0.81	96	1.78	136	0.94
57	0.93	97	1.32	137	0.82
58	0.93	98	1.45	138	0.86
59	0.81	99	1.44	139	0.77
60	0.94	100	1.60	140	1.01
61	0.82	101	1.22	141	0.81
62	0.86	102	1.32	142	0.93
63	0.77	103	1.32	143	0.83
64	1.01	104	1.49	144	1.06
65	0.81	105	1.11	145	0.77
66	0.93	106	1.24	146	0.99
67	0.83	107	1.22	147	0.79
68	1.06	108	1.34	148	--
69	0.77	109	0.99	149	1.40
70	0.99	110	1.08	150	1.63
71	0.79	111	1.08	151	1.27
72	--	112	1.25	152	1.49
73	1.40	113	0.90	153	--
74	1.63	114	0.95	154	--
75	1.27	115	1.49	155	--
76	1.49	116	1.27	156	--
77	0.95	117	1.63	157	--
78	0.90	118	1.40	158	--
79	1.25	119	--	159	--
80	1.08	120	0.79	160	--

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5.8.2 Off-Chip Metalization Capacitance

Table 5-40 lists the RAM input/output loading units.

Table 5-40. RAM Input/Output Loading

LOADING IN LU MODULE	Address MIN	Address MAX	Din MIN	Din MAX	BS* MIN	BS* MAX	WE MIN	WE MAX	DOUT MIN	DOUT MAX
1	131	215	29	77	151	228	41	57	28	38
2	138	214	71	107	261	346	90	113	13	35
3	131	215	31	70	123	167	97	122	13	35
4	67	91	72	117	123	167	95	119	13	35
5	137	205	113	147	151	209	41	56	13	35
6	68**	92	70	92	76	104	90	114	64	92
6	149***	234								
7	171	343	90	137	43	78	40	66	46	60
8	136	230	152	206	76	107	90	114	139	172

*BS in Modules 1 thru 6 and 8 are the same as CS in Module 7.
**A0, A1
***A2-A7

LSI Chip Carrier Crossing: 24 LU
(Does not include chip metalization or Base/Emitter capacitance. A typical value for a two-base chip crossing is 30 LU)

Lead Extension for R-pack on MCC: 6 LU
(Includes vias connected to Lead Extensions)

Lead Extension for RAM Module inputs and outputs: 8.8 LU
(Includes vias and bonding pads connected to the Lead Extension)

Via on MC: 6 LU

Via on SP: 6 LU

MCC to SP Connector: 10 LU

SP to Cable Connector: 20 LU

Stub:

MCC Printed Wire: 19 LU/in

SP Printed Wire: 19 LU/in

Discrete Wire: 10 LU/in

MCC to SP Connector: 80 LU

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5.8.3 Delay Prediction for Accuracy and Tolerance

The delay equation is simply a mathematical model of a physical phenomenon that allows us to predict the performance of nets before the hardware is actually built. Due to the complexity of the phenomenon and the large number of nets to be analyzed, simplifications have been made to the model. These simplifications require that restrictions be placed on the designer to ensure that critical nets are predictable. In addition, certain elements change characteritics with temperature, voltage and normal processing variations. Therefore, the following tolerances have been assigned:

Amdahl Custom ECL LSI basic gate delay (T_B) = ±30%

Transmission media: printed trace, wire connectors, etc. = ±5%

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CHAPTER 6 - CHIP DESIGN

6.1 CELL FEATURES

Each LSI chip contains 100 cells arranged in a 10 x 10 array. Up to 400 3 input OR/NOR gates can be defined and interconnected on any LSI chip. Each cell, according to its position in the array, is designated either high or low power. The high power cells have larger transistors and smaller value resistors than the low power cells. They are intended for driving the large emitter followers outside the array. When driving off-chip, signals must be generated by high power cells through the large emitter followers. Signals internal to the chip, may be driven by transistors. High power cells have somewhat larger transistors for the current switches, but include small transistors for emitter followers. This allows output signals from high power cells to be used on-chip to reduce power usage. In high power cells, the small emitter followers can be bypassed if it is necessary to provide a connection to a larger transistor for driving off-chip. Signals which are driven by large transistors are called external outputs.

6.2 CHIP TOPOGRAPHY

A detailed discription of cell structure is given in the following paragraphs.

6.2.1 Cell Numbering

To provide for an automated cell placement and routing procedure, all pads cells, external emitter followers and routing lanes are numbered. Figure 6-1 shows the numbering scheme. Cells are numbered from 00 to 99, pads from P01 to P84, external emitter followers from X001 to X152, wiring rows from R1 to R488, and wiring columns from C1 to C411. The die itself is always oriented, for reference purposes, with the large VCC pads at the top and bottom, and the large VEE pads at the sides. I/O pads are P01 through P80, except for P23, P38, P63 and P78. They are numbered counter-clockwise starting from the top right corner. Power pads are P81 through P84, plus P23, P38, P63 and P78.

External emitter followers are numbered starting from the top right corner. There are eight groups of 19 transistors. The maximum possible number of external emitter followers dotted together is 19. Conditions limiting emitter dotting are discussed in paragraph 6.3.

Rows are numbered from bottom to top; columns from left to right.

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There are two diffusion patterns for LSI cells. The two diffusion patterns enable cells to be high or low power. These diffusion patterns are placed in fixed positions as shown in figure 6-2. Cell 01, for example, can only be high power due to its position. Whereas, Cell 54 can only be low power.

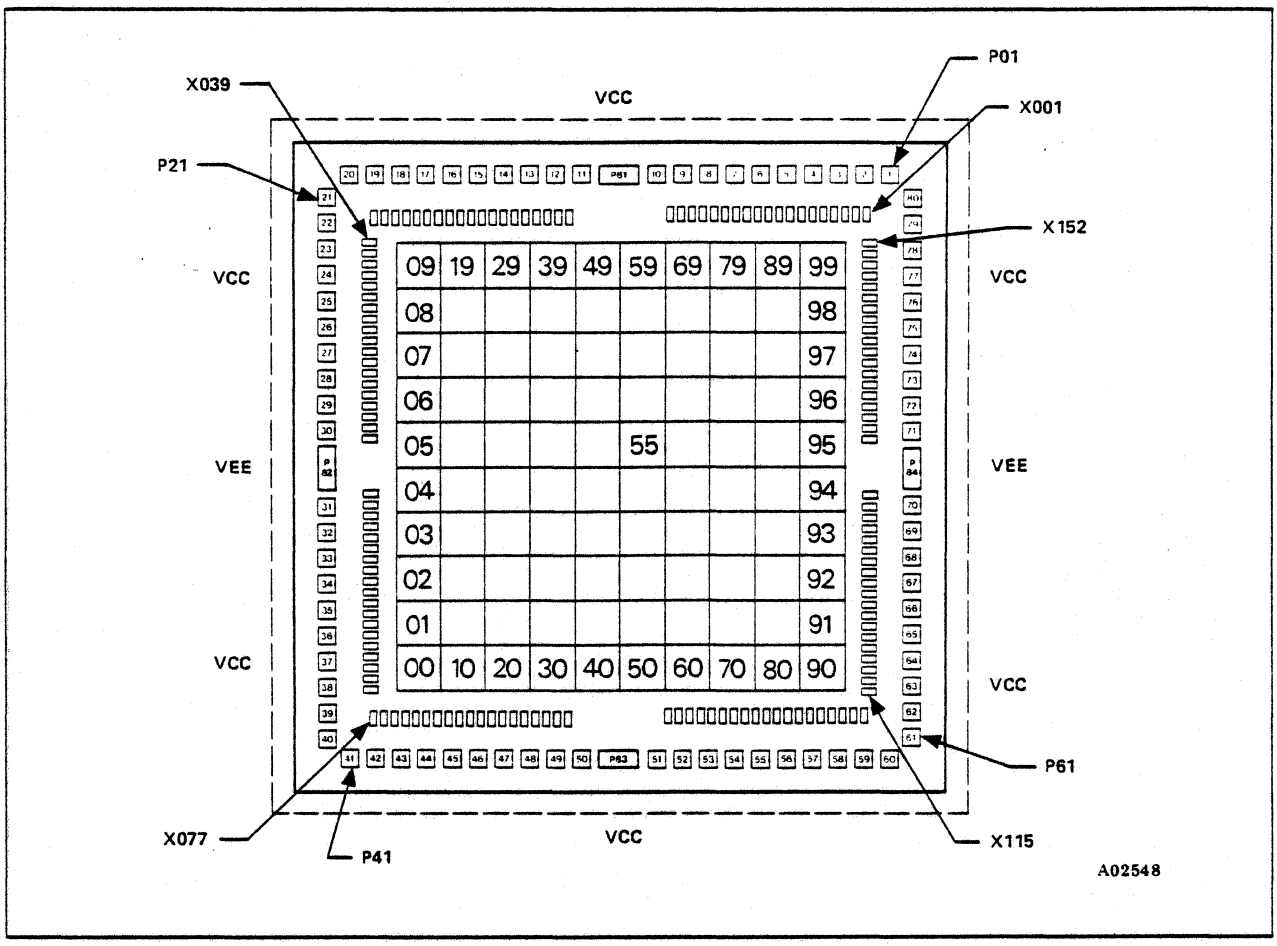

Figure 6-1. LSI Cell Numbering (Chip Top View, Cooling STUD Down)

6.2.2 Cell I/O

The wiring channels are used to interconnect macros. There are 22 first metal channels running horizontally over the cells, and 26 second metal channels running vertically. To simplify the design automation process, the wiring between cells is connected to the outside wiring grid through fixed I/O hitpoints. There are a total of 24 hitpoints, of which 16 are input ports and 8 are output ports. These port locations are shown in figure 6-3. Ports 3-10 and 15-22 are

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input ports. Associated with each output port is one or two resistors connected to VEE. If a macro does not use a particular output port, that port can become an Rp port. An Rp port consists of one 4.0 Kohm pulldown resistor connected to VEE. An internal net which would not otherwise have a pulldown resistor can be connected to an Rp port.

Input ports 3 and 5 go to a dual (common collector) transistor. Any macro which uses port 5, for example, and not port 3 would have the base of the port 3 transistor shorted to its emitter. In other words, the parasitics associated with unused halves of dual transistors cannot be eliminated. Input port pairs 8/9, 15/17, and 20/22 also have a dual (common collector) transistor. Unused input ports can completely disconnect their transistors from the circuits.

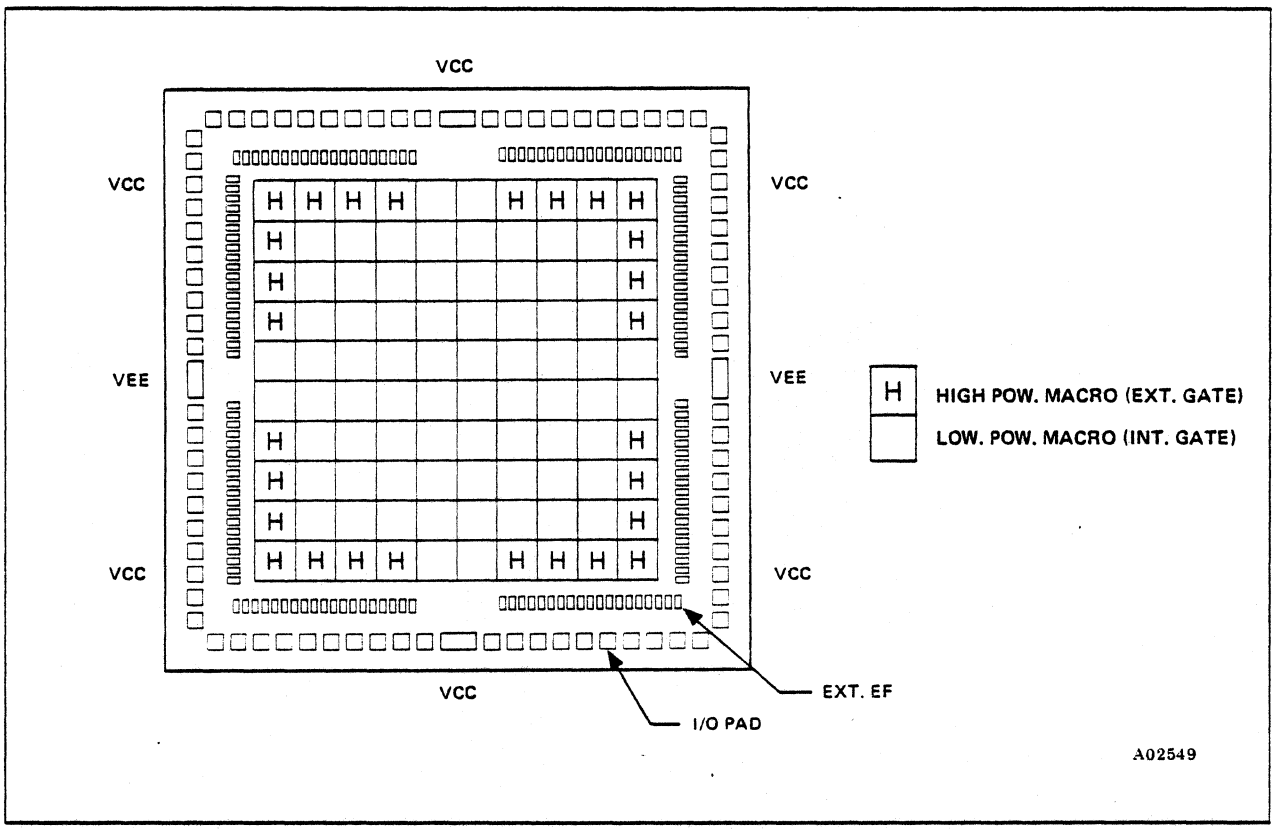

Figure 6-2. High/Low Power Cell Placement

In figure 6-1, I/O port numbers are shown in their normal macro positions. All macros can assume a flipped orientation. In this case, the port number Nf in the flipped position can be found by using the normal position port number Nn and the following equations.

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If Nn $\leq$ 12, Nf = Nn + 12

If Nn $\geq$ 13, Nf = Nn - 12

Logic diagrams show macros with maximum available inputs and outputs (see chapter 5).

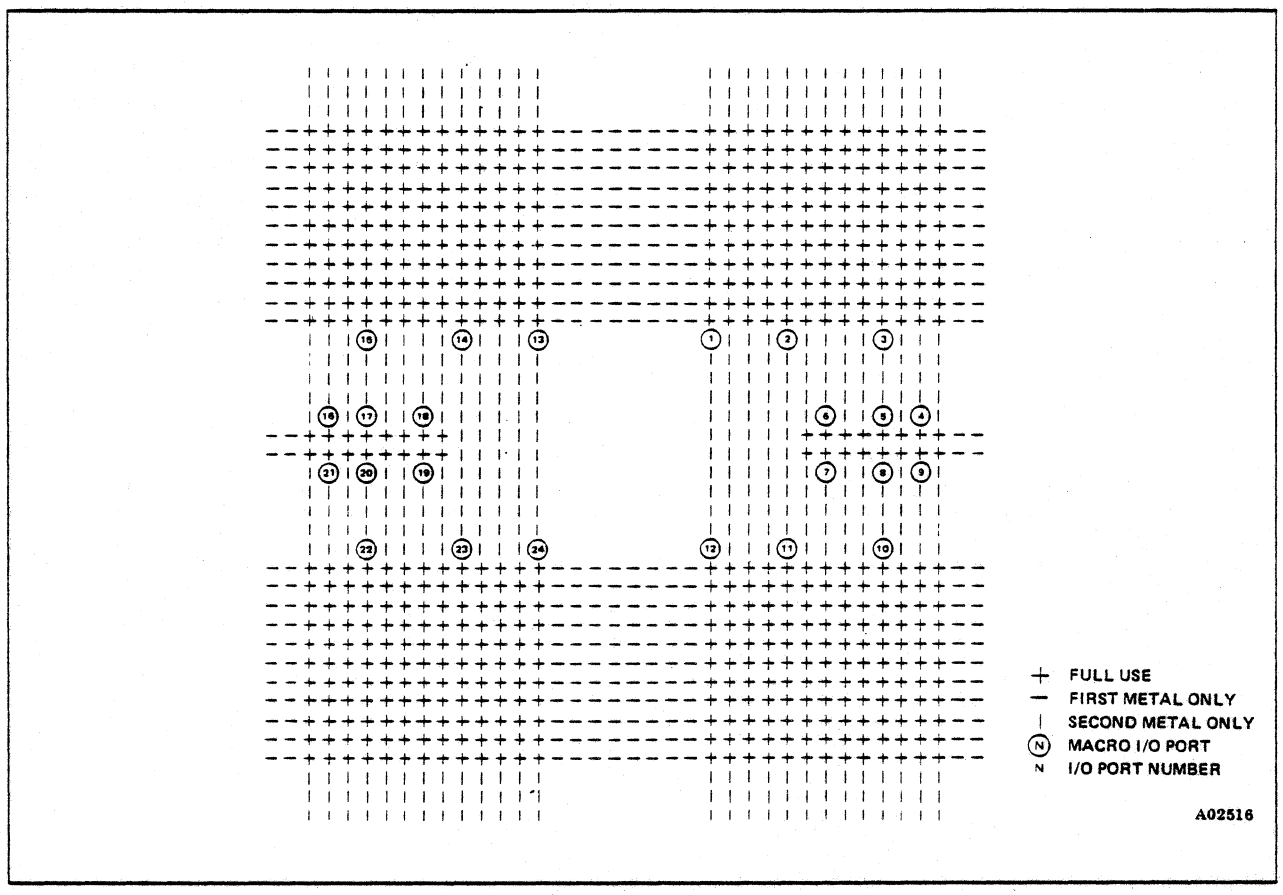

Figure 6-3. Interconnect Grid and I/O Hit Ports (Full Macro)

6.2.3 Average Interconnect Length

The precise signal propagation delay from one macro to another depends on, among other factors, the length of the interconnection. In order to estimate propagation delays on-chip, an average interconnection length can be used. The average interconnection length for gate arrays is 1.5 to 1.7 times the center-to-center spacing of macros. For LSI, the average center-to-center spacing of macros is 357u. An average interconnect length is 600u.

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Using a typical figure of 40 milliohms per square for the aluminum interconnect resistance, the total dc resistance of the average interconnect is 6 ohms. The ac resistance will be approximately the same.

When several gates from the same cell have outputs dotted together, as is often the case, smaller values of interconnect length should be used to estimate the propagation delay. The length of interconnect from emitter to emitter will be approximately 160u, while the total net length is 600u.

6.2.4 Emitter Followers

Surrounding the cell array are 152 common-collector transistors used for driving off-chip 90 ohm nets. There are 76 signal I/O pads, any of which could be used for an output to a 90 ohm net. There are more emitter followers available than pads to allow for a high degree of emitter dotting. For example, if a particular chip has 36 outputs, there are 28 high power cells to drive the large emitter followers. Each cell can have 8 outputs, for a total of 224 high power outputs. This is more than the number of large emitter followers available. For this reason, not all high power cell outputs can drive off-chip. Of the 224 possibilities, however, only about half are independent. The other half is complementary outputs or second copies. There are enough large emitter followers to drive all the independent high power outputs which can be generated on a chip.

6.2.5 Bonding Pads

A total of 76 pads are available for I/O signals. Pads P23, P38, P63 P78, P81 and P83 are VCC pads. The VCC pads are used to minimize the voltage drop from internal chip VCC busses to system ground. Pads P82 and P84 are used for VEE. Pads P82 and P84 are wider to allow for two to three bonding wires each, depending on wire diameter.

The resistance of a packaged I/O pin, from the external package lead to the bonding pads, depends on the pin number in question. Pin and bonding wire resistance will be less than 0.1 ohm. An input would have an additional 6 ohm resistance from the pad to the input macro, and an output would have an additional 0.2 ohm resistance from the external emitter follower E-port to the pad.

Pads are implemented with both layers of metal. I/O signal pads P01 and P20 have 8 possible interconnection wire hit points on R488 of the grid. P41-P61 have 8 hitpoints on R1. On C1 and C411 of the grid, signal pads have 9 hitpoints.

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6.3 ON-CHIP DESIGN RESTRICTIONS

On-chip design restrictions are given in the following paragraphs.

6.3.1 Macro Outputs

In general, each current switch can have two outputs designated as Øin or OR phase output and Øout or Nor phase output. One current switch phase of a low power macro can drive up to three internal emitter followers, if they are available in the macro. Macro 22, for example, has 3 in-phase outputs.

For high power macros, if available, each phase of a current switch can drive one external emitter follower, three internal emitter followers, or one internal and one external emitter follower. There are exceptions for some high power macros in that the outputs may be internal only, as, for example, output P1 on Macro 3299.

6.3.2 Fan Out

The following fan out limits apply to all on-chip nets.

A. Critical Nets:

Clock nets can drive up to 5 bases. One ECL gate input is defined to be one base. Nets critical or non critical that drive a NOR gate that drives off-chip can have a maximum of 10 bases.

B. Non Critical Nets:

The maximum fan out on-chip is 31 bases providing the following conditions are met:

1. Maximum "unit load" $\leq$ 20

   A "unit load" is defined as:

   1 high power base = 1.0 unit load
   1 low power base = 0.33 unit load

   "Unit load" should not be confused with loading units (LU).

2. When the driving gate has multiple emitter followers, a high power gate should be used for the driver.

3. The metal length between the driver and the load gates should be no longer than 10mm. (See paragraph 6.4 for length restrictions.)

4. The pull down resistor(s) should be connected at the output port of the driving gate.

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6.3.3 Emitter Dotting

The following limits apply to all on-chip nets:

Critical Nets.....8 emitters maximum
Non Critical Nets.....16 emitters maximum
Collector Dot Gates.....8 emitters maximum

Table 6-1 contains a list of macro outputs which cannot be dotted.

Table 6-1. EF Dotting Restrictions

MACRO	OUTPUT PORT	COMMENTS
21	All (Skewed Driver Only)	
31	1	Feedback Loop
32	11,12	Feedback Loops
3199	1,23	Feedback Loops
3299	1	Feedback Loop
3399	1,23	Feedback Loops

6.3.4 Multiple Emitter Output (Macro 02, 21, 22)

No more than 1 external EF per gate per phase.

6.3.5 Special Outputs

Table 6-2 lists the macros with outputs that contain multiple emitter followers for counting purposes.

6.3.6 Gate Inputs (Bases)

Multiple inputs of the same gate should not be tied together.

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Table 6-2. Macros with Multiple Emitter Followers

MACROS	UNIT	REMARK
31,-State	2	NOR Internal EF
3299,-State	2	NOR Internal EF
12,-Out	2	NOR Internal EF, External EF
13,-Out	2	NOR Internal EF, External EF
42,+Out	2	OR External EF
43,-Out	2	NOR External EF
43,+Out	2	OR External EF

1. Internal EFs and external EFs can be dotted only within respective groups. An internal EF cannot be dotted with an external EF.
2. When two or more internal EFs are dotted, two pulldown resistors must be used as terminators on-chip.
3. When Macro 42 is used as a RAM driver, the output of Macro 42 cannot be dotted.
4. "On-chip EF-Dot" of external EF of M42 cannot drive on/off-chip loads. EF-Dot of M42 is made as an "off-chip EF-Dot." "On-chip EF-Dot" means EF-Dot is within the same chip and is using one LSI pin for off-chip driving. "Off-chip EF-Dot" means EF-Dot is through the LSI chip.
5. "On chip EF Dot" of external EF of M43 can drive off-chip loads through one LSI pin when the output is dotted OR.

6.4 LIMITATIONS OF INTERNAL NET WIRE

A main line is defined as a line connecting a driver of interest to a receiver gate of interest. The equation that follows should be applied to all combinations of driver gates and receiver gates on a net.

$$L_N \geq \sum_{N=1}^{\#\ of\ stubs} ((NWLD_N) \times (KL\ (NLPB_N) + KH\ (NHPB_N) + KR\ (NPD_N))$$

where:

$NWLD_N$ Normalized wire length from the driver gate of interest to stub n.

$NLPB_N$ Total number of low power bases on stub n.

$NHPB_N$ Total number of high power bases on stub n.

NPD_N Total number of pull down resistors on stub n.

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ln Wire length of the first metal (um) + 2/3 x wire length of the second metal (um). Thus, ln is the normalized wire length from the driver gate of interest to stub n.

KL 0.005

KH 0.015

KR 0.5

L_N (limited length) is defined in table 6-3.

Table 6-3. L_N (Limited Length)

DRIVER GATE OF INTEREST \ RECEIVER GATE OF INTEREST			high power gate with external "NOR" output	high power gate without external "NOR" output and low power gate
low power gate	without same phase other output		3000 um	5000 um
	with same phase other outputs	total # of Rps on same phase other outputs = 1	2600	4600
		total # of Rps on same phase other outputs = 2	2200	4200
		total # of Rps on same phase other outputs = 3	1800	3800
		total # of Rps on same phase other outputs = 4	1400	3400
high power internal gate	without same phase other output		3500	5500
	with only internal outputs on same phase other outputs	total # of Rps on same phase other outputs = 1	3350	5350
		total # of Rps on same phase other outputs = 2	3200	5200
		total # of Rps on same phase other outputs = 3	3050	5050
		total # of Rps on same phase other outputs = 4	2900	4900
	with an external output on same phase other outputs	total # of Rps on same phase other outputs = 0	2000	4000
		total # of Rps on same phase other outputs = 1	1850	3850
		total # of Rps on same phase other outputs = 2	1700	3700

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In counting the number of bases on each stub, the following macros should be counted as follows:

Macro 43 = 2 x high power bases/fan out
Macro 42 = 3 x high power bases/fan out

If the receiver gate of interest is Macro 12 or 13 with external outputs, the LN (limited length) of the external "NOR" gate should be applied.

In counting the wire length, the following values should be used:

first metal = 8 um/grid
second metal = 10 um/grid

If the "+STATE" output of all latches was the output of the driver gate of interest, the "+STATE 2" output should be considered the same as the same phase other output.

Figure 6-4 shows the limitations of metal length on a chip. The driver gate of interest is a low power gate. The driver gate of interest has 1 same phase other output and 1 Rp. The receiver gate of interest has external "NOR" output.

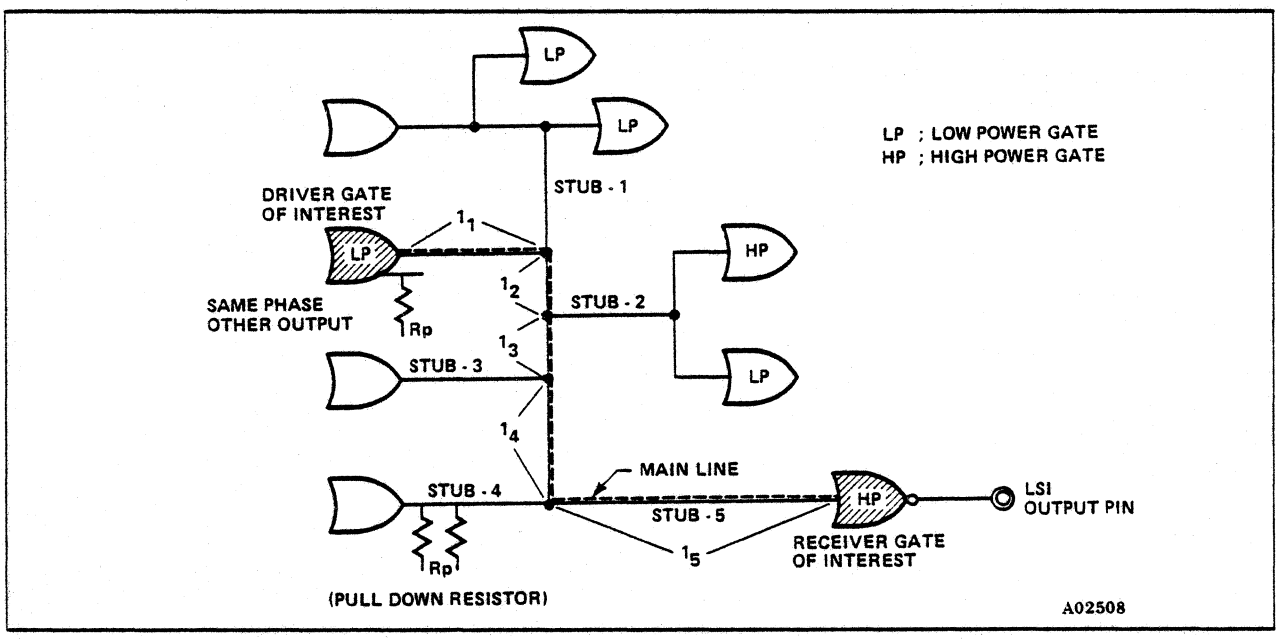

Figure 6-4. Limitations of Internal Net

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Referring to Table 6-3 and using the following conditions, the length limitation would be calculated as follows:

Section	First Metal Length	Second Metal Length
L1	400 um	600 um
L2	800 um	450 um
L3	100 um	300 um
L4	200 um	0 um
L5	700 um	900 um

LN = 2600 um (refer to table 6-3).

Then the normalized wire length of each section is:

L1 = 400 + 2/3 x 600 = 800 um
L2 = 800 + 2/3 x 450 = 1100 um
L3 = 100 + 2/3 x 300 = 300 um
L4 = 200 + 2/3 x 0 = 200 um
L5 = 700 + 2/3 x 900 = 1300um

$2600 \geq 800 + (800 + 1100) + (800 + 1100 + 300) +$
$(800 + 1100 + 300 + 200) + (800 + 300 + 200 + 1300) =$
$3500 \times KL + 5600 \times KH + 4800 \times KR = 2501.5$

Therefore, this example satisfies the length limitation.

6.4.1 Limitation of Wiring Length for External Emitter Followers

Total wire length (LM3) from the macro output port of the high power external gate to the base port of the external emitter follower should be as follows:

"+STATE" output macros 32, 31, 3399, 3199,3299 = LM3 $\leq$ 2 mm

other outputs = LM3 $\leq$ 4 mm

6.5 CHIP POWER DISSIPATION

The normal power dissipation of each circuit element is tabulated in tables 6-4 and 6-5.

6.5.1 Power Consumption of MB12K LSI Chip

Table 6-5 shows the power consumption of a current switch. Unused gates consume no power. The value of the table includes the power consumption of the on-chip net for Macros 2399, 32, 31, 3399, 3199 and 3299.

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Table 6-4. Nominal Power Dissipation (Milliwatts)

DESCRIPTION	TYPE	LOW POWER VIL/VOL VIH/VOH	HIGH POWER VIL/VOL VIH/VOH
CURRENT SWITCH	NORMAL	1.78/2.37	5.76/7.66
	MACRO 13	2.6	6.3
	MACRO 42 (BD)	--	17.75/21.9
	MACRO 43 (MD)	--	11.5/15.3
INTERNAL EF	W/2 Pull Down 2K ohms	3.24/4.68	
	W/1 Pull Down 4K ohms	1.71/2.43	
EXTERNAL EF 90 ohms TERM		--	5.9/10.9
BIAS DRIVER for V *		3.4	6.6
BIAS DRIVER for V *		1.5	2.9
*Each Macro.			

6.5.2 Internal EF ($P_{int.ef}$)

Table 6-5 shows the power consumption of internal EFs. In EF dotting, despite the number dotted, every dot consumes 4.18 mW. The EF power consumption of Macro 3299 -CLOCK output and -PSTATE output are included in the CS. Unused EFs consume no power.

6.5.3 External EF ($P_{ext.ef}$)

Despite the number of EFs dotted, every dot consumes 8.3 mW. Macro 42 consumes 16.6 mW because of its two 90 ohm terminations.

6.5.4 Bias Driver (P_{bd})

The circuit to generate Vref and the circuit to generate Vcd, used for collector dotted macros, are the two types of Bias Drivers used. Every full macro includes both kinds of Bias Drivers. When the full macro uses one or more gates, it consumes 3.35 mW (in low power macro) or 6.62 mW (in high power macro). If Macros 11, 0299, 0199, 3299, 10,

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Table 6-5. Power Consumption of 580 LSI

	CS		EF	
MACRO	Low Power	High Power	Internal	External
8	1.98 mW	6.37 mW		
21				
02				
05				
04			2.09/4.18	
11	3.96	12.74		
0299	5.94	19.111Rp/2Rp		
0199	7.92	25.48		
10	3.96	12.74	4.18	
12	3.96	12.74	2.09/4.18	8.3 mW
13	5.26	12.74	4.18	
13	5.26	12.74		
32	8.14	16.92		
31	6.05	14.83		
3399	14.19	31.75	2.09/4.18	
3199	14.19	31.75		
3299	10.01	27.57		
2399	26.73	-----	4.18	
21	1.98	-----	4.18 (+Clock)	
42	-----	18.5	----	16.6
43	-----	12.74	2.09/4.18	8.3
10	3.96	12.74	2.09/4.188.3	
23	14.52	-----	4.18 (+Clock)	

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13 or 12 are included in the full macro, 1.40 mW (in low power macro) or 2.88 mW (in high power macro) should be added to the power consumption. Bias Drivers of unused full macros consume no power.

6.5.5 Power Consumption Computation of 580 LSI

The typical power consumption of 580 LSI is calculated by using the following equation:

$$P_{ltyp} = P_{c3} + P_{int.ef} + P_{ext.ef} + P_{bd}$$

The current consumption of 580 LSI is calculated by the following expressions:

-3.6 V Current:

$$I_{ltyp}\ (-3.6) = P_{ltyp}\ \frac{(mW) - P_{ext.ef}\ (mW)}{3.6\ (V)}\ (mA)$$

Ground Current:

$$I_{ltyp}\ (GND) = I_{ltyp}\ (-3.6) + \sum \frac{P_{ext.ef}\ (mW)}{1.067\ (V)}\ (mA)$$

6.5.6 Max/Min Power Consumption of an LSI Chip

Max/Min power consumption and Max/Min current of an LSI chip are calculated by the following equations:

$$P_{lmax/min} = P_{ltyp} * \left(1 \pm \frac{36}{100}\right)$$

$$I_{lmax/min} = I_{ltyp} * \left(1 \pm \frac{34}{100}\right)$$

6.6 R-PACK POWER CONSUMPTION

R-pack consists of 24 90 ohm resistors to -2V. It is used for terminating nets on MCCs. When a termination resistor isn't used, it doesn't consume any power. Each terminator that is used consumes 7.06 mWatts (7.68 in mAmps). When all 24 terminators are used, the R-pack dissipation is 169.4 mWatts (184.3 in mAmps). If a terminator is used as an unused LSI input tie-down (no outputs), then it can be considered to dissipate no power.

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For max/min power consumption and current of R-pack use the following equations:

$$P_{rmax/min} = P_{rtyp} * (1 \pm \frac{30}{100})$$

$$I_{rmax/min} = I_{rtyp} * (1 \pm \frac{20}{100})$$

6.7 NOMINAL CHIP POWER DISSIPATION CALCULATION EXAMPLE

The power dissipation of a basic gate circuit can be calculated as shown in table 6-6.

Table 6-6. Nominal Power Dissipation with One Pull Down Resistor

DEVICE	POWER
Low Power NOR (OR)	4.9 mw
High Power Internal NOR (OR)	10.1 mw
High Power External NOR (OR)	15.5 mw

The nominal power dissipation of a 400 gate chip (1 Rp/gate) is calculated as follows:

288	Low Power Internal	
	4.9 mw x 288 =	1411 mw
82	High Power Internal	
	10.1 mw x 82 =	828 mw
30	High Power External	
	15.5 mw x 30 =	465 mw
		2704 mw (Total)

6.8 CHIP DESIGN RESTRICTIONS

Emitter follower restrictions are explained in the following paragraphs.

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6.8.1 Simultaneous Emitter Follower Switching

Due to on-chip inductance and other noise margin considerations, the number of EFs that switch at the same time must be limited. This limitation is also dependent on their location on the chip. Table 6-7 provides the limitations.

6.8.2 Skewing EF Switching

By skewing in time, the number of EFs on a chip that can be switched increases as shown in figure 6-5. Cases A and B are from table 6-7.

Refer to table 6-8 to determine the EF switching case.

6.8.3 Exceptions to Simultaneous EF Switching Rules

A large number of simultaneous switching emitter followers will cause a glitch on the quiet output lines of a chip. The limit to 18/36 simultaneous switching EF ensures that the glitch stays below a tolerable magnitude. In some applications, however, it may be possible to live with a larger glitch. Following is a list of conditions when exceeding the 18/36 limit may be considered:

1. No latch on the chip.
2. Quiet lines cannot be a clock, set/rest term of latch, RAM Address, RAM WE.
3. Enough time must be available in the path from the quiet line to the next latch level such that the glitch subsides at the latch before the clock.

NOTE
The ASAP delay program will not be able to take the glitch into account.

For delay calculations, it can be assumed that the glitch dies down no later than 700 psec after the last of the simultaneous switching EF has switched.

6.8.4 Additional Delay

An additional delay per output for simultaneous EFs' switching of 10 psec per output must be added.

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Table 6-7. Simultaneous EF Switching Limitations

CASE	CIRCUIT TYPE ON LSI	MAXIMUM # OF EF	EF LOCATION
A	MEMORY DRIVER (Driving RAM input) ASYNCHRONOUS DRIVER (SET, RESET, SCAN IN)	18	4 | 5 / 5 | 4
B	NORMAL	36	9 | 9 / 9 | 9

1. To insure that no more than 9 EFs get placed by the router in one quadrant, the designer needs to make a physical assignment for EFs and the associated Chip I/Os using the physical extension of DRL.
2. Macro 42, when terminated in 45 ohms (two 90 ohm terminators), is counted as 2 emitter followers.
3. Macro 43, when terminated in 90 ohms, is counted as 1 emitter follower. Up to 36 Macro 43s may switch simultaneously if none of the macros drive a RAM or asynchronous input.
4. A dot of several emitter followers terminated in a single 90 ohm terminator counts as a single EF.
5. Opposite phases of these EFs driving off-chip will practically compensate the simultaneous switching effect. Use the following NA formula to determine the allowable maximum of simultaneous EF switching.

Where: $N_S\left(1+\frac{\Delta t1}{1.5}ns\right)+N_D\left(1-\frac{\Delta t2}{.5ns}\right)$

$\overline{N}_A$ = allowable number of EFs switching in the same direction within the skew of t1.

N_S = 36 for normal gates; 18 for Macro 43's driving RAMs, asynchronous set, rest, scan in.

N_D = number of pairs of EF switching in opposite direction within the max skew of t2.

Δt_2 = .22 for macro 43; .14 for normal gate.

Δt_1 = 0 (in general)

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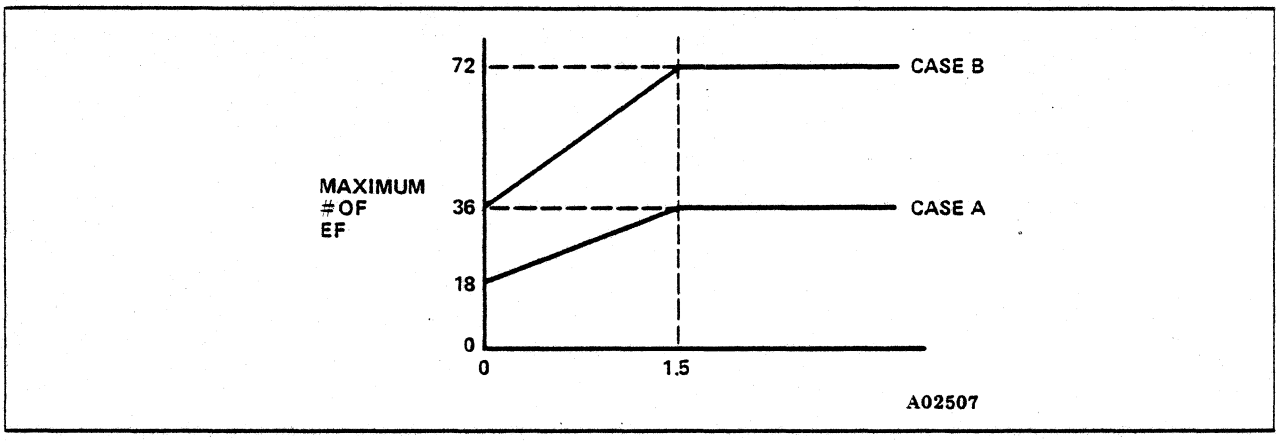

Figure 6-5. EF Switching Skew

Table 6-8. Simultaneous EF Switching Case Determination

DRIVER TYPE	INPUT TYPE	CASE (LIMIT)
Macro 43 (OR output)	RAM	A (18)
Macro 43 (NOR output)	RAM	Not Allowed
Macro 43	Asynchronous	A (18)
Macro 43	Normal*	B (36)
Other**	RAM	Not Allowed
Other**	Asynchronous	A (18)
Other**	Normal*	B (36)

* Normal = any but RAM or Asynchronous
** Other = any but Macro 43

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CHAPTER 7 - LATCH RESTRICTIONS

7.1 GENERAL

Macros 31, 32, 3199, 3299, and 3399 are latch macros. Refer to figures 7-1 thru 7-5 for schematics and logic diagrams. Latches should not be made from other macros. Each latch macro has sample and hold inputs. Only skewed drivers, Macros 21 and 22, should be used to drive latch sample and hold inputs. On any single latch, all sample and hold inputs should be driven by the same skewed driver gate. Skewed driver (SD) outputs should not be dotted. The fan out of the skewed driver sample and hold outputs should be equalized, with a maximum fan out of five bases.

A re-entry net, a chip output which has loads on-chip as well as off-chip, should not be used as a latch input.

The latch feedback net, IPFB, needs two 4K pulldowns to drive other gates.

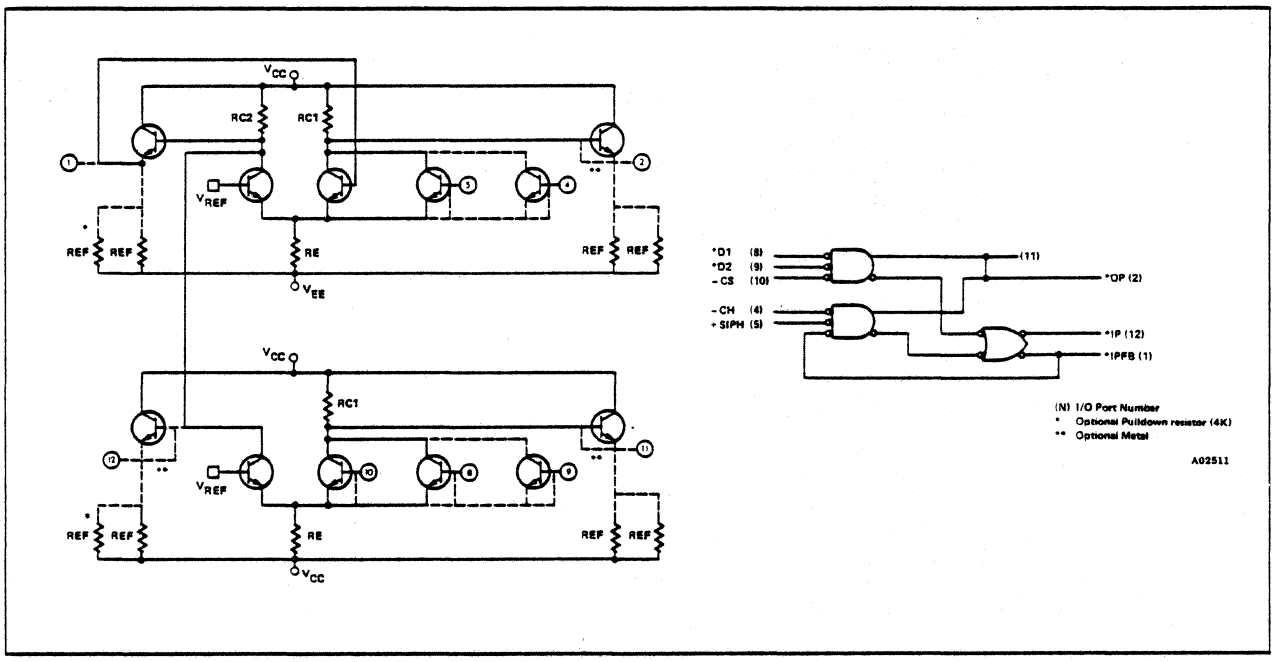

Figure 7-1. Macro 31 In-Phase Latch

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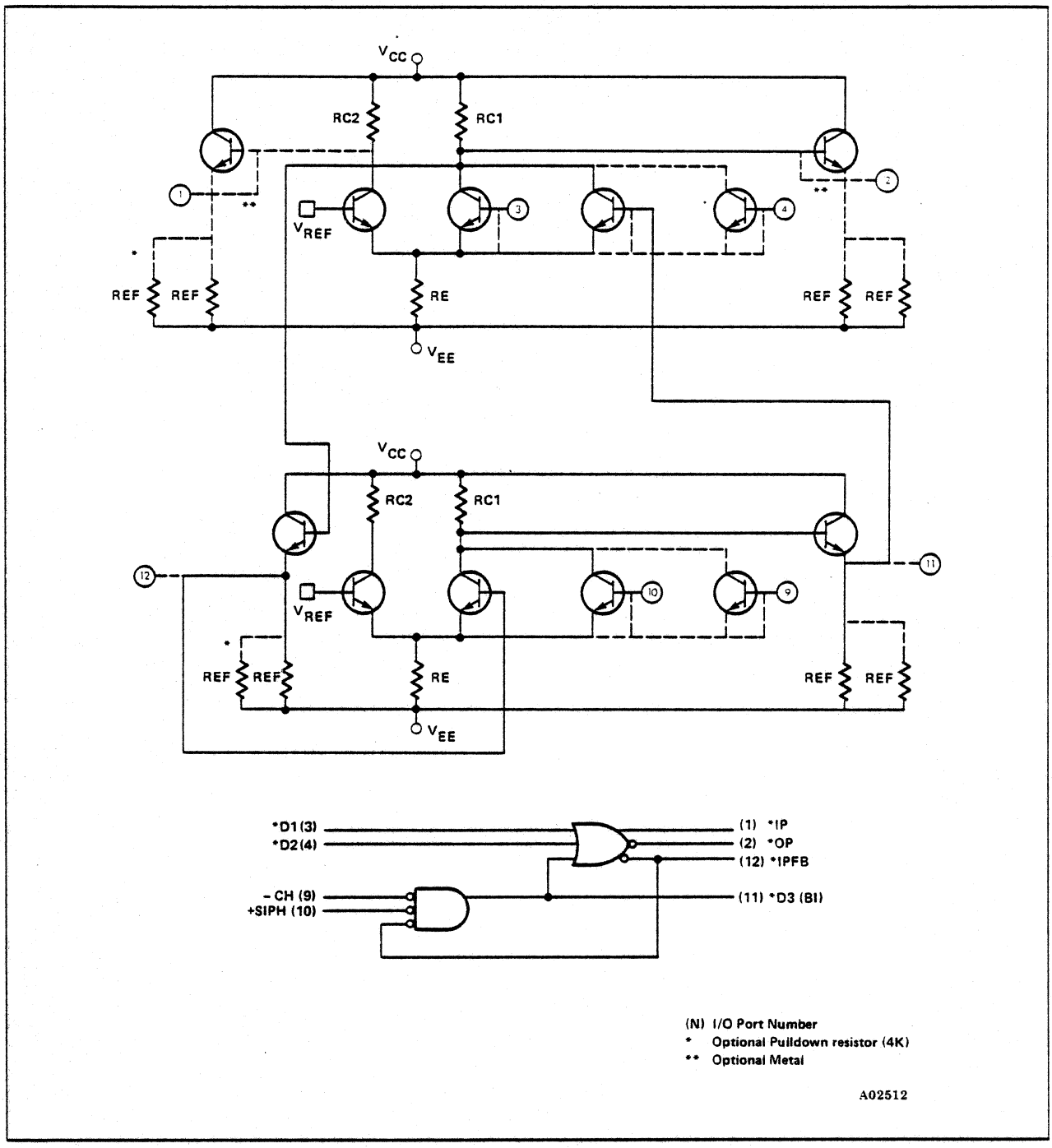

Figure 7-2. Macro 32 Out-of-Phase Latch

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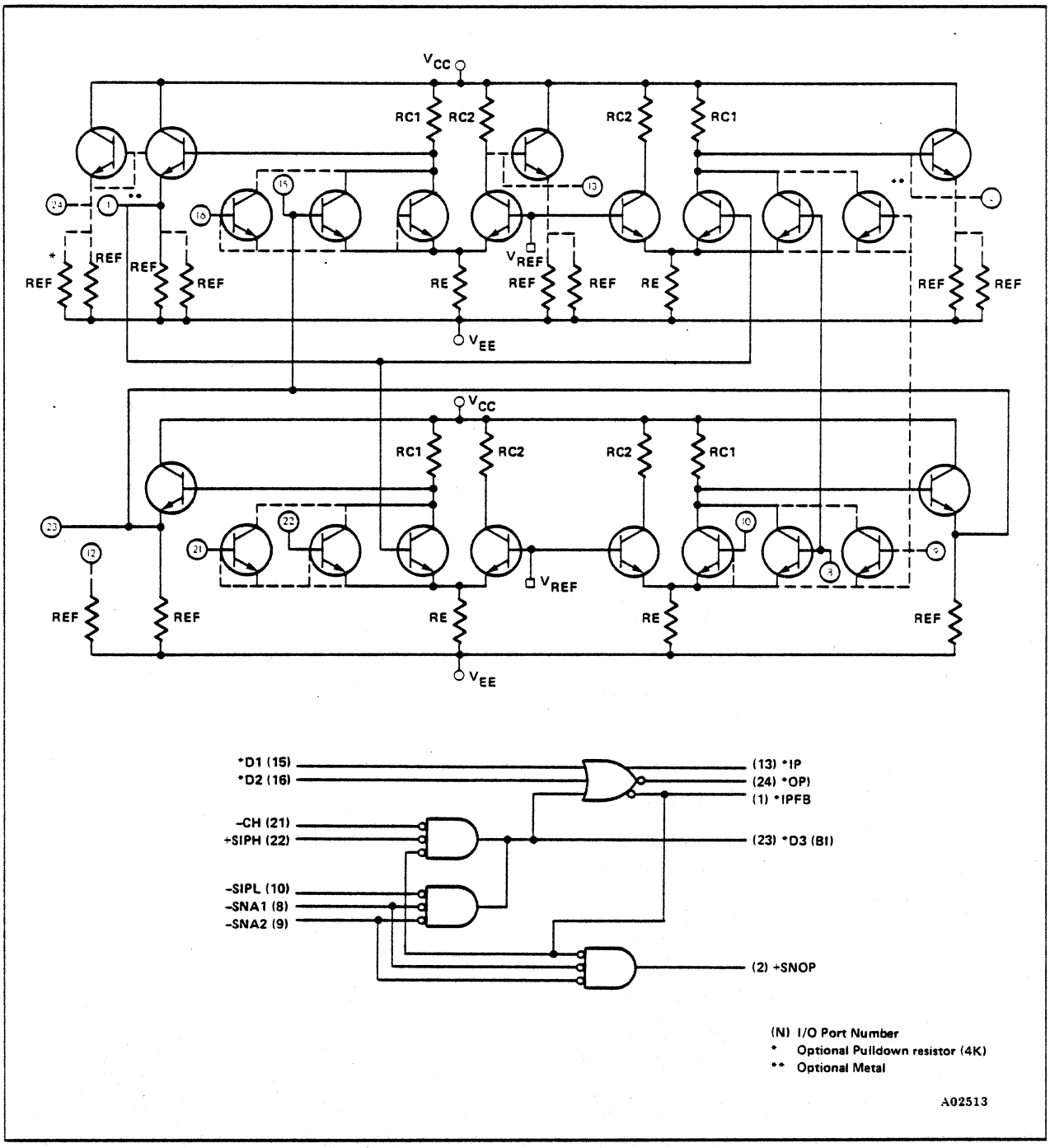

Figure 7-3. Macro 3199 Out-of-Phase Latch

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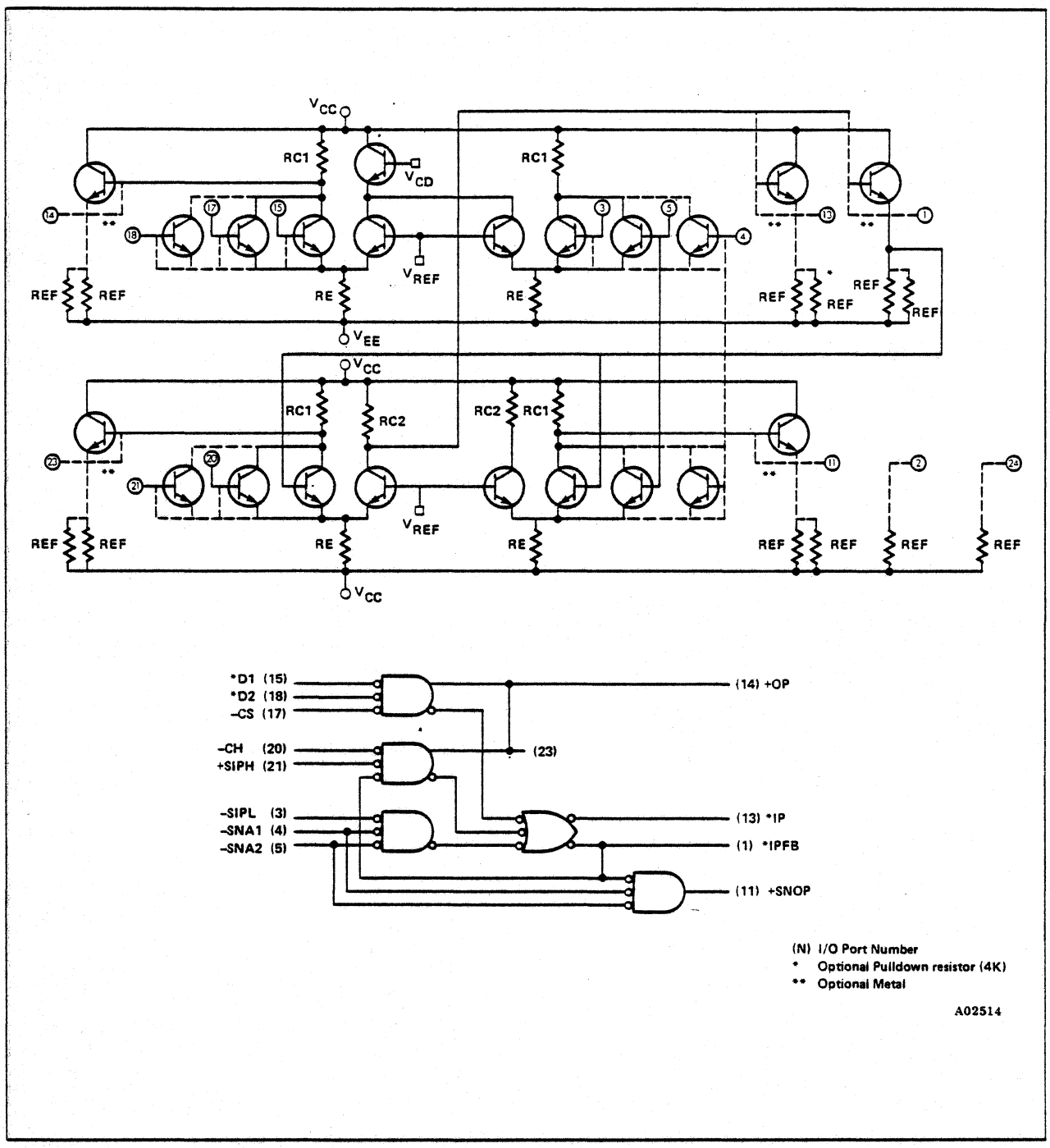

Figure 7-4. Macro 3299 In-Phase Latch

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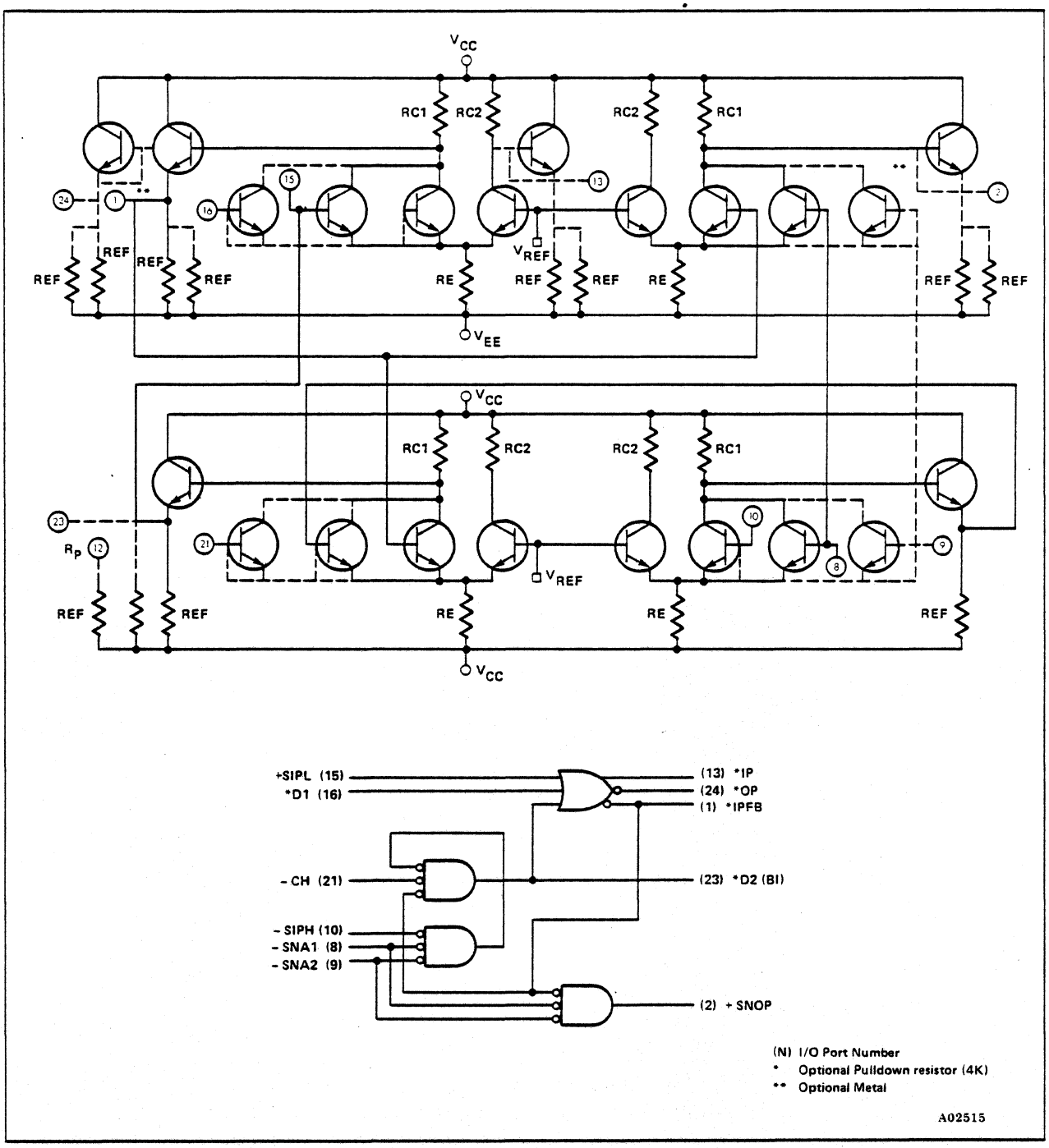

Figure 7-5. Macro 3399 Out-of-Phase Latch

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7.2 SKEWED CLOCK DRIVER

A skewed clock driver is designed to minimize the noise problem on latch outputs. Macro M21 and Macro M22 are designed as a skewed clock driver. A skewed driver must be located in a low power cell. Refer to figures 7-6 and 7-7.

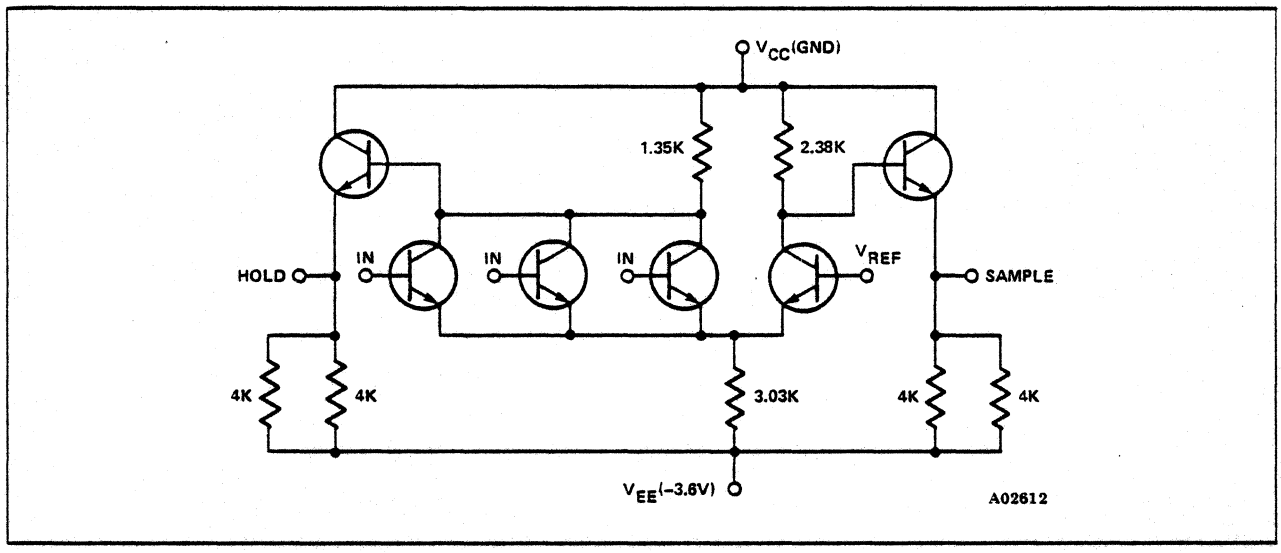

Figure 7-6. Skewed Clock Driver Schematic

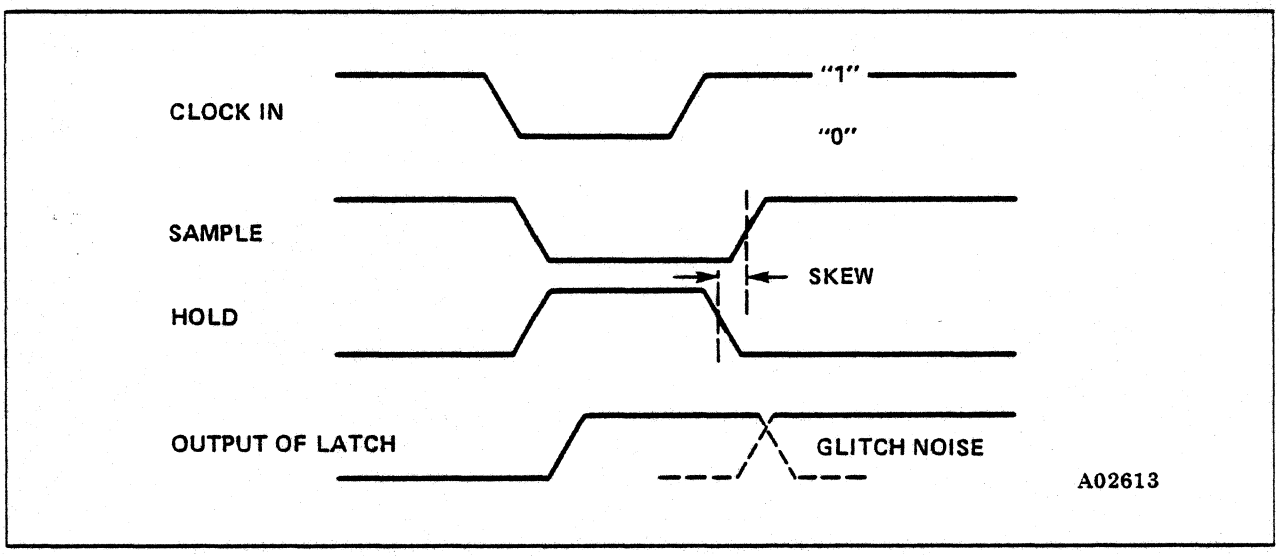

Figure 7-7. Skewed Driver (SD) Signal Waveform

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7.3 IN-PHASE LATCH RESTRICTIONS

All in-phase latches (Macros 31 and 3299) must adhere to the following restrictions:

1. Fan out of latch feedback net, IPFB, should not exceed two, not including the intra macro loads.

2. The out-of-phase (ØOUT) output of the in-phase latch (Macros 31 and 3299) must be buffered when driving off-chip.

3. The out-of-phase output of an in-phase latch glitches when the clock sample and hold lines switch. There is a glitch generated by the leading edge of the clock as well as by the trailing edge.

When the following equation cannot be met, leading edge glitch occurs.

$$(T_{SAMPLE}\ (DN\emptyset IN) + T_{DATA1}\ (UP\emptyset OUT)) -$$

$$(T_{HOLD}\ (DN\emptyset OUT) + T_{LATCH1}\ (DN\emptyset OUT)) \leq 0 \text{ psec}$$

When the following equation cannot be met, trailing edge glitch occurs.

$$(T_{SAMPLE}\ (UP\emptyset IN) + T_{DATA1}\ (DN\emptyset OUT)) -$$

$$(T_{HOLD}\ (DN\emptyset OUT) + T_{LATCH1}\ (UP\emptyset OUT)) \geq 100 \text{ psec}$$

7.3.1 Glitches

Asynchronous set or reset signals and signals which control clocks or write strobes cannot tolerate any glitches. The leading edge glitch is in general no problem. The trailing edge glitch must be avoided. The trailing edge glitch can occur as late as a full clock width (3.5 nsec) after the data switches. Therefore, an allowance of 3.5 nsec delay must be made when timing out the paths driven by the out-of-phase outputs of an in-phase latch. The in-phase output (ØIN) of the in-phase latch equation for glitch free operations follows (refer to figure 7-8).

Clock trailing edge glitch suppression equation:

$$(T_{SAMPLE}\ (UP\emptyset IN) + T_{DATA2}\ (UP\emptyset IN)) -$$

$$(T_{HOLD}\ (DN\emptyset OUT) + T_{LATCH2}\ (DN\emptyset IN)) \geq 0 \text{ psec}$$

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Clock leading edge glitch equation:

$(T_{SAMPLE}\ (DN\emptyset IN) + T_{DATA2}\ (DN\emptyset IN)) -$

$(T_{HOLD}\ (UP\emptyset OUT) + T_{LATCH2}\ (UP\emptyset IN)) \leq 0$ psec

Collector dot saturation check for Macro 31 only:

$(T_{SAMPLE}\ (DN\emptyset IN) + T_{DATA2}\ (DN\emptyset IN)) -$

$(T_{HOLD}\ (UP\emptyset OUT) + T_{LATCH2}\ (UP\emptyset IN)) \geq T1$

$(T_{SAMPLE}\ (UP\emptyset IN) + T_{DATA2}\ (UP\emptyset IN)) -$

$(T_{HOLD}\ (DN\emptyset OUT) + T_{LATCH2}\ (DN\emptyset IN)) \leq T2$

where:

T1 = -800 psec (low power) or -500 psec (high power)

T2 = 800 psec (low power) or 500 psec (high power)

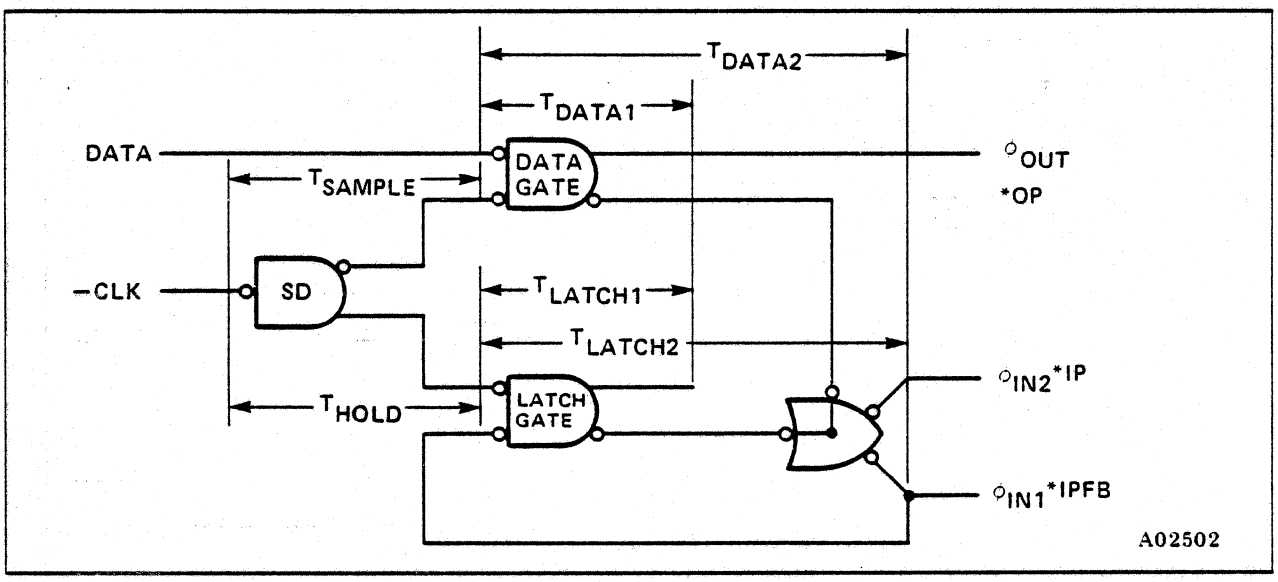

Figure 7-8. In-Phase Latch Path Definitions

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Clock pulse width check. Refer to figure 7-9.

$(T_{WCLK} + T_{HOLD}\ (DN\emptyset OUT)) -$

$(T_{HOLD}\ (UP\emptyset OUT) + T_{LATCH}\ (UP\emptyset IN)) \geq 300$ psec

$(T_{WCLK} + T_{SAMPLE}\ (UP\emptyset IN) + T_{DATA1}\ (DN\emptyset IN)) -$

$(T_{SAMPLE}\ (DN\emptyset IN) + T_{LATCH}\ (DN\emptyset OUT)) \geq T_{SKEW} + 200$ psec

Setup time check for In-Phase latches:

To set up data "V_{OH}":

$(T_{WCLK} + T_{HOLD}\ (DN\emptyset OUT)) -$

$(T_{SAMPLE}\ (DN\emptyset IN) + T_{DATA}\ (UP\emptyset IN)) \geq T_{SKEW} + 300$ psec

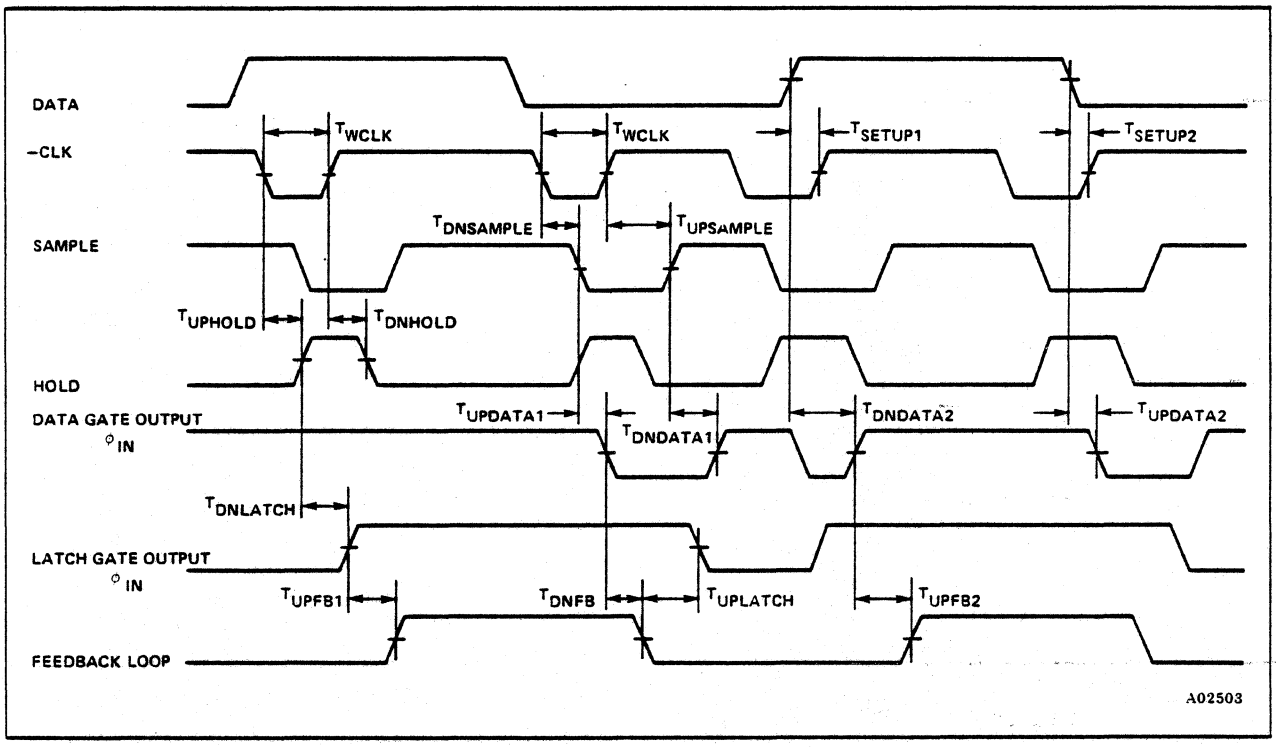

Figure 7-9. In-Phase Latch Timing Diagrams

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To set up data "V_{OL}":

$(T_{WCLK} + T_{SAMPLE}\ (UP\emptyset IN) + T_{DATA}\ (UP\emptyset IN)) -$

$(T_{SAMPLE}\ (DN\emptyset IN) + T_{DATA}\ (DN\emptyset IN) + T_{LATCH}\ (DN\emptyset IN))$

$\geq T_{SKEW} + 200$ psec

7.4 OUT-OF-PHASE LATCH RESTRICTIONS

The following restrictions apply to out-of-phase latches (Macros 32 and 3199):

1. Data Gate Emitter Follower Dot ≤ 8.
2. All data gates of the same latch must be driven from the same sample output.
3. No dotting is allowed to latch feedback paths.
4. Fan outs of the sum of D3 and IPFB must not exceed two, including the intra macro loads.
5. The following equations insure that there are no glitches due to the clock edges.

   For the trailing edge of the clock:

   $(T_{SAMPLE}\ (UP\emptyset IN) + T_{DATA}\ (DN\emptyset OUT)) -$

   $(T_{HOLD}\ (DN\emptyset OUT) + T_{LATCH}\ (UP\emptyset OUT)) \geq 100$ psec

   For the clock's leading edge glitch:

   $(T_{SAMPLE}\ (DN\emptyset IN) + T_{DATA}\ (UP\emptyset OUT)) -$

   $(T_{HOLD}\ (UP\emptyset OUT) + T_{LATCH}\ (DN\emptyset OUT)) \leq 0$ psec

   Refer to figure 7-10 for out-of-phase path definitions and figure 7-11 for out-of-phase latch timing.
6. The following equations are to ensure that the clock pulse width (T_{WCLK}) is wide enough to ensure that the latch will work.

   $(T_{WCLK} + T_{HOLD}\ (DN\emptyset OUT)\ ) -$

   $(T_{HOLD}\ (UP\emptyset OUT) + T_{LATCH}\ (DN\emptyset OUT) + T_{FB1}\ (UP\emptyset OUT)) \geq 300$ psec

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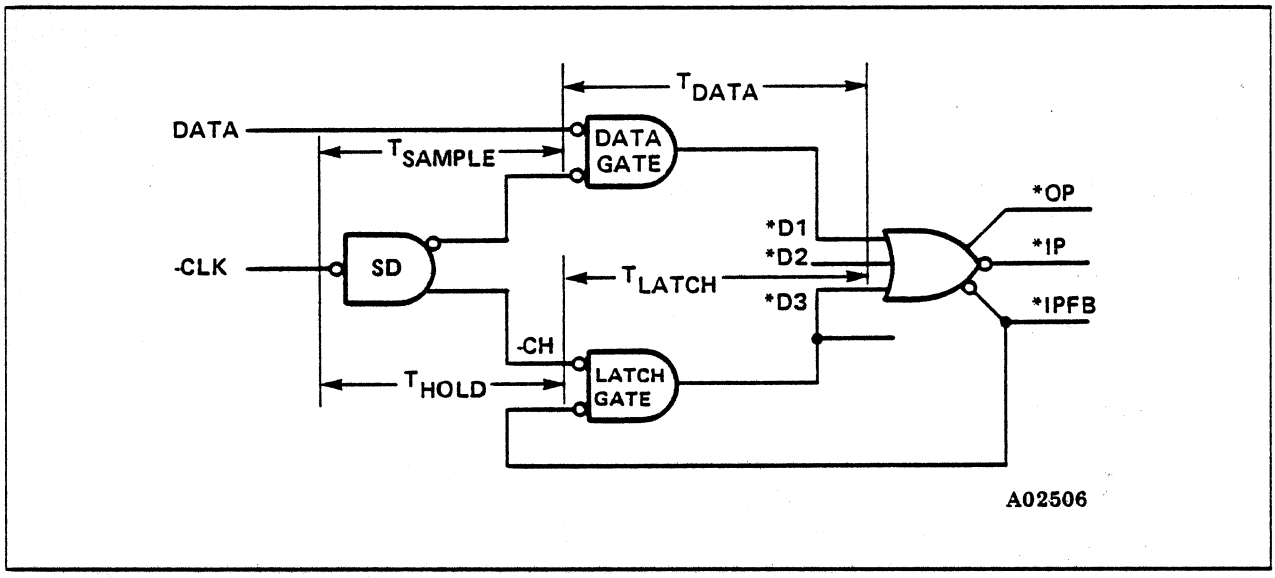

Figure 7-10. Out-of-Phase Latch Path Definitions

$(T_{WCLK} + T_{SAMPLE}\ (UP\emptyset IN) + T_{DATA1}\ (DN\emptyset OUT)) -$

$(T_{SAMPLE}\ (DN\emptyset IN) + T_{DATA1}\ (UP\emptyset OUT) + T_{FB}\ (DN\emptyset OUT) +$

$T_{LATCH}\ (UP\emptyset OUT)) \geq T_{SKEW} + 300$ psec

where:

T_{FB} Delay from the Data Gate Output to the Feedback Loop.

T_{FB1} Delay from the Latch Gate Output to the Feedback Loop.

T_{DATA1} Sample to Data Gate Output delay.

7. The data input must remain unchanged during the time interval before the positive transition of the clock. This time interval is called the data setup time, and T_{SKEW} is the clock skew.

For data switching from a "V_{OL}" to "V_{OH}":

$(T_{WCLK} + T_{HOLD}\ (DN\emptyset OUT)) - (T_{SAMPLE}\ (DN\emptyset IN) +$

$T_{DATA}\ (DN\emptyset OUT) + T_{FB}\ (UP\emptyset OUT) \geq T_{SKEW} + 300$ psec

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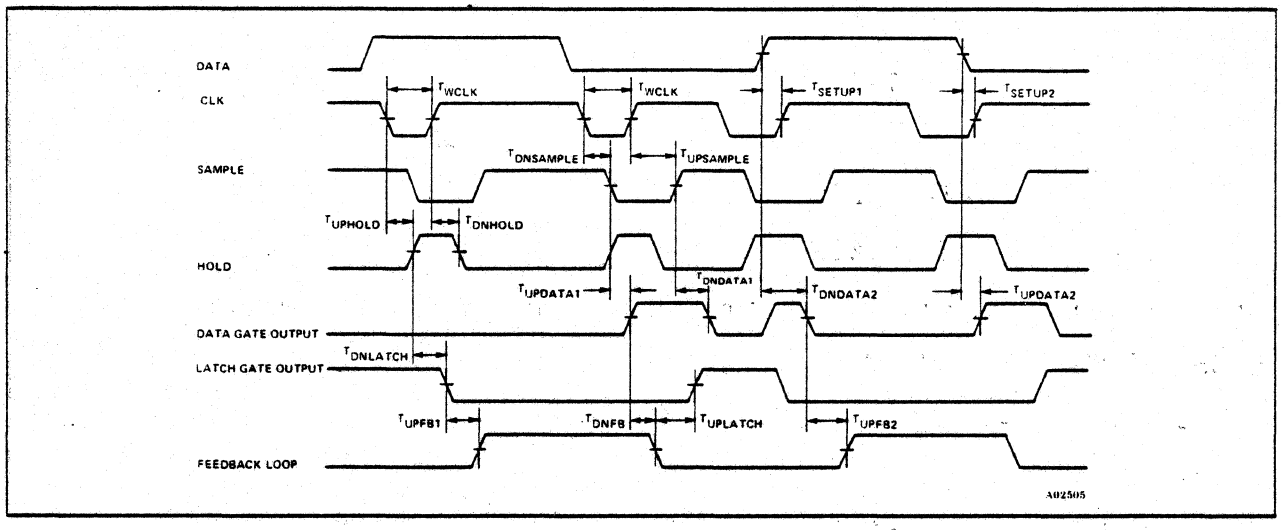

Figure 7-11. Out-of-Phase Latch Timing Diagram

For setting up a "V_{OL}" on the data input:

$$(T_{WCLK} + T_{SAMPLE}\ (UP\emptyset IN) + T_{DATA}\ (DN\emptyset OUT)) -$$
$$(T_{SAMPLE}\ (DN\emptyset IN) + T_{DATA}\ (UP\emptyset OUT) + T_{FB}\ (DN\emptyset OUT) +$$
$$T_{LATCH}\ (UP\emptyset OUT)) \geq T_{SKEW} + 300\ psec$$

7.5 MASTER-SLAVE LATCHES

As a rule, use the in-phase output of an in-phase master latch to drive the slave data input. Both master and slave clock should be derived from a clock entering on the same chip pin. When an out-of-phase output of a master latch is used to drive the slave, there is a possibility that the leading edge glitch races into the slave. If such an arrangement is implemented, then the master and slave paths have to be timed out to avoid this problem. Each designer must insure that master-slave latches do not race. The following race analysis is intended for race conditions between the master and slave, and race conditions between the slave and its target latch. The master to slave analysis is done on the leading edge of the clock pulse, while the slave to target latch anaylsis is done on the trailing edge of the clock.

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7.5.1 Out-of-Phase Master/Slave Latch Restrictions

Both master and slave latches must satisfy the latch restrictions. Refer to figures 7-12, 7-13 and the following restrictions.

To prevent a race condition between the master and slave:

T_{MS} (DNØIN) + T_{DATA} (UPØOUT) + T_{INV} (DNØOUT) >

T_{MH} (UPØOUT) + T_{SS} (UPØIN) + 100 psec

To prevent a race condition between the slave and the target:

T_{CLK1} (UPØIN) + T_{MH} (DNØOUT) + T_{SS} (DNØIN) + T_{SLAVE} >

T_{CLK2} (UPØIN) + T_{TNS} (UPØIN) + 100 psec

where:

T_{SLAVE} = T_{SLAVE} (UPØOUT) or T_{SLAVE} (DNØIN)

T_{CLK1} (UPØIN) = T_{CLK2} (UPØIN) (Only if both the slave and target master latches use the same clock driver.)

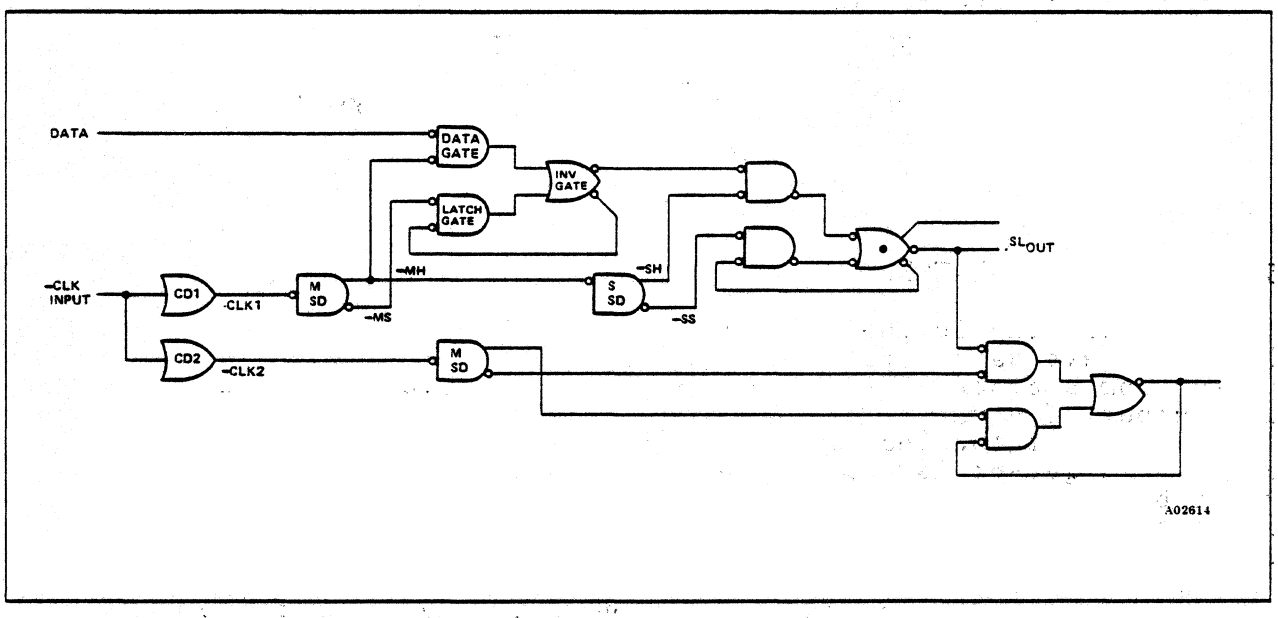

Figure 7-12. Out-of-Phase Master/Slave Latch

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7.5.2 In-Phase Master/Slave Latch Restrictions

Refer to figures 2-12 and 3-1.

To prevent a race condition between the master and slave:

T_{CLK1} (DNØIN) + T_{MS} (DNØIN) + $T_{MASTER\ OUTPUT}$ >

T_{CLK1} (UPØOUT) + T_{SS} (UPØIN) + 100 psec

where:

T_{MASTER} = $T_{MASTER\ OUTPUT}$ (UPØOUT) or $T_{MASTER\ OUTPUT}$ (DNØIN)

To prevent a race condition between the slave and the target master:

T_{CLK1} (DNØOUT) + T_{SS} (DNØIN) + T_{SLAVE} >

T_{CLK2} (UPØIN) + T_{TNS} (UPØIN) + 100 psec

where:

T_{SLAVE}= T_{SLAVE} (UPØOUT) or T_{SLAVE} (DNØIN)

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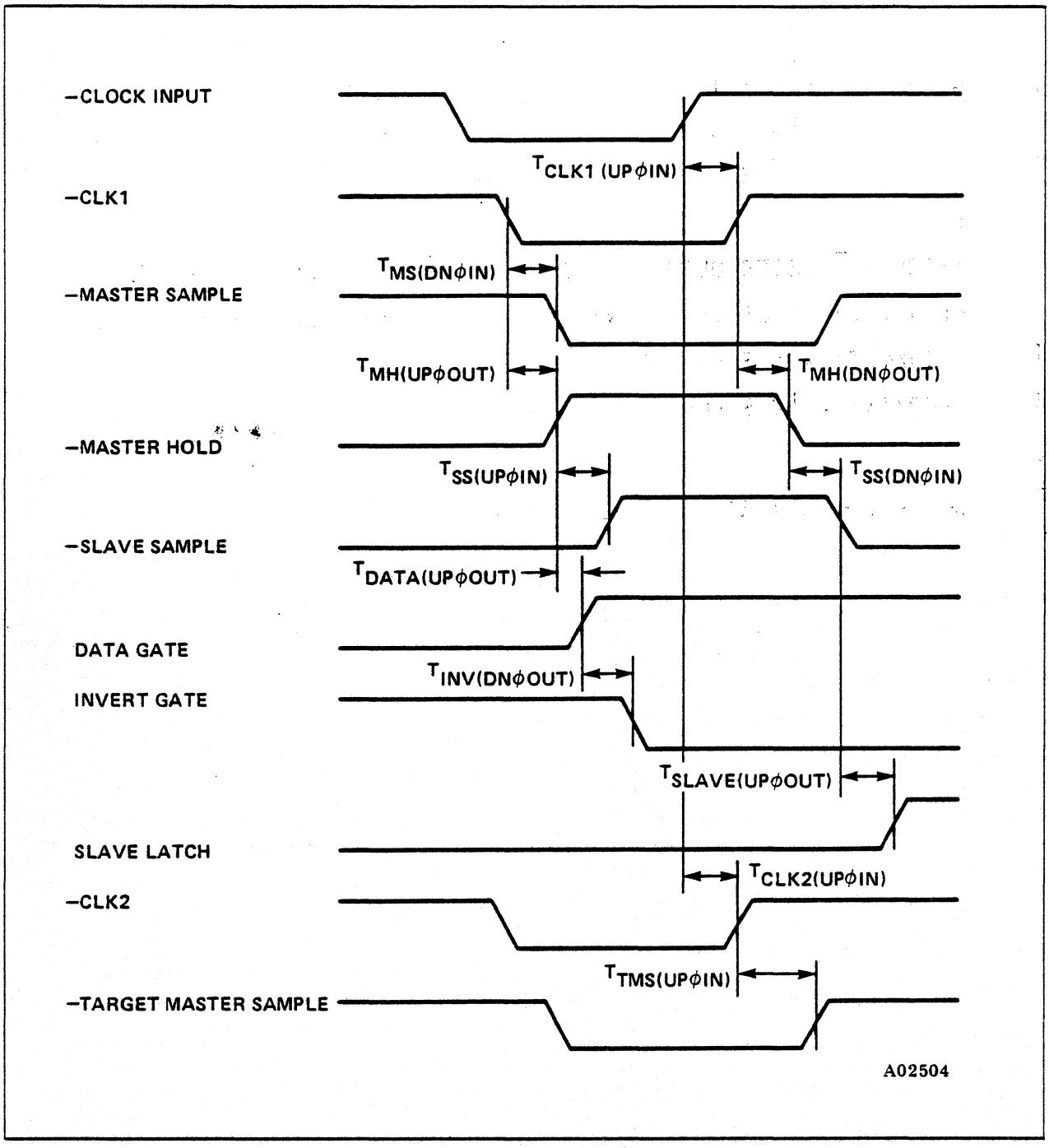

Figure 7-13. Out-of-Phase Master/Slave Latch Timing Diagram

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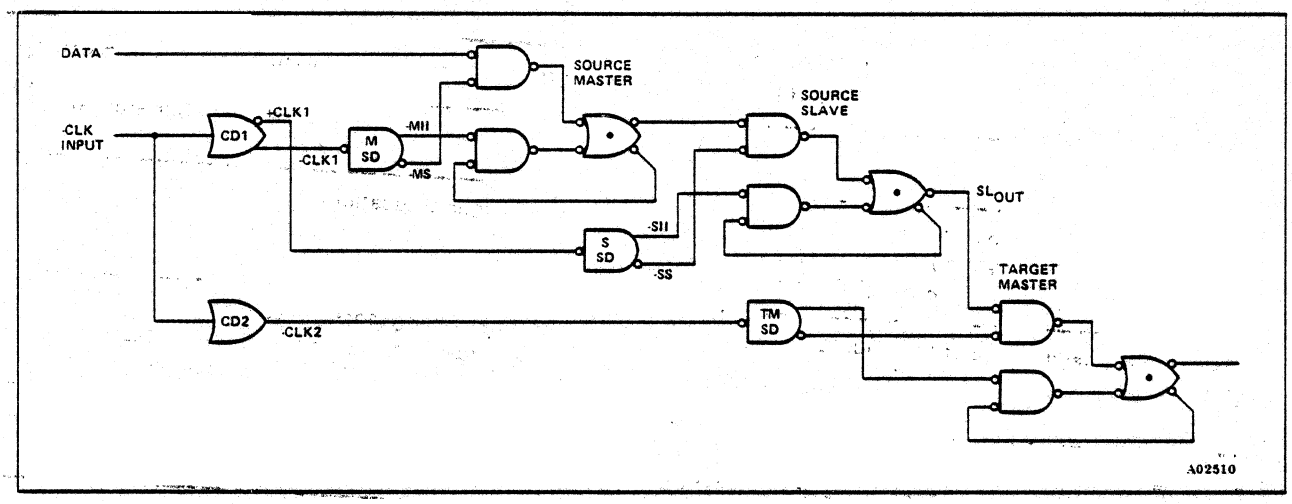

Figure 7-14. In-Phase Master/Slave Latch

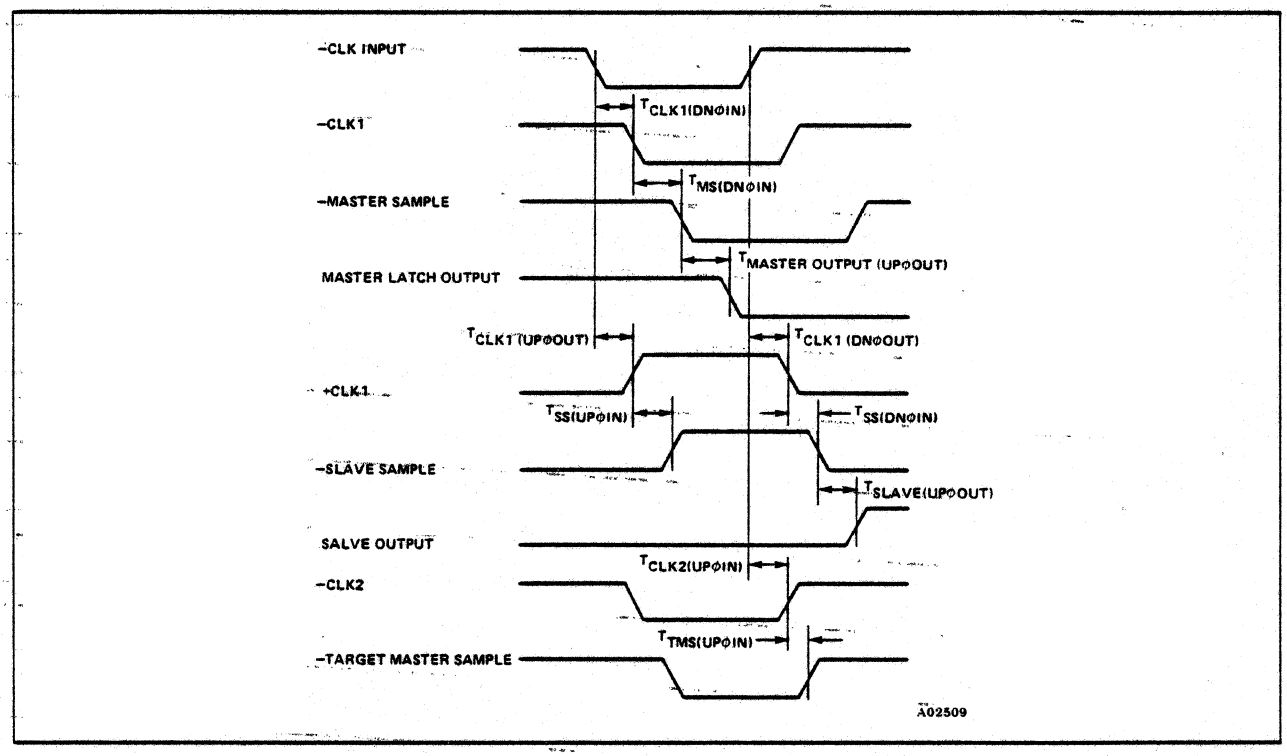

Figure 7-15. In-Phase Latch Timing Diagram

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